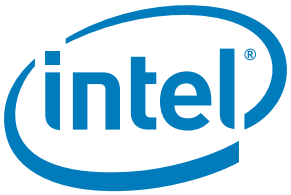

Intel® Atom™ Z8000 Processor Series

Datasheet (Volume 2 of 2)

For Volume 1 of 2 refer Document ID: 332065-002

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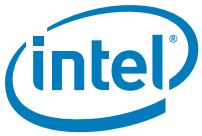

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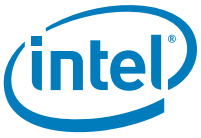

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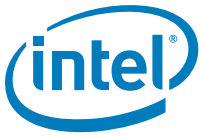


1 Register Access Methods

Note: Throughout this document Intel® Atom™ Z8000 Processor Series is referred as Processor or SoC.

There are six different common register access methods:

- Fixed IO Register Access
- Fixed Memory Mapped Register Access
- IO Referenced Register Access
- Memory Referenced Register Access
- PCI Configuration Register Access (Indirect - via Memory or IO registers)
- Message Bus Register Access (Indirect - via PCI Configuration Registers)

1.1 Fixed IO Register Access

Fixed IO registers are accessed by specifying their 16-bit address in a PORT IN and/or PORT OUT transaction from the CPU core. This allows direct manipulation of the registers. Fixed IO registers are unmovable register in IO space.

Table 1. Fixed IO Register Access Method Example (P80 Register)

Type: I/O Register (Size: 32 bits)	**P80:** 80h

1.2 Fixed Memory Mapped Register Access

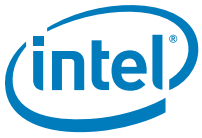
Fixed Memory Mapped IO (MMIO) registers are accessed by specifying their 32/36-bit address in a memory transaction from the CPU core. This allows direct manipulation of the registers. Fixed MMIO registers are unmovable registers in memory space.

Table 2. Fixed Memory Mapped Register Access Method Example (IDX Register)

Type: Memory Mapped I/O Register (Size: 32 bits)	**IDX:** FEC00000h

1.3 IO Referenced Register Access

IO referenced registers use programmable base address registers (BARs) to select a range of IO addresses that it will use to decode PORT IN and/or PORT OUT transactions from the CPU to directly access a register. Thus, the IO BARs act as pointers to blocks of actual IO registers. To access an IO referenced register for a specific IO base address, start with that base address and add the register's offset. Example pseudo code for an IO referenced register read is shown below:



```
Register_Snapshot = IOREAD([IO_BAR]+Register_Offset)
```

Base address registers are often located in the PCI configuration space and are programmable by the BIOS/OS. Other base address register types may include fixed memory registers, fixed IO registers or message bus registers.

Table 3. Referenced IO Register Access Method Example (HSTS Register)

Type: I/O Register (Size: 8bits)	**HSTS:** [SMB_IOBAR] + 0h **SMB_IOBAR Type:** PCI Configuration Register (Size: 32 bits) **SMB_IOBAR Reference:** [B:0, D:31, F:3] + 20h

1.4 Memory Referenced Register Access

The SoC uses programmable base address registers (BARs) to set a range of physical address (memory) locations that it will use to decode memory reads and writes from the CPU to directly access a register. These BARs act as pointers to blocks of actual memory mapped IO (MMIO) registers. To access a memory referenced register for a specific base address, start with that base address and add the register's offset. Example pseudo code for a read is shown below:

```
Register_Snapshot = MEMREAD([Mem_BAR]+Register_Offset)
```

Base address registers are often located in the PCI configuration space and are programmable by the BIOS/OS. Other common base address register types include fixed memory registers and IO registers that point to MMIO register blocks.

Table 4. Memory Mapped Register Access Method Example (SMB_MBAR Register)

Type: Memory Mapped I/O Register (Size: 8bits)	**HSTS:** [SMB_MBAR] + 0h **SMB_MBAR Type:** PCI Configuration Register (Size: 32 bits) **SMB_MBAR Reference:** [B:0, D:31, F:3] + 10h

1.5 PCI Configuration Register Access

Access to PCI configuration space registers is performed through one of two different configuration access methods (CAMs):

- IO indexed - PCI CAM
- Memory mapped - PCI Enhanced CAM (ECAM)

Each PCI function has a standard PCI header consisting of 256 bytes for the IO access scheme (CAM), or 4096 bytes for the enhanced memory access method (ECAM). Invalid read accesses return binary strings of 1s.

Table 5. PCI Register Access Method Example (VID Register)

Type: PCI Configuration Register (Size: 16bits)	**VID:** [B:0, D:31, F:3] + 0h

1.5.1 PCI Configuration Access - CAM: IO Indexed Scheme

Accesses to configuration space using the IO method relies on two 32-bit IO registers:

- **CONFIG_ADDRESS** - IO Port CF8h
- **CONFIG_DATA** - IO Port CFCh

These two registers are both 32-bit registers in IO space. Using this indirect access mode, software uses CONFIG_ADDRESS (CF8h) as an index register, indicating which configuration space register to access, and CONFIG_DATA (CFCh) acts as a window to the register pointed to in CONFIG_ADDRESS. Accesses to CONFIG_ADDRESS (CF8h) are internally captured. Upon a read or write access to CONFIG_DATA (CFCh), configuration cycles will be generated to the PCI function specified by the address captured in CONFIG_ADDRESS. The format of the address is shown below.

Table 6. PCI CONFIG_ADDRESS Register (IO PORT CF8h) Mapping

Field	CONFIG_ADDRESS Bits
Enable PCI Config. Space Mapping	31
Reserved	30:24
Bus Number	23:16
Device Number	15:11
Function Number	10:08
Register/Offset Number	07:02

Note: Bit 31 of CONFIG_ADDRESS must be set for a configuration cycle to be generated.

Pseudo code for a PCI register read is shown below:

- MyCfgAddr[23:16] = bus; MyCfgAddr[15:11] = device; MyCfgAddr[10:8] = funct;
- MyCfgAddr[7:2] = dWordMask(offset); MyCfgAddr[31] = 1;
- IOWRITE(0xCF8, MyCfgAddr)
- Register_Snapshot = IOREAD(0xCFC)

1.5.2 PCI Configuration Access - ECAM: Memory Mapped Scheme

A flat, 256 MiB memory space may also be allocated to perform configuration transactions. This is enabled through the BUNIT.BECREG message bus register (Port: 3h, Register: 27h) found in the SoC. BUNIT.BECREG allows remapping this 256 MiB region anywhere in physical memory space. Memory accesses within the programmed MMIO range result in configuration cycles to the appropriate PCI devices specified by the memory address as shown below.

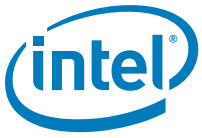


Table 7. PCI Configuration Memory Bar Mapping

ECAM Memory Address Field	ECAM Memory Address Bits
Use from BAR: BUNIT.BECREG[31:28]	31:28
Bus Number	27:20
Device Number	19:15
Function Number	14:12
Register Number	11:02

NOTE: ECAM accesses are only possible when BUNIT.BECREG.ECENABLE (bit 0) is set.
NOTE: Pseudo code for an enhanced PCI configuration register read is shown below:

1. MyCfgAddr[27:20] = bus; MyCfgAddr[19:15] = device; MyCfgAddr[14:12] = funct;
2. MyCfgAddr[11:2] = dw_offset; MyCfgAddr[31:28] = BECREG[31:28];
3. Register_Snapshot = MEMREAD(MyCfgAddr)

1.6 Message Bus Register Access

Accesses to the message bus space is through the SoC's PCI configuration registers. This unit relies on three 32-bit PCI configuration registers to generate messages:

- Message Bus Control Register (MCR) - PCI[B:0,D:0,F:0] + D0h
- Message Data Register (MDR) - PCI[B:0,D:0,F:0] + D4h
- Message Control Register eXtension (MCRX) - PCI[B:0,D:0,F:0] + D8h

This indirect access mode is similar to PCI CAM. Software uses the MCR/MCRX as an index register, indicating which message bus space register to access (MCRX only when required), and MDR as the data register. Writes to the MCR trigger message bus transactions.

Writes to MCRX and MDR will be captured. Writes to MCR will generate an internal 'message bus' transaction with the opcode and target (port, offset, bytes) specified in the MCR and the captured MCRX. When a write opcode is specified in MCR, the data that was captured by MDR is used for the write. When a data read opcode is specified in MCR, the data will be available in the MDR register after the MCR write completes (non-posted). The format of MCR and MCRX are shown below.

Table 8. MCR Description

Field	MBPR Bits
OpCode (typically 10h for read, 11h for write)	31:24
Port	23:16
Offset/Register	15:08
Byte Enable	07:04

Table 9. MCRX Description

Field	MBPER Bits
Offset/Register Extension. This is used for messages sent to end points that require more than 8 bits for the offset/register. These bits are a direct extension of MCR[15:8].	31:08

Most message bus registers are located in the SoC. The default opcode messages for those registers are as follows:

- Message 'Read Register' Opcode: 06h
- Message 'Write Register' Opcode: 07h

Registers with different opcodes will be specified as applicable. Pseudo code of a message bus register read is shown below (where ReadOp==0x06):

- MyMCR[31:24] = ReadOp; MyMCR[23:16] = port; MyMCR[15:8] = offset;
- MyMCR[7:4] = 0xf
- PCIWRITE(0, 0, 0, 0xD0, MyMCR)
- Register_Snapshot = PCIREAD(0, 0, 0, 0xD4)

1.7 Register Field Access Types

Table 10. Register Access Types and Definitions (Sheet 1 of 2)

Access Type	Meaning	Description
RO	Read Only	In some cases, if a register is read only, writes to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. Refer the I/O and memory map tables for details.
WO	Write Only	In some cases, if a register is write only, reads to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. Refer the I/O and memory map tables for details.
R/W	Read/Write	A register with this attribute can be read and written.
R/WC	Read/Write Clear	A register bit with this attribute can be read and written. However, a write of 1 clears (sets to 0) the corresponding bit and a write of 0 has no effect.

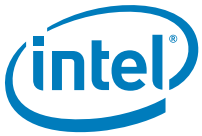


Table 10. Register Access Types and Definitions (Sheet 2 of 2)

Access Type	Meaning	Description
R/WO	Read/Write-Once	A register bit with this attribute can be written only once after power up. After the first write, the bit becomes read only.
R/WLO	Read/Write, Lock-Once	A register bit with this attribute can be written to the non-locked value multiple times, but to the locked value only once. After the locked value has been written, the bit becomes read only.
Default	Default	When the processor is reset, it sets its registers to predetermined default states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software to determine configuration, operating parameters, and optional system features that are applicable, and to program the processor registers accordingly.

§

2 Mapping Address Space Registers

The Processor core can only directly access *memory space* through memory reads and writes and *I/O space* through the IN and OUT I/O port instructions. *PCI configuration space* is indirectly accessed through I/O or memory space, and the *Message Bus space* is accessed through PCI configuration space. Refer Chapter 1, "Register Access Methods"for details.

This chapter describes how the memory, I/O, PCI and Message Bus spaces are mapped to interfaces in the SoC.

Note: Refer Chapter 6, "SoC Storage" for registers specified in the chapter.

2.1 Physical Address Space Mappings

There are 64 GB (36-bits) of physical address space that can be used as:

- Memory Mapped I/O (MMIO - I/O fabric)
- Physical Memory (DRAM)

The Processor core can access the full physical address space, while downstream devices can only access SoC DRAM, and each Processor core's local APIC. Peer to peer transactions are not supported.

Most devices map their registers and memory to the physical address space. This chapter summarizes the possible mappings.

2.1.1 SoC Memory Map

The SoC maps the physical address space as follows:

- Processor core to DRAM
- Processor core to I/O fabric (MMIO)
- Processor core to extended PCI registers (ECAM accesses)
- I/O fabric to Processor cores (local APIC interrupts)

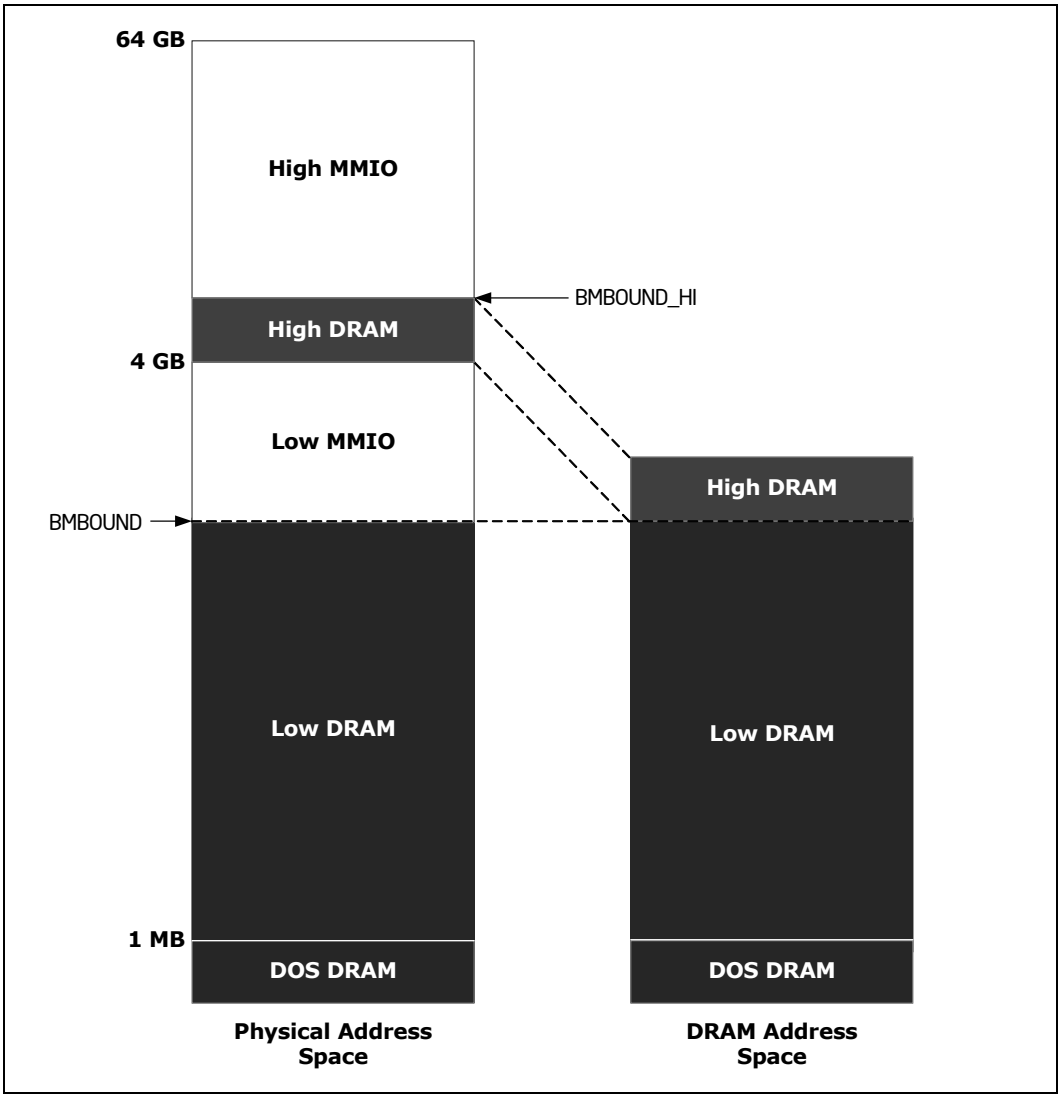
Although 64 GB (36-bits) of physical address space is accessible, some MMIO must exist for devices and software with 32-bit limits. Further, all DRAM should remain accessible for devices and software with access to memory above 4 GB. These goals are accomplished by moving a section DRAM to start at the fixed 4 GB boundary, leaving a hole below 4 GB for MMIO. This creates the following distinct memory regions:

- DOS DRAM + Low DRAM

- Low MMIO
- High DRAM
- High MMIO

There are two registers used to create these regions, BMBOUND and BMBOUND_HI. Their use is shown in Figure 11.

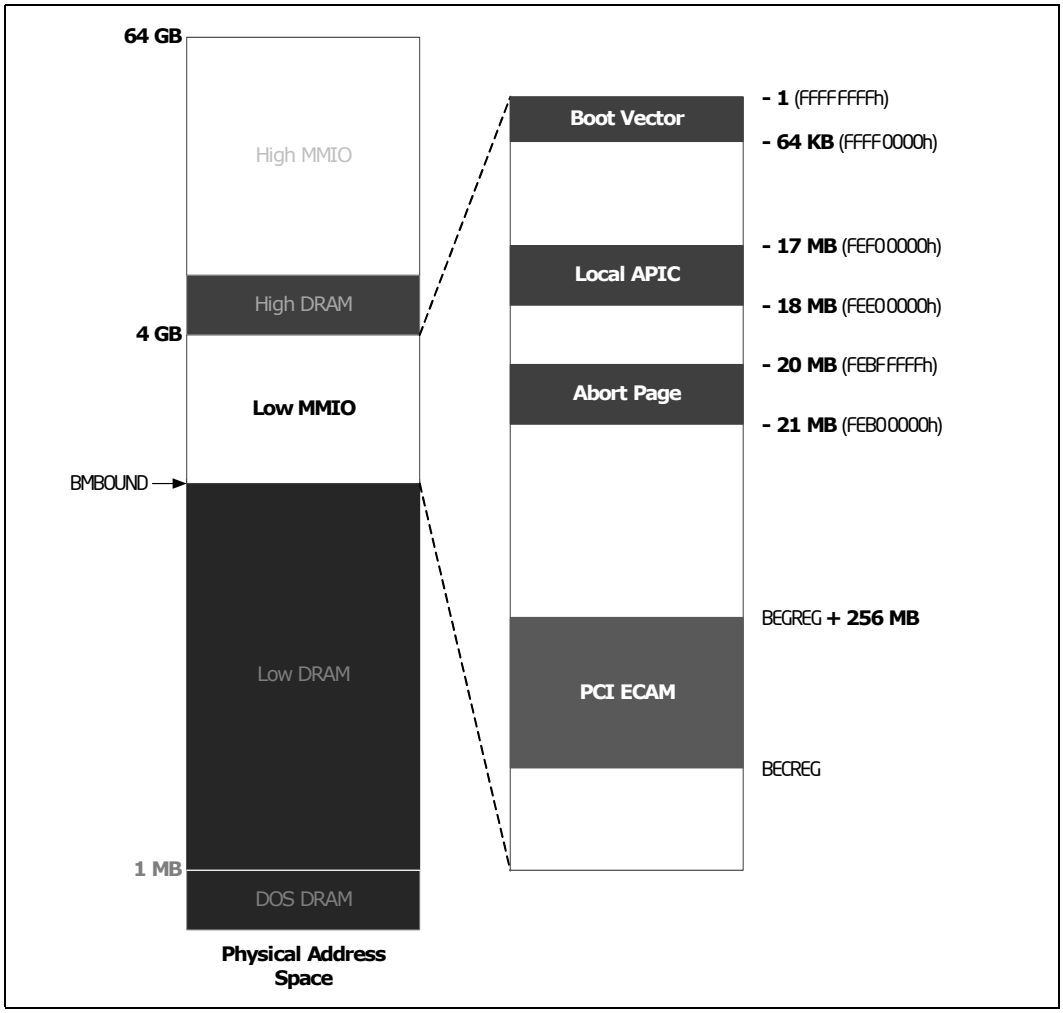
Figure 11. Physical Address Space—DRAM and MMIO



2.1.1.1 Low MMIO

The low MMIO mappings are shown in Figure 12.

Figure 12. Physical Address Space—Low MMIO



By default, Processor core reads targeting the **Boot Vector** range (FFFFFFFFh-FFFF0000h) are sent to the boot Flash connected to the Platform Controller Unit, and write accesses target DRAM. This allows the boot strap Processor core to fetch boot code from the boot Flash, and then shadow that code to DRAM.

Upstream writes from the I/O fabric to the **Local APIC** range (FEE00000h-FEF00000h) are sent to the appropriate Processor core APIC.

Write accesses from a Processor core to the **Abort Page** range (FEB00000h-FEBFFFFFh) will be dropped, and reads will always return all 1s in binary.

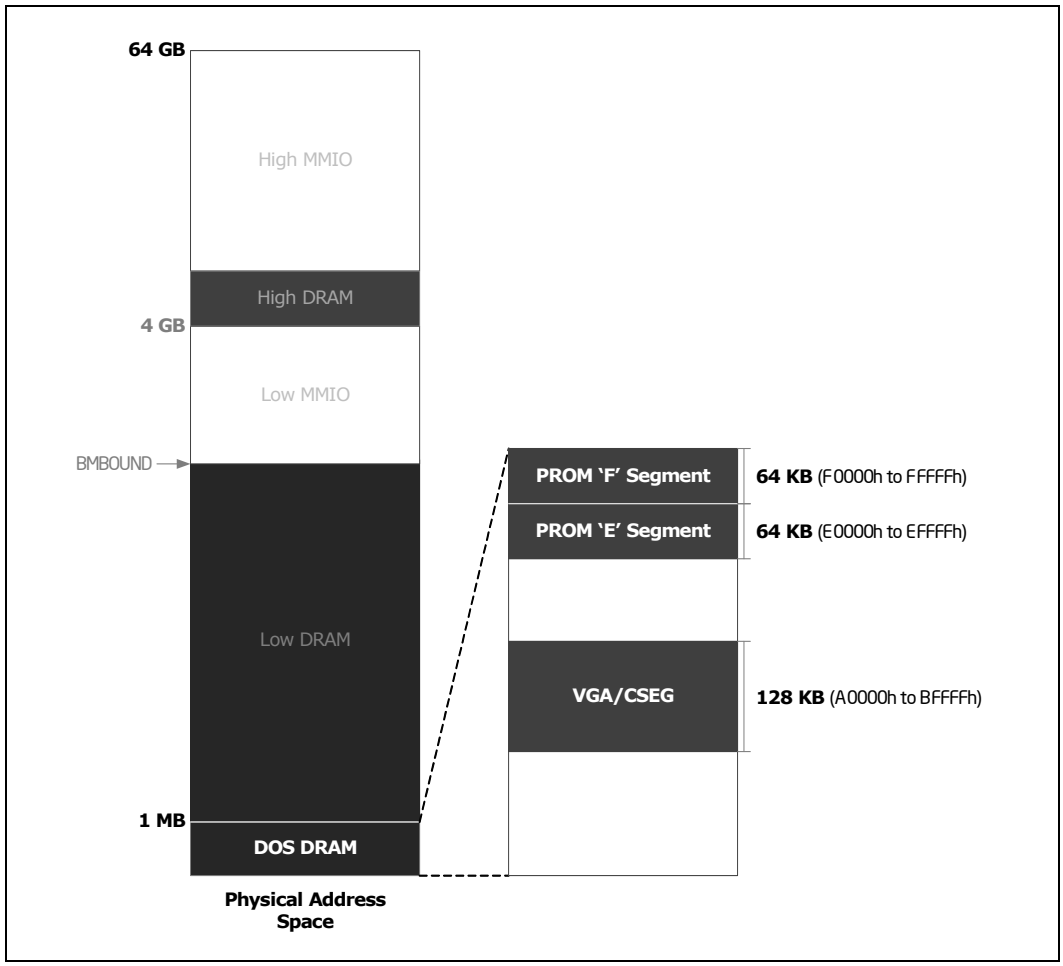
Accesses in the 256MB **PCI ECAM** range starting at BECREG generate enhanced PCI configuration register accesses when enabled (BECREG.ECENABLE). Unlike traditional memory writes, writes to this range are non-posted when enabled.

All other downstream accesses in the Low MMIO range are sent to the I/O Fabric for further decode based on PCI resource allocations. The I/O Fabric's subtractive agent (for unclaimed accesses) is the Platform Controller Hub.

2.1.1.2 DOS DRAM

The DOS DRAM is the memory space below 1MB. In general, accesses from a processor targeting DOS DRAM target system DRAM. Exceptions are shown in the below figure.

Figure 13. Physical Address Space—DOS DRAM



Processor writes to the 64KB (each) **PROM 'E'** and **'F'** segments (E0000h-EFFFFh and F0000h-FFFFFh) always target DRAM. The BMISC register is used to direct Processor core reads in these two segments to DRAM or the I/O fabric (MMIO).

Processor core accesses to the 128KB **CSEG** range (A0000h-BFFFFh) can target DRAM or the I/O fabric (MMIO). The target is selected with the BMISC.ABSEGINDRAM register.

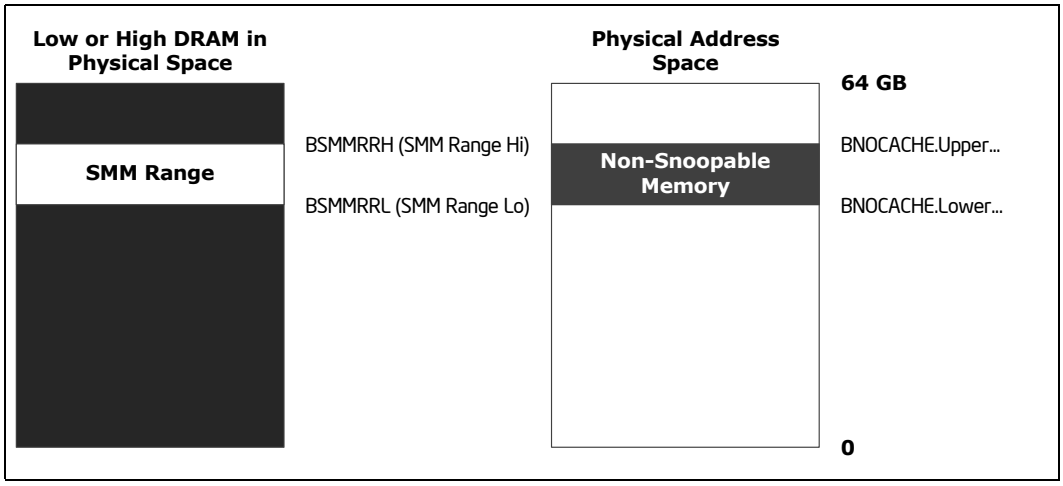
2.1.1.3 Additional Mappings

There are two additional mappings available in the SoC:

- SMM range
- Non-snoop range

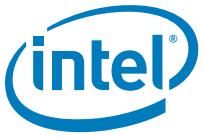
Figure 14 shows these mappings.

Figure 14. Physical Address Space—SMM and Non-Snoop Mappings



SMI handlers running on a Processor core execute out of SMM memory. To protect this memory from non-Processor core access, the **SMM Range** (BSMMRRL-BSMMRRH) may be programmed anywhere in low or high DRAM space (1MB aligned). This range will only allow accesses from the Processor cores.

To prevent snoops of the Processor cores when DMA devices access a specific memory region, the **Non-Snoopable Memory range** (BNOCACHE.Lower-BNOCACHE.Upper) can be programmed anywhere in physical address space. This range is enabled by means of the BNOCACHECTL register's enable bit (BNOCACHECTL.Enable).



2.1.2 I/O Fabric (MMIO) Map

Memory accesses targeting MMIO are routed by the I/O fabric to programmed PCI ranges, or routed to the PCU by default (subtractive agent). Programmed PCI ranges can be moved within low or high MMIO, and most can be disabled.

Note: Not all devices can be mapped to high MMIO.

Fixed MMIO is claimed by the Platform Controller Unit (PCU). The default regions are listed below. Movable ranges are not shown. Refer the register maps of all PCU devices for details.

Table 15. Fixed Memory Ranges in the Platform Controller Unit (PCU)

Device	Start Address	End Address	Comments
Low BIOS (Flash Boot)	000E0000h	000FFFFFh	Starts 128KB below 1MB; Firmware/ BIOS
I/O APIC	FEC00000h	FEC00040h	Starts 20MB below 4GB
HPET	FED00000h	FED003FFh	Starts 19MB below 4GB
TPM (LPC)	FFD40000h	FFD40FFFh	Starts 16KB above HPET range
High BIOS/Boot Vector	FFFF0000h	FFFFFFFFh	Starts 64KB below 4GB; Firmware/ BIOS

The following PCI devices may claim memory resources in MMIO space:

- Graphics/Display (High MMIO capable)
- SD/MMC
- SIO
- Platform Controller Unit (PCU) (Multiple BARs)
- xHCI USB

Refer each device's interface chapter for details.

Warning: Variable memory ranges should not be set to conflict with other memory ranges. There will be unpredictable results if the configuration software allows conflicts to occur. Hardware does not check for conflicts.

2.2 I/O Address Space

There are 64KB + 3 bytes of I/O space (0h-10002h) for accessing I/O registers. Most I/O registers exists for legacy functions in the PCU or for PCI devices, while some are claimed by the SoC for graphics and for the PCI configuration space access registers.

2.2.1 I/O Fabric I/O Map

2.2.1.1 PCU Fixed I/O Address Ranges

Below table shows the fixed I/O space ranges seen by a processor.

Table 16. Fixed I/O Ranges in the Platform Controller Unit (PCU)

Device	I/O Address	Comments
8259 Master	20h-21h, 24h-25h, 28h-29h, 2Ch-2Dh, 30h-31h, 34h-35h, 38h-39-, 3Ch-3Dh	
8254s	40h-43h, 50h-53h	
PS2 Control	60h, 64h	
NMI Controller	61h, 63h, 65h, 67h	
RTC	70h-77h	
Port 80h	80h-83h	
INIT Register	92h	
8259 Slave	A0h-A1h, A4h-A5h, A8h-A9h, ACh-ADh, B0h-B1h, B4h-B5h, B8h-B9h, BCh-BDh, 4D0h-4D1h	
PCU UART	3F8h-3FFh	
Reset Control	CF9h	Overlaps PCI I/O registers
Active Power Management	B2h-B3h	

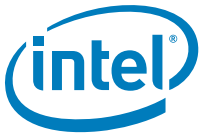
2.2.1.2 Variable I/O Address Ranges

Table 17 shows the variable I/O decode ranges. They are set using base address registers (BARs) or other similar means. Plug-and-play (PnP) software (PCI/ACPI) can use their configuration mechanisms to set and adjust these values.

Warning: The variable I/O ranges should not be set to conflict with other I/O ranges. There will be unpredictable results if the configuration software allows conflicts to occur. Hardware does not check for conflicts.

Table 17. Movable I/O Ranges Decoded by PCI Devices on the I/O Fabric

Device	Size (Bytes)	Target
ACPI Power Management (PCU)	128	ACPI_BASE_ADDR (PM1BLK): PCI[B:0,D:31,F:0] + 40h
GPIO (PCU)	256	GBA: PCI[B:0,D:31,F:0] + 48h
RCBA (PCU)	1024	RCRB_BA: PCI[B:0,D:31,F:0] + F0h



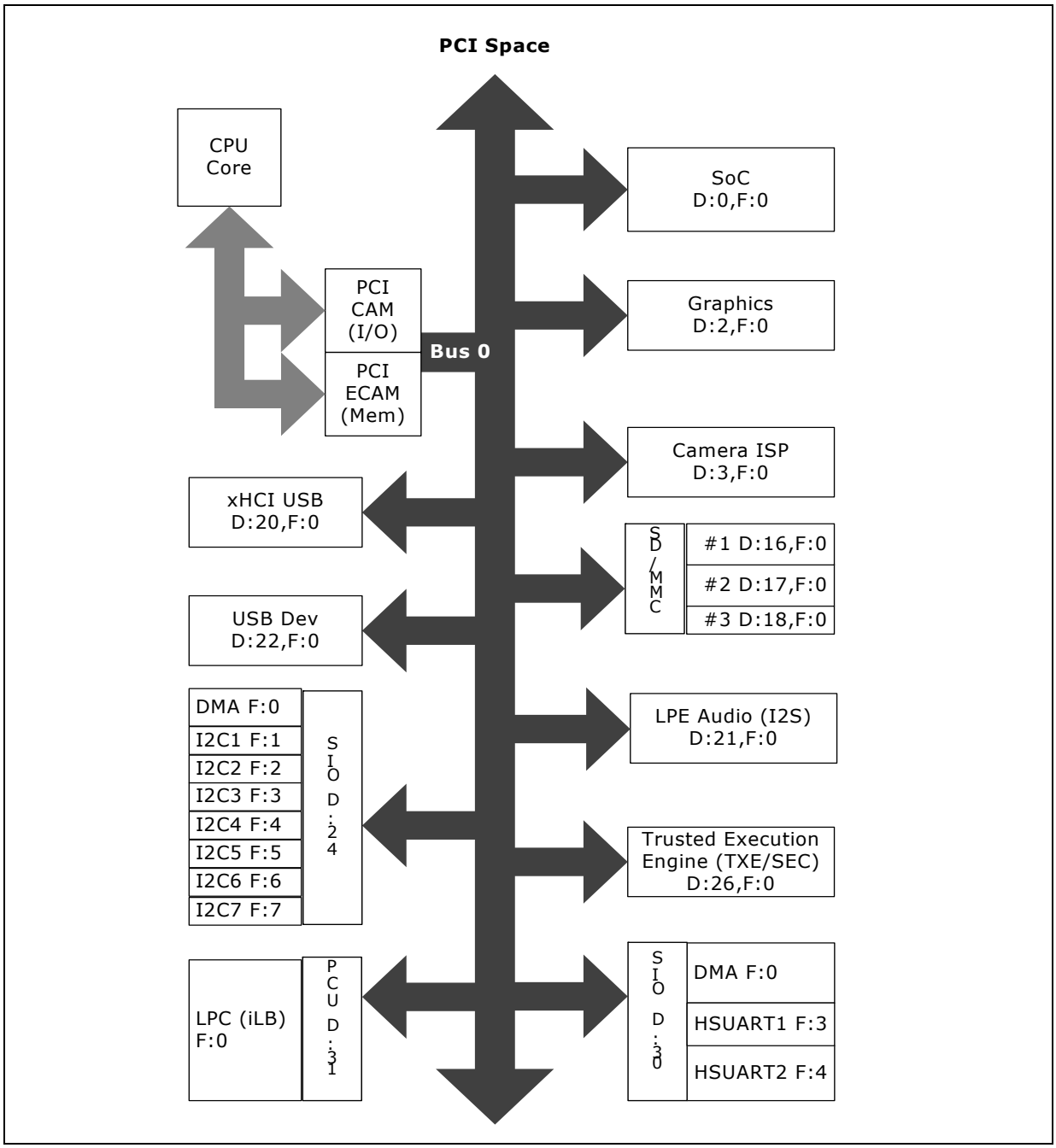
2.3 PCI Configuration Space

All PCI devices/functions are shown in Table 18.

Table 18. PCI Devices and Functions

Bus	Device	Function	Device ID	Device Description	Function Description
0	0	0	2280h	SoC	
0	2	0	22B0h	Graphics and Display	
0	3	0	22B8h	ISP Camera	
0	11	0	22DCh	P-Unit	Power Management
0	16	0	2294h	Storage Control Cluster (SCC)	MMC Port
0	17	0	2295h		SDIO Port
0	18	0	2296h		SD Port
0	20	0	22B5h	xHCI USB	
0	21	0	22A8h	Low Power Engine Audio	Host Bridge + three I^2S Ports (0-2)
0	24	0	22C0h	Serial I/O (SIO)	DMA
		1	22C1h		I^2C Port 1
		2	22C2h		I^2C Port 2
		3	22C3h		I^2C Port 3
		4	22C4h		I^2C Port 4
		5	22C5h		I^2C Port 5
		6	22C6h		I^2C Port 6
		7	22C7h		I^2C Port 7
0	26	0	2298h	Trusted Execution Engine	
0	28	0	22C8h	PCIe	PCIe Port 1
		1	22CAh		PCIe Port 2
		2	22CCh		PCIe Port 3
		3	22CEh		PCIe Port 4
0	30	0	2286h	Serial I/O (SIO)	DMA
		3	228Ah		HSUART Port 1
		4	228Ch		HSUART Port 2
0	31	0	229Ch	Platform Controller Unit LPC	LPC: Bridge to Intel Legacy Block

Figure 19. Bus 0 PCI Devices and Functions



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3 System Memory Controller Registers

3.1 System Memory Controller (D UNIT) Registers

Table 20. Summary of System Memory Controller (D-Unit) Message Registers

Table 1.

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–0h	1	"DRP—Offset 0h" on page 28	00000000h
1–1h	1	"DTR0A (DTR0)—Offset 1h" on page 29	43402108h
2–2h	1	"DTR1A (DTR1)—Offset 2h" on page 30	08C90320h
3–3h	1	"DTR2A (DTR2)—Offset 3h" on page 32	00020508h
4–4h	1	"DTR3A (DTR3)—Offset 4h" on page 33	06106108h
5–5h	1	"DTR4A (DTR4)—Offset 5h" on page 34	8C063322h
6–6h	1	"DPMC0—Offset 6h" on page 35	00000000h
7–7h	1	"DPMC1—Offset 7h" on page 36	09000000h
8–8h	1	"DRFC—Offset 8h" on page 38	00012CA7h
9–9h	1	"DSCH—Offset 9h" on page 39	00071107h
A–Ah	1	"DCAL—Offset Ah" on page 40	00001300h
B–Bh	1	"DRMC—Offset Bh" on page 41	00000000h
C–Ch	1	"PMSTS—Offset Ch" on page 42	00000000h
D–Dh	1	"VNNTIMER—Offset Dh" on page 43	00000000h
E–Eh	1	"TQCTL—Offset Eh" on page 43	00000000h
F–Fh	1	"DCO—Offset Fh" on page 44	20000000h
10–10h	1	"DTRC—Offset 10h" on page 45	00000000h
11–11h	1	"DTR0B—Offset 11h" on page 46	43402108h
12–12h	1	"DTR1B—Offset 12h" on page 47	08C90320h
13–13h	1	"DTR2B—Offset 13h" on page 49	00020508h
14–14h	1	"DTR3B—Offset 14h" on page 50	06106108h
15–15h	1	"DTR4B—Offset 15h" on page 51	8C063322h
16–16h	1	"DMR0aDDR3—Offset 16h" on page 52	00000000h
17–17h	1	"DMR1aDDR3—Offset 17h" on page 53	00000000h
18–19h	2	"DMR2aDDR3—Offset 18h" on page 54	00000000h
1A–1Ah	1	"DMR0bDDR3—Offset 1Ah" on page 54	00000000h
1B–1Bh	1	"DMR1bDDR3—Offset 1Bh" on page 55	00000000h
1C–1Eh	3	"DMR2bDDR3—Offset 1Ch" on page 56	00000000h

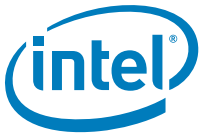


Table 1.

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1F–1Fh	1	"DCBR—Offset 1Fh" on page 56	00000400h
20–20h	1	"DSTAT—Offset 20h" on page 57	0000000Ah
21–24h	4	"PGTBL—Offset 21h" on page 58	00000000h
30–30h	1	"C2DICCA—Offset 30h" on page 59	0000FF38h
31–31h	1	"C2DRCCA—Offset 31h" on page 60	0000FF38h
32–32h	1	"D2CICCA—Offset 32h" on page 60	0000FF38h
33–36h	4	"D2CRCCA—Offset 33h" on page 61	0000FF38h
38–38h	1	"C2DICCB—Offset 38h" on page 62	0000FF38h
39–39h	1	"C2DRCCB—Offset 39h" on page 62	0000FF38h
3A–3Ah	1	"D2CICCB—Offset 3Ah" on page 63	0000FF38h
3B–3Eh	4	"D2CRCCB—Offset 3Bh" on page 64	0000FF38h
4A–4Ah	1	"SSKPD0—Offset 4Ah" on page 64	00000000h
4B–4Eh	4	"SSKPD1—Offset 4Bh" on page 65	00000000h
50–50h	1	"BONUS0—Offset 50h" on page 65	00000000h
51–54h	4	"BONUS1—Offset 51h" on page 66	00000000h
70–73h	4	"DFUSESTAT—Offset 70h" on page 66	00000000h
80–80h	1	"DSCRMSEED—Offset 80h" on page 67	00000000h
81–81h	1	"DSCRMLO—Offset 81h" on page 67	00000000h
82–82h	1	"DSCRMHI—Offset 82h" on page 68	00000000h
83–83h	1	"DQCALRDATLO—Offset 83h" on page 68	00000000h
84–84h	1	"DQCALRDATHI—Offset 84h" on page 69	00000000h
85–88h	4	"DQCALRDATECC—Offset 85h" on page 69	00000000h
E0–E0h	1	"PMSEL0—Offset E0h" on page 70	00000002h
E1–E1h	1	"PMSEL1—Offset E1h" on page 70	00000002h
E2–E2h	1	"PMSEL2—Offset E2h" on page 71	00000002h
E3–E6h	4	"PMSEL3—Offset E3h" on page 72	00000002h
E8–E8h	1	"PMAUXMAX—Offset E8h" on page 72	00000000h
E9–E9h	1	"PMAUXMIN—Offset E9h" on page 73	00000000h
EA–EDh	4	"PMAUXMAX—Offset E8h" on page 72	00000000h
F0–F0h	1	"SWACA—Offset F0h" on page 74	00008110h
F1–F3h	3	"SCPA—Offset F1h" on page 74	00000310h
F4–F4h	1	"SACB—Offset F4h" on page 75	00008110h
F5–F7h	3	"SCPB—Offset F5h" on page 75	00000310h
F8–F8h	1	"SACD—Offset F8h" on page 75	00008110h

Table 1.

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
F9–FBh	3	"SCPD—Offset F9h" on page 76	00000310h
FC–FCh	1	"SWACE—Offset FCh" on page 76	FFFFFFFFh
FD–100h	4	"SCPE—Offset FDh" on page 77	00008310h

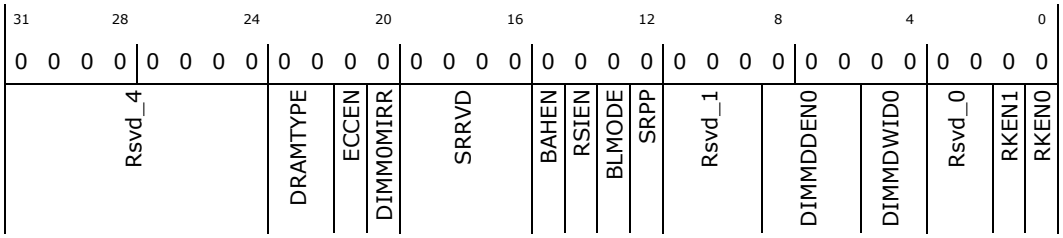
3.1.1 DRP—Offset 0h

DRAM Rank Population

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Rsvd_4:** Reserved
23:22	0x0 RW/P	**DRAMTYPE:** DRAM Type 0 - DDR3 1 - LPDDR2
21	0x0 RW/P	**ECCEN:** ECC Enable. This bit determines if Dunit treats the PMI BE_ECC bits as ECC bits or Byte Enable. 0 - ECC Disabled 1 - ECC Enable
20	0x0 RW/P	**DIMM0MIRR:** Address mapping to DIMM0 is mirrored. BIOS writes value defined in SPD Byte 63. Used as indication to Punit to flip MRS opcode to 2nd rank on DIMM0. This bit has no functional impact on Dunit. 0 - Standard 1 - Mirrored
19:16	0x0 RW/P	**SRRVD:** Static Read Return Valid Delay
15	0x0 RW/P	**BAHEN:** Bank Address Hashing Select. Refer Address Mapping section for full description. 0 Bank Address Hashing Disabled 1 Bank Address Hashing Enabled Note: The hashing select should be set the same for both the Dunit and Bunit.
14	0x0 RW/P	**RSIEN:** Address Map Select. Refer Address Mapping section for full description. 0 Map 0 1 Map 1 Note: The address map select should be set the same for both the Dunit and Bunit.
13	0x0 RW	**BLMODE:** Burst Length Mode. Selects the DDR3 Burst Length mode: 0h - BL8 Fixed. 1h - BL8/BC4 On-the-Fly

Bit Range	Default & Access	Field Name (ID): Description
12	0x0 RW/P	**SRPP:** Single Rank Per Package. 0 Two ranks in package 1 One rank in package.
11:9	0x0 RO	**Rsvd_1:** Reserved
8:6	0x0 RW/P	**DIMMDDEN0:** DIMM 0 Device Density. This sets the density of the DRAM devices populated in DIMM 0 (Rank 0 and Rank 1). 000 1Gbit 001 2Gbit 010 4Gbit 011 8Gbit 100 16Gbit
5:4	0x0 RW/P	**DIMMDWID0:** DIMM 0 Device Width. Indicates the width of the DRAM devices populated in DIMM 0 (Rank 0 and Rank 1). 00 x8 01 x16 10 x32 11 Reserved
3:2	0x0 RO	**Rsvd_0:** Reserved
1	0x0 RW/P	**RKEN1:** DIMM 0, Rank 1 Enabled. Should be set to 1 when DIMM0 is populated and has 2 ranks to enable the use of this rank. Otherwise, must be set to 0.
0	0x0 RW/P	**RKEN0:** DIMM 0, Rank 0 Enabled. Should be set to 1 when DIMM0 is populated to enable the use of this rank. Otherwise, must be set to 0.

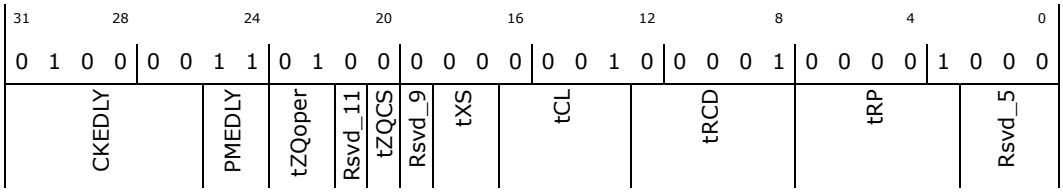
3.1.2 DTR0A (DTR0)—Offset 1h

DRAM Timing Register 0

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 43402108h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x10 RW	**CKEDLY:** Additional delay between CK/CKB start and SRX command. This delay is needed for clock to stabilize to meet JEDEC requirements. Delay is CKEDLY multiples of 256 DRAM Clocks. 0ns to 9,600ns (DDR3-800) 0ns to 7,200ns (DDR3-1066)
25:24	0x3 RW	**PMEDLY:** The delay, in DRAM clocks, between SR Entry command and Power-Mode message to DDRIO. 0h - 6 DRAM Clocks. 1h - 8 DRAM Clocks. 2h - 10 DRAM Clocks. 3h - 12 DRAM Clocks.
23:22	0x1 RW	**tZQoper:** The delay, in DRAM clocks, between ZQC-Long command to any command. Note, ZQCL command during DRAM Init flow requires longer latency which is controlled be BIOS. 0h - 256 DRAM Clocks. 1h - 384 DRAM Clocks.

Bit Range	Default & Access	Field Name (ID): Description
21	0x0 RO	**Rsvd_11:** Reserved
20	0x0 RW	**tZQCS:** The delay, in DRAM clocks, between a ZQC-Short command to any command. 0h - 64 DRAM Clocks. 1h - 96 DRAM Clocks.
19	0x0 RO	**Rsvd_9:** Reserved
18:17	0x0 RW	**tXS:** The delay, in DRAM clocks, between SRX command to command not requiring locked DLL. The Dunit can send a ZQCL command after tXS. JEDEC defines MAX(5CK, tRFC(min)+10ns) so both values take safety margin. 0h - 256 DRAM Clocks. 1h - 384 DRAM Clocks.
16:13	0x1 RW	**tCL:** CAS Latency. Specifies the delay, in DRAM clocks, between the issue of a RD command and the return of valid data on the DQ bus. 0h - 5 DRAM Clocks (DDR3- 800) 1h - 6 DRAM Clocks (DDR3- 800, 1066) 2h - 7 DRAM Clocks (DDR3- 1066, 1333) 3h - 8 DRAM Clocks (DDR3- 1066, 1333, 1600) 4h - 9 DRAM Clocks (DDR3- 1333, 1600) 5h - 10 DRAM Clocks (DDR3- 1333, 1600) 6h - 11 DRAM Clocks (DDR3- 1600) 7h - 12 DRAM Clocks 8h - 13 DRAM Clocks Others - Reserved
12:8	0x1 RW	**tRCD:** Activate (RAS) to CAS Delay. Specifies the delay, in DRAM clocks, between an ACT command and a RD/WR command to the same bank. 0h - 5 DRAM Clocks (DDR3- 800) 1h - 6 DRAM Clocks (DDR3- 800, 1066) 2h - 7 DRAM Clocks (DDR3- 1066, 1333) 3h - 8 DRAM Clocks (DDR3- 1066, 1333, 1600) 4h - 9 DRAM Clocks (DDR3- 1333, 1600) 5h - 10 DRAM Clocks (DDR3- 1333, 1600) 6h - 11 DRAM Clocks (DDR3- 1600) 7h - 12 DRAM Clocks 8h - 13 DRAM Clocks 9h - 14 DRAM Clocks Ah - 15 DRAM Clocks Bh - 16 DRAM Clocks Ch - 17 DRAM Clocks Dh - 18 DRAM Clocks Eh - 19 DRAM Clocks Fh - 20 DRAM Clocks 10h - 21 DRAM Clocks 11h - 22 DRAM Clocks Others - Reserved
7:3	0x1 RW	**tRP:** Precharge to Activate Delay. Specifies the delay, in DRAM clocks, between a PRE command and an ACT command to the same bank. 0h - 5 DRAM Clocks (DDR3- 800) 1h - 6 DRAM Clocks (DDR3- 800, 1066) 2h - 7 DRAM Clocks (DDR3- 1066, 1333) 3h - 8 DRAM Clocks (DDR3- 1066, 1333, 1600) 4h - 9 DRAM Clocks (DDR3- 1333, 1600) 5h - 10 DRAM Clocks (DDR3- 1333, 1600) 6h - 11 DRAM Clocks (DDR3- 1600) 7h - 12 DRAM Clocks 8h - 13 DRAM Clocks 9h - 14 DRAM Clocks Ah - 15 DRAM Clocks Bh - 16 DRAM Clocks Ch - 17 DRAM Clocks Dh - 18 DRAM Clocks Eh - 19 DRAM Clocks Fh - 20 DRAM Clocks 10h - 21 DRAM Clocks 11h - 22 DRAM Clocks Others - Reserved
2:0	0x0 RO	**Rsvd_5:** Reserved

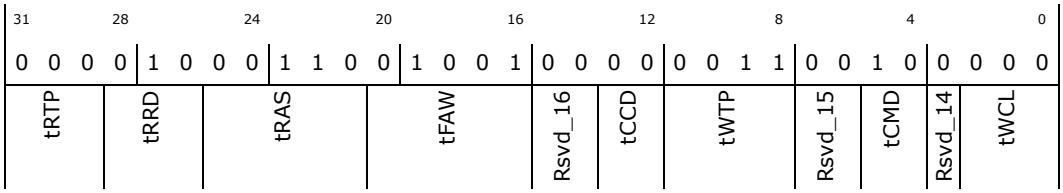
3.1.3 DTR1A (DTR1)—Offset 2h

DRAM Timing Register 1

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 08C90320h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**tRTP:** Read to Precharge Delay. The minimal delay between RD command and PRE command to same bank. 00 - 4 DRAM Clocks (DDR3-800 DDR3-1066) 01 - 5 DRAM Clocks (DDR3-1333) 10 - 6 DRAM Clocks (DDR3-1600) 11 - 7 DRAM Clocks
28:26	0x2 RW	**tRRD:** Row Activation to Row Activation Delay. The minimal time interval between 2 ACT commands to any bank in the same DRAM device. Limits peak current profile. 00 - 4 DRAM Clocks (1KB page DDR3-800, 1066, 1333), (2KB page DDR3-800) 01 - 5 DRAM Clocks (1KB page DDR3-1600), (2KB page DDR3-1333) 10 - 6 DRAM Clocks (2KB page DDR3-1066, 1600) 11 - 7 DRAM Clocks
25:21	0x6 RW	**tRAS:** Row Activation Period. The minimal delay, in DRAM clocks, between ACT command and PRE command to same bank. At least equal to tRCD + tCWL + tCCD + tWR 0h -14 DRAM Clocks. 1h -15 DRAM Clocks (DDR3-800) 2h -16 DRAM Clocks. 3h -17 DRAM Clocks. 4h -18 DRAM Clocks. 5h -19 DRAM Clocks. 6h -20 DRAM Clocks (DDR3-1066) 7h -21 DRAM Clocks. 8h -22 DRAM Clocks. 9h -23 DRAM Clocks. Ah -24 DRAM Clocks (DDR3-1333) Bh -25 DRAM Clocks. Ch -26 DRAM Clocks. Dh -27 DRAM Clocks. Eh -28 DRAM Clocks (DDR3-1600) Fh -29 DRAM Clocks.
20:16	0x9 RW	**tFAW:** Four Bank Activation Window. A rolling time-frame, in which a maximum of 4 ACT commands (per rank) can be sent. Limits peak current profile. 0h - Reserved. 1h - Reserved. 2h - 14 DRAM Clocks. 3h - 16 DRAM Clocks (1KB page DDR3-800) 4h - 18 DRAM Clocks. 5h - 20 DRAM Clocks (2KB page DDR3-800, 1KB page DDR3-1066, 1333) 6h - 22 DRAM Clocks. 7h - 24 DRAM Clocks (1KB page DDR3-1600). 8h - 26 DRAM Clocks. 9h - 28 DRAM Clocks (2KB page DDR3-1066). Ah - 30 DRAM Clocks (2KB page DDR3-1333) Bh - 32 DRAM Clocks (2KB page DDR3-1600) Ch - 34 DRAM Clocks. Dh - Reserved Eh - Reserved. Fh - Reserved.
15:14	0x0 RO	**Rsvd_16:** Reserved
13:12	0x0 RW	**tCCD:** CAS to CAS delay. The minimum delay, in DRAM clocks, between 2 RD/WR commands. 0h - 4 DRAM Clocks. Functional mode. (DDR3-800, 1066, 1333, 1600) 1h - 12 DRAM Clocks. DFX stretch mode (x2). 2h - 18 DRAM Clocks. DFX stretch mode (x4). 3h - Reserved
11:8	0x3 RW	**tWTP:** Write to Prechange. The minimum delay, in DRAM clocks, between a WR command and a PRE command to the same bank. Value should be computed as 4 + tWCL + tWR. 0h - 15 DRAM Clocks DDR3-800). 1h - 16 DRAM Clocks. 2h - 17 DRAM Clocks. 3h - 18 DRAM Clocks DDR3-1066). 4h - 19 DRAM Clocks. 5h - 20 DRAM Clocks. 6h - 21 DRAM Clocks DDR3-1333). 7h - 22 DRAM Clocks. 8h - 23 DRAM Clocks. 9h - 24 DRAM Clocks DDR3-1600). Ah - 25 DRAM Clocks Others - Reserved
7:6	0x0 RO	**Rsvd_15:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:4	0x2 RW	**tCMD:** Command Transport Duration. The time period, in DRAM clocks, that a command occupies the DRAM command bus. 1N is the DDR3 basic requirement. 2N and 3N are extended modes for board signal-integrity. 0h - 1 DRAM Clock (1N). 1h - 2 DRAM Clocks (2N). 2h - 3 DRAM Clocks (3N).
3	0x0 RO	**Rsvd_14:** Reserved
2:0	0x0 RW	**tWCL:** CAS Write Latency. The delay, in DRAM clocks, between the internal write command and the availability of the first bit of DRAM input data. 0h - 3 DRAM Clocks (DDR3-800) 1h - 4 DRAM Clocks (DDR3-1066) 2h - 5 DRAM Clocks (DDR3-1333) 3h - 6 DRAM Clocks (DDR3-1600) 4h - 7 DRAM Clocks 5h - 8 DRAM Clocks 6h - 9 DRAM Clocks

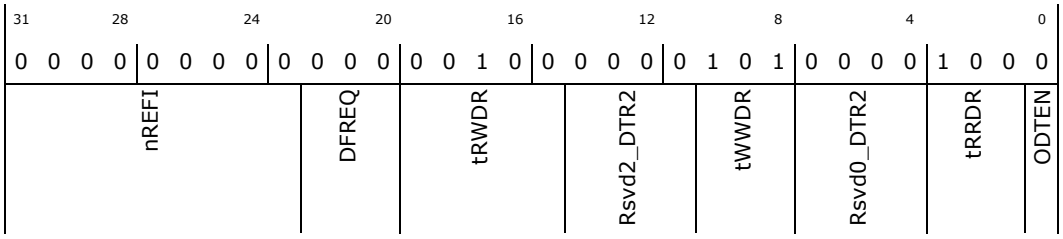
3.1.4 DTR2A (DTR2)—Offset 3h

DRAM Timing Register 2

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00020508h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RW	**nREFI:** JEDEC based refresh interval expressed in periods of DRAM clock/32 (rounded down)
22:20	0x0 RW	**DFREQ:** DRAM Frequency. Specifies the DDR3 frequency used by Dunit for computing proper cycle to cycle timings. Note this configuration has no impact on the actual DRAM clock. 0h - DDR3-800 1h - DDR3-1066 2h - DDR3-1333 3h - DDR3-1600 4h - DDR3-1867 5h - DDR3-2133 Others - Reserved
19:15	0x4 RW	**tRWDR:** Read to Write DQ delay, different ranks, same DIMM 0h - Reserved. 1h - 6 DRAM Clocks. 2h - 7 DRAM Clocks. 3h - 8 DRAM Clocks. 4h - 9 DRAM Clocks. 5h - 10 DRAM Clocks. 6h - 11 DRAM Clocks. 7h - 12 DRAM Clocks. 8h - 13 DRAM Clocks. 9h - 14 DRAM Clocks. Ah - 15 DRAM Clocks. Bh - 16 DRAM Clocks. Ch - 17 DRAM Clocks. Dh - 18 DRAM Clocks. Others - Reserved
14:11	0x0 RO	**Rsvd2_DTR2A (Rsvd2_DTR2):** Reserved
10:8	0x5 RW	**tWWDR:** Write to Write DQ delay, different ranks, same DIMM 0h - Reserved 1h - Reserved 2h - 6 DRAM Clocks. 3h - 7 DRAM Clocks. 4h - 8 DRAM Clocks. 5h - 9 DRAM Clocks. 6h - 10 DRAM Clocks 7h - Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RO	**Rsvd0_DTR2A (Rsvd0_DTR2):** Reserved
3:1	0x4 RW	**tRRDR:** Read to Read DQ delay, different ranks, same DIMM 0h - Reserved 1h - 6 DRAM Clocks. 2h - 7 DRAM Clocks. 3h - 8 DRAM Clocks. 4h - 9 DRAM Clocks. 5h - 10 DRAM Clocks. 6h - 11 DRAM Clocks. Others - Reserved
0	0x0 RW	**ODTEN:** ODT Enable

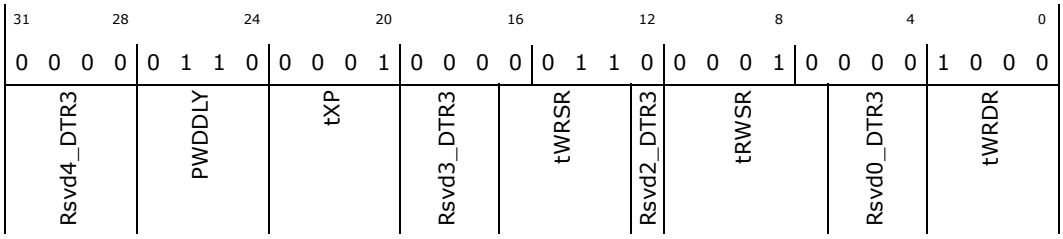
3.1.5 DTR3A (DTR3)—Offset 4h

DRAM Timing Register 3

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 06106108h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Rsvd4_DTR3A (Rsvd4_DTR3):** Reserved
27:24	0x6 RW	**PWDDLY:** RD/WR command to Power-down delay. Non-JEDEC delay for performance enhancement. Delay = PWDDLY x 4 DRAM Clocks.
23:20	0x1 RW	**tXP:** Delay from CKE asserted high to any DRAM command 0h - 2 DRAM Clocks (DDR3-800). 1h - 3 DRAM Clocks (DDR3-1066, 1333) 2h - 4 DRAM Clocks (DDR3-1600). 3h - 5 DRAM Clocks 4h - 6 DRAM Clocks 5h - 7 DRAM Clocks 6h - 8 DRAM Clocks 7h - 9 DRAM Clocks.
19:17	0x0 RO	**Rsvd3_DTR3A (Rsvd3_DTR3):** Reserved
16:13	0x3 RW	**tWRSR:** Write to Read same rank command delay. Should be set to 4 + tWCL + tWTR 0h - 11 DRAM Clocks (LPDDR2-800). 1h - 12 DRAM Clocks. 2h - 13 DRAM Clocks (DDR3-800,LPDDR2-1066). 3h - 14 DRAM Clocks (DDR3-1066,LPDDR3-1333). 4h - 15 DRAM Clocks. 5h - 16 DRAM Clocks (DDR3-1333). 6h - 17 DRAM Clocks. 7h - 18 DRAM Clocks (DDR3-1600). 8h - 19 DRAM Clocks. 9h - 20 DRAM Clocks. Others - Reserved
12	0x0 RO	**Rsvd2_DTR3A (Rsvd2_DTR3):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
11:7	0x2 RW	**tRWSR:** Read to Write same rank command delay. Should be set to tCL - tWCL + 6 + board delay if needed. 0h - 6 DRAM Clocks. 1h - 7 DRAM Clocks. 2h - 8 DRAM Clocks. 3h - 9 DRAM Clocks. 4h - 10 DRAM Clocks. 5h - 11 DRAM Clocks. 6h - 12 DRAM Clocks. 7h - 13 DRAM Clocks. 8h - 14 DRAM Clocks. 9h - 15 DRAM Clocks. Ah - 16 DRAM Clocks. Bh - 17 DRAM Clocks. Others - Reserved
6:4	0x0 RO	**Rsvd0_DTR3A (Rsvd0_DTR3):** Reserved
3:0	0x8 RW	**tWRDR:** Write to Read DQ delay, different ranks, same DIMM 0h - Reserved 1h - 4 DRAM Clocks. 2h - 5 DRAM Clocks. 3h - 6 DRAM Clocks. 4h - 7 DRAM Clocks. 5h - 8 DRAM Clocks. 6h - 9 DRAM Clocks. 7h - 10 DRAM Clocks.

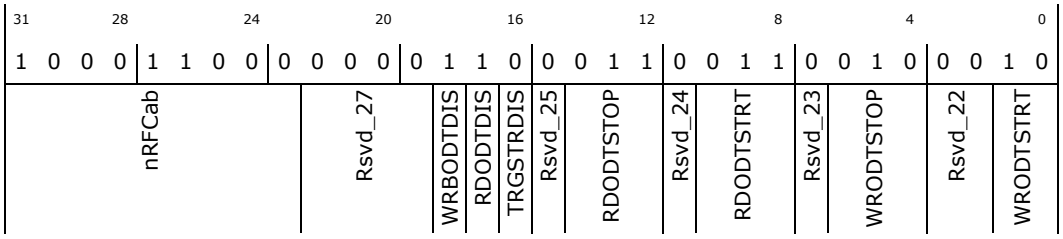
3.1.6 DTR4A (DTR4)—Offset 5h

DRAM Timing Register 4

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 8C063322h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x118 RW	**nRFCab:** The number of DRAM clocks used to define tRFC for DDR3, tRFCab for LPDDR2/3
22:19	0x0 RO	**Rsvd_27:** Reserved
18	0x1 RW	**WRBODTDIS:** Disable Write ODT on non-targeted DIMM. When writing to DIMM A, ODT is asserted to the target rank of DIMM A and also to the low rank of DIMM B. This defeature bit is used to disable ODT assertion to the opposite DIMM during write.
17	0x1 RW	**RDODTDIS:** Disable Read ODT. When reading from DIMM A, ODT is asserted to the low rank of DIMM B. This defeature bit is used to disable ODT assertion during reads.
16	0x0 RW	**TRGSTRDIS:** Write target rank is not stretched. When set, stretched ODT as defined above is not applied to the write target rank and ODT command is asserted for 6 DRAM clocks. Should not be used when ODT is pulled-in.
15	0x0 RO	**Rsvd_25:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
14:12	0x3 RW	**RDODTSTOP:** Read command to ODT de-assert delay Value should be set to: RDODTSTRT+6+(WRODTSTOP-WRODTSTRT) 0h - 6 DRAM Clocks. 1h - 7 DRAM Clocks. 2h - 8 DRAM Clocks. 3h - 9 DRAM Clocks. 4h - 10 DRAM Clocks. 5h - 11 DRAM Clocks. 6h - 12 DRAM Clocks. 7h - 13 DRAM Clocks. Other - Reserved.
11	0x0 RO	**Rsvd_24:** Reserved
10:8	0x3 RW	**RDODTSTRT:** Read command to ODT assert delay. Value should be set to tCMD+tCL-tWCL-ODT_PULLIN, where ODT_PULLIN must have the same value as in WRODTSTRT. 0h - 0 DRAM Clocks. 1h - 1 DRAM Clocks. 2h - 2 DRAM Clocks. 3h - 3 DRAM Clocks. 4h - 4 DRAM Clocks. 5h - 5 DRAM Clocks. Other - Reserved.
7	0x0 RO	**Rsvd_23:** Reserved
6:4	0x2 RW	**WRODTSTOP:** Write command to ODT de-assert delay. WRODTSTOP 1N 2N 3N 0h WR+6 N/A N/A 1h WR+7 WR+6 N/A 2h WR+8 WR+7 WR+6 3h WR+9 WR+8 WR+7 4h WR+10 WR+9 WR+8 Other Reserved Reserved Reserved
3:2	0x0 RO	**Rsvd_22:** Reserved
1:0	0x2 RW	**WRODTSTRT:** WR command to ODT assert delay. JEDEC requires ODT to be asserted on the same clock with the WR command. Dunit allows to pull-in by 1 clock in 2N mode and by 1-2 clocks in 3N mode. For most DIMM configurations, this register should be programmed to same value as tCMD. A value of tCMD - ODT_PULLIN can be used according to the table below which shows the ODT command assertion with respect to the WR command assertion. WRODTSTRT 1N 2N 3N 0h WR WR-1 WR-2 1h N/A WR WR-1 2h N/A N/A WR 3h Reserved Reserved Reserved

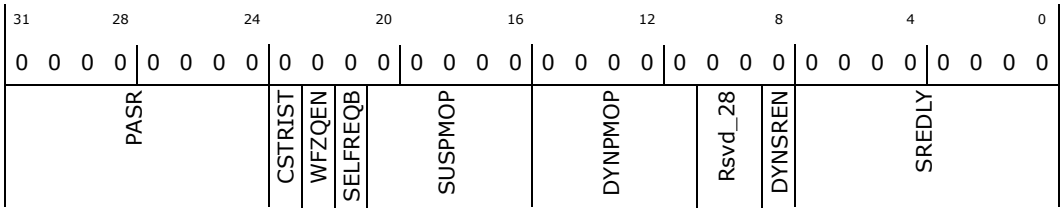
3.1.7 DPMC0—Offset 6h

DRAM Power Management Control 0

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**PASR:** This is the Segment Mask used for the MRW to MR17 during SUSPENDP (Partial Array Self Refresh support. This is only used for LPDDR2/3.
23	0x0 RW	**CSTRIST:** Tristate Chip-Select 0 - Never tristate. 1 - From SRE to SRX+tXS. Note, DDRIO may tristate during SR so this adds on the boundaries.
22	0x0 RW	**WFZQEN:** Enable ZQ Calibration (long) in WAKEF
21	0x0 RW	**SELFREQB:** Select Frequency Parameter Set B
20:16	0x0 RW	**SUSPMOP:** SPID Power Mode Opcode. The PM Message ID the Dunit will send to DDRIO on ispid_pm_pm bus after SR Entry command to DRAM as result of SUSPEND from P-unit. This message defines the DDRIO power-mode during SR period. Value can be changed on-the-fly to allow different power modes (for example, deeper PM for S3 than for C6). Power saving and Entry/Exit latencies are described in the MODMEM HAS.
15:11	0x0 RW	**DYNPMOP:** SPID Power Mode Opcode. The PM Message ID the Dunit will send to DDRIO on ispid_pm_pm bus after SR Entry command to DRAM as result of Dynamic Self-refresh. This message defines the DDRIO power-mode during SR period. Value can be changed on-the-fly to allow different power modes (for example, deeper PM for S3 than for C6). Power saving and Entry/Exit latencies are described in the MODMEM HAS.
10:9	0x0 RO	**Rsvd_28:** Reserved
8	0x0 RW	**DYNSREN:** Dynamic Self-Refresh Enable. Setting this bit to 1, enables automatic SR command to DRAM and PM message to DDRIO when the PMI bus is idle, all pending requests have been served and the and PMI status is less than 2, SREDLY has timed-out, and all JEDEC requirements are satisfied. This register may be changed by BIOS/FW on-the-fly.
7:0	0x0 RW	**SREDLY:** Self-Refresh Entry delay. The delay, in core-clocks, between PMI idle (no pending requests and PMI status is less than 2) and SR Entry when Dunit is in Dynamic SR mode.

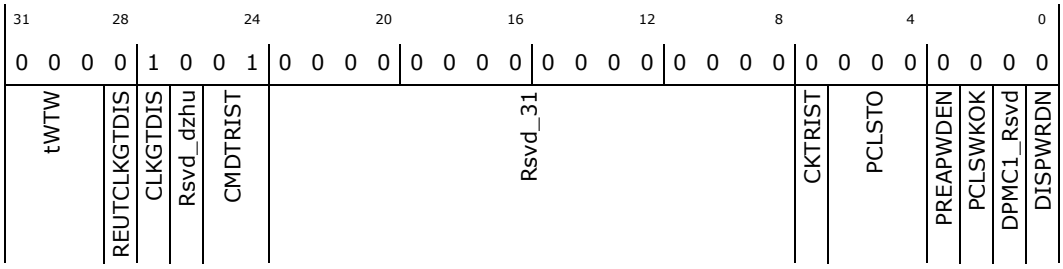
3.1.8 DPMC1—Offset 7h

DRAM Power Management Control 1

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 09000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**tWTW:** Minimum idle time between non back-to-back memory writes (BIB breaker)
28	0x0 RW	**REUTCLKGTDIS:** REUT Clock Gate Disable 0h REUT clock is gated when DCO.PMICTL is set to 0. 1h REUT clock is upgated, overriding the DCO.PMICTL config bit. Note: The DCO.REUTLOCK bit overrides this bit.
27	0x1 RW	**CLKGTDIS:** Clock Gating Disabled. Setting this bit to 0 allows a large number of internal Dunit clocks to be gated when there is no activity in order to save power. When set to 1, internal clock-gating is disabled. 0 - Enable. 1 - Disable.
26	0x0 RO	**Rsvd_dzhu:** Reserved
25:24	0x1 RW	**CMDTRIST:** Tristate Command and Address Bus to DRAM 0h - CMD/ADDR are never tristated. 1h - CMD/ADDR are tristated only when all CKE are low. 2h - CMD/ADDR are tristated when no valid command. 3h - CMD/ADDR are tristated when no valid command but may never be tristated for less than 2 DRAM clocks. This mode is only valid when tCMD is set to 0h (1N mode).
23:8	0x0 RO	**Rsvd_31:** Reserved
7	0x0 RW	**CKTRIST:** Tristate CK 0 - Never tristate. 1 - PDE Note, DDRIO may tristate during PD so this adds on the boundaries.
6:4	0x0 RW	**PCLSTO:** Page Close Timeout Period. Specifies the time frame, in ns, from last access to a DRAM page until that page may be scheduled for closing (by sending a PRE command). 0h - Disable page close timer (init/training). 1h - Immediate page close. 2h - 30-60 ns to page close. 3h - 60-120 ns to page close. 4h - 120-240 ns to page close. 5h - 240-480 ns to page close. 6h - 480-960 ns to page close. 7h - 1-2 s to page close.
3	0x0 RW	**PREAPWDEN:** Send Precharge All Command to a Rank before PD-Enter. Setting this bit to 1 will allow sending a PREA command before PDE command. 0 - Disable. 1 - Enable.
2	0x0 RW	**PCLSWKOK:** Wake Allowed for Page Close Timeout. Setting this bit to 1 indicates the Dunit can send DRAM devices a PD-Exit command in order to close single bank if the page timer expired. Note this bit applies only to cases where at least one other bank in the same rank is open but not timed-out. If all banks in the rank timed-out, a PD-Exit command will be sent regardless of this bit. Must be set to 0 during init/training mode. 0 - Disable. 1 - Enable.
1	0x0 RO	**DPMC1_Rsvd:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**DISPWRDN:** Disable Power Down. Setting this bit to 1 will block CKE high-)low transitions. May be used by BIOS during init flow and should be set to 0 for functional mode. 0 - The Dunit dynamically controls the CKE pins to place the DRAM device in power down mode. 1 - The Dunit constantly drives the CKE pins high.

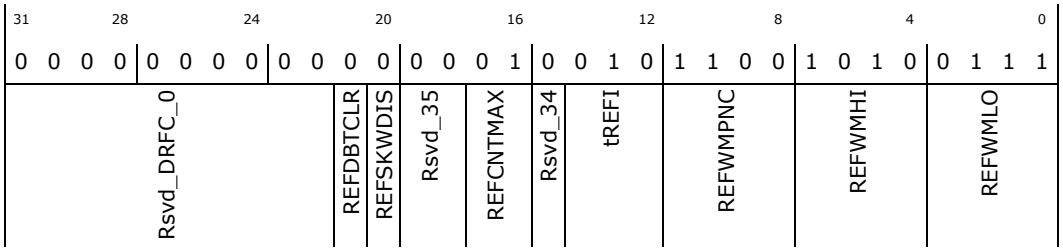
3.1.9 DRFC—Offset 8h

DRAM Refresh Control

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00012CA7h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Rsvd_DRFC_0:** Reserved
21	0x0 RW	**REFDBTCLR:** Clear Refresh Debit before SR Entry When this bit is set, if enough REF commands are pulled-in, Dunit will not send additional REF commands before SR Entry. 0h - Disabled. 1h - Enabled.
20	0x0 RW	**REFSKWDIS:** Refresh counters may be increased in 2 policies - skewed or simultaneously. 0h - counters are updated per rank every tREFI. 1h - all counters are updated every tREFI.
19:18	0x0 RO	**Rsvd_35:** Reserved
17:16	0x1 RW	**REFCNTMAX:** Refresh Max tREFI Interval. The maximum interval between ant two REF commands per rank. JEDEC allows a maximum of 9 x tREFI intervals. 0h - 6 x tREFI. 1h - 7 x tREFI. 2h - 8 x tREFI. 3h - 9 x tREFI. Should not be changed after initial setting.
15	0x0 RO	**Rsvd_34:** Reserved
14:12	0x2 RW	**tREFI:** Refresh Period. Specifies the average time between sending REF commands to DRAM. The Dunit will guarantee that the average time is met, but maintains a certain degree of flexibility in the exact REF scheduling in order to increase overall performance. 0h - Refresh disabled 1h - Reserved for pre-silicon simulation. 2h - 3.9 s (Extended Temperature Range, 85-95 C) 3h - 7.8 s (Normal Temperature Range, 0-85 C)

Bit Range	Default & Access	Field Name (ID): Description
11:8	0xc RW	**REFWMPNC:** Refresh Panic Watermark. When the refresh debit counter, per rank, is greater than this value, the Dunit will send a REF command even if there are some pending requests and regardless of the PMI status level. Refer DDR3 spec for Refresh Postponing/Pulling-In flexibility. May be changed to functional value after init sequence. Value should be greater than, or equal, to REFWMHI. 0-5h - Reserved 6h - Allow REF command every tREFI. 7h - Postpone 2 REF commands. 8h - Postpone 3 REF commands. 9h - Postpone 4 REF commands. Ah - Postpone 5 REF commands. Bh - Postpone 6 REF commands. Ch - Postpone 7 REF commands. Dh - Postpone 8 REF commands. E-Fh - Reserved.
7:4	0xa RW	**REFWMHI:** Refresh High Watermark. When the refresh debit counter, per rank, is greater than this value, the Dunit will send a REF command even if there are some pending requests to the rank but not if the PMI status is equal to 3. Refer DDR3 spec for Refresh Postponing/Pulling-In flexibility. May be changed to functional value after init sequence. Value should be greater than, or equal, to REFWMLO. 0-5h - Reserved 6h - Allow REF command every tREFI. 7h - Postpone 2 REF commands. 8h - Postpone 3 REF commands. 9h - Postpone 4 REF commands. Ah - Postpone 5 REF commands. Bh - Postpone 6 REF commands. Ch - Postpone 7 REF commands. Dh - Postpone 8 REF commands. E-Fh - Reserved.
3:0	0x7 RW	**REFWMLO:** Opportunistic Refresh Watermark. When the refresh debit counter, per rank, is greater than this value, the Dunit will send a REF command only if there are no pending requests to the rank and the PMI status is less than 3. Refer DDR3 spec for Refresh Postponing/Pulling-In flexibility. May be changed to functional value after init sequence. 0-3h - Reserved 4h - Allow pulling-in 2 REF commands. 5h - Allow pulling-in 1 REF commands. 6h - Allow REF command every tREFI. 7h - Postpone 2 REF commands. 8h - Postpone 3 REF commands. 9h - Postpone 4 REF commands. Ah - Postpone 5 REF commands. Bh - Postpone 6 REF commands. Ch - Postpone 7 REF commands. Dh - Postpone 8 REF commands. E-Fh - Reserved.

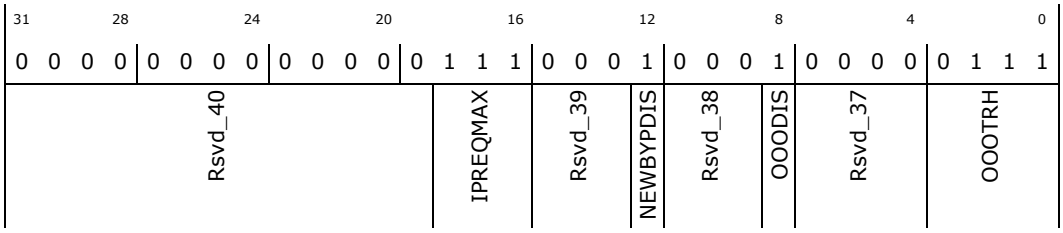
3.1.10 DSCH—Offset 9h

DRAM Scheduler Control

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00071107h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0x0 RO	**Rsvd_40:** Reserved
18:16	0x7 RW	**IPREQMAX:** Maximal number of In-Process Requests stored in the Dunit. Number of pending requests = IPREQMAX+1; Value may be changed after init/training when PMI is idle.
15:13	0x0 RO	**Rsvd_39:** Reserved
12	0x1 RW	**NEWBYPDIS:** Disable New Request Bypass. Setting this bit to 0 will allow a new request to bypass the normal Dunit internal arbiter when there are no pending commands. 0h - Enable New Request Bypass. 1h - Disable New Request Bypass.
11:9	0x0 RO	**Rsvd_38:** Reserved
8	0x1 RW	**OOODIS:** Disable Out-of-Order . 0h - OOO enabled. 1h - OOO disabled. Should be disabled during init/training and can be enabled for functional mode.
7:4	0x0 RO	**Rsvd_37:** Reserved
3:0	0x7 RW	**OOOTRH:** Out-of-Order Aging Threshold. Number of PMI requests that can bypass any pending request before OOO will be disabled. This mechanism prevents starvation of pending commands.

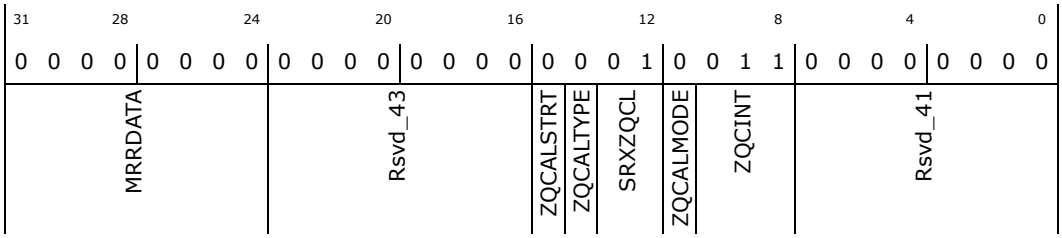
3.1.11 DCAL—Offset Ah

DRAM Calibration Control

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00001300h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MRRDATA:** MRR Data
23:16	0x0 RO	**Rsvd_43:** Reserved
15	0x0 RW/AC	**ZQCALSTRT:** ZQ Calibration Start

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW/P	**ZQCALTYPE:** ZQ Calibration Type
13:12	0x1 RW/P	**SRXZQCL:** ZQ Calibration Long After SR Exit Control 0h - ZQCL commands after SRX are sent in parallel. 1h - ZQCL commands are sent serially to ranks. 2h - No ZQCL is sent after SR Exit. 3h Reserved.
11	0x0 RW/P	**ZQCALMODE:** ZQ Calibration Mode
10:8	0x3 RW/P	**ZQCINT:** ZQ Calibration Short Interval. The time interval, in ms, between ZQCS commands to a DRAM device. ZQCS commands are sent to a single DRAM device and commands are distributed and non-overlapping in the interval. 0h - Disabled. 1h - 62s (for pre-silicon simulation only) 2h - 31ms. 3h - 63ms. 4h - 126ms. 5-7h - Reserved. May be changed on-the-fly in response to thermal events.
7:0	0x0 RO	**Rsvd_41:** Reserved

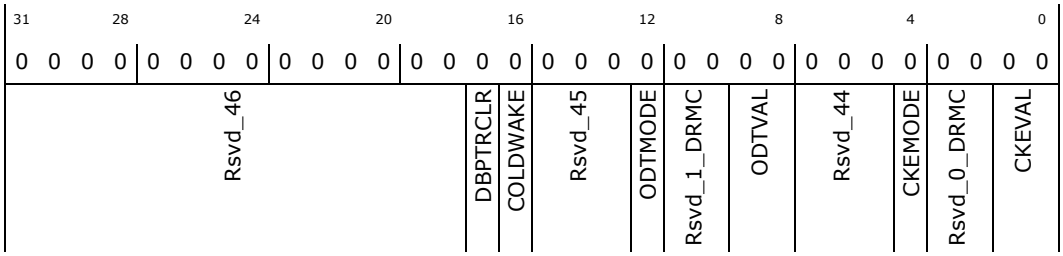
3.1.12 DRMC—Offset Bh

DRAM Reset Management Control

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0x0 RO	**Rsvd_46:** Reserved
17	0x0 RW/AC	**DBPTRCLR:** When this bit is set, Dunit data buffer read/write pointers are cleared to 0. This bit auto-clears when pointer reset are done.
16	0x0 RW	**COLDWAKE:** BIOS should set this bit to 1 before sending WAKE command to Dunit after Cold Reset. For S3 Exit, or any other mode in which the DRAM is in SR, this bit must be set to 0.
15:13	0x0 RO	**Rsvd_45:** Reserved
12	0x0 RW	**ODTMODE:** ODT Control Mode 0h - Dunit. 1h - SW override.

Bit Range	Default & Access	Field Name (ID): Description
11:10	0x0 RO	**Rsvd_1_DRMC:** Reserved
9:8	0x0 RW	**ODTVAL:** When ODTMODE is set to 1, ODT pins to DRAM are overridden by ODTVAL. Used only during init flow by BIOS.
7:5	0x0 RO	**Rsvd_44:** Reserved
4	0x0 RW	**CKEMODE:** CKE Control Mode 0h - Dunit. 1h - SW override.
3:2	0x0 RO	**Rsvd_0_DRMC:** Reserved
1:0	0x0 RW	**CKEVAL:** When CKEMODE is set to 1, CKE pins to DRAM are overridden by CKEVAL. Used only during init flow by BIOS.

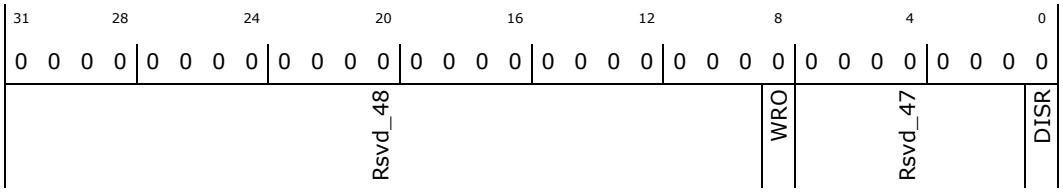
3.1.13 PMSTS—Offset Ch

Power Management Status

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**Rsvd_48:** Reserved
8	0x0 RW/P	**WRO:** Warm Reset Occurred. Set by the Punit whenever a Reset Warn is received, and cleared by powergood=0. 0h: No Warm Reset occurred. 1h: Warm Reset occurred. BIOS Requirement. BIOS can check and clear this bit whenever executing POST code. This way BIOS knows that if the bit is set, then DISR indicates whether DRAM entered Self-Refresh.
7:1	0x0 RO	**Rsvd_47:** Reserved
0	0x0 RW/P	**DISR:** DRAM In Self-Refresh. Set by Dunit hardware after Channel is placed in self refresh as a result of a Power State or a Reset Warn sequence. Cleared by Dunit hardware before starting Channel 0 self refresh exit sequence initiated by a power management exit. Cleared by the BIOS by writing 1 in a warm reset (Reset# asserted while PWROK is asserted) exit sequence. 0 - DRAM not guaranteed to be in Self-Refresh. 1 - DRAM in Self-Refresh.

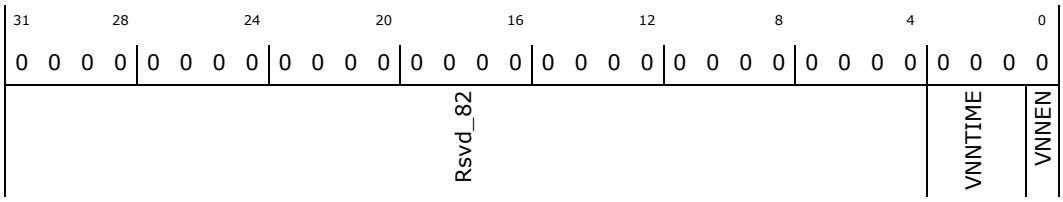
3.1.14 VNNTIMER—Offset Dh

DRAM VNN Scaling Timer

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**Rsvd_82:** Reserved
3:1	0x0 RW/P	**VNNTIME:** VNN Scaling Timer
0	0x0 RW/P	**VNNEN:** VNN Scaling Enable

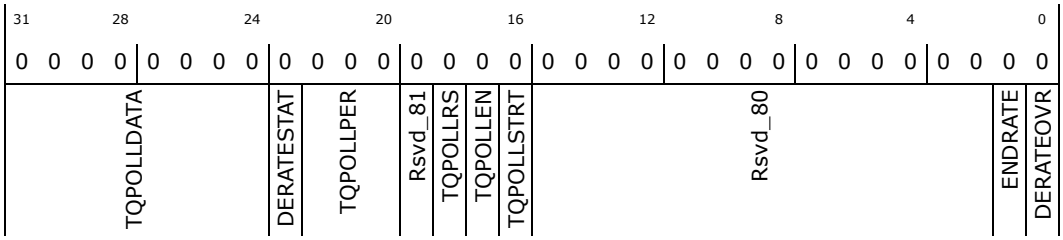
3.1.15 TQCTL—Offset Eh

DRAM TQ Control

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**TQDATA (TQPOLLDATA):** TQ Data
23	0x0 RO	**DERATESTAT:** Timing De-rating Status

Bit Range	Default & Access	Field Name (ID): Description
22:20	0x0 RW/P	**TQPOLLPER:** TQ Poll Period
19	0x0 RO	**Rsvd_81:** Reserved
18	0x0 RW/P	**TQPOLLRS:** TQ Poll RS
17	0x0 RW/P	**TQPOLLEN:** TQ Poll Enable
16	0x0 RW/AC	**TQPOLLSTRT:** TQ Poll Start
15:2	0x0 RO	**Rsvd_80:** Reserved
1	0x0 RW	**ENDRATE:** Enabled Dynamic Timing De-rating
0	0x0 RW	**DERATEOVR:** Enabled Timing De-rating Override

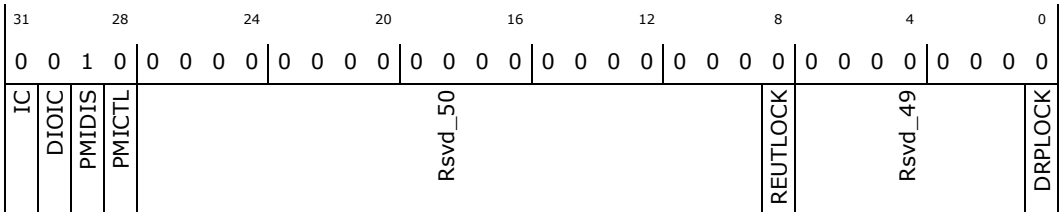
3.1.16 DCO—Offset Fh

DRAM Control Operation

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 20000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**IC:** Dunit Initialization Complete. This bit should be set by BIOS after Dunit programming is complete and Dunit is ready to accept PMI requests and perform DRAM maintenance operations.
30	0x0 RO	**DIOIC:** Status indication that DDRIO initialization is complete. Reflects ospid_init_complete.
29	0x1 RW	**PMIDIS:** Disable PMI interface. When this bit is set to 1, the Dunit will not response to requests from either the Bunit or REUT.

Bit Range	Default & Access	Field Name (ID): Description
28	0x0 RW	**PMICTL:** PMI Control Select. 0h - PMI is owned by Bunit. 1h - PMI is owned by REUT. Whenever this bit is toggled, Dunit will flush all pending DRAM requests from previous owner before it accepts requests from new owner. This bit is also used when REUT is disabled in order to gracefully flush pending request and putting DRAM into IDLE state before sending MRS commands in functional mode.
27:9	0x0 RO	**Rsvd_50:** Reserved
8	0x0 RW/P	**REUTLOCK:** After this bit is set to 1, all REUT is clock gated and locked and cannot be used. REUTLOCK can be set only once, and will only reset when powergood = 0.
7:1	0x0 RO	**Rsvd_49:** Reserved
0	0x0 RW/P	**DRPLOCK:** After this bit is set to 1, all DRP bits are locked and cannot be written again. DRPLOCK can be written only once. DRPLOCK and DRP bit values will only reset when powergood = 0.

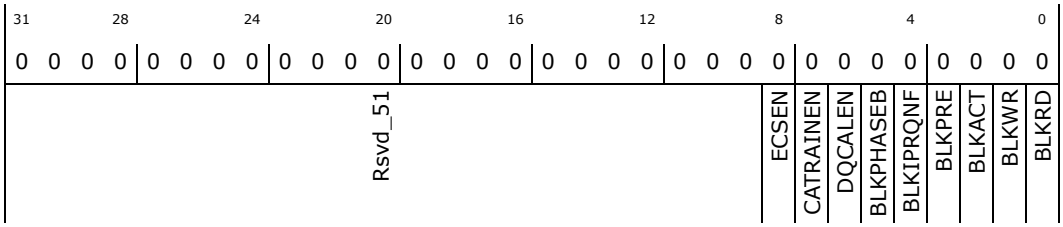
3.1.17 DTRC—Offset 10h

DRAM Training Control

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**Rsvd_51:** Reserved
8	0x0 RW	**ECSEN:** Extended CS# Enable
7	0x0 RW	**CATRAINEN:** CA Training Enable
6	0x0 RW	**DQCALEN:** DQ Calibration Enable

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**BLKPHASEB:** Block All PhaseB Commands. Dunit operates at coreclock which is half the frequency of the DRAM clock. When this bit is set, only one command can be scheduled each coreclock. This bit may be used for DFX applications.
4	0x0 RW/V	**BLKIPRQNF:** Block all IP Requests until Queue is Full. When this bit is set to 1, all Dunit are stalled until the IP pool is full. This bit is self-clearing, and once asserted, writing 0 has no impact. The IPREQ pool is only reopened when the number of pending requests reaches DSCH.IPREQMAX+1.
3	0x0 RW	**BLKPRE:** Block Precharge Commands to DRAM 0 - No Block 1 - Block
2	0x0 RW	**BLKACT:** Block Activate Commands to DRAM 0 - No Block 1 - Block
1	0x0 RW	**BLKWR:** Block Write Commands to DRAM 0 - No Block 1 - Block
0	0x0 RW	**BLKRD:** Block Read Commands to DRAM 0 - No Block 1 - Block

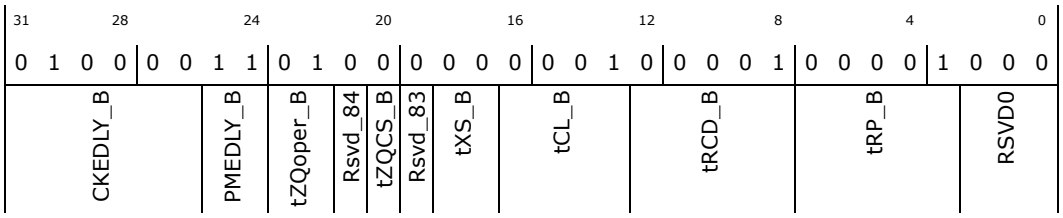
3.1.18 DTR0B—Offset 11h

DRAM Timing Register 0B

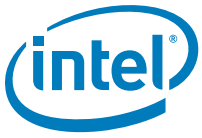
Access Method

Type: ??? Register
(Size: 32 bits)

Default: 43402108h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x10 RW	**CKEDLY_B:** Additional delay between CK/CKB start and SRX command. This delay is needed for clock to stabilize to meet JEDEC requirements. Delay is CKEDLY multiples of 256 DRAM Clocks. 0ns to 9,600ns (DDR3-800) 0ns to 7,200ns (DDR3-1066)
25:24	0x3 RW	**PMEDLY_B:** The delay, in DRAM clocks, between SR Entry command and Power-Mode message to DDRIO. 0h - 6 DRAM Clocks. 1h - 8 DRAM Clocks. 2h - 10 DRAM Clocks. 3h - 12 DRAM Clocks.
23:22	0x1 RW	**tZQoper_B:** The delay, in DRAM clocks, between ZQC-Long command to any command. Note, ZQCL command during DRAM Init flow requires longer latency which is controlled be BIOS. 0h - 256 DRAM Clocks. 1h - 384 DRAM Clocks.



Bit Range	Default & Access	Field Name (ID): Description
21	0x0 RO	**Rsvd_84:** Reserved
20	0x0 RW	**tZQCS_B:** The delay, in DRAM clocks, between a ZQC-Short command to any command. 0h - 64 DRAM Clocks. 1h - 96 DRAM Clocks.
19	0x0 RO	**Rsvd_83:** Reserved
18:17	0x0 RW	**tXS_B:** The delay, in DRAM clocks, between SRX command to command not requiring locked DLL. The Dunit can send a ZQCL command after tXS. JEDEC defines MAX(5CK, tRFC(min)+10ns) so both values take safety margin. 0h - 256 DRAM Clocks. 1h - 384 DRAM Clocks.
16:13	0x1 RW	**tCL_B:** CAS Latency. Specifies the delay, in DRAM clocks, between the issue of a RD command and the return of valid data on the DQ bus. 0h - 5 DRAM Clocks (DDR3- 800) 1h - 6 DRAM Clocks (DDR3- 800, 1066) 2h - 7 DRAM Clocks (DDR3- 1066, 1333) 3h - 8 DRAM Clocks (DDR3- 1066, 1333, 1600) 4h - 9 DRAM Clocks (DDR3- 1333, 1600) 5h - 10 DRAM Clocks (DDR3- 1333, 1600) 6h - 11 DRAM Clocks (DDR3- 1600) 7h - 12 DRAM Clocks 8h - 13 DRAM Clocks Others - Reserved
12:8	0x1 RW	**tRCD_B:** Activate (RAS) to CAS Delay. Specifies the delay, in DRAM clocks, between an ACT command and a RD/WR command to the same bank. 0h - 5 DRAM Clocks (DDR3- 800) 1h - 6 DRAM Clocks (DDR3- 800, 1066) 2h - 7 DRAM Clocks (DDR3- 1066, 1333) 3h - 8 DRAM Clocks (DDR3- 1066, 1333, 1600) 4h - 9 DRAM Clocks (DDR3- 1333, 1600) 5h - 10 DRAM Clocks (DDR3- 1333, 1600) 6h - 11 DRAM Clocks (DDR3- 1600) 7h - 12 DRAM Clocks 8h - 13 DRAM Clocks 9h - 14 DRAM Clocks Ah - 15 DRAM Clocks Bh - 16 DRAM Clocks Ch - 17 DRAM Clocks Dh - 18 DRAM Clocks Eh - 19 DRAM Clocks Fh - 20 DRAM Clocks 10h - 21 DRAM Clocks 11h - 22 DRAM Clocks Others - Reserved
7:3	0x1 RW	**tRP_B:** Precharge to Activate Delay. Specifies the delay, in DRAM clocks, between a PRE command and an ACT command to the same bank. 0h - 5 DRAM Clocks (DDR3- 800) 1h - 6 DRAM Clocks (DDR3- 800, 1066) 2h - 7 DRAM Clocks (DDR3- 1066, 1333) 3h - 8 DRAM Clocks (DDR3- 1066, 1333, 1600) 4h - 9 DRAM Clocks (DDR3- 1333, 1600) 5h - 10 DRAM Clocks (DDR3- 1333, 1600) 6h - 11 DRAM Clocks (DDR3- 1600) 7h - 12 DRAM Clocks 8h - 13 DRAM Clocks 9h - 14 DRAM Clocks Ah - 15 DRAM Clocks Bh - 16 DRAM Clocks Ch - 17 DRAM Clocks Dh - 18 DRAM Clocks Eh - 19 DRAM Clocks Fh - 20 DRAM Clocks 10h - 21 DRAM Clocks 11h - 22 DRAM Clocks Others - Reserved
2:0	0x0 RO	**RSVD0:** Reserved

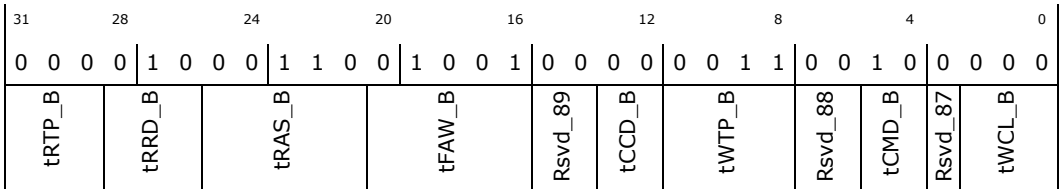
3.1.19 DTR1B—Offset 12h

DRAM Timing Register 1B

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 08C90320h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**tRTP_B:** Read to Precharge Delay. The minimal delay between RD command and PRE command to same bank. 00 - 4 DRAM Clocks (DDR3-800 DDR3-1066) 01 - 5 DRAM Clocks (DDR3-1333) 10 - 6 DRAM Clocks (DDR3-1600) 11 - 7 DRAM Clocks
28:26	0x2 RW	**tRRD_B:** Row Activation to Row Activation Delay. The minimal time interval between 2 ACT commands to any bank in the same DRAM device. Limits peak current profile. 00 - 4 DRAM Clocks (1KB page DDR3-800, 1066, 1333), (2KB page DDR3-800) 01 - 5 DRAM Clocks (1KB page DDR3-1600), (2KB page DDR3-1333) 1 0 - 6 DRAM Clocks (2KB page DDR3-1066, 1600) 11 - 7 DRAM Clocks
25:21	0x6 RW	**tRAS_B:** Row Activation Period. The minimal delay, in DRAM clocks, between ACT command and PRE command to same bank. At least equal to tRCD + tCWL + tCCD + tWR 0h -14 DRAM Clocks. 1h -15 DRAM Clocks (DDR3-800) 2h -16 DRAM Clocks. 3h -17 DRAM Clocks. 4h -18 DRAM Clocks. 5h -19 DRAM Clocks. 6h -20 DRAM Clocks (DDR3-1066) 7h -21 DRAM Clocks. 8h -22 DRAM Clocks. 9h -23 DRAM Clocks. Ah -24 DRAM Clocks (DDR3-1333) Bh -25 DRAM Clocks. Ch -26 DRAM Clocks. Dh -27 DRAM Clocks. Eh -28 DRAM Clocks (DDR3-1600) Fh -29 DRAM Clocks.
20:16	0x9 RW	**tFAW_B:** Four Bank Activation Window. A rolling time-frame, in which a maximum of 4 ACT commands (per rank) can be sent. Limits peak current profile. 0h - Reserved. 1h - Reserved. 2h - 14 DRAM Clocks. 3h - 16 DRAM Clocks (1KB page DDR3-800) 4h - 18 DRAM Clocks. 5h - 20 DRAM Clocks (2KB page DDR3-800, 1KB page DDR3-1066, 1333) 6h - 22 DRAM Clocks. 7h - 24 DRAM Clocks (1KB page DDR3-1600). 8h - 26 DRAM Clocks. 9h - 28 DRAM Clocks (2KB page DDR3-1066). Ah - 30 DRAM Clocks (2KB page DDR3-1333) Bh - 32 DRAM Clocks (2KB page DDR3-1600) Ch - 34 DRAM Clocks. Dh - Reserved Eh - Reserved. Fh - Reserved.
15:14	0x0 RO	**Rsvd_89:** Reserved
13:12	0x0 RW	**tCCD_B:** CAS to CAS delay. The minimum delay, in DRAM clocks, between 2 RD/WR commands. 0h - 4 DRAM Clocks. Functional mode. (DDR3-800, 1066, 1333, 1600) 1h - 12 DRAM Clocks. DFX stretch mode (x2). 2h - 18 DRAM Clocks. DFX stretch mode (x4). 3h - Reserved
11:8	0x3 RW	**tWTP_B:** Write to Prechange. The minimum delay, in DRAM clocks, between a WR command and a PRE command to the same bank. Value should be computed as 4 + tWCL + tWR. 0h - 15 DRAM Clocks DDR3-800). 1h - 16 DRAM Clocks. 2h - 17 DRAM Clocks. 3h - 18 DRAM Clocks DDR3-1066). 4h - 19 DRAM Clocks. 5h - 20 DRAM Clocks. 6h - 21 DRAM Clocks DDR3-1333). 7h - 22 DRAM Clocks. 8h - 23 DRAM Clocks. 9h - 24 DRAM Clocks DDR3-1600). Ah - 25 DRAM Clocks Others - Reserved
7:6	0x0 RO	**Rsvd_88:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
5:4	0x2 RW	**tCMD_B:** Command Transport Duration. The time period, in DRAM clocks, that a command occupies the DRAM command bus. 1N is the DDR3 basic requirement. 2N and 3N are extended modes for board signal-integrity. 0h - 1 DRAM Clock (1N). 1h - 2 DRAM Clocks (2N). 2h - 3 DRAM Clocks (3N).
3	0x0 RO	**Rsvd_87:** Reserved
2:0	0x0 RW	**tWCL_B:** CAS Write Latency. The delay, in DRAM clocks, between the internal write command and the availability of the first bit of DRAM input data. 0h - 3 DRAM Clocks (DDR3-800) 1h - 4 DRAM Clocks (DDR3-1066) 2h - 5 DRAM Clocks (DDR3-1333) 3h - 6 DRAM Clocks (DDR3-1600) 4h - 7 DRAM Clocks 5h - 8 DRAM Clocks 6h - 9 DRAM Clocks

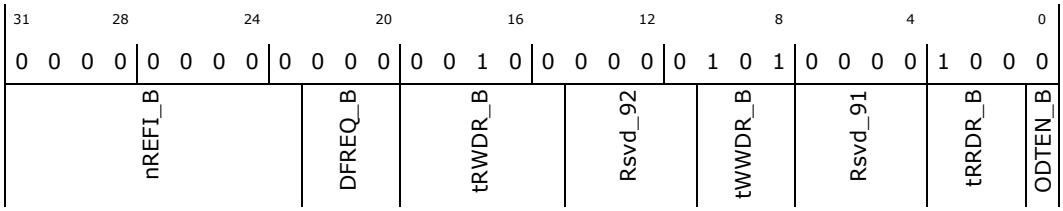
3.1.20 DTR2B—Offset 13h

DRAM Timing Register 2B

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00020508h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RW	**nREFI_B:** JEDEC based refresh interval expressed in periods of DRAM clock/ 32 (rounded down)
22:20	0x0 RW	**DFREQ_B:** DRAM Frequency. Specifies the DDR3 frequency used by Dunit for computing proper cycle to cycle timings. Note this configuration has no impact on the actual DRAM clock. 0h - DDR3-800 1h - DDR3-1066 2h - DDR3-1333 3h - DDR3-1600 4h - DDR3-1867 5h - DDR3-2133 Others - Reserved
19:15	0x4 RW	**tRWDR_B:** Read to Write DQ delay, different ranks, same DIMM 0h - Reserved. 1h - 6 DRAM Clocks. 2h - 7 DRAM Clocks. 3h - 8 DRAM Clocks. 4h - 9 DRAM Clocks. 5h - 10 DRAM Clocks. 6h - 11 DRAM Clocks. 7h - 12 DRAM Clocks. 8h - 13 DRAM Clocks. 9h - 14 DRAM Clocks. Ah - 15 DRAM Clocks. Bh - 16 DRAM Clocks. Ch - 17 DRAM Clocks. Dh - 18 DRAM Clocks. Others - Reserved
14:11	0x0 RO	**Rsvd_92:** Reserved
10:8	0x5 RW	**tWWDR_B:** Write to Write DQ delay, different ranks, same DIMM 0h - Reserved 1h - Reserved 2h - 6 DRAM Clocks. 3h - 7 DRAM Clocks. 4h - 8 DRAM Clocks. 5h - 9 DRAM Clocks. 6h - 10 DRAM Clocks 7h - Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RO	**Rsvd_91:** Reserved
3:1	0x4 RW	**tRRDR_B:** Read to Read DQ delay, different ranks, same DIMM 0h - Reserved 1h - 6 DRAM Clocks. 2h - 7 DRAM Clocks. 3h - 8 DRAM Clocks. 4h - 9 DRAM Clocks. 5h - 10 DRAM Clocks. 6h - 11 DRAM Clocks. Others - Reserved
0	0x0 RW	**ODTEN_B:** ODT Enable

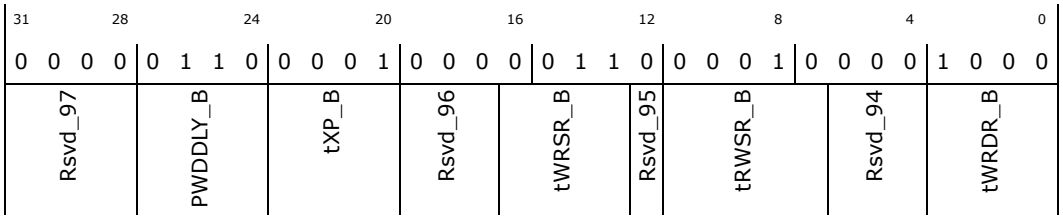
3.1.21 DTR3B—Offset 14h

DRAM Timing Register 3B

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 06106108h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Rsvd_97:** Reserved
27:24	0x6 RW	**PWDDLY_B:** RD/WR command to Power-down delay. Non-JEDEC delay for performance enhancement. Delay = PWDDLY x 4 DRAM Clocks.
23:20	0x1 RW	**tXP_B:** Delay from CKE asserted high to any DRAM command 0h - 2 DRAM Clocks (DDR3-800). 1h - 3 DRAM Clocks (DDR3-1066, 1333) 2h - 4 DRAM Clocks (DDR3-1600). 3h - 5 DRAM Clocks 4h - 6 DRAM Clocks 5h - 7 DRAM Clocks 6h - 8 DRAM Clocks 7h - 9 DRAM Clocks.
19:17	0x0 RO	**Rsvd_96:** Reserved
16:13	0x3 RW	**tWRSR_B:** Write to Read same rank command delay. Should be set to 4 + tWCL + tWTR 0h - 11 DRAM Clocks (LPDDR2-800). 1h - 12 DRAM Clocks. 2h - 13 DRAM Clocks (DDR3-800,LPDDR2-1066). 3h - 14 DRAM Clocks (DDR3-1066,LPDDR3-1333). 4h - 15 DRAM Clocks. 5h - 16 DRAM Clocks (DDR3-1333). 6h - 17 DRAM Clocks. 7h - 18 DRAM Clocks (DDR3-1600). 8h - 19 DRAM Clocks. 9h - 20 DRAM Clocks. Others - Reserved
12	0x0 RO	**Rsvd_95:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
11:7	0x2 RW	**tRWSR_B:** Read to Write same rank command delay. Should be set to tCL - tWCL + 6 + board delay if needed. 0h - 6 DRAM Clocks. 1h - 7 DRAM Clocks. 2h - 8 DRAM Clocks. 3h - 9 DRAM Clocks. 4h - 10 DRAM Clocks. 5h - 11 DRAM Clocks. 6h - 12 DRAM Clocks. 7h - 13 DRAM Clocks. 8h - 14 DRAM Clocks. 9h - 15 DRAM Clocks. Ah - 16 DRAM Clocks. Bh - 17 DRAM Clocks. Others - Reserved
6:4	0x0 RO	**Rsvd_94:** Reserved
3:0	0x8 RW	**tWRDR_B:** Write to Read DQ delay, different ranks, same DIMM 0h - Reserved 1h - 4 DRAM Clocks. 2h - 5 DRAM Clocks. 3h - 6 DRAM Clocks. 4h - 7 DRAM Clocks. 5h - 8 DRAM Clocks. 6h - 9 DRAM Clocks. 7h - 10 DRAM Clocks.

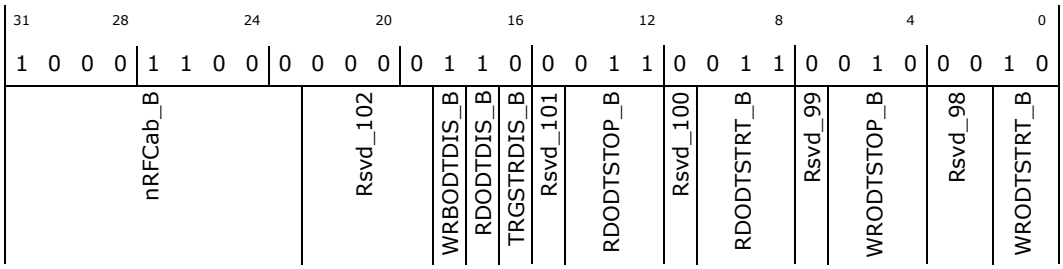
3.1.22 DTR4B—Offset 15h

DRAM Timing Register 4B

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 8C063322h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x118 RW	**nRFCab_B:** The number of DRAM clocks used to define tRFC for DDR3, tRFCab for LPDDR2/3
22:19	0x0 RO	**Rsvd_102:** Reserved
18	0x1 RW	**WRBODTDIS_B:** Disable Write ODT on non-targeted DIMM. When writing to DIMM A, ODT is asserted to the target rank of DIMM A and also to the low rank of DIMM B. This defeature bit is used to disable ODT assertion to the opposite DIMM during write.
17	0x1 RW	**RDODTDIS_B:** Disable Read ODT. When reading from DIMM A, ODT is asserted to the low rank of DIMM B. This defeature bit is used to disable ODT assertion during reads.
16	0x0 RW	**TRGSTRDIS_B:** Write target rank is not stretched. When set, stretched ODT as defined above is not applied to the write target rank and ODT command is asserted for 6 DRAM clocks. Should not be used when ODT is pulled-in.

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**Rsvd_101:** Reserved
14:12	0x3 RW	**RDODTSTOP_B:** Read command to ODT de-assert delay Value should be set to: RDODTSTRT+6+(WRODTSTOP-WRODTSTRT) 0h - 6 DRAM Clocks. 1h - 7 DRAM Clocks. 2h - 8 DRAM Clocks. 3h - 9 DRAM Clocks. 4h - 10 DRAM Clocks. 5h - 11 DRAM Clocks. 6h - 12 DRAM Clocks. 7h - 13 DRAM Clocks. Other - Reserved.
11	0x0 RO	**Rsvd_100:** Reserved
10:8	0x3 RW	**RDODTSTRT_B:** Read command to ODT assert delay. Value should be set to tCMD+tCL-tWCL-ODT_PULLIN, where ODT_PULLIN must have the same value as in WRODTSTRT. 0h - 0 DRAM Clocks. 1h - 1 DRAM Clocks. 2h - 2 DRAM Clocks. 3h - 3 DRAM Clocks. 4h - 4 DRAM Clocks. 5h - 5 DRAM Clocks. Other - Reserved.
7	0x0 RO	**Rsvd_99:** Reserved
6:4	0x2 RW	**WRODTSTOP_B:** Write command to ODT de-assert delay. WRODTSTOP 1N 2N 3N 0h WR+6 N/A N/A 1h WR+7 WR+6 N/A 2h WR+8 WR+7 WR+6 3h WR+9 WR+8 WR+7 4h WR+10 WR+9 WR+8 Other Reserved Reserved Reserved
3:2	0x0 RO	**Rsvd_98:** Reserved
1:0	0x2 RW	**WRODTSTRT_B:** WR command to ODT assert delay. JEDEC requires ODT to be asserted on the same clock with the WR command. Dunit allows to pull-in by 1 clock in 2N mode and by 1-2 clocks in 3N mode. For most DIMM configurations, this register should be programmed to same value as tCMD. A value of tCMD - ODT_PULLIN can be used according to the table below which shows the ODT command assertion with respect to the WR command assertion. WRODTSTRT 1N 2N 3N 0h WR WR-1 WR-2 1h N/A WR WR-1 2h N/A N/A WR 3h Reserved Reserved Reserved

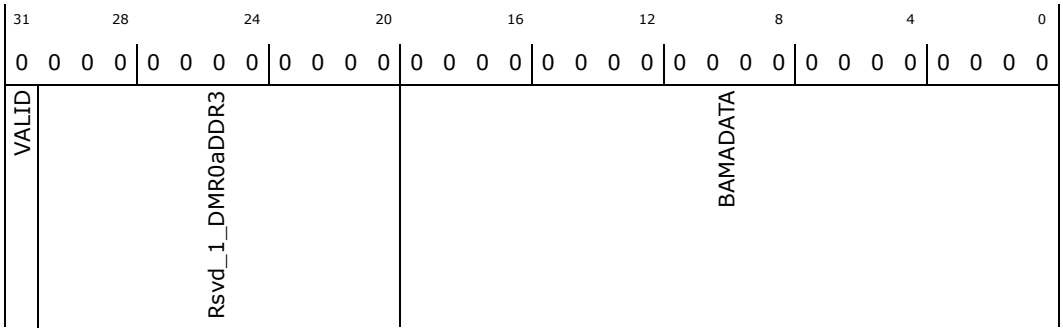
3.1.23 DMR0aDDR3—Offset 16h

DRAM Mode Register Value 0a DDR3

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**VALID:** Entry is Valid
30:20	0x0 RO	**Rsvd_1_DMR0aDDR3:** Reserved
19:0	0x0 RW	**BAMADATA:** Bank Address used to select the DDR3 MR, Value to be written to the DDR3 MR; or Mode Register Address for LPDDR, Value to be written to the LPDDR MR

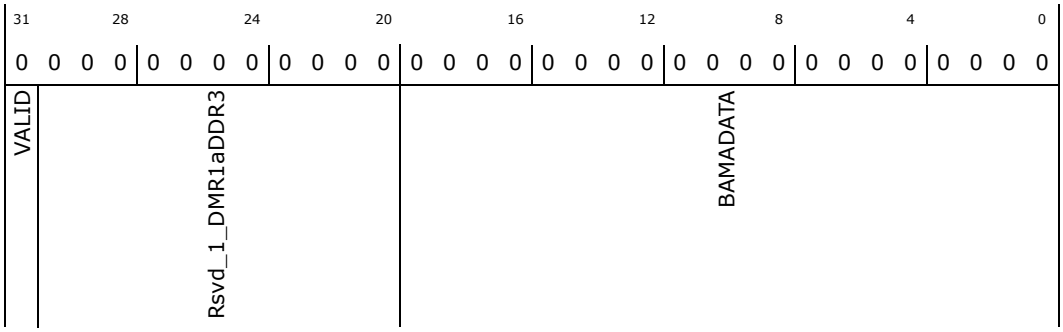
3.1.24 DMR1aDDR3—Offset 17h

DRAM Mode Register Value 1a DDR3

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**VALID:** Entry is Valid
30:20	0x0 RO	**Rsvd_1_DMR1aDDR3:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
19:0	0x0 RW	**BAMADATA:** Bank Address used to select the DDR3 MR, Value to be written to the DDR3 MR; or Mode Register Address for LPDDR, Value to be written to the LPDDR MR

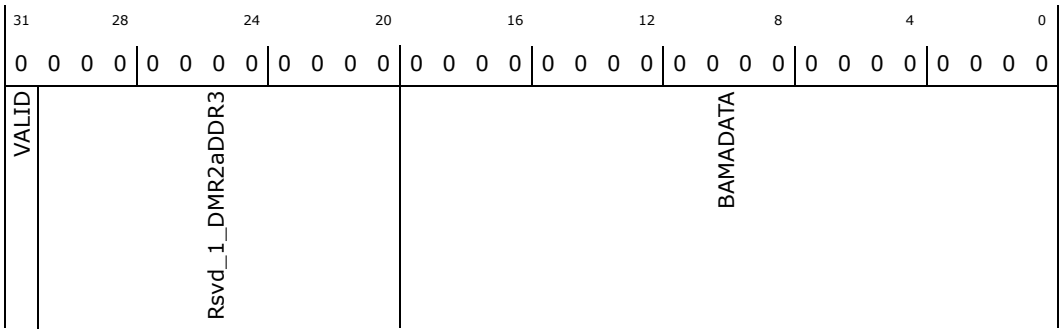
3.1.25 DMR2aDDR3—Offset 18h

DRAM Mode Register Value 2a DDR3

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**VALID:** Entry is Valid
30:20	0x0 RO	**Rsvd_1_DMR2aDDR3:** Reserved
19:0	0x0 RW	**BAMADATA:** Bank Address used to select the DDR3 MR, Value to be written to the DDR3 MR; or Mode Register Address for LPDDR, Value to be written to the LPDDR MR

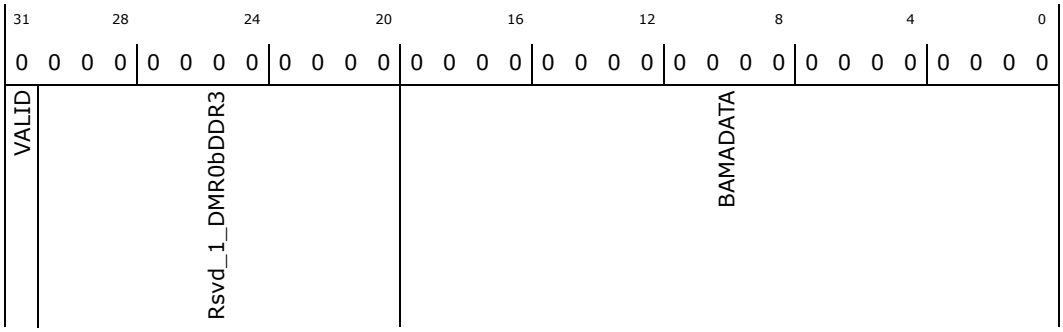
3.1.26 DMR0bDDR3—Offset 1Ah

DRAM Mode Register Value 0b DDR3

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**VALID:** Entry is Valid
30:20	0x0 RO	**Rsvd_1_DMR0bDDR3:** Reserved
19:0	0x0 RW	**BAMADATA:** Bank Address used to select the DDR3 MR, Value to be written to the DDR3 MR; or Mode Register Address for LPDDR, Value to be written to the LPDDR MR

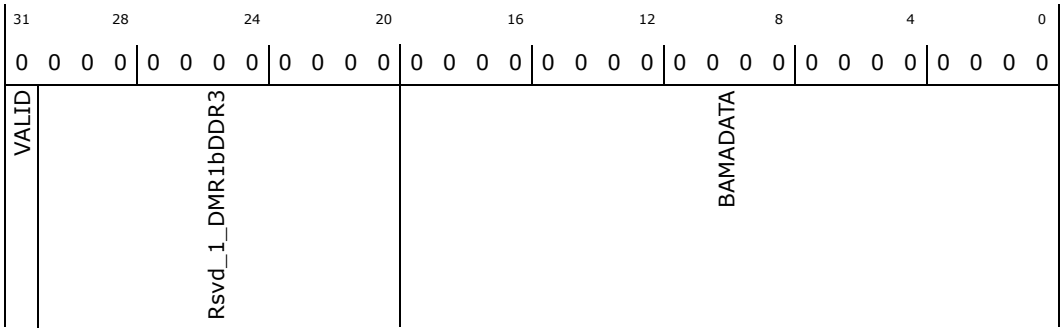
3.1.27 DMR1bDDR3—Offset 1Bh

DRAM Mode Register Value 1b DDR3

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**VALID:** Entry is Valid
30:20	0x0 RO	**Rsvd_1_DMR1bDDR3:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
19:0	0x0 RW	**BAMADATA:** Bank Address used to select the DDR3 MR, Value to be written to the DDR3 MR; or Mode Register Address for LPDDR, Value to be written to the LPDDR MR

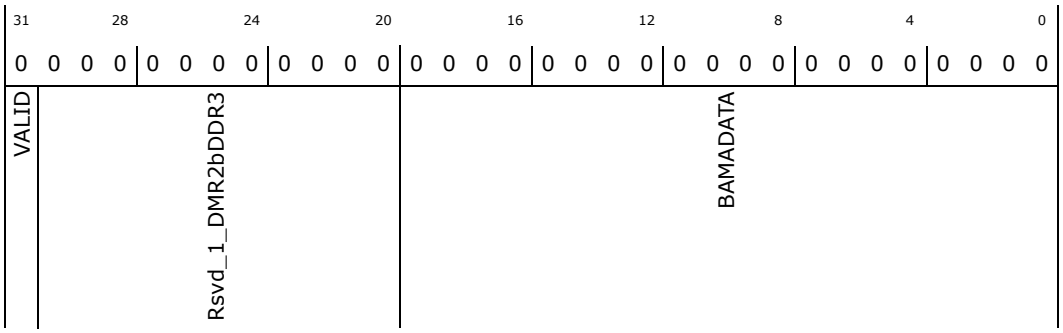
3.1.28 DMR2bDDR3—Offset 1Ch

DRAM Mode Register Value 2b DDR3

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**VALID:** Entry is Valid
30:20	0x0 RO	**Rsvd_1_DMR2bDDR3:** Reserved
19:0	0x0 RW	**BAMADATA:** Bank Address used to select the DDR3 MR, Value to be written to the DDR3 MR; or Mode Register Address for LPDDR, Value to be written to the LPDDR MR

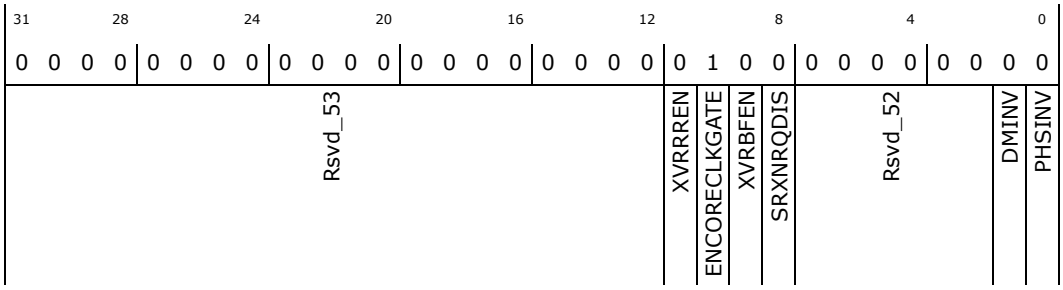
3.1.29 DCBR—Offset 1Fh

DRAM CB Register

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000400h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Rsvd_53:** Reserved
11	0x0 RW	**XVRRREN:** Enable the Crossover Buffer to act as increased Read Return Buffer depth
10	0x1 RW	**ENCORECLKGATE:** Enable Dunit Core Clock Gate During SR
9	0x0 RW	**XVRBFEN:** Enable the Crossover Buffer to act as increased IPReq Queue depth
8	0x0 RW	**SRXNRQDIS:** 0h - Load PMI requests to Dunit in SR Exit tXSDLL and ZQCoper period. 1h - Load PMI requests only after tXSDLL and ZQCoper are complete.
7:2	0x0 RO	**Rsvd_52:** Reserved
1	0x0 RW	**DMINV:** Inverse Data Mask When this bit is set to 1, the Data Mask will be inversed.
0	0x0 RW	**PHSINV:** Core/SPID CDC phase control invert. Backup inverter for internal phase indicator in Dunit.

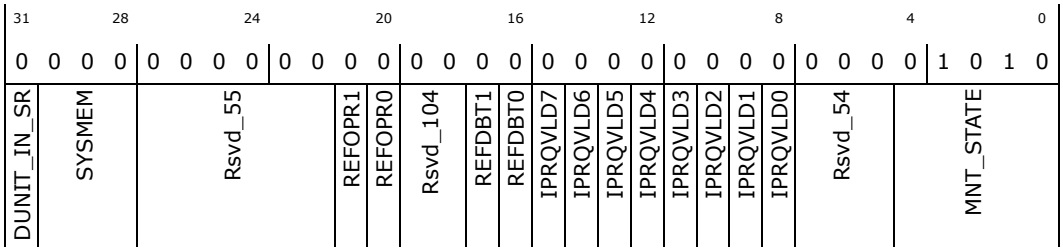
3.1.30 DSTAT—Offset 20h

Dunit Status

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 0000000Ah



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**DUNIT_IN_SR:** Dunit is in self-refresh
30:28	0x0 RO	**SYSMEM:** Reflects the Dunit Memory Depth Configuration
27:22	0x0 RO	**Rsvd_55:** Reserved
21	0x0 RO	**REFOPR1:** Rank 1 Refresh Dept is greater than DRFC.REFWMLO
20	0x0 RO	**REFOPR0:** Rank 0 Refresh Dept is greater than DRFC.REFWMLO
19:18	0x0 RO	**Rsvd_104:** Reserved
17	0x0 RO	**REFDBT1:** Rank 1 has a Refresh Dept
16	0x0 RO	**REFDBT0:** Rank 0 has a Refresh Dept
15	0x0 RO	**IPRQVLD7:** IPREQ Entry 7 contains a valid request.
14	0x0 RO	**IPRQVLD6:** IPREQ Entry 6 contains a valid request.
13	0x0 RO	**IPRQVLD5:** IPREQ Entry 5 contains a valid request.
12	0x0 RO	**IPRQVLD4:** IPREQ Entry 4 contains a valid request.
11	0x0 RO	**IPRQVLD3:** IPREQ Entry 3 contains a valid request.
10	0x0 RO	**IPRQVLD2:** IPREQ Entry 2 contains a valid request.
9	0x0 RO	**IPRQVLD1:** IPREQ Entry 1 contains a valid request.
8	0x0 RO	**IPRQVLD0:** IPREQ Entry 0 contains a valid request.
7:5	0x0 RO	**Rsvd_54:** Reserved
4:0	0xa RO	**MNT_STATE:** Dunit Maintenance Internal State

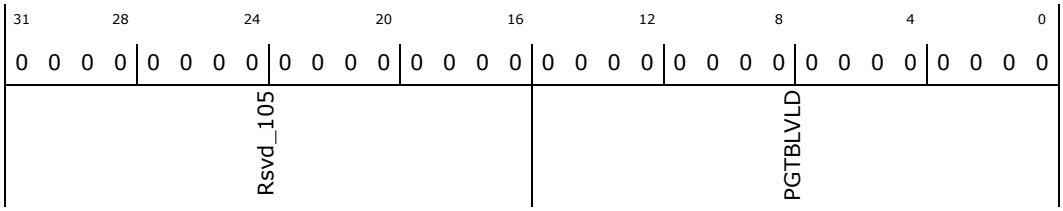
3.1.31 PGTBL—Offset 21h

DRAM Page Table Status

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd_105:** Reserved
15:0	0x0 RO	**PGTBLVLD:** Reflects the open page table entries (2 Ranks x 8 Banks)

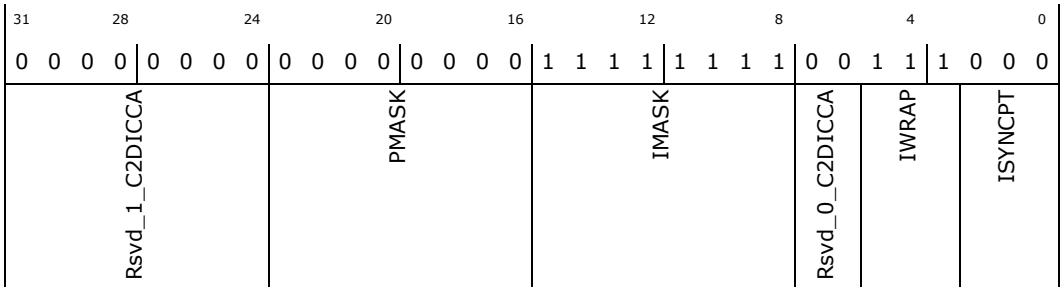
3.1.32 C2DICCA—Offset 30h

CZ to DDR Freq A Initiator Crossover Control

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 0000FF38h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Rsvd_1_C2DICCA:** Reserved
23:16	0x0 RW/P	**PMASK:** Initiator Phase Shift Enable Mask for Crossover.
15:8	0xff RW/P	**IMASK:** Initiator Flop Enable Mask for Crossover.
7:6	0x0 RO	**Rsvd_0_C2DICCA:** Reserved
5:3	0x7 RW/P	**IWRAP:** Wrap Position for Initiator Clock Crossover Counter.
2:0	0x0 RW/P	**ISYNCPT:** Crossover Counter Starting Point from Initiator Clock Sync Pulse.

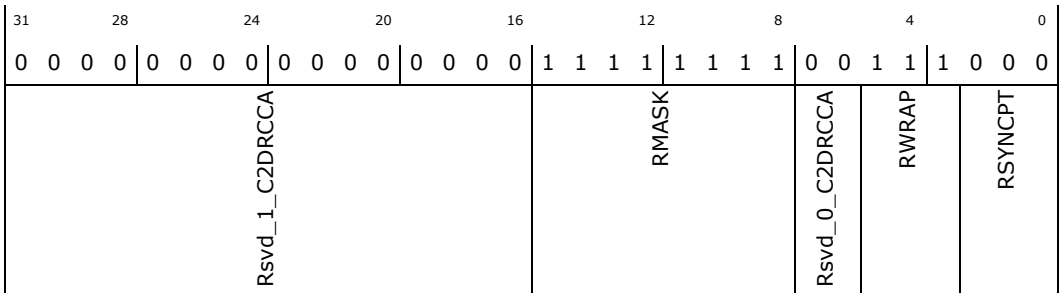
3.1.33 C2DRCCA—Offset 31h

CZ to DDR Freq A Receiver Crossover Control

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 0000FF38h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd_1_C2DRCCA:** Reserved
15:8	0xff RW/P	**RMASK:** Receiver Flop Enable Mask for Crossover.
7:6	0x0 RO	**Rsvd_0_C2DRCCA:** Reserved
5:3	0x7 RW/P	**RWRAP:** Wrap Position for Receiver Clock Crossover Counter.
2:0	0x0 RW/P	**RSYNCPT:** Crossover Counter Starting Point from Receiver Clock Sync Pulse.

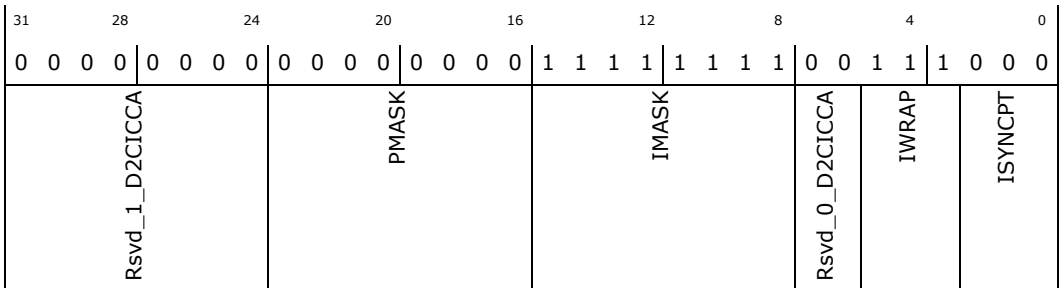
3.1.34 D2CICCA—Offset 32h

DDR to CZ Freq A Initiator Crossover Control

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 0000FF38h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Rsvd_1_D2CICCA:** Reserved
23:16	0x0 RW/P	**PMASK:** Initiator Phase Shift Enable Mask for Crossover.
15:8	0xff RW/P	**IMASK:** Initiator Flop Enable Mask for Crossover.
7:6	0x0 RO	**Rsvd_0_D2CICCA:** Reserved
5:3	0x7 RW/P	**IWRAP:** Wrap Position for Initiator Clock Crossover Counter.
2:0	0x0 RW/P	**ISYNCPT:** Crossover Counter Starting Point from Initiator Clock Sync Pulse.

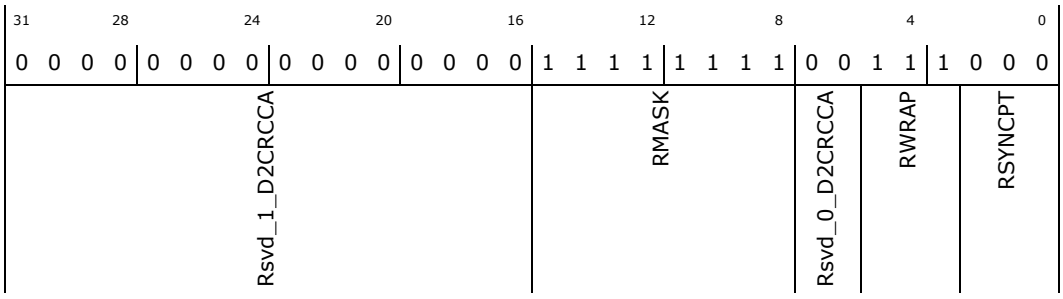
3.1.35 D2CRCCA—Offset 33h

DDR to CZ Freq A Receiver Crossover Control

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 0000FF38h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd_1_D2CRCCA:** Reserved
15:8	0xff RW/P	**RMASK:** Receiver Flop Enable Mask for Crossover.
7:6	0x0 RO	**Rsvd_0_D2CRCCA:** Reserved
5:3	0x7 RW/P	**RWRAP:** Wrap Position for Receiver Clock Crossover Counter.
2:0	0x0 RW/P	**RSYNCPT:** Crossover Counter Starting Point from Receiver Clock Sync Pulse.

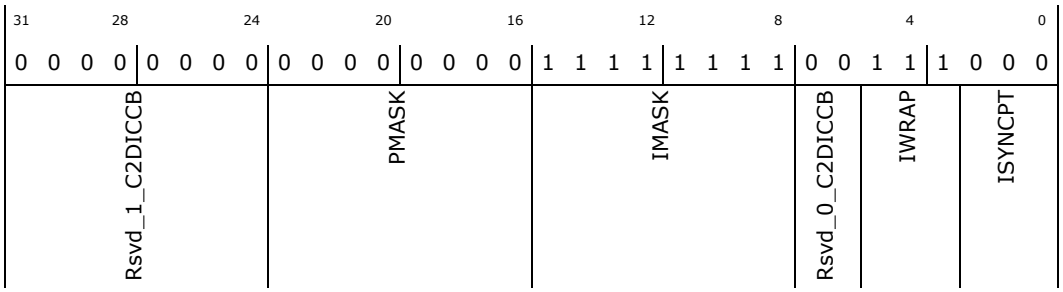
3.1.36 C2DICCB—Offset 38h

CZ to DDR Freq B Initiator Crossover Control

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 0000FF38h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Rsvd_1_C2DICCB:** Reserved
23:16	0x0 RW/P	**PMASK:** Initiator Phase Shift Enable Mask for Crossover.
15:8	0xff RW/P	**IMASK:** Initiator Flop Enable Mask for Crossover.
7:6	0x0 RO	**Rsvd_0_C2DICCB:** Reserved
5:3	0x7 RW/P	**IWRAP:** Wrap Position for Initiator Clock Crossover Counter.
2:0	0x0 RW/P	**ISYNCPT:** Crossover Counter Starting Point from Initiator Clock Sync Pulse.

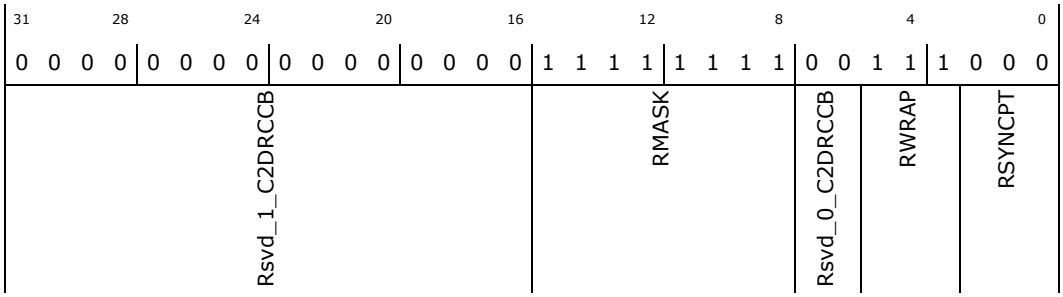
3.1.37 C2DRCCB—Offset 39h

CZ to DDR Freq B Receiver Crossover Control

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 0000FF38h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd_1_C2DRCCB:** Reserved
15:8	0xff RW/P	**RMASK:** Receiver Flop Enable Mask for Crossover.
7:6	0x0 RO	**Rsvd_0_C2DRCCB:** Reserved
5:3	0x7 RW/P	**RWRAP:** Wrap Position for Receiver Clock Crossover Counter.
2:0	0x0 RW/P	**RSYNCPT:** Crossover Counter Starting Point from Receiver Clock Sync Pulse.

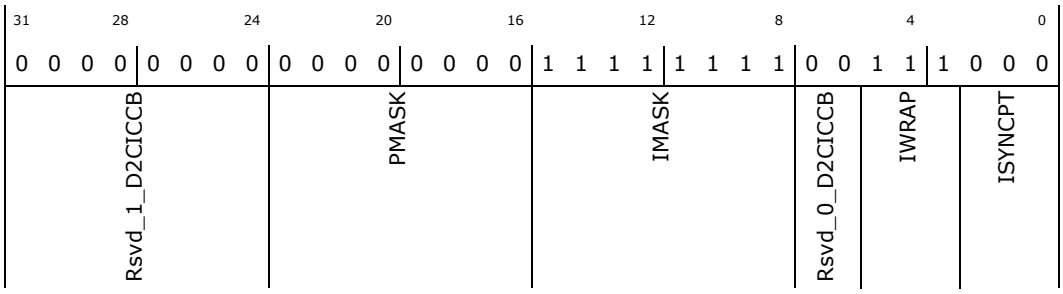
3.1.38 D2CICCB—Offset 3Ah

DDR to CZ Freq B Initiator Crossover Control

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 0000FF38h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Rsvd_1_D2CICCB:** Reserved
23:16	0x0 RW/P	**PMASK:** Initiator Phase Shift Enable Mask for Crossover.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0xff RW/P	**IMASK:** Initiator Flop Enable Mask for Crossover.
7:6	0x0 RO	**Rsvd_0_D2CICCB:** Reserved
5:3	0x7 RW/P	**IWRAP:** Wrap Position for Initiator Clock Crossover Counter.
2:0	0x0 RW/P	**ISYNCPT:** Crossover Counter Starting Point from Initiator Clock Sync Pulse.

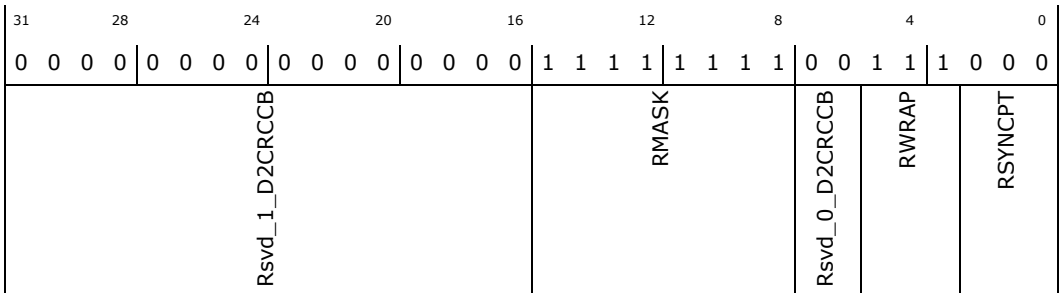
3.1.39 D2CRCCB—Offset 3Bh

DDR to CZ Freq B Receiver Crossover Control

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 0000FF38h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd_1_D2CRCCB:** Reserved
15:8	0xff RW/P	**RMASK:** Receiver Flop Enable Mask for Crossover.
7:6	0x0 RO	**Rsvd_0_D2CRCCB:** Reserved
5:3	0x7 RW/P	**RWRAP:** Wrap Position for Receiver Clock Crossover Counter.
2:0	0x0 RW/P	**RSYNCPT:** Crossover Counter Starting Point from Receiver Clock Sync Pulse.

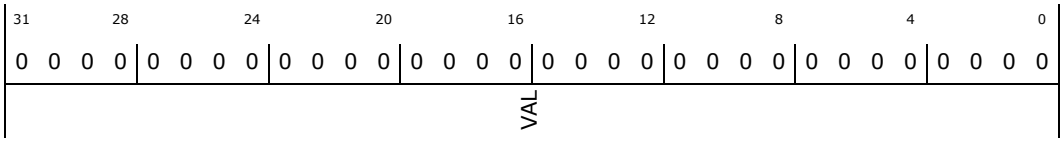
3.1.40 SSKPD0—Offset 4Ah

Sticky Scratchpad 0

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/P	**VAL:** General Purpose Scratchpad. May be used for BIOS for data storage. Value is preserved in warm-reset.

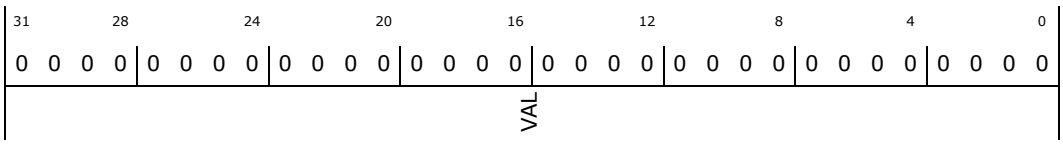
3.1.41 SSKPD1—Offset 4Bh

Sticky Scratchpad 1

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/P	**VAL:** General Purpose Scratchpad. May be used for BIOS for data storage. Value is preserved in warm-reset.

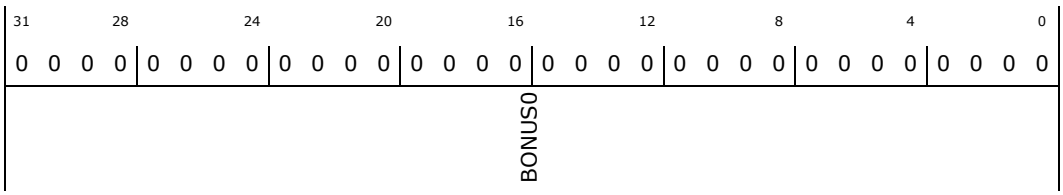
3.1.42 BONUS0—Offset 50h

Bonus Register 0

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**BONUS0:** Bonus Register 0 (This register is reserved for ECO).

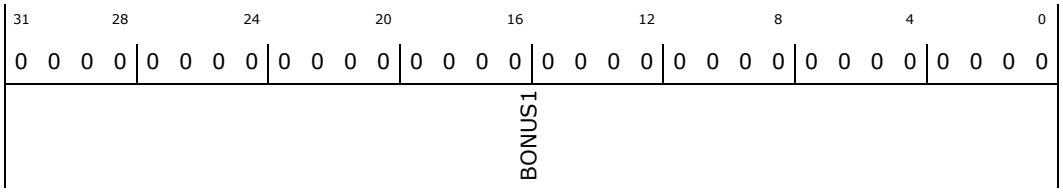
3.1.43 BONUS1—Offset 51h

Bonus Register 1

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**BONUS1:** Bonus Register 1 (This register is reserved for ECO).

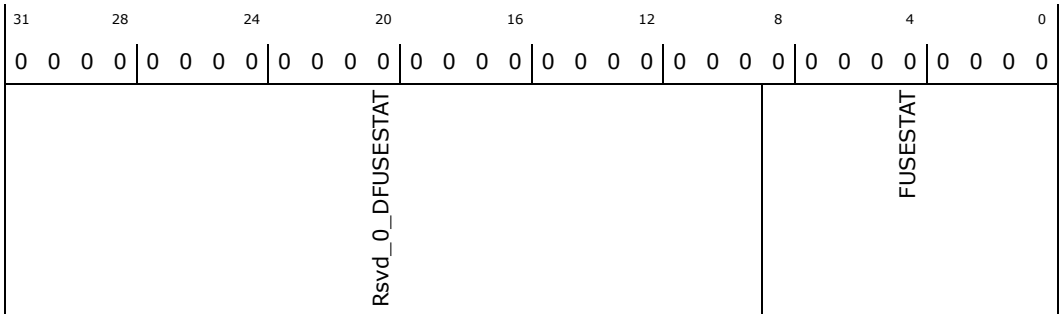
3.1.44 DFUSESTAT—Offset 70h

Dunit fuse status register

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**Rsvd_0_DFUSESTAT:** Reserved
8:0	0x0 RO	**FUSESTAT:** Dunit fuse bits are captured into this register and is available for read [0] fus_dun_ecc_dis. [3:1] fus_dun_max_supporte_memory[2:0]. [4] fus_dun_ddr3_dis. [5] fus_dun_lpddr_dis. [6] fud_dun_ch0_dis. [7] fus_dun_ch1_dis. [8] fus_dun_32bit_dram_ifc.

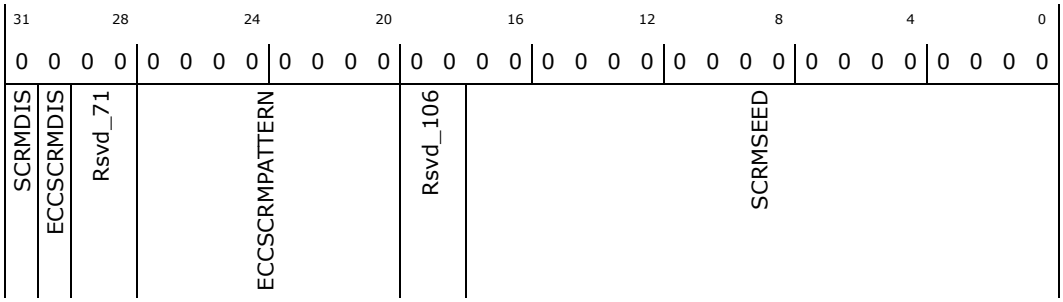
3.1.45 DSCRMSEED—Offset 80h

Dynamic data scrambler seed register

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SCRMDIS:** Disable scrambler.
30	0x0 RW	**ECCSCRMDIS:** Disable scrambler for ECC.
29:28	0x0 RO	**Rsvd_71:** Reserved
27:20	0x0 RW	**ECCSCRMPATTERN:** Holds 8 bit ecc scrambler pattern value used to XOR with LFSR array output.
19:18	0x0 RO	**Rsvd_106:** Reserved
17:0	0x0 RW	**SCRMSEED:** Holds 18 bit scrambler seed value used to feed into LFSR array matrix.

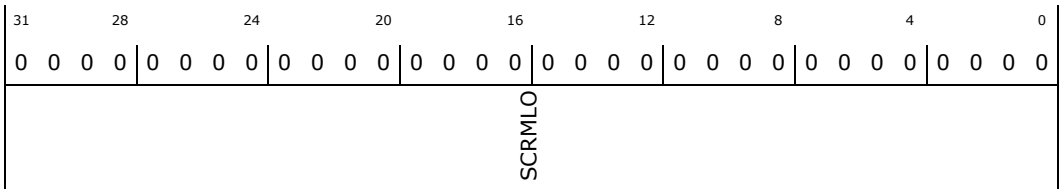
3.1.46 DSCRMLO—Offset 81h

Dynamic data scrambler pattern low register.

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SCRMLO:** Holds 31:0 bits of scrambler parrem value used to XOR with LFSR array output.

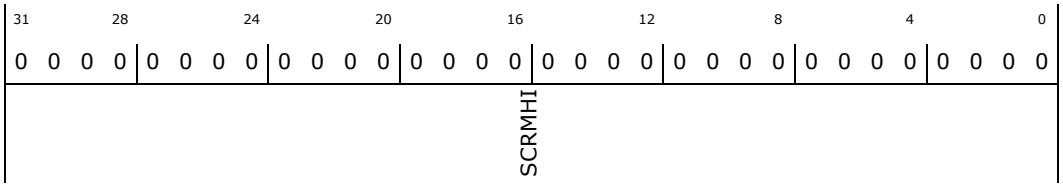
3.1.47 DSCRMHI—Offset 82h

Dynamic data scrambler pattern high register.

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SCRMHI:** Holds 63:32 bits of scrambler parrem value used to XOR with LFSR array output.

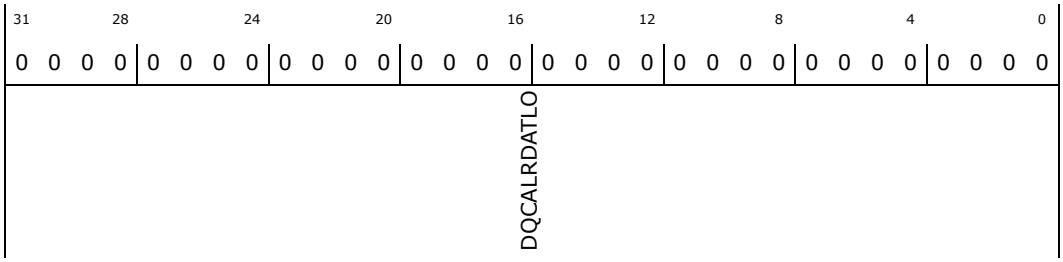
3.1.48 DQCALRDATLO—Offset 83h

DQ Calibration Read Return Low

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**DQCALRDATLO:** DQ Calibration Read Return Low

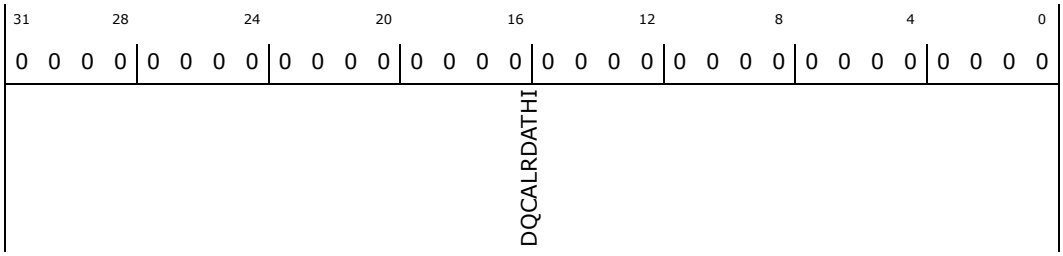
3.1.49 DQCALRDATHI—Offset 84h

DQ Calibration Read Return High

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**DQCALRDATHI:** DQ Calibration Read Return High

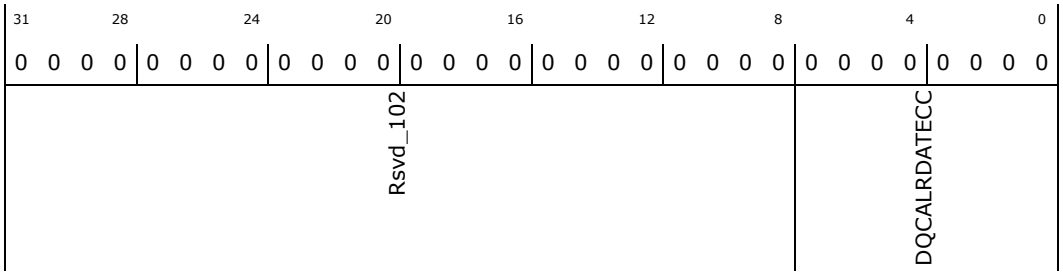
3.1.50 DQCALRDATECC—Offset 85h

DQ Calibration Read Return ECC

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Rsvd_103 (Rsvd_102):** Reserved
7:0	0x0 RO	**DQCALRDATECC:** DQ Calibration Read Return ECC

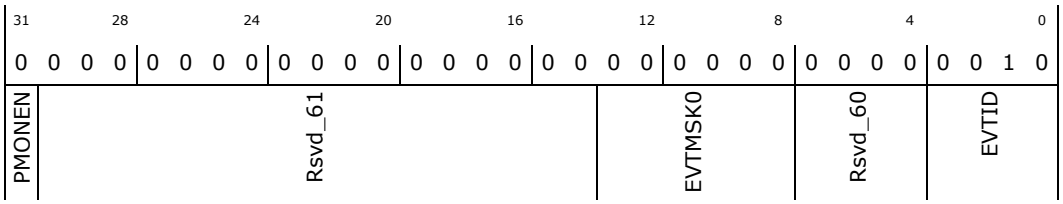
3.1.51 PMSEL0—Offset E0h

Performance Monitor Event Select 0

Access Method

Type: ??? Register
(Size: 32 bits)

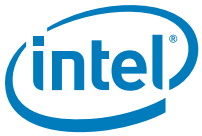
Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**PMONEN:** Dunit Perfmon Enable. 0 Dunit perfmon is disabled. 1 Dunit perfmon is enabled.
30:14	0x0 RO	**Rsvd_61:** Reserved
13:8	0x0 RW	**EVTMSK0:** Event Mask
7:4	0x0 RO	**Rsvd_60:** Reserved
3:0	0x2 RW	**EVTID:** Event ID

3.1.52 PMSEL1—Offset E1h

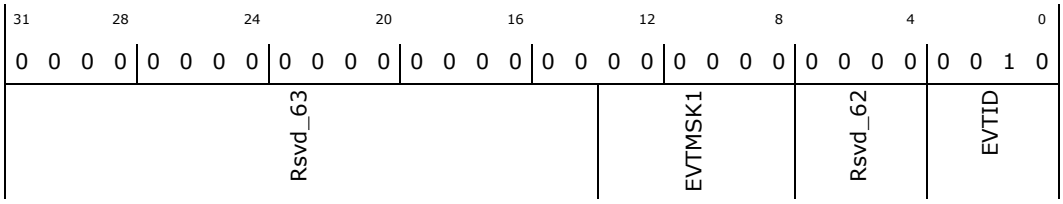
Performance Monitor Event Select 1



Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**Rsvd_63:** Reserved
13:8	0x0 RW	**EVTMSK1:** Event Mask
7:4	0x0 RO	**Rsvd_62:** Reserved
3:0	0x2 RW	**EVTID:** Event ID

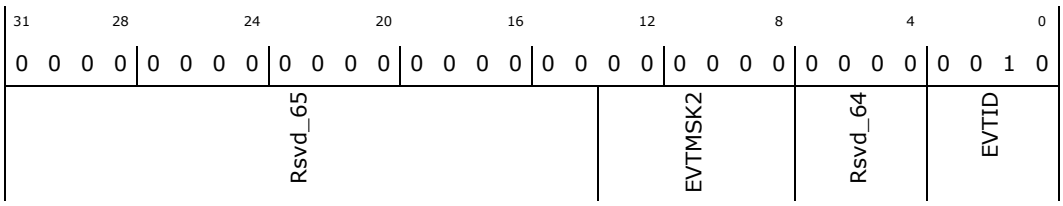
3.1.53 PMSEL2—Offset E2h

Performance Monitor Event Select 2

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**Rsvd_65:** Reserved
13:8	0x0 RW	**EVTMSK2:** Event Mask
7:4	0x0 RO	**Rsvd_64:** Reserved
3:0	0x2 RW	**EVTID:** Event ID

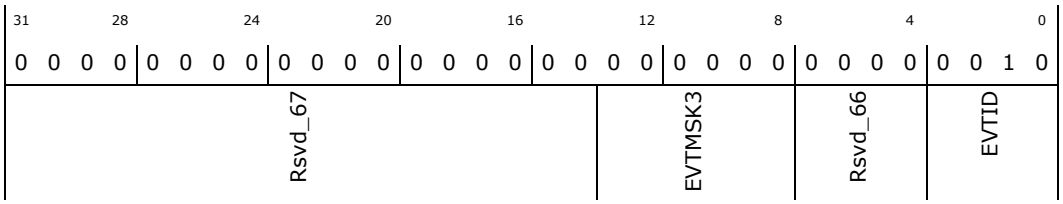
3.1.54 PMSEL3—Offset E3h

Performance Monitor Event Select 3

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**Rsvd_67:** Reserved
13:8	0x0 RW	**EVTMSK3:** Event Mask
7:4	0x0 RO	**Rsvd_66:** Reserved
3:0	0x2 RW	**EVTID:** Event ID

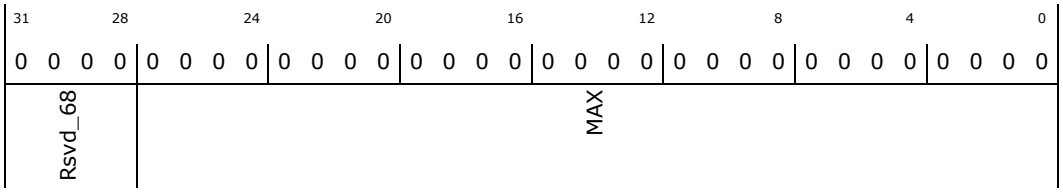
3.1.55 PMAUXMAX—Offset E8h

Performance Monitor Address Limit High

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Rsvd_68:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
27:0	0x0 RW	**MAX:** Maximal address or maximal latency count. When PMSEL0.EVTID == Ch, this register should be initialized to 0h and at the end of the test bits [11:0] will contain the max latency. When PMSEL0/1/2.EVTID == 5h, this register should be initialized to the highest address the Perfmon test will cover. Bits [27:0] of this register correspond to the physical address bits [35:8].

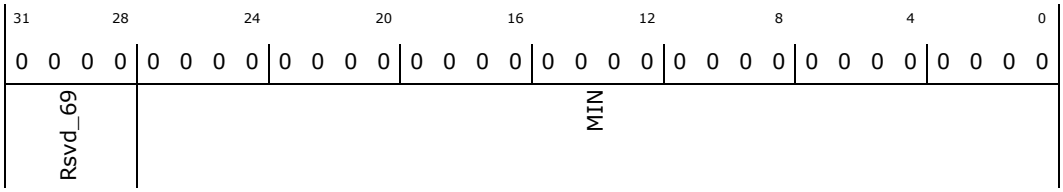
3.1.56 PMAUXMIN—Offset E9h

Performance Monitor Address Limit Low

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Rsvd_69:** Reserved
27:0	0x0 RW	**MIN:** Minimal address or minimal latency count. When PMSEL0.EVTID == Ch, this register should be initialized to FFFh and at the end of the test bits [11:0] will contain the min latency. When PMSEL0/1/2.EVTID == 5h, this register should be initialized to the lowest address the Perfmon test will cover. Bits [27:0] of this register correspond to the physical address bits [35:8].

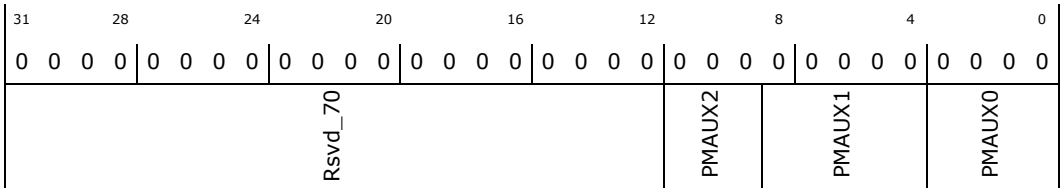
3.1.57 PMAUX—Offset EAh

Performance Monitor Aux

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Rsvd_70:** Reserved
11:9	0x0 RW	**PMAUX2:** Additional mask and configuration. Refer Perfmon Guide.
8:4	0x0 RW	**PMAUX1:** Additional mask and configuration. Refer Perfmon Guide.
3:0	0x0 RW	**PMAUX0:** Additional mask and configuration. Refer Perfmon Guide.

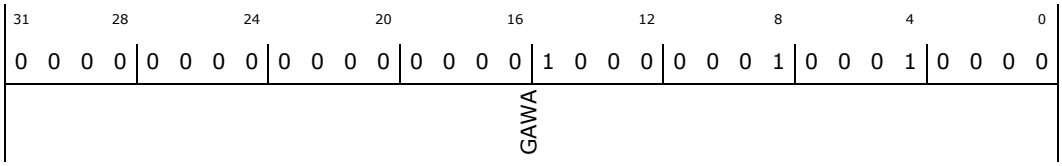
3.1.58 SWACA—Offset F0h

SAI Write Access Control - Group A

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00008110h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x8110 RW	**GAWA:** Group A Write Access

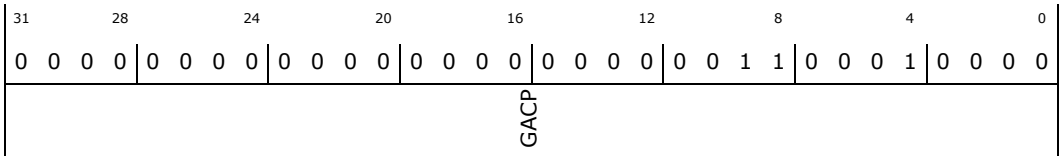
3.1.59 SCPA—Offset F1h

SAI Control Policy - Group A

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000310h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x310 RW	**GACP:** Group A Control Policy

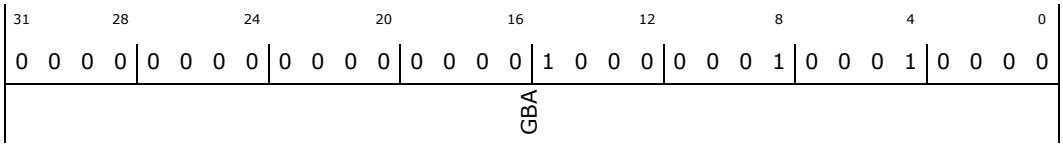
3.1.60 SACB—Offset F4h

SAI Access Control - Group B

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00008110h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x8110 RW	**GBA:** Group B Access

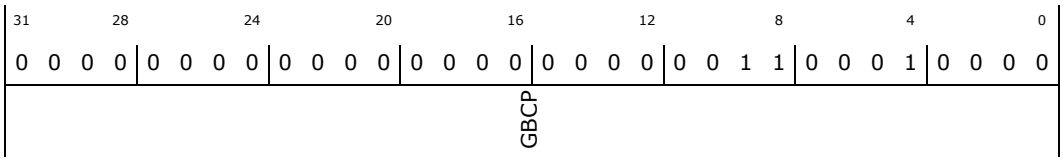
3.1.61 SCPB—Offset F5h

SAI Control Policy - Group B

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000310h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x310 RW	**GBCP:** Group B Control Policy

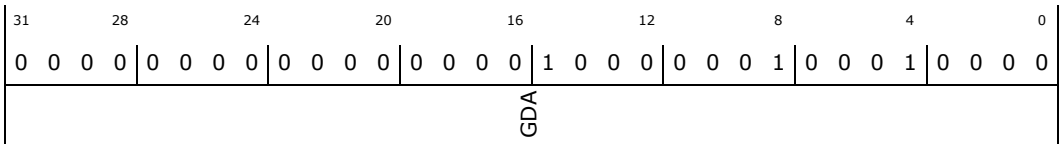
3.1.62 SACD—Offset F8h

SAI Access Control - Group D

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00008110h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x8110 RW	**GDA:** Group D Access

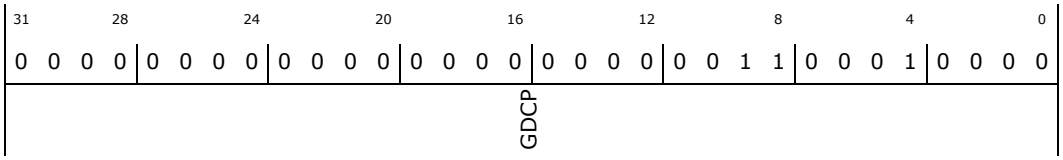
3.1.63 SCPD—Offset F9h

SAI Control Policy - Group D

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00000310h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x310 RW	**GDCP:** Group D Control Policy

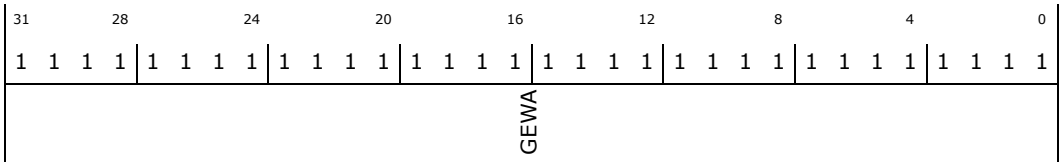
3.1.64 SWACE—Offset FCh

SAI Write Access Control - Group E

Access Method

Type: ??? Register
(Size: 32 bits)

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**GEWA:** Group E Write Access

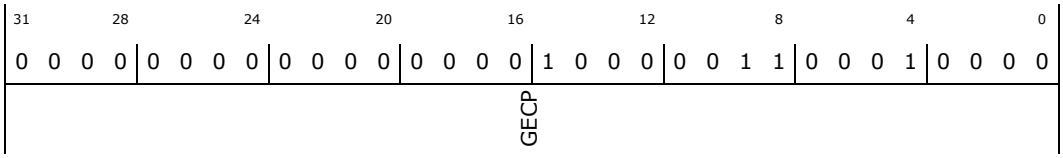
3.1.65 SCPE—Offset FDh

SAI Control Policy - Group E

Access Method

Type: ??? Register
(Size: 32 bits)

Default: 00008310h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x8310 RW	**GECP:** Group E Control Policy

4 Graphics Video Display

4.1 Graphics, Video and Display PCI Configuration Registers

Table 21. Summary of Graphics, Video and Display PCI Configuration Registers—0/2/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"DID—Offset 0h" on page 79	22B08086h
4–7h	4	"PCICMD_STS—Offset 4h" on page 79	00100000h
8–Bh	4	"RID_CC—Offset 8h" on page 80	00000000h
C–Fh	4	"HDR—Offset Ch" on page 81	00000000h
10–13h	4	"GTTMMADR_LSB—Offset 10h" on page 82	00000004h
14–17h	4	"GTTMMADR_MSB—Offset 14h" on page 83	00000000h
18–1Bh	4	"GMADR_LSB—Offset 18h" on page 84	0000000Ch
1C–1Fh	4	"GMADR_MSB—Offset 1Ch" on page 85	00000000h
20–23h	4	"IOBAR—Offset 20h" on page 85	00000001h
2C–2Fh	4	"SSID_SID—Offset 2Ch" on page 86	00000000h
34–37h	4	"CAPPOINT—Offset 34h" on page 87	000000D0h
3C–3Fh	4	"INTRLINE—Offset 3Ch" on page 87	00000100h
50–53h	4	"GGC—Offset 50h" on page 88	00000028h
5C–5Fh	4	"BDSM—Offset 5Ch" on page 89	00000000h
60–63h	4	"MSAC—Offset 60h" on page 90	00010000h
70–73h	4	"BGSM—Offset 70h" on page 92	00000000h
90–93h	4	"MSI_CAPID_MC—Offset 90h" on page 92	0000B005h
94–97h	4	"MA—Offset 94h" on page 93	00000000h
98–9Bh	4	"MD—Offset 98h" on page 94	00000000h
A4–A7h	4	"Advanced Features Length and Capabilities (AFLC)—Offset A4h" on page 94	03060013h
A8–ABh	4	"AFCTLSTS—Offset A8h" on page 95	00000000h
B0–B3h	4	"VCID—Offset B0h" on page 96	01070009h
B4–B7h	4	"VCID—Offset B0h" on page 96	00000000h
C4–C7h	4	"FD—Offset C4h" on page 97	00000000h
D0–D3h	4	"PMCAPID—Offset D0h" on page 98	00229001h
D4–D7h	4	"PMCS—Offset D4h" on page 99	00000000h
E0–E3h	4	"SWSMISCI—Offset E0h" on page 100	00000000h
E4–E7h	4	"ASLE—Offset E4h" on page 101	00000000h
FC–FFh	4	"ASLS—Offset FCh" on page 102	00000000h

4.1.1 DID—Offset 0h

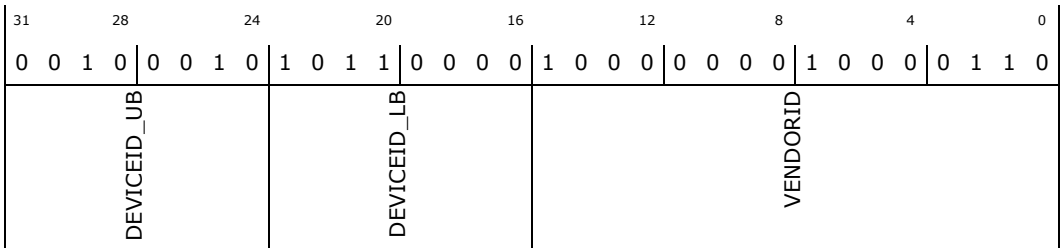
D2: PCI Device ID and Vendor ID Register

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: 0h

Default: 22B08086h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x22 RW	**DEVICEID_UB:** DID_MSB: Identifier assigned to the dev2 PCI.Punit will update this bitfield before handing control to BIOS.
23:16	0xb0 RO	**DEVICEID_LB:** DID_LSB: Identifier assigned to the dev2 PCI.This bitfield is updated from metal straps.SoC allocated values :0xB0,0xB1,0xB2,0xB3.
15:0	0x8086 RO	**VENDORID:** VID: PCI standard identification for Intel

4.1.2 PCICMD_STS—Offset 4h

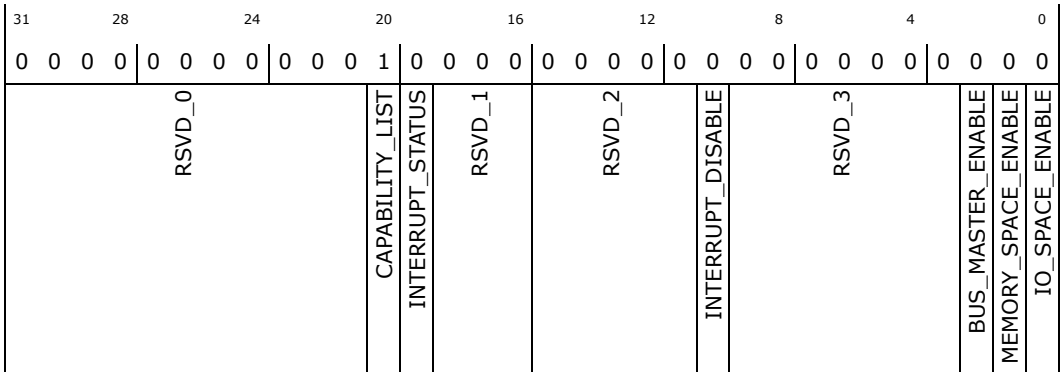
04h: PCI Command Register. 06h: PCI Status Register

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RO	**RESERVED (RSVD_0):** Reserved
20	0x1 RO	**CAPABILITY_LIST:** CAP: Indicates that the CAPPOINT register at 34h provides an offset into PCI Configuration Space containing a pointer to the location of the first item in the list
19	0x0 RO	**INTERRUPT_STATUS:** IS: Reflects the state of the interrupt in the graphics device. 1 : Determined by IIR and IER memory interface registers. Indicates a device 2 (Display/Media/Render) interrupt request.0 : No interrupt pending.Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the assert_IntX message be sent.
18:16	0x0 RO	**RESERVED (RSVD_1):** Reserved
15:11	0x0 RO	**RESERVED (RSVD_2):** Reserved
10	0x0 RW	**INTERRUPT_DISABLE:** ID: 0 : Legacy interrupt message is enabled.1 : Disables legacy interrupt message generation on IOSF Sideband. Note : The interrupt status is not blocked from being reflected in PCISTS.IS.Note: MSI interrupt generation : (PCISTS.IS and PCICMD.BME and MSI_CAPID.MSIE) changes from 0 to 1.Note: Message bus interrupt assert is sent : (PCISTS.IS and ~PCICMD.ID and ~MSI_CAPID.MSIE) changes from 0 to 1.Note: Message bus interrupt de-assert is sent : (PCISTS.IS and ~PCICMD.ID and ~MSI_CAPID.MSIE) changes from 1 to 0.
9:3	0x0 RO	**RESERVED (RSVD_3):** Reserved
2	0x0 RW	**BUS_MASTER_ENABLE:** BME: (BME and MAE are observed. But context save/restore can occur.)0 : Blocks the sending of MSI interrupts.1 : Permits the sending of MSI interrupts
1	0x0 RW	**MEMORY_SPACE_ENABLE:** MSE:0 : Memory space disabled. MEMRD or MEMWR commands will be disabled.1 : Memory space is enabled. A MemRd or MemWr compare hit (with GTTMMADR, GMADR) will be claimed. Care should be taken in setting up GTTMMADR and GMADR that more than 1 match is not made as this will result in unpredictable behavior. Three compares will occur :a. Address[35:20] is compared with GTTMMADR[35:20]. b. Address[35:31,30,29,28,or 27] is compared with GMADR[35:31,30,29,28,or 27],respectively. (Whether the comparison is 35:31, 35:30, 35:29, 35:28 or 35:27 depends on the value of MSAC[20:16].).
0	0x0 RW	**IO_SPACE_ENABLE:** IOSE: 0 : I/O space is disabled. IORD and IOWr cycles will not be claimed.1 : I/O space is enabled. Gfx_IOBAR is checked. If an IORD/IOWR matches (GFX_IOBAR), the cycle will beclaimed. Care should be taken in setting up GFX_IOBAR that more than 1match is not made as this will result in unpredictable behavior. Gfx_IOBAR : Address[15:3] is compared to GFX_IOBAR[15:3].

4.1.3 RID_CC—Offset 8h

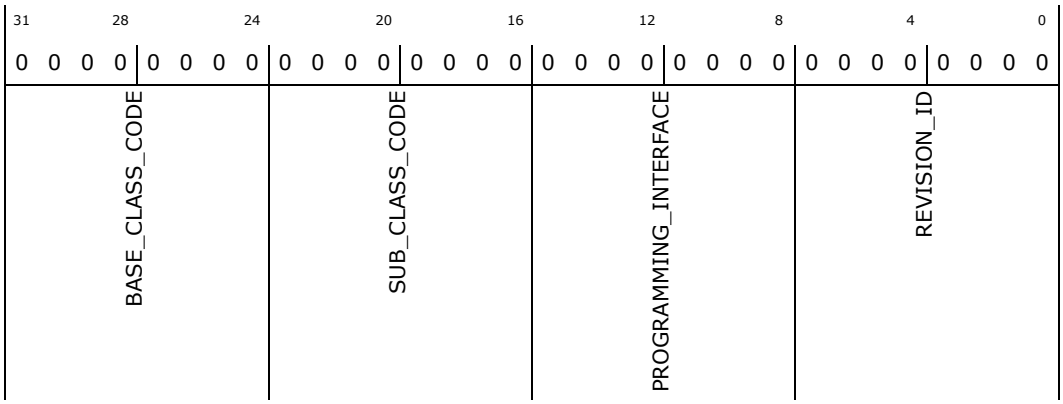
Revision Identification and Class code register. SOXi Context Save/Restore: Yes.

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**BASE_CLASS_CODE:** BCC: This is an 8-bit value that indicates the base class code. When MGGC0[VAMEN] is 0 this code has the value 03h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this code has the value 04h, indicating a Multimedia Device.
23:16	0x0 RO	**SUB_CLASS_CODE:** When MGGC0[VAMEN] is 1, this value is 80h, indicating other multimedia device. When MGGC0[VAMEN] is 0 this value will be determined based on GGC register, GMS and IVD fields. When GGC[1] = 1 or GGC[7:3] = 5'b00000 this value is 80h.
15:8	0x0 RO	**PROGRAMMING_INTERFACE:** PI: When MGGC0[VAMEN] is 0 this value is 00h, indicating a Display Controller.When MGGC0[VAMEN] is 1 this value is 00h, indicating a NOP.
7:0	0x0 RW	**REVISION_ID:** RID: The value in this field reflects the value of strapRID[7:0] (which is an input pin of GVD).For VV: The reset value will be the same as MID bits 23:16 (reference the MID register for MID register details).This register is read-able by any agent.Under SAI protection, the PMC and Punit (ie. 'Trusted_FW') can write this register and change the default value.No other agent has the ability to update this register. The PMC implementation will consider SRID and CRID before updating this register. Any PMC updates will be prior to Device 2 configuration.Note : The MID register will always reflect the stepping information. Even if PMC updates this register, the MID is available as a SRID reference.

4.1.4 HDR—Offset Ch

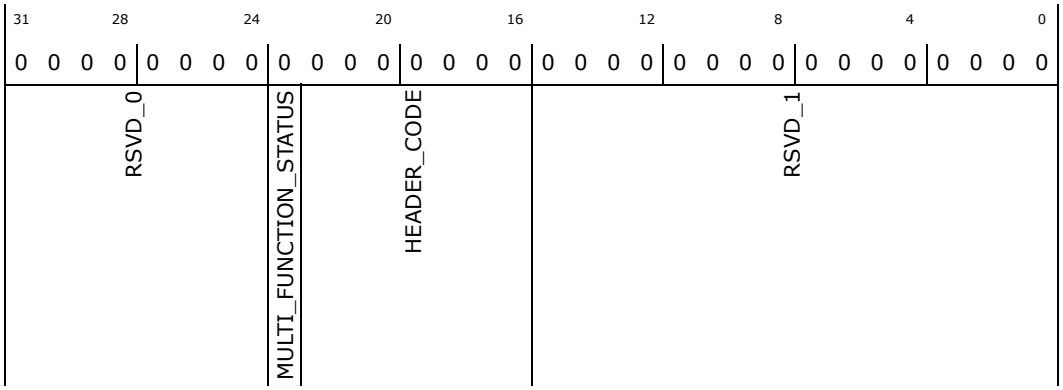
Header Type

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED (RSVD_0):** Reserved
23	0x0 RO	**MULTI_FUNCTION_STATUS:** MFUNC: Integrated graphics is a single function
22:16	0x0 RO	**HEADER_CODE:** HDR: Indicates a type 0 configuration space header format
15:0	0x0 RO	**RESERVED (RSVD_1):** Reserved

4.1.5 GTTMMADR_LSB—Offset 10h

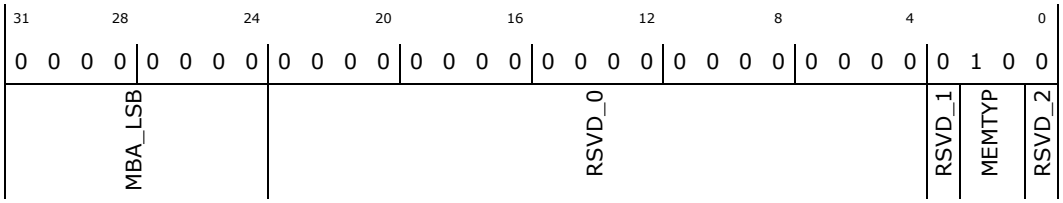
Gfx Memory Mapped Address Range. This is the base address for all memory mapped registers and GTT table.This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. For the Global GTT, this range is defined asa memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area. Prior to this feature it had a max size of 4M with 2M MMADR + 0,1M, 2M GTT.Now GTTMMADR will have a max size of 16M.GTTMMADR = 2M MMADR + 6M rsvd+ 0, 2M, 4M, 8M GTT.GTTMMADR will be 16M aligned.

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: 10h

Default: 00000004h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**MBA_LSB:** Memory Base Address (MBA): Set by the OS, these bits correspond to address signals [35:24].16MB combined for MMIO and Global GTT table aperture (2MB for MMIO, 6MB reserved and 8 MB for GTT).
23:4	0x0 RO	**Reserved (RSVD_0):** RSVD:Hardwired to 0 to indicate at least 4MB address range.
3	0x0 RO	**Reserved (RSVD_1):** Prefetchable Memory (PREFMEM): Hardwired to 0to prevent prefetching.
2:1	0x2 RO	**MEMTYP:** Memory Type (MEMTYP):00: To indicate 32 bit base address01: Reserved10: To indicate 64 bit base address11: Reserved
0	0x0 RO	**Reserved (RSVD_2):** Memory/IO Space (MIOS): Hardwired to 0 to indicate memory space.

4.1.6 GTTMMADR_MSB—Offset 14h

Gfx Memory Mapped Address Range. This is the base address for all memory mapped registers and GTT table.This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. For the Global GTT, this range is defined asa memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area.Prior to this feature it had a max size of 4M with 2M MMADR + 0,1M, 2M GTT.Now GTTMMADR will have a max size of 16M.GTTMMADR = 2M MMADR + 6M rsvd+ 0, 2M, 4M, 8M GTT.GTTMMADR will be 16M aligned.

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: 14h

Default: 00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RW	**MBA_MSB28:** This field must be set to 0 since addressing above 64GB is not supported.In SoC - Made them spare RW bits. MEMTYP=2'b10 indicating 64-bit addressing and PCI compliance test was failing in X0/A0 when this bitfield was left as Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x0 RW	**MBA_MSB:** Memory Base Address (MBA): Set by the OS, these bits correspond to address signals [35:24].16MB combined for MMIO and Global GTT table aperture (2MB for MMIO, 6MB reserved and 8 MB for GTT).

4.1.7 GMADR_LSB—Offset 18h

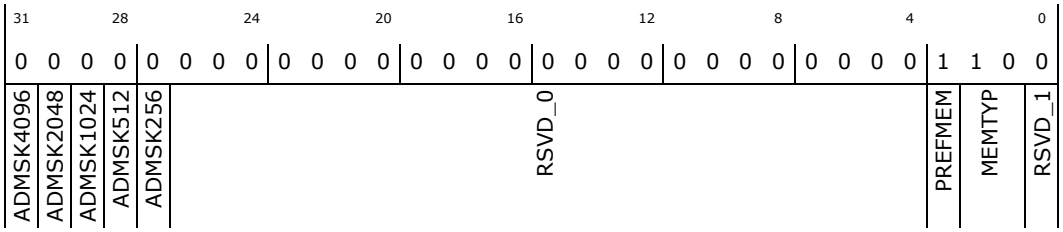
Gfx Aperture location.GMADR is a Prefetchable range in order to apply USWC attribute (from the processor point of view)to that range. The USWC attribute is used by the processor for write combining.Accesses to this range will be translated to DRAM Physical memory addresses. Fence registers may be used to sub-divide this range and allow tiled surfaces (determined by fence registers).The supported sizes are determined by the MSAC register.

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: 18h

Default: 0000000Ch



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/L	**ADMSK4096:** 4096MB Address Mask (ADMSK4096): Locked with MSAC.APSZ[4]. Refer MSAC (Dev2, Func 0, offset 62h) for details.
30	0x0 RW/L	**ADMSK2048:** 2048MB Address Mask (ADMSK2048): Locked with MSAC.APSZ[3]. Refer MSAC (Dev2, Func 0, offset 62h) for details.
29	0x0 RW/L	**ADMSK1024:** 1024MB Address Mask (ADMSK1024): Locked with MSAC.APSZ[2]. Refer MSAC (Dev2, Func 0, offset 62h) for details.
28	0x0 RW/L	**ADMSK512:** 512MB Address Mask (ADMSK512): Locked with MSAC.APSZ[1]. Refer MSAC (Dev2, Func 0, offset 62h) for details.
27	0x0 RW/L	**ADMSK256:** 256MB Address Mask (ADMSK256): Locked with MSAC.APSZ[0].Refer MSAC (Dev2, Func 0, offset 62h) for details.
26:4	0x0 RO	**Reserved (RSVD_0):** Address Mask (ADM): Hardwired to 0s to indicate at least 128MB address range.
3	0x1 RO	**PREFMEM:** Prefetchable Memory (PREFMEM): Hardwired to 1 to enable prefetching.
2:1	0x2 RO	**MEMTYP:** Memory Type (MEMTYP):00: To indicate 32 bit base address01: Reserved10: To indicate 64 bit base address11: Reserved
0	0x0 RO	**Reserved (RSVD_1):** Memory/IO Space (MIOS): Hardwired to 0 to indicate memory space.

4.1.8 GMADR_MSB—Offset 1Ch

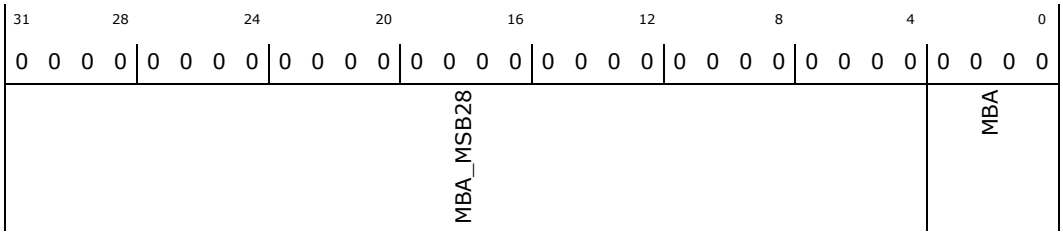
Gfx Aperture location.GMADR is a Prefetchable range in order to apply USWC attribute (from the processor point of view)to that range. The USWC attribute is used by the processor for write combining.Accesses to this range will be translated to DRAM Physical memory addresses. Fence registers may be used to sub-divide this range and allow tiled surfaces (determined by fence registers).The supported sizes are determined by the MSAC register.

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: 1Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RW	**MBA_MSB28:** This filed must be set to 0 since addressing above 64GB is not supported.In SoC - Made them spare RW bits. MEMTYP=2'b10 indicating 64-bit addressing and PCI compliance test was failing in X0/A0 when this bitfield was left as Reserved.
3:0	0x0 RW	**MBA:** Memory Base Address (MBA)Set by the OS, these bits correspond to address signals [35:32]

4.1.9 IOBAR—Offset 20h

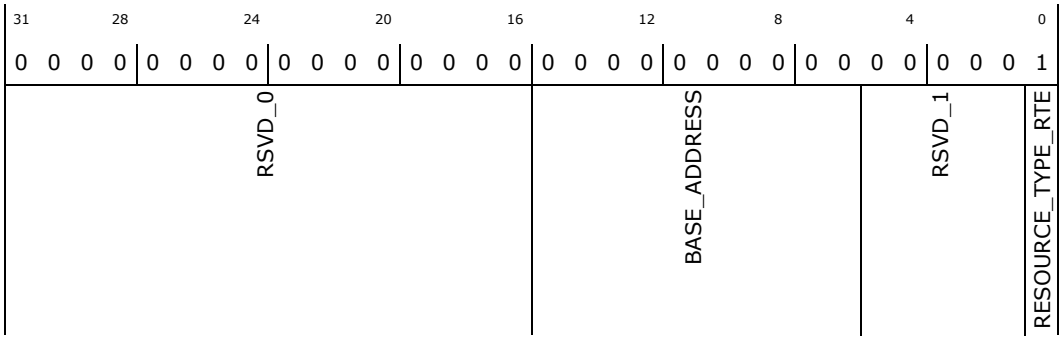
I/O Base Address. This is used only by SBIOS. This register is the base address for the MMIO_INDEX and MMIO_DATA registers.This register provides the Base offset of the I/O registers within Device #2. Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed :* in PM states D1-D3 or* if IO Enable is clear or* if Device #2 is turned off or* if Internal graphics is disabled thru the fuse or fuse override mechanisms. If accesses to this IO bar is allowed then the GMCH claims all 8, 16 or 32 bit IO cycles from the CPU that falls within the 8B claimed.

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: 20h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED (RSVD_0):** Reserved
15:6	0x0 RW	**BASE_ADDRESS:** BA:Set by the OS, these bits correspond to address signals [15:6].IOBAR is to be used for both GTLC register programming and GTT table programming. This is an indirect access method.
5:1	0x0 RO	**RESERVED (RSVD_1):** Reserved
0	0x1 RO	**RESOURCE_TYPE_RTE:** Indicates a request for I/O space

4.1.10 SSID_SID—Offset 2Ch

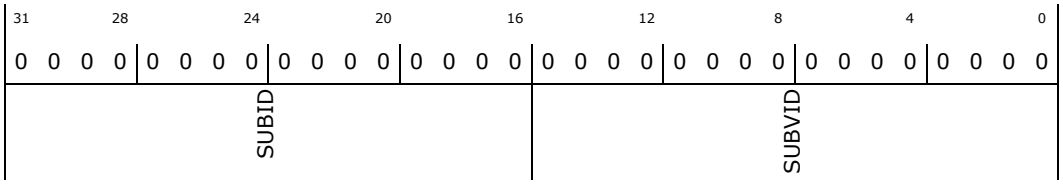
This register is used to uniquely identify the subsystem where the PCI device resides.

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBID:** This value is used to identify the vendor of the subsystem.This register is programmed by BIOS during boot-up.Once written, this register becomes Read_Only.This register is cleared by a Reset.
15:0	0x0 RW/O	**SUBVID:** This value is used to identify the vendor of the subsystem.This register is programmed by BIOS during boot-up.Once written, this register becomes Read_Only.This register is cleared by a Reset.

4.1.11 CAPPOINT—Offset 34h

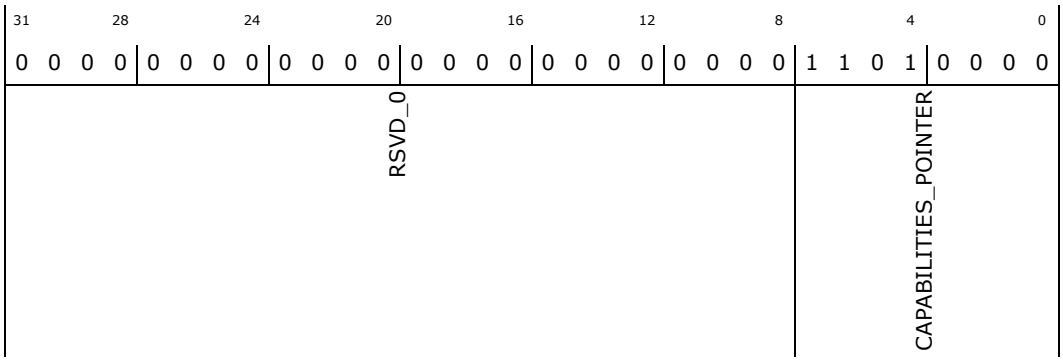
This register points to a linked list of capabilities implemented by this device.For VV, the capability linked list is expected to be : (Head-34, PMCAP-D0, MSI-90, VID-B0, ..End)Old : (Head-34, PMCAP-D0, MSI-90, AFLC-A4, VID-B0, .. End)

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: 34h

Default: 000000D0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED (RSVD_0):** Reserved
7:0	0xd0 RW/O	**CAPABILITIES_POINTER:** The first item in the capabilities list is at address D0h (PMCS).This register is programmed by BIOS during boot-up.Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

4.1.12 INTRLINE—Offset 3Ch

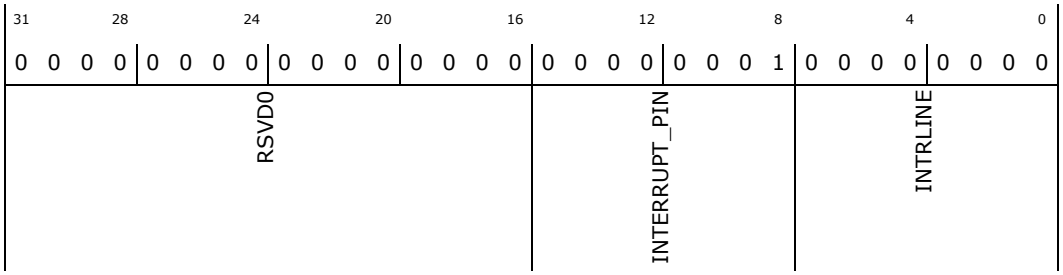
3C - Interrupt. This register is programmed by SBIOS. It is not used by the graphics/ display driver. This8-bit register is used to communicate interrupt line routing information. It is read/write and must be implemented by the device. POST software will write the routing information into this register as it initializes and configures the system.The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to.The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information. 3D - Interrupt. This register is programmed by SBIOS. It is not used by the graphics/display driver

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD0:** Reserved
15:8	0x1 RO	**INTERRUPT_PIN:** IPIN: Value indicates which interrupt pin this device uses. The PCI spec requires that it use INTA#.01h: INTA
7:0	0x0 RW	**INTRLINE:** ILIN: BIOS written value to communicate interrupt line routing information to the device driver.Used to communicate interrupt line routing information.POST software writes the routing information into this register as it initializes and configures the system.The value in this register indicates to which input of the system interrupt controller the device's interrupt pin is connected.

4.1.13 GGC—Offset 50h

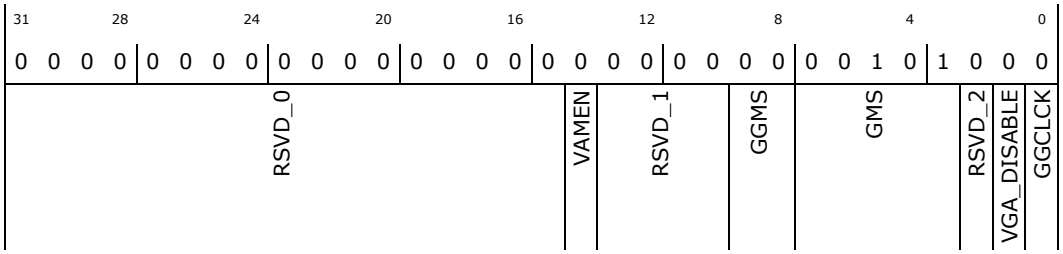
GMCH Graphics Control Register.

Access Method

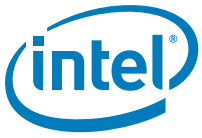
Type: ??? Register
(Size: 32 bits)

Offset: 50h

Default: 00000028h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RO	**RESERVED (RSVD_0):** Reserved
14	0x0 RW/L	**VAMEN:** Enables the use of the iGFX engines for Versatile Acceleration.1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h.0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.



Bit Range	Default & Access	Field Name (ID): Description
13:10	0x0 RO	**RESERVED (RSVD_1):** Reserved
9:8	0x0 RW/L	**GGMS:** GTT Graphics Memory Size (GGMS):This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register.Hardware functionality in case of programming this value to Reserved is not guaranteed.0h:No Preallocated Memory1h: 2MB of Preallocated Memory2h: 4MB of Preallocated Memory3h: 8MB of Preallocated Memory
7:3	0x5 RW/L	**GMS:** Graphics Mode Select(GMS):This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in Native (linear) modes.The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0. BIOS Requirement : Display screen resolution and WOPCM size requirements must be considered as part of programming this registers. Otherwise, invalidation combinations can result. For example, WOPCM size of 8MB with a GMS size of 8MB.That combination is invalid as there is not memory left for the frame buffer.0h = 0MB1h = 32MB2h = 64MB3h = 96MB4h = 128MB5h = 160MB6h = 192MB7h = 224MB8h = 256MB9h = 288MBAh = 320MBBh = 352MBCh = 384MBDh = 416MBEh = 448MBFh = 480MB10h = 512MB11h = 8MB12h = 12MB13h = 16MB14h = 20MB15h = 24MB16h = 28MB17h = 36MB18h = 40MB19h = 44MB1Ah = 48MB1Bh = 52MB1Ch = 56MB1Dh = 60MB1Eh = Reserved1Fh = Reserved.....20h:1024MB (Not supported for SoC).....30h:1536MB (Not supported for SoC).....40h:2048MB (Not supported for SoC).....80h:4096MB (Not supported for SoC)81h - FF:ReservedOther = Reserved When GMS != '0 (and VD=0).If there is a match and MSE = 1 and MEMRD or MEMWR, the access will route as a Rmdwvgamemen_cr cycle on the RMbus.If the RMbus returns a hit the GVD will select the command. If there is a match and IOSE = 1 and the SCLcommand is either an IORD or IOWR, the GVD will initiate a register cycle on the RMbus.
2	0x0 RO	**RESERVED (RSVD_2):** Reserved
0	0x0 RW/L	**GGCLCK:** When set to 1b, this will lock all the bits in this register.

4.1.14 BDSM—Offset 5Ch

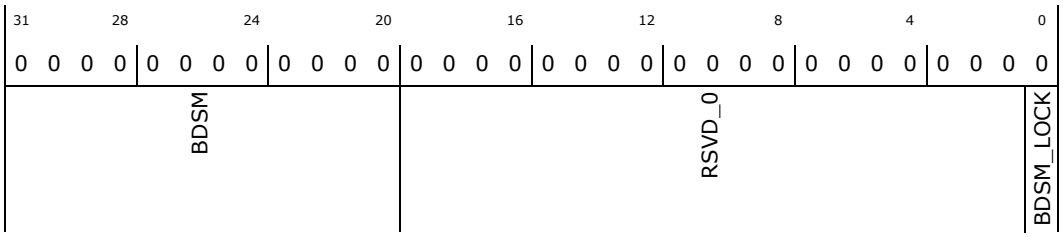
This register contains the base address of Graphics Data Stolen DRAM memory.Note : IVB located this register in device 0, 0xB0. Mirrored into device 2, 0x5C.Graphics Stolen Memory is within DRAM space. The base of stolen memory will always be below 4G.

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: 5Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW/L	**BDSM:** BDSM: BASE_OF_Data_STOLEN_MEMORY.This register contains bits 31 to 20 of the base address of Data stolen DRAM memory. For certain GTLC generated accesses, this base register will be added to GTLC provided offset address, forming the full physical address for the PFI fabric. The display engine also uses the register.Signal : gvd_dsp_cfg_BSM_zcznfwh[31:20].
19:1	0x0 RO	**RESERVED (RSVD_0):** Reserved
0	0x0 RW/L	**BDSM_LOCK:** This bit will lock all writable settings in this register, including itself.

4.1.15 MSAC—Offset 60h

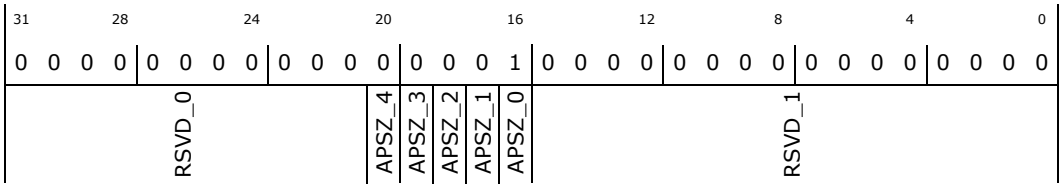
This register determines the size of the graphics memory aperture. Only the system BIOS will write this register based on pre- boot address allocation efforts.Graphics may read this register to determine the correct aperture size. System BIOS needs to save this value on bootso that it can reset it correctly during S3 resume. The size of the aperture must not be modified by software after its location is written into GMADR (offset 18h).

Access Method

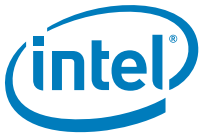
Type: ??? Register
(Size: 32 bits)

Offset: 60h

Default: 00010000h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RO	**RESERVED (RSVD_0):** Reserved



Bit Range	Default & Access	Field Name (ID): Description
20	0x0 RW	**APSZ_4:** This field is used to determine the size of Aperture (GMADR) and controls affects certain bits of GMADR register.00000 = 128MB =GMADR.B [26:4] is hardwired to 0 00001 = 256MB =GMADR.B[27] = 0, RO00010 = illegal (hardware will treat this as 00011)00011 = 512MB =GMADR.B[28:27] = 0, RO00100-00110 = illegal (hardware will treat this as 00111)00111 = 1024MB =GMADR.B[29:27] = 0, RO01000-01110= illegal (hardware will treat this as 01111)01111= 2048MB= GMADR.B[30:27] = 0, RO10000-11110 = illegal (hardware will treat this as 11111)11111= 4096MB = GMADR.B[31:27] = 0, RO
19	0x0 RW	**APSZ_3:** This field is used to determine the size of Aperture (GMADR) and controls affects certain bits of GMADR register.00000 = 128MB =GMADR.B [26:4] is hardwired to 0 00001 = 256MB =GMADR.B[27] = 0, RO00010 = illegal (hardware will treat this as 00011)00011 = 512MB =GMADR.B[28:27] = 0, RO00100-00110 = illegal (hardware will treat this as 00111)00111 = 1024MB =GMADR.B[29:27] = 0, RO01000-01110= illegal (hardware will treat this as 01111)01111= 2048MB= GMADR.B[30:27] = 0, RO10000-11110 = illegal (hardware will treat this as 11111)11111= 4096MB = GMADR.B[31:27] = 0, RO
18	0x0 RW	**APSZ_2:** This field is used to determine the size of Aperture (GMADR) and controls affects certain bits of GMADR register.00000 = 128MB =GMADR.B [26:4] is hardwired to 0 00001 = 256MB =GMADR.B[27] = 0, RO00010 = illegal (hardware will treat this as 00011)00011 = 512MB =GMADR.B[28:27] = 0, RO00100-00110 = illegal (hardware will treat this as 00111)00111 = 1024MB =GMADR.B[29:27] = 0, RO01000-01110= illegal (hardware will treat this as 01111)01111= 2048MB= GMADR.B[30:27] = 0, RO10000-11110 = illegal (hardware will treat this as 11111)11111= 4096MB = GMADR.B[31:27] = 0, RO
17	0x0 RW	**APSZ_1:** This field is used to determine the size of Aperture (GMADR) and controls affects certain bits of GMADR register.00000 = 128MB =GMADR.B [26:4] is hardwired to 0 00001 = 256MB =GMADR.B[27] = 0, RO00010 = illegal (hardware will treat this as 00011)00011 = 512MB =GMADR.B[28:27] = 0, RO00100-00110 = illegal (hardware will treat this as 00111)00111 = 1024MB =GMADR.B[29:27] = 0, RO01000-01110= illegal (hardware will treat this as 01111)01111= 2048MB= GMADR.B[30:27] = 0, RO10000-11110 = illegal (hardware will treat this as 11111)11111= 4096MB = GMADR.B[31:27] = 0, RO
16	0x1 RW	**APSZ_0:** This field is used to determine the size of Aperture (GMADR) and controls affects certain bits of GMADR register.00000 = 128MB =GMADR.B [26:4] is hardwired to 0 00001 = 256MB =GMADR.B[27] = 0, RO00010 = illegal (hardware will treat this as 00011)00011 = 512MB =GMADR.B[28:27] = 0, RO00100-00110 = illegal (hardware will treat this as 00111)00111 = 1024MB =GMADR.B[29:27] = 0, RO01000-01110= illegal (hardware will treat this as 01111)01111= 2048MB= GMADR.B[30:27] = 0, RO10000-11110 = illegal (hardware will treat this as 11111)11111= 4096MB = GMADR.B[31:27] = 0, RO
15:0	0x0 RO	**RESERVED (RSVD_1):** Reserved

4.1.16 BGSM—Offset 70h

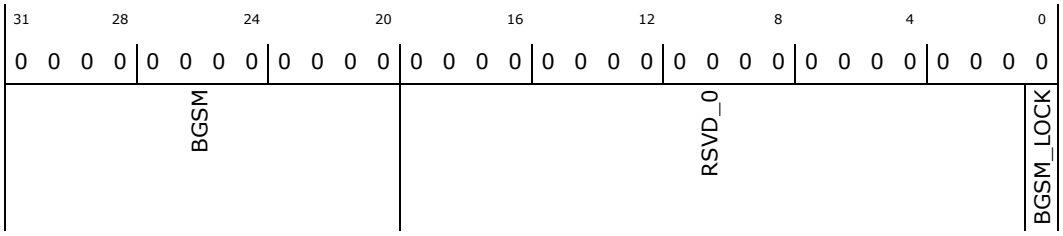
Base of GTT table in Gfx Stolen Memory Note : IVB located this register in device 0, 0xB4. Mirrored into Device 2.The GTT table is located within Graphics Stolen Memory in DRAM space. The base of stolen memory will always be below 4G.

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: 70h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW/L	**BGSM:** BGSM: Gfx Base of GTT Stolen Memory. This register contains bits 31 to 20 of the base address of GTT Table in stolen DRAM memory.BIOS determines base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI offset 50 bits 9:8) from the Graphics Base of Data stolen(PCI offset 5C bits 31:20). Signal: gvd_dsp_Cspgtbladdr_dczfwoh[31:20].
19:1	0x0 RO	**RESERVED (RSVD_0):** Reserved
0	0x0 RW/L	**BGSM_LOCK:** This bit will lock all writeable settings in this register including itself

4.1.17 MSI_CAPID_MC—Offset 90h

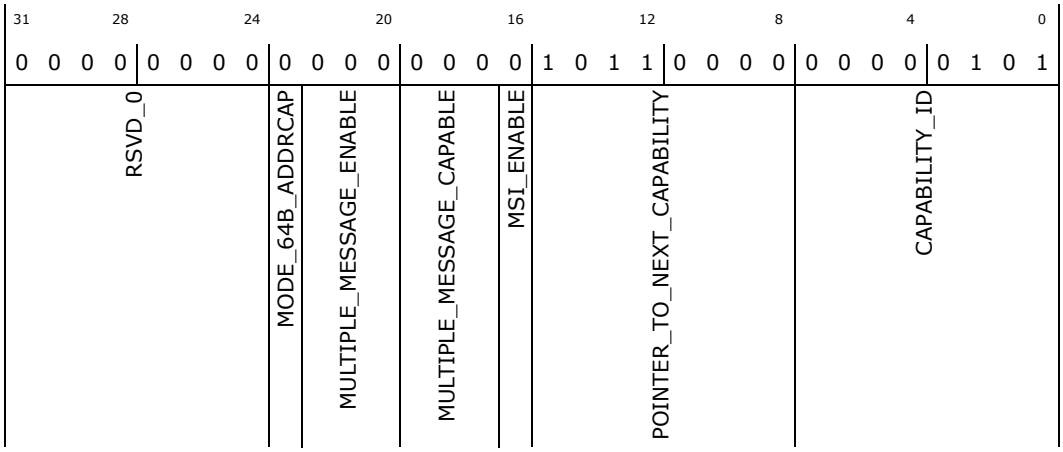
90-91h: Message Signaled Interrupts Capability ID92-93h: Message Signaled Control Register

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: 90h

Default: 0000B005h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED (RSVD_0):** Reserved
23	0x0 RO	**MODE_64B_ADDRCAP:** C64: 32-bit capable only
22:20	0x0 RW	**MULTIPLE_MESSAGE_ENABLE:** MME: This field is RW for software compatibility, but only a single message is ever generated.System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested.The encoding is the same as for the MMC field below.
19:17	0x0 RO	**MULTIPLE_MESSAGE_CAPABLE:** MMC: This device is only single message capable.System Software reads this field to determine the number of messages being requested by this device.Value: Number of requests000: 1001-111: Reserved
16	0x0 RW	**MSI_ENABLE:** MSIE: If set, MSI is enabled and traditional interrupts are not used to generate interrupts. PCICMDSTS.BME must be set for an MSI to be generated.0 : MSI interrupts are disabled.1 : MSI interrupts are enabled. Permits sending an MSI interrupt.
15:8	0xb0 RW/O	**POINTER_TO_NEXT_CAPABILITY:** Points to the next item in the list(B0=VCID support).This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.
7:0	0x5 RO	**CAPABILITY_ID:** CAPID: Indicates an MSI capability

4.1.18 MA—Offset 94h

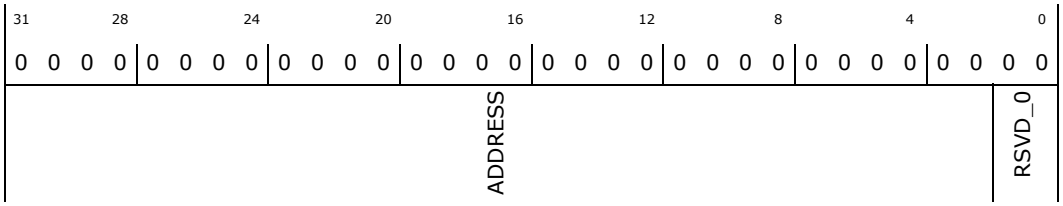
Message Address

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: 94h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**ADDRESS:** MA: Lower 32-bits of the system specified message address, always DW aligned. When GVD issues an MSI interrupt as a MEMWR on the SCL, the memory address corresponds to the value of this field.
1:0	0x0 RO	**RESERVED (RSVD_0):** Reserved

4.1.19 MD—Offset 98h

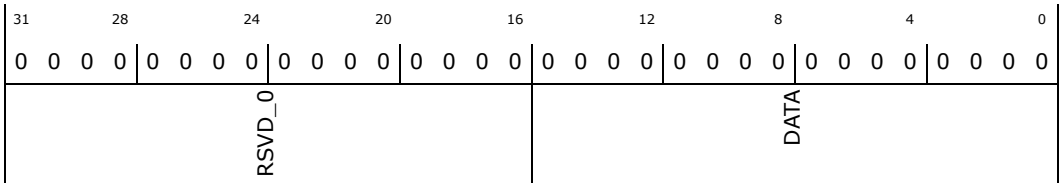
Message Data

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: 98h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED (RSVD_0):** Reserved
15:0	0x0 RW	**DATA:** MD: This 16-bit field is programmed by system software. This forms the lower word of data for the MSI write transaction.

4.1.20 Advanced Features Length and Capabilities (AFLC)—Offset A4h

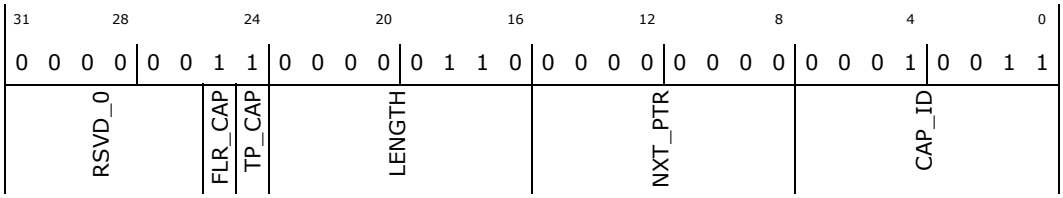
FLR capability advertisement

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: A4h

Default: 03060013h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RESERVED (RSVD_0):** Reserved
25	0x1 RO	**FLR_CAP:** Function Level Reset Capability (FLR_CAP):0: Function Level Reset is not supported1: Function Level Reset is supported
24	0x1 RO	**TP_CAP:** Transactions Pending Capability (TP_CAP):0: Transactions Pending bit is not supported1: Transactions Pending bit is supported
23:16	0x6 RO	**LENGTH:** Advanced Features Structure Length(LENGTH): The Advanced Features capability structure is 6bytes long.
15:8	0x0 RW/O	**NXT_PTR:** Next Pointer (NXT_PTR): Removed FLR capability per HSD 259253. Nulled the next pointer.Points to the next item in the list (B0=Vendor Capabilities ID)This register should be programmed by BIOS during boot-up. Once written,this register becomes Read_Only. This register can only be cleared by a Reset.Write once so capabilities list can be changed if needed.
7:0	0x13 RO	**CAP_ID:** Capability Identifier (CAP_ID): A value of 13h identifies that this PCI Function is capable of Advanced Features.

4.1.21 AFCTLSTS—Offset A8h

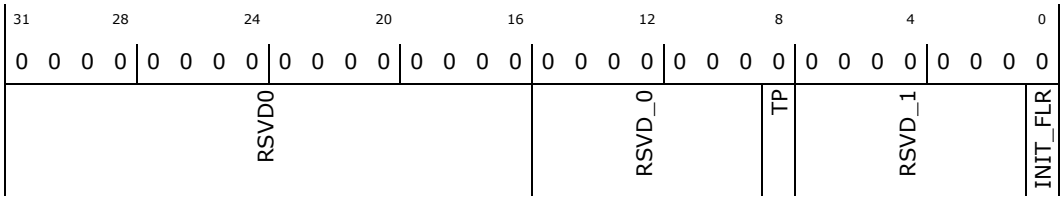
FLR control refer the July 27th 2006 Engineering Change Notice for Conventional PCI Advanced Capabilities.Advanced Feature Status

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD0:** Reserved
15:9	0x0 RO	**Reserved (RSVD_0):** Reserved (RSVD)

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RO	**TP:** Transaction Pending (TP):1: The Function has issued one or more non-posted transactions which have not been completed, including non-posted transactions that a target has terminated with Retry.0: All non-posted transactions have been completed.
7:1	0x0 RO	**Reserved (RSVD_1):** Reserved (RSVD)
0	0x0 RW/S	**INIT_FLR:** Initiate Function Level Reset (INIT_FLR):A write of 1b initiates Function Level Reset (FLR).FLR requirements are defined in the PCI Express Base Specification.Registers and state information that do not apply to conventional PCIare exempt from the FLR requirements given there.Once written 1, FLR will be initiated. During FLR, a read will return1's since device 2 reads abort. Once FLR completes, hardware will clear the bit to 0.

4.1.22 VCID—Offset B0h

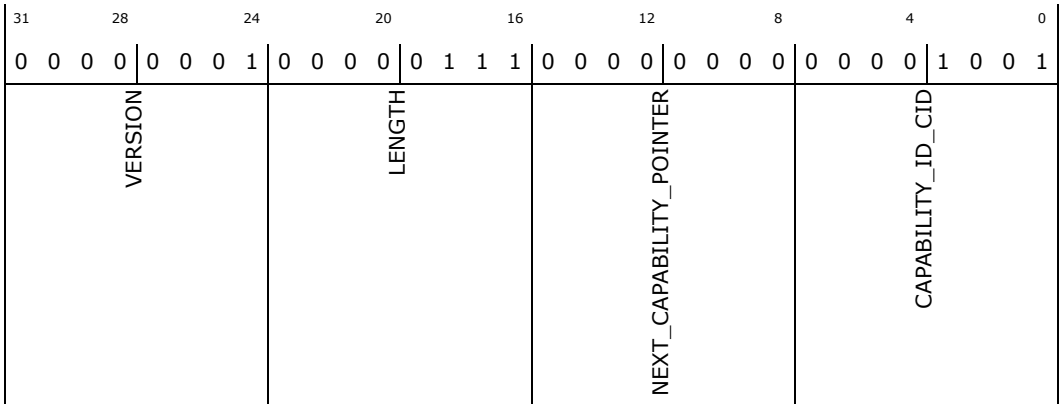
Vendor Capability ID

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: B0h

Default: 01070009h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x1 RO	**VERSION:** VS: Identifies this as the first revision of the CAPID register definition.
23:16	0x7 RO	**LENGTH:** LEN: This field has the value 07h to indicate structure length (8 bytes)
15:8	0x0 RW/O	**NEXT_CAPABILITY_POINTER:** 00 indicates capability list ends here.This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.Write-once allowing the capability list to be changed.
7:0	0x9 RO	**CAPABILITY_ID_CID:** Identifies this as a vendor dependent capability pointers.

4.1.23 VC—Offset B4h

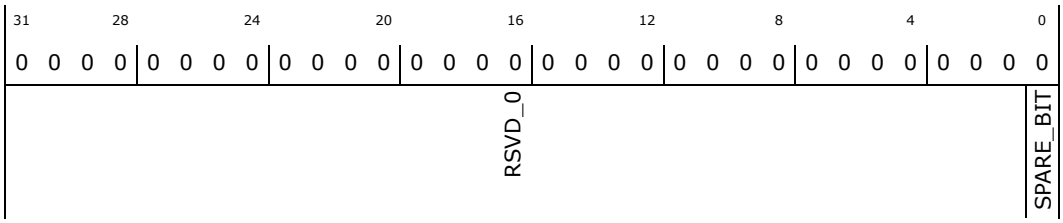
Vendor Capabilities. Any SKU related fuses would be added here.

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: B4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**Reserved (RSVD_0):** Reserved
0	0x0 RO	**Spare_bit (SPARE_BIT):** Placeholder for sku related fusing.

4.1.24 FD—Offset C4h

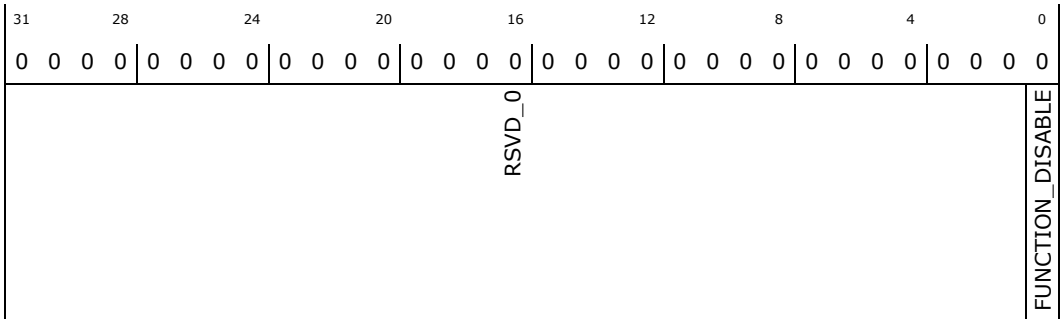
Functional Disable. This register is used by SBIOS, not by driver.

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: C4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RESERVED (RSVD_0):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**FUNCTION_DISABLE:** FD:0 : Default - normal operation.1 : When set, the function is disabled (configuration space is disabled). All new requests on the IOSF Primary bus, including any new configuration cycle requests are not claimed on IOSF Primary.This bit as no effect register accessibility via IOSF SB. Once programmed to '1', the only way to re-enable device 2 is via an IOSF SB write of '0' to this register.SoC : Wire is sent to PSF for decode purposes gvd_psf_dev2disable_nczfwoh.

4.1.25 PMCAPID—Offset D0h

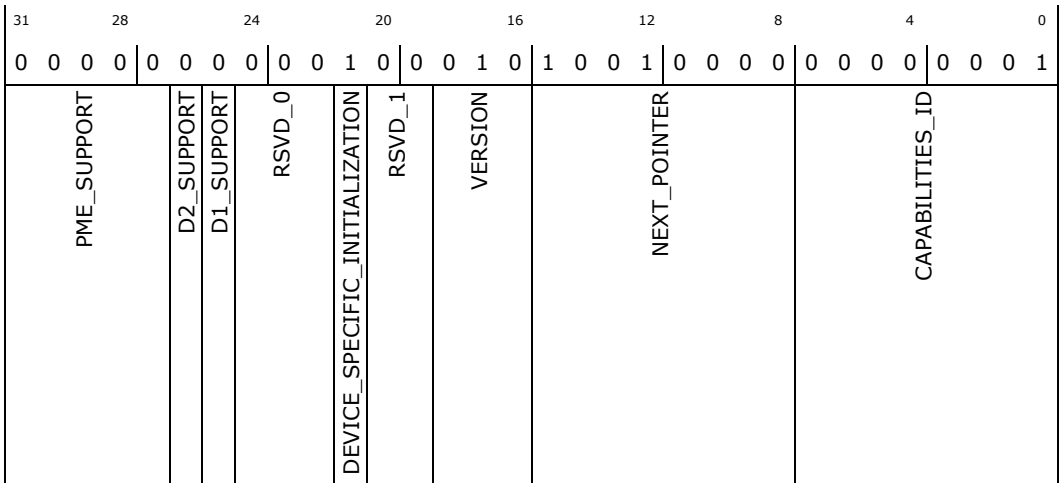
PCI Address: D0-D1h Description : Power Management Capabilities IDPCI Address: D2-D3h Description : Power Management Capabilities

Access Method

Type: ??? Register (Size: 32 bits)

Offset: D0h

Default: 00229001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PME_SUPPORT:** PMES The graphics controller does not generate PME.
26	0x0 RO	**D2_SUPPORT:** D2S: D2 power management state is not supported.
25	0x0 RO	**D1_SUPPORT:** D1S: D1 power management state is not supported.
24:22	0x0 RO	**RESERVED (RSVD_0):** Reserved
21	0x1 RO	**DEVICE_SPECIFIC_INITIALIZATION:** Hardwired to 1 to indicate that special initialization of the graphics controller is required before generic class device driver is to use it.

Bit Range	Default & Access	Field Name (ID): Description
20:19	0x0 RO	**RESERVED (RSVD_1):** Reserved
18:16	0x2 RO	**VERSION:** Version compliance with revision 1.1 of PCI Power management spec.
15:8	0x90 RW/O	**NEXT_POINTER:** Indicates the next item in the capabilities list(90=MSI)This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.Write once allowing changing of the capabilities list.
7:0	0x1 RO	**CAPABILITIES_ID:** CAPID: SIG defines this ID is 01h for power management.

4.1.26 PMCS—Offset D4h

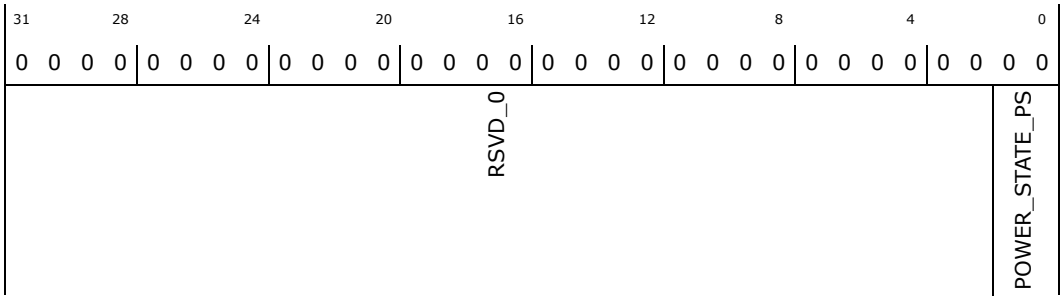
Power Management Control/Status. Driver does not use this register. SBIOS does not use this register

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: D4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**RESERVED (RSVD_0):** Reserved
1:0	0x0 RW	**POWER_STATE_PS:** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state.If software attempts to write an unsupported state to this field, write operation must complete normally on the bus,but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Behavior of the graphics controller in supported states is detailed in the power management section of the Bspec.Bits[1:0] Power state00: D0 Default01: D1 Not Supported10: D2 Not Supported11: D3Signal : gvd_dsp_power_state_d3_nczfwoh output to 2D.

4.1.27 SWSMISCI—Offset E0h

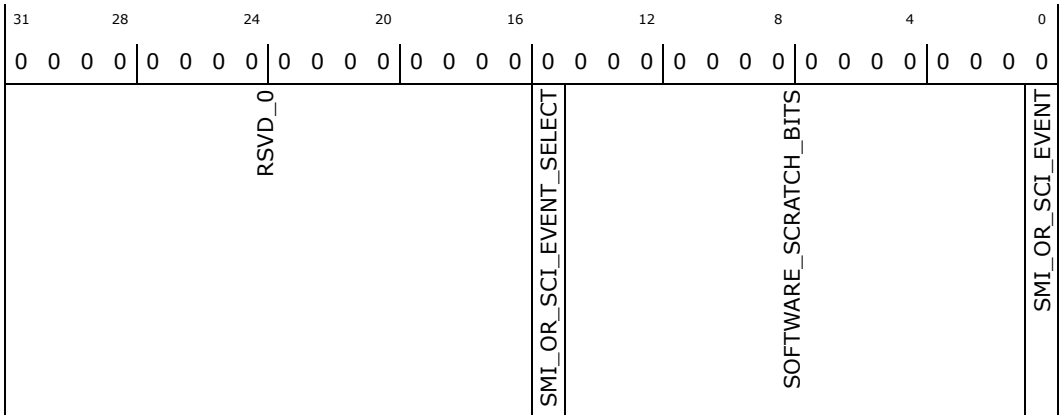
Software SMI or SCI. Note : ILK/SNB/IVB had SCI and SMI separated (E0 and E8). As long as there is the potential that DVO port legacy drivers exist which expect this register at this address, this must be reserved for this register.The SCI mechanism for driver / BIOS communication. SMI is a system wide lock interrupt (halts all the cores) as opposed to SCI. Vista and Win7 recommend to use the SCI. The SMI is slowly being phased out.This register serves 2 purposes: 1) Support selection of SMI or SCI event source (SMISCISEL - bit15) 2) Event trigger (bit 0). To generate a SW SCI event, software (System BIOS/Graphics driver) should program bit 15 (SMISCISEL) to 1.This is typically programmed once (assuming SM Is are never triggered). On a '0' to '1' subsequent transition in bit 0 of this register (caused by a software write operation), GMCH sends a single SCI message. The SCI will set the DMISCI bit in its TCO1_STS register and TCOSCI_STS bit in its GPE0 register upon receiving this message from DMI.Once written as 1, software must write a '0' to this bit to clear it, and all other write transitions (1-0, 0-0, 1-1) or if bit 15 is '0' will not cause GMCH to send SCI message to DMI link.To generate a SW SMI event, software should program bit 15:0 and trigger SMI.

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: E0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED (RSVD_0):** Reserved
15	0x0 RW	**SMI_OR_SCI_EVENT_SELECT:** MCS: SMI or SCI event select. 0 = SMI,1 = SCI
14:1	0x0 RW	**SOFTWARE_SCRATCH_BITS:** Used by driver to communicate information to SBIOS

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**SMI_OR_SCI_EVENT:** MCE:MCS=1, setting this bit causes an SCI.MCS=0, setting this bit causes an SMI. A 1 to 0, 0 to 0 or 1 to 1 transition of this bit does not trigger any events. The graphics driver writes to this register as a means to interrupt the SBIOS.

4.1.28 ASLE—Offset E4h

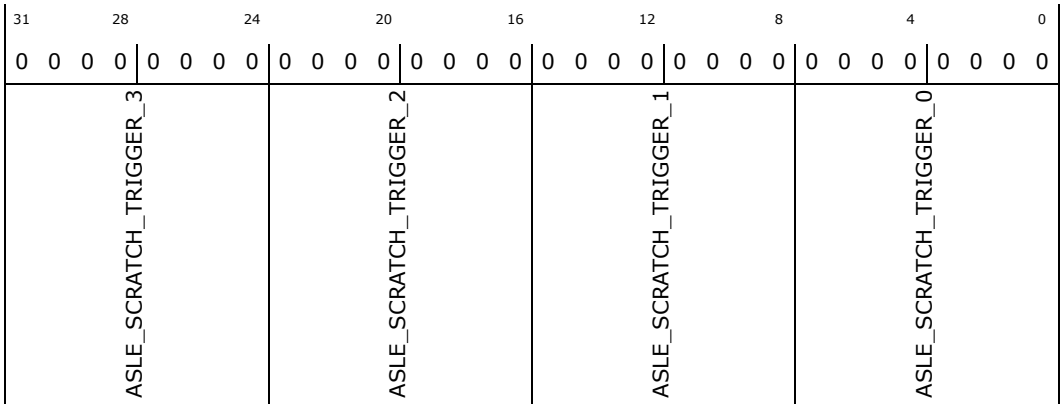
System Display Event Register. SBIOS writes this reg to generate interrupt to graphics/ display driver. Note : This was renamed to GSE (General System Event) on Ironlake/ SNB/IVB.

Access Method

Type: ??? Register
(Size: 32 bits)

Offset: E4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**ASLE_SCRATCH_TRIGGER_3:** AST3: The writing of this by field (byte) - even if just writing back the original contents- will trigger a display controller interrupt (when the memory interface register bitsIER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
23:16	0x0 RW	**ASLE_SCRATCH_TRIGGER_2:** AST2: The writing of this by field (byte) - even if just writing back the original contents- will trigger a display controller interrupt (when the memory interface register bits IER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
15:8	0x0 RW	**ASLE_SCRATCH_TRIGGER_1:** AST1: The writing of this by field (byte) - even if just writing back the original contents- will trigger a display controller interrupt (when the memory interface register bits IER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ASLE_SCRATCH_TRIGGER_0:** AST0: The writing of this by field (byte) - even if just writing back the original contents - will trigger a display controller interrupt (when the memory interface register bitsIER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.

4.1.29 ASLS—Offset FCh

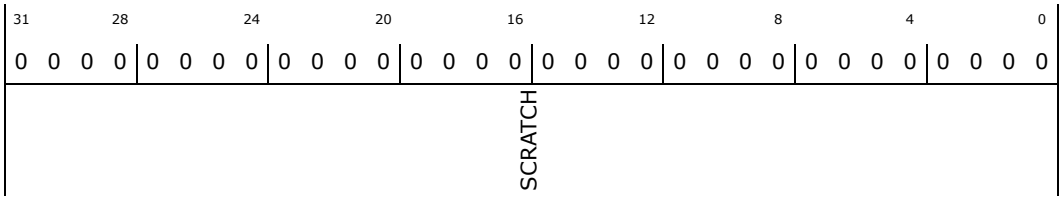
ASL Storage. This register is kept for use as scratch space.This software scratch register only needs to be read/write accessible. The exact bit register usage must be worked out in common between System BIOS and driver software, but storage for switching/indicating up to 6 devices is possible with this amount. For each device, the ASL control method with require two bits for _DOD (BIOS detectable yes or no), one bit for _DGS (enable/disable requested), and two bits for _DCS (enabled now/disabled now, connected or not).

Access Method

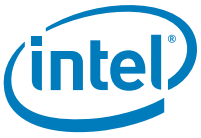
Type: ??? Register
(Size: 32 bits)

Offset: FCh

Default: 00000000h



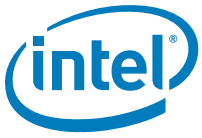
Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SCRATCH:** This register provides a means for the BIOS to communicate with the driver.This definition of this scratch register is worked out in common between System BIOS and driver software. Storage for up to 6 devices is possible.For each device, the ASL control method requires two bits for _DOD (BIOS detectable yes or no), one bit for _DGS (enable/disable requested), and two bits for DCS (enabled now/disabled now, connected or not).



4.2 DEFAULT Address Map

Table 22. Summary of Memory Mapped I/O Registers—

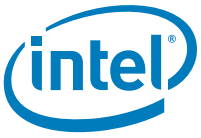
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3B4–3B4h	1	"CRX (CRX_MDA)—Offset 3B4h" on page 116	00h
3B5–3B5h	1	"CR (CR_MDA)—Offset 3B5h" on page 116	00h
3C0–3C0h	1	"ARX—Offset 3C0h" on page 117	00h
3C1–3C3h	3	"ARX—Offset 3C0h" on page 117	00h
3C4–3C4h	1	"SRX—Offset 3C4h" on page 118	00h
3C5–3C5h	1	"SRX—Offset 3C4h" on page 118	00h
3C6–3C7h	2	"DACMASK—Offset 3C6h" on page 119	00h
3C8–3C8h	1	"DACWX—Offset 3C8h" on page 120	00h
3C9–3C9h	1	"DACDATA—Offset 3C9h" on page 121	00h
3CA–3CBh	2	"FCR (FCR_Read)—Offset 3CAh" on page 122	00h
3CC–3CDh	2	"MSR (MSR_READ)—Offset 3CCh" on page 122	00h
3CE–3CEh	1	"GRX—Offset 3CEh" on page 123	00h
3CF–3CFh	1	"GRX—Offset 3CEh" on page 123	00h
3D4–3D4h	1	"CRX (CRX_CGA)—Offset 3D4h" on page 125	00h
3D5–3D5h	1	"CR (CR_CGA)—Offset 3D5h" on page 125	00h
5010–5013h	4	"GPIOCTL_0—Offset 5010h" on page 126	00000808h
5014–5017h	4	"GPIOCTL_1—Offset 5014h" on page 128	00000808h
5018–501Bh	4	"GPIOCTL_2—Offset 5018h" on page 130	00000808h
501C–501Fh	4	"GPIOCTL_3—Offset 501Ch" on page 132	00000808h
5020–5023h	4	"GPIOCTL_4—Offset 5020h" on page 134	00000808h
5100–5103h	4	"GMBUS0—Offset 5100h" on page 136	00000000h
5104–5107h	4	"GMBUS1—Offset 5104h" on page 137	00000000h
5108–510Bh	4	"GMBUS2—Offset 5108h" on page 140	00000800h
510C–510Fh	4	"GMBUS3—Offset 510Ch" on page 142	00000000h
5110–5113h	4	"GMBUS4—Offset 5110h" on page 143	00000000h
5120–5123h	4	"GMBUS5—Offset 5120h" on page 144	00000000h
5130–5133h	4	"GMBUS6—Offset 5130h" on page 144	00000000h
5134–5137h	4	"GMBUS7—Offset 5134h" on page 145	00000000h
6014–6017h	4	"DPLLA_CTRL—Offset 6014h" on page 146	00002000h
6018–601Bh	4	"DPLLB_CTRL—Offset 6018h" on page 149	00006000h
601C–601Fh	4	"DPLLAMD—Offset 601Ch" on page 152	00000003h
6020–6023h	4	"DPLLBMD—Offset 6020h" on page 154	00000003h
6024–6027h	4	"RAWCLK_FREQ—Offset 6024h" on page 155	0000007Dh
6030–6033h	4	"DPLLC_CTRL—Offset 6030h" on page 156	00006000h



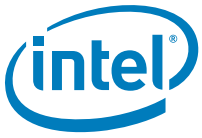
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
6034–6037h	4	"DSPCLK1_GATE_D—Offset 6034h" on page 159	00000000h
6038–603Bh	4	"DOT_MIPI—Offset 6038h" on page 160	00000000h
603C–603Fh	4	"DPLLCMD—Offset 603Ch" on page 161	00000003h
6104–6107h	4	"D_STATE—Offset 6104h" on page 163	20D00400h
6200–6203h	4	"DSPCLK_GATE_D—Offset 6200h" on page 164	10000000h
6204–6207h	4	"DPPSR_CGDIS—Offset 6204h" on page 168	00000200h
6210–6213h	4	"RAMCLK_GATE_D—Offset 6210h" on page 170	00000000h
6220–6223h	4	"DPPSR1_CGDIS—Offset 6220h" on page 174	00000000h
6240–6243h	4	"DPIO_PHY_STATUS—Offset 6240h" on page 176	00000000h
6300–630Fh	10	"DSPCSS—Offset 6300h" on page 176	00000000000000000000000000000000h
6500–6503h	4	"FW_BLC_SELF—Offset 6500h" on page 178	00000000h
6504–6507h	4	"MI_ARB—Offset 6504h" on page 179	00000000h
6508–650Bh	4	"CZCLK_CDCLK_FREQ_RATIO—Offset 6508h" on page 179	00000077h
650C–650Fh	4	"GCI_CONTROL—Offset 650Ch" on page 184	00004000h
6510–6513h	4	"GMBUSFREQ—Offset 6510h" on page 186	000000A0h
A000–A003h	4	"DPALETTE_A—Offset A000h" on page 187	00000000h
A800–A803h	4	"DPALETTE_B—Offset A800h" on page 188	00000000h
B000–B003h	4	"MIPIA_DEVICE_READY_REG—Offset B000h" on page 189	00000000h
B004–B007h	4	"MIPIA_INTR_STAT_REG—Offset B004h" on page 189	00000000h
B008–B00Bh	4	"MIPIA_INTR_EN_REG—Offset B008h" on page 192	00000000h
B00C–B00Fh	4	"MIPIA_DSI_FUNC_PRG__REG—Offset B00Ch" on page 194	00000001h
B010–B013h	4	"MIPIA_HS_TX_TIMEOUT_REG—Offset B010h" on page 195	00000000h
B014–B017h	4	"MIPIA_LP_RX_TIMEOUT_REG—Offset B014h" on page 196	00000000h
B018–B01Bh	4	"MIPIA_TURN_AROUND_TIMEOUT_REG—Offset B018h" on page 196	00000000h
B01C–B01Fh	4	"MIPIA_DEVICE_RESET_TIMER—Offset B01Ch" on page 197	00000000h
B020–B023h	4	"MIPIA_DPI_RESOLUTION_REG—Offset B020h" on page 198	00000000h
B024–B027h	4	"MIPIA_DBI_RESOLUTION_REG—Offset B024h" on page 198	00000000h
B028–B02Bh	4	"MIPIA_HORIZ_SYNC_PADDING_COUNT—Offset B028h" on page 199	00000000h
B02C–B02Fh	4	"MIPIA_HORIZ_BACK_PORCH_COUNT—Offset B02Ch" on page 200	00000000h
B030–B033h	4	"MIPIA_HORIZ_FRONT_PORCH_COUNT—Offset B030h" on page 200	00000000h
B034–B037h	4	"MIPIA_HORIZ_ACTIVE_AREA_COUNT—Offset B034h" on page 201	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
B038–B03Bh	4	"MIPIA_VERT_SYNC_PADDING_COUNT—Offset B038h" on page 202	00000000h
B03C–B03Fh	4	"MIPIA_VERT_BACK_PORCH_COUNT—Offset B03Ch" on page 202	00000000h
B040–B043h	4	"MIPIA_VERT_FRONT_PORCH_COUNT—Offset B040h" on page 203	00000000h
B044–B047h	4	"MIPIA_HIGH_LOW_SWITCH_COUNT—Offset B044h" on page 204	00000000h
B048–B04Bh	4	"MIPIA_DPI_CTRL_REG—Offset B048h" on page 205	00000000h
B04C–B04Fh	4	"MIPIA_DPI_DATA_REGISTER—Offset B04Ch" on page 206	00000000h
B050–B053h	4	"MIPIA_INIT_COUNT_REGISTER—Offset B050h" on page 206	00000000h
B054–B057h	4	"MIPIA_MAX_RETURN_PKT_SIZE_REGISTER—Offset B054h" on page 207	00000000h
B058–B05Bh	4	"MIPIA_VIDEO_MODE_FORMAT_REGISTER—Offset B058h" on page 207	00000000h
B05C–B05Fh	4	"MIPIA_EOT_DISABLE_REGISTER—Offset B05Ch" on page 208	00000000h
B060–B063h	4	"MIPIA_LP_BYTECLK_REGISTER—Offset B060h" on page 210	00000000h
B064–B067h	4	"MIPIA_LP_GEN_DATA_REGISTER—Offset B064h" on page 211	00000000h
B068–B06Bh	4	"MIPIA_HS_GEN_DATA_REGISTER—Offset B068h" on page 211	00000000h
B06C–B06Fh	4	"MIPIA_LP_GEN_CTRL_REGISTER—Offset B06Ch" on page 212	00000000h
B070–B073h	4	"MIPIA_HS_GEN_CTRL_REGISTER—Offset B070h" on page 213	00000000h
B074–B077h	4	"MIPIA_GEN_FIFO_STAT_REGISTER—Offset B074h" on page 214	1E060606h
B078–B07Bh	4	"MIPIA_HS_LS_DBI_ENABLE_REG—Offset B078h" on page 215	00000000h
B07C–B07Fh	4	"MIPIA_RESERVED—Offset B07Ch" on page 216	00000000h
B080–B083h	4	"MIPIA_DPHY_PARAM_REG—Offset B080h" on page 216	0B061A04h
B084–B087h	4	"MIPIA_DBI_BW_CTRL_REG—Offset B084h" on page 217	00000000h
B088–B08Bh	4	"MIPIA_CLK_LANE_SWITCHING_TIME_CNT—Offset B088h" on page 217	00000000h
B08C–B08Fh	4	"MIPIA_STOP_STATE_STALL—Offset B08Ch" on page 218	00000000h
B090–B093h	4	"MIPIA_INTR_STAT_REG_1—Offset B090h" on page 219	00000000h
B094–B097h	4	"MIPIA_INTR_EN_REG_1—Offset B094h" on page 220	00000000h
B100–B103h	4	"MIPIA_DBI_TYPEC_CTRL—Offset B100h" on page 221	00000000h
B104–B107h	4	"MIPIA_CTRL—Offset B104h" on page 222	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
B108–B10Bh	4	"MIPIA_DATA_ADD—Offset B108h" on page 223	00000000h
B10C–B10Fh	4	"MIPIA_DATA_LEN—Offset B10Ch" on page 224	00000000h
B110–B113h	4	"MIPIA_CMD_ADD—Offset B110h" on page 224	00000000h
B114–B117h	4	"MIPIA_CMD_LEN—Offset B114h" on page 225	00000000h
B118–B11Bh	4	"MIPIA_RD_DATA_RETURN0—Offset B118h" on page 225	00000000h
B11C–B11Fh	4	"MIPIA_RD_DATA_RETURN1—Offset B11Ch" on page 226	00000000h
B120–B123h	4	"MIPIA_RD_DATA_RETURN2—Offset B120h" on page 226	00000000h
B124–B127h	4	"MIPIA_RD_DATA_RETURN3—Offset B124h" on page 227	00000000h
B128–B12Bh	4	"MIPIA_RD_DATA_RETURN4—Offset B128h" on page 227	00000000h
B12C–B12Fh	4	"MIPIA_RD_DATA_RETURN5—Offset B12Ch" on page 228	00000000h
B130–B133h	4	"MIPIA_RD_DATA_RETURN6—Offset B130h" on page 228	00000000h
B134–B137h	4	"MIPIA_RD_DATA_RETURN7—Offset B134h" on page 229	00000000h
B138–B13Bh	4	"MIPIA_RD_DATA_VALID—Offset B138h" on page 229	00000000h
B800–B803h	4	"MIPIC_DEVICE_READY_REG—Offset B800h" on page 230	00000000h
B804–B807h	4	"MIPIC_INTR_STAT_REG—Offset B804h" on page 231	00000000h
B808–B80Bh	4	"MIPIC_INTR_EN_REG—Offset B808h" on page 233	00000000h
B80C–B80Fh	4	"MIPIC_DSI_FUNC_PRG__REG—Offset B80Ch" on page 235	00000001h
B810–B813h	4	"MIPIC_HS_TX_TIMEOUT_REG—Offset B810h" on page 236	00000000h
B814–B817h	4	"MIPIC_LP_RX_TIMEOUT_REG—Offset B814h" on page 237	00000000h
B818–B81Bh	4	"MIPIC_TURN_AROUND_TIMEOUT_REG—Offset B818h" on page 237	00000000h
B81C–B81Fh	4	"MIPIC_DEVICE_RESET_TIMER—Offset B81Ch" on page 238	00000000h
B820–B823h	4	"MIPIC_DPI_RESOLUTION_REG—Offset B820h" on page 239	00000000h
B824–B827h	4	"MIPIC_DBI_RESOLUTION_REG—Offset B824h" on page 239	00000000h
B828–B82Bh	4	"MIPIC_HORIZ_SYNC_PADDING_COUNT—Offset B828h" on page 240	00000000h
B82C–B82Fh	4	"MIPIC_HORIZ_BACK_PORCH_COUNT—Offset B82Ch" on page 241	00000000h
B830–B833h	4	"MIPIC_HORIZ_FRONT_PORCH_COUNT—Offset B830h" on page 241	00000000h
B834–B837h	4	"MIPIC_HORIZ_ACTIVE_AREA_COUNT—Offset B834h" on page 242	00000000h
B838–B83Bh	4	"MIPIC_VERT_SYNC_PADDING_COUNT—Offset B838h" on page 243	00000000h
B83C–B83Fh	4	"MIPIC_VERT_BACK_PORCH_COUNT—Offset B83Ch" on page 243	00000000h
B840–B843h	4	"MIPIC_VERT_FRONT_PORCH_COUNT—Offset B840h" on page 244	00000000h
B844–B847h	4	"MIPIC_HIGH_LOW_SWITCH_COUNT—Offset B844h" on page 245	00000000h

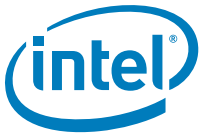


Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
B848–B84Bh	4	"MIPIC_DPI_CTRL_REG—Offset B848h" on page 246	00000000h
B84C–B84Fh	4	"MIPIC_DPI_DATA_REGISTER—Offset B84Ch" on page 247	00000000h
B850–B853h	4	"MIPIC_INIT_COUNT_REGISTER—Offset B850h" on page 247	00000000h
B854–B857h	4	"MIPIC_MAX_RETURN_PKT_SIZE_REGISTER—Offset B854h" on page 248	00000000h
B858–B85Bh	4	"MIPIC_VIDEO_MODE_FORMAT_REGISTER—Offset B858h" on page 248	00000000h
B85C–B85Fh	4	"MIPIC_EOT_DISABLE_REGISTER—Offset B85Ch" on page 249	00000000h
B860–B863h	4	"MIPIC_LP_BYTECLK_REGISTER—Offset B860h" on page 251	00000000h
B864–B867h	4	"MIPIC_LP_GEN_DATA_REGISTER—Offset B864h" on page 252	00000000h
B868–B86Bh	4	"MIPIC_HS_GEN_DATA_REGISTER—Offset B868h" on page 252	00000000h
B86C–B86Fh	4	"MIPIC_LP_GEN_CTRL_REGISTER—Offset B86Ch" on page 253	00000000h
B870–B873h	4	"MIPIC_HS_GEN_CTRL_REGISTER—Offset B870h" on page 254	00000000h
B874–B877h	4	"MIPIC_GEN_FIFO_STAT_REGISTER—Offset B874h" on page 255	1E060606h
B878–B87Bh	4	"MIPIC_HS_LS_DBI_ENABLE_REG—Offset B878h" on page 256	00000000h
B87C–B87Fh	4	"MIPIC_RESERVED—Offset B87Ch" on page 257	00000000h
B880–B883h	4	"MIPIC_DPHY_PARAM_REG—Offset B880h" on page 257	0B061A04h
B884–B887h	4	"MIPIC_DBI_BW_CTRL_REG—Offset B884h" on page 258	00000000h
B888–B88Bh	4	"MIPIC_CLK_LANE_SWITCHING_TIME_CNT—Offset B888h" on page 258	00000000h
B88C–B88Fh	4	"MIPIC_STOP_STATE_STALL—Offset B88Ch" on page 259	00000000h
B890–B893h	4	"MIPIC_INTR_STAT_REG_1—Offset B890h" on page 260	00000000h
B894–B897h	4	"MIPIC_INTR_EN_REG_1—Offset B894h" on page 261	00000000h
B908–B90Bh	4	"MIPIC_DATA_ADD—Offset B908h" on page 262	00000000h
B90C–B90Fh	4	"MIPIC_DATA_LEN—Offset B90Ch" on page 263	00000000h
B910–B913h	4	"MIPIC_CMD_ADD—Offset B910h" on page 263	00000000h
B914–B917h	4	"MIPIC_CMD_LEN—Offset B914h" on page 264	00000000h
B918–B91Bh	4	"MIPIC_RD_DATA_RETURN0—Offset B918h" on page 265	00000000h
B91C–B91Fh	4	"MIPIC_RD_DATA_RETURN1—Offset B91Ch" on page 265	00000000h
B920–B923h	4	"MIPIC_RD_DATA_RETURN2—Offset B920h" on page 266	00000000h
B924–B927h	4	"MIPIC_RD_DATA_RETURN3—Offset B924h" on page 266	00000000h
B928–B92Bh	4	"MIPIC_RD_DATA_RETURN4—Offset B928h" on page 267	00000000h



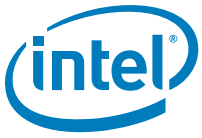
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
B92C–B92Fh	4	"MIPIC_RD_DATA_RETURN5—Offset B92Ch" on page 267	00000000h
B930–B933h	4	"MIPIC_RD_DATA_RETURN6—Offset B930h" on page 268	00000000h
B934–B937h	4	"MIPIC_RD_DATA_RETURN7—Offset B934h" on page 268	00000000h
B938–B93Bh	4	"MIPIC_RD_DATA_VALID—Offset B938h" on page 269	00000000h
C000–C003h	4	"DPALETTE_C—Offset C000h" on page 269	00000000h
60000–60003h	4	"HTOTAL_A—Offset 60000h" on page 270	00000000h
60004–60007h	4	"HBLANK_A—Offset 60004h" on page 271	00000000h
60008–6000Bh	4	"HSYNC_A—Offset 60008h" on page 273	00000000h
6000C–6000Fh	4	"VTOTAL_A—Offset 6000Ch" on page 274	00000000h
60010–60013h	4	"VBLANK_A—Offset 60010h" on page 275	00000000h
60014–60017h	4	"VSYNC_A—Offset 60014h" on page 276	00000000h
6001C–6001Fh	4	"PIPESRCA—Offset 6001Ch" on page 277	00000000h
60020–60023h	4	"BCLRPAT_A—Offset 60020h" on page 279	00000000h
60028–6002Bh	4	"VSYNCSHIFT_A—Offset 60028h" on page 279	00000000h
60030–60033h	4	"TRANSADATAM1—Offset 60030h" on page 280	7E000000h
60034–60037h	4	"TRANSADATAN1—Offset 60034h" on page 281	00000000h
60038–6003Bh	4	"TRANSADATAM2—Offset 60038h" on page 282	7E000000h
6003C–6003Fh	4	"TRANSADATAN2—Offset 6003Ch" on page 282	00000000h
60040–60043h	4	"TRANSADPLINKM1—Offset 60040h" on page 283	00000000h
60044–60047h	4	"TRANSADPLINKN1—Offset 60044h" on page 284	00000000h
60048–6004Bh	4	"TRANSADPLINKM2—Offset 60048h" on page 284	00000000h
6004C–6004Fh	4	"TRANSADPLINKN2—Offset 6004Ch" on page 285	00000000h
60050–60053h	4	"CRCCTRLREDA—Offset 60050h" on page 285	00000000h
60054–60057h	4	"CRCCTRLGREENA—Offset 60054h" on page 286	00000000h
60058–6005Bh	4	"CRCCTRLBLUEA—Offset 60058h" on page 287	00000000h
6005C–6005Fh	4	"CRCCTRLALPHAA—Offset 6005Ch" on page 288	00000000h
60060–60063h	4	"CRCRESREDA—Offset 60060h" on page 288	00000000h
60064–60067h	4	"CRCRESGREENA—Offset 60064h" on page 289	00000000h
60068–6006Bh	4	"CRCRESBLUEA—Offset 60068h" on page 290	00000000h
6006C–6006Fh	4	"CRCRESALPHAA—Offset 6006Ch" on page 291	00000000h
60070–60073h	4	"CRCCTRLRESIDUE2A—Offset 60070h" on page 292	00000000h
60080–60083h	4	"CRCRESRESIDUE2A—Offset 60080h" on page 293	00000000h
60090–60093h	4	"PSRCTLA—Offset 60090h" on page 293	00000000h
60094–60097h	4	"PSRSTATA—Offset 60094h" on page 295	00000000h
60098–6009Bh	4	"PSRCRC1A—Offset 60098h" on page 296	00000000h
6009C–6009Fh	4	"PSRCRC2A—Offset 6009Ch" on page 297	00000000h
600A0–600A3h	4	"VSCSDPA—Offset 600A0h" on page 298	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
600B0–600B3h	4	"PIPEAWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS—Offset 600B0h" on page 299	00000000h
600B4–600B7h	4	"PIPEAWIDEGAMUTCOLORCORRECTIONC02COEFFICIENT—Offset 600B4h" on page 300	00000000h
600B8–600BBh	4	"PIPEAWIDEGAMUTCOLORCORRECTIONC11_C10COEFFICIENTS—Offset 600B8h" on page 300	00000000h
600BC–600BFh	4	"PIPEAWIDEGAMUTCOLORCORRECTIONC12COEFFICIENT—Offset 600BCh" on page 301	00000000h
600C0–600C3h	4	"PIPEAWIDEGAMUTCOLORCORRECTIONC21_C20COEFFICIENTS—Offset 600C0h" on page 301	00000000h
600C4–600C7h	4	"PIPEAWIDEGAMUTCOLORCORRECTIONC22COEFFICIENT—Offset 600C4h" on page 302	00000000h
60100–60103h	4	"DISPLAY_PHY_CONTROL_REGISTER (DISPLAY_PHY_CONTROL_REGISTER1)—Offset 60100h" on page 303	00000000h
60104–60107h	4	"DISPLAY_PHY_STATUS_REGISTER1—Offset 60104h" on page 305	00000000h
60108–6010Bh	4	"DISPLAY_PHY_GPIO_DATA_REGISTER—Offset 60108h" on page 306	00000000h
6010C–6010Fh	4	"DISPLAY_PHY_STATUS_REGISTER2—Offset 6010Ch" on page 306	00000000h
60200–60203h	4	"VIDEO_DIP_CTL_A—Offset 60200h" on page 307	20200900h
60208–6020Bh	4	"VIDEO_DIP_DATA_A—Offset 60208h" on page 309	00000000h
60210–60213h	4	"VIDEO_DIP_GDCP_PAYLOAD_A—Offset 60210h" on page 310	00000000h
60A04–60A07h	4	"CANVAS_A—Offset 60A04h" on page 311	00000000h
60A08–60A0Bh	4	"PRIMPOS_A—Offset 60A08h" on page 311	00000000h
60A0C–60A0Fh	4	"PRIMSIZE_A—Offset 60A0Ch" on page 312	00000000h
60A10–60A13h	4	"PRIMA_CONSTANT—Offset 60A10h" on page 313	00000000h
61000–61003h	4	"HTOTAL_B—Offset 61000h" on page 314	00000000h
61004–61007h	4	"HBLANK_B—Offset 61004h" on page 315	00000000h
61008–6100Bh	4	"HSYNC_B—Offset 61008h" on page 315	00000000h
6100C–6100Fh	4	"VTOTAL_B—Offset 6100Ch" on page 316	00000000h
61010–61013h	4	"VBLANK_B—Offset 61010h" on page 317	00000000h
61014–61017h	4	"VSYNC_B—Offset 61014h" on page 318	00000000h
6101C–6101Fh	4	"PIPEBSRC—Offset 6101Ch" on page 319	00000000h
61020–61023h	4	"BCLRPAT_B—Offset 61020h" on page 320	00000000h
61028–6102Bh	4	"VSYNCSHIFT_B—Offset 61028h" on page 320	00000000h
61030–61033h	4	"TRANSBDATAM1—Offset 61030h" on page 321	7E000000h
61034–61037h	4	"TRANSBDATAN1—Offset 61034h" on page 322	00000000h
61038–6103Bh	4	"TRANSBDATAM2—Offset 61038h" on page 323	7E000000h

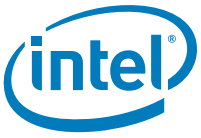


Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
6103C–6103Fh	4	"TRANSBDATAN2—Offset 6103Ch" on page 323	00000000h
61040–61043h	4	"TRANSBDPLINKM1—Offset 61040h" on page 324	00000000h
61044–61047h	4	"TRANSBDPLINKN1—Offset 61044h" on page 325	00000000h
61048–6104Bh	4	"TRANSBDPLINKM2—Offset 61048h" on page 325	00000000h
6104C–6104Fh	4	"TRANSBDPLINKN2—Offset 6104Ch" on page 326	00000000h
61050–61053h	4	"CRCCTRLREDB—Offset 61050h" on page 326	00000000h
61054–61057h	4	"CRCCTRLGREENB—Offset 61054h" on page 327	00000000h
61058–6105Bh	4	"CRCCTRLBLUEB—Offset 61058h" on page 328	00000000h
6105C–6105Fh	4	"CRCCTRLALPHAB—Offset 6105Ch" on page 329	00000000h
61060–61063h	4	"CRCRESREDB—Offset 61060h" on page 329	00000000h
61064–61067h	4	"CRCRESGREENB—Offset 61064h" on page 330	00000000h
61068–6106Bh	4	"CRCRESBLUEB—Offset 61068h" on page 331	00000000h
6106C–6106Fh	4	"CRCRESALPHAB—Offset 6106Ch" on page 332	00000000h
61070–61073h	4	"CRCCTRLRESIDUE2B—Offset 61070h" on page 333	00000000h
61080–61083h	4	"CRCRESRESIDUAL2B—Offset 61080h" on page 334	00000000h
61090–61093h	4	"PSRCTLB—Offset 61090h" on page 334	00000000h
61094–61097h	4	"PSRSTATB—Offset 61094h" on page 336	00000000h
61098–6109Bh	4	"PSRCRC1B—Offset 61098h" on page 337	00000000h
6109C–6109Fh	4	"PSRCRC2B—Offset 6109Ch" on page 338	00000000h
610A0–610A3h	4	"VSCSDPB—Offset 610A0h" on page 339	00000000h
610B0–610B3h	4	"PIPEBWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS—Offset 610B0h" on page 340	00000000h
610B4–610B7h	4	"PIPEBWIDEGAMUTCOLORCORRECTIONC02COEFFICIENT—Offset 610B4h" on page 341	00000000h
610B8–610BBh	4	"PIPEBWIDEGAMUTCOLORCORRECTIONC11_C10COEFFICIENTS—Offset 610B8h" on page 341	00000000h
610BC–610BFh	4	"PIPEBWIDEGAMUTCOLORCORRECTIONC12COEFFICIENT—Offset 610BCh" on page 342	00000000h
610C0–610C3h	4	"PIPEBWIDEGAMUTCOLORCORRECTIONC21_C20COEFFICIENTS—Offset 610C0h" on page 342	00000000h
610C4–610C7h	4	"PIPEBWIDEGAMUTCOLORCORRECTIONC22COEFFICIENT—Offset 610C4h" on page 343	00000000h
61100–61103h	4	"ADPA—Offset 61100h" on page 344	00040000h
61104–61107h	4	"CRTIO_DFX—Offset 61104h" on page 346	00008000h
61110–61113h	4	"PORT_HOTPLUG_EN—Offset 61110h" on page 347	00000020h
61114–61117h	4	"PORT_HOTPLUG_STAT—Offset 61114h" on page 350	00000000h
61120–61123h	4	"HDP_LONG_VALUE_REGISTER—Offset 61120h" on page 355	00000000h

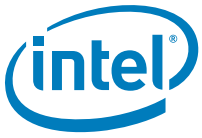
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
61124–61127h	4	"HDP_FILTER_VALUE_REGISTER—Offset 61124h" on page 356	00000000h
61140–61143h	4	"SDVOHDMIB—Offset 61140h" on page 357	00000018h
61154–61157h	4	"SDVOHDMIB—Offset 61140h" on page 357	00000000h
61160–61163h	4	"HDMIC—Offset 61160h" on page 362	00000018h
61164–61167h	4	"DISPLAY_DIGITAL_PORT_HOT_PLUG_CONTROL_REGISTER—Offset 61164h" on page 366	00000000h
61168–6116Bh	4	"DV_DETERM—Offset 61168h" on page 369	00000000h
6116C–6116Fh	4	"HDMID—Offset 6116Ch" on page 371	00000018h
61170–61173h	4	"VIDEO_DIP_CTL_B—Offset 61170h" on page 375	20200900h
61174–61177h	4	"VIDEO_DIP_DATA_B—Offset 61174h" on page 377	00000000h
61178–6117Bh	4	"VIDEO_DIP_GDCP_PAYLOAD_B—Offset 61178h" on page 377	00000000h
61190–61193h	4	"MIPIA_PORT_CTRL—Offset 61190h" on page 378	00800000h
61198–6119Bh	4	"DPA_PIX_GEN_CTRL—Offset 61198h" on page 381	00000000h
611B0–611B3h	4	"DPB_PIX_GEN_CTRL—Offset 611B0h" on page 383	00000000h
611D0–611D3h	4	"DPC_PIX_GEN_CTRL—Offset 611D0h" on page 385	00000000h
611F0–611F3h	4	"VIDEO_DIP_CTL_C—Offset 611F0h" on page 387	20200900h
611F4–611F7h	4	"VIDEO_DIP_DATA_C—Offset 611F4h" on page 388	00000000h
611F8–611FBh	4	"VIDEO_DIP_GDCP_PAYLOAD_C—Offset 611F8h" on page 389	00000000h
61200–61203h	4	"PIPEA_PP_STATUS—Offset 61200h" on page 389	08000000h
61204–61207h	4	"PIPEA_PP_CONTROL—Offset 61204h" on page 391	00000000h
61208–6120Bh	4	"PIPEA_PP_ON_DELAYS—Offset 61208h" on page 393	00000000h
6120C–6120Fh	4	"PIPEA_PP_OFF_DELAYS—Offset 6120Ch" on page 394	00000000h
61210–61213h	4	"PIPEA_PP_DIVISOR—Offset 61210h" on page 395	00270F04h
61230–61233h	4	"PFIT_CONTROL—Offset 61230h" on page 396	20000000h
61234–61237h	4	"PFIT_PGM_RATIOS—Offset 61234h" on page 398	00000000h
61238–6123Bh	4	"RESERVEDUSEDTOBEAUTOSCALINGRATIOSREADBACK—Offset 61238h" on page 399	00000000h
6123C–6123Fh	4	"RESERVEDUSEDTOBESCALINGINITIALPHASE—Offset 6123Ch" on page 400	00000000h
61250–61253h	4	"PIPEA_BLC_PWM_CLT2—Offset 61250h" on page 400	00000000h
61254–61257h	4	"PIPEA_BLC_PWM_CTL—Offset 61254h" on page 401	00000000h
61260–61263h	4	"PIPEA_BLM_HIST_CTL—Offset 61260h" on page 402	00000000h
61264–61267h	4	"PIPEA_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER—Offset 61264h" on page 404	00000000h
61268–6126Bh	4	"PIPEAHISTOGRAMTHRESHOLDGUARDBANDREGISTER—Offset 61268h" on page 405	00000000h



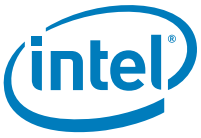
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
61300–61303h	4	"PIPEB_PP_STATUS—Offset 61300h" on page 406	08000000h
61304–61307h	4	"PIPEB_PP_CONTROL—Offset 61304h" on page 408	00000000h
61308–6130Bh	4	"PIPEB_PP_ON_DELAYS—Offset 61308h" on page 410	00000000h
6130C–6130Fh	4	"PIPEB_PP_OFF_DELAYS—Offset 6130Ch" on page 411	00000000h
61310–61313h	4	"PIPEB_PP_DIVISOR—Offset 61310h" on page 412	00270F04h
61350–61353h	4	"PIPEB_BLC_PWM_CLT2—Offset 61350h" on page 413	00000000h
61354–61357h	4	"PIPEB_BLC_PWM_CTL—Offset 61354h" on page 415	00000000h
61360–61363h	4	"PIPEB_BLM_HIST_CTL—Offset 61360h" on page 416	00000000h
61364–61367h	4	"PIPEB_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER—Offset 61364h" on page 417	00000000h
61368–6136Bh	4	"PIPEBHISTOGRAMTHRESHOLDGUARDBANDREGISTER—Offset 61368h" on page 418	00000000h
61700–61703h	4	"MIPIC_PORT_CTRL—Offset 61700h" on page 419	00000000h
61704–61707h	4	"MIPIC_TEARING_CTR—Offset 61704h" on page 421	00000000h
61900–61903h	4	"PIPEC_PP_STATUS—Offset 61900h" on page 422	08000000h
61904–61907h	4	"PIPEC_PP_CONTROL—Offset 61904h" on page 424	00000000h
61908–6190Bh	4	"PIPEC_PP_ON_DELAYS—Offset 61908h" on page 426	00000000h
6190C–6190Fh	4	"PIPEC_PP_OFF_DELAYS—Offset 6190Ch" on page 427	00000000h
61910–61913h	4	"PIPEC_PP_DIVISOR—Offset 61910h" on page 428	00270F04h
61A00–61A03h	4	"BLEND_B—Offset 61A00h" on page 429	00000000h
61A04–61A07h	4	"CANVAS_B—Offset 61A04h" on page 430	00000000h
61A08–61A0Bh	4	"PRIMPOS_B—Offset 61A08h" on page 431	00000000h
61A0C–61A0Fh	4	"PRIMSIZE_B—Offset 61A0Ch" on page 432	00000000h
61A10–61A13h	4	"PRIMB_CONSTANT—Offset 61A10h" on page 432	00000000h
62000–62003h	4	"AUD_CONFIG_A—Offset 62000h" on page 433	00000000h
62010–62013h	4	"AUD_MISC_CTRL_A—Offset 62010h" on page 435	00000044h
62020–62023h	4	"AUD_VID_DID—Offset 62020h" on page 437	80862882h
62024–62027h	4	"AUD_RID—Offset 62024h" on page 437	00100000h
62028–6202Bh	4	"AUD_CTS_ENABLE_A—Offset 62028h" on page 438	00000000h
6204C–6204Fh	4	"AUD_PWRST—Offset 6204Ch" on page 439	00FFFFFFh
62050–62053h	4	"AUD_HDMIW_HDMIEDID_A—Offset 62050h" on page 442	00000000h
62054–62057h	4	"AUD_HDMIW_INFOFR_A—Offset 62054h" on page 442	00000000h
6207C–6207Fh	4	"AUD_PORT_EN_HD_CFG—Offset 6207Ch" on page 443	00077003h
62080–62083h	4	"AUD_OUT_DIG_CNVT_A—Offset 62080h" on page 445	00000000h
62084–62087h	4	"AUD_OUT_STR_DESC_A—Offset 62084h" on page 447	00000032h
62088–6208Bh	4	"AUD_OUT_CH_STR—Offset 62088h" on page 448	00000000h
620A8–620ABh	4	"AUD_PINW_CONNLNG_LIST—Offset 620A8h" on page 450	00030202h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
620AC–620AFh	4	"AUD_PINW_CONNLNG_SEL—Offset 620ACh" on page 450	00000000h
620B4–620B7h	4	"AUD_CNTL_ST_A—Offset 620B4h" on page 451	00005400h
620C0–620C3h	4	"AUD_CNTL_ST2—Offset 620C0h" on page 453	00000000h
620D4–620D7h	4	"AUD_HDMIW_STATUS—Offset 620D4h" on page 455	00000000h
62100–62103h	4	"AUD_CONFIG_B—Offset 62100h" on page 456	00000000h
62110–62113h	4	"AUD_MISC_CTRL_B—Offset 62110h" on page 458	00000044h
62128–6212Bh	4	"AUD_CTS_ENABLE_B—Offset 62128h" on page 459	00000000h
62150–62153h	4	"AUD_HDMIW_HDMIEDID_B—Offset 62150h" on page 460	00000000h
62154–62157h	4	"AUD_HDMIW_INFOFR_B—Offset 62154h" on page 460	00000000h
62180–62183h	4	"AUD_OUT_DIG_CNVT_B—Offset 62180h" on page 461	00000000h
62184–62187h	4	"AUD_OUT_STR_DESC_B—Offset 62184h" on page 462	00000032h
621B4–621B7h	4	"AUD_CNTL_ST_B—Offset 621B4h" on page 464	00005400h
62200–62203h	4	"AUD_CONFIG_C—Offset 62200h" on page 466	00000000h
62210–62213h	4	"AUD_MISC_CTRL_C—Offset 62210h" on page 468	00000044h
62228–6222Bh	4	"AUD_CTS_ENABLE_C—Offset 62228h" on page 469	00000000h
62250–62253h	4	"AUD_HDMIW_HDMIEDID_C—Offset 62250h" on page 470	00000000h
62254–62257h	4	"AUD_HDMIW_INFOFR_C—Offset 62254h" on page 470	00000000h
62280–62283h	4	"AUD_OUT_DIG_CNVT_C—Offset 62280h" on page 471	00000000h
62284–62287h	4	"AUD_OUT_STR_DESC_C—Offset 62284h" on page 472	00000032h
622B4–622B7h	4	"AUD_CNTL_ST_B (AUD_CNTL_ST_C)—Offset 622B4h" on page 474	00005400h
62F00–62F03h	4	"AUD_SSID_DBG—Offset 62F00h" on page 476	80860101h
62F04–62F07h	4	"AUD_PWST1_DBG—Offset 62F04h" on page 477	00000C0Fh
62F08–62F0Bh	4	"AUD_OUT_STR_DESC_A_DBG—Offset 62F08h" on page 478	00000032h
62F0C–62F0Fh	4	"AUD_OUT_DIG_CNVT_A_DBG—Offset 62F0Ch" on page 480	00000001h
62F14–62F17h	4	"AUD_PWST2_DBG—Offset 62F14h" on page 482	0000000Fh
62F18–62F1Bh	4	"AUD_OUT_STR_DESC_B_DBG—Offset 62F18h" on page 483	00000032h
62F1C–62F1Fh	4	"AUD_OUT_DIG_CNVT_B_DBG—Offset 62F1Ch" on page 484	00000001h
62F20–62F23h	4	"AUD_PORT_EN_B_DBG—Offset 62F20h" on page 486	00000003h
62F24–62F27h	4	"AUD_PWST3_DBG—Offset 62F24h" on page 488	00000003h
62F28–62F2Bh	4	"AUD_PORT_EN_C_DBG—Offset 62F28h" on page 488	00000003h
62F2C–62F2Fh	4	"AUD_PORT_EN_D_DBG—Offset 62F2Ch" on page 490	00000003h
62F38–62F3Bh	4	"AUD_CHICKENBIT_REG—Offset 62F38h" on page 491	00000001h
62F40–62F43h	4	"AUD_OUT_DIG_CNVTA_DBG—Offset 62F40h" on page 492	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
62F44–62F47h	4	"AUD_OUT_DIG_CNVTB_DBG—Offset 62F44h" on page 493	00000000h
62F60–62F63h	4	"AUD_CNTL_ST_B_DBG—Offset 62F60h" on page 493	00000000h
62F64–62F67h	4	"AUD_HDMIW_INFOFR_B_DBG—Offset 62F64h" on page 495	00000000h
62F70–62F73h	4	"AUD_CNTL_ST_C_DBG—Offset 62F70h" on page 495	00000000h
62F74–62F77h	4	"AUD_HDMIW_INFOFR_C_DBG—Offset 62F74h" on page 497	00000000h
62F80–62F83h	4	"AUD_CNTL_ST_D_DBG—Offset 62F80h" on page 497	00000000h
62F84–62F87h	4	"AUD_HDMIW_INFOFR_D_DBG—Offset 62F84h" on page 499	00000000h
62F88–62F8Bh	4	"AUD_CONFIG_DEFAULT2_REG_PORTB—Offset 62F88h" on page 499	00000000h
62F8C–62F8Fh	4	"AUD_CONFIG_DEFAULT2_REG_PORTC—Offset 62F8Ch" on page 500	00000000h
62F90–62F93h	4	"AUD_CONFIG_DEFAULT2_REG_PORTD—Offset 62F90h" on page 500	00000000h
62F94–62F97h	4	"AUD_MCTSA—Offset 62F94h" on page 500	00000000h
62F98–62F9Bh	4	"AUD_MCTSB—Offset 62F98h" on page 501	00000000h
62F9C–62F9Fh	4	"AUD_MCTSC—Offset 62F9Ch" on page 502	00000000h
63000–63003h	4	"HTOTAL_C—Offset 63000h" on page 503	00000000h
63004–63007h	4	"HBLANK_C—Offset 63004h" on page 504	00000000h
63008–6300Bh	4	"HSYNC_C—Offset 63008h" on page 505	00000000h
6300C–6300Fh	4	"VTOTAL_C—Offset 6300Ch" on page 506	00000000h
63010–63013h	4	"VBLANK_C—Offset 63010h" on page 507	00000000h
63014–63017h	4	"VSYNC_C—Offset 63014h" on page 508	00000000h
6301C–6301Fh	4	"PIPECSRC—Offset 6301Ch" on page 509	00000000h
63020–63023h	4	"BCLRPAT_C—Offset 63020h" on page 510	00000000h
63028–6302Bh	4	"VSYNCSHIFT_C—Offset 63028h" on page 510	00000000h
63030–63033h	4	"TRANSCDATAM1—Offset 63030h" on page 511	7E000000h
63034–63037h	4	"TRANSCDATAN1—Offset 63034h" on page 512	00000000h
63038–6303Bh	4	"TRANSCDATAM2—Offset 63038h" on page 513	7E000000h
6303C–6303Fh	4	"TRANSCDATAN2—Offset 6303Ch" on page 513	00000000h
63040–63043h	4	"TRANSCDPLINKM1—Offset 63040h" on page 514	00000000h
63044–63047h	4	"TRANSCDPLINKN1—Offset 63044h" on page 515	00000000h
63048–6304Bh	4	"TRANSCDPLINKM2—Offset 63048h" on page 515	00000000h
6304C–6304Fh	4	"TRANSCDPLINKN2—Offset 6304Ch" on page 516	00000000h



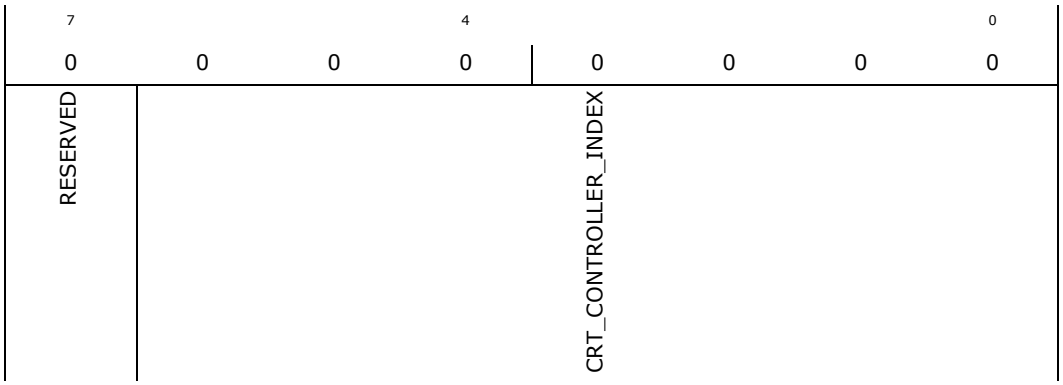
4.2.1 CRX (CRX_MDA)—Offset 3B4h

CRT Controller Index Register

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits) **Offset:** 3B4h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**RESERVED:** Read as 0.
6:0	0x0 RW	**CRT_CONTROLLER_INDEX:** These 7 bits are used to select any one of the CRT controller registers to be accessed via the data port at I/O location 3B5h or 3D5h, depending upon whether the graphics system is configured for MDA or CGA emulation. The data port memory address offsets are 3B5h/3D5h.

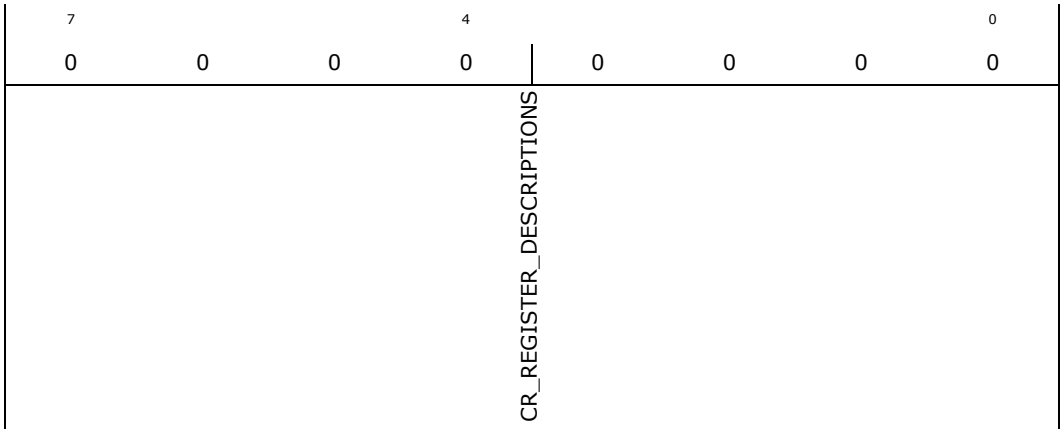
4.2.2 CR (CR_MDA)—Offset 3B5h

CR index registers

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits) **Offset:** 3B5h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**CR_REGISTER_DESCRIPTIONS:** CR indexed register descriptions

4.2.3 ARX—Offset 3C0h

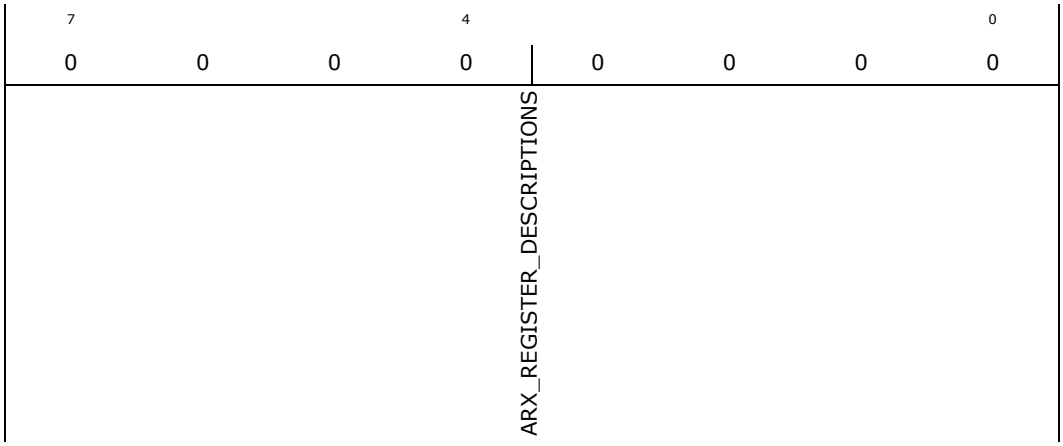
Attribute Controller Index Register. Includes the 22 registers that share this offset (with different indexes). -enum ARX_e

Access Method

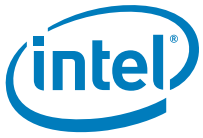
Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: 3C0h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ARX_REGISTER_DESCRIPTIONS:** ARX indexed register descriptions



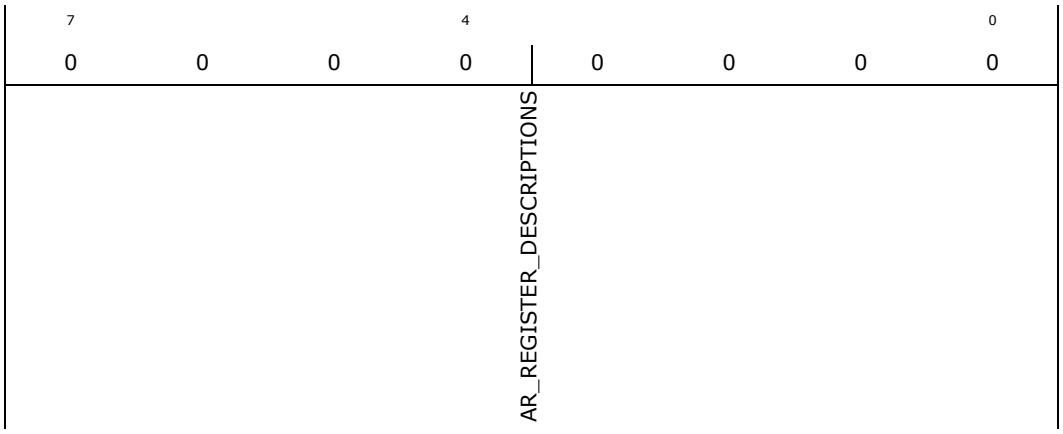
4.2.4 AR—Offset 3C1h

AR index registers. Includes the 21 registers that share this offset (with different indexes.) -enum AR_e- in this document will lead to register definitions

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits) **Offset:** 3C1h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**AR_REGISTER_DESCRIPTIONS:** AR indexed register descriptions

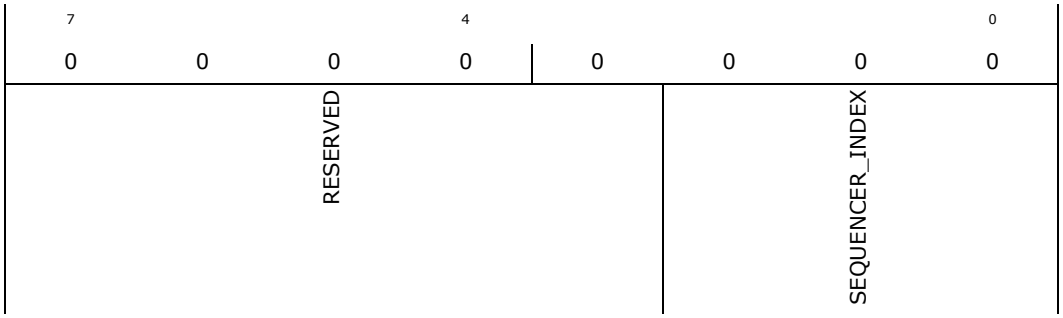
4.2.5 SRX—Offset 3C4h

Sequencer Index

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits) **Offset:** 3C4h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0x0 RO	**RESERVED:** Read as 0s.
2:0	0x0 RW	**SEQUENCER_INDEX:** This field contains a 3-bit Sequencer Index value used to access sequencer data registers at indices 0 through 7.

4.2.6 SR—Offset 3C5h

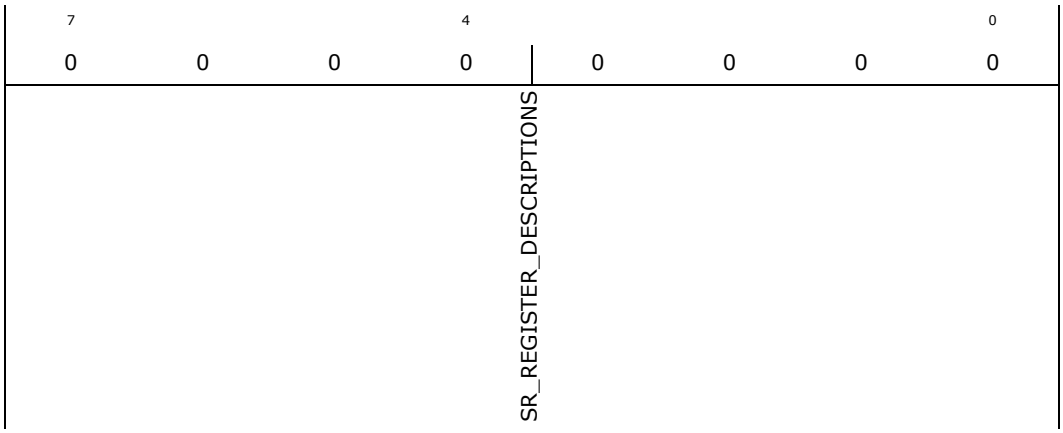
SR index registers

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: 3C5h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**SR_REGISTER_DESCRIPTIONS:** SR indexed register descriptions

4.2.7 DACMASK—Offset 3C6h

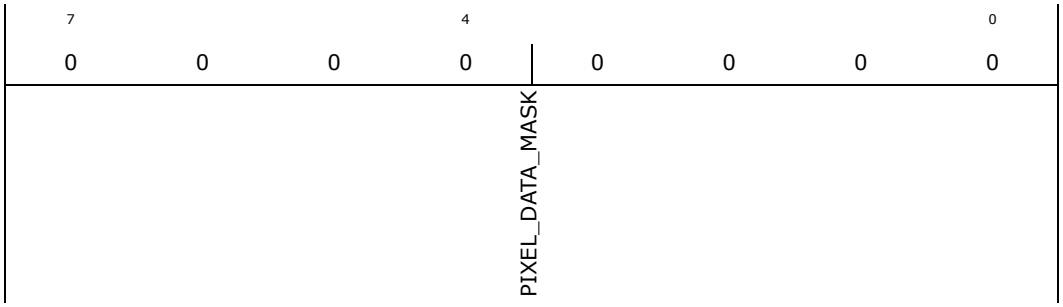
Pixel Data Mask Register

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: 3C6h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**PIXEL_DATA_MASK:** In indexed-color mode, the 8 bits of this register are logically ANDed with the 8 bits of pixel data received from the frame buffer for each pixel. The result of this ANDing process becomes the actual index used to select color data positions within the palette. This has the effect of limiting the choice of color data positions that may be specified by the incoming 8-bit data. 0 = Corresponding bit in the resulting 8-bit index being forced to 0. 1 = Allows the corresponding bit in the resulting index to reflect the actual value of the corresponding bit in the incoming 8-bit pixel data.

4.2.8 DACWX—Offset 3C8h

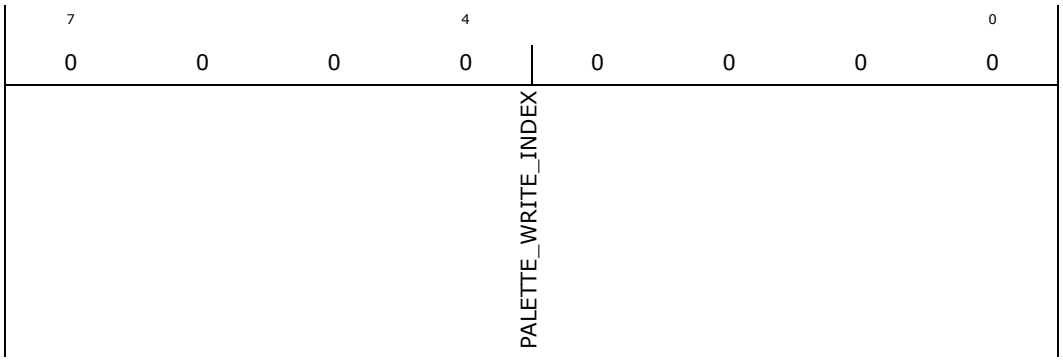
Palette Write Index Register

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: 3C8h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 WO	**PALETTE_WRITE_INDEX:** The 8-bit index value programmed into this register chooses which of 256 standard color data positions within the palette are to be made accessible for being written via the Palette Data Register (DACDATA). The index value held in this register is automatically incremented when all three bytes of the color data position selected by the current index have been written. This register allows access to the palette even when running on display modes.

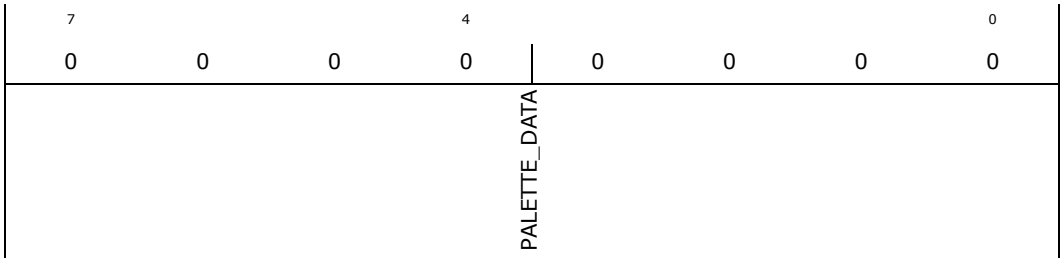
4.2.9 DACDATA—Offset 3C9h

Palette Data Register

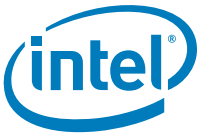
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits) **Offset:** 3C9h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**PALETTE_DATA:** This byte-wide data port provides read or write access to the three bytes of data of each color data position selected using the Palette Read Index Register (DACRX) or the Palette Write Index Register (DACWX). The three bytes in each color data position are read or written in three successive read or write operations. The first byte read or written specifies the intensity of the red component of the color specified in the selected color data position. The second byte is for the green component, and the third byte is for the blue component. When writing data to a color data position, all three bytes must be written before the hardware will actually update the three bytes of the selected color data position. When reading or writing to a color data position, ensure that neither the Palette Read Index Register (DACRX) or the Palette Write Index Register (DACWX) are written to before all three bytes are read or written. A write to either of these two registers causes the circuitry that automatically cycles through providing access to the bytes for red, green and blue components to be reset such that the byte for the red component is the one that will be accessed by the next read or write operation via this register. This register allows access to the palette even when running display modes. Writes to the palette can cause sparkle if not done during inactive video periods. This sparkle is caused by an attempt to write and read the same address on the same cycle. Anti-sparkle circuits will substitute the previous pixel value for the read output.



4.2.10 FCR (FCR_Read)—Offset 3CAh

Feature Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits) **Offset:** 3CAh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RESERVED				VSYNC_CONTROL	RESERVED_1		

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RO	**RESERVED:** Read as 0.
3	0x0 RW	**VSYNC_CONTROL:** This bit is provided for compatibility only and has no other function. Reads and writes to this bit have no effect other than to change the value of this bit. The previous definition of this bit selected the output on the VSYNC pin. 0 = Was used to set VSYNC out put on the VSYNC pin (default). 1 = Was used to set the log i cal 'OR' of VSYNC and Display Enable output on the VSYNC pin. This capability was not typically very useful..
2:0	0x0 RO	**RESERVED_1:** Read as 0.

4.2.11 MSR (MSR_READ)—Offset 3CCh

Miscellaneous Output

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits) **Offset:** 3CCh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CRT_VSYNC_POLARITY	CRT_HSYNC_POLA_RITY	PAGE_SELECT	RESERVED	CLOCK_SELECT		A0000_BFFFFH_MEMORY_ACCESS_ENABLE	I_O_ADDRESS_SELECT

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**PAGE_SELECT:** In Odd/Even Memory Map Mode 1 (GR6), this bit selects the upper or lower 64 KB page in dis play memory for CPU access: 0 = Upper page (default) 1 = Lower page.
4	0x0 RO	**RESERVED:** Read as 0.
0	0x0 RW	**I_O_ADDRESS_SELECT:** This bit selects 3Bxh or 3Dxh as the I/O address for the CRT Controller registers, the Feature Control Register (FCR), and Input Status Register 1 (ST01). Presently ignored (whole range is claimed), but will ignore 3Bx for color configuration or 3Dx for monochrome. Note that it is typical in AGP chipsets to shadow this bit and properly steer I/O cycles to the proper bus for operation where a MDA exists on another bus such as ISA. 0 = Select 3Bxh I/O address (MDA emulation) (default). 1 = Select 3Dxh I/O address (CGA emulation).

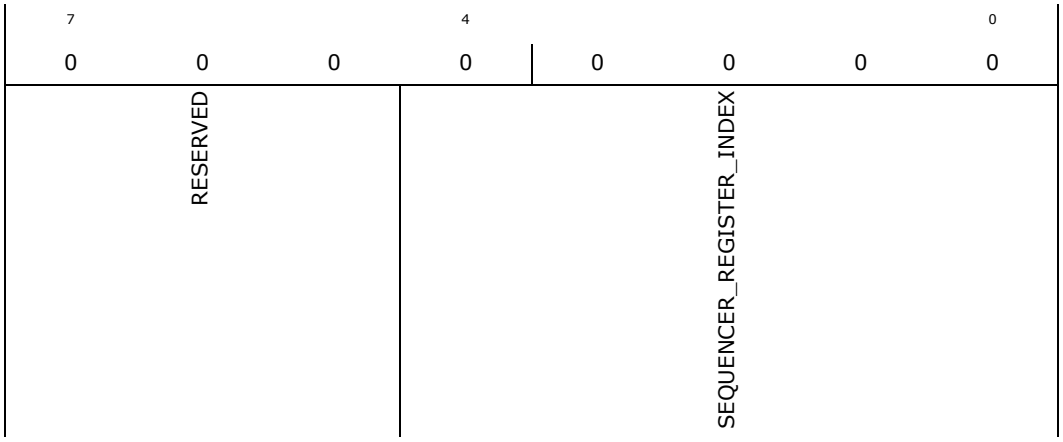
4.2.12 GRX—Offset 3CEh

GRX Graphics Controller Index Register

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits) **Offset:** 3CEh

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:5	0x0 RO	**RESERVED:** Read as 0.
4:0	0x0 RW	**SEQUENCER_REGISTER_INDEX:** This field selects any one of the graphics controller registers (GR00-GR11]) to be accessed via the data port at I/O (or memory offset) location 3CFh.

4.2.13 GR—Offset 3CFh

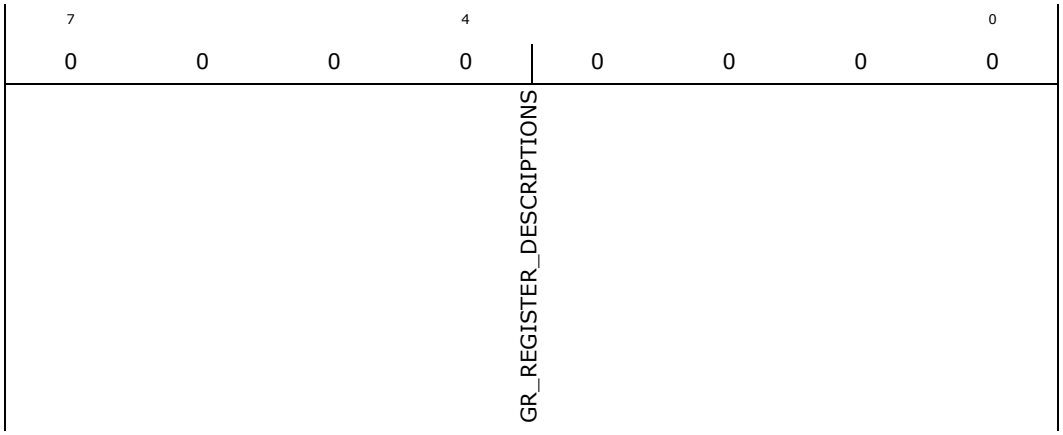
GR index registers

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: 3CFh

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**GR_REGISTER_DESCRIPTIONS:** GR indexed register descriptions

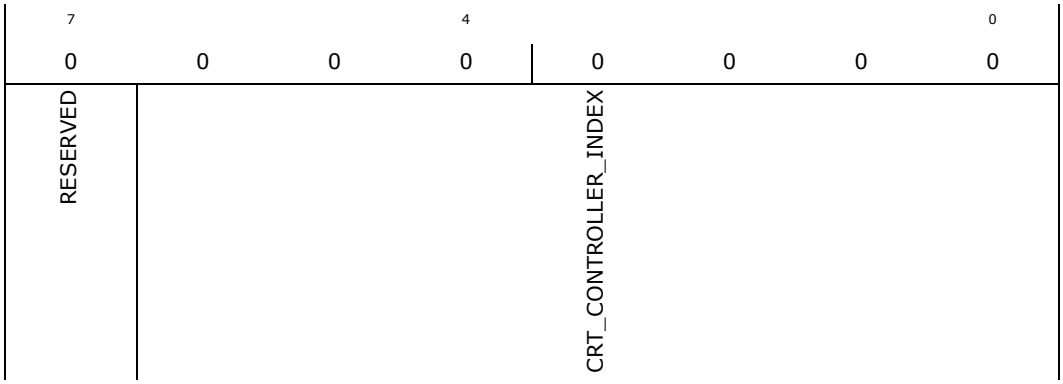
4.2.14 CRX (CRX_CGA)—Offset 3D4h

CRT Controller Index Register

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits) **Offset:** 3D4h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**RESERVED:** Read as 0.
6:0	0x0 RW	**CRT_CONTROLLER_INDEX:** These 7 bits are used to select any one of the CRT controller registers to be accessed via the data port at I/O location 3B5h or 3D5h, depending upon whether the graphics system is configured for MDA or CGA emulation. The data port memory address offsets are 3B5h/3D5h.

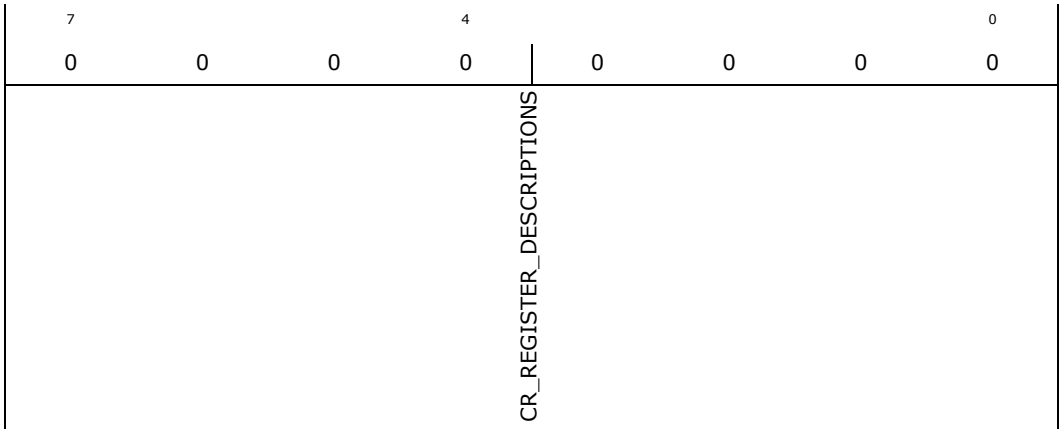
4.2.15 CR (CR_CGA)—Offset 3D5h

CR index registers

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits) **Offset:** 3D5h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**CR_REGISTER_DESCRIPTIONS:** CR indexed register descriptions

4.2.16 GPIOCTL_0—Offset 5010h

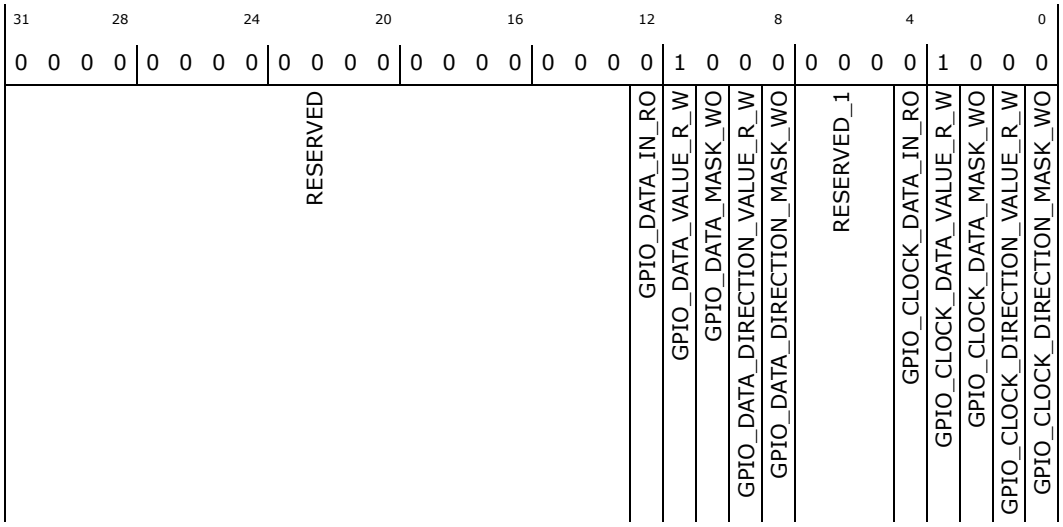
GPIO Control Registers GPIO I2C register (gmbus_register.v reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

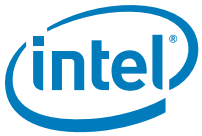
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 5010h

Default: 00000808h





Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RESERVED:** Reserved.
12	0x0 RO	**GPIO_DATA_IN_RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
11	0x1 RW	**GPIO_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
10	0x0 WO	**GPIO_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only
9	0x0 RW	**GPIO_DATA_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	0x0 WO	**GPIO_DATA_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	0x0 RO	**RESERVED_1:** must be written with zeros.
4	0x0 RO	**GPIO_CLOCK_DATA_IN_RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
3	0x1 RW	**GPIO_CLOCK_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 WO	**GPIO_CLOCK_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	0x0 RW	**GPIO_CLOCK_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.
0	0x0 WO	**GPIO_CLOCK_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

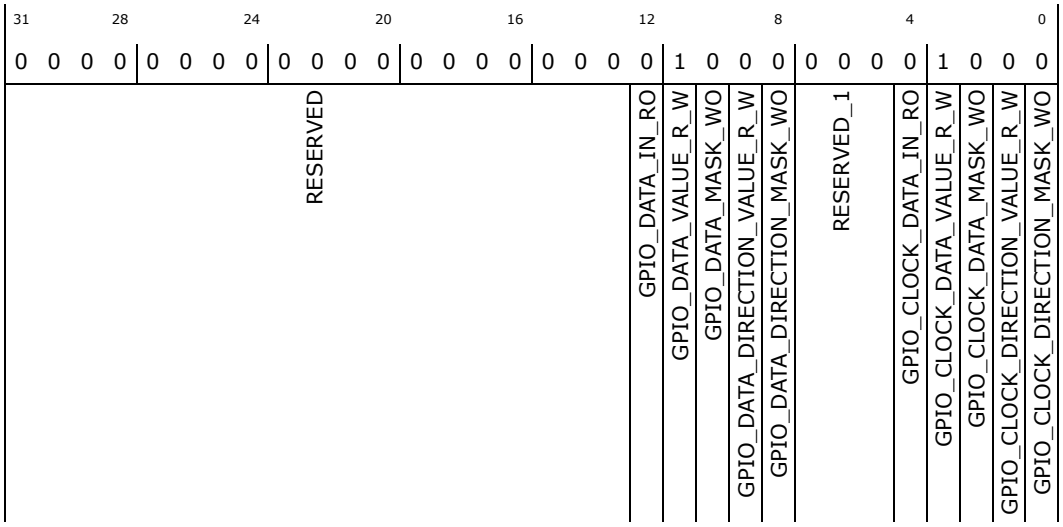
4.2.17 GPIOCTL_1—Offset 5014h

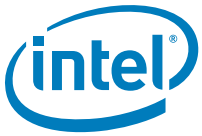
GPIO Control Registers GPIO I2C register (gmbus_register.v reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 5014h

Default: 00000808h





Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RESERVED:** Reserved.
12	0x0 RO	**GPIO_DATA_IN_RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
11	0x1 RW	**GPIO_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
10	0x0 WO	**GPIO_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only
9	0x0 RW	**GPIO_DATA_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	0x0 WO	**GPIO_DATA_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	0x0 RO	**RESERVED_1:** must be written with zeros.
4	0x0 RO	**GPIO_CLOCK_DATA_IN_RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
3	0x1 RW	**GPIO_CLOCK_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 WO	**GPIO_CLOCK_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	0x0 RW	**GPIO_CLOCK_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.
0	0x0 WO	**GPIO_CLOCK_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

4.2.18 GPIOCTL_2—Offset 5018h

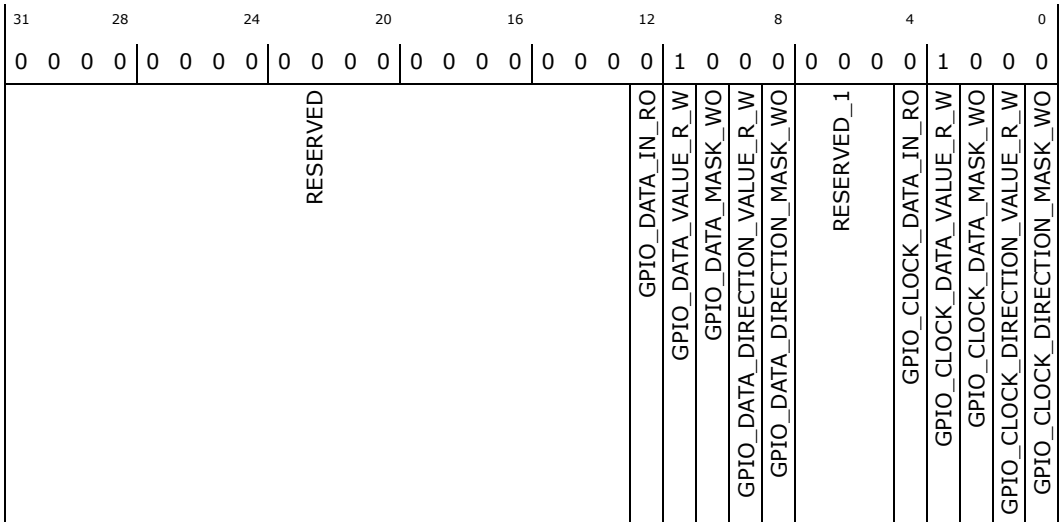
GPIO Control Registers GPIO I2C register (gmbus_register.v reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

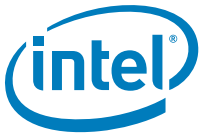
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 5018h

Default: 00000808h





Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RESERVED:** Reserved.
12	0x0 RO	**GPIO_DATA_IN_RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
11	0x1 RW	**GPIO_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
10	0x0 WO	**GPIO_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only
9	0x0 RW	**GPIO_DATA_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	0x0 WO	**GPIO_DATA_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	0x0 RO	**RESERVED_1:** must be written with zeros.
4	0x0 RO	**GPIO_CLOCK_DATA_IN_RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
3	0x1 RW	**GPIO_CLOCK_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 WO	**GPIO_CLOCK_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	0x0 RW	**GPIO_CLOCK_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.
0	0x0 WO	**GPIO_CLOCK_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

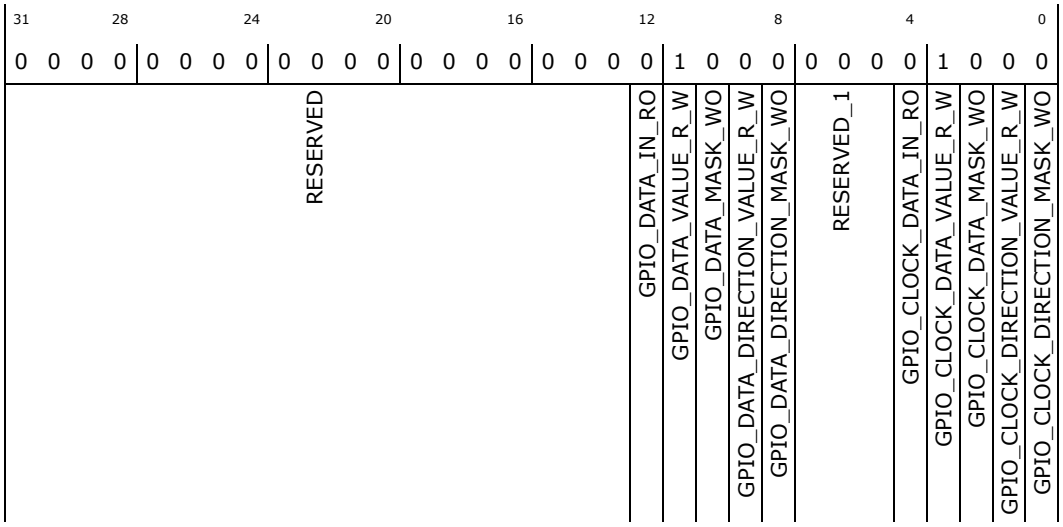
4.2.19 GPIOCTL_3—Offset 501Ch

GPIO Control Registers GPIO I2C register (gmbus_register.v reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 501Ch

Default: 00000808h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RESERVED:** Reserved.
12	0x0 RO	**GPIO_DATA_IN_RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
11	0x1 RW	**GPIO_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
10	0x0 WO	**GPIO_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only
9	0x0 RW	**GPIO_DATA_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	0x0 WO	**GPIO_DATA_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	0x0 RO	**RESERVED_1:** must be written with zeros.
4	0x0 RO	**GPIO_CLOCK_DATA_IN_RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
3	0x1 RW	**GPIO_CLOCK_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 WO	**GPIO_CLOCK_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	0x0 RW	**GPIO_CLOCK_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.
0	0x0 WO	**GPIO_CLOCK_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

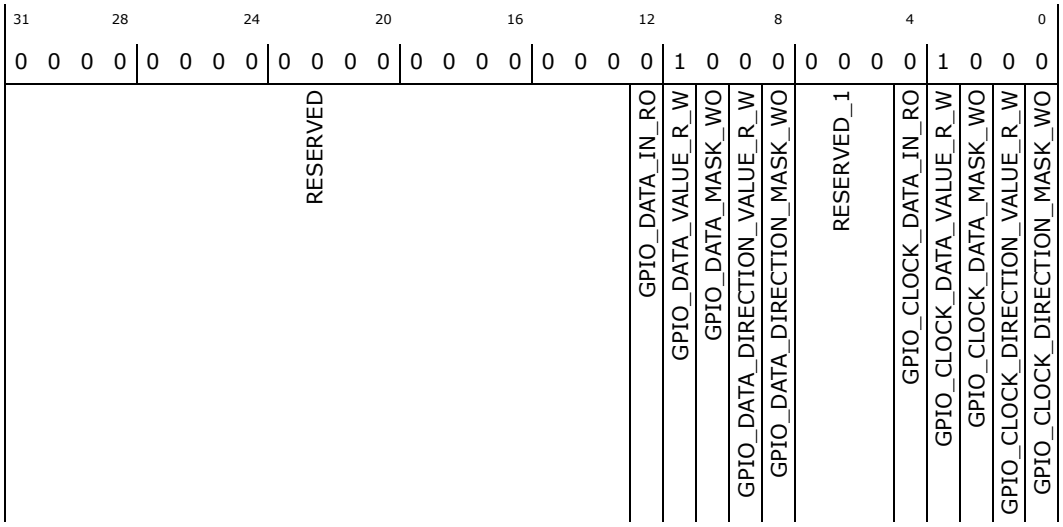
4.2.20 GPIOCTL_4—Offset 5020h

GPIO Control Registers GPIO I2C register (gmbus_register.v reg_gpio0, reg_gpio1, reg_gpio2. reg_gpio3, reg_gpio4)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 5020h

Default: 00000808h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RESERVED:** Reserved.
12	0x0 RO	**GPIO_DATA_IN_RO:** This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
11	0x1 RW	**GPIO_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)
10	0x0 WO	**GPIO_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT write GPIO Data Value bit (default). 1 = Write GPIO Data Value bit. AccessType: Write Only
9	0x0 RW	**GPIO_DATA_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 = Pin is configured as an input (default) 1 = Pin is configured as an output.
8	0x0 WO	**GPIO_DATA_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Data Direction Value bit (default). 1 = Write GPIO Data Direction Value bit. AccessType: Write Only
7:5	0x0 RO	**RESERVED_1:** must be written with zeros.
4	0x0 RO	**GPIO_CLOCK_DATA_IN_RO:** This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset. AccessType: Read Only
3	0x1 RW	**GPIO_CLOCK_DATA_VALUE_R_W:** This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default = 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . (this mimics the I2C external pull-ups on the bus)

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 WO	**GPIO_CLOCK_DATA_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 = Do NOT write GPIO Clock Data Value bit (default). 1 = Write GPIO Clock Data Value bit. AccessType: Write Only
1	0x0 RW	**GPIO_CLOCK_DIRECTION_VALUE_R_W:** This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 = Pin is configured as an input and the output driver is set to tri-state (default) 1 = Pin is configured as an output.
0	0x0 WO	**GPIO_CLOCK_DIRECTION_MASK_WO:** This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 = Do NOT update the GPIO Clock Direction Value bit on a write (default). 1 = Update the GPIO Clock Direction Value bit. on a write operation to this register. AccessType: Write Only

4.2.21 GMBUS0—Offset 5100h

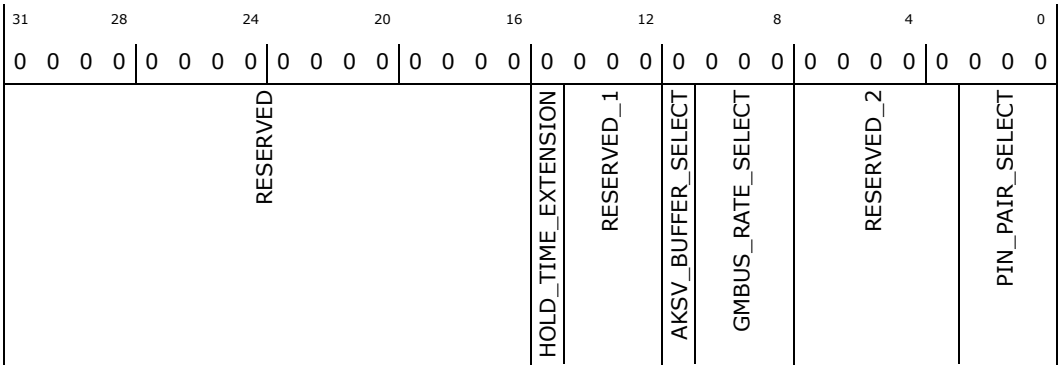
GMBUS Clock/Port Select gmbus clock and port select (gmbus_register.v reg_gmbus0)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 5100h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**HOLD_TIME_EXTENSION:** This bit selects the hold time on the data line driven from the GMCH. 0 = Hold time of 0ns 1 = Hold time of 300 ns
14:12	0x0 RO	**RESERVED_1:** Reserved.
11	0x0 RW	**AKSV_BUFFER_SELECT:** This bit selects whether the data to be written over GMBUS comes from the Aksv buffer for HDCP authentication, or from the GMBUS data buffer. Please note that when writing data from the Aksv buffer, all GMBUS protocol must be followed, including indicating the number of bytes to be transferred during the DATA phase of a GMBUS cycle. 0 (Default) Use the GMBUS data buffer (GMBUS3) for data transmission 1 Use the Aksv data buffer (GMBUS6 and GMBUS7) for data transmission. [DevBW, DevCL] Reserved:
10:8	0x0 RW	**GMBUS_RATE_SELECT:** These two bits select the rate that the GMBUS will run at. It also defines the AC timing parameters used. It should only be changed when between transfers when the GMBUS is idle. 1xx = Reserved. 000 = 100 KHz 001 = 50 KHz 010 = 400 KHz 011 = 1 MHz for SDVO
7:3	0x0 RO	**RESERVED_2:** Reserved.
2:0	0x0 RW	**PIN_PAIR_SELECT:** This field selects an GMBUS pin pair for use in the GMBUS communication. Use the table above to determine which pin pairs are available for a particular device and the intended function of that pin pair. Note that it is not a straight forward mapping of port numbers to pair select numbers. 000 = None (disabled) 001 = MIPI I2C use 010 = Dedicated Analog Monitor DDC Pins (DDC1DATA, DDC1CLK) 011 = HDMI D 100 = DP/HDMI port C Use [DevCTG] 101 = sDVO/HDMI Use 110 = Reserved 111 = D connector control signals

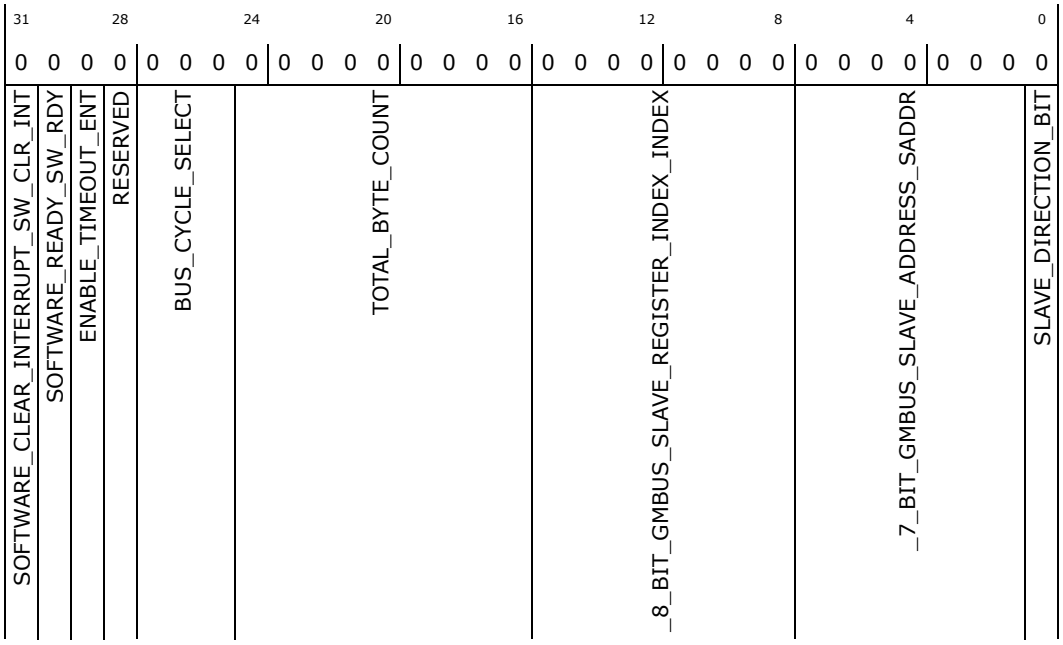
4.2.22 GMBUS1—Offset 5104h

GMBUS Command and Status gmbus command and status (gmbus_register.v reg_gmbus1)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 5104h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SOFTWARE_CLEAR_INTERRUPT_SW_CLR_INT:** This bit must be clear for normal operation. Setting the bit , then clearing it acts as local reset to the GMBUS controller. This bit is commonly used by software to clear a BUS_ERROR when a slave device delivers a NACK. 0 = If this bit is written as a zero when its current state is a one, will clear the HW_RDY bit and allows register writes to be accepted to the GMBUS registers (Write Protect Off). This bit is cleared to zero when an event causes the HW_RDY bit transition to occur. 1 = Asserted by software after servicing the GMBUS interrupt. Setting this bit causes the INT status bit to be cleared. Setting (1) this bit also asserts the HW_RDY bit (until this bit is written with a 0). When this bit is set, no writes to GMBUS registers will cause the contents to change with the exception of this bit which can be written.
30	0x0 RW	**SOFTWARE_READY_SW_RDY:** Data handshake bit used in conjunction with HW_RDY bit. 0 = De-asserted via the assertion event for HW_RDY bit 1 = When asserted by software, results in de-assertion of HW_RDY bit
29	0x0 RW	**ENABLE_TIMEOUT_ENT:** Enables timeout for slave response. When this bit is enabled and the slave device response has exceeded the timeout period, the GMBUS Slave Stall Timeout Error interrupt bit is set. 0 = disable timeout counter 1 = enable timeout counter
28	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
27:25	0x0 RW	**BUS_CYCLE_SELECT:** 000 = No GMBUS cycle is generated. 001 = GMBUS cycle is generated without an INDEX, with no STOP, and ends with a WAIT 010 = Reserved 011 = GMBUS cycle is generated with an INDEX, with no STOP, and ends with a WAIT 100 = Generates a STOP if currently in a WAIT or after the completion of the current byte if active. 101 = GMBUS cycle is generated without an INDEX and with a STOP 110 = Reserved 111 = GMBUS cycle is generated with an INDEX and with a STOP GMBUS cycle will always consist of a START followed by Slave Address, followed by an optional read or write data phase. A read cycle with an index will consist of a START followed by a Slave Address a WRITE indication and the INDEX and then a RESTART with a Slave Address and an optional read data phase. The GMBUS cycle will terminate either with a STOP or by entering a wait state. The WAIT state is exited by generating a STOP or by starting another GMBUS cycle. This can only cause a STOP to be generated if a GMBUS cycle is generated, the GMBUS is currently in a data phase, or it is in a WAIT phase: Note that the three bits can be decoded as follows: 27 = STOP generated 26 = INDEX used 25 = cycle ends in a WAIT
24:16	0x0 RW	**TOTAL_BYTE_COUNT:** (9-bits). This determines the total number of bytes to be transferred during the DATA phase of a GMBUS cycle. The DATA phase can be prematurely terminated by generating a STOP while in the DATA phase (see Bus Cycle Select). Do not change the value of this field during GMBUS cycles transactions.
15:8	0x0 RW	**_8_BIT_GMBUS_SLAVE_REGISTER_INDEX_INDEX:** This field specifies the 8-bits of index to be used for the generated bus write transaction or the index used for the WRITE portion of the WRITE/READ pair. It only has an effect if the enable Index bit is set. Do not change this field during a GMBUS transaction.
7:1	0x0 RW	**_7_BIT_GMBUS_SLAVE_ADDRESS_SADDR:** When a GMBUS cycle is to be generated using the Bus Cycle Select field, this field specifies the value of the slave address that is to be sent out. For use with 10-bit slave address devices, set this value to 11110XXb (where the last two bits (xx) are the two MSBs of the 10-bit address) and the slave direction bit to a write. This is followed by the first data byte being the 8 LSBs of the 10-bit slave address. Special Slave Addresses 0000 000R = General Call Address 0000 000W = Start byte 0000 001x = CBUS Address 0000 010x = Reserved 0000 011x = Reserved 0000 1xxx = Reserved 1111 1xxx = Reserved 1111 0xxx = 10-Bit addressing

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**SLAVE_DIRECTION_BIT:** When a GMBUS cycle is to be generated based on the Bus Cycle Select, this bit determines if the operation will be a read or a write. A read operation with the index enabled will perform a write with just the index followed by a re-start and a read. 1 = Indicates that a Read from the slave device operation is to be performed. 0 = Indicates that a Write to slave device operation is to be performed.

4.2.23 GMBUS2—Offset 5108h

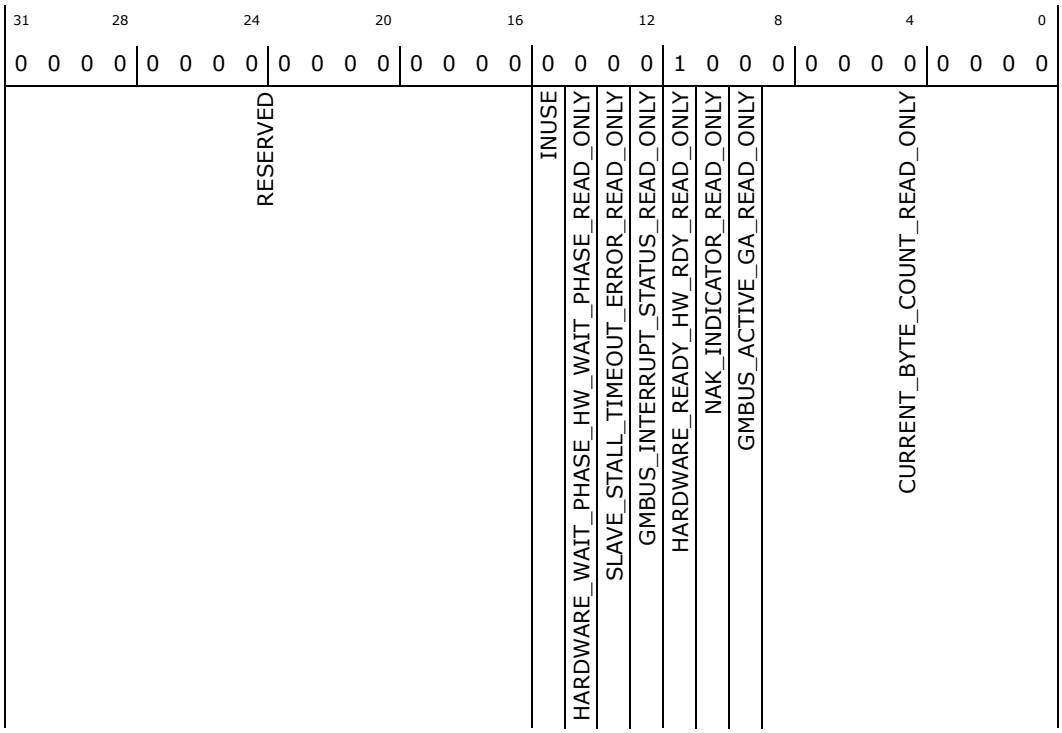
GMBUS Status Register gmbus status (gmbus_register.v reg_gmbus2)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 5108h

Default: 00000800h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW/1C	**INUSE:** 0 = read operation that contains a zero in this bit position indicates that the GMBUS engine is now acquired and the subsequent reads of this register will now have this bit set. Writing a 0 to this bit has no effect. 1 = read operation that contains a one for this bit indicates that the GMBUS is currently allocated to someone else and In use . Once set, a write of a 1 to this bit indicates that the software has relinquished the GMBUS resource and will reset the value of this bit to a 0. Software wishing to arbitrate for the GMBUS resource can poll this bit until it reads a zero and will then own usage of the GMBUS controller. This bit has no effect on the hardware, and is only used as semaphore among various independent software threads that don t know how to synchronize their use of this resource that may need to use the GMBUS logic. Writing a one to this bit is software s indication that the software use of this resource is now terminated and it is available for other clients. AccessType: One to clear
14	0x0 RO	**HARDWARE_WAIT_PHASE_HW_WAIT_PHASE_READ_ONLY:** 0 = The GMBUS engine is not in a wait phase. 1 = Set when GMBUS engine is in wait phase. Wait phase is entered at the end of the current transaction when that transaction is selected not to terminate with a STOP. Once in a WAIT_PHASE, the software can now choose to generate a STOP cycle or a repeated start (RESTART) cycle followed by another GMBUS transaction on the GMBUS. AccessType: Read Only
13	0x0 RO	**SLAVE_STALL_TIMEOUT_ERROR_READ_ONLY:** This bit indicates that a slave stall timeout has occurred. It is tied to the Enable Timeout (ENT) bit. 0 = No slave timeout has occurred. 1 = A slave acknowledge timeout has occurred AccessType: Read Only
12	0x0 RO	**GMBUS_INTERRUPT_STATUS_READ_ONLY:** This bit indicates that an event that causes a GMBUS interrupt has occurred. 0 = The conditions that could cause a GMBUS interrupt have not occurred or this bit has been cleared by software assertion of the SW_CLR_INT bit. 1 = GMBUS interrupt event occurred. This interrupt must have been one of the types enabled in the GMBUS4 register. Reserved AccessType: Read Only

Bit Range	Default & Access	Field Name (ID): Description
11	0x1 RO	**HARDWARE_READY_HW_RDY_READ_ONLY:** This provides a method of detecting when the current software client routine can proceed with the next step in a sequence of GMBUS operations. This data handshake bit is used in conjunction with the SW_RDY bit. When this bit is changed to asserted by the GMBUS controller, it results in the de-assertion of the SW_RDY bit. 0 = Condition required for assertion has not occurred or when this bit was a one and: SW_RDY bit has been asserted. During a GMBUS read transaction, after the each read of the data register. During a GMBUS write transaction, after each write of the data register. SW_CLR_INT bit has been cleared. 1 = This bit is asserted under the following conditions: After a reset or when the transaction is aborted by the setting of the SW_CLR_INT bit. When an active GMBUS cycle has terminated with a STOP. When during a GMBUS write transaction, the data register needs and can accept another four bytes of data. During a GMBUS read transaction, this bit is asserted when the data register has four bytes of new data or the read transaction DATA phase is complete and the data register contains the last few bytes of the read data. This bit resumes to normal operation when the SW_CLR_INT bit is written to a 0. AccessType: Read Only
10	0x0 RO	**NAK_INDICATOR_READ_ONLY:** Was previously called Slave Acknowledge Timeout Error SATOER. 0 = No bus error has been detected or SW_CLR_INT has been written as a zero since the last bus error. 1 = Set by hardware if any expected device acknowledge is not received from the slave within the timeout. AccessType: Read Only
9	0x0 RO	**GMBUS_ACTIVE_GA_READ_ONLY:** This is a status bit that indicates whether the GMBUS controller is in an IDLE state or not. 0 = The GMBUS controller is currently IDLE. 1 = This indicates that the bus is in START, ADDRESS, INDEX, DATA, WAIT, or STOP Phase. Set when GMBUS hardware is not IDLE. AccessType: Read Only
8:0	0x0 RO	**CURRENT_BYTE_COUNT_READ_ONLY:** Can be used to determine the number of bytes currently transmitted/received by the GMBUS controller hardware. Set to zero at the start of a GMBUS transaction data transfer and incremented after the completion of each byte of the data phase. Note that because reads have internal storage, the byte count on a read operation may be ahead of the data that has been accepted from the data register. AccessType: Read Only

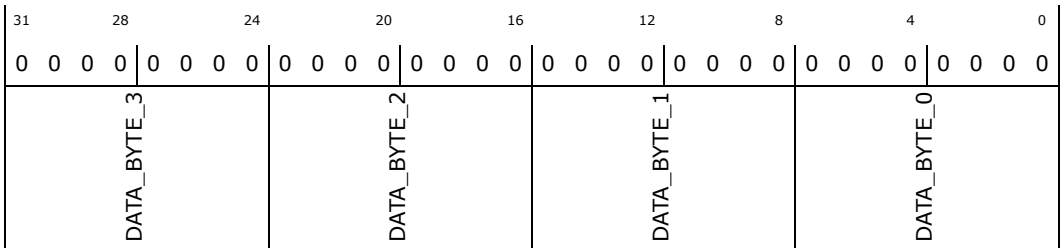
4.2.24 GMBUS3—Offset 510Ch

GMBUS Data Buffer gmbus data buffer (gmbus_register.v reg_gmbus3)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 510Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**DATA_BYTE_3:** Reserved.
23:16	0x0 RW	**DATA_BYTE_2:** Reserved.
15:8	0x0 RW	**DATA_BYTE_1:** Reserved.
7:0	0x0 RW	**DATA_BYTE_0:** Reserved.

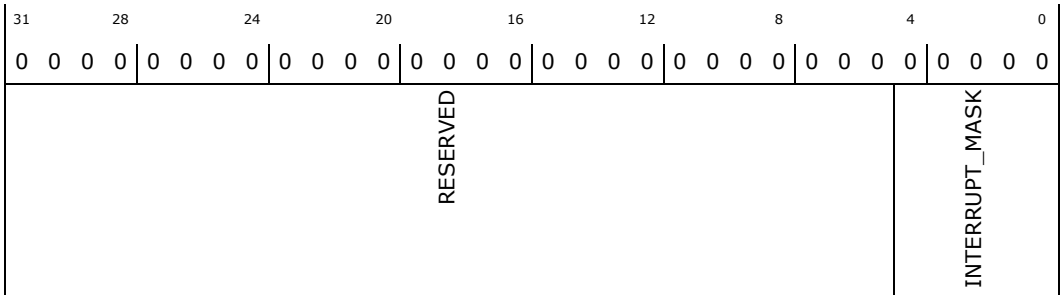
4.2.25 GMBUS4—Offset 5110h

GMBUS Interrupt Mask gmbus interrupt mask (gmbus_register.v reg_gmbus4)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 5110h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4:0	0x0 RW	**INTERRUPT_MASK:** This field specifies which GMBUS interrupts events may contribute to the setting of gmbus interrupt status bit in second level interrupt status register PIPEASTAT. Bit 4: GMBUS Slave stall timeout Bit 3: GMBUS NAK Bit 2: GMBUS Idle Bit 1: Hardware wait (GMBUS cycle without a stop has completed) Bit 0: Hardware ready (Data has been transferred) 0 = Disable this type of GMBUS interrupt 1 = Enable this type of GMBUS interrupt

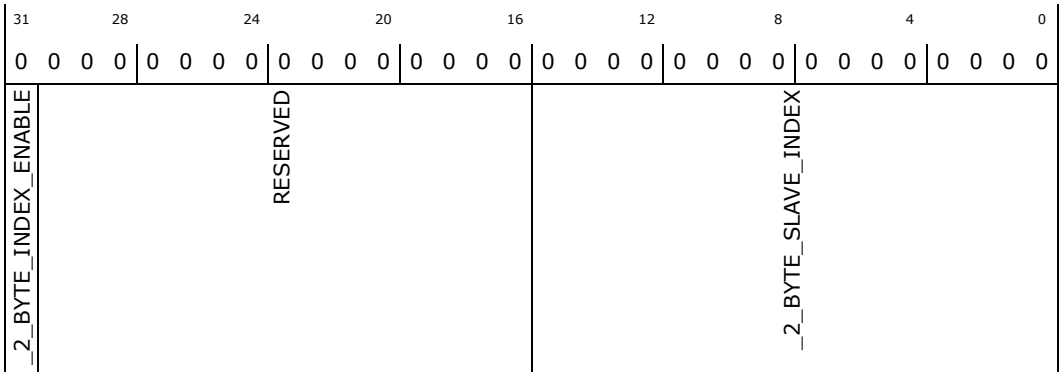
4.2.26 GMBUS5—Offset 5120h

2 Byte Index Register gmbus index (gmbus_register.v reg_gmbus5)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 5120h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**_2_BYTE_INDEX_ENABLE:** When this bit is asserted (1), then bits 15:00 are used as the index. Bits 15:8 are used in the first byte which is the most significant index bits. The slave index in the GMBUS1(15:8) are ignored. Bits 7:0 are used in the second byte which is the least significant index bits.
30:16	0x0 RO	**RESERVED:** Reserved.
15:0	0x0 RW	**_2_BYTE_SLAVE_INDEX:** This is the 2 byte index used in all GMBUS accesses when bit 31 is asserted (1).

4.2.27 GMBUS6—Offset 5130h

GMBUS Aksv Buffer Low gmbus data buffer (gmbus_register.v reg_gmbus6

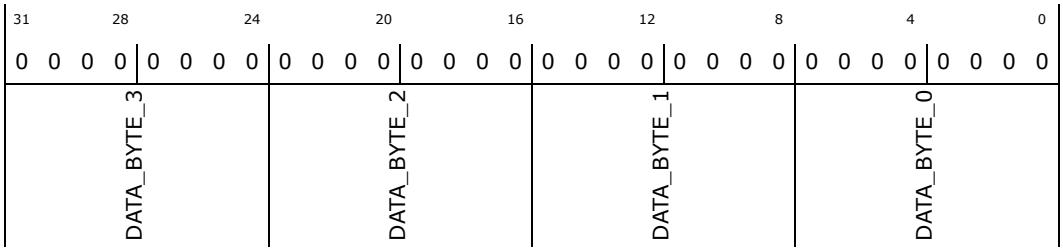
)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 5130h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 WO	**DATA_BYTE_3:** Reserved.
23:16	0x0 WO	**DATA_BYTE_2:** Reserved.
15:8	0x0 WO	**DATA_BYTE_1:** Reserved.
7:0	0x0 WO	**DATA_BYTE_0:** Reserved.

4.2.28 GMBUS7—Offset 5134h

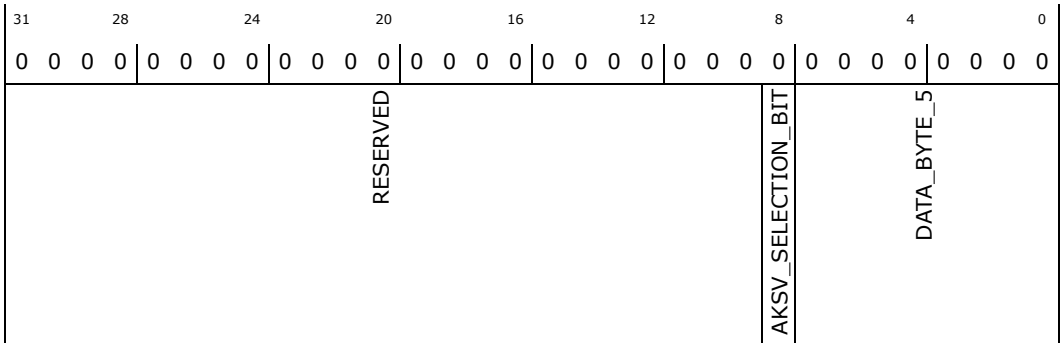
GMBUS Aksv Buffer High gmbus data buffer (gmbus_register.v reg_gmbus7)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 5134h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**RESERVED:** MBZ

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 WO	**AKSV_SELECTION_BIT:** 0 = The fuse value of the Aksv is used. 1 = The register value of the Aksv is used. Aksv Selection Bit: 0 = The register value of the Aksv is used. 1 = The fuse value of the Aksv is used. Reserved
7:0	0x0 WO	**DATA_BYTE_5:** Reserved.

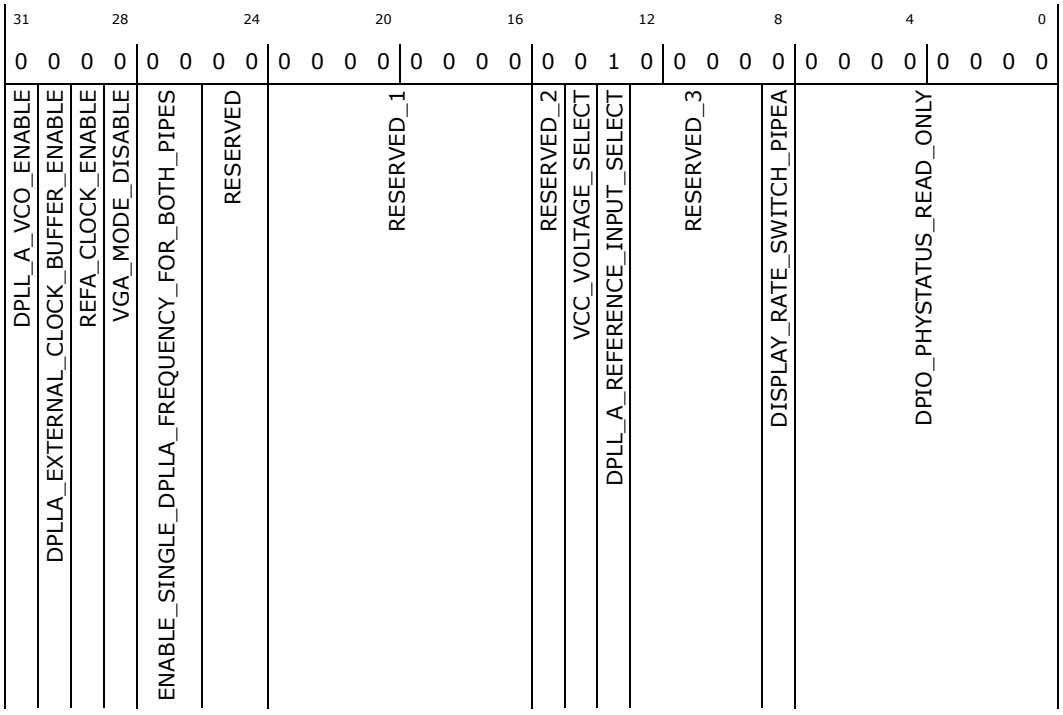
4.2.29 DPLLA_CTRL—Offset 6014h

DPLL A Control Register DPLL A Control (cpdmmreg.v reg03_lt)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6014h

Default: 00002000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**DPLL_A_VCO_ENABLE:** Disabling the PLLA will cause the display dot clock to stop. 0 = DPLLA is disabled in its lowest power state (default) 1 = DPLLA is enabled and operational (42usec until lock without calibration and 110usec for calibration)
30	0x0 RW	**DPLLA_EXTERNAL_CLOCK_BUFFER_ENABLE:** 0 = Disable DPLLA clock from being driven out 1 = Enable DPLLA clock to be drive out Reserved DPLLA Serial DVO High Speed IO clock Enable 0 = High Speed IO Clock Disabled (default) 1 = High Speed IO Clock Enabled (must be set in Serial DVO and HDMI modes)
29	0x0 RW	**REFA_CLOCK_ENABLE:** Indicate the reference clock of PLL A is enable 0 Disable (default) 1 Enable
27:26	0x0 RW	**ENABLE_SINGLE_DPLLA_FREQUENCY_FOR_BOTH_PIPES:** When two pipes are enabled for eDP and both pipes can run with the same DP frequency either 162MHz or 270MHz. Setting this mode can allow using only DPLLA to feed both pipes. DPLLB should be shutdown to save power. This control is double buffered. 00 = Disabled 01 = Enabled 10 = Reserved 11 = Reserved Reserved DPLLA Mode Select : Configure the DPLLA for various supported Display Modes 00 = Reserved 01 = DPLLA in DAC/Serial DVO/UDI/Integrated TV mode 10 = DPLLA in LVDS mode (Mobile devices ONLY) otherwise RESERVED 11 = DP
25:24	0x0 RO	**RESERVED:** FPA0/FPA1 P2 Clock Divide: 00 = Divide by 10. This is used when Dot Clock =(270MHz in sDVO, HDMI, or DAC modes 01 = Divide by 5. This is used when Dot Clock)270MHz 10 = Reserved 11 = Reserved For DPLLA in LVDS mode, BITS(27:26)=10 00 = Divide by 14. This is used in Single-Channel LVDS 01 = Divide by 7. This is used in Dual-Channel LVDS 10 = Reserved 11 = Reserved
15	0x0 RO	**RESERVED_2:** Write as zero PLLA Lock (RO) 1 - PLLA Lock 0 PLLA unlock

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**VCC_VOLTAGE_SELECT:** This control selects the VCC voltage in DPLL 0 = 1.0 V (default) 1 = voltage for LDO circuit Reserved
13	0x1 RW	**DPLL_A_REFERENCE_INPUT_SELECT:** This control selects the integrated core refclk or external OSC refclk as the input clock source to DPLL A. 0 = SSC 1 = non SSC Reserved PLL Reference Input Select: The PLL reference should be selected based on the display device that is being driven. The standard reference clock is used for CRT modes using the analog display port or LCD panels for both the sDVO connected transmitter or the integrated LVDS. TV Clock in should be selected when driving an sDVO connected TV encoder.
12:9	0x0 RO	**RESERVED_3:** Parallel to Serial Load Pulse phase selection: Programmable select bits to choose the relative phase of the high speed (10X) DPLL clock used for generating the parallel to serial load pulse for digital display port on PCIe. The relative phase is the number of flop delays (phase 0 represents 1 flop delay) of the 1X parallel data synchronization signal in the 10X clock domain. The earliest selectable clock phase is 4. A phase selection of 10 or greater simply extends the flop delay count to sample delayed data. 0100 = use clock phase-4 0101 = use clock phase-5 0110 = use clock phase-6 (Default value) 0111 = use clock phase-7 1000 = use clock phase-8 1001 = use clock phase-9 1010 = use clock phase-10 1011 = use clock phase-11 1100 = use clock phase-12 1101 = use clock phase-13 Phases 0 through 3 are not available for Load Pulse selection. [DevCL] The following programming is recommended for Crestline based on PV timing analysis: 1101 use clock phase-13 [DevBLC, DevCTG] Reserved. Programming for load pulse is in PXP AFE config space.
8	0x0 RW	**DISPLAY_RATE_SWITCH_PIPEA:** Switching this bit (transition 0 to 1 or 1 to 0) causes the DSP HW to disable and than enable the DPLL during vblank (2 row) in order to switch the frequency at the DPLL (new dividers stored at the DPIO which is double buffered) (This bit is only available when bits 17:16 of the PIPEACONF register are 00) [DevBW, DevCL, DevBLC] Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**DPIO_PHYSTATUS_READ_ONLY:** This field contains the two 4-bit ModPhy lane status. One for PortB and one for PortC Bit 7:4 = Port C PhyStatus[3:0] Bit 3:0 = Port B PhyStatus[3:0] 00000001b - Divide by one 00000010b - Divide by two 00000100b - Divide by three 00001000b - Divide by four 00010000b - Divide by five 00100000b - Divide by six 01000000b - Divide by seven 10000000b - Divide by Eight All other values are illegal and should not be used AccessType: Read Only

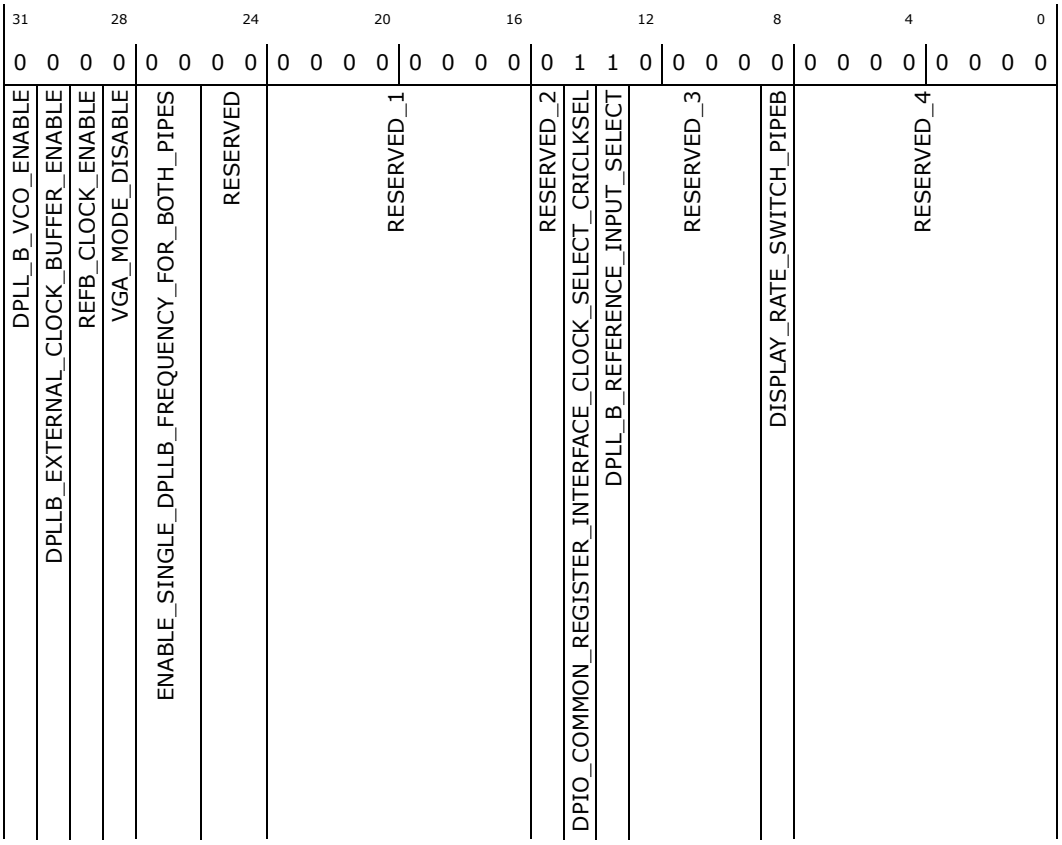
4.2.30 DPLLB_CTRL—Offset 6018h

DPLL B Control Registers DPLL B Control (cpdmmreg.v reg04_lt)

Access Method

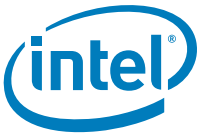
Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6018h

Default: 00006000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**DPLL_B_VCO_ENABLE:** Disabling the PLLB will cause the display dot clock to stop. 0 = DPLLB is disabled in its lowest power state (default) 1 = DPLLB is enabled and operational (42usec until lock without calibration and 110usec for calibration)
30	0x0 RW	**DPLLB_EXTERNAL_CLOCK_BUFFER_ENABLE:** 0 = Disable DPLLB clock from being driven out 1 = Enable DPLLB clock to be drive out Reserved DPLLB Serial DVO High Speed IO clock Enable 0 = High Speed IO Clock Disabled (default) 1 = High Speed IO Clock Enabled (must be set in Serial DVO and HDMI modes)
29	0x0 RW	**REFB_CLOCK_ENABLE:** Indicate the reference clock of PLL A is enable 0 Disable (default) 1 Enable

Bit Range	Default & Access	Field Name (ID): Description
27:26	0x0 RW	**ENABLE_SINGLE_DPLLB_FREQUENCY_FOR_BOTH_PIPES:** When two pipes are enabled for eDP and both pipes can run with the same DP frequency either 162MHz or 270MHz. Setting this mode can allow using only DPLLB to feed both pipes. DPLLA should be shutdown to save power. 00 = Disabled 01 = Enabled 10 = Reserved 11 = Reserved Reserved DPLLB Mode Select : Configure the DPLLB for various supported Display Modes 00 = Reserved 01 = DPLLA in DAC/Serial DVO/UDI/Integrated TV mode 10 = DPLLA in LVDS mode (Mobile devices ONLY) otherwise RESERVED 11 = DP
25:24	0x0 RO	**RESERVED:** FPB0/FPB1 P2 Clock Divide: 00 = Divide by 10. This is used when Dot Clock =(270MHz in sDVO, HDMI, or DAC modes 01 = Divide by 5. This is used when Dot Clock)270MHz 10 = Reserved 11 = Reserved For DPLLB in LVDS mode, BITS(27:26)=10 00 = Divide by 14. This is used in Single-Channel LVDS 01 = Divide by 7. This is used in Dual-Channel LVDS 10 = Reserved 11 = Reserved
15	0x0 RO	**RESERVED_2:** Write as zero PLLB Lock (RO) 1 - PLLB Lock 0 PLLB unlock
14	0x1 RW	**DPIO_COMMON_REGISTER_INTERFACE_CLOCK_SELECT_CRICLKSEL:** This bit is to control the clock source for DPIO Common Register Interface 0 = Use external reclk pad 1 = Use integrated core refclk (default)
13	0x1 RW	**DPLL_B_REFERENCE_INPUT_SELECT:** This control selects the integrated core refclk or external OSC refclk as the input clock source to DPLL B. 0 = SSC 1 = non SSC Reserved PLL Reference Input Select: The PLL reference should be selected based on the display device that is being driven. The standard reference clock is used for CRT modes using the analog display port or LCD panels for both the sDVO connected transmitter or the integrated LVDS. TV Clock in should be selected when driving an sDVO connected TV encoder.



Bit Range	Default & Access	Field Name (ID): Description
12:9	0x0 RO	**RESERVED_3:** Parallel to Serial Load Pulse phase selection: Programmable select bits to choose the relative phase of the high speed (10X) DPLL clock used for generating the parallel to serial load pulse for digital display port on PCIe. The relative phase is the number of flop delays (phase 0 represents 1 flop delay) of the 1X parallel data synchronization signal in the 10X clock domain. The earliest selectable clock phase is 4. A phase selection of 10 or greater simply extends the flop delay count to sample delayed data. 0100 = use clock phase-4 0101 = use clock phase-5 0110 = use clock phase-6 (Default value) 0111 = use clock phase-7 1000 = use clock phase-8 1001 = use clock phase-9 1010 = use clock phase-10 1011 = use clock phase-11 1100 = use clock phase-12 1101 = use clock phase-13 Phases 0 through 3 are not available for Load Pulse selection. [DevCL] The following programming is recommended for Crestline based on PV timing analysis: 1101 use clock phase-13 [DevBLC, DevCTG] Reserved. Programming for load pulse is in PXP AFE config space.
8	0x0 RW	**DISPLAY_RATE_SWITCH_PIPEB:** Switching this bit (transition 0 to 1 or 1 to 0) causes the DSP HW to disable and than enable the DPLL during vblank (2 row) in order to switch the frequency at the DPLL (new dividers stored at the DPIO which is double buffered) (This bit is only available when bits 17:16 of the PIPEACONF register are 00) [DevBW, DevCL, DevBLC] Reserved

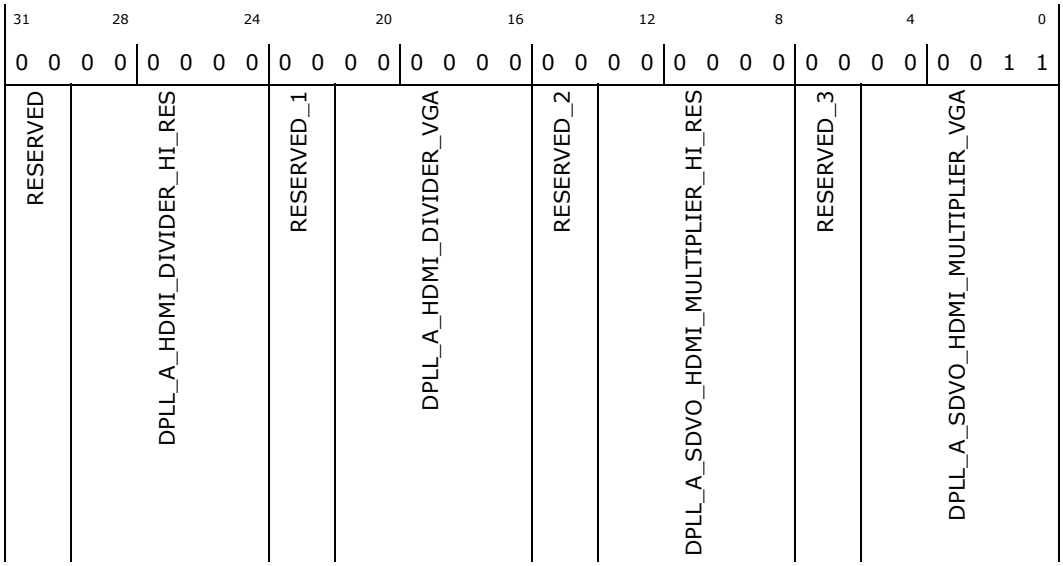
4.2.31 DPLLAMD—Offset 601Ch

DPLL A SDVO/HDMI Multiplier/Divisor Register Pipe A multiply (cpdmmreg.v reg15_lt)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 601Ch

Default: 00000003h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RESERVED:** Reserved.
29:24	0x0 RW	**DPLL_A_HDMI_DIVIDER_HI_RES:** When the source is high resolution, this field determines the number of pixels to be included in the multiplied packet defined by the SDVO/HDMI multiplier. For SDVO and CRT, the only valid setting is 1x. HDMI example: If the pixel clock on the display should be 180MHz and the display PLL is set to 270MHz, two pixels and one fill code must be sent over HDMI (fixed frequency mode only). Therefore, the HDMI divider should be set to 2 and the SDVO/HDMI multiplier should be set to 3, since 180 MHz (pixel clock) = 2/3*270MHz (link character clock) This divider must be set to 1x for any mode except HDMI fixed frequency mode. Value in this register = number of pixels per packet 1 Default: 0000 1 pixel per packet (Default value, must be set to 1x for any mode except HDMI fixed frequency mode) Range: 0-63 (1 pixel per packet 64 pixels per packet)
23:22	0x0 RO	**RESERVED_1:** Reserved.
15:14	0x0 RO	**RESERVED_2:** Reserved.
13:8	0x0 RW	**DPLL_A_SDVO_HDMI_MULTIPLIER_HI_RES:** This field determines the data multiplier for sDVO and is also applied to CRT. In order to keep the clock rate to a more narrow range of rates, the multiplier is set and the Display PLL programmed to a multiple of the display mode s actual clock rate. This is unrelated to the pixel multiply that is selectable per plane. 6x and higher multipliers can only be used for HDMI mode. Value in this register = multiplication factor - 1 Default: 000000 (1X) Range: 0 63 (1X 64X)

Bit Range	Default & Access	Field Name (ID): Description
7:6	0x0 RO	**RESERVED_3:** Reserved.

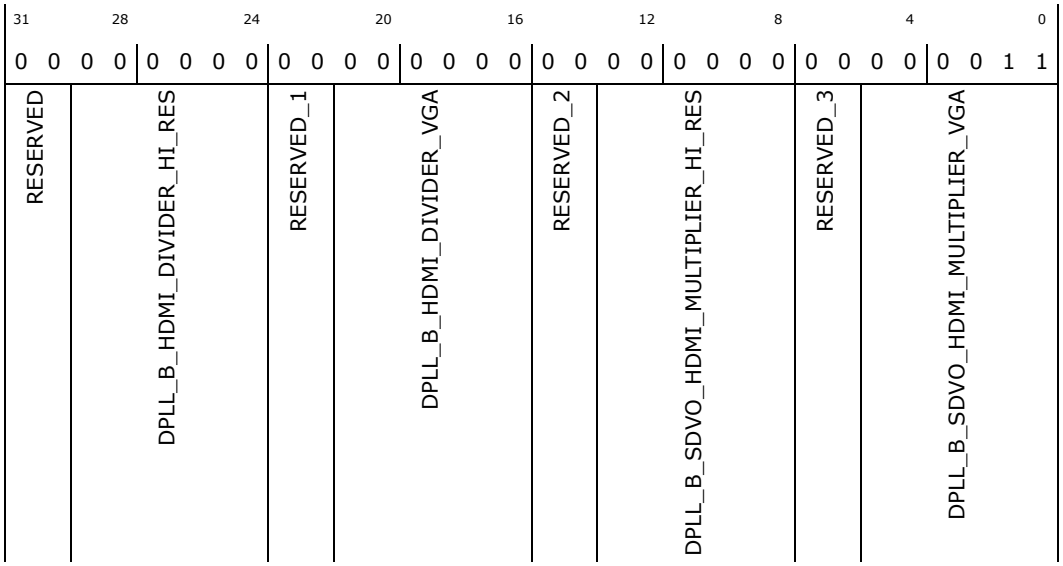
4.2.32 DPLLBMD—Offset 6020h

DPLL B SDVO/HDMI Multiplier/Divisor Register Pipe B multiplyer (cpdmmreg.vreg16_lt)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6020h

Default: 00000003h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
29:24	0x0 RW	**DPLL_B_HDMI_DIVIDER_HI_RES:** When the source is high resolution, this field determines the number of pixels to be included in the multiplied packet defined by the SDVO/HDMI multiplier. For SDVO and CRT, the only valid setting is 1x. HDMI example: If the pixel clock on the display should be 180MHz and the display PLL is set to 270MHz, two pixels and one fill code must be sent over HDMI (fixed frequency mode only). Therefore, the HDMI divider should be set to 2 and the SDVO/HDMI multiplier should be set to 3, since 180 MHz (pixel clock) = 2/3*270MHz (link character clock) This divider must be set to 1x for any mode except HDMI fixed frequency mode. Value in this register = number of pixels per packet 1 Default: 0000 1 pixel per packet (Default value, must be set to 1x for any mode except HDMI fixed frequency mode) Range: 0-63 (1 pixel per packet 64 pixels per packet)
23:22	0x0 RO	**RESERVED_1:** Reserved.
15:14	0x0 RO	**RESERVED_2:** Reserved.
13:8	0x0 RW	**DPLL_B_SDVO_HDMI_MULTIPLIER_HI_RES:** This field determines the data multiplier for sDVO and is also applied to CRT. In order to keep the clock rate to a more narrow range of rates, the multiplier is set and the Display PLL programmed to a multiple of the display mode s actual clock rate. This is unrelated to the pixel multiply that is selectable per plane. 6x and higher multipliers can only be used for HDMI mode. Value in this register = multiplication factor - 1 Default: 000011 (4X) Range: 0 63 (1X 64X)
7:6	0x0 RO	**RESERVED_3:** Reserved.

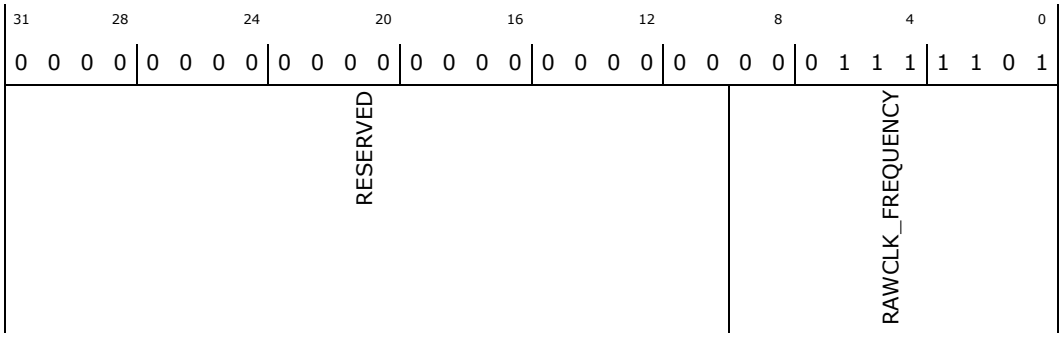
4.2.33 RAWCLK_FREQ—Offset 6024h

Rawclk Frequency

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6024h

Default: 0000007Dh



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**RESERVED:** Project: All Format:
9:0	0x7d RW	**RAWCLK_FREQUENCY:** Project: All Format: Program this field with rawclk frequency. This is used to generate a divided down clock for miscellaneous timers in display.

4.2.34 DPLLC_CTRL—Offset 6030h

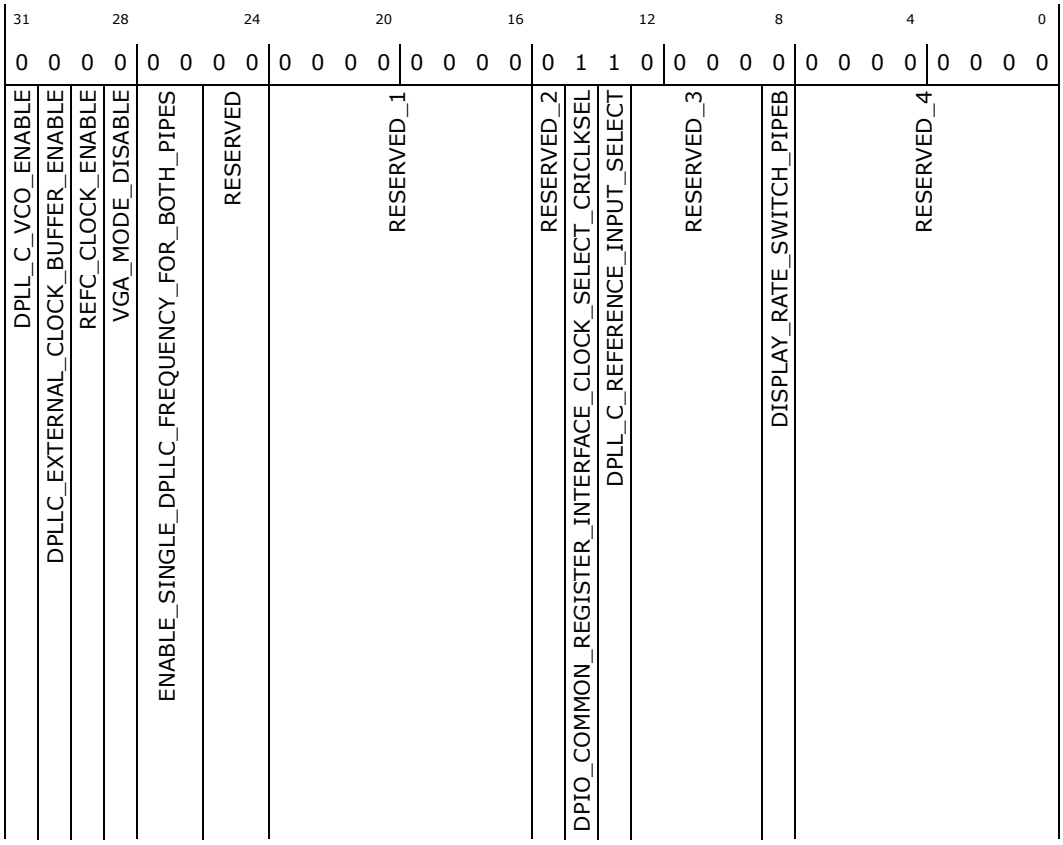
DPLL C Control Registers DPLL C Control (cpdmmreg.v reg04_lt)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6030h

Default: 00006000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**DPLL_C_VCO_ENABLE:** Disabling the PLLC will cause the display dot clock to stop. 0 = DPLLC is disabled in its lowest power state (default) 1 = DPLLC is enabled and operational (42usec until lock without calibration and 110usec for calibration)
30	0x0 RW	**DPLLC_EXTERNAL_CLOCK_BUFFER_ENABLE:** 0 = Disable DPLLC clock from being driven out 1 = Enable DPLLC clock to be drive out Reserved DPLLC Serial DVO High Speed IO clock Enable 0 = High Speed IO Clock Disabled (default) 1 = High Speed IO Clock Enabled (must be set in Serial DVO and HDMI modes)
29	0x0 RW	**REFC_CLOCK_ENABLE:** Indicate the reference clock of PLL C is enable 0 Disable (default) 1 Enable

Bit Range	Default & Access	Field Name (ID): Description
27:26	0x0 RW	**ENABLE_SINGLE_DPLLC_FREQUENCY_FOR_BOTH_PIPES:** When two pipes are enabled for eDP and both pipes can run with the same DP frequency either 162MHz or 270MHz. Setting this mode can allow using only DPLLC to feed both pipes. DPLLC should be shutdown to save power. 00 = Disabled 01 = Enabled 10 = Reserved 11 = Reserved Reserved DPLLC Mode Select : Configure the DPLLC for various supported Display Modes 00 = Reserved 01 = DPLLC in DAC/Serial DVO/UDI/Integrated TV mode 10 = DPLLC in LVDS mode (Mobile devices ONLY) otherwise RESERVED 11 = DP
25:24	0x0 RO	**RESERVED:** FPB0/FPB1 P2 Clock Divide: 00 = Divide by 10. This is used when Dot Clock =(270MHz in sDVO, HDMI, or DAC modes 01 = Divide by 5. This is used when Dot Clock)270MHz 10 = Reserved 11 = Reserved For DPLLB in LVDS mode, BITS(27:26)=10 00 = Divide by 14. This is used in Single-Channel LVDS 01 = Divide by 7. This is used in Dual-Channel LVDS 10 = Reserved 11 = Reserved
15	0x0 RO	**RESERVED_2:** Write as zero PLLB Lock (RO) 1 - PLLB Lock 0 PLLB unlock
14	0x1 RW	**DPIO_COMMON_REGISTER_INTERFACE_CLOCK_SELECT_CRICLKSEL:** This bit is to control the clock source for DPIO Common Register Interface 0 = Use external reclk pad 1 = Use integrated core refclk (default)
13	0x1 RW	**DPLL_C_REFERENCE_INPUT_SELECT:** This control selects the integrated core refclk or external OSC refclk as the input clock source to DPLL C. 0 = SSC 1 = non SSC Reserved PLL Reference Input Select: The PLL reference should be selected based on the display device that is being driven. The standard reference clock is used for CRT modes using the analog display port or LCD panels for both the sDVO connected transmitter or the integrated LVDS. TV Clock in should be selected when driving an sDVO connected TV encoder.

Bit Range	Default & Access	Field Name (ID): Description
12:9	0x0 RO	**RESERVED_3:** Parallel to Serial Load Pulse phase selection: Programmable select bits to choose the relative phase of the high speed (10X) DPLL clock used for generating the parallel to serial load pulse for digital display port on PCIe. The relative phase is the number of flop delays (phase 0 represents 1 flop delay) of the 1X parallel data synchronization signal in the 10X clock domain. The earliest selectable clock phase is 4. A phase selection of 10 or greater simply extends the flop delay count to sample delayed data. 0100 = use clock phase-4 0101 = use clock phase-5 0110 = use clock phase-6 (Default value) 0111 = use clock phase-7 1000 = use clock phase-8 1001 = use clock phase-9 1010 = use clock phase-10 1011 = use clock phase-11 1100 = use clock phase-12 1101 = use clock phase-13 Phases 0 through 3 are not available for Load Pulse selection. [DevCL] The following programming is recommended for Crestline based on PV timing analysis: 1101 use clock phase-13 [DevBLC, DevCTG] Reserved. Programming for load pulse is in PXP AFE config space.
8	0x0 RW	**DISPLAY_RATE_SWITCH_PIPEB:** Switching this bit (transition 0 to 1 or 1 to 0) causes the DSP HW to disable and than enable the DPLL during vblank (2 row) in order to switch the frequency at the DPLL (new dividers stored at the DPIO which is double buffered) (This bit is only available when bits 17:16 of the PIPEACONF register are 00) [DevBW, DevCL, DevBLC] Reserved

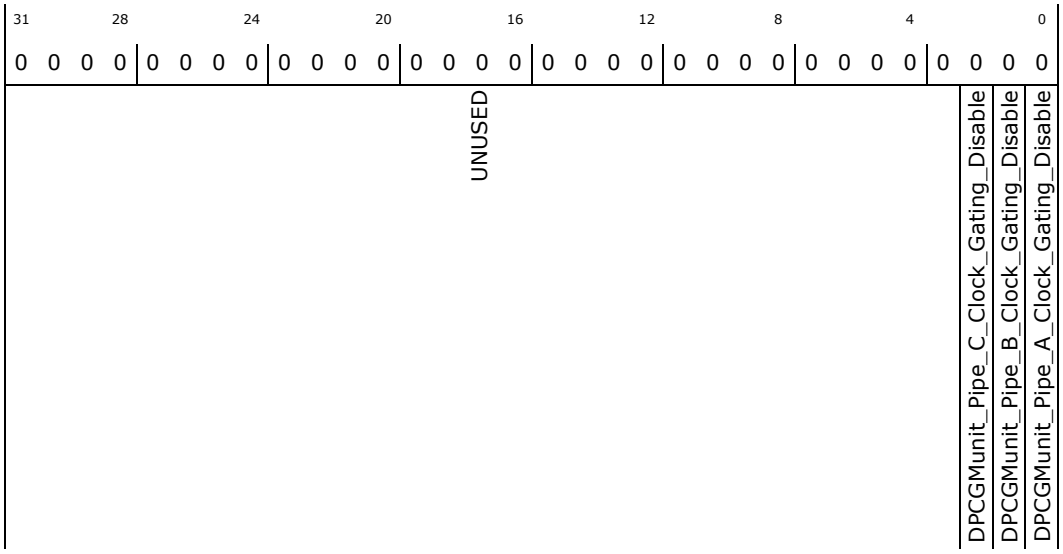
4.2.35 DSPCLK1_GATE_D—Offset 6034h

Clock gating disable for Display Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6034h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**unused (UNUSED):** unused
2	0x0 RW	**DPCGMunit Pipe C Clock Gating Disable (DPCGMunit_Pipe_C_Clock_Gating_Disable):** DPCGMunit Pipe C Clock Gating Disable 0 = Clock gating controlled by unit enabling logic. 1 = Disable clock gating function
1	0x0 RW	**DPCGMunit Pipe B Clock Gating Disable (DPCGMunit_Pipe_B_Clock_Gating_Disable):** DPCGMunit Pipe B Clock Gating Disable 0 = Clock gating controlled by unit enabling logic. 1 = Disable clock gating function
0	0x0 RW	**DPCGMunit Pipe A Clock Gating Disable (DPCGMunit_Pipe_A_Clock_Gating_Disable):** DPCGMunit Pipe A Clock Gating Disable 0 = Clock gating controlled by unit enabling logic. 1 = Disable clock gating function

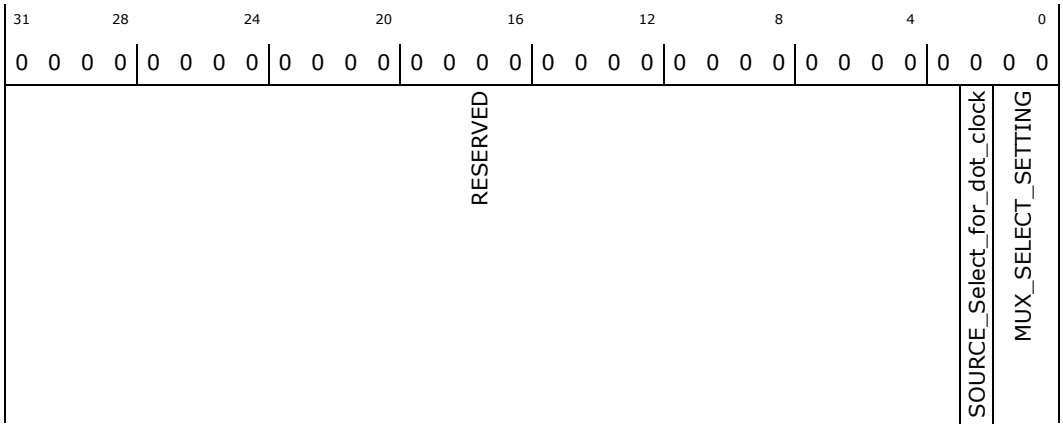
4.2.36 DOT_MIPI—Offset 6038h

Dot clock source selection for MIPI mode

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6038h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**RESERVED:** (read only).
2	0x0 RW	**SOURCE_Select_for_dot_clock:** 0 = Mux Select is based on sTAP setting in clk 1 = Mux Select is based on display configuration
1:0	0x0 RW	**MUX_SELECT_SETTING:** Default=1'b00 Set this field to 2b'01 for MIPI use cases

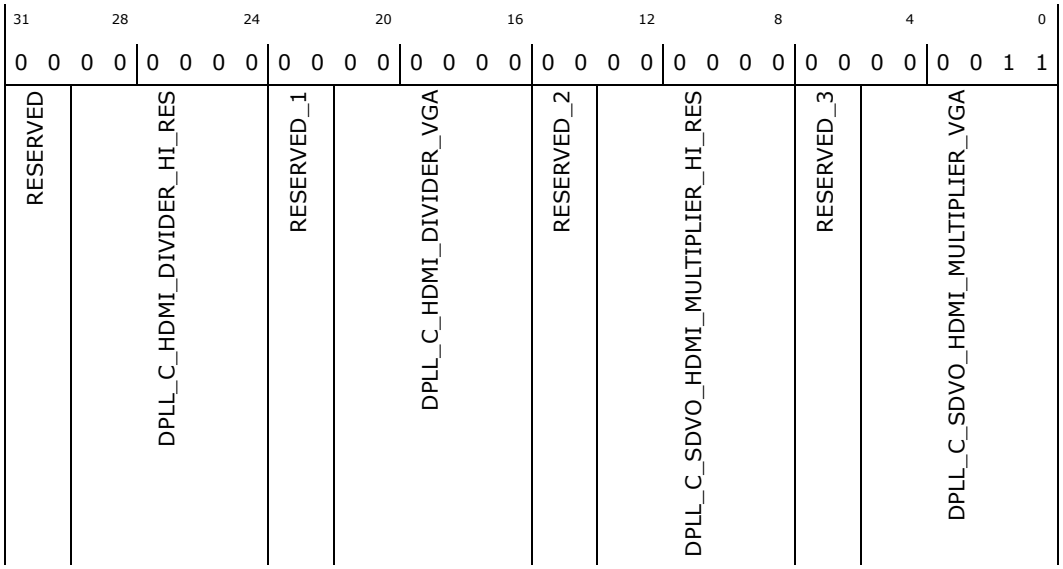
4.2.37 DPLLCMD—Offset 603Ch

DPLL C SDVO/HDMI Multiplier/Divisor Register Pipe C multiply (cpdmmreg.v reg15_lt)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 603Ch

Default: 00000003h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RESERVED:** Reserved.
29:24	0x0 RW	**DPLL_C_HDMI_DIVIDER_HI_RES:** When the source is high resolution, this field determines the number of pixels to be included in the multiplied packet defined by the SDVO/HDMI multiplier. For SDVO and CRT, the only valid setting is 1x. HDMI example: If the pixel clock on the display should be 180MHz and the display PLL is set to 270MHz, two pixels and one fill code must be sent over HDMI (fixed frequency mode only). Therefore, the HDMI divider should be set to 2 and the SDVO/HDMI multiplier should be set to 3, since 180 MHz (pixel clock) = 2/3*270MHz (link character clock) This divider must be set to 1x for any mode except HDMI fixed frequency mode. Value in this register = number of pixels per packet 1 Default: 0000 1 pixel per packet (Default value, must be set to 1x for any mode except HDMI fixed frequency mode) Range: 0-63 (1 pixel per packet 64 pixels per packet)
23:22	0x0 RO	**RESERVED_1:** Reserved.
15:14	0x0 RO	**RESERVED_2:** Reserved.
13:8	0x0 RW	**DPLL_C_SDVO_HDMI_MULTIPLIER_HI_RES:** This field determines the data multiplier for sDVO and is also applied to CRT. In order to keep the clock rate to a more narrow range of rates, the multiplier is set and the Display PLL programmed to a multiple of the display mode s actual clock rate. This is unrelated to the pixel multiply that is selectable per plane. 6x and higher multipliers can only be used for HDMI mode. Value in this register = multiplication factor - 1 Default: 000000 (1X) Range: 0 63 (1X 64X)

Bit Range	Default & Access	Field Name (ID): Description
7:6	0x0 RO	**RESERVED_3:** Reserved.

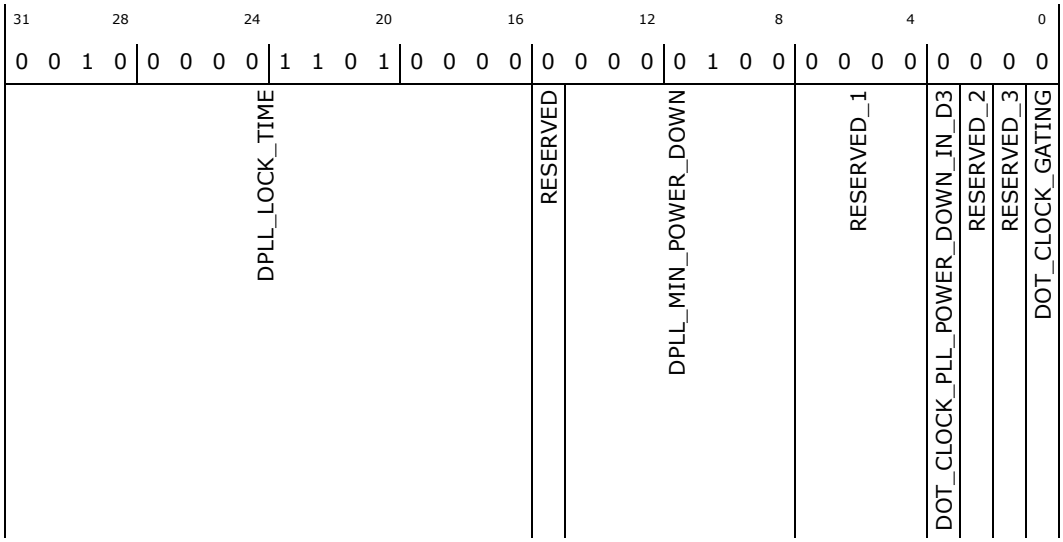
4.2.38 D_STATE—Offset 6104h

D State Function Control Register Power state behavior (cpdmmreg.v reg11_lt)

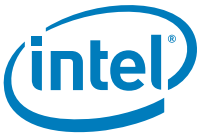
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6104h

Default: 20D00400h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x20d0 RW	**DPLL_LOCK_TIME:** This is the time required to the DPLL to relock. The counter using the HRAW clk (5nsec) and resolution of 5nsec. (SEG DPLL lock time is 42usec)
15	0x0 RO	**RESERVED:** : MBZ
14:8	0x4 RW	**DPLL_MIN_POWER_DOWN:** This is the minimum time required the DPLL to be power down until it is allowed to turn it on again. The HW counter using HRAW clk (5nsec) and has resolution of 160nsec (SEG DPLL required time is 0.5usec)
7:4	0x0 RO	**RESERVED_1:** : MBZ



Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**DOT_CLOCK_PLL_POWER_DOWN_IN_D3:** This bit determines whether the PCI Power State Powers down the Dot Clock PLLs when in D3. A 0 on this bit does not power down the DPLLs, requiring software to gate them if necessary. When this bit is a 1, the dot PLLs are powered down when in D3. The PCI power state is determined by bits 1:0 of the PCI Power Management Control/Status register.
2	0x0 RO	**RESERVED_2:** Reserved.
1	0x0 RO	**RESERVED_3:** Graphics Core Clock Gating: This bit determines whether the PCI Power State gates the Graphics Core clocks when in the D3 state. A 0 on this bit does not gate the clocks, requiring software to gate them if necessary. When this bit is a 1, the graphics core clocks are gated at the outputs of the PLLs when in D3. The PCI power state is determined by bits 1:0 of the PCI Power Management Control/Status register. This register field has no use in current products.
0	0x0 RW	**DOT_CLOCK_GATING:** This bit determines whether the PCI Power State gates the Dot clocks when in the D3 state. A 0 on this bit does not gate the clocks, requiring software to gate them if necessary. When this bit is a 1, the dot clocks are gated at the outputs of the PLLs when in D3. The PCI power state is determined by bits 1:0 of the PCI Power Management Control/Status register.

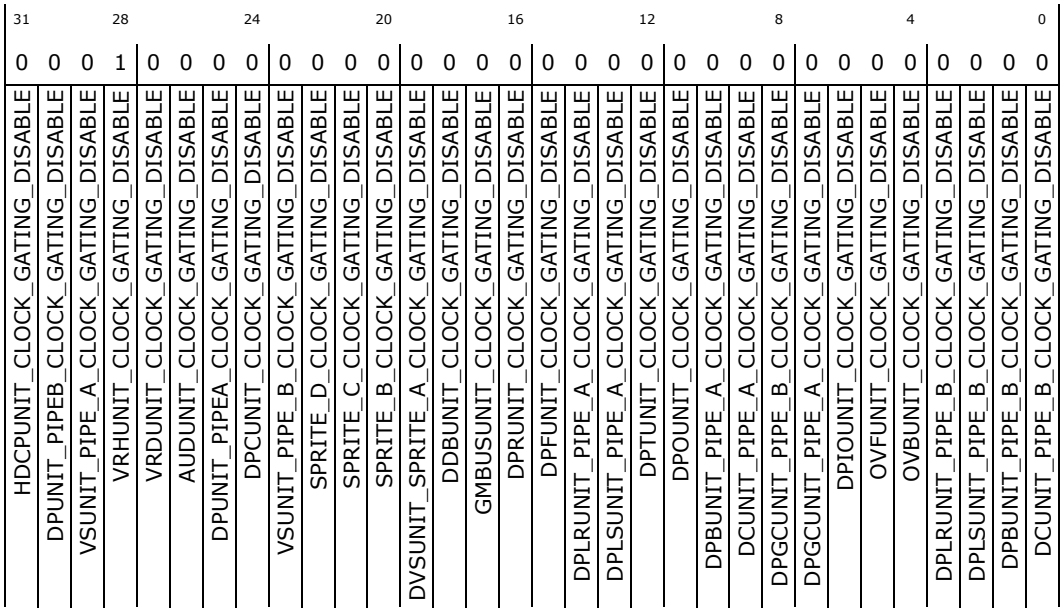
4.2.39 DSPCLK_GATE_D—Offset 6200h

Clock Gating Disable for Display Register clock gating (cpdmmreg.v reg12_lt)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6200h

Default: 10000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**HDCPUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW]: Reserved. MBZ. This bit is not connected on [DevBW].
30	0x0 RW	**DPUNIT_PIPEB_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
29	0x0 RW	**VSUNIT_PIPE_A_CLOCK_GATING_DISABLE:** (this bit used to be in PCI space in Calistoga) 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
28	0x1 RW	**VRHUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logicg 1 = Disable clock gating function Clock gating should not be enabled for this unit (this bit should always be set to 1.) [DevBW]: Reserved. MBZ. This bit is not connected on [DevBW].
27	0x0 RW	**VRDUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
26	0x0 RW	**AUDUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW]: Reserved. MBZ. This bit is not connected on [DevBW].
25	0x0 RW	**DPUNIT_PIPEA_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function

Bit Range	Default & Access	Field Name (ID): Description
24	0x0 RW	**DPCUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
23	0x0 RW	**VSUNIT_PIPE_B_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW]: Reserved. MBZ. This bit is not connected on [DevBW].
22	0x0 RW	**SPRITE_D_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
21	0x0 RW	**SPRITE_C_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW]: Reserved. MBZ. This bit is not connected on [DevBW].
20	0x0 RW	**SPRITE_B_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW] and [DevBLC]: Reserved. MBZ. This bit is not connected on [DevBW] and [DevBLC].
19	0x0 RW	**DVSUNIT_SPRITE_A_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBLC] and [DevCTG]: Reserved. MBZ. This bit is not connected on [DevBLC] and [DevCTG].
18	0x0 RW	**DDBUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevCTG] Always program this bit to 1
17	0x0 RW	**GMBUSUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
16	0x0 RW	**DPRUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
15	0x0 RW	**DPFUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
14	0x0 RW	**DPLRUNIT_PIPE_A_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW] and [DevBLC]: Reserved. MBZ. This bit is not connected on [DevBW] and [DevBLC].
13	0x0 RW	**DPLSUNIT_PIPE_A_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW] and [DevBLC]: Reserved. MBZ. This bit is not connected on [DevBW] and [DevBLC].

Bit Range	Default & Access	Field Name (ID): Description
12	0x0 RW	**DPTUNIT_CLOCK_GATING_DISABLE:** Dplunit Clock Gating Disable: 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBW] and [DevBLC]: Reserved. MBZ. This bit is not connected on [DevBW] and [DevBLC].
11	0x0 RW	**DPOUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
10	0x0 RW	**DPBUNIT_PIPE_A_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
9	0x0 RW	**DCUNIT_PIPE_A_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
8	0x0 RW	**DPGCUNIT_PIPE_B_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
7	0x0 RW	**DPGCUNIT_PIPE_A_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
6	0x0 RW	**DPIOUNIT_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
5	0x0 RW	**OVFUNIT_CLOCK_GATING_DISABLE:** [DevCTG] DPFCunit Clock Gating Disable: 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
4	0x0 RW	**OVBUNIT_CLOCK_GATING_DISABLE:** [DevCTG] DPFDunit Clock Gating Disable: 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
3	0x0 RW	**DPLRUNIT_PIPE_B_CLOCK_GATING_DISABLE:**
2	0x0 RW	**DPLSUNIT_PIPE_B_CLOCK_GATING_DISABLE:**
1	0x0 RW	**DPBUNIT_PIPE_B_CLOCK_GATING_DISABLE:** Ovuunit Clock Gating Disable: 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBLC] and [DevCTG]: Reserved. MBZ. This bit is not connected on [DevBLC] and [DevCTG].
0	0x0 RW	**DCUNIT_PIPE_B_CLOCK_GATING_DISABLE:** Ovlunit Clock Gating Disable: 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function [DevBLC] and [DevCTG]: Reserved. MBZ. This bit is not connected on [DevBLC] and [DevCTG].

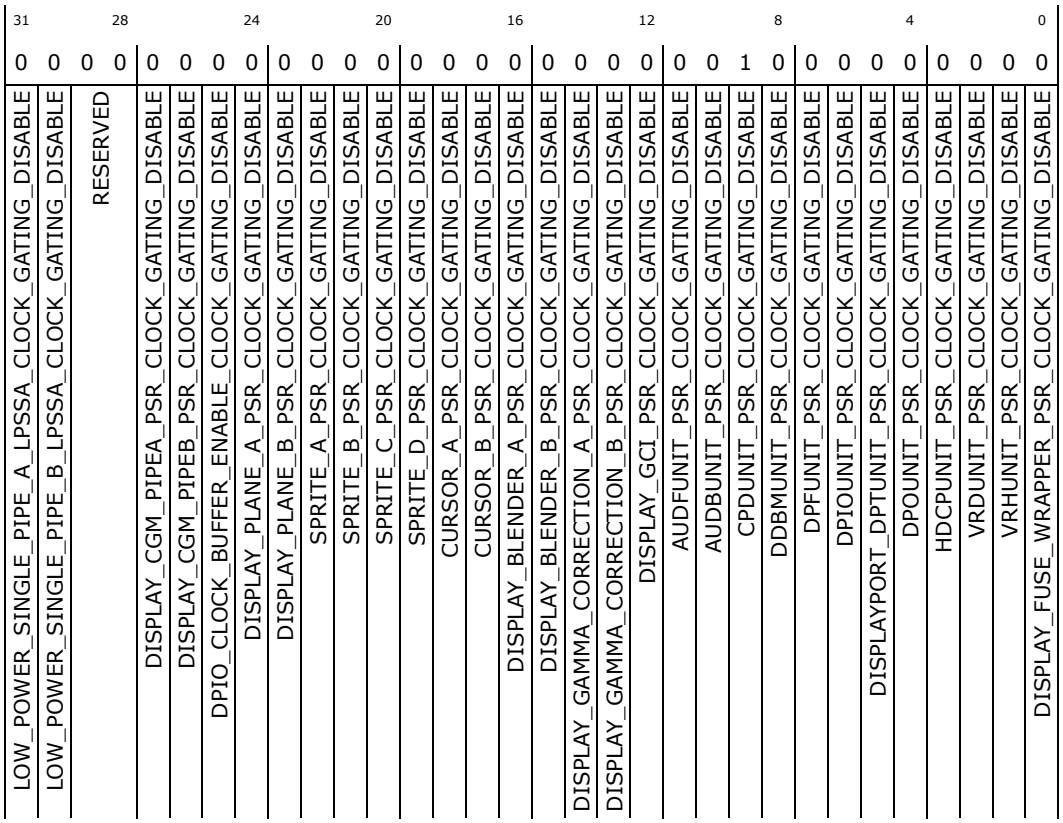
4.2.40 DPPSR_CGDIS—Offset 6204h

Panel Self Refresh Clock Gating Disable for Display PSR clock gating disable controls (cpdmmreg.v)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6204h

Default: 00000200h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**LOW_POWER_SINGLE_PIPE_A_LPSSA_CLOCK_GATING_DISABLE:** 0 = clock gating controlled by enabling logic. Pipe A shall be enabled 1 = Disable trunk clock gating on pipe A even when LPSSA is on
30	0x0 RW	**LOW_POWER_SINGLE_PIPE_B_LPSSA_CLOCK_GATING_DISABLE:** 0 = clock gating controlled by enabling logic. Pipe B shall be enabled 1 = Disable trunk clock gating on pipe B even when LPSSA is on
29:28	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
27	0x0 RW	**DISPLAY CGM PIPEA PSR Clock Gating Disable (DISPLAY_CGM_PIPEA_PSR_CLOCK_GATING_DISABLE):** 0 = clock gating controlled by enabling logic. Pipe A shall be enabled 1 = Disable clock gating
26	0x0 RW	**DISPLAY CGM PIPEB PSR Clock Gating Disable (DISPLAY_CGM_PIPEB_PSR_CLOCK_GATING_DISABLE):** 0 = clock gating controlled by enabling logic. Pipe B shall be enabled 1 = Disable clock gating
25	0x0 RW	**DPIO_CLOCK_BUFFER_ENABLE_CLOCK_GATING_DISABLE:** 0 = clock gating controlled by DPIO clock buffer enable 1=Disable clock gating function by DPIO clock buffer enable
24	0x0 RW	**DISPLAY_PLANE_A_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
23	0x0 RW	**DISPLAY_PLANE_B_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
22	0x0 RW	**SPRITE_A_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
21	0x0 RW	**SPRITE_B_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
20	0x0 RW	**SPRITE_C_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
19	0x0 RW	**SPRITE_D_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
18	0x0 RW	**CURSOR_A_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
17	0x0 RW	**CURSOR_B_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
16	0x0 RW	**DISPLAY_BLENDER_A_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
15	0x0 RW	**DISPLAY_BLENDER_B_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
14	0x0 RW	**DISPLAY_GAMMA_CORRECTION_A_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
13	0x0 RW	**DISPLAY_GAMMA_CORRECTION_B_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function

Bit Range	Default & Access	Field Name (ID): Description
12	0x0 RW	**DISPLAY_GCI_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
11	0x0 RW	**AUDFUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function(default)
10	0x0 RW	**AUDBUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
9	0x1 RW	**CPDUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function (default)
8	0x0 RW	**DDBMUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
7	0x0 RW	**DPFUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
6	0x0 RW	**DPIOUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
5	0x0 RW	**DISPLAYPORT_DPTUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
4	0x0 RW	**DPOUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
3	0x0 RW	**HDCPUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
2	0x0 RW	**VRDUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
1	0x0 RW	**VRHUNIT_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
0	0x0 RW	**DISPLAY_FUSE_WRAPPER_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function

4.2.41 RAMCLK_GATE_D—Offset 6210h

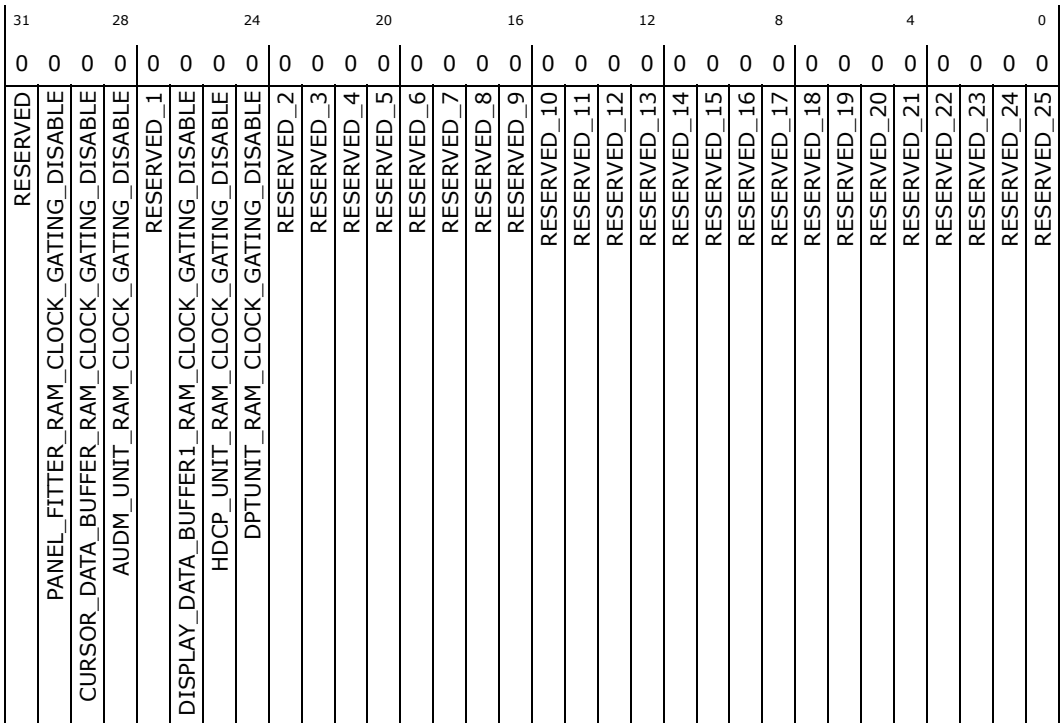
GFX RAM Clock Gating Disable Register memory clock gating (cpdmmreg.v gfxramcg2)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

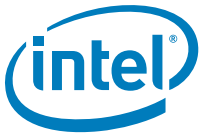
Offset: 6210h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RESERVED:** TVOUT RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
30	0x0 RW	**PANEL_FITTER_RAM_CLOCK_GATING_DISABLE:** 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
29	0x0 RW	**CURSOR_DATA_BUFFER_RAM_CLOCK_GATING_DISABLE:** 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
28	0x0 RW	**AUDM_UNIT_RAM_CLOCK_GATING_DISABLE:** [DeBLC] Reserved. [DevCL] WIZ Z coeff readback return FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
27	0x0 RW	**RESERVED_1:** [DevCTG] DPFC Unit RAM Clock Gating Disable: [DevBLC] Reserved. [DevCL] Display Data Buffer2 (Overlay) Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function

Bit Range	Default & Access	Field Name (ID): Description
26	0x0 RW	**DISPLAY_DATA_BUFFER1_RAM_CLOCK_GATING_DISABLE:** 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
25	0x0 RW	**HDCP_UNIT_RAM_CLOCK_GATING_DISABLE:** [DevCL] ME RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
24	0x0 RW	**DPTUNIT_RAM_CLOCK_GATING_DISABLE:** DPIOM Unit RAM Clock Gating Disable: [DevBLC] Reserved. [DevCL] WIZ polygon FIFO RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
23	0x0 RW	**RESERVED_2:** [DevBLC] and [DevCTG] Reserved. [DevCL] VF RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
22	0x0 RW	**RESERVED_3:** [DevBLC] and [DevCTG] Reserved. [DevCL] SF RAMClock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
21	0x0 RW	**RESERVED_4:** [DevBLC] and [DevCTG] Reserved. [DevCL] WMIZ Latency FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
20	0x0 RW	**RESERVED_5:** [DevBLC] and [DevCTG] Reserved. [DevCL] TC FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
19	0x0 RW	**RESERVED_6:** [DevCL] SV FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
18	0x0 RW	**RESERVED_7:** [DevBLC] and [DevCTG] BD Unit RAM Clock Gating Disable: [DevCL] Latency FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
17	0x0 RW	**RESERVED_8:** [DevBLC] and [DevCTG] BF Unit RAM Clock Gating Disable: [DevCL] URB Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function



Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW	**RESERVED_9:** [DevBLC] and [DevCTG] CS Unit RAM Clock Gating Disable: [DevCL] L2 Instruction Tag RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
15	0x0 RW	**RESERVED_10:** [DevCTG] FH Unit RAM Clock Gating Disable: [DevCL] Data RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
14	0x0 RW	**RESERVED_11:** [DevBLC] and [DevCTG] Reserved. [DevCL] TAG RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
13	0x0 RW	**RESERVED_12:** [DevBLC] and [DevCTG] Reserved. [DevCL] L2 Instruction Cache Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
12	0x0 RW	**RESERVED_13:** [DevBLC] and [DevCTG] Reserved. [DevCL] MRFRAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
11	0x0 RW	**RESERVED_14:** [DevBLC] and [DevCTG] VFM Unit RAM Clock Gating Disable: [DevCL] GRF RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
10	0x0 RW	**RESERVED_15:** [DevBLC] and [DevCTG] SFM Unit RAM Clock Gating Disable: [DevCL] Data Cache CAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
9	0x0 RW	**RESERVED_16:** [DevBLC] and [DevCTG] WIZM Unit RAM Clock Gating Disable: [DevCL] Data Cache Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
8	0x0 RW	**RESERVED_17:** [DevBLC] and [DevCTG] URB Unit RAM Clock Gating Disable: [DevCL] Render Cache Latency FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
7	0x0 RW	**RESERVED_18:** [DevBLC] and [DevCTG] IC Unit RAM Clock Gating Disable: [DevCL] Render PA Tag RAM (Z) Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function

Bit Range	Default & Access	Field Name (ID): Description
6	0x0 RW	**RESERVED_19:** [DevBLC] and [DevCTG] ISC Unit RAM Clock Gating Disable: [DevCL] Render PA Tag RAM (Color) Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
5	0x0 RW	**RESERVED_20:** [DevBLC] and [DevCTG] GA Unit RAM Clock Gating Disable: [DevCL] Render Cache Write Back FIFO Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
4	0x0 RW	**RESERVED_21:** [DevBLC] and [DevCTG] MS Unit RAM Clock Gating Disable: [DevCL] Render Cache (Z) Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
3	0x0 RW	**RESERVED_22:** [DevBLC] and [DevCTG] RCBP Unit RAM Clock Gating Disable: [DevCL] Render Cache (color) Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
2	0x0 RW	**RESERVED_23:** [DevBLC] and [DevCTG] RCC Unit RAM Clock Gating Disable: [DevCL] L2 Mapping Cache CAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
1	0x0 RW	**RESERVED_24:** [DevBLC] and [DevCTG] RCZ Unit RAM Clock Gating Disable: [DevCL] L2 Mapping Tag RAM Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function
0	0x0 RW	**RESERVED_25:** [DevBLC] and [DevCTG] MT Unit RAM Clock Gating Disable: [DevCL] L2 Mapping Cache Clock Gating Disable: 0 = Enable RAM bank clock gating function (default) 1 = Disable RAM bank clock gating function

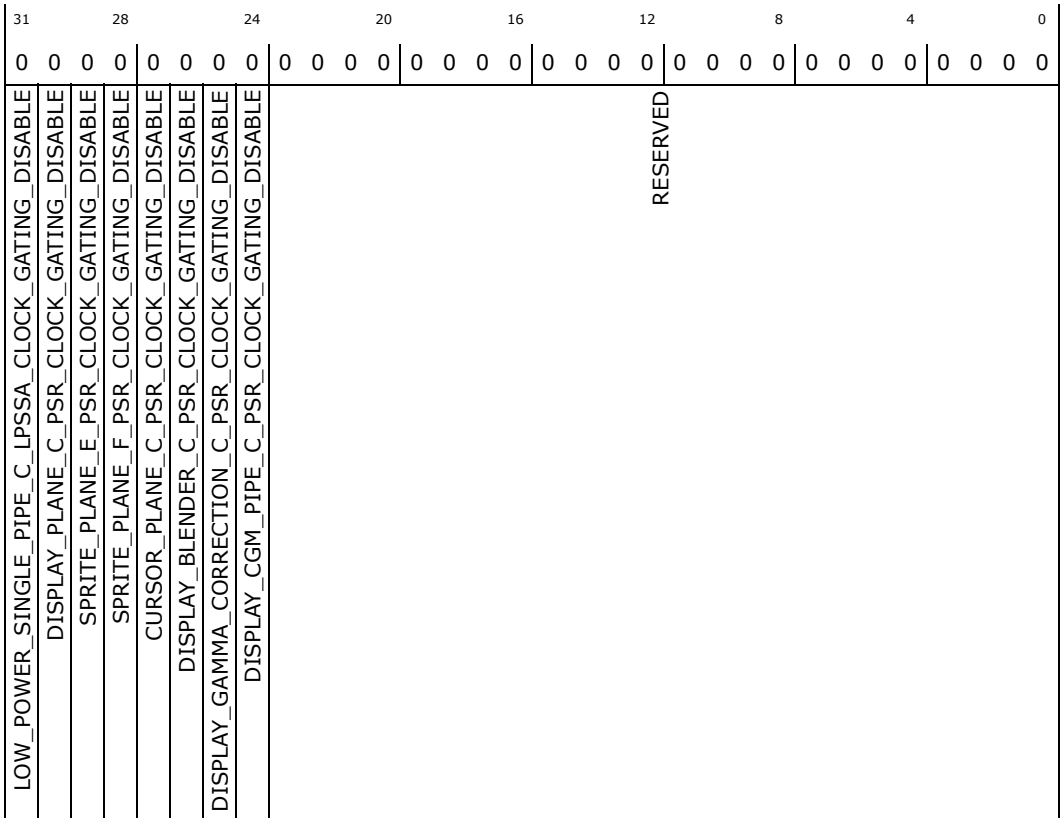
4.2.42 DPPSR1_CGDIS—Offset 6220h

Panel Self Refresh Clock Gating Disable for Display PSR clock gating disable controls (cpdmmreg.v)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6220h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**LOW_POWER_SINGLE_PIPE_C_LPSSA_CLOCK_GATING_DISABLE:** 0 = clock gating controlled by enabling logic. Pipe C shall be enabled 1 = Disable trunk clock gating on pipe C even when LPSSA is on
30	0x0 RW	**DISPLAY_PLANE_C_PSR_CLOCK_GATING_DISABLE:** 0 = clock gating controlled by enabling logic. 1 = Disable clock gating function
29	0x0 RW	**SPRITE_PLANE_E_PSR_CLOCK_GATING_DISABLE:** 0 = clock gating controlled by enabling logic. 1 = Disable clock gating function
28	0x0 RW	**SPRITE_PLANE_F_PSR_CLOCK_GATING_DISABLE:** 0 = clock gating controlled by enabling logic. 1 = Disable clock gating function
27	0x0 RW	**CURSOR_PLANE_C_PSR_CLOCK_GATING_DISABLE:** 0 = clock gating controlled by enabling logic. 1 = Disable clock gating function
26	0x0 RW	**DISPLAY_BLENDER_C_PSR_CLOCK_GATING_DISABLE:** 0 = clock gating controlled by enabling logic. 1 = Disable clock gating function

Bit Range	Default & Access	Field Name (ID): Description
25	0x0 RW	**DISPLAY_GAMMA_CORRECTION_C_PSR_CLOCK_GATING_DISABLE:** 0 = clock gating controlled by DPIO clock buffer enable 1=Disable clock gating function by DPIO clock buffer enable
24	0x0 RW	**DISPLAY_CGM_PIPE_C_PSR_CLOCK_GATING_DISABLE:** 0 = Clock gating controlled by unit enabling logic 1 = Disable clock gating function
23:0	0x0 RO	**RESERVED:** RSVD

4.2.43 DPIO_PHY_STATUS—Offset 6240h

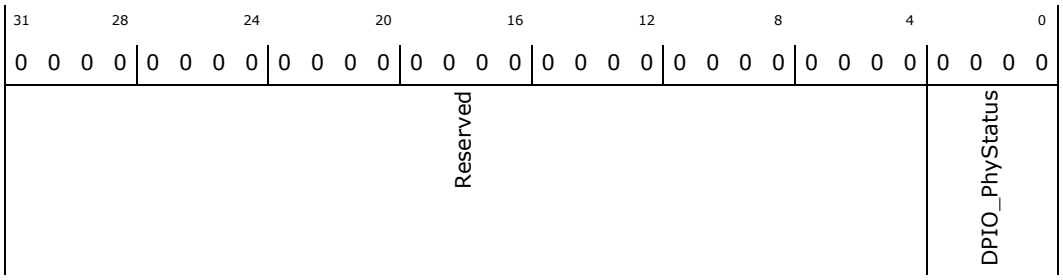
DPIO_PHY_STATUS DPIO D PHY status Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6240h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved:** Reserved
3:0	0x0 RO	**DPIO_PhyStatus:** DPIO PhyStatus(Read Only): [SoC] This field contains the 4-bit PHY lane status.

4.2.44 DSPCSS—Offset 6300h

Display connection state status DSPCSS Display Connection State Status register

Access Method

Type: Memory Mapped I/O Register (Size: 128 bits)

Offset: 6300h

Default: 00000000000000000000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
127:91	0x0 RO	**RESERVED:** : MBZ
90	0x0 RO	**RESERVED_1:** : For TV CP enable status
89	0x0 RO	**PIPE_A_HDCP_STICKY_BIT:** 1 indicates display port has been enabled on pipe A sometime when HDCP was enabled on pipe A, including at invocation of HDCP. This bit is cleared when HDCP is disabled on pipe A.
88	0x0 RO	**PIPE_B_HDCP_STICKY_BIT:** 1 indicates display port has been enabled on pipe B sometime when HDCP was enabled on pipe B, including at invocation of HDCP. This bit is cleared when HDCP is disabled on pipe B.
87	0x0 RO	**RESERVED_2:** : For LVDS CP enable status
86	0x0 RO	**RESERVED_3:** LVDS Pipe A HDCP sticky bit
85	0x0 RO	**RESERVED_4:** LVDS Pipe B HDCP sticky bit
84	0x0 RO	**RESERVED_5:** For CRT CP enable Status
83	0x0 RO	**RESERVED_6:** CRT Pipe A Sticky Bit
82	0x0 RO	**RESERVED_7:** CRT Pipe B Sticky bit
81	0x0 RO	**HDMI_B_HDCP_ENABLE_STATUS:** Reserved.
80	0x0 RO	**HDMI_B_PIPE_A_HDCP_STICKY_BIT:** 1 indicates HDCP enabled on HDMI B on pipe A
79	0x0 RO	**HDMI_B_PIPE_B_HDCP_STICKY_BIT:** 1 indicates HDCP enabled on HDMI B on pipe B
78	0x0 RO	**HDMI_C_HDCP_ENABLE_STATUS:** Reserved.
77	0x0 RO	**HDMI_C_PIPE_A_HDCP_STICKY_BIT:** : 1 indicates HDCP enabled on HDMI C on pipe A
76	0x0 RO	**HDMI_C_PIPE_B_HDCP_STICKY_BIT:** : 1 indicates HDCP enabled on HDMI C on pipe B
75:73	0x0 RO	**RESERVED_8:** : Bits reserved for giving the future status of HDMI D/DVI port.
72	0x0 RO	**DISPLAY_PORT_B_HDCP_ENABLE_STATUS:** Reserved.
71	0x0 RO	**DISPLAY_PORT_B_PIPE_A_HDCP_STICKY_BIT:** : 1 indicates HDCP enabled on eDP/DP B on pipe A
70	0x0 RO	**DISPLAY_PORT_B_PIPE_B_HDCP_STICKY_BIT:** : (1 indicates HDCP enabled on eDP/DP B on pipe B
69	0x0 RO	**DISPLAY_PORT_C_HDCP_ENABLE_STATUS:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
68	0x0 RO	**DISPLAY_PORT_C_PIPE_A_HDCP_STICKY_BIT:** : 1 indicates HDCP enabled on eDP/DP C on pipe A
67	0x0 RO	**DISPLAY_PORT_C_PIPE_B_HDCP_STICKY_BIT:** : 1 indicates HDCP enabled on eDP/DP C on pipe B
66	0x0 RO	**RESERVED_9:** Display Port D HDCP enable status
65	0x0 RO	**RESERVED_10:** Display Port D Pipe A HDCP sticky bit
64	0x0 RO	**RESERVED_11:** Display Port D Pipe B HDCP sticky bit
63:48	0x0 RO	**RESERVED_12:** mbz
47:32	0x0 RO	**RESERVED_13:** : mbz
31:0	0x0 RO	**RESERVED_14:** : mbz

4.2.45 FW_BLC_SELF—Offset 6500h

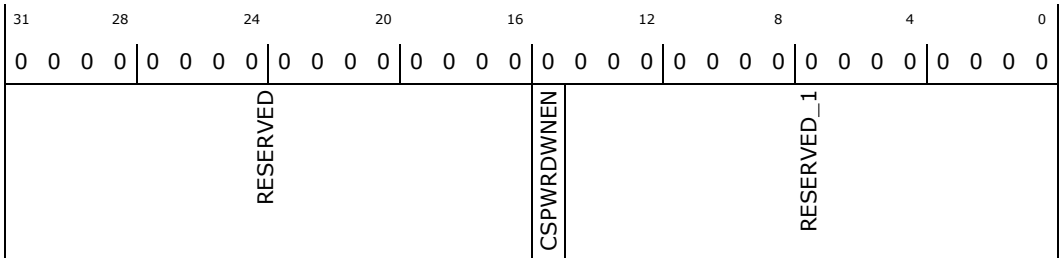
Display FIFO Watermark

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6500h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**CSPWRDWNEN:** 1 = Display FIFO can go into max_fifo configuration if only one plane A/B is enabled and all other planes, including overlay, are off. 0 = Dont put display FIFO in max_fifo configuration
14:0	0x0 RO	**RESERVED_1:** Reserved.

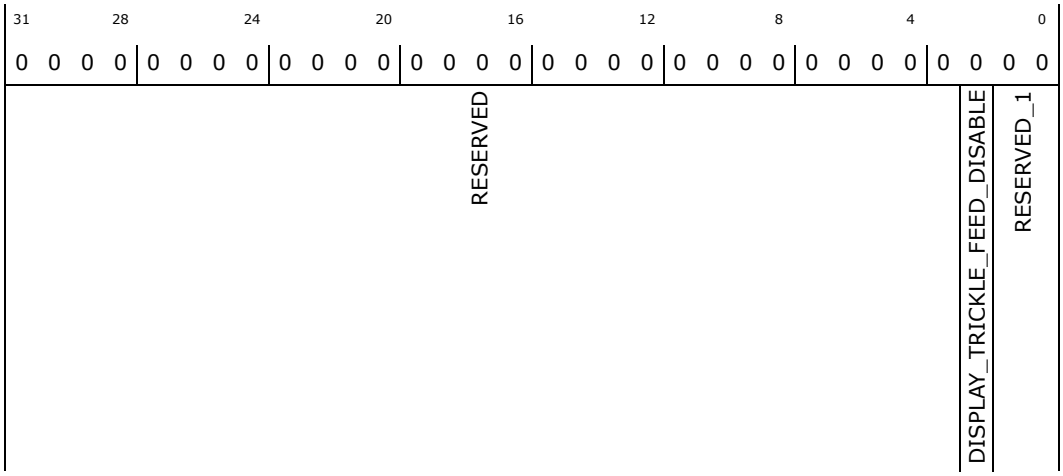
4.2.46 MI_ARB—Offset 6504h

Display Arbiter

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6504h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**RESERVED:** Reserved.
2	0x0 RW	**DISPLAY_TRICKLE_FEED_DISABLE:** 1 Disable (Turn off trickle feed Display request). 0 Enable (Default)
1:0	0x0 RO	**RESERVED_1:** Reserved.

4.2.47 CZCLK_CDCLK_FREQ_RATIO—Offset 6508h

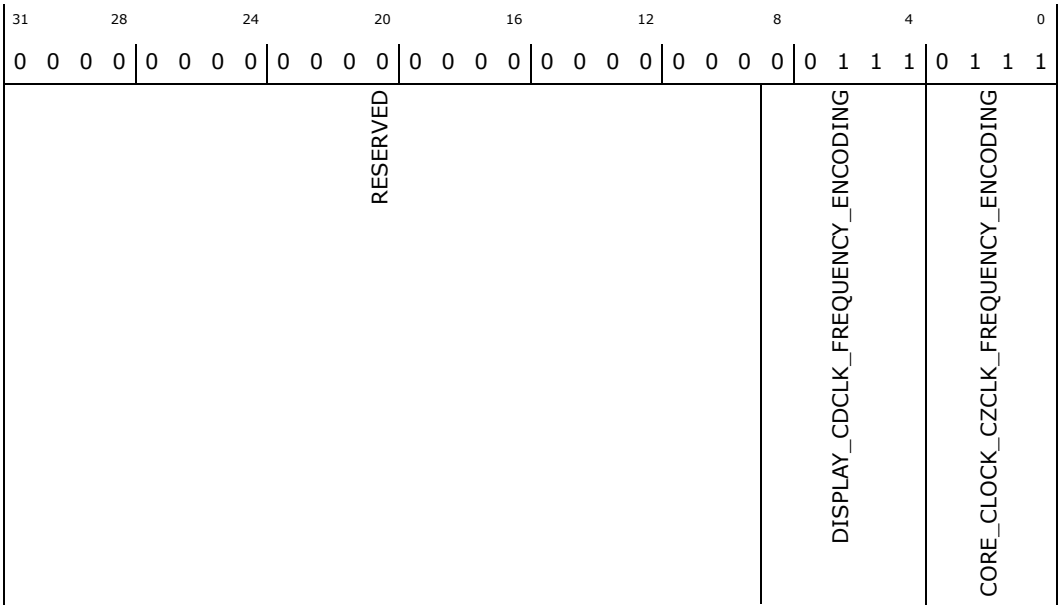
Display CZCLK/CDCLK FREQ Ratio for RMBUS sync

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6508h

Default: 00000077h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**RESERVED:** Reserved.
8:4	0x7 RO	**DISPLAY_CDCLK_FREQUENCY_ENCODING:** DISPLAY CDCLK FREQUENCY ENCODING (* symbol frequencies are POR) |_____| |=====CDCLK FREQ.======|===CDCLK DEVIDE RATIO===|==CD REGISTER ENCODING==|===SKU200==|===SKU266====|====SKU333===|====CD======| |=====ENCODING=========|=======(DECIMAL)========|===VCO 800=|===VCO 1600==|====VCO 2000=|===QUAL GEN=| |======5'b00001========|=====(MHz)===|====RATIO===| |_____| |==========|==========1==========|=====800===|====1600=====|===2000=====|======1=====| |_____|

Bit Range	Default & Access	Field Name (ID): Description
8:4	0x7 RO	|======5'b00010========|=========1.5===========|==========2===========|=====533===|====1067=====|=====1333=====|======2=====| |_____| |======5'b00011========|===========2===========|==========3===========|=====400===|=====800=====|=====1000=====|======3=====| |_____| |======5'b00100========|=========2.5===========|==========4===========|=====320*==|=====640=====|=====800=====|======4=====| |_____| |======5'b00101========|===========3===========|==========5===========|=====267*==|=====533=====|=====667=====|======5=====| |_____| |======5'b00111========|===========4===========|==========6===========|=====200*==|=====400=====|=====500=====|======7=====| |_____| |======5'b01000========|=========4.5===========|==========7===========|=====178===|=====356=====|=====444=====|======8=====| |_____| |======5'b01001========|===========5===========|==========9===========|=====160===|=====320*====|=====400=====|======9=====| |_____| |======5'b01011========|===========6===========|========11===========|=====133===|=====267*====|=====300*====|=====11=====| |_____| |======5'b01110========|=========7.5===========|========14===========|=====107===|=====213=====|=====267*====|=====14=====| |_____|

Bit Range	Default & Access	Field Name (ID): Description
8:4	0x7 RO	|======5'b01111========|===========8===========|========15===========|=====100===|=====200*====|=====250=====|=====15=====| |_____| |======5'b10001========|===========9===========|========17===========|======89===|=====178=====|=====222=====|=====17=====| |_____| |======5'b10011========|==========10===========|========19===========|======80===|=====160=====|=====200*====|=====19=====| |_____| |======5'b10111========|==========12===========|========23===========|======67===|=====133=====|=====167=====|=====23=====| |_____| |======5'b11101========|==========15===========|========29===========|======53===|=====107=====|=====133=====|=====29=====| |_____| |======5'b11111========|==========16===========|========31===========|======50===|=====100=====|=====125=====|=====31=====| |_____|

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x7 RO	**CORE_CLOCK_CZCLK_FREQUENCY_ENCODING:** CORE CLOCK (CZCLK) FREQUENCY ENCODING (* symbol are POR freq for each SKU) |_____ _____ _____| |=====CZCLK FREQ.======|===CZCLK DEVIDE RATIO===|==CZ REGISTER ENCODING==|===SKU200==|===SKU266====|====SKU333===|== ==CZ======| |=====ENCODING=========|=======================| =======(DECIMAL)========|===VCO 800=|===VCO 1600==|====VCO 2000=|===QUAL GEN=| |=======================|======================= |=======================|====(MHz)==|===(MHz)===== |=====(MHz)===|====RATIO===| |_____ _____ _____| |======5'b00001========|===========1===========|== =========1===========|=====800===|====1600=====|= ===2000=====|======1=====| |_____ _____ _____| |======5'b00010========|=========1.5===========|== =========2===========|=====533===|====1067=====|= ===1333=====|======2=====| |_____ _____ _____| |======5'b00011========|===========2===========|== =========3===========|=====400===|=====800=====|= ===1000=====|======3=====| |_____ _____ _____| |======5'b00100========|=========2.5===========|== =========4===========|=====320===|=====640=====|= ====800=====|======4=====| |_____ _____ _____| |======5'b00101========|===========3===========|== =========5===========|=====267===|=====533=====|= ====667=====|======5=====| |_____ _____ _____| |======5'b00111========|===========4===========|== =========6===========|=====200*==|=====400=====|= ====500=====|======7=====|

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x7 RO	|_____ _____ _____| |======5'b01000========|=========4.5============|== =========7============|=====178===|=====356=====|= ====444=====|======8=====| |_____ _____ _____| |======5'b01001========|===========5============|== =========9============|=====160===|=====320=====|= ====400=====|======9=====| |_____ _____ _____| |======5'b01011========|===========6============|== ========11============|=====133===|=====267*====|= ====333*====|=====11=====| |_____ _____ _____| |======5'b01110========|=========7.5============|== ========14============|=====107===|=====213=====|= ====267=====|=====14=====| |_____ _____ _____| |======5'b01111========|===========8============|== ========15============|=====100===|=====200*====|= ====250=====|=====15=====| |_____ _____ _____|

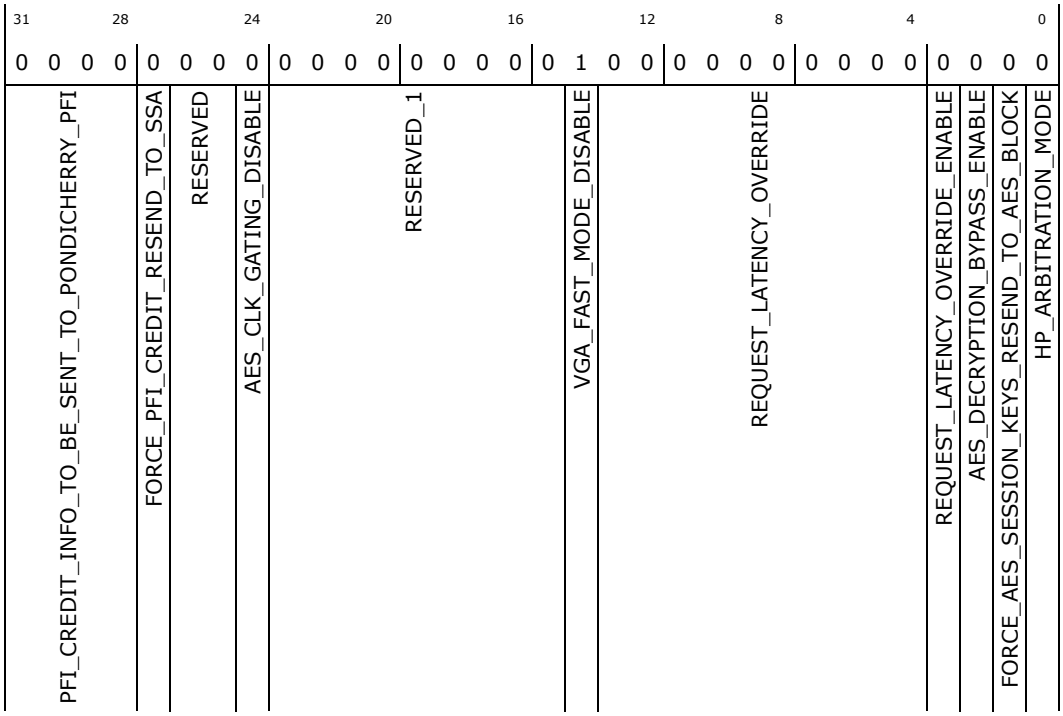
4.2.48 GCI_CONTROL—Offset 650Ch

GCI Control Register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 650Ch

Default: 00004000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW	**PFI_CREDIT_INFO_TO_BE_SENT_TO_PONDICHERRY_PFI:** Others = reserved 0111 = 15 credits 0110 = 14 credits 0101 = 13 credits 0100 = 12 credits 0011 = 11 credits 0010 = 10 credits 0001 = 9 credits 0000 = 8 credits available to PND (default) Based on the czclk/cdclk ratio, display driver has to determine the appropriate PFI credits to be used
27	0x0 RW	**FORCE PFI CREDIT RESEND TO SSA (FORCE_PFI_CREDIT_RESEND_TO_SSA):** 0 = Disable PFI credit to resend to SSA. Hardware is responsible to clear this bit after the PFI credit initialization request is sent. 1 = Enable PFI credit to resend to SSA. When driver sets this bit, Display PFI request engine will resend the new PFI credit bit [31:28] to SSA. Hardware is responsible to clear this bit after the PFI credit initialization request is sent.
26:25	0x0 RO	**RESERVED:** Reserved.
24	0x0 RW	**AES_CLK_GATING_DISABLE:** 0 = Enable clock gating for AES clock (default) 1 = Disable clock gating for AES clock

Bit Range	Default & Access	Field Name (ID): Description
23:15	0x0 RO	**RESERVED_1:** Reserved.
13:4	0x0 RW	**REQUEST_LATENCY_OVERRIDE:** If bit 3 of this register is set, the 10-btt Request Latency Override value programmed here is used as the latency offset from the global timer for requests that win arbitration. If bit 3 is not set, normal request latency from streamers is used. Programming note: This value should not be larger than the actual required request latency. Otherwise, it will cause underrun. The guideline is to use latency corresponds to low watermark level or even smaller. When this field is used, the actual request latency is defeatured, either zero or a small value is used but still not causing underrun.
3	0x0 RW	**REQUEST_LATENCY_OVERRIDE_ENABLE:** 1 = Request Latency Override values in bit[13:4] is used as the latency offset from global timer 0 = Request Latency Override values is disabled. Normal request latency from streamer is used. (default)
2	0x0 RW	**AES_DECRYPTION_BYPASS_ENABLE:** 0 = AES decryption engine is enabled (Default) 1 = AES decryption engine is bypassed
1	0x0 RW	**FORCE_AES_SESSION_KEYS_RESEND_TO_AES_BLOCK:** 0 = Disable sending AES session keys to AES when going from Panel Self Refresh (PSR) inactive to PSR active mode (Default). Hardware is responsible to clear this bit after this bit is set to resend the session keys. 1 = Enable sending AES session keys to AES engine when going from PSR inactive to PSR active mode. When driver sets this bit, PAVP engine will resend the session keys to AES engine. Hardware is responsible to clear this bit after the session keys are sent.
0	0x0 RW	**HP_ARBITRATION_MODE:** 0 = Select hierarchical arbiter 1 = Select backup round robin arbiter

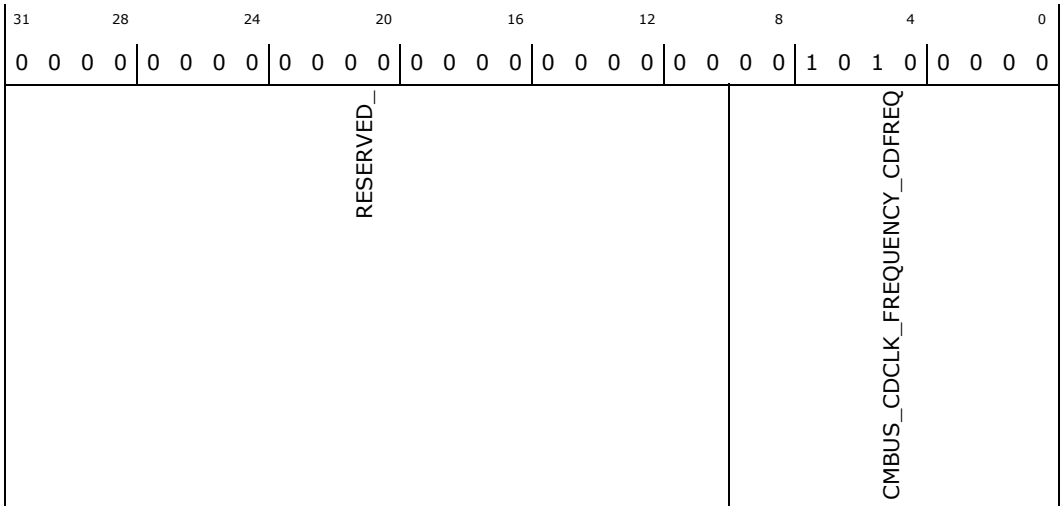
4.2.49 GMBUSFREQ—Offset 6510h

GMBUS frequency binary encoding GMBUS Frequency Binary Encoding Register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6510h

Default: 000000A0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**RESERVED_:** Reserved.
9:0	0xa0 RW	**CMBUS_CDCLK_FREQUENCY_CDFREQ:** Programming note: bit[9:2] should be programmed to the number of cdclk that generates 4MHz reference clock freq which is used to generate GMBus clock. This will vary with the cdclk freq.

4.2.50 DPALETTE_A—Offset A000h

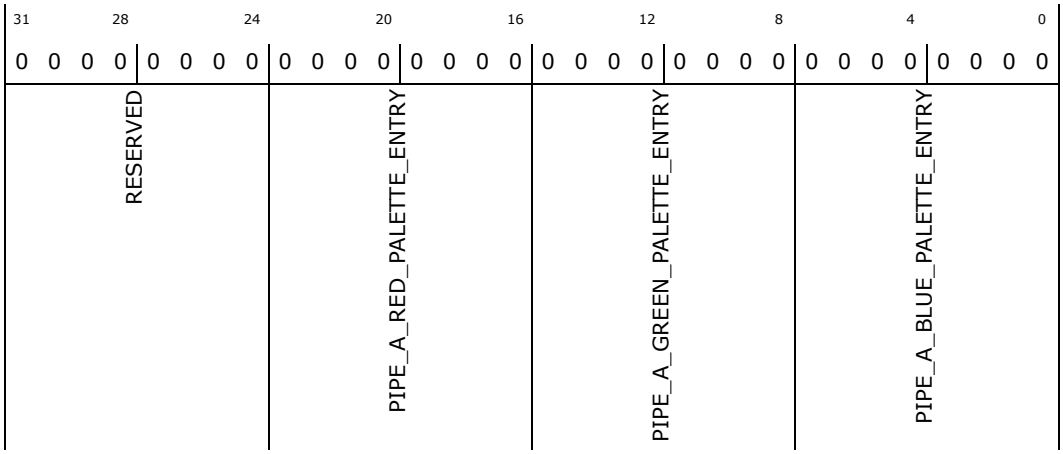
Pipe A Display Palette

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: A000h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** (read only).
23:16	0x0 RW	**PIPE_A_RED_PALETTE_ENTRY:** Reserved.
15:8	0x0 RW	**PIPE_A_GREEN_PALETTE_ENTRY:** Reserved.
7:0	0x0 RW	**PIPE_A_BLUE_PALETTE_ENTRY:** Reserved.

4.2.51 DPALETTE_B—Offset A800h

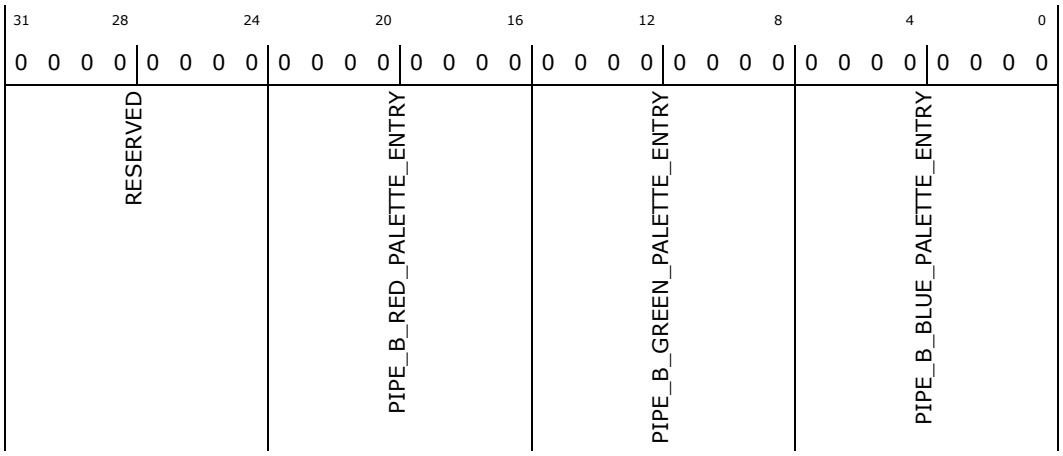
Pipe B Display Palette

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: A800h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Read Only.
23:16	0x0 RW	**PIPE_B_RED_PALETTE_ENTRY:** Reserved.
15:8	0x0 RW	**PIPE_B_GREEN_PALETTE_ENTRY:** Reserved.
7:0	0x0 RW	**PIPE_B_BLUE_PALETTE_ENTRY:** Reserved.

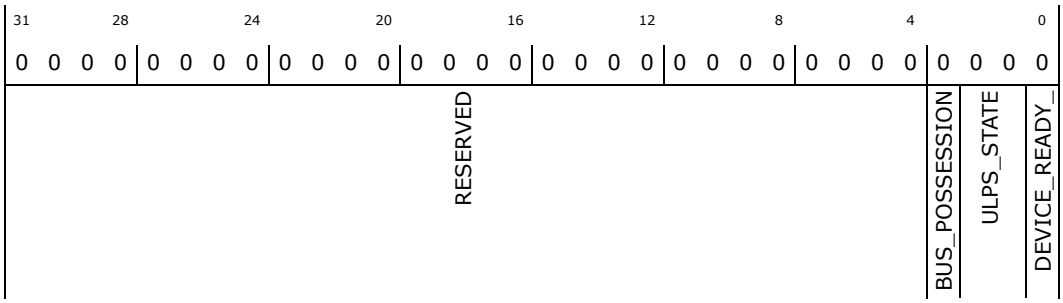
4.2.52 MIPIA_DEVICE_READY_REG—Offset B000h

MIPI A Device Ready Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** B000h

Default: 00000000h



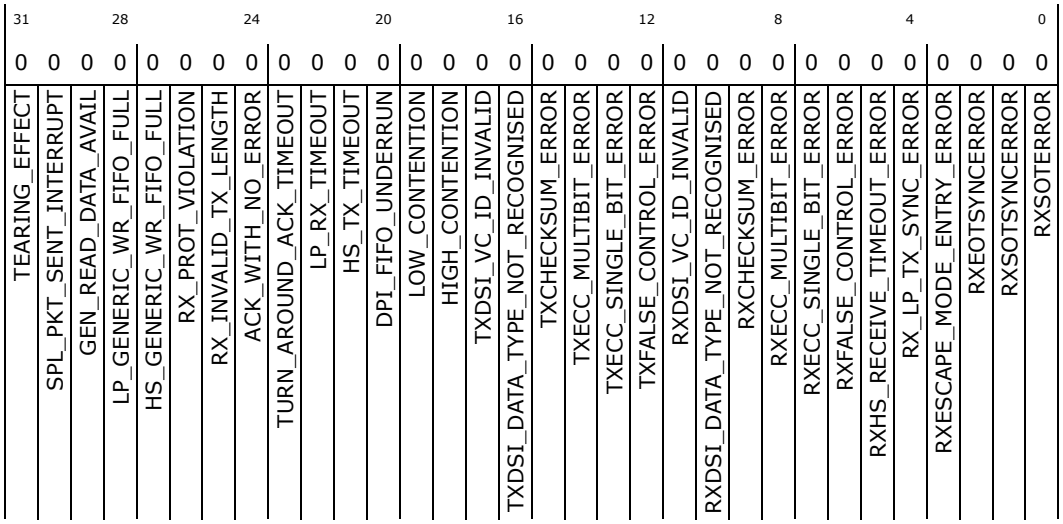
Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RESERVED:** Reserved.
3	0x0 RW	**BUS_POSSESSION:** Reserved.
2:1	0x0 RW	**ULPS_STATE:** Reserved.
0	0x0 RW	**DEVICE_READY_:** Set by the processor to inform that device is ready

4.2.53 MIPIA_INTR_STAT_REG—Offset B004h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** B004h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**TEARING_EFFECT:** Set to indicate that tearing effect trigger message is Received
30	0x0 RW	**SPL_PKT_SENT_INTERRUPT:** Set to confirm the transmission of the DPI event specific commands set in the dpi control and dpi data register
29	0x0 RW	**GEN_READ_DATA_AVAIL:** Set to indicate that the requested data for a Generic Read request is available in the buffer i.e., generic read response data is available in the read FIFO
28	0x0 RW	**LP_GENERIC_WR_FIFO_FULL:** Set to indicate that the LP generic write fifo is full
27	0x0 RW	**HS_GENERIC_WR_FIFO_FULL:** Set to indicate that the HS generic write fifo is full
26	0x0 RW	**RX_PROT_VIOLATION:** Set if DSI protocol violation error is reported in the acknowledge packet by the display device
25	0x0 RW	**RX_INVALID_TX_LENGTH:** Set if invalid transmission length error is reported in the acknowledge packet by the display device
24	0x0 RW	**ACK_WITH_NO_ERROR:** Set if acknowledge trigger message is received with out any error
23	0x0 RW	**TURN_AROUND_ACK_TIMEOUT:** Set if a turn around acknowledgement sequence is not received from the display device
22	0x0 RW	**LP_RX_TIMEOUT:** Set if a low power reception count expires this interrupt is generated
21	0x0 RW	**HS_TX_TIMEOUT:** Set if a high speed transmission prevails for more than the expected count value this interrupt is raised
20	0x0 RW	**DPI_FIFO_UNDERRUN:** Set to '1' if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver
19	0x0 RW	**LOW_CONTENTION:** Set to '1' if a LP low fault is registered by at the D-PHY contention detector

Bit Range	Default & Access	Field Name (ID): Description
18	0x0 RW	**HIGH_CONTENTION:** Set to '1' if a LP high fault is registered by at the D-PHY contention detector
17	0x0 RW	**TXDSI_VC_ID_INVALID:** Set to '1' if the received virtual channel ID is invalid
16	0x0 RW	**TXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to '1' if the received data type is not recognized
15	0x0 RW	**TXCHECKSUM_ERROR:** Set to '1' if the computed CRC differs from the received CRC value during the reception of packets by Arasan_DSI host.
14	0x0 RW	**TXECC_MULTIBIT_ERROR:** Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan_DSI_host
13	0x0 RW	**TXECC_SINGLE_BIT_ERROR:** Set to '1' if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan_DSI_host
12	0x0 RW	**TXFALSE_CONTROL_ERROR:** Set to '1' if a control error is observed on the lanes by the Arasan_DSI_host
11	0x0 RW	**RXDSI_VC_ID_INVALID:** Set to '1' if the virtual channel ID is invalid by the display device is reported in the Acknowledge packet by the display device
10	0x0 RW	**RXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to '1' if the data type is not recognized by the display device is reported in the Acknowledge packet by the display device
9	0x0 RW	**RXCHECKSUM_ERROR:** Set to '1' if the computed CRC differs from the received CRC value and is reported in the Acknowledge packet by the display device
8	0x0 RW	**RXECC_MULTIBIT_ERROR:** Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet is reported in the Acknowledge packet by the display device
7	0x0 RW	**RXECC_SINGLE_BIT_ERROR:** Set to '1' if ECC syndrome was computed and corrected for one bit error is reported in the Acknowledge packet by the display device
6	0x0 RW	**RXFALSE_CONTROL_ERROR:** Set to '1' if a control error is reported in the Acknowledge packet by the display device
5	0x0 RW	**RXHS_RECEIVE_TIMEOUT_ERROR:** Set to '1' if the high speed receive timer value expires and data transfer lasts on the data lane is reported in the Acknowledge packet by the display device
4	0x0 RW	**RX_LP_TX_SYNC_ERROR:** Set to '1' if Low power transmission sync error occurs in the display device and is reported in the Acknowledge packet by the display device
3	0x0 RW	**RXESCAPE_MODE_ENTRY_ERROR:** Set to '1' if Escape Mode Entry command is not understandable by the display device and is reported in the Acknowledge packet by the display device
2	0x0 RW	**RXEOTSYNCERROR:** Reserved.
1	0x0 RW	**RXSOTSYNCERROR:** Set to '1' if a start of transmission synchronisation error is reported in the Acknowledge packet by the display device

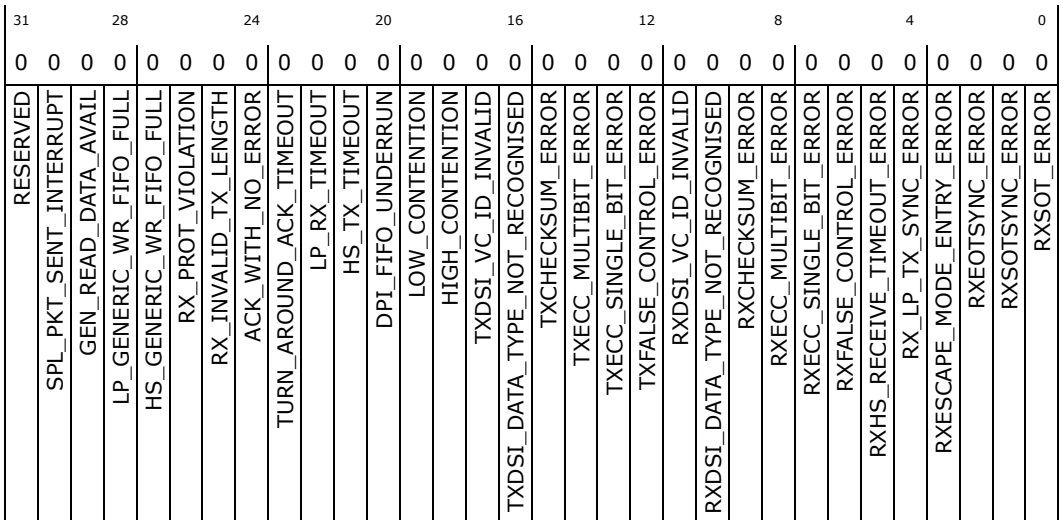
Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**RXSOTERROR:** Set to '1' if a start of transmission error is reported in the Acknowledge packet by the display device

4.2.54 MIPIA_INTR_EN_REG—Offset B008h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** B008h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** Reserved.
30	0x0 RW	**SPL_PKT_SENT_INTERRUPT:** Set to enable the confirmation of transmission of the DPI event specific commands set in the dpi control and dpi data register
29	0x0 RW	**GEN_READ_DATA_AVAIL:** Set to enable Generic Read available interrupt
28	0x0 RW	**LP_GENERIC_WR_FIFO_FULL:** Set to indicate that the LP generic write fifo is full
27	0x0 RW	**HS_GENERIC_WR_FIFO_FULL:** Set to indicate that the HS generic write fifo is full
26	0x0 RW	**RX_PROT_VIOLATION:** Set to enable protocol violation error
25	0x0 RW	**RX_INVALID_TX_LENGTH:** Set to enable invalid transmission length error
24	0x0 RW	**ACK_WITH_NO_ERROR:** Set to enable acknowledge trigger message reception with out any error

Bit Range	Default & Access	Field Name (ID): Description
23	0x0 RW	**TURN_AROUND_ACK_TIMEOUT:** Set to enable turn around acknowledgement ,sequence timeout
22	0x0 RW	**LP_RX_TIMEOUT:** Set to enable low power reception count timeouts
21	0x0 RW	**HS_TX_TIMEOUT:** Set to enable a high speed transmission timeout
20	0x0 RW	**DPI_FIFO_UNDERRUN:** Set to enable if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver
19	0x0 RW	**LOW_CONTENTION:** Set to enable a LP low fault interrupt
18	0x0 RW	**HIGH_CONTENTION:** Set to enable a LP high fault interrupt
17	0x0 RW	**TXDSI_VC_ID_INVALID:** Set to enable the interrupt if the received packets virtual channel ID is invalid
16	0x0 RW	**TXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to enable the interrupt if the received packets data type is not recognized
15	0x0 RW	**TXCHECKSUM_ERROR:** Set to enable the interrupt if the computed CRC differs from the received CRC value for the received packets
14	0x0 RW	**TXECC_MULTIBIT_ERROR:** Set to enable the interrupt if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan DSI host
13	0x0 RW	**TXECC_SINGLE_BIT_ERROR:** Set to enable the interrupt if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan DSIhost
12	0x0 RW	**TXFALSE_CONTROL_ERROR:** Set to enable the interrupt for the control error.,observed on the lanes by the Arasan_DSI_host
11	0x0 RW	**RXDSI_VC_ID_INVALID:** Set to enable the interrupt for invalid virtual channel ID in the acknowledgment packet reports
10	0x0 RW	**RXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to enable the interrupt for the un recognized data type in the acknowledgment packet reports
9	0x0 RW	**RXCHECKSUM_ERROR:** Set to enable the interrupt for the computed CRC differs from the received CRC value in the acknowledgment packet reports
8	0x0 RW	**RXECC_MULTIBIT_ERROR:** Set to enable the interrupt for no ECC correction for the packet or there are more than 2 bit errors reported in the acknowledgment packet
7	0x0 RW	**RXECC_SINGLE_BIT_ERROR:** Set to enable the interrupt for ECC syndrome computation and one bit error correction for the acknowledgment packet
6	0x0 RW	**RXFALSE_CONTROL_ERROR:** Set to enable the interrupt for control error in the acknowledgment packet reports
5	0x0 RW	**RXHS_RECEIVE_TIMEOUT_ERROR:** Set to enable the interrupt for the high speed receive timeout Error in the acknowledgment packet reports
4	0x0 RW	**RX_LP_TX_SYNC_ERROR:** Set to enable the interrupt for Low power transmission sync error in the acknowledgment packet reports

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**RXESCAPE_MODE_ENTRY_ERROR:** Set to enable the interrupt for Escape Mode Entry command error in the acknowledgment packet reports
2	0x0 RW	**RXEOTSYNC_ERROR:** Set to enable the interrupt for End of transmission synchronisation Error in the acknowledgement packet reports
1	0x0 RW	**RXSOTSYNC_ERROR:** Set to enable the interrupt for start of transmission synchronisation error in the acknowledgement packet reports
0	0x0 RW	**RXSOT_ERROR:** Set to enable the interrupt for start of transmission error in the acknowledgment packet reports

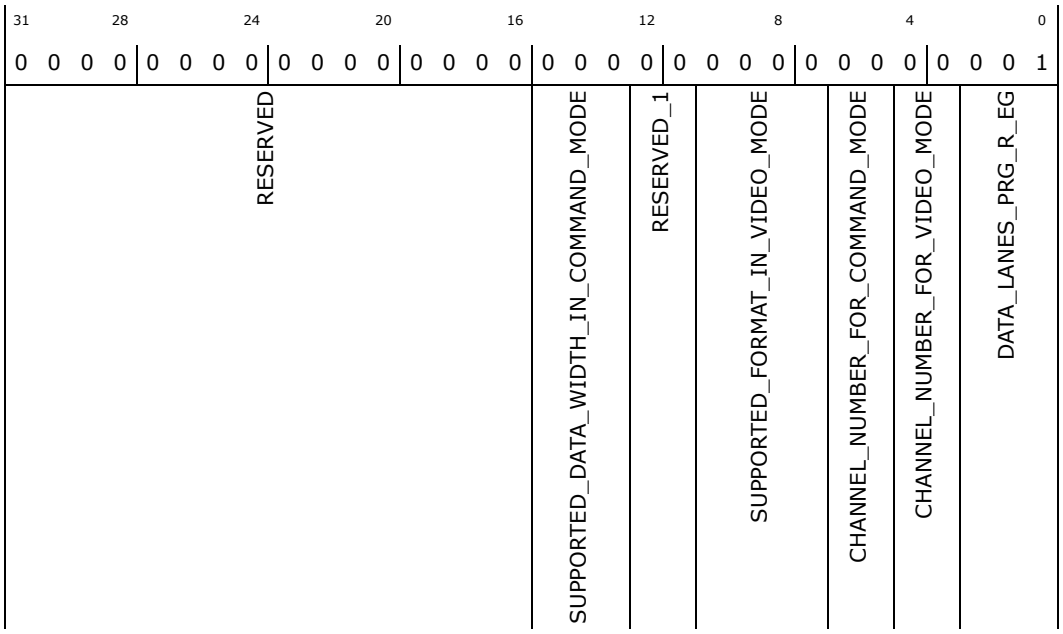
4.2.55 MIPIA_DSI_FUNC_PRG__REG—Offset B00Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B00Ch

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:13	0x0 RW	**SUPPORTED_DATA_WIDTH_IN_COMMAND_MODE:** 000 --) Reserved, 001 --) 16 bit data , 010 --) 9 bit data , 011 --) 8 bit data , 100 --) option 1 : 101 --) option 2 : 110 to 111 --) Reserved
12:11	0x0 RO	**RESERVED_1:** Reserved.
10:7	0x0 RW	**SUPPORTED_FORMAT_IN_VIDEO_MODE:** Supported colour format, 0001 --) RGB565, 0010 --) RGB666, 0011 --) RGB 666 loosely packed format, 0100 --) RGB888
6:5	0x0 RW	**CHANNEL_NUMBER_FOR_COMMAND_MODE:** Virtual channel number for command mode is programmed by the processor
4:3	0x0 RW	**CHANNEL_NUMBER_FOR_VIDEO_MODE:** Virtual channel number for command mode is programmed by the processor
2:0	0x1 RW	**DATA_LANES_PRG_R_EG:** Number of data lanes to be supported is programmed by the processor

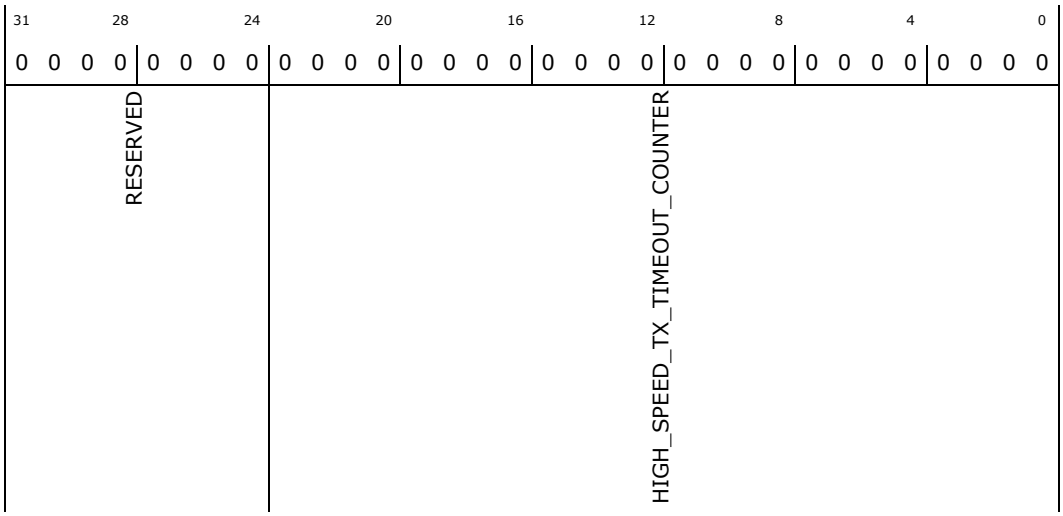
4.2.56 MIPIA_HS_TX_TIMEOUT_REG—Offset B010h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B010h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:0	0x0 RW	**HIGH_SPEED_TX_TIMEOUT_COUNTER:** The maximum duration allowed for the DSI host ,to remain in high speed mode for a transmission. If the counter expires, HS mode is terminated with EOT and the lanes enter stop state

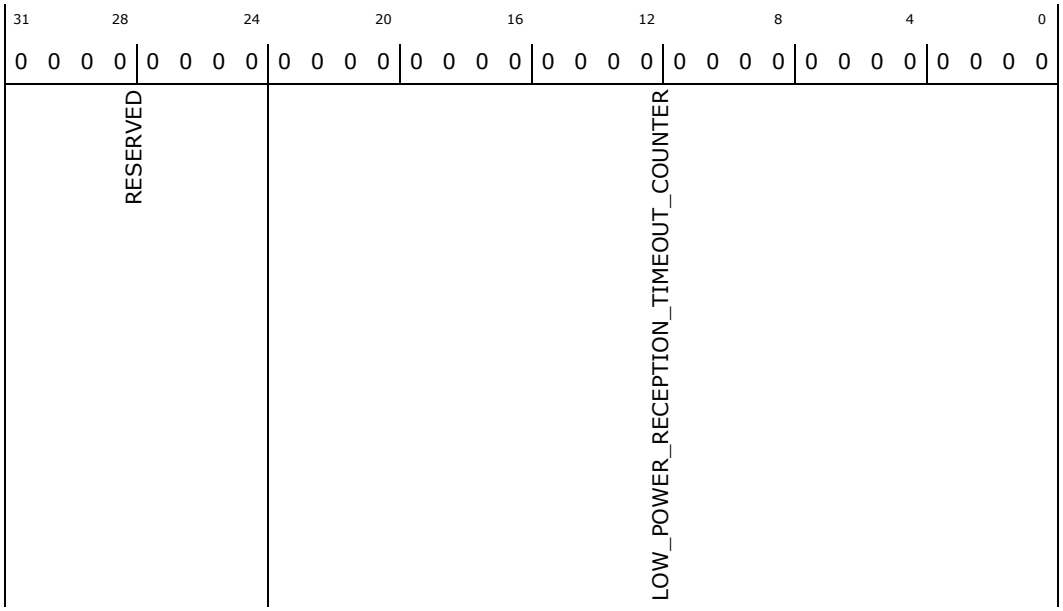
4.2.57 MIPIA_LP_RX_TIMEOUT_REG—Offset B014h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B014h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:0	0x0 RW	**LOW_POWER_RECEPTION_TIMEOUT_COUNTER:** Timeout value to be checked for received short packets .If the timer expires the DSI Host enters stop state

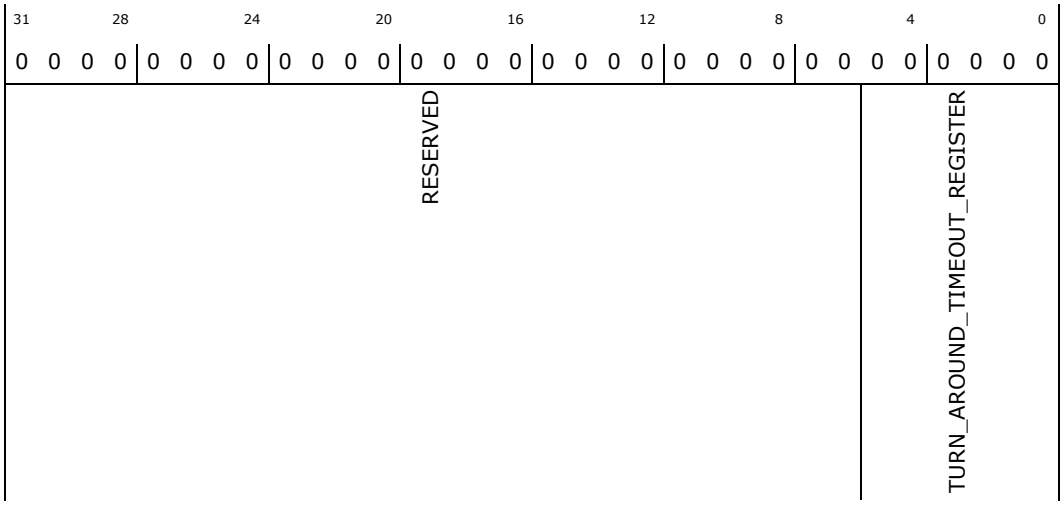
4.2.58 MIPIA_TURN_AROUND_TIMEOUT_REG—Offset B018h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B018h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**RESERVED:** Reserved.
5:0	0x0 RW	**TURN_AROUND_TIMEOUT_REGISTER:** Timeout value to be checked after the DSI host makes a turn around in the direction of transfers. If the timer expires the DSI Host enters stop state

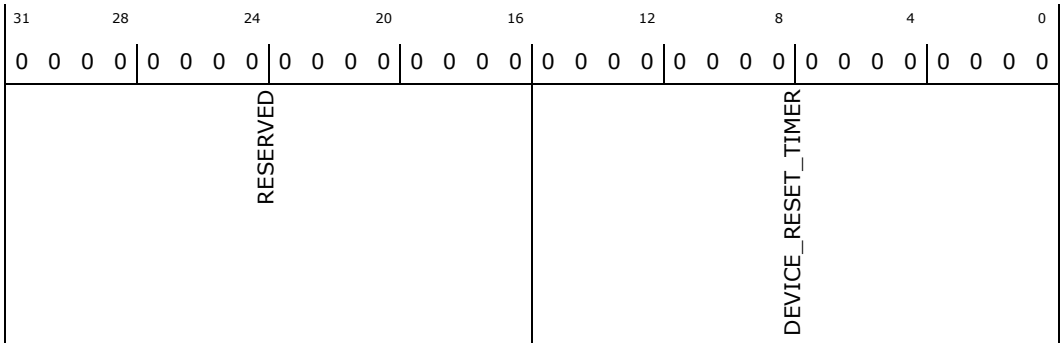
4.2.59 MIPIA_DEVICE_RESET_TIMER—Offset B01Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B01Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15:0	0x0 RW	**DEVICE_RESET_TIMER:** Timeout value to be checked for device to be reset after issuing reset entry command. If the timer expires the DSI Host enters normal operation

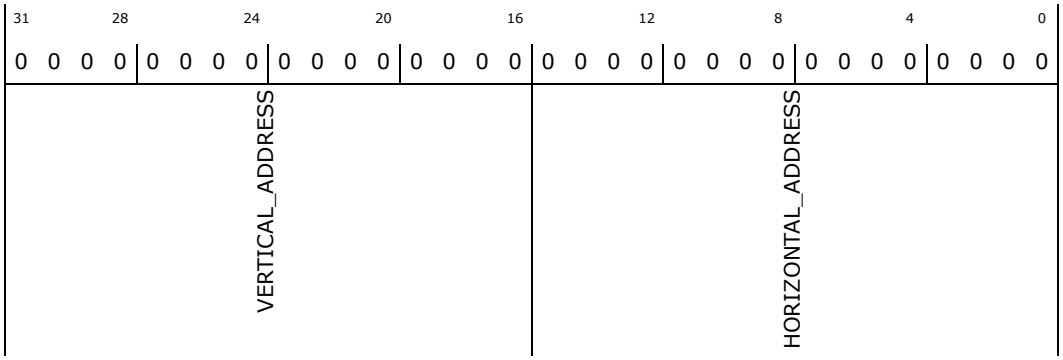
4.2.60 MIPIA_DPI_RESOLUTION_REG—Offset B020h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B020h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**VERTICAL_ADDRESS:** Shows the vertical address count in lines
15:0	0x0 RW	**HORIZONTAL_ADDRESS:** Shows the horizontal address count in pixels

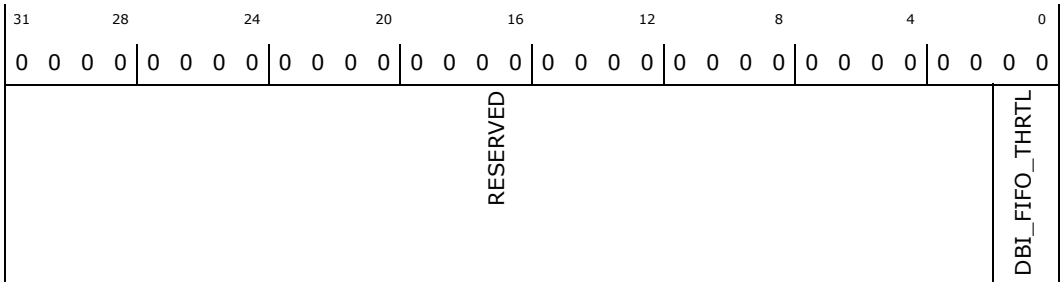
4.2.61 MIPIA_DBI_RESOLUTION_REG—Offset B024h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B024h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**RESERVED:** Reserved.
1:0	0x0 RW	**DBI_FIFO_THRTL:** DBI FIFO's watermark can be set using the following bits so as to enable dbi_stall de-assertion whenever the below FIFO condition is reached: 00 - (1/2) DBI fifo empty 01 - (1/4) DBI fifo empty 10 - 7 locations are empty 11 - Reserved

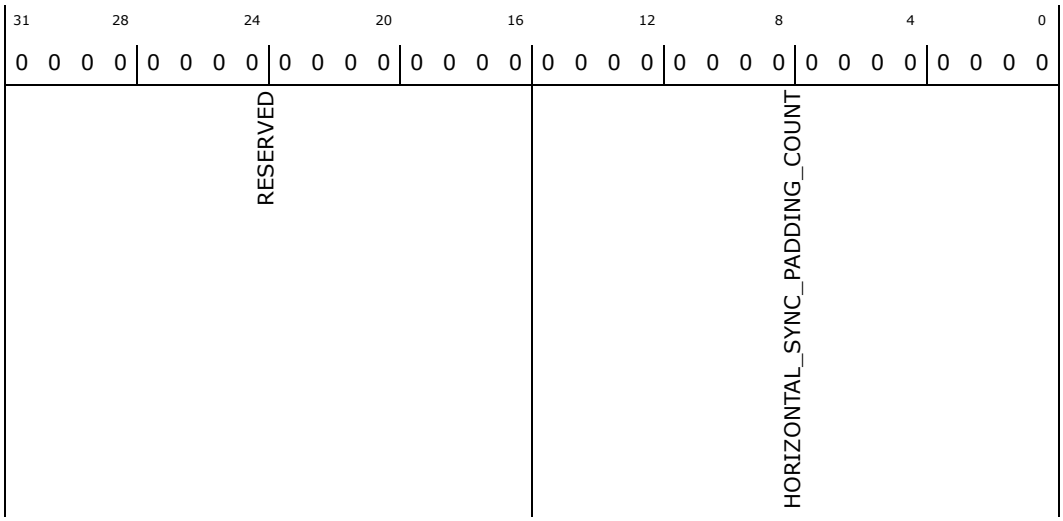
4.2.62 MIPIA_HORIZ_SYNC_PADDING_COUNT—Offset B028h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B028h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15:0	0x0 RW	**HORIZONTAL_SYNC_PADDING_COUNT:** Shows the horizontal sync padding value in terms of txbyteclkhs

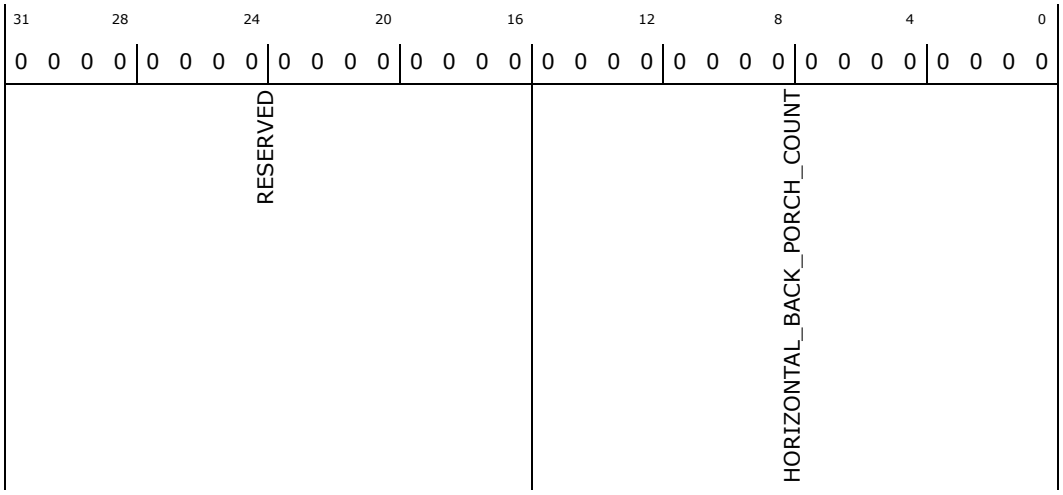
4.2.63 MIPIA_HORIZ_BACK_PORCH_COUNT—Offset B02Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B02Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15:0	0x0 RW	**HORIZONTAL_BACK_PORCH_COUNT:** Shows the horizontal back porch value in terms of txbyteclkhs

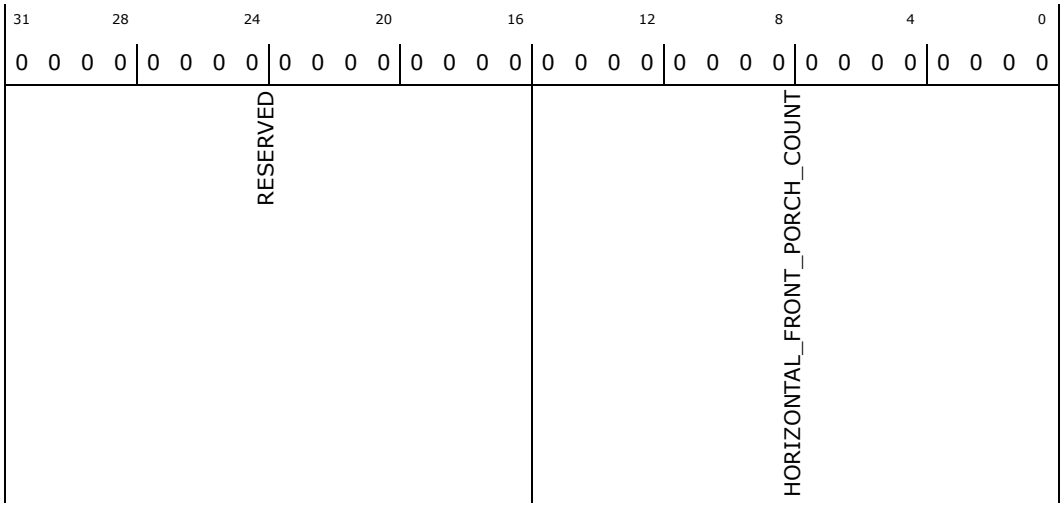
4.2.64 MIPIA_HORIZ_FRONT_PORCH_COUNT—Offset B030h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B030h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15:0	0x0 RW	**HORIZONTAL_FRONT_PORCH_COUNT:** Shows the horizontal front porch value in terms of txbyteclkhs

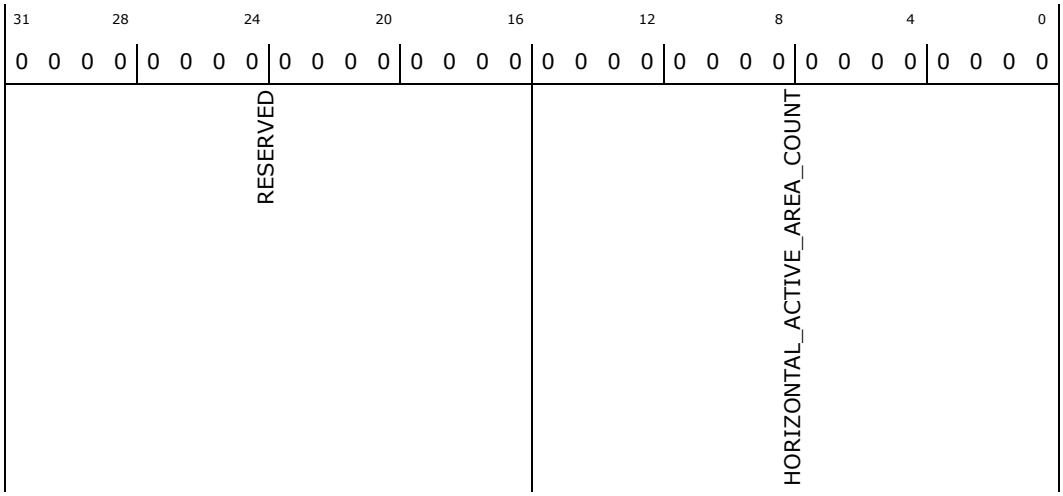
4.2.65 MIPIA_HORIZ_ACTIVE_AREA_COUNT—Offset B034h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B034h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15:0	0x0 RW	**HORIZONTAL_ACTIVE_AREA_COUNT:** Shows the horizontal active area value in terms of txbyteclkhs

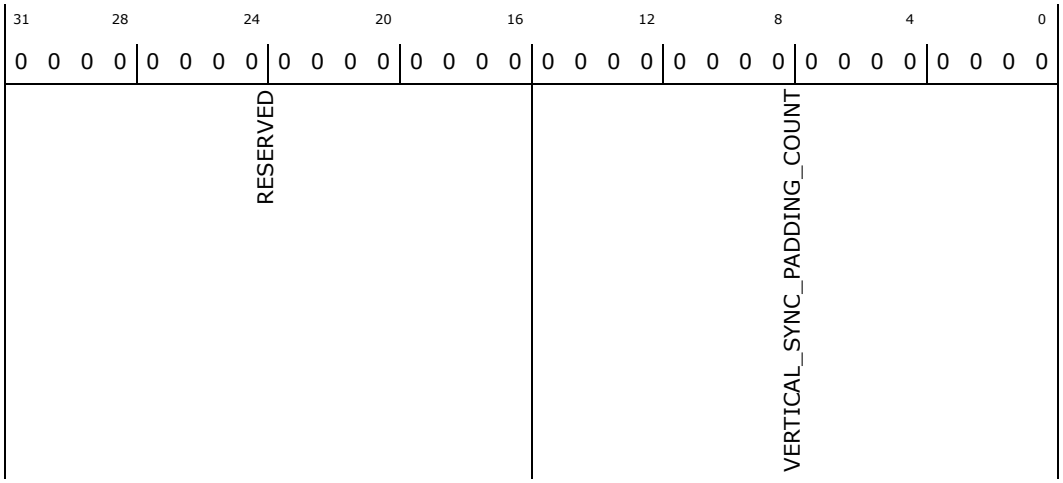
4.2.66 MIPIA_VERT_SYNC_PADDING_COUNT—Offset B038h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B038h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15:0	0x0 RW	**VERTICAL_SYNC_PADDING_COUNT:** Shows the vertical sync padding value in terms of lines

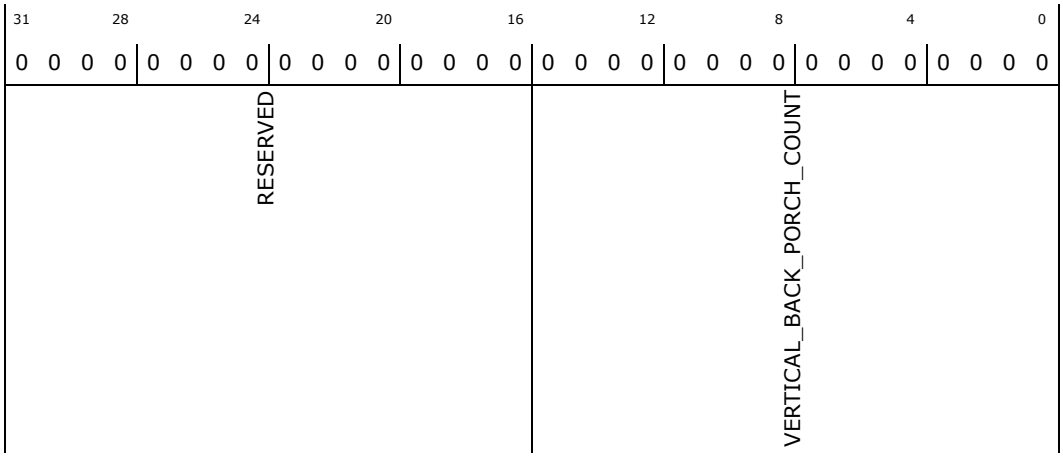
4.2.67 MIPIA_VERT_BACK_PORCH_COUNT—Offset B03Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B03Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15:0	0x0 RW	**VERTICAL_BACK_PORCH_COUNT:** Shows the vertical back porch value in terms of lines

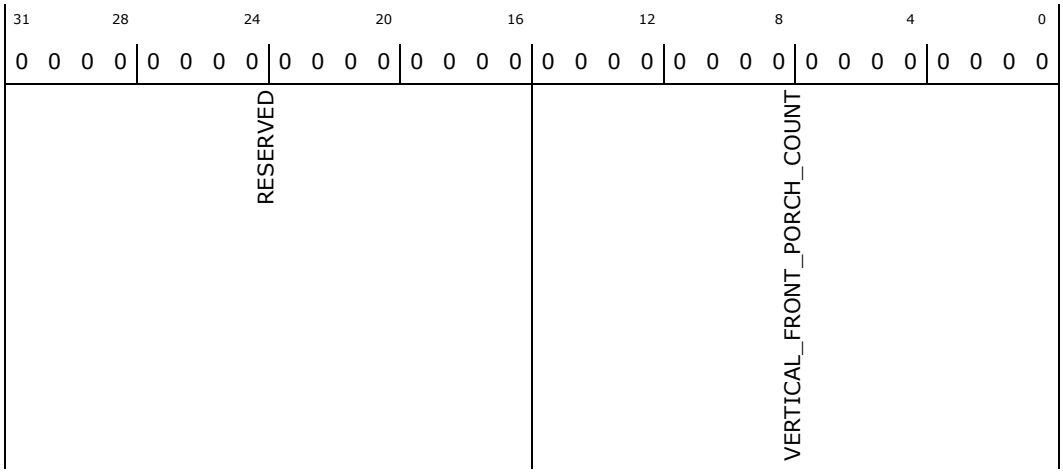
4.2.68 MIPIA_VERT_FRONT_PORCH_COUNT—Offset B040h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B040h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW	**VERTICAL_FRONT_PORCH_COUNT:** Shows the vertical front porch value in terms of lines

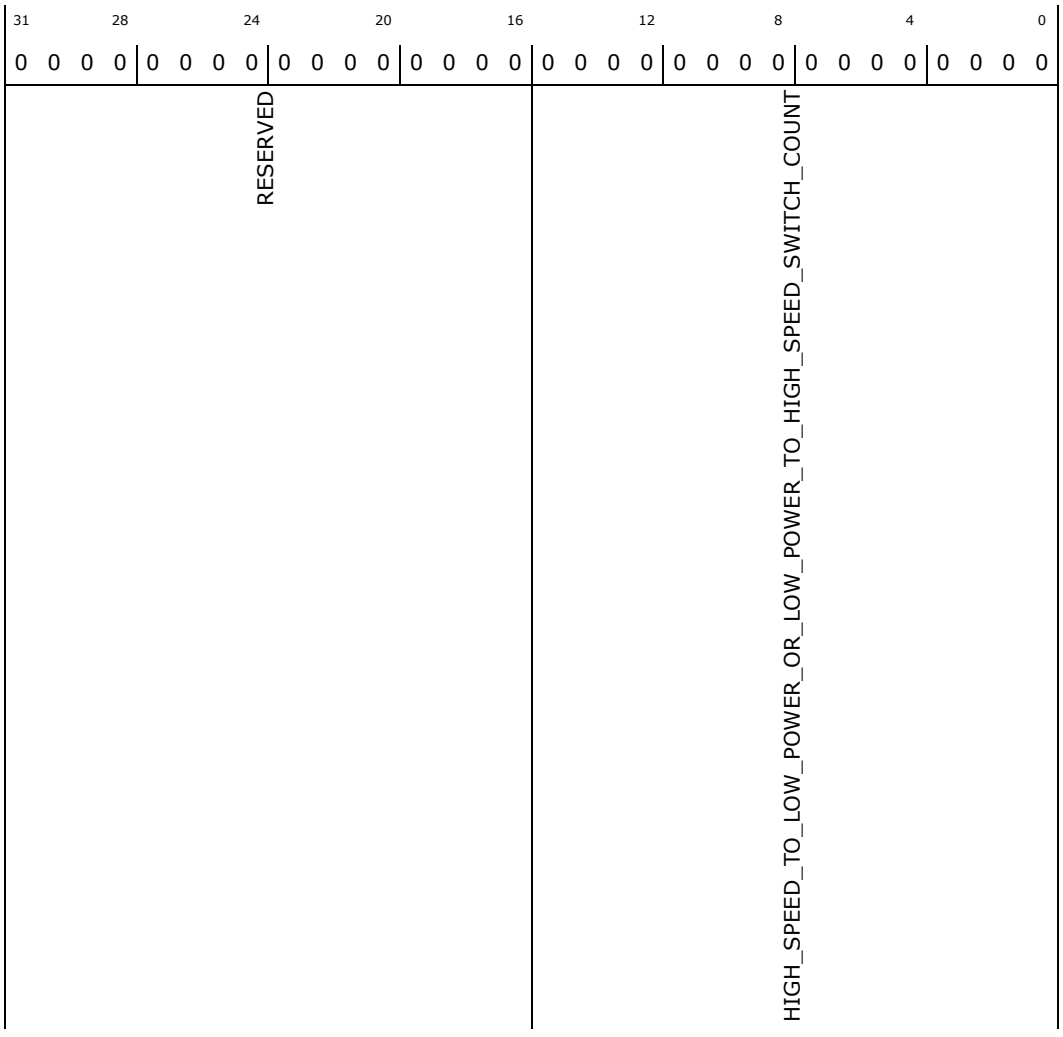
4.2.69 MIPIA_HIGH_LOW_SWITCH_COUNT—Offset B044h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B044h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** High speed to low power or Low power to high speed switching time in terms of txbyteclkhs
15:0	0x0 RW	**HIGH_SPEED_TO_LOW_POWER_OR_LOW_POWER_TO_HIGH_SPEED_SWITCH_COUNT:** High speed to low power or Low power to high speed switching time in terms of txbyteclkhs

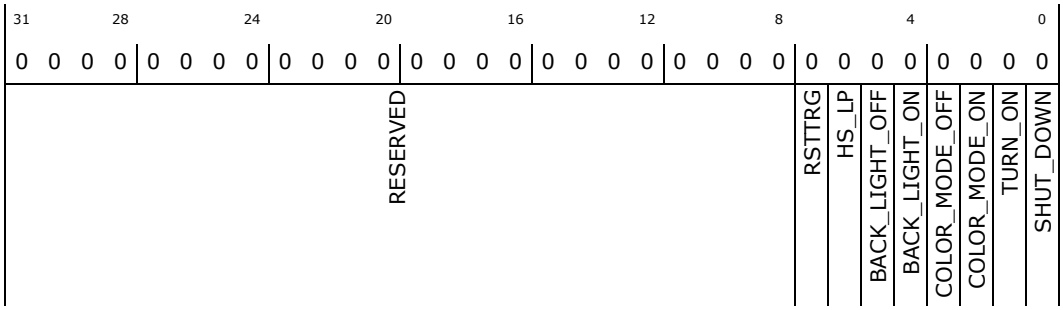
4.2.70 MIPIA_DPI_CTRL_REG—Offset B048h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B048h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED:**
7	0x0 RW	**RSTTRG:** Reserved.
6	0x0 RW	**HS_LP:** Set to '0' to indicate the special packets are sent through the DSI link using HS transmission and set to '1' to indicate that the special packets are sent through the DSI link using low power mode
5	0x0 RW	**BACK_LIGHT_OFF:** Set to '1' to indicate a backlight OFF short packet has to be packetised for the DPI's virtual channel
4	0x0 RW	**BACK_LIGHT_ON:** Set to '1' to indicate a backlight ON short packet has to be packetised for the DPI's virtual channel
3	0x0 RW	**COLOR_MODE_OFF:** Set to '1' to indicate a color mode OFF short packet has to be packetised for the DPI's virtual channel
2	0x0 RW	**COLOR_MODE_ON:** Set to '1' to indicate a color mode ON short packet has to be packetised for the DPI's virtual channel
1	0x0 RW	**TURN_ON:** Set to '1' to indicate a turn on short packet has to be packetised for the DPI's virtual channel
0	0x0 RW	**SHUT_DOWN:** Set to '1' to indicate a shut down short packet has to be packetised for the DPI's virtual channel

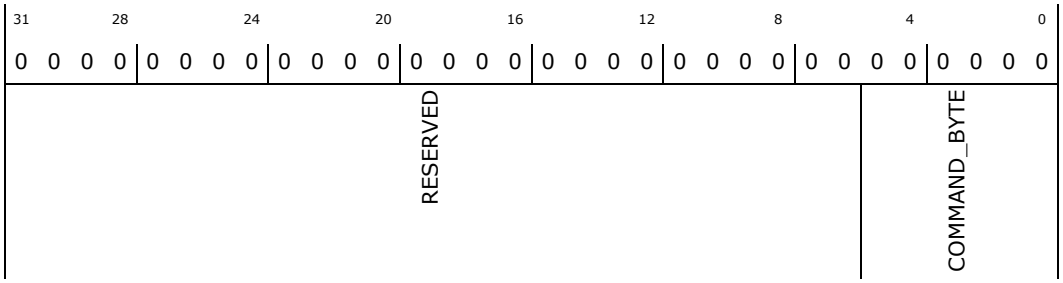
4.2.71 MIPIA_DPI_DATA_REGISTER—Offset B04Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B04Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**RESERVED:** Reserved.
5:0	0x0 RW	**COMMAND_BYTE:** Command Byte to represent the new or not defined command bytes usage for special features representation. [Like backlight ON and OFF]. This register should be programmed before the DPI control register is being programmed for backlight ON/OFF

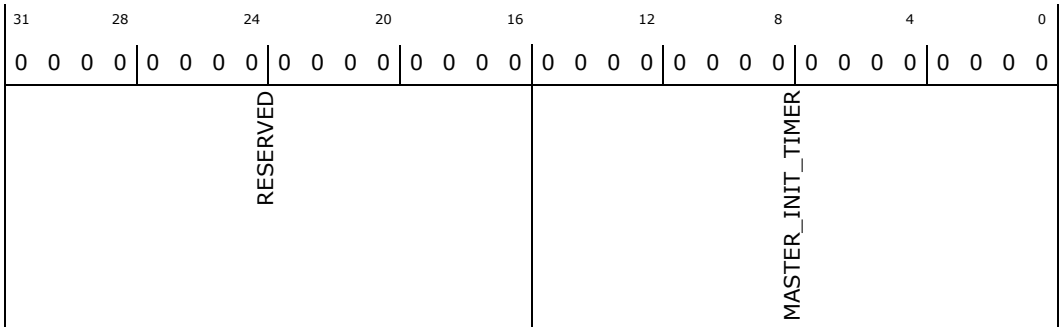
4.2.72 MIPIA_INIT_COUNT_REGISTER—Offset B050h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B050h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW	**MASTER_INIT_TIMER:** Counter value in terms of low power clock to initialise the DSI Host IP [TINT] that drives a stop state on the mipi's D-PHY bus

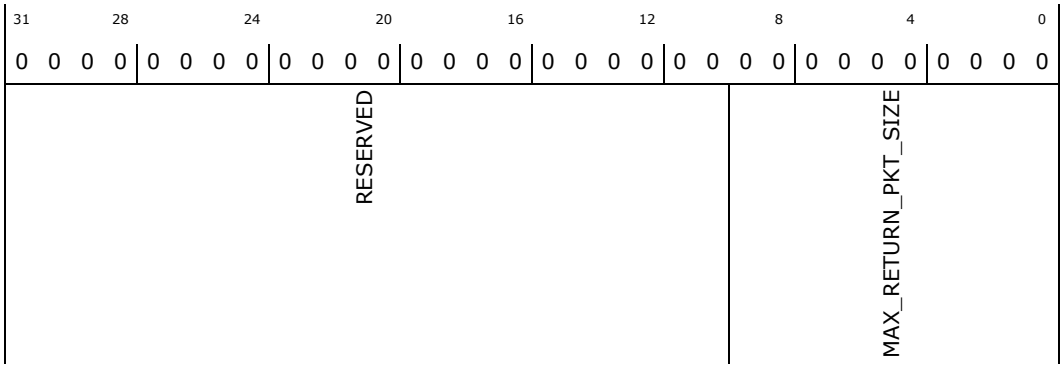
4.2.73 MIPIA_MAX_RETURN_PKT_SIZE_REGISTER—Offset B054h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B054h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**RESERVED:** Reserved.
9:0	0x0 RW	**MAX_RETURN_PKT_SIZE:** Set the count value in bytes to collect the return data packet for reverse direction data flow in data lane0 in response to a DBI read operation

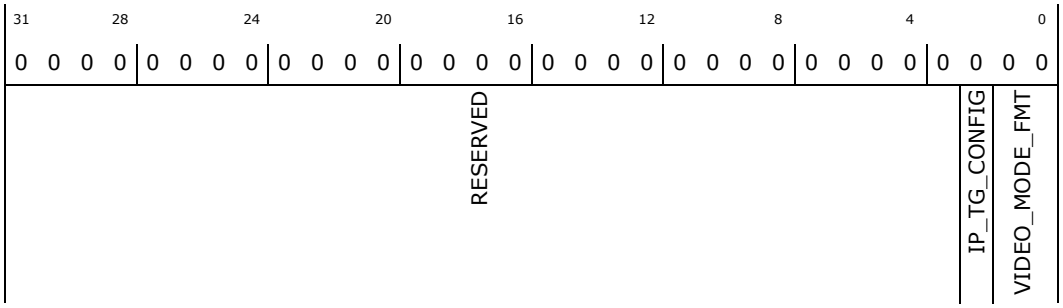
4.2.74 MIPIA_VIDEO_MODE_FORMAT_REGISTER—Offset B058h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B058h

Default: 00000000h



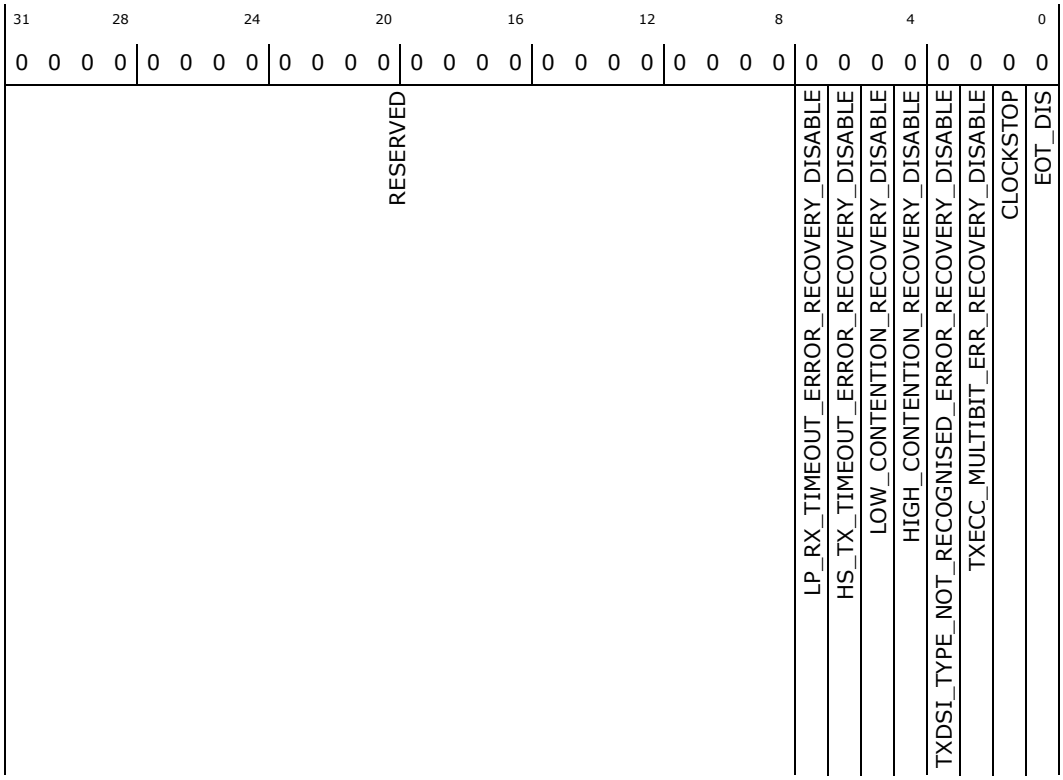
Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**RESERVED:** Reserved.
2	0x0 RW	**IP_TG_CONFIG:** Set by the processor to inform that the DSI controller should discontinue the DPI transfer after the last line of the VFP after ip_tg_enable deassertion. By default, this bit is set to 0. 0 - After ip_tg_enable deassertion, DSI Tx controller stops the DPI transfer immediately after the current packet is transmitted. 1 - After ip_tg_enable deassertion, DSI Tx controller discontinues the DPI transfer after the last line of the VFP
1:0	0x0 RW	**VIDEO_MODE_FMT:** Sets the Video mode format (packet sequence) to be supported in DSI. In Non Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed equal to RGB word count value In Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed greater than the RGB word count value, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link. 00 Reserved 01 - Non Burst Mode with Sync Pulse 10 - Non Burst Mode with Sync events 11 - Burst Mode

4.2.75 MIPIA_EOT_DISABLE_REGISTER—Offset B05Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** B05Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED:** Reserved.
7	0x0 RW	**LP_RX_TIMEOUT_ERROR_RECOVERY_DISABLE:** Set by the processor to enable or disable the LP_Rx_timeout error recovery if the processor clears LP_Rx_timeout error interrupt. 0 - LP_Rx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the LP_Rx_timeout error interrupt. 1 - If the processor clears the LP_Rx_timeout error interrupt, LP_Rx_timeout error recovery action will not happen in DSI Tx controller. LP Rx timeout error interrupt will act as an informative interrupt
6	0x0 RW	**HS_TX_TIMEOUT_ERROR_RECOVERY_DISABLE:** Set by the processor to enable or disable the HS_Tx_timeout error recovery if the processor clears HS_Tx_timeout interrupt. 0 - HS_Tx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the HS_Tx_timeout error interrupt. 1 - If the processor clears the HS_Tx_timeout error interrupt, HS_Tx_timeout error recovery action will not happen in DSI Tx controller. HS Tx timeout error interrupt will act as an informative interrupt

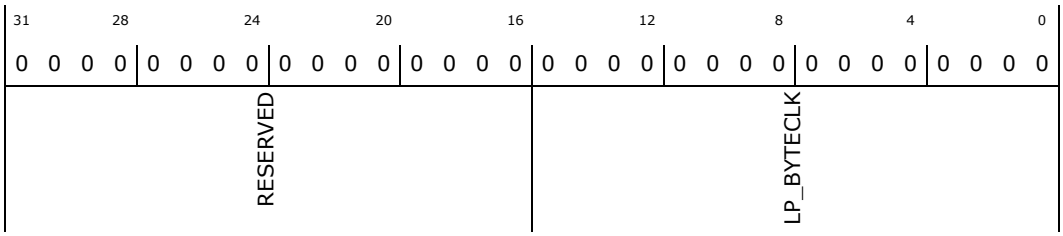
Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**LOW_CONTENTION_RECOVERY_DISABLE:** Set by the processor to enable or disable the contention recovery procedure if the processor clears Low contention interrupt. 0 - Contention recovery will happen if the processor clears Low contention interrupt. 1 - If the processor clears the low contention interrupt, contention recovery procedure will not be initiated by the DSI Tx controller. Low contention interrupt will act as an informative interrupt
4	0x0 RW	**HIGH_CONTENTION_RECOVERY_DISABLE:** Set by the processor to enable or disable the contention recovery procedure if the processor clears High contention interrupt. 0 - Contention recovery will happen if the processor clears High contention interrupt. 1 - If the processor clears the high contention interrupt, contention recovery procedure will not be initiated by the DSI Tx controller. Ignore the High Contention Interrupt in MIPI_INTR_STAT_REG
3	0x0 RW	**TXDSI_TYPE_NOT_RECOGNISED_ERROR_RECOVERY_DISABLE:** Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if TxDSI data type not recognized error interrupt is cleared by the processor. 0 - Error recovery action will be taken if TxDSI data type not recognized error interrupt is cleared by the processor. 1 - If TxDSI data type not recognized error interrupt is cleared by the processor, error recovery action will not be taken by the DSI TX controller. Tx DSI data type not recognized error interrupt will act as an informative interrupt
2	0x0 RW	**TXECC_MULTIBIT_ERR_RECOVERY_DISABLE:** Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if Tx ECC multibit error interrupt is cleared by the processor. 0 - Error recovery action will be taken if Tx ECC multibit error interrupt is cleared by the processor. 1 - If Tx ECC multibit error interrupt is cleared by the processor, error recovery action will not be taken by the DSI TX controller. Tx multibit error interrupt will act as an informative interrupt
1	0x0 RW	**CLOCKSTOP:** Set by the processor to enable or disable clock stopping feature during BLLP timing in a DPI transfer in dual channel mode or during DPI only mode and also when there is no traffic in the DBI interface in DBI only enabled mode. By default this register value is 0. 0 - clock stopping disabled 1 - clock stopping enabled
0	0x0 RW	**EOT_DIS:** Set by the processor to enable or disable EOT short packet transmission. By default this register value is 0. For backward compatibility of earlier DSI systems, EOT short packet transmission can be disabled. 0 - EOT short packet transmission enabled 1 - EOT short packet transmission disabled

4.2.76 MIPIA_LP_BYTECLK_REGISTER—Offset B060h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** B060h

Default: 00000000h



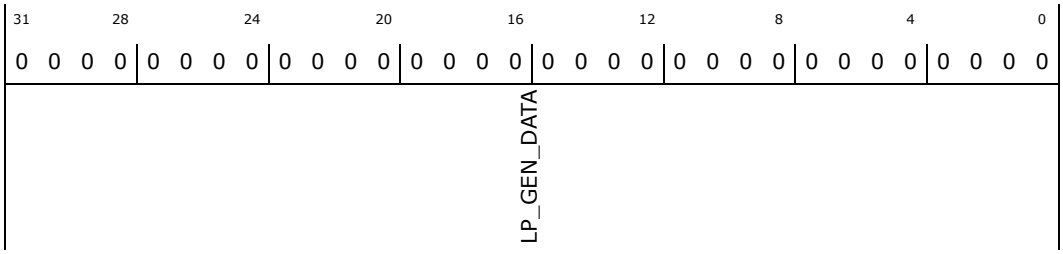
Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15:0	0x0 RW	**LP_BYTECLK:** Low power clock equivalence in terms of byte clock. The value programmed in this register is equal to the number of byte clocks occupied in one low power clock. This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc)

4.2.77 MIPIA_LP_GEN_DATA_REGISTER—Offset B064h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** B064h

Default: 00000000h



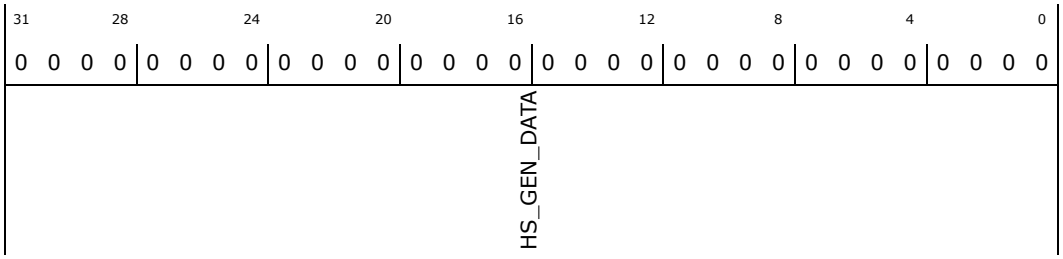
Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**LP_GEN_DATA:** Data port register used for generic data transfers in low power mode

4.2.78 MIPIA_HS_GEN_DATA_REGISTER—Offset B068h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** B068h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**HS_GEN_DATA:** Data port register used for generic data transfers in low power mode

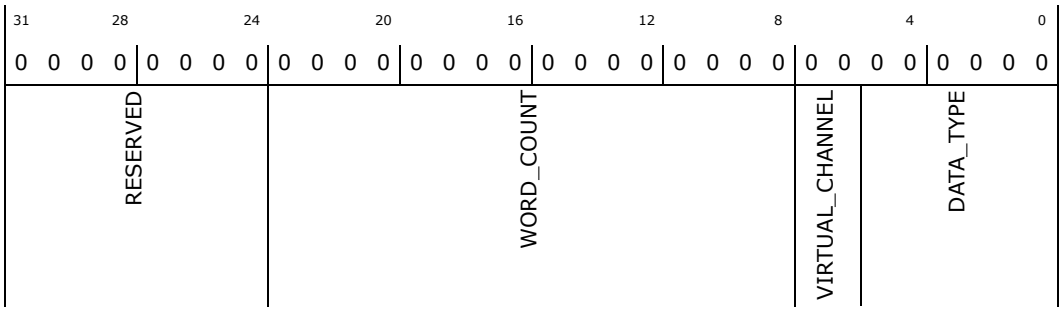
4.2.79 MIPIA_LP_GEN_CTRL_REGISTER—Offset B06Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B06Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:8	0x0 WO	**WORD_COUNT:** Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets. Note: Invalid parameters must be set to 00h
7:6	0x0 WO	**VIRTUAL_CHANNEL:** Used to specify the virtual channel for which the generic data transmission is intended

Bit Range	Default & Access	Field Name (ID): Description
5:0	0x0 WO	**DATA_TYPE:** Used to specify the generic data types 03h - Generic short write, no parameters 13h - Generic short write, 1 parameter 23h - Generic short write, 2 parameters 04h - Generic read, no parameters 14h - Generic read, 1 parameter 24h - Generic read 2 parameter 29h - Generic long write 05h - Manufacturer DCS short write, no parameter 15h - Manufacturer DCS short write , one parameter 06h - Manufacturer DCS read, no parameter 39h - Manufacturer DCS long write

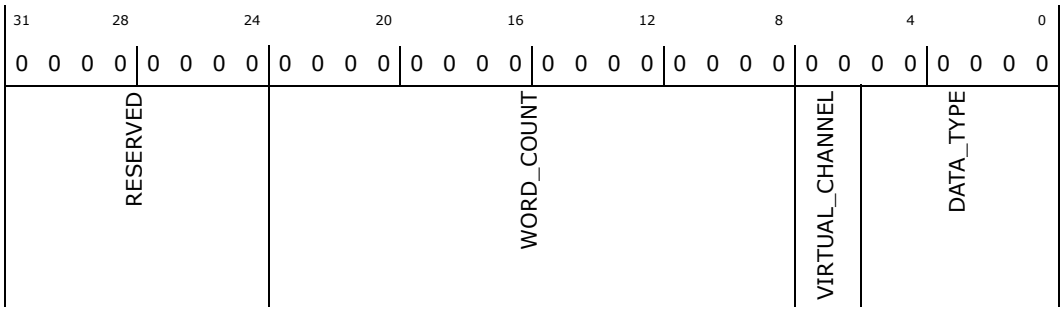
4.2.80 MIPIA_HS_GEN_CTRL_REGISTER—Offset B070h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B070h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:8	0x0 WO	**WORD_COUNT:** Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets. Note: Invalid parameters must be set to 00h
7:6	0x0 WO	**VIRTUAL_CHANNEL:** Used to specify the virtual channel for which the generic data transmission is intended

Bit Range	Default & Access	Field Name (ID): Description
5:0	0x0 WO	**DATA_TYPE:** Used to specify the generic data types 03h - Generic short write, no parameters 13h - Generic short write, 1 parameter 23h - Generic short write, 2 parameters 04h - Generic read, no parameters 14h - Generic read, 1 parameter 24h - Generic read 2 parameter 29h - Generic long write 05h - Manufacturer DCS short write, no parameter 15h - Manufacturer DCS short write, one parameter 06h - Manufacturer DCS read, no parameter 39h - Manufacturer DCS long write

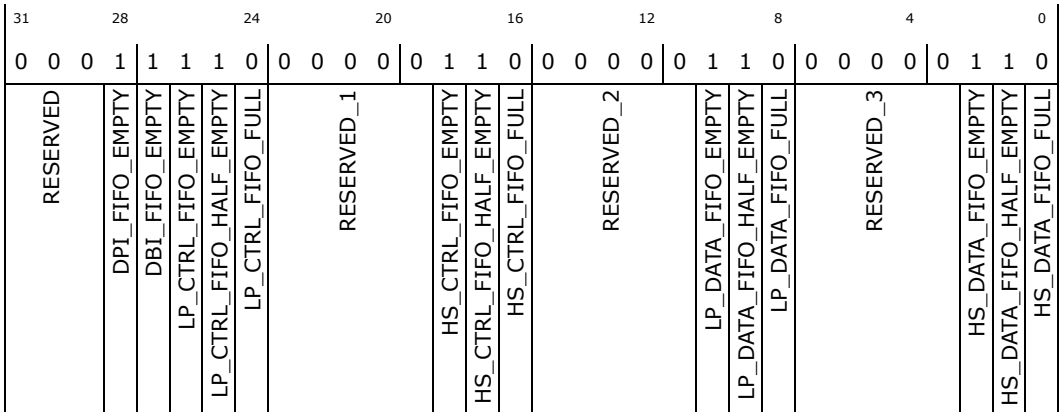
4.2.81 MIPIA_GEN_FIFO_STAT_REGISTER—Offset B074h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B074h

Default: 1E060606h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Reserved.
28	0x1 RO	**DPI_FIFO_EMPTY:** Default 1
27	0x1 RO	**DBI_FIFO_EMPTY:** Default 1
26	0x1 RO	**LP_CTRL_FIFO_EMPTY:** Default 1
25	0x1 RO	**LP_CTRL_FIFO_HALF_EMPTY:** Default 1
24	0x0 RO	**LP_CTRL_FIFO_FULL:** Default 0

Bit Range	Default & Access	Field Name (ID): Description
23:19	0x0 RO	**RESERVED_1:** Reserved.
18	0x1 RO	**HS_CTRL_FIFO_EMPTY:** Default 1
17	0x1 RO	**HS_CTRL_FIFO_HALF_EMPTY:** Default 1
16	0x0 RO	**HS_CTRL_FIFO_FULL:** Default 0
15:11	0x0 RO	**RESERVED_2:** Reserved.
10	0x1 RO	**LP_DATA_FIFO_EMPTY:** Default 1
9	0x1 RO	**LP_DATA_FIFO_HALF_EMPTY:** Default 1
8	0x0 RO	**LP_DATA_FIFO_FULL:** Default 0
7:3	0x0 RO	**RESERVED_3:** Reserved.
2	0x1 RO	**HS_DATA_FIFO_EMPTY:** Default 1
1	0x1 RO	**HS_DATA_FIFO_HALF_EMPTY:** Default 1
0	0x0 RO	**HS_DATA_FIFO_FULL:** Default 0

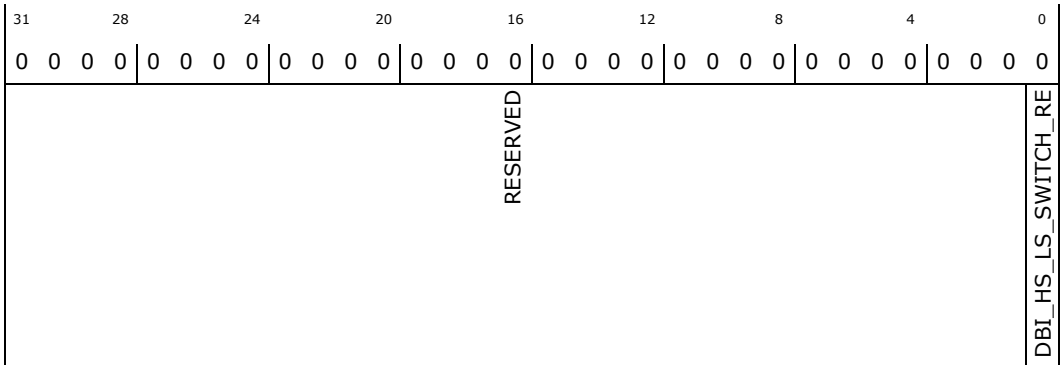
4.2.82 MIPIA_HS_LS_DBI_ENABLE_REG—Offset B078h

Note : dbi_hs_lp_switch_reg has to be written only if DBI FIFO is empty

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** B078h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RESERVED:** Reserved.
0	0x0 RW	**DBI_HS_LS_SWITCH_RE:** Set to 1 if DBI packets have to be transmitted in Low power mode Set to 0 if DBI packets have to be transmitted in High speed mode

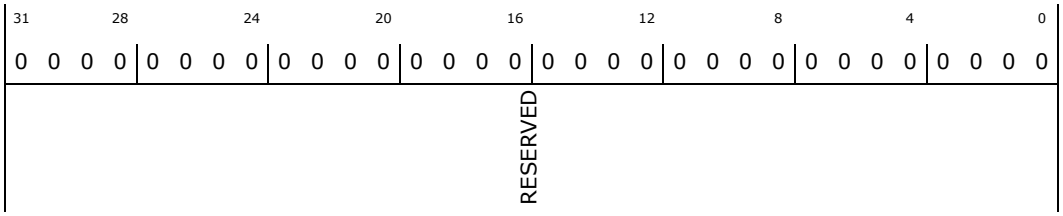
4.2.83 MIPIA_RESERVED—Offset B07Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B07Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RESERVED:** Reserved.

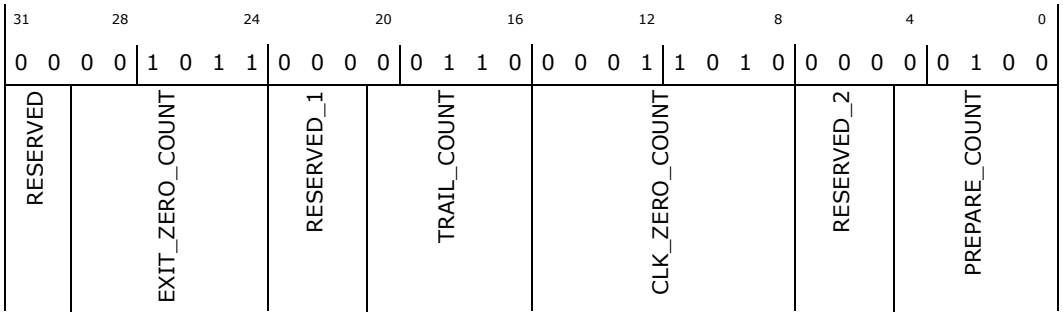
4.2.84 MIPIA_DPHY_PARAM_REG—Offset B080h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B080h

Default: 0B061A04h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RESERVED:** Reserved.
29:24	0xb RW	**EXIT_ZERO_COUNT:** THS_0_TIM_UI_CNT and THS_EXIT_TIM_UI_CNT for dphy are programmed as exit zero count by the processor
23:21	0x0 RO	**RESERVED_1:** Reserved.
20:16	0x6 RW	**TRAIL_COUNT:** TCLK_POST_TIM_UI_CNT and TCLK_TRAIL_TIM_UI_CNT for dphy are programmed as trail count by the processor
15:8	0x1a RW	**CLK_ZERO_COUNT:** TCLK_0_TIM_UI_CNT for dphy is programmed as clk zero count by the processor
7:5	0x0 RO	**RESERVED_2:** Reserved.
4:0	0x4 RW	**PREPARE_COUNT:** TCLK_PREP_TIM_UI_CNT and THS_PREP_TIM_UI_CNT for dphy are programmed as prepare count by the processor

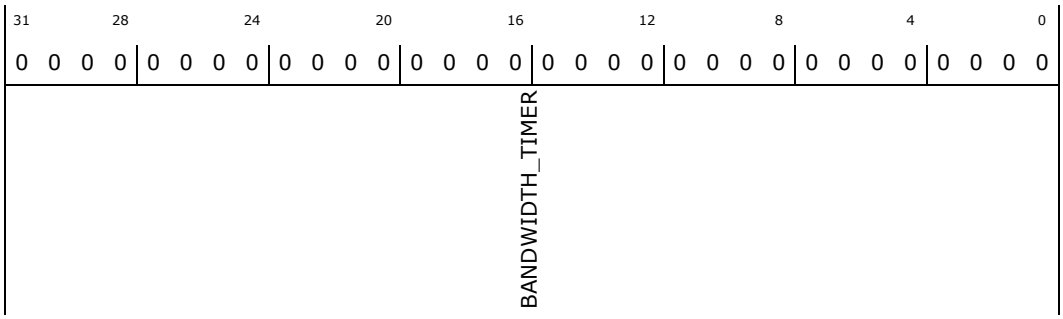
4.2.85 MIPIA_DBI_BW_CTRL_REG—Offset B084h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B084h

Default: 00000000h



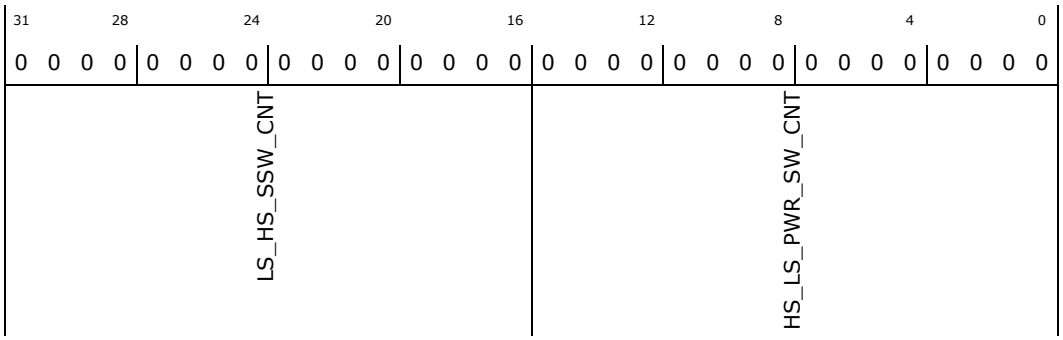
Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**BANDWIDTH_TIMER:** DBI Bandwidth control Register. The bandwidth essential for transmitting 16 long packets containing 252 bytes meant for DCS write memory command is programmed in this register in terms of byte clocks. Based on the DSI transfer rate and the number of lanes configured the time taken to transmit 16 long packets in a DSI stream varies. Note: The value programmed in this timer must be greater than the actual time taken to carryout 16 long packets transmission in DSI stream plus the time taken to transmit two blanking packets

4.2.86 MIPIA_CLK_LANE_SWITCHING_TIME_CNT—Offset B088h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** B088h

Default: 00000000h



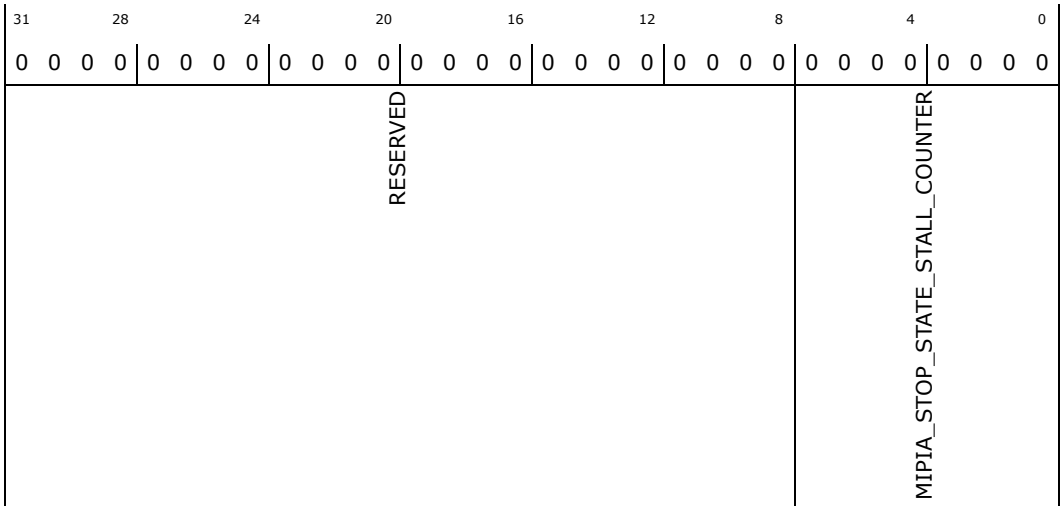
Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**LS_HS_SSW_CNT:** Low power to high speed switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks required to switch from low power mode to high speed mode after txrequesths_clk is asserted. Current Value is ah = 10 txbyteclkhs
15:0	0x0 RW	**HS_LS_PWR_SW_CNT:** High speed to low power switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks request to switch from high speed mode to low power mode after txrequesths_clk is de-asserted. Current Value is 14h = 20 txbyteclkhs

4.2.87 MIPIA_STOP_STATE_STALL—Offset B08Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** B08Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED:**
7:0	0x0 RW	**MIPIA_STOP_STATE_STALL_COUNTER:** Delay between (stall the stop state signal) the data transfer is increased based on this counter value. This counter is calculated from txclkesc. Note: If processor programs this register then it needs to reprogram the high_low_ switch counter in B044h and lp_equivalent_byteclk reg in B060h to compensate this delay. High_low_switch_count B044h: High to low switch counter = Actual High to low switch + stop_sta_stall_reg value * Low power clock equivalence value in terms of byte clock LP equivalent byteclk register B060h: LP equivalent byteclk value = txclkesc time/ txbyteclk time * (105 + stop_sta_stall_reg value) / 105 Minimum time of Low Power short packet transfer = 105 txclkesc

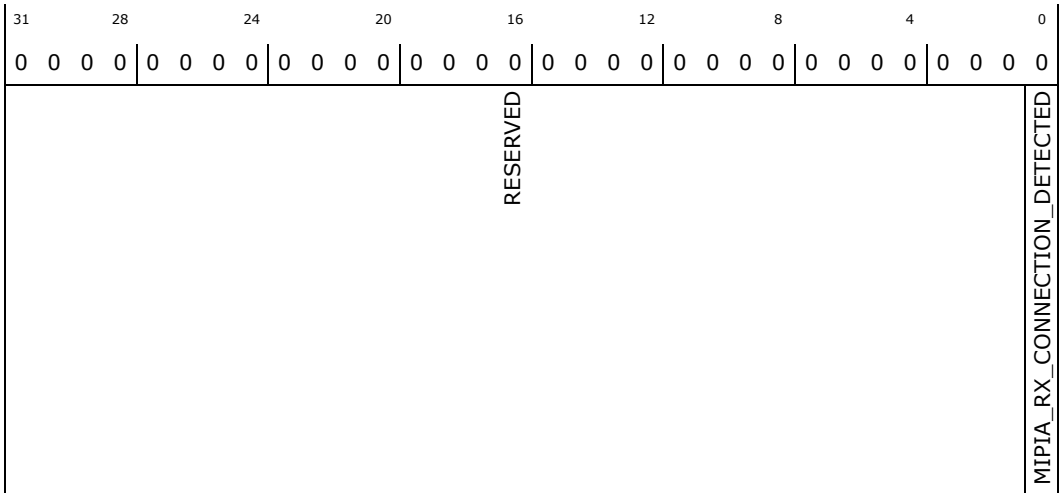
4.2.88 MIPIA_INTR_STAT_REG_1—Offset B090h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B090h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RESERVED:**
0	0x0 RW	**MIPIA_RX_CONNECTION_DETECTED:** Set to 1'b1 if the contention detected in the display device and is reported in the Acknowledge packet by the display device

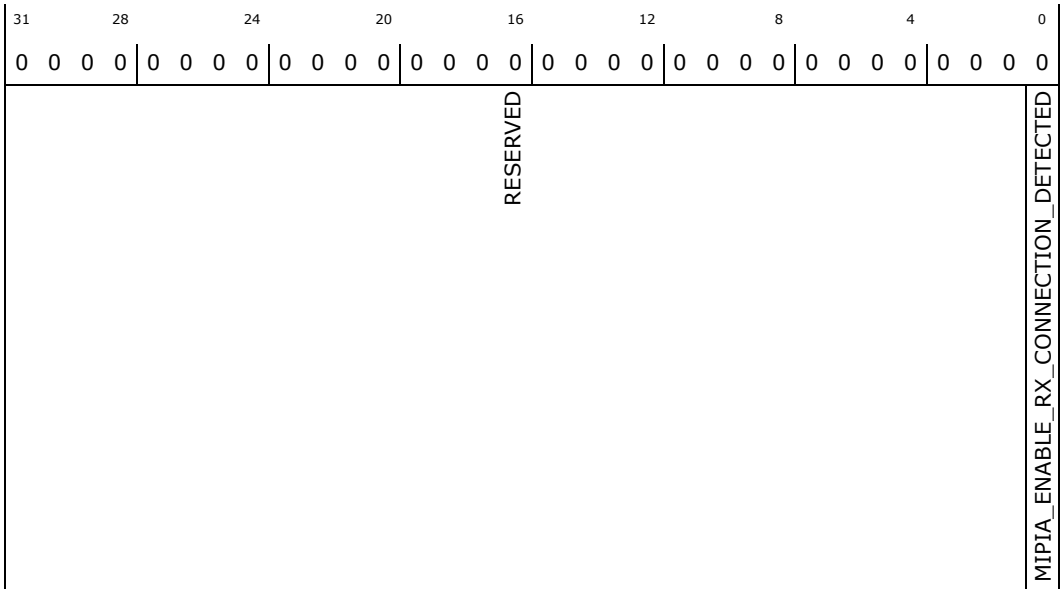
4.2.89 MIPIA_INTR_EN_REG_1—Offset B094h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B094h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RESERVED:**
0	0x0 RW	**MIPIA_ENABLE_RX_CONNECTION_DETECTED:** Set to enable the interrupt for contention detected error in the acknowledgement packet reports

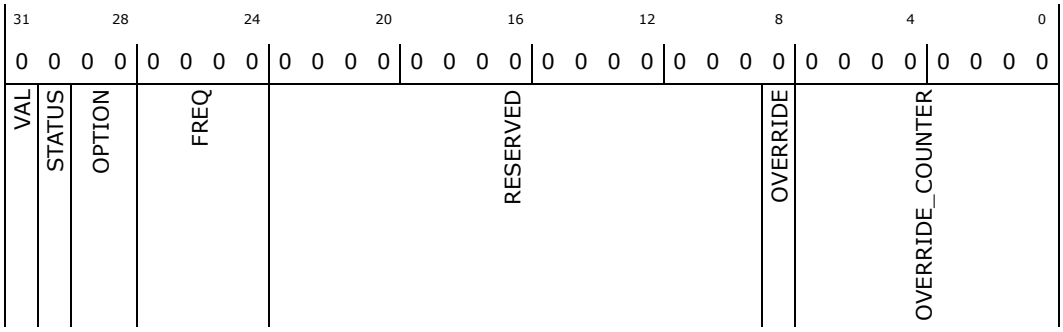
4.2.90 MIPIA_DBI_TYPEC_CTRL—Offset B100h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B100h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**VAL:** 0= disable DBI TYPE-C interface (default) 1= enable DBI TYPE-C interface Driver to make sure that the command and data buffers are cleared before this bit is changed
30	0x0 RW	**STATUS:** command and data buffer empty and link completed sending out all serialized data and IDLE 0 = IDLE 1 = work in progress
29:28	0x0 RW	**OPTION:** TYPE-C option selection 00 option 1 01 option 2 10 option 3 11 no defined functionality
27:24	0x0 RW	**FREQ:** Type-C clock frequency ; A counter based onczclk is used to generate the TYPE-C Clock. So based on the czclk, a frequency close to the specified below will be generated. Not the exact frequency. (TBD we may just support a subset frequencies) 0000 1Mhz (default) 0001 1Mhz 0010 2Mhz 1111 15Mhz
23:9	0x0 RO	**RESERVED:** Reserved.
8	0x0 RW	**OVERRIDE:** Use override counter value to derive the TYPE-C clock frequency
7:0	0x0 RW	**OVERRIDE_COUNTER:** Override counter value to generate the TYPE-C clock

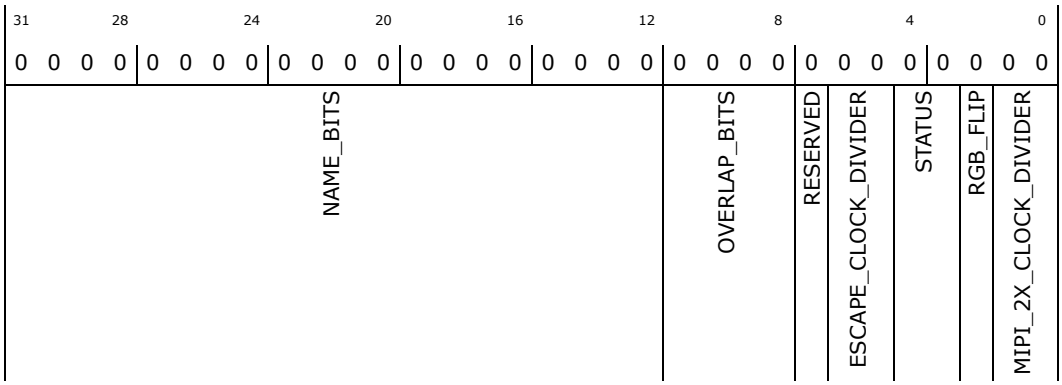
4.2.91 MIPIA_CTRL—Offset B104h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B104h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**NAME_BITS:** Reserved
11:8	0x0 RW	**OVERLAP_BITS:** Number of overlap pixels to support MIPI Video Mode dual Link Z Inversion for FB type panels with Zig Zag Sub pxel layout.
7	0x0 RO	**RESERVED:** Reserved.
6:5	0x0 RW	**ESCAPE_CLOCK_DIVIDER:** Read Only Escape clock divider select for Pipe A and Pipe C Escape clock is shared by both Pipe A and Pipe C so it cant be set different. 00= 1 X (20 Mhz) (default) 01= X (10Mhz) 10= X (5Mhz) Changing this register can only be done when the MIPI device_ready is turned OFF
4:3	0x0 RW	**STATUS:** 2'b00: low priority on read requests to G-unit 2'b11 : high priority
2	0x0 RW	**RGB_FLIP:** 1'b0 : RGB data from disp2d is reverted to BGR 1'b1 : RGB data from disp2d is passed as is to MIPI IP
1:0	0x0 RW	**MIPI_2X_CLOCK_DIVIDER:** Reserved

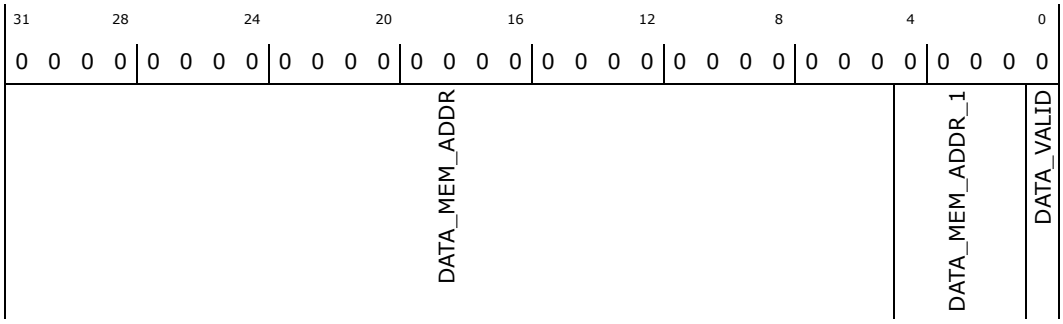
4.2.92 MIPIA_DATA_ADD—Offset B108h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B108h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RW	**DATA_MEM_ADDR:** When there is updated data for the display panel, S/W programs this register with the memory address to read from
4:1	0x0 RW	**DATA_MEM_ADDR_1:** Reserved
0	0x0 RW	**DATA_VALID:** This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

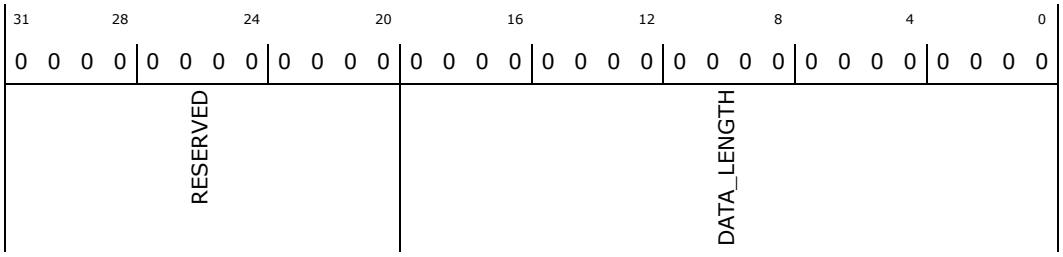
4.2.93 MIPIA_DATA_LEN—Offset B10Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B10Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RESERVED:** Reserved.
19:0	0x0 RW	**DATA_LENGTH:** This field shows the remaining length of data that needs to be read from memory, Initially set by S/W and is decremented by H/W as reads are issued

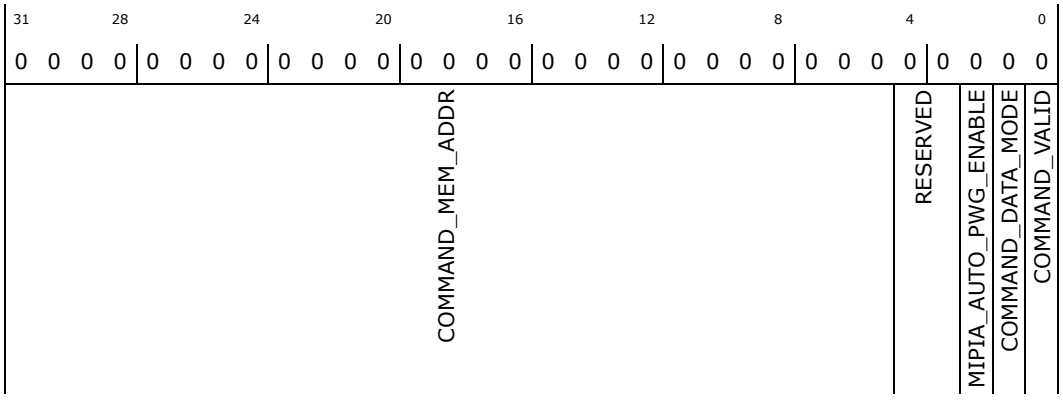
4.2.94 MIPIA_CMD_ADD—Offset B110h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B110h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RW	**COMMAND_MEM_ADDR:** When there are new commands that need to be sent to the display panel, S/W programs this register with the memory address to read the commands from

Bit Range	Default & Access	Field Name (ID): Description
4:3	0x0 RO	**RESERVED:** MBZ
2	0x0 RW	**MIPIA_AUTO_PWG_ENABLE:** Idle state: SW driver writes to this bit to enable auto power gating for MIPIA controller 0: default 1: auto power gate is enabled
1	0x0 RW	**COMMAND_DATA_MODE:** 0: data for memory write command from system buffer that is specified by MIPI data address register 1: data for memory write command from pipe A rendering
0	0x0 RW	**COMMAND_VALID:** This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

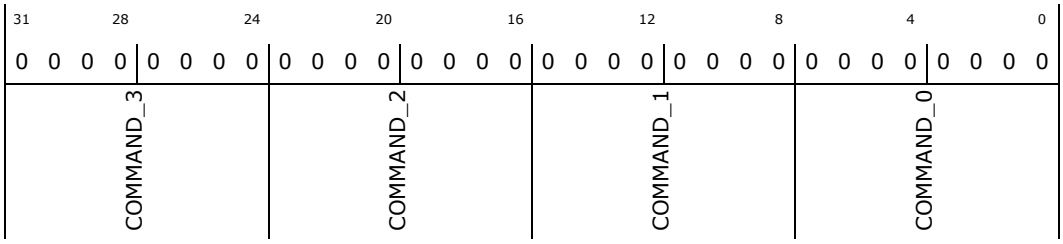
4.2.95 MIPIA_CMD_LEN—Offset B114h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B114h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**COMMAND_3:** This is command 3 length (command + parameters) in bytes
23:16	0x0 RW	**COMMAND_2:** This is command 2 length (command + parameters) in bytes
15:8	0x0 RW	**COMMAND_1:** This is command 1 length (command + parameters) in bytes
7:0	0x0 RW	**COMMAND_0:** This is command 0 length (command + parameters) in bytes

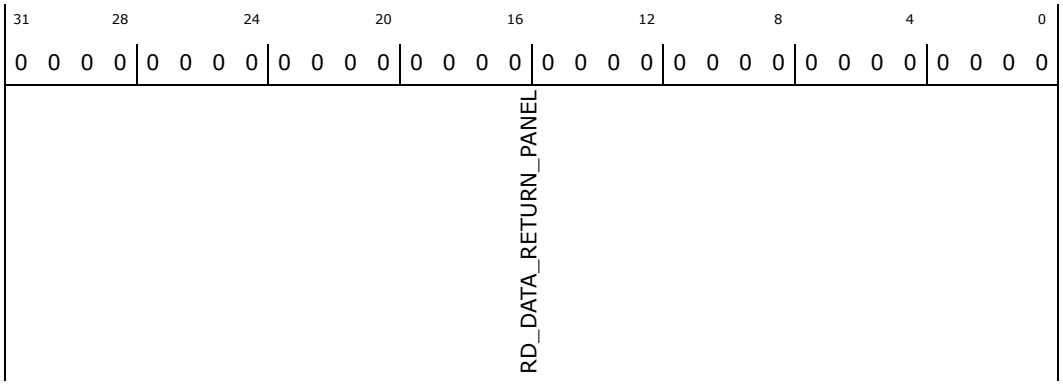
4.2.96 MIPIA_RD_DATA_RETURN0—Offset B118h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B118h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

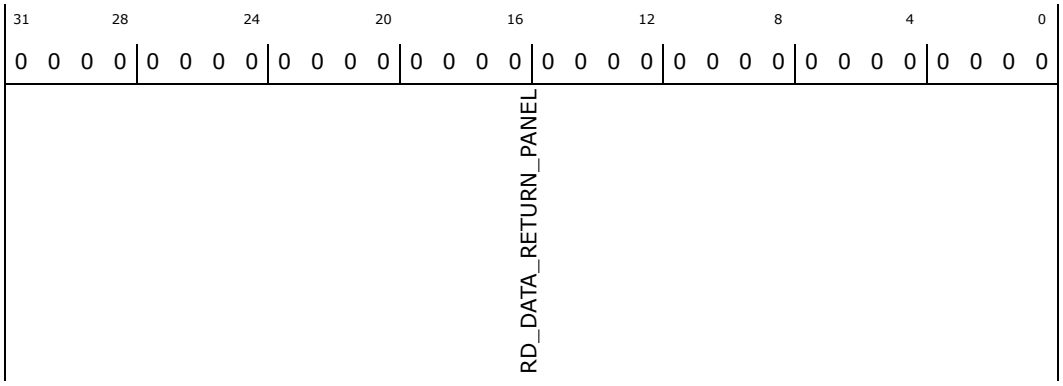
4.2.97 MIPIA_RD_DATA_RETURN1—Offset B11Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B11Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

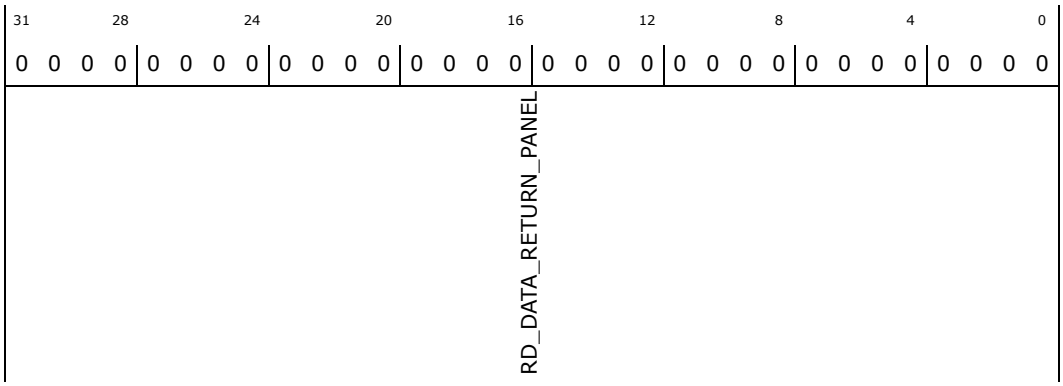
4.2.98 MIPIA_RD_DATA_RETURN2—Offset B120h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B120h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

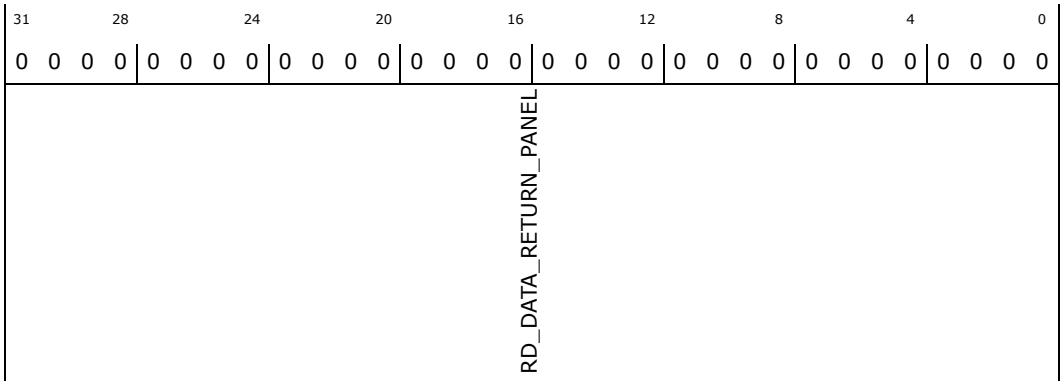
4.2.99 MIPIA_RD_DATA_RETURN3—Offset B124h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B124h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

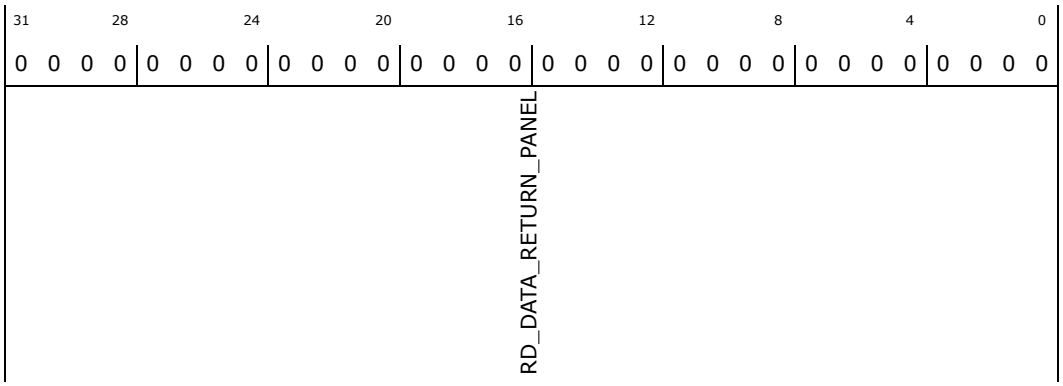
4.2.100 MIPIA_RD_DATA_RETURN4—Offset B128h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B128h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

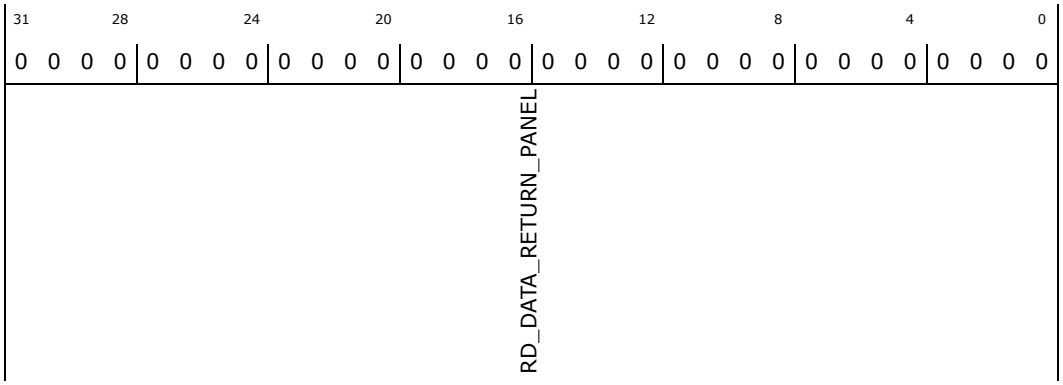
4.2.101 MIPIA_RD_DATA_RETURN5—Offset B12Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B12Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

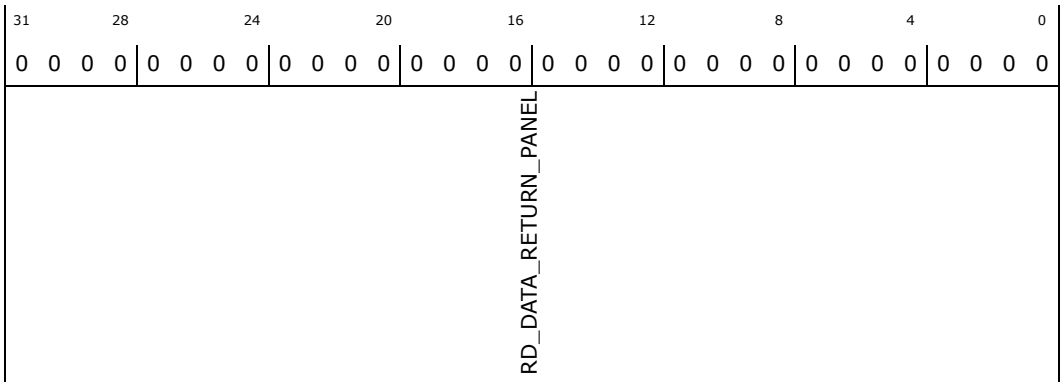
4.2.102 MIPIA_RD_DATA_RETURN6—Offset B130h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B130h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

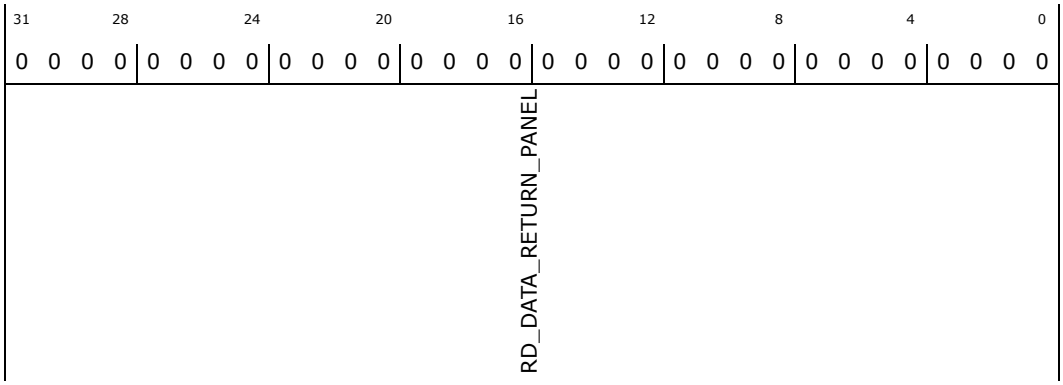
4.2.103 MIPIA_RD_DATA_RETURN7—Offset B134h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B134h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

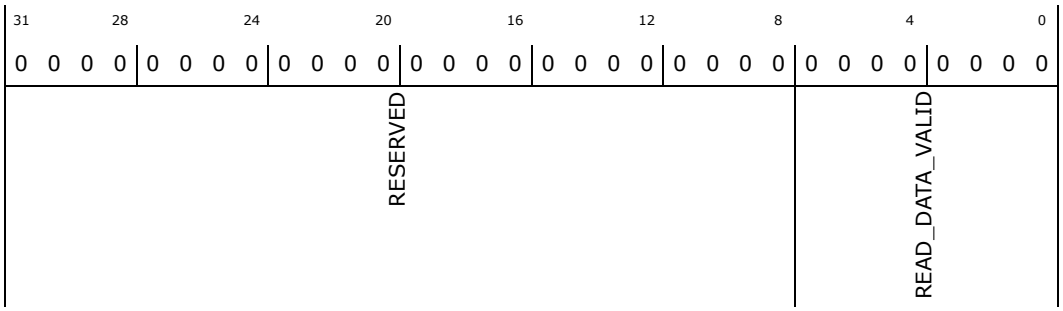
4.2.104 MIPIA_RD_DATA_VALID—Offset B138h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B138h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED:** Reserved.
7:0	0x0 RW	**READ_DATA_VALID:** Each bit corresponds to presence of valid data in the registers above. When data is returned from the panel, H/W will write into these registers in sequence, and set the corresponding valid bit. When S/W issues a write '1 to the registers, this bit is cleared

4.2.105 MIPIC_DEVICE_READY_REG—Offset B800h

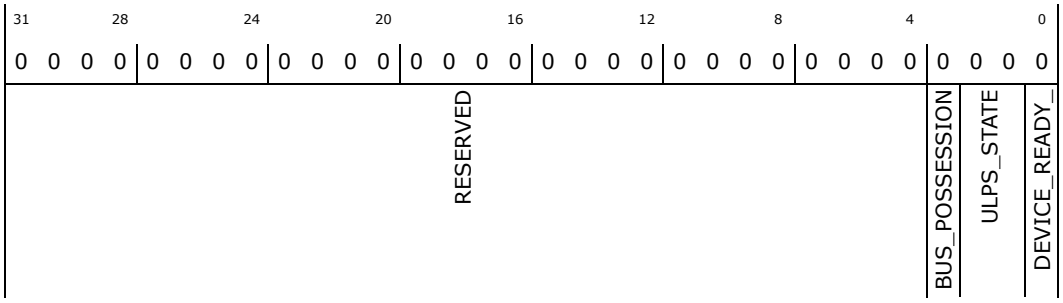
MIPI C Device Ready Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B800h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RESERVED:** Reserved.
3	0x0 RW	**BUS_POSSESSION:** Reserved.
2:1	0x0 RW	**ULPS_STATE:** Reserved.
0	0x0 RW	**DEVICE_READY_:** Set by the processor to inform that device is ready

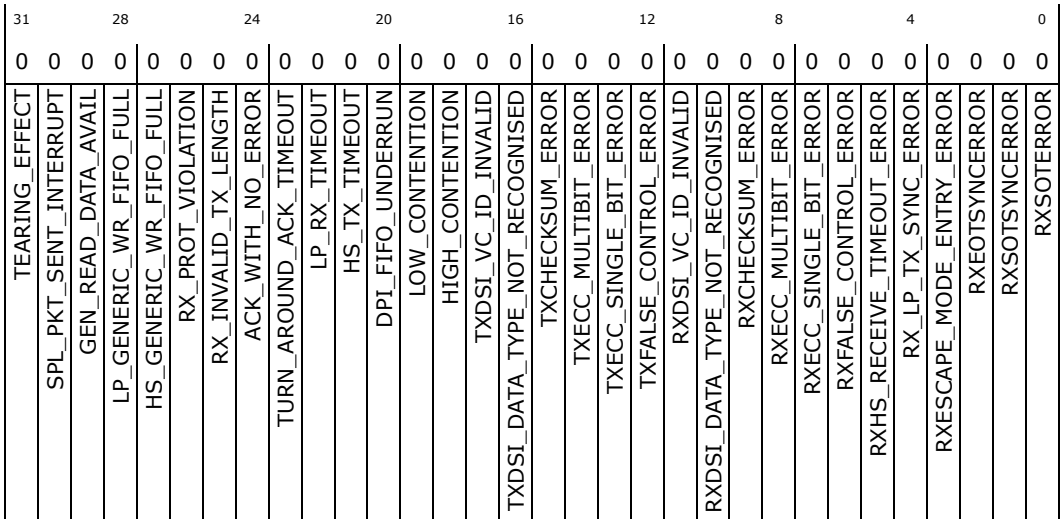
4.2.106 MIPIC_INTR_STAT_REG—Offset B804h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B804h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**TEARING_EFFECT:** Set to indicate that tearing effect trigger message is received
30	0x0 RW	**SPL_PKT_SENT_INTERRUPT:** Set to confirm the transmission of the DPI event specific commands set in the dpi control and dpi data register
29	0x0 RW	**GEN_READ_DATA_AVAIL:** Set to indicate that the requested data for a Generic Read request is available in the buffer i.e., generic read response data is available in the read FIFO
28	0x0 RW	**LP_GENERIC_WR_FIFO_FULL:** Set to indicate that the LP generic write fifo is full
27	0x0 RW	**HS_GENERIC_WR_FIFO_FULL:** Set to indicate that the HS generic write fifo is full
26	0x0 RW	**RX_PROT_VIOLATION:** Set if DSI protocol violation error is reported in the acknowledge packet by the display device
25	0x0 RW	**RX_INVALID_TX_LENGTH:** Set if invalid transmission length error is reported in the acknowledge packet by the display device
24	0x0 RW	**ACK_WITH_NO_ERROR:** Set if acknowledge trigger message is received with out any error
23	0x0 RW	**TURN_AROUND_ACK_TIMEOUT:** Set if a turn around acknowledgement sequence is not received from the display device
22	0x0 RW	**LP_RX_TIMEOUT:** Set if a low power reception count expires this interrupt is generated

Bit Range	Default & Access	Field Name (ID): Description
21	0x0 RW	**HS_TX_TIMEOUT:** Set if a high speed transmission prevails for more than the expected count value this interrupt is raised
20	0x0 RW	**DPI_FIFO_UNDERRUN:** Set to '1' if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver
19	0x0 RW	**LOW_CONTENTION:** Set to '1' if a LP low fault is registered by at the D-PHY contention detector
18	0x0 RW	**HIGH_CONTENTION:** Set to '1' if a LP high fault is registered by at the D-PHY contention detector
17	0x0 RW	**TXDSI_VC_ID_INVALID:** Set to '1' if the received virtual channel ID is invalid
16	0x0 RW	**TXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to '1' if the received data type is not recognized
15	0x0 RW	**TXCHECKSUM_ERROR:** Set to '1' if the computed CRC differs from the received CRC value during the reception of packets by Arasan_DSI host.
14	0x0 RW	**TXECC_MULTIBIT_ERROR:** Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan_DSI_host
13	0x0 RW	**TXECC_SINGLE_BIT_ERROR:** Set to '1' if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan_DSI_host
12	0x0 RW	**TXFALSE_CONTROL_ERROR:** Set to '1' if a control error is observed on the lanes by the Arasan_DSI_host
11	0x0 RW	**RXDSI_VC_ID_INVALID:** Set to '1' if the virtual channel ID is invalid by the display device is reported in the Acknowledge packet by the display device
10	0x0 RW	**RXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to '1' if the data type is not recognized by the display device is reported in the Acknowledge packet by the display device
9	0x0 RW	**RXCHECKSUM_ERROR:** Set to '1' if the computed CRC differs from the received CRC value and is reported in the Acknowledge packet by the display device
8	0x0 RW	**RXECC_MULTIBIT_ERROR:** Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet is reported in the Acknowledge packet by the display device
7	0x0 RW	**RXECC_SINGLE_BIT_ERROR:** Set to '1' if ECC syndrome was computed and corrected for one bit error is reported in the Acknowledge packet by the display device
6	0x0 RW	**RXFALSE_CONTROL_ERROR:** Set to '1' if a control error is reported in the Acknowledge packet by the display device
5	0x0 RW	**RXHS_RECEIVE_TIMEOUT_ERROR:** Set to '1' if the high speed receive timer value expires and data transfer lasts on the data lane is reported in the Acknowledge packet by the display device
4	0x0 RW	**RX_LP_TX_SYNC_ERROR:** Set to '1' if Low power transmission sync error occurs in the display device and is reported in the Acknowledge packet by the display device

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**RXESCAPE_MODE_ENTRY_ERROR:** Set to '1' if Escape Mode Entry command is not understandable by the display device and is reported in the Acknowledge packet by the display device
2	0x0 RW	**RXEOTSYNCERROR:** Reserved.
1	0x0 RW	**RXSOTSYNCERROR:** Set to '1' if a start of transmission synchronisation error is reported in the Acknowledge packet by the display device
0	0x0 RW	**RXSOTERROR:** Set to '1' if a start of transmission error is reported in the Acknowledge packet by the display device

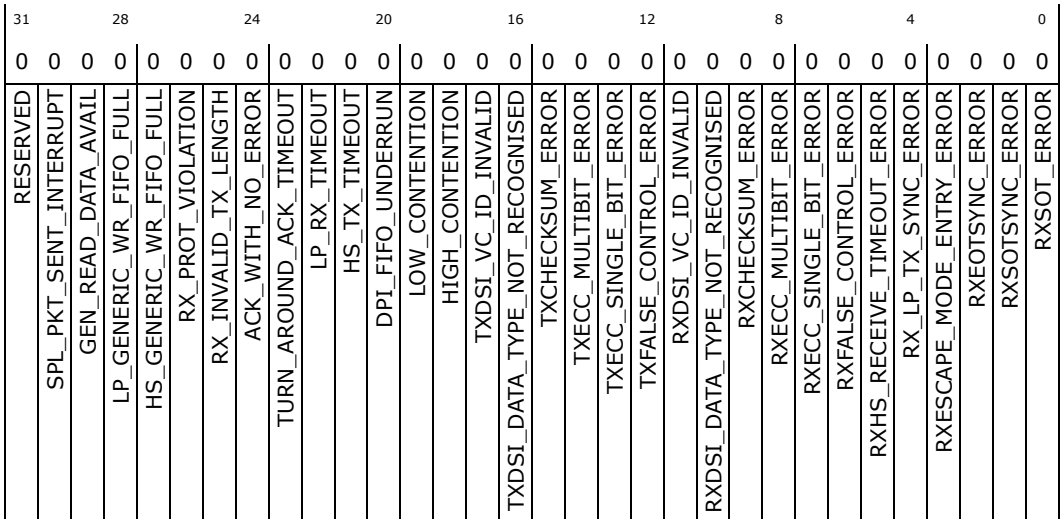
4.2.107 MIPIC_INTR_EN_REG—Offset B808h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B808h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** Reserved.
30	0x0 RW	**SPL_PKT_SENT_INTERRUPT:** Set to enable the confirmation of transmission of the DPI event specific commands set in the dpi control and dpi data register
29	0x0 RW	**GEN_READ_DATA_AVAIL:** Set to enable Generic Read available interrupt
28	0x0 RW	**LP_GENERIC_WR_FIFO_FULL:** Set to indicate that the LP generic write fifo is full

Bit Range	Default & Access	Field Name (ID): Description
27	0x0 RW	**HS_GENERIC_WR_FIFO_FULL:** Set to indicate that the HS generic write fifo is full
26	0x0 RW	**RX_PROT_VIOLATION:** Set to enable protocol violation error
25	0x0 RW	**RX_INVALID_TX_LENGTH:** Set to enable invalid transmission length error
24	0x0 RW	**ACK_WITH_NO_ERROR:** Set to enable acknowledge trigger message reception with out any error
23	0x0 RW	**TURN_AROUND_ACK_TIMEOUT:** Set to enable turn around acknowledgement ,sequence timeout
22	0x0 RW	**LP_RX_TIMEOUT:** Set to enable low power reception count timeouts
21	0x0 RW	**HS_TX_TIMEOUT:** Set to enable a high speed transmission timeout
20	0x0 RW	**DPI_FIFO_UNDERRUN:** Set to enable if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver
19	0x0 RW	**LOW_CONTENTION:** Set to enable a LP low fault interrupt
18	0x0 RW	**HIGH_CONTENTION:** Set to enable a LP high fault interrupt
17	0x0 RW	**TXDSI_VC_ID_INVALID:** Set to enable the interrupt if the received packets virtual channel ID is invalid
16	0x0 RW	**TXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to enable the interrupt if the received packets data type is not recognized
15	0x0 RW	**TXCHECKSUM_ERROR:** Set to enable the interrupt if the computed CRC differs from the received CRC value for the received packets
14	0x0 RW	**TXECC_MULTIBIT_ERROR:** Set to enable the interrupt if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan DSI host
13	0x0 RW	**TXECC_SINGLE_BIT_ERROR:** Set to enable the interrupt if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan DSIhost
12	0x0 RW	**TXFALSE_CONTROL_ERROR:** Set to enable the interrupt for the control error.,observed on the lanes by the Arasan_DSI_host
11	0x0 RW	**RXDSI_VC_ID_INVALID:** Set to enable the interrupt for invalid virtual channel ID in the acknowledgment packet reports
10	0x0 RW	**RXDSI_DATA_TYPE_NOT_RECOGNISED:** Set to enable the interrupt for the un recognized data type in the acknowledgment packet reports
9	0x0 RW	**RXCHECKSUM_ERROR:** Set to enable the interrupt for the computed CRC differs from the received CRC value in the acknowledgment packet reports
8	0x0 RW	**RXECC_MULTIBIT_ERROR:** Set to enable the interrupt for no ECC correction for the packet or there are more than 2 bit errors reported in the acknowledgment packet

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW	**RXECC_SINGLE_BIT_ERROR:** Set to enable the interrupt for ECC syndrome computation and one bit error correction for the acknowledgment packet
6	0x0 RW	**RXFALSE_CONTROL_ERROR:** Set to enable the interrupt for control error in the acknowledgment packet reports
5	0x0 RW	**RXHS_RECEIVE_TIMEOUT_ERROR:** Set to enable the interrupt for the high speed receive timeout Error in the acknowledgment packet reports
4	0x0 RW	**RX_LP_TX_SYNC_ERROR:** Set to enable the interrupt for Low power transmission sync error in the acknowledgment packet reports
3	0x0 RW	**RXESCAPE_MODE_ENTRY_ERROR:** Set to enable the interrupt for Escape Mode Entry command error in the acknowledgment packet reports
2	0x0 RW	**RXEOTSYNC_ERROR:** Set to enable the interrupt for End of transmission synchronisation Error in the acknowledgement packet reports
1	0x0 RW	**RXSOTSYNC_ERROR:** Set to enable the interrupt for start of transmission synchronisation error in the acknowledgement packet reports
0	0x0 RW	**RXSOT_ERROR:** Set to enable the interrupt for start of transmission error in the acknowledgment packet reports

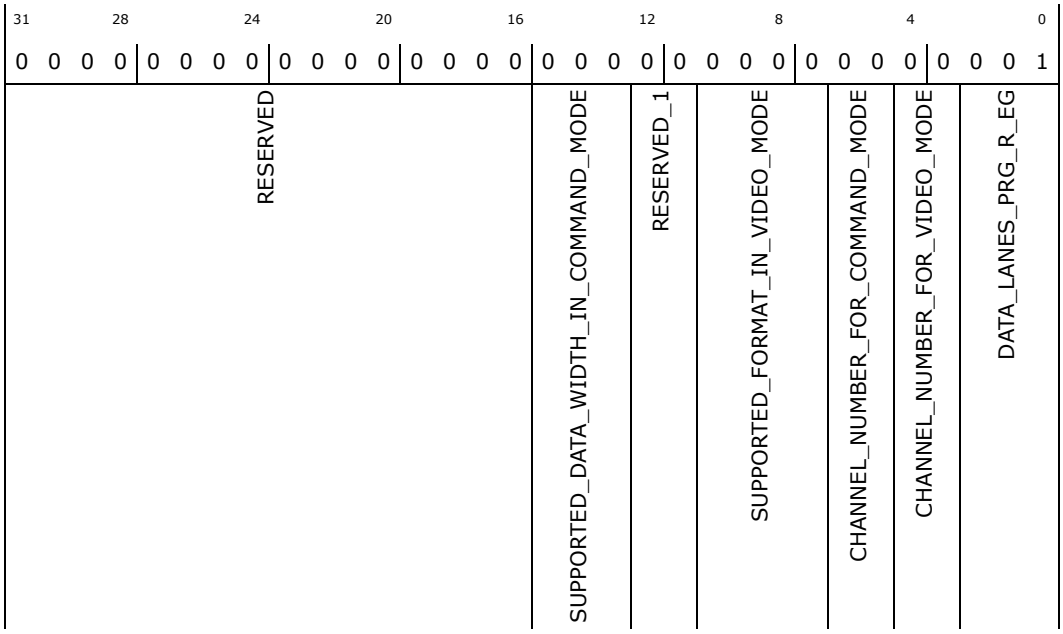
4.2.108 MIPIC_DSI_FUNC_PRG__REG—Offset B80Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B80Ch

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15:13	0x0 RW	**SUPPORTED_DATA_WIDTH_IN_COMMAND_MODE:** 000 --) Reserved, 001 --) 16 bit data , 010 --) 9 bit data , 011 --) 8 bit data , 100 --) option 1 : 101 --) option 2 : 110 to 111 --) Reserved
12:11	0x0 RO	**RESERVED_1:** Reserved.
10:7	0x0 RW	**SUPPORTED_FORMAT_IN_VIDEO_MODE:** Supported colour format, 0001 --) RGB565, 0010 --) RGB666, 0011 --) RGB 666 loosely packed format, 0100 --) RGB888
6:5	0x0 RW	**CHANNEL_NUMBER_FOR_COMMAND_MODE:** Virtual channel number for command mode is programmed by the processor
4:3	0x0 RW	**CHANNEL_NUMBER_FOR_VIDEO_MODE:** Virtual channel number for command mode is programmed by the processor
2:0	0x1 RW	**DATA_LANES_PRG_R_EG:** Number of data lanes to be supported is programmed by the processor

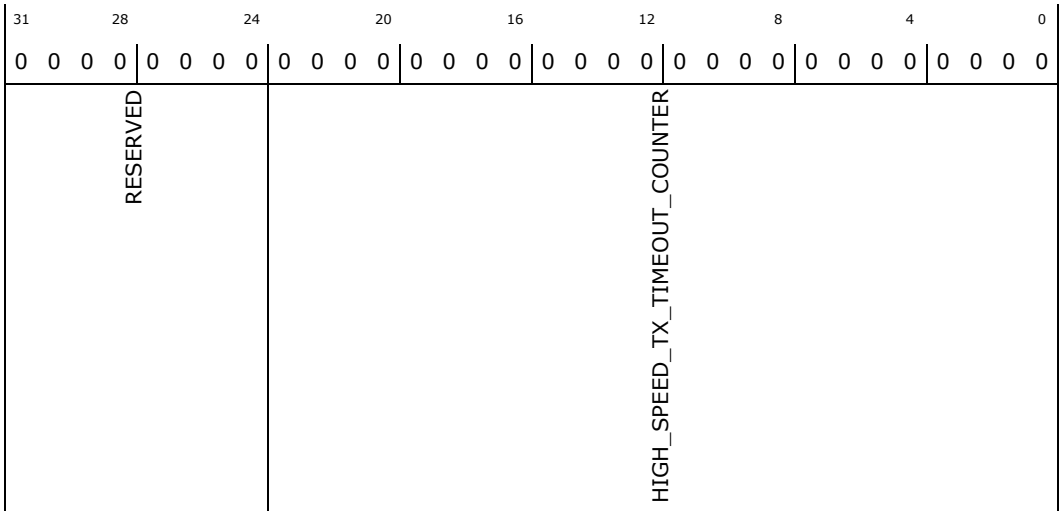
4.2.109 MIPIC_HS_TX_TIMEOUT_REG—Offset B810h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B810h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:0	0x0 RW	**HIGH_SPEED_TX_TIMEOUT_COUNTER:** The maximum duration allowed for the DSI host ,to remain in high speed mode for a transmission. If the counter expires, HS mode is terminated with EOT and the lanes enter stop state

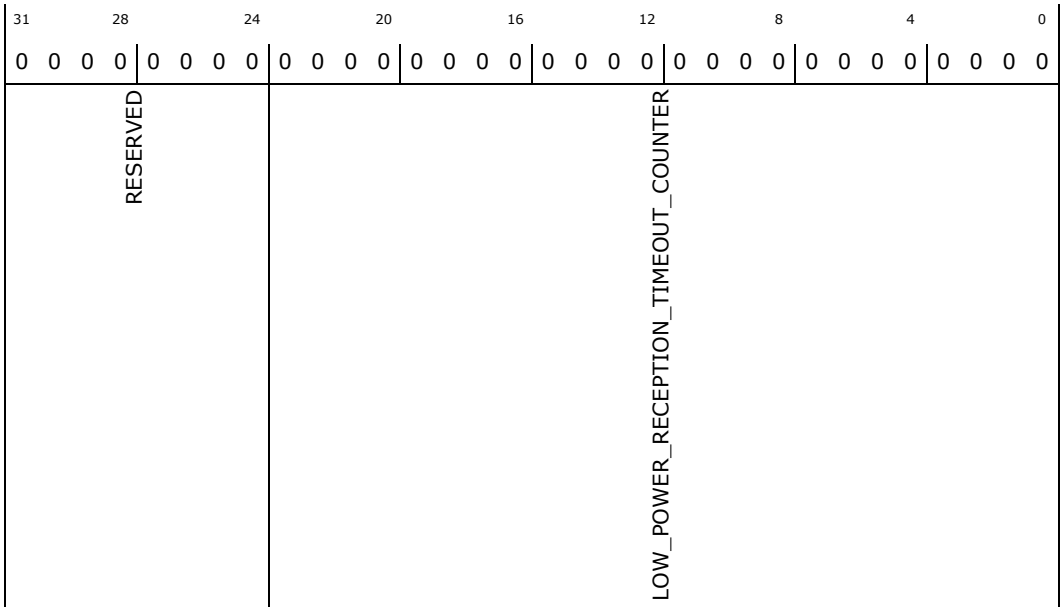
4.2.110 MIPIC_LP_RX_TIMEOUT_REG—Offset B814h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B814h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:0	0x0 RW	**LOW_POWER_RECEPTION_TIMEOUT_COUNTER:** Timeout value to be checked for received short packets .If the timer expires the DSI Host enters stop state

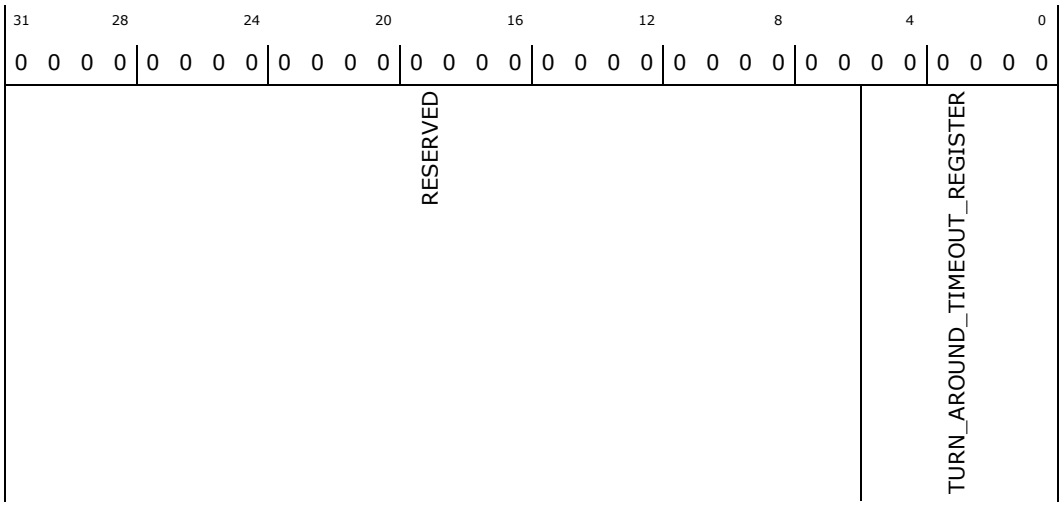
4.2.111 MIPIC_TURN_AROUND_TIMEOUT_REG—Offset B818h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B818h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**RESERVED:** Reserved.
5:0	0x0 RW	**TURN_AROUND_TIMEOUT_REGISTER:** Timeout value to be checked after the DSI host makes a turn around in the direction of transfers. If the timer expires the DSI Host enters stop state

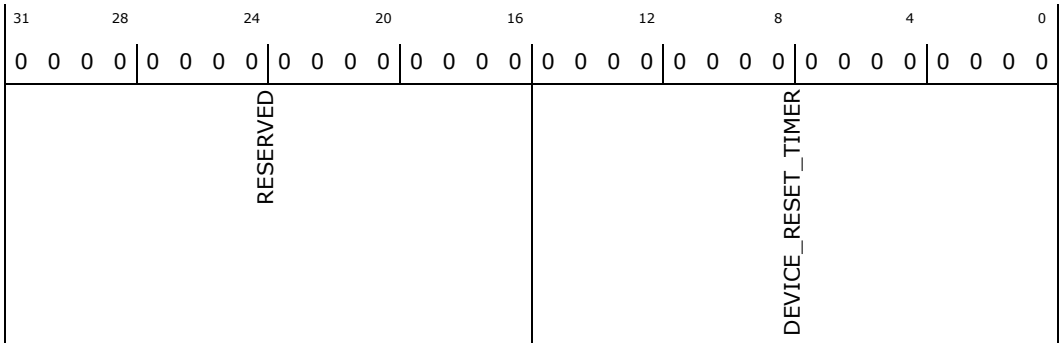
4.2.112 MIPIC_DEVICE_RESET_TIMER—Offset B81Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B81Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15:0	0x0 RW	**DEVICE_RESET_TIMER:** Timeout value to be checked for device to be reset after issuing reset entry command. If the timer expires the DSI Host enters normal operation

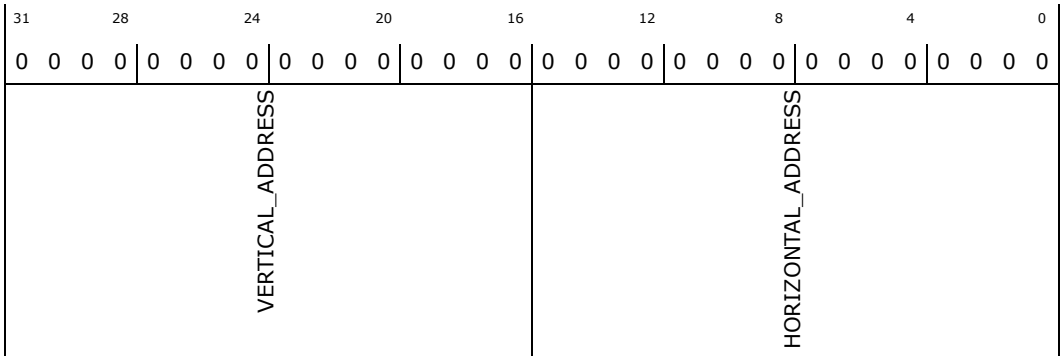
4.2.113 MIPIC_DPI_RESOLUTION_REG—Offset B820h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B820h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**VERTICAL_ADDRESS:** Shows the vertical address count in lines
15:0	0x0 RW	**HORIZONTAL_ADDRESS:** Shows the horizontal address count in pixels

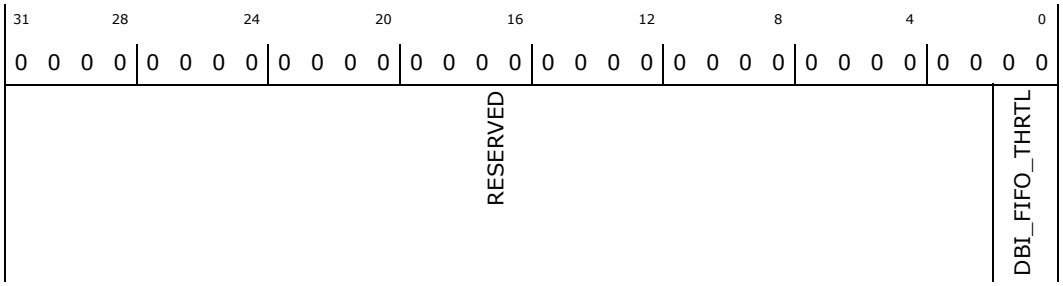
4.2.114 MIPIC_DBI_RESOLUTION_REG—Offset B824h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B824h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**RESERVED:** Reserved.
1:0	0x0 RW	**DBI_FIFO_THRTL:** DBI FIFO's watermark can be set using the following bits so as to enable dbi_stall de-assertion whenever the below FIFO condition is reached: 00 - (1/2) DBI fifo empty 01 - (1/4) DBI fifo empty 10 - 7 locations are empty 11 - Reserved

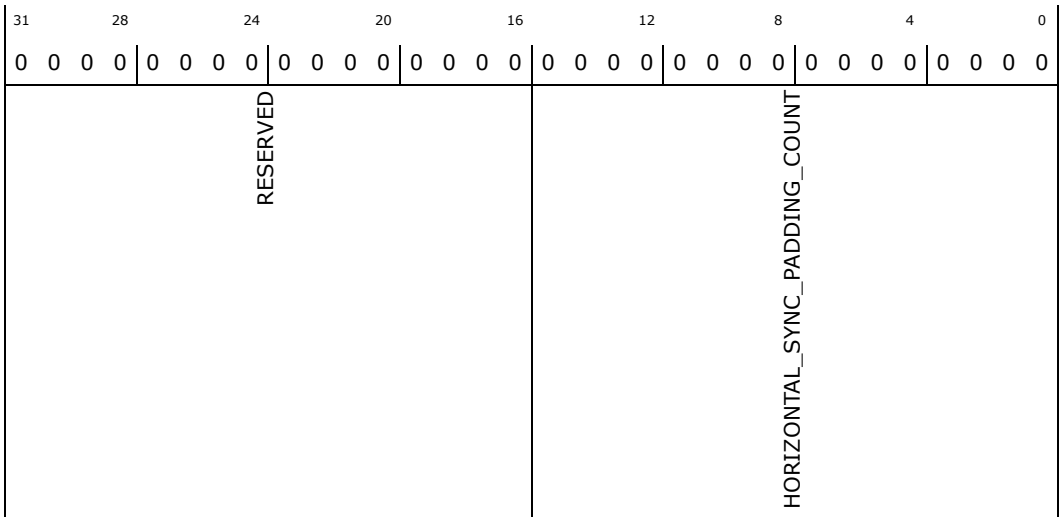
4.2.115 MIPIC_HORIZ_SYNC_PADDING_COUNT—Offset B828h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B828h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15:0	0x0 RW	**HORIZONTAL_SYNC_PADDING_COUNT:** Shows the horizontal sync padding value in terms of txbyteclkhs

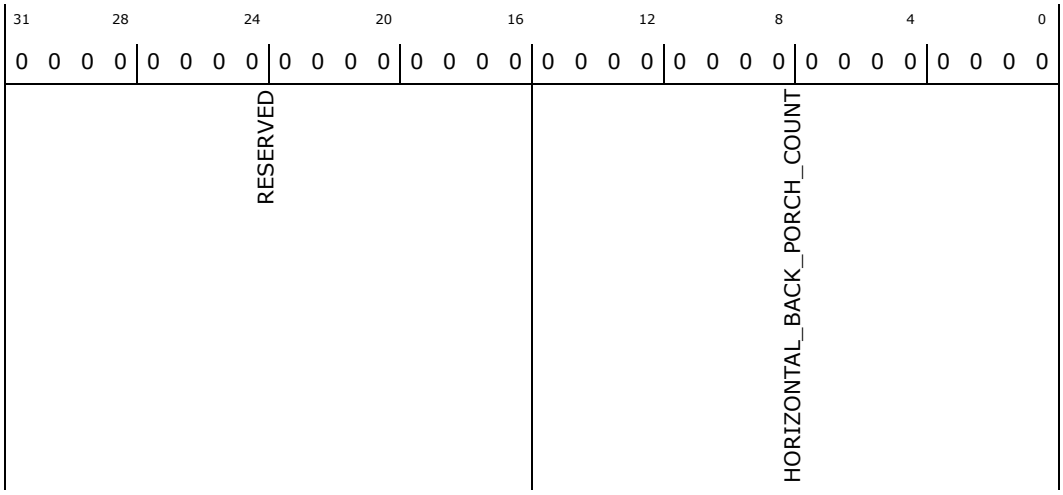
4.2.116 MIPIC_HORIZ_BACK_PORCH_COUNT—Offset B82Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B82Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15:0	0x0 RW	**HORIZONTAL_BACK_PORCH_COUNT:** Shows the horizontal back porch value in terms of txbyteclkhs

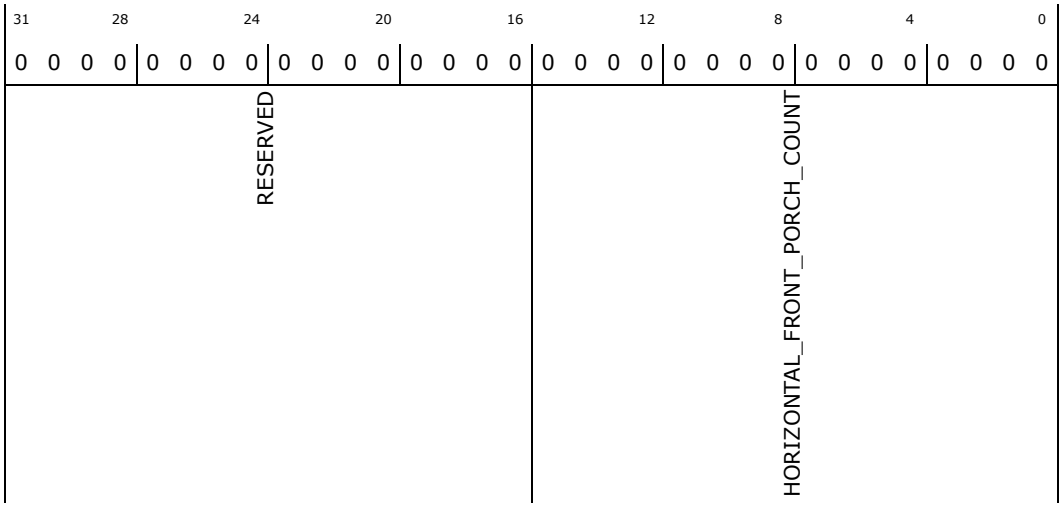
4.2.117 MIPIC_HORIZ_FRONT_PORCH_COUNT—Offset B830h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B830h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15:0	0x0 RW	**HORIZONTAL_FRONT_PORCH_COUNT:** Shows the horizontal front porch value in terms of txbyteclkhs

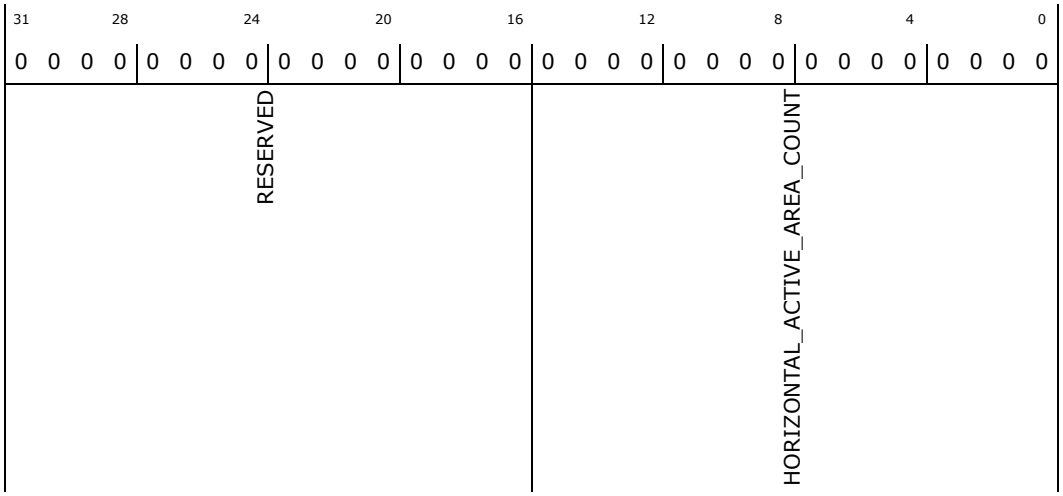
4.2.118 MIPIC_HORIZ_ACTIVE_AREA_COUNT—Offset B834h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B834h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15:0	0x0 RW	**HORIZONTAL_ACTIVE_AREA_COUNT:** Shows the horizontal active area value in terms of txbyteclkhs

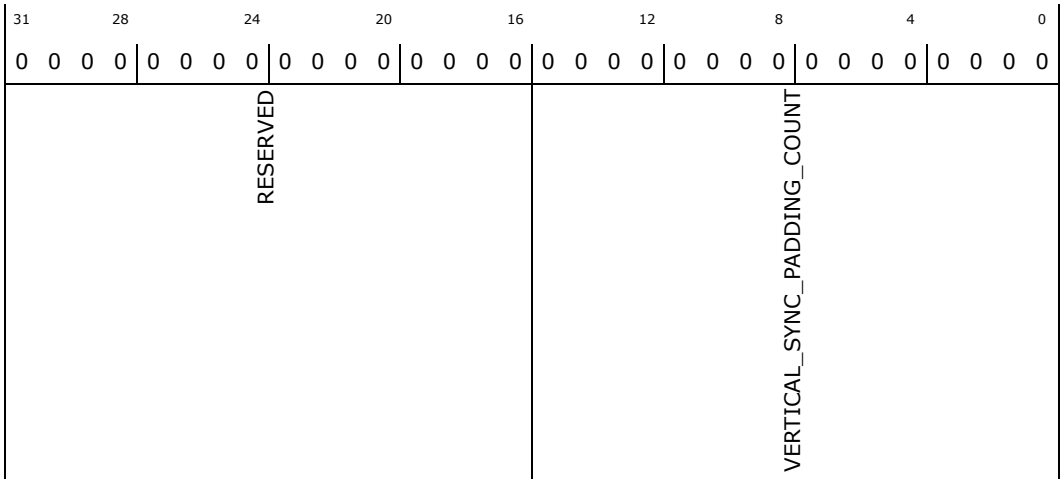
4.2.119 MIPIC_VERT_SYNC_PADDING_COUNT—Offset B838h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B838h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15:0	0x0 RW	**VERTICAL_SYNC_PADDING_COUNT:** Shows the vertical sync padding value in terms of lines

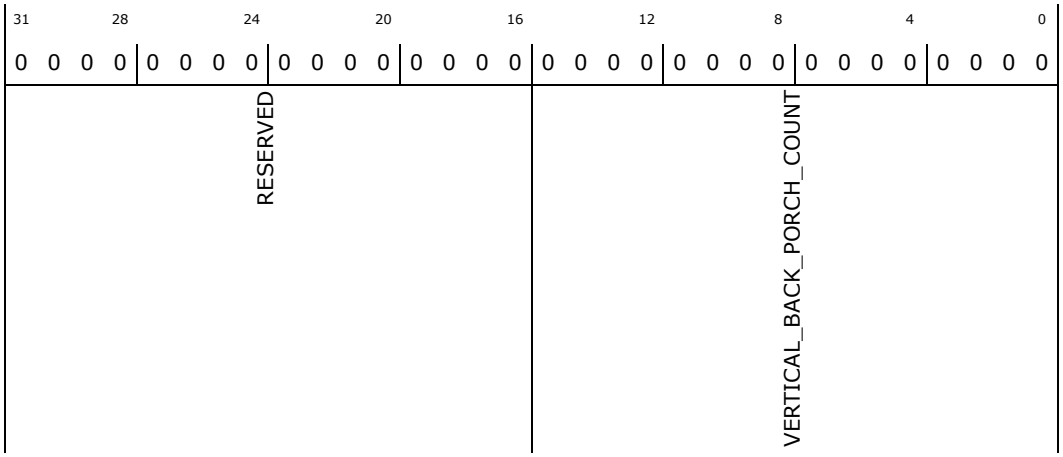
4.2.120 MIPIC_VERT_BACK_PORCH_COUNT—Offset B83Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B83Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15:0	0x0 RW	**VERTICAL_BACK_PORCH_COUNT:** Shows the vertical back porch value in terms of lines

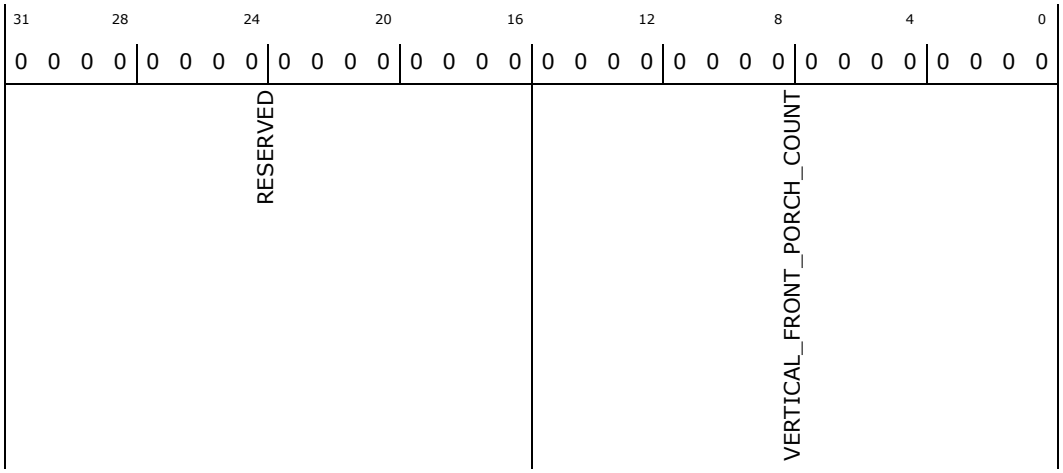
4.2.121 MIPIC_VERT_FRONT_PORCH_COUNT—Offset B840h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B840h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW	**VERTICAL_FRONT_PORCH_COUNT:** Shows the vertical front porch value in terms of lines

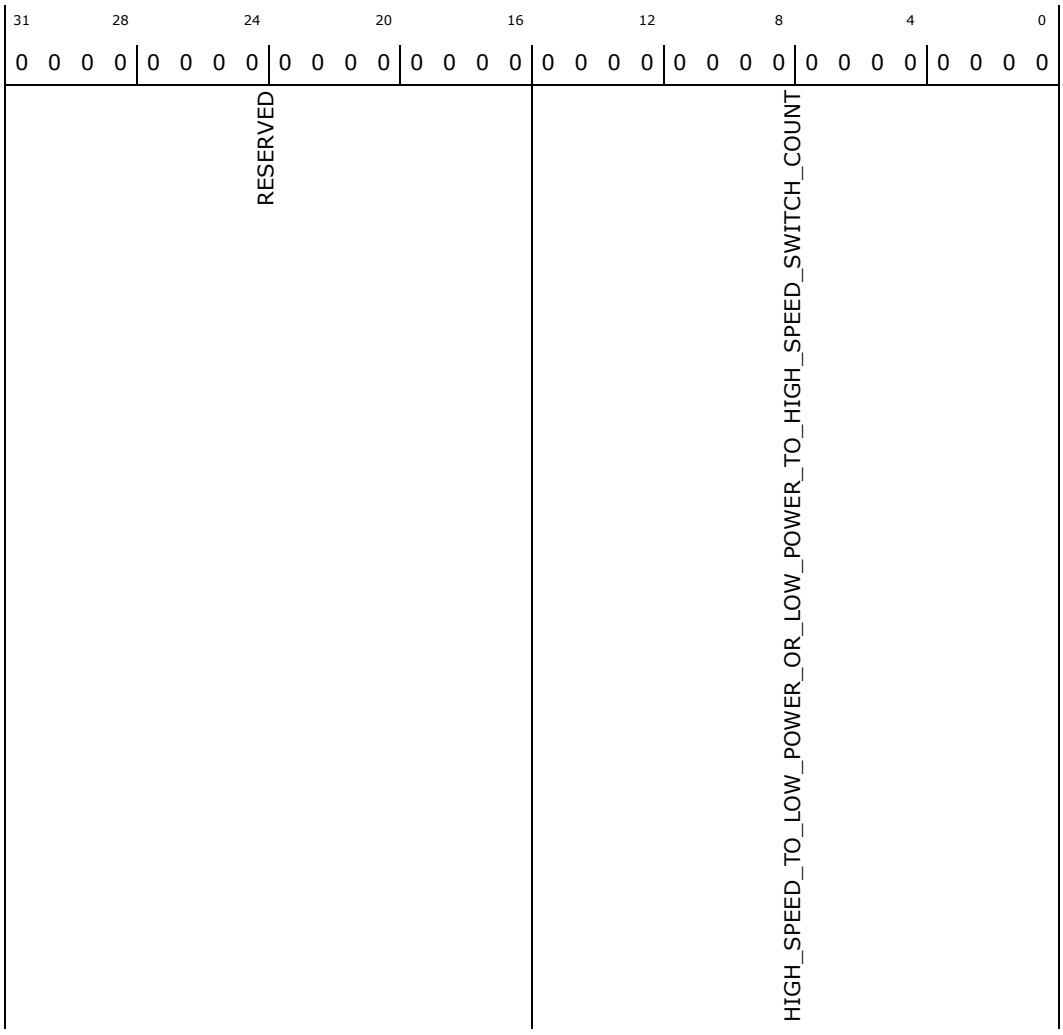
4.2.122 MIPIC_HIGH_LOW_SWITCH_COUNT—Offset B844h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B844h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** High speed to low power or Low power to high speed switching time in terms of txbyteclkhs
15:0	0x0 RW	**HIGH_SPEED_TO_LOW_POWER_OR_LOW_POWER_TO_HIGH_SPEED_SWITCH_COUNT:** High speed to low power or Low power to high speed switching time in terms of txbyteclkhs

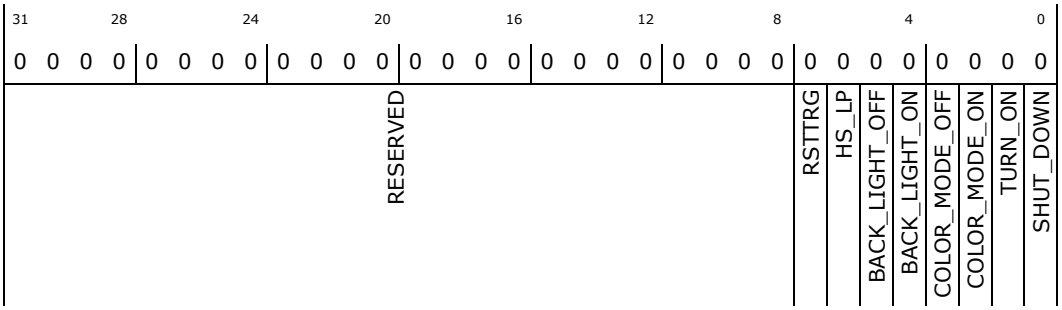
4.2.123 MIPIC_DPI_CTRL_REG—Offset B848h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B848h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED:**
7	0x0 RW	**RSTTRG:** Reserved.
6	0x0 RW	**HS_LP:** Set to '0' to indicate the special packets are sent through the DSI link using HS transmission and set to '1' to indicate that the special packets are sent through the DSI link using low power mode
5	0x0 RW	**BACK_LIGHT_OFF:** Set to '1' to indicate a backlight OFF short packet has to be packetised for the DPI's virtual channel
4	0x0 RW	**BACK_LIGHT_ON:** Set to '1' to indicate a backlight ON short packet has to be packetised for the DPI's virtual channel
3	0x0 RW	**COLOR_MODE_OFF:** Set to '1' to indicate a color mode OFF short packet has to be packetised for the DPI's virtual channel
2	0x0 RW	**COLOR_MODE_ON:** Set to '1' to indicate a color mode ON short packet has to be packetised for the DPI's virtual channel
1	0x0 RW	**TURN_ON:** Set to '1' to indicate a turn on short packet has to be packetised for the DPI's virtual channel
0	0x0 RW	**SHUT_DOWN:** Set to '1' to indicate a shut down short packet has to be packetised for the DPI's virtual channel

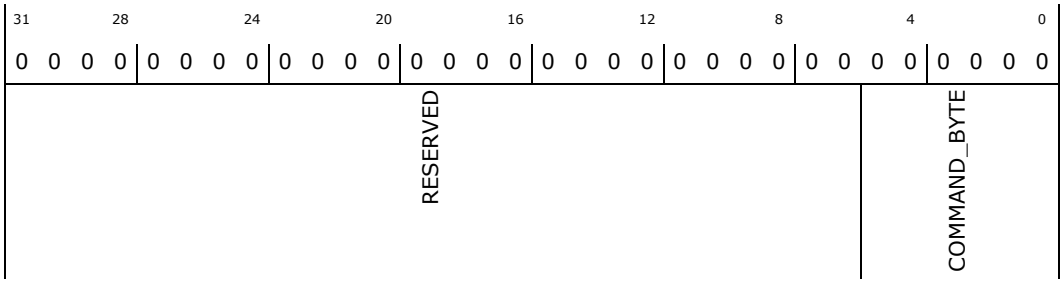
4.2.124 MIPIC_DPI_DATA_REGISTER—Offset B84Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B84Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**RESERVED:** Reserved.
5:0	0x0 RW	**COMMAND_BYTE:** Command Byte to represent the new or not defined command bytes usage for special features representation. [Like backlight ON and OFF]. This register should be programmed before the DPI control register is being programmed for backlight ON/OFF

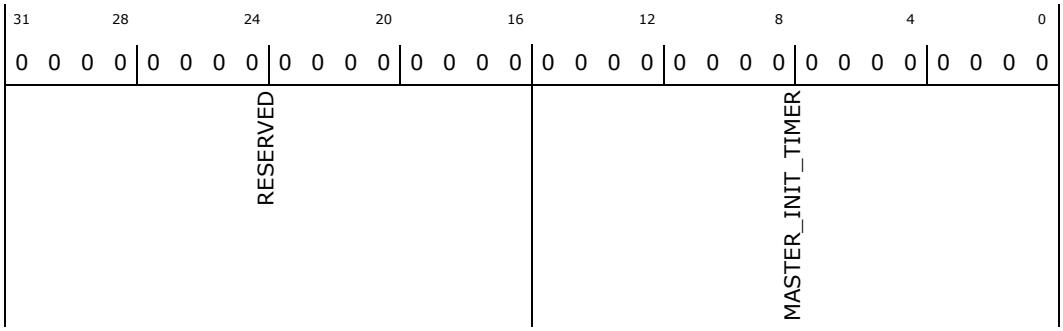
4.2.125 MIPIC_INIT_COUNT_REGISTER—Offset B850h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B850h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW	**MASTER_INIT_TIMER:** Counter value in terms of low power clock to initialise the DSI Host IP [TINT] that drives a stop state on the mipi's D-PHY bus

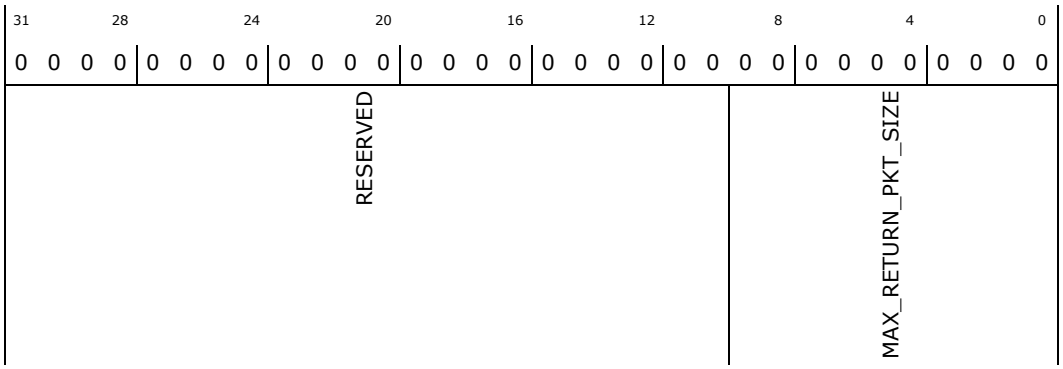
4.2.126 MIPIC_MAX_RETURN_PKT_SIZE_REGISTER—Offset B854h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B854h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**RESERVED:** Reserved.
9:0	0x0 RW	**MAX_RETURN_PKT_SIZE:** Set the count value in bytes to collect the return data packet for reverse direction data flow in data lane0 in response to a DBI read operation

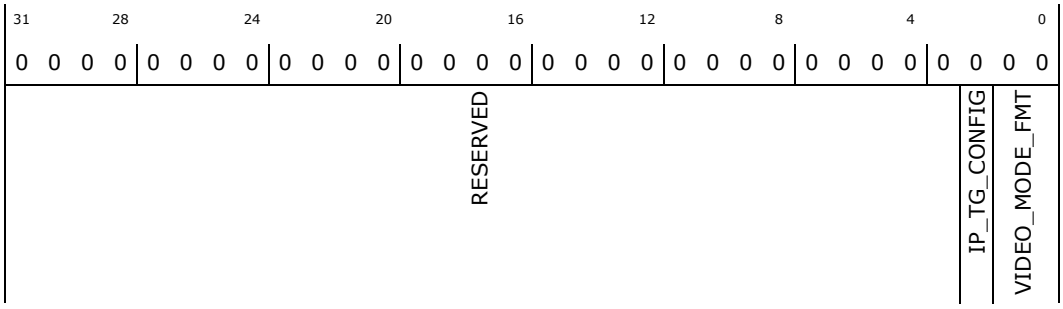
4.2.127 MIPIC_VIDEO_MODE_FORMAT_REGISTER—Offset B858h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B858h

Default: 00000000h



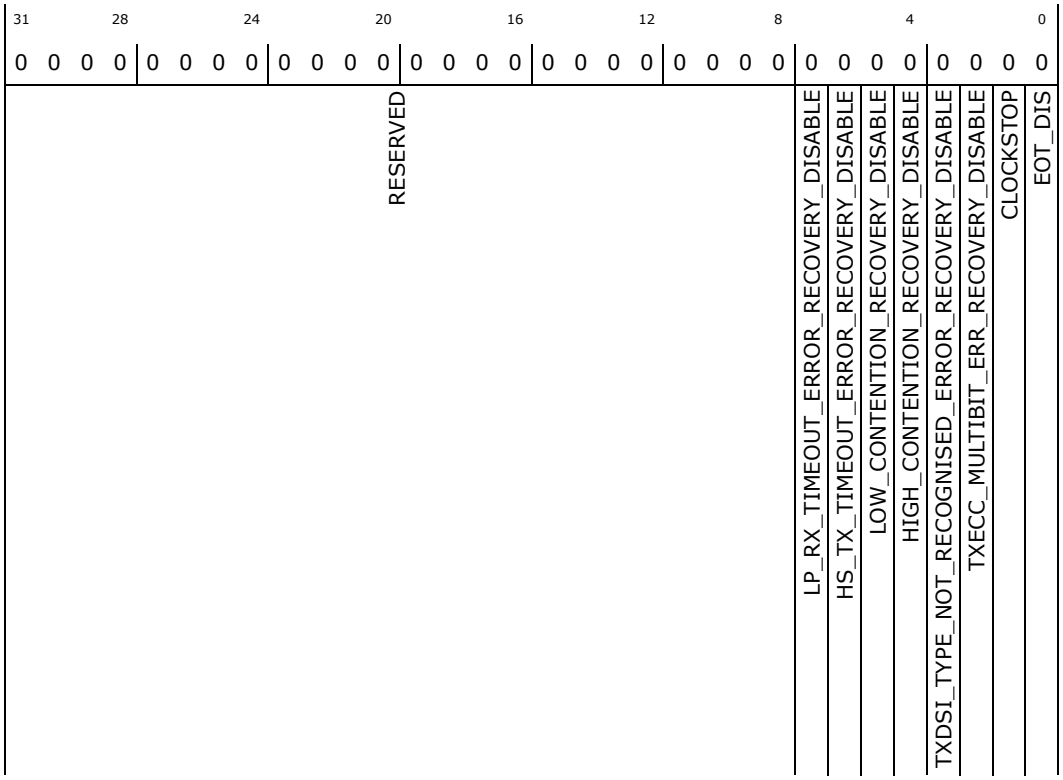
Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**RESERVED:** Reserved.
2	0x0 RW	**IP_TG_CONFIG:** Set by the processor to inform that the DSI controller should discontinue the DPI transfer after the last line of the VFP after ip_tg_enable deassertion. By default, this bit is set to 0. 0 - After ip_tg_enable deassertion, DSI Tx controller stops the DPI transfer immediately after the current packet is transmitted. 1 - After ip_tg_enable deassertion, DSI Tx controller discontinues the DPI transfer after the last line of the VFP
1:0	0x0 RW	**VIDEO_MODE_FMT:** Sets the Video mode format (packet sequence) to be supported in DSI. In Non Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed equal to RGB word count value In Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed greater than the RGB word count value, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link. 00 Reserved 01 - Non Burst Mode with Sync Pulse 10 - Non Burst Mode with Sync events 11 - Burst Mode

4.2.128 MIPIC_EOT_DISABLE_REGISTER—Offset B85Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** B85Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED:** Reserved.
7	0x0 RW	**LP_RX_TIMEOUT_ERROR_RECOVERY_DISABLE:** Set by the processor to enable or disable the LP_Rx_timeout error recovery if the processor clears LP_Rx_timeout error interrupt. 0 - LP_Rx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the LP_Rx_timeout error interrupt. 1 - If the processor clears the LP_Rx_timeout error interrupt, LP_Rx_timeout error recovery action will not happen in DSI Tx controller. LP Rx timeout error interrupt will act as an informative interrupt
6	0x0 RW	**HS_TX_TIMEOUT_ERROR_RECOVERY_DISABLE:** Set by the processor to enable or disable the HS_Tx_timeout error recovery if the processor clears HS_Tx_timeout interrupt. 0 - HS_Tx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the HS_Tx_timeout error interrupt. 1 - If the processor clears the HS_Tx_timeout error interrupt, HS_Tx_timeout error recovery action will not happen in DSI Tx controller. HS Tx timeout error interrupt will act as an informative interrupt

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**LOW_CONTENTION_RECOVERY_DISABLE:** Set by the processor to enable or disable the contention recovery procedure if the processor clears Low contention interrupt. 0 - Contention recovery will happen if the processor clears Low contention interrupt. 1 - If the processor clears the low contention interrupt, contention recovery procedure will not be initiated by the DSI Tx controller. Low contention interrupt will act as an informative interrupt
4	0x0 RW	**HIGH_CONTENTION_RECOVERY_DISABLE:** Set by the processor to enable or disable the contention recovery procedure if the processor clears High contention interrupt. 0 - Contention recovery will happen if the processor clears High contention interrupt. 1 - If the processor clears the high contention interrupt, contention recovery procedure will not be initiated by the DSI Tx controller. Ignore the High Contention Interrupt in MIPI_INTR_STAT_REG
3	0x0 RW	**TXDSI_TYPE_NOT_RECOGNISED_ERROR_RECOVERY_DISABLE:** Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if TxDSI data type not recognized error interrupt is cleared by the processor. 0 - Error recovery action will be taken if TxDSI data type not recognized error interrupt is cleared by the processor. 1 - If TxDSI data type not recognized error interrupt is cleared by the processor, error recovery action will not be taken by the DSI TX controller. Tx DSI data type not recognized error interrupt will act as an informative interrupt
2	0x0 RW	**TXECC_MULTIBIT_ERR_RECOVERY_DISABLE:** Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if Tx ECC multibit error interrupt is cleared by the processor. 0 - Error recovery action will be taken if Tx ECC multibit error interrupt is cleared by the processor. 1 - If Tx ECC multibit error interrupt is cleared by the processor, error recovery action will not be taken by the DSI TX controller. Tx multibit error interrupt will act as an informative interrupt
1	0x0 RW	**CLOCKSTOP:** Set by the processor to enable or disable clock stopping feature during BLLP timing in a DPI transfer in dual channel mode or during DPI only mode and also when there is no traffic in the DBI interface in DBI only enabled mode. By default this register value is 0. 0 - clock stopping disabled 1 - clock stopping enabled
0	0x0 RW	**EOT_DIS:** Set by the processor to enable or disable EOT short packet transmission. By default this register value is 0. For backward compatibility of earlier DSI systems, EOT short packet transmission can be disabled. 0 - EOT short packet transmission enabled 1 - EOT short packet transmission disabled

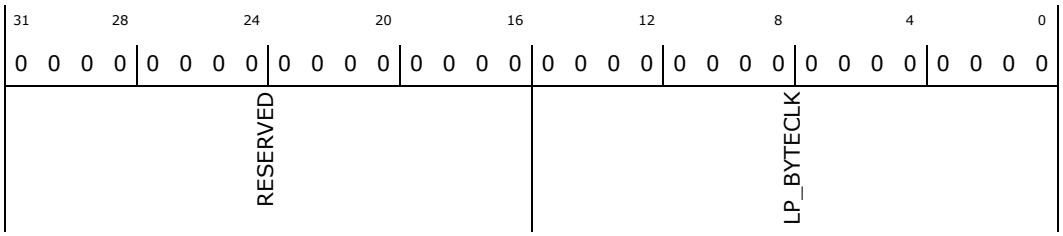
4.2.129 MIPIC_LP_BYTECLK_REGISTER—Offset B860h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B860h

Default: 00000000h



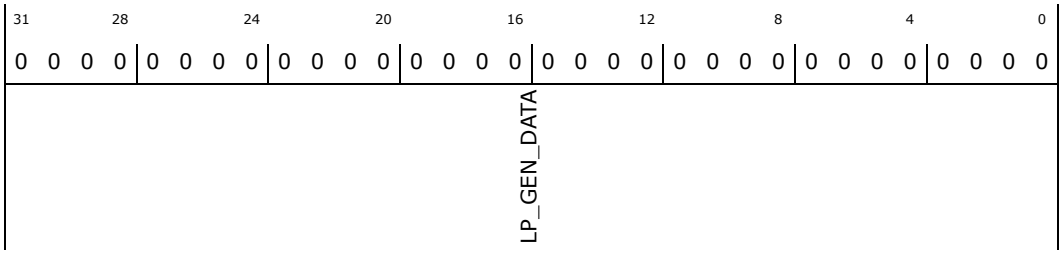
Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15:0	0x0 RW	**LP_BYTECLK:** Low power clock equivalence in terms of byte clock. The value programmed in this register is equal to the number of byte clocks occupied in one low power clock. This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc)

4.2.130 MIPIC_LP_GEN_DATA_REGISTER—Offset B864h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** B864h

Default: 00000000h



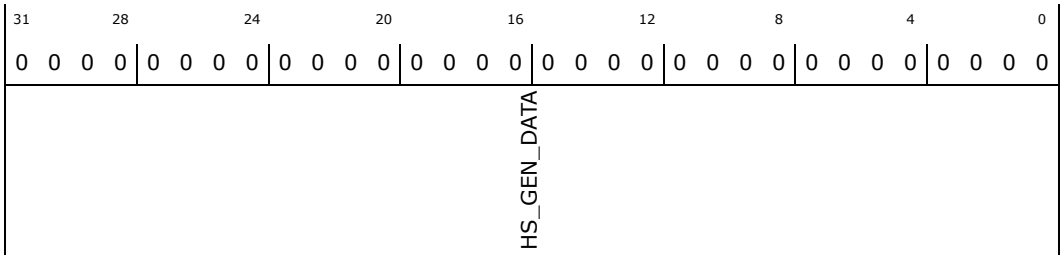
Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**LP_GEN_DATA:** Data port register used for generic data transfers in low power mode

4.2.131 MIPIC_HS_GEN_DATA_REGISTER—Offset B868h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** B868h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**HS_GEN_DATA:** Data port register used for generic data transfers in low power mode

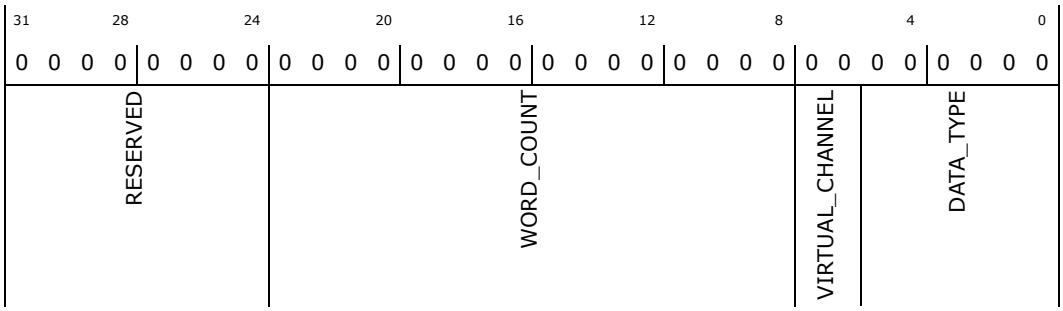
4.2.132 MIPIC_LP_GEN_CTRL_REGISTER—Offset B86Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B86Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:8	0x0 WO	**WORD_COUNT:** Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets. Note: Invalid parameters must be set to 00h
7:6	0x0 WO	**VIRTUAL_CHANNEL:** Used to specify the virtual channel for which the generic data transmission is intended

Bit Range	Default & Access	Field Name (ID): Description
5:0	0x0 WO	**DATA_TYPE:** Used to specify the generic data types 03h - Generic short write, no parameters 13h - Generic short write, 1 parameter 23h - Generic short write, 2 parameters 04h - Generic read, no parameters 14h - Generic read, 1 parameter 24h - Generic read 2 parameter 29h - Generic long write 05h - Manufacturer DCS short write, no parameter 15h - Manufacturer DCS short write, one parameter 06h - Manufacturer DCS read, no parameter 39h - Manufacturer DCS long write

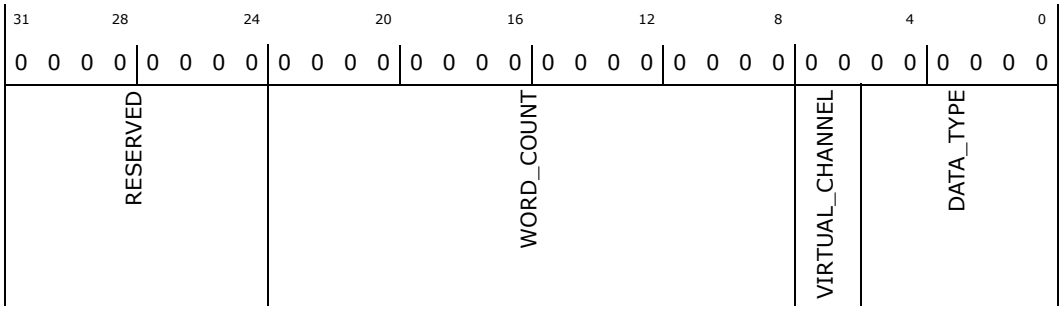
4.2.133 MIPIC_HS_GEN_CTRL_REGISTER—Offset B870h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B870h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:8	0x0 WO	**WORD_COUNT:** Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets. Note: Invalid parameters must be set to 00h
7:6	0x0 WO	**VIRTUAL_CHANNEL:** Used to specify the virtual channel for which the generic data transmission is intended

Bit Range	Default & Access	Field Name (ID): Description
5:0	0x0 WO	**DATA_TYPE:** Used to specify the generic data types 03h - Generic short write, no parameters 13h - Generic short write, 1 parameter 23h - Generic short write, 2 parameters 04h - Generic read, no parameters 14h - Generic read, 1 parameter 24h - Generic read 2 parameter 29h - Generic long write 05h - Manufacturer DCS short write, no parameter 15h - Manufacturer DCS short write, one parameter 06h - Manufacturer DCS read, no parameter 39h - Manufacturer DCS long write

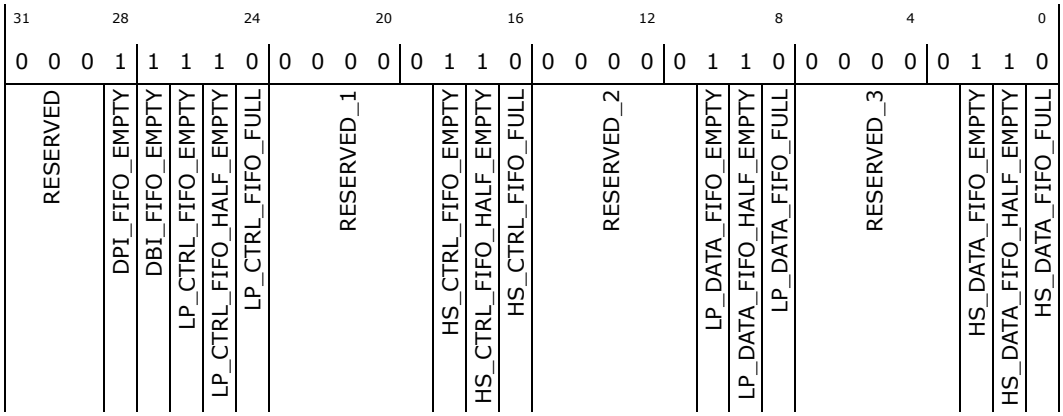
4.2.134 MIPIC_GEN_FIFO_STAT_REGISTER—Offset B874h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B874h

Default: 1E060606h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Reserved.
28	0x1 RO	**DPI_FIFO_EMPTY:** Default 1
27	0x1 RO	**DBI_FIFO_EMPTY:** Default 1
26	0x1 RO	**LP_CTRL_FIFO_EMPTY:** Default 1
25	0x1 RO	**LP_CTRL_FIFO_HALF_EMPTY:** Default 1
24	0x0 RO	**LP_CTRL_FIFO_FULL:** Default 0

Bit Range	Default & Access	Field Name (ID): Description
23:19	0x0 RO	**RESERVED_1:** Reserved.
18	0x1 RO	**HS_CTRL_FIFO_EMPTY:** Default 1
17	0x1 RO	**HS_CTRL_FIFO_HALF_EMPTY:** Default 1
16	0x0 RO	**HS_CTRL_FIFO_FULL:** Default 0
15:11	0x0 RO	**RESERVED_2:** Reserved.
10	0x1 RO	**LP_DATA_FIFO_EMPTY:** Default 1
9	0x1 RO	**LP_DATA_FIFO_HALF_EMPTY:** Default 1
8	0x0 RO	**LP_DATA_FIFO_FULL:** Default 0
7:3	0x0 RO	**RESERVED_3:** Reserved.
2	0x1 RO	**HS_DATA_FIFO_EMPTY:** Default 1
1	0x1 RO	**HS_DATA_FIFO_HALF_EMPTY:** Default 1
0	0x0 RO	**HS_DATA_FIFO_FULL:** Default 0

4.2.135 MIPIC_HS_LS_DBI_ENABLE_REG—Offset B878h

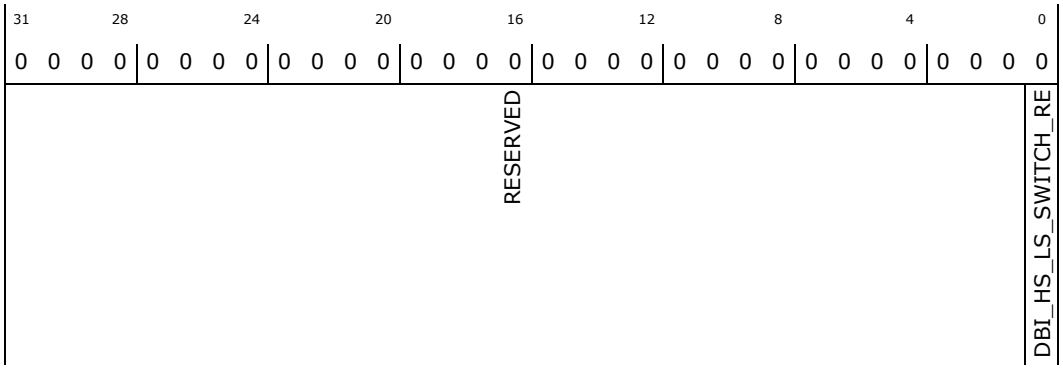
Note : dbi_hs_lp_switch_reg has to be written only if DBI FIFO is empty

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B878h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RESERVED:** Reserved.
0	0x0 RW	**DBI_HS_LS_SWITCH_RE:** Set to 1 if DBI packets have to be transmitted in Low power mode Set to 0 if DBI packets have to be transmitted in High speed mode

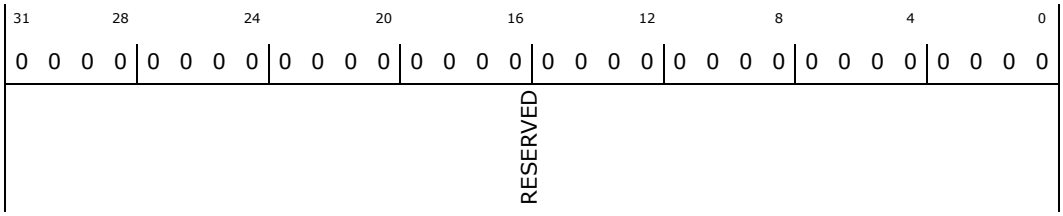
4.2.136 MIPIC_RESERVED—Offset B87Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B87Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RESERVED:** Reserved.

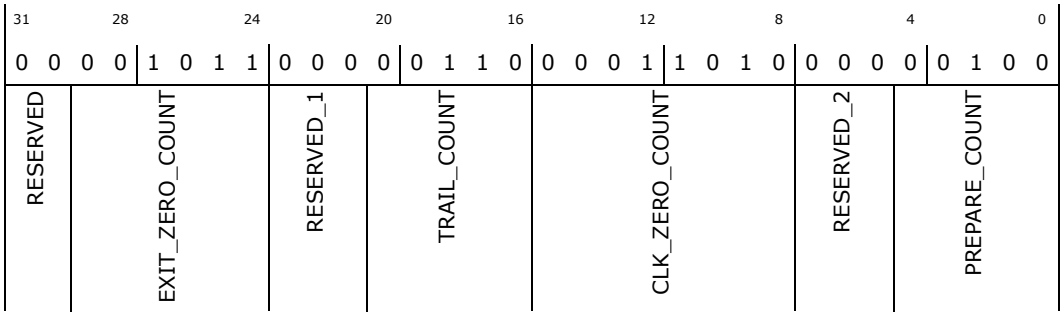
4.2.137 MIPIC_DPHY_PARAM_REG—Offset B880h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B880h

Default: 0B061A04h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RESERVED:** Reserved.
29:24	0xb RW	**EXIT_ZERO_COUNT:** THS_0_TIM_UI_CNT and THS_EXIT_TIM_UI_CNT for dphy are programmed as exit zero count by the processor
23:21	0x0 RO	**RESERVED_1:** Reserved.
20:16	0x6 RW	**TRAIL_COUNT:** TCLK_POST_TIM_UI_CNT and TCLK_TRAIL_TIM_UI_CNT for dphy are programmed as trail count by the processor
15:8	0x1a RW	**CLK_ZERO_COUNT:** TCLK_0_TIM_UI_CNT for dphy is programmed as clk zero count by the processor
7:5	0x0 RO	**RESERVED_2:** Reserved.
4:0	0x4 RW	**PREPARE_COUNT:** TCLK_PREP_TIM_UI_CNT and THS_PREP_TIM_UI_CNT for dphy are programmed as prepare count by the processor

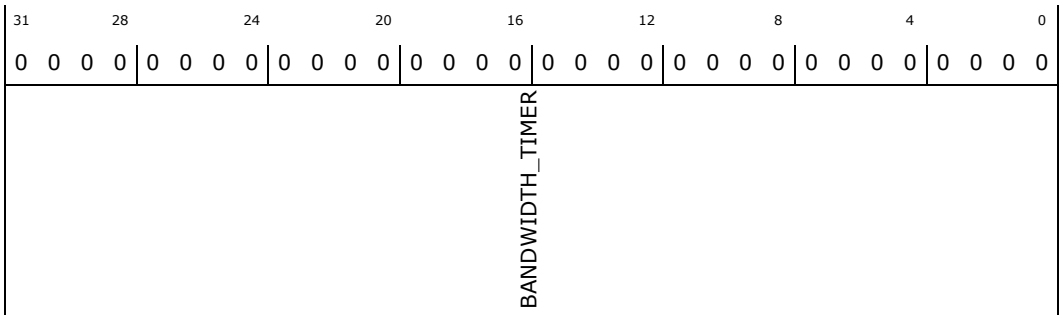
4.2.138 MIPIC_DBI_BW_CTRL_REG—Offset B884h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B884h

Default: 00000000h



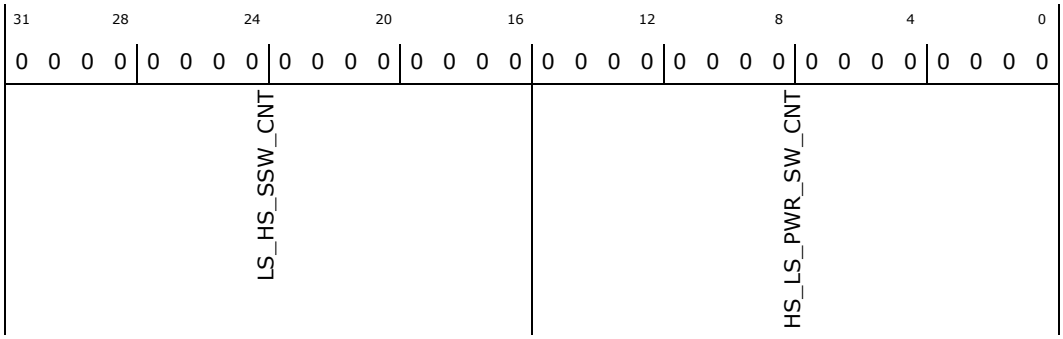
Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**BANDWIDTH_TIMER:** DBI Bandwidth control Register. The bandwidth essential for transmitting 16 long packets containing 252 bytes meant for DCS write memory command is programmed in this register in terms of byte clocks. Based on the DSI transfer rate and the number of lanes configured the time taken to transmit 16 long packets in a DSI stream varies. Note: The value programmed in this timer must be greater than the actual time taken to carry out 16 long packets transmission in DSI stream plus the time taken to transmit two blanking packets

4.2.139 MIPIC_CLK_LANE_SWITCHING_TIME_CNT—Offset B888h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** B888h

Default: 00000000h



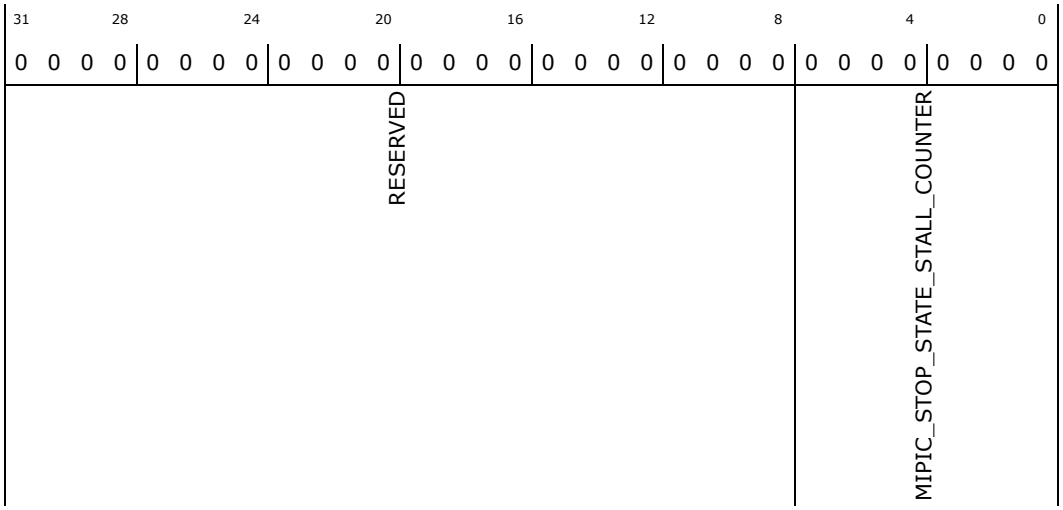
Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**LS_HS_SSW_CNT:** Low power to high speed switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks required to switch from low power mode to high speed mode after txrequesths_clk is asserted. Current Value is ah = 10 txbyteclkhs
15:0	0x0 RW	**HS_LS_PWR_SW_CNT:** High speed to low power switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks request to switch from high speed mode to low power mode after txrequesths_clk is de-asserted. Current Value is 14h = 20 txbyteclkhs

4.2.140 MIPIC_STOP_STATE_STALL—Offset B88Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** B88Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED:**
7:0	0x0 RW	**MIPIC_STOP_STATE_STALL_COUNTER:** Delay between (stall the stop state signal) the data transfer is increased based on this counter value. This counter is calculated from txclkesc. Note: If processor programs this register then it needs to reprogram the high_low_ switch counter in B844h and lp_equivalent_byteclk reg in B860h to compensate this delay. High_low_switch_count B844h: High to low switch counter = Actual High to low switch + stop_sta_stall_reg value * Low power clock equivalence value in terms of byte clock LP equivalent byteclk register B860h: LP equivalent byteclk value = txclkesc time/ txbyteclk time * (105 + stop_sta_stall_reg value) / 105 Minimum time of Low Power short packet transfer = 105 txclkesc

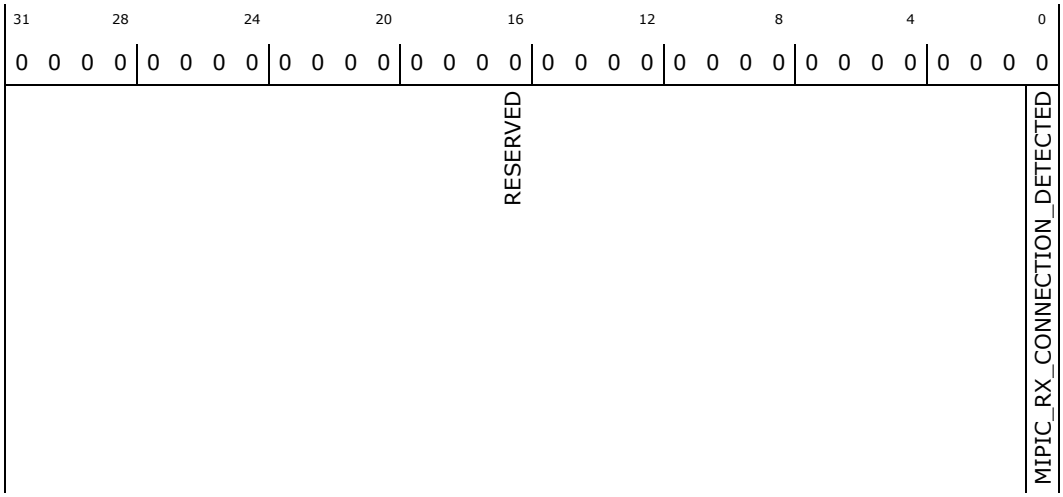
4.2.141 MIPIC_INTR_STAT_REG_1—Offset B890h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B890h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RESERVED:**
0	0x0 RW	**MIPIC_RX_CONNECTION_DETECTED:** Set to 1'b1 if the contention detected in the display device and is reported in the Acknowledge packet by the display device

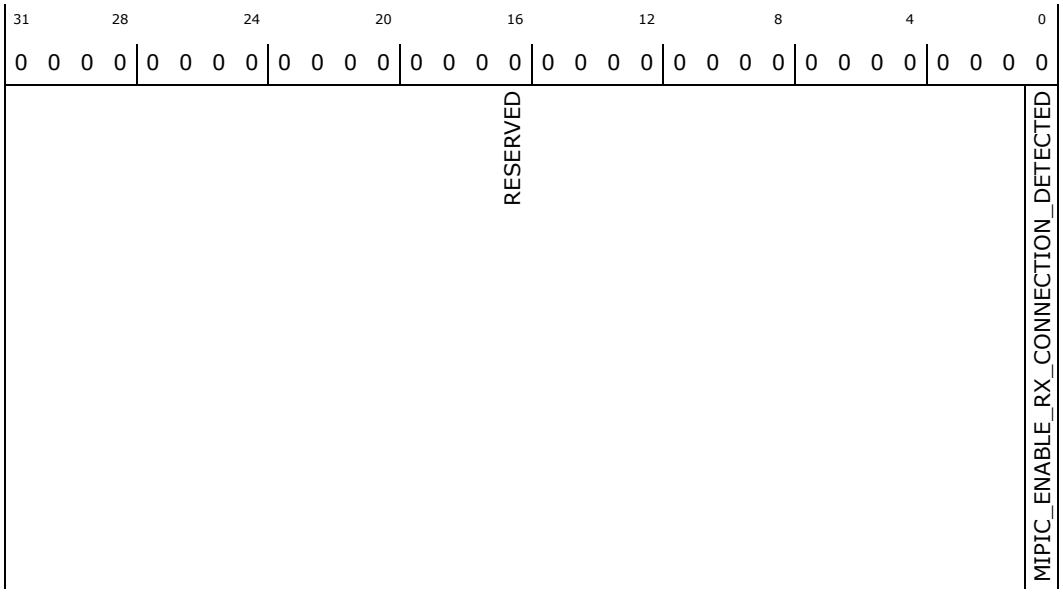
4.2.142 MIPIC_INTR_EN_REG_1—Offset B894h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B894h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RESERVED:**
0	0x0 RW	**MIPIC_ENABLE_RX_CONNECTION_DETECTED:** Set to enable the interrupt for contention detected error in the acknowledgement packet reports

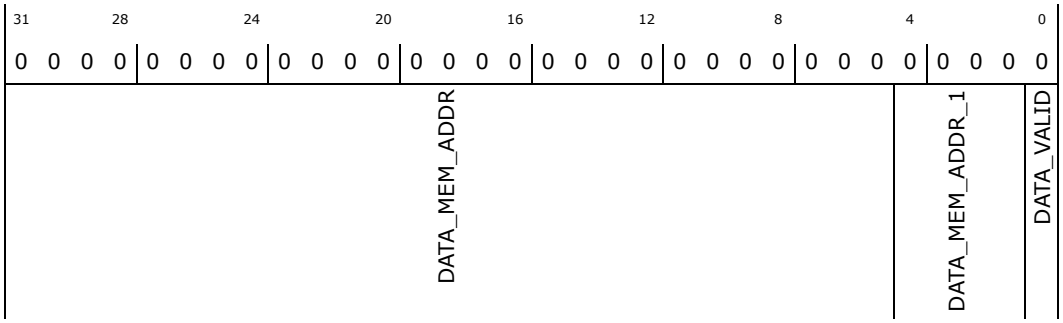
4.2.143 MIPIC_DATA_ADD—Offset B908h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B908h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RW	**DATA_MEM_ADDR:** When there is updated data for the display panel, S/W programs this register with the memory address to read from
4:1	0x0 RW	**DATA_MEM_ADDR_1:** Reserved
0	0x0 RW	**DATA_VALID:** This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

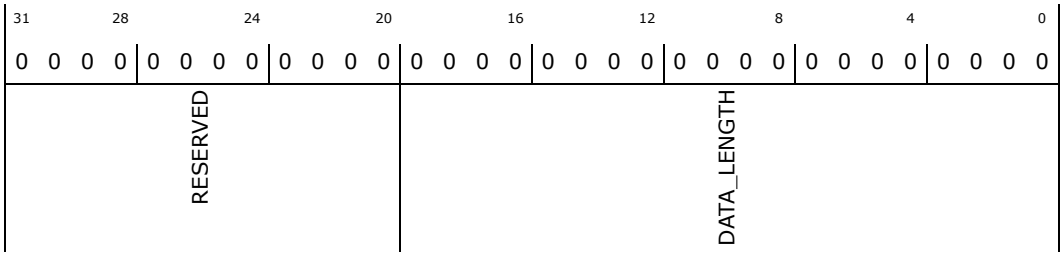
4.2.144 MIPIC_DATA_LEN—Offset B90Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B90Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RESERVED:** Reserved.
19:0	0x0 RW	**DATA_LENGTH:** This field shows the remaining length of data that needs to be read from memory, Initially set by S/W and is decremented by H/W as reads are issued

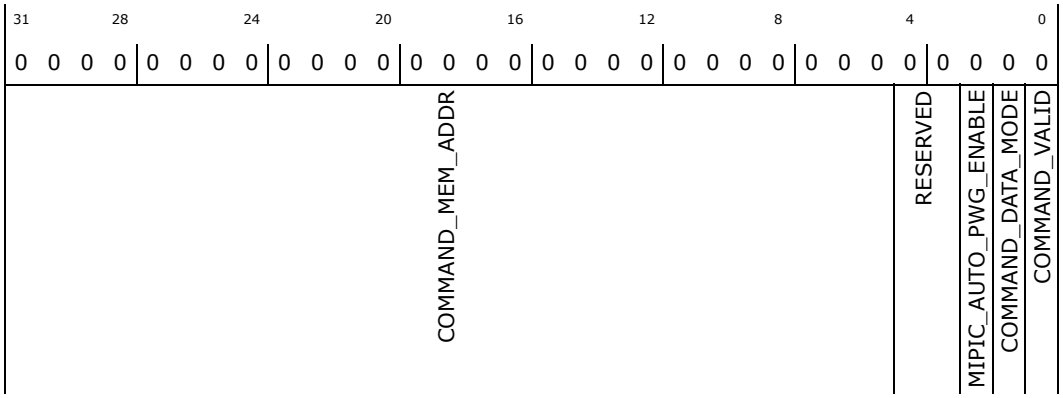
4.2.145 MIPIC_CMD_ADD—Offset B910h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B910h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RW	**COMMAND_MEM_ADDR:** When there are new commands that need to be sent to the display panel, S/W programs this register with the memory address to read the commands from
4:3	0x0 RO	**RESERVED:** MBZ
2	0x0 RW	**MIPIC_AUTO_PWG_ENABLE:** Idle state: SW driver writes to this bit to enable auto power gating for MIPIC controller 0: default 1: auto power gate is enabled
1	0x0 RW	**COMMAND_DATA_MODE:** 0: data for memory write command from system buffer that is specified by MIPI data address register 1: data for memory write command from pipe A rendering
0	0x0 RW	**COMMAND_VALID:** This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

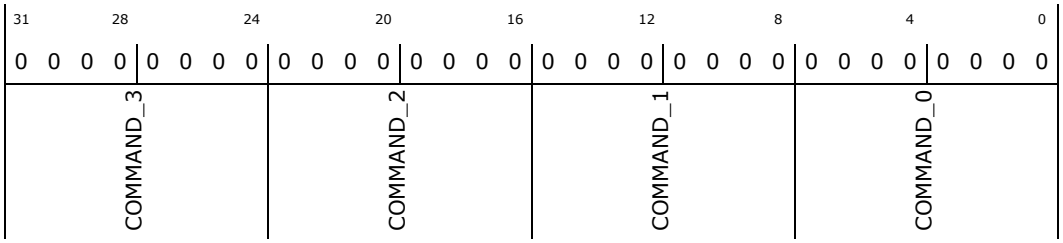
4.2.146 MIPIC_CMD_LEN—Offset B914h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B914h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**COMMAND_3:** This is command 3 length (command + parameters) in bytes
23:16	0x0 RW	**COMMAND_2:** This is command 2 length (command + parameters) in bytes
15:8	0x0 RW	**COMMAND_1:** This is command 1 length (command + parameters) in bytes
7:0	0x0 RW	**COMMAND_0:** This is command 0 length (command + parameters) in bytes

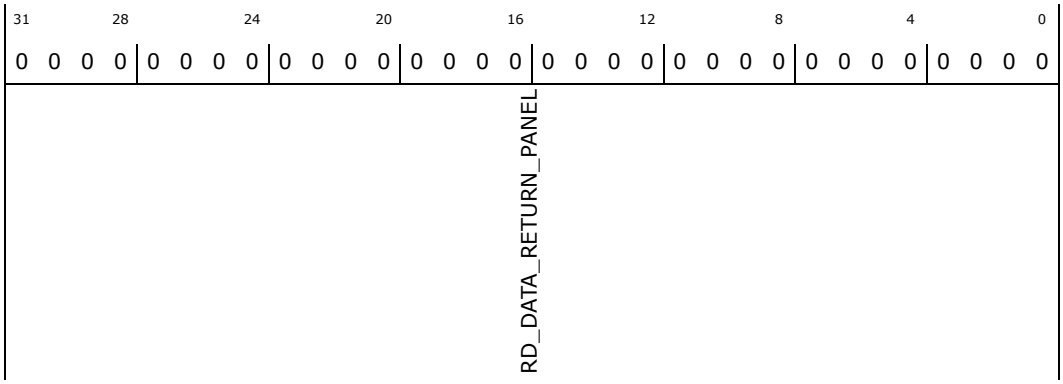
4.2.147 MIPIC_RD_DATA_RETURN0—Offset B918h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B918h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

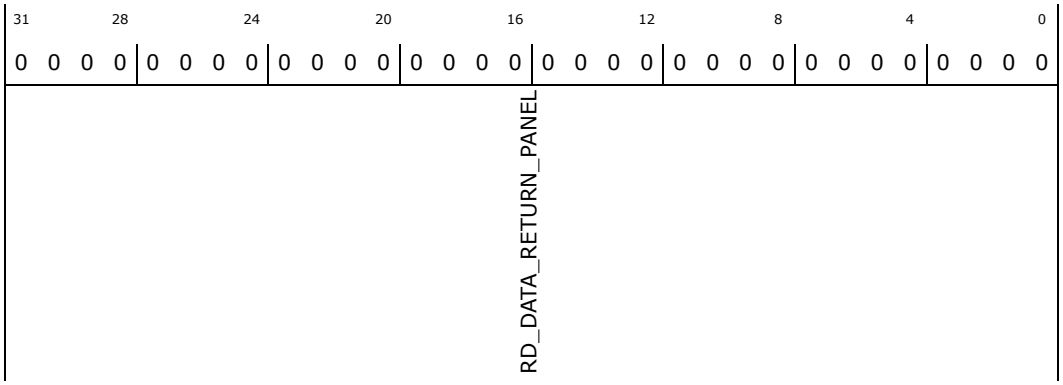
4.2.148 MIPIC_RD_DATA_RETURN1—Offset B91Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B91Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

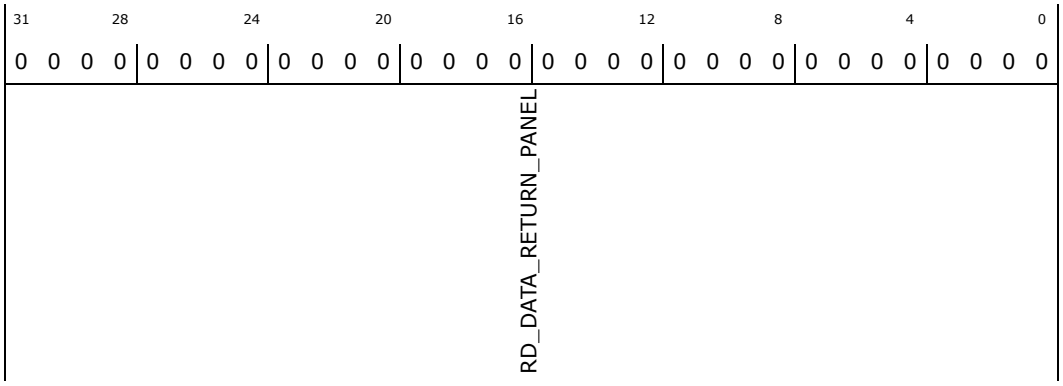
4.2.149 MIPIC_RD_DATA_RETURN2—Offset B920h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B920h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

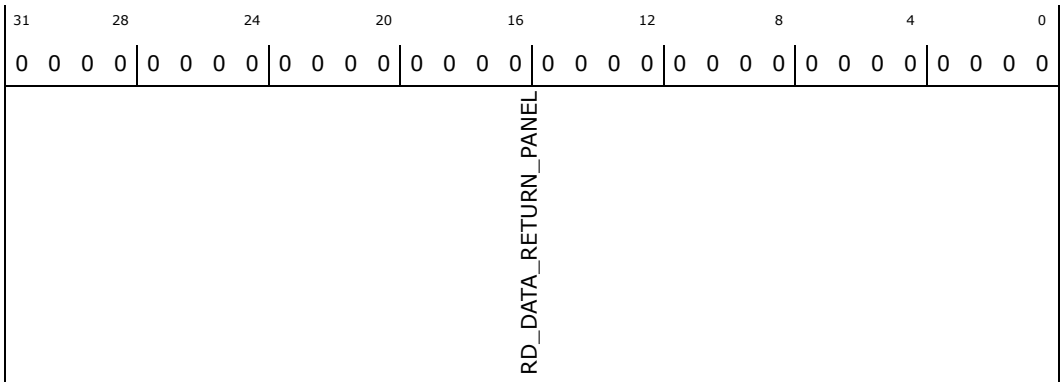
4.2.150 MIPIC_RD_DATA_RETURN3—Offset B924h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B924h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

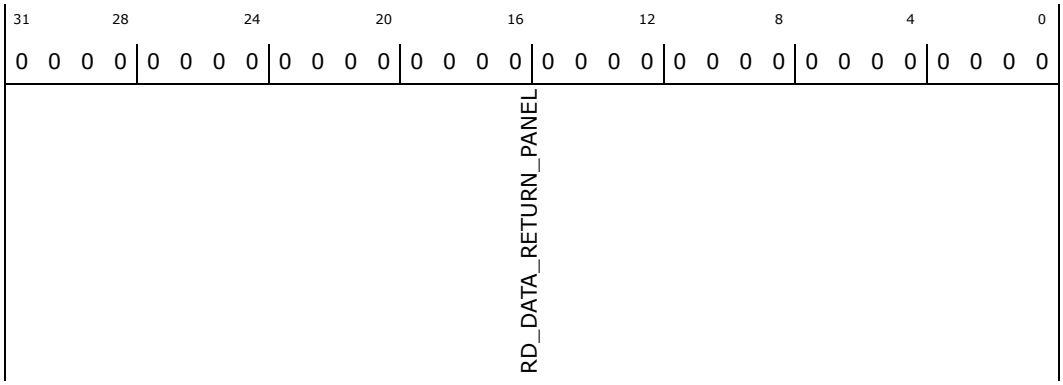
4.2.151 MIPIC_RD_DATA_RETURN4—Offset B928h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B928h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

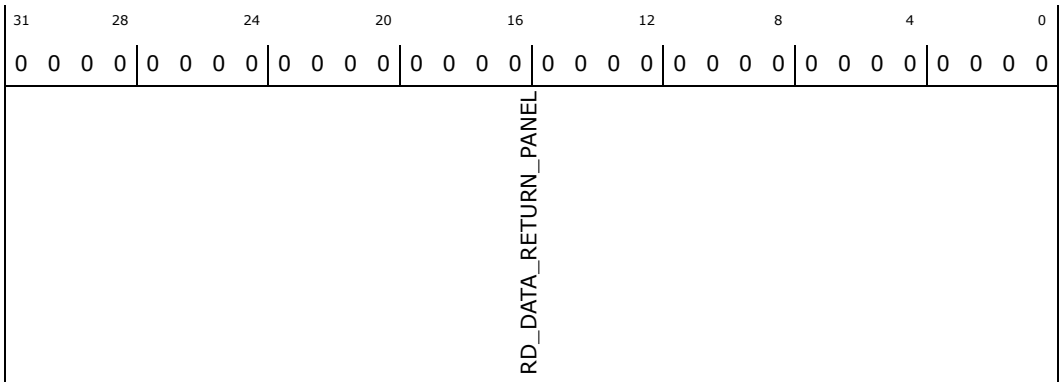
4.2.152 MIPIC_RD_DATA_RETURN5—Offset B92Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B92Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

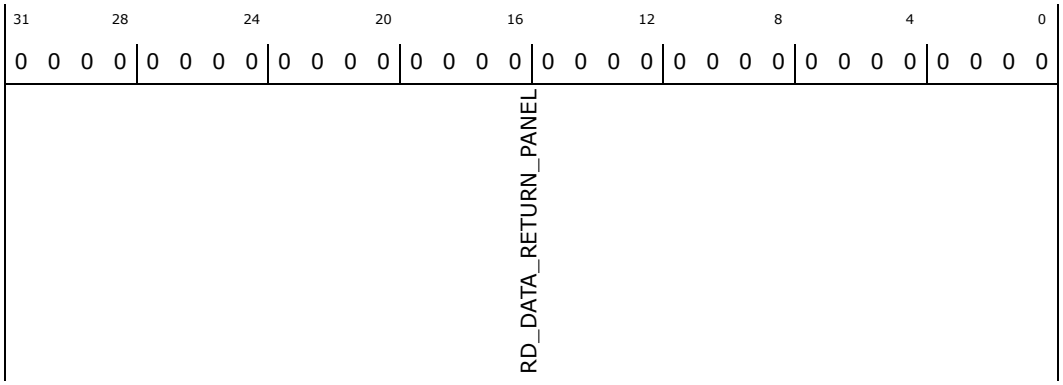
4.2.153 MIPIC_RD_DATA_RETURN6—Offset B930h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B930h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

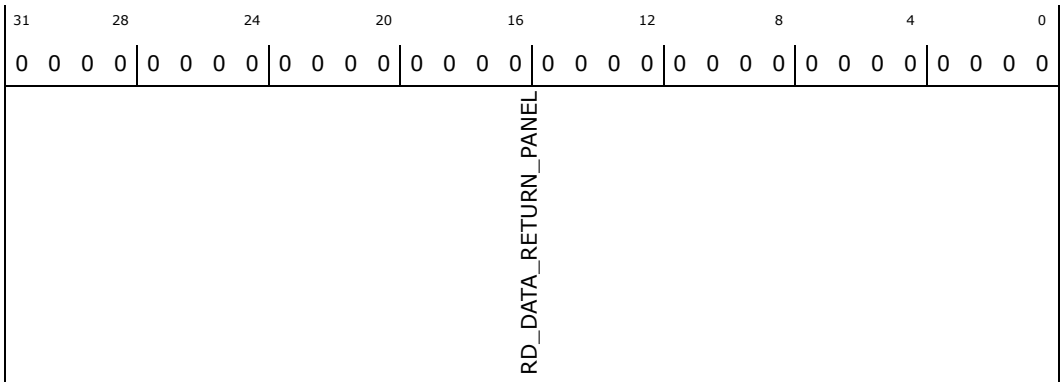
4.2.154 MIPIC_RD_DATA_RETURN7—Offset B934h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B934h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RD_DATA_RETURN_PANEL:** This is the configuration data returned from the panel

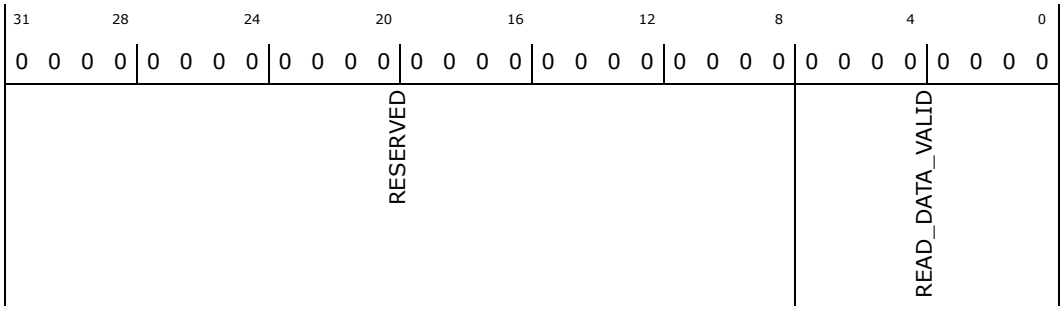
4.2.155 MIPIC_RD_DATA_VALID—Offset B938h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: B938h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED:** Reserved.
7:0	0x0 RW	**READ_DATA_VALID:** Each bit corresponds to presence of valid data in the registers above. When data is returned from the panel, H/W will write into these registers in sequence, and set the corresponding valid bit. When S/W issues a write '1 to the registers, this bit is cleared

4.2.156 DPALETTE_C—Offset C000h

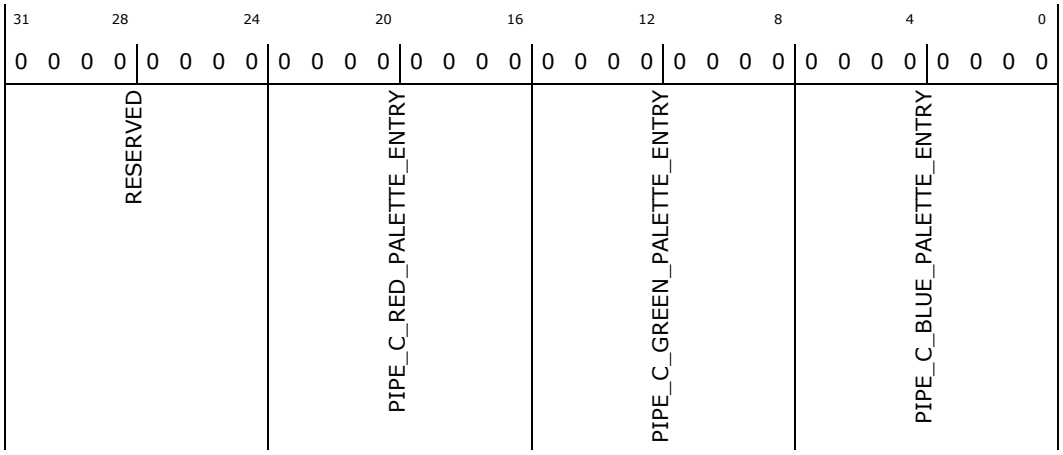
Pipe C Display Palette

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: C000h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** (read only).
23:16	0x0 RW	**PIPE_C_RED_PALETTE_ENTRY:** Reserved.
15:8	0x0 RW	**PIPE_C_GREEN_PALETTE_ENTRY:** Reserved.
7:0	0x0 RW	**PIPE_C_BLUE_PALETTE_ENTRY:** Reserved.

4.2.157 HTOTAL_A—Offset 60000h

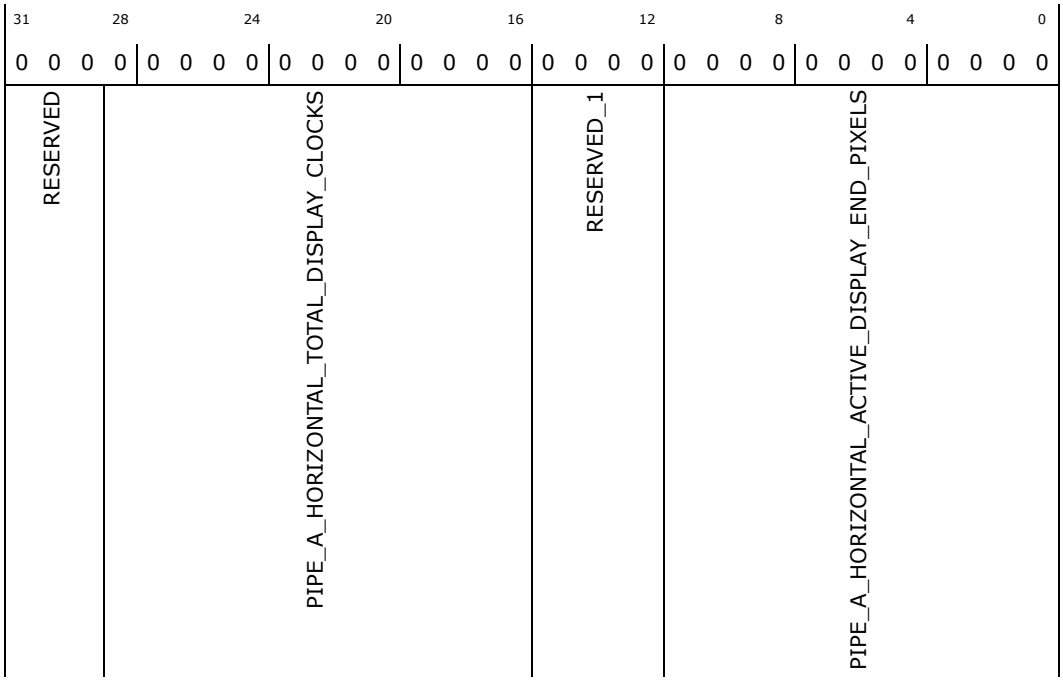
Pipe A Horizontal Total Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60000h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Write as zero.
28:16	0x0 RW	**PIPE_A_HORIZONTAL_TOTAL_DISPLAY_CLOCKS:** This 13-bit field provides Horizontal Total up to 8192 pixels encompassing the Horizontal Active Display period, front/back border and retrace period. Any pending event (HSYNC, ACTIVE, HBLANK) is reset at HTOTAL and the programmed sequence begins again. This field is programmed to the number of clocks desired minus one. This number of clocks needs to be a multiple of two when driving data out the digital port out the LVDS port in two channel mode. This value should always be equal or greater to the sum of the horizontal active and the horizontal blank, and border region sizes.
15:12	0x0 RO	**RESERVED_1:** Write as zero.
11:0	0x0 RW	**PIPE_A_HORIZONTAL_ACTIVE_DISPLAY_END_PIXELS:** This 12-bit field provides Horizontal Active Display resolutions up to 4096 pixels. Note that the first horizontal active display pixel is considered pixel number 0. The value programmed should be the (active pixels/line 1). The number of active pixels will be limited to multiples of two pixels when driving the integrated LVDS port in two channel mode.

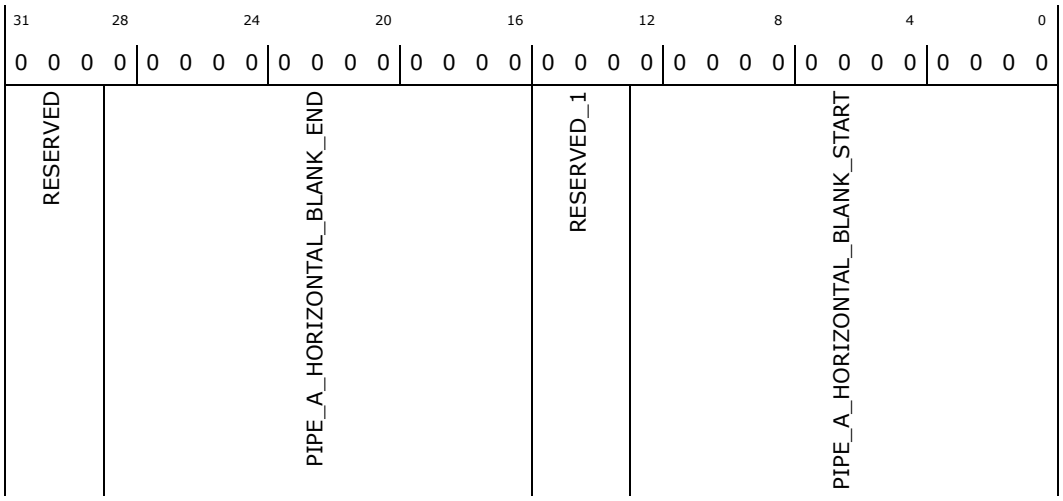
4.2.158 HBLANK_A—Offset 60004h

Pipe A Horizontal Blank Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 60004h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Read Only.
28:16	0x0 RW	**PIPE_A_HORIZONTAL_BLANK_END:** This 13-bit field specifies the position of Horizontal Blank End expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK End pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. Horizontal blank ending at the same point as the horizontal total indicates that there is no left hand border area. HBLANK size has a minimum value of 32 clocks. The number of clocks within blank needs to be a multiple of two when driving data out LVDS in two channel mode. The value loaded in the register would be equal to RightBorder+Active+HBlank-1. If this pipe is connected to the TVout port or Panel Fitter 2 the border must be zero. In that case this register is programmed to the same value as the HTOTAL register.
15:13	0x0 RO	**RESERVED_1:** Read Only.

Bit Range	Default & Access	Field Name (ID): Description
12:0	0x0 RW	**PIPE_A_HORIZONTAL_BLANK_START:** This 13-bit field specifies the Horizontal Blank Start position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK Start pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. The number of clocks for both left and right borders need to be a multiple of two when driving data out the LVDS port in two channel mode. Horizontal blank should only start after the end of the horizontal active region. The value loaded in the register would be equal to RightBorder+Active-1. If this pipe is connected to the TVout port or Panel Fitter 2 the border must be zero. In that case this register is programmed to the same value as the HACTIVE register.

4.2.159 HSYNC_A—Offset 60008h

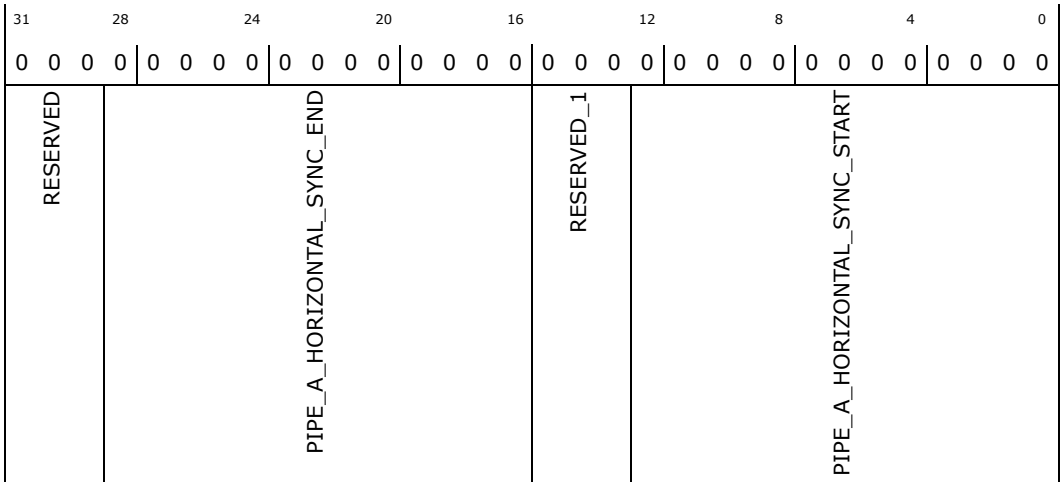
Pipe A Horizontal Sync Register

Access Method

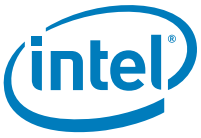
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60008h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Write as zero.



Bit Range	Default & Access	Field Name (ID): Description
28:16	0x0 RW	**PIPE_A_HORIZONTAL_SYNC_END:** This 13-bit field specifies the horizontal Sync End position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HSYNC End pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. The number of clocks in the sync period needs to be a multiple of two when driving data out the LVDS port in two channel mode. This value should be greater than the horizontal sync start position and would be loaded with the Active+RightBorder+FrontPorch+Sync-1.
15:13	0x0 RO	**RESERVED_1:** Read Only.
12:0	0x0 RW	**PIPE_A_HORIZONTAL_SYNC_START:** This 13-bit field specifies the horizontal Sync Start position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HSYNC Start pixel position, where the first active pixel is considered position 0; the second active pixel is considered position 1, etc. Note that when HSYNC Start is programmed equal to HBLANK Start, both HSYNC and HBLANK will be asserted on the same pixel clock. It should never be programmed to less than HBLANK start. The number of cycles from the beginning of the line needs to be a multiple of two when driving data out the LVDS port in two channel mode. This register should not be less than the horizontal active end. This register should be loaded with the Active+RightBorder+FrontPorch-1.

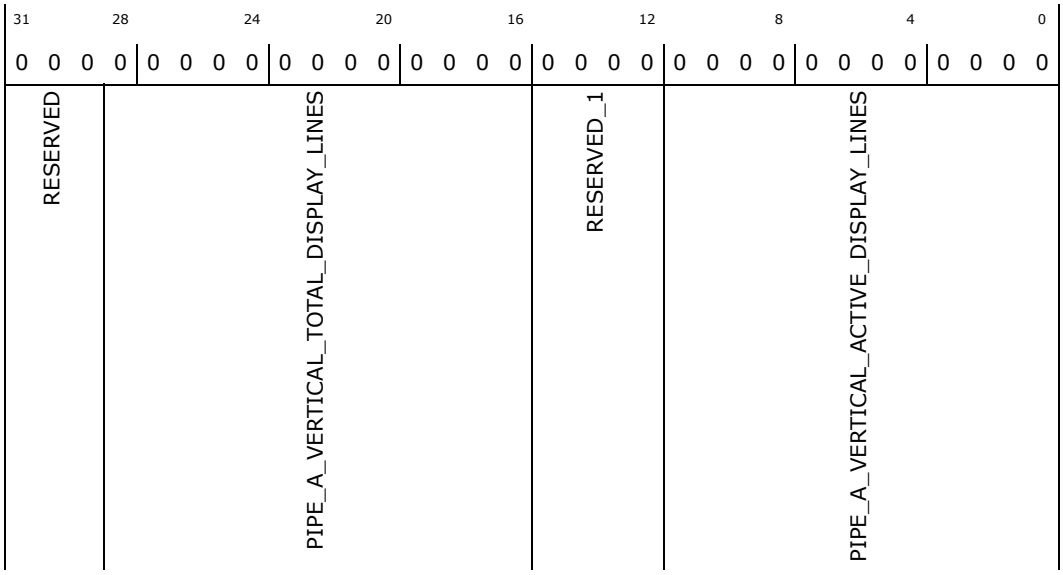
4.2.160 VTOTAL_A—Offset 6000Ch

Pipe A Vertical Total Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6000Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Read Only.
28:16	0x0 RW	**PIPE_A_VERTICAL_TOTAL_DISPLAY_LINES:** This 13 bit field provides Vertical Total up to 8192 lines encompassing the Vertical Active Display Lines, top/bottom border and retrace period. The value programmed should be the number of lines required minus one. Vertical total needs to be large enough to be greater than the sum of the vertical active, vertical border, and the vertical blank regions. The vertical counter is incremented on the leading edge of the horizontal sync. For interlaced display modes, this indicates the total number of lines in both fields. In interlaced modes, hardware automatically divides this number by 2 to get the number of lines in each field.
15:12	0x0 RO	**RESERVED_1:** Read Only.
11:0	0x0 RW	**PIPE_A_VERTICAL_ACTIVE_DISPLAY_LINES:** This 12-bit field provides vertical active display resolutions up to 4096 lines. It should be programmed with the desired number of lines minus one. When using the internal panel fitting logic, the minimum vertical active area must be three lines. For interlaced display modes, this indicates the total number of lines in both fields. In interlaced modes, hardware automatically divides this number by 2 to get the number of lines in each field.

4.2.161 VBLANK_A—Offset 60010h

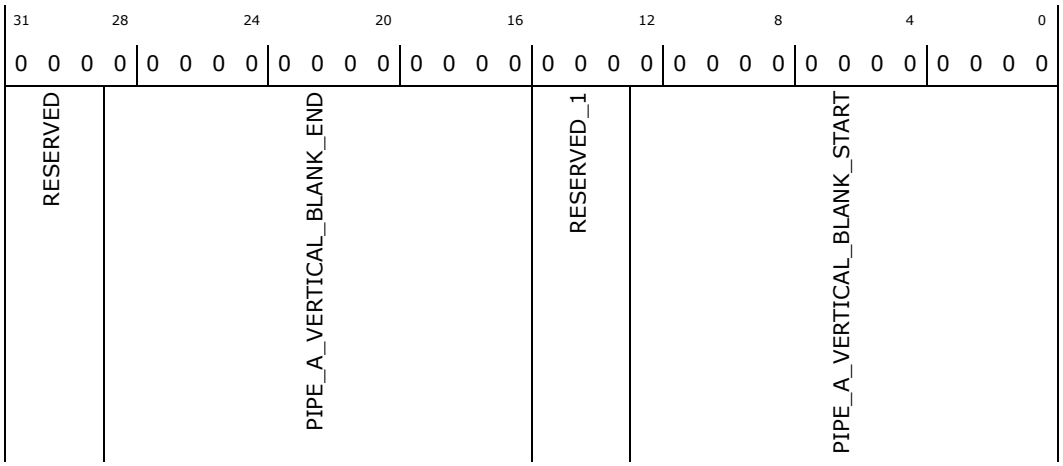
Pipe A Vertical Blank Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60010h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Read Only.
28:16	0x0 RW	**PIPE_A_VERTICAL_BLANK_END:** This 13-bit field specifies the Vertical Blank End position expressed in terms of the absolute Line number relative to the vertical active display start. The value programmed should be the VBLANK End line position, where the first active line is considered line 0, the second active line is considered line 1, etc. The end of vertical blank should be after the start of vertical blank and before or equal to the vertical total. This register should be loaded with the Vactive+BottomBorder+VBlank-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical blank end in each field. It does not count the two half lines that get added when operating in modes with half lines. If this pipe is connected to the TVout port or Panel Fitter 2 the border must be zero. In that case this register is programmed to the same value as the VTOTAL register.
15:13	0x0 RO	**RESERVED_1:** Read Only.
12:0	0x0 RW	**PIPE_A_VERTICAL_BLANK_START:** This 13-bit field specifies the Vertical Blank Start expressed in terms of the absolute line number relative to the vertical active display start. The value programmed should be the VBLANK Start line position, where the first active line is considered line 0, the second active line is considered line 1, etc. Minimum vertical blank size is required to be at least three lines. Blank should start after the end of active. This register is loaded with the Vactive+BottomBorder-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical blank start in each field. It does not count the two half lines that get added when operating in modes with half lines. If this pipe is connected to the TVout port or Panel Fitter 2 the border must be zero. In that case this register is programmed to the same value as the VACTIVE register.

4.2.162 VSYNC_A—Offset 60014h

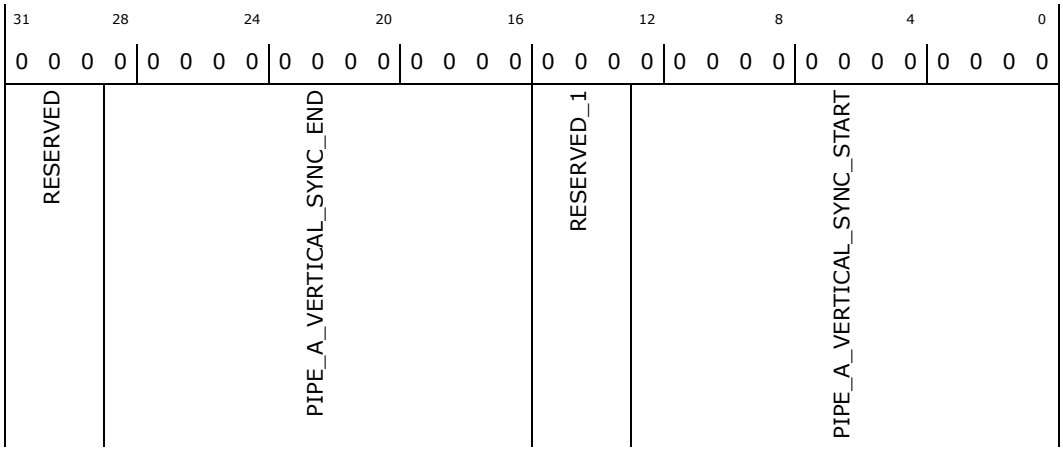
Pipe A Vertical Sync Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60014h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Read Only.
28:16	0x0 RW	**PIPE_A_VERTICAL_SYNC_END:** This 13-bit field specifies the Vertical Sync End position expressed in terms of the absolute Line number relative to the vertical active display start. The value programmed should be the VSYNC End line position, where the first active line is considered line 0, the second active line is considered line 1, etc. This register should be loaded with Vactive+BottomBorder+FrontPorch+Sync-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical sync end in each field. It does not count the two half lines that get added when operating in modes with half lines.
15:13	0x0 RO	**RESERVED_1:** Read Only.
12:0	0x0 RW	**PIPE_A_VERTICAL_SYNC_START:** This 13-bit field specifies the Vertical Sync Start position expressed in terms of the absolute line number relative to the vertical active display start. The value programmed should be the VSYNC Start line position, where the first active line is considered line 0, the second active line is considered line 1, etc. This register would be loaded with Vactive+BottomBorder+FrontPorch-1. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical sync start in each field. It does not count the two half lines that get added when operating in modes with half lines.

4.2.163 PIPESRCA—Offset 6001Ch

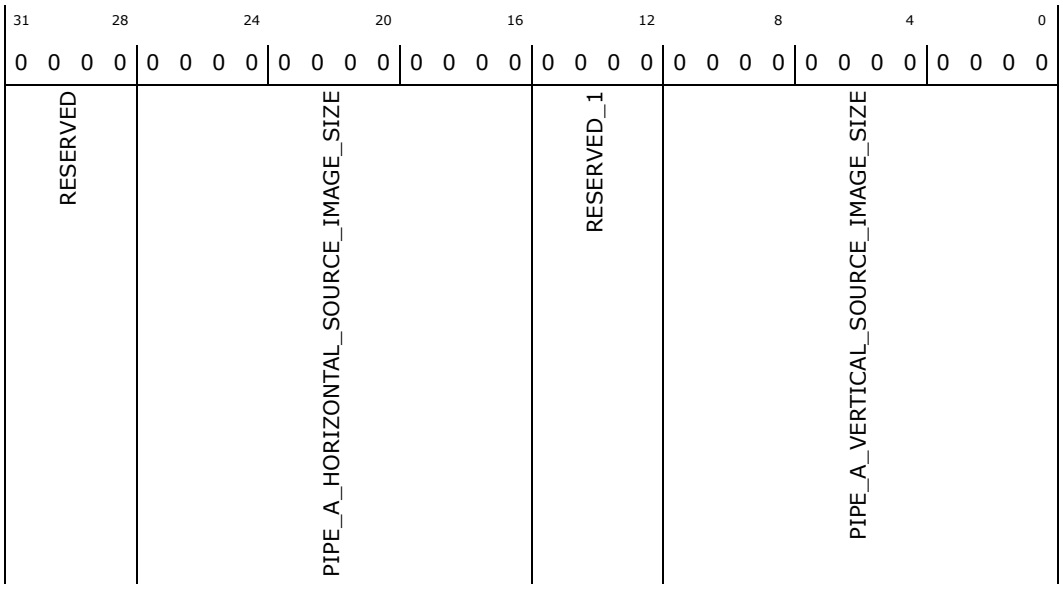
Pipe A Source Image Size

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6001Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**PIPE_A_HORIZONTAL_SOURCE_IMAGE_SIZE:** This 12-bit field specifies Horizontal source image size up to 4096. This determines the size of the image created by the display planes sent to the blender. The value programmed should be the source image size minus one. The actual source size must be two times the programmed value in the pixel multiply mode. It must represent a size that is a multiple of two (even numbers) when driving the LVDS port in two channel mode. This implies that for this mode, the value programmed will always be an odd number. Except in the case of panel fitting internal or in an external device, this register field would be programmed to a value identical to the horizontal active. This is the only register of the timing registers that is allowed to be programmed while the pipe is enabled.
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**PIPE_A_VERTICAL_SOURCE_IMAGE_SIZE:** This 12-bit field specifies the vertical source image size up to 4096 lines. This determines the size of the image created by the display planes sent to the blender. The value programmed should be the source image size minus one. Note that the actual number of lines needs to be at least twice the planes programmed value when in the pixel multiply mode. Except in the case of panel fitting internal or in an external device, this register field would be programmed to a value identical to the vertical active. For interlaced display modes, hardware automatically divides this number by 2 to get the vertical source image size in each field.

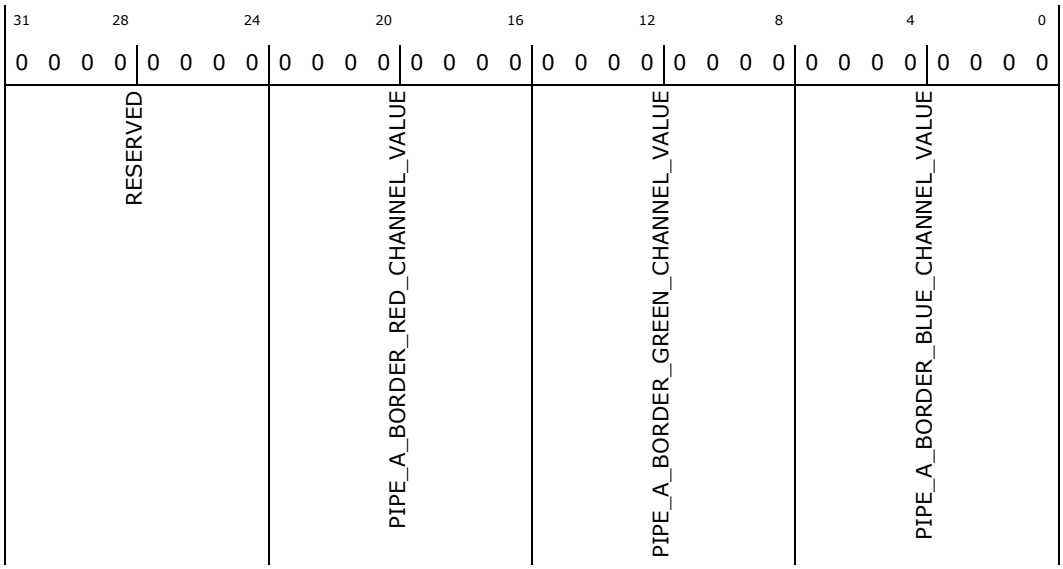
4.2.164 BCLRPAT_A—Offset 60020h

Pipe A Border Color Pattern Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 60020h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:16	0x0 RW	**PIPE_A_BORDER_RED_CHANNEL_VALUE:** Reserved.
15:8	0x0 RW	**PIPE_A_BORDER_GREEN_CHANNEL_VALUE:** Reserved.
7:0	0x0 RW	**PIPE_A_BORDER_BLUE_CHANNEL_VALUE:** Reserved.

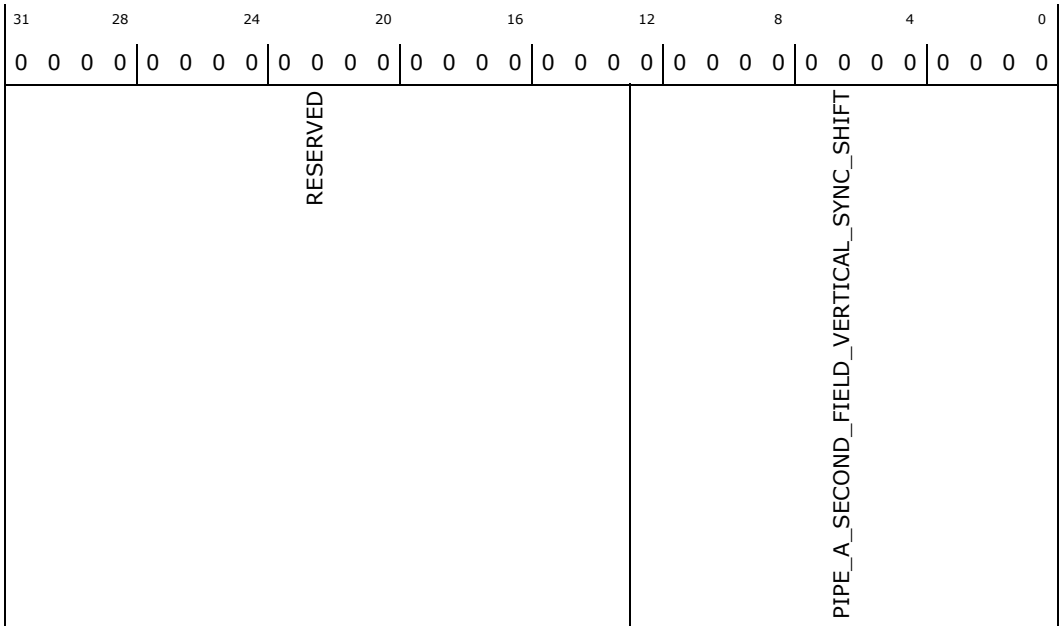
4.2.165 VSYNCSHIFT_A—Offset 60028h

Vertical Sync Shift Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 60028h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RESERVED:** Write as zero.
12:0	0x0 RW	**PIPE_A_SECOND_FIELD_VERTICAL_SYNC_SHIFT:** This value specifies the vertical sync alignment for the start of the interlaced second field expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the PIPEACONF is programmed to an interlaced mode using vsync shift. Otherwise a legacy value of floor[htotal / 2] will be used. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed to: (horizontal sync start - floor[horizontal total / 2]) (use the actual horizontal sync start and horizontal total values and not the minus one values programmed into registers). This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.

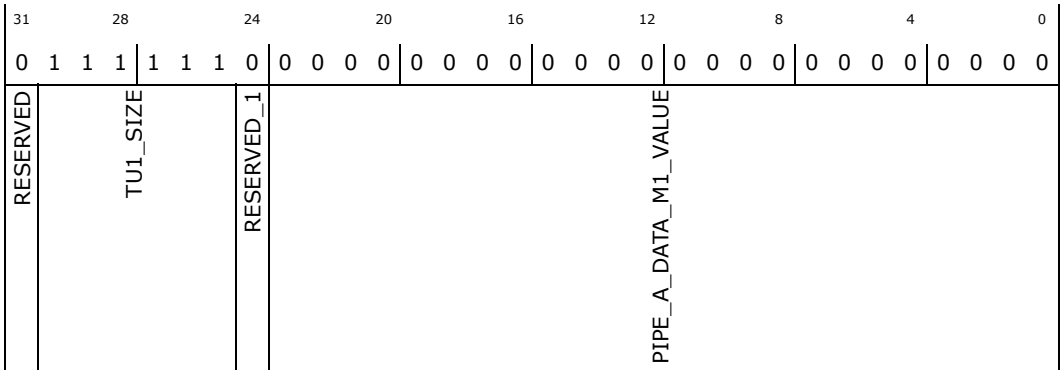
4.2.166 TRANSADATAM1—Offset 60030h

Pipe A Data M value 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 60030h

Default: 7E000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** Project: All Format: MBZ
30:25	0x3f RW	**TU1_SIZE:** Project: All This field is the size of the transfer unit for DP, minus one.
24	0x0 RO	**RESERVED_1:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_A_DATA_M1_VALUE:** Project: All This field is the M1 value for internal use of the DDA.

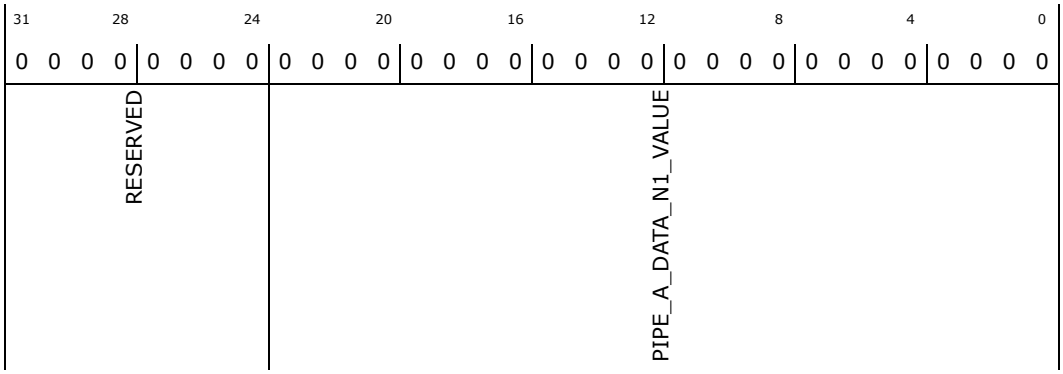
4.2.167 TRANSADATAN1—Offset 60034h

Pipe A Data N value 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 60034h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ

Bit Range	Default & Access	Field Name (ID): Description
23:0	0x0 RW	**PIPE_A_DATA_N1_VALUE:** Project: All This field is the N1 value for internal use of the DDA.

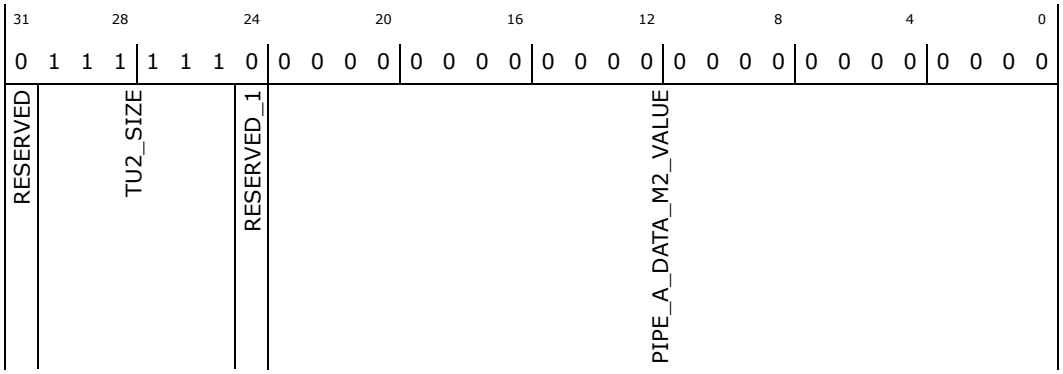
4.2.168 TRANSADATAM2—Offset 60038h

Pipe A Data M value 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 60038h

Default: 7E000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** Project: All Format: MBZ
30:25	0x3f RW	**TU2_SIZE:** Project: All Default Value: ;111111b 64 This field is the size of the transfer unit for DP, minus one.
24	0x0 RO	**RESERVED_1:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_A_DATA_M2_VALUE:** Project: All This field is the M2 value for internal use of the DDA.

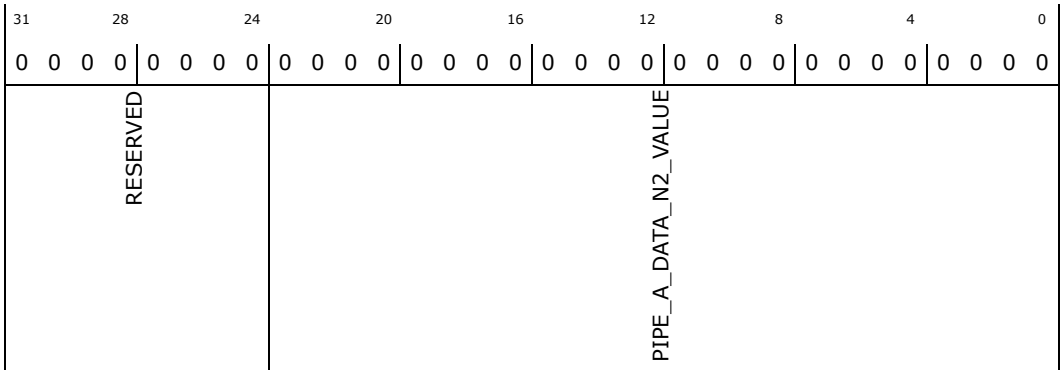
4.2.169 TRANSADATAN2—Offset 6003Ch

Pipe A Data N value 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6003Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_A_DATA_N2_VALUE:** Project: All This field is the N2 value for internal use of the DDA.

4.2.170 TRANSADPLINKM1—Offset 60040h

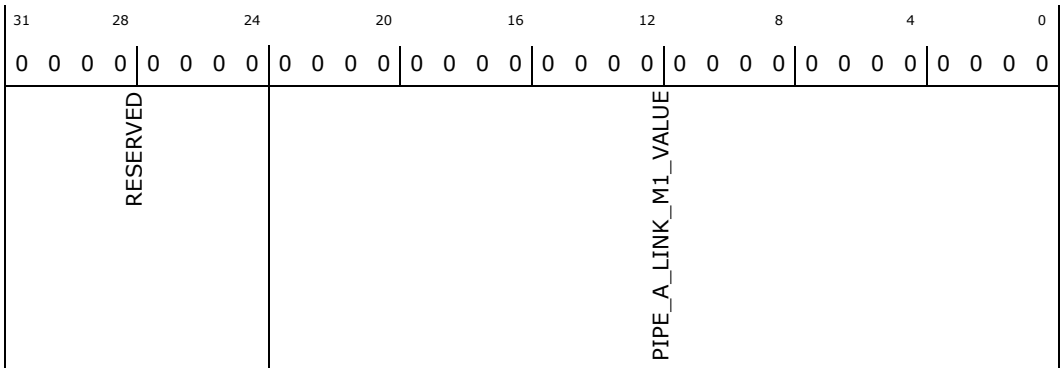
Pipe A Link M value 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60040h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_A_LINK_M1_VALUE:** Project: All This field is the M1 value for external transmission in the Main Stream Attributes.

4.2.171 TRANSADPLINKN1—Offset 60044h

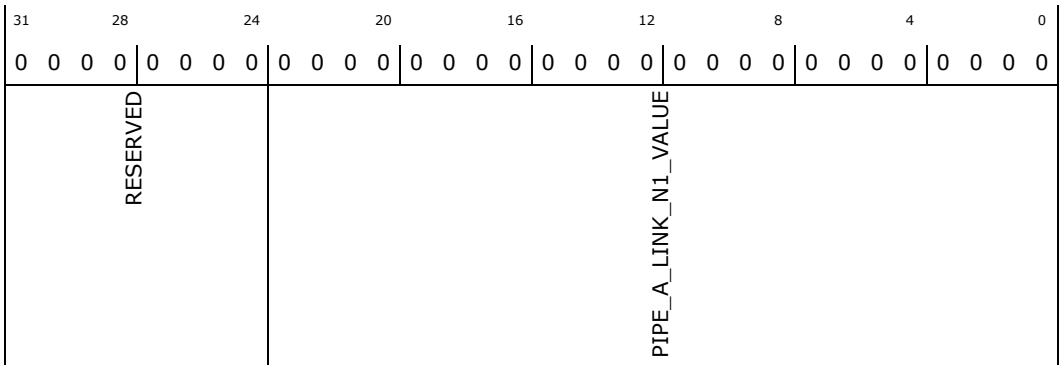
Pipe A Link N value 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60044h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_A_LINK_N1_VALUE:** Project: All This field is the N1 value for external transmission in the Main Stream Attributes and VB-ID.

4.2.172 TRANSADPLINKM2—Offset 60048h

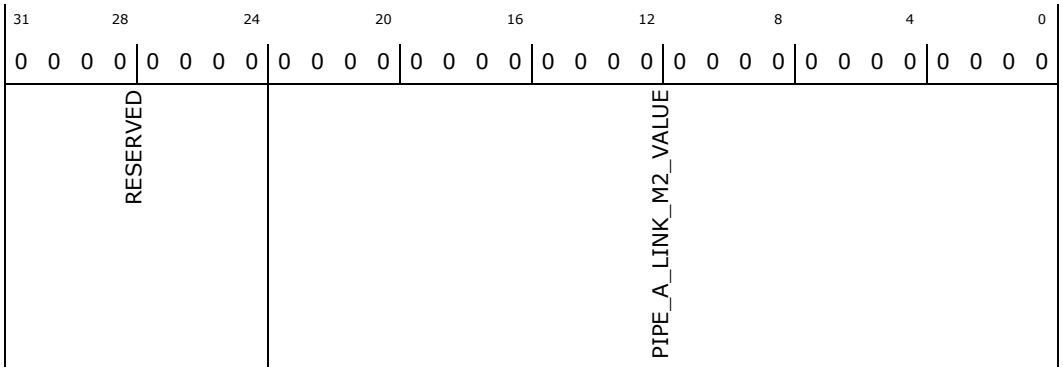
Pipe A Link M value 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60048h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_A_LINK_M2_VALUE:** Project: All This field is the M2 value for external transmission in the Main Stream Attributes.

4.2.173 TRANSADPLINKN2—Offset 6004Ch

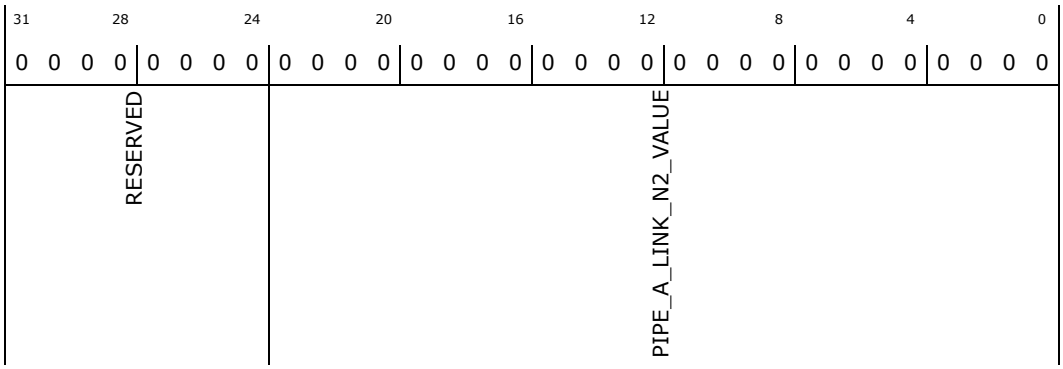
Pipe A Link N value 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6004Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_A_LINK_N2_VALUE:** Project: All This field is the N2 value for external transmission in the Main Stream Attributes and VB-ID.

4.2.174 CRCCTRLREDA—Offset 60050h

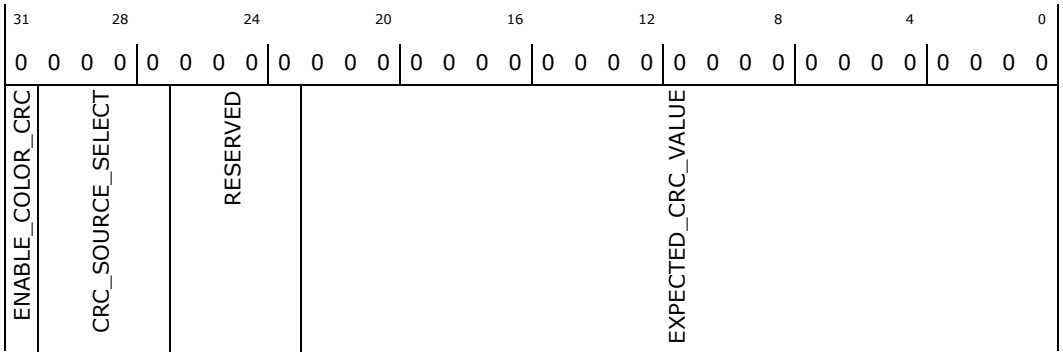
Pipe A CRC Color Channel Control Register (Red)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60050h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**ENABLE_COLOR_CRC:** Enables the CRC calculations. After being enabled for the first time, you need to wait for two VBLANK events for a valid CRC result. After that, a CRC will be generated each frame. 0 = CRC Calculations are disabled 1 = CRC Calculations are enabled
30:27	0x0 RW	**CRC_SOURCE_SELECT:** These bits select the source of the data to put into the CRC logic. 0000: Pipe A (Not available when DisplayPort or TV is enabled on this pipe) 0001: sDVOB/HDMIB (30 bit format. Only select when HDMIB is set to pipeA) 0010: sDVOC/HDMIC (30 bit format. Only select when HDMIC is set to pipeA) 0011: DisplayPort D (40 bit format) [DevCTG] 0100: TV Encoder outputs (30 bit format) 0101: TV filter outputs (30 bit format) 0110: DisplayPort B (40 bit format) 0111: DisplayPort C (40 bit format) 1000: Audio DP (Audio for DisplayPort (pcdclk). Only select when Audio is on DisplayPort on Pipe A) 1001: Audio HDMI (Audio for HDMI (dotclock) Only select when Audio is on HDMI on Pipe A) Others: Reserved
26:23	0x0 RO	**RESERVED:** Write as zero
22:0	0x0 RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

4.2.175 CRCCTRLGREENA—Offset 60054h

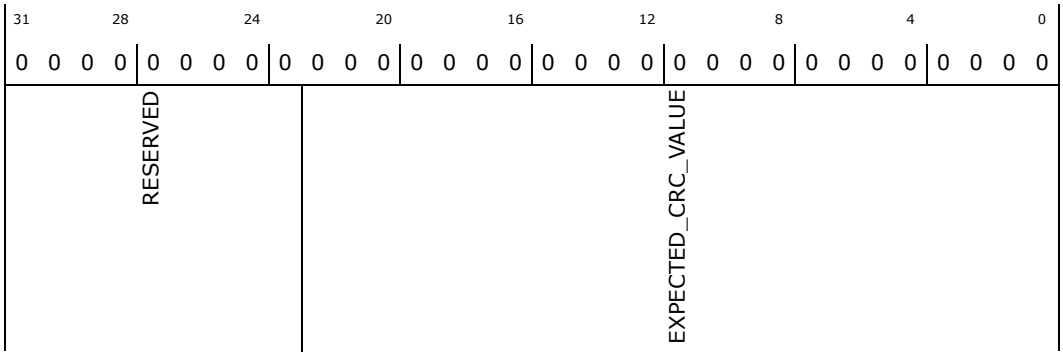
Pipe A CRC Color Channel Control Register (, Residual)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60054h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Write as zero
22:0	0x0 RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

4.2.176 CRCCTRLBLUEA—Offset 60058h

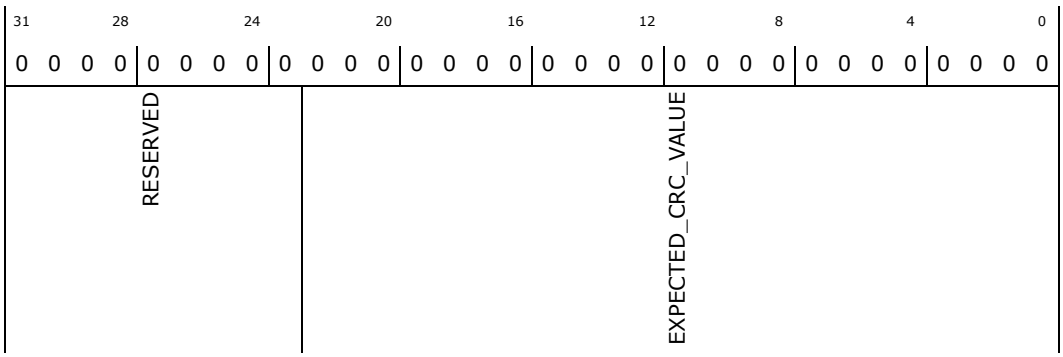
Pipe A CRC Color Channel Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60058h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
22:0	0x0 RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

4.2.177 CRCCTRLALPHAA—Offset 6005Ch

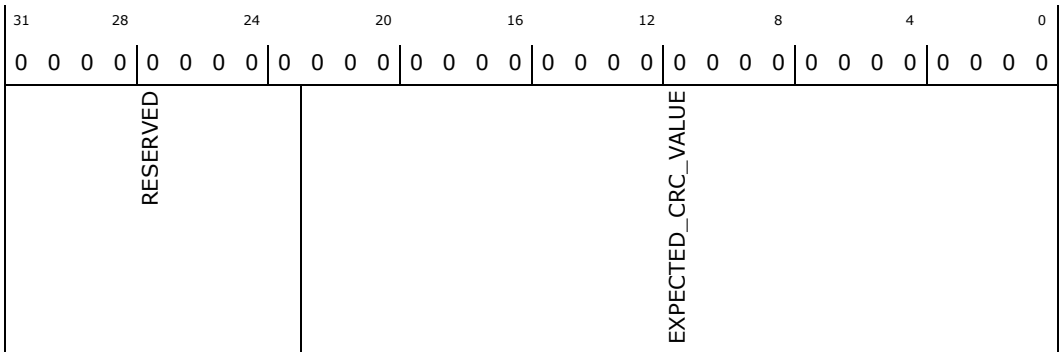
Pipe A CRC Color Channel Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6005Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Write as zero
22:0	0x0 RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

4.2.178 CRCRESREDA—Offset 60060h

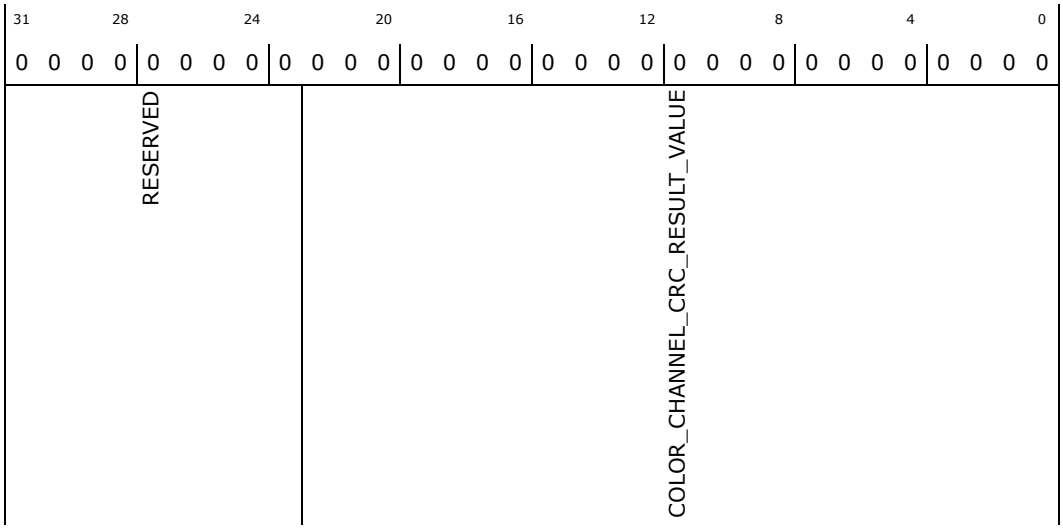
Pipe A A CRC Color Channel Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60060h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Read only
22:0	0x0 RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

4.2.179 CRCRESGREENA—Offset 60064h

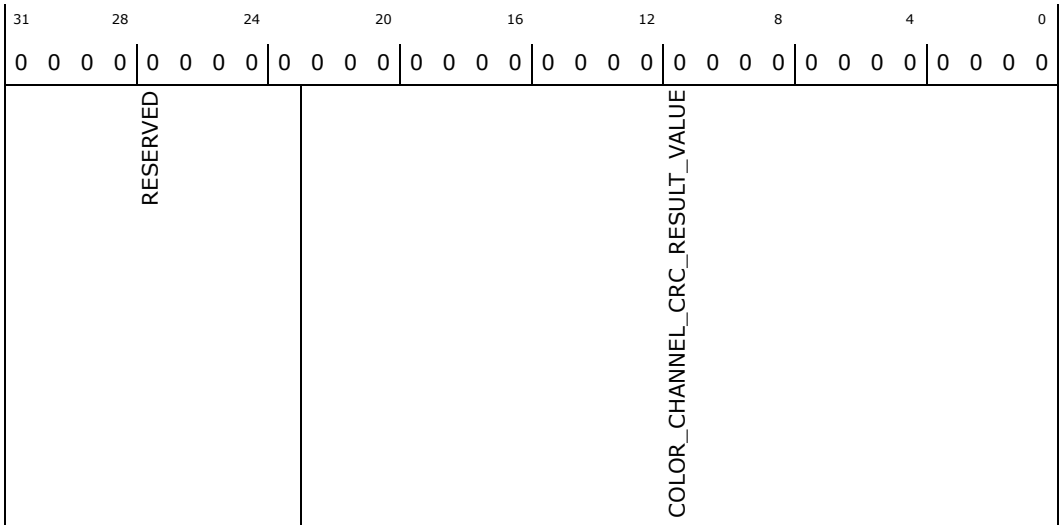
Pipe A A CRC Color Channel Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60064h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Read only
22:0	0x0 RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

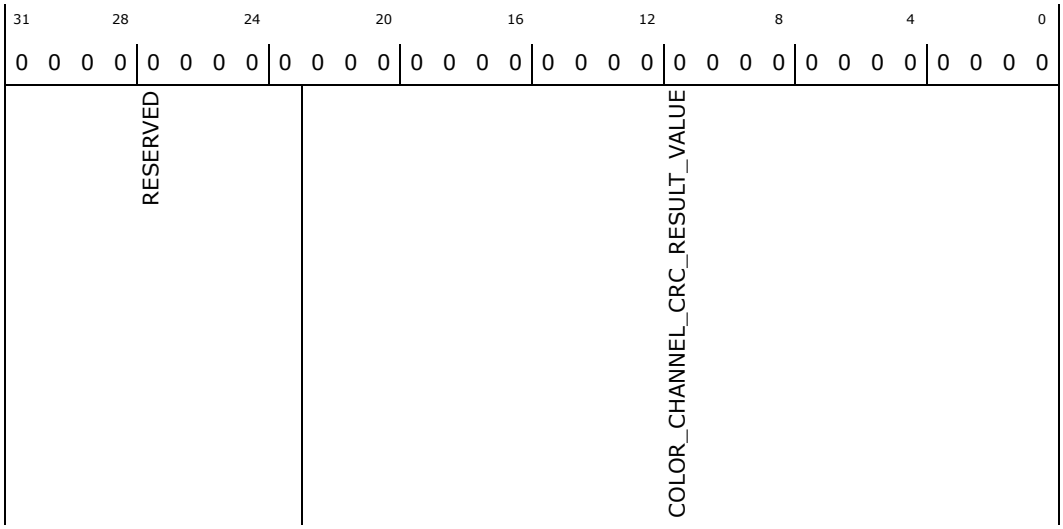
4.2.180 CRCRESBLUEA—Offset 60068h

Pipe A A CRC Color Channel Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 60068h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Read only
22:0	0x0 RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

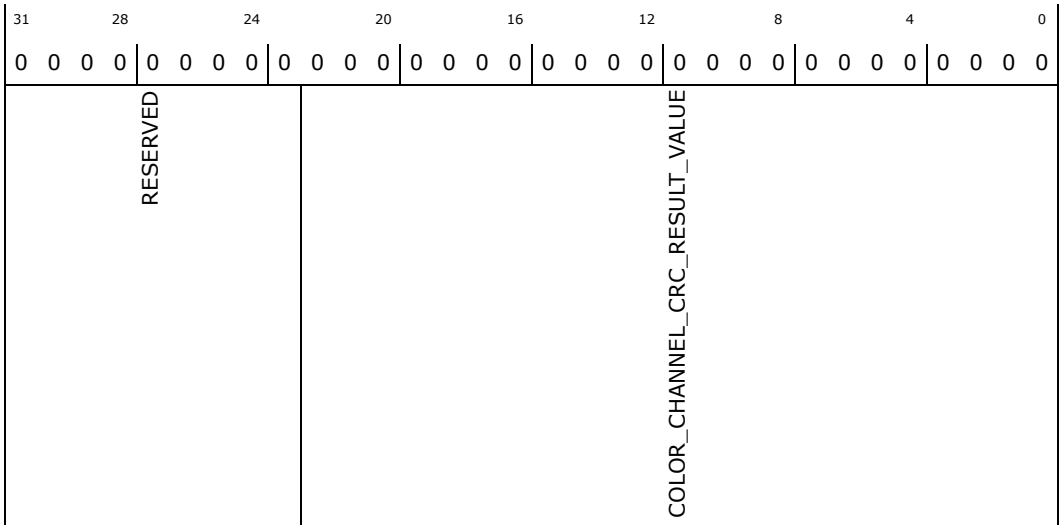
4.2.181 CRCRESALPHAA—Offset 6006Ch

Pipe A A CRC Color Channel Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6006Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Read only
22:0	0x0 RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

4.2.182 CRCCTRLRESIDUE2A—Offset 60070h

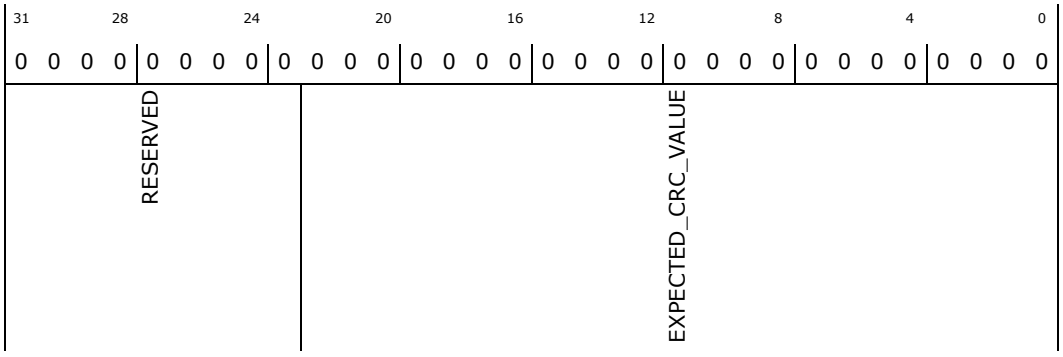
Pipe A CRC Color Channel Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60070h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Write as zero
22:0	0x0 RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

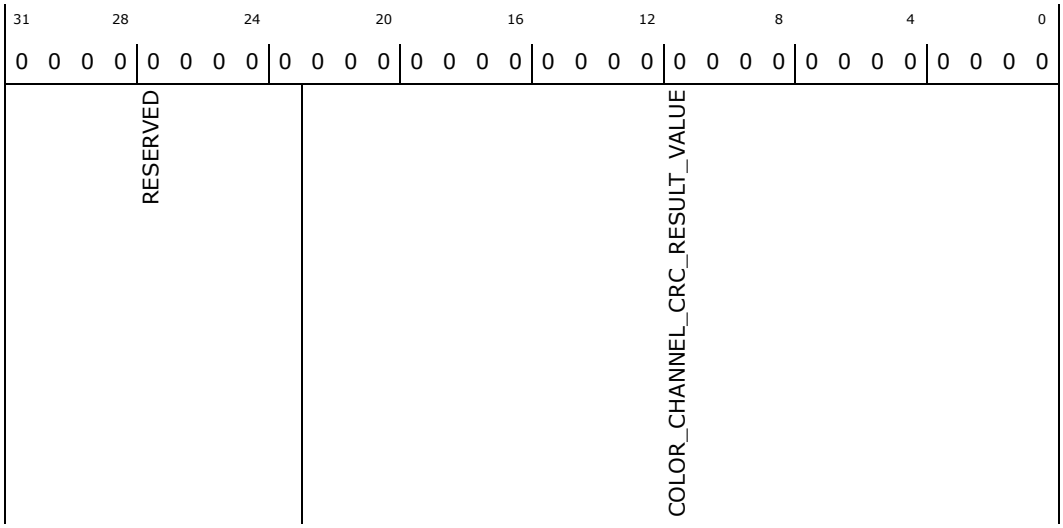
4.2.183 CRCRESRESIDUE2A—Offset 60080h

Pipe A CRC Color Channel Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 60080h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Read only
22:0	0x0 RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

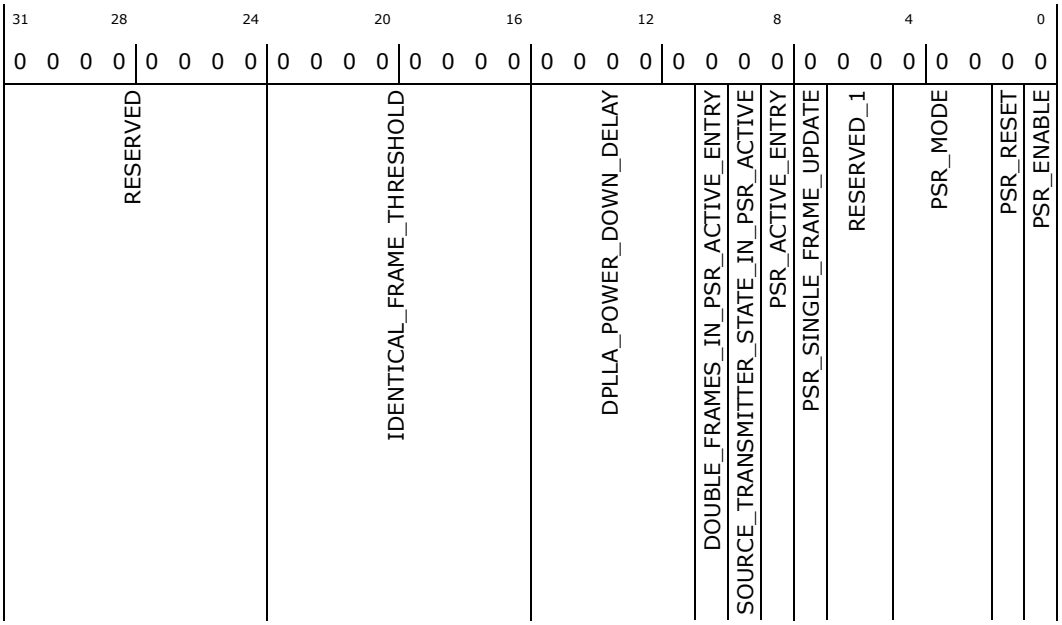
4.2.184 PSRCTLA—Offset 60090h

Pipe A Panel Self Refresh Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 60090h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:16	0x0 RW	**IDENTICAL_FRAME_THRESHOLD:** : Number of identical frames that display controller needs to exceed in order to transition to PSR active state in HW timer mode
15:11	0x0 RW	**DPLLA_POWER_DOWN_DELAY:** programmable delay from main link powerdown to DPLLA powerdown. The delay is in number of cdclk clocks.
10	0x0 RW	**DOUBLE_FRAMES_IN_PSR_ACTIVE_ENTRY:** . If asserted, HW will send two frames with same SDP active setting when entry PSR active state. This bit is set if the vertical blanking time is less than 330us.
9	0x0 RW	**SOURCE_TRANSMITTER_STATE_IN_PSR_ACTIVE:** . If asserted, HW will keep transmitter active during PSR active state and sends only idle symbols. If deasserted, HW will turn off transmitter during PSR active state. Display driver will keep this bit consistent with Source transmitter state in PSR active bit in DPCD register of the sink.
8	0x0 RW	**PSR_ACTIVE_ENTRY:** This bit is only valid in PSR_mode is SW timer mode. If it is asserted, HW will transition into PSR_active state. If it is deasserted, HW will transition to PSR_inactive state. SW should not set or clear this bit more than once within one vblank period.
7	0x0 RW	**PSR_SINGLE_FRAME_UPDATE:** In PSR persistent mode, SW set this bit before writing registers for a flip. It will be self-clear when it gets to the PSR active state.

Bit Range	Default & Access	Field Name (ID): Description
6:5	0x0 RO	**RESERVED_1:** Reserved.
4:2	0x0 RW	**PSR_MODE:** b011-111: reserved. b010: PSR with HW timer. HW timer decides PSR active entry point. PSR active state exits upon MMIO write registers that may change the frame buffer. b001: PSR with SW timer. In this mode, SW will keep track of idle frames and buffer modification in the driver and explicitly specify the entry and exit PSR active state point. b000: PSR manual (debug) mode. All of PSR state transitions and SDP content is managed by SW driver. SW is responsible to change SDP content for every frame with appropriate values to keep PSR panel in synchronized states.
1	0x0 RW	**PSR_RESET:** If assert all PSR functions are reset back to PSR inactive state. When it needs to resynchronize source and sync, SW writes 0x2 to DPCD register 600h and to this bit to get system back to PSR active states. This bit is self clear.
0	0x0 RW	**PSR_ENABLE:** Panel Self-refresh is enabled. When it is asserted PSR is enabled and operate in one of the mode that specified by PSR mode.

4.2.185 PSRSTATA—Offset 60094h

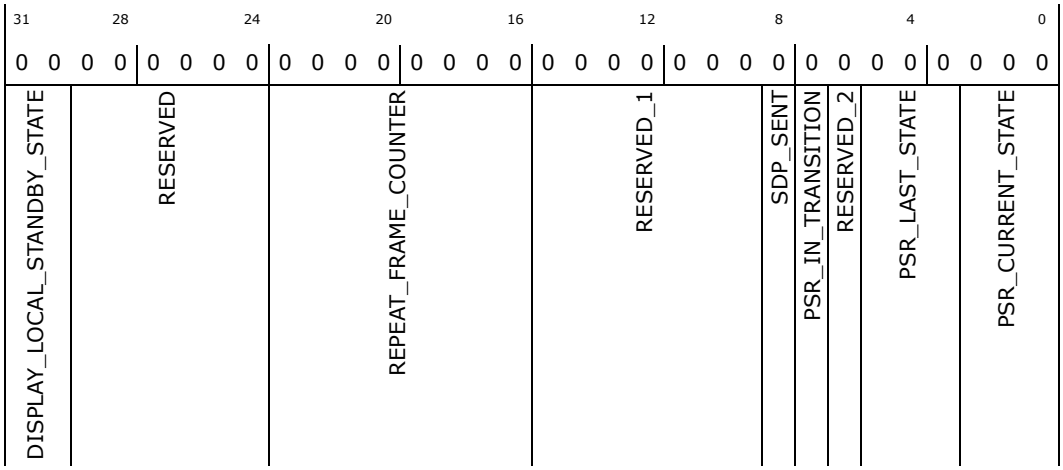
Pipe A PSR status register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60094h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**DISPLAY_LOCAL_STANDBY_STATE:** :00: D0 idle state, fetch frame buffer from system memory 02: D0i2 PSR is active, display controller is trunk gated 03: D0i3 PSR is active, display controller is power gated
29:24	0x0 RO	**RESERVED:** Reserved.
23:16	0x0 RO	**REPEAT_FRAME_COUNTER:** : Number of identical frames has been sent by display controller. Value is not roll over at 255.
15:9	0x0 RO	**RESERVED_1:** Reserved.
8	0x0 RO	**SDP_SENT:** it indicates if SDP packet has been sent in current frame.
7	0x0 RO	**PSR_IN_TRANSITION:** There is a period that source already committed to PSR active but sink did not. SW should not change the source state at this time but wait until this status bit is clear. The wait time should in the range of 120-250us in the worst case.
6	0x0 RO	**RESERVED_2:** Reserved.
5:3	0x0 RO	**PSR_LAST_STATE:** indicate last source state that PSR state machine were in (debug) 000: PSR_disabled 001: PSR_inactive 010: PSR_transition_to_active 011: PSR_active no RFB update 100: PSR_active single frame update 101: PSR_exit
2:0	0x0 RO	**PSR_CURRENT_STATE:** indicate current source state that PSR state machine are in 000: PSR_disabled 001: PSR_inactive 010: PSR_transition_to_active 011: PSR_active no RFB update 100: PSR_active single frame update 101: PSR_exit

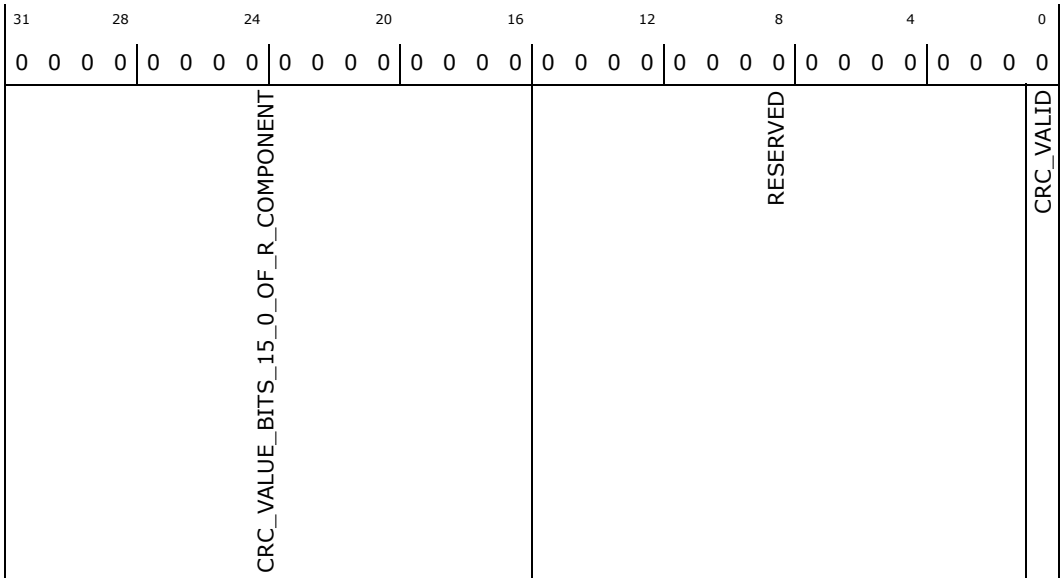
4.2.186 PSRCRC1A—Offset 60098h

Pipe A PSR CRC1 register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 60098h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**CRC_VALUE_BITS_15_0_OF_R_COMPONENT:** Reserved.
15:1	0x0 RO	**RESERVED:** .
0	0x0 RO	**CRC_VALID:** CRC calculation complete and valid for previous frame.

4.2.187 PSRCRC2A—Offset 6009Ch

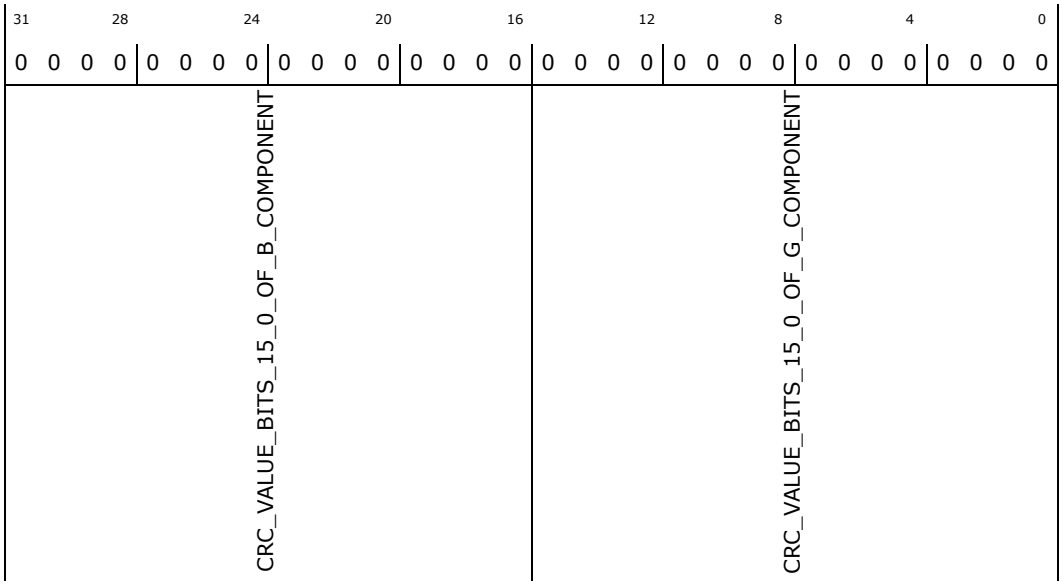
Pipe A PSR CRC2 register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6009Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**CRC_VALUE_BITS_15_0_OF_B_COMPONENT:** Reserved.
15:0	0x0 RO	**CRC_VALUE_BITS_15_0_OF_G_COMPONENT:** Reserved.

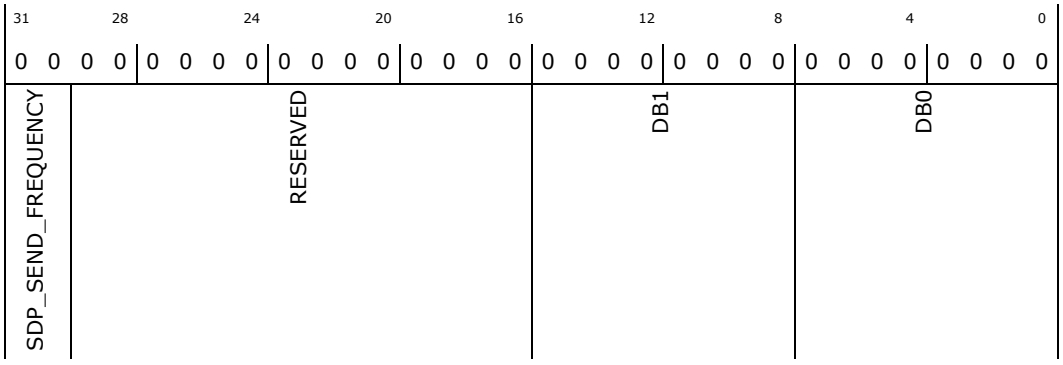
4.2.188 VSCSDPA—Offset 600A0h

Pipe A VSC SDP register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 600A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**SDP_SEND_FREQUENCY:** 00: off, not sending 01: send one every frame 10: send once 11: reserved When PSR is enabling this field is ignored. One SDP is sent in every frame until source is in PSR active state
29:16	0x0 RO	**RESERVED:** Reserved.
15:8	0x0 RW	**DB1:** : Programmed by display driver in manual mode, auto-generate by display controller in all other modes
7:0	0x0 RW	**DB0:** : Bits 7:4: Stereo Interface Method Specific ParameterBits 3:0: Stereo Interface Method Code. This field is programmed by display driver for stereo display configuration

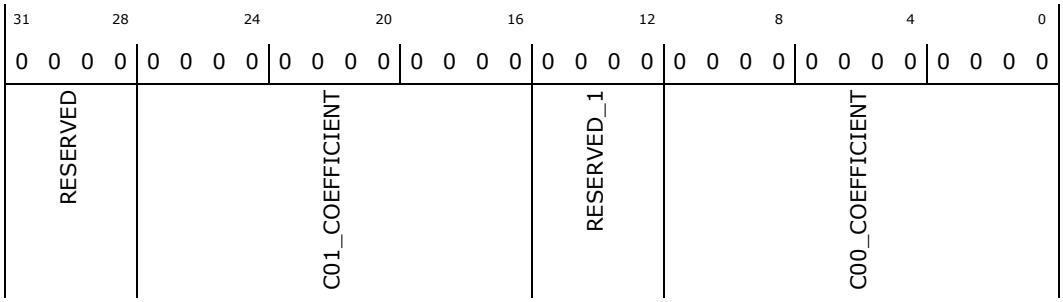
4.2.189 PIPEAWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS—Offset 600B0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 600B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Reserved.
27:16	0x0 RW	**C01_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
15:12	0x0 RO	**RESERVED_1:** Reserved.
11:0	0x0 RW	**C00_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

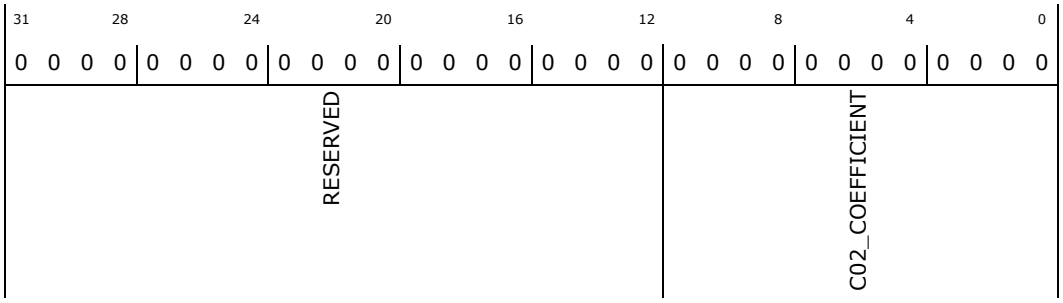
4.2.190 PIPEAWIDEGAMUTCOLORCORRECTIONC02COEFFICIENT—Offset 600B4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 600B4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RESERVED:** Reserved.
11:0	0x0 RW	**C02_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

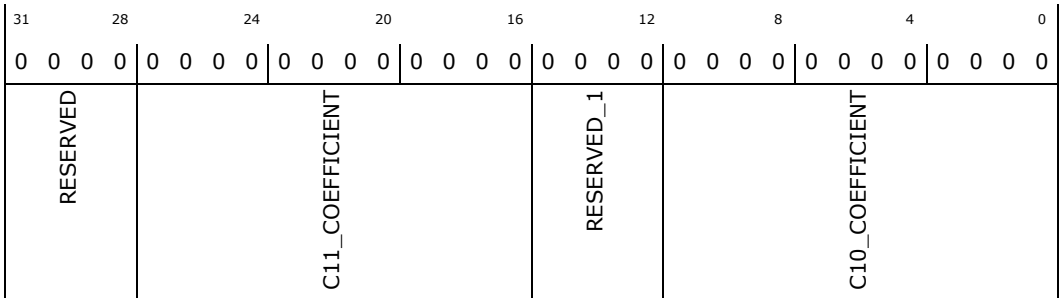
4.2.191 PIPEAWIDEGAMUTCOLORCORRECTIONC11_C10COEFFICIENTS—Offset 600B8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 600B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Reserved.
27:16	0x0 RW	**C11_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0x0 RO	**RESERVED_1:** Reserved.
11:0	0x0 RW	**C10_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

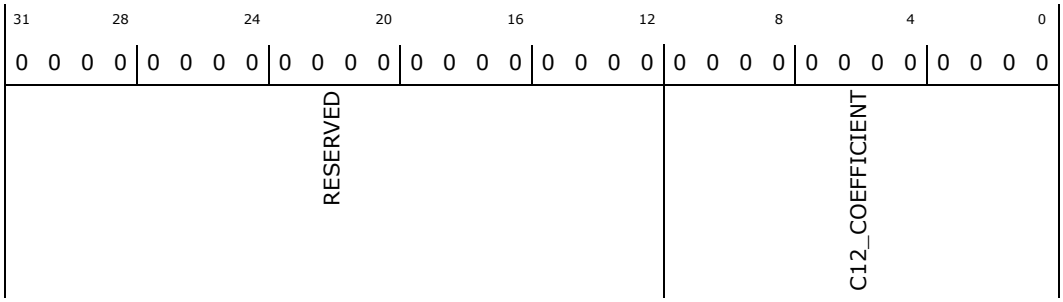
4.2.192 PIPEAWIDEGAMUTCOLORCORRECTIONC12COEFFICIENT—Offset 600BCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 600BCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RESERVED:** Reserved.
11:0	0x0 RW	**C12_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

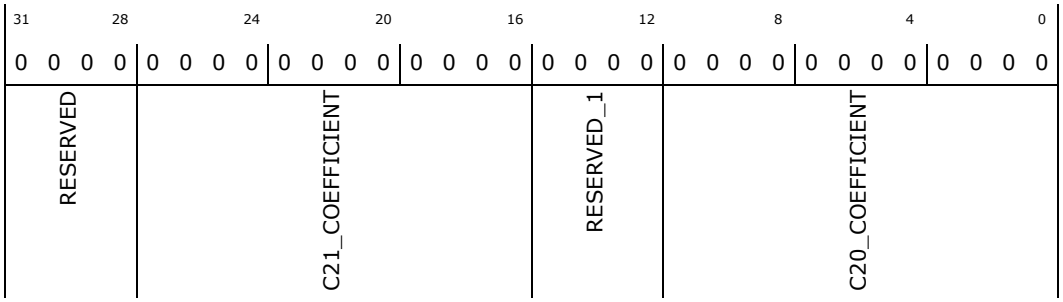
4.2.193 PIPEAWIDEGAMUTCOLORCORRECTIONC21_C20COEFFICIENTS—Offset 600C0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 600C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Reserved.
27:16	0x0 RW	**C21_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
15:12	0x0 RO	**RESERVED_1:** Reserved.
11:0	0x0 RW	**C20_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

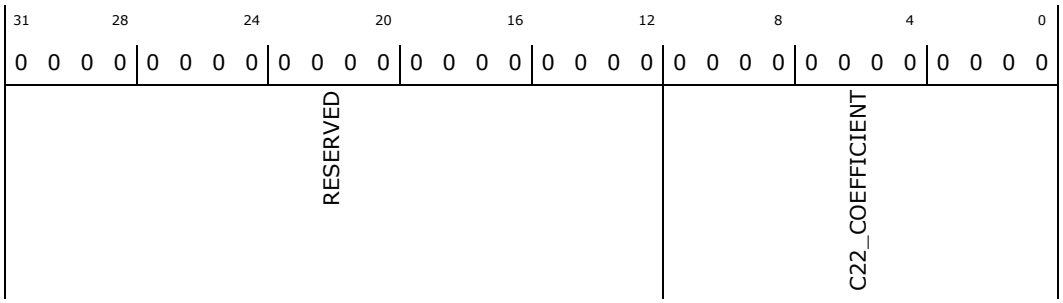
4.2.194 PIPEAWIDEGAMUTCOLORCORRECTIONC22COEFFICIENT—Offset 600C4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 600C4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RESERVED:** Reserved.
11:0	0x0 RW	**C22_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

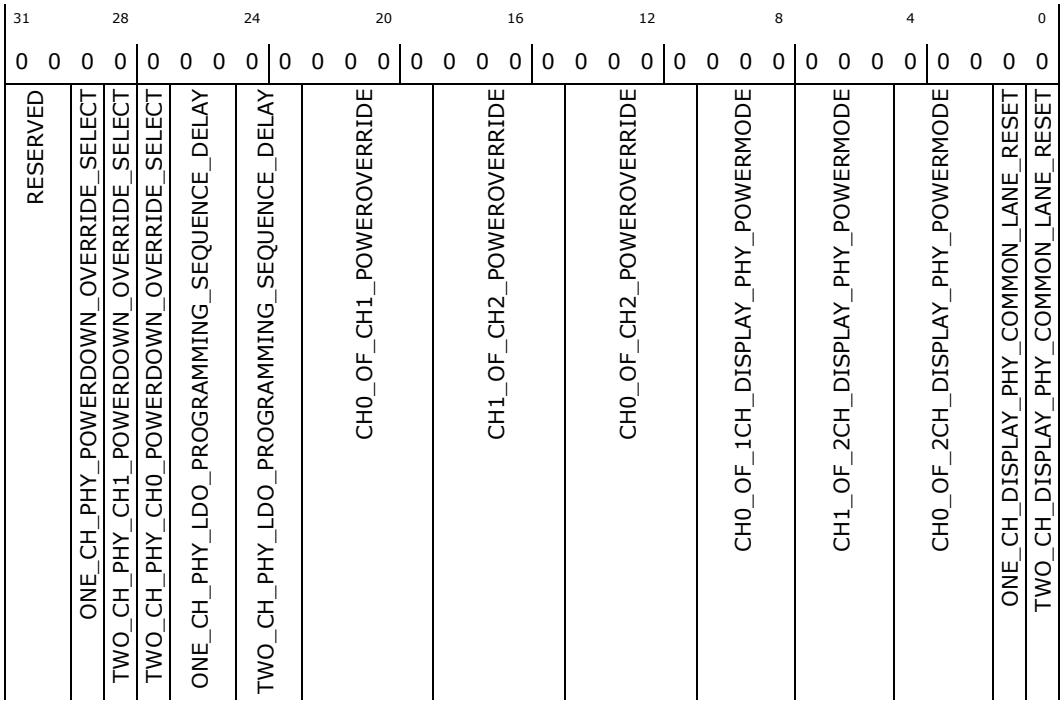
4.2.195 DISPLAY_PHY_CONTROL_REGISTER (DISPLAY_PHY_CONTROL_REGISTER1)—Offset 60100h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60100h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**RESERVED:** Reserved.
29	0x0 RW	**ONE_CH_PHY_POWERDOWN_OVERRIDE_SELECT:** 0 = powerdown/ mode signals from controller logic 1 = powerdown/mode signals from driver configuration
28	0x0 RW	**TWO_CH_PHY_CH1_POWERDOWN_OVERRIDE_SELECT:** 0 = powerdown/mode signals from controller logic 1 = powerdown/mode signals from driver configuration
27	0x0 RW	**TWO_CH_PHY_CH0_POWERDOWN_OVERRIDE_SELECT:** 0 = powerdown/mode signals from controller logic 1 = powerdown/mode signals from driver configuration

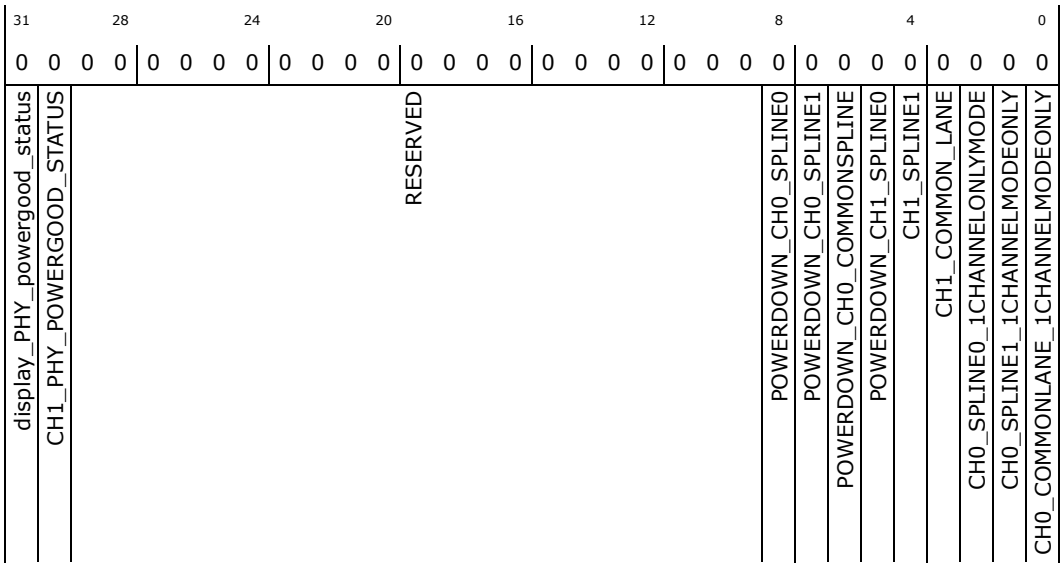
Bit Range	Default & Access	Field Name (ID): Description
26:25	0x0 RW	**ONE_CH_PHY_LDO_PROGRAMMING_SEQUENCE_DELAY:** 00 - Parallel Bringup of LDO/PG 01 - 200ns between power up of each LDO/PG 10 - 600ns between power up of each LDO/PG (Used by default for initial bringup)
24:23	0x0 RW	**TWO_CH_PHY_LDO_PROGRAMMING_SEQUENCE_DELAY:** 00 - Parallel Bringup of LDO/PG 01 - 200ns between power up of each LDO/PG 10 - 600ns between power up of each LDO/PG (Used by default for initial bringup)
22:19	0x0 RO	**CH0_OF_CH1_POWEROVERRIDE:** This value takes effect when bit 29 of this register is set to 1
18:15	0x0 RO	**CH1_OF_CH2_POWEROVERRIDE:** This value takes effect when bit 28 of this register is set to 1
14:11	0x0 RO	**CH0_OF_CH2_POWEROVERRIDE:** This value takes effect when bit 27 of this register is set to 1
10:8	0x0 RO	**CH0_OF_1CH_DISPLAY_PHY_POWERMODE:** 001 - Clock distribution from PLL EBB is gated. All data lane clocks gated in clock buffer module. But dclkp is free running (must). TX driver is put in high z. Usage model is in SU PSR mode where fast exit latency is required. PLL must be ON for SU PSR. 111 - Usage model is in deep PSR and legacy PSR mode where power saving is of high importance. POR for SoC. Data spline power gated if both i_pwrdown is ?11? for a spline. Unused Data lane is clock gated if one of i_pwrdown is ?1? for a spline.
7:5	0x0 RO	**CH1_OF_2CH_DISPLAY_PHY_POWERMODE:** 001 - Clock distribution from PLL EBB is gated. All data lane clocks gated in clock buffer module. But dclkp is free running (must). TX driver is put in high z. Usage model is in SU PSR mode where fast exit latency is required. PLL must be ON for SU PSR. 111 - Usage model is in deep PSR and legacy PSR mode where power saving is of high importance. POR for SoC. Data spline power gated if both i_pwrdown is ?11? for a spline. Unused Data lane is clock gated if one of i_pwrdown is ?1? for a spline.
4:2	0x0 RO	**CH0_OF_2CH_DISPLAY_PHY_POWERMODE:** 001 - Clock distribution from PLL EBB is gated. All data lane clocks gated in clock buffer module. But dclkp is free running (must). TX driver is put in high z. Usage model is in SU PSR mode where fast exit latency is required. PLL must be ON for SU PSR. 111 - Usage model is in deep PSR and legacy PSR mode where power saving is of high importance. POR for SoC. Data spline power gated if both i_pwrdown is ?11? for a spline. Unused Data lane is clock gated if one of i_pwrdown is ?1? for a spline.
1	0x0 RW	**ONE_CH_DISPLAY_PHY_COMMON_LATE_RESET (ONE_CH_DISPLAY_PHY_COMMON_LANE_RESET):** 0 means reset assert and 1 means reset deassert
0	0x0 RW	**TWO_CH_DISLAY_PHY_COMMON_LANE_RESET (TWO_CH_DISPLAY_PHY_COMMON_LANE_RESET):** 1 means deassert and 0 means reset assert

4.2.196 DISPLAY_PHY_STATUS_REGISTER1—Offset 60104h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 60104h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**display_PHY_powergood_status:** Reserved.
30	0x0 RW	**CH1_PHY_POWERGOOD_STATUS:** Reserved.
29:9	0x0 RO	**RESERVED:** Reserved.
8	0x0 RW	**POWERDOWN_CH0_SPLINE0:** 1 means LDO is off and 0 means LDO is on
7	0x0 RW	**This is powerdown ack for ch0 spline 1 LDO (POWERDOWN_CH0_SPLINE1):** 1 means LDO is off and 0 means LDO is on
6	0x0 RW	**This is powerdown ack for ch0 Common lane LDO (POWERDOWN_CH0_COMMONSPLINE):** 1 means LDO is off and 0 means LDO is on
5	0x0 RW	**POWERDOWN_CH1_SPLINE0:** 1 means LDO is off and 0 means LDO is on
4	0x0 RW	**CH1_SPLINE1:** 1 means LDO is off and 0 means LDO is on
3	0x0 RW	**CH1_COMMON_LANE:** 1 means LDO is off and 0 means LDO is on

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**CH0_SPLINE0_1CHANNELONLYMODE:** 1 means LDO is off and 0 means LDO is on
1	0x0 RW	**CH0_SPLINE1_1CHANNELMODEONLY:** 1 means LDO is off and 0 means LDO is on
0	0x0 RW	**CH0_COMMONLANE_1CHANNELMODEONLY:** 1 means LDO is off and 0 means LDO is on

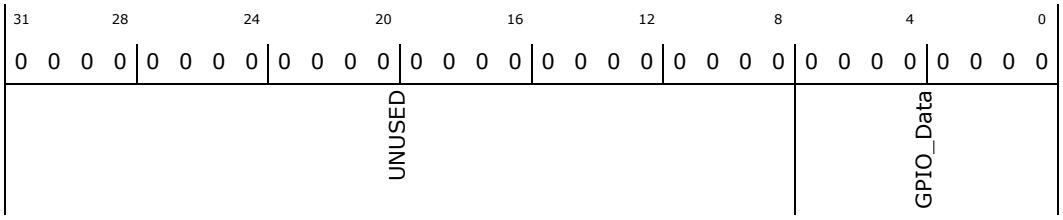
4.2.197 DISPLAY_PHY_GPIO_DATA_REGISTER—Offset 60108h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60108h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**UNUSED:** mbz
7:0	0x0 RO	**GPIO_Data:** GPIO data lane3,lane2,lan1,lane0

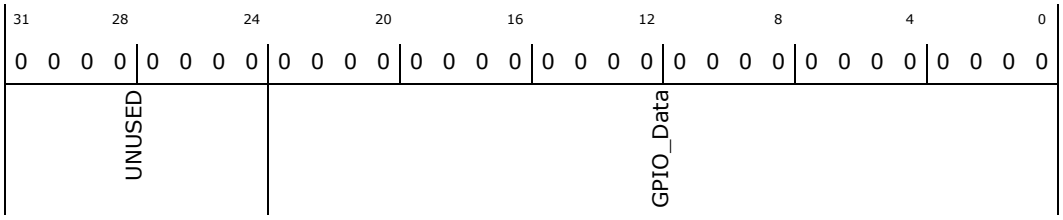
4.2.198 DISPLAY_PHY_STATUS_REGISTER2—Offset 6010Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6010Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**UNUSED:** mbz
23:0	0x0 RO	**GPIO_Data:** GPIO data PipeD GPIO,PipeC GPIO,PipeBGPIO

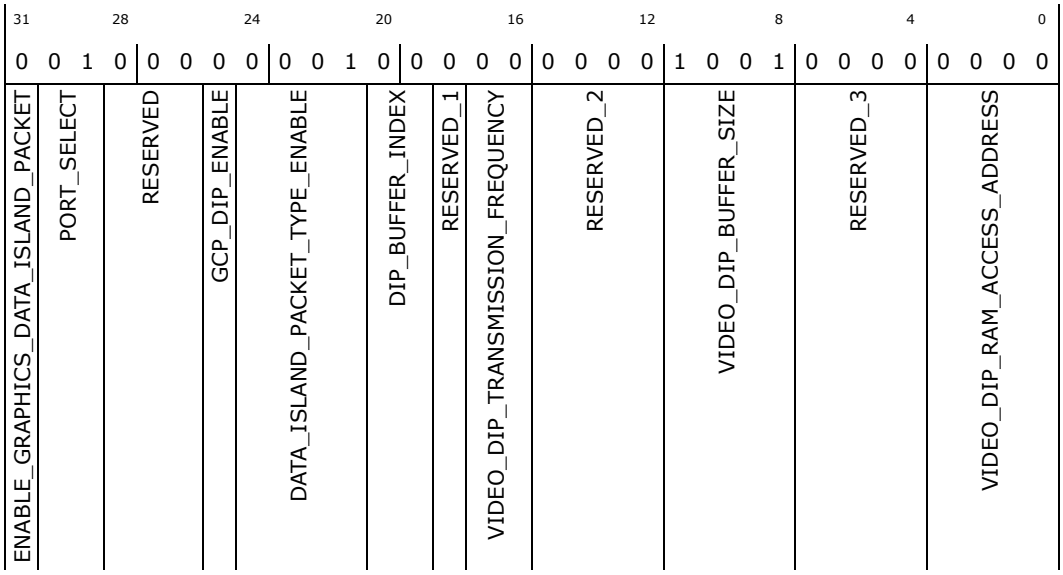
4.2.199 VIDEO_DIP_CTL_A—Offset 60200h

Video DIP Control for Pipe A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 60200h

Default: 20200900h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**ENABLE_GRAPHICS_DATA_ISLAND_PACKET:** mode (bit #9 of port control register) overrides this behavior.
30:29	0x1 RW	**PORT_SELECT:** Project: All Default Value: ;01b Digital Port B This selects which port is to transmit the data island. This field must not be changed while data island transmission is enabled. Value Name Description Project 00b Reserved Reserved All 01b Digital Port B Digital Port B (Default) All 10b Digital Port C Digital Port C All 11b Reserved Reserved All
28:26	0x0 RO	**RESERVED:** Project: All Format:

Bit Range	Default & Access	Field Name (ID): Description
25	0x0 RW	**GCP_DIP_ENABLE:** Project: All Default Value: ;0b This bit enables the output of the General Control Packet. GCP is different from other DIPs in that much of the payload is automatically reflected in the packet, and therefore a DIP buffer for GCP is not needed. Please refer to the GCP payload register for payload details. Writes to this bit take effect immediately. This bit should not be enabled for 8bpc mode if at least one of the other HDMI ports is enabled in 12bpc mode. Value Name Description Project 0b Disable GCP DIP disabled All 1b Enable GCP DIP enabled All
24:21	0x1 RW	**DATA_ISLAND_PACKET_TYPE_ENABLE:** Project: All Default Value: ;0001b Enable AVI DIP These bits enable the output of a given data island packet (DIP) type. It can be updated while the port is enabled and is immediately updated (not double-buffered). Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Value Name Description Project XXX1b Enable AVI Enable AVI DIP (Default = enabled) All XX1Xb Enable Vendor Enable Vendor-specific DIP (Default = disabled) All X1XXb Enable Gamut Enable Gamut Metadata Packet (Default = disabled) All 1XXXb Enable Source Enable Source Product Description DIP (Default = disabled) All
20:19	0x0 RW	**DIP_BUFFER_INDEX:** Project: All Default Value: ;00b This field is used during programming of different DIPs. These bits are used as an index to their respective DIP buffers. The transmission frequency must also be written when programming the buffer. Value Name Description Project 00b AVI AVI DIP (31 bytes of space available) All 01b Vendor-specific Vendor-specific DIP All 10b Reserved Reserved All 11b Source Product Source Product Description DIP All
18	0x0 RO	**RESERVED_1:** Project: All Format:
17:16	0x0 RW	**VIDEO_DIP_TRANSMISSION_FREQUENCY:** Project: All Default Value: ;00b These bits dictate the frequency of Video DIP transmission for the DIP buffer index designated in bits 20:19. When writing Video DIP data, this value is also latched when the first DW of the Video DIP is written. When read, this value reflects the Video DIP transmission frequency for the Video DIP buffer designated in bits 20:19. This field shall be ignored for Gamut Metadata Packet transmission. Value Name Description Project 00b Send Once Send Once All 01b Every VSync Send Every VSync (Default for AVI) All 10b Every Other Vsync Send at least every other VSync All 11b Reserved Reserved All
15:12	0x0 RO	**RESERVED_2:** Project: All Format: MBZ

Bit Range	Default & Access	Field Name (ID): Description
11:8	0x9 RO	**VIDEO_DIP_BUFFER_SIZE:** Project: All AccessType: Read Only Default Value: ;1001b This reflects the buffer size in dwords available for the type of Video DIP being indexed by bits 20:19 of this register, including the header. It is hardwired to the maximum size of a Video DIP, 36 bytes. Please note that this count includes ECC bytes, which are not writable by software. These bits are immediately valid after write of the DIP index.
7:4	0x0 RO	**RESERVED_3:** Project: All Format: MBZ
3:0	0x0 RO	**VIDEO_DIP_RAM_ACCESS_ADDRESS:** Project: All AccessType: Read Only Selects the DWORD address for access to the Video DIP buffers. This value is automatically incremented after each read or write of the Video DIP Data Register. The value wraps back to zero when it autoincrements past the max address value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

4.2.200 VIDEO_DIP_DATA_A—Offset 60208h

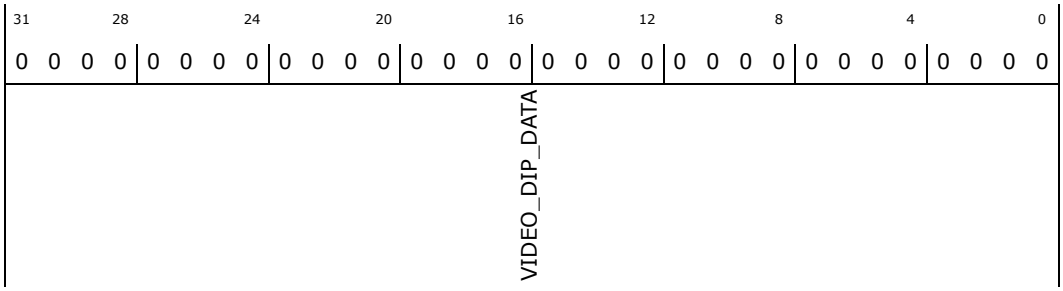
Video Data Island Packet Data for Pipe A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60208h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VIDEO_DIP_DATA:** Project: All When read, this returns the current value at the location specified in the Video DIP buffer index select and Video DIP RAM access address fields. The index used to address the RAM is incremented after each read or write of this register. DIP data can be read at any time. Data should be loaded into the RAM before enabling the transmission through the DIP type enable bit. Accesses to this register are on a per-DWORD basis.

4.2.201 VIDEO_DIP_GDCP_PAYLOAD_A—Offset 60210h

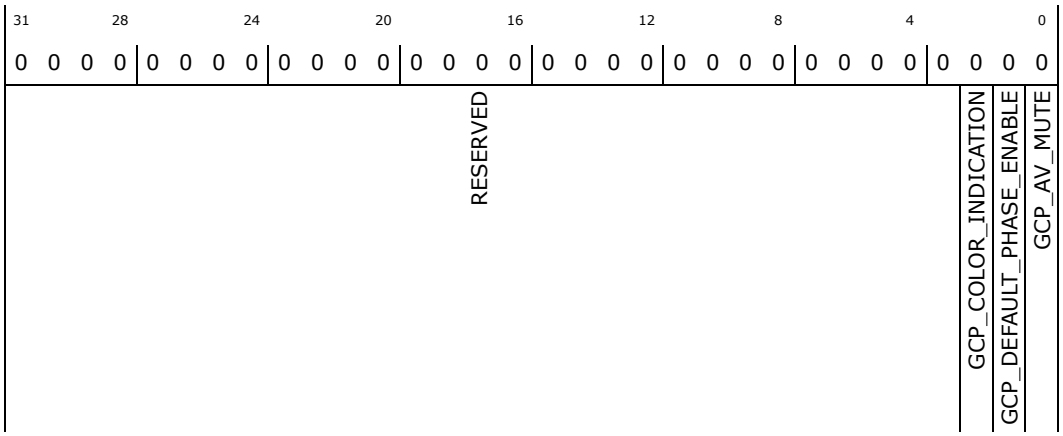
Video Data Island Payload for Pipe A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60210h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**RESERVED:** Project: All Format: MBZ
2	0x0 RW	**GCP_COLOR_INDICATION:** Project: All Default Value: ;0b This bit must be set when in deep color mode. It may optionally be set for 24-bit mode. It must be set if the sink attached to Pipe A can receive GCP data. Value Name Description Project 0b Dont Indicate Dont indicate color depth. CD and PP bits in GCP set to zero All 1b Indicate Indicate color depth using CD bits in GCP. It will be set depending on programmed pixel depth in port control register All
1	0x0 RW	**GCP_DEFAULT_PHASE_ENABLE:** Project: All Default Value: ;0b Indicates the video timings meet alignment requirements such that the following conditions are met: Htotal is an even number Hactive is an even number Hsync is an even number Front and back porches for Hsync are even numbers Vsync always starts on an even-numbered pixel within a line in interlaced modes (starting counting with 0) Value Name Description Project 0b Clear Default phase bit in GCP is cleared All 1b Require Met Default phase bit in GCP is set. All requirements must be met before setting this bit All

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**GCP_AV_MUTE:** Project: All Default Value: ;0b Set AV mute bit in GCP Value Name Description Project 0b Clear AV mute bit in GCP is cleared. When this bit transitions to 0, the AV mute clear flag is sent in the next GCP packet All 1b Set AV mute bit in GCP is set. When this bit transitions to 1, the AV mute set flag is sent in the next GCP packet All

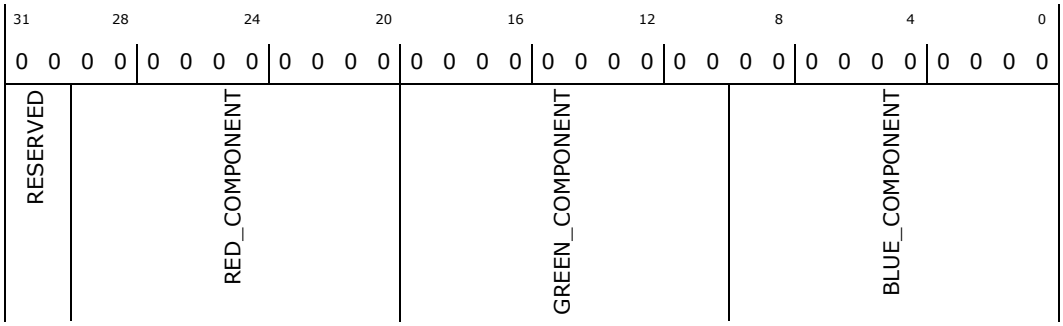
4.2.202 CANVAS_A—Offset 60A04h

Pipe A Canvas Color Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 60A04h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RESERVED:** Reserved.
29:20	0x0 RO	**RED_COMPONENT:** Red Component
19:10	0x0 RO	**GREEN_COMPONENT:** GREEN Component
9:0	0x0 RO	**BLUE_COMPONENT:** BLUE Component

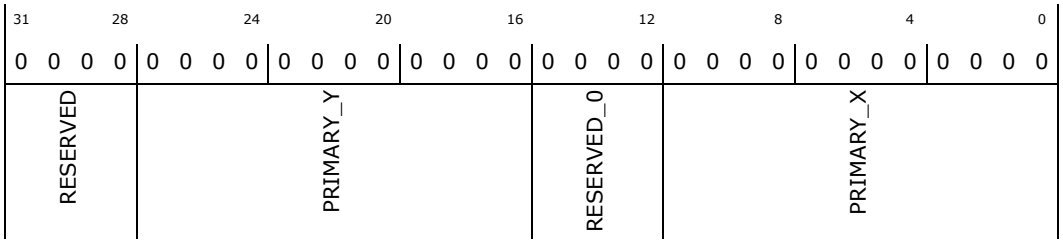
4.2.203 PRIMPOS_A—Offset 60A08h

These registers specify the screen position and size of the primary. This register is double buffered. The load register is transferred into the active register on the asserting edge of Vertical Blank for the pipe that the display is assigned. When using the primary as a secondary display, this should be set to the entire display rectangle.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 60A08h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as Zero.
27:16	0x0 RW	**Primary_Y (PRIMARY_Y):** These 12 bits specify the vertical position in lines of the primary (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the un-rotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0x0 RO	**RESERVED_0:** Write as Zero
11:0	0x0 RW	**PRIMARY_X:** These 12 bits specify the horizontal position in lines of the primary (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the end of the active video area in the un-rotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

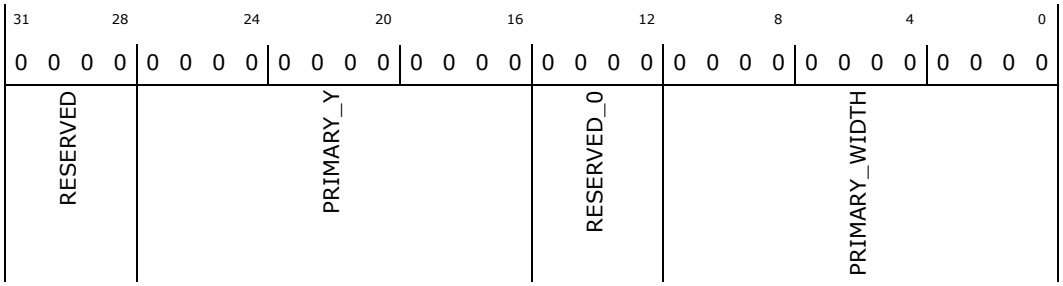
4.2.204 PRIMSIZE_A—Offset 60A0Ch

This register specifies the height and width of the primary in pixels and lines. The rectangle defined by the size and position should never exceed the boundaries of the display rectangle that the primary is assigned to.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 60A0Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as Zero.
27:16	0x0 RW	**Primary_Height (PRIMARY_Y):** This register field is used to specify the height of the primary in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0x0 RO	**RESERVED_0:** Write as Zero
11:0	0x0 RW	**PRIMARY_WIDTH:** This register field is used to specify the width of the primary in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined primary rectangle must always be completely contained within the displayable area of the screen image.

4.2.205 PRIMA_CONSTANT—Offset 60A10h

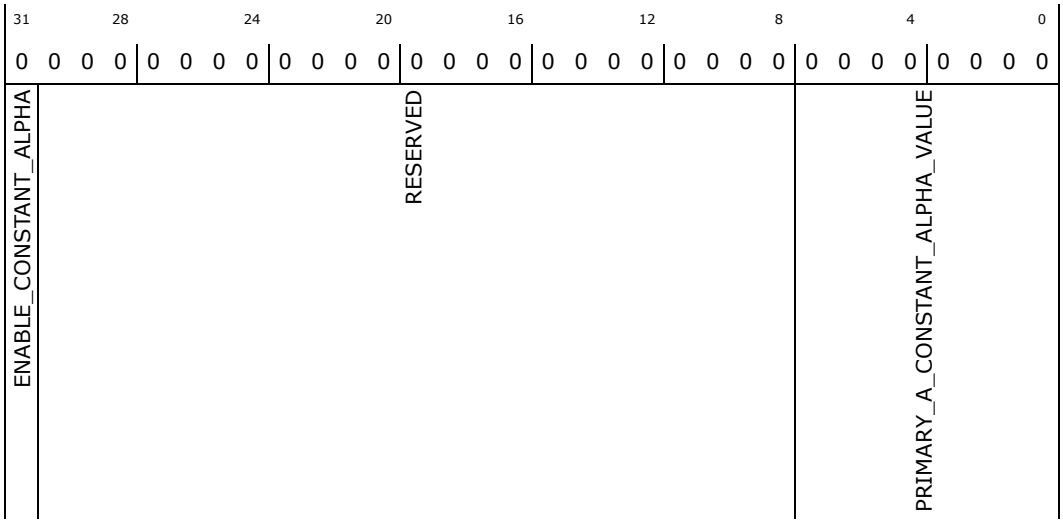
Primary A constant Alpha

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 60A10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Enable_CONSTANT_ALPHA (ENABLE_CONSTANT_ALPHA):** Primary A constant alpha provides a way to apply an alpha value to all primary pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. 0-Primary A Constant Alpha is disabled. 1-Primary A Constant Alpha Enabled
30:8	0x0 RO	**RESERVED:** RESERVED: MBZ
7:0	0x0 RW	**PRIMARY_A_CONSTATN_ALPHA_VALUE (PRIMARY_A_CONSTANT_ALPHA_VALUE):** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of primary with other surfaces.

4.2.206 HTOTAL_B—Offset 61000h

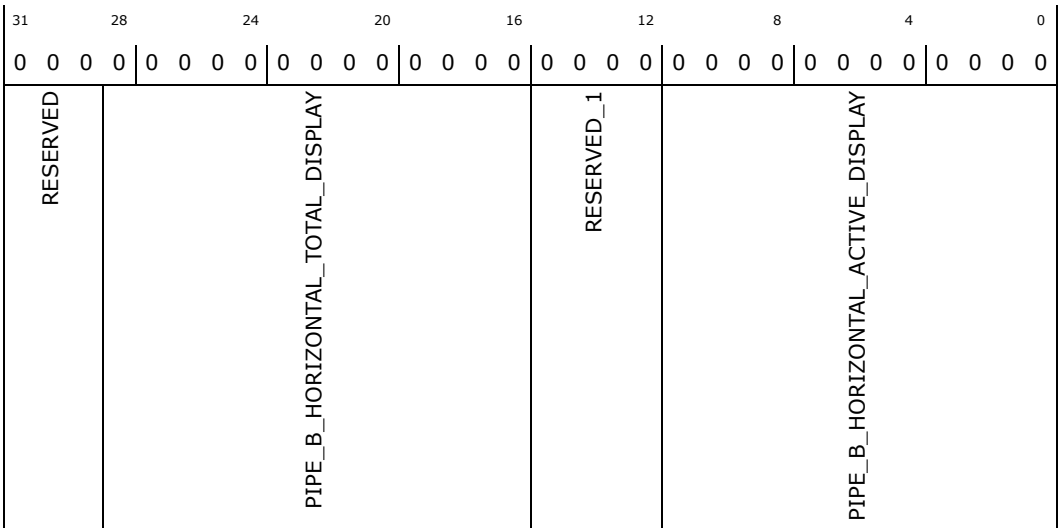
Pipe B Horizontal Total Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61000h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Write as zero.
28:16	0x0 RW	**PIPE_B_HORIZONTAL_TOTAL_DISPLAY:** Refer pipe A description.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0x0 RO	**RESERVED_1:** Write as zero.
11:0	0x0 RW	**PIPE_B_HORIZONTAL_ACTIVE_DISPLAY:** Refer pipe A description

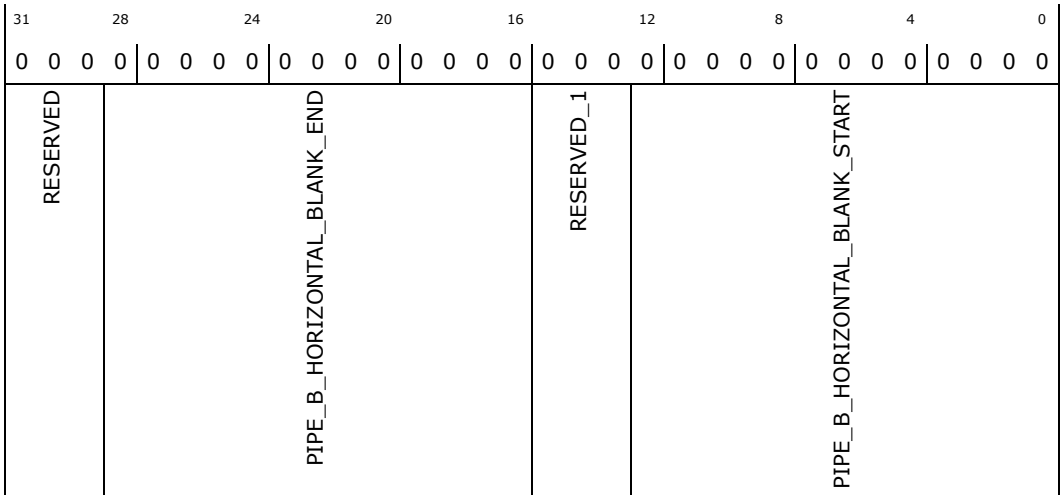
4.2.207 HBLANK_B—Offset 61004h

Pipe B Horizontal Blank Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61004h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** . Write as zero.
28:16	0x0 RW	**PIPE_B_HORIZONTAL_BLANK_END:** Refer pipe A description
15:13	0x0 RO	**RESERVED_1:** Write as zero.
12:0	0x0 RW	**PIPE_B_HORIZONTAL_BLANK_START:** Refer pipe A description.

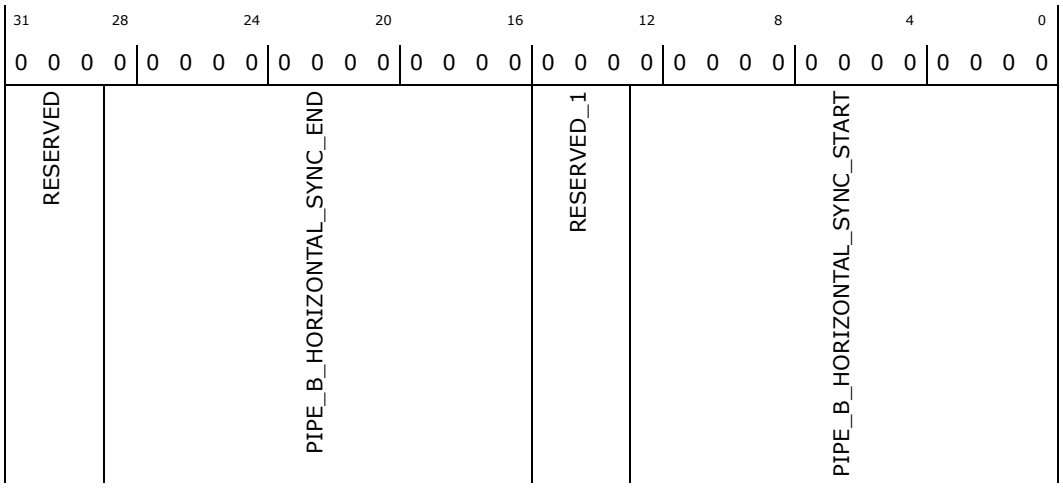
4.2.208 HSYNC_B—Offset 61008h

Pipe B Horizontal Sync Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61008h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Write as zero.
28:16	0x0 RW	**PIPE_B_HORIZONTAL_SYNC_END:** Refer pipe A description.
15:13	0x0 RO	**RESERVED_1:** Write as zero.
12:0	0x0 RW	**PIPE_B_HORIZONTAL_SYNC_START:** Refer pipe A description

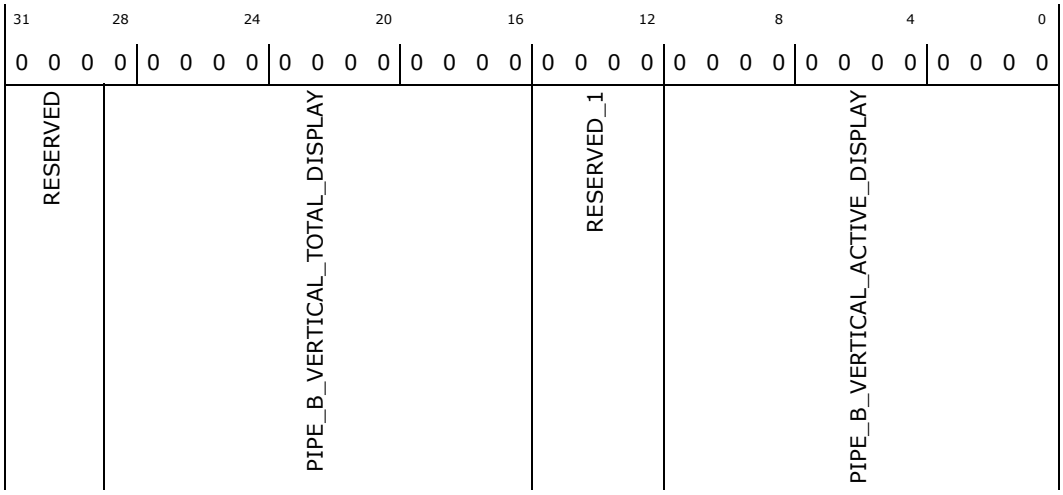
4.2.209 VTOTAL_B—Offset 6100Ch

Pipe B Vertical Total Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6100Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Write as zero.
28:16	0x0 RW	**PIPE_B_VERTICAL_TOTAL_DISPLAY:** Refer pipe A description.
15:12	0x0 RO	**RESERVED_1:** Write as zero.
11:0	0x0 RW	**PIPE_B_VERTICAL_ACTIVE_DISPLAY:** Refer pipe A description.

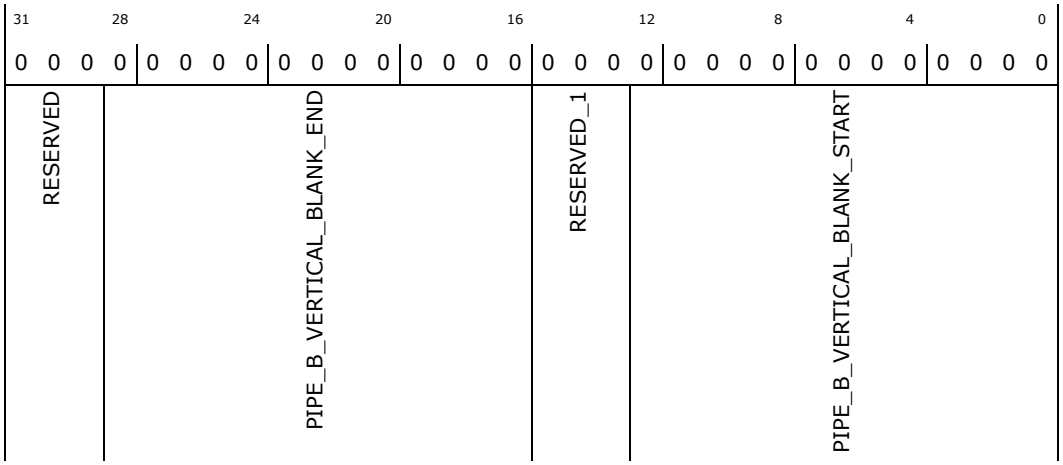
4.2.210 VBLANK_B—Offset 61010h

Pipe B Vertical Blank Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61010h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Write as zero.
28:16	0x0 RW	**PIPE_B_VERTICAL_BLANK_END:** Refer pipe A description.
15:13	0x0 RO	**RESERVED_1:** Write as zero.
12:0	0x0 RW	**PIPE_B_VERTICAL_BLANK_START:** Refer pipe A description.

4.2.211 VSYNC_B—Offset 61014h

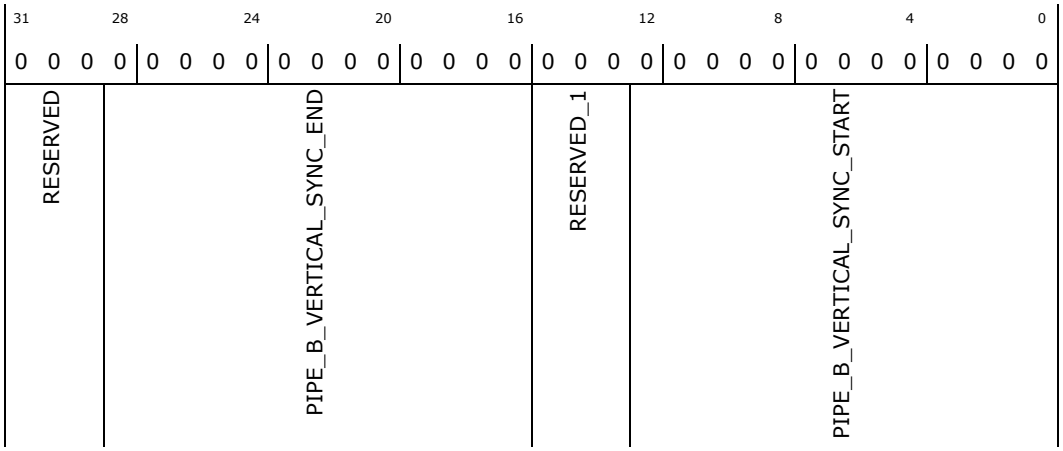
Pipe B Vertical Sync Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61014h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Write as zero.
28:16	0x0 RW	**PIPE_B_VERTICAL_SYNC_END:** Refer pipe A description.
15:13	0x0 RO	**RESERVED_1:** Write as zero.
12:0	0x0 RW	**PIPE_B_VERTICAL_SYNC_START:** Refer pipe A description.

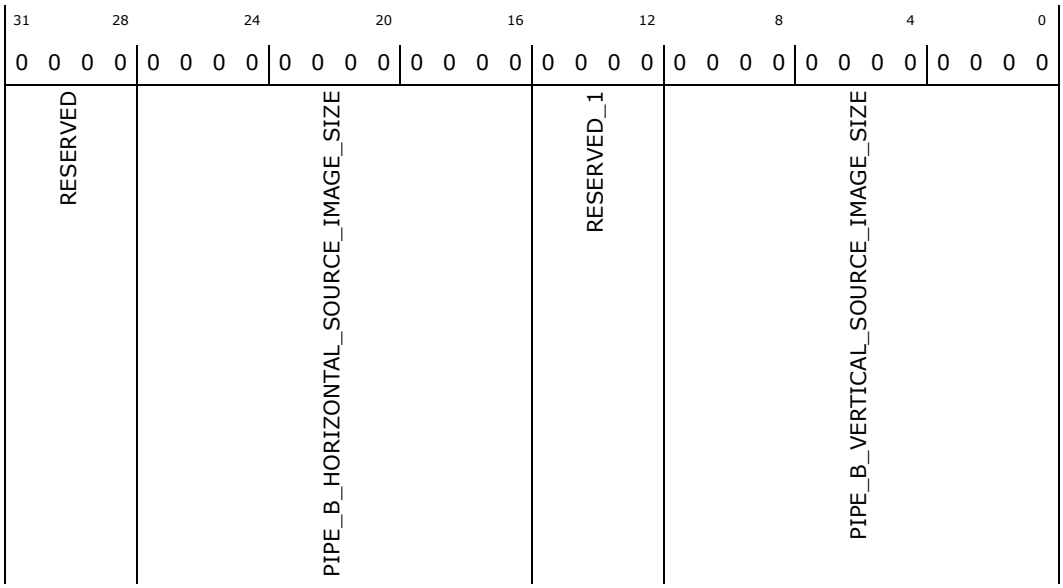
4.2.212 PIPEBSRC—Offset 6101Ch

Pipe B Source Image Size

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6101Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**PIPE_B_HORIZONTAL_SOURCE_IMAGE_SIZE:** Refer pipe A description.
15:12	0x0 RO	**RESERVED_1:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
11:0	0x0 RW	**PIPE_B_VERTICAL_SOURCE_IMAGE_SIZE:** Refer pipe A description.

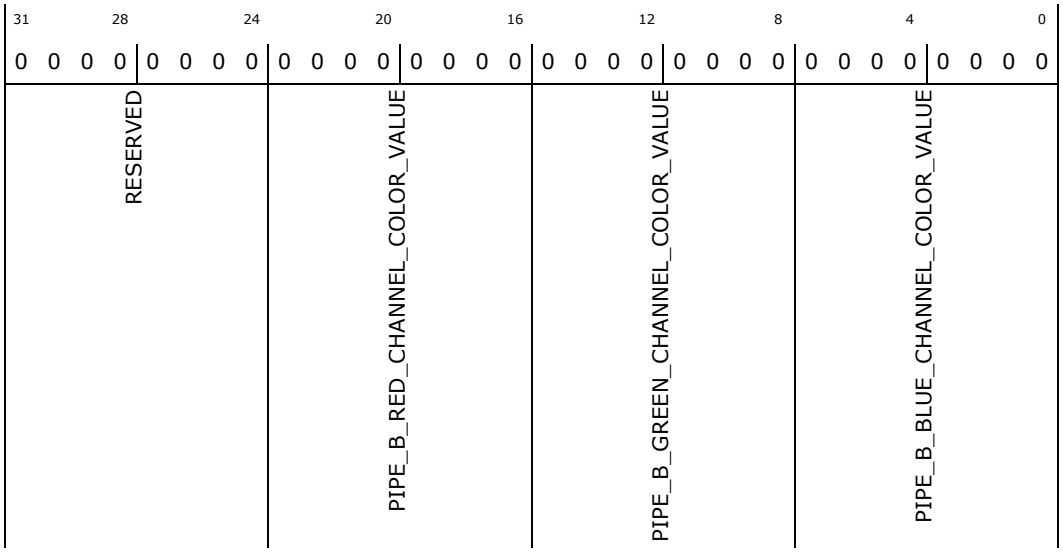
4.2.213 BCLRPAT_B—Offset 61020h

Pipe B Border Color Pattern Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61020h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:16	0x0 RW	**PIPE_B_RED_CHANNEL_COLOR_VALUE:** Reserved.
15:8	0x0 RW	**PIPE_B_GREEN_CHANNEL_COLOR_VALUE:** Reserved.
7:0	0x0 RW	**PIPE_B_BLUE_CHANNEL_COLOR_VALUE:** Reserved.

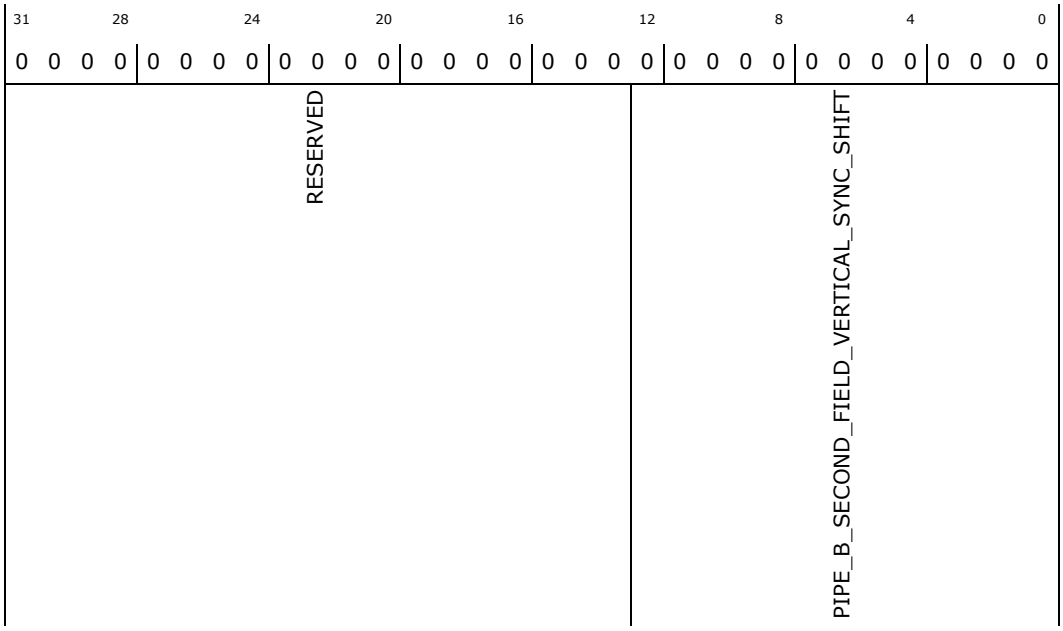
4.2.214 VSYNCSHIFT_B—Offset 61028h

Vertical Sync Shift Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61028h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RESERVED:** Write as zero.
12:0	0x0 RW	**PIPE_B_SECOND_FIELD_VERTICAL_SYNC_SHIFT:** This value specifies the vertical sync alignment for the start of the interlaced second field expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the PIPEBCONF is programmed to an interlaced mode using vsync shift. Otherwise a legacy value of floor[htotal / 2] will be used. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed to: (horizontal sync start - floor[horizontal total / 2]) (use the actual horizontal sync start and horizontal total values and not the minus one values programmed into registers). This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.

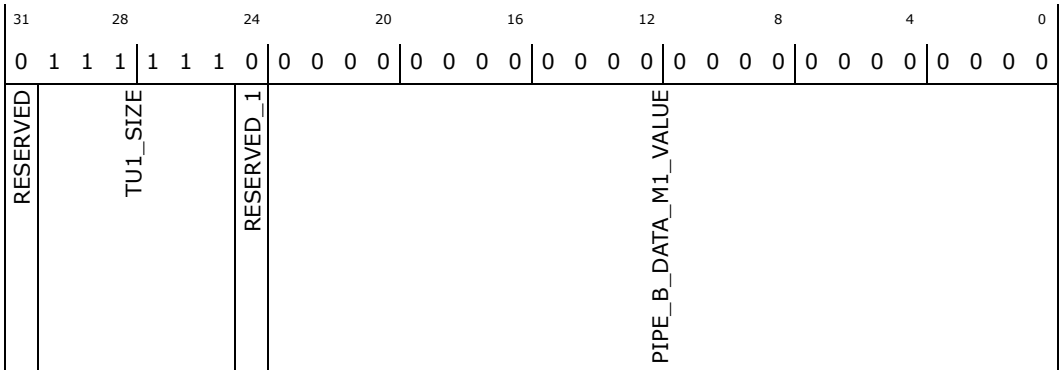
4.2.215 TRANSBDATAM1—Offset 61030h

Pipe B Data M value 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61030h

Default: 7E000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** Project: All Format: MBZ
30:25	0x3f RW	**TU1_SIZE:** Project: All Default Value: ;111111b 64 Refer Pipe A description.
24	0x0 RO	**RESERVED_1:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_B_DATA_M1_VALUE:** Project: All Refer Pipe A description.

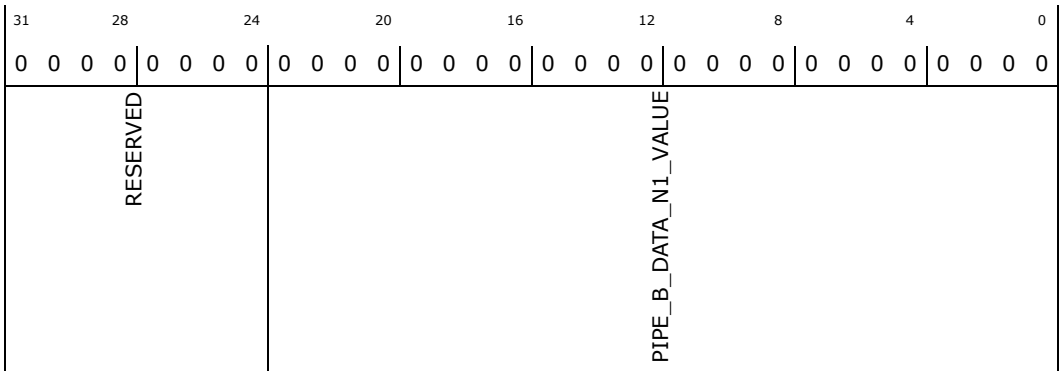
4.2.216 TRANSBDATAN1—Offset 61034h

Pipe B Data N value 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61034h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_B_DATA_N1_VALUE:** Project: All Refer Pipe A description.

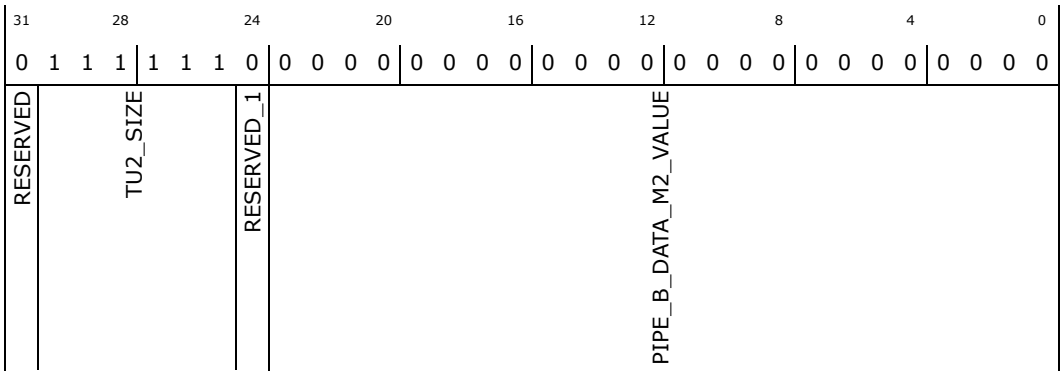
4.2.217 TRANSBDATAM2—Offset 61038h

Pipe B Data M value 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61038h

Default: 7E000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** Project: All Format: MBZ
30:25	0x3f RW	**TU2_SIZE:** Project: All Default Value: ;111111b 64 Refer Pipe A description.
24	0x0 RO	**RESERVED_1:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_B_DATA_M2_VALUE:** Project: All Refer Pipe A description.

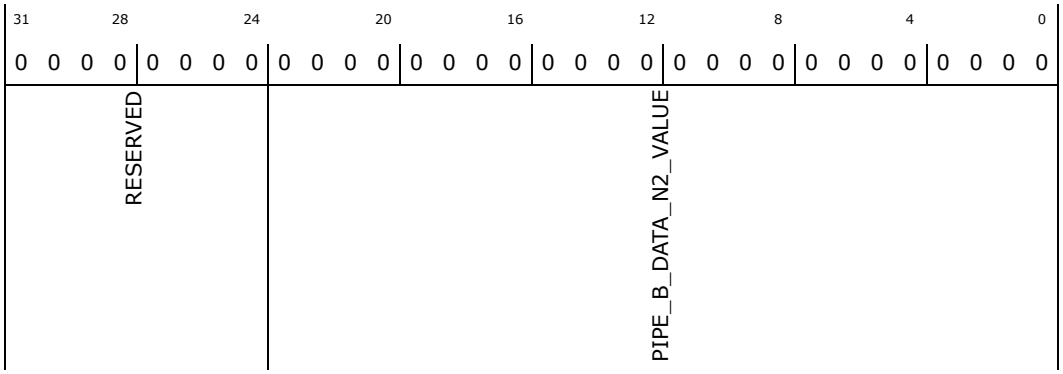
4.2.218 TRANSBDATAN2—Offset 6103Ch

Pipe B Data N value 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6103Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_B_DATA_N2_VALUE:** Project: All Refer Pipe A description.

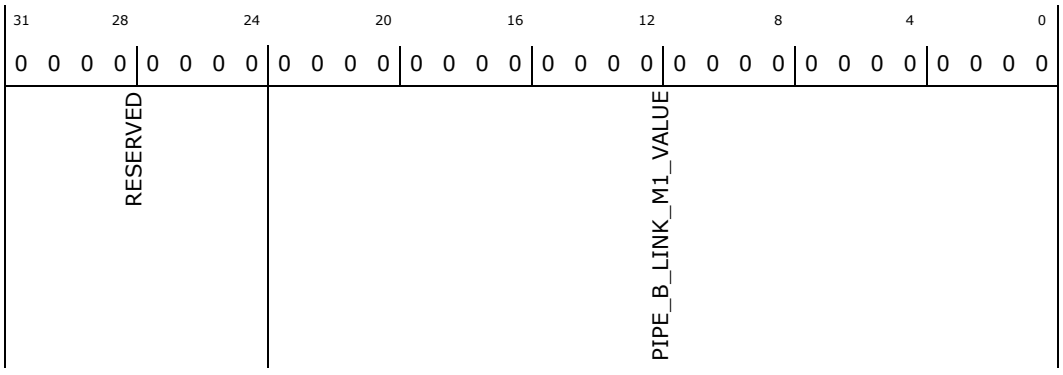
4.2.219 TRANSBDPLINKM1—Offset 61040h

Pipe B Link M value 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61040h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_B_LINK_M1_VALUE:** Project: All Refer Pipe A description.

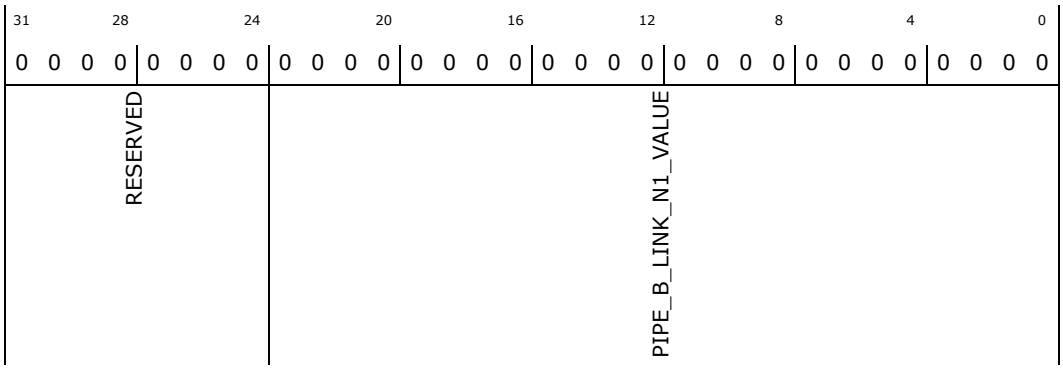
4.2.220 TRANSBDPLINKN1—Offset 61044h

Pipe B Link N value 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61044h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_B_LINK_N1_VALUE:** Project: All Refer Pipe A description.

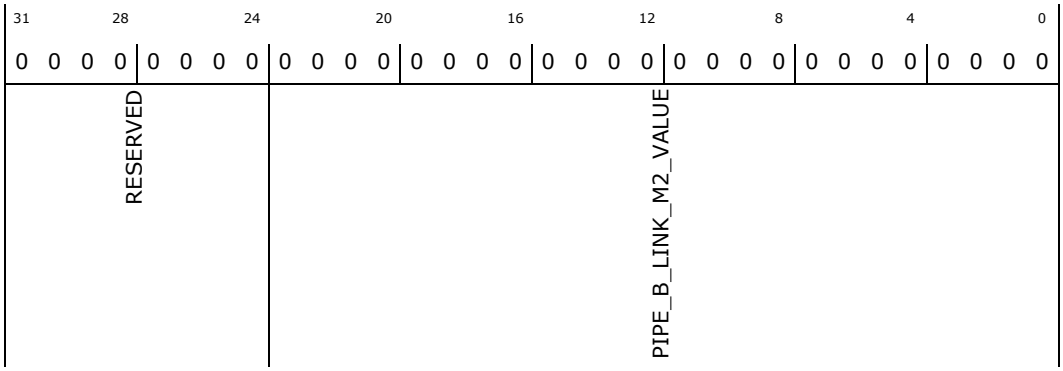
4.2.221 TRANSBDPLINKM2—Offset 61048h

Pipe B Link M value 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61048h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_B_LINK_M2_VALUE:** Project: All Refer Pipe A description.

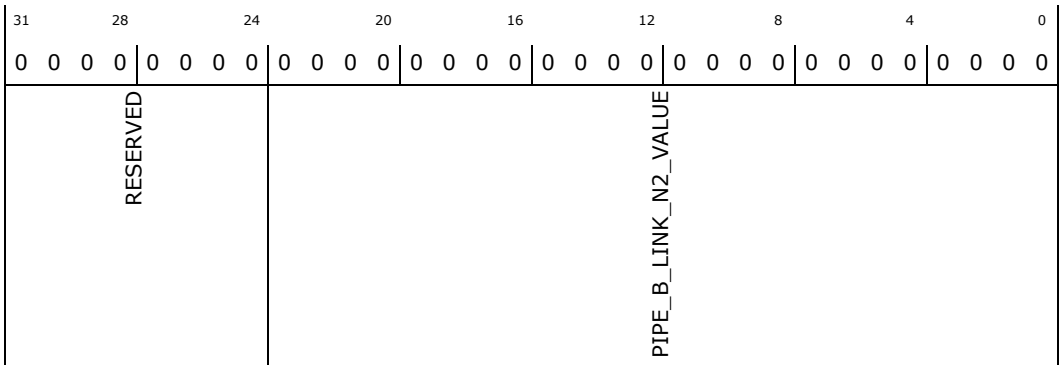
4.2.222 TRANSBDPLINKN2—Offset 6104Ch

Pipe B Link N value 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6104Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_B_LINK_N2_VALUE:** Project: All Refer Pipe A description.

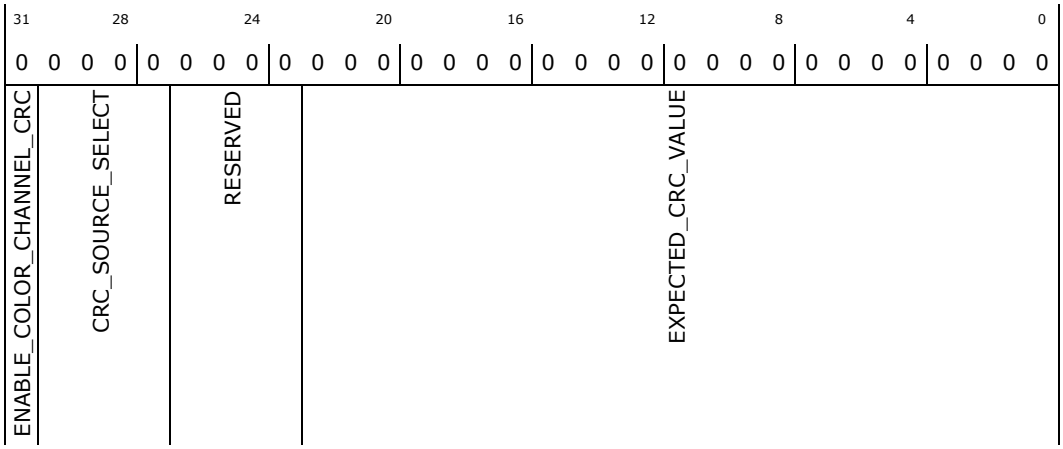
4.2.223 CRCCTRLREDB—Offset 61050h

Pipe B CRC Color Control Register (Red)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61050h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**ENABLE_COLOR_CHANNEL_CRC:** After being enabled for the first time, you need to wait for two VBLANK events for a valid CRC result. After that, a CRC will be generated each frame. 0 = CRC Calculations are disabled 1 = CRC Calculations are enabled
30:27	0x0 RW	**CRC_SOURCE_SELECT:** These bits select the source of the data to put into the CRC logic. 0000: Pipe B (Not available when DisplayPort or TV is enabled on this pipe) 0001: sDVOB/HDMIB (30 bit format. Only select when HDMIB is set to pipe B) 0010: sDVOC/HDMIC (30 bit format. Only select when HDMIC is set to pipe B) 0011: DisplayPort D (40 bit format) 0100: TV Encoder outputs (30 bit format) 0101: TV filter outputs (30 bit format) 0110: DisplayPort B (40 bit format) 0111: DisplayPort C (40 bit format) 1000: Audio DP (Audio for DisplayPort (pcdclk). Only select when Audio is on DisplayPort on Pipe B) 1001: Audio HDMI (Audio for HDMI (dotclock) Only select when Audio is on HDMI on Pipe B) Others: Reserved
26:23	0x0 RO	**RESERVED:** Write as zero
22:0	0x0 RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

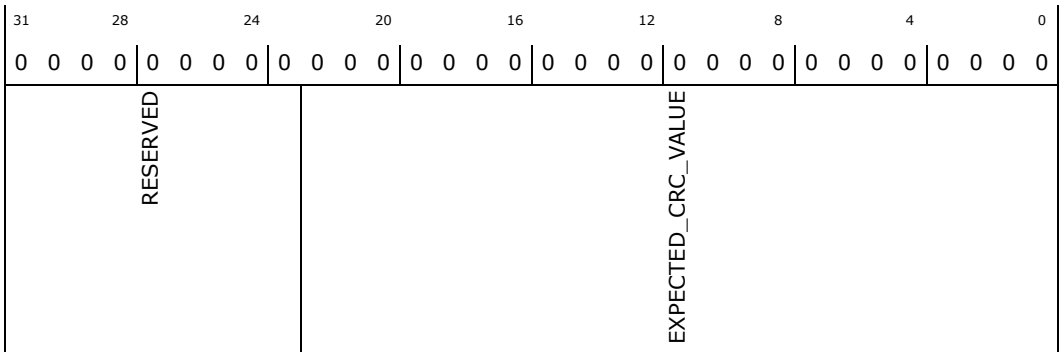
4.2.224 CRCCTRLGREENB—Offset 61054h

Pipe B CRC Color Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61054h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Write as zero
22:0	0x0 RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

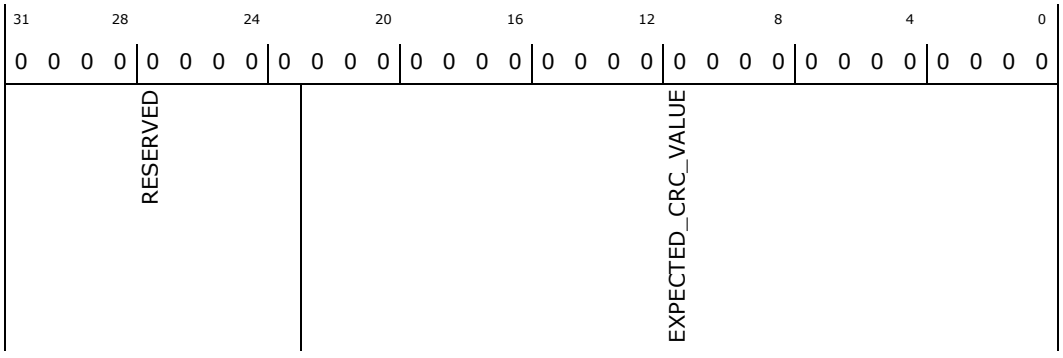
4.2.225 CRCCTRLBLUEB—Offset 61058h

Pipe B CRC Color Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61058h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
22:0	0x0 RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

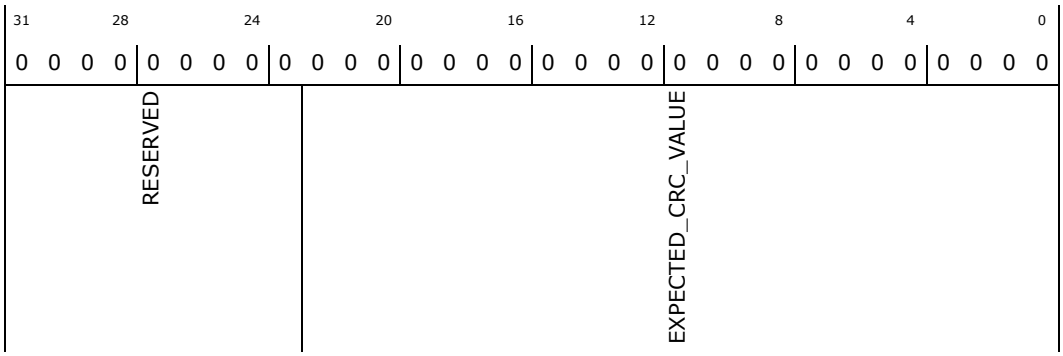
4.2.226 CRCCTRLALPHAB—Offset 6105Ch

Pipe B CRC Color Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6105Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Write as zero
22:0	0x0 RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

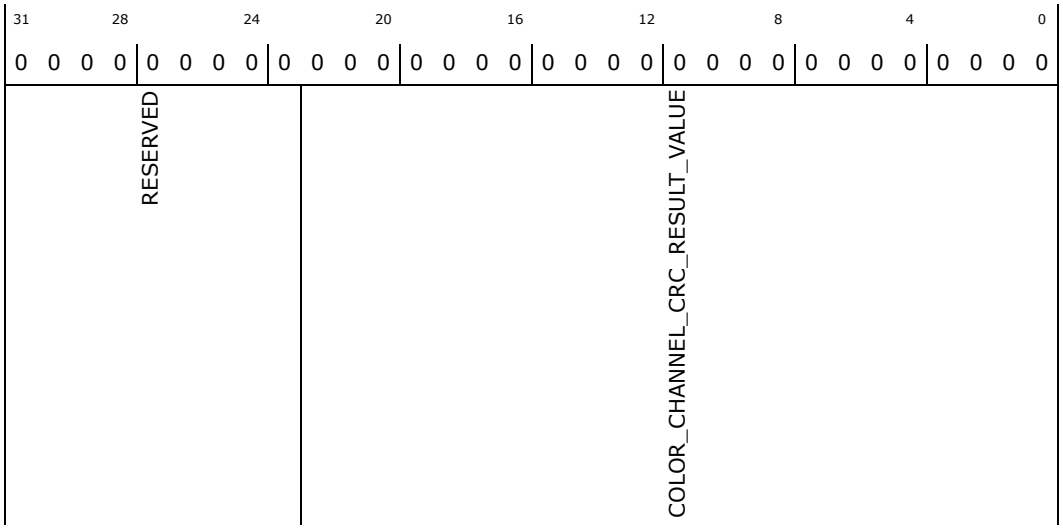
4.2.227 CRCRESREDB—Offset 61060h

Pipe B CRC Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61060h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Read only
22:0	0x0 RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

4.2.228 CRCRESGREENB—Offset 61064h

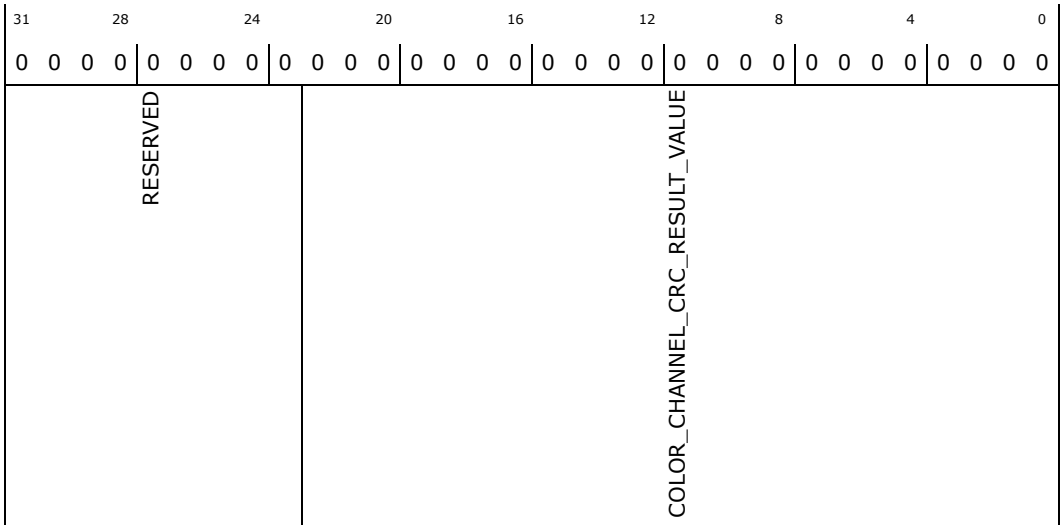
Pipe B CRC Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61064h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Read only
22:0	0x0 RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

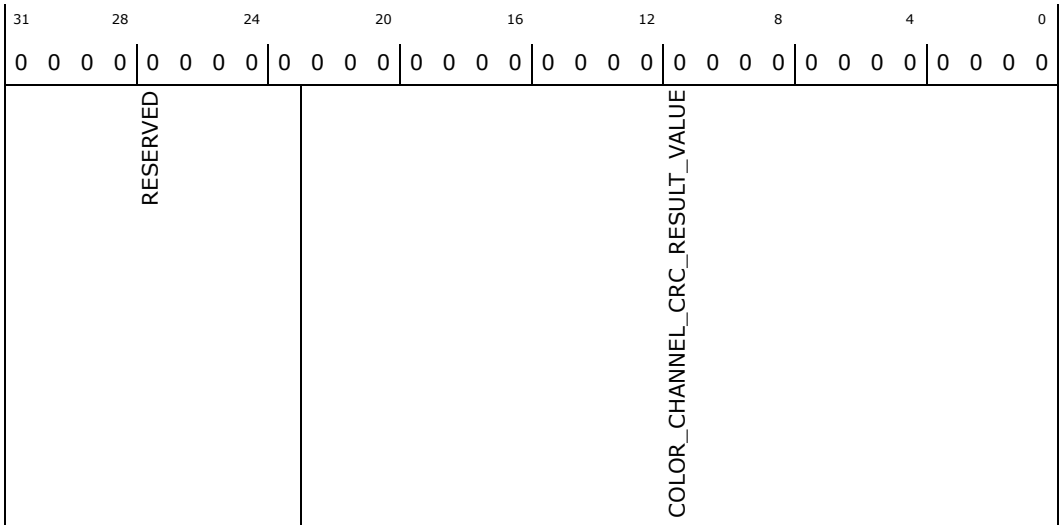
4.2.229 CRCRESBLUEB—Offset 61068h

Pipe B CRC Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61068h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Read only
22:0	0x0 RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

4.2.230 CRCRESALPHAB—Offset 6106Ch

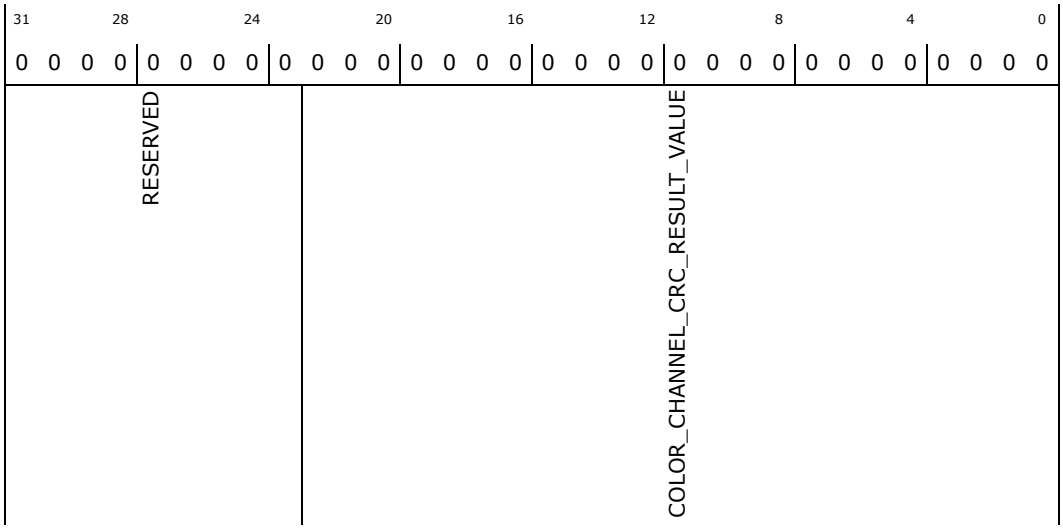
Pipe B CRC Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6106Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Read only
22:0	0x0 RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

4.2.231 CRCCTRLRESIDUE2B—Offset 61070h

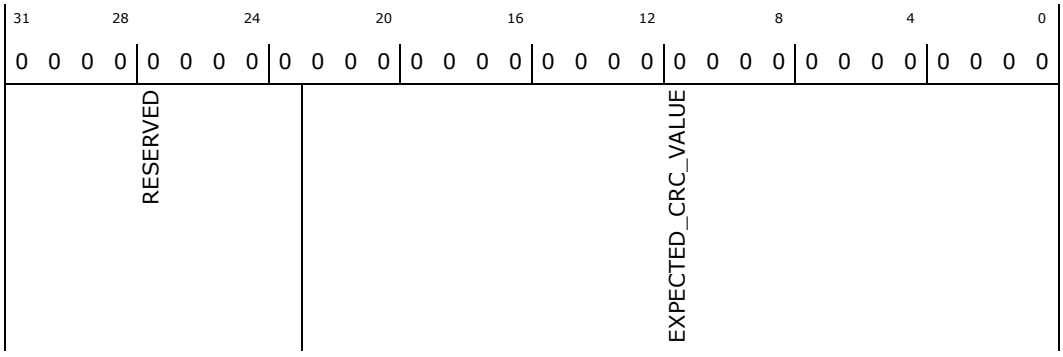
Pipe B CRC Color Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61070h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Write as zero
22:0	0x0 RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

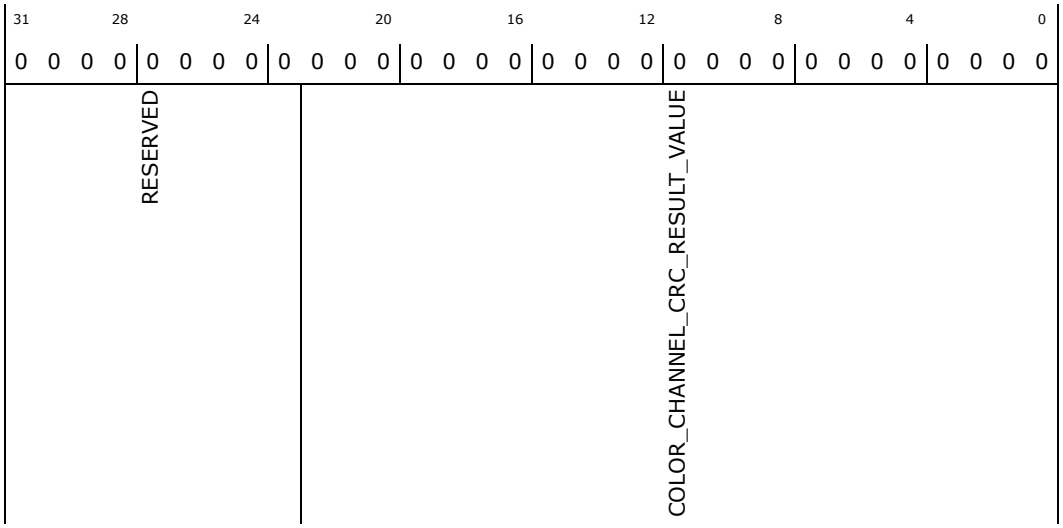
4.2.232 CRCRESRESIDUAL2B—Offset 61080h

Pipe B CRC Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61080h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Read only
22:0	0x0 RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

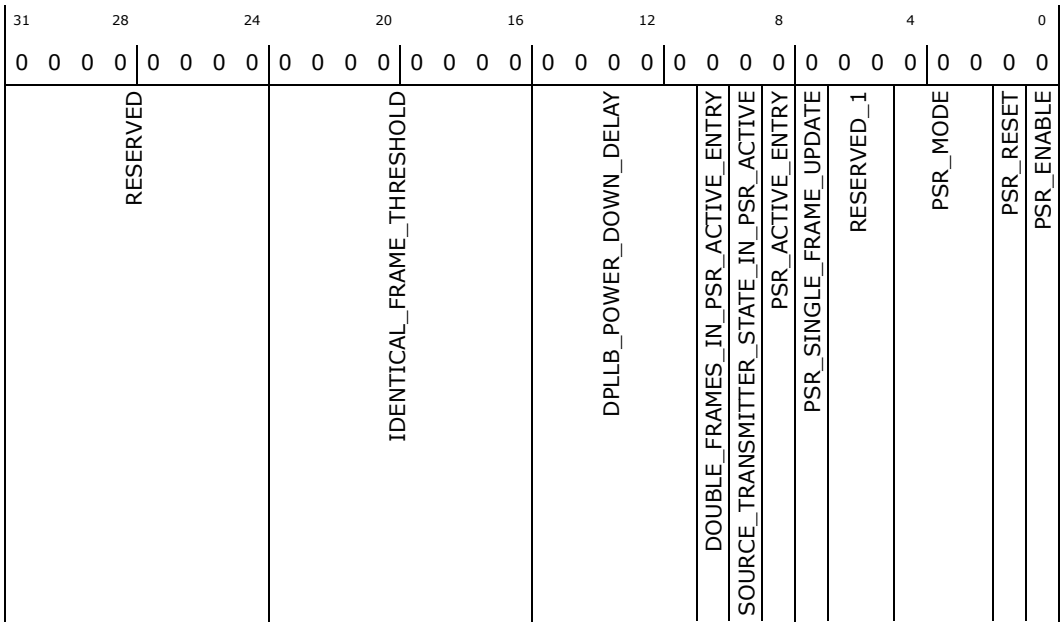
4.2.233 PSRCTLB—Offset 61090h

Pipe B Panel Self Refresh Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61090h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:16	0x0 RW	**IDENTICAL_FRAME_THRESHOLD:** : Number of identical frames that display controller needs to exceed in order to transition to PSR active state in HW timer mode
15:11	0x0 RW	**DPLLB_POWER_DOWN_DELAY:** programmable delay from main link powerdown to DPLLB powerdown. The delay is in number of cdclk clocks.
10	0x0 RW	**DOUBLE_FRAMES_IN_PSR_ACTIVE_ENTRY:** . If asserted, HW will send two frames with same SDP active setting when entry PSR active state. This bit is set if the vertical blanking time is less than 330us.
9	0x0 RW	**SOURCE_TRANSMITTER_STATE_IN_PSR_ACTIVE:** . If asserted, HW will keep transmitter active during PSR active state and sends only idle symbols. If deasserted, HW will turn off transmitter during PSR active state. Display driver will keep this bit consistent with Source transmitter state in PSR active bit in DPCD register of the sink.
8	0x0 RW	**PSR_ACTIVE_ENTRY:** This bit is only valid in PSR_mode is SW timer mode. If it is asserted, HW will transition into PSR_active state. If it is deasserted, HW will transition to PSR_inactive state. SW should not set or clear this bit more than once within one vblank period.
7	0x0 RW	**PSR_SINGLE_FRAME_UPDATE:** In PSR persistent mode, SW set this bit before writing registers for a flip. It will be self-clear when it gets to the PSR active state.

Bit Range	Default & Access	Field Name (ID): Description
6:5	0x0 RO	**RESERVED_1:** Reserved.
4:2	0x0 RW	**PSR_MODE:** b011-111: reserved. b010: PSR with HW timer. HW timer decides PSR active entry point. PSR active state exits upon MMIO write registers that may change the frame buffer. b001: PSR with SW timer. In this mode, SW will keep track of idle frames and buffer modification in the driver and explicitly specify the entry and exit PSR active state point. b000: PSR manual (debug) mode. All of PSR state transitions and SDP content is managed by SW driver. SW is responsible to change SDP content for every frame with appropriate values to keep PSR panel in synchronized states.
1	0x0 RW	**PSR_RESET:** If assert all PSR functions are reset back to PSR inactive state. When it needs to resynchronize source and sync, SW writes 0x2 to DPCD register 600h and to this bit to get system back to PSR active states. This bit is self clear.
0	0x0 RW	**PSR_ENABLE:** Panel Self-refresh is enabled. When it is asserted PSR is enabled and operate in one of the mode that specified by PSR mode.

4.2.234 PSRSTATB—Offset 61094h

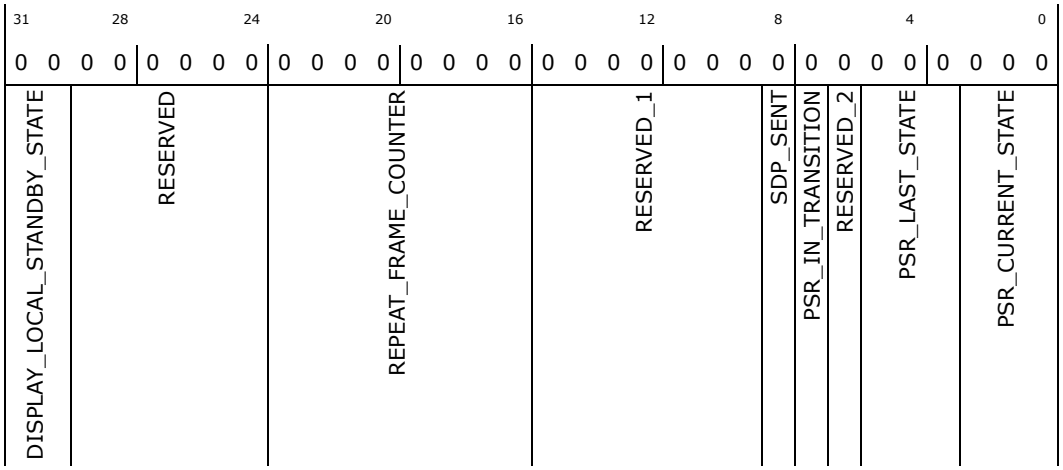
Pipe B PSR status register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61094h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**DISPLAY_LOCAL_STANDBY_STATE:** :00: D0 idle state, fetch frame buffer from system memory 02: D0i2 PSR is active, display controller is trunk gated 03: D0i3 PSR is active, display controller is power gated
29:24	0x0 RO	**RESERVED:** Reserved.
23:16	0x0 RO	**REPEAT_FRAME_COUNTER:** : Number of identical frames has been sent by display controller. Value is not roll over at 255.
15:9	0x0 RO	**RESERVED_1:** Reserved.
8	0x0 RO	**SDP_SENT:** it indicates if SDP packet has been sent in current frame.
7	0x0 RO	**PSR_IN_TRANSITION:** There is a period that source already committed to PSR active but sink did not. SW should not change the source state at this time but wait until this status bit is clear. The wait time should in the range of 120-250us in the worst case.
6	0x0 RO	**RESERVED_2:** Reserved.
5:3	0x0 RO	**PSR_LAST_STATE:** indicate last source state that PSR state machine were in (debug) 000: PSR_disabled 001: PSR_inactive 010: PSR_transition_to_active 011: PSR_active no RFB update 100: PSR_active single frame update 101: PSR_exit
2:0	0x0 RO	**PSR_CURRENT_STATE:** indicate current source state that PSR state machine are in 000: PSR_disabled 001: PSR_inactive 010: PSR_transition_to_active 011: PSR_active no RFB update 100: PSR_active single frame update 101: PSR_exit

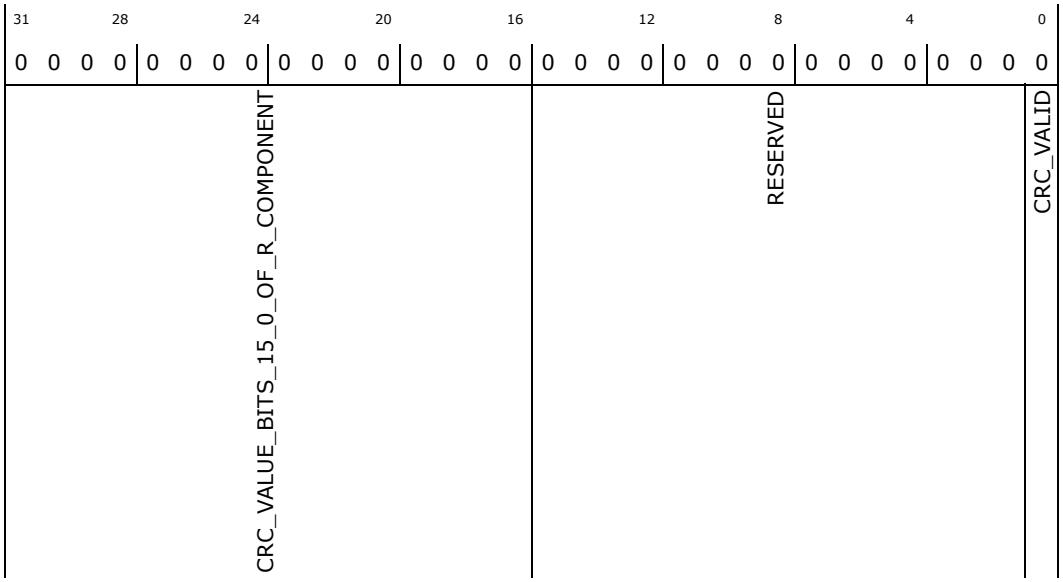
4.2.235 PSRCRC1B—Offset 61098h

Pipe B PSR CRC1 register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61098h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**CRC_VALUE_BITS_15_0_OF_R_COMPONENT:** Reserved.
15:1	0x0 RO	**RESERVED:** .
0	0x0 RO	**CRC_VALID:** CRC calculation complete and valid for previous frame.

4.2.236 PSRCRC2B—Offset 6109Ch

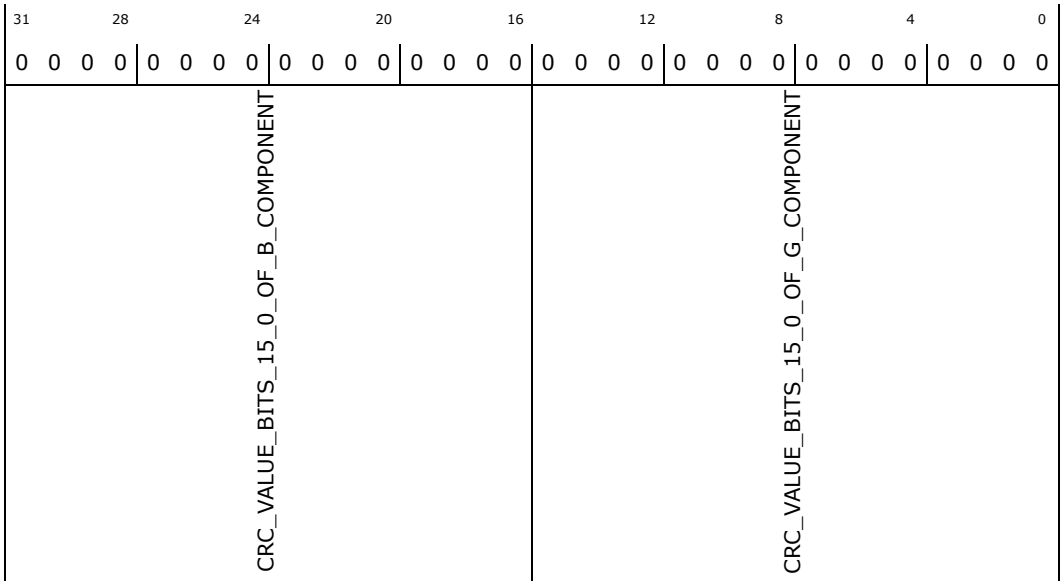
Pipe B PSR CRC2 register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6109Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**CRC_VALUE_BITS_15_0_OF_B_COMPONENT:** Reserved.
15:0	0x0 RO	**CRC_VALUE_BITS_15_0_OF_G_COMPONENT:** Reserved.

4.2.237 VSCSDPB—Offset 610A0h

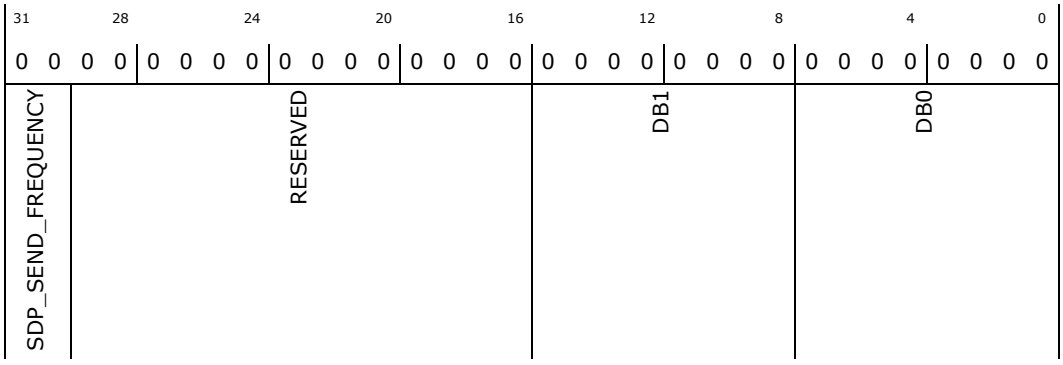
Pipe B VSC SDP register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 610A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**SDP_SEND_FREQUENCY:** 00: off, not sending 01: send one every frame 10: send once 11: reserved When PSR is enabling this field is ignored. One SDP is sent in every frame until source is in PSR active state
29:16	0x0 RO	**RESERVED:** Reserved.
15:8	0x0 RW	**DB1:** Programmed by display driver in manual mode, auto-generate by display controller in all other modes
7:0	0x0 RW	**DB0:** Bits 7:4: Stereo Interface Method Specific Parameter Bits 3:0: Stereo Interface Method Code. This field is programmed by display driver for stereo display configuration

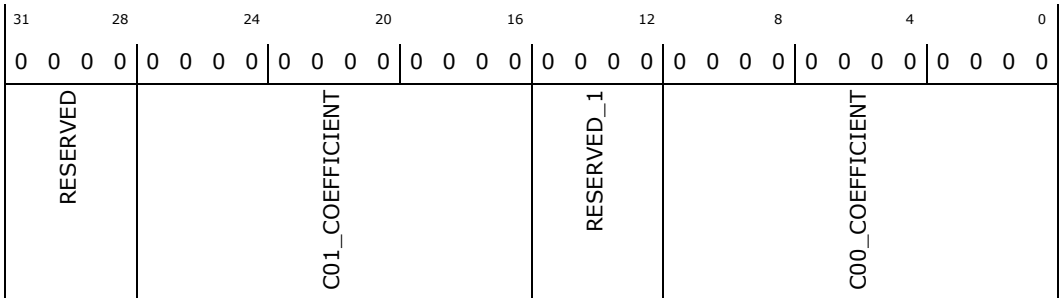
4.2.238 PIPEBWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS—Offset 610B0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 610B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Reserved.
27:16	0x0 RW	**C01_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
15:12	0x0 RO	**RESERVED_1:** Reserved.
11:0	0x0 RW	**C00_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

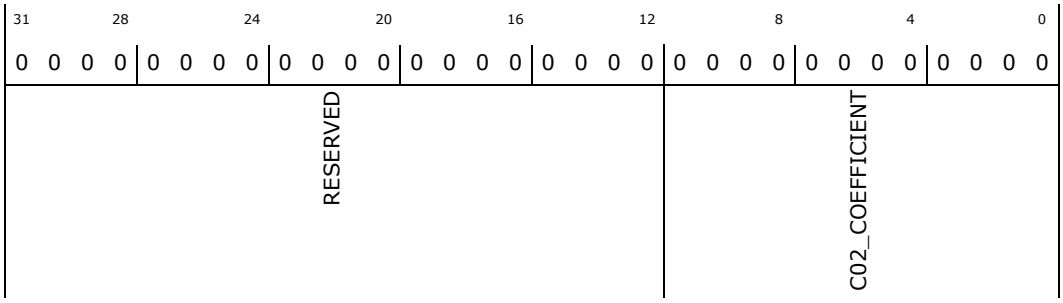
4.2.239 PIPEBWIDEGAMUTCOLORCORRECTIONC02COEFFICIENT—Offset 610B4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 610B4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RESERVED:** Reserved.
11:0	0x0 RW	**C02_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

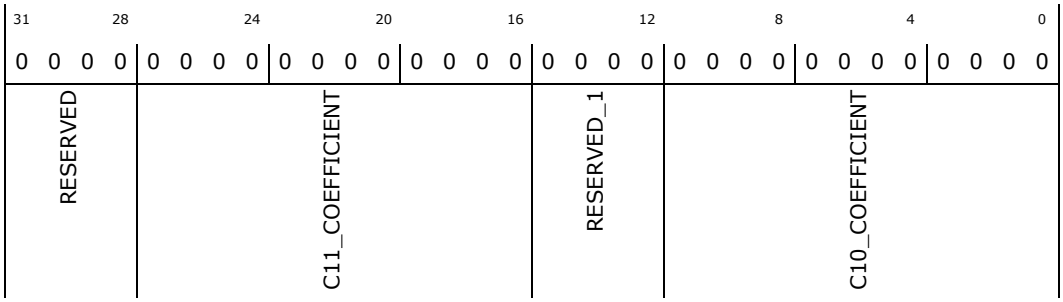
4.2.240 PIPEBWIDEGAMUTCOLORCORRECTIONC11_C10COEFFICIENTS—Offset 610B8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 610B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Reserved.
27:16	0x0 RW	**C11_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0x0 RO	**RESERVED_1:** Reserved.
11:0	0x0 RW	**C10_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

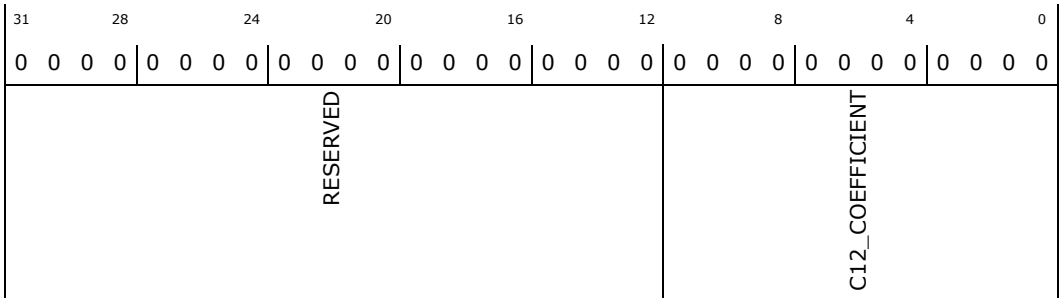
4.2.241 PIPEBWIDEGAMUTCOLORCORRECTIONC12COEFFICIENT—Offset 610BCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 610BCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RESERVED:** Reserved.
11:0	0x0 RW	**C12_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

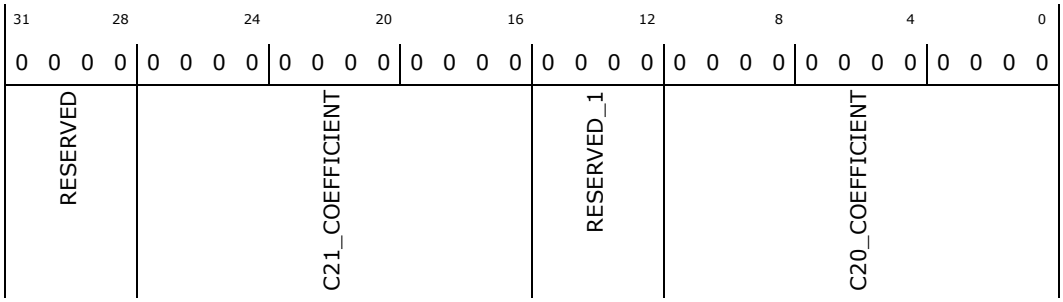
4.2.242 PIPEBWIDEGAMUTCOLORCORRECTIONC21_C20COEFFICIENTS—Offset 610C0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 610C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Reserved.
27:16	0x0 RW	**C21_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
15:12	0x0 RO	**RESERVED_1:** Reserved.
11:0	0x0 RW	**C20_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

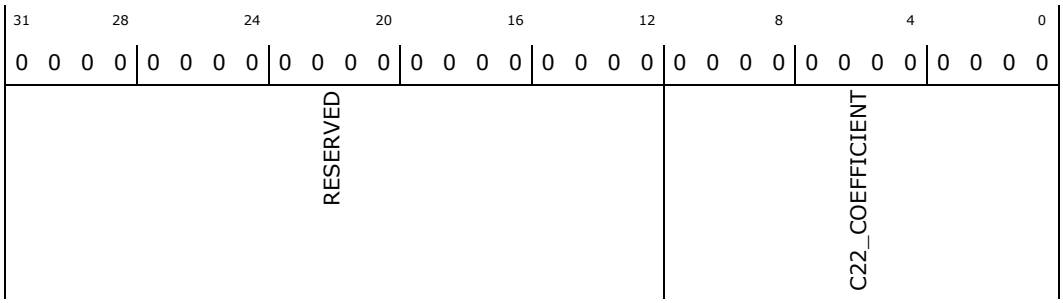
4.2.243 PIPEBWIDEGAMUTCOLORCORRECTIONC22COEFFICIENT—Offset 610C4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 610C4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RESERVED:** Reserved.
11:0	0x0 RW	**C22_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

4.2.244 ADPA—Offset 61100h

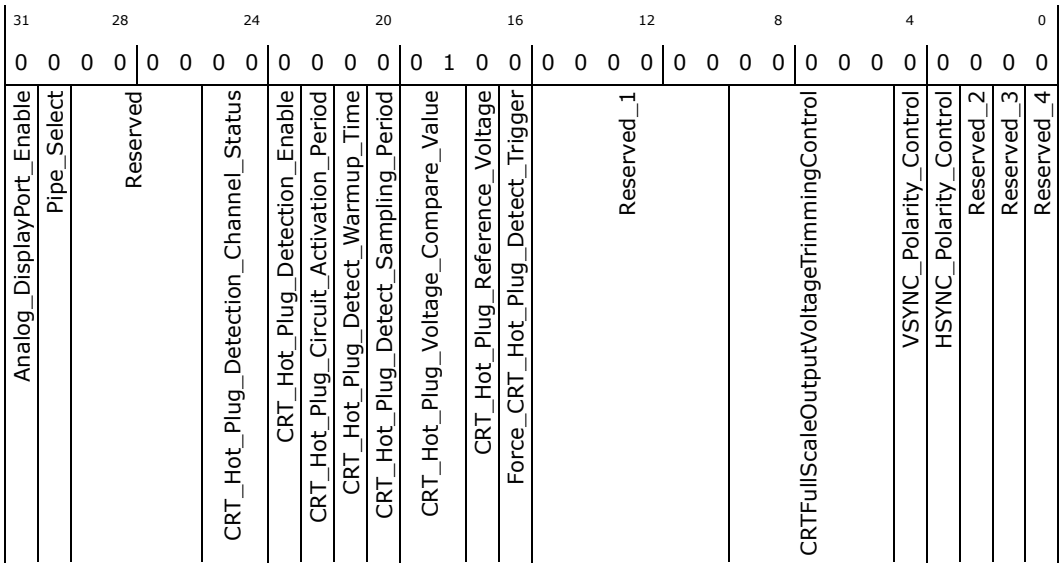
Analog Display Port Register CRT port control (dprrega.v adp_Q)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61100h

Default: 00040000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Analog_DisplayPort_Enable:** Project: All Default Value: 0b This bit enables or disables the analog port CRT DAC and syncs outputs. Value Name Description Project 0b Disable Disable the analog port DAC and disable output of syncs All 1b Enable Enable the analog port DAC and enable output of syncs All
30	0x0 RW	**Pipe_Select:** Project: All Default Value: 0b Determines which pipe output will feed this DAC port. Value Name Description Project 0b Pipe A Pipe A All 1b Pipe B Pipe B All
29:26	0x0 RO	**Reserved:** Project: All Format:

Bit Range	Default & Access	Field Name (ID): Description
25:24	0x0 RO	**CRT_Hot_Plug_Detection_Channel_Status:** Project: All AccessType: Read Only Default Value: 00b These bits are set when a CRT hot plug or unplug event has been detected and indicate which color channels were attached. Write a one to these bits to clear the status. The rising or falling edges of these bits are ORed together to go to the main ISR CRT hot plug register bit. Value Name Description Project 00b None No channels attached All 01b Blue Blue channel only is attached All 10b Green Green channel only is attached All 11b Both Both blue and green channel attached All
23	0x0 RW	**CRT_Hot_Plug_Detection_Enable:** Project: All Default Value: 0b Hot plug detection is used to set status bits or an interrupt on the connection or disconnection of a CRT to the analog display port. Value Name Description Project 0b Disable CRT hot plug detection is disabled All 1b Enable CRT hot plug detection is enabled All
22	0x0 RW	**CRT_Hot_Plug_Circuit_Activation_Period:** Project: All Default Value: 0b This bit sets the activation period for the CRT hot plug circuit. Value Name Description Project 0b 64 cdclk 64 cdclk periods All 1b 128 cdclk 128 cdclk periods All
21	0x0 RW	**CRT_Hot_Plug_Detect_Warmup_Time:** Project: All Default Value: 0b This bit sets the warmup time for the CRT hot plug circuit. Value Name Description Project 0b 2M pcdclks 2M pcdclks warmup (approximately 5ms) All 1b 4M pcdclks 4M pcdclks warmup (approximately 10ms) All
20	0x0 RW	**CRT_Hot_Plug_Detect_Sampling_Period:** Project: All Default Value: 0b This bit determines the length of time between sampling periods when the transcoder is disabled. Value Name Description Project 0b 1G pcdclks 1G pcdclks (approximately 2 seconds) All 1b 2G pcdclks 2G pcdclks (approximately 4 seconds) All
19:18	0x1 RW	**CRT_Hot_Plug_Voltage_Compare_Value:** Project: All Default Value: 01b A0 Compare value for Vref to determine whether the analog port is connected to a CRT. Value Name Description Project 00b 80 80 All 01b A0 A0 (Default) All 10b C0 C0 All 11b E0 E0 (bit 17 must be = 1) All
17	0x0 RW	**CRT_Hot_Plug_Reference_Voltage:** Project: All Default Value: 0b Value Name Description Project 0b 325mv 325mv All 1b 475mv 475mv (bits 19:18 must be = 11) All

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW	**Force_CRT_Hot_Plug_Detect_Trigger:** Project: All Default Value: 0b Triggers a CRT hotplug/unplug detection cycle independent of the hot plug detection enable bit. This bit is automatically cleared after the detection is completed. The result of this trigger is reflected in the CRT Hot Plug Detection Status. Software must reset status after a force CRT detect trigger. Value Name Description Project 0b No Trigger No Trigger All 1b Force Trigger Force Trigger All
15:10	0x0 RO	**Reserved_1:** Project: All Format:
9:5	0x0 RW	**CRTFullScaleOutputVoltageTrimmingControl:** Project: All Default Value: 0b This controls CRT output voltage trimming to ensure the output voltage is withing VESA spec.
4	0x0 RW	**VSYNC_Polarity_Control:** Project: All Default Value: 0b The output VSYNC polarity is controlled by this bit. This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the VSYNC signal. Value Name Description Project 0b Low Active Low All 1b High Active High All
3	0x0 RW	**HSYNC_Polarity_Control:** Project: All Default Value: 0b The output HSYNC polarity is controlled by this bit. This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the HSYNC signal. Value Name Description Project 0b Low Active Low All 1b High Active High All
2	0x0 RO	**Reserved_2:** Project: All Forma
1	0x0 RW	**Reserved_3:** Project: All Forma Monochrome Enable: If the CRT display is a monochrom type, SW driver shall set this bit to enable the CRT circuit to drive only the green channel to CRT and gate off the red and blue channels. 0 = Monochrome disabled (default) 1 = Monochrome enabled
0	0x0 RO	**Reserved_4:** Project: All Forma Monochrome Enable: If the CRT display is a monochrom type, SW driver shall set this bit to enable the CRT circuit to drive only the green channel to CRT and gate off the red and blue channels. 0 = Monochrome disabled (default) 1 = Monochrome enabled 0 = 1.35V is used for analog supply voltage (default) 1 = 1.25V is used for analog supply voltage

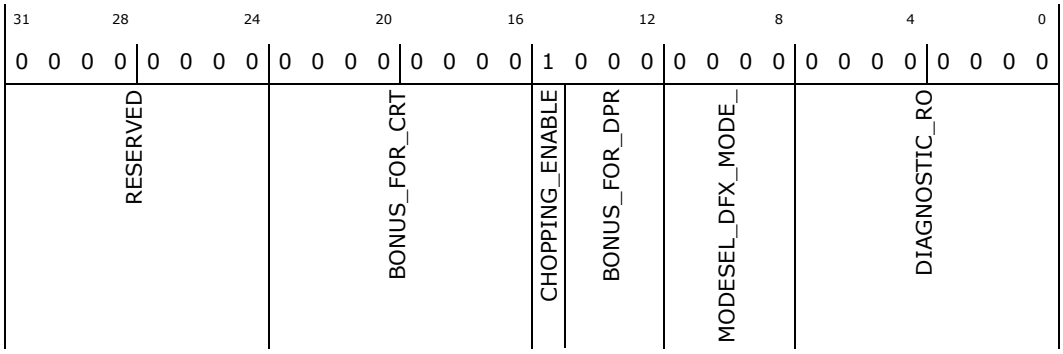
4.2.245 CRTIO_DFX—Offset 61104h

CRT port control (dprrega.v crt_dfx)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61104h

Default: 00008000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** read as zero
23:16	0x0 RW	**BONUS_FOR_CRT:** Reserved.
15	0x1 RW	**CHOPPING_ENABLE:** Chopping enable (for BG circuit)
14:12	0x0 RW	**BONUS_FOR_DPR:** Reserved.
11:8	0x0 RW	**MODESEL_DFX_MODE_:** Reserved.
7:0	0x0 RO	**DIAGNOSTIC_RO:** Observe signals at CRTIO AccessType: Read Only

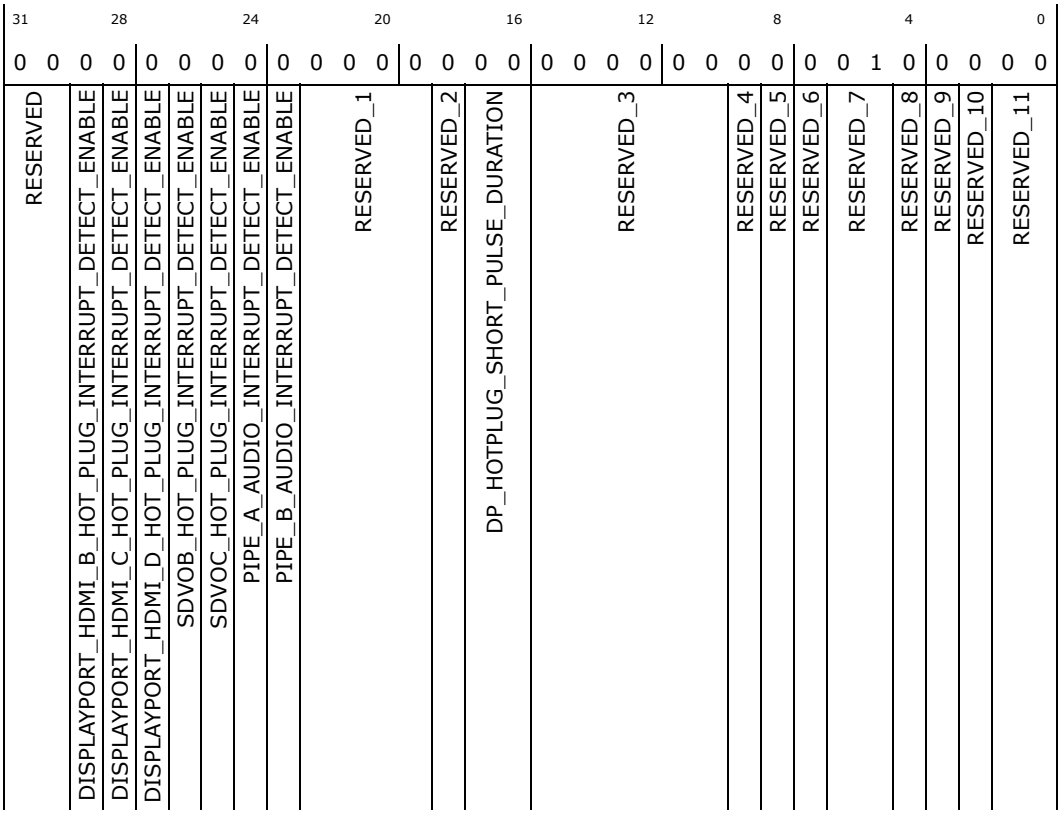
4.2.246 PORT_HOTPLUG_EN—Offset 61110h

DPD enable control (dprrega.v ql_hotplugen_Q)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61110h

Default: 00000020h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RESERVED:** mbz
29	0x0 RW	**DISPLAYPORT_HDMI_B_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** This will enable the consideration of the hot plug interrupt status bit for DisplayPort B in the Port Hotplug Status register, offset 61114h. Please note that software must set this bit at boot in order to detect the HPD input buffer live state. Since setting this bit may generate an interrupt, it must not be cleared and reset as part of interrupt processing. 0 = DisplayPort or HDMIB Hot Plug Detect Disabled (Default) 1 = DisplayPort or HDMIB Hot Plug Detect Enabled
28	0x0 RW	**DISPLAYPORT_HDMI_C_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** This will enable the consideration of the hot plug interrupt status bit for DisplayPort C in the Port Hotplug Status register, offset 61114h. Please note that software must set this bit at boot in order to detect the HPD input buffer live state. Since setting this bit may generate an interrupt, it must not be cleared and reset as part of interrupt processing. 0 = DisplayPort or HDMIC Hot Plug Detect Disabled (Default) 1 = DisplayPort or HDMIC Hot Plug Detect Enabled

Bit Range	Default & Access	Field Name (ID): Description
27	0x0 RW	**DISPLAYPORT_HDMI_D_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** [DevCTG] This will enable the consideration of the hot plug interrupt status bit for DisplayPort D in the Port Hotplug Status register, offset 61114h. Please note that software must set this bit at boot in order to detect the HPD input buffer live state. Since setting this bit may generate an interrupt, it must not be cleared and reset as part of interrupt processing. 0 = DisplayPort or HDMID Hot Plug Detect Disabled (Default) 1 = DisplayPort or HDMID Hot Plug Detect Enabled
26	0x0 RW	**SDVOB_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** [DevCTG] This will enable the consideration of the hot plug interrupt status bit in the Port Hotplug Status register, offset 61114h. This bit enables detection on the SDVOB interrupt input pin pair. 0 = SDVOB Hot Plug Detect Disabled (Default) 1 = SDVOB Hot Plug Detect Enabled
25	0x0 RW	**SDVOC_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** [DevCTG] This will enable the consideration of the hot plug interrupt status bit in the Port Hotplug Status register, offset 61114h. This bit enables detection on the SDVOC interrupt input pin pair. 0 = SDVOC Hot Plug Detect Disabled (Default) 1 = SDVOC Hot Plug Detect Enabled
24	0x0 RW	**PIPE_A_AUDIO_INTERRUPT_DETECT_ENABLE:** This bit enables consideration of the pipe A audio interrupt status bit in the Port Hotplug Status Register, offset 61114h. It relates to the HDMI port that has audio enabled and can only be used in combination with TMDS encoding. This bit is only to be used for integrated HDMI. 0 = Audio interrupt detect disabled (Default) 1 = Audio interrupt detect enabled
23	0x0 RW	**PIPE_B_AUDIO_INTERRUPT_DETECT_ENABLE:** This bit enables consideration of the pipe B audio interrupt status bit in the Port Hotplug Status Register, offset 61114h. It relates to the HDMI port that has audio enabled and can only be used in combination with TMDS encoding. This bit is only to be used for integrated HDMI. 0 = Audio interrupt detect disabled (Default) 1 = Audio interrupt detect enabled
22:19	0x0 RW	**RESERVED_1:** mbz
18	0x0 RW	**RESERVED_2:** MBZ TV Hot Plug Detect Interrupt Enable: [DevCL, DevCTG] This will enable the consideration of the TV hot plug interrupt status bit. 0 = TV Hot Plug Detect Disabled (bit 10 of the port hotplug status register no longer detects interrupts, Default) 1 = TV Hot Plug Detect Enabled
17:16	0x0 RW	**DP_HOTPLUG_SHORT_PULSE_DURATION:** These bits define the duration of the pulse defined as a short pulse for DisplayPort ports. 00 = 2mS (Default) 01 = 4.5mS 10 = 6mS 11 = 100mS
15:10	0x0 RO	**RESERVED_3:** mbz

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RW	**RESERVED_4:** MBZ. This bit is the same as bit 23 in 61100h CRT Hot plug Interrupt Enable: Hotplug detection is used to cause an interrupt or status bit based on the connection or disconnection of a CRT to the analog video connection. 0 = No hot plug interrupt is enabled (Default) 1 = Hot plug detection is enabled
8	0x0 RW	**RESERVED_5:** MBZ. This bit is the same as bit 22 in 61100h CRT Hot plug Circuit Activation Period: This bit sets the activation period for the CRT hot plug circuit detection. Setting this bit to 1 is required for the correct operation of CRT DAC detection. 0 = 32 cdclk periods (Default) 1 = 64 cdclk periods
7	0x0 RW	**RESERVED_6:** MBZ. This bit is the same as bit 21 in 61100h CRT DAC on time Value: Powerup time for 0 = CRT DAC requires 2M cdclks for warmup (Default) 1 = CRT DAC requires 4M cdclks for warmup
6:5	0x1 RW	**RESERVED_7:** MBZ. This bit is the same as bit 19:18 in 61100h CRT Hot plug Voltage Compare Value: Compare value for CRT hotplug detect Vref to determine whether the analog port is connected to a CRT. The voltage is forced at the beginning of the active region of the screen every 2 seconds. 00 = A0, 01 = B0, (Default) 10 = C0 11 = D0
4	0x0 RW	**RESERVED_8:** MBZ. This bit is the same as bit 20 in 61100h CRT Hot Plug Detect Delay: This bit determines the length of time between polling periods when the DAC/pipe are disabled 0 = 1G cdclks (default) 1 = 2G cdclks
3	0x0 RW	**RESERVED_9:** MBZ Force CRT detect trigger: Triggers a CRT hotplug/unplug detection cycle independent of the interrupt enable bit. Bits 5:8 of this register must be correctly programmed when forcing a trigger. This bit is automatically cleared after the detection is completed. The result of this trigger is reflected in bits 9:8 of the port hotplug interrupt status register. The CRT interrupt status bit #11 in the hot plug status register (61114) will get set the first time Force CRC detect trigger is used after reset. Software must reset status after a force CRT detect trigger. 0 = No trigger (Default) 1 = Trigger
2	0x0 RW	**RESERVED_10:** MBZ. This bit is the same as bit 17 in 61100h [DevCTG-B] CRT DAC hot plug detection reference voltage selection: 0 = 325mv, bits[6:5] should be set to 01 (Default) 1 = 475mv, bits[6:5] should be set to 11
1:0	0x0 RW	**RESERVED_11:** mbz

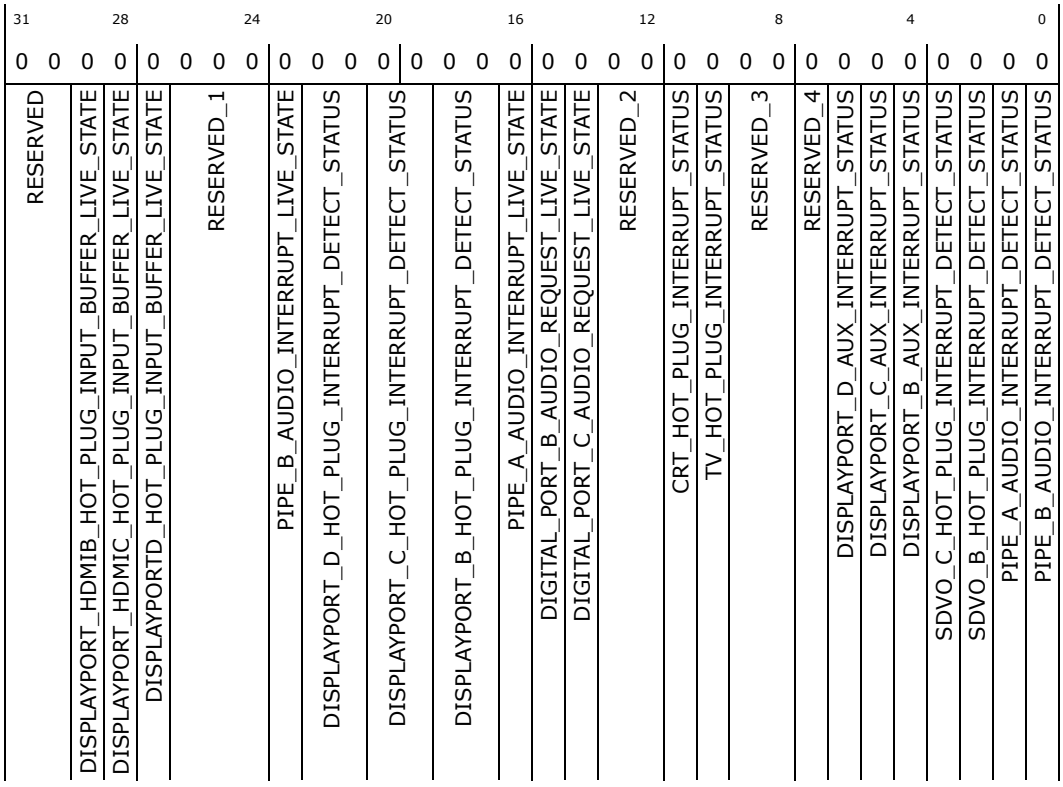
4.2.247 PORT_HOTPLUG_STAT—Offset 61114h

CRT port control (dprrega.v porthotst_aR)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61114h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RESERVED:** mbz
29	0x0 RO	**DISPLAYPORT_HDMIB_HOT_PLUG_INPUT_BUFFER_LIVE_STATE:** This bit is read-only. It reflects the real-time state of the of the hot plug input (HPD pin) on DisplayPort or HDMI B when bit 29 of the hotplug enable register, offset 61110h is set. This pin signal is active high. This does not feed into the first line interrupt status register. This bit should be read to confirm cable connection prior to attempting EDID read. 1 = HPD detected active 0 = HPD detected inactive AccessType: Read Only
28	0x0 RO	**DISPLAYPORT_HDMIC_HOT_PLUG_INPUT_BUFFER_LIVE_STATE:** This bit is read-only. It reflects the real-time state of the of the hot plug input (HPD pin) on DisplayPortC when bit of this register is set. This pin signal is active high. This does not feed into the first line interrupt status register. This bit should be read to confirm cable connection prior to attempting EDID read. 1 = HPD detected high 0 = HPD detected low AccessType: Read Only

Bit Range	Default & Access	Field Name (ID): Description
27	0x0 RO	**DISPLAYPORTD_HOT_PLUG_INPUT_BUFFER_LIVE_STATE:** [DevCTG] This bit is read-only. It reflects the real-time state of the of the hot plug input (HPD pin) on DisplayPortD when bit of this register is set. This pin signal is active high. This does not feed into the first line interrupt status register. Please note that port D is intended for LFP use and therefore HPD may not be present. Bit 2 of the DPD control register must therefore be read to determine whether DPD is used in the system. 1 = HPD detected high 0 = HPD detected low AccessType: Read Only
26:24	0x0 RO	**RESERVED_1:** mbz
23	0x0 RO	**PIPE_B_AUDIO_INTERRUPT_LIVE_STATE:** This read-only bit is used only in ports that use TMDS encoding. It reflects the state of the pipe B audio interrupt request for HDCP when bit 1 of this register is set. This pin signal is active high. It does not feed into the first line interrupt status register. 1 = HDCP invocation requested from audio 0 = HDCP disable requested from audio AccessType: Read Only
22:21	0x0 RW/1C	**DISPLAYPORT_D_HOT_PLUG_INTERRUPT_DETECT_STATUS:** [DevCTG] This reflects hot plug interrupt status on DisplayPort D. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. This bit feeds into the first line interrupt status register when bit 27 of the hotplug enable status register is set. 00 = DisplayPort D Hot Plug event not detected 1x = DisplayPort D long pulse Hot Plug event detected X1 = DisplayPort D short pulse Hot Plug event detected AccessType: One to Clear
20:19	0x0 RW/1C	**DISPLAYPORT_C_HOT_PLUG_INTERRUPT_DETECT_STATUS:** This reflects hot plug interrupt status on DisplayPort or HDMI C. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. This bit feeds into the first line interrupt status register when bit 28 of the hotplug enable status register is set. Please note that these bits should be considered in conjunction with bit 28, the hot plug input buffer live state, when determining further action: if bit 28 = 0, the bits should be cleared and the port must be disabled. 00 = DisplayPort/HDMI C Hot Plug event not detected 1x = DisplayPort/HDMI C long pulse Hot Plug event detected X1 = DisplayPort C short pulse Hot Plug event detected AccessType: One to Clear

Bit Range	Default & Access	Field Name (ID): Description
18:17	0x0 RW/1C	**DISPLAYPORT_B_HOT_PLUG_INTERRUPT_DETECT_STATUS:** This reflects hot plug interrupt status on DisplayPort B. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. This bit feeds into the first line interrupt status register when bit 29 of the hotplug enable status register is set. Please note that these bits should be considered in conjunction with bit 29, the hot plug input buffer live state, when determining further action: if bit 29 = 0, the bits should be cleared and the port must be disabled. 00 = DisplayPort/HDMI B Hot Plug event not detected 1x = DisplayPort/HDMI B long pulse Hot Plug event detected X1 = DisplayPort B short pulse Hot Plug event detected AccessType: One to Clear
16	0x0 RO	**PIPE_A_AUDIO_INTERRUPT_LIVE_STATE:** This read-only bit is used only in ports that use TMDS encoding. It reflects the state of the pipe A audio interrupt request for HDCP when bit 1 of this register is set. This pin signal is active high. It does not feed into the first line interrupt status register. 1 = HDCP invocation requested from audio 0 = HDCP disable requested from audio AccessType: Read Only
15	0x0 RO	**DIGITAL_PORT_B_AUDIO_REQUEST_LIVE_STATE:** This read-only bit is only used on ports using audio. It reflects the state of audio HDCP request when bit 17 of this register is set if audio is enabled on this port. This pin signal is active high. This does not feed into the first line interrupt status register. 1 = HDCP invocation requested from audio 0 = HDCP disable requested from audio AccessType: Read Only
14	0x0 RO	**DIGITAL_PORT_C_AUDIO_REQUEST_LIVE_STATE:** This read-only bit is only used on ports using audio. It reflects the state of audio HDCP request when bit 19 of this register is set if audio is enabled on this port. This pin signal is active high. This does not feed into the first line interrupt status register. 1 = HDCP invocation requested from audio 0 = HDCP disable requested from audio AccessType: Read Only
13:12	0x0 RO	**RESERVED_2:** mbz
11	0x0 RW/1C	**CRT_HOT_PLUG_INTERRUPT_STATUS:** This bit is set when a CRT hot plug or unplug event has been detected. A hot plug or unplug event is defined as the change in connection state of the CRT as determined by the hardware CRT detect sequence which is enabled through bit #9 (CRT hot plug interrupt enable) or bit #3 (Force CRT detect trigger) in the Port_HotPlug_En register 0x61110. After reset, the CRT is considered unconnected even if physically connected until the first detect sequence occurs. Physically plugging or unplugging the CRT device will also be detected as a change of connection state. Writing a 1 to this bit clears it. 0 =CRT Interrupt has not occurred 1 = CRT Interrupt has occurred AccessType: One to Clear

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RW/1C	**TV_HOT_PLUG_INTERRUPT_STATUS:** [DevCTG, DevBW, DevCL, DevBLC] This bit is set when a TV hot plug or unplug event has been detected. Reflects the state of bit 31 of the TV DAC state register, offset 68004-68007h. Software must write a one to these bits to clear the status. 0 =TV Interrupt has not occurred 1 = TV Interrupt has occurred AccessType: One to Clear
9:8	0x0 RO	**RESERVED_3:** MBZ. These info are recorded in 61100h ADPA register[25:24] CRT Hot Plug Detection Status (read only): These bits are set when a CRT hot plug or unplug event has been detected. 00 = No channels attached (default) 01 = Blue channel only is attached 10 = Green channel only is attached 11 = Both blue and green channel attached AccessType: One to Clear
7	0x0 RO	**RESERVED_4:** mbz
6	0x0 RW/1C	**DISPLAYPORT_D_AUX_INTERRUPT_STATUS:** [DevCTG] This bit is set when a transaction on AUX channel D has completed or timed out. This bit feeds into the first line interrupt status register when bit 29 of the AUX channel D control register is set. Writing a 1 to this bit clears it. 0 = AUX channel D Interrupt has not occurred 1 = AUX channel D Interrupt has occurred AccessType: One to Clear
5	0x0 RW/1C	**DISPLAYPORT_C_AUX_INTERRUPT_STATUS:** This bit is set when a transaction on AUX channel C has completed or timed out. This bit feeds into the first line interrupt status register when bit 29 of the AUX channel C control register is set. Writing a 1 to this bit clears it. 0 = AUX channel C Interrupt has not occurred 1 = AUX channel C Interrupt has occurred AccessType: One to Clear
4	0x0 RW/1C	**DISPLAYPORT_B_AUX_INTERRUPT_STATUS:** This bit is set when a transaction on AUX channel B has completed or timed out. This bit feeds into the first line interrupt status register when bit 29 of the AUX channel B control register is set. Writing a 1 to this bit clears it. 0 = AUX channel B Interrupt has not occurred 1 = AUX channel B Interrupt has occurred AccessType: One to Clear
3	0x0 RW/1C	**SDVO_C_HOT_PLUG_INTERRUPT_DETECT_STATUS:** This reflects hot plug interrupt status on SDVO port C. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/ unplug or for notification of an HDCP state change request from the audio driver over SDVO only. This bit feeds into the first line interrupt status register when bit 25 of the hotplug enable status register is set. 0 = SDVO Hot Plug event not detected 1 = SDVO Hot Plug event detected AccessType: One to Clear

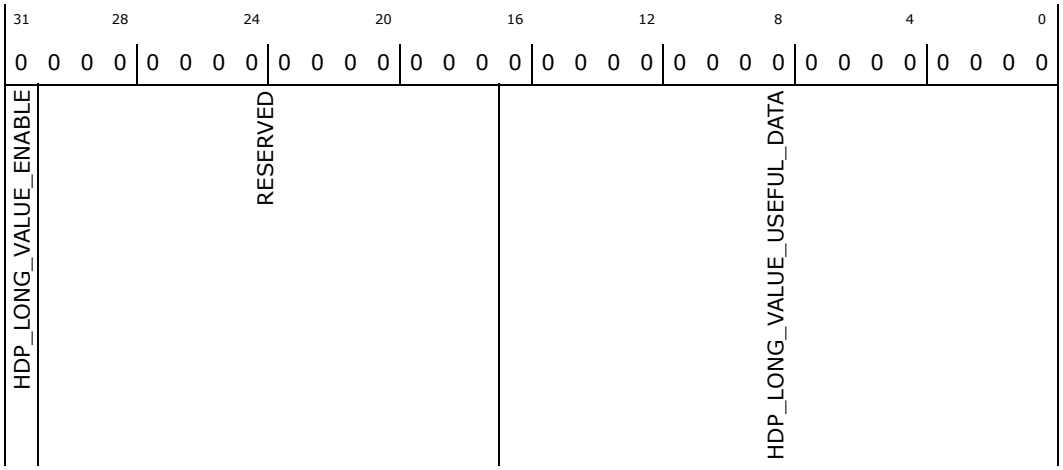
Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW/1C	**SDVO_B_HOT_PLUG_INTERRUPT_DETECT_STATUS:** This reflects hot plug interrupt status on SDVO port B. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/ unplug or for notification of an HDCP state change request from the audio driver over SDVO only. This bit feeds into the first line interrupt status register when bit 26 of the hotplug enable status register is set. 0 = SDVO Hot Plug event not detected 1 = SDVO Hot Plug event detected AccessType: One to Clear
1	0x0 RW/1C	**PIPE_A_AUDIO_INTERRUPT_DETECT_STATUS:** This reflects a request for integrated HDCP state change set by audio driver and propagated through the audio hardware. The graphics software must write a one to this bit to clear the status. Upon clearing this bit, the audio ready bit is cleared in the audio registers. The graphics software then must reset audio ready bit 14 in the audio control register, offset 620B4h to 1 when the HDCP interrupt has been serviced. This bit feeds into the first line interrupt status register when bit 24 of the hotplug enable status register is set 0 = Audio interrupt event not detected 1 = Audio interrupt event detected AccessType: One to Clear
0	0x0 RW/1C	**PIPE_B_AUDIO_INTERRUPT_DETECT_STATUS:** This reflects a request for integrated HDCP state change set by audio driver and propagated through the audio hardware. The graphics software must write a one to this bit to clear the status. Upon clearing this bit, the audio ready bit is cleared in the audio registers. The graphics software then must reset audio ready bit 14 in the audio control register, offset 620B4h to 1 when the HDCP interrupt has been serviced. This bit feeds into the first line interrupt status register when bit 23 of the hotplug enable status register is set 0 = Audio interrupt event not detected 1 = Audio interrupt event detected AccessType: One to Clear

4.2.248 HDP_LONG_VALUE_REGISTER—Offset 61120h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61120h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**HDP_LONG_VALUE_ENABLE:**
30:17	0x0 RW	**RESERVED:** Reserved.
16:0	0x0 RW	**HDP_LONG_VALUE_USEFUL_DATA:** Reserved.

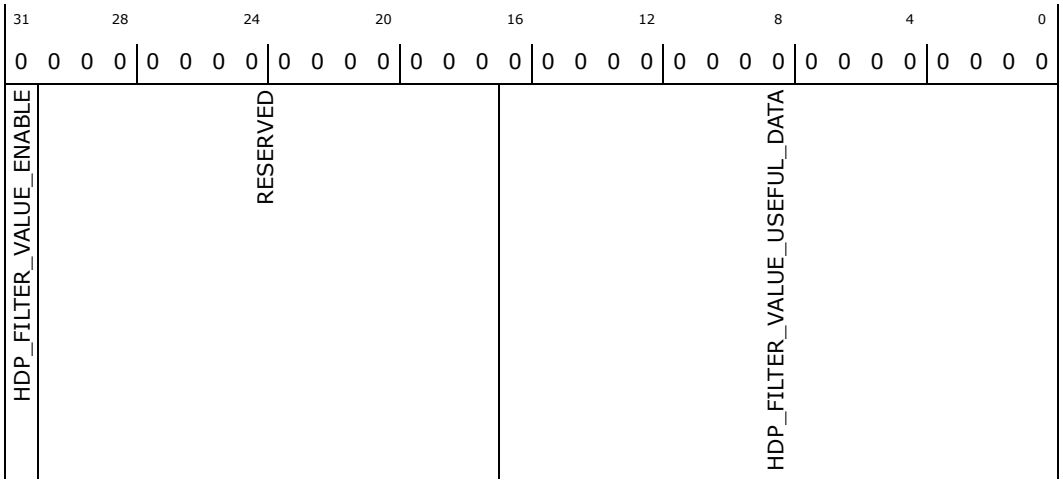
4.2.249 HDP_FILTER_VALUE_REGISTER—Offset 61124h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61124h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**HDP_FILTER_VALUE_ENABLE:**
30:17	0x0 RW	**RESERVED:** Reserved.
16:0	0x0 RW	**HDP_FILTER_VALUE_USEFUL_DATA:** Reserved.

4.2.250 SDVOHDMIB—Offset 61140h

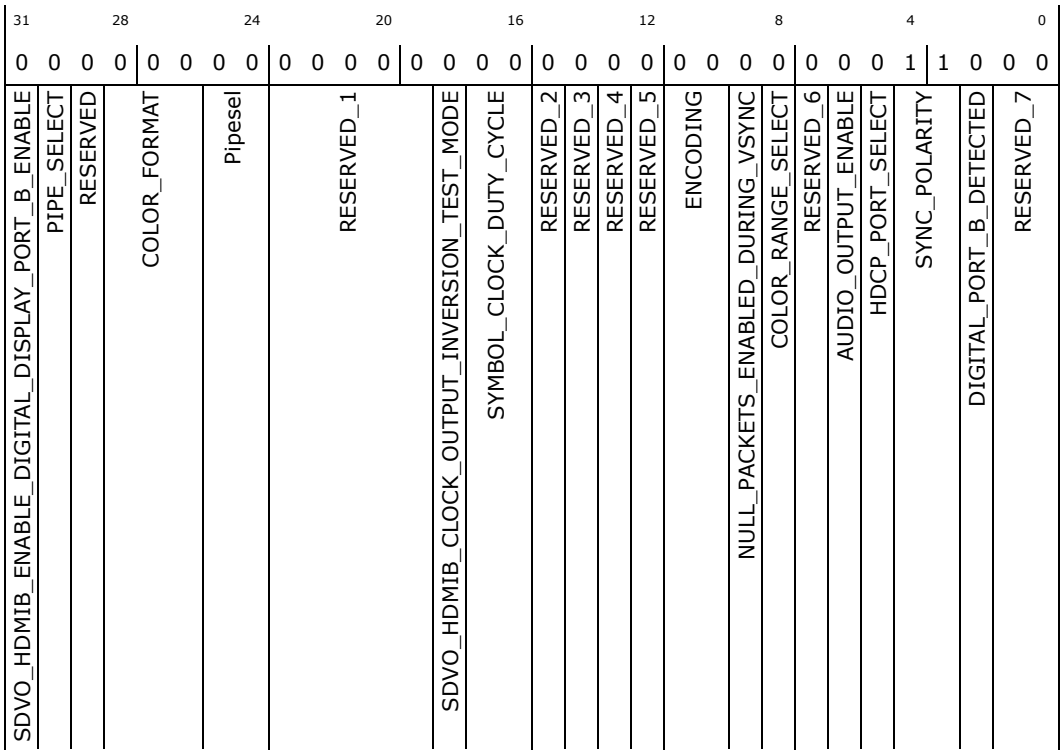
Digital Display Port B Control Register HDMIB port control (dprrega.v sdvo_bQ)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61140h

Default: 00000018h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SDVO_HDMIB_ENABLE_DIGITAL_DISPLAY_PORT_B_ENABLE:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and bit 6 of this register must be enabled to send audio over this port. This port must not be enabled simultaneously with DisplayPort B. [DevIBX] When disabling the port, software must temporarily enable the port with transcoder select (bit #30) cleared to 0 after disabling the port. This is workaround for hardware issue where the transcoder select set to 1 will prevent DisplayPortB from being enabled on transcoder A. [DevIBX] Software must write this bit twice when enabling the port (setting to 1) as a workaround for hardware issue that may result in first write getting masked. [DevIBX] Toggle this bit off then on at the end of mode set sequence when enabling HDMI 12-bit per color with pixel repeat 1 = Enable. This bit enables the Digital Display Port B interface for HDMI or SDVO modes. 0 = Disable and tristates the Digital Display Port B interface for HDMI or SDVO modes.
30	0x0 RW	**PIPE_SELECT:** This bit determines from which display pipe the source data will originate. This only applies to devices with dual display pipes. Pipe selection takes place on the Vblank after being written 0 = Pipe A 1 = Pipe B
29	0x0 RW	**RESERVED:** : [DevCTG, DevBW, DevCL, DevBLC] Stall Select: This bit selects stall for external scaling functionality only on SDVO. Programming notes: It is only valid to have a single stall indication to a particular pipe. In cases where two ports are being driven from a single pipe, one of the ports must set this bit to 0. Only sDVOB or sDVOC can select the stall function, as only a single stall input is available between the two interfaces. Set the stall input to unused before programming the external device creating the stall. 0 = Stall input signal is unused on this port 1 = Stall input signal is used to stall the pipe attached to this port
28:26	0x0 RW	**COLOR_FORMAT:** This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change must be done as a part of mode set since different color depths require different pixel clock settings. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. 000 = 8 bits per color (Default, x3 mode) 001 = RESERVED for 10 bits per color 010 = RESERVED for 6 bits per color 011 = RESERVED 1xx = RESERVED
25:24	0x0 RW	**PipeSel (Pipesel):** Reserved.
23:19	0x0 RO	**RESERVED_1:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
18	0x0 RW	**SDVO_HDMIB_CLOCK_OUTPUT_INVERSION_TEST_MODE:** Please note that this applies to all modes and is instantly updated. 1 = sDVO/HDMIB Clock output is inverted 0 = sDVO/HDMIB Clock output is NOT inverted (DEFAULT)
17:16	0x0 RW	**SYMBOL_CLOCK_DUTY_CYCLE:** These bits control the output clock duty cycle to enable EMI mitigation on the external UDI link. 10/90 cycle has been measured to have ~13dB EMI improvement over a 50/50 duty cycle. 00 = (Default) 50/50 duty cycle: Clock output is 0000011111 01 = 10/90 duty cycle: Clock output is 0111111111 followed by 0000000001 10 = 20/80 duty cycle: Clock output is 0011111111 followed by 0000000011 11 = Reserved
15	0x0 RW	**RESERVED_2:** Port Lane Reversal: This bit reverses the order of the 4 lanes within the port. Port lane reversal takes place on the Vblank after being written. It is an OEM configurable feature. 0 = (Default) Not reversed 1 = Reversed
14	0x0 RO	**RESERVED_3:** Reserved.
13	0x0 RW	**RESERVED_4:** Clock Output Disable: This bit disables the clock output on the digital output port. For 8b/10b modes the clock output should be disabled. 0 = (Default) Clock output enabled 1 = Clock output disabled
12	0x0 RW	**RESERVED_5:** Scrambling enable: This bit enables scrambling for UDI-related modes using ANSI 8b/10b or TMDS encoding. It is not used with SDVO encoding. Software must set this bit appropriately when enabling the port. Scrambling is reset at the beginning of horizontal sync. 0 = Scrambling disabled (Default) 1 = Scrambling enabled
11:10	0x0 RW	**ENCODING:** These bits select among encoding types. It is set as part of the display detection process. Control codes for ANSI 8b/10b and TMDS encoding must be programmed using these bits. Please note that ANSI 8b/10b and TMDS encoding can only be enabled on one port at a time, as only one HPD pin is available for use between ports B and C. 00 = Reserved 01 = Reserved 10 = TMDS encoding (external link and HDMI only) Refer the HDMI specification for control codes. In this mode, the external HPD pin is used to generate hotplug. In fixed frequency mode, start of fill and end of fill values for TMDS must be programmed using register 6114C. 11 = Reserved
9	0x0 RW	**NULL_PACKETS_ENABLED_DURING_VSYNC:** This bit enables a null packet (32 bytes of a value of 0) to be sent when Vsync=1 on this port, required for HDMI operation. It also enables preambles and guardbands prior to the null packets, in accordance with the HDMI specification. It is only valid for modes that use TMDS encoding. 0 = Disable null infoframe packets when Vsync=1 on this port. (Default) 1 = Enable null infoframe packets when Vsync=1 on this port.

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**COLOR_RANGE_SELECT:** This bit is used to select the color range of RBG outputs in HDMI mode. It is only valid when using TMDS encoding and 8 bit per color mode. 0 = Apply full 0-255 color range to the output (Default) 1 = Apply 16-235 color range to the output
6	0x0 RW	**AUDIO_OUTPUT_ENABLE:** This bit directs audio to this port. When enabled and audio data is available, the audio data will be combined with the video data and sent over this port. The audio unit uses the status of this bit to indicate presence of the HDMI output to the audio driver. 0 = (Default) No audio output on this port 1 = Enable audio on this port
5	0x0 RW	**HDCP_PORT_SELECT:** This bit directs HDCP to this port. When enabled, the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own, but must be used in conjunction with HDCP registers. 0 = (Default) No HDCP encryption on this port 1 = Enable HDCP on this port
4:3	0x3 RW	**SYNC_POLARITY:** Please note that sync polarity does not apply to ANSI coding. Indicates the polarity of Hsync and Vsync. Inverted polarity is transmitted as SYNC-BLANK-SYNC and standard polarity is transmitted as BLANK-SYNC-BLANK. For example, if Vsync is not inverted and Hsync is inverted, an Hsync period transmitted during Vsync would be transmitted as BLANK+VS+HS BLANK+VS BLANK+VS+HS. 00 = VS and HS are active low (inverted) 01 = VS is active low (inverted), HS is active high 10 = VS is active high, HS is active low (inverted) 11 = (Default) VS and HS are active high
2	0x0 RO	**DIGITAL_PORT_B_DETECTED:** Read-only bit indicating whether a digital port B was detected during initialization. It signifies the level of the GMBUS port 4 (sDVO B/C) data line at boot. This bit is valid regardless of whether the port is enabled. 0 = Digital Port B not detected during initialization 1 = Digital Port B detected during initialization AccessType: Read Only
1:0	0x0 RO	**RESERVED_7:** MBZ

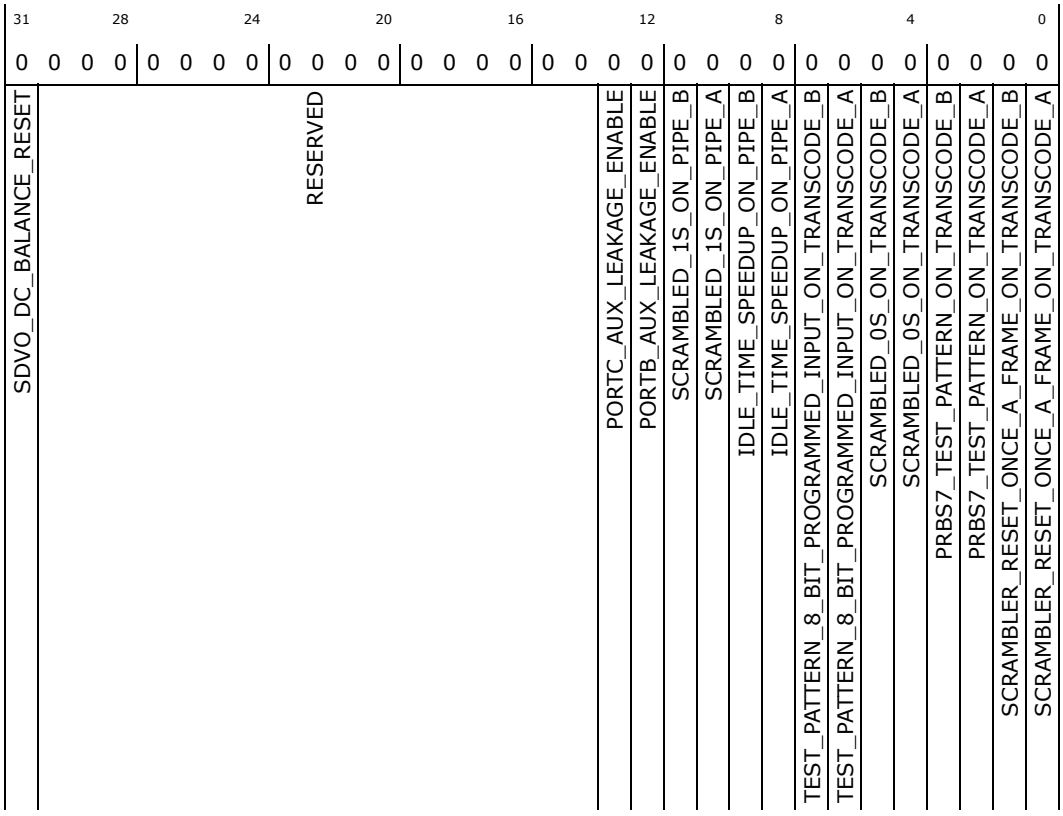
4.2.251 SDVO—Offset 61154h

DP2 - Digital Port DFT Register ;

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61154h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SDVO_DC_BALANCE_RESET:** Project: All Format: Value Name Description Project 0b Not Reset DC Balance circuitry will not be reset on every frame All 1b Reset DC Balance circuitry will be reset on every frame All
30:14	0x0 RO	**RESERVED:** Project: All Format: MBZ
13	0x0 RW	**PORTC_AUX_LEAKAGE_ENABLE:** Project: All Format:
12	0x0 RW	**PORTB_AUX_LEAKAGE_ENABLE:** Project: All Format:
11	0x0 RW	**SCRAMBLED_1S_ON_PIPE_B:** Project: All Format: Value Name Description Project 0b Disable Disable scrambled 1s All 1b Enable Enable scrambled 1s All
10	0x0 RW	**SCRAMBLED_1S_ON_PIPE_A:** Project: All Format: Value Name Description Project 0b Disable Disable scrambled 1s All 1b Enable Enable scrambled 1s All

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RW	**IDLE_TIME_SPEEDUP_ON_PIPE_B:** Project: All Format: Value Name Description Project 0b Normal Normal idle time All 1b Speedup Speedup idle time All
8	0x0 RW	**IDLE_TIME_SPEEDUP_ON_PIPE_A:** Project: All Format: Value Name Description Project 0b Normal Normal idle time All 1b Speedup Speedup idle time All
7	0x0 RW	**TEST_PATTERN_8_BIT_PROGRAMMED_INPUT_ON_TRANSCODE_B:** Project: All Format: Value Name Description Project 0b Disable Disable the test pattern All 1b Enable Enable the test pattern All
6	0x0 RW	**TEST_PATTERN_8_BIT_PROGRAMMED_INPUT_ON_TRANSCODE_A:** Project: All Format: Value Name Description Project 0b Disable Disable the test pattern All 1b Enable Enable the test pattern All
5	0x0 RW	**SCRAMBLED_0S_ON_TRANSCODE_B:** Project: All Format: Value Name Description Project 0b Disable Disable the scramble 0s All 1b Enable Enable the scramble 0s All
4	0x0 RW	**SCRAMBLED_0S_ON_TRANSCODE_A:** Project: All Format: Value Name Description Project 0b Disable Disable the scramble 0s All 1b Enable Enable the scramble 0s All
3	0x0 RW	**PRBS7_TEST_PATTERN_ON_TRANSCODE_B:** Project: All Format: Value Name Description Project 0b Disable Disable the test pattern All 1b Enable Enable the test pattern All
2	0x0 RW	**PRBS7_TEST_PATTERN_ON_TRANSCODE_A:** Project: All Format: Value Name Description Project 0b Disable Disable the test pattern All 1b Enable Enable the test pattern All
1	0x0 RW	**SCRAMBLER_RESET_ONCE_A_FRAME_ON_TRANSCODE_B:** Project: All Format: Value Name Description Project 0b Disable Disable the scrambler reset once a frame All 1b Enable Enable the scrambler reset once a frame All
0	0x0 RW	**SCRAMBLER_RESET_ONCE_A_FRAME_ON_TRANSCODE_A:** All Format: Value Name Description Project 0b Disable Disable the scrambler reset once a frame All 1b Enable Enable the scrambler reset once a frame All

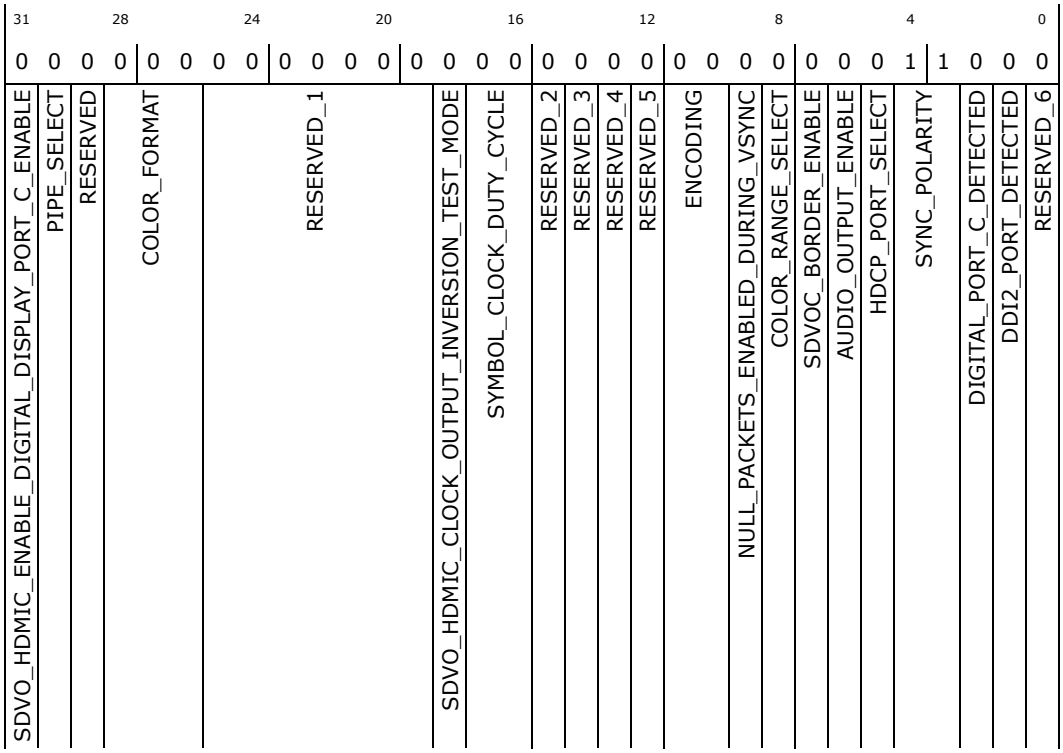
4.2.252 HDMIC—Offset 61160h

Digital Display Port C Register HDMIC port control (dprrega.v sdvo_cQ)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61160h

Default: 00000018h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SDVO_HDMIC_ENABLE_DIGITAL_DISPLAY_PORT_C_ENABLE:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and bit 6 of this register must be enabled to send audio over this port in HDMI. This port must not be enabled simultaneously with DisplayPort C. [DevIBX] When disabling the port, software must temporarily enable the port with transcoder select (bit #30) cleared to 0 after disabling the port. This is workaround for hardware issue where the transcoder select set to 1 will prevent DPC from being enabled on transcoder A. [DevIBX] Software must write this bit twice when enabling the port (setting to 1) as a workaround for hardware issue that may result in first write getting masked. [DevIBX] Toggle this bit off then on at the end of mode set sequence when enabling HDMI 12-bit per color with pixel repeat. 1 = Enable. This bit enables the Digital Display Port C interface for HDMI or DVI modes. 0 = Disable and tristates the Digital Display Port C interface for HDMI or DVI modes.

Bit Range	Default & Access	Field Name (ID): Description
30	0x0 RW	**PIPE_SELECT:** This bit determines from which display pipe the source data will originate. This only applies to devices with dual display pipes. Pipe selection takes place on the Vblank after being written 0 = Pipe A 1 = Pipe B
29	0x0 RO	**RESERVED:** : stall Select: This bit selects stall for external scaling functionality only on SDVO. Programming notes: It is only valid to have a single stall indication to a particular pipe. In cases where two ports are being driven from a single pipe, one of the ports must set this bit to 0. Only sDVOB or sDVOC can select the stall function, as only a single stall input is available between the two interfaces. Set the stall input to unused before programming the external device creating the stall. 0 = Stall input signal is unused on this port 1 = Stall input signal is used to stall the pipe attached to this port
28:26	0x0 RW	**COLOR_FORMAT:** This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change must be done as a part of mode set since different color depths require different pixel clock settings. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. 000 = 8 bits per color (Default) 001 = RESERVED for 10 bits per color 010 = RESERVED for 6 bits per color 011 = RESERVED 1xx = RESERVED
25:19	0x0 RO	**RESERVED_1:** Reserved.
18	0x0 RW	**SDVO_HDMIC_CLOCK_OUTPUT_INVERSION_TEST_MODE:** Please note that this applies to all modes and is instantly updated. 1 = sDVO/HDMIB Clock output is inverted 0 = sDVO/HDMIB Clock output is NOT inverted (DEFAULT)
17:16	0x0 RW	**SYMBOL_CLOCK_DUTY_CYCLE:** These bits control the output clock duty cycle to enable EMI mitigation on the external HDMI link. 10/90 cycle has been measured to have ~13dB EMI improvement over a 50/50 duty cycle. 00 = (Default) 50/50 duty cycle: Clock output is 0000011111 01 = 10/90 duty cycle: Clock output is 0111111111 followed by 0000000001 (HDMI only) 10 = 20/80 duty cycle: Clock output is 0011111111 followed by 0000000011 (HDMI only) 11 = Reserved
15	0x0 RO	**RESERVED_2:** Port Lane Reversal: This bit reverses the order of the 4 lanes within the port. Port lane reversal takes place on the Vblank after being written. It is an OEM configurable feature. 0 = (Default) Not reversed 1 = Reversed

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RO	**RESERVED_3:** Reserved.
13	0x0 RO	**RESERVED_4:** Clock Output Disable: This bit disables the clock output on the digital output port. For 8b/10b modes the clock output should be disabled. 0 = (Default) Clock output enabled 1 = Clock output disabled ([DevCL] only)
12	0x0 RO	**RESERVED_5:** Scrambling enable: This bit enables scrambling for UDI-related modes using ANSI 8b/10b or TMDS encoding. It is not used with SDVO encoding. Software must set this bit appropriately when enabling the port. Scrambling is reset at the beginning of horizontal sync. 0 Scrambling disabled (Default) 1 = Scrambling enabled ([DevCL] only)
11:10	0x0 RW	**ENCODING:** These bits select among encoding types. It is set as part of the display detection process. Control codes for ANSI 8b/10b and TMDS encoding must be programmed using these bits. Please note that ANSI 8b/10b and TMDS encoding can only be enabled on one port at a time, as only one HPD pin is available for use between ports B and C. 00 = Reserved 01 = Reserved 10 = TMDS encoding (external link and HDMI only) Refer the HDMI specification for control codes. In this mode, the external HPD pin is used to generate hotplug. In fixed frequency mode, start of fill and end of fill values for TMDS must be programmed using register 6114C. 11 = Reserved
9	0x0 RW	**NULL_PACKETS_ENABLED_DURING_VSYNC:** This bit enables a null packet (32 bytes of a value of 0) to be sent when Vsync=1 on this port, required for HDMI operation. It also enables preambles and guardbands prior to the null packets, in accordance with the HDMI specification. It is only valid for modes that use TMDS encoding. 0 = Disable null infoframe packets when Vsync=1 on this port. (Default) 1 = Enable null infoframe packets when Vsync=1 on this port.
8	0x0 RW	**COLOR_RANGE_SELECT:** This bit is used to select the color range of RBG outputs in HDMI mode. It is only valid when using TMDS encoding and 8 bit per color mode. 0 = Apply full 0-255 color range to the output (Default) 1 = Apply 16-235 color range to the output ([DevCL and DevCTG] only)
6	0x0 RW	**AUDIO_OUTPUT_ENABLE:** This bit directs audio to this port. When enabled and audio data is available, the audio data will be combined with the video data and sent over this port. The audio unit uses the status of this bit to indicate presence of the HDMI output to the audio driver. 0 = (Default) No audio output on this port 1 = Enable audio on this port
5	0x0 RW	**HDCP_PORT_SELECT:** This bit directs HDCP to this port. When enabled, the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own, but must be used in conjunction with HDCP registers. 0 = (Default) No HDCP encryption on this port 1 = Enable HDCP on this port

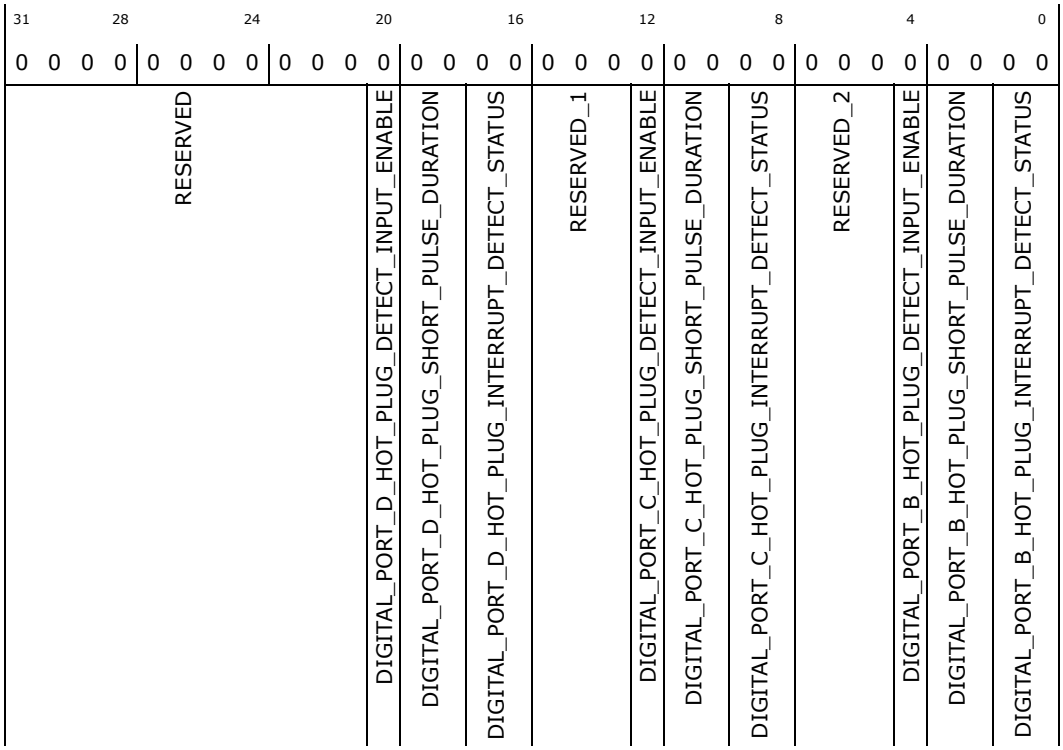
Bit Range	Default & Access	Field Name (ID): Description
4:3	0x3 RW	**SYNC_POLARITY:** Please note that sync polarity does not apply to ANSI coding. Indicates the polarity of Hsync and Vsync. Inverted polarity is transmitted as SYNC-BLANK-SYNC and standard polarity is transmitted as BLANK-SYNC-BLANK. For example, if Vsync is not inverted and Hsync is inverted, an Hsync period transmitted during Vsync would be transmitted as BLANK+VS+HS BLANK+VS BLANK+VS+HS. 00 = VS and HS are active low (inverted) 01 = VS is active low (inverted), HS is active high 10 = VS is active high, HS is active low (inverted) 11 = (Default) VS and HS are active high
2	0x0 RO	**DIGITAL_PORT_C_DETECTED:** Read-only bit indicating whether a digital port C was detected during initialization. It signifies the level of the GMBUS port 3 (port C) data line at boot. This bit is valid regardless of whether the port is enabled. 0 = Digital Port C not detected during initialization 1 = Digital Port C detected during initialization (default) AccessType: Read Only
1	0x0 RO	**DDI2_PORT_DETECTED:** Read-only bit indicating whether the DDI2 port was detected during initialization. It signifies the level of the GMBUS port 1 data line at boot. This bit is valid regardless of whether the port is enabled. 0 = DDI2 Port not detected during initialization 1 = DDI2 Port detected during initialization (default) AccessType: Read Only
0	0x0 RO	**RESERVED_6:** MBZ

4.2.253 DISPLAY_DIGITAL_PORT_HOT_PLUG_CONTROL_REGISTER—Offset 61164h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61164h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RO	**RESERVED:** Project: All Format:
20	0x0 RW	**DIGITAL_PORT_D_HOT_PLUG_DETECT_INPUT_ENABLE:** Project: All Default Value: ;0b Controls the state of the HPD buffer for the digital port. The buffer state is independent of whether the port is enabled or not. Value Name Description Project 0b Disable Buffer disabled All 1b Enable Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin All
19:18	0x0 RW	**DIGITAL_PORT_D_HOT_PLUG_SHORT_PULSE_DURATION:** Project: All Default Value: ;0b These bits define the duration of the pulse defined as a short pulse. Value Name Description Project 00b 2ms 2mS All 01b 4.5ms 4.5mS All 10b 6ms 6mS All 11b 100ms 100mS All

Bit Range	Default & Access	Field Name (ID): Description
17:16	0x0 RW/1C	**DIGITAL_PORT_D_HOT_PLUG_INTERRUPT_DETECT_STATUS:** Project: All Default Value: ;0b AccessType: One to Clear This reflects hot plug detect status on the digital port. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit. Value Name Description Project 00b No Detect Digital port hot plug event not detected All X1b Short Detect Digital port short pulse hot plug event detected All 1Xb Long Detect Digital port long pulse hot plug event detected All
15:13	0x0 RO	**RESERVED_1:** Project: All Format:
12	0x0 RW	**DIGITAL_PORT_C_HOT_PLUG_DETECT_INPUT_ENABLE:** Project: All Default Value: ;0b Controls the state of the HPD buffer for the digital port. The buffer state is independent of whether the port is enabled or not. Value Name Description Project 0b Disable Buffer disabled All 1b Enable Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin All
11:10	0x0 RW	**DIGITAL_PORT_C_HOT_PLUG_SHORT_PULSE_DURATION:** Project: All Default Value: ;0b These bits define the duration of the pulse defined as a short pulse. Value Name Description Project 00b 2ms 2mS All 01b 4.5ms 4.5mS All 10b 6ms 6mS All 11b 100ms 100mS All
9:8	0x0 RW/1C	**DIGITAL_PORT_C_HOT_PLUG_INTERRUPT_DETECT_STATUS:** Project: All Default Value: ;0b AccessType: One to Clear This reflects hot plug detect status on the digital port. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit. Value Name Description Project 00b No Detect Digital port hot plug event not detected All X1b Short Detect Digital port short pulse hot plug event detected All 1Xb Long Detect Digital port long pulse hot plug event detected All
7:5	0x0 RO	**RESERVED_2:** Project: All Format:

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**DIGITAL_PORT_B_HOT_PLUG_DETECT_INPUT_ENABLE:** Project: All Default Value: ;0b Controls the state of the HPD buffer for the digital port. The buffer state is independent of whether the port is enabled or not. Value Name Description Project 0b Disable Buffer disabled All 1b Enable Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin All
3:2	0x0 RW	**DIGITAL_PORT_B_HOT_PLUG_SHORT_PULSE_DURATION:** Project: All Default Value: ;0b These bits define the duration of the pulse defined as a short pulse. Value Name Description Project 00b 2ms 2mS All 01b 4.5ms 4.5mS All 10b 6ms 6mS All 11b 100ms 100mS All
1:0	0x0 RW/1C	**DIGITAL_PORT_B_HOT_PLUG_INTERRUPT_DETECT_STATUS:** Project: All Default Value: ;0b AccessType: One to Clear This reflects hot plug detect status on the digital port. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit. Value Name Description Project 00b No Detect Digital port hot plug event not detected All X1b Short Detect Digital port short pulse hot plug event detected All 1Xb Long Detect Digital port long pulse hot plug event detected All

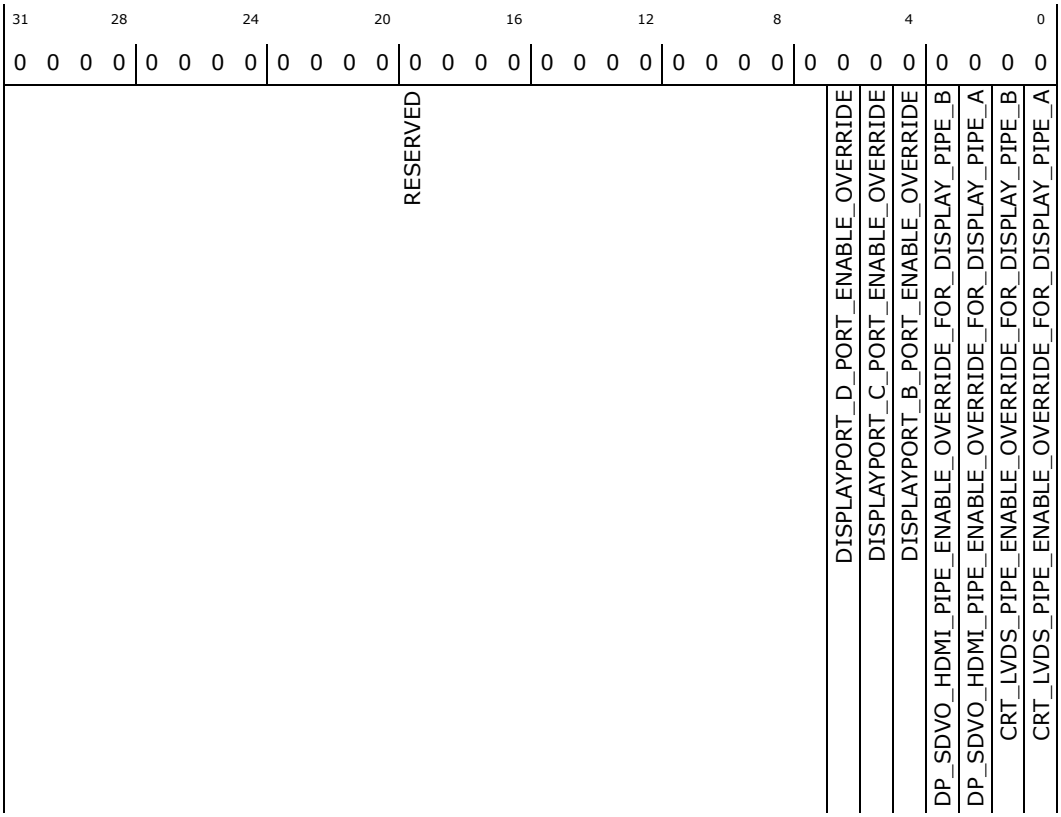
4.2.254 DV_DETERM—Offset 61168h

DV Determinism Mode Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61168h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**RESERVED:** Project: All Format:
6	0x0 RW	**DISPLAYPORT_D_PORT_ENABLE_OVERRIDE:** Project: All Default Value: ;0b Value Name Description Project 0b Normal Normal operation All 1b Override DisplayPort D port enable override (controlled from sml0alertb_gp60_mgpio4 pin) All
5	0x0 RW	**DISPLAYPORT_C_PORT_ENABLE_OVERRIDE:** Project: All Default Value: ;0b Value Name Description Project 0b Normal Normal operation All 1b Override DisplayPort C port enable override (controlled from sus_statb_gp61 pin) All
4	0x0 RW	**DISPLAYPORT_B_PORT_ENABLE_OVERRIDE:** Project: All Default Value: ;0b Value Name Description Project 0b Normal Normal operation All 1b Override DisplayPort B port enable override (controlled from gp57_mgpio5 pin) All

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**DP_SDVO_HDMI_PIPE_ENABLE_OVERRIDE_FOR_DISPLAY_PIPE_B:** Project: All Default Value: ;0b Value Name Description Project 0b Normal Normal operation All 1b Override DP/SDVO/HDMI pipe enable override for display pipe B (controlled from gp74_batlowb pin) All
2	0x0 RW	**DP_SDVO_HDMI_PIPE_ENABLE_OVERRIDE_FOR_DISPLAY_PIPE_A:** Project: All Default Value: ;0b Value Name Description Project 0b Normal Normal operation All 1b Override DP/SDVO/HDMI pipe enable override for display pipe A (controlled from slp_s4b pin) All
1	0x0 RW	**CRT_LVDS_PIPE_ENABLE_OVERRIDE_FOR_DISPLAY_PIPE_B:** Project: All Default Value: ;0b Value Name Description Project 0b Normal Normal operation All 1b Override CRT/LVDS pipe enable override for display pipe B (controlled from susclk_gp62 pin) All
0	0x0 RW	**CRT_LVDS_PIPE_ENABLE_OVERRIDE_FOR_DISPLAY_PIPE_A:** Project: All Default Value: ;0b Value Name Description Project 0b Normal Normal operation All 1b Override CRT/LVDS pipe enable override for display pipe A (controlled from slp_mb pin) All

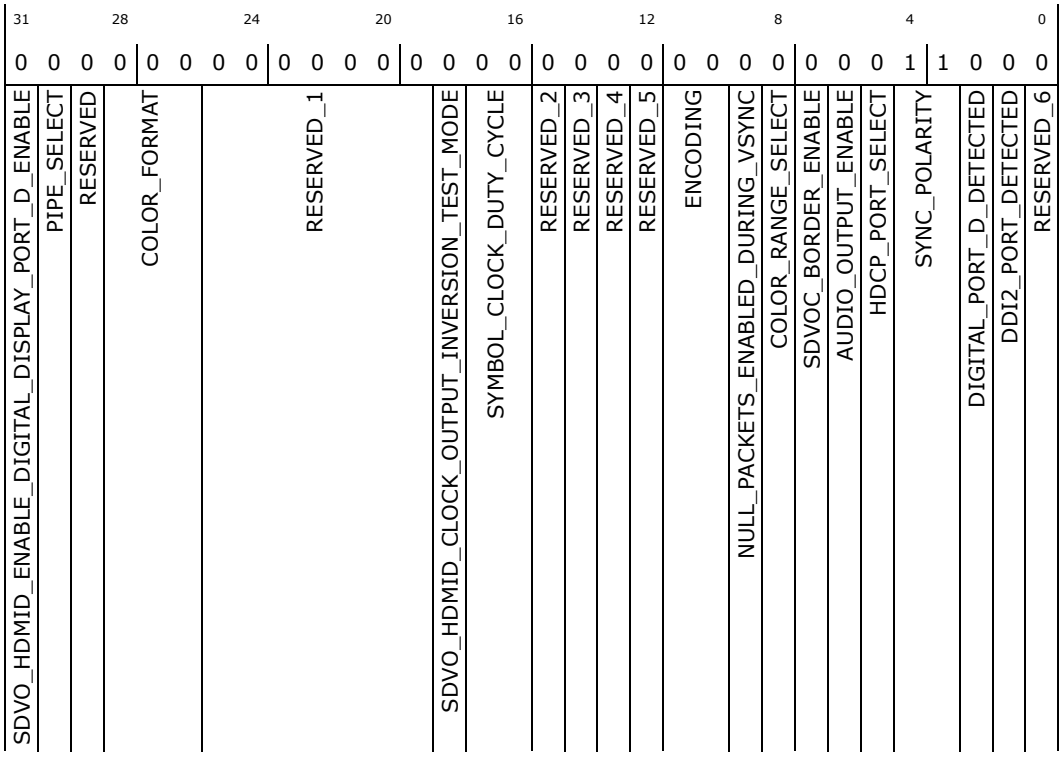
4.2.255 HDMID—Offset 6116Ch

Digital Display Port D Register HDMID port control (dprrega.v sdvo_cQ)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6116Ch

Default: 00000018h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SDVO_HDMID_ENABLE_DIGITAL_DISPLAY_PORT_D_ENABLE:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and bit 6 of this register must be enabled to send audio over this port in HDMI. This port must not be enabled simultaneously with DisplayPort D. [DevIBX] When disabling the port, software must temporarily enable the port with transcoder select (bit #30) cleared to 0 after disabling the port. This is workaround for hardware issue where the transcoder select set to 1 will prevent DPC from being enabled on transcoder A. [DevIBX] Software must write this bit twice when enabling the port (setting to 1) as a workaround for hardware issue that may result in first write getting masked. [DevIBX] Toggle this bit off then on at the end of mode set sequence when enabling HDMI 12-bit per color with pixel repeat. 1 = Enable. This bit enables the Digital Display Port D interface for HDMI or DVI modes. 0 = Disable and tristates the Digital Display Port D interface for HDMI or DVI modes.
30	0x0 RW	**PIPE_SELECT:** This bit determines from which display pipe the source data will originate. This only applies to devices with dual display pipes. Pipe selection takes place on the Vblank after being written 0 = Pipe A 1 = Pipe B

Bit Range	Default & Access	Field Name (ID): Description
29	0x0 RO	**RESERVED:** : stall Select: This bit selects stall for external scaling functionality only on SDVO. Programming notes: It is only valid to have a single stall indication to a particular pipe. In cases where two ports are being driven from a single pipe, one of the ports must set this bit to 0. Only sDVOB or sDVOC can select the stall function, as only a single stall input is available between the two interfaces. Set the stall input to unused before programming the external device creating the stall. 0 = Stall input signal is unused on this port 1 = Stall input signal is used to stall the pipe attached to this port
28:26	0x0 RW	**COLOR_FORMAT:** This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change must be done as a part of mode set since different color depths require different pixel clock settings. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. 000 = 8 bits per color (Default) 001 = RESERVED for 10 bits per color 010 = RESERVED for 6 bits per color 011 = RESERVED 1xx = RESERVED
25:19	0x0 RO	**RESERVED_1:** Reserved.
18	0x0 RW	**SDVO_HDMID_CLOCK_OUTPUT_INVERSION_TEST_MODE:** Please note that this applies to all modes and is instantly updated. 1 = sDVO/HDMID Clock output is inverted 0 = sDVO/HDMID Clock output is NOT inverted (DEFAULT)
17:16	0x0 RW	**SYMBOL_CLOCK_DUTY_CYCLE:** These bits control the output clock duty cycle to enable EMI mitigation on the external HDMI link. 10/90 cycle has been measured to have ~13dB EMI improvement over a 50/50 duty cycle. 00 = (Default) 50/50 duty cycle: Clock output is 0000011111 01 = 10/90 duty cycle: Clock output is 0111111111 followed by 0000000001 (HDMI only) 10 = 20/80 duty cycle: Clock output is 0011111111 followed by 0000000011 (HDMI only) 11 = Reserved
15	0x0 RO	**RESERVED_2:** Port Lane Reversal: This bit reverses the order of the 4 lanes within the port. Port lane reversal takes place on the Vblank after being written. It is an OEM configurable feature. 0 = (Default) Not reversed 1 = Reversed
14	0x0 RO	**RESERVED_3:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13	0x0 RO	**RESERVED_4:** Clock Output Disable: This bit disables the clock output on the digital output port. For 8b/10b modes the clock output should be disabled. 0 = (Default) Clock output enabled 1 = Clock output disabled ([DevCL] only)
12	0x0 RO	**RESERVED_5:** Scrambling enable: This bit enables scrambling for UDI-related modes using ANSI 8b/10b or TMDS encoding. It is not used with SDVO encoding. Software must set this bit appropriately when enabling the port. Scrambling is reset at the beginning of horizontal sync. 0 Scrambling disabled (Default) 1 = Scrambling enabled ([DevCL] only)
11:10	0x0 RW	**ENCODING:** These bits select among encoding types. It is set as part of the display detection process. Control codes for ANSI 8b/10b and TMDS encoding must be programmed using these bits. Please note that ANSI 8b/10b and TMDS encoding can only be enabled on one port at a time, as only one HPD pin is available for use between ports B and C. 00 = Reserved 01 = Reserved 10 = TMDS encoding (external link and HDMI only) Refer the HDMI specification for control codes. In this mode, the external HPD pin is used to generate hotplug. In fixed frequency mode, start of fill and end of fill values for TMDS must be programmed using register 6114C. 11 = Reserved
9	0x0 RW	**NULL_PACKETS_ENABLED_DURING_VSYNC:** This bit enables a null packet (32 bytes of a value of 0) to be sent when Vsync=1 on this port, required for HDMI operation. It also enables preambles and guardbands prior to the null packets, in accordance with the HDMI specification. It is only valid for modes that use TMDS encoding. 0 = Disable null infoframe packets when Vsync=1 on this port. (Default) 1 = Enable null infoframe packets when Vsync=1 on this port.
8	0x0 RW	**COLOR_RANGE_SELECT:** This bit is used to select the color range of RBG outputs in HDMI mode. It is only valid when using TMDS encoding and 8 bit per color mode. 0 = Apply full 0-255 color range to the output (Default) 1 = Apply 16-235 color range to the output ([DevCL and DevCTG] only)
6	0x0 RW	**AUDIO_OUTPUT_ENABLE:** This bit directs audio to this port. When enabled and audio data is available, the audio data will be combined with the video data and sent over this port. The audio unit uses the status of this bit to indicate presence of the HDMI output to the audio driver. 0 = (Default) No audio output on this port 1 = Enable audio on this port
5	0x0 RW	**HDCP_PORT_SELECT:** This bit directs HDCP to this port. When enabled, the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own, but must be used in conjunction with HDCP registers. 0 = (Default) No HDCP encryption on this port 1 = Enable HDCP on this port

Bit Range	Default & Access	Field Name (ID): Description
4:3	0x3 RW	**SYNC_POLARITY:** Please note that sync polarity does not apply to ANSI coding. Indicates the polarity of Hsync and Vsync. Inverted polarity is transmitted as SYNC-BLANK-SYNC and standard polarity is transmitted as BLANK-SYNC-BLANK. For example, if Vsync is not inverted and Hsync is inverted, an Hsync period transmitted during Vsync would be transmitted as BLANK+VS+HS BLANK+VS BLANK+VS+HS. 00 = VS and HS are active low (inverted) 01 = VS is active low (inverted), HS is active high 10 = VS is active high, HS is active low (inverted) 11 = (Default) VS and HS are active high
2	0x0 RO	**DIGITAL_PORT_D_DETECTED:** Read-only bit indicating whether a digital port D was detected during initialization. It signifies the level of the GMBUS port 3 (port C) data line at boot. This bit is valid regardless of whether the port is enabled. 0 = Digital Port C not detected during initialization 1 = Digital Port C detected during initialization (default) AccessType: Read Only
1	0x0 RO	**DDI2_PORT_DETECTED:** Read-only bit indicating whether the DDI2 port was detected during initialization. It signifies the level of the GMBUS port 1 data line at boot. This bit is valid regardless of whether the port is enabled. 0 = DDI2 Port not detected during initialization 1 = DDI2 Port detected during initialization (default) AccessType: Read Only
0	0x0 RO	**RESERVED_6:** MBZ

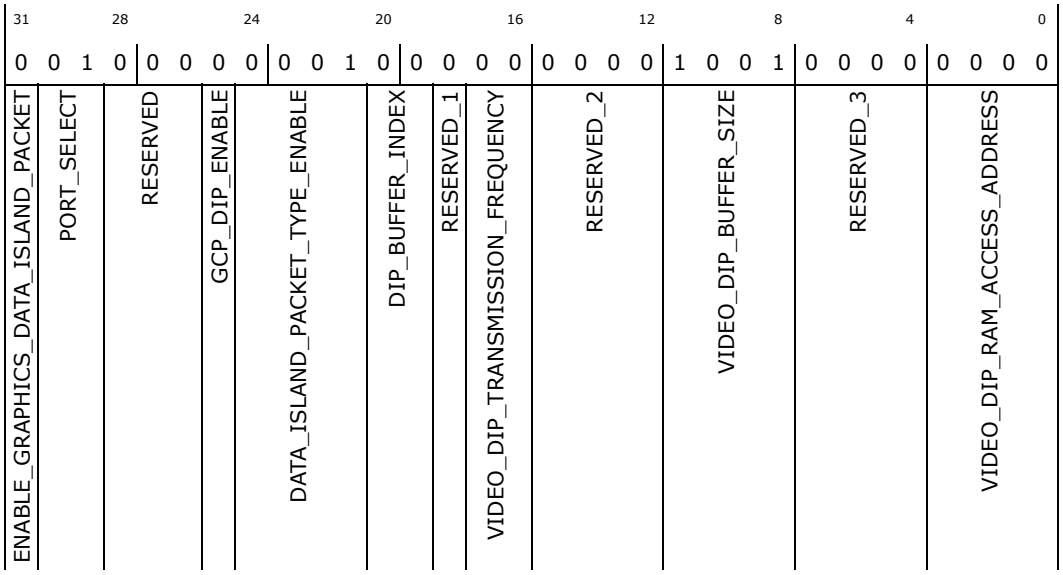
4.2.256 VIDEO_DIP_CTL_B—Offset 61170h

Video DIP Control for Pipe B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61170h

Default: 20200900h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**ENABLE_GRAPHICS_DATA_ISLAND_PACKET:** Project: All Refer Pipe A description.
30:29	0x1 RW	**PORT_SELECT:** Project: All Refer Pipe A description.
28:26	0x0 RO	**RESERVED:** Project: All Format:
25	0x0 RW	**GCP_DIP_ENABLE:** Project: All Refer Pipe A description. This bit should not be enabled for 8bpc mode if at least one of the other HDMI ports is enabled in 12bpc mode.
24:21	0x1 RW	**DATA_ISLAND_PACKET_TYPE_ENABLE:** Project: All Refer Pipe A description.
20:19	0x0 RW	**DIP_BUFFER_INDEX:** Project: All Refer Pipe A description.
18	0x0 RO	**RESERVED_1:** Project: All Format:
17:16	0x0 RW	**VIDEO_DIP_TRANSMISSION_FREQUENCY:** Project: All Refer Pipe A description.
15:12	0x0 RO	**RESERVED_2:** Project: All Format: MBZ
11:8	0x9 RO	**VIDEO_DIP_BUFFER_SIZE:** Project: All AccessType: Read Only Default Value: ;1001b Refer Pipe A description.
7:4	0x0 RO	**RESERVED_3:** Project: All Format: MBZ

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x0 RO	**VIDEO_DIP_RAM_ACCESS_ADDRESS:** Project: All AccessType: Read only Refer Pipe A description.

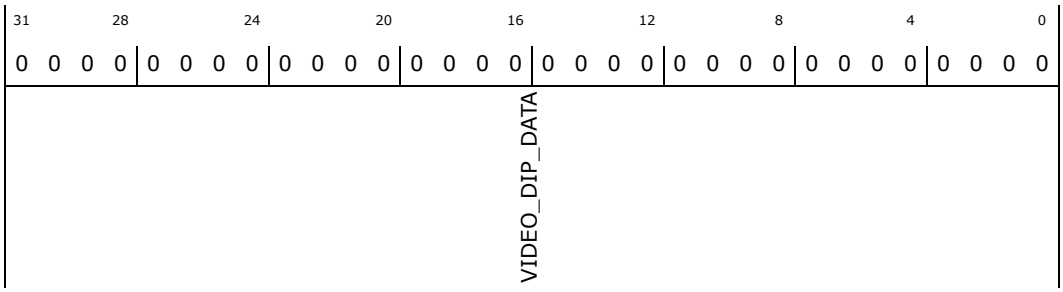
4.2.257 VIDEO_DIP_DATA_B—Offset 61174h

Video Data Island Packet Data for Pipe B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61174h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VIDEO_DIP_DATA:** Project: All Format: Refer Pipe A description.

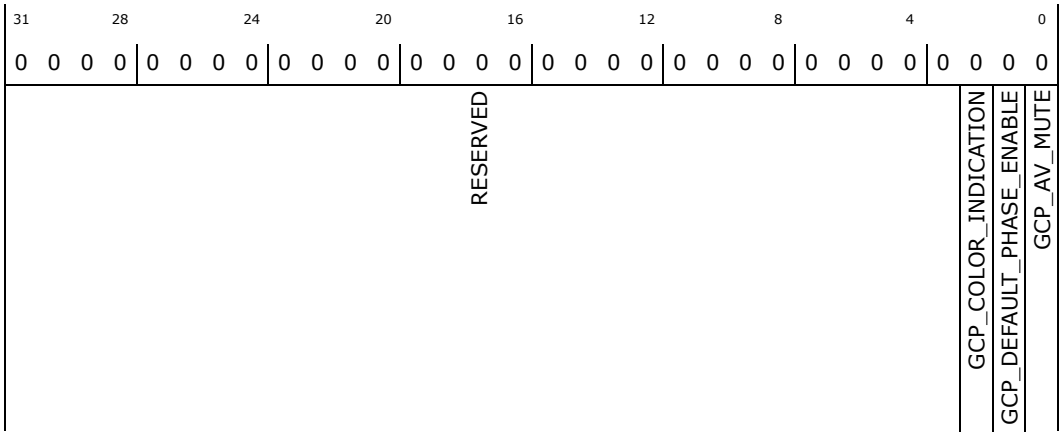
4.2.258 VIDEO_DIP_GDCP_PAYLOAD_B—Offset 61178h

Video Data Island Payload for Pipe B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61178h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**RESERVED:** Project: All Format: MBZ
2	0x0 RW	**GCP_COLOR_INDICATION:** Project: All Refer Pipe A description.
1	0x0 RW	**GCP_DEFAULT_PHASE_ENABLE:** Project: All Refer Pipe A description.
0	0x0 RW	**GCP_AV_MUTE:** All Refer Pipe A description.

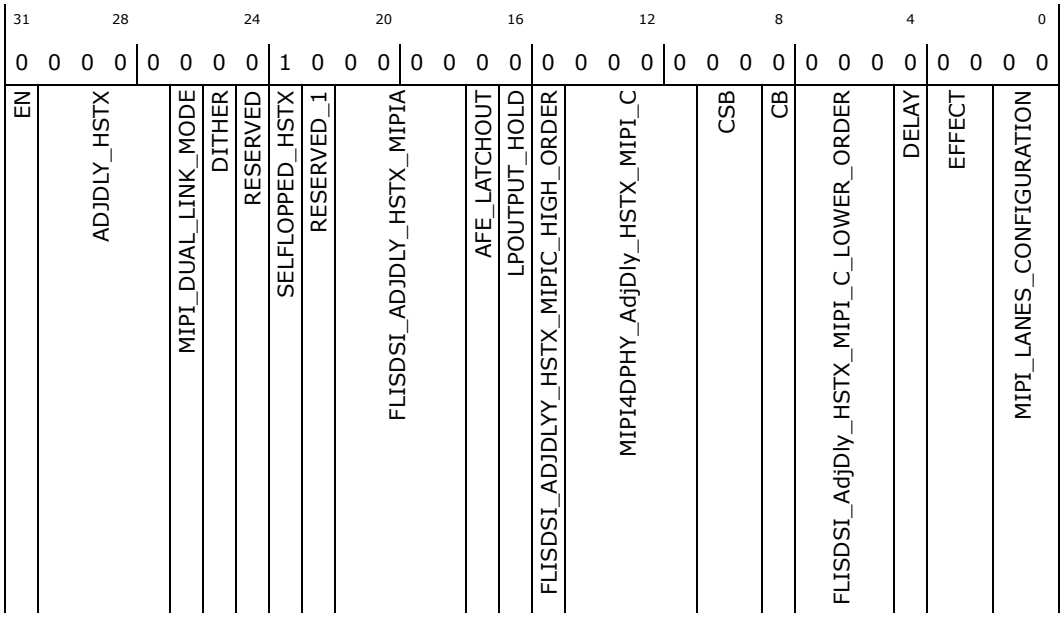
4.2.259 MIPIA_PORT_CTRL—Offset 61190h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61190h

Default: 00800000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**EN:** When this bit is disabled the MIPI DPI (video mode) is inactive and in it's low power state. When it is enable it starts to generate timing for this MIPI port 0 = The port is disabled and all MIPI DPI interface are disable (timing generator is off) 1 = The port is enabled
30:27	0x0 RW	**ADJDLY_HSTX:** These four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 4'b0000 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature
26	0x0 RW	**MIPI_DUAL_LINK_MODE_APPLICABLE_ONLY_IF_MIPI_DUAL_LINK_MODE_IS_ENABLED_THROUGH_MIPI_LANES_CONFIGURATION_BITS (MIPI_DUAL_LINK_MODE):** 0 = Front-Back mode (default) 1 = Pixel alternative mode
25	0x0 RW	**DITHER:** This bit enables or disables (bypassing) 8-6-bit color dithering function. The usage of this bit would be on for 18-bpp panels and off for 24-bpp panels. 0 = disabled 1 = enabled
24	0x0 RO	**RESERVED:** Reserved.
23	0x1 RW	**SELFLOPPED_HSTX:** This bit will be used to mux between the flopped (new) and unflopped (original) versions of the TX HS clock and data. Default 0 = pass through original unflopped version, if set to 1 = pass through the new flopped version of these signals. We probably need to enable validation to always set these to 1 during startup so we're fully testing this logic as it is the intended way we will run A0

Bit Range	Default & Access	Field Name (ID): Description
22	0x0 RO	**RESERVED_1:** Reserved.
21:18	0x0 RW	**FLISDSI_ADJDLY_HSTX_MIPIA:** These four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 4'b0000 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature
17	0x0 RW	**AFE_LATCHOUT:** This bit reflect the value of the output latch of CLK A lane in DSI AFE b1 = current value of output latch is 1 (D-PHY is in LP11 state) b0 = current value of output latch is 0 (D-PHY is in LP00 state) The software driver can read this bit to see if the hold value (LP11 or LP00) to initialize from a sleep state (s0i1 or S0i3) correctly
16	0x0 RW	**LPOUTPUT_HOLD:** 0= disable transparent latche inside DSI AFE. Output are driven by latch value. 1= enable transparent latch inside DSI AFE so data are driven by DSI DPHY
15	0x0 RW	**FLISDSI_ADJDLYY_HSTX_MIPIC_HIGH_ORDER:** The fourth bit of four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 1'b0 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature
14:11	0x0 RW	**MIPI4DPHY_AdjDly_HSTX_MIPI_C:** These four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals.[Br] Default is 4'b0000 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature
10:9	0x0 RW	**CSB:** Clock input for bandgap voltage sample and hold circuit. Final setting will be based silicon characterization. 00b = 20mhz clock 01b = 10mhz clock 10b = 40mhz clock 11b = reserved
8	0x0 RW	**CB:** Bandgap chicken bit 0 = using SoC band gap circuit 1 = back to LNC circuit
7:5	0x0 RW	**FLISDSI_AdjDly_HSTX_MIPI_C_LOWER_ORDER:** The lower 3-bit of four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 3'b000 which is the equivalent of 1 buffer delay. Will need to set these bits to a value determined by clock timing team before using the MIPI DSI HS TX feature
4	0x0 RW	**DELAY:** When set, the TE counter will be count down until

Bit Range	Default & Access	Field Name (ID): Description
3:2	0x0 RW	**EFFECT:** 00: No tearing effect required - memory write start as soon as write data is available 01: TE trigger by MIPI DPHY and DSI protocol 10: TE trigger by GPIO pin 11: Reserved
1:0	0x0 RW	**MIPI_LANES_CONFIGURATION:** 00: All 4 MIPI A lanes are assigned to pipe A. All 4 MIPI C lanes are assigned to pipe B. 01: MIPI dual-link mode with data from pipe A 10: MIPI dual-link mode with data from pipe B 11: Reserved Programming note: when MIPI dual-link mode is enabled, the port enable bits in both MIPI A control register and MIPI C control register shall be enabled.

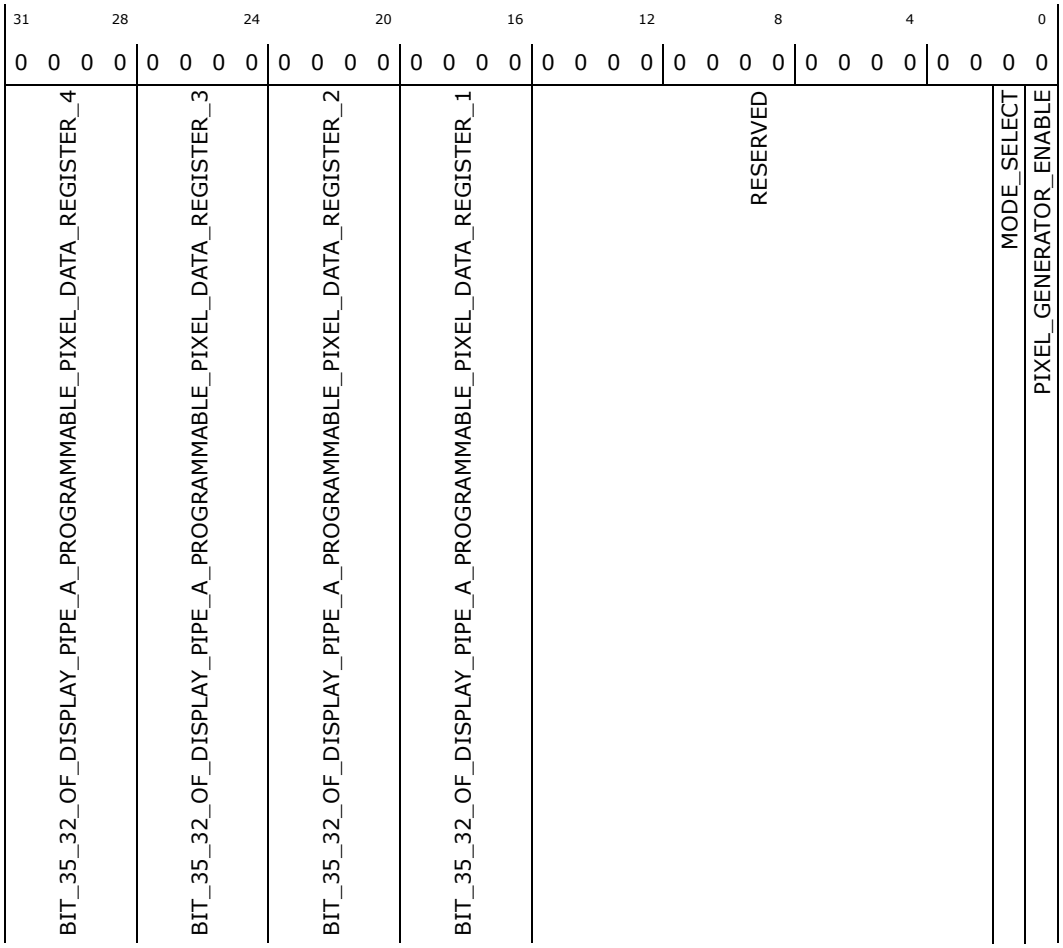
4.2.260 DPA_PIX_GEN_CTRL—Offset 61198h

Display Pipe A Pixel Generator Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61198h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW	**BIT_35_32_OF_DISPLAY_PIPE_A_PROGRAMMABLE_PIXEL_DATA_REGISTER_4:** Project: All Default Value: ;0b
27:24	0x0 RW	**BIT_35_32_OF_DISPLAY_PIPE_A_PROGRAMMABLE_PIXEL_DATA_REGISTER_3:** Project: All Default Value: ;0b
23:20	0x0 RW	**BIT_35_32_OF_DISPLAY_PIPE_A_PROGRAMMABLE_PIXEL_DATA_REGISTER_2:** Project: All Default Value: ;0b
19:16	0x0 RW	**BIT_35_32_OF_DISPLAY_PIPE_A_PROGRAMMABLE_PIXEL_DATA_REGISTER_1:** Project: All Default Value: ;0b
15:2	0x0 RO	**RESERVED:** Project: All Format:

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**MODE_SELECT:** Project: All Default Value: ;0b Pixel generator mode select Value Name Description Project 0b LFSR LFSR All 1b Programmable Programmable pixel data register. Setting mode select to 1 will also start the 2-bit counter. All
0	0x0 RW	**PIXEL_GENERATOR_ENABLE:** All

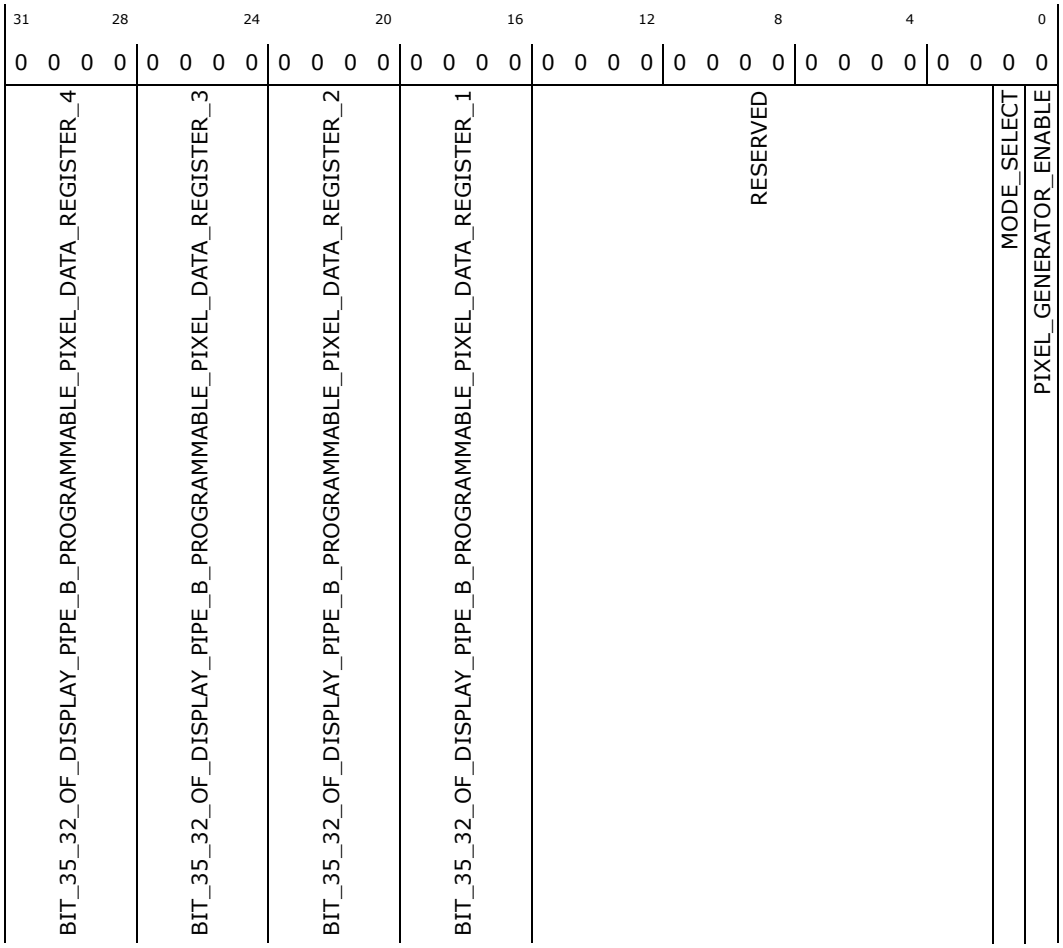
4.2.261 DPB_PIX_GEN_CTRL—Offset 611B0h

Display Pipe B Pixel Generator Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 611B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW	**BIT_35_32_OF_DISPLAY_PIPE_B_PROGRAMMABLE_PIXEL_DATA_REGISTER_4:** Project: All Default Value: ;0b
27:24	0x0 RW	**BIT_35_32_OF_DISPLAY_PIPE_B_PROGRAMMABLE_PIXEL_DATA_REGISTER_3:** Project: All Default Value: ;0b Address: GraphicsAddress[35:32]
23:20	0x0 RW	**BIT_35_32_OF_DISPLAY_PIPE_B_PROGRAMMABLE_PIXEL_DATA_REGISTER_2:** Project: All Default Value: ;0b
19:16	0x0 RW	**BIT_35_32_OF_DISPLAY_PIPE_B_PROGRAMMABLE_PIXEL_DATA_REGISTER_1:** Project: All Default Value: ;0b
15:2	0x0 RO	**RESERVED:** Project: All Format:

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**MODE_SELECT:** Project: All Default Value: ;0b Pixel generator mode select Value Name Description Project 0b LFSR LFSR All 1b Programmable Programmable pixel data register. Setting mode select to 1 will also start the 2-bit counter. All
0	0x0 RW	**PIXEL_GENERATOR_ENABLE:** All Format: Enable

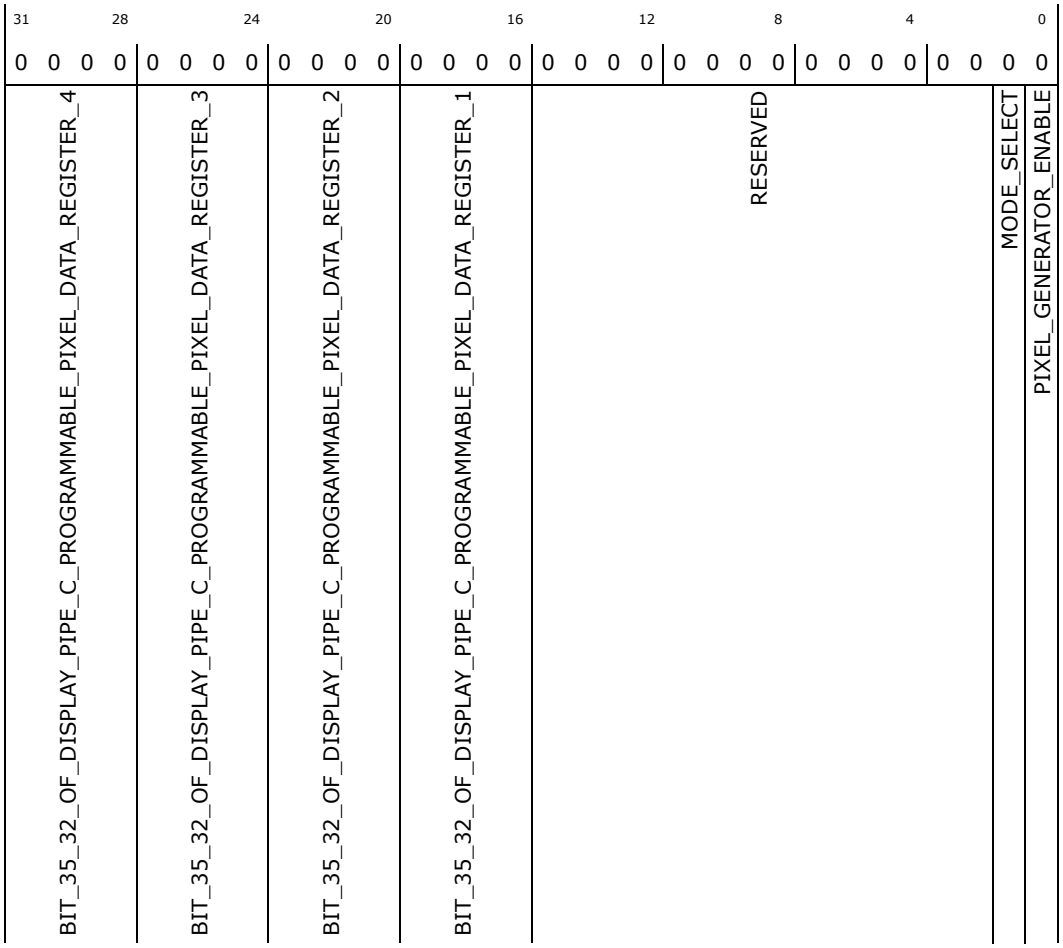
4.2.262 DPC_PIX_GEN_CTRL—Offset 611D0h

Display Pipe C Pixel Generator Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 611D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW	**BIT_35_32_OF_DISPLAY_PIPE_B_PROGRAMMABLE_PIXEL_DATA_REGISTER_4 (BIT_35_32_OF_DISPLAY_PIPE_C_PROGRAMMABLE_PIXEL_DATA_REGISTER_4):** Project: All Default Value: ;0b
27:24	0x0 RW	**BIT_35_32_OF_DISPLAY_PIPE_C_PROGRAMMABLE_PIXEL_DATA_REGISTER_3:** Project: All Default Value: ;0b Address: GraphicsAddress[35:32]
23:20	0x0 RW	**BIT_35_32_OF_DISPLAY_PIPE_C_PROGRAMMABLE_PIXEL_DATA_REGISTER_2:** Project: All Default Value: ;0b
19:16	0x0 RW	**BIT_35_32_OF_DISPLAY_PIPE_C_PROGRAMMABLE_PIXEL_DATA_REGISTER_1:** Project: All Default Value: ;0b
15:2	0x0 RO	**RESERVED:** Project: All Format:

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**MODE_SELECT:** Project: All Default Value: ;0b Pixel generator mode select Value Name Description Project 0b LFSR LFSR All 1b Programmable Programmable pixel data register. Setting mode select to 1 will also start the 2-bit counter. All
0	0x0 RW	**PIXEL_GENERATOR_ENABLE:** All Format: Enable

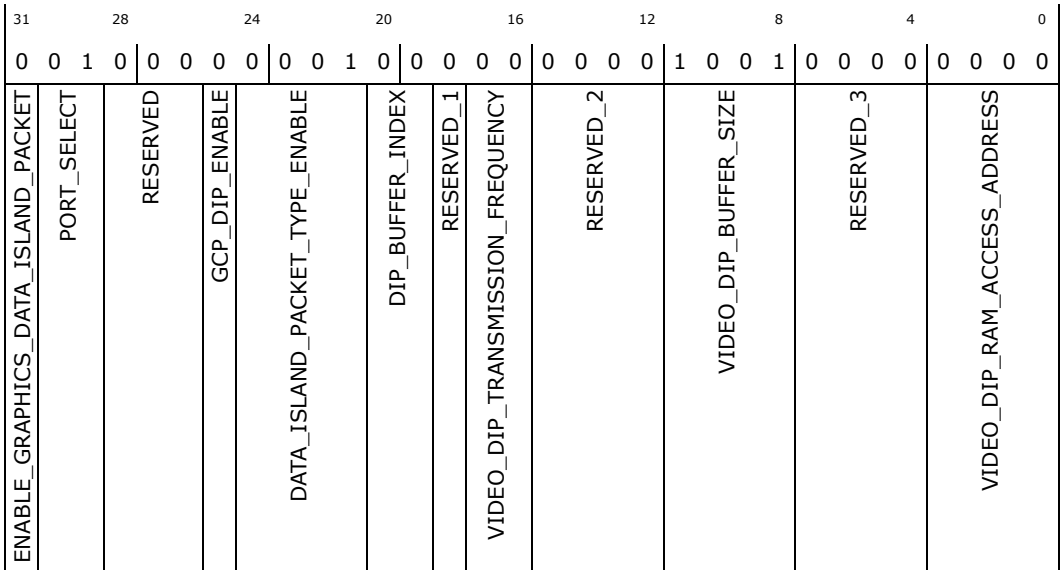
4.2.263 VIDEO_DIP_CTL_C—Offset 611F0h

Video DIP Control for Pipe C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 611F0h

Default: 20200900h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**ENABLE_GRAPHICS_DATA_ISLAND_PACKET:** Project: All Refer Pipe A description.
30:29	0x1 RW	**PORT_SELECT:** Project: All Refer Pipe A description.
28:26	0x0 RO	**RESERVED:** Project: All Format:

Bit Range	Default & Access	Field Name (ID): Description
25	0x0 RW	**GCP_DIP_ENABLE:** Project: All Refer Pipe A description. This bit should not be enabled for 8bpc mode if at least one of the other HDMI ports is enabled in 12bpc mode.
24:21	0x1 RW	**DATA_ISLAND_PACKET_TYPE_ENABLE:** Project: All Refer Pipe A description.
20:19	0x0 RW	**DIP_BUFFER_INDEX:** Project: All Refer Pipe A description.
18	0x0 RO	**RESERVED_1:** Project: All Format:
17:16	0x0 RW	**VIDEO_DIP_TRANSMISSION_FREQUENCY:** Project: All Refer Pipe A description.
15:12	0x0 RO	**RESERVED_2:** Project: All Format: MBZ
11:8	0x9 RO	**VIDEO_DIP_BUFFER_SIZE:** Project: All AccessType: Read Only Default Value: ;1001b Refer Pipe A description.
7:4	0x0 RO	**RESERVED_3:** Project: All Format: MBZ
3:0	0x0 RO	**VIDEO_DIP_RAM_ACCESS_ADDRESS:** Project: All AccessType: Read only Refer Pipe A description.

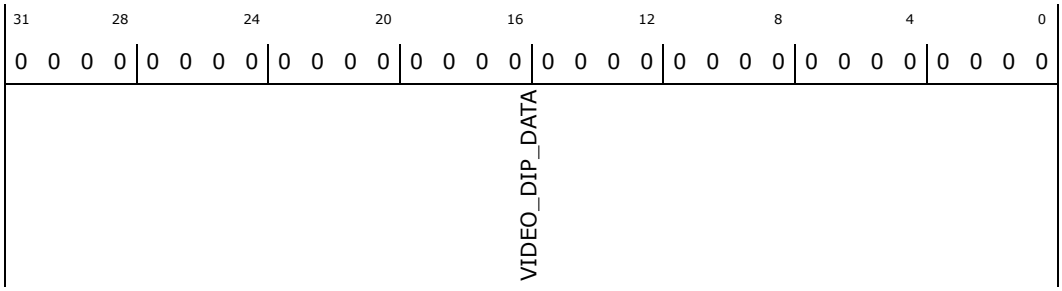
4.2.264 VIDEO_DIP_DATA_C—Offset 611F4h

Video Data Island Packet Data for Pipe C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 611F4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VIDEO_DIP_DATA:** Project: All Format: Refer Pipe A description.

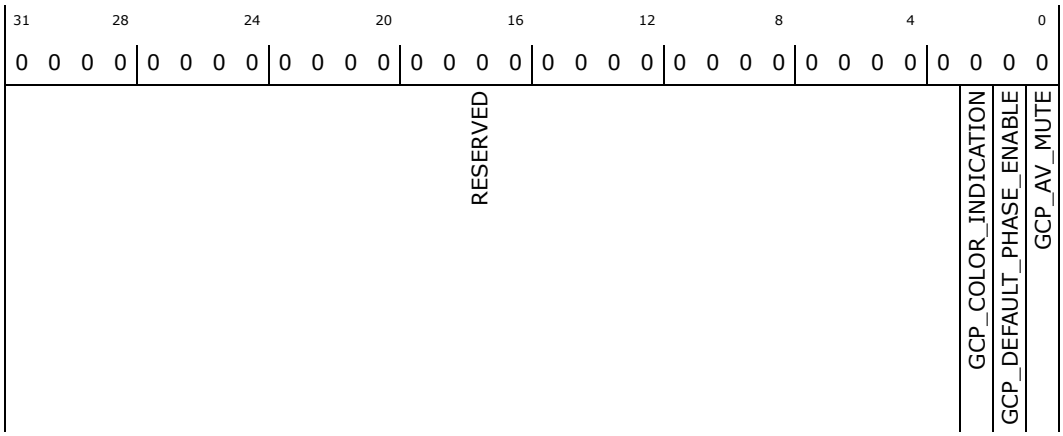
4.2.265 VIDEO_DIP_GDCP_PAYLOAD_C—Offset 611F8h

Video Data Island Payload for Pipe C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 611F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**RESERVED:** Project: All Format: MBZ
2	0x0 RW	**GCP_COLOR_INDICATION:** Project: All Refer Pipe A description.
1	0x0 RW	**GCP_DEFAULT_PHASE_ENABLE:** Project: All Refer Pipe A description.
0	0x0 RW	**GCP_AV_MUTE:** All Refer Pipe A description.

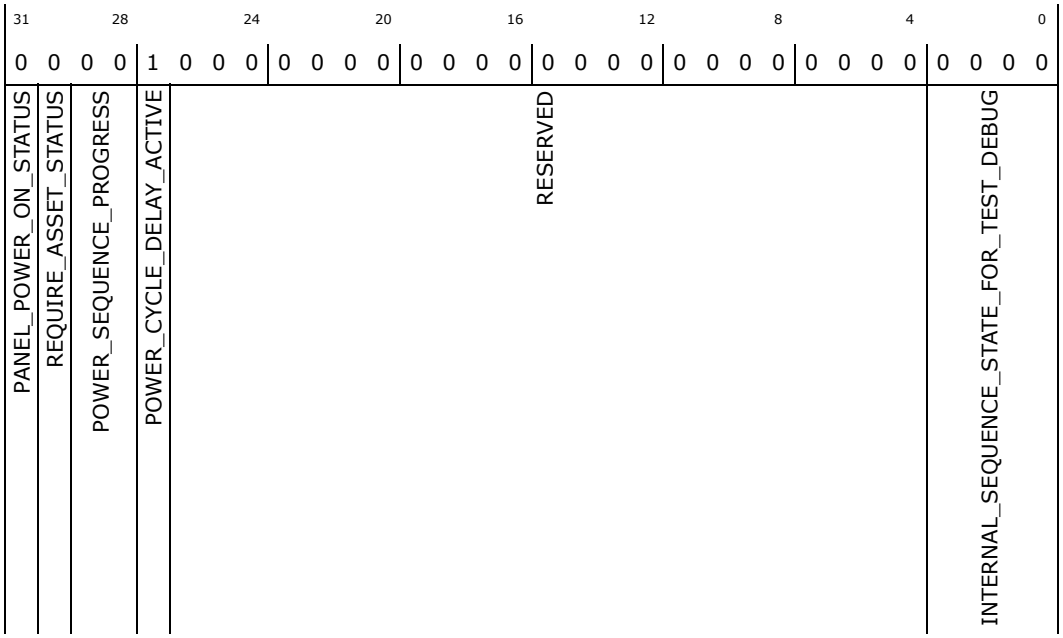
4.2.266 PIPEA_PP_STATUS—Offset 61200h

PipeA Panel Power Status Register PP Status (dplrreg.v panel_pwr_sr)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61200h

Default: 08000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**PANEL_POWER_ON_STATUS:** 0 = Indicates that the panel power down sequencing has completed. A power cycle delay may be currently active. It is safe and allowed to program pipe timing and DPLL registers. If this bit is not a zero, it activates the register write protect and writes to those registers will be ignored unless the write protect key value is set in the panel sequencing control register. 1 = In conjunction with bits Power Sequence Progress field and Power Cycle Delay Active, this bit set to a one indicates that the panel is currently powered up or is currently in the power down sequence and it is unsafe to change the pipe timing and DPLL registers for the pipe that is assigned to the embedded panel output. If the embedded panel port is selected as the target for the panel control, Software is responsible for enabling the LCD display by writing a 1 to the port enable bit only after all pipe timing, DPLL registers are properly programmed, and the PLL has locked to the reference signal. This bit is cleared (set to 0) only after the panel power down sequencing is completed.
30	0x0 RO	**REQUIRE_ASSET_STATUS:** This bit indicates the status of programming of the display PLL and the selected display port. This a power on cycle will not be allowed unless this status indicates that the required assets are programmed and ready for use. 0 = All required assets are not properly programmed. 1 = All required assets are ready for the driving of a panel. The following conditions determine that the assets are ready: 1) Display Pipe PLL Enabled and frequency locked (bit-31 of DPLL Control Register for the pipe attached to the embedded panel port). 2) Display Pipe Enabled (bit-31 of PIPECONF Pipe Configuration Register. For the pipe attached to the embedded panel port) 3) Embedded Panel Port is Programmed Enabled

Bit Range	Default & Access	Field Name (ID): Description
29:28	0x0 RO	**POWER_SEQUENCE_PROGRESS:** 00 = Indicates that the panel is not in a power sequence 01 = Indicates that the panel is in a power up sequence (may include power cycle delay) 10 = Indicates that the panel is in a power down sequence 11 = Reserved
27	0x1 RO	**POWER_CYCLE_DELAY_ACTIVE:** Power cycle delays occur after a panel power down sequence or after a hardware reset. On reset, a power cycle delay will occur using the default value for the timing. 0 = A power cycle delay is not currently active 1 = A power cycle delay (T4) is currently active
26:4	0x0 RO	**RESERVED:** Reserved.
3:0	0x0 RO	**INTERNAL_SEQUENCE_STATE_FOR_TEST_DEBUG:** 0000 = Power Off Idle (S0.0) 0001 = Power Off, Wait for cycle delay (S0.1) 0010 = Power Off (S0.2) 0011 = Power Off (S0.3) 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = Power On Idle (S1.0) 1001 = Power On, (S1.1) 1010 = Power On, (S1.2) 1011 = Power On, Wait for cycle delay (S1.3) 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reset

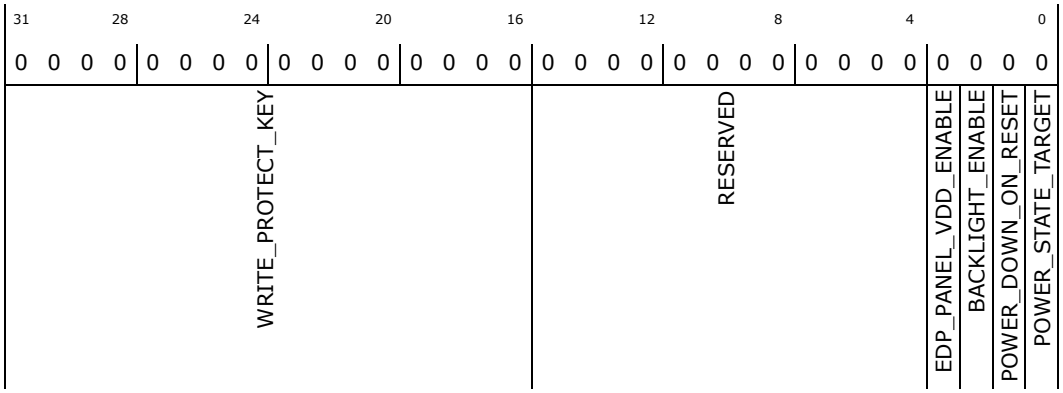
4.2.267 PIPEA_PP_CONTROL—Offset 61204h

PipeA Panel Power Control Register PP Control (dplrreg.v pnl_pwr_cntl)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61204h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**WRITE_PROTECT_KEY:** ABCD Write protect off When this field is programmed to anything except the write protect off setting and the panel is either powered up or in the process of a power up sequence, a set of registers involved in generation of panel timing or control become write protected. Any write cycles to those write protected registers, while they will complete as normal, will not change the value of the register when write protected. When this register field contains the write protect off key value, write protect will be unconditionally disabled. In situations where the embedded panel port is unused, the port should remain powered down and the write protect will be inactive. This field in normal operation should be left to all zeros and never programmed with the key value. It exists only to allow testing and workarounds. List of Write protected registers: (LVDS and Panel sequencing Registers): LVDS Digital Display Port Control Address: 61180h 61183h Pipe A Panel power on sequencing delays - Address: 61208-6120Bh Pipe A Panel power off sequencing delays Address: 6120Ch 6120Fh Pipe A Panel power cycle delay and Reference Divisor Address: 61210h 61213 (DPLL registers): DPLL Control Registers FPA0 DPLL Divisor Register FPA1 DPLL Divisor Register 1 FPB0 DPLL Divisor Register FPB1 DPLL Divisor Register 1 (Display Pipe timing registers except source size) HTOTAL Horizontal Total Register HBLANK Horizontal Blank Register HSYNC_ Horizontal Sync Register VTOTAL_ Vertical Total Register VBLANK_ Vertical Blank Register VSYNC_ Vertical Sync Register
15:4	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**EDP_PANEL_VDD_ENABLE:** : Enabling this bit enables the panel vdd if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit for eDP link training. After eDP link training is done, software must disable it and let the normal panel power sequencing to take control. 0 = eDP panel Vdd disabled 1 = eDP panel Vdd enabled [DevCLN] Reserved
2	0x0 RW	**BACKLIGHT_ENABLE:** Enabling this bit enables the panel backlight if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit after training the link, and disable it when disabling the panel power state target. 0 = Backlight disabled 1 = Backlight enabled [DevCL] Reserved
1	0x0 RW	**POWER_DOWN_ON_RESET:** Enabling this bit causes the panel to power down when a reset warning comes to the GMCH from the ICH. When system reset is initiated, the embedded panel port automatically begins the panel power down sequence. If the panel is not on during a reset event, this bit is ignored. 0 = Do not run panel power down sequence when reset is detected 1 = Run panel power down sequence when system is reset
0	0x0 RW	**POWER_STATE_TARGET:** Writing this bit can occur any time, it will only be used at the completion of any current power cycle. 0 = The panel power state target is off, if the panel is either on or in a power on sequence, a power off sequence is started as soon as the panel reaches the power on state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. 1= The panel power state target is on, if the panel is in either the off state or a power off sequence, if all pre-conditions are met, a power on sequence is started as soon as the panel reaches the power off state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. While the panel is on or in a power on sequence, the register write lock will be enabled.

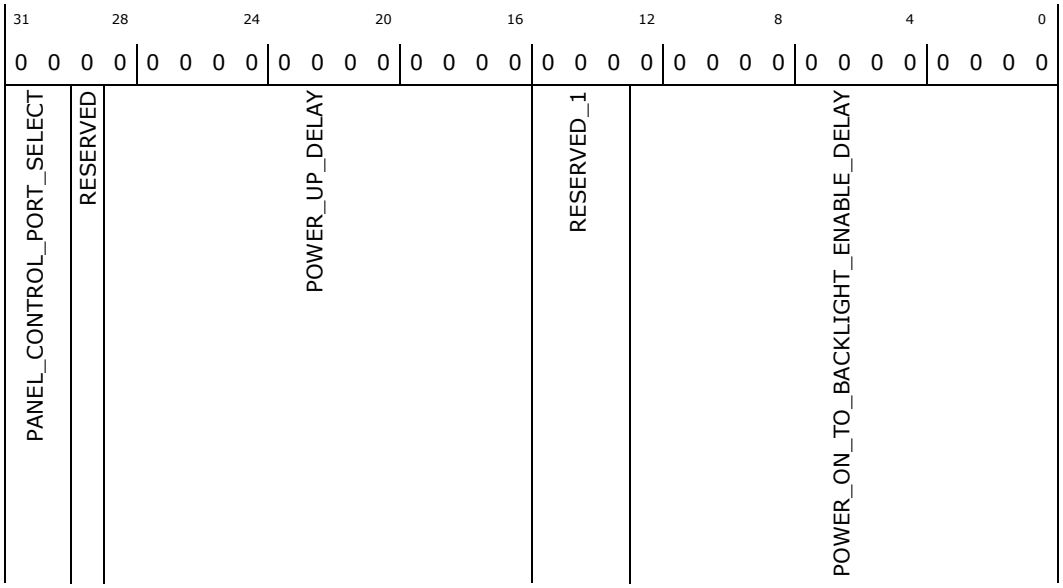
4.2.268 PIPEA_PP_ON_DELAYS—Offset 61208h

PipeA Panel Power on Sequencing Delays PP On Delay values (dplrreg.v DPLRppon_sd)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61208h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**PANEL_CONTROL_PORT_SELECT:** These bits define to which port the embedded panel is connected. This is used for automatic control of the panel power. If the selected port is disabled or if the port is not on pipe-B, then, the power sequence will not allow a panel power up. 00 = Reserved 01 = Panel is connected to the embedded DisplayPort B 10 = Panel is connected to the embedded DisplayPort C 11 = Reserved The selection of non-existent ports are not allowed. This programming will disable panel power sequencing logic.
29	0x0 RO	**RESERVED:** Reserved.
28:16	0x0 RW	**POWER_UP_DELAY:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T1+T2 time sequence. The time unit used is the 100us timer.
15:13	0x0 RO	**RESERVED_1:** Reserved.
12:0	0x0 RW	**POWER_ON_TO_BACKLIGHT_ENABLE_DELAY:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T5 (T3 for DisplayPort) time sequence. The time unit used is the 100us timer.

4.2.269 PIPEA_PP_OFF_DELAYS—Offset 6120Ch

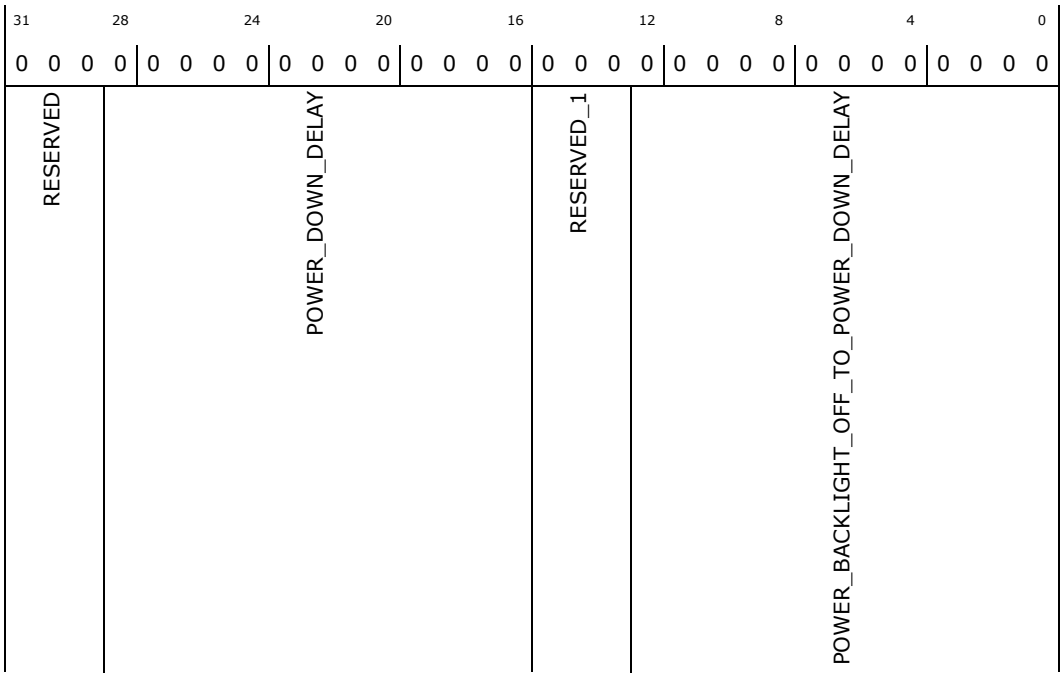
PipeA Panel Power off Sequencing Delays PP Delay Off values (dplrreg.v DPLRppoff_sd)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6120Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Reserved.
28:16	0x0 RW	**POWER_DOWN_DELAY:** Programmable value of panel power sequencing delay during power up. This provides the time delay for the T3 (T5 for DisplayPort) time sequence. The time unit used is the 100us timer.
15:13	0x0 RO	**RESERVED_1:** Reserved.
12:0	0x0 RW	**POWER_BACKLIGHT_OFF_TO_POWER_DOWN_DELAY:** Programmable value of panel power sequencing delay during power down. This provides the time delay for the Tx (T4 for DisplayPort) time sequence. The time unit used is the 100us timer.

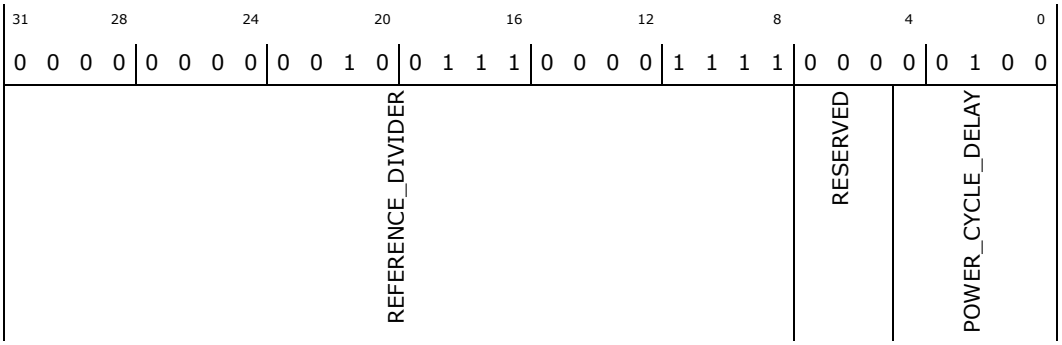
4.2.270 PIPEA_PP_DIVISOR—Offset 61210h

PipeA Panel Power Cycle Delay and Reference Divisor PP Divisor (dplrreg.v DPLRrefdiv_pp_cd)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61210h

Default: 00270F04h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x270f RW	**REFERENCE_DIVIDER:** This field provides the value of the divider used for the creation of the panel timer reference clock. The output of the divider is used as the fastest of the three time bases (100us) for all other timers. The other time bases are divided from this frequency. The value of zero should not be used. When it is desired to divide by N, the actual value to be programmed is (N/2)-1. The value should be (100*RefinMHz/2)-1. The default value assumes the default value for the display core clock that is for [DevCL and DevCTG] a 200MHz reference value. The following are examples for other memory speeds. Display Core Frequency Value of Field 233MHz 2D81h 200MHz 270Fh 133MHz 19F9h
7:5	0x0 RO	**RESERVED:** Reserved.
4:0	0x4 RW	**POWER_CYCLE_DELAY:** Programmable value of time panel must remain in a powered down state after powering down. For devices coming out of reset, the default values will define how much time must pass before a power on sequence can be started. This field uses the .1 S time base unit from the divider. If the panel power on sequence is attempted during this delay, the power on sequence will commence once the power cycle delay is complete. Writing a value of 0 selects no delay or is used to abort the delay if it is active. During the initial power up reset, a D3 cold power cycle, or a user instigated system reset, the timer will be set to the default value and the count down will begin after the de-assertion of reset. Writing this field to a zero while the count is active will abort this portion of the sequence. This corresponds to the T4 of the SPWG specification. Note: Even if the panel is not enabled, the T4 count happens after reset. This register needs to be programmed to a +1 value. For instance for meeting the SPWG specification of 400mS, program 5 to achieve at least 400mS delay prior to powerup.

4.2.271 PFIT_CONTROL—Offset 61230h

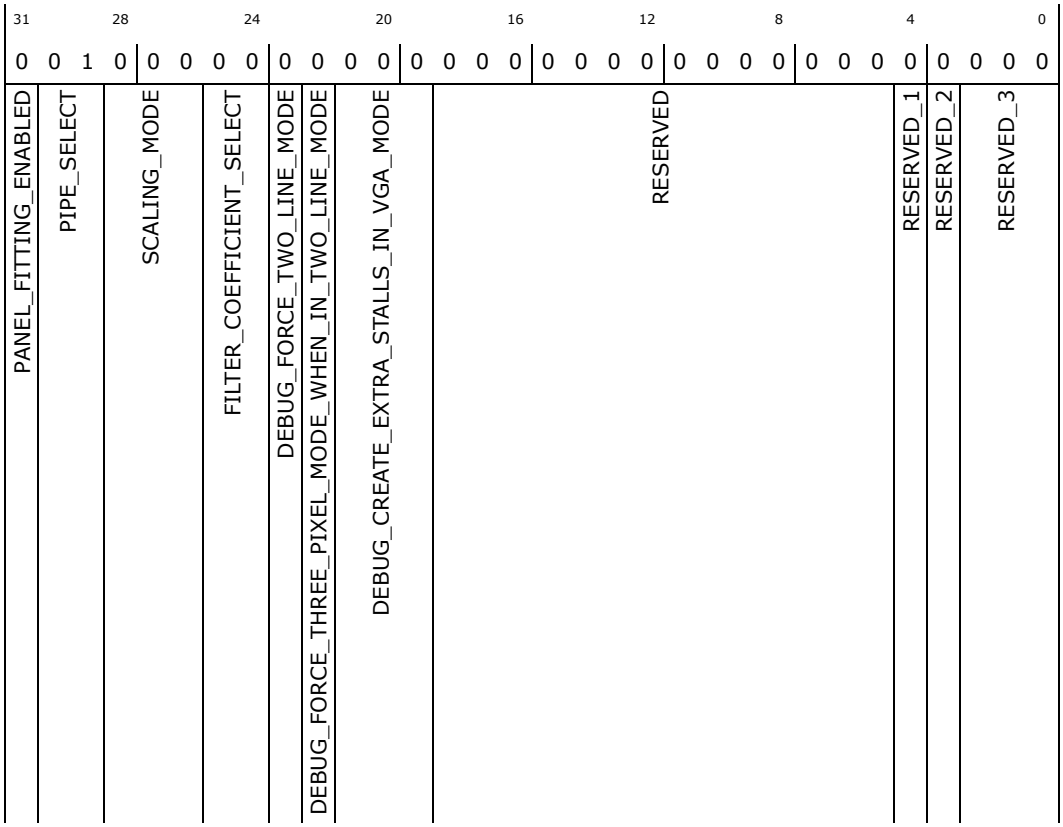
Panel Fitting Controls

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61230h

Default: 20000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**PANEL_FITTING_ENABLED:** Disables the panel fitting function by forcing pixels to bypass. Panel fitting should be enabled or disabled before the pipe is enabled. 0 = Bypass the panel fitting (1:1 ratio) 1 = Enable panel fitting (Ratios include 1:1)
30:29	0x1 RW	**PIPE_SELECT:** Indicates the pipe attached to the panel fitter 00 = Panel fitter is attached to Display Pipe A. 01 = Panel fitter is attached to Display Pipe B. This is the default after reset. 10 = Reserved for pipe C 11 = Reserved for pipe D

Bit Range	Default & Access	Field Name (ID): Description
28:26	0x0 RW	**SCALING_MODE:** 000 = Auto-scale (source and destination should have the same aspect ratios) 001 = Programmed scaling: Values in register 61234h will be used for horizontal and vertical scaling factors 010 = Pillarbox (example: 4:3 to 16:9 auto conversion) use only when destination has wider aspect ratio than source 011 = Letterbox (example: 16:9 to 4:3 auto conversion) use only when destination has taller aspect ratio than source 1xx = Reserved
25:24	0x0 RW	**FILTER_COEFFICIENT_SELECT:** Selects the set of predefined filter coefficients to use for panel fitting 00 = Fuzzy filtering 01 = Crisp edge enhancing filtering 10 = Median between fuzzy and crisp filtering 11 = Reserved
23	0x0 RW	**DEBUG_FORCE_TWO_LINE_MODE:** Reserved.
22	0x0 RW	**DEBUG_FORCE_THREE_PIXEL_MODE_WHEN_IN_TWO_LINE_MODE:** Reserved.
18:5	0x0 RO	**RESERVED:** Reserved.
4	0x0 RO	**RESERVED_1:** (was Force One Line Mode) write as zero
3	0x0 RO	**RESERVED_2:** (was Dither Enable which moved to register 61180h)
2:0	0x0 RO	**RESERVED_3:** Reserved.

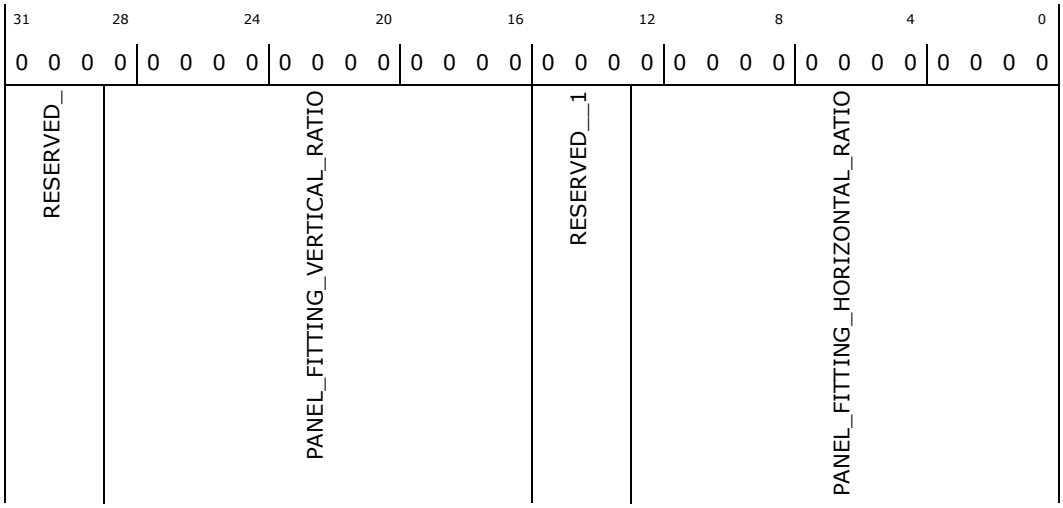
4.2.272 PFIT_PGM_RATIOS—Offset 61234h

Programmed Panel Fitting Ratios

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61234h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED_:** Reads as zeros
28:16	0x0 RW	**PANEL_FITTING_VERTICAL_RATIO:** Vertical scaling ratio for panel fitting.
15:13	0x0 RO	**RESERVED__1:** Reads as zeros
12:0	0x0 RW	**PANEL_FITTING_HORIZONTAL_RATIO:** Horizontal scaling ratio for panel fitting.

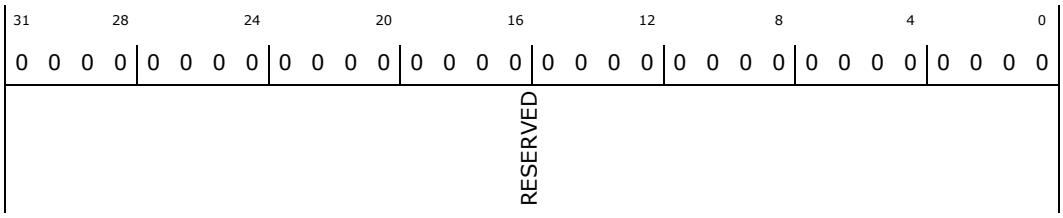
4.2.273 RESERVEDUSEDTOBEAUTOSCALINGRATIOSREADBACK—Offset 61238h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61238h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RESERVED:** Reserved.

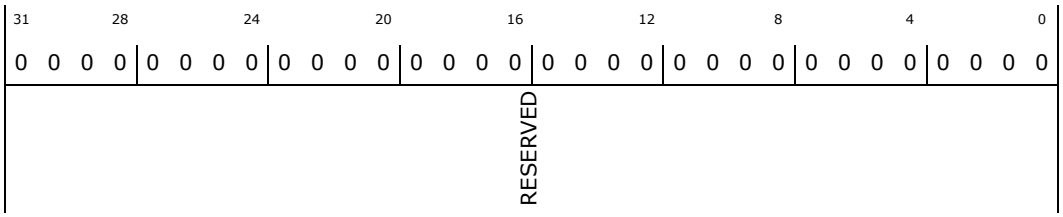
4.2.274 RESERVEDUSEDTOBESCALINGINITIALPHASE—Offset 6123Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6123Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RESERVED:** Reserved.

4.2.275 PIPEA_BLC_PWM_CLT2—Offset 61250h

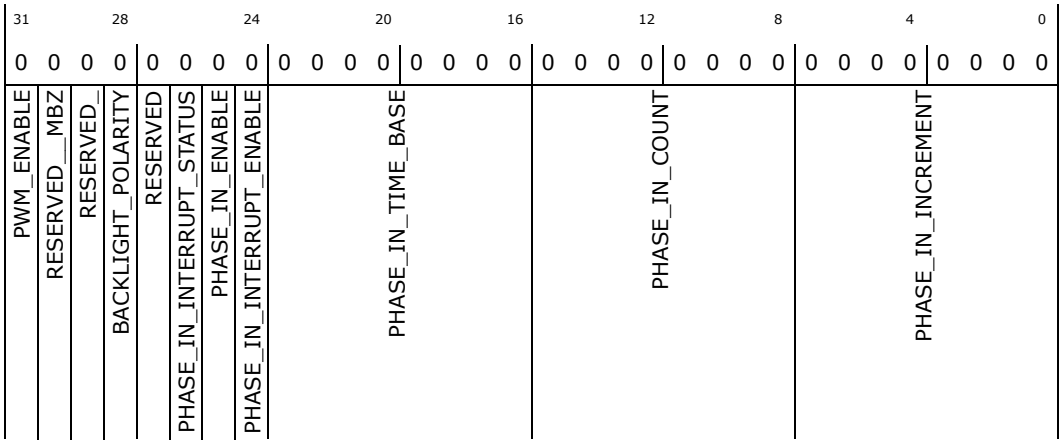
PipeA Backlight PWM Control Register 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61250h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**PWM_ENABLE:** This bit enables the PWM counter logic 0 = PWM disabled (drives 0 always) 1 = PWM enabled

Bit Range	Default & Access	Field Name (ID): Description
30	0x0 RO	**RESERVED__MBZ:** Reserved.
29	0x0 RO	**RESERVED_:** Reserved.
28	0x0 RW	**BACKLIGHT_POLARITY:** This field controls the polarity of the PWM signal. 0 = Active High 1 = Active Low
27	0x0 RO	**RESERVED:** MBZ
26	0x0 RW/1C	**PHASE_IN_INTERRUPT_STATUS:** This bit will be set by hardware when a Phase-In interrupt has occurred. Software will clear this bit by writing a 1 , which will reset the interrupt generation. [DevCL-A,B] Reserved AccessType: One to Clear
25	0x0 RW	**PHASE_IN_ENABLE:** Setting this bit enables a PWM phase in based on the programming of the Phase In registers below. This bit clears itself when the phase in is completed.
24	0x0 RW	**PHASE_IN_INTERRUPT_ENABLE:** Setting this bit enables an interrupt to be generated when the PWM phase in is completed.
23:16	0x0 RW	**PHASE_IN_TIME_BASE:** This field determines the number of VBLANK events that pass before one increment occurs. 0 = invalid 1 = 1 vblank 2 = 2 vblanks etc.
15:8	0x0 RW	**PHASE_IN_COUNT:** This field determines the number of increment events in this phase in. Writes to this register should only occur when hardware-phase-ins are disabled. Reads to this register can occur any time, where the value in this field indicates the number of increment events remaining to fully apply a phase-in request as hardware automatically decrements this value. A value of 0 is invalid. In order to write the same value to this field for the second time, one must write a dummy value to this field, for example, 0 , before writing the real value for the second time.
7:0	0x0 RW	**PHASE_IN_INCREMENT:** This field indicates the amount to adjust the PWM duty cycle register on each increment event. This is a two s complement number.

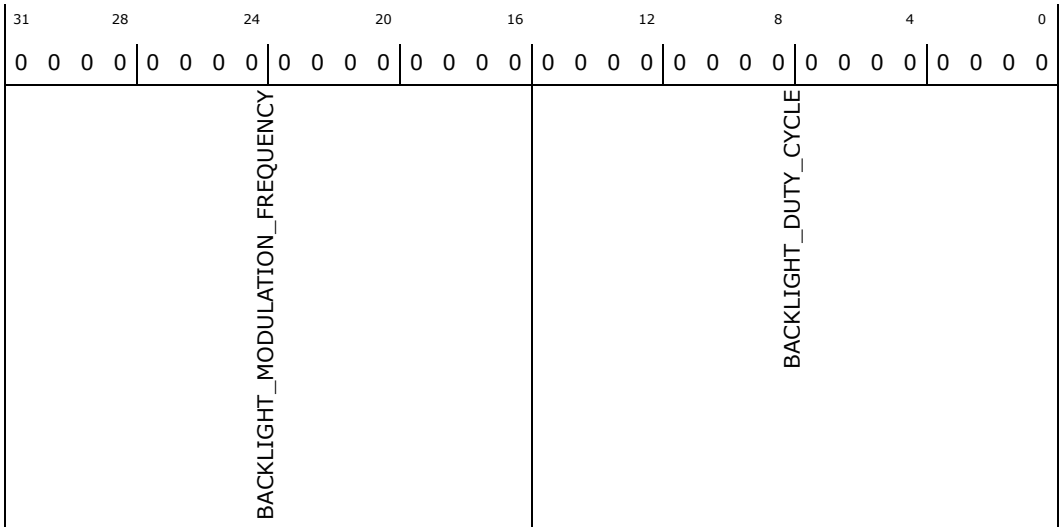
4.2.276 PIPEA_BLC_PWM_CTL—Offset 61254h

PipeA Backlight PWM Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61254h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**BACKLIGHT_MODULATION_FREQUENCY:** This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is normally set once during initialization based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in display core clocks ([DevCTG] 100MHz HRAW clocks) multiplied by 128 or 25MHz S0IX clocks multiplied by 16.
15:0	0x0 RW	**BACKLIGHT_DUTY_CYCLE:** This field determines the number of time base events for the active portion of the PWM backlight control. This should never be larger than the frequency field. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. This field gets updated when it is desired to change the intensity of the backlight, it will take affect at the end of the current PWM cycle. This value represents the active time of the PWM stream in display core clock ([DevCTG] HRAW clock) periods multiplied by 128 or 25MHz S0IX clocks multiplied by 16.

4.2.277 PIPEA_BLM_HIST_CTL—Offset 61260h

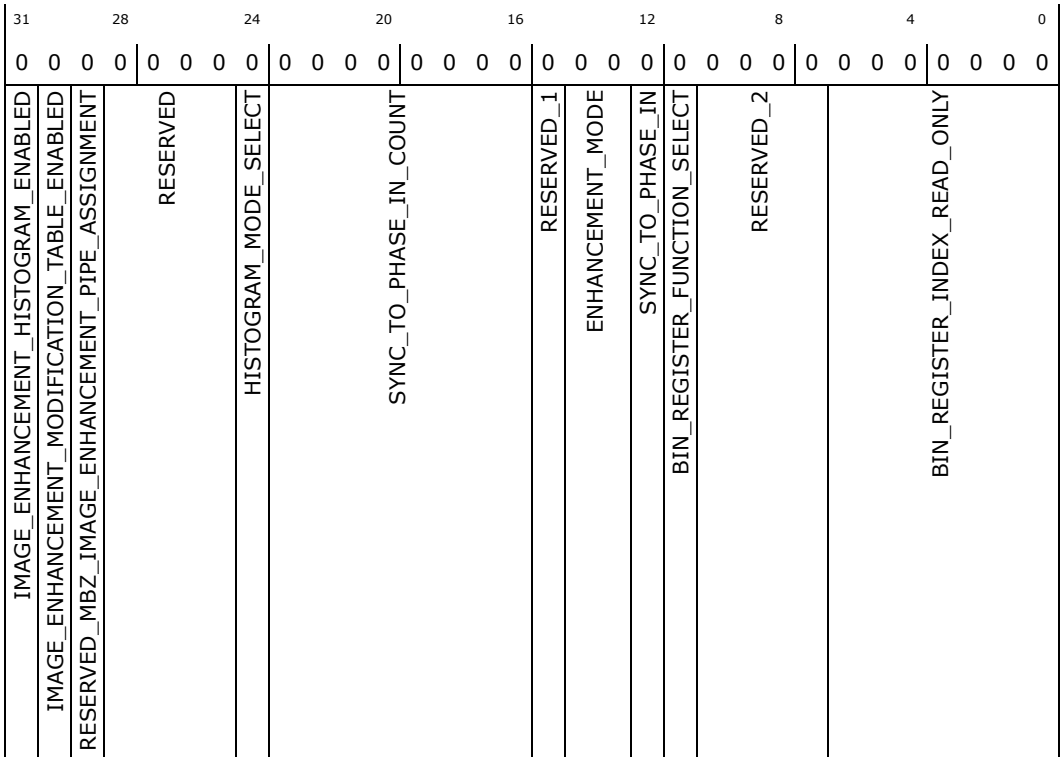
PipeA Image Enhancement Histogram Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61260h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**IMAGE_ENHANCEMENT_HISTOGRAM_ENABLED:** This bit enables the Image Enhancement histogram logic to collect data. 0 = Image histogram is disabled 1 = The Image histogram is enabled. When this bit is changed from a zero to a one, histogram calculations will begin after the next VBLANK of the assigned pipe.
30	0x0 RW	**IMAGE_ENHANCEMENT_MODIFICATION_TABLE_ENABLED:** This bit enables the Image Enhancement modification table. 0 = disabled 1 = enabled. When this bit is changed from a zero to a one, modifications begin after the next VBLANK of the assigned pipe.
29	0x0 RO	**RESERVED_MBZ_IMAGE_ENHANCEMENT_PIPE_ASSIGNMENT:** Each pipe has its own IE function
28:25	0x0 RO	**RESERVED:** Always write as 0 s.
24	0x0 RW	**HISTOGRAM_MODE_SELECT:** 0: YUV Luma Mode 1: HSV Intensity Mode - Reserved on [DevCL]
23:16	0x0 RW	**SYNC_TO_PHASE_IN_COUNT:** This field indicates the phase in count number on which the Image Enhancement table will be loaded if the Sync to Phase in is enabled.
15	0x0 RO	**RESERVED_1:** Always write as 0.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0x0 RW	**ENHANCEMENT_MODE:** 00: Direct look up mode 01: Additive mode 10: Multiplicative mode - Reserved on [DevCL] 11: Reserved
12	0x0 RW	**SYNC_TO_PHASE_IN:** Setting this bit enables the double buffered registers to be loaded on the phase in count value specified instead of the next vblank.
11	0x0 RW	**BIN_REGISTER_FUNCTION_SELECT:** This field indicates what data is being written to or read from the bin data register. 0 = Bin Threshold Count. A read from the bin data register returns that bin s threshold value from the most recent vblank load event (guardband threshold trip). Valid range for the Bin Index is 0 to 31. 1 = Bin Image Enhancement Value. Valid range for the Bin Index is 0 to 32
10:7	0x0 RO	**RESERVED_2:** Always write as 0's.
6:0	0x0 RW	**BIN_REGISTER_INDEX_READ_ONLY:** This field indicates the bin number whose data can be accessed through the bin data register. This value is automatically incremented by a read or a write to the bin data register if the busy bit is not set.

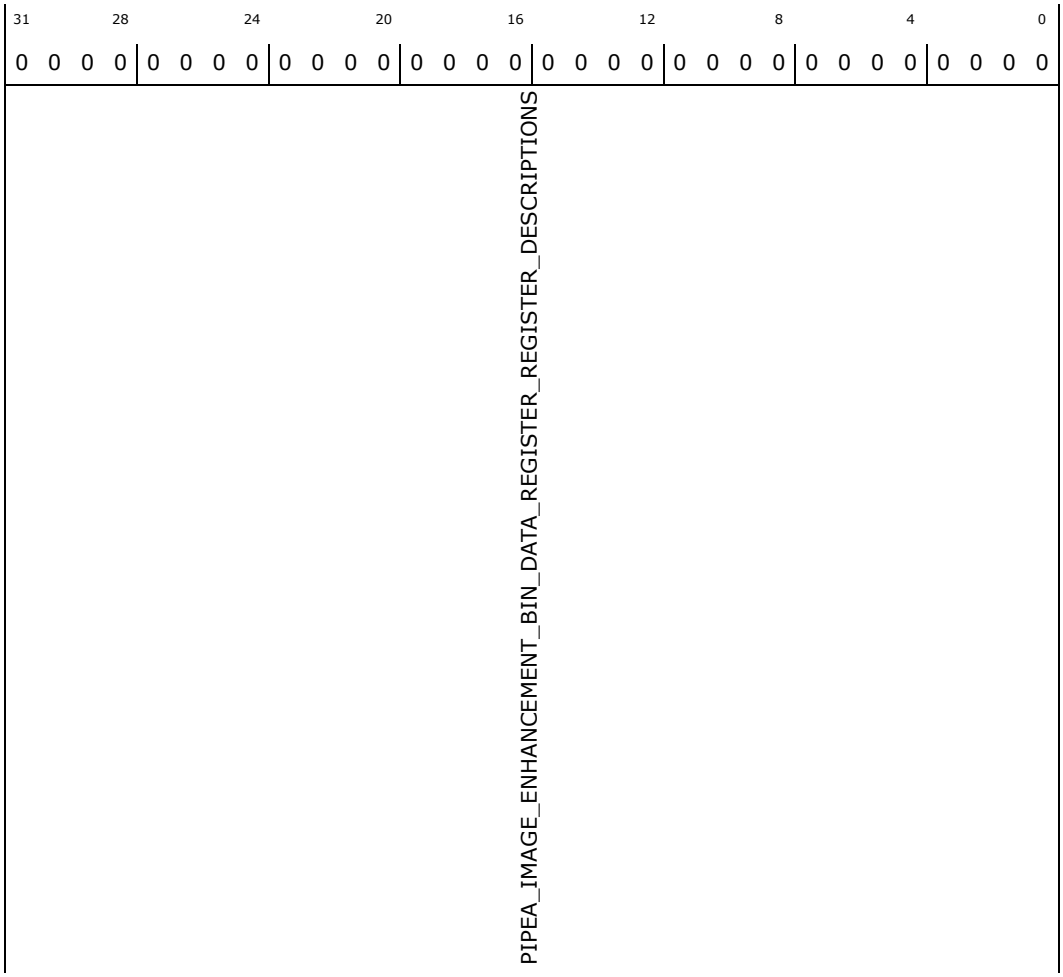
4.2.278 PIPEA_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER—Offset 61264h

PIPEA_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER index registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61264h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**PIPEA_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER_REGISTER_DESCRIPTIONS:** PIPEA_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER indexed register descriptions

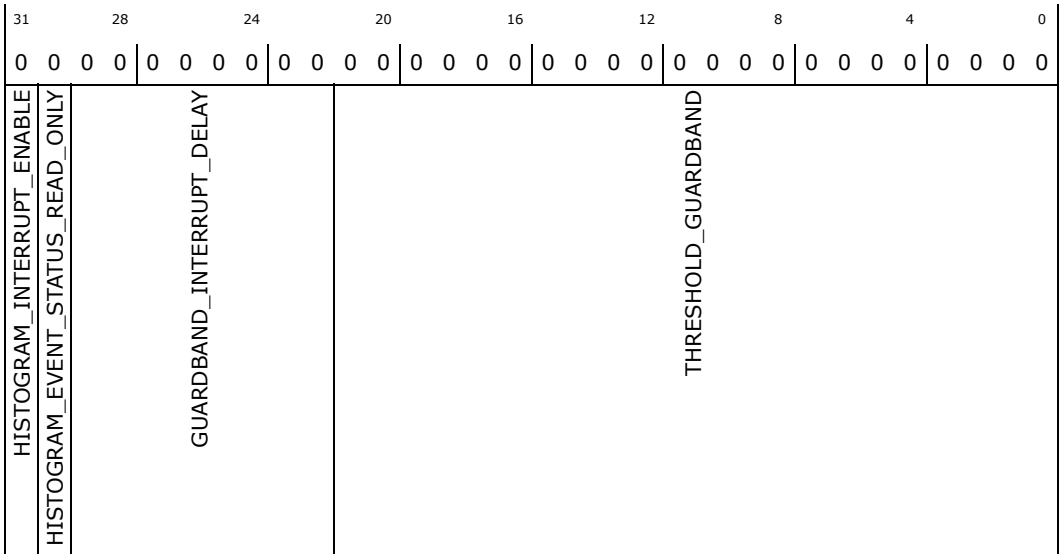
4.2.279 PIPEAHISTOGRAMTHRESHOLDGUARDBANDREGISTER—Offset 61268h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61268h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**HISTOGRAM_INTERRUPT_ENABLE:** 0 = Disabled 1 = Enabled. This generates a histogram interrupt once a Histogram event occurs.
30	0x0 RO	**HISTOGRAM_EVENT_STATUS_READ_ONLY:** When a Histogram event has occurred, this will get set by the hardware. For any more Histogram events to occur, the software needs to clear this bit by writing a '1'. The default state for this bit is '0'. 0 = Histogram event has not occurred. 1 = Histogram event has occurred. AccessType: Read Only
29:22	0x0 RW	**GUARDBAND_INTERRUPT_DELAY:** An interrupt is generated after this many consecutive frames of the guardband threshold being surpassed. This value is double buffered on start of vblank. A value of 0 is invalid.
21:0	0x0 RW	**THRESHOLD_GUARDBAND:** This value is used to determine the guardband for the threshold interrupt generation. This single value is used for all the segments. This value is double buffered on start of vblank

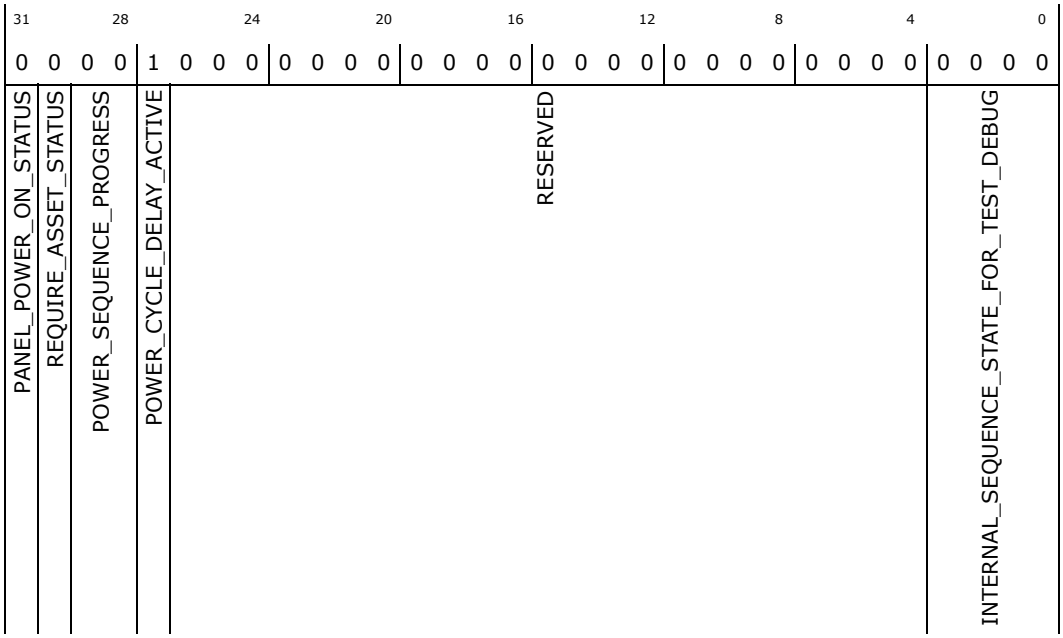
4.2.280 PIPEB_PP_STATUS—Offset 61300h

PipeB Panel Power Status Register PP Status (dplrreg.v panel_pwr_sr)

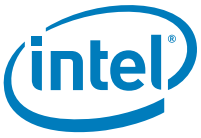
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61300h

Default: 08000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**PANEL_POWER_ON_STATUS:** 0 = Indicates that the panel power down sequencing has completed. A power cycle delay may be currently active. It is safe and allowed to program pipe timing and DPLL registers. If this bit is not a zero, it activates the register write protect and writes to those registers will be ignored unless the write protect key value is set in the panel sequencing control register. 1 = In conjunction with bits Power Sequence Progress field and Power Cycle Delay Active, this bit set to a one indicates that the panel is currently powered up or is currently in the power down sequence and it is unsafe to change the pipe timing and DPLL registers for the pipe that is assigned to the embedded panel output. If the embedded panel port is selected as the target for the panel control, Software is responsible for enabling the LCD display by writing a 1 to the port enable bit only after all pipe timing, DPLL registers are properly programmed, and the PLL has locked to the reference signal. This bit is cleared (set to 0) only after the panel power down sequencing is completed.
30	0x0 RO	**REQUIRE_ASSET_STATUS:** This bit indicates the status of programming of the display PLL and the selected display port. This a power on cycle will not be allowed unless this status indicates that the required assets are programmed and ready for use. 0 = All required assets are not properly programmed. 1 = All required assets are ready for the driving of a panel. The following conditions determine that the assets are ready: 1) Display Pipe PLL Enabled and frequency locked (bit-31 of DPLL Control Register for the pipe attached to the embedded panel port). 2) Display Pipe Enabled (bit-31 of PIPECONF Pipe Configuration Register. For the pipe attached to the embedded panel port) 3) Embedded Panel Port is Programmed Enabled



Bit Range	Default & Access	Field Name (ID): Description
29:28	0x0 RO	**POWER_SEQUENCE_PROGRESS:** 00 = Indicates that the panel is not in a power sequence 01 = Indicates that the panel is in a power up sequence (may include power cycle delay) 10 = Indicates that the panel is in a power down sequence 11 = Reserved
27	0x1 RO	**POWER_CYCLE_DELAY_ACTIVE:** Power cycle delays occur after a panel power down sequence or after a hardware reset. On reset, a power cycle delay will occur using the default value for the timing. 0 = A power cycle delay is not currently active 1 = A power cycle delay (T4) is currently active
26:4	0x0 RO	**RESERVED:** Reserved.
3:0	0x0 RO	**INTERNAL_SEQUENCE_STATE_FOR_TEST_DEBUG:** 0000 = Power Off Idle (S0.0) 0001 = Power Off, Wait for cycle delay (S0.1) 0010 = Power Off (S0.2) 0011 = Power Off (S0.3) 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = Power On Idle (S1.0) 1001 = Power On, (S1.1) 1010 = Power On, (S1.2) 1011 = Power On, Wait for cycle delay (S1.3) 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reset

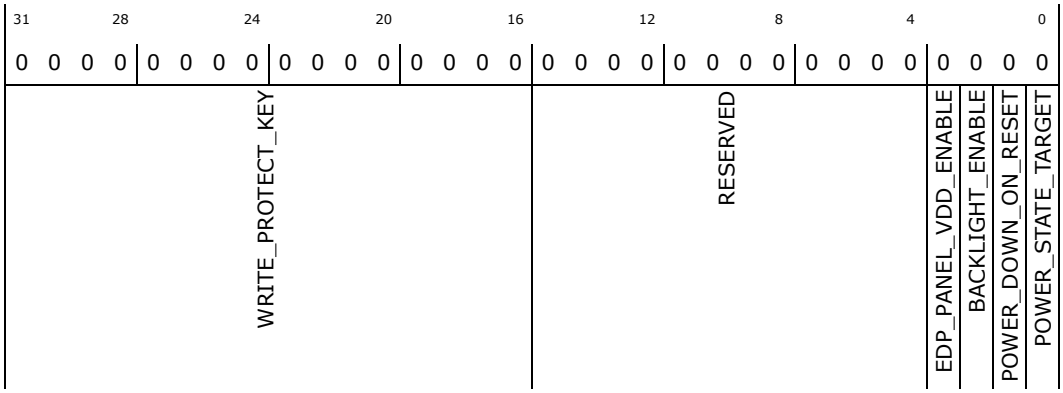
4.2.281 PIPEB_PP_CONTROL—Offset 61304h

PipeB Panel Power Control Register PP Control (dplrreg.v pnl_pwr_cntl)

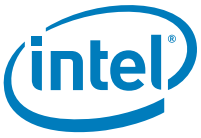
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61304h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**WRITE_PROTECT_KEY:** ABCD Write protect off When this field is programmed to anything except the write protect off setting and the panel is either powered up or in the process of a power up sequence, a set of registers involved in generation of panel timing or control become write protected. Any write cycles to those write protected registers, while they will complete as normal, will not change the value of the register when write protected. When this register field contains the write protect off key value, write protect will be unconditionally disabled. In situations where the embedded panel port is unused, the port should remain powered down and the write protect will be inactive. This field in normal operation should be left to all zeros and never programmed with the key value. It exists only to allow testing and workarounds. List of Write protected registers: (Panel sequencing Registers): Pipe B Panel power on sequencing delays - Address: 61308-6130Bh Pipe B Panel power off sequencing delays Address: 6130Ch 6130Fh Pipe B Panel power cycle delay and Reference Divisor Address: 61310h 61313 (DPLL registers): DPLL Control Registers FPA0 DPLL Divisor Register FPA1 DPLL Divisor Register 1 FPB0 DPLL Divisor Register FPB1 DPLL Divisor Register 1 (Display Pipe timing registers except source size) HTOTAL Horizontal Total Register HBLANK Horizontal Blank Register HSYNC_ Horizontal Sync Register VTOTAL_ Vertical Total Register VBLANK_ Vertical Blank Register VSYNC_ Vertical Sync Register
15:4	0x0 RO	**RESERVED:** Reserved.



Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**EDP_PANEL_VDD_ENABLE:** : Enabling this bit enables the panel vdd if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit for eDP link training. After eDP link training is done, software must disable it and let the normal panel power sequencing to take control. 0 = eDP panel Vdd disabled 1 = eDP panel Vdd enabled [DevCLN] Reserved
2	0x0 RW	**BACKLIGHT_ENABLE:** Enabling this bit enables the panel backlight if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit after training the link, and disable it when disabling the panel power state target. 0 = Backlight disabled 1 = Backlight enabled [DevCL] Reserved
1	0x0 RW	**POWER_DOWN_ON_RESET:** Enabling this bit causes the panel to power down when a reset warning comes to the GMCH from the ICH. When system reset is initiated, the embedded panel port automatically begins the panel power down sequence. If the panel is not on during a reset event, this bit is ignored. 0 = Do not run panel power down sequence when reset is detected 1 = Run panel power down sequence when system is reset
0	0x0 RW	**POWER_STATE_TARGET:** Writing this bit can occur any time, it will only be used at the completion of any current power cycle. 0 = The panel power state target is off, if the panel is either on or in a power on sequence, a power off sequence is started as soon as the panel reaches the power on state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. 1= The panel power state target is on, if the panel is in either the off state or a power off sequence, if all pre-conditions are met, a power on sequence is started as soon as the panel reaches the power off state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. While the panel is on or in a power on sequence, the register write lock will be enabled.

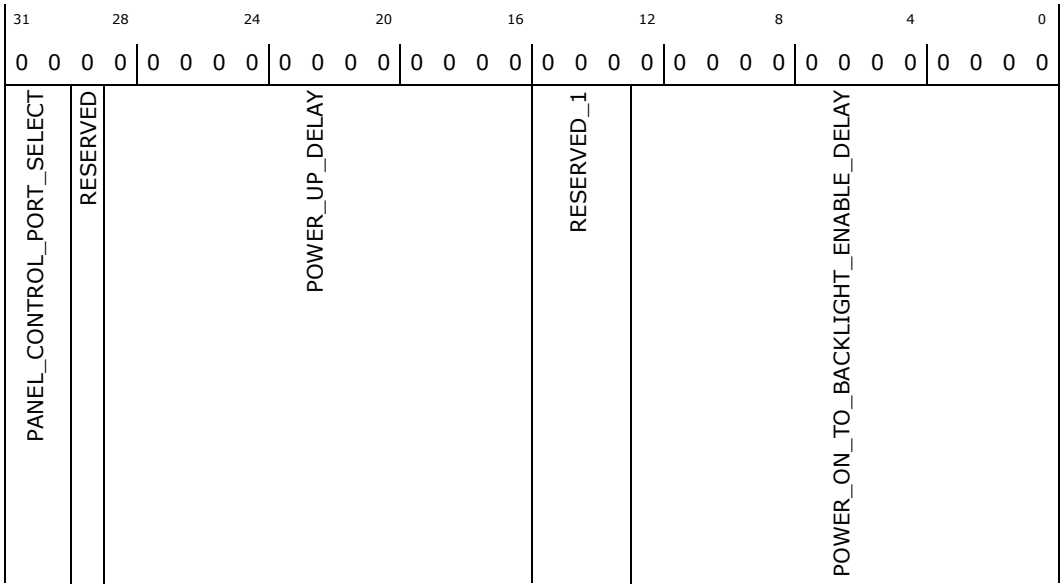
4.2.282 PIPEB_PP_ON_DELAYS—Offset 61308h

PipeB Panel Power on Sequencing Delays PP On Delay values (dplrreg.vDPLRppon_sd)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61308h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**PANEL_CONTROL_PORT_SELECT:** These bits define to which port the embedded panel is connected. This is used for automatic control of the panel power. If the selected port is disabled or if the port is not on pipe-B, then, the power sequence will not allow a panel power up. 00 = Reserved 01 = Panel is connected to the embedded DisplayPort B 10 = Panel is connected to the embedded DisplayPort C 11 = Reserved The selection of non-existent ports are not allowed. This programming will disable panel power sequencing logic.
29	0x0 RO	**RESERVED:** Reserved.
28:16	0x0 RW	**POWER_UP_DELAY:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T1+T2 time sequence. The time unit used is the 100us timer.
15:13	0x0 RO	**RESERVED_1:** Reserved.
12:0	0x0 RW	**POWER_ON_TO_BACKLIGHT_ENABLE_DELAY:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T5 (T3 for DisplayPort) time sequence. The time unit used is the 100us timer.

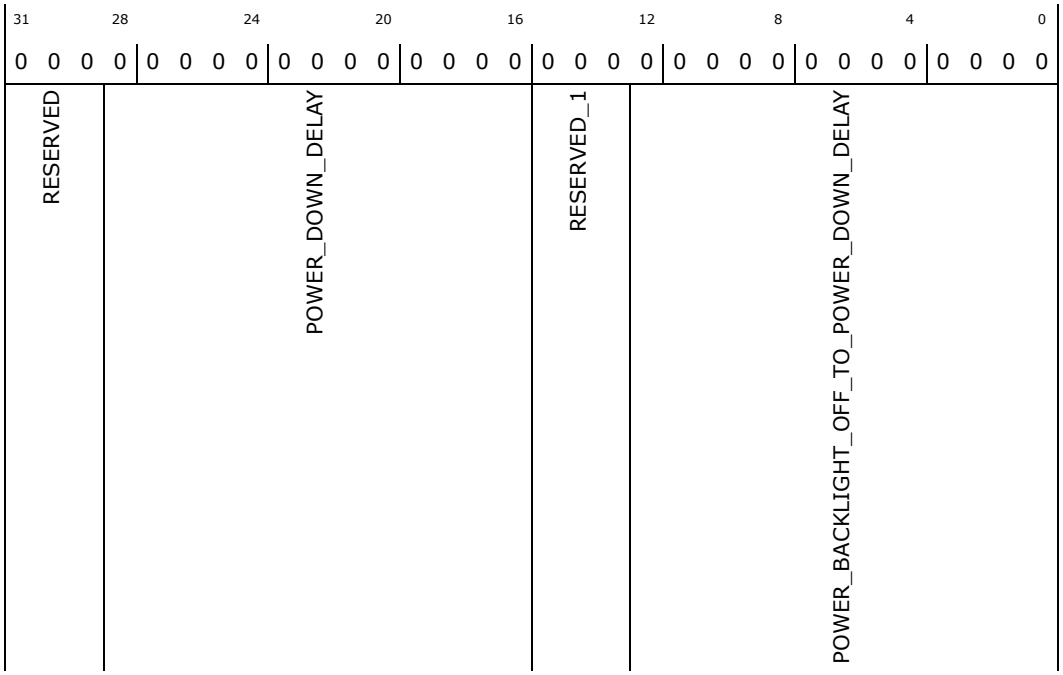
4.2.283 PIPEB_PP_OFF_DELAYS—Offset 6130Ch

PipeB Panel Power off Sequencing Delays PP Delay Off values (dplrreg.v DPLRppoff_sd)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6130Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Reserved.
28:16	0x0 RW	**POWER_DOWN_DELAY:** Programmable value of panel power sequencing delay during power up. This provides the time delay for the T3 (T5 for DisplayPort) time sequence. The time unit used is the 100us timer.
15:13	0x0 RO	**RESERVED_1:** Reserved.
12:0	0x0 RW	**POWER_BACKLIGHT_OFF_TO_POWER_DOWN_DELAY:** Programmable value of panel power sequencing delay during power down. This provides the time delay for the Tx (T4 for DisplayPort) time sequence. The time unit used is the 100us timer.

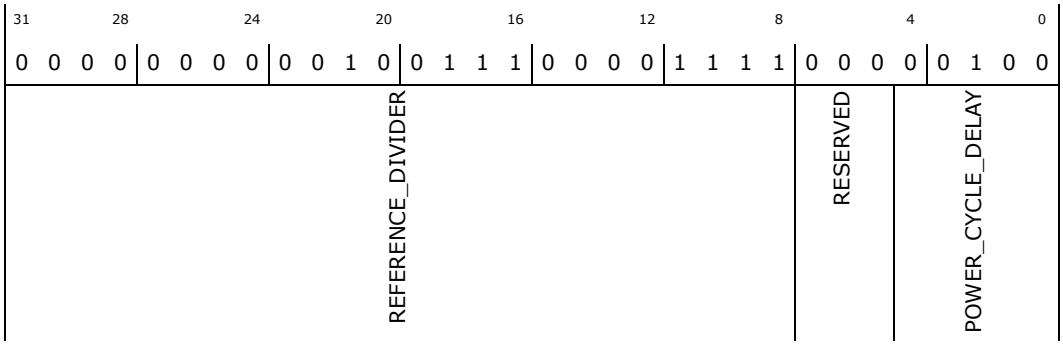
4.2.284 PIPEB_PP_DIVISOR—Offset 61310h

PipeB Panel Power Cycle Delay and Reference Divisor PP Divisor (dplrreg.v DPLRrefdiv_pp_cd)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61310h

Default: 00270F04h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x270f RW	**REFERENCE_DIVIDER:** This field provides the value of the divider used for the creation of the panel timer reference clock. The output of the divider is used as the fastest of the three time bases (100us) for all other timers. The other time bases are divided from this frequency. The value of zero should not be used. When it is desired to divide by N, the actual value to be programmed is (N/2)-1. The value should be (100*RefinMHz/2)-1. The default value assumes the default value for the display core clock that is for [DevCL and DevCTG] a 200MHz reference value. The following are examples for other memory speeds. Display Core Frequency Value of Field 233MHz 2D81h 200MHz 270Fh 133MHz 19F9h
7:5	0x0 RO	**RESERVED:** Reserved.
4:0	0x4 RW	**POWER_CYCLE_DELAY:** Programmable value of time panel must remain in a powered down state after powering down. For devices coming out of reset, the default values will define how much time must pass before a power on sequence can be started. This field uses the .1 S time base unit from the divider. If the panel power on sequence is attempted during this delay, the power on sequence will commence once the power cycle delay is complete. Writing a value of 0 selects no delay or is used to abort the delay if it is active. During the initial power up reset, a D3 cold power cycle, or a user instigated system reset, the timer will be set to the default value and the count down will begin after the de-assertion of reset. Writing this field to a zero while the count is active will abort this portion of the sequence. This corresponds to the T4 of the SPWG specification. Note: Even if the panel is not enabled, the T4 count happens after reset. This register needs to be programmed to a +1 value. For instance for meeting the SPWG specification of 400mS, program 5 to achieve at least 400mS delay prior to powerup.

4.2.285 PIPEB_BLC_PWM_CLT2—Offset 61350h

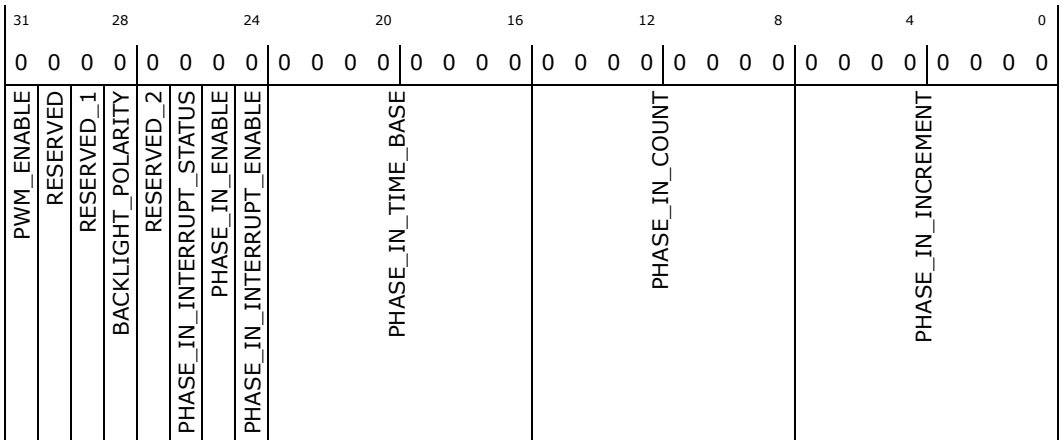
PipeB Backlight PWM Control Register 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61350h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**PWM_ENABLE:** This bit enables the PWM counter logic 0 = PWM disabled (drives 0 always) 1 = PWM enabled
30	0x0 RO	**RESERVED:** MBZ
29	0x0 RO	**RESERVED_1:** Reserved.
28	0x0 RW	**BACKLIGHT_POLARITY:** This field controls the polarity of the PWM signal. 0 = Active High 1 = Active Low
27	0x0 RO	**RESERVED_2:** MBZ
26	0x0 RW/1C	**PHASE_IN_INTERRUPT_STATUS:** This bit will be set by hardware when a Phase-In interrupt has occurred. Software will clear this bit by writing a 1 , which will reset the interrupt generation. [DevCL-A,B] Reserved AccessType: One to Clear
25	0x0 RW	**PHASE_IN_ENABLE:** Setting this bit enables a PWM phase in based on the programming of the Phase In registers below. This bit clears itself when the phase in is completed.
24	0x0 RW	**PHASE_IN_INTERRUPT_ENABLE:** Setting this bit enables an interrupt to be generated when the PWM phase in is completed.
23:16	0x0 RW	**PHASE_IN_TIME_BASE:** This field determines the number of VBLANK events that pass before one increment occurs. 0 = invalid 1 = 1 vblank 2 = 2 vblanks etc.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RW	**PHASE_IN_COUNT:** This field determines the number of increment events in this phase in. Writes to this register should only occur when hardware-phase-ins are disabled. Reads to this register can occur any time, where the value in this field indicates the number of increment events remaining to fully apply a phase-in request as hardware automatically decrements this value. A value of 0 is invalid. In order to write the same value to this field for the second time, one must write a dummy value to this field, for example, 0 , before writing the real value for the second time.
7:0	0x0 RW	**PHASE_IN_INCREMENT:** This field indicates the amount to adjust the PWM duty cycle register on each increment event. This is a two s complement number.

4.2.286 PIPEB_BLC_PWM_CTL—Offset 61354h

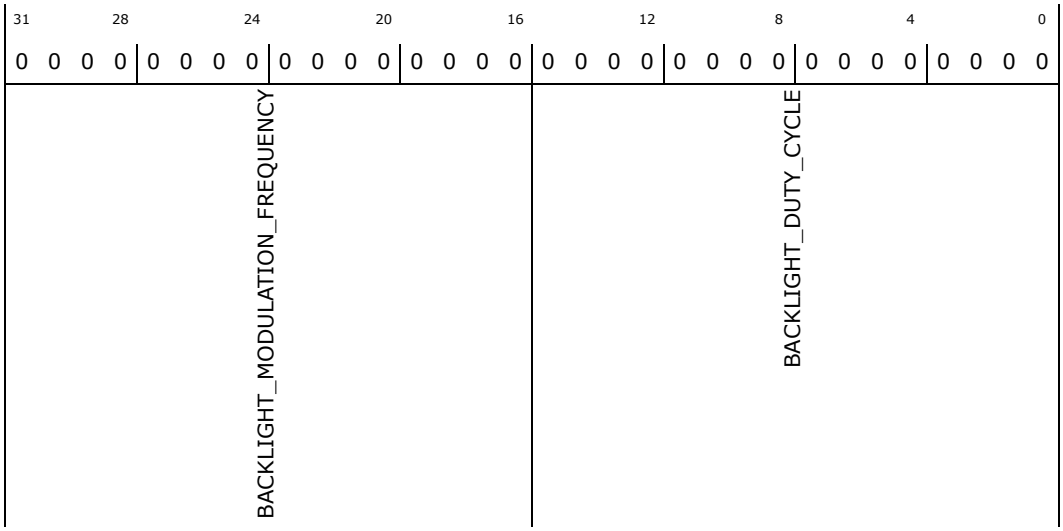
PipeB Backlight PWM Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61354h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**BACKLIGHT_MODULATION_FREQUENCY:** This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is normally set once during initialization based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in display core clocks ([DevCTG] HRAW clocks) multiplied by 128 or 25MHz S0IX clocks multiplied by 16.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW	**BACKLIGHT_DUTY_CYCLE:** This field determines the number of time base events for the active portion of the PWM backlight control. This should never be larger than the frequency field. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. This field gets updated when it is desired to change the intensity of the backlight, it will take affect at the end of the current PWM cycle. This value represents the active time of the PWM stream in display core clock ([DevCTG] HRAW clock) periods multiplied by 128 or 25MHz S0IX clocks multiplied by 16.

4.2.287 PIPEB_BLM_HIST_CTL—Offset 61360h

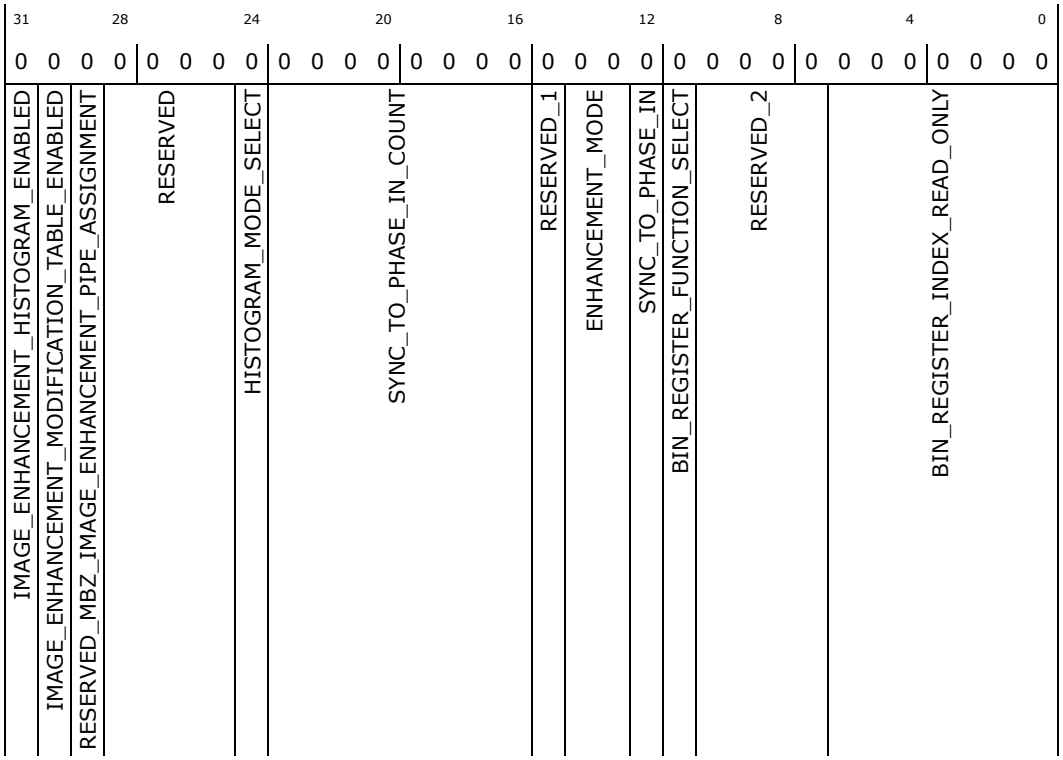
PipeB Image Enhancement Histogram Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61360h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**IMAGE_ENHANCEMENT_HISTOGRAM_ENABLED:** This bit enables the Image Enhancement histogram logic to collect data. 0 = Image histogram is disabled 1 = The Image histogram is enabled. When this bit is changed from a zero to a one, histogram calculations will begin after the next VBLANK of the assigned pipe.
30	0x0 RW	**IMAGE_ENHANCEMENT_MODIFICATION_TABLE_ENABLED:** This bit enables the Image Enhancement modification table. 0 = disabled 1 = enabled. When this bit is changed from a zero to a one, modifications begin after the next VBLANK of the assigned pipe.
29	0x0 RO	**RESERVED_MBZ_IMAGE_ENHANCEMENT_PIPE_ASSIGNMENT:** Each pipe has its own dedicated IE function.
28:25	0x0 RO	**RESERVED:** Always write as 0 s.
24	0x0 RW	**HISTOGRAM_MODE_SELECT:** 0: YUV Luma Mode 1: HSV Intensity Mode - Reserved on [DevCL]
23:16	0x0 RW	**SYNC_TO_PHASE_IN_COUNT:** This field indicates the phase in count number on which the Image Enhancement table will be loaded if the Sync to Phase in is enabled.
15	0x0 RO	**RESERVED_1:** Always write as 0.
14:13	0x0 RW	**ENHANCEMENT_MODE:** 00: Direct look up mode 01: Additive mode 10: Multiplicative mode - Reserved on [DevCL] 11: Reserved
12	0x0 RW	**SYNC_TO_PHASE_IN:** Setting this bit enables the double buffered registers to be loaded on the phase in count value specified instead of the next vblank.
11	0x0 RW	**BIN_REGISTER_FUNCTION_SELECT:** This field indicates what data is being written to or read from the bin data register. 0 = Bin Threshold Count. A read from the bin data register returns that bin s threshold value from the most recent vblank load event (guardband threshold trip). Valid range for the Bin Index is 0 to 31. 1 = Bin Image Enhancement Value. Valid range for the Bin Index is 0 to 32
10:7	0x0 RO	**RESERVED_2:** Always write as 0's.
6:0	0x0 RO	**BIN_REGISTER_INDEX_READ_ONLY:** This field indicates the bin number whose data can be accessed through the bin data register. This value is automatically incremented by a read or a write to the bin data register if the busy bit is not set. AccessType: Read Only

4.2.288 PIPEB_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER—Offset 61364h

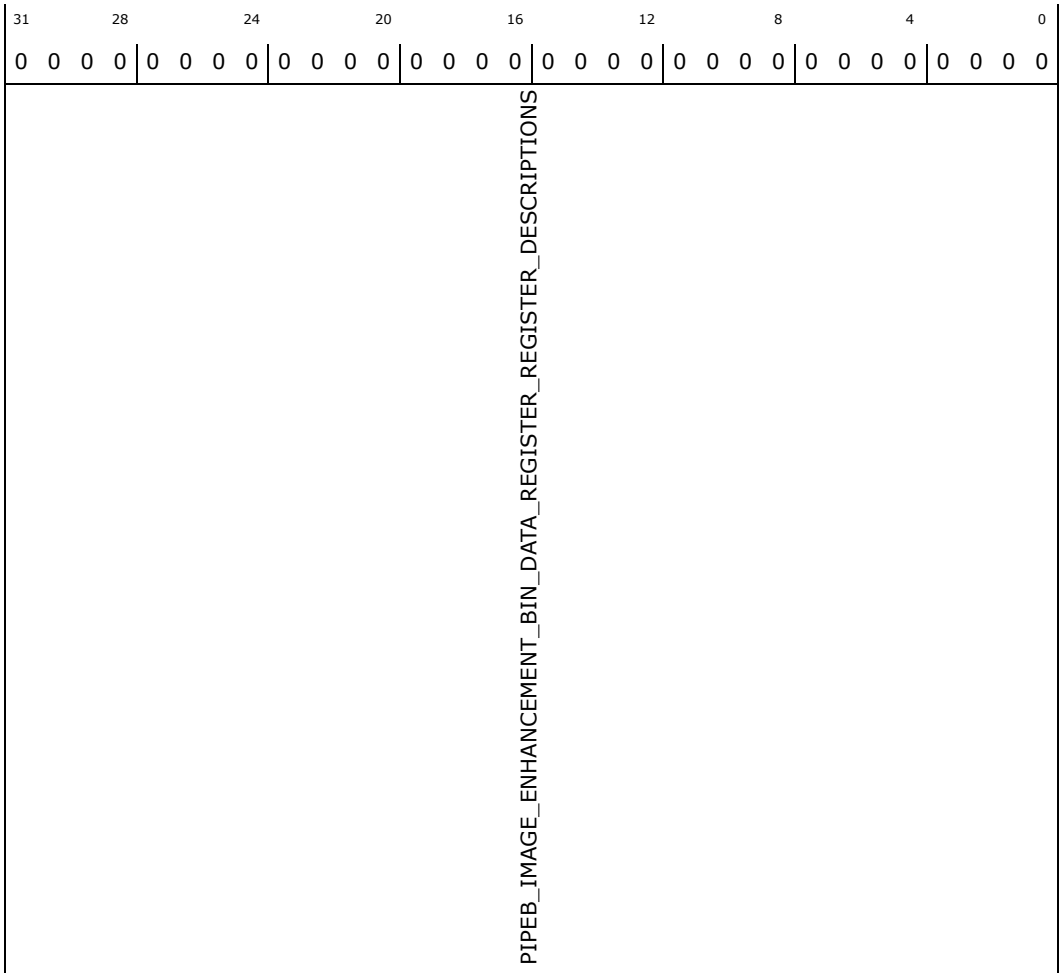
PIPEB_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER index registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61364h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**PIPEB_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER_REGISTER_DESCRIPTIONS:** PIPEB_IMAGE_ENHANCEMENT_BIN_DATA_REGISTER indexed register descriptions

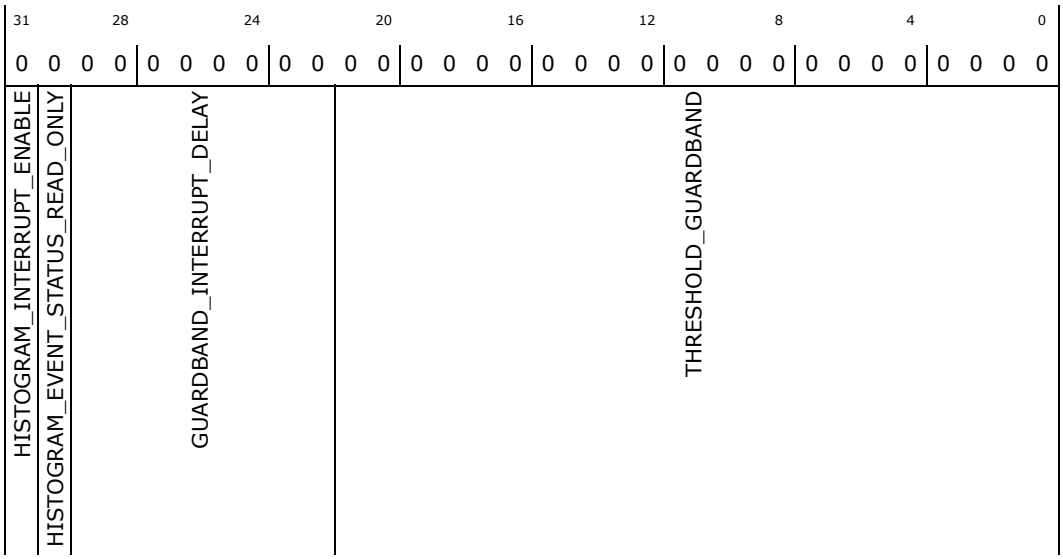
4.2.289 PIPEBHISTOGRAMTHRESHOLDGUARDBANDREGISTER—Offset 61368h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61368h

Default: 00000000h



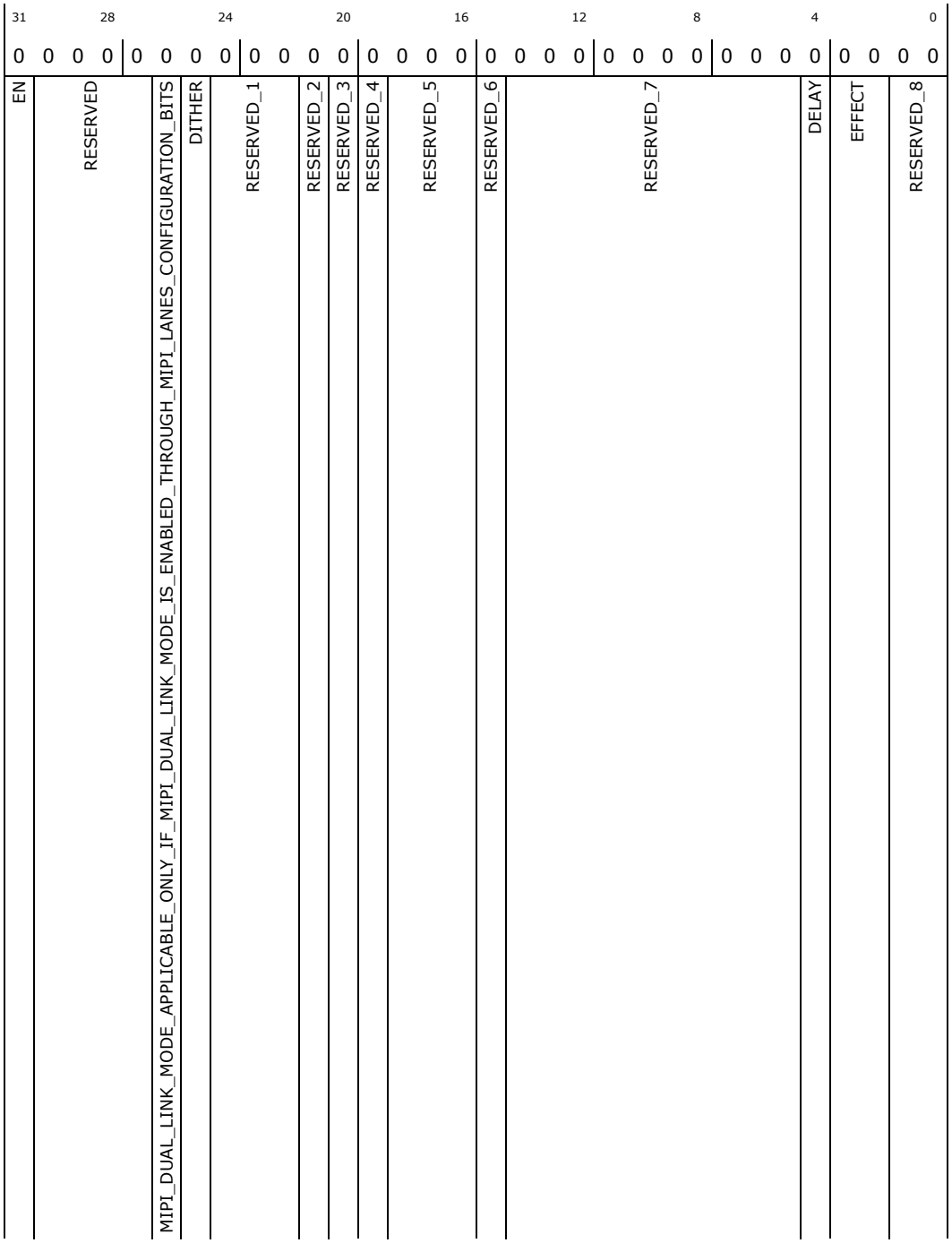
Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**HISTOGRAM_INTERRUPT_ENABLE:** 0 = Disabled 1 = Enabled. This generates a histogram interrupt once a Histogram event occurs.
30	0x0 RO	**HISTOGRAM_EVENT_STATUS_READ_ONLY:** When a Histogram event has occurred, this will get set by the hardware. For any more Histogram events to occur, the software needs to clear this bit by writing a '1'. The default state for this bit is '0'. 0 = Histogram event has not occurred. 1 = Histogram event has occurred. AccessType: Read Only
29:22	0x0 RW	**GUARDBAND_INTERRUPT_DELAY:** An interrupt is generated after this many consecutive frames of the guardband threshold being surpassed. This value is double buffered on start of vblank. A value of 0 is invalid.
21:0	0x0 RW	**THRESHOLD_GUARDBAND:** This value is used to determine the guardband for the threshold interrupt generation. This single value is used for all the segments. This value is double buffered on start of vblank

4.2.290 MIPIC_PORT_CTRL—Offset 61700h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61700h

Default: 00000000h


31 28 24 20 16 12 8 4 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
EN
RESERVED
MIPI_DUAL_LINK_MODE_APPLICABLE_ONLY_IF_MIPI_DUAL_LINK_MODE_IS_ENABLED_THROUGH_MIPI_LANES_CONFIGURATION_BITS
DITHER
RESERVED_1
RESERVED_2
RESERVED_3
RESERVED_4
RESERVED_5
RESERVED_6
RESERVED_7
DELAY
EFFECT
RESERVED_8

Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**EN:** When this bit is disabled the MIPI DPI (video mode) is inactive and in it's low power state. When it is enable it starts to generate timing for this MIPI port 0 = The port is disabled and all MIPI DPI interface are disable (timing generator is off) 1 = The port is enabled
30:27	0x0 RO	**RESERVED:** Reserved.
26	0x0 RW	**MIPI_DUAL_LINK_MODE_APPLICABLE_ONLY_IF_MIPI_DUAL_LINK_MODE_IS_ENABLED_THROUGH_MIPI_LANES_CONFIGURATION_BITS:** 0 = Front-Back mode (default) 1 = Pixel alternative mode
25	0x0 RW	**DITHER:** This bit enables or disables (bypassing) 8-6-bit color dithering function. The usage of this bit would be on for 18-bpp panels and off for 24-bpp panels. 0 = disabled 1 = enabled
24:22	0x0 RO	**RESERVED_1:** Reserved.
21	0x0 RO	**RESERVED_2:** Reserved.
20	0x0 RO	**RESERVED_3:** Reserved.
19	0x0 RO	**RESERVED_4:** Reserved.
18:16	0x0 RO	**RESERVED_5:** Reserved.
15	0x0 RO	**RESERVED_6:** Reserved.
14:5	0x0 RO	**RESERVED_7:** Reserved.
4	0x0 RW	**DELAY:** When set, the TE counter will be count down until
3:2	0x0 RW	**EFFECT:** 00: No tearing effect required - memory write start as soon as write data is available 01: TE trigger by MIPI DPHY and DSI protocol 10: TE trigger by GPIO pin 11: Reserved
1:0	0x0 RO	**RESERVED_8:** Reserved.

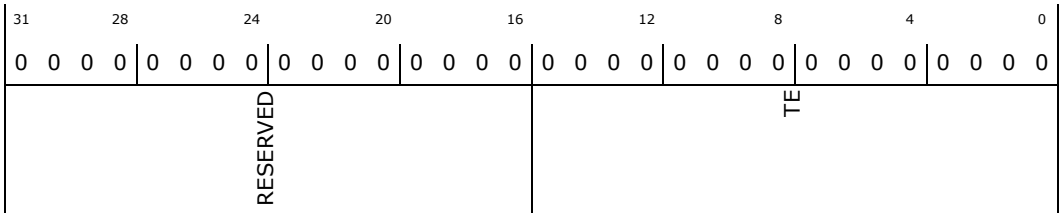
4.2.291 MIPIC_TEARING_CTR—Offset 61704h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61704h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15:0	0x0 RW	**TE:** Number of delay clocks from TE trigger to start sending data to DSI controller

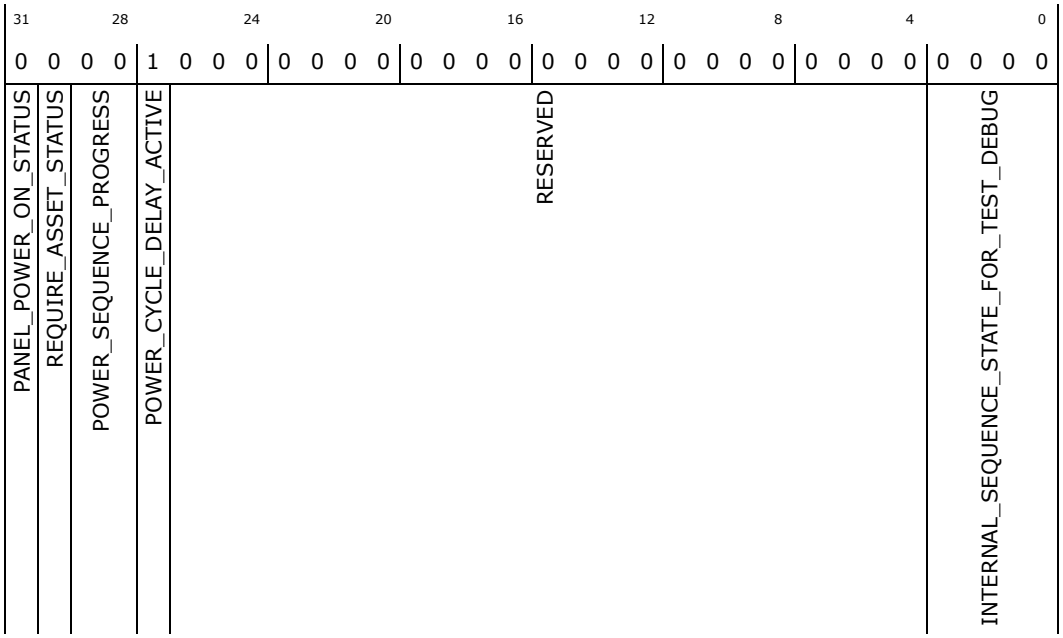
4.2.292 PIPEC_PP_STATUS—Offset 61900h

PipeC Panel Power Status Register PP Status (dplrreg.v panel_pwr_sr)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61900h

Default: 08000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**PANEL_POWER_ON_STATUS:** 0 = Indicates that the panel power down sequencing has completed. A power cycle delay may be currently active. It is safe and allowed to program pipe timing and DPLL registers. If this bit is not a zero, it activates the register write protect and writes to those registers will be ignored unless the write protect key value is set in the panel sequencing control register. 1 = In conjunction with bits Power Sequence Progress field and Power Cycle Delay Active, this bit set to a one indicates that the panel is currently powered up or is currently in the power down sequence and it is unsafe to change the pipe timing and DPLL registers for the pipe that is assigned to the embedded panel output. If the embedded panel port is selected as the target for the panel control, Software is responsible for enabling the LCD display by writing a 1 to the port enable bit only after all pipe timing, DPLL registers are properly programmed, and the PLL has locked to the reference signal. This bit is cleared (set to 0) only after the panel power down sequencing is completed.
30	0x0 RO	**REQUIRE_ASSET_STATUS:** This bit indicates the status of programming of the display PLL and the selected display port. This a power on cycle will not be allowed unless this status indicates that the required assets are programmed and ready for use. 0 = All required assets are not properly programmed. 1 = All required assets are ready for the driving of a panel. The following conditions determine that the assets are ready: 1) Display Pipe PLL Enabled and frequency locked (bit-31 of DPLL Control Register for the pipe attached to the embedded panel port). 2) Display Pipe Enabled (bit-31 of PIPECONF Pipe Configuration Register. For the pipe attached to the embedded panel port) 3) Embedded Panel Port is Programmed Enabled
29:28	0x0 RO	**POWER_SEQUENCE_PROGRESS:** 00 = Indicates that the panel is not in a power sequence 01 = Indicates that the panel is in a power up sequence (may include power cycle delay) 10 = Indicates that the panel is in a power down sequence 11 = Reserved
27	0x1 RO	**POWER_CYCLE_DELAY_ACTIVE:** Power cycle delays occur after a panel power down sequence or after a hardware reset. On reset, a power cycle delay will occur using the default value for the timing. 0 = A power cycle delay is not currently active 1 = A power cycle delay (T4) is currently active
26:4	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x0 RO	**INTERNAL_SEQUENCE_STATE_FOR_TEST_DEBUG:** 0000 = Power Off Idle (S0.0) 0001 = Power Off, Wait for cycle delay (S0.1) 0010 = Power Off (S0.2) 0011 = Power Off (S0.3) 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = Power On Idle (S1.0) 1001 = Power On, (S1.1) 1010 = Power On, (S1.2) 1011 = Power On, Wait for cycle delay (S1.3) 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reset

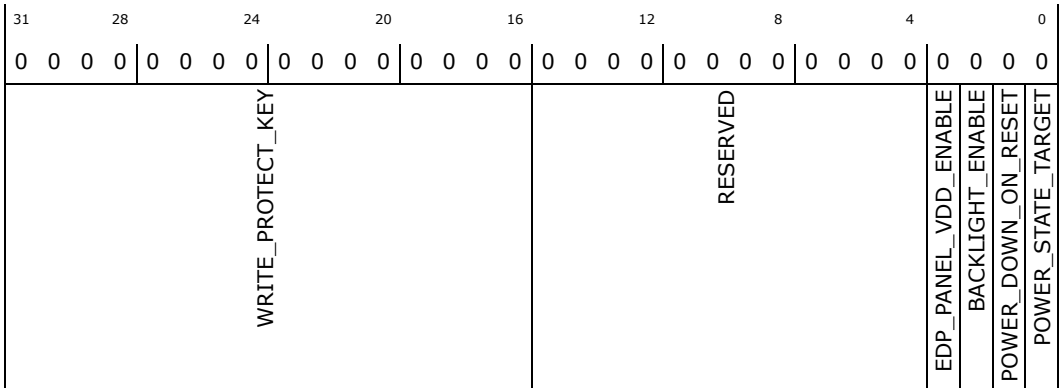
4.2.293 PIPEC_PP_CONTROL—Offset 61904h

PipeC Panel Power Control Register PP Control (dplrreg.v pnl_pwr_cntl)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61904h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**WRITE_PROTECT_KEY:** ABCD Write protect off When this field is programmed to anything except the write protect off setting and the panel is either powered up or in the process of a power up sequence, a set of registers involved in generation of panel timing or control become write protected. Any write cycles to those write protected registers, while they will complete as normal, will not change the value of the register when write protected. When this register field contains the write protect off key value, write protect will be unconditionally disabled. In situations where the embedded panel port is unused, the port should remain powered down and the write protect will be inactive. This field in normal operation should be left to all zeros and never programmed with the key value. It exists only to allow testing and workarounds. List of Write protected registers: (Panel sequencing Registers): Pipe B Panel power on sequencing delays - Address: 61308-6130Bh Pipe C Panel power off sequencing delays Address: 6130Ch 6130Fh Pipe B Panel power cycle delay and Reference Divisor Address: 61310h 61313 (DPLL registers): DPLL Control Registers FPA0 DPLL Divisor Register FPA1 DPLL Divisor Register 1 FPB0 DPLL Divisor Register FPB1 DPLL Divisor Register 1 (Display Pipe timing registers except source size) HTOTAL Horizontal Total Register HBLANK Horizontal Blank Register HSYNC_ Horizontal Sync Register VTOTAL_ Vertical Total Register VBLANK_ Vertical Blank Register VSYNC_ Vertical Sync Register
15:4	0x0 RO	**RESERVED:** Reserved.
3	0x0 RW	**EDP_PANEL_VDD_ENABLE:** Enabling this bit enables the panel vdd if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit for eDP link training. After eDP link training is done, software must disable it and let the normal panel power sequencing to take control. 0 = eDP panel Vdd disabled 1 = eDP panel Vdd enabled [DevCLN] Reserved
2	0x0 RW	**BACKLIGHT_ENABLE:** Enabling this bit enables the panel backlight if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit after training the link, and disable it when disabling the panel power state target. 0 = Backlight disabled 1 = Backlight enabled [DevCL] Reserved

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**POWER_DOWN_ON_RESET:** Enabling this bit causes the panel to power down when a reset warning comes to the GMCH from the ICH. When system reset is initiated, the embedded panel port automatically begins the panel power down sequence. If the panel is not on during a reset event, this bit is ignored. 0 = Do not run panel power down sequence when reset is detected 1 = Run panel power down sequence when system is reset
0	0x0 RW	**POWER_STATE_TARGET:** Writing this bit can occur any time, it will only be used at the completion of any current power cycle. 0 = The panel power state target is off, if the panel is either on or in a power on sequence, a power off sequence is started as soon as the panel reaches the power on state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. 1= The panel power state target is on, if the panel is in either the off state or a power off sequence, if all pre-conditions are met, a power on sequence is started as soon as the panel reaches the power off state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. While the panel is on or in a power on sequence, the register write lock will be enabled.

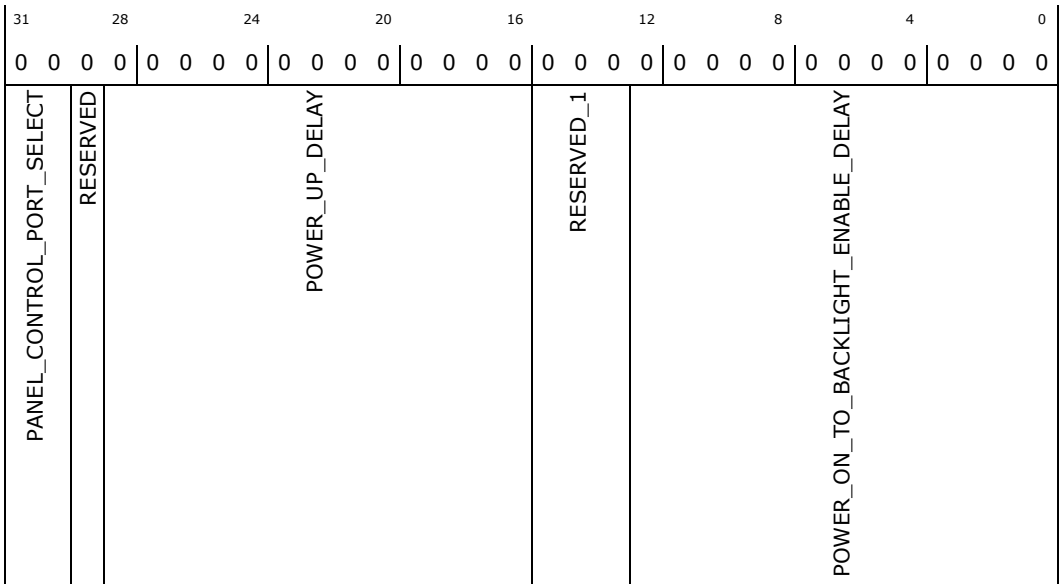
4.2.294 PIPEC_PP_ON_DELAYS—Offset 61908h

PipeC Panel Power on Sequencing Delays PP On Delay values (dplrreg.v DPLRppon_sd)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61908h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**PANEL_CONTROL_PORT_SELECT:** These bits define to which port the embedded panel is connected. This is used for automatic control of the panel power. If the selected port is disabled or if the port is not on pipe-B, then, the power sequence will not allow a panel power up. 00 = Reserved 01 = Panel is connected to the embedded DisplayPort B 10 = Panel is connected to the embedded DisplayPort C 11 = Reserved The selection of non-existent ports are not allowed. This programming will disable panel power sequencing logic.
29	0x0 RO	**RESERVED:** Reserved.
28:16	0x0 RW	**POWER_UP_DELAY:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T1+T2 time sequence. The time unit used is the 100us timer.
15:13	0x0 RO	**RESERVED_1:** Reserved.
12:0	0x0 RW	**POWER_ON_TO_BACKLIGHT_ENABLE_DELAY:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T5 (T3 for DisplayPort) time sequence. The time unit used is the 100us timer.

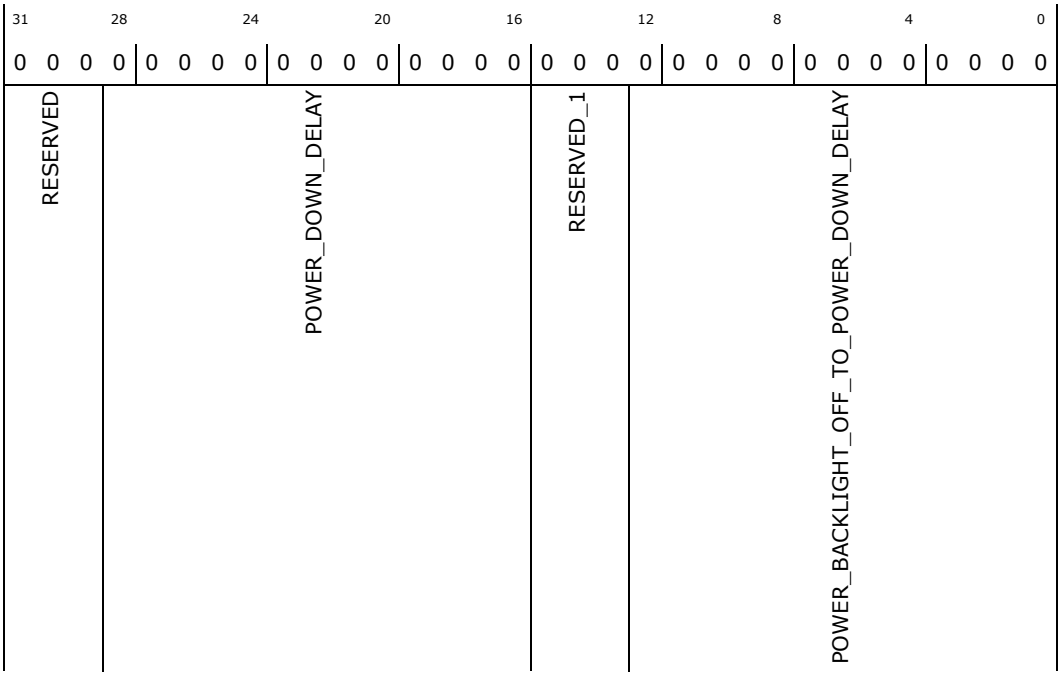
4.2.295 PIPEC_PP_OFF_DELAYS—Offset 6190Ch

PipeC Panel Power off Sequencing Delays PP Delay Off values (dplrreg.v DPLRppoff_sd)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6190Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Reserved.
28:16	0x0 RW	**POWER_DOWN_DELAY:** Programmable value of panel power sequencing delay during power up. This provides the time delay for the T3 (T5 for DisplayPort) time sequence. The time unit used is the 100us timer.
15:13	0x0 RO	**RESERVED_1:** Reserved.
12:0	0x0 RW	**POWER_BACKLIGHT_OFF_TO_POWER_DOWN_DELAY:** Programmable value of panel power sequencing delay during power down. This provides the time delay for the Tx (T4 for DisplayPort) time sequence. The time unit used is the 100us timer.

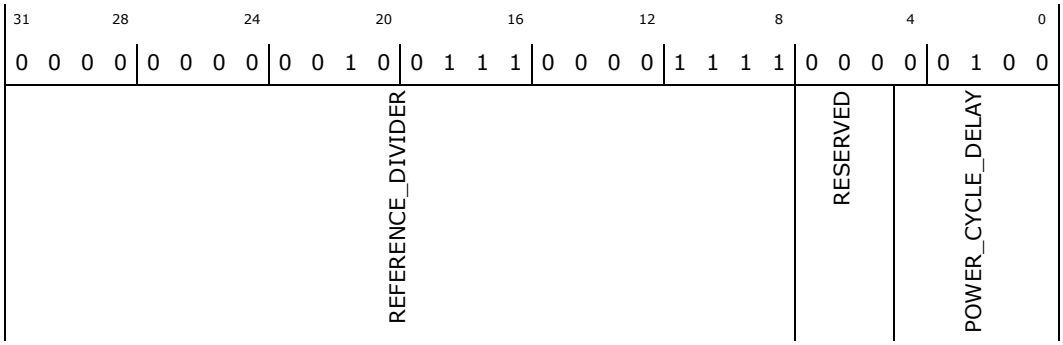
4.2.296 PIPEC_PP_DIVISOR—Offset 61910h

PipeC Panel Power Cycle Delay and Reference Divisor PP Divisor (dplrreg.v DPLRrefdiv_pp_cd)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61910h

Default: 00270F04h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x270f RW	**REFERENCE_DIVIDER:** This field provides the value of the divider used for the creation of the panel timer reference clock. The output of the divider is used as the fastest of the three time bases (100us) for all other timers. The other time bases are divided from this frequency. The value of zero should not be used. When it is desired to divide by N, the actual value to be programmed is (N/2)-1. The value should be (100*RefinMHz/2)-1. The default value assumes the default value for the display core clock that is for [DevCL and DevCTG] a 200MHz reference value. The following are examples for other memory speeds. Display Core Frequency Value of Field 233MHz 2D81h 200MHz 270Fh 133MHz 19F9h
7:5	0x0 RO	**RESERVED:** Reserved.
4:0	0x4 RW	**POWER_CYCLE_DELAY:** Programmable value of time panel must remain in a powered down state after powering down. For devices coming out of reset, the default values will define how much time must pass before a power on sequence can be started. This field uses the .1 S time base unit from the divider. If the panel power on sequence is attempted during this delay, the power on sequence will commence once the power cycle delay is complete. Writing a value of 0 selects no delay or is used to abort the delay if it is active. During the initial power up reset, a D3 cold power cycle, or a user instigated system reset, the timer will be set to the default value and the count down will begin after the de-assertion of reset. Writing this field to a zero while the count is active will abort this portion of the sequence. This corresponds to the T4 of the SPWG specification. Note: Even if the panel is not enabled, the T4 count happens after reset. This register needs to be programmed to a +1 value. For instance for meeting the SPWG specification of 400mS, program 5 to achieve at least 400mS delay prior to powerup.

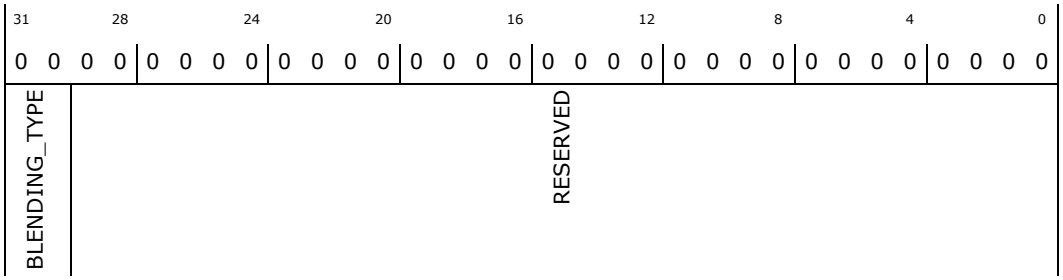
4.2.297 BLEND_B—Offset 61A00h

Register for Blending for Pipe.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61A00h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 Rw	**Blending_Type (BLENDING_TYPE):** 00=SoC A0 Legacy Behavior. 01=Android Requirement. 10=Microsoft Requirement. 11=Reserved.
29:0	0x0 RO	**Reserved (RESERVED):**

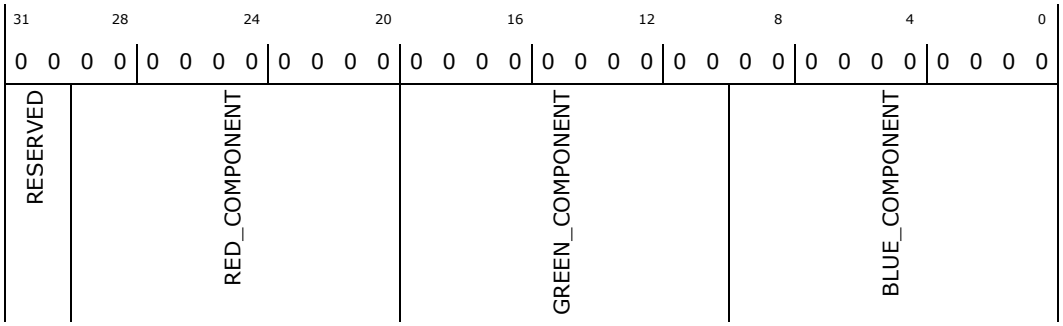
4.2.298 CANVAS_B—Offset 61A04h

Pipe B Canvas Color Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61A04h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RESERVED:** Reserved.
29:20	0x0 RO	**RED_COMPONENT:** Red Component

Bit Range	Default & Access	Field Name (ID): Description
19:10	0x0 RO	**GREEN_COMPONENT:** GREEN Component
9:0	0x0 RO	**BLUE_COMPONENT:** BLUE Component

4.2.299 PRIMPOS_B—Offset 61A08h

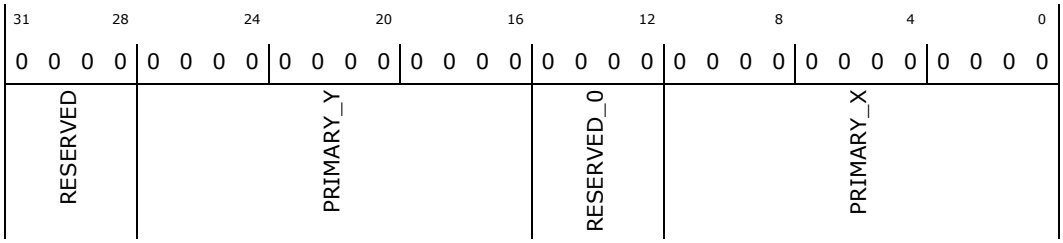
These registers specify the screen position and size of the primary. This register is double buffered. The load register is transferred into the active register on the asserting edge of Vertical Blank for the pipe that the display is assigned. When using the primary as a secondary display, this should be set to the entire display rectangle.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 61A08h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as Zero.
27:16	0x0 RW	**Primary_Y (PRIMARY_Y):** These 12 bits specify the vertical position in lines of the primary (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the un-rotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0x0 RO	**RESERVED_0:** Write as Zero
11:0	0x0 RW	**PRIMARY_X:** These 12 bits specify the horizontal position in lines of the primary (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the end of the active video area in the un-rotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

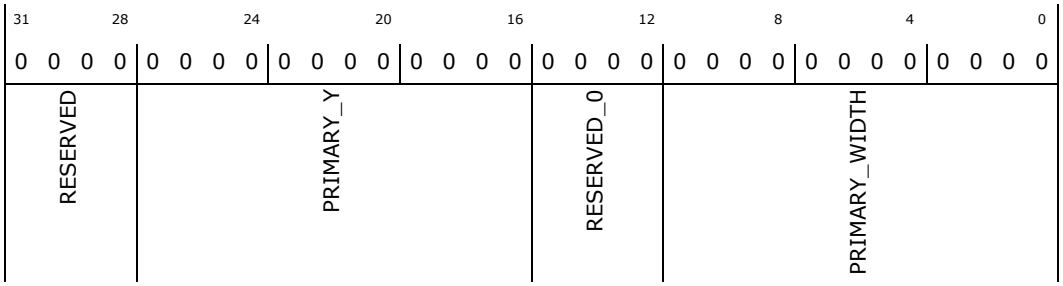
4.2.300 PRIMSIZE_B—Offset 61A0Ch

This register specifies the height and width of the primary in pixels and lines. The rectangle defined by the size and position should never exceed the boundaries of the display rectangle that the primary is assigned to.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61A0Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as Zero.
27:16	0x0 RW	**Primary_Height (PRIMARY_Y):** This register field is used to specify the height of the primary in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0x0 RO	**RESERVED_0:** Write as Zero
11:0	0x0 RW	**PRIMARY_WIDTH:** This register field is used to specify the width of the primary in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined primary rectangle must always be completely contained within the displayable area of the screen image.

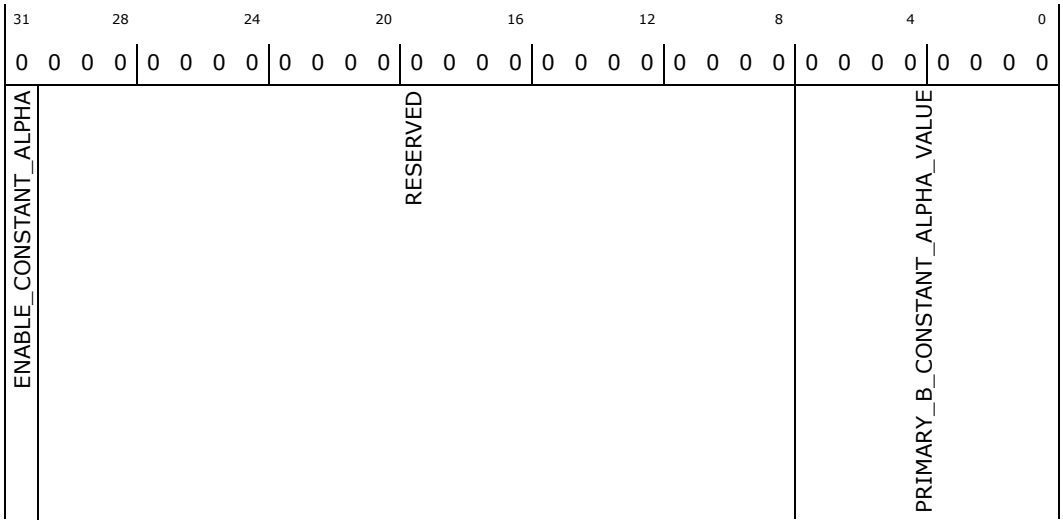
4.2.301 PRIMB_CONSTANT—Offset 61A10h

Primary B constant Alpha

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 61A10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Enable_CONSTANT_ALPHA (ENABLE_CONSTANT_ALPHA):** Primary B constant alpha provides a way to apply an alpha value to all primary pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. 0-Primary B Constant Alpha is disabled. 1-Primary B Constant Alpha Enabled
30:8	0x0 RO	**RESERVED:** RESERVED: MBZ
7:0	0x0 RW	**PRIMARY_B_CONSTATN_ALPHA_VALUE (PRIMARY_B_CONSTANT_ALPHA_VALUE):** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of primary with other surfaces.

4.2.302 AUD_CONFIG_A—Offset 62000h

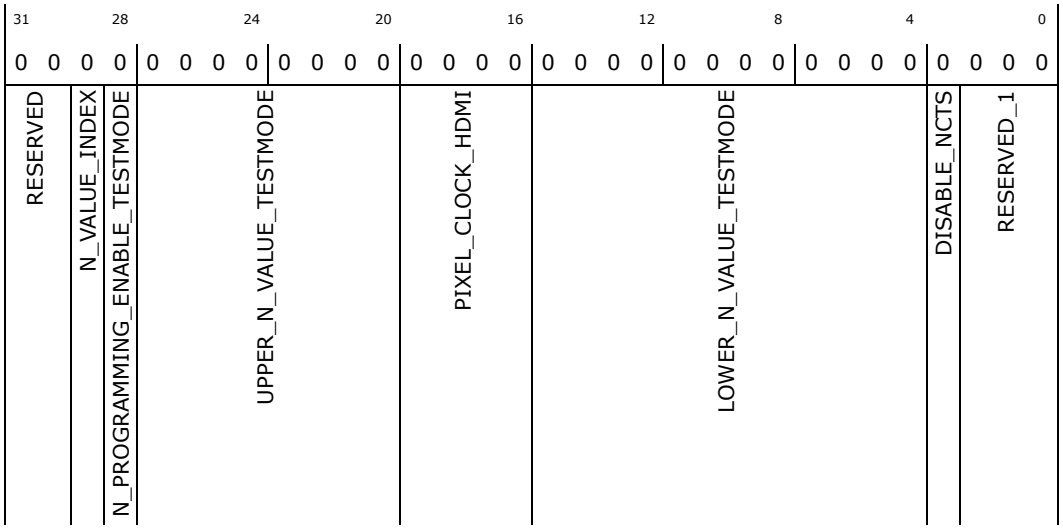
Audio Configuration Pipe A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62000h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RESERVED:** Project: All Format:
29	0x0 RW	**N_VALUE_INDEX:** Project: All Default Value: ;0b Value Name Description Project 0b HDMI N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are is programmable to any N value - default h7FA6. All 1b DP N value read on bits 27:20 and 15:4 reflects DP N value. Set this bit to 1 before programming N value register. When this is set to 1, 27:20 and 15:4 will reflect the current N value default h8000. All
28	0x0 RW	**N_PROGRAMMING_ENABLE_TESTMODE:** Project: All Security: Test This bit enables programming of N values for non-CEA modes. Please note that the Pipe to which audio is attached must be disabled when changing this field.
27:20	0x0 RW	**UPPER_N_VALUE_TESTMODE:** Project: All Security: Test These are bits [19:12] of programmable N values for non-CEA modes. Bit 25 of this register must also be written in order to enable programming. Please note that the Pipe to which audio is attached must be disabled when changing this field. This register can also be used to program N value for DP for a specific Port. Default value on this register when bit 29 is set to 1 is h7FA6

Bit Range	Default & Access	Field Name (ID): Description
19:16	0x0 RW	**PIXEL_CLOCK_HDMI:** Project: All Default Value: ;0b This is the target frequency of the CEA/HDMI video mdoe to which the audio stream is added. This value is used for generating N_CTS packets. This refers to only HDMI Pixel clock and does not refer to DP Link clock. DP Link clock does not require this programming. Note: The Pipe on which audio is attached must be disabled when changing this field. Value Name Description Project 0000b 25.2 / 1.001 MHz 25.2 / 1.001 MHz All 0001b 25.2 MHz 25.2 MHz Program this value for pixel clocks not listed in this field All 0010b 27 MHz 27 MHz All 0011b 27 * 1.001 MHz 27 * 1.001 MHz All 0100b 54 MHz 54 MHz All 0101b 54 * 1.001 MHz 54 * 1.001 MHz All 0110b 74.25 / 1.001 MHz 74.25 / 1.001 MHz All 0111b 74.25 MHz 74.25 MHz All 1000b 148.5 / 1.001 MHz 148.5 / 1.001 MHz All 1001b 148.5 MHz 148.5 MHz All Others Reserved Reserved All
15:4	0x0 RW	**LOWER_N_VALUE_TESTMODE:** Project: All Security: Test These are bits [11:0] of programmable N values for non-CEA modes. Bit 25 of this register must also be written in order to enable programming. Please note that the Pipe to which audio is attached must be disabled when changing this field. This register can also be used to program N value for DP for a specific Port. Default value on this register when bit 29 is set to 1 is h7FA6
3	0x0 RW	**DISABLE_NCTS:** Project: All Set this bit to disable N and CTS or M generation for CTM modes. This is to enable prediction of CRC in CTM modes.
2:0	0x0 RO	**RESERVED_1:** Project: All Format:

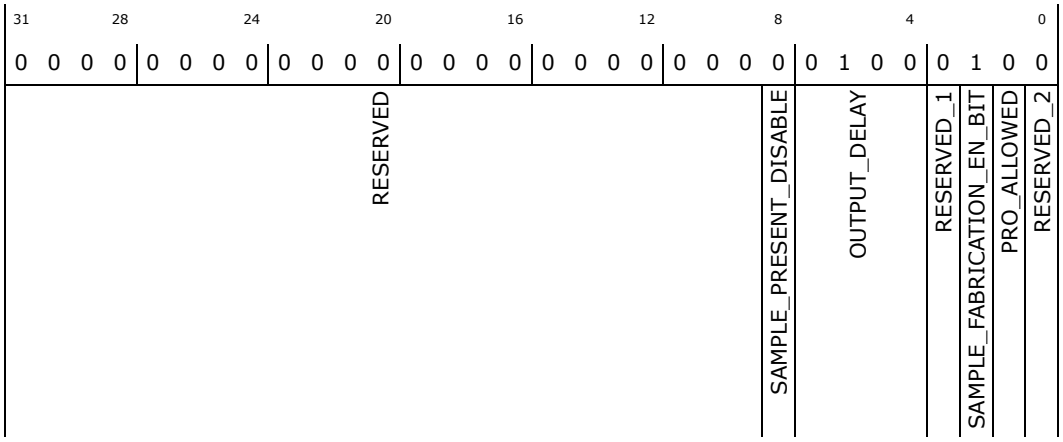
4.2.303 AUD_MISC_CTRL_A—Offset 62010h

Audio MISC Control for Pipe A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 62010h

Default: 00000044h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**RESERVED:** Project: All Format: MBZ
8	0x0 RW	**SAMPLE_PRESENT_DISABLE:** Project: All Security: Debug This bit is used to Disable sample present for HDMI or DP (Chicken Bit)
7:4	0x4 RW	**OUTPUT_DELAY:** Project: All Default Value: ;0100b The number of samples between when the sample is received from the HD Audio link and when it appears as an analog signal at the pin.
3	0x0 RO	**RESERVED_1:** Project: All Format: MBZ
2	0x1 RW	**SAMPLE_FABRICATION_EN_BIT:** Project: All Access: R/W Default Value: ;1b This bit indicates whether internal fabrication of audio samples is enabled during a link underrun. Value Name Description Project 0b Disable Audio fabrication disabled All 1b Enable Audio fabrication enabled All
1	0x0 RW	**PRO_ALLOWED:** Project: All Access: R/W Default Value: ;0b By default, the audio device is configured to consumer mode and does not allow the mode to be changed to professional mode by an HD Audio verb. When Pro is allowed by setting this configuration bit, the HD Audio codec allows a verb to set the device into professional mode. Note: Setting this configuration bit does not change the default Pro bit value to be 1. Pro must be set to 1 through the normal process, using a verb. Value Name Description Project 0b Consumer Consumer use only All 1b Professional Professional use allowed All
0	0x0 RO	**RESERVED_2:** All Format: MBZ

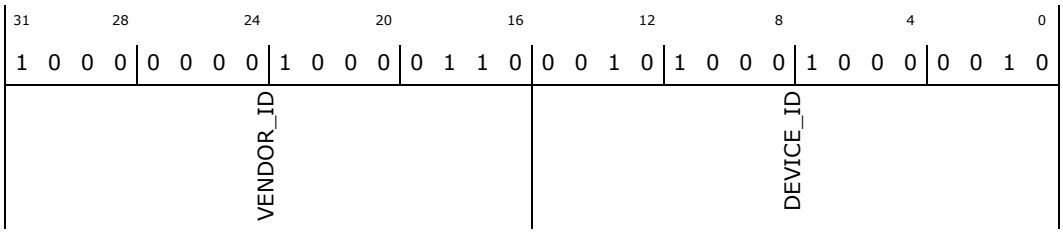
4.2.304 AUD_VID_DID—Offset 62020h

Audio Vendor ID / Device ID

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 62020h

Default: 80862882h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x8086 RO	**VENDOR_ID:** Project: All Format: U16 Used to identify the codec within the PnP system. This field is hardwired within the device. Value = 0x8086
15:0	0x2882 RO	**DEVICE_ID:** Project: All Format: U16 Constant used to identify the codec within the PnP system. This field is set by the device hardware. Value = 0x2882

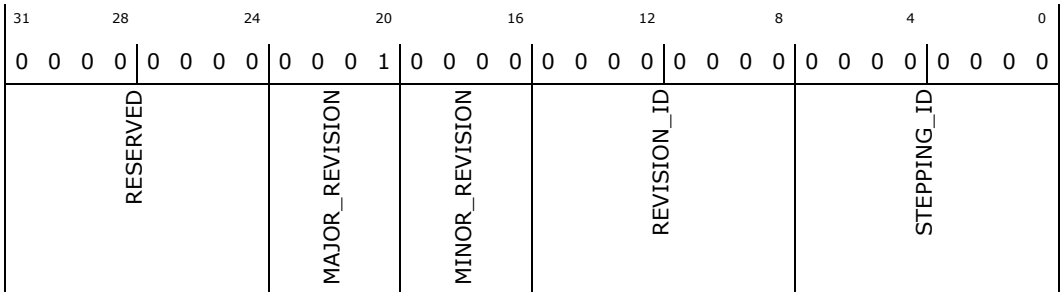
4.2.305 AUD_RID—Offset 62024h

Audio Revision ID

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 62024h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format:

Bit Range	Default & Access	Field Name (ID): Description
23:20	0x1 RO	**MAJOR_REVISION:** Project: All Default Value: ;0001b The major revision number (left of the decimal) of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device. Value = 0x1
19:16	0x0 RO	**MINOR_REVISION:** Project: All The minor revision number (rights of the decimal) or dot number of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device. Value = 0x0
15:8	0x0 RO	**REVISION_ID:** Project: All The vendors revision number for this given Device ID. This field is hardwired within the device. Value = 0x0
7:0	0x0 RO	**STEPPING_ID:** Project: All An optional vendor stepping number within the given Revision ID. This field is hardwired within the device. Value = 0x0

4.2.306 AUD_CTS_ENABLE_A—Offset 62028h

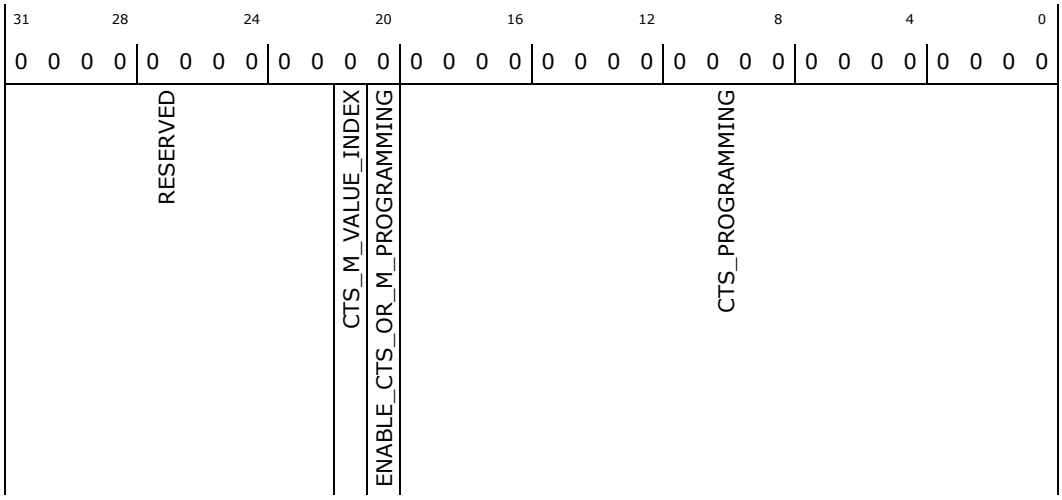
Audio CTS Programming Enable Pipe A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62028h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**RESERVED:** Project: All Format:

Bit Range	Default & Access	Field Name (ID): Description
21	0x0 RW	**CTS_M_VALUE_INDEX:** Project: All Default Value: ;0b Value Name Description Project 0b CTS CTS value read on bits 23:4 reflects CTS value. Bit 23:4 is programmable to any CTS value. default is 0 All 1b M M value read on bits 21:4 reflects DP M value. Set this bit to 1 before programming M value register. When this is set to 1 23:4 will reflect the current N value All
20	0x0 RW	**ENABLE_CTS_OR_M_PROGRAMMING:** Project: All When set will enable CTS or M programming.
19:0	0x0 RW	**CTS_PROGRAMMING:** Project: All These are bits [19:0] of programmable CTS values for non-CEA modes. Bit 21 of this register must also be written in order to enable programming. Please note that the Pipe to which audio is attached must be disabled when changing this field.

4.2.307 AUD_PWRST—Offset 6204Ch

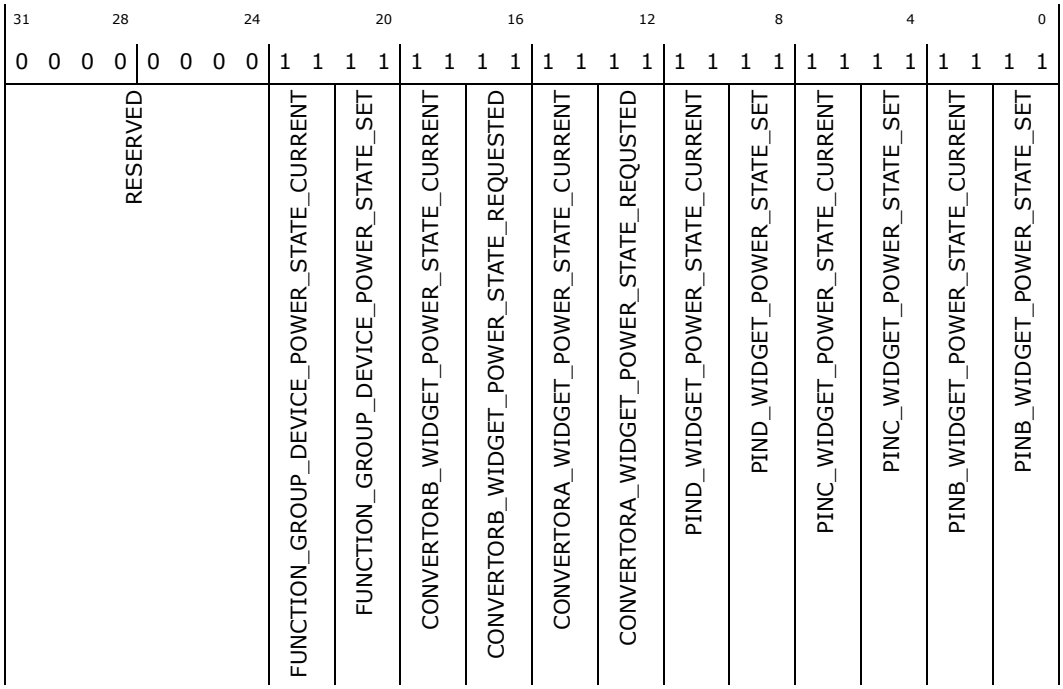
Audio Power State (Function Group, Convertor, Pin Widget)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6204Ch

Default: 00FFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format:
23:22	0x3 RO	**FUNCTION_GROUP_DEVICE_POWER_STATE_CURRENT:** Project: All Format: Audio Power State Format Current power state Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
21:20	0x3 RO	**FUNCTION_GROUP_DEVICE_POWER_STATE_SET:** Project: All Format: Audio Power State Format Power state that was set Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
19:18	0x3 RO	**CONVERTORB_WIDGET_POWER_STATE_CURRENT:** Project: All Format: Audio Power State Format Current power state Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
17:16	0x3 RO	**CONVERTORB_WIDGET_POWER_STATE_REQUESTED:** Project: All Format: Audio Power State Format Power state that was requested by audio software Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
15:14	0x3 RO	**CONVERTORA_WIDGET_POWER_STATE_CURRENT:** Project: All Format: Audio Power State Format Current power state Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All

Bit Range	Default & Access	Field Name (ID): Description
13:12	0x3 RO	**CONVERTORA_WIDGET_POWER_STATE_REQUSTED:** Project: All Format: Audio Power State Format Power state that was requested by audio software Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
11:10	0x3 RO	**PIND_WIDGET_POWER_STATE_CURRENT:** Project: All Format: Audio Power State Format Current power state Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
9:8	0x3 RO	**PIND_WIDGET_POWER_STATE_SET:** Project: All Format: Audio Power State Format Power state that was set Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
7:6	0x3 RO	**PINC_WIDGET_POWER_STATE_CURRENT:** Project: All Format: Audio Power State Format Current power state Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
5:4	0x3 RO	**PINC_WIDGET_POWER_STATE_SET:** Project: All Format: Audio Power State Format Power state that was set Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All
3:2	0x3 RO	**PINB_WIDGET_POWER_STATE_CURRENT:** Project: All Format: Audio Power State Current power state

Bit Range	Default & Access	Field Name (ID): Description
1:0	0x3 RO	**PINB_WIDGET_POWER_STATE_SET:** Project: All Format: Audio Power State Format Power state that was set Project: All Default Value: ;11b D3 Value Name Description Project 00b D0 D0 All 01b,10b Unsupported Unsupported All 11b D3 D3 All

4.2.308 AUD_HDMIW_HDMIEDID_A—Offset 62050h

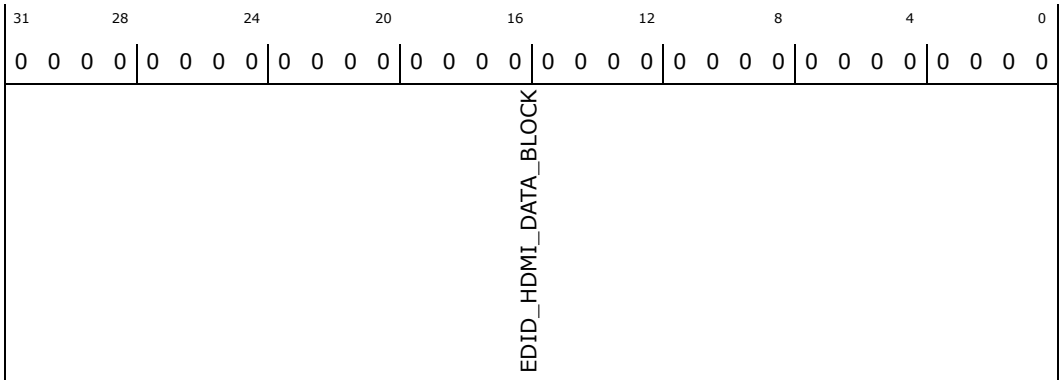
HDMI Data EDID Block Pipe A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62050h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**EDID_HDMI_DATA_BLOCK:** Project: All Format: Please note that the contents of this buffer are not cleared when ELD is disabled. The contents of this buffer are cleared during gfx reset

4.2.309 AUD_HDMIW_INFOFR_A—Offset 62054h

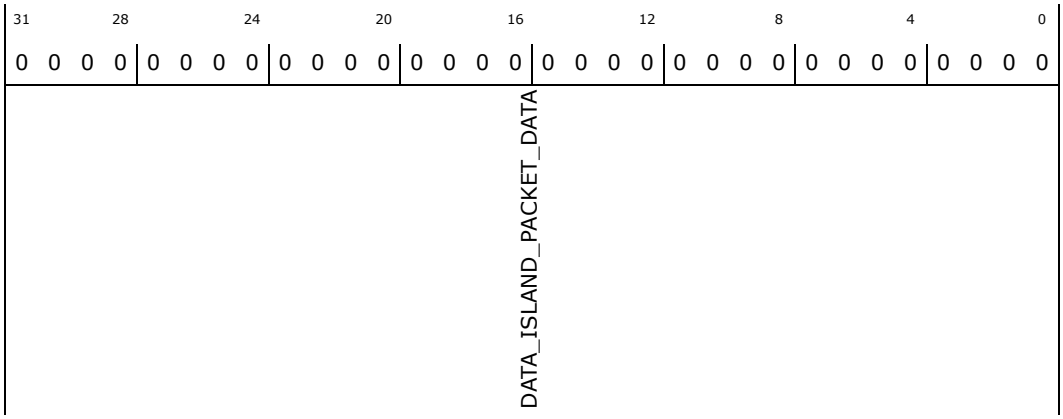
Audio Widget Data Island Packet Pipe A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62054h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DATA_ISLAND_PACKET_DATA:** Project: All Format: This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

4.2.310 AUD_PORT_EN_HD_CFG—Offset 6207Ch

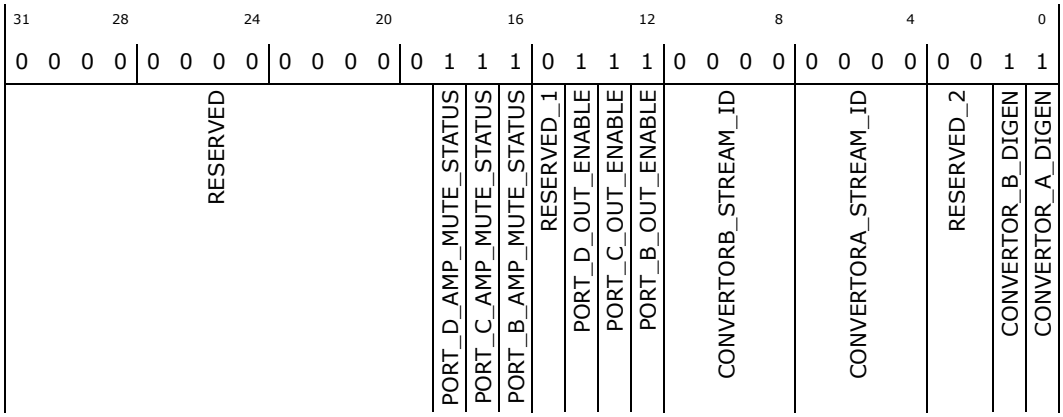
Audio Port Enable HDAudio Config

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6207Ch

Default: 00077003h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0x0 RO	**RESERVED:** Project: All Format:

Bit Range	Default & Access	Field Name (ID): Description
18	0x1 RO	**PORT_D_AMP_MUTE_STATUS:** Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b Amp not muted Amp not muted All 1b Amp muted Amp muted All
17	0x1 RO	**PORT_C_AMP_MUTE_STATUS:** Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b Amp not muted Amp not muted All 1b Amp muted Amp muted All
16	0x1 RO	**PORT_B_AMP_MUTE_STATUS:** Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b Amp not muted Amp not muted All 1b Amp muted Amp muted All
15	0x0 RO	**RESERVED_1:** Project: All Format:
14	0x1 RO	**PORT_D_OUT_ENABLE:** Project: All Default Value: ;1b Audio is Enabled This bit reflects the state of the output path of the Pin Widget. Value Name Description Project 0b Disable Audio is Disabled All 1b Enable Audio is Enabled All
13	0x1 RO	**PORT_C_OUT_ENABLE:** Project: All Default Value: ;1b Audio is Enabled This bit reflects the state of the output path of the Pin Widget. Value Name Description Project 0b Disable Audio is Disabled All 1b Enable Audio is Enabled All
12	0x1 RO	**PORT_B_OUT_ENABLE:** Project: All Default Value: ;1b Audio is Enabled This bit reflects the state of the output path of the Pin Widget. Value Name Description Project 0b Disable Audio is Disabled All 1b Enable Audio is Enabled All
11:8	0x0 RO	**CONVERTORB_STREAM_ID:** Project: All Format: Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 (stream 0)
7:4	0x0 RO	**CONVERTORA_STREAM_ID:** Project: All Format: Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 (stream 0)
3:2	0x0 RO	**RESERVED_2:** Project: All Format:

Bit Range	Default & Access	Field Name (ID): Description
1	0x1 RO	**CONVERTOR_B_DIGEN:** Project: All Default Value: ;1b Digital Transmission Enabled Enables digital transmission through this node. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Block Digital data is blocked from passing through the node, regardless of the state All 1b Pass Digital data can pass through the node (Default) All
0	0x1 RO	**CONVERTOR_A_DIGEN:** Project: All Default Value: ;1b Digital Transmission Enabled Enables digital transmission through this node. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Block Digital data is blocked from passing through the node, regardless of the state All 1b Pass Digital data can pass through the node (Default) All

4.2.311 AUD_OUT_DIG_CNVT_A—Offset 62080h

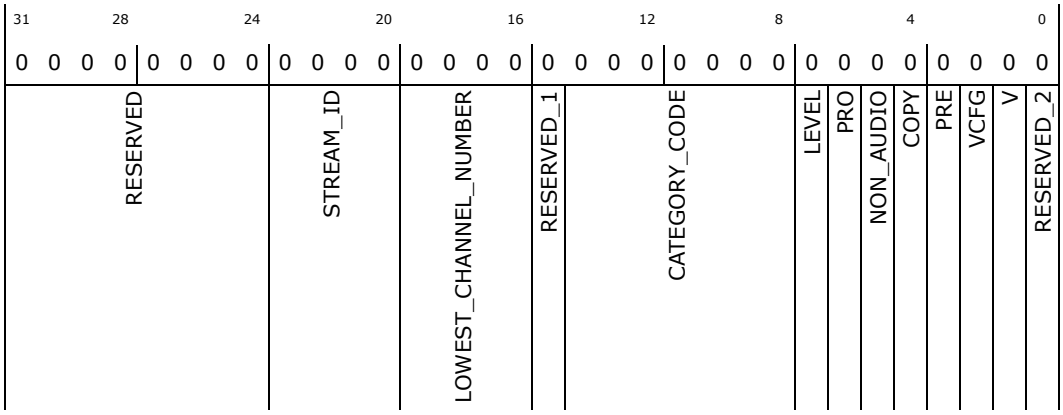
Audio Digital Converter Conv A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62080h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format:
23:20	0x0 RO	**STREAM_ID:** Project: All Format: Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 (stream 0)

Bit Range	Default & Access	Field Name (ID): Description
19:16	0x0 RO	**LOWEST_CHANNEL_NUMBER:** Project: All Format: Represents the lowest channel used by the converter. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0
15	0x0 RO	**RESERVED_1:** Project: All Format:
14:8	0x0 RO	**CATEGORY_CODE:** Project: All Format: S/PDIF IEC Category Code. This value is set in the Digital Converter 1 through the Set Audio Output Converter Widget command. Default = 0
7	0x0 RO	**LEVEL:** Project: All Format: S/PDIF IEC Generation Level. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
6	0x0 RO	**PRO:** Project: All Default Value: ;0b This bit indicates professional or consumer use of channel. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. This value can only be set to 1 if the Pro Allowed bit is set in the audio configuration register. Value Name Description Project 0b Consumer Consumer use All 1b Professional Professional use All
5	0x0 RO	**NON_AUDIO:** Project: All Default Value: ;0b Data is non PCM format. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b PCM Data is PCM All 1b Non PCM Data is non PCM format All
4	0x0 RO	**COPY:** Project: All Default Value: ;0b Copyright asserted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Not Asserted Copyright is not asserted All 1b Asserted Copyright is asserted All
3	0x0 RO	**PRE:** Project: All Default Value: ;0b Filter preemphasis. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Disabled Preemphasis is disabled All 1b Enabled Filter preemphasis is enabled All
2	0x0 RO	**VCFG:** Project: All Format: Validity Configuration. Determines S/PDIF transmitter behavior when data is not being transmitted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RO	**V:** Project: All Format: Affects the validity flag transmitted in each subframe, and enables the S/PDIF transmitter to maintain connection during error or mute conditions. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
0	0x0 RO	**RESERVED_2:** All Format: MBZ

4.2.312 AUD_OUT_STR_DESC_A—Offset 62084h

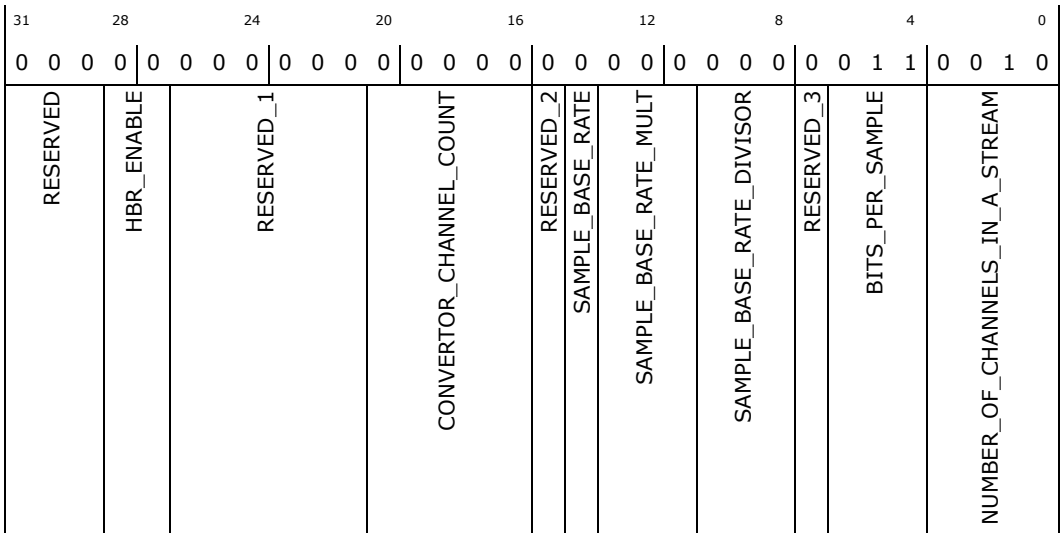
Audio Stream Descriptor Format Conv A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62084h

Default: 00000032h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Project: All Format:
28:27	0x0 RO	**HBR_ENABLE:** Project: All Format: This reflects the current HBR settings.
26:21	0x0 RO	**RESERVED_1:** Project: All Format:
20:16	0x0 RO	**CONVERTOR_CHANNEL_COUNT:** Project: All Format: This reflects the Convertor Channel Count programmed through HDAudio.
15	0x0 RO	**RESERVED_2:** Project: All Format:

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RO	**SAMPLE_BASE_RATE:** Project: All Default Value: ;0b 48 kHz Sampling base rate of audio stream. Value Name Description Project 0b 48 kHz 48 kHz All 1b 44.1 kHz 44.1 kHz All
13:11	0x0 RO	**SAMPLE_BASE_RATE_MULT:** Project: All Default Value: ;000b 48 kHz Audio stream sample base rate multiple. Value Name Description Project 000b x1 x1 (48 kHz/44.1 kHz or less) All 001b x2 x2 (96 kHz, 88.2 kHz, 32 kHz) All 010b x3 x3 (144 kHz) All 011b x4 x4 (192 kHz, 176.4 kHz) All 1XXb Reserved Reserved All
10:8	0x0 RO	**SAMPLE_BASE_RATE_DIVISOR:** Project: All Default Value: ;000b 48 kHz Audio stream sample base rate divisor. Value Name Description Project 000b Div 1 Divide by 1 (48 kHz, 44.1 kHz) All 001b Div 2 Divide by 2 (24 kHz, 22.05 kHz) All 010b Div 3 Divide by 3 (16 kHz, 32 kHz) All 011b Div 4 Divide by 4 (11.025 kHz) All 100b Div 5 Divide by 5 (9.6 kHz) All 101b Div 6 Divide by 6 (8 kHz) All 110b Div 7 Divide by 7 All 111b Div 8 Divide by 8 (6 kHz) All
7	0x0 RO	**RESERVED_3:** Project: All Format: MBZ
6:4	0x3 RO	**BITS_PER_SAMPLE:** Project: All Default Value: ;011b 32 bits Value Name Description Project 000b 8 bit The data will be packed in memory in 8 bit containers on 16 bit boundaries All 001b 16 bits The data will be packed in memory in 16 bit containers on 16 bit boundaries All 100b 20 bits The data will be packed in memory in 20 bit containers on 32 bit boundaries All 010b 24 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All 011b 32 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All Others Reserved Reserved All
3:0	0x2 RO	**NUMBER_OF_CHANNELS_IN_A_STREAM:** Project: All Default Value: ;0010b 3 channels in each frame Format: U4+1 Binary value plus 1. 0000 = 1, 1111= 16 Number of channels in each frame of the stream.

4.2.313 AUD_OUT_CH_STR—Offset 62088h

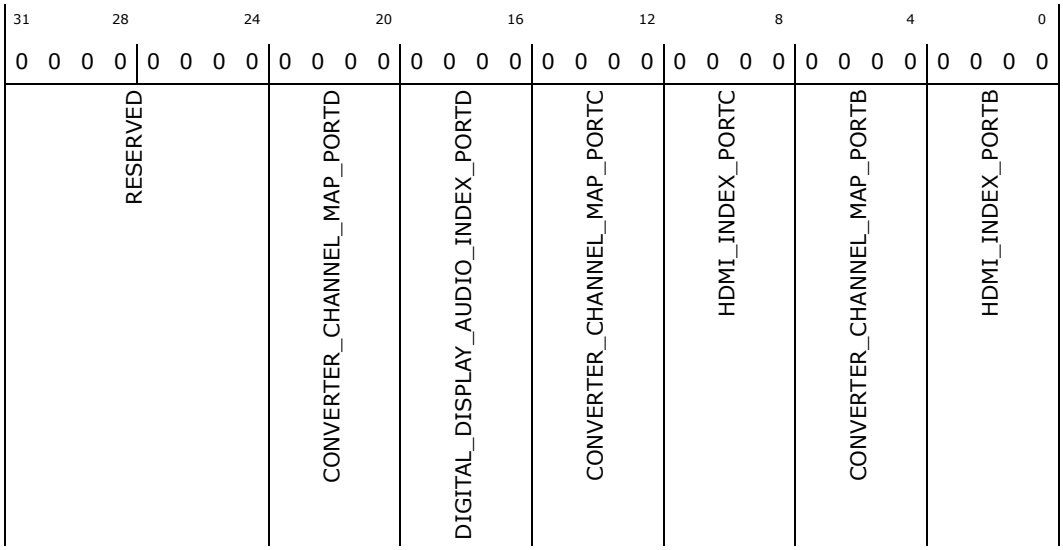
Audio Channel ID and Stream ID

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62088h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format:
23:20	0x0 RO	**CONVERTER_CHANNEL_MAP_PORTD:** Project: All The number in this field reflects the HD audio channel to which the Digital Display Audio channel in bits 19:16 is mapped. This field is read only
19:16	0x0 RO	**DIGITAL_DISPLAY_AUDIO_INDEX_PORTD:** Project: All This field is the Digital Display Audio channel number. When these bits are written, the audio channel number assigned to the Digital Display Audio channel number are reflected in bits 20:23 of this register.
15:12	0x0 RO	**CONVERTER_CHANNEL_MAP_PORTC:** Project: All The number in this field reflects the HD audio channel to which the Digital Display Audio channel in bits 11:8 is mapped. This field is read only
11:8	0x0 RO	**HDMI_INDEX_PORTC:** Project: All This field is the Digital Display Audio channel number. When these bits are written, the audio channel number assigned to the Digital Display Audio channel number are reflected in bits 12:15 of this register.
7:4	0x0 RO	**CONVERTER_CHANNEL_MAP_PORTB:** Project: All The number in this field reflects the HD audio channel to which the Digital Display Audio channel in bits 3:0 is mapped. This field is read only
3:0	0x0 RO	**HDMI_INDEX_PORTB:** Project: All This field is the Digital Display Audio channel number. When these bits are written, the audio channel number assigned to the Digital Display Audio channel number are reflected in bits 4:7 of this register.

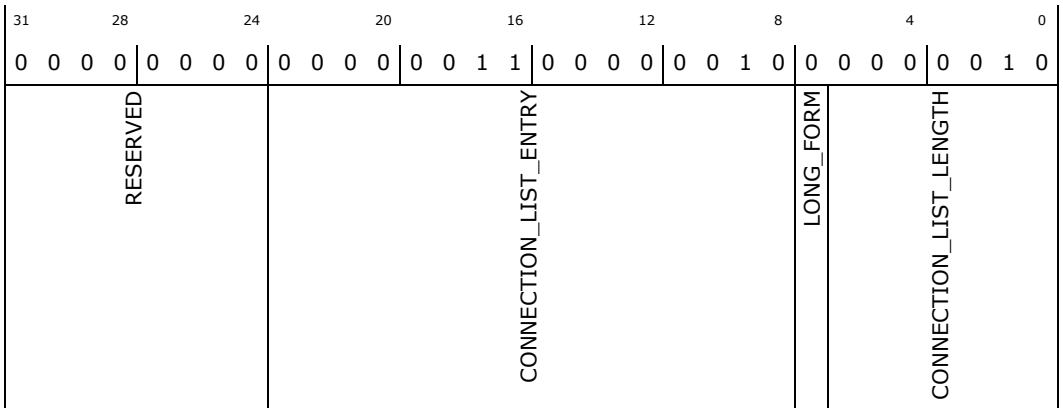
4.2.314 AUD_PINW_CONNLNG_LIST—Offset 620A8h

Audio Connection List

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 620A8h

Default: 00030202h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format:
23:8	0x302 RO	**CONNECTION_LIST_ENTRY:** Project: All Default Value: ;0000001100000010b Connection to Convertor Widget Node 0x0302
7	0x0 RO	**LONG_FORM:** Project: All Default Value: ;0b This bit indicates whether the items in the connection list are long form or short form. This bit is hardwired to 0 (items in connection list are short form)
6:0	0x2 RO	**CONNECTION_LIST_LENGTH:** Project: All Default Value: ;02h This field indicates the number of items in the connection list. If this field is 2, there is only one hardwired input possible, which is read from the Connection List, and there is no Connection Select Control.

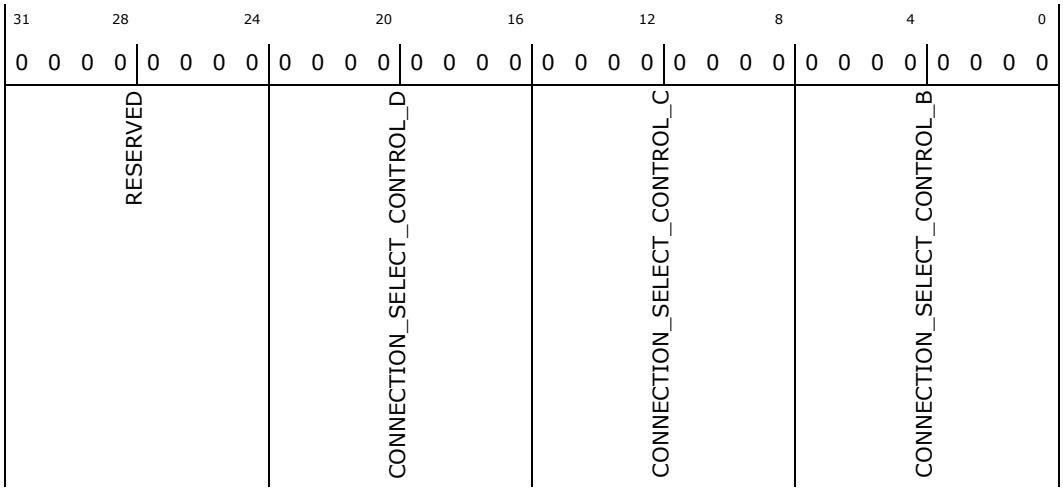
4.2.315 AUD_PINW_CONNLNG_SEL—Offset 620ACh

Audio Connection Select

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 620ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format:
23:16	0x0 RO	**CONNECTION_SELECT_CONTROL_D:** Project: All Format: Connection Index Currently Set [Default 0x00], Port D Widget is set to 0x00
15:8	0x0 RO	**CONNECTION_SELECT_CONTROL_C:** Project: All Format: Connection Index Currently Set [Default 0x00], Port C Widget is set to 0x00
7:0	0x0 RO	**CONNECTION_SELECT_CONTROL_B:** Project: All Format: Connection Index Currently Set [Default 0x00], Port B Widget is set to 0x00

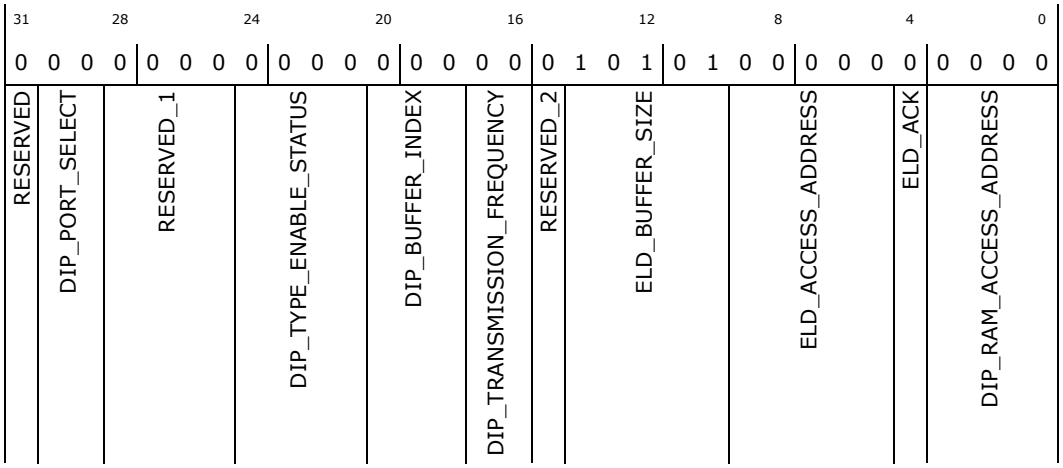
4.2.316 AUD_CNTL_ST_A—Offset 620B4h

Audio Control State Register Pipe A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 620B4h

Default: 00005400h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** Project: All Format: MBZ
30:29	0x0 RO	**DIP_PORT_SELECT:** Project: All AccessType: Read Only Default Value: ;00b This read-only bit reflects which port is used to transmit the DIP data. This can only change when DIP is disabled. If one or more audio-related DIP packets is enabled and audio is enabled on a digital port, these bits will reflect the digital port to which audio is directed. Value Name Description Project 00b Reserved Reserved All 01b Digital Port B Digital Port B All 10b Digital Port C Digital Port C All 11b Digital Port D Digital Port D All
28:25	0x0 RO	**RESERVED_1:** Project: All Format: MBZ
24:21	0x0 RO	**DIP_TYPE_ENABLE_STATUS:** Project: All AccessType: Read Only Default Value: ;0000b These bits reflect the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling a DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP. Value Name Description Project XXX0b Disable Audio DIP disabled All XXX1b Enable Audio DIP enabled All XX0Xb Disable Generic 1 (ACP) DIP disabled All XX1Xb Enable Generic 1 (ACP) DIP enabled All X0XXb Disable Generic 2 DIP disabled All X1XXb Enable Generic 2 DIP enabled, can be used by ISRC1 or ISRC2 All 1XXXb Reserved Reserved All

Bit Range	Default & Access	Field Name (ID): Description
20:18	0x0 RW	**DIP_BUFFER_INDEX:** Project: All Default Value: ;0000b This field is used during read of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0s. Value Name Description Project 000b Audio Audio DIP (31 bytes of address space, 31 bytes of data) All 001b Gen 1 Generic 1 (ACP) Data Island Packet (31 bytes of address space, 31 bytes of data) All 010b Gen 2 Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data) All 011b Gen 3 Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data) All 1XXb Reserved Reserved All
17:16	0x0 RO	**DIP_TRANSMISSION_FREQUENCY:** Project: All AccessType: Read Only Default Value: ;00b These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written. When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18. Value Name Description Project 00b Disable Disabled All 01b Reserved Reserved All 10b Send Once Send Once All 11b Best Effort Best effort (Send at least every other vsync) All
15	0x0 RO	**RESERVED_2:** Project: All Format: MBZ
14:10	0x15 RO	**ELD_BUFFER_SIZE:** Project: All AccessType: Read only 10101 = This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)
9:5	0x0 RW	**ELD_ACCESS_ADDRESS:** Project: All Selects the DWORD address for access to the ELD buffer (84 bytes). The value wraps back to zero when incremented past the max addressing value 0x1F. This field change takes effect immediately after being written. The read value indicates the current access address.
4	0x0 RO	**ELD_ACK:** Project: All AccessType: Read Only Acknowledgement from the audio driver that ELD read has been completed
3:0	0x0 RO	**DIP_RAM_ACCESS_ADDRESS:** Project: All AccessType: Read Only Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

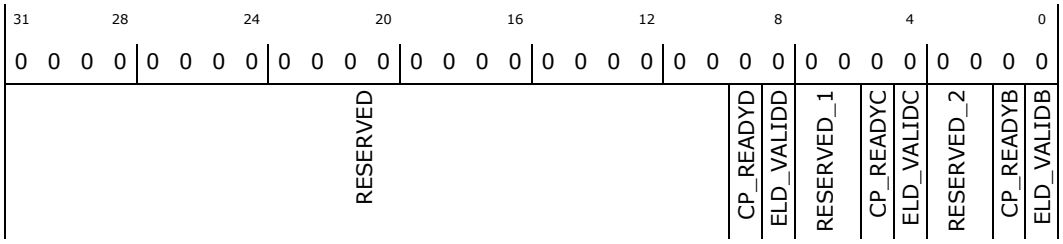
4.2.317 AUD_CNTL_ST2—Offset 620C0h

Audio Control State 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 620C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**RESERVED:** Project: All Format:
9	0x0 RW	**CP_READYD:** Project: All Default Value: ;0b This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. Value Name Description Project 0b Pending or Not Ready CP request pending or not ready to receive requests All 1b Ready CP request ready All
8	0x0 RW	**ELD_VALIDD:** Project: All Default Value: ;0b This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit. Value Name Description Project 0b Invalid ELD data invalid (default, when writing ELD data, set 0 by software) All 1b Valid ELD data valid (Set by video software only) All
7:6	0x0 RO	**RESERVED_1:** Project: All Format:
5	0x0 RW	**CP_READYC:** Project: All Default Value: ;0b Refer CP_ReadyD description. Value Name Description Project 0b Not Ready CP request pending or not ready to receive requests All 1b Ready CP request ready All
4	0x0 RW	**ELD_VALIDC:** Project: All Default Value: ;0b Refer ELD_validD descripion. Value Name Description Project 0b Invalid ELD data invalid (default, when writing ELD data, set 0 by software) All 1b Valid ELD data valid (Set by video software only) All

Bit Range	Default & Access	Field Name (ID): Description
3:2	0x0 RO	**RESERVED_2:** Project: All Format:
1	0x0 RW	**CP_READYB:** Project: All Default Value: ;0b Refer CP_ReadyD description. Value Name Description Project 0b Not Ready CP request pending or not ready to receive requests All 1b Ready CP request ready All
0	0x0 RW	**ELD_VALIDB:** Project: All Default Value: ;0b Refer ELD_validD descripion. Value Name Description Project 0b Invalid ELD data invalid (default, when writing ELD data, set 0 by software) All 1b Valid ELD data valid (Set by video software only) All

4.2.318 AUD_HDMIW_STATUS—Offset 620D4h

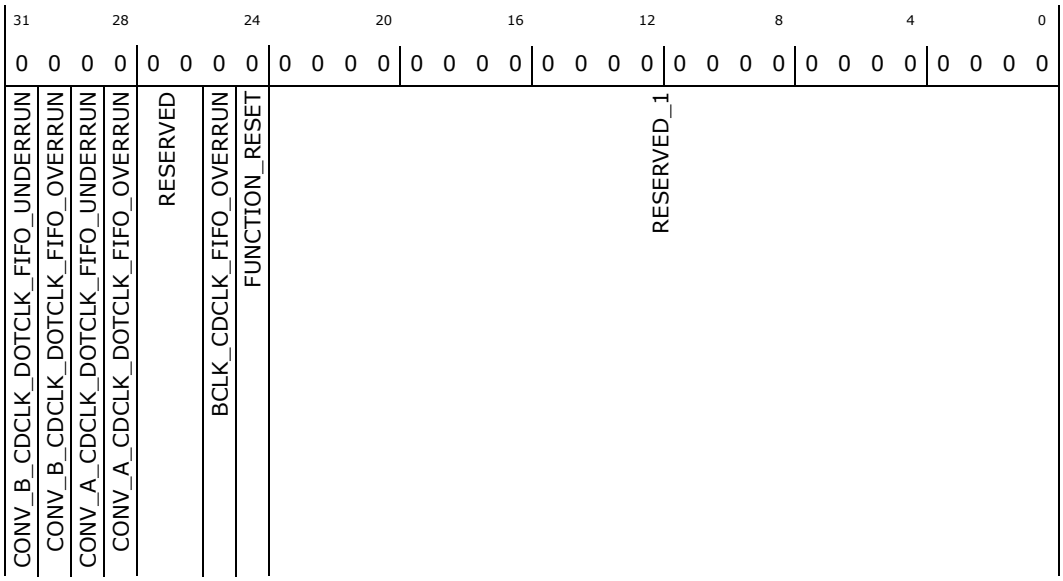
Audio HDMI Status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 620D4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**CONV_B_CDCLK_DOTCLK_FIFO_UNDERRUN:** Project: All This bit indicates an underrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
30	0x0 RW	**CONV_B_CDCLK_DOTCLK_FIFO_OVERRUN:** Project: All This bit indicates an overrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
29	0x0 RW	**CONV_A_CDCLK_DOTCLK_FIFO_UNDERRUN:** Project: All This bit indicates an underrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
28	0x0 RW	**CONV_A_CDCLK_DOTCLK_FIFO_OVERRUN:** Project: All This bit indicates an overrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
27:26	0x0 RO	**RESERVED:** Project: All Format:
25	0x0 RW	**BCLK_CDCLK_FIFO_OVERRUN:** Project: All This bit indicates an overrun in the FIFO inside the clock crossing logic between BCLK and CDCLK. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
24	0x0 RW	**FUNCTION_RESET:** Project: All Security: Debug This bit indicates that an audio function reset occurred through the reset signal on the HD audio bus. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.
23:0	0x0 RO	**RESERVED_1:** Project: All Format:

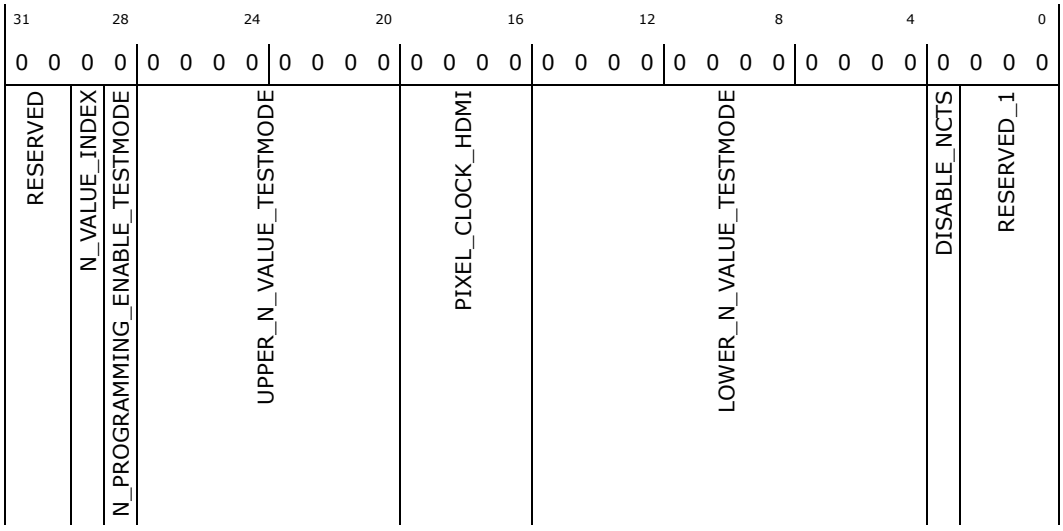
4.2.319 AUD_CONFIG_B—Offset 62100h

Audio Configuration Pipe B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 62100h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RESERVED:** Project: All Format:
29	0x0 RW	**N_VALUE_INDEX:** Project: All Default Value: ;0b Value Name Description Project 0b HDMI N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are is programmable to any N value - default h7FA6. All 1b DP N value read on bits 27:20 and 15:4 reflects DP N value. Set this bit to 1 before programming N value register. When this is set to 1, 27:20 and 15:4 will reflect the current N value default h8000. All
28	0x0 RW	**N_PROGRAMMING_ENABLE_TESTMODE:** Project: All Security: Test Refer Pipe A description.
27:20	0x0 RW	**UPPER_N_VALUE_TESTMODE:** Project: All Security: Test Refer Pipe A description
19:16	0x0 RW	**PIXEL_CLOCK_HDMI:** Project: All Default Value: ;0b Refer Pipe A description. Value Name Description Project 0000b 25.2 / 1.001 MHz 25.2 / 1.001 MHz All 0001b 25.2 MHz 25.2 MHz Program this value for pixel clocks not listed in this field All 0010b 27 MHz 27 MHz All 0011b 27 * 1.001 MHz 27 * 1.001 MHz All 0100b 54 MHz 54 MHz All 0101b 54 * 1.001 MHz 54 * 1.001 MHz All 0110b 74.25 / 1.001 MHz 74.25 / 1.001 MHz All 0111b 74.25 MHz 74.25 MHz All 1000b 148.5 / 1.001 MHz 148.5 / 1.001 MHz All 1001b 148.5 MHz 148.5 MHz All others Reserved Reserved All
15:4	0x0 RW	**LOWER_N_VALUE_TESTMODE:** Project: All Security: Test Refer Pipe A description

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**DISABLE_NCTS:** Project: All Refer Pipe A description
2:0	0x0 RO	**RESERVED_1:** Project: All Format:

4.2.320 AUD_MISC_CTRL_B—Offset 62110h

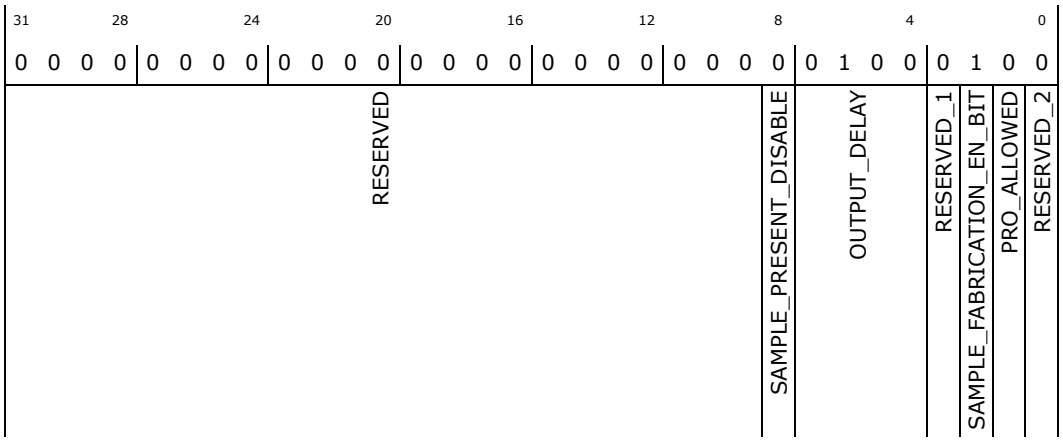
Audio MISC Control for Pipe B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62110h

Default: 00000044h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**RESERVED:** Project: All Format: MBZ
8	0x0 RW	**SAMPLE_PRESENT_DISABLE:** Project: All Security: Debug Refer Pipe A description
7:4	0x4 RW	**OUTPUT_DELAY:** Project: All Default Value: ;0100b Refer Pipe A description.
3	0x0 RO	**RESERVED_1:** Project: All Format: MBZ
2	0x1 RW	**SAMPLE_FABRICATION_EN_BIT:** Project: All Access: R/W Default Value: ;1b Refer Pipe A description. Value Name Description Project 0b Disable Audio fabrication disabled All 1b Enable Audio fabrication enabled All

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**PRO_ALLOWED:** Project: All Access: R/W Default Value: ;0b Refer Pipe A description. Value Name Description Project 0b Consumer Consumer use only All 1b Professional Professional use allowed All
0	0x0 RO	**RESERVED_2:** All Format: MBZ

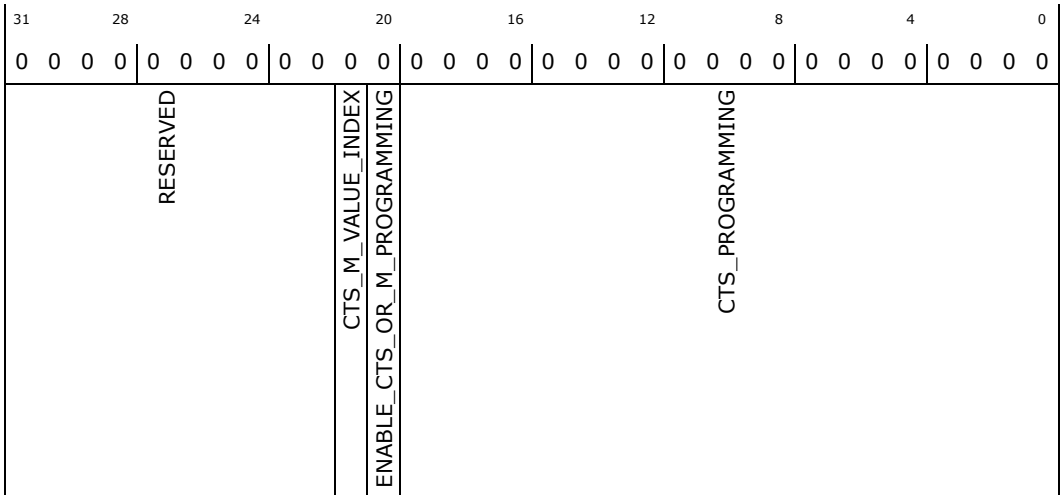
4.2.321 AUD_CTS_ENABLE_B—Offset 62128h

Audio CTS Programming Enable Pipe B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 62128h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**RESERVED:** Project: All Format:
21	0x0 RW	**CTS_M_VALUE_INDEX:** Project: All Default Value: ;0b Value Name Description Project 0b CTS CTS value read on bits 23:4 reflects CTS value. Bit 23:4 is programmable to any CTS value. default is 0 All 1b M M value read on bits 21:4 reflects DP M value. Set this bit to 1 before programming M value register. When this is set to 1 23:4 will reflect the current N value All

Bit Range	Default & Access	Field Name (ID): Description
20	0x0 RW	**ENABLE_CTS_OR_M_PROGRAMMING:** Project: All Refer Pipe A description.
19:0	0x0 RW	**CTS_PROGRAMMING:** Project: All Refer Pipe A description.

4.2.322 AUD_HDMIW_HDMIEDID_B—Offset 62150h

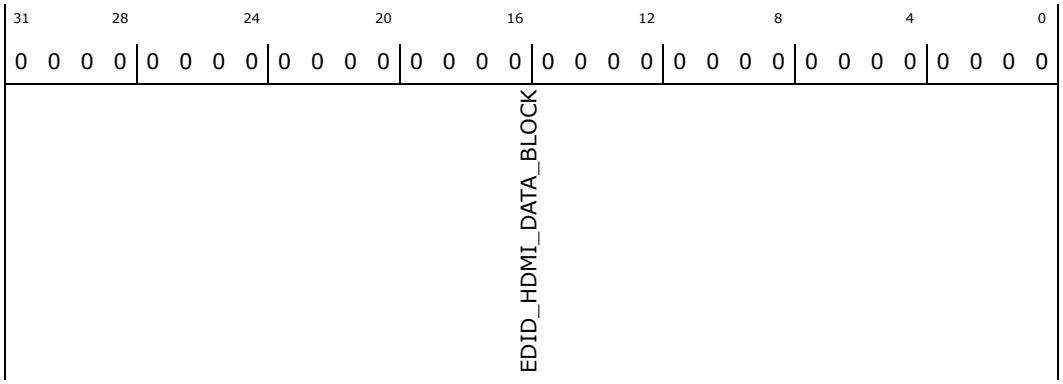
HDMI Data EDID Block Pipe B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62150h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**EDID_HDMI_DATA_BLOCK:** Project: All Format: Refer Pipe A description

4.2.323 AUD_HDMIW_INFOFR_B—Offset 62154h

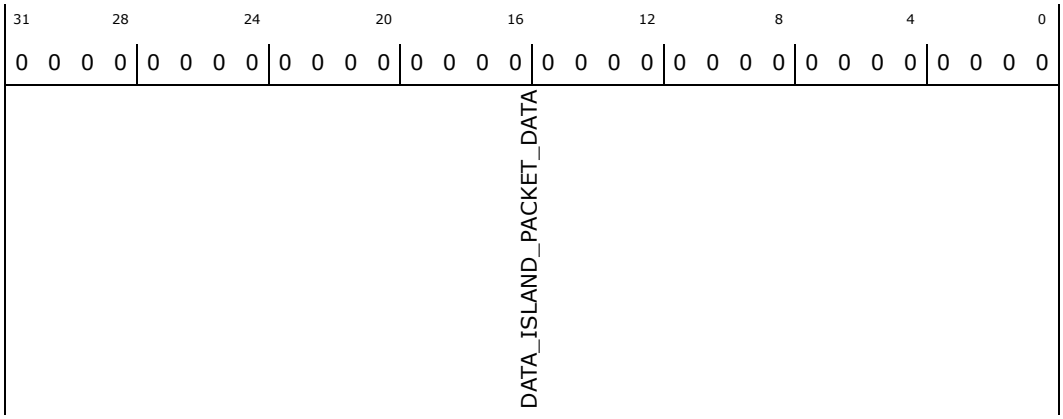
Audio Widget Data Island Packet Pipe B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62154h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**DATA_ISLAND_PACKET_DATA:** Project: All Format: Refer Pipe A description.

4.2.324 AUD_OUT_DIG_CNVT_B—Offset 62180h

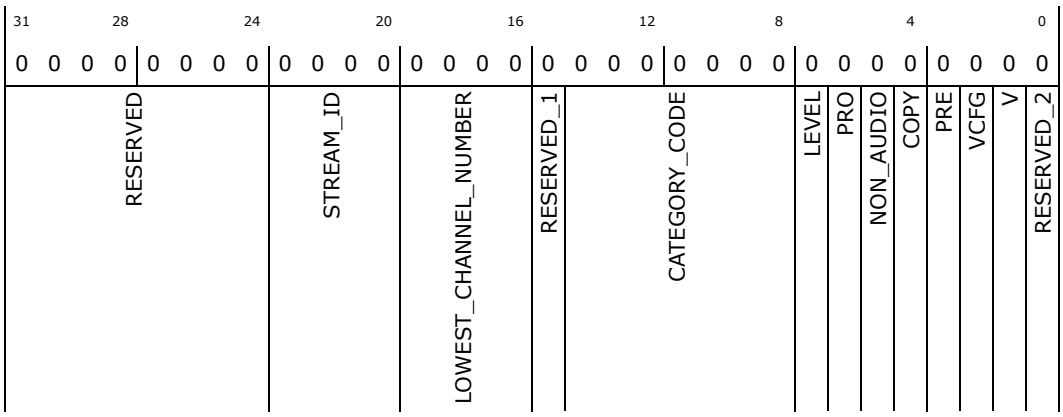
Audio Digital Converter Conv B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62180h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format:
23:20	0x0 RO	**STREAM_ID:** Project: All Format: Refer Conv A description.

Bit Range	Default & Access	Field Name (ID): Description
19:16	0x0 RO	**LOWEST_CHANNEL_NUMBER:** Project: All Format: Refer Conv A description
15	0x0 RO	**RESERVED_1:** Project: All Format:
14:8	0x0 RO	**CATEGORY_CODE:** Project: All Format: Refer Conv A description
7	0x0 RO	**LEVEL:** Project: All Format: Refer Conv A description
6	0x0 RO	**PRO:** Project: All Default Value: ;0b Refer Conv A description Value Name Description Project 0b Consumer Consumer use All 1b Professional Professional use All
5	0x0 RO	**NON_AUDIO:** Project: All Default Value: ;0b Refer Conv A description. Value Name Description Project 0b PCM Data is PCM All 1b Non PCM Data is non PCM format All
4	0x0 RO	**COPY:** Project: All Default Value: ;0b Refer Conv A description Value Name Description Project 0b Not Asserted Copyright is not asserted All 1b Asserted Copyright is asserted All
3	0x0 RO	**PRE:** Project: All Default Value: ;0b Refer Conv A description Value Name Description Project 0b Disabled Preemphasis is disabled All 1b Enabled Filter preemphasis is enabled All
2	0x0 RO	**VCFG:** Project: All Format: Refer Conv A description
1	0x0 RO	**V:** Project: All Format: Refer Conv A description
0	0x0 RO	**RESERVED_2:** All Format: MBZ

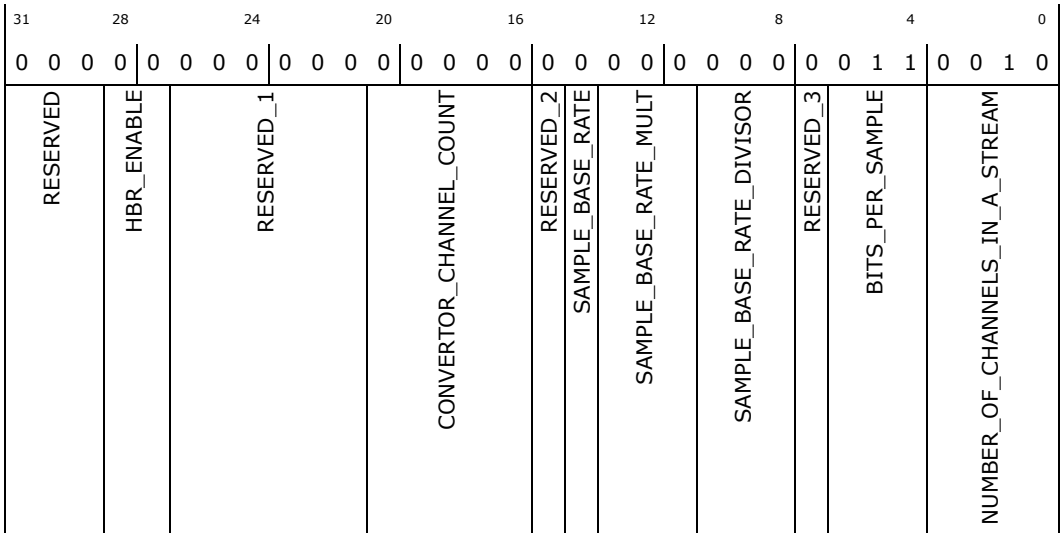
4.2.325 AUD_OUT_STR_DESC_B—Offset 62184h

Audio Stream Descriptor Format Conv B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 62184h

Default: 00000032h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Project: All Format:
28:27	0x0 RO	**HBR_ENABLE:** Project: All Format: Refer Conv A description.
26:21	0x0 RO	**RESERVED_1:** Project: All Format:
20:16	0x0 RO	**CONVERTOR_CHANNEL_COUNT:** Project: All Format: Refer Conv A description.
15	0x0 RO	**RESERVED_2:** Project: All Format:
14	0x0 RO	**SAMPLE_BASE_RATE:** Project: All Default Value: ;0b 48 kHz Refer Conv A description. Value Name Description Project 0b 48 kHz 48 kHz All 1b 44.1 kHz 44.1 kHz All
13:11	0x0 RO	**SAMPLE_BASE_RATE_MULT:** Project: All Default Value: ;000b 48 kHz Refer Conv A description. Value Name Description Project 000b x1 x1 (48 kHz/44.1 kHz or less) All 001b x2 x2 (96 kHz, 88.2 kHz, 32 kHz) All 010b x3 x3 (144 kHz) All 011b x4 x4 (192 kHz, 176.4 kHz) All 1XXb Reserved Reserved All

Bit Range	Default & Access	Field Name (ID): Description
10:8	0x0 RO	**SAMPLE_BASE_RATE_DIVISOR:** Project: All Default Value: ;000b 48 kHz Refer Conv A description. Value Name Description Project 000b Div 1 Divide by 1 (48 kHz, 44.1 kHz) All 001b Div 2 Divide by 2 (24 kHz, 22.05 kHz) All 010b Div 3 Divide by 3 (16 kHz, 32 kHz) All 011b Div 4 Divide by 4 (11.025 kHz) All 100b Div 5 Divide by 5 (9.6 kHz) All 101b Div 6 Divide by 6 (8 kHz) All 110b Div 7 Divide by 7 All 111b Div 8 Divide by 8 (6 kHz) All
7	0x0 RO	**RESERVED_3:** Project: All Format: MBZ
6:4	0x3 RO	**BITS_PER_SAMPLE:** Project: All Default Value: ;011b 32 bits Value Name Description Project 000b 8 bit The data will be packed in memory in 8 bit containers on 16 bit boundaries All 001b 16 bits The data will be packed in memory in 16 bit containers on 16 bit boundaries All 100b 20 bits The data will be packed in memory in 20 bit containers on 32 bit boundaries All 010b 24 bits The data will be packed in memory in 24 bit containers on 32 bit boundaries All 011b 32 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All others Res. Reserved All
3:0	0x2 RO	**NUMBER_OF_CHANNELS_IN_A_STREAM:** Project: All Default Value: ;0010b 3 channels in each frame Format: U4+1 Binary value plus 1. 0000 = 1, 1111= 16 Refer Conv A description.

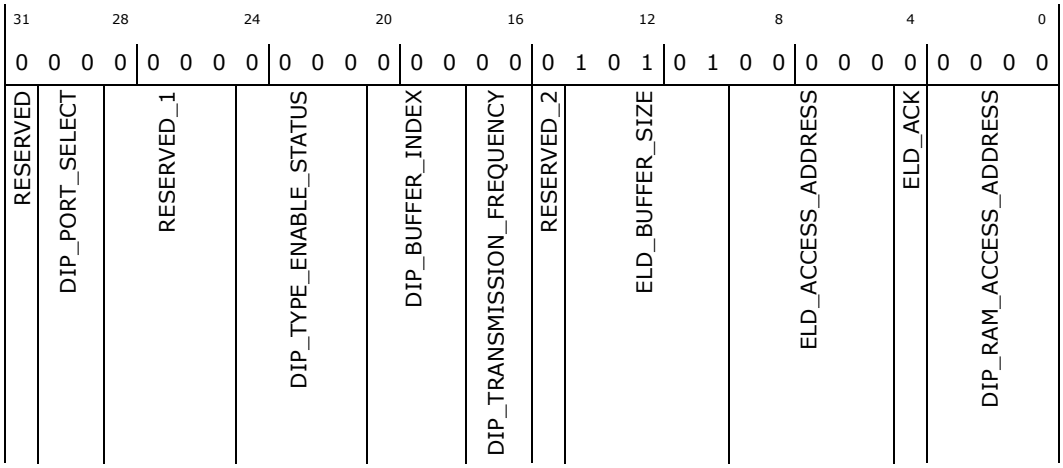
4.2.326 AUD_CNTL_ST_B—Offset 621B4h

Audio Control State Register Pipe B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 621B4h

Default: 00005400h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** Project: All Format: MBZ
30:29	0x0 RO	**DIP_PORT_SELECT:** Project: All AccessType: Read Only Default Value: ;00b Refer Pipe A description. Value Name Description Project 00b Reserved Reserved All 01b Digital Port B Digital Port B All 10b Digital Port C Digital Port C All 11b Digital Port D Digital Port D All
28:25	0x0 RO	**RESERVED_1:** Project: All Format: MBZ
24:21	0x0 RO	**DIP_TYPE_ENABLE_STATUS:** Project: All AccessType: Read Only Default Value: ;0000b Refer Pipe A description. Value Name Description Project XXX0b Disable Audio DIP disabled (Default) All XXX1b Enable Audio DIP enabled All XX0Xb Disable Generic 1 (ACP) DIP disabled All XX1Xb Enable Generic 1 (ACP) DIP enabled All X0XXb Disable Generic 2 DIP disabled All X1XXb Enable Generic 2 DIP enabled, can be used by ISRC1 or ISRC2 All 1XXXb Reserved Reserved All

Bit Range	Default & Access	Field Name (ID): Description
20:18	0x0 RW	**DIP_BUFFER_INDEX:** Project: All Default Value: ;000b Refer Pipe A description. Value Name Description Project 000b Audio Audio DIP (31 bytes of address space, 31 bytes of data) All 001b Gen 1 Generic 1 (ACP) Data Island Packet (31 bytes of address space, 11 bytes of data) All 010b Gen 2 Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data) All 011b Gen 3 Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data) All 1XXb Reserved Reserved All
17:16	0x0 RO	**DIP_TRANSMISSION_FREQUENCY:** Project: All AccessType: Read Only Default Value: ;00b Refer Pipe A description Value Name Description Project 00b Disable Disabled All 01b Reserved Reserved All 10b Send Once Send Once All 11b Best Effort Best effort (Send at least every other vsync) All
15	0x0 RO	**RESERVED_2:** Project: All Format: MBZ
14:10	0x15 RO	**ELD_BUFFER_SIZE:** Project: All AccessType: Read Only 10101 = This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)
9:5	0x0 RW	**ELD_ACCESS_ADDRESS:** Project: All Refer Pipe A description.
4	0x0 RO	**ELD_ACK:** Project: All AccessType: Read Only Refer Pipe A description.
3:0	0x0 RO	**DIP_RAM_ACCESS_ADDRESS:** Project: All AccessType: Read only Refer Pipe A description.

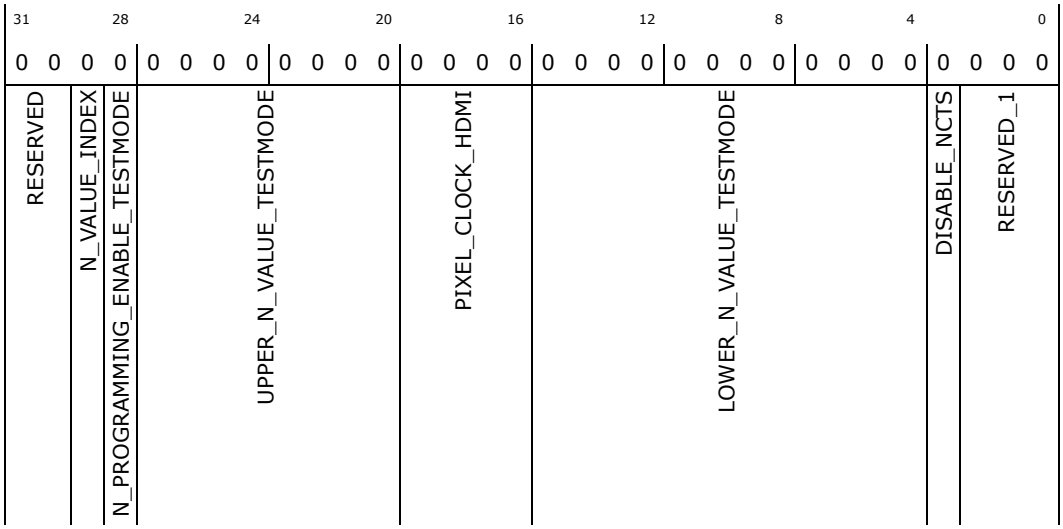
4.2.327 AUD_CONFIG_C—Offset 62200h

Audio Configuration Pipe C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 62200h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RESERVED:** Project: All Format:
29	0x0 RW	**N_VALUE_INDEX:** Project: All Default Value: ;0b Value Name Description Project 0b HDMI N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are is programmable to any N value - default h7FA6. All 1b DP N value read on bits 27:20 and 15:4 reflects DP N value. Set this bit to 1 before programming N value register. When this is set to 1, 27:20 and 15:4 will reflect the current N value default h8000. All
28	0x0 RW	**N_PROGRAMMING_ENABLE_TESTMODE:** Project: All Security: Test Refer Pipe A description.
27:20	0x0 RW	**UPPER_N_VALUE_TESTMODE:** Project: All Security: Test Refer Pipe A description
19:16	0x0 RW	**PIXEL_CLOCK_HDMI:** Project: All Default Value: ;0b Refer Pipe A description. Value Name Description Project 0000b 25.2 / 1.001 MHz 25.2 / 1.001 MHz All 0001b 25.2 MHz 25.2 MHz Program this value for pixel clocks not listed in this field All 0010b 27 MHz 27 MHz All 0011b 27 * 1.001 MHz 27 * 1.001 MHz All 0100b 54 MHz 54 MHz All 0101b 54 * 1.001 MHz 54 * 1.001 MHz All 0110b 74.25 / 1.001 MHz 74.25 / 1.001 MHz All 0111b 74.25 MHz 74.25 MHz All 1000b 148.5 / 1.001 MHz 148.5 / 1.001 MHz All 1001b 148.5 MHz 148.5 MHz All others Reserved Reserved All
15:4	0x0 RW	**LOWER_N_VALUE_TESTMODE:** Project: All Security: Test Refer Pipe A description

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**DISABLE_NCTS:** Project: All Refer Pipe A description
2:0	0x0 RO	**RESERVED_1:** Project: All Format:

4.2.328 AUD_MISC_CTRL_C—Offset 62210h

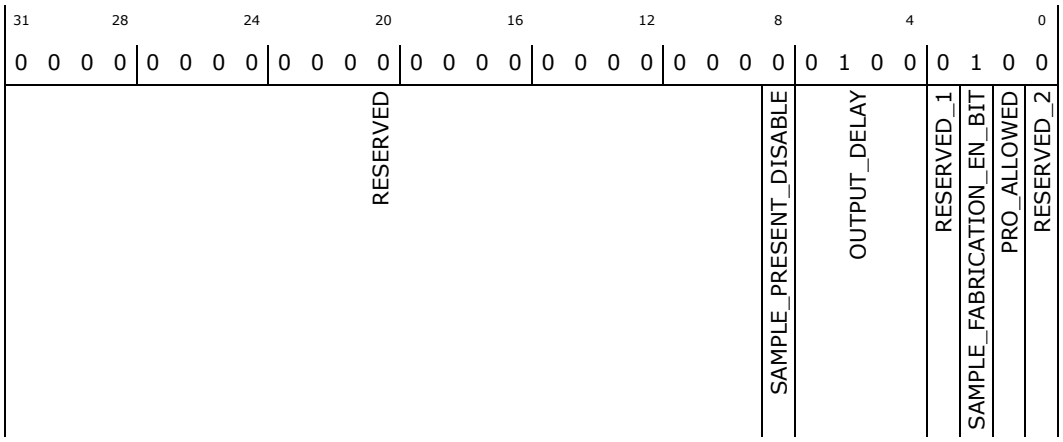
Audio MISC Control for Pipe C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62210h

Default: 00000044h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**RESERVED:** Project: All Format: MBZ
8	0x0 RW	**SAMPLE_PRESENT_DISABLE:** Project: All Security: Debug Refer Pipe A description
7:4	0x4 RW	**OUTPUT_DELAY:** Project: All Default Value: ;0100b Refer Pipe A description.
3	0x0 RO	**RESERVED_1:** Project: All Format: MBZ
2	0x1 RW	**SAMPLE_FABRICATION_EN_BIT:** Project: All Access: R/W Default Value: ;1b Refer Pipe A description. Value Name Description Project 0b Disable Audio fabrication disabled All 1b Enable Audio fabrication enabled All

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**PRO_ALLOWED:** Project: All Access: R/W Default Value: ;0b Refer Pipe A description. Value Name Description Project 0b Consumer Consumer use only All 1b Professional Professional use allowed All
0	0x0 RO	**RESERVED_2:** All Format: MBZ

4.2.329 AUD_CTS_ENABLE_C—Offset 62228h

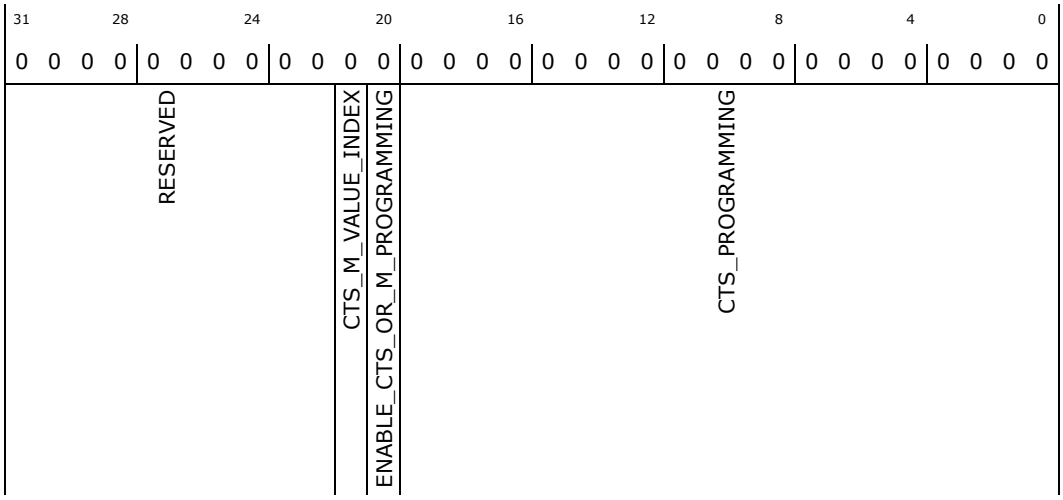
Audio CTS Programming Enable Pipe C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62228h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**RESERVED:** Project: All Format:
21	0x0 RW	**CTS_M_VALUE_INDEX:** Project: All Default Value: ;0b Value Name Description Project 0b CTS CTS value read on bits 23:4 reflects CTS value. Bit 23:4 is programmable to any CTS value. default is 0 All 1b M M value read on bits 21:4 reflects DP M value. Set this bit to 1 before programming M value register. When this is set to 1 23:4 will reflect the current N value All

Bit Range	Default & Access	Field Name (ID): Description
20	0x0 RW	**ENABLE_CTS_OR_M_PROGRAMMING:** Project: All Refer Pipe A description.
19:0	0x0 RW	**CTS_PROGRAMMING:** Project: All Refer Pipe A description.

4.2.330 AUD_HDMIW_HDMIEDID_C—Offset 62250h

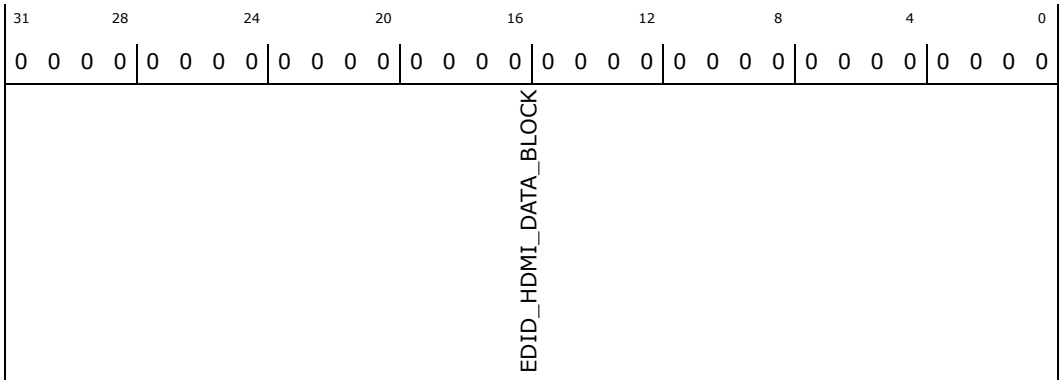
HDMI Data EDID Block Pipe C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62250h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**EDID_HDMI_DATA_BLOCK:** Project: All Format: Refer Pipe A description

4.2.331 AUD_HDMIW_INFOFR_C—Offset 62254h

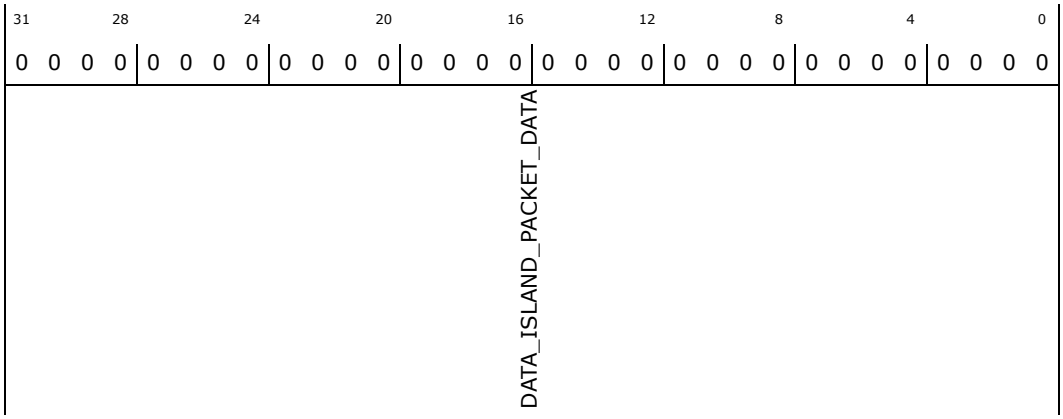
Audio Widget Data Island Packet Pipe C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62254h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**DATA_ISLAND_PACKET_DATA:** Project: All Format: Refer Pipe A description.

4.2.332 AUD_OUT_DIG_CNVT_C—Offset 62280h

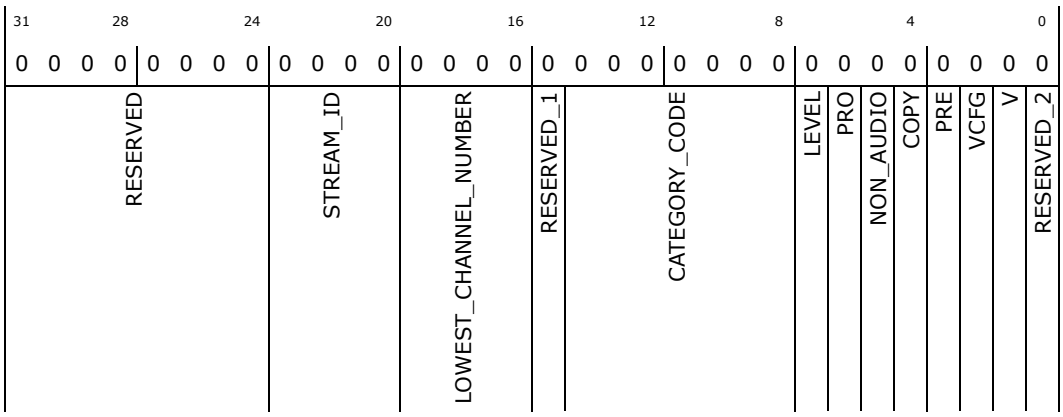
Audio Digital Converter Conv C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62280h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format:
23:20	0x0 RO	**STREAM_ID:** Project: All Format: Refer Conv A description.

Bit Range	Default & Access	Field Name (ID): Description
19:16	0x0 RO	**LOWEST_CHANNEL_NUMBER:** Project: All Format: Refer Conv A description
15	0x0 RO	**RESERVED_1:** Project: All Format:
14:8	0x0 RO	**CATEGORY_CODE:** Project: All Format: Refer Conv A description
7	0x0 RO	**LEVEL:** Project: All Format: Refer Conv A description
6	0x0 RO	**PRO:** Project: All Default Value: ;0b Refer Conv A description Value Name Description Project 0b Consumer Consumer use All 1b Professional Professional use All
5	0x0 RO	**NON_AUDIO:** Project: All Default Value: ;0b Refer Conv A description. Value Name Description Project 0b PCM Data is PCM All 1b Non PCM Data is non PCM format All
4	0x0 RO	**COPY:** Project: All Default Value: ;0b Refer Conv A description Value Name Description Project 0b Not Asserted Copyright is not asserted All 1b Asserted Copyright is asserted All
3	0x0 RO	**PRE:** Project: All Default Value: ;0b Refer Conv A description Value Name Description Project 0b Disabled Preemphasis is disabled All 1b Enabled Filter preemphasis is enabled All
2	0x0 RO	**VCFG:** Project: All Format: Refer Conv A description
1	0x0 RO	**V:** Project: All Format: Refer Conv A description
0	0x0 RO	**RESERVED_2:** All Format: MBZ

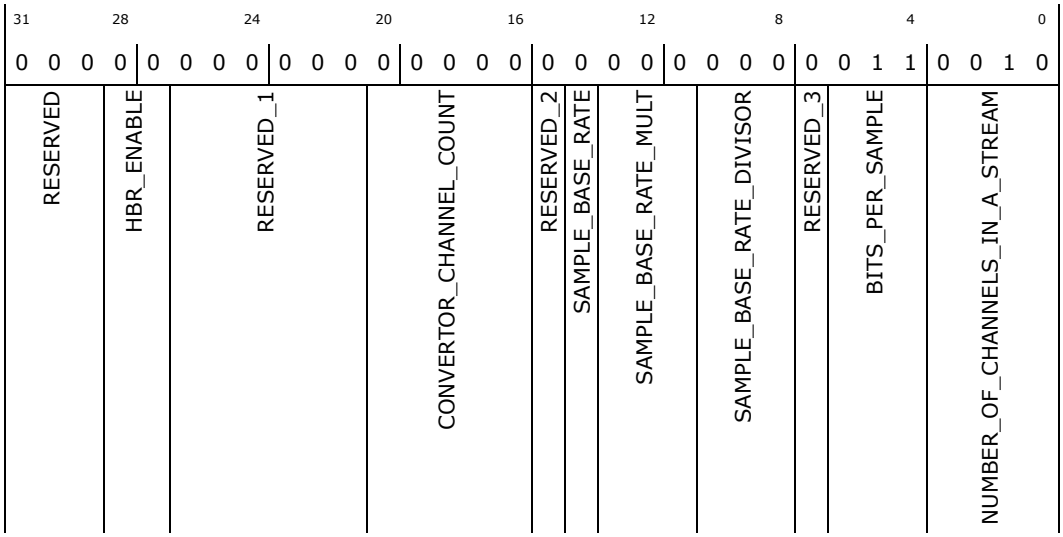
4.2.333 AUD_OUT_STR_DESC_C—Offset 62284h

Audio Stream Descriptor Format Conv C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 62284h

Default: 00000032h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Project: All Format:
28:27	0x0 RO	**HBR_ENABLE:** Project: All Format: Refer Conv A description.
26:21	0x0 RO	**RESERVED_1:** Project: All Format:
20:16	0x0 RO	**CONVERTOR_CHANNEL_COUNT:** Project: All Format: Refer Conv A description.
15	0x0 RO	**RESERVED_2:** Project: All Format:
14	0x0 RO	**SAMPLE_BASE_RATE:** Project: All Default Value: ;0b 48 kHz Refer Conv A description. Value Name Description Project 0b 48 kHz 48 kHz All 1b 44.1 kHz 44.1 kHz All
13:11	0x0 RO	**SAMPLE_BASE_RATE_MULT:** Project: All Default Value: ;000b 48 kHz Refer Conv A description. Value Name Description Project 000b x1 x1 (48 kHz/44.1 kHz or less) All 001b x2 x2 (96 kHz, 88.2 kHz, 32 kHz) All 010b x3 x3 (144 kHz) All 011b x4 x4 (192 kHz, 176.4 kHz) All 1XXb Reserved Reserved All

Bit Range	Default & Access	Field Name (ID): Description
10:8	0x0 RO	**SAMPLE_BASE_RATE_DIVISOR:** Project: All Default Value: ;000b 48 kHz Refer Conv A description. Value Name Description Project 000b Div 1 Divide by 1 (48 kHz, 44.1 kHz) All 001b Div 2 Divide by 2 (24 kHz, 22.05 kHz) All 010b Div 3 Divide by 3 (16 kHz, 32 kHz) All 011b Div 4 Divide by 4 (11.025 kHz) All 100b Div 5 Divide by 5 (9.6 kHz) All 101b Div 6 Divide by 6 (8 kHz) All 110b Div 7 Divide by 7 All 111b Div 8 Divide by 8 (6 kHz) All
7	0x0 RO	**RESERVED_3:** Project: All Format: MBZ
6:4	0x3 RO	**BITS_PER_SAMPLE:** Project: All Default Value: ;011b 32 bits Value Name Description Project 000b 8 bit The data will be packed in memory in 8 bit containers on 16 bit boundaries All 001b 16 bits The data will be packed in memory in 16 bit containers on 16 bit boundaries All 100b 20 bits The data will be packed in memory in 20 bit containers on 32 bit boundaries All 010b 24 bits The data will be packed in memory in 24 bit containers on 32 bit boundaries All 011b 32 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All others Res. Reserved All
3:0	0x2 RO	**NUMBER_OF_CHANNELS_IN_A_STREAM:** Project: All Default Value: ;0010b 3 channels in each frame Format: U4+1 Binary value plus 1. 0000 = 1, 1111= 16 Refer Conv A description.

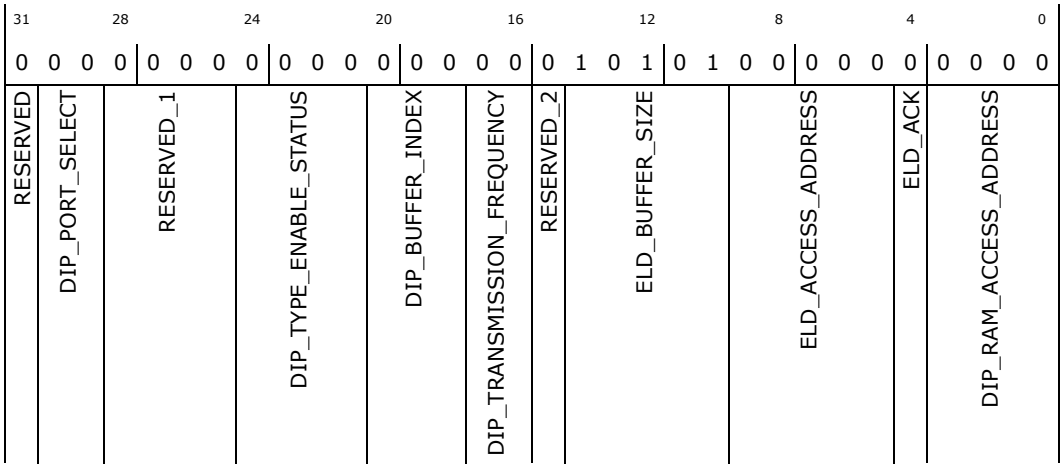
4.2.334 AUD_CNTL_ST_B (AUD_CNTL_ST_C)—Offset 622B4h

Audio Control State Register Pipe C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 622B4h

Default: 00005400h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** Project: All Format: MBZ
30:29	0x0 RO	**DIP_PORT_SELECT:** Project: All AccessType: Read Only Default Value: ;00b Refer Pipe A description. Value Name Description Project 00b Reserved Reserved All 01b Digital Port B Digital Port B All 10b Digital Port C Digital Port C All 11b Digital Port D Digital Port D All
28:25	0x0 RO	**RESERVED_1:** Project: All Format: MBZ
24:21	0x0 RO	**DIP_TYPE_ENABLE_STATUS:** Project: All AccessType: Read Only Default Value: ;0000b Refer Pipe A description. Value Name Description Project XXX0b Disable Audio DIP disabled (Default) All XXX1b Enable Audio DIP enabled All XX0Xb Disable Generic 1 (ACP) DIP disabled All XX1Xb Enable Generic 1 (ACP) DIP enabled All X0XXb Disable Generic 2 DIP disabled All X1XXb Enable Generic 2 DIP enabled, can be used by ISRC1 or ISRC2 All 1XXXb Reserved Reserved All

Bit Range	Default & Access	Field Name (ID): Description
20:18	0x0 RW	**DIP_BUFFER_INDEX:** Project: All Default Value: ;000b Refer Pipe A description. Value Name Description Project 000b Audio Audio DIP (31 bytes of address space, 31 bytes of data) All 001b Gen 1 Generic 1 (ACP) Data Island Packet (31 bytes of address space, 11 bytes of data) All 010b Gen 2 Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data) All 011b Gen 3 Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data) All 1XXb Reserved Reserved All
17:16	0x0 RO	**DIP_TRANSMISSION_FREQUENCY:** Project: All AccessType: Read Only Default Value: ;00b Refer Pipe A description Value Name Description Project 00b Disable Disabled All 01b Reserved Reserved All 10b Send Once Send Once All 11b Best Effort Best effort (Send at least every other vsync) All
15	0x0 RO	**RESERVED_2:** Project: All Format: MBZ
14:10	0x15 RO	**ELD_BUFFER_SIZE:** Project: All AccessType: Read Only 10101 = This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)
9:5	0x0 RW	**ELD_ACCESS_ADDRESS:** Project: All Refer Pipe A description.
4	0x0 RO	**ELD_ACK:** Project: All AccessType: Read Only Refer Pipe A description.
3:0	0x0 RO	**DIP_RAM_ACCESS_ADDRESS:** Project: All AccessType: Read only Refer Pipe A description.

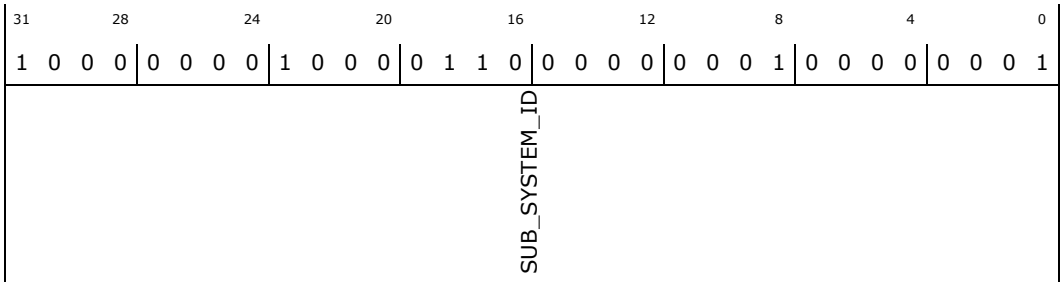
4.2.335 AUD_SSID_DBG—Offset 62F00h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F00h

Default: 80860101h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x80860101 WO	**SUB_SYSTEM_ID:** Project: All

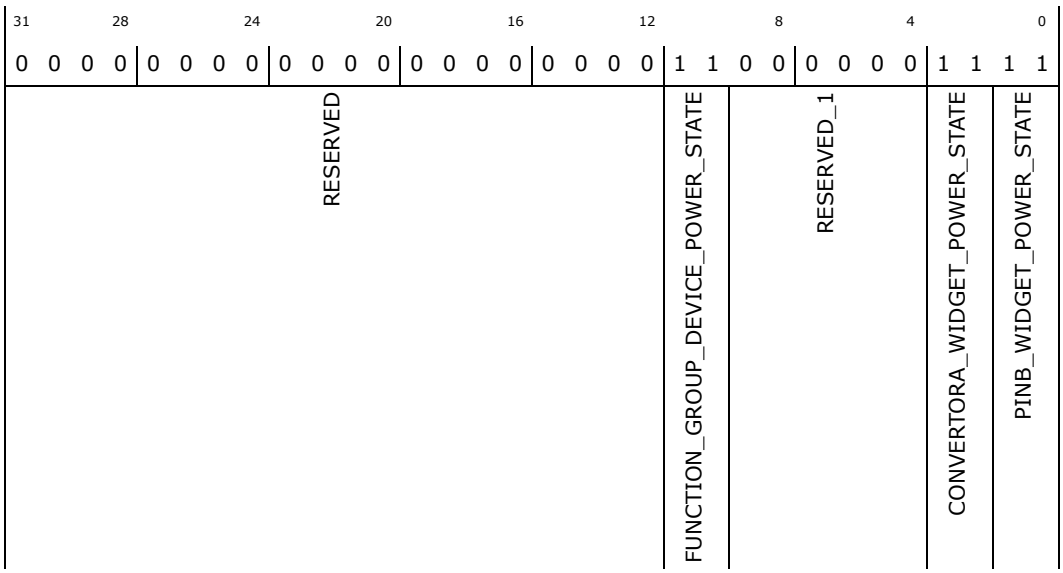
4.2.336 AUD_PWST1_DBG—Offset 62F04h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F04h

Default: 00000C0Fh



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RESERVED:** Project: All Format: MBZ

Bit Range	Default & Access	Field Name (ID): Description
11:10	0x3 WO	**FUNCTION_GROUP_DEVICE_POWER_STATE:** Project: All Default Value: ;11b D3 Power state that was set Value Name Description Project 00b D0 D0 All 01b, 10b Unsupported Unsupported All 11b D3 D3 (Default)
9:4	0x0 RO	**RESERVED_1:** Project: All Format: MBZ
3:2	0x3 WO	**CONVERTORA_WIDGET_POWER_STATE:** Project: All Default Value: ;11b D3 Power state that was requested by audio software Value Name Description Project 00b D0 D0 All 01b, 10b Unsupported Unsupported All 11b D3 D3 (Default)
1:0	0x3 WO	**PINB_WIDGET_POWER_STATE:** Project: All Default Value: ;11b D3 Power state that was set Value Name Description Project 00b D0 D0 All 01b, 10b Unsupported Unsupported All 11b D3 D3 (Default)

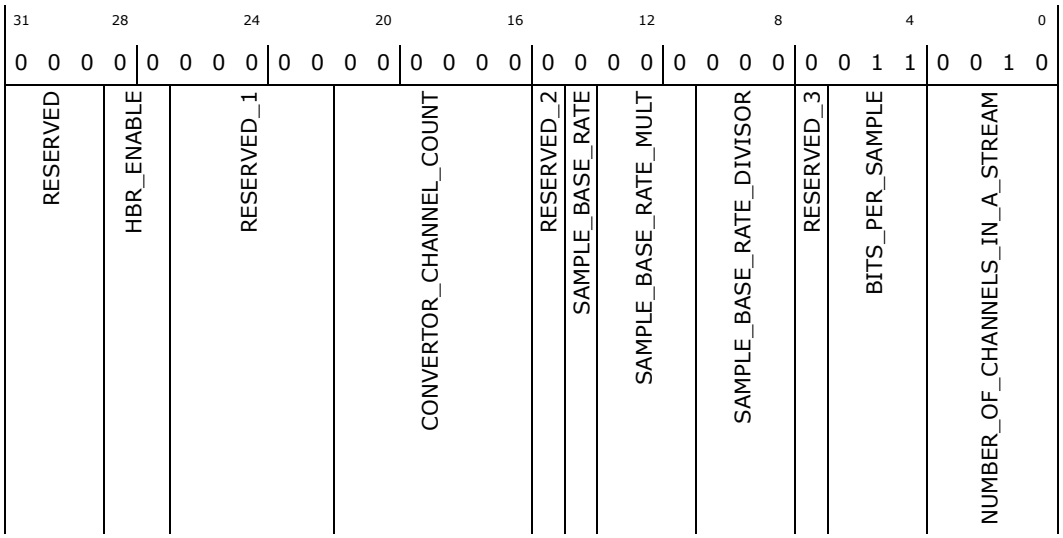
4.2.337 AUD_OUT_STR_DESC_A_DBG—Offset 62F08h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F08h

Default: 00000032h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Project: All Format: MBZ
28:27	0x0 WO	**HBR_ENABLE:** Project: All This reflects the current HBR settings
26:22	0x0 RO	**RESERVED_1:** Project: All Format: MBZ
21:16	0x0 WO	**CONVERTOR_CHANNEL_COUNT:** Project: All This reflects the Convertor Channel Count programmed through HDAudio.
15	0x0 RO	**RESERVED_2:** Project: All Format: MBZ
14	0x0 WO	**SAMPLE_BASE_RATE:** Project: All Default Value: ;0b (48 KHz) Sampling base rate of audio stream Value Name Description Project 0b 48 kHz 48 kHz All 1b 44.1 kHz 44.1 kHz All
13:11	0x0 WO	**SAMPLE_BASE_RATE_MULT:** Project: All Default Value: ;000b (48 KHz) Audio stream sample base rate multiple Value Name Description Project 000b 1x 48 kHz/44.1 kHz or less All 001b 2x x2 (96 kHz, 88.2 kHz, 32 kHz) All 010b 3x x3 (144 kHz) All 011b 4x x4 (192 kHz, 176.4 kHz) All 1XXb Reserved Reserved
10:8	0x0 WO	**SAMPLE_BASE_RATE_DIVISOR:** Project: All Default Value: ;000b (indicates divide by 1 which results in 48 KHz) Audio stream sample base rate divisor Value Name Description Project 000b Divide by 1 Divide by 1 (48 kHz, 44.1 kHz) All 001b Divide by 2 Divide by 2 (24 kHz, 22.05 kHz) All 010b Divide by 3 Divide by 3 (16 kHz, 32 kHz) All 011b Divide by 4 Divide by 4 (11.025 kHz) All 100b Divide by 5 Divide by 5 (9.6 kHz) All 101b Divide by 6 Divide by 6 (8 kHz) All 110b Divide by 7 Divide by 7 All 111b Divide by Divide by 8 (6 kHz) All
7	0x0 RO	**RESERVED_3:** Project: All Format: MBZ

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x3 WO	**BITS_PER_SAMPLE:** Project: All Default Value: ;011b (Indicates 24 bits) Audio stream sample base rate multiple Value Name Description Project 000b 8 bits The data will be packed in memory in 8 bit containers on 16 bit boundaries All 001b 16 bits The data will be packed in memory in 16 bit containers on 16 bit boundaries All 010b 24 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All 011b 32 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All 100b 20 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All Others Reserved Reserved
3:0	0x2 WO	**NUMBER_OF_CHANNELS_IN_A_STREAM:** Project: All Format: U4+1 Default Value: ;0010b (3 channels in each frame) Number of channels in each frame of the stream

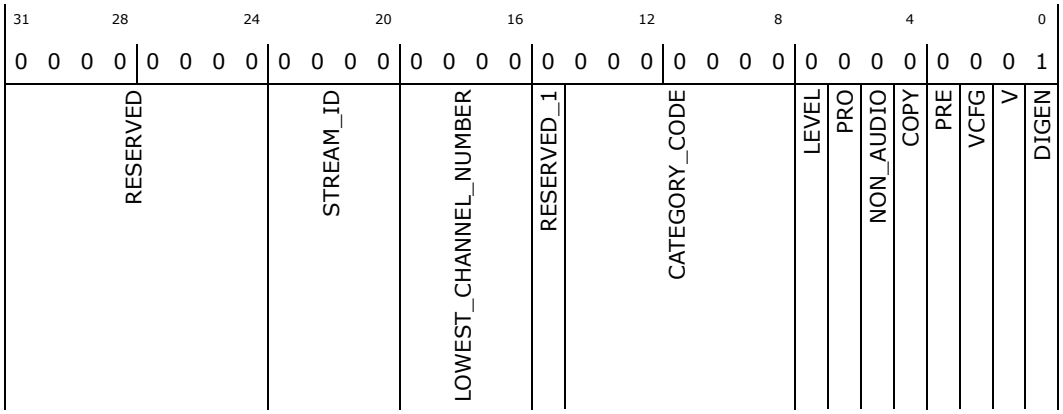
4.2.338 AUD_OUT_DIG_CNVT_A_DBG—Offset 62F0Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F0Ch

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:20	0x0 WO	**STREAM_ID:** Project: All Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 (stream 0)

Bit Range	Default & Access	Field Name (ID): Description
19:16	0x0 WO	**LOWEST_CHANNEL_NUMBER:** Project: All Represents the lowest channel used by the converter. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0
15	0x0 RO	**RESERVED_1:** Project: All Format: MBZ
14:8	0x0 WO	**CATEGORY_CODE:** Project: All S/PDIF IEC Category Code. This value is set in the Digital Converter 1 through the Set Audio Output Converter Widget command. Default = 0
7	0x0 WO	**LEVEL:** Project: All S/PDIF IEC Generation Level. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
6	0x0 WO	**PRO:** Project: All This bit indicates professional or consumer use of channel. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. This value can only be set to 1 if the Pro Allowed bit is set in the audio configuration register. Value Name Description Project 0b Consumer Consumer use. Default (Consumer) All 1b Professional Professional use All
5	0x0 WO	**NON_AUDIO:** Project: All Data is non PCM format. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b PCM Data is PCM (Default) All 1b Non-PCM Data is non PCM format All
4	0x0 WO	**COPY:** Project: All Copyright asserted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Not Asserted Copyright is not asserted All 1b Asserted Copyright is asserted All
3	0x0 WO	**PRE:** Project: All Filter preemphasis. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b None Pre-emphasis is non All 1b Enabled Filter pre-emphasis is enabled All
2	0x0 WO	**VCFG:** Project: All Validity Configuration. Determines S/PDIF transmitter behavior when data is not being transmitted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
1	0x0 WO	**V:** Project: All Affects the validity flag transmitted in each subframe, and enables the S/PDIF transmitter to maintain connection during error or mute conditions. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 WO	**DIGEN:** All Filter preemphasis. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Blocked Digital data is blocked from passing through the node, regardless of the state All 1b Passed Digital data can pass through the node (Default = 1, enabled) All

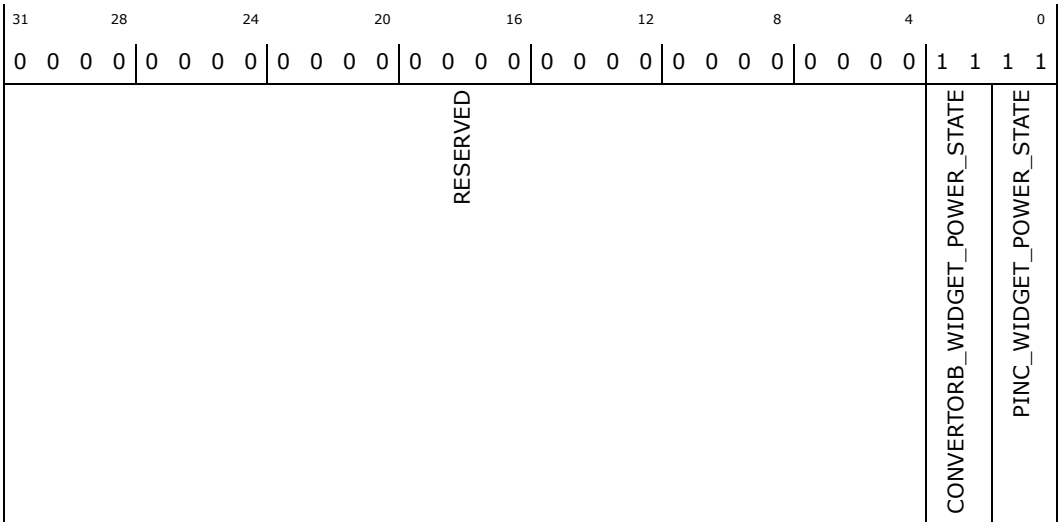
4.2.339 AUD_PWST2_DBG—Offset 62F14h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F14h

Default: 0000000Fh



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RESERVED:** Project: All Format: MBZ
3:2	0x3 WO	**CONVERTORB_WIDGET_POWER_STATE:** Project: All Default Value: ;11b D3 Power state that was requested by audio software Value Name Description Project 00b D0 D0 All 01b, 10b Unsupported Unsupported All 11b D3 D3 (Default)

Bit Range	Default & Access	Field Name (ID): Description
1:0	0x3 WO	**PINC_WIDGET_POWER_STATE:** Project: All Default Value: ;11b D3 Power state that was set Value Name Description Project 00b D0 D0 All 01b, 10b Unsupported Unsupported All 11b D3 D3 (Default)

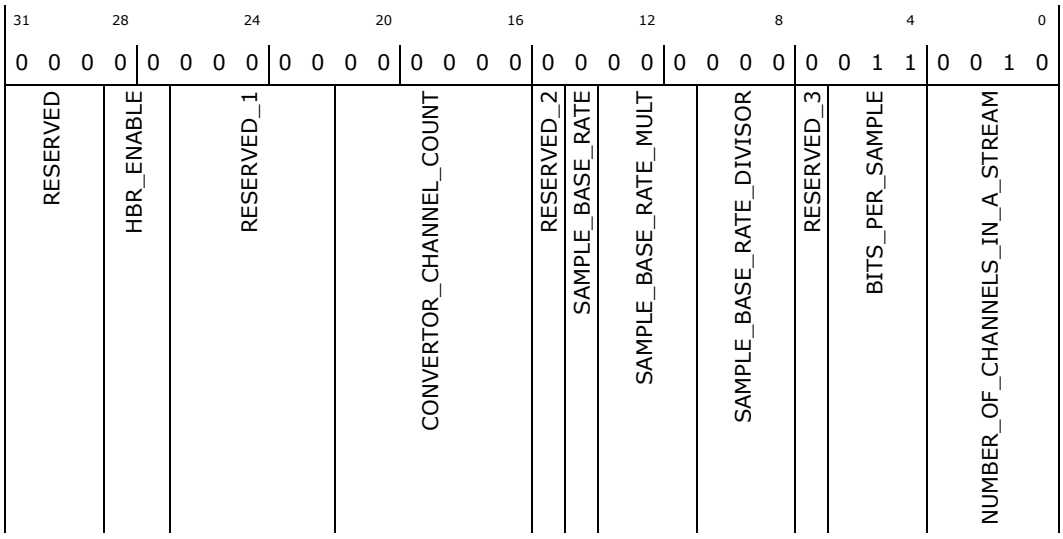
4.2.340 AUD_OUT_STR_DESC_B_DBG—Offset 62F18h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F18h

Default: 00000032h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Project: All Format: MBZ
28:27	0x0 WO	**HBR_ENABLE:** Project: All This reflects the current HBR settings
26:22	0x0 RO	**RESERVED_1:** Project: All Format: MBZ
21:16	0x0 WO	**CONVERTOR_CHANNEL_COUNT:** Project: All This reflects the Convertor Channel Count programmed through HDAudio.
15	0x0 RO	**RESERVED_2:** Project: All Format: MBZ

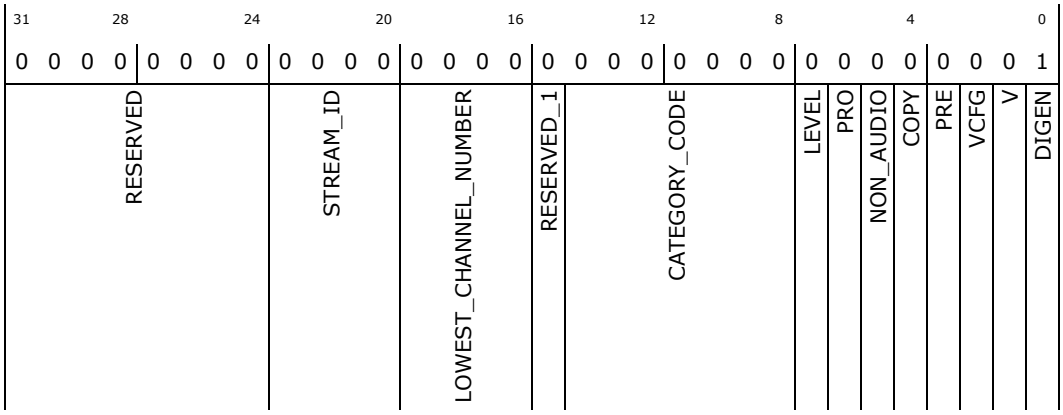
Bit Range	Default & Access	Field Name (ID): Description
14	0x0 WO	**SAMPLE_BASE_RATE:** Project: All Default Value: ;0b (48 KHz) Sampling base rate of audio stream Value Name Description Project 0b 48 kHz 48 kHz All 1b 44.1 kHz 44.1 kHz All
13:11	0x0 WO	**SAMPLE_BASE_RATE_MULT:** Project: All Default Value: ;000b (48 KHz) Audio stream sample base rate multiple Value Name Description Project 000b 1x 48 kHz/44.1 kHz or less All 001b 2x x2 (96 kHz, 88.2 kHz, 32 kHz) All 010b 3x x3 (144 kHz) All 011b 4x x4 (192 kHz, 176.4 kHz) All 1XXb Reserved Reserved
10:8	0x0 WO	**SAMPLE_BASE_RATE_DIVISOR:** Project: All Default Value: ;000b (indicates divide by 1 which results in 48 KHz) Audio stream sample base rate divisor Value Name Description Project 000b Divide by 1 Divide by 1 (48 kHz, 44.1 kHz) All 001b Divide by 2 Divide by 2 (24 kHz, 22.05 kHz) All 010b Divide by 3 Divide by 3 (16 kHz, 32 kHz) All 011b Divide by 4 Divide by 4 (11.025 kHz) All 100b Divide by 5 Divide by 5 (9.6 kHz) All 101b Divide by 6 Divide by 6 (8 kHz) All 110b Divide by 7 Divide by 7 All 111b Divide by Divide by 8 (6 kHz) All
7	0x0 RO	**RESERVED_3:** Project: All Format: MBZ
6:4	0x3 WO	**BITS_PER_SAMPLE:** Project: All Default Value: ;011b (Indicates 24 bits) Audio stream sample base rate multiple Value Name Description Project 000b 8 bits The data will be packed in memory in 8 bit containers on 16 bit boundaries All 001b 16 bits The data will be packed in memory in 16 bit containers on 16 bit boundaries All 010b 24 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All 011b 32 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All 100b 20 bits The data will be packed in memory in 32 bit containers on 32 bit boundaries All Others Reserved Reserved
3:0	0x2 WO	**NUMBER_OF_CHANNELS_IN_A_STREAM:** Project: All Format: U4+1 Default Value: ;0010b (3 channels in each frame) Number of channels in each frame of the stream

4.2.341 AUD_OUT_DIG_CNVT_B_DBG—Offset 62F1Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 62F1Ch

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:20	0x0 WO	**STREAM_ID:** Project: All Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0 (stream 0)
19:16	0x0 WO	**LOWEST_CHANNEL_NUMBER:** Project: All Represents the lowest channel used by the converter. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default = 0
15	0x0 RO	**RESERVED_1:** Project: All Format: MBZ
14:8	0x0 WO	**CATEGORY_CODE:** Project: All S/PDIF IEC Category Code. This value is set in the Digital Converter 1 through the Set Audio Output Converter Widget command. Default = 0
7	0x0 WO	**LEVEL:** Project: All S/PDIF IEC Generation Level. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
6	0x0 WO	**PRO:** Project: All This bit indicates professional or consumer use of channel. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. This value can only be set to 1 if the Pro Allowed bit is set in the audio configuration register. Value Name Description Project 0b Consumer Consumer use. Default (Consumer) All 1b Professional Professional use All

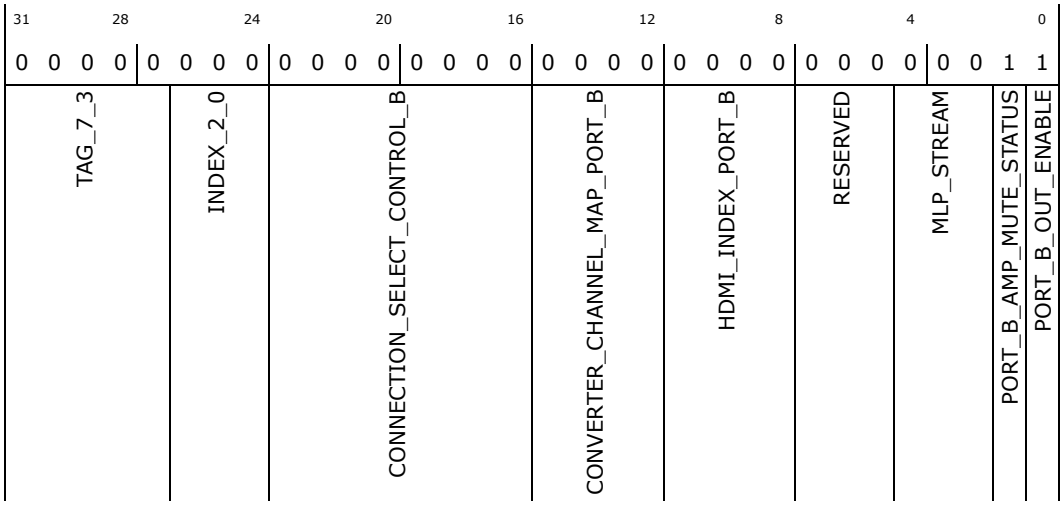
Bit Range	Default & Access	Field Name (ID): Description
5	0x0 WO	**NON_AUDIO:** Project: All Data is non PCM format. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b PCM Data is PCM (Default) All 1b Non-PCM Data is non PCM format All
4	0x0 WO	**COPY:** Project: All Copyright asserted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Not Asserted Copyright is not asserted All 1b Asserted Copyright is asserted All
3	0x0 WO	**PRE:** Project: All Filter preemphasis. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b None Pre-emphasis is non All 1b Enabled Filter pre-emphasis is enabled All
2	0x0 WO	**VCFG:** Project: All Validity Configuration. Determines S/PDIF transmitter behavior when data is not being transmitted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
1	0x0 WO	**V:** Project: All Affects the validity flag transmitted in each subframe, and enables the S/PDIF transmitter to maintain connection during error or mute conditions. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default = 0
0	0x1 WO	**DIGEN:** All Filter preemphasis. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Value Name Description Project 0b Blocked Digital data is blocked from passing through the node, regardless of the state All 1b Passed Digital data can pass through the node (Default = 1, enabled) All

4.2.342 AUD_PORT_EN_B_DBG—Offset 62F20h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 62F20h

Default: 00000003h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 WO	**TAG_7_3:** Project: All This represents the SSID that will go in the lower 5 bits of the SSID
26:24	0x0 WO	**INDEX_2_0:** Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
23:16	0x0 WO	**CONNECTION_SELECT_CONTROL_B:** Access Read Only Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
15:12	0x0 WO	**CONVERTER_CHANNEL_MAP_PORT_B:** Access Read Only Project: All The number in this field reflects the HD audio channel to which the HDMI channel is mapped. This field is read only
11:8	0x0 WO	**HDMI_INDEX_PORT_B:** Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
7:5	0x0 RO	**RESERVED:** Project: All Format: MBZ
4:2	0x0 WO	**MLP_STREAM:** Project: All Default Value: ;000b Default Value Name Description Project 000b Default Default All 011b MLP Stream MLP Stream All Others Reserved Reserved All
1	0x1 WO	**PORT_B_AMP_MUTE_STATUS:** Access Read Only Project: All Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b Amp not muted Amp not muted All 1b Amp muted Amp muted All

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 WO	**PORT_B_OUT_ENABLE:** All This bit reflects the state of the output path of the Pin Widget. When 0, audio is disabled . Default = 1

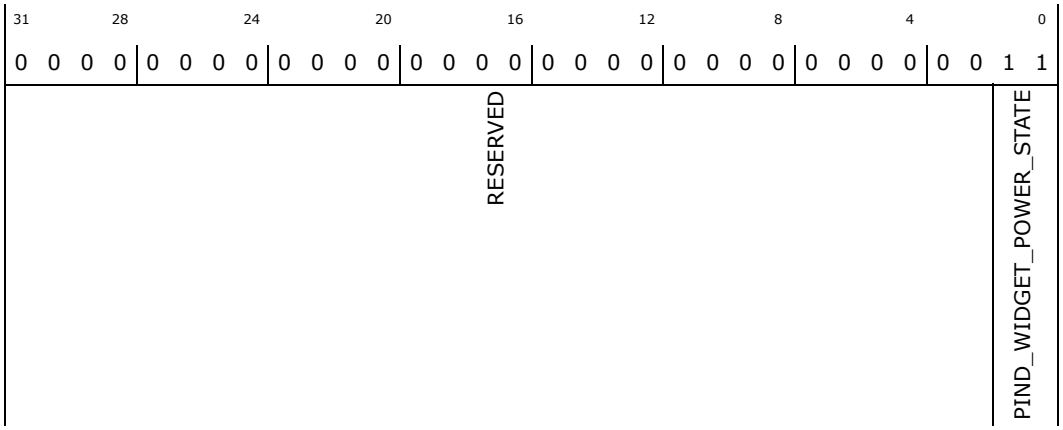
4.2.343 AUD_PWST3_DBG—Offset 62F24h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F24h

Default: 00000003h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**RESERVED:** Project: All Format: MBZ
1:0	0x3 WO	**PIND_WIDGET_POWER_STATE:** Project: All Default Value: ;11b D3 Power state that was set Value Name Description Project 00b D0 D0 All 01b, 10b Unsupported Unsupported All 11b D3 D3 (Default)

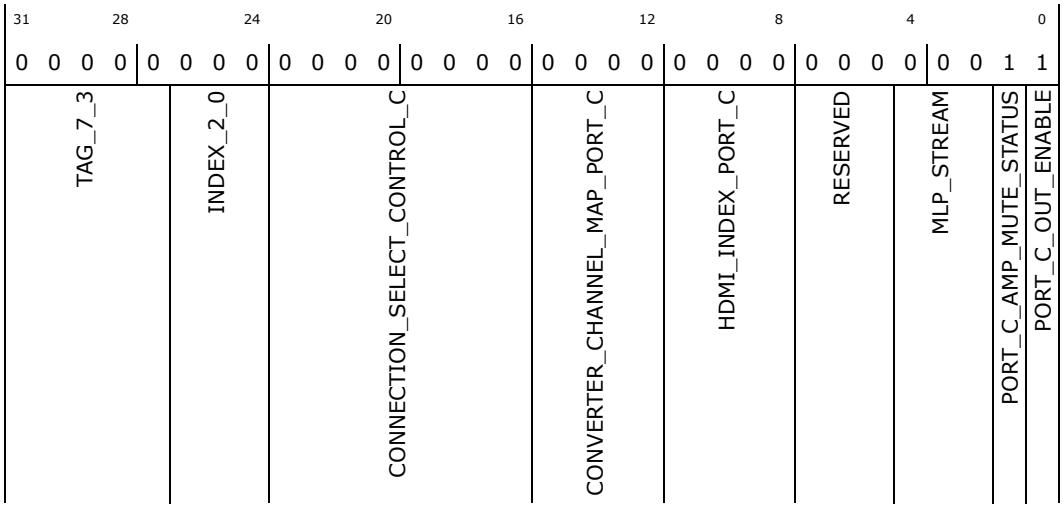
4.2.344 AUD_PORT_EN_C_DBG—Offset 62F28h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F28h

Default: 00000003h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 WO	**TAG_7_3:** Project: All This represents the SSID that will go in the lower 5 bits of the SSID
26:24	0x0 WO	**INDEX_2_0:** Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
23:16	0x0 WO	**CONNECTION_SELECT_CONTROL_C:** Access Read Only Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
15:12	0x0 WO	**CONVERTER_CHANNEL_MAP_PORT_C:** Access Read Only Project: All The number in this field reflects the HD audio channel to which the HDMI channel is mapped. This field is read only
11:8	0x0 WO	**HDMI_INDEX_PORT_C:** Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
7:5	0x0 RO	**RESERVED:** Project: All Format: MBZ
4:2	0x0 WO	**MLP_STREAM:** Project: All Default Value: ;000b Default Value Name Description Project 000b Default Default All 011b MLP Stream MLP Stream All Others Reserved Reserved All
1	0x1 WO	**PORT_C_AMP_MUTE_STATUS:** Access Read Only Project: All Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b Amp not muted Amp not muted All 1b Amp muted Amp muted All

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 WO	**PORT_C_OUT_ENABLE:** All This bit reflects the state of the output path of the Pin Widget. When 0, audio is disabled . Default = 1

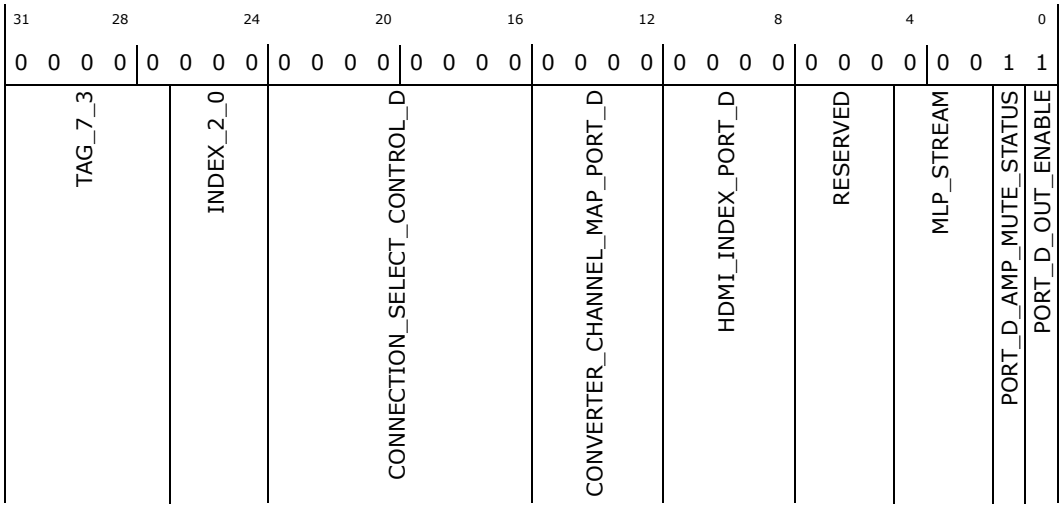
4.2.345 AUD_PORT_EN_D_DBG—Offset 62F2Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F2Ch

Default: 00000003h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 WO	**TAG_7_3:** Project: All This represents the SSID that will go in the lower 5 bits of the SSID
26:24	0x0 WO	**INDEX_2_0:** Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
23:16	0x0 WO	**CONNECTION_SELECT_CONTROL_D:** Access Read Only Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
15:12	0x0 WO	**CONVERTER_CHANNEL_MAP_PORT_D:** Access Read Only Project: All The number in this field reflects the HD audio channel to which the HDMI channel is mapped. This field is read only
11:8	0x0 WO	**HDMI_INDEX_PORT_D:** Project: All This is used as a pointer to program multiple SSID (only 0 is supported for Cantiga)
7:5	0x0 RO	**RESERVED:** Project: All Format: MBZ

Bit Range	Default & Access	Field Name (ID): Description
4:2	0x0 WO	**MLP_STREAM:** Project: All Default Value: ;000b Default Value Name Description Project 000b Default Default All 011b MLP Stream MLP Stream All Others Reserved Reserved All
1	0x1 WO	**PORT_D_AMP_MUTE_STATUS:** Access Read Only Project: All Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b Amp not muted Amp not muted All 1b Amp muted Amp muted All
0	0x1 WO	**PORT_D_OUT_ENABLE:** All This bit reflects the state of the output path of the Pin Widget. When 0, audio is disabled . Default = 1

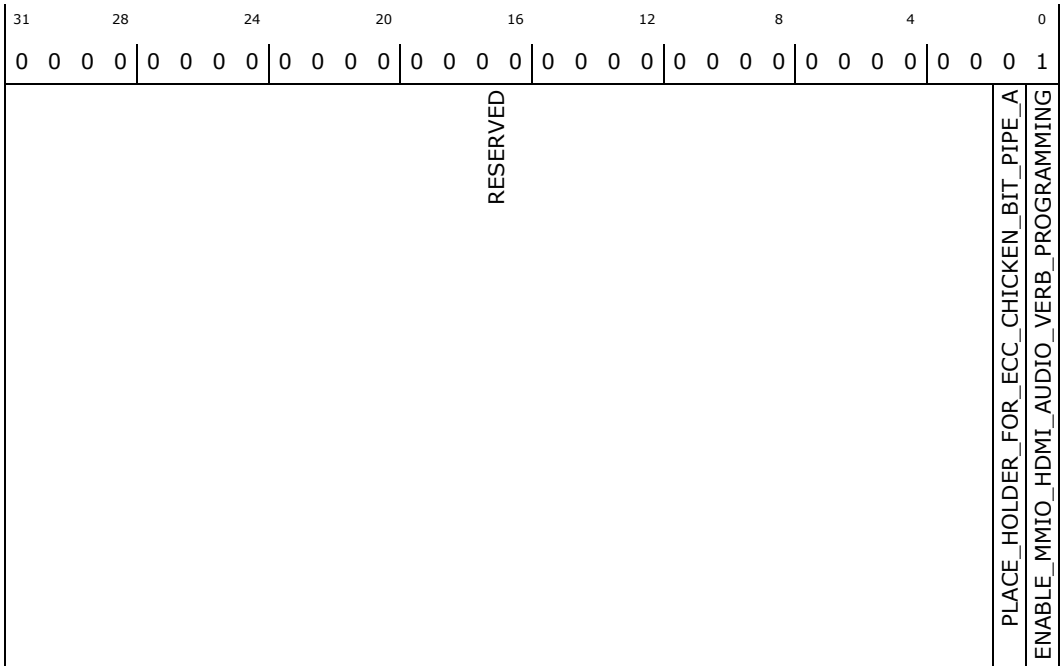
4.2.346 AUD_CHICKENBIT_REG—Offset 62F38h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F38h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**RESERVED:** Project: All Format: MBZ
1	0x0 WO	**PLACE_HOLDER_FOR_ECC_CHICKEN_BIT_PIPE_A:** Project: All audr_ecc_flip_chicken_bit
0	0x1 WO	**ENABLE_MMIO_HDMI_AUDIO_VERB_PROGRAMMING:** All Project: All Default Value: ;1b Amp muted This read-only bit reflects the mute status of the amplifier Value Name Description Project 0b HDAudio Programming through HDAudio Azalia All 1b MMIO Programming through MMIO Debug registers All

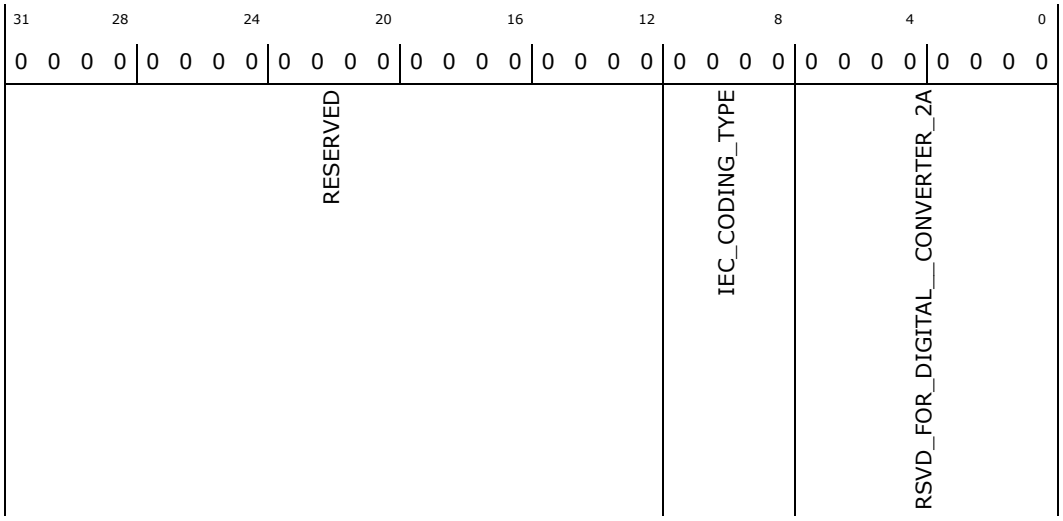
4.2.347 AUD_OUT_DIG_CNVTA_DBG—Offset 62F40h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F40h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RESERVED:** Project: All Format: MBZ
11:8	0x0 WO	**IEC_CODING_TYPE:** Project: All
7:0	0x0 WO	**RSVD_FOR_DIGITAL__CONVERTER_2A:** Project: All

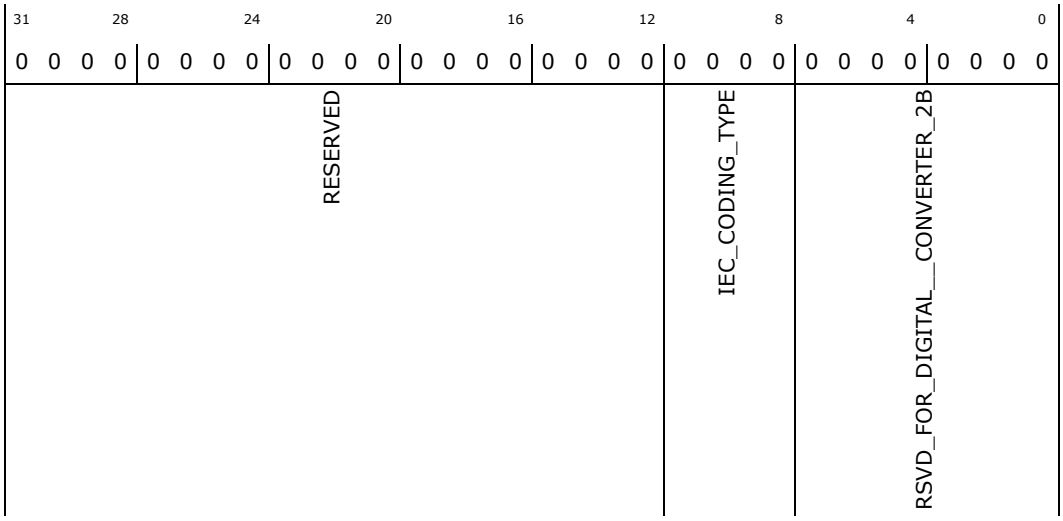
4.2.348 AUD_OUT_DIG_CNVTB_DBG—Offset 62F44h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F44h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RESERVED:** Project: All Format: MBZ
11:8	0x0 WO	**IEC_CODING_TYPE:** Project: All
7:0	0x0 WO	**RSVD_FOR_DIGITAL__CONVERTER_2B:** Project: All

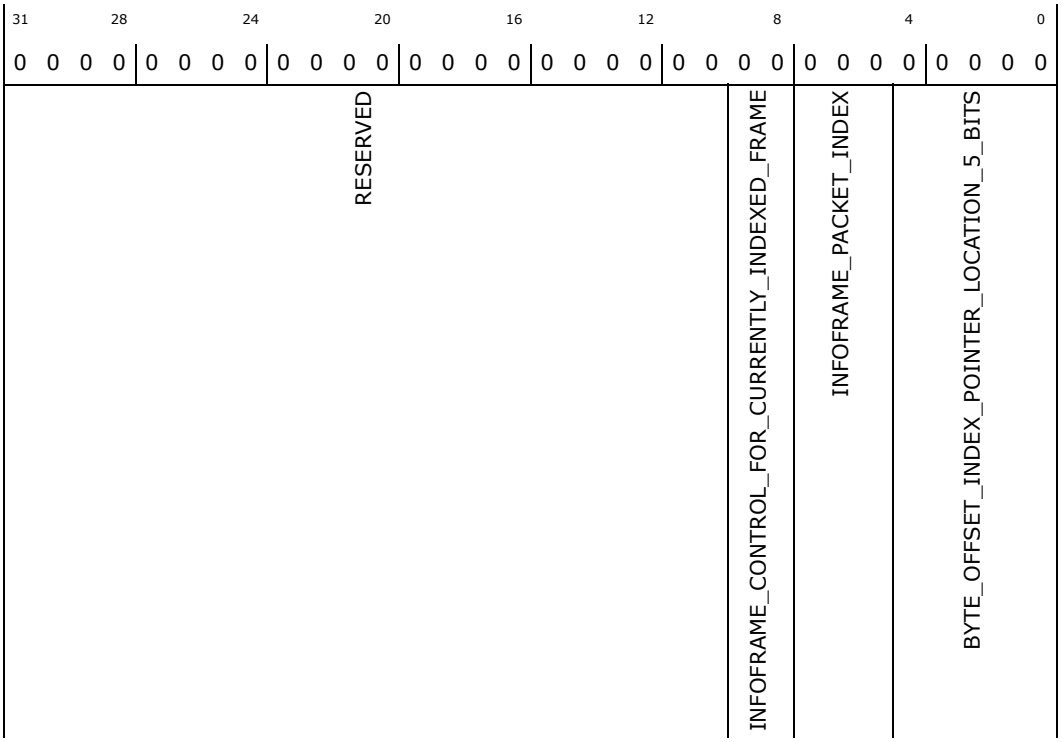
4.2.349 AUD_CNTL_ST_B_DBG—Offset 62F60h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F60h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**RESERVED:** Project: All Format: MBZ
9:8	0x0 WO	**INFOFRAME_CONTROL_FOR_CURRENTLY_INDEXED_FRAME:** Project: All Default Value: ;00b disable xmit Value Name Description Project 00b Disable xmit Disable xmit All 01b Reserved Reserved All 10b Xmit once Xmit once All 11b Best Effort Best Effort All
7:5	0x0 WO	**INFOFRAME_PACKET_INDEX:** Project: All Default Value: ;00b Audio Value Name Description Project 000b Audio Audio All 001b GP GP All 010b GP2 GP2 All 011b GP3 GP3 All 100b GP4 GP4 All Others Reserved Reserved All
4:0	0x0 WO	**BYTE_OFFSET_INDEX_POINTER_LOCATION_5_BITS:** Project: All

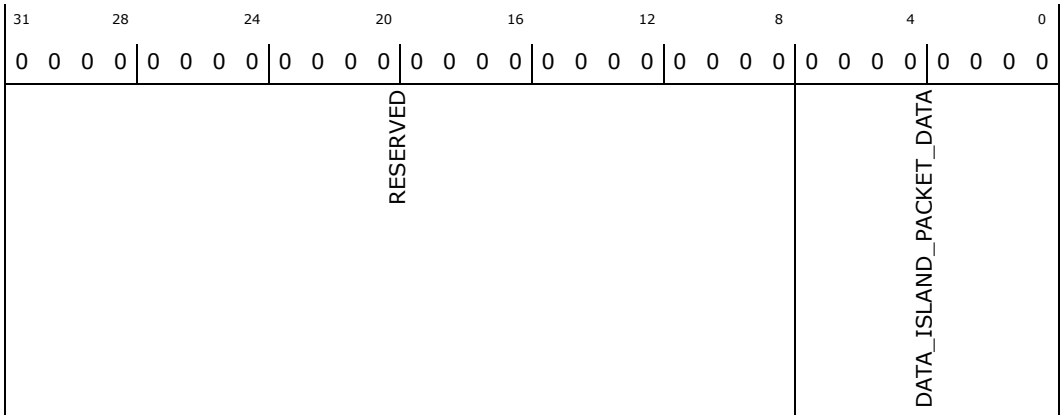
4.2.350 AUD_HDMIW_INFOFR_B_DBG—Offset 62F64h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F64h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED:** Project: All Format: MBZ
7:0	0x0 WO	**DATA_ISLAND_PACKET_DATA:** Project: All This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

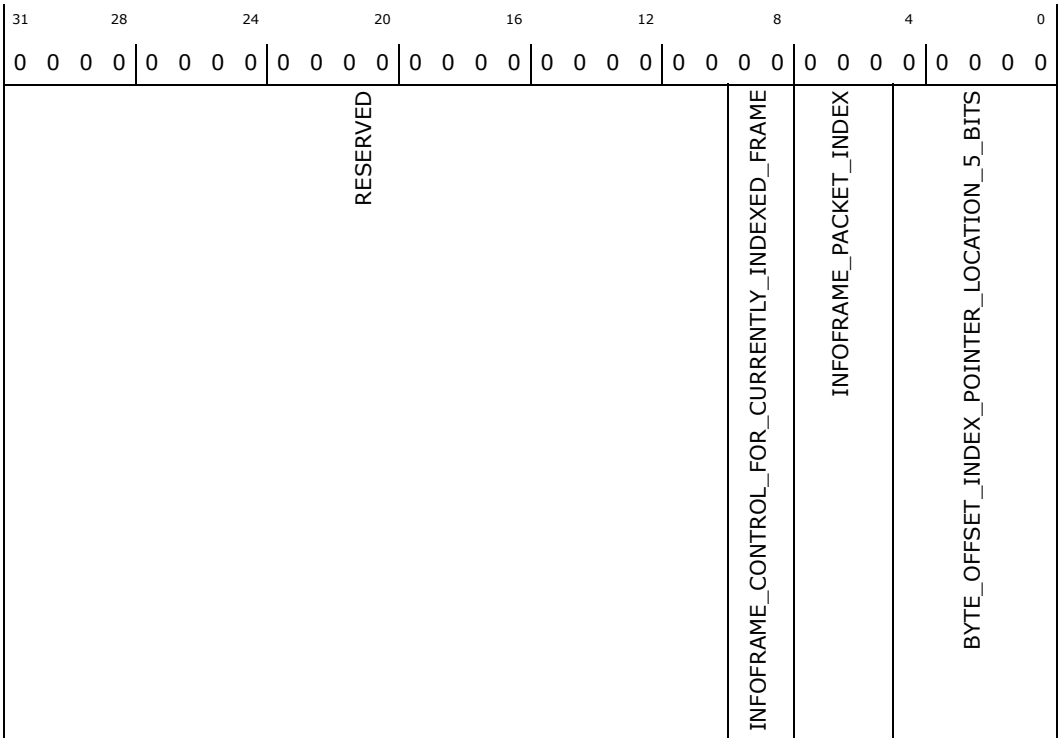
4.2.351 AUD_CNTL_ST_C_DBG—Offset 62F70h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F70h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**RESERVED:** Project: All Format: MBZ
9:8	0x0 WO	**INFOFRAME_CONTROL_FOR_CURRENTLY_INDEXED_FRAME:** Project: All Default Value: ;00b disable xmit Value Name Description Project 00b Disable xmit Disable xmit All 01b Reserved Reserved All 10b Xmit once Xmit once All 11b Best Effort Best Effort All
7:5	0x0 WO	**INFOFRAME_PACKET_INDEX:** Project: All Default Value: ;00b Audio Value Name Description Project 000b Audio Audio All 001b GP GP All 010b GP2 GP2 All 011b GP3 GP3 All 100b GP4 GP4 All Others Reserved Reserved All
4:0	0x0 WO	**BYTE_OFFSET_INDEX_POINTER_LOCATION_5_BITS:** Project: All

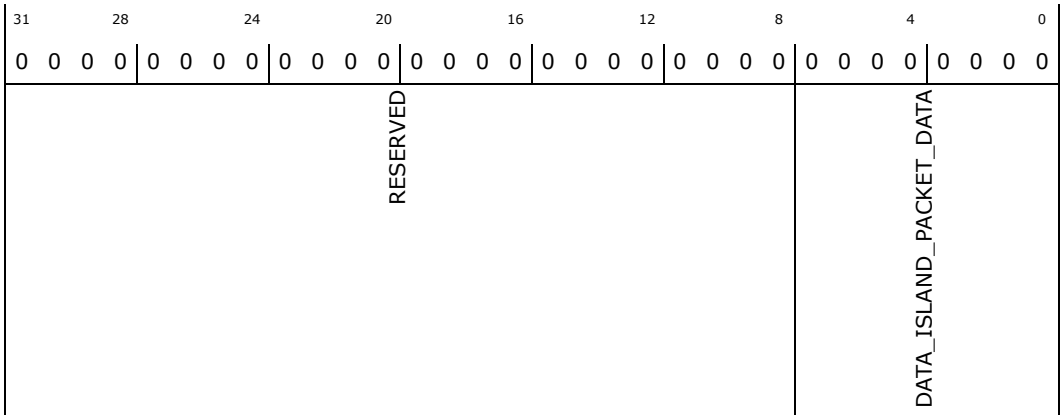
4.2.352 AUD_HDMIW_INFOFR_C_DBG—Offset 62F74h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F74h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**RESERVED:** Project: All Format: MBZ
7:0	0x0 WO	**DATA_ISLAND_PACKET_DATA:** Project: All This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

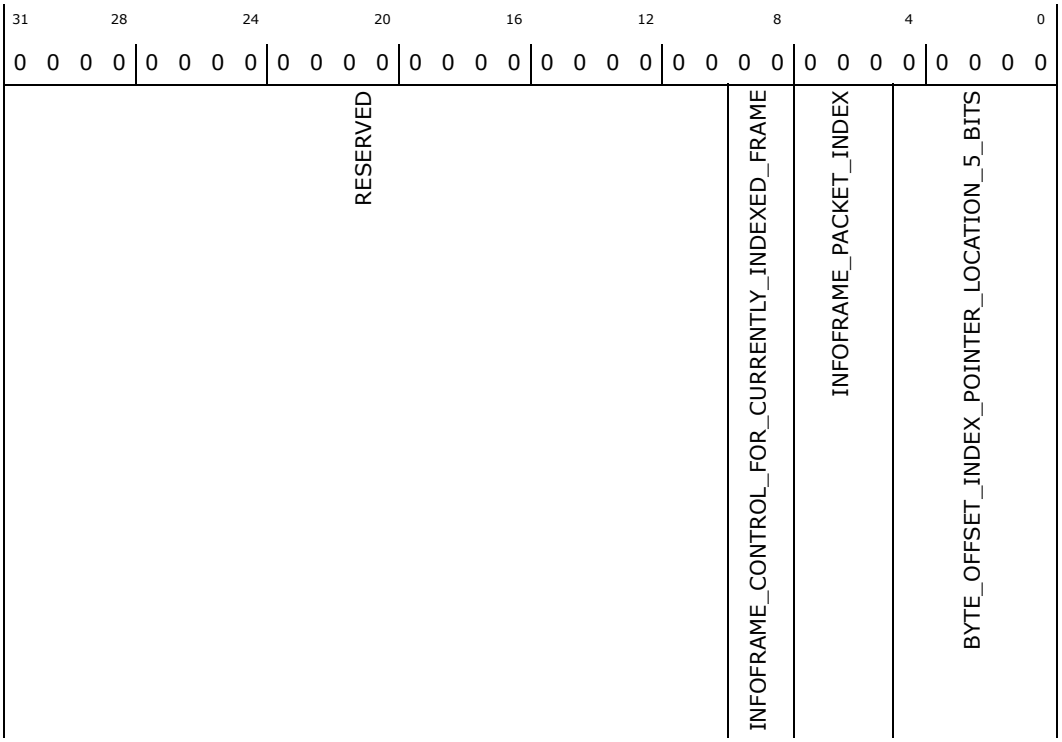
4.2.353 AUD_CNTL_ST_D_DBG—Offset 62F80h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F80h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**RESERVED:** Project: All Format: MBZ
9:8	0x0 WO	**INFOFRAME_CONTROL_FOR_CURRENTLY_INDEXED_FRAME:** Project: All Default Value: ;00b disable xmit Value Name Description Project 00b Disable xmit Disable xmit All 01b Reserved Reserved All 10b Xmit once Xmit once All 11b Best Effort Best Effort All
7:5	0x0 WO	**INFOFRAME_PACKET_INDEX:** Project: All Default Value: ;00b Audio Value Name Description Project 000b Audio Audio All 001b GP GP All 010b GP2 GP2 All 011b GP3 GP3 All 100b GP4 GP4 All Others Reserved Reserved All
4:0	0x0 WO	**BYTE_OFFSET_INDEX_POINTER_LOCATION_5_BITS:** Project: All

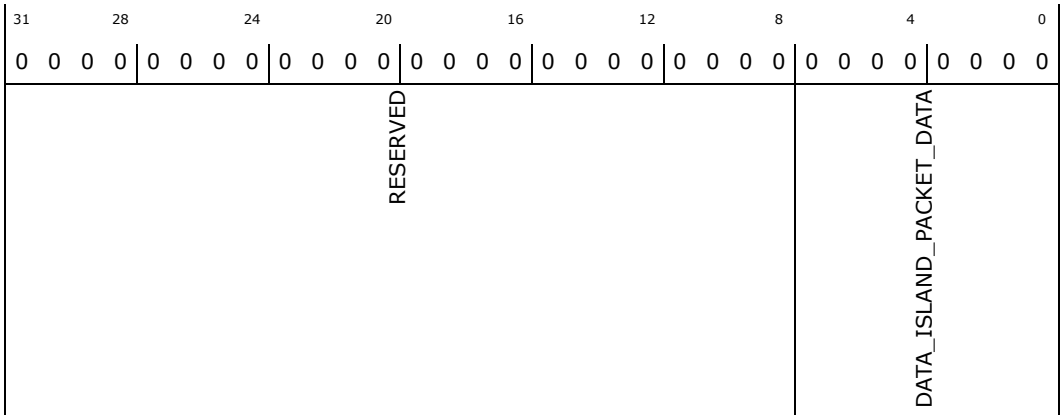
4.2.354 AUD_HDMIW_INFOFR_D_DBG—Offset 62F84h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F84h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED:** Project: All Format: MBZ
7:0	0x0 WO	**DATA_ISLAND_PACKET_DATA:** Project: All This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

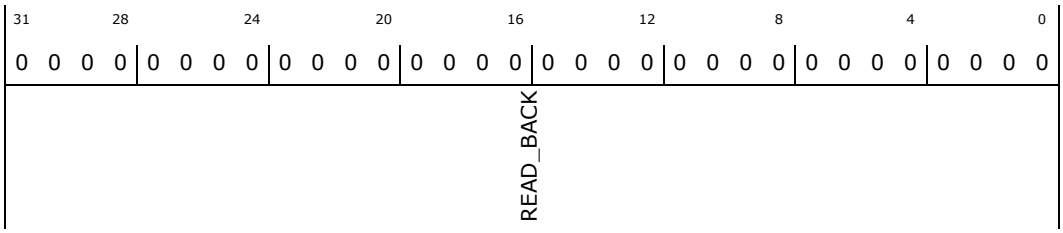
4.2.355 AUD_CONFIG_DEFAULT2_REG_PORTB—Offset 62F88h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F88h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 WO	**READ_BACK:** Project: All Config Default 2 values of port B rgars being written using the 738/739/73A/73B

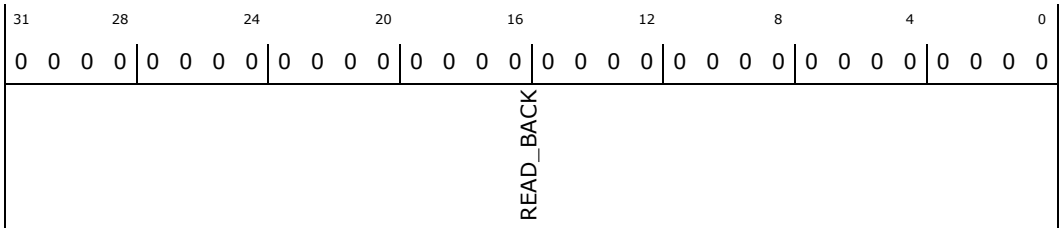
4.2.356 AUD_CONFIG_DEFAULT2_REG_PORTC—Offset 62F8Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F8Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 WO	**READ_BACK:** Project: All Config Default 2 values of port C rgars being written using the 738/739/73A/73B

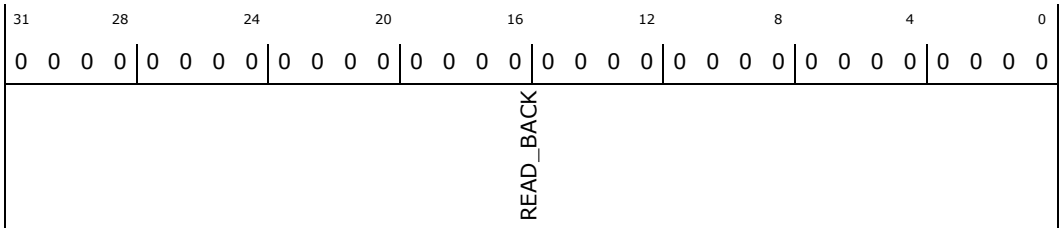
4.2.357 AUD_CONFIG_DEFAULT2_REG_PORTD—Offset 62F90h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F90h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 WO	**READ_BACK:** Project: All Config Default 2 values of port D rgars being written using the 738/739/73A/73B

4.2.358 AUD_MCTSA—Offset 62F94h

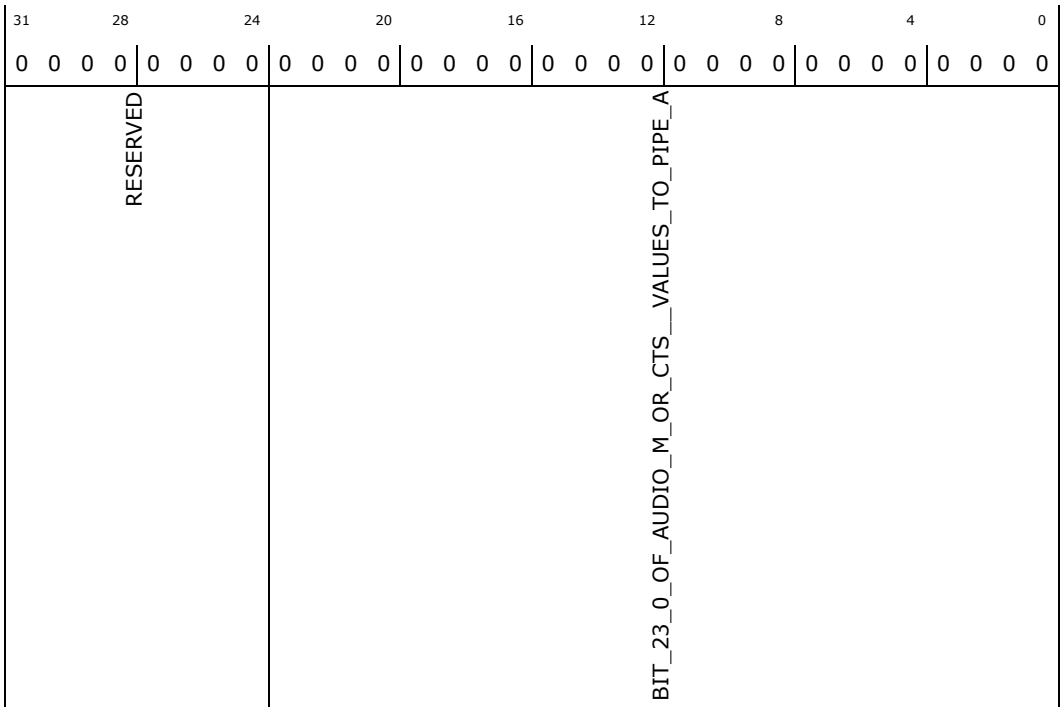
Audio M or CTS Pipe A Values Readback Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F94h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RO	**BIT_23_0_OF_AUDIO_M_OR_CTS__VALUES_TO_PIPE_A:** Project: All

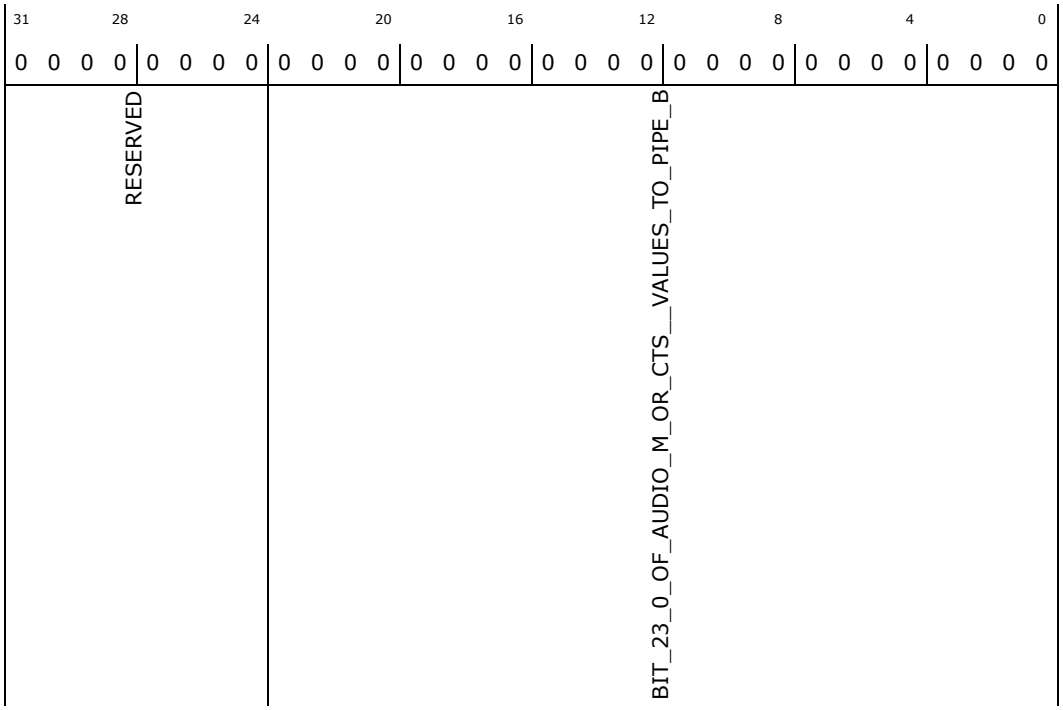
4.2.359 AUD_MCTSB—Offset 62F98h

Audio M or CTS Pipe B Values Readback Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 62F98h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RO	**BIT_23_0_OF_AUDIO_M_OR_CTS__VALUES_TO_PIPE_B:** Project: All

4.2.360 AUD_MCTSC—Offset 62F9Ch

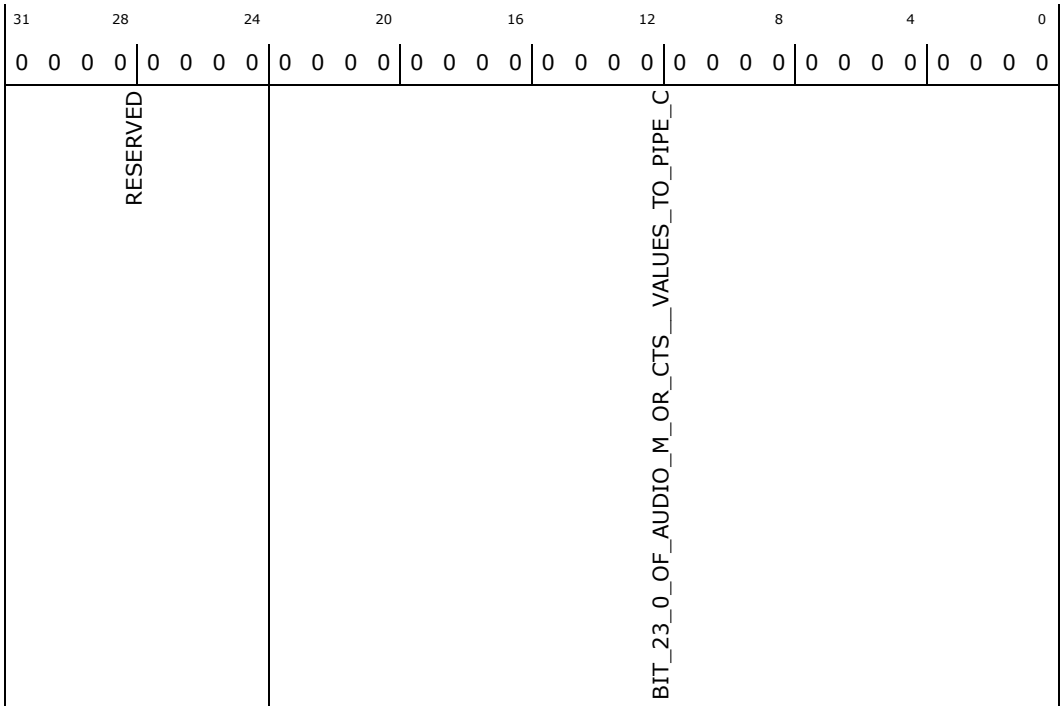
Audio M or CTS Pipe C Values Readback Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 62F9Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RO	**BIT_23_0_OF_AUDIO_M_OR_CTS__VALUES_TO_PIPE_C:** Project: All

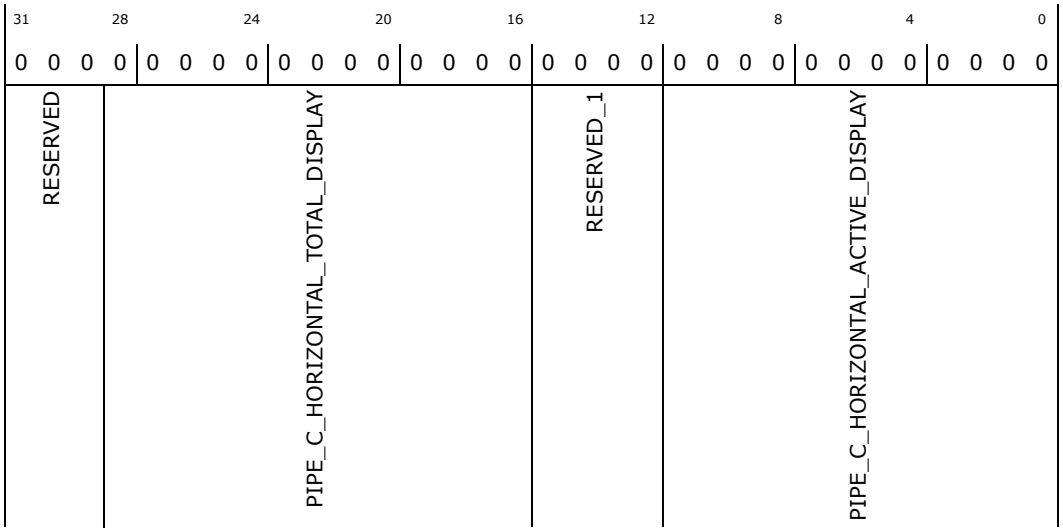
4.2.361 HTOTAL_C—Offset 63000h

Pipe C Horizontal Total Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63000h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Write as zero.
28:16	0x0 RW	**PIPE_C_HORIZONTAL_TOTAL_DISPLAY:** Refer pipe C description.
15:12	0x0 RO	**RESERVED_1:** Write as zero.
11:0	0x0 RW	**PIPE_C_HORIZONTAL_ACTIVE_DISPLAY:** Refer pipe A description

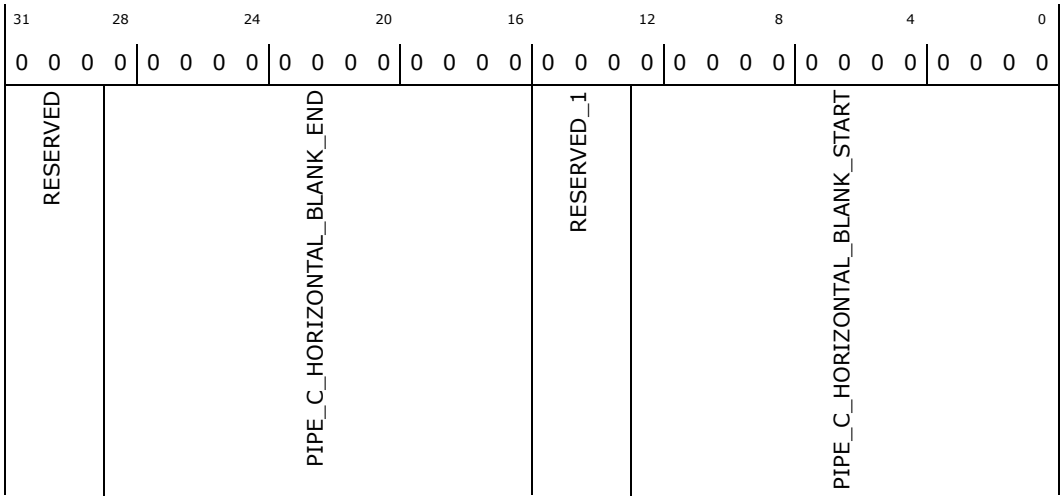
4.2.362 HBLANK_C—Offset 63004h

Pipe C Horizontal Blank Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63004h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** . Write as zero.
28:16	0x0 RW	**PIPE_C_HORIZONTAL_BLANK_END:** Refer pipe C description
15:13	0x0 RO	**RESERVED_1:** Write as zero.
12:0	0x0 RW	**PIPE_C_HORIZONTAL_BLANK_START:** Refer pipe C description.

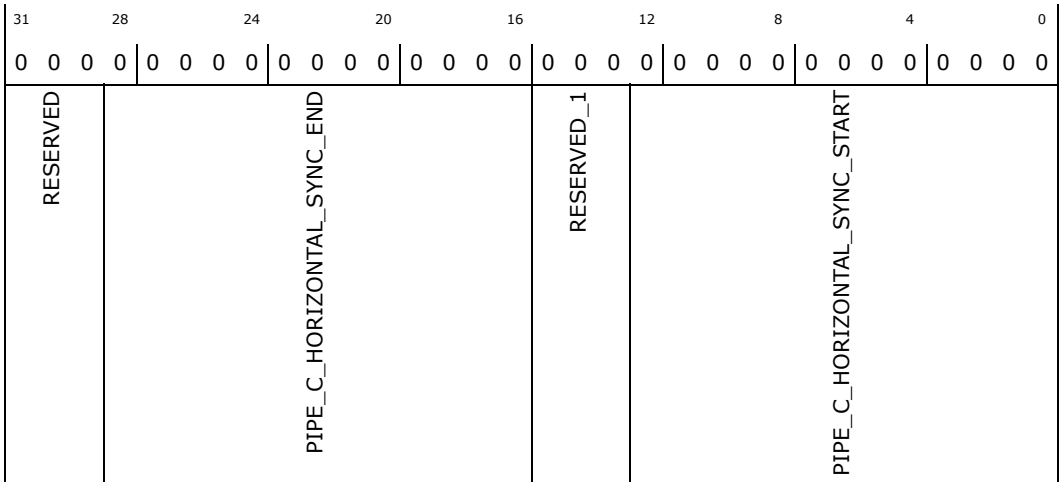
4.2.363 HSYNC_C—Offset 63008h

Pipe C Horizontal Sync Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63008h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Write as zero.
28:16	0x0 RW	**PIPE_C_HORIZONTAL_SYNC_END:** Refer pipe C description.
15:13	0x0 RO	**RESERVED_1:** Write as zero.
12:0	0x0 RW	**PIPE_C_HORIZONTAL_SYNC_START:** Refer pipe C description

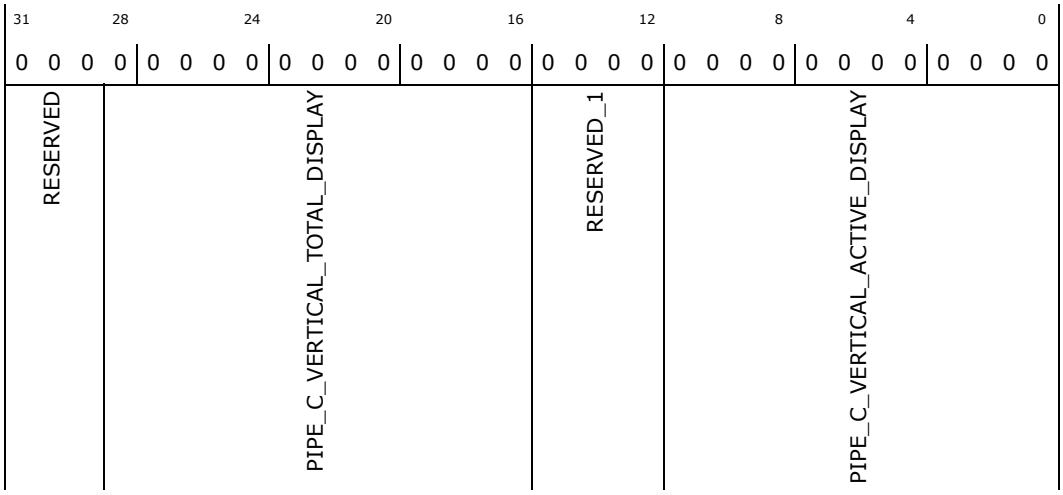
4.2.364 VTOTAL_C—Offset 6300Ch

Pipe C Vertical Total Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6300Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Write as zero.
28:16	0x0 RW	**PIPE_C_VERTICAL_TOTAL_DISPLAY:** Refer pipe A description.
15:12	0x0 RO	**RESERVED_1:** Write as zero.
11:0	0x0 RW	**PIPE_C_VERTICAL_ACTIVE_DISPLAY:** Refer pipe A description.

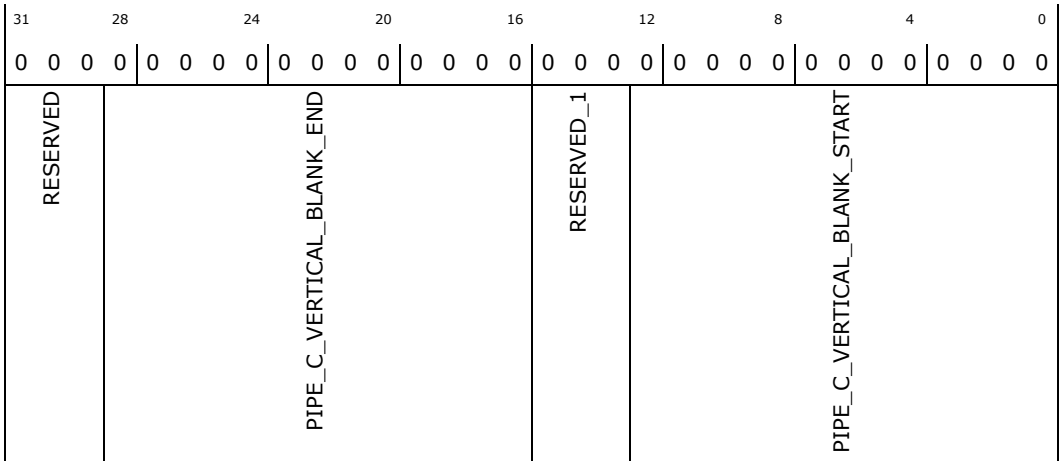
4.2.365 VBLANK_C—Offset 63010h

Pipe C Vertical Blank Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63010h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Write as zero.
28:16	0x0 RW	**PIPE_C_VERTICAL_BLANK_END:** Refer pipe A description.
15:13	0x0 RO	**RESERVED_1:** Write as zero.
12:0	0x0 RW	**PIPE_C_VERTICAL_BLANK_START:** Refer pipe A description.

4.2.366 VSYNC_C—Offset 63014h

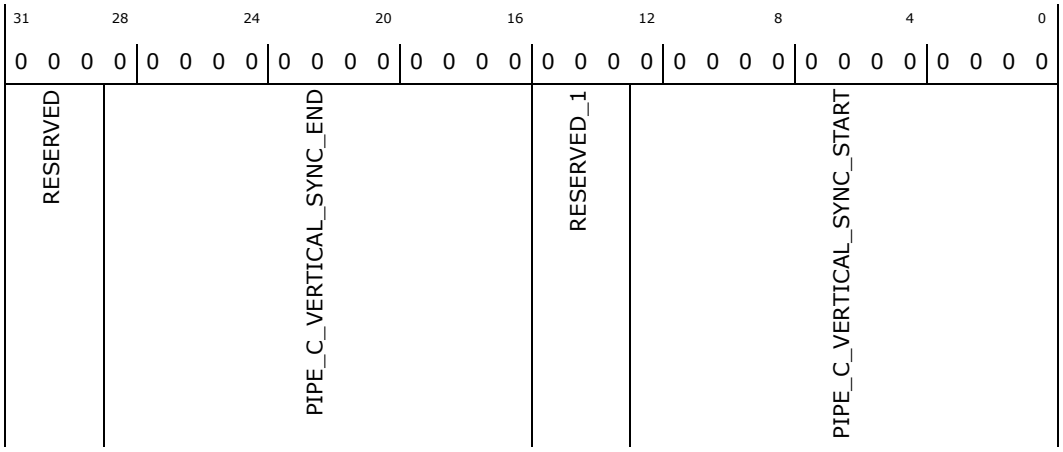
Pipe C Vertical Sync Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 63014h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** Write as zero.
28:16	0x0 RW	**PIPE_C_VERTICAL_SYNC_END:** Refer pipe A description.
15:13	0x0 RO	**RESERVED_1:** Write as zero.
12:0	0x0 RW	**PIPE_C_VERTICAL_SYNC_START:** Refer pipe A description.

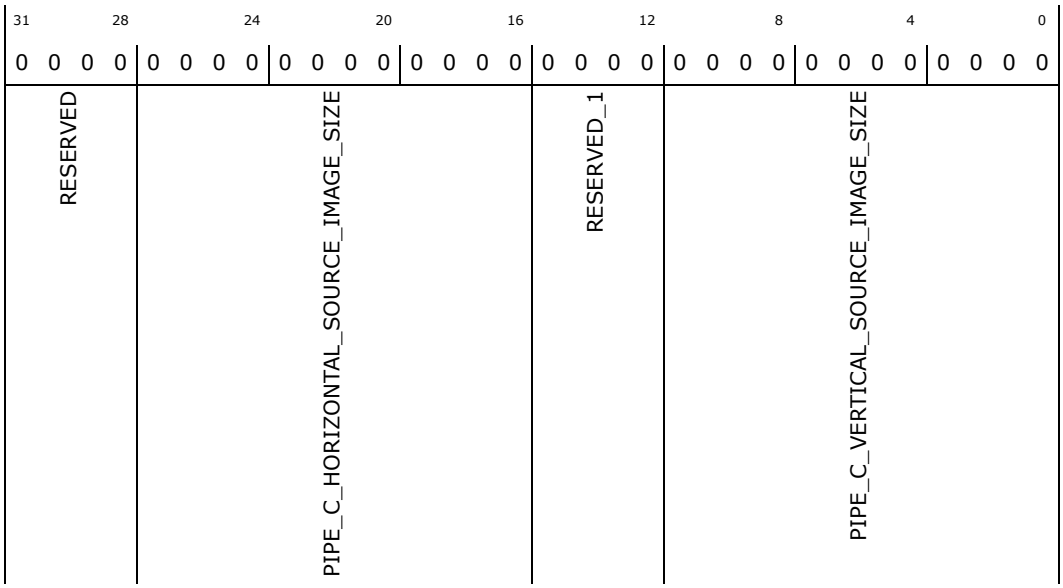
4.2.367 PIPECSRC—Offset 6301Ch

Pipe B Source Image Size

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6301Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**PIPE_C_HORIZONTAL_SOURCE_IMAGE_SIZE:** Refer pipe A description.
15:12	0x0 RO	**RESERVED_1:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
11:0	0x0 RW	**PIPE_C_VERTICAL_SOURCE_IMAGE_SIZE:** Refer pipe A description.

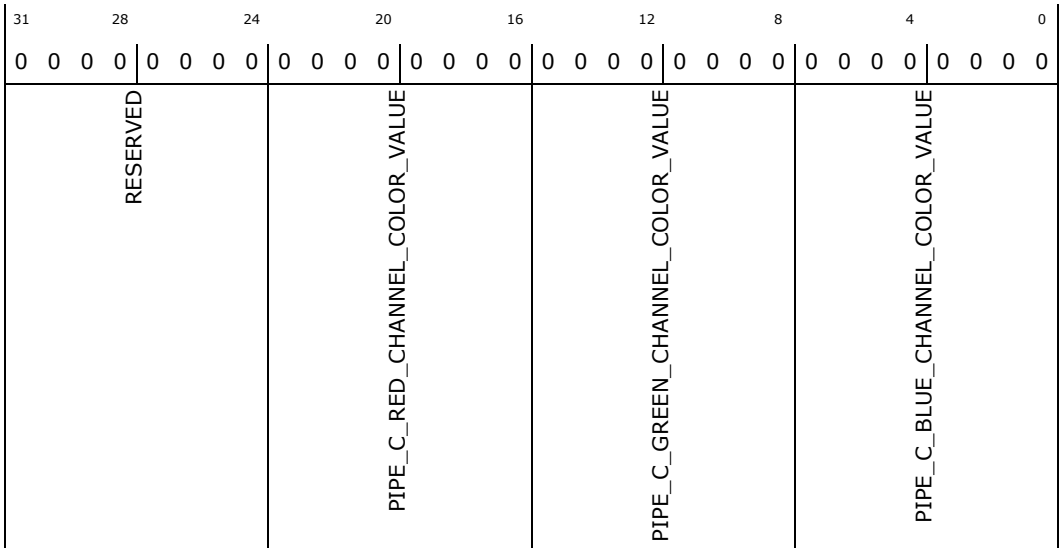
4.2.368 BCLRPAT_C—Offset 63020h

Pipe C Border Color Pattern Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63020h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:16	0x0 RW	**PIPE_C_RED_CHANNEL_COLOR_VALUE:** Reserved.
15:8	0x0 RW	**PIPE_C_GREEN_CHANNEL_COLOR_VALUE:** Reserved.
7:0	0x0 RW	**PIPE_C_BLUE_CHANNEL_COLOR_VALUE:** Reserved.

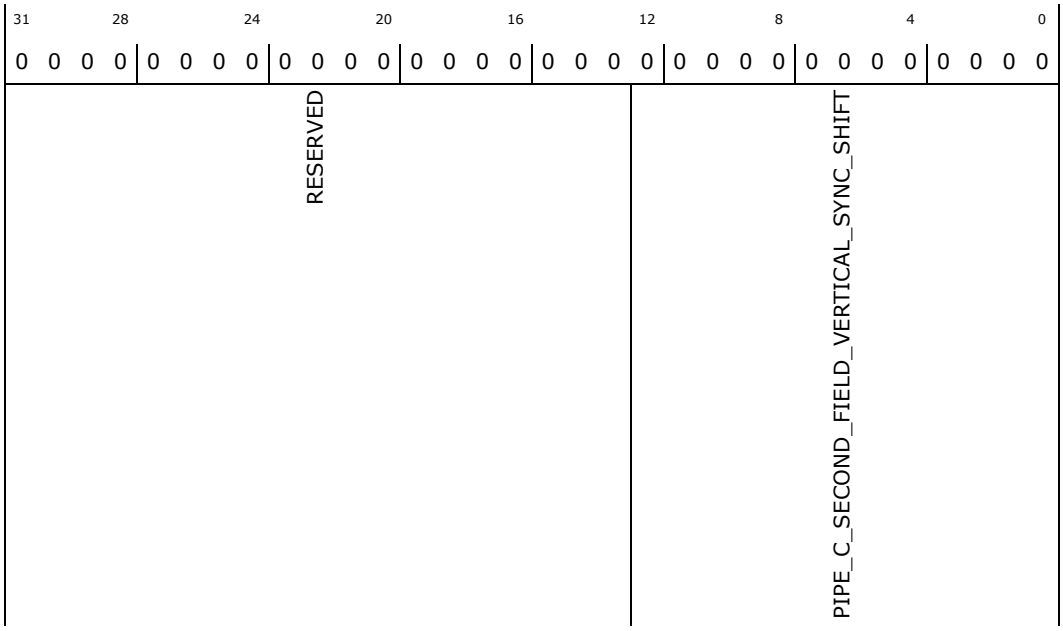
4.2.369 VSYNCSHIFT_C—Offset 63028h

Vertical Sync Shift Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63028h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RESERVED:** Write as zero.
12:0	0x0 RW	**PIPE_C_SECOND_FIELD_VERTICAL_SYNC_SHIFT:** This value specifies the vertical sync alignment for the start of the interlaced second field expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the PIPEBCONF is programmed to an interlaced mode using vsync shift. Otherwise a legacy value of floor[htotal / 2] will be used. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed to: (horizontal sync start - floor[horizontal total / 2]) (use the actual horizontal sync start and horizontal total values and not the minus one values programmed into registers). This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.

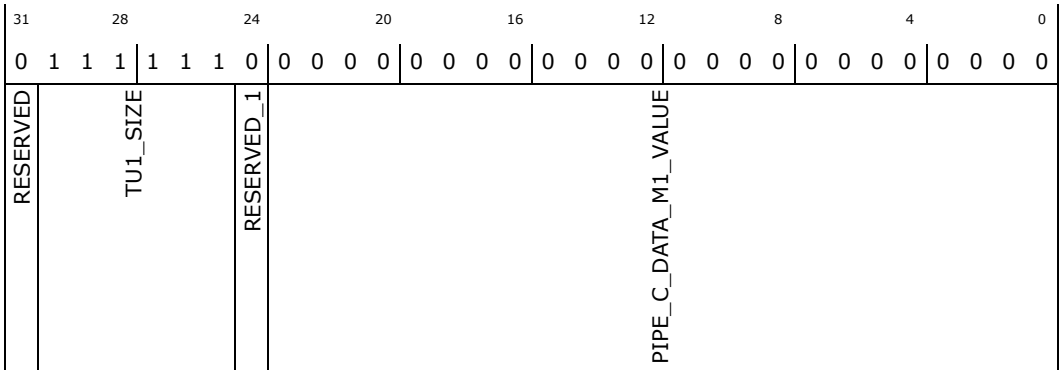
4.2.370 TRANSCDATAM1—Offset 63030h

Pipe B Data M value 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63030h

Default: 7E000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** Project: All Format: MBZ
30:25	0x3f RW	**TU1_SIZE:** Project: All Default Value: ;111111b 64 Refer Pipe A description.
24	0x0 RO	**RESERVED_1:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_C_DATA_M1_VALUE:** Project: All Refer Pipe A description.

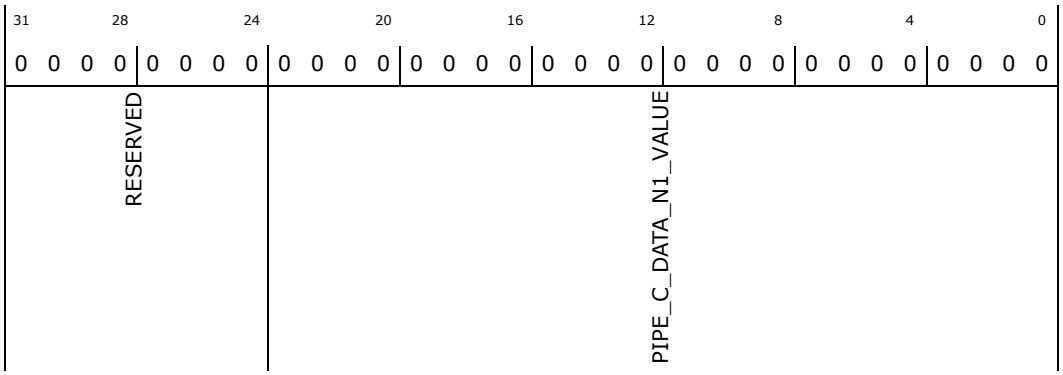
4.2.371 TRANSCDATAN1—Offset 63034h

Pipe C Data N value 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63034h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_C_DATA_N1_VALUE:** Project: All Refer Pipe A description.

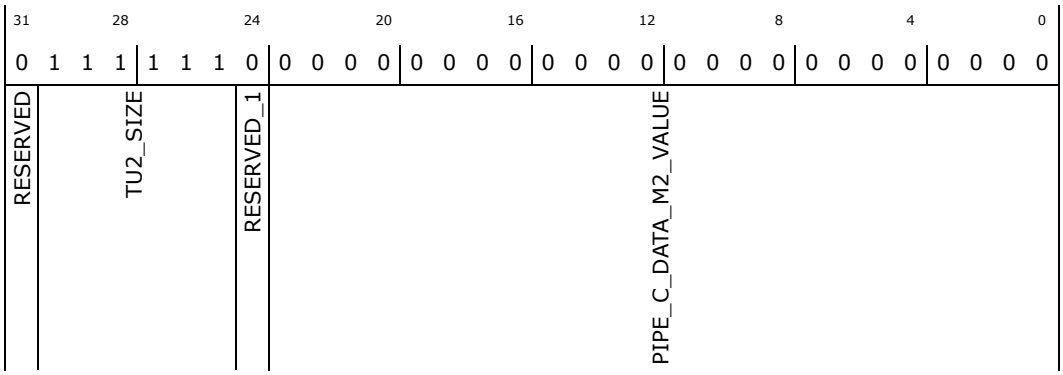
4.2.372 TRANSCDATAM2—Offset 63038h

Pipe C Data M value 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63038h

Default: 7E000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** Project: All Format: MBZ
30:25	0x3f RW	**TU2_SIZE:** Project: All Default Value: ;111111b 64 Refer Pipe A description.
24	0x0 RO	**RESERVED_1:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_C_DATA_M2_VALUE:** Project: All Refer Pipe A description.

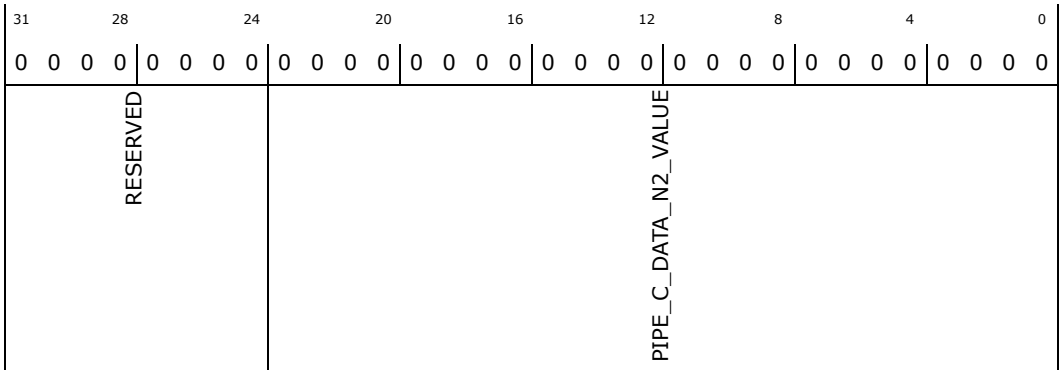
4.2.373 TRANSCDATAN2—Offset 6303Ch

Pipe C Data N value 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6303Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_C_DATA_N2_VALUE:** Project: All Refer Pipe A description.

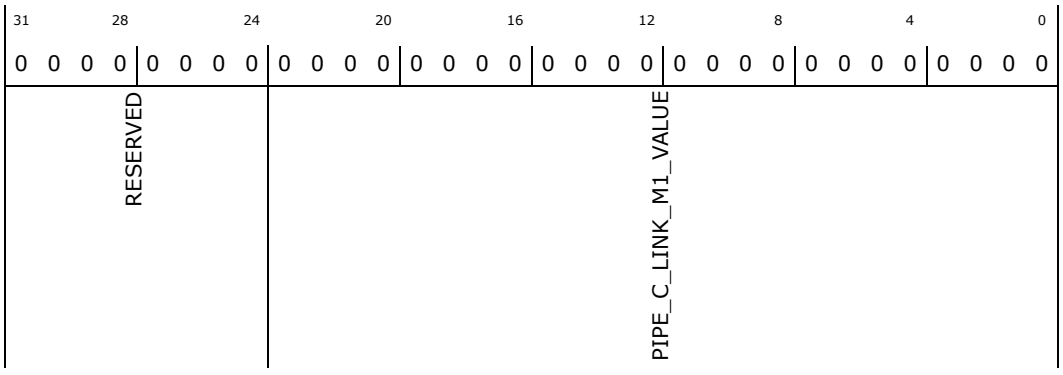
4.2.374 TRANSCDPLINKM1—Offset 63040h

Pipe B Link M value 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63040h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_C_LINK_M1_VALUE:** Project: All Refer Pipe A description.

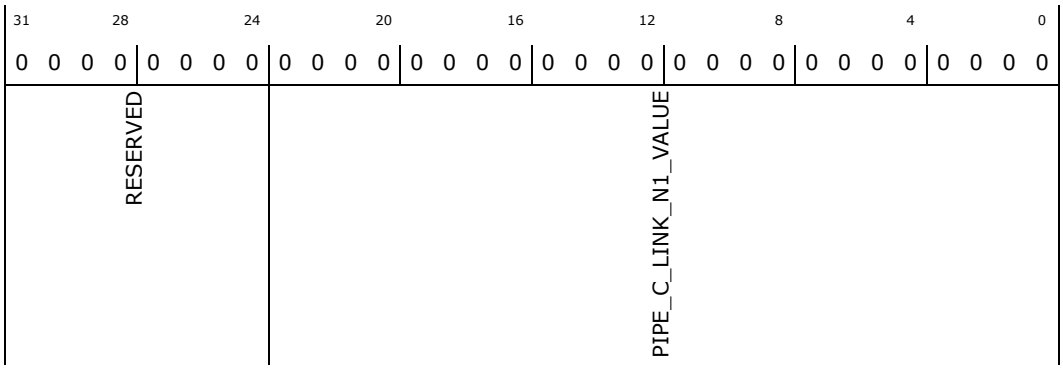
4.2.375 TRANSCDPLINKN1—Offset 63044h

Pipe C Link N value 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63044h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_C_LINK_N1_VALUE:** Project: All Refer Pipe A description.

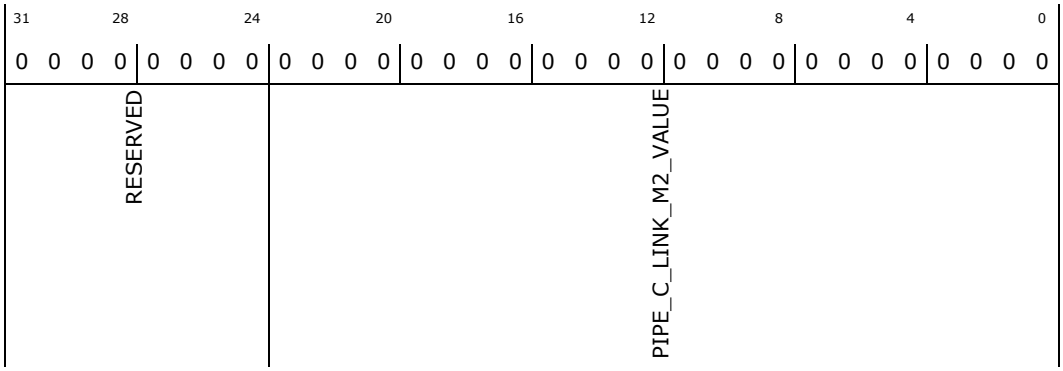
4.2.376 TRANSCDPLINKM2—Offset 63048h

Pipe C Link M value 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63048h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_C_LINK_M2_VALUE:** Project: All Refer Pipe A description.

4.2.377 TRANSCDPLINKN2—Offset 6304Ch

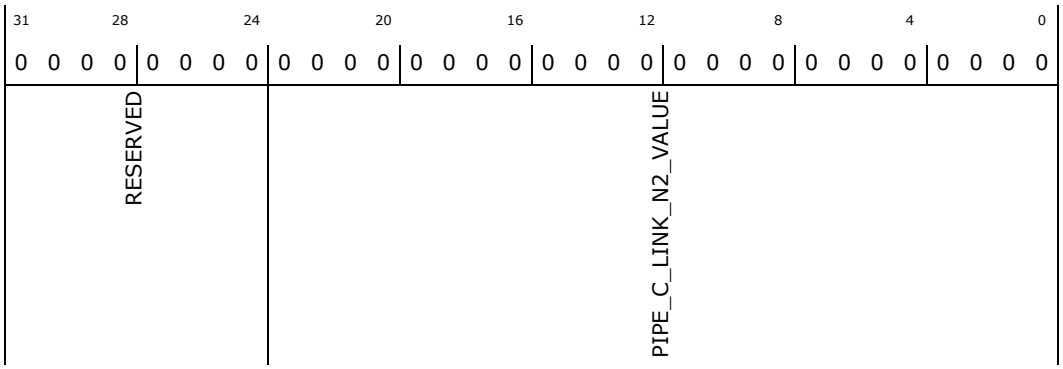
Pipe C Link N value 2

Access Method

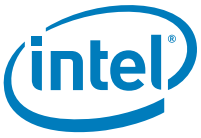
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6304Ch

Default: 00000000h



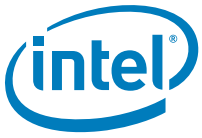
Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Project: All Format: MBZ
23:0	0x0 RW	**PIPE_C_LINK_N2_VALUE:** Project: All Refer Pipe A description.



4.3 DEFAULT Address Map

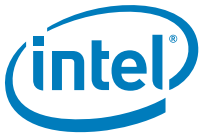
Table 23. Summary of Memory Mapped I/O Registers—

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
63050–63053h	4	"CRCCTRLREDC—Offset 63050h" on page 532	00000000h
63054–63057h	4	"CRCCTRLGREENC—Offset 63054h" on page 533	00000000h
63058–6305Bh	4	"CRCCTRLBLUEC—Offset 63058h" on page 533	00000000h
6305C–6305Fh	4	"CRCCTRLALPHAC—Offset 6305Ch" on page 534	00000000h
63060–63063h	4	"CRCRESREDC—Offset 63060h" on page 535	00000000h
63064–63067h	4	"CRCRESGREENC—Offset 63064h" on page 535	00000000h
63068–6306Bh	4	"CRCRESBLUEC—Offset 63068h" on page 536	00000000h
6306C–6306Fh	4	"CRCRESALPHAC—Offset 6306Ch" on page 537	00000000h
63070–63073h	4	"CRCCTRLRESIDUE2C—Offset 63070h" on page 538	00000000h
63080–63083h	4	"CRCRESRESIDUAL2C—Offset 63080h" on page 539	00000000h
63090–63093h	4	"PSRCTLC—Offset 63090h" on page 539	00000000h
63094–63097h	4	"PSRSTATC—Offset 63094h" on page 541	00000000h
63098–6309Bh	4	"PSRCRC1C—Offset 63098h" on page 542	00000000h
6309C–6309Fh	4	"PSRCRC2C—Offset 6309Ch" on page 543	00000000h
630A0–630A3h	4	"VSCSDPC—Offset 630A0h" on page 544	00000000h
630B0–630B3h	4	"PIPECWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS—Offset 630B0h" on page 545	00000000h
630B4–630B7h	4	"PIPECWIDEGAMUTCOLORCORRECTIONC02COEFFICIENT—Offset 630B4h" on page 546	00000000h
630B8–630BBh	4	"PIPECWIDEGAMUTCOLORCORRECTIONC11_C10COEFFICIENTS—Offset 630B8h" on page 546	00000000h
630BC–630BFh	4	"PIPECWIDEGAMUTCOLORCORRECTIONC12COEFFICIENT—Offset 630BCh" on page 547	00000000h
630C0–630C3h	4	"PIPECWIDEGAMUTCOLORCORRECTIONC21_C20COEFFICIENTS—Offset 630C0h" on page 547	00000000h
630C4–630C7h	4	"PIPECWIDEGAMUTCOLORCORRECTIONC22COEFFICIENT—Offset 630C4h" on page 548	00000000h
63A04–63A07h	4	"CANVAS_C—Offset 63A04h" on page 549	00000000h
63A08–63A0Bh	4	"PRIMPOS_C—Offset 63A08h" on page 549	00000000h
63A0C–63A0Fh	4	"PRIMSIZE_C—Offset 63A0Ch" on page 550	00000000h
63A10–63A13h	4	"PRIMC_CONSTANT—Offset 63A10h" on page 551	00000000h
64100–64103h	4	"DP_B—Offset 64100h" on page 552	00000018h
64110–64113h	4	"DPB_AUX_CH_CTL—Offset 64110h" on page 554	00050000h
64114–64117h	4	"DPB_AUX_CH_DATA1—Offset 64114h" on page 556	00000000h
64118–6411Bh	4	"DPB_AUX_CH_DATA2—Offset 64118h" on page 557	00000000h
6411C–6411Fh	4	"DPB_AUX_CH_DATA3—Offset 6411Ch" on page 558	00000000h



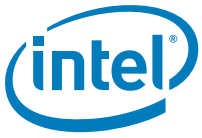
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
64120–64123h	4	"DPB_AUX_CH_DATA4—Offset 64120h" on page 558	00000000h
64124–64127h	4	"DPB_AUX_CH_DATA5—Offset 64124h" on page 559	00000000h
64130–64133h	4	"DP_AUX_CH_AKSV_HI—Offset 64130h" on page 559	00000000h
64134–64137h	4	"DP_AUX_CH_AKSV_LO—Offset 64134h" on page 560	00000000h
64150–64153h	4	"DPB_AUX_TST—Offset 64150h" on page 560	00000000h
64200–64203h	4	"DP_C—Offset 64200h" on page 563	00000018h
64210–64213h	4	"DPC_AUX_CH_CTL—Offset 64210h" on page 566	00050000h
64214–64217h	4	"DPC_AUX_CH_DATA1—Offset 64214h" on page 568	00000000h
64218–6421Bh	4	"DPC_AUX_CH_DATA2—Offset 64218h" on page 569	00000000h
6421C–6421Fh	4	"DPC_AUX_CH_DATA3—Offset 6421Ch" on page 569	00000000h
64220–64223h	4	"DPC_AUX_CH_DATA4—Offset 64220h" on page 570	00000000h
64224–64227h	4	"DPC_AUX_CH_DATA5—Offset 64224h" on page 570	00000000h
64228–6422Bh	4	"DPC_AUX_TST—Offset 64228h" on page 571	00000000h
64300–64303h	4	"DP_D—Offset 64300h" on page 573	00000018h
64310–64313h	4	"DPD_AUX_CH_CTL—Offset 64310h" on page 575	00050000h
64314–64317h	4	"DPD_AUX_CH_DATA1—Offset 64314h" on page 578	00000000h
64318–6431Bh	4	"DPD_AUX_CH_DATA2—Offset 64318h" on page 578	00000000h
6431C–6431Fh	4	"DPD_AUX_CH_DATA3—Offset 6431Ch" on page 579	00000000h
64320–64323h	4	"DPD_AUX_CH_DATA4—Offset 64320h" on page 579	00000000h
64324–64327h	4	"DPD_AUX_CH_DATA5—Offset 64324h" on page 580	00000000h
64328–6432Bh	4	"DPD_AUX_TST—Offset 64328h" on page 580	00000000h
65000–65003h	4	"STREAM_A_LPE_AUD_CONFIG—Offset 65000h" on page 582	00000280h
65008–6500Bh	4	"STREAM_A_LPE_AUD_CH_STATUS_0—Offset 65008h" on page 585	00000000h
6500C–6500Fh	4	"STREAM_A_LPE_AUD_CH_STATUS_1—Offset 6500Ch" on page 585	00000000h
65010–65013h	4	"STREAM_A_LPE_AUD_HDMI_CTS_DP_MAUD—Offset 65010h" on page 586	00000000h
65014–65017h	4	"STREAM_A_LPE_AUD_HDMI_N_DP_NAUD—Offset 65014h" on page 587	00000000h
65020–65023h	4	"STREAM_A_LPE_AUD_BUFFER_CONFIG—Offset 65020h" on page 587	00000100h
65024–65027h	4	"STREAM_A_LPE_AUD_BUF_CH_SWP—Offset 65024h" on page 588	00FAC688h
65040–65043h	4	"STREAM_A_LPE_AUD_BUF_A_ADDR—Offset 65040h" on page 590	00000000h
65044–65047h	4	"STREAM_A_LPE_AUD_BUF_A_LENGTH—Offset 65044h" on page 590	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
65048–6504Bh	4	"STREAM_A_LPE_AUD_BUF_B_ADDR—Offset 65048h" on page 591	00000000h
6504C–6504Fh	4	"STREAM_A_LPE_AUD_BUF_B_LENGTH—Offset 6504Ch" on page 592	00000000h
65050–65053h	4	"STREAM_A_LPE_AUD_BUF_C_ADDR—Offset 65050h" on page 592	00000000h
65054–65057h	4	"STREAM_A_LPE_AUD_BUF_C_LENGTH—Offset 65054h" on page 593	00000000h
65058–6505Bh	4	"STREAM_A_LPE_AUD_BUF_D_ADDR—Offset 65058h" on page 594	00000000h
6505C–6505Fh	4	"STREAM_A_LPE_AUD_BUF_D_LENGTH—Offset 6505Ch" on page 594	00000000h
65060–65063h	4	"STREAM_A_LPE_AUD_CNTL_ST—Offset 65060h" on page 595	00000000h
65064–65067h	4	"STREAM_A_LPE_AUD_HDMI_STATUS—Offset 65064h" on page 597	00000000h
65068–6506Bh	4	"STREAM_A_LPE_AUD_HDMIW_INFOFR—Offset 65068h" on page 599	00000000h
65800–65803h	4	"STREAM_B_LPE_AUD_CONFIG—Offset 65800h" on page 600	00000280h
65808–6580Bh	4	"STREAM_B_LPE_AUD_CH_STATUS_0—Offset 65808h" on page 603	00000000h
6580C–6580Fh	4	"STREAM_B_LPE_AUD_CH_STATUS_1—Offset 6580Ch" on page 603	00000000h
65810–65813h	4	"STREAM_B_LPE_AUD_HDMI_CTS_DP_MAUD—Offset 65810h" on page 604	00000000h
65814–65817h	4	"STREAM_B_LPE_AUD_HDMI_N_DP_NAUD—Offset 65814h" on page 605	00000000h
65820–65823h	4	"STREAM_B_LPE_AUD_BUFFER_CONFIG—Offset 65820h" on page 605	00000100h
65824–65827h	4	"STREAM_B_LPE_AUD_BUF_CH_SWP—Offset 65824h" on page 606	00FAC688h
65840–65843h	4	"STREAM_B_LPE_AUD_BUF_A_ADDR—Offset 65840h" on page 608	00000000h
65844–65847h	4	"STREAM_B_LPE_AUD_BUF_A_LENGTH—Offset 65844h" on page 608	00000000h
65848–6584Bh	4	"STREAM_B_LPE_AUD_BUF_B_ADDR—Offset 65848h" on page 609	00000000h
6584C–6584Fh	4	"STREAM_B_LPE_AUD_BUF_B_LENGTH—Offset 6584Ch" on page 610	00000000h
65850–65853h	4	"STREAM_B_LPE_AUD_BUF_C_ADDR—Offset 65850h" on page 610	00000000h
65854–65857h	4	"STREAM_B_LPE_AUD_BUF_C_LENGTH—Offset 65854h" on page 611	00000000h

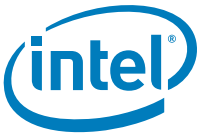


Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
65858–6585Bh	4	"STREAM_B_LPE_AUD_BUF_D_ADDR—Offset 65858h" on page 612	00000000h
6585C–6585Fh	4	"STREAM_B_LPE_AUD_BUF_D_LENGTH—Offset 6585Ch" on page 612	00000000h
65860–65863h	4	"STREAM_B_LPE_AUD_CNTL_ST—Offset 65860h" on page 613	00000000h
65864–65867h	4	"STREAM_B_LPE_AUD_HDMI_STATUS—Offset 65864h" on page 615	00000000h
65868–6586Bh	4	"STREAM_B_LPE_AUD_HDMIW_INFOFR—Offset 65868h" on page 617	00000000h
65900–65903h	4	"STREAM_C_LPE_AUD_CONFIG—Offset 65900h" on page 618	00000280h
65908–6590Bh	4	"STREAM_C_LPE_AUD_CH_STATUS_0—Offset 65908h" on page 621	00000000h
6590C–6590Fh	4	"STREAM_C_LPE_AUD_CH_STATUS_1—Offset 6590Ch" on page 621	00000000h
65910–65913h	4	"STREAM_C_LPE_AUD_HDMI_CTS_DP_MAUD—Offset 65910h" on page 622	00000000h
65914–65917h	4	"STREAM_C_LPE_AUD_HDMI_N_DP_NAUD—Offset 65914h" on page 623	00000000h
65920–65923h	4	"STREAM_C_LPE_AUD_BUFFER_CONFIG—Offset 65920h" on page 623	00000100h
65924–65927h	4	"STREAM_B_LPE_AUD_BUF_CH_SWP (STREAM_C_LPE_AUD_BUF_CH_SWP)—Offset 65924h" on page 624	00FAC688h
65940–65943h	4	"STREAM_C_LPE_AUD_BUF_A_ADDR—Offset 65940h" on page 626	00000000h
65944–65947h	4	"STREAM_C_LPE_AUD_BUF_A_LENGTH—Offset 65944h" on page 626	00000000h
65948–6594Bh	4	"STREAM_C_LPE_AUD_BUF_B_ADDR—Offset 65948h" on page 627	00000000h
6594C–6594Fh	4	"STREAM_C_LPE_AUD_BUF_B_LENGTH—Offset 6594Ch" on page 628	00000000h
65950–65953h	4	"STREAM_C_LPE_AUD_BUF_C_ADDR—Offset 65950h" on page 628	00000000h
65954–65957h	4	"STREAM_C_LPE_AUD_BUF_C_LENGTH—Offset 65954h" on page 629	00000000h
65958–6595Bh	4	"STREAM_C_LPE_AUD_BUF_D_ADDR—Offset 65958h" on page 630	00000000h
6595C–6595Fh	4	"STREAM_C_LPE_AUD_BUF_D_LENGTH—Offset 6595Ch" on page 630	00000000h
65960–65963h	4	"STREAM_C_LPE_AUD_CNTL_ST—Offset 65960h" on page 631	00000000h

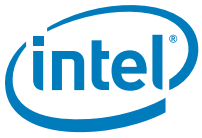
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
65964–65967h	4	"STREAM_C_LPE_AUD_HDMI_STATUS—Offset 65964h" on page 633	00000000h
65968–6596Bh	4	"STREAM_C_LPE_AUD_HDMIW_INFOFR—Offset 65968h" on page 635	00000000h
66000–66003h	4	"PIPEX_CGM_DEGAMME (PIPEX_CGM_DEGAMMA)—Offset 66000h" on page 636	00000000h
67A00–67A03h	4	"PIPEX_CGM_CONTROL—Offset 67A00h" on page 637	00000000h
6D000–6D003h	4	"PCPSXCONFIG—Offset 6D000h" on page 637	00000000h
6D104–6D107h	4	"PCPSXHS_H—Offset 6D104h" on page 638	00000000h
6D108–6D10Bh	4	"PCPSXHS_W—Offset 6D108h" on page 638	00000000h
6D10C–6D10Fh	4	"PCPSXHS_NBP—Offset 6D10Ch" on page 639	00000000h
6D110–6D113h	4	"PCPSXHS_ISF—Offset 6D110h" on page 640	00000000h
6D114–6D117h	4	"PCPSXHS_PC—Offset 6D114h" on page 640	00000000h
6D200–6D20Fh	10	"PCPSX HSC PolyPhase YCbCr Co efficient Memory (PCPSXHS_PM)—Offset 6D200h" on page 641	0000000000000000 0000000000000000 00h
6D300–6D30Fh	10	"PCPSX HSC PolyPhase YCbCr Co efficient Memory (PCPSXHS_APM)—Offset 6D300h" on page 642	0000000000000000 0000000000000000 00h
6D500–6D503h	4	"PCPSXVS_CTRL—Offset 6D500h" on page 642	00000010h
6D504–6D507h	4	"PCPSXVS_H—Offset 6D504h" on page 643	00000000h
6D508–6D50Bh	4	"PCPSXVS_W—Offset 6D508h" on page 644	00000000h
6D510–6D513h	4	"PCPSXVS_ISF—Offset 6D510h" on page 644	00000000h
6D514–6D517h	4	"PCPSXVS_PC—Offset 6D514h" on page 644	00000000h
6D600–6D607h	8	"PCPSX HSC PolyPhase YCbCr Co efficient Memory (PCPSXVS_PM)—Offset 6D600h" on page 645	0000000000000000h
6D700–6D707h	8	"PCPSX HSC PolyPhase YCbCr Co efficient Memory (PCPSXVS_APM)—Offset 6D700h" on page 646	0000000000000000h
6D900–6D903h	4	"SPCSCYGOFF_C—Offset 6D900h" on page 646	00000000h
6D904–6D907h	4	"SPCSCCBOFF_C—Offset 6D904h" on page 647	00000000h
6D908–6D90Bh	4	"SPCSCCROFF_C—Offset 6D908h" on page 648	00000000h
6D90C–6D90Fh	4	"SPCSCC01_C—Offset 6D90Ch" on page 648	00000000h
6D910–6D913h	4	"SPCSCC23_C—Offset 6D910h" on page 649	00000000h
6D914–6D917h	4	"SPCSCC45_C—Offset 6D914h" on page 650	00000000h
6D918–6D91Bh	4	"SPCSCC67_C—Offset 6D918h" on page 650	00000000h
6D91C–6D91Fh	4	"SPCSCC8_C—Offset 6D91Ch" on page 651	00000000h
6D920–6D923h	4	"SPCSCYGICLAMP_C—Offset 6D920h" on page 651	00000000h
6D924–6D927h	4	"SPCSCCBICLAMP_C—Offset 6D924h" on page 652	00000000h
6D928–6D92Bh	4	"SPCSCCRICLAMP_C—Offset 6D928h" on page 652	00000000h
6D92C–6D92Fh	4	"SPCSCYGOCLAMP_C—Offset 6D92Ch" on page 653	00000000h



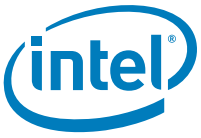
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
6D930–6D933h	4	"SPCSCCBOCLAMP_C—Offset 6D930h" on page 654	00000000h
6D934–6D937h	4	"SPCSCCROCLAMP_C—Offset 6D934h" on page 654	00000000h
6E000–6E003h	4	"PCPSXCONFIG (PCPSXCONFIG_SPR)—Offset 6E000h" on page 655	00000000h
6E104–6E107h	4	"PCPSXHS_H (PCPSXHS_SPR_H)—Offset 6E104h" on page 655	00000000h
6E108–6E10Bh	4	"PCPSXHS_W (PCPSXHS_SPR_W)—Offset 6E108h" on page 656	00000000h
6E10C–6E10Fh	4	"PCPSXHS_NBP (PCPSXHS_SPR_NBP)—Offset 6E10Ch" on page 656	00000000h
6E110–6E113h	4	"PCPSXHS_ISF (PCPSXHS_SPR_ISF)—Offset 6E110h" on page 657	00000000h
6E114–6E117h	4	"PCPSXHS_PC (PCPSXHS_SPR_PC)—Offset 6E114h" on page 657	00000000h
6E200–6E20Fh	10	"PCPSX HSC PolyPhase YCbCr Co efficient Memory (PCPSXHS_SPR_PM)—Offset 6E200h" on page 658	00000000000000000000000000000000h
6E300–6E30Fh	10	"PCPSX HSC PolyPhase YCbCr Co efficient Memory (PCPSXHS_SPR_APM)—Offset 6E300h" on page 659	00000000000000000000000000000000h
6E500–6E503h	4	"PCPSXVS_SPR_CTRL—Offset 6E500h" on page 660	00000010h
6E504–6E507h	4	"PCPSXVS_H (PCPSXVS_SPR_H)—Offset 6E504h" on page 660	00000000h
6E508–6E50Bh	4	"PCPSXVS_W (PCPSXVS_SPR_W)—Offset 6E508h" on page 661	00000000h
6E510–6E513h	4	"PCPSXVS_ISF (PCPSXVS_SPR_ISF)—Offset 6E510h" on page 661	00000000h
6E514–6E517h	4	"PCPSXVS_PC (PCPSXVS_SPR_PC)—Offset 6E514h" on page 662	00000000h
6E600–6E607h	8	"PCPSX HSC PolyPhase YCbCr Co efficient Memory (PCPSXVS_SPR_PM)—Offset 6E600h" on page 662	0000000000000000h
6E700–6E707h	8	"PCPSX HSC PolyPhase YCbCr Co efficient Memory (PCPSXVS_SPR_APM)—Offset 6E700h" on page 663	0000000000000000h
6E900–6E903h	4	"SPCSCYGOFF_D—Offset 6E900h" on page 664	00000000h
6E904–6E907h	4	"SPCSCCBOFF_D—Offset 6E904h" on page 664	00000000h
6E908–6E90Bh	4	"SPCSCCROFF_D—Offset 6E908h" on page 665	00000000h
6E90C–6E90Fh	4	"SPCSCC01_D—Offset 6E90Ch" on page 666	00000000h
6E910–6E913h	4	"SPCSCC23_D—Offset 6E910h" on page 666	00000000h
6E914–6E917h	4	"SPCSCC45_D—Offset 6E914h" on page 667	00000000h
6E918–6E91Bh	4	"SPCSCC67_D—Offset 6E918h" on page 667	00000000h
6E91C–6E91Fh	4	"SPCSCC8_D—Offset 6E91Ch" on page 668	00000000h
6E920–6E923h	4	"SPCSCYGICLAMP_D—Offset 6E920h" on page 668	00000000h



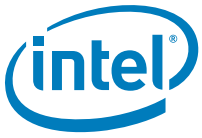
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
6E924–6E927h	4	"SPCSCCBICLAMP_D—Offset 6E924h" on page 669	00000000h
6E928–6E92Bh	4	"SPCSCCRICLAMP_D—Offset 6E928h" on page 670	00000000h
6E92C–6E92Fh	4	"SPCSCYGOCLAMP_D—Offset 6E92Ch" on page 670	00000000h
6E930–6E933h	4	"SPCSCCBOCLAMP_D—Offset 6E930h" on page 671	00000000h
6E934–6E937h	4	"SPCSCCROCLAMP_D—Offset 6E934h" on page 672	00000000h
70000–70003h	4	"PIPEA_DSL—Offset 70000h" on page 672	00000000h
70004–70007h	4	"PIPEA_SLC—Offset 70004h" on page 673	00000000h
70008–7000Bh	4	"PIPEACONF—Offset 70008h" on page 674	00000000h
70010–70013h	4	"PIPEAGCMAXRED—Offset 70010h" on page 679	00010000h
70014–70017h	4	"PIPEAGCMAXGREEN—Offset 70014h" on page 680	00010000h
70018–7001Bh	4	"PIPEAGCMAXBLUE—Offset 70018h" on page 680	00010000h
70024–70027h	4	"PIPEASTAT—Offset 70024h" on page 681	00000000h
70028–7002Bh	4	"DPFLIPSTAT—Offset 70028h" on page 686	00000000h
7002C–7002Fh	4	"DPINVGTT—Offset 7002Ch" on page 689	00000000h
70030–70033h	4	"DSPARB—Offset 70030h" on page 691	80008000h
70034–70037h	4	"FW1—Offset 70034h" on page 692	3F8F0F0Fh
70038–7003Bh	4	"FW2—Offset 70038h" on page 694	0B0F0F0Fh
7003C–7003Fh	4	"FW3—Offset 7003Ch" on page 695	00000000h
70040–70043h	4	"PIPEAFRAMECOUNT—Offset 70040h" on page 697	00000000h
70044–70047h	4	"PIPEAFLIPCOUNT—Offset 70044h" on page 697	00000000h
70048–7004Bh	4	"PIPEAMSAMISC—Offset 70048h" on page 698	00000000h
70050–70053h	4	"DDL1—Offset 70050h" on page 699	00000000h
70054–70057h	4	"DDL2—Offset 70054h" on page 701	00000000h
70058–7005Bh	4	"DDL3—Offset 70058h" on page 702	00000000h
70060–70063h	4	"DSPARB2—Offset 70060h" on page 704	00111111h
70064–70067h	4	"DSPHOWM—Offset 70064h" on page 706	00000000h
70068–7006Bh	4	"DSPHOWM1—Offset 70068h" on page 708	00000000h
70070–70073h	4	"FW4—Offset 70070h" on page 711	00040404h
70074–70077h	4	"FW5—Offset 70074h" on page 712	04040404h
70078–7007Bh	4	"FW6—Offset 70078h" on page 713	00000078h
7007C–7007Fh	4	"FW9—Offset 7007Ch" on page 714	040F040Fh
70080–70083h	4	"CURACNTR—Offset 70080h" on page 715	00000000h
70084–70087h	4	"CURABASE—Offset 70084h" on page 716	00000000h
70088–7008Bh	4	"CURAPOS—Offset 70088h" on page 717	00000000h
70090–70093h	4	"CURAPALET_0—Offset 70090h" on page 719	00000000h
70094–70097h	4	"CURAPALET_1—Offset 70094h" on page 719	00000000h
70098–7009Bh	4	"CURAPALET_2—Offset 70098h" on page 720	00000000h



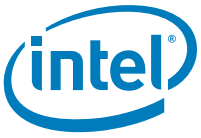
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
7009C–7009Fh	4	"CURAPALET_3—Offset 7009Ch" on page 721	00000000h
700AC–700AFh	4	"CURALIVEBASE—Offset 700ACh" on page 721	00000000h
700B4–700B7h	4	"FW7—Offset 700B4h" on page 722	040F040Fh
700B8–700BBh	4	"FW8—Offset 700B8h" on page 723	040F040Fh
700C0–700C3h	4	"CURBCNTR—Offset 700C0h" on page 724	00000000h
700C4–700C7h	4	"CURBBASE—Offset 700C4h" on page 726	00000000h
700C8–700CBh	4	"CURBPOS—Offset 700C8h" on page 727	00000000h
700D0–700D3h	4	"CURBPALET_0—Offset 700D0h" on page 729	00000000h
700D4–700D7h	4	"CURBPALET_1—Offset 700D4h" on page 729	00000000h
700D8–700DBh	4	"CURBPALET_2—Offset 700D8h" on page 730	00000000h
700DC–700DFh	4	"CURBPALET_3—Offset 700DCh" on page 731	00000000h
700E0–700E3h	4	"CURCCNTR—Offset 700E0h" on page 731	00000000h
700E4–700E7h	4	"CURCBASE—Offset 700E4h" on page 733	00000000h
700E8–700EBh	4	"CURCPOS—Offset 700E8h" on page 734	00000000h
700EC–700EFh	4	"CURCLIVEBASE—Offset 700ECh" on page 736	00000000h
700F0–700F3h	4	"CURCPALET_0—Offset 700F0h" on page 737	00000000h
700F4–700F7h	4	"CURCPALET_1—Offset 700F4h" on page 738	00000000h
700F8–700FBh	4	"CURCPALET_2—Offset 700F8h" on page 738	00000000h
700FC–700FFh	4	"CURCPALET_3—Offset 700FCh" on page 739	00000000h
7017C–7017Fh	4	"DSPAADDR—Offset 7017Ch" on page 740	00000000h
70180–70183h	4	"DSPACNTR—Offset 70180h" on page 741	00000000h
70184–70187h	4	"DSPALINOFF—Offset 70184h" on page 745	00000000h
70188–7018Bh	4	"DSPASTRIDE—Offset 70188h" on page 746	00000000h
70194–70197h	4	"DSPAKEYVAL—Offset 70194h" on page 747	00000000h
70198–7019Bh	4	"DSPAKEYMSK—Offset 70198h" on page 747	00000000h
7019C–7019Fh	4	"DSPASURF—Offset 7019Ch" on page 748	00000000h
701A4–701A7h	4	"DSPATILEOFF—Offset 701A4h" on page 750	00000000h
701AC–701AFh	4	"DSPASURFLIVE—Offset 701ACh" on page 750	00000000h
70400–70403h	4	"CBR1—Offset 70400h" on page 751	00000000h
70404–70407h	4	"CBR2—Offset 70404h" on page 754	00000000h
70408–7040Bh	4	"CCBR—Offset 70408h" on page 756	00000000h
7040C–7040Fh	4	"CBR3—Offset 7040Ch" on page 757	00000000h
70410–70413h	4	"SWF00—Offset 70410h" on page 758	00000000h
70414–70417h	4	"SWF01—Offset 70414h" on page 758	00000000h
70418–7041Bh	4	"SWF02—Offset 70418h" on page 759	00000000h
7041C–7041Fh	4	"SWF03—Offset 7041Ch" on page 759	00000000h
70420–70423h	4	"SWF04—Offset 70420h" on page 760	00000000h



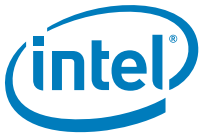
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
70424–70427h	4	"SWF05—Offset 70424h" on page 760	00000000h
70428–7042Bh	4	"SWF06—Offset 70428h" on page 761	00000000h
7042C–7042Fh	4	"SWF07—Offset 7042Ch" on page 761	00000000h
70430–70433h	4	"SWF08—Offset 70430h" on page 762	00000000h
70434–70437h	4	"SWF09—Offset 70434h" on page 762	00000000h
70438–7043Bh	4	"SWF0A—Offset 70438h" on page 763	00000000h
7043C–7043Fh	4	"SWF0B—Offset 7043Ch" on page 763	00000000h
70440–70443h	4	"SWF0C—Offset 70440h" on page 764	00000000h
70444–70447h	4	"SWF0D—Offset 70444h" on page 764	00000000h
70448–7044Bh	4	"SWF0E—Offset 70448h" on page 765	00000000h
7044C–7044Fh	4	"SWF0F—Offset 7044Ch" on page 765	00000000h
70450–70453h	4	"CBR4—Offset 70450h" on page 766	00000000h
71000–71003h	4	"PIPEB_DSL—Offset 71000h" on page 768	00000000h
71004–71007h	4	"PIPEB_SLC—Offset 71004h" on page 769	00000000h
71008–7100Bh	4	"PIPEBCONF—Offset 71008h" on page 770	00000000h
71010–71013h	4	"PIPEBGCMAXRED—Offset 71010h" on page 774	00010000h
71014–71017h	4	"PIPEBGCMAXGREEN—Offset 71014h" on page 775	00010000h
71018–7101Bh	4	"PIPEBGCMAXBLUE—Offset 71018h" on page 776	00010000h
71024–71027h	4	"PIPEBSTAT—Offset 71024h" on page 777	00000000h
71040–71043h	4	"PIPEBFRAMECOUNT—Offset 71040h" on page 782	00000000h
71044–71047h	4	"PIPEBFLIPCOUNT—Offset 71044h" on page 782	00000000h
71048–7104Bh	4	"PIPEBMSAMISC—Offset 71048h" on page 783	00000000h
7117C–7117Fh	4	"DSPBADDR—Offset 7117Ch" on page 784	00000000h
71180–71183h	4	"DSPBCNTR—Offset 71180h" on page 786	01000000h
71184–71187h	4	"DSPBLINOFFSET—Offset 71184h" on page 789	00000000h
71188–7118Bh	4	"DSPBSTRIDE—Offset 71188h" on page 790	00000000h
71194–71197h	4	"DSPBKEYVAL—Offset 71194h" on page 791	00000000h
71198–7119Bh	4	"DSPBKEYMSK—Offset 71198h" on page 792	00000000h
7119C–7119Fh	4	"DSPBSURF—Offset 7119Ch" on page 792	00000000h
711A4–711A7h	4	"DSPBTILEOFF—Offset 711A4h" on page 794	00000000h
711AC–711AFh	4	"DSPBSURFLIVE—Offset 711ACh" on page 795	00000000h
71200–71203h	4	"DSPBFLPQSTAT—Offset 71200h" on page 796	00000000h
71400–71403h	4	"SWF10—Offset 71410h" on page 797	00000000h
71410–71413h	4	"SWF10—Offset 71410h" on page 797	00000000h
71414–71417h	4	"SWF11—Offset 71414h" on page 797	00000000h
71418–7141Bh	4	"SWF12—Offset 71418h" on page 798	00000000h
7141C–7141Fh	4	"SWF13—Offset 7141Ch" on page 798	00000000h



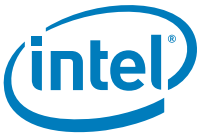
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
71420–71423h	4	"SWF14—Offset 71420h" on page 798	00000000h
71424–71427h	4	"SWF15—Offset 71424h" on page 799	00000000h
71428–7142Bh	4	"SWF16—Offset 71428h" on page 799	00000000h
7142C–7142Fh	4	"SWF17—Offset 7142Ch" on page 799	00000000h
71430–71433h	4	"SWF18—Offset 71430h" on page 800	00000000h
71434–71437h	4	"SWF19—Offset 71434h" on page 800	00000000h
71438–7143Bh	4	"SWF1A—Offset 71438h" on page 801	00000000h
7143C–7143Fh	4	"SWF1B—Offset 7143Ch" on page 801	00000000h
71440–71443h	4	"SWF1C—Offset 71440h" on page 801	00000000h
71444–71447h	4	"SWF1D—Offset 71444h" on page 802	00000000h
71448–7144Bh	4	"SWF1E—Offset 71448h" on page 802	00000000h
7144C–7144Fh	4	"SWF1F—Offset 7144Ch" on page 802	00000000h
72180–72183h	4	"SPACNTR—Offset 72180h" on page 803	00000000h
72184–72187h	4	"SPALINOFF—Offset 72184h" on page 807	00000000h
72188–7218Bh	4	"SPASTRIDE—Offset 72188h" on page 807	00000000h
7218C–7218Fh	4	"SPAPOS—Offset 7218Ch" on page 808	00000000h
72190–72193h	4	"SPASIZE—Offset 72190h" on page 808	00000000h
72194–72197h	4	"SPAKEYMINVAL—Offset 72194h" on page 809	00000000h
72198–7219Bh	4	"SPAKEYMSK—Offset 72198h" on page 809	00000000h
7219C–7219Fh	4	"SPASURF—Offset 7219Ch" on page 810	00000000h
721A0–721A3h	4	"SPAKEYMAXVAL—Offset 721A0h" on page 813	00000000h
721A4–721A7h	4	"SPATILEOFF—Offset 721A4h" on page 813	00000000h
721A8–721ABh	4	"SPACONTALPHA—Offset 721A8h" on page 814	00000000h
721AC–721AFh	4	"SPALIVESURF—Offset 721ACh" on page 815	00000000h
721D0–721D3h	4	"SPACLRC0—Offset 721D0h" on page 817	01000000h
721D4–721D7h	4	"SPACLRC1—Offset 721D4h" on page 817	00000080h
721E0–721E3h	4	"SPAGAMC5—Offset 721E0h" on page 818	00C0C0C0h
721E4–721E7h	4	"SPAGAMC4—Offset 721E4h" on page 819	00808080h
721E8–721EBh	4	"SPAGAMC3—Offset 721E8h" on page 819	00404040h
721EC–721EFh	4	"SPAGAMC2—Offset 721ECh" on page 820	00202020h
721F0–721F3h	4	"SPAGAMC1—Offset 721F0h" on page 820	00101010h
721F4–721F7h	4	"SPAGAMC0—Offset 721F4h" on page 821	00080808h
72280–72283h	4	"SPBCNTR—Offset 72280h" on page 821	00000000h
72284–72287h	4	"SPBLINOFF—Offset 72284h" on page 825	00000000h
72288–7228Bh	4	"SPBSTRIDE—Offset 72288h" on page 825	00000000h
7228C–7228Fh	4	"SPBPOS—Offset 7228Ch" on page 826	00000000h
72290–72293h	4	"SPBSIZE—Offset 72290h" on page 827	00000000h



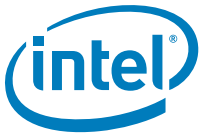
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
72294–72297h	4	"SPBKEYMINVAL—Offset 72294h" on page 827	00000000h
72298–7229Bh	4	"SPBKEYMSK—Offset 72298h" on page 828	00000000h
7229C–7229Fh	4	"SPBSURF—Offset 7229Ch" on page 829	00000000h
722A0–722A3h	4	"SPBKEYMAXVAL—Offset 722A0h" on page 831	00000000h
722A4–722A7h	4	"SPBTILEOFF—Offset 722A4h" on page 832	00000000h
722A8–722ABh	4	"SPBCONTALPHA—Offset 722A8h" on page 832	00000000h
722AC–722AFh	4	"SPBLIVESURF—Offset 722ACh" on page 833	00000000h
722D0–722D3h	4	"SPBCLRC0—Offset 722D0h" on page 835	01000000h
722D4–722D7h	4	"SPBCLRC1—Offset 722D4h" on page 836	00000080h
722E0–722E3h	4	"SPBGAMC5—Offset 722E0h" on page 837	00C0C0C0h
722E4–722E7h	4	"SPBGAMC4—Offset 722E4h" on page 838	00808080h
722E8–722EBh	4	"SPBGAMC3—Offset 722E8h" on page 838	00404040h
722EC–722EFh	4	"SPBGAMC2—Offset 722ECh" on page 839	00202020h
722F0–722F3h	4	"SPBGAMC1—Offset 722F0h" on page 839	00101010h
722F4–722F7h	4	"SPBGAMC0—Offset 722F4h" on page 840	00080808h
72380–72383h	4	"SPCCNTR—Offset 72380h" on page 840	00000000h
72384–72387h	4	"SPCLINOFF—Offset 72384h" on page 844	00000000h
72388–7238Bh	4	"SPCSTRIDE—Offset 72388h" on page 845	00000000h
7238C–7238Fh	4	"SPCPOS—Offset 7238Ch" on page 845	00000000h
72390–72393h	4	"SPCSIZE—Offset 72390h" on page 846	00000000h
72394–72397h	4	"SPCKEYMINVAL—Offset 72394h" on page 847	00000000h
72398–7239Bh	4	"SPCKEYMSK—Offset 72398h" on page 847	00000000h
7239C–7239Fh	4	"SPCSURF—Offset 7239Ch" on page 848	00000000h
723A0–723A3h	4	"SPCKEYMAXVAL—Offset 723A0h" on page 851	00000000h
723A4–723A7h	4	"SPCTILEOFF—Offset 723A4h" on page 851	00000000h
723A8–723ABh	4	"SPCCONTALPHA—Offset 723A8h" on page 852	00000000h
723AC–723AFh	4	"SPCLIVESURF—Offset 723ACh" on page 853	00000000h
723D0–723D3h	4	"SPCCLRC0—Offset 723D0h" on page 855	01000000h
723D4–723D7h	4	"SPCCLRC1—Offset 723D4h" on page 855	00000080h
723E0–723E3h	4	"SPCGAMC5—Offset 723E0h" on page 856	00C0C0C0h
723E4–723E7h	4	"SPCGAMC4—Offset 723E4h" on page 857	00808080h
723E8–723EBh	4	"SPCGAMC3—Offset 723E8h" on page 857	00404040h
723EC–723EFh	4	"SPCGAMC2—Offset 723ECh" on page 858	00202020h
723F0–723F3h	4	"SPCGAMC1—Offset 723F0h" on page 858	00101010h
723F4–723F7h	4	"SPCGAMC0—Offset 723F4h" on page 859	00080808h
72414–72417h	4	"SWF30—Offset 72414h" on page 859	00000000h
72418–7241Bh	4	"SWF31—Offset 72418h" on page 860	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
7241C–7241Fh	4	"SWF32—Offset 7241Ch" on page 860	00000000h
72480–72483h	4	"SPDCNTR—Offset 72480h" on page 860	00000000h
72484–72487h	4	"SPDLINOFF—Offset 72484h" on page 864	00000000h
72488–7248Bh	4	"SPDSTRIDE—Offset 72488h" on page 865	00000000h
7248C–7248Fh	4	"SPDPOS—Offset 7248Ch" on page 865	00000000h
72490–72493h	4	"SPDSIZE—Offset 72490h" on page 866	00000000h
72494–72497h	4	"SPDKEYMINVAL—Offset 72494h" on page 867	00000000h
72498–7249Bh	4	"SPDKEYMSK—Offset 72498h" on page 867	00000000h
7249C–7249Fh	4	"SPDSURF—Offset 7249Ch" on page 868	00000000h
724A0–724A3h	4	"SPDKEYMAXVAL—Offset 724A0h" on page 871	00000000h
724A4–724A7h	4	"SPDTILEOFF—Offset 724A4h" on page 871	00000000h
724A8–724ABh	4	"SPDCONTALPHA—Offset 724A8h" on page 872	00000000h
724AC–724AFh	4	"SPDLIVESURF—Offset 724ACh" on page 873	00000000h
724D0–724D3h	4	"SPDCLRC0—Offset 724D0h" on page 875	01000000h
724D4–724D7h	4	"SPDCLRC1—Offset 724D4h" on page 875	00000080h
724E0–724E3h	4	"SPDGAMC5—Offset 724E0h" on page 876	00C0C0C0h
724E4–724E7h	4	"SPDGAMC4—Offset 724E4h" on page 877	00808080h
724E8–724EBh	4	"SPDGAMC3—Offset 724E8h" on page 877	00404040h
724EC–724EFh	4	"SPDGAMC2—Offset 724ECh" on page 878	00202020h
724F0–724F3h	4	"SPDGAMC1—Offset 724F0h" on page 878	00101010h
724F4–724F7h	4	"SPDGAMC0—Offset 724F4h" on page 879	00080808h
72580–72583h	4	"SPECNTR—Offset 72580h" on page 879	00000000h
72584–72587h	4	"SPELINOFF—Offset 72584h" on page 883	00000000h
72588–7258Bh	4	"SPESTRIDE—Offset 72588h" on page 884	00000000h
7258C–7258Fh	4	"SPEPOS—Offset 7258Ch" on page 884	00000000h
72590–72593h	4	"SPESIZE—Offset 72590h" on page 885	00000000h
72594–72597h	4	"SPEKEYMINVAL—Offset 72594h" on page 886	00000000h
72598–7259Bh	4	"SPEKEYMSK—Offset 72598h" on page 886	00000000h
7259C–7259Fh	4	"SPESURF—Offset 7259Ch" on page 887	00000000h
725A0–725A3h	4	"SPEKEYMAXVAL—Offset 725A0h" on page 890	00000000h
725A4–725A7h	4	"SPETILEOFF—Offset 725A4h" on page 890	00000000h
725A8–725ABh	4	"SPECONTALPHA—Offset 725A8h" on page 891	00000000h
725AC–725AFh	4	"SPELIVESURF—Offset 725ACh" on page 892	00000000h
725D0–725D3h	4	"SPECLRC0—Offset 725D0h" on page 894	01000000h
725D4–725D7h	4	"SPECLRC1—Offset 725D4h" on page 894	00000080h
725E0–725E3h	4	"SPEGAMC5—Offset 725E0h" on page 895	00C0C0C0h
725E4–725E7h	4	"SPEGAMC4—Offset 725E4h" on page 896	00808080h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
725E8–725EBh	4	"SPEGAMC3—Offset 725E8h" on page 896	00404040h
725EC–725EFh	4	"SPEGAMC2—Offset 725ECh" on page 897	00202020h
725F0–725F3h	4	"SPEGAMC1—Offset 725F0h" on page 897	00101010h
725F4–725F7h	4	"SPEGAMC0—Offset 725F4h" on page 898	00080808h
72680–72683h	4	"SPFCNTR—Offset 72680h" on page 898	00000000h
72684–72687h	4	"SPFLINOFF—Offset 72684h" on page 902	00000000h
72688–7268Bh	4	"SPFSTRIDE—Offset 72688h" on page 903	00000000h
7268C–7268Fh	4	"SPFPOS—Offset 7268Ch" on page 903	00000000h
72690–72693h	4	"SPFSIZE—Offset 72690h" on page 904	00000000h
72694–72697h	4	"SPFKEYMINVAL—Offset 72694h" on page 905	00000000h
72698–7269Bh	4	"SPFKEYMSK—Offset 72698h" on page 905	00000000h
7269C–7269Fh	4	"SPFSURF—Offset 7269Ch" on page 906	00000000h
726A0–726A3h	4	"SPFKEYMAXVAL—Offset 726A0h" on page 909	00000000h
726A4–726A7h	4	"SPFTILEOFF—Offset 726A4h" on page 909	00000000h
726A8–726ABh	4	"SPFCONTALPHA—Offset 726A8h" on page 910	00000000h
726AC–726AFh	4	"SPFLIVESURF—Offset 726ACh" on page 911	00000000h
726D0–726D3h	4	"SPFCLRC0—Offset 726D0h" on page 913	01000000h
726D4–726D7h	4	"SPFCLRC1—Offset 726D4h" on page 913	00000080h
726E0–726E3h	4	"SPFGAMC5—Offset 726E0h" on page 914	00C0C0C0h
726E4–726E7h	4	"SPFGAMC4—Offset 726E4h" on page 915	00808080h
726E8–726EBh	4	"SPFGAMC3—Offset 726E8h" on page 915	00404040h
726EC–726EFh	4	"SPFGAMC2—Offset 726ECh" on page 916	00202020h
726F0–726F3h	4	"SPFGAMC1—Offset 726F0h" on page 916	00101010h
726F4–726F7h	4	"SPFGAMC0—Offset 726F4h" on page 917	00080808h
73000–73003h	4	"PCSRC—Offset 73000h" on page 917	00000000h
73004–73007h	4	"PCSTAT—Offset 73004h" on page 920	00000000h
73008–7300Bh	4	"PCSRC2—Offset 73008h" on page 922	00000000h
7300C–7300Fh	4	"PCSTAT2—Offset 7300Ch" on page 924	00000000h
73010–73013h	4	"PCSRC3—Offset 73010h" on page 926	00000000h
73014–73017h	4	"PCSTAT3—Offset 73014h" on page 928	00000000h
74000–74003h	4	"PIPEC_DSL—Offset 74000h" on page 930	00000000h
74004–74007h	4	"PIPEC_SLC—Offset 74004h" on page 931	00000000h
74008–7400Bh	4	"PIPECCONF—Offset 74008h" on page 932	00000000h
74010–74013h	4	"PIPECGCMAXRED—Offset 74010h" on page 937	00010000h
74014–74017h	4	"PIPECGCMAXGREEN—Offset 74014h" on page 937	00010000h
74018–7401Bh	4	"PIPECGCMAXBLUE—Offset 74018h" on page 938	00010000h
74024–74027h	4	"PIPECSTAT—Offset 74024h" on page 938	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
74040–74043h	4	"PIPECFRAMECOUNT—Offset 74040h" on page 943	00000000h
74044–74047h	4	"PIPECFLIPCOUNT—Offset 74044h" on page 943	00000000h
74048–7404Bh	4	"PIPECMSAMISC—Offset 74048h" on page 944	00000000h
7417C–7417Fh	4	"DSPCADDR—Offset 7417Ch" on page 946	00000000h
74180–74183h	4	"DSPCCNTR—Offset 74180h" on page 948	01000000h
74184–74187h	4	"DSPCLINOFFSET—Offset 74184h" on page 952	00000000h
74188–7418Bh	4	"DSPCSTRIDE—Offset 74188h" on page 953	00000000h
74194–74197h	4	"DSPCKEYVAL—Offset 74194h" on page 953	00000000h
74198–7419Bh	4	"DSPCKEYMSK—Offset 74198h" on page 954	00000000h
7419C–7419Fh	4	"DSPCSURF—Offset 7419Ch" on page 954	00000000h
741A4–741A7h	4	"DSPCTILEOFF—Offset 741A4h" on page 956	00000000h
741AC–741AFh	4	"DSPCSURFLIVE—Offset 741ACh" on page 957	00000000h
74200–74203h	4	"DSPCFLPQSTAT—Offset 74200h" on page 957	00000000h

4.3.1 CRCCTRLREDC—Offset 63050h

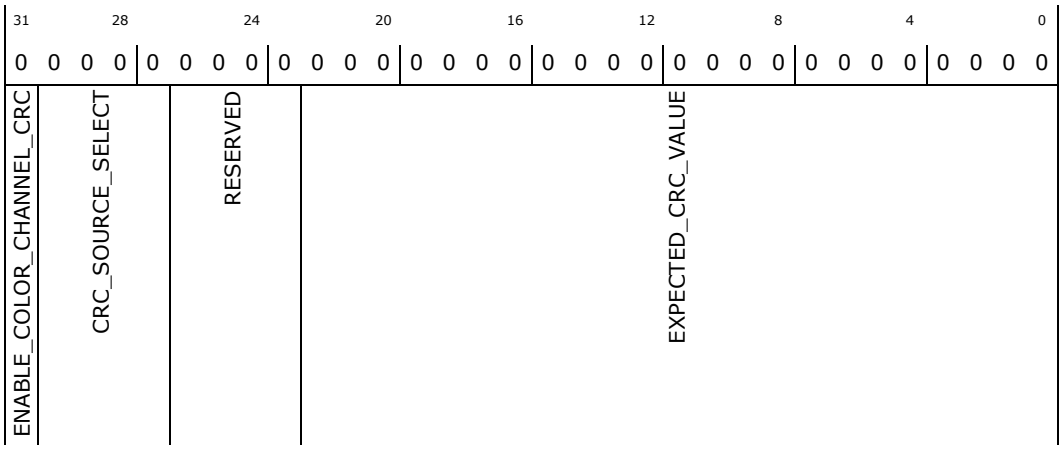
Pipe B CRC Color Control Register (Red)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 63050h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**ENABLE_COLOR_CHANNEL_CRC:** After being enabled for the first time, you need to wait for two VBLANK events for a valid CRC result. After that, a CRC will be generated each frame. 0 = CRC Calculations are disabled 1 = CRC Calculations are enabled
30:27	0x0 RW	**CRC_SOURCE_SELECT:** These bits select the source of the data to put into the CRC logic. 0000: Pipe B (Not available when DisplayPort or TV is enabled on this pipe) 0001: sDVOB/HDMIB (30 bit format. Only select when HDMIB is set to pipe B) 0010: sDVOC/HDMIC (30 bit format. Only select when HDMIC is set to pipe B) 0011: DisplayPort D (40 bit format) [DevCTG] 0100: TV Encoder outputs (30 bit format) 0101: TV filter outputs (30 bit format) 0110: DisplayPort B (40 bit format) 0111: DisplayPort C (40 bit format) 1000: Audio DP (Audio for DisplayPort (pcdclk). Only select when Audio is on DisplayPort on Pipe B) 1001: Audio HDMI (Audio for HDMI (dotclock) Only select when Audio is on HDMI on Pipe B) Others: Reserved
26:23	0x0 RO	**RESERVED:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
22:0	0x0 RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

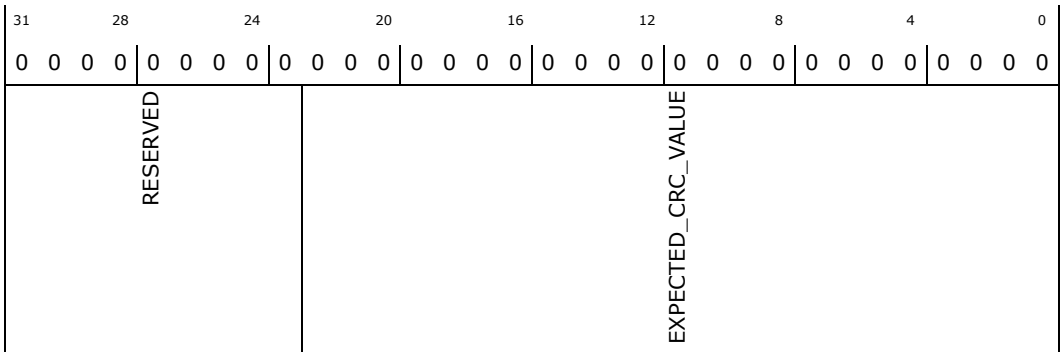
4.3.2 CRCCTRLGREENC—Offset 63054h

Pipe C CRC Color Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63054h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Write as zero
22:0	0x0 RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

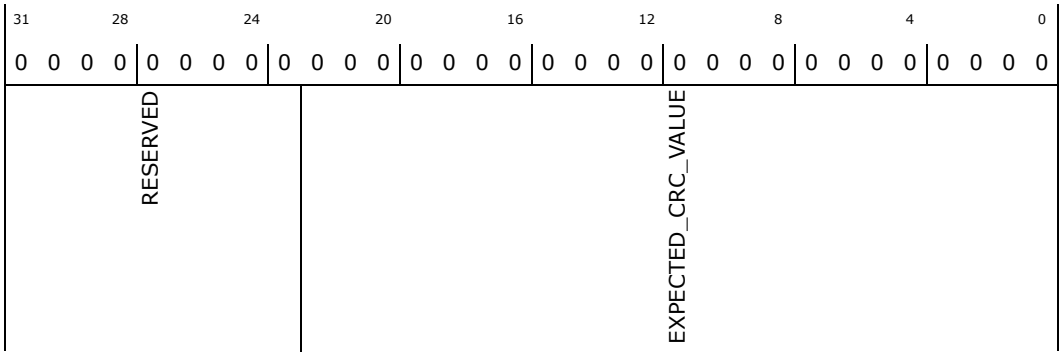
4.3.3 CRCCTRLBLUEC—Offset 63058h

Pipe C CRC Color Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63058h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Write as zero
22:0	0x0 RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

4.3.4 CRCCTRLALPHAC—Offset 6305Ch

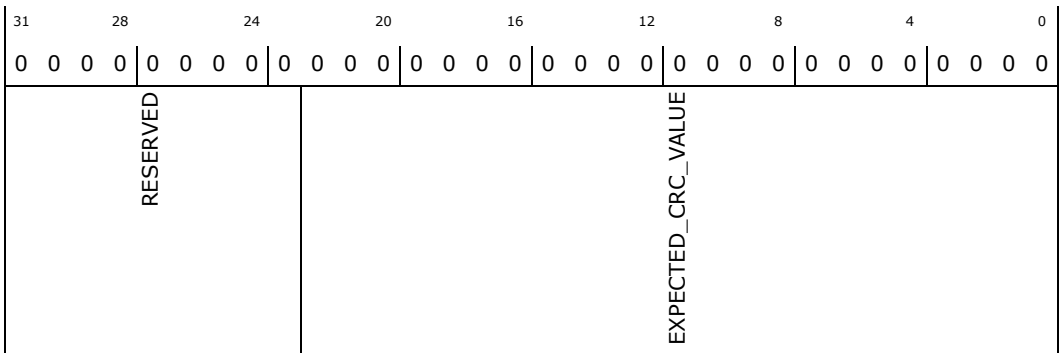
Pipe C CRC Color Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6305Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
22:0	0x0 RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

4.3.5 CRCRESREDC—Offset 63060h

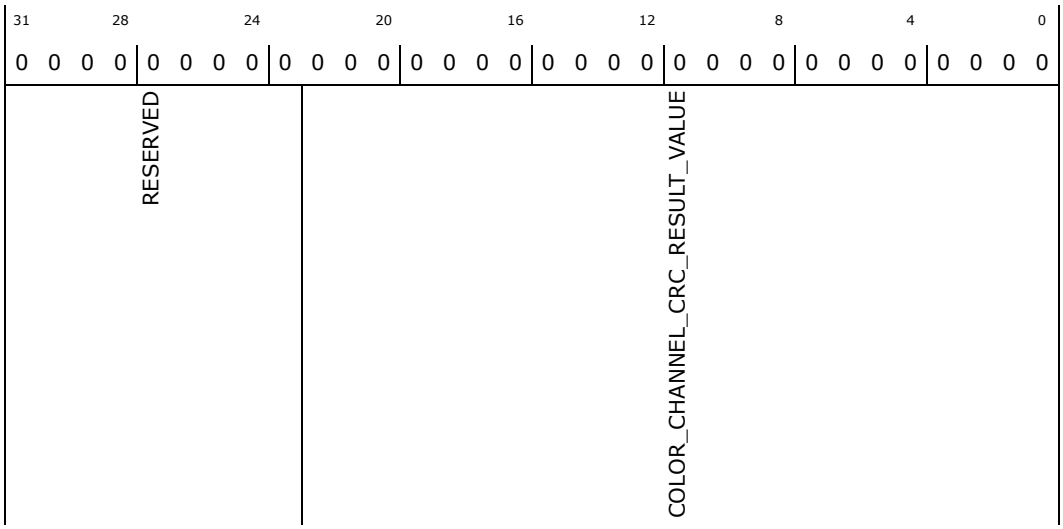
Pipe B CRC Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 63060h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Read only
22:0	0x0 RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

4.3.6 CRCRESGREENC—Offset 63064h

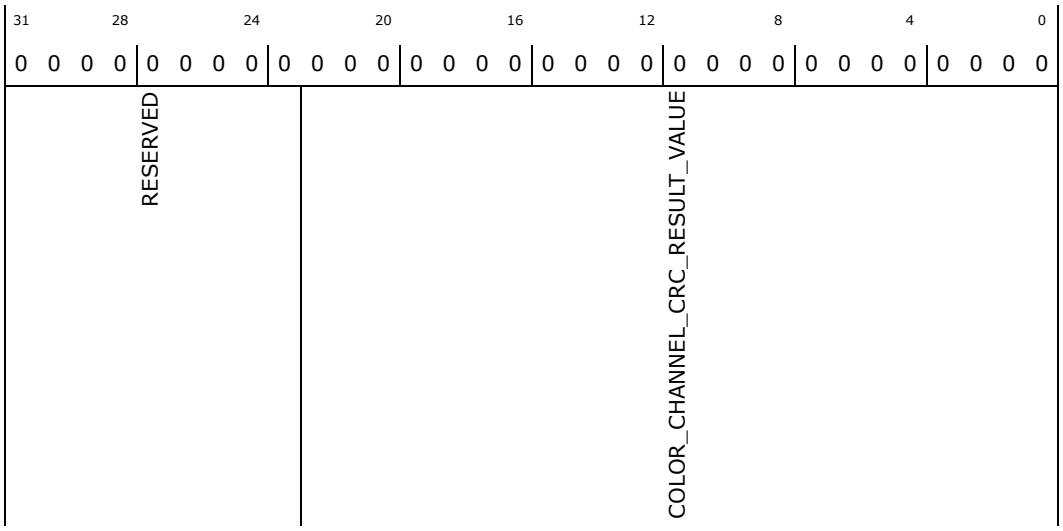
Pipe C CRC Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 63064h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Read only
22:0	0x0 RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

4.3.7 CRCRESBLUEC—Offset 63068h

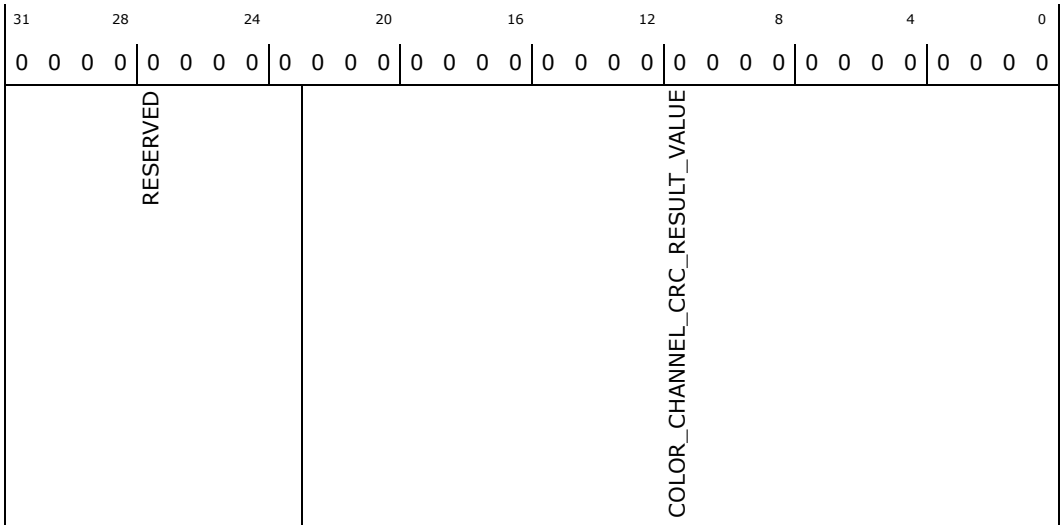
Pipe B CRC Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 63068h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Read only
22:0	0x0 RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

4.3.8 CRCRESALPHAC—Offset 6306Ch

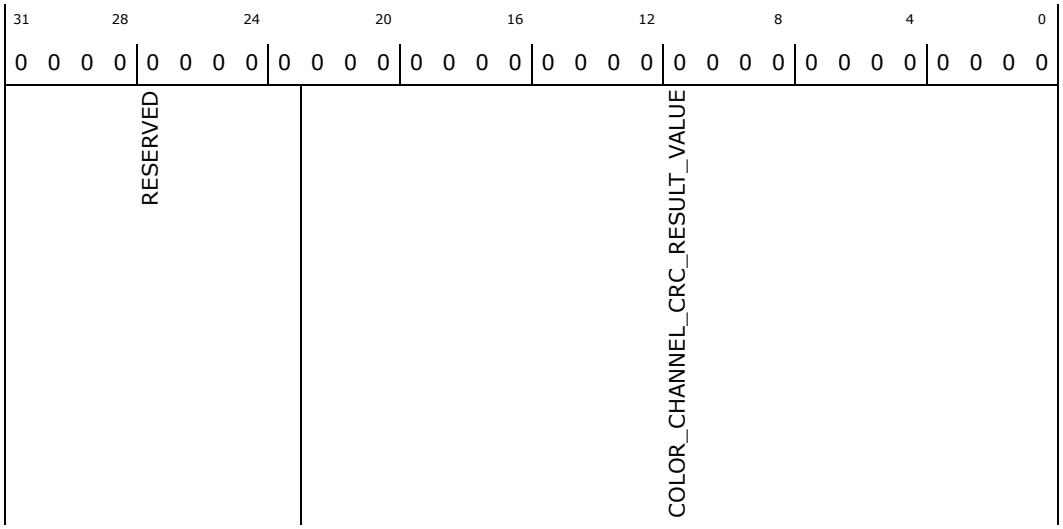
Pipe C CRC Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6306Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Read only
22:0	0x0 RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

4.3.9 CRCCTRLRESIDUE2C—Offset 63070h

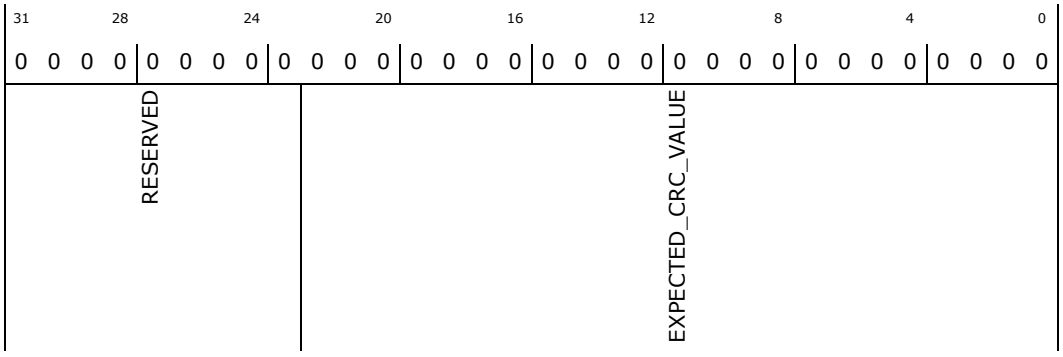
Pipe C CRC Color Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 63070h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Write as zero
22:0	0x0 RW	**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

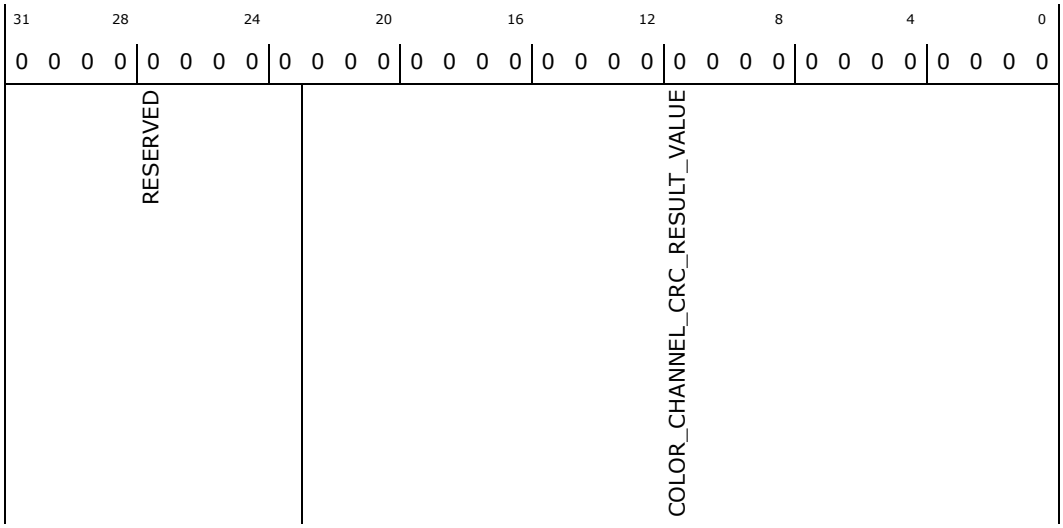
4.3.10 CRCRESRESIDUAL2C—Offset 63080h

Pipe B CRC Result Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63080h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RESERVED:** Read only
22:0	0x0 RO	**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

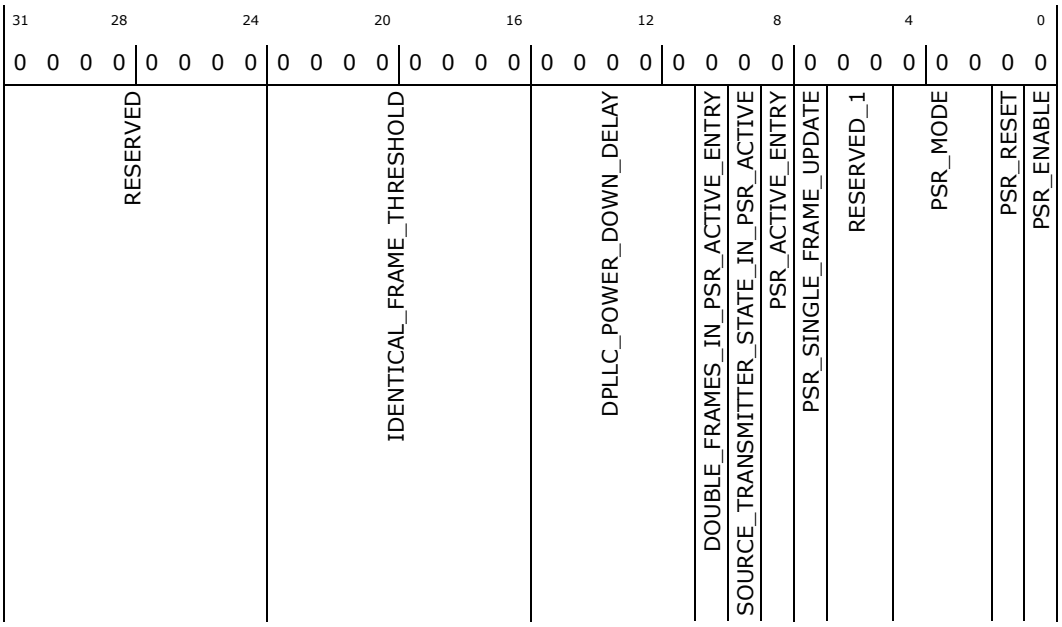
4.3.11 PSRCTLC—Offset 63090h

Pipe C Panel Self Refresh Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63090h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:16	0x0 RW	**IDENTICAL_FRAME_THRESHOLD:** Number of identical frames that display controller needs to exceed in order to transition to PSR active state in HW timer mode
15:11	0x0 RW	**DPLLC_POWER_DOWN_DELAY:** programmable delay from main link powerdown to DPLLC powerdown. The delay is in number of cdclk clocks.
10	0x0 RW	**DOUBLE_FRAMES_IN_PSR_ACTIVE_ENTRY:** . If asserted, HW will send two frames with same SDP active setting when entry PSR active state. This bit is set if the vertical blanking time is less than 330us.
9	0x0 RW	**SOURCE_TRANSMITTER_STATE_IN_PSR_ACTIVE:** . If asserted, HW will keep transmitter active during PSR active state and sends only idle symbols. If deasserted, HW will turn off transmitter during PSR active state. Display driver will keep this bit consistent with Source transmitter state in PSR active bit in DPCD register of the sink.
8	0x0 RW	**PSR_ACTIVE_ENTRY:** This bit is only valid in PSR_mode is SW timer mode. If it is asserted, HW will transition into PSR_active state. If it is deasserted, HW will transition to PSR_inactive state. SW should not set or clear this bit more than once within one vblank period.
7	0x0 RW	**PSR_SINGLE_FRAME_UPDATE:** In PSR persistent mode, SW set this bit before writing registers for a flip. It will be self-clear when it gets to the PSR active state.

Bit Range	Default & Access	Field Name (ID): Description
6:5	0x0 RO	**RESERVED_1:** Reserved.
4:2	0x0 RW	**PSR_MODE:** b011-111: reserved. b010: PSR with HW timer. HW timer decides PSR active entry point. PSR active state exits upon MMIO write registers that may change the frame buffer. b001: PSR with SW timer. In this mode, SW will keep track of idle frames and buffer modification in the driver and explicitly specify the entry and exit PSR active state point. b000: PSR manual (debug) mode. All of PSR state transitions and SDP content is managed by SW driver. SW is responsible to change SDP content for every frame with appropriate values to keep PSR panel in synchronized states.
1	0x0 RW	**PSR_RESET:** If assert all PSR functions are reset back to PSR inactive state. When it needs to resynchronize source and sync, SW writes 0x2 to DPCD register 600h and to this bit to get system back to PSR active states. This bit is self clear.
0	0x0 RW	**PSR_ENABLE:** Panel Self-refresh is enabled. When it is asserted PSR is enabled and operate in one of the mode that specified by PSR mode.

4.3.12 PSRSTATC—Offset 63094h

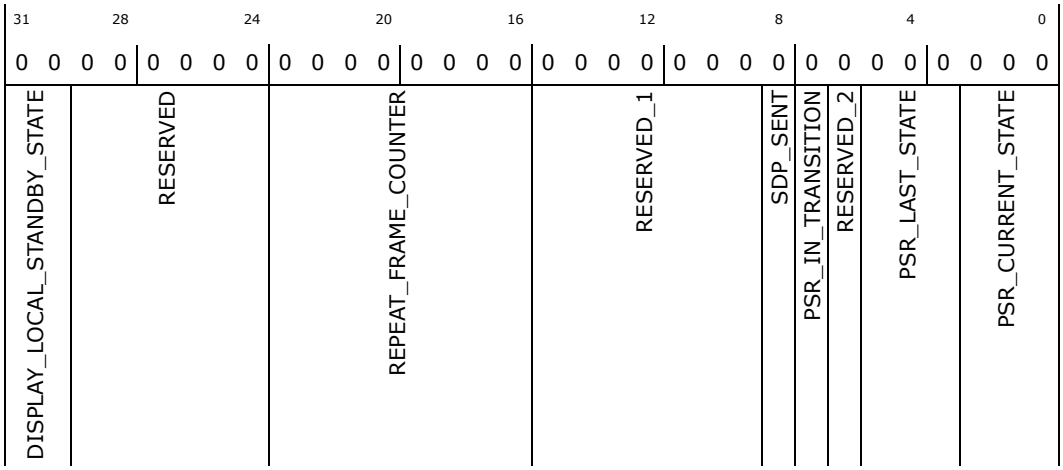
Pipe C PSR status register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 63094h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**DISPLAY_LOCAL_STANDBY_STATE:**00: D0 idle state, fetch frame buffer from system memory 02: D0i2 PSR is active, display controller is trunk gated 03: D0i3 PSR is active, display controller is power gated
29:24	0x0 RO	**RESERVED:** Reserved.
23:16	0x0 RO	**REPEAT_FRAME_COUNTER:** Number of identical frames has been sent by display controller. Value is not roll over at 255.
15:9	0x0 RO	**RESERVED_1:** Reserved.
8	0x0 RO	**SDP_SENT:** it indicates if SDP packet has been sent in current frame.
7	0x0 RO	**PSR_IN_TRANSITION:** There is a period that source already committed to PSR active but sink did not. SW should not change the source state at this time but wait until this status bit is clear. The wait time should in the range of 120-250us in the worst case.
6	0x0 RO	**RESERVED_2:** Reserved.
5:3	0x0 RO	**PSR_LAST_STATE:** indicate last source state that PSR state machine were in (debug) 000: PSR_disabled 001: PSR_inactive 010: PSR_transition_to_active 011: PSR_active no RFB update 100: PSR_active single frame update 101: PSR_exit
2:0	0x0 RO	**PSR_CURRENT_STATE:** indicate current source state that PSR state machine are in 000: PSR_disabled 001: PSR_inactive 010: PSR_transition_to_active 011: PSR_active no RFB update 100: PSR_active single frame update 101: PSR_exit

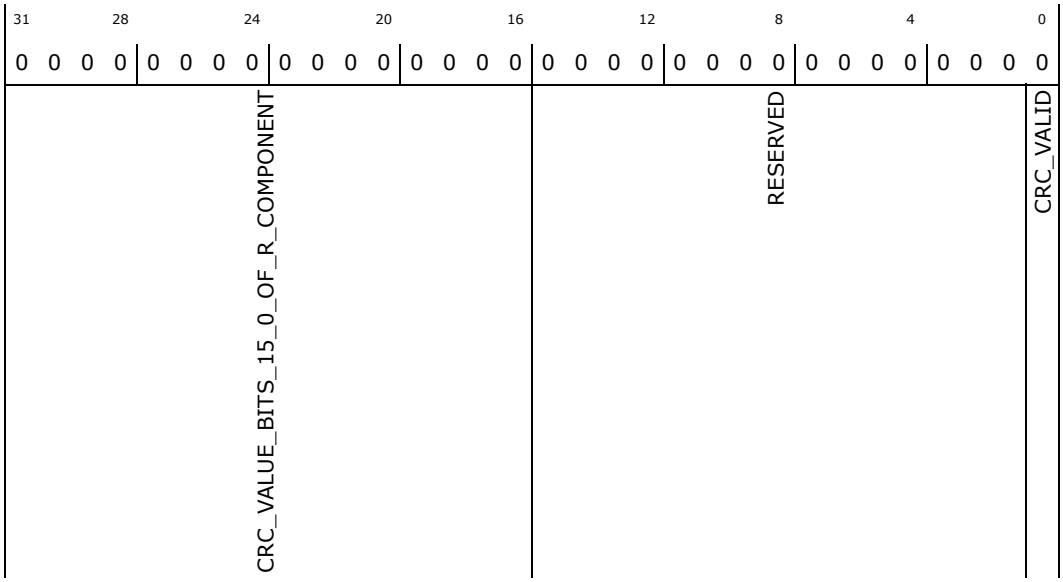
4.3.13 PSRCRC1C—Offset 63098h

Pipe C PSR CRC1 register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63098h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**CRC_VALUE_BITS_15_0_OF_R_COMPONENT:** Reserved.
15:1	0x0 RO	**RESERVED:** .
0	0x0 RO	**CRC_VALID:** CRC calculation complete and valid for previous frame.

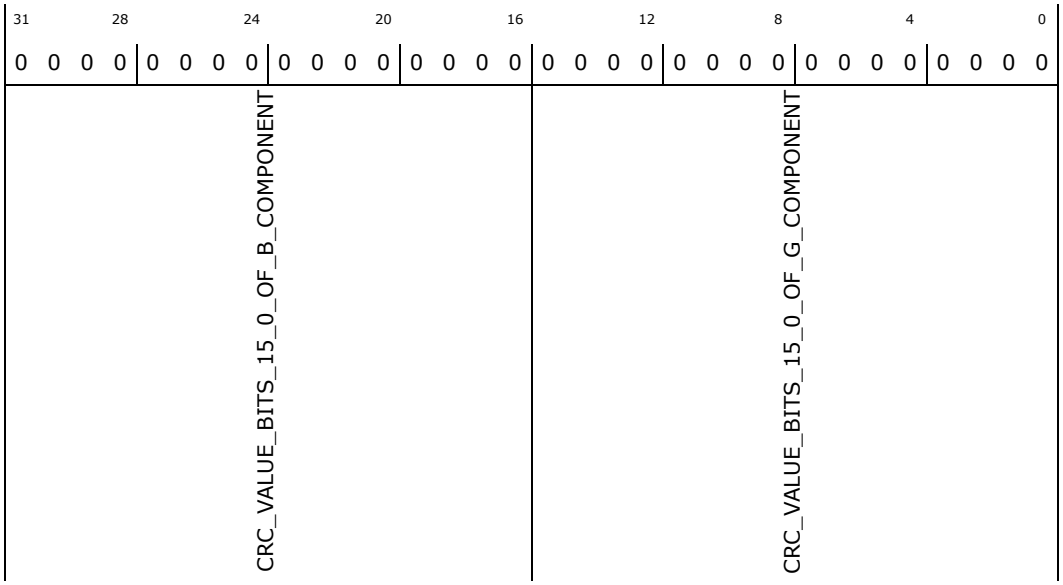
4.3.14 PSRCRC2C—Offset 6309Ch

Pipe C PSR CRC2 register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6309Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**CRC_VALUE_BITS_15_0_OF_B_COMPONENT:** Reserved.
15:0	0x0 RO	**CRC_VALUE_BITS_15_0_OF_G_COMPONENT:** Reserved.

4.3.15 VSCSDPC—Offset 630A0h

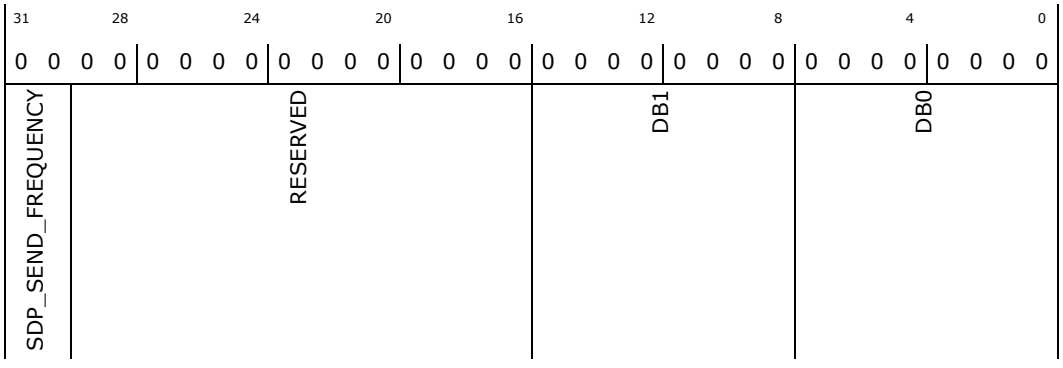
Pipe C VSC SDP register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 630A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**SDP_SEND_FREQUENCY:** 00: off, not sending 01: send one every frame 10: send once 11: reserved When PSR is enabling this field is ignored. One SDP is sent in every frame until source is in PSR active state
29:16	0x0 RO	**RESERVED:** Reserved.
15:8	0x0 RW	**DB1:** Programmed by display driver in manual mode, auto-generate by display controller in all other modes
7:0	0x0 RW	**DB0:** Bits 7:4: Stereo Interface Method Specific Parameter Bits 3:0: Stereo Interface Method Code. This field is programmed by display driver for stereo display configuration

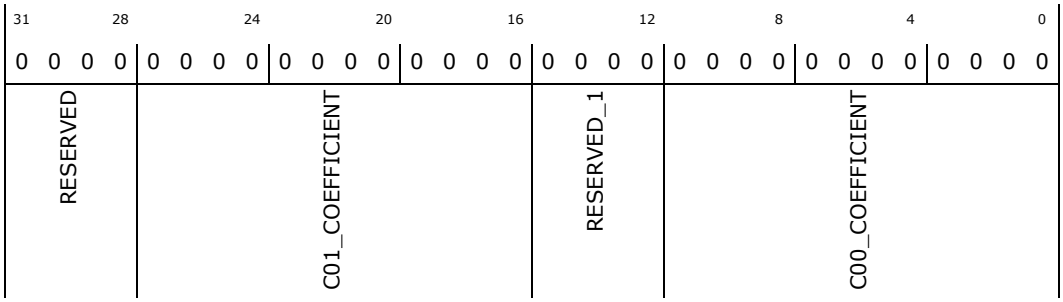
4.3.16 PIPECWIDEGAMUTCOLORCORRECTIONC01_C00COEFFICIENTS—Offset 630B0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 630B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Reserved.
27:16	0x0 RW	**C01_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
15:12	0x0 RO	**RESERVED_1:** Reserved.
11:0	0x0 RW	**C00_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

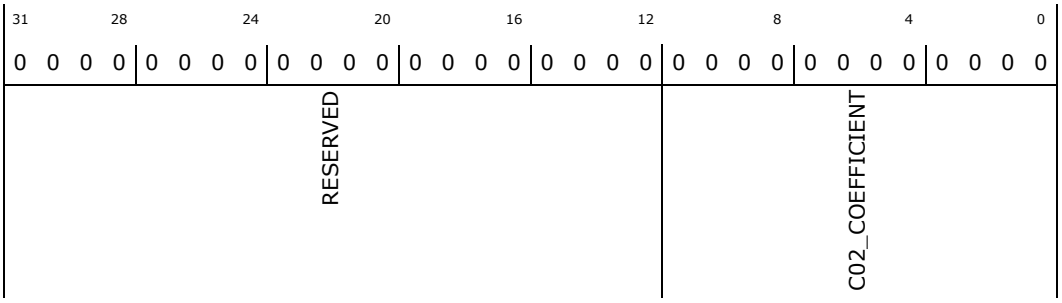
4.3.17 PIPECWIDEGAMUTCOLORCORRECTIONC02COEFFICIENT—Offset 630B4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 630B4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RESERVED:** Reserved.
11:0	0x0 RW	**C02_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

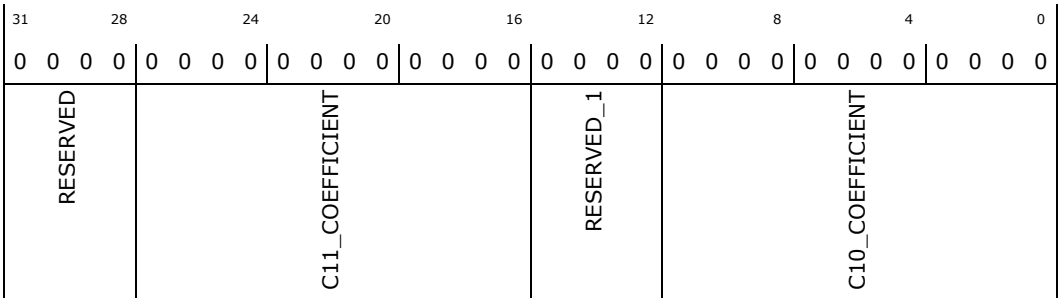
4.3.18 PIPECWIDEGAMUTCOLORCORRECTIONC11_C10COEFFICIENTS—Offset 630B8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 630B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Reserved.
27:16	0x0 RW	**C11_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0x0 RO	**RESERVED_1:** Reserved.
11:0	0x0 RW	**C10_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

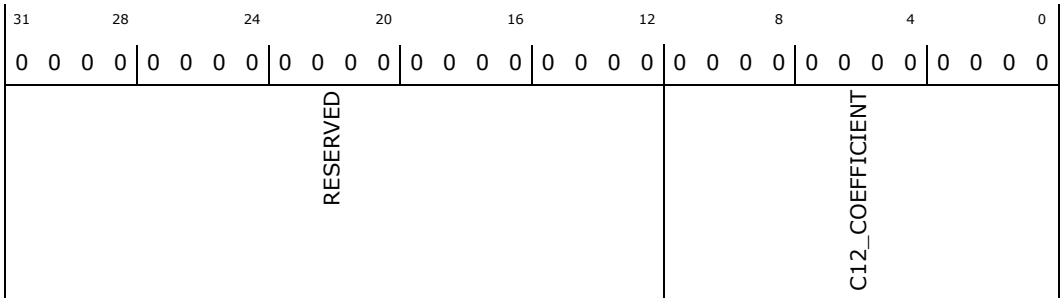
4.3.19 PIPECWIDEGAMUTCOLORCORRECTIONC12COEFFICIENT—Offset 630BCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 630BCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RESERVED:** Reserved.
11:0	0x0 RW	**C12_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

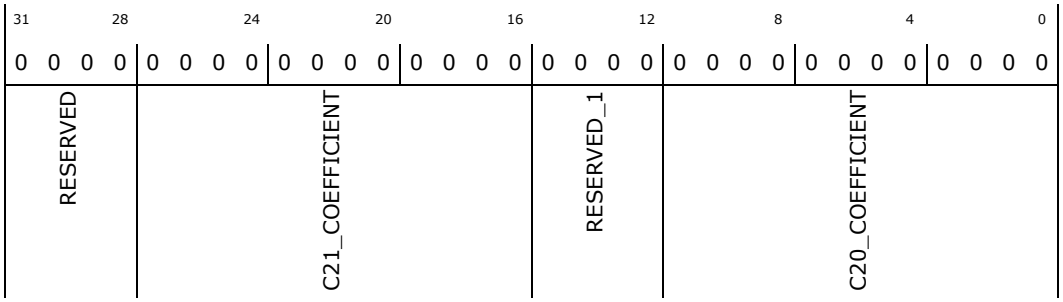
4.3.20 PIPECWIDEGAMUTCOLORCORRECTIONC21_C20COEFFICIENTS—Offset 630C0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 630C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Reserved.
27:16	0x0 RW	**C21_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.
15:12	0x0 RO	**RESERVED_1:** Reserved.
11:0	0x0 RW	**C20_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

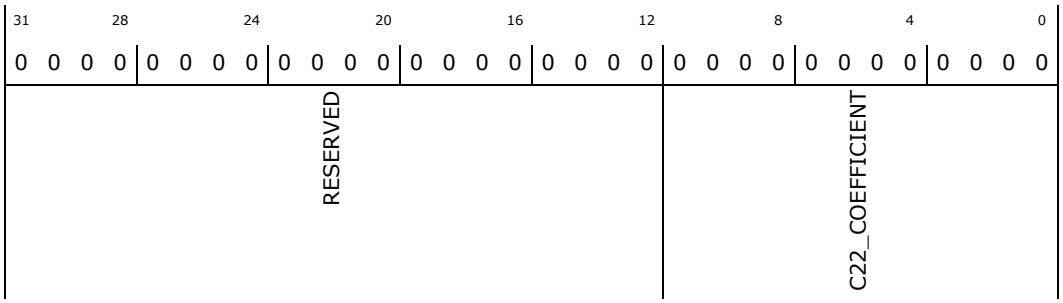
4.3.21 PIPECWIDEGAMUTCOLORCORRECTIONC22COEFFICIENT—Offset 630C4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 630C4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RESERVED:** Reserved.
11:0	0x0 RW	**C22_COEFFICIENT:** 12-bit 2 s complement signed value that is programmed for linea. The range of the value can be from -1.999 to +1.999.

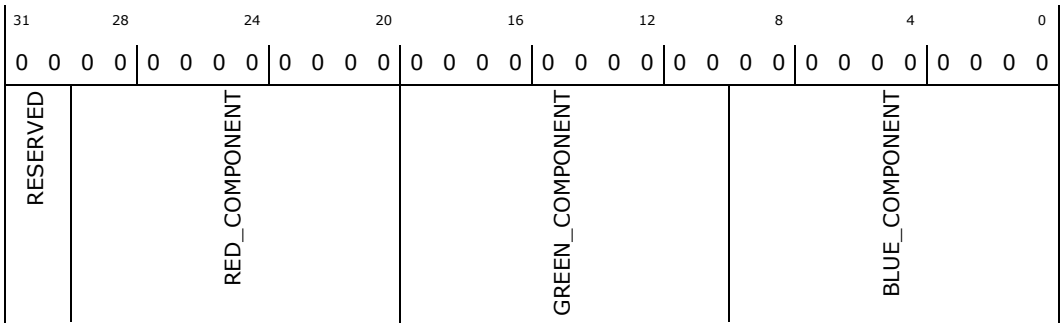
4.3.22 CANVAS_C—Offset 63A04h

Pipe C Canvas Color Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63A04h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RESERVED:** Reserved.
29:20	0x0 RO	**RED_COMPONENT:** Red Component
19:10	0x0 RO	**GREEN_COMPONENT:** GREEN Component
9:0	0x0 RO	**BLUE_COMPONENT:** BLUE Component

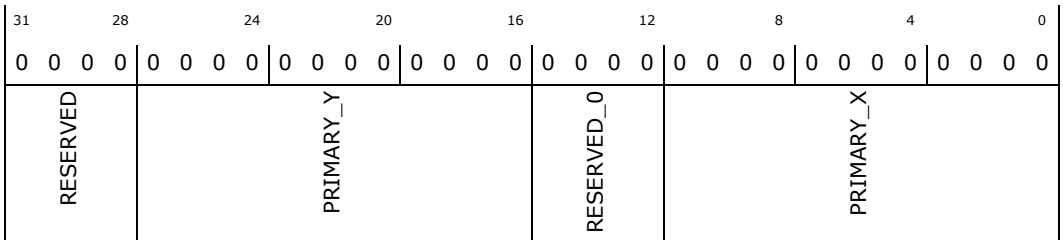
4.3.23 PRIMPOS_C—Offset 63A08h

These registers specify the screen position and size of the primary. This register is double buffered. The load register is transferred into the active register on the asserting edge of Vertical Blank for the pipe that the display is assigned. When using the primary as a secondary display, this should be set to the entire display rectangle.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 63A08h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as Zero.
27:16	0x0 RW	**Primary_Y (PRIMARY_Y):** These 12 bits specify the vertical position in lines of the primary (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the un-rotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0x0 RO	**RESERVED_0:** Write as Zero
11:0	0x0 RW	**PRIMARY_X:** These 12 bits specify the horizontal position in lines of the primary (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the end of the active video area in the un-rotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

4.3.24 PRIMSIZE_C—Offset 63A0Ch

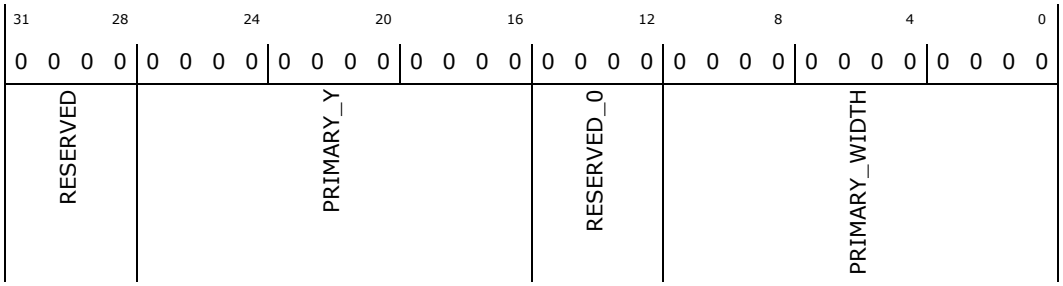
This register specifies the height and width of the primary in pixels and lines. The rectangle defined by the size and position should never exceed the boundaries of the display rectangle that the primary is assigned to.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 63A0Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as Zero.
27:16	0x0 RW	**Primary_Height (PRIMARY_Y):** This register field is used to specify the height of the primary in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0x0 RO	**RESERVED_0:** Write as Zero

Bit Range	Default & Access	Field Name (ID): Description
11:0	0x0 RW	**PRIMARY_WIDTH:** This register field is used to specify the width of the primary in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined primary rectangle must always be completely contained within the displayable area of the screen image.

4.3.25 PRIMC_CONSTANT—Offset 63A10h

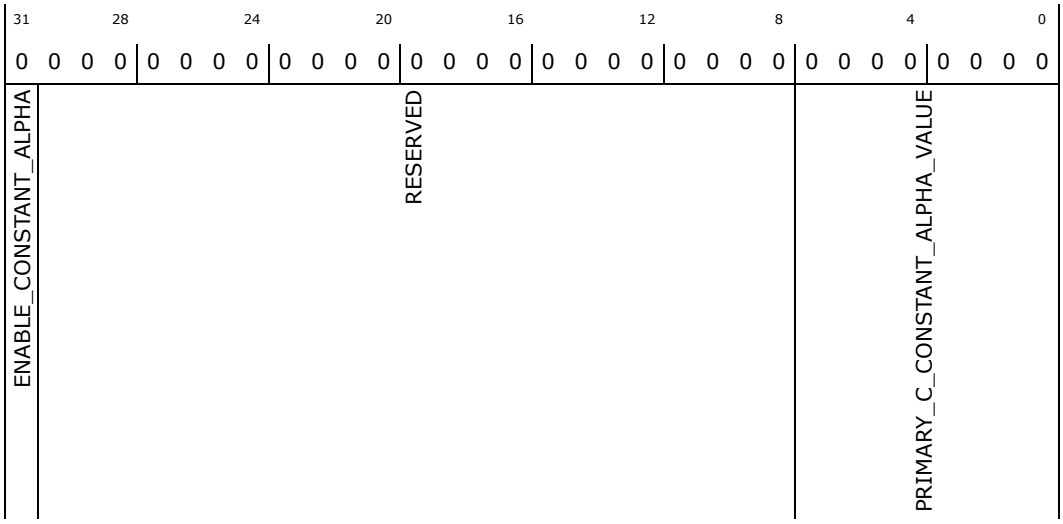
Primary C constant Alpha

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 63A10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Enable_CONSTANT_ALPHA (ENABLE_CONSTANT_ALPHA):** Primary C constant alpha provides a way to apply an alpha value to all primary pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. 0-Primary C Constant Alpha is disabled. 1-Primary C Constant Alpha Enabled
30:8	0x0 RO	**RESERVED:** RESERVED: MBZ
7:0	0x0 RW	**PRIMARY_C_CONSTATN_ALPHA_VALUE (PRIMARY_C_CONSTANT_ALPHA_VALUE):** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of primary with other surfaces.

4.3.26 DP_B—Offset 64100h

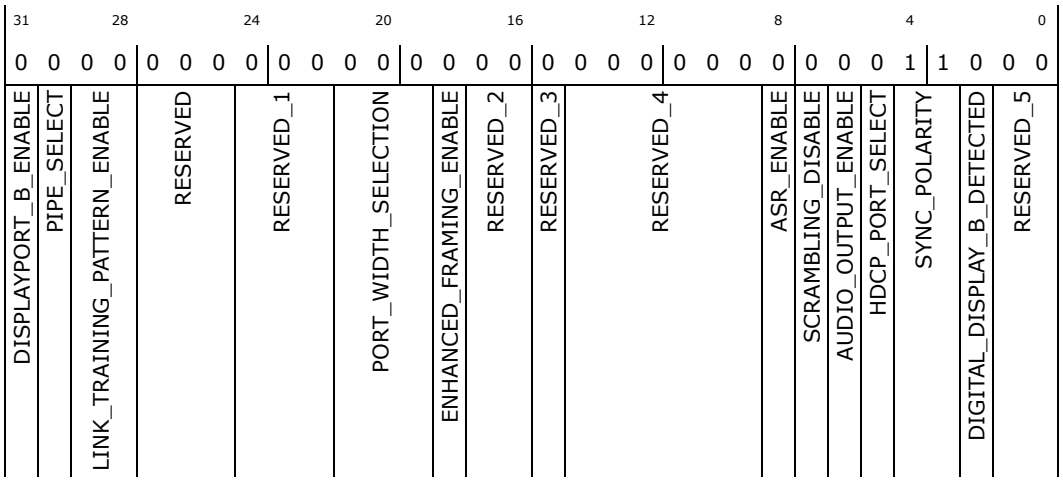
DisplayPort B Control Register Display Port B control (dprrega_b0.v ql_displayb1)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 64100h

Default: 00000018h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**DISPLAYPORT_B_ENABLE:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. 1 = Enable. This bit enables the Display Port B interface. 0 = Disable and tristates the Display Port B interface.
30	0x0 RW	**PIPE_SELECT:** This bit determines from which display pipe the source data will originate. Pipe selection takes place on the Vblank after being written 0 = Pipe A 1 = Pipe B
29:28	0x0 RW	**LINK_TRAINING_PATTERN_ENABLE:** These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns. 00 Pattern 1 enabled: Repetition of D10.2 characters Default. 01 Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2. 10 Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, at a minimum five times 11 Link not in training: Send normal pixels

Bit Range	Default & Access	Field Name (ID): Description
27:25	0x0 RO	**RESERVED:** Voltage swing level set: [DevCTG]: These bits are used for setting the voltage swing for pattern 1, defined as Vdiff_pp in the DisplayPort specification. They mirror registers in the PCI express configuration 000 0.4V (DEFAULT) 001 0.6V 010 0.8V 011 1.2V RESERVED 1xx RESERVED
24:22	0x0 RO	**RESERVED_1:** Pre-emphasis level set [DevCTG]: These bits are used for setting link pre-emphasis for pattern 2, as defined in the DisplayPort specification. They mirror registers in the PCI express configuration. 000 no pre-emphasis (default) 001 3.5dB pre-emphasis (1.5x) 010 6dB pre-emphasis (2x) 011 9.5dB pre-emphasis (3x) RESERVED 1xx RESERVED
21:19	0x0 RW	**PORT_WIDTH_SELECTION:** This bit selects the number of lanes to be enabled on the DisplayPort link. Port width selection takes place on the Vblank after being written. Port width change must be done as a part of mode set. 000 = x1 Mode (Default) 001 = x2 Mode. 010 = RESERVED 011 = x4 Mode. 1xx = RESERVED
18	0x0 RW	**ENHANCED_FRAMING_ENABLE:** This bit selects enhanced framing. It must be set when HDCP will be used invoked. 0 (Default) Enhanced framing disabled 1 Enhanced framing enabled. Locked once port is enabled. Updates when the port is disabled then re-enabled
17:16	0x0 RO	**RESERVED_2:** MBZ
15	0x0 RO	**RESERVED_3:** Port reversal [DevCTG]: Locked once port is enabled. Updates when the port is disabled then re-enabled
14:9	0x0 RO	**RESERVED_4:** MBZ
8	0x0 RW	**ASR_ENABLE:** this bit enables the Alternate Scrammbler Reset capability for eDP port to use alternate scrambler reset value of FFFEh 1 - ASR enable 0 ASR disable
7	0x0 RW	**SCRAMBLING_DISABLE:** This bit disables scrambling for this port. 0 = Scrambling enabled (Default) 1 = Scrambling disabled, no SR after initialization at loop 2 of training

Bit Range	Default & Access	Field Name (ID): Description
6	0x0 RW	**AUDIO_OUTPUT_ENABLE:** This bit enables audio on this output port. It may be enabled or disabled only when the link training is complete and set to Normal 0 = Audio output disabled 1 = Audio output enabled
5	0x0 RW	**HDCP_PORT_SELECT:** This bit directs HDCP to this port. When enabled, the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own, but must be used in conjunction with HDCP registers. 0 = (Default) No HDCP encryption on this port 1 = Enable HDCP on this port
4:3	0x3 RW	**SYNC_POLARITY:** Indicates the polarity of Hsync and Vsync. 00 = VS and HS are active low (inverted) 01 = VS is active low (inverted), HS is active high 10 = VS is active high, HS is active low (inverted) 11 = (Default) VS and HS are active high
2	0x0 RO	**DIGITAL_DISPLAY_B_DETECTED:** Read-only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port 4 (port B) data line at boot. 0 = digital display not detected during initialization (Default) 1 = digital display detected during initialization AccessType: Read Only
1:0	0x0 RO	**RESERVED_5:** MBZ

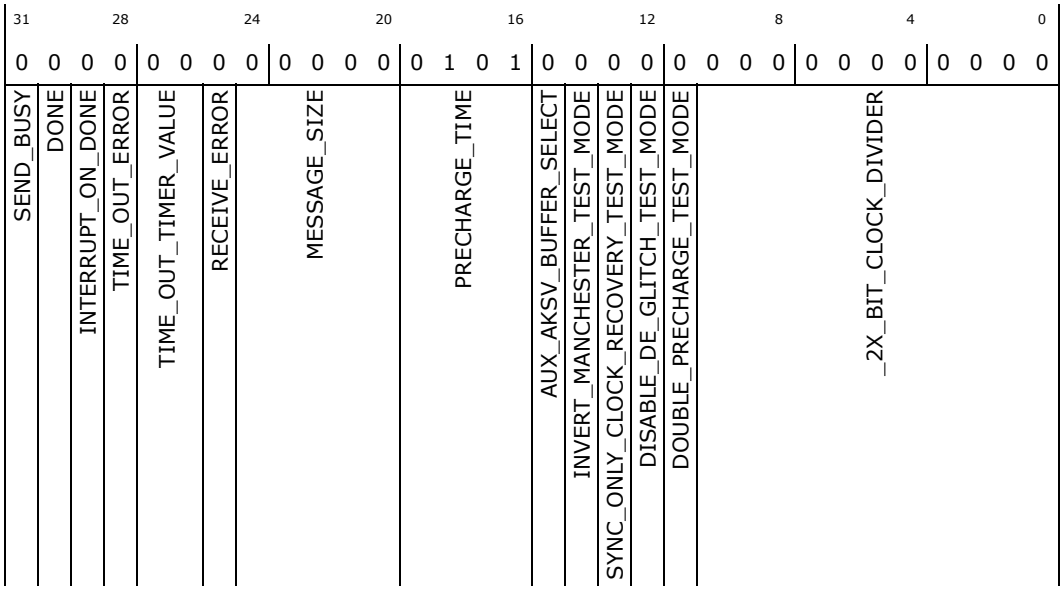
4.3.27 DPB_AUX_CH_CTL—Offset 64110h

Display Port B AUX Channel Control AuxB control (dprrega_b0.v auxb_ctl_rdback)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 64110h

Default: 00050000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SEND_BUSY:** Setting this bit to a one initiates the transaction, when read this bit will be a 1 until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. Do not write a 1 again until transaction completes. Writes of 0 will be ignored.
30	0x0 RW/1C	**DONE:** A sticky bit that indicates the transaction has completed. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
29	0x0 RW	**INTERRUPT_ON_DONE:** Enable an interrupt in the hotplug status register when the transaction completes or times out.
28	0x0 RW/1C	**TIME_OUT_ERROR:** A sticky bit that indicates the transaction has timed out. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
27:26	0x0 RW	**TIME_OUT_TIMER_VALUE:** 00: 400us (default) 01: 600us 10: 800us 11: 1600us The time count depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz.
25	0x0 RW/1C	**RECEIVE_ERROR:** A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes. SW must write a 1 to this bit to clear the event. AccessType: One to Clear

Bit Range	Default & Access	Field Name (ID): Description
24:20	0x0 RW	**MESSAGE_SIZE:** This field is used to indicate the total number bytes to transmit (including the header). It also indicates the number of bytes received in a transaction (including the header). This field is valid only only when the done bit is set and timeout or receive error has not occurred. Sync/ Stop are not part of the message or the message size. Reads of this field will give the response message size. The read value will not be valid while Busy bit 31 is asserted. Message sizes of 0 or)20 are not allowed.
19:16	0x5 RW	**PRECHARGE_TIME:** Used to determine the precharge time for the Aux Channel drivers. The value is the number of microseconds times 2. This depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz. Default is 5 decimal which gives 10us of precharge. Example: For 12us precharge, program 6 (12us/2us).
15	0x0 RW	**AUX_AKSV_BUFFER_SELECT:** This bit selects whether some of the data to be written over Display Port AUX comes from the Aksv buffer for HDCP authentication, or all from the AUX Data registers. Set this bit before initiating a transaction to write Aksv to the Display Port sink. All AUX protocol must be followed and Message Size set to 9 bytes. The first DWord transmitted will be from the AUX Data Register 1 for the header, then the DP_AUX_CH_AKSV_HI, then the last byte from DP_AUX_CH_AKSV_LO. The sink response is read back as usual from the AUX Data registers. More than one AUX channel can select to use the Aksv buffer simultaneously. 0 (Default) Use AUX Data registers for regular data transmission 1 Use Aksv Buffer for part of the data transmission.
14	0x0 RW	**INVERT_MANCHESTER_TEST_MODE:** 1 = Manchester code rising edge mid-clk signifies one (test mode) 0 = Manchester code rising edge mid-clk signifies zero (default)
13	0x0 RW	**SYNC_ONLY_CLOCK_RECOVERY_TEST_MODE:** 1 = Only recover clock during sync pattern (test mode) 0 = Recover clock during sync pattern and data phase (default)
12	0x0 RW	**DISABLE_DE_GLITCH_TEST_MODE:** 1 = Disable serial input de-glitch logic (test mode) 0 = Enable serial input de-glitch logic (default)
11	0x0 RW	**DOUBLE_PRECHARGE_TEST_MODE:** 1 = Precharge time is doubled 0 = Precharge time is as programmed
10:0	0x0 RW	**_2X_BIT_CLOCK_DIVIDER:** Used to determine the 2X bit clock the Aux Channel logic runs on. This value divides the input clock frequency down to 2X bit clock rate. The 2X bit clock rate is ideally 2MHz (0.5us). [DevCTG-A] the input clock is cdclk. the input clock is hrawclk (200MHz) Example: For 300MHz input clock and desired 2MHz 2X bit clock, program 150 (300MHz/2MHz).

4.3.28 DPB_AUX_CH_DATA1—Offset 64114h

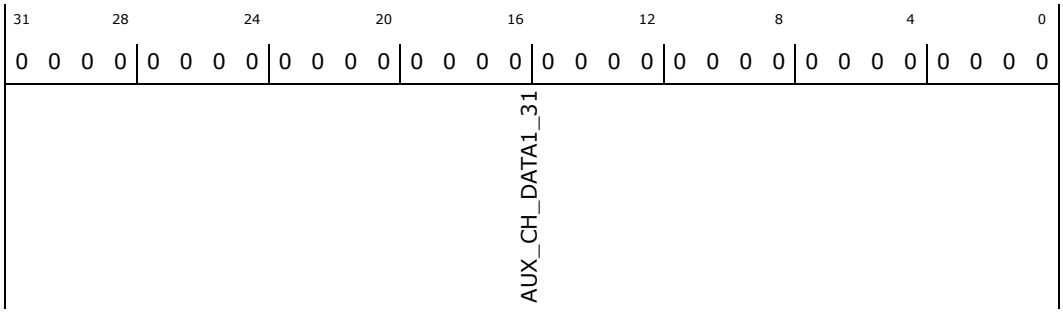
Display Port B AUX Data Register 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 64114h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**AUX_CH_DATA1_31:** 0]: The first Dword of the message. The Msbyte is transmitted first. Reads will give the response data after transaction complete.

4.3.29 DPB_AUX_CH_DATA2—Offset 64118h

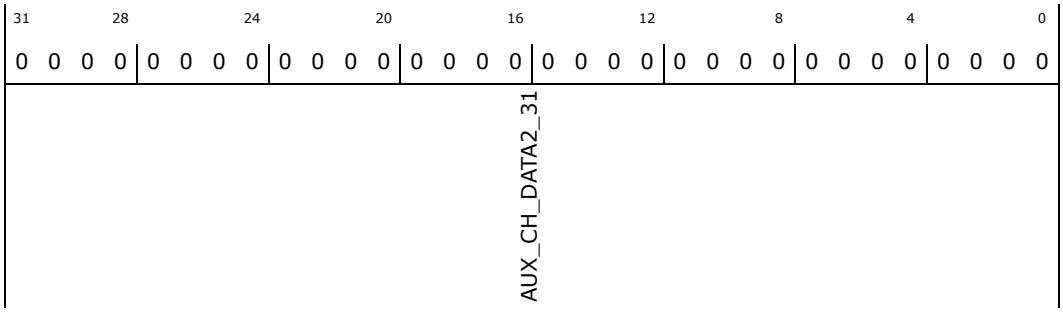
Display Port B AUX Data Register 2 AuxB Data2 (dprrega_b0.v auxb_dpr_data2, ql_auxb_d2)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 64118h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**AUX_CH_DATA2_31:** 0]: The second Dword of the message. The Msbyte is transmitted first. Only used if the message size is greater than 4. Reads will give the response data after transaction complete.

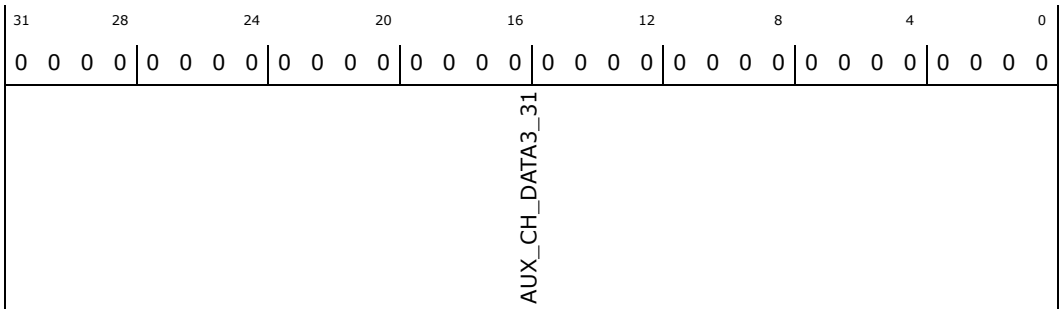
4.3.30 DPB_AUX_CH_DATA3—Offset 6411Ch

Display Port B AUX Data Register 3 AuxB Data3 (dprrega_b0.v auxb_dpr_data3, ql_auxb_d3)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6411Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**AUX_CH_DATA3_31:** 0]: The third Dword of the message. The Msbyte is transmitted first. Only used if the message size is greater than 8. Reads will give the response data after transaction complete.

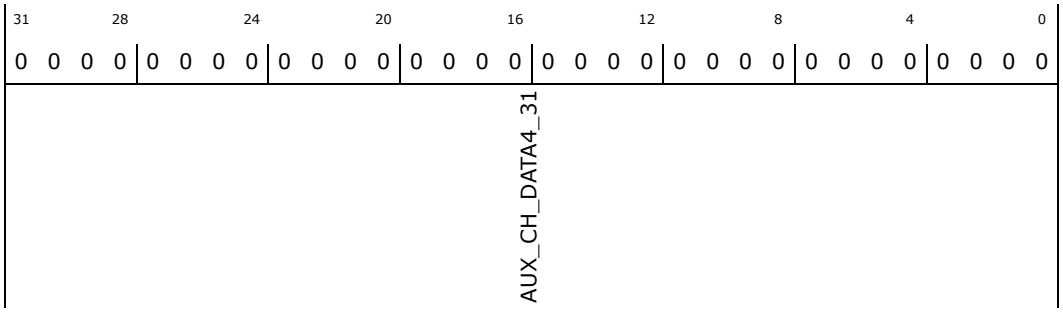
4.3.31 DPB_AUX_CH_DATA4—Offset 64120h

Display Port B AUX Data Register 4 AuxB Data4 (dprrega_b0.v auxb_dpr_data4, ql_auxb_d4)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 64120h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**AUX_CH_DATA4_31:** 0]: The fourth Dword of the message. The Msbyte is transmitted first. Only used if the message size is greater than 12. Reads will give the response data after transaction complete.

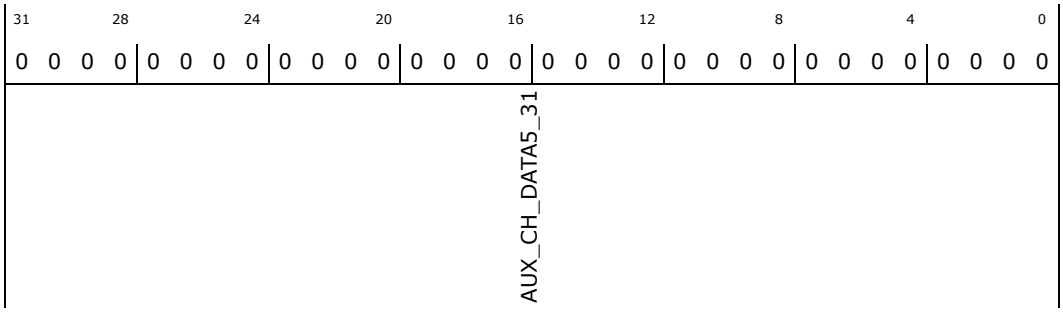
4.3.32 DPB_AUX_CH_DATA5—Offset 64124h

Display Port B AUX Data Register 5 AuxB Data5 (dprrega_b0.v auxb_dpr_data5, ql_auxb_d5)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 64124h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**AUX_CH_DATA5_31:** 0]: The fifth Dword of the message. The Msbyte is transmitted first. Only used if the message size is greater than 16. Reads will give the response data after transaction complete.

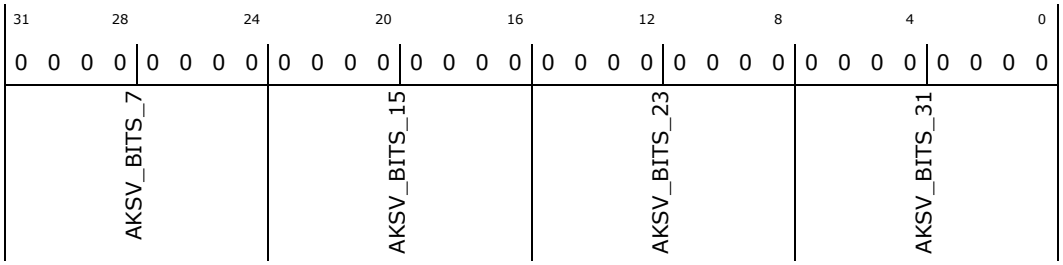
4.3.33 DP_AUX_CH_AKSV_HI—Offset 64130h

Display Port AUX Aksv Buffer High AuxB AKSV High (dprrega_b0.v dpr_aux_aksv_hi)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 64130h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 WO	**AKSV_BITS_7:** 0]
23:16	0x0 WO	**AKSV_BITS_15:** 8]
15:8	0x0 WO	**AKSV_BITS_23:** 16]
7:0	0x0 WO	**AKSV_BITS_31:** 24]

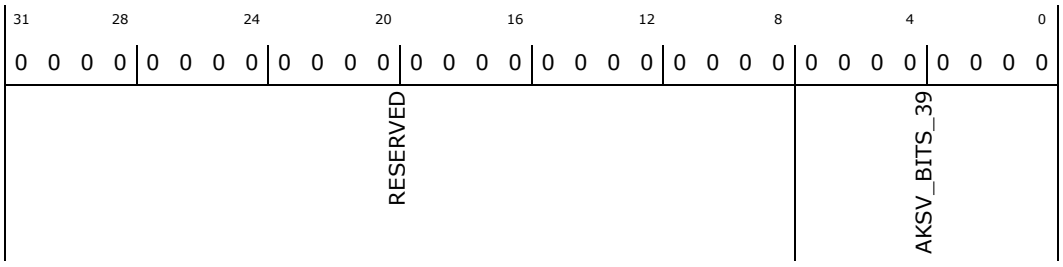
4.3.34 DP_AUX_CH_AKSV_LO—Offset 64134h

Display Port AUX Aksv Buffer Low AuxB AKSV High (dprrega_b0.v dpr_aux_aksv_lo)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 64134h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED:** MBZ
7:0	0x0 WO	**AKSV_BITS_39:** 32]

4.3.35 DPB_AUX_TST—Offset 64150h

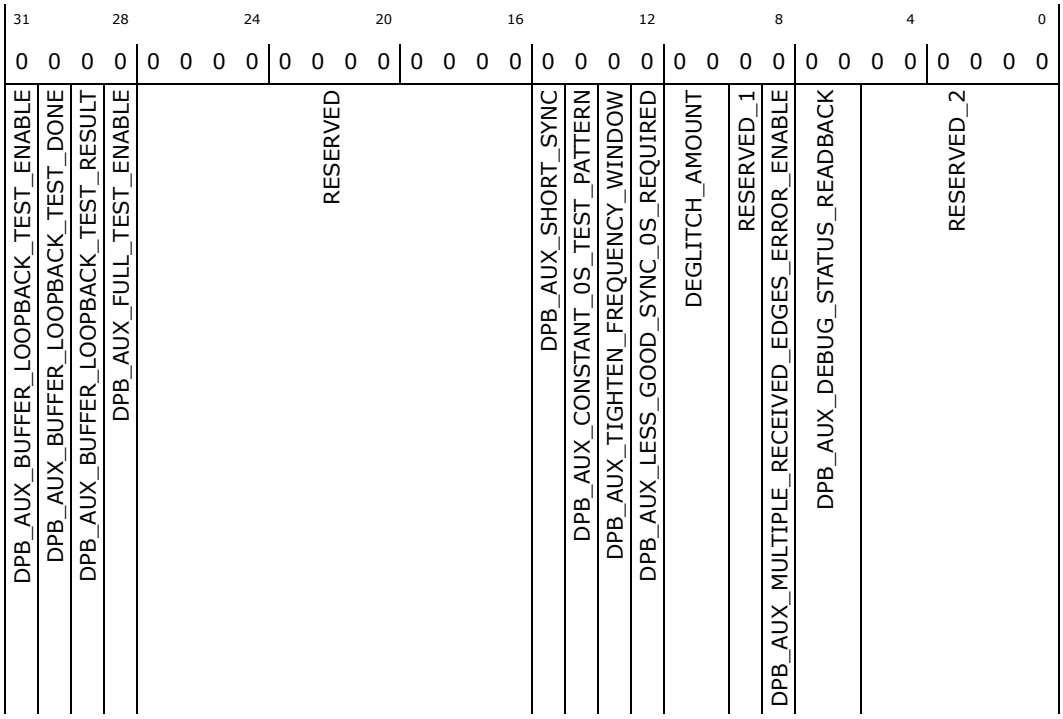
Display Port B AUX Test Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 64150h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**DPB_AUX_BUFFER_LOOPBACK_TEST_ENABLE:** Project: All Default Value: ;0b Enables test for the DPB-AUX I/O buffer. A 16 cycle clock pattern is output to the I/O buffer and compared against the looped back buffer output. The input clock is cdclk. With input clock at 512MHz the pattern will bea 1 MHz clock. It scales down with lower clock frequencies. The result is found in DP-AUX Buffer Loopback Test Result after DP-AUX Buffer Loopback Test Done is set. Clear this bit to 0 after test is done to return DP-AUX to normal operation. Loopback Test can be run simultaneously on all AUX buffers. Do not enable DP-AUX Buffer Loopback Test and DP-AUX Full Test simultaneously. Value Name Description Project 0b Disable Test disabled All 1b Enable Enable test. All

Bit Range	Default & Access	Field Name (ID): Description
30	0x0 RO	**DPB_AUX_BUFFER_LOOPBACK_TEST_DONE:** Project: All Default Value: ;0b AccessType: Read Only DPB-AUX Buffer Loopback Test has been run and completed. This is not the done for the DP-AUX Full Test. Value Name Description Project 0b Not Done Test not done. DP-AUX Buffer Loopback Test Result is not valid All 1b Done Test done. DP-AUX Buffer Loopback Test Result is now valid All
29	0x0 RO	**DPB_AUX_BUFFER_LOOPBACK_TEST_RESULT:** Project: All Default Value: ;0b AccessType: Read Only Result of the DPB-AUX Buffer Loopback Test. Value is only valid after a DP-AUX Loopback Test Done is 1. This is not the result of the DP-AUX Full Test. Value Name Description Project 0b Pass Pass All 1b Fail All
28	0x0 RW	**DPB_AUX_FULL_TEST_ENABLE:** Project: All Default Value: ;0b Enables test for the DPB-AUX core logic transmit and receive functions through the DPB-AUX and DPC-AUX buffers. DPB-AUX and DPC-AUX are interconnected through I/O buffer loopbacks. DPB-AUX is programmed as source to output a 20 byte test pattern. DPC-AUX is programmed as sink to receive the test pattern and reply with a different 20 byte test pattern. Test pattern 1 = 0xA55CC33E E770080C 0E0F0F8F CFEFF81C 3E77E3C8 Test pattern 2 = 0X183C7EE7 C381FF7F 3F1F0F07 030100EE 77CC33A5 Programming sequence: 1. Set DPB-AUX Full Test Enable to 1. 2. Program DPB_AUX_CH_DATA[1-5] with test pattern 1 to transmit as the source. 3. Program DPC_AUX_CH_DATA[1-5] with test pattern 2 to reply with as the sink. 4. Program all DPC_AUX_CH_CTL fields and set Send to 1. 5. Program all DPB_AUX_CH_CTL fields and set Send to 1. Then the test will start. Results checking sequence: 1. Poll DPB_AUX_CH_CTL for Done. To pass, Done must be set within 500us. 2. Read DPB_AUX_CH_CTL register. To pass, Timeout Error and Receive Error must be 0. 3. Read DPC_AUX_CH_CTL register. To pass, Receive Error must be 0. 4. Read DPB_AUX_CH_DATA[1-5] registers. To pass, they must contain test pattern 2. 5. Read DPC_AUX_CH_DATA[1-5] registers. To pass, they must contain test pattern 1. Clear this bit to 0 after test is done to return DP-AUX to normal operation. Test must be repeated with and without lane reversal to verify DPB-AUX buffer combinations. Only enable one DP-AUX Full Test at a time. To abort a test in progress, write the AUX_CH_CTL Send bits to 0 and Full Test Enable to 0. Value Name Description Project 0b Disable Test disabled All 1b Enable Enable test All
27:16	0x0 RO	**RESERVED:** Project: All Format:
15	0x0 RW	**DPB_AUX_SHORT_SYNC:** Project: All Output just 16 manchester 0s for sync (otherwise 26)

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**DPB_AUX_CONSTANT_0S_TEST_PATTERN:** Project: All Output neverending Manchester encoded 0s for electrical testing
13	0x0 RW	**DPB_AUX_TIGHTEN_FREQUENCY_WINDOW:** Project: All Tighten the window of allowable receive frequencies
12	0x0 RW	**DPB_AUX_LESS_GOOD_SYNC_0S_REQUIRED:** Project: All Check for only 8 good sync 0s instead of 12 when receiving
11:10	0x0 RW	**DEGLITCH_AMOUNT:** Project: All Default Value: ;0b Select clock count for deglitch Value Name Description Project 00b 50 ns 25 clocks - GMBUS type - 50ns at 500MHz cdclk All 01b 125 ns 1/4 2X bit clock divider value - 125ns All 10b 62.5 ns 1/8 2X bit clock divider value - 62.5ns All 11b 31.125 ns 1/16 2X bit clock divider value - 31.125ns All
9	0x0 RO	**RESERVED_1:** Project: All Format:
8	0x0 RW	**DPB_AUX_MULTIPLE_RECEIVED_EDGES_ERROR_ENABLE:** Project: All Default Value: ;0b Value Name Description Project 0b Okay Multiple edges in window is okay All 1b Error Multiple edges in window is an error All
7:6	0x0 RW	**DPB_AUX_DEBUG_STATUS_READBACK:** Readback of bit clock divide field gives the error type io_aux_data_syncro and aux_io_data and sm_noa[3:0] and clkregen_baddatastop and mdec_toomuchdata and mdec_notbytealign and mdec_multiedgeinwin and Input data Output data Control state machine Error - bad STOP at end of data Error - too much data Error - data not byte aligned Error - multiple edges inside of window Error - multiple edges outside of window All
5:0	0x0 RO	**RESERVED_2:** Project: All Format:

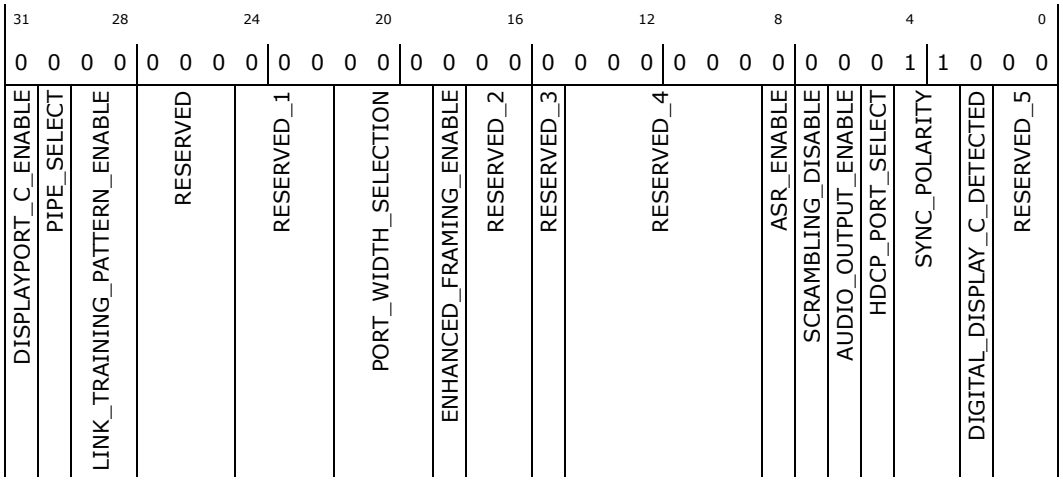
4.3.36 DP_C—Offset 64200h

Display Port C Control Register Display Port C control (dprrega_b0.v ql_displayc1)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 64200h

Default: 00000018h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**DISPLAYPORT_C_ENABLE:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and bit 6 of this register must be enabled to send audio over this port. 1 = Enable. This bit enables the Display Port C interface. 0 = Disable and tristates the Display Port C interface.
30	0x0 RW	**PIPE_SELECT:** This bit determines from which display pipe the source data will originate. Pipe selection takes place on the Vblank after being written 0 = Pipe A 1 = Pipe B
29:28	0x0 RW	**LINK_TRAINING_PATTERN_ENABLE:** These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns. 00 Pattern 1 enabled: Repetition of D10.2 characters Default. 01 Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2. 10 Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times 11 Link not in training: Send normal pixels
27:25	0x0 RO	**RESERVED:** Voltage swing level set [DevCTG]: These bits are used for setting the voltage swing for pattern 1, defined as Vdiff_pp in the DisplayPort specification. They mirror registers in the PCI express configuration. 000 0.4V (DEFAULT) 001 0.6V 010 0.8V 011 1.2V RESERVED 1xx RESERVED

Bit Range	Default & Access	Field Name (ID): Description
24:22	0x0 RO	**RESERVED_1:** Pre-emphasis level set [DevCTG]: These bits are used for setting link pre-emphasis for pattern 2, as defined in the DisplayPort specification. They mirror registers in the PCI express configuration. 000 no pre-emphasis (default) 001 3.5dB pre-emphasis (1.5x) 010 6dB pre-emphasis (2x) 011 9.5dB pre-emphasis (3x) RESERVED 1xx RESERVED
21:19	0x0 RW	**PORT_WIDTH_SELECTION:** This bit selects the number of lanes to be enabled on the DisplayPort link. Port width selection takes place on the Vblank after being written. Port width change must be done as a part of mode set. 000 = x1 Mode (Default) 001 = x2 Mode. 010 = RESERVED 011 = x4 Mode. 1xx = RESERVED
18	0x0 RW	**ENHANCED_FRAMING_ENABLE:** This bit selects enhanced framing. It must be set when HDCP will be used invoked. 0 (Default) Enhanced framing disabled 1 Enhanced framing enabled. Locked once port is enabled. Updates when the port is disabled then re-enabled
17:16	0x0 RO	**RESERVED_2:** MBZ
15	0x0 RO	**RESERVED_3:** Port reversal [DevCTG]: Locked once port is enabled. Updates when the port is disabled then re-enabled
14:9	0x0 RO	**RESERVED_4:** MBZ
8	0x0 RW	**ASR_ENABLE:** this bit enables the Alternate Scrammbler Reset capability for eDP port to use alternate scrambler reset value of FFFEh 1 - ASR enable 0 ASR disable
7	0x0 RW	**SCRAMBLING_DISABLE:** This bit disables scrambling for this port. 0 = Scrambling enabled (Default) 1 = Scrambling disabled, no SR after initialization at loop 2 of training
6	0x0 RW	**AUDIO_OUTPUT_ENABLE:** This bit enables audio on this output port. It may be enabled or disabled only when the link training is complete and set to Normal 0 = Audio output disabled 1 = Audio output enabled
5	0x0 RW	**HDCP_PORT_SELECT:** This bit directs HDCP to this port. When enabled, the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own, but must be used in conjunction with HDCP registers. 0 = (Default) No HDCP encryption on this port 1 = Enable HDCP on this port

Bit Range	Default & Access	Field Name (ID): Description
4:3	0x3 RW	**SYNC_POLARITY:** Indicates the polarity of Hsync and Vsync. 00 = VS and HS are active low (inverted) 01 = VS is active low (inverted), HS is active high 10 = VS is active high, HS is active low (inverted) 11 = (Default) VS and HS are active high
2	0x0 RO	**DIGITAL_DISPLAY_C_DETECTED:** Read-only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port (sDVO B/C) data line at boot. 0 = digital display not detected during initialization (Default) 1 = digital display detected during initialization AccessType: Read only
1:0	0x0 RO	**RESERVED_5:** MBZ

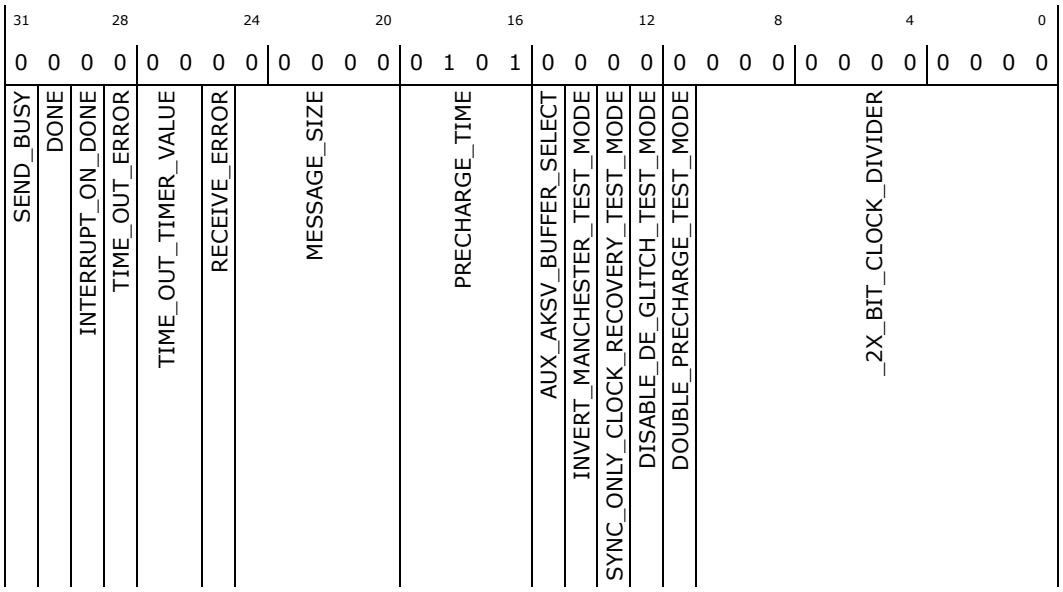
4.3.37 DPC_AUX_CH_CTL—Offset 64210h

Display Port C AUX Channel Control [DevCTG] AuxC Data1 (dprrega_b0.v auxc_dpr_data1, ql_auxc_d1)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 64210h

Default: 00050000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SEND_BUSY:** Setting this bit to a one initiates the transaction, when read this bit will be a 1 until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. Do not write a 1 again until transaction completes. Writes of 0 will be ignored.
30	0x0 RW/1C	**DONE:** A sticky bit that indicates the transaction has completed. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
29	0x0 RW	**INTERRUPT_ON_DONE:** Enable an interrupt in the hotplug status register when the transaction completes or times out.
28	0x0 RW/1C	**TIME_OUT_ERROR:** A sticky bit that indicates the transaction has timed out. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
27:26	0x0 RW	**TIME_OUT_TIMER_VALUE:** 00: 400us (default) 01: 600us 10: 800us 11: 1600us The time count depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz.
25	0x0 RW/1C	**RECEIVE_ERROR:** A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
24:20	0x0 RW	**MESSAGE_SIZE:** This field is used to indicate the total number bytes to transmit (including the header). It also indicates the number of bytes received in a transaction (including the header). This field is valid only only when the done bit is set and timeout or receive error has not occurred. Sync/ Stop are not part of the message or the message size. Reads of this field will give the response message size. The read value will not be valid while Busy bit 31 is asserted. Message sizes of 0 or)20 are not allowed.
19:16	0x5 RW	**PRECHARGE_TIME:** Used to determine the precharge time for the Aux Channel drivers. The value is the number of microseconds times 2. This depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz. Default is 5 decimal which gives 10us of precharge. Example: For 12us precharge, program 6 (12us/2us).
15	0x0 RW	**AUX_AKSV_BUFFER_SELECT:** This bit selects whether some of the data to be written over Display Port AUX comes from the Aksv buffer for HDCP authentication, or all from the AUX Data registers. Set this bit before initiating a transaction to write Aksv to the Display Port sink. All AUX protocol must be followed and Message Size set to 9 bytes. The first DWord transmitted will be from the AUX Data Register 1 for the header, then the DP_AUX_CH_AKSV_HI, then the last byte from DP_AUX_CH_AKSV_LO. The sink response is read back as usual from the AUX Data registers. More than one AUX channel can select to use the Aksv buffer simultaneously. 0 (Default) Use AUX Data registers for regular data transmission 1 Use Aksv Buffer for part of the data transmission.

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**INVERT_MANCHESTER_TEST_MODE:** 1 = Manchester code rising edge mid-clk signifies one (test mode) 0 = Manchester code rising edge mid-clk signifies zero (default)
13	0x0 RW	**SYNC_ONLY_CLOCK_RECOVERY_TEST_MODE:** 1 = Only recover clock during sync pattern (test mode) 0 = Recover clock during sync pattern and data phase (default)
12	0x0 RW	**DISABLE_DE_GLITCH_TEST_MODE:** 1 = Disable serial input de-glitch logic (test mode) 0 = Enable serial input de-glitch logic (default)
11	0x0 RW	**DOUBLE_PRECHARGE_TEST_MODE:** 1 = Precharge time is doubled 0 = Precharge time is as programmed
10:0	0x0 RW	**_2X_BIT_CLOCK_DIVIDER:** Used to determine the 2X bit clock the Aux Channel logic runs on. This value divides the input clock frequency down to 2X bit clock rate. The 2X bit clock rate is ideally 2MHz (0.5us). [DevCTG-A] the input clock is cdclk. [DevCTG-B] the input clock is hrawclk. Example: For 300MHz input clock and desired 2MHz 2X bit clock, program 150 (300MHz/2MHz).

4.3.38 DPC_AUX_CH_DATA1—Offset 64214h

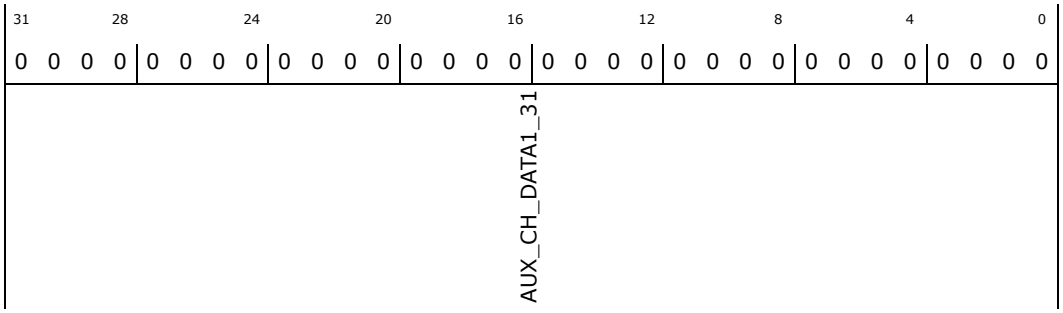
Display Port C AUX Data Register 1 AuxC Data1 (dprrega_b0.v auxc_dpr_data1, ql_auxc_d1)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 64214h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**AUX_CH_DATA1_31:** 0]: The first DWord of the message. The MSbyte is transmitted first. Reads will give the response data after transaction complete.

4.3.39 DPC_AUX_CH_DATA2—Offset 64218h

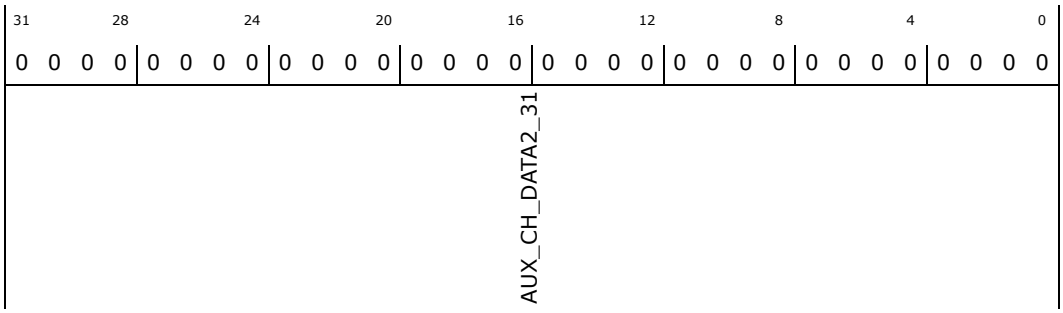
Display Port C AUX Data Register 2 AuxC Data2 (dprrega_b0.v auxc_dpr_data2, ql_auxc_d2)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 64218h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**AUX_CH_DATA2_31:** 0]: The second DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 4. Reads will give the response data after transaction complete.

4.3.40 DPC_AUX_CH_DATA3—Offset 6421Ch

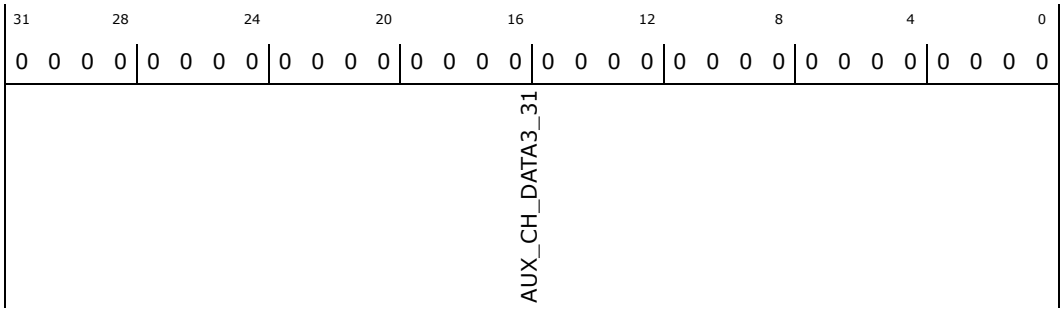
Display Port C AUX Data Register 3 AuxC Data3 (dprrega_b0.v auxc_dpr_data3, ql_auxc_d3)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6421Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**AUX_CH_DATA3_31:** 0]: The third DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 8. Reads will give the response data after transaction complete.

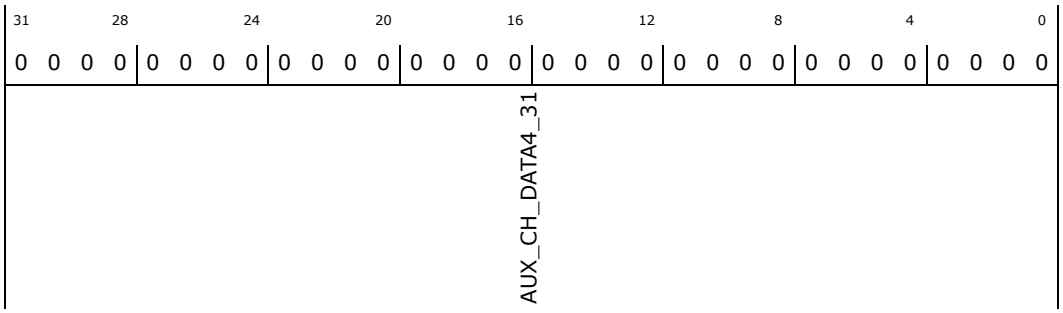
4.3.41 DPC_AUX_CH_DATA4—Offset 64220h

Display Port C AUX Data Register 4 AuxC Data4 (dprrega_b0.v auxc_dpr_data4, ql_auxc_d4)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 64220h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**AUX_CH_DATA4_31:** 0]: The fourth DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 12. Reads will give the response data after transaction complete.

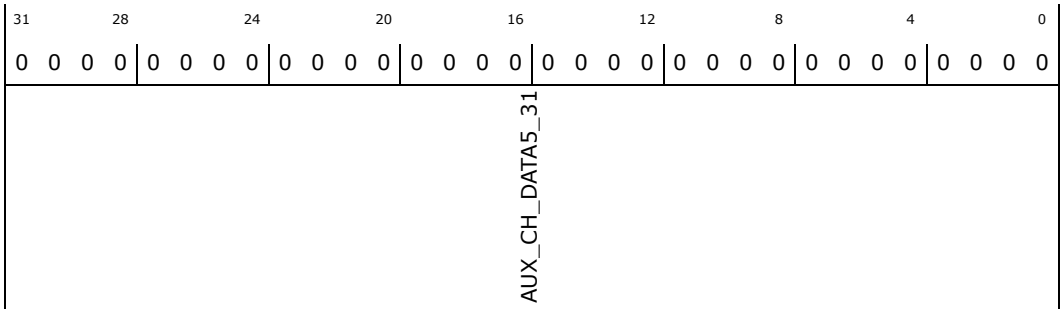
4.3.42 DPC_AUX_CH_DATA5—Offset 64224h

Display Port C AUX Data Register 5 AuxC Data5 (dprrega_b0.v auxc_dpr_data5, ql_auxc_d5)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 64224h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**AUX_CH_DATA5_31:** 0]: The fifth DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 16. Reads will give the response data after transaction complete.

4.3.43 DPC_AUX_TST—Offset 64228h

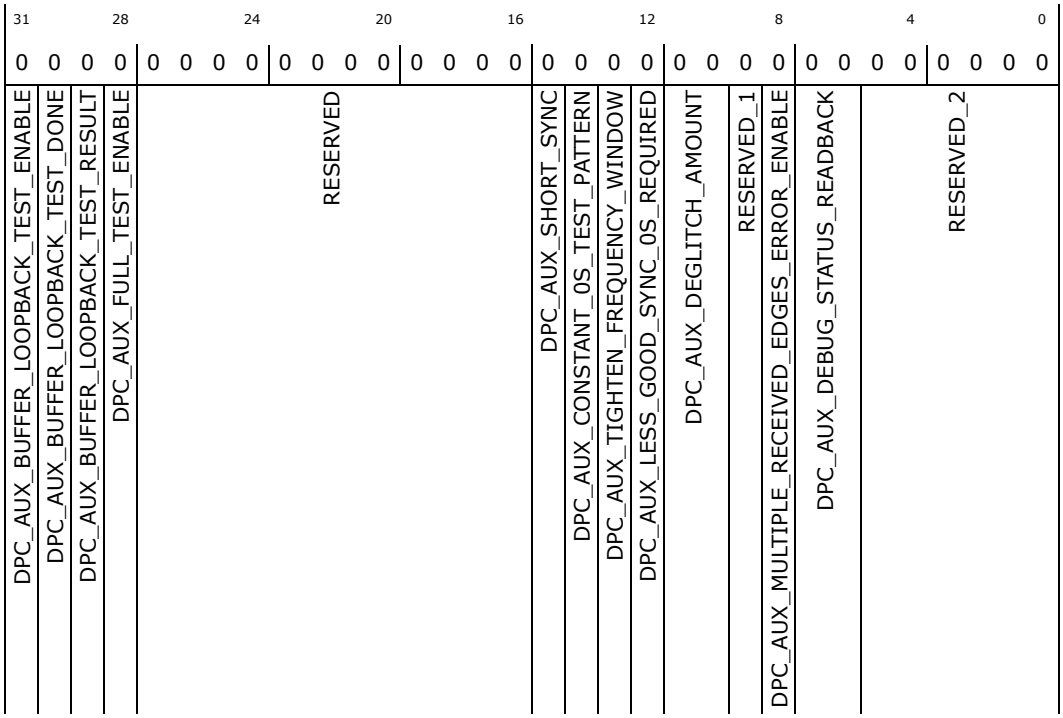
Display Port C AUX Test Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 64228h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**DPC_AUX_BUFFER_LOOPBACK_TEST_ENABLE:** Project: All Default Value: ;0b Refer DPB description. Value Name Description Project 0b Disable Test disabled All 1b Enable Enable test. All
30	0x0 RO	**DPC_AUX_BUFFER_LOOPBACK_TEST_DONE:** Project: All Default Value: ;0b AccessType: Read Only Refer DPB description. Value Name Description Project 0b Not Done Test not done. DP-AUX Buffer Loopback Test Result is not valid All 1b Done Test done. DP-AUX Buffer Loopback Test Result is now valid All
29	0x0 RO	**DPC_AUX_BUFFER_LOOPBACK_TEST_RESULT:** Project: All Default Value: ;0b AccessType: Read Only Refer description for DPB-AUX Buffer Loopback Test Result Value Name Description Project 0b Pass Pass All 1b Fail Fail All
28	0x0 RW	**DPC_AUX_FULL_TEST_ENABLE:** Project: All Default Value: ;0b Refer DPB description. Value Name Description Project 0b Disable Test disabled All 1b Enable Enable test All
27:16	0x0 RO	**RESERVED:** Project: All Format:
15	0x0 RW	**DPC_AUX_SHORT_SYNC:** Project: All Refer DPB description.
14	0x0 RW	**DPC_AUX_CONSTANT_0S_TEST_PATTERN:** Project: All Refer DPB description.
13	0x0 RW	**DPC_AUX_TIGHTEN_FREQUENCY_WINDOW:** Project: All Refer DPB description.
12	0x0 RW	**DPC_AUX_LESS_GOOD_SYNC_0S_REQUIRED:** Project: All Refer DPB description.
11:10	0x0 RW	**DPC_AUX_DEGLITCH_AMOUNT:** Project: All Default Value: ;0b Refer DPB description. Value Name Description Project 00b 50 ns 25 clocks - GMBUS type - 50ns at 500MHz cdclk All 01b 125 ns 1/4 2X bit clock divider value - 125ns All 10b 62.5 ns 1/8 2X bit clock divider value - 62.5ns All 11b 31.125 ns 1/16 2X bit clock divider value - 31.125ns All
9	0x0 RO	**RESERVED_1:** Project: All Format:

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**DPC_AUX_MULTIPLE_RECEIVED_EDGES_ERROR_ENABLE:** Project: All Default Value: ;0b Value Name Description Project 0b Okay Multiple edges in window is okay All 1b Error Multiple edges in window is an error All
7:6	0x0 RW	**DPC_AUX_DEBUG_STATUS_READBACK:** Project: All Default Value: ;0b Value Name Description Project 00b Program Readback of bit clock divide field gives the programmed clock frequency All 01b Recover Readback of bit clock divide field gives the recovered clock frequency All 10b Error Type Readback of bit clock divide field gives the error type All
5:0	0x0 RO	**RESERVED_2:** Project: All Format:

4.3.44 DP_D—Offset 64300h

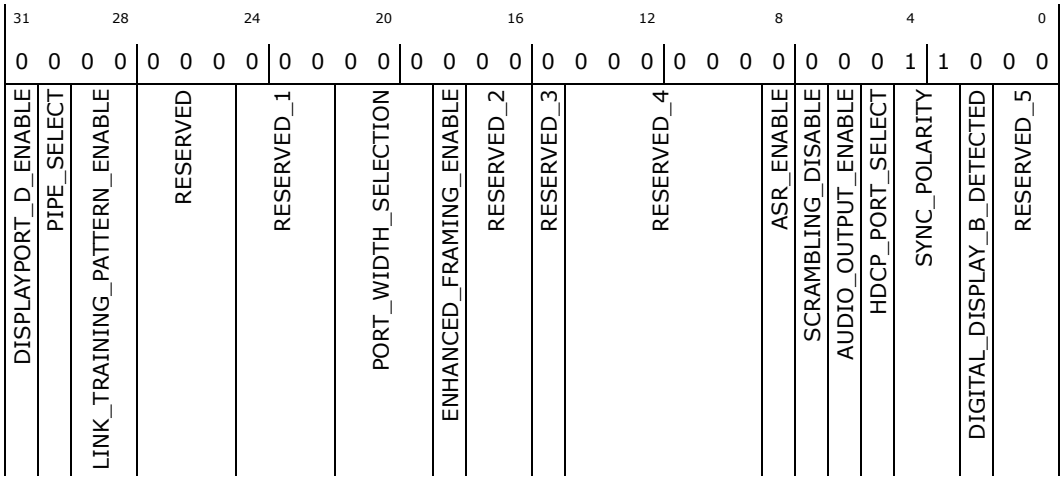
DisplayPort D Control Register Display Port D control (dprrega_b0.v ql_displayb1)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 64300h

Default: 00000018h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**DISPLAYPORT_D_ENABLE:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. 1 = Enable. This bit enables the Display Port D interface. 0 = Disable and tristates the Display Port D interface.

Bit Range	Default & Access	Field Name (ID): Description
30	0x0 RW	**PIPE_SELECT:** This bit determines from which display pipe the source data will originate. Pipe selection takes place on the Vblank after being written 0 = Pipe A 1 = Pipe B
29:28	0x0 RW	**LINK_TRAINING_PATTERN_ENABLE:** These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns. 00 Pattern 1 enabled: Repetition of D10.2 characters Default. 01 Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2. 10 Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times 11 Link not in training: Send normal pixels
27:25	0x0 RO	**RESERVED:** Voltage swing level set: [DevCTG]: These bits are used for setting the voltage swing for pattern 1, defined as Vdiff_pp in the DisplayPort specification. They mirror registers in the PCI express configuration 000 0.4V (DEFAULT) 001 0.6V 010 0.8V 011 1.2V RESERVED 1xx RESERVED
24:22	0x0 RO	**RESERVED_1:** Pre-emphasis level set [DevCTG]: These bits are used for setting link pre-emphasis for pattern 2, as defined in the DisplayPort specification. They mirror registers in the PCI express configuration. 000 no pre-emphasis (default) 001 3.5dB pre-emphasis (1.5x) 010 6dB pre-emphasis (2x) 011 9.5dB pre-emphasis (3x) RESERVED 1xx RESERVED
21:19	0x0 RW	**PORT_WIDTH_SELECTION:** This bit selects the number of lanes to be enabled on the DisplayPort link. Port width selection takes place on the Vblank after being written. Port width change must be done as a part of mode set. 000 = x1 Mode (Default) 001 = x2 Mode. 010 = RESERVED 011 = x4 Mode. 1xx = RESERVED
18	0x0 RW	**ENHANCED_FRAMING_ENABLE:** This bit selects enhanced framing. It must be set when HDCP will be used invoked. 0 (Default) Enhanced framing disabled 1 Enhanced framing enabled. Locked once port is enabled. Updates when the port is disabled then re-enabled
17:16	0x0 RO	**RESERVED_2:** MBZ

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**RESERVED_3:** Port reversal [DevCTG]: Locked once port is enabled. Updates when the port is disabled then re-enabled
14:9	0x0 RO	**RESERVED_4:** MBZ
8	0x0 RW	**ASR_ENABLE:** this bit enables the Alternate Scrammbler Reset capability for eDP port to use alternate scrambler reset value of FFFEh 1 - ASR enable 0 ASR disable
7	0x0 RW	**SCRAMBLING_DISABLE:** This bit disables scrambling for this port. 0 = Scrambling enabled (Default) 1 = Scrambling disabled, no SR after initialization at loop 2 of training
6	0x0 RW	**AUDIO_OUTPUT_ENABLE:** This bit enables audio on this output port. It may be enabled or disabled only when the link training is complete and set to Normal 0 = Audio output disabled 1 = Audio output enabled
5	0x0 RW	**HDCP_PORT_SELECT:** This bit directs HDCP to this port. When enabled, the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own, but must be used in conjunction with HDCP registers. 0 = (Default) No HDCP encryption on this port 1 = Enable HDCP on this port
4:3	0x3 RW	**SYNC_POLARITY:** Indicates the polarity of Hsync and Vsync. 00 = VS and HS are active low (inverted) 01 = VS is active low (inverted), HS is active high 10 = VS is active high, HS is active low (inverted) 11 = (Default) VS and HS are active high
2	0x0 RO	**DIGITAL_DISPLAY_D_DETECTED (DIGITAL_DISPLAY_B_DETECTED):** Read-only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port 4 (port D) data line at boot. 0 = digital display not detected during initialization (Default) 1 = digital display detected during initialization AccessType: Read Only
1:0	0x0 RO	**RESERVED_5:** MBZ

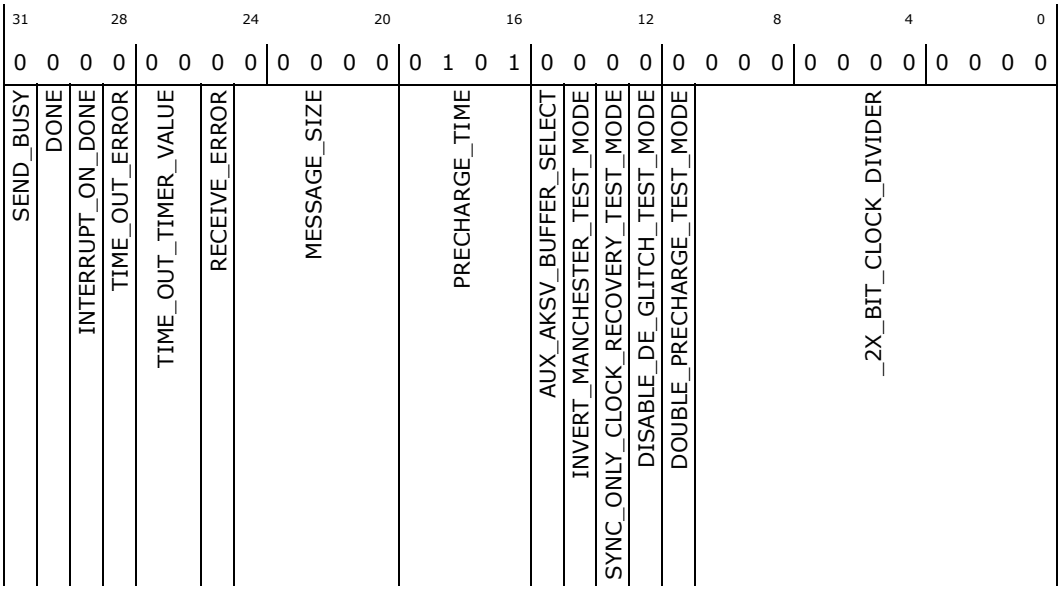
4.3.45 DPD_AUX_CH_CTL—Offset 64310h

Display Port D AUX Channel Control [DevCTG] AuxD Data1 (dprrega_b0.v auxd_dpr_data1, ql_auxc_d1)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 64310h

Default: 00050000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SEND_BUSY:** Setting this bit to a one initiates the transaction, when read this bit will be a 1 until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. Do not write a 1 again until transaction completes. Writes of 0 will be ignored.
30	0x0 RW/1C	**DONE:** A sticky bit that indicates the transaction has completed. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
29	0x0 RW	**INTERRUPT_ON_DONE:** Enable an interrupt in the hotplug status register when the transaction completes or times out.
28	0x0 RW/1C	**TIME_OUT_ERROR:** A sticky bit that indicates the transaction has timed out. SW must write a 1 to this bit to clear the event. AccessType: One to Clear
27:26	0x0 RW	**TIME_OUT_TIMER_VALUE:** 00: 400us (default) 01: 600us 10: 800us 11: 1600us The time count depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz.
25	0x0 RW/1C	**RECEIVE_ERROR:** A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes. SW must write a 1 to this bit to clear the event. AccessType: One to Clear

Bit Range	Default & Access	Field Name (ID): Description
24:20	0x0 RW	**MESSAGE_SIZE:** This field is used to indicate the total number bytes to transmit (including the header). It also indicates the number of bytes received in a transaction (including the header). This field is valid only only when the done bit is set and timeout or receive error has not occurred. Sync/ Stop are not part of the message or the message size. Reads of this field will give the response message size. The read value will not be valid while Busy bit 31 is asserted. Message sizes of 0 or)20 are not allowed.
19:16	0x5 RW	**PRECHARGE_TIME:** Used to determine the precharge time for the Aux Channel drivers. The value is the number of microseconds times 2. This depends on the 2X bit clock divider (bits 10:0) being programmed for 2MHz. Default is 5 decimal which gives 10us of precharge. Example: For 12us precharge, program 6 (12us/2us).
15	0x0 RW	**AUX_AKSV_BUFFER_SELECT:** This bit selects whether some of the data to be written over Display Port AUX comes from the Aksv buffer for HDCP authentication, or all from the AUX Data registers. Set this bit before initiating a transaction to write Aksv to the Display Port sink. All AUX protocol must be followed and Message Size set to 9 bytes. The first DWord transmitted will be from the AUX Data Register 1 for the header, then the DP_AUX_CH_AKSV_HI, then the last byte from DP_AUX_CH_AKSV_LO. The sink response is read back as usual from the AUX Data registers. More than one AUX channel can select to use the Aksv buffer simultaneously. 0 (Default) Use AUX Data registers for regular data transmission 1 Use Aksv Buffer for part of the data transmission.
14	0x0 RW	**INVERT_MANCHESTER_TEST_MODE:** 1 = Manchester code rising edge mid-clk signifies one (test mode) 0 = Manchester code rising edge mid-clk signifies zero (default)
13	0x0 RW	**SYNC_ONLY_CLOCK_RECOVERY_TEST_MODE:** 1 = Only recover clock during sync pattern (test mode) 0 = Recover clock during sync pattern and data phase (default)
12	0x0 RW	**DISABLE_DE_GLITCH_TEST_MODE:** 1 = Disable serial input de-glitch logic (test mode) 0 = Enable serial input de-glitch logic (default)
11	0x0 RW	**DOUBLE_PRECHARGE_TEST_MODE:** 1 = Precharge time is doubled 0 = Precharge time is as programmed
10:0	0x0 RW	**_2X_BIT_CLOCK_DIVIDER:** Used to determine the 2X bit clock the Aux Channel logic runs on. This value divides the input clock frequency down to 2X bit clock rate. The 2X bit clock rate is ideally 2MHz (0.5us). [DevCTG-A] the input clock is cdclk. [DevCTG-B] the input clock is hrawclk. Example: For 300MHz input clock and desired 2MHz 2X bit clock, program 150 (300MHz/2MHz).

4.3.46 DPD_AUX_CH_DATA1—Offset 64314h

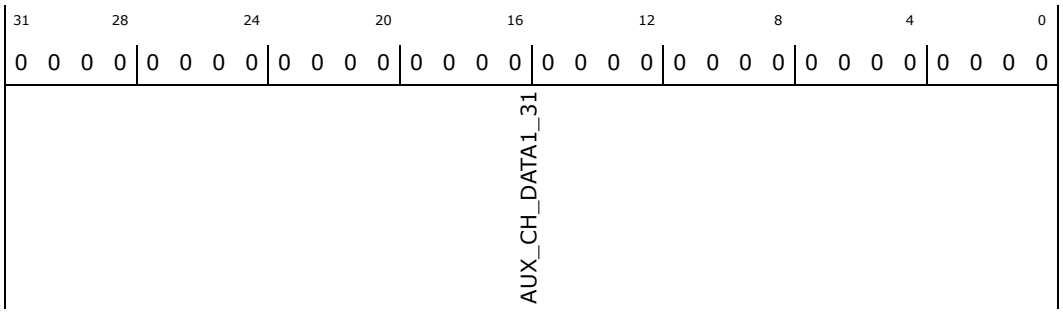
Display Port D AUX Data Register 1 AuxC Data1 (dprrega_b0.v auxc_dpr_data1, ql_auxc_d1)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 64314h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**AUX_CH_DATA1_31:** 0]: The first DWord of the message. The MSbyte is transmitted first. Reads will give the response data after transaction complete.

4.3.47 DPD_AUX_CH_DATA2—Offset 64318h

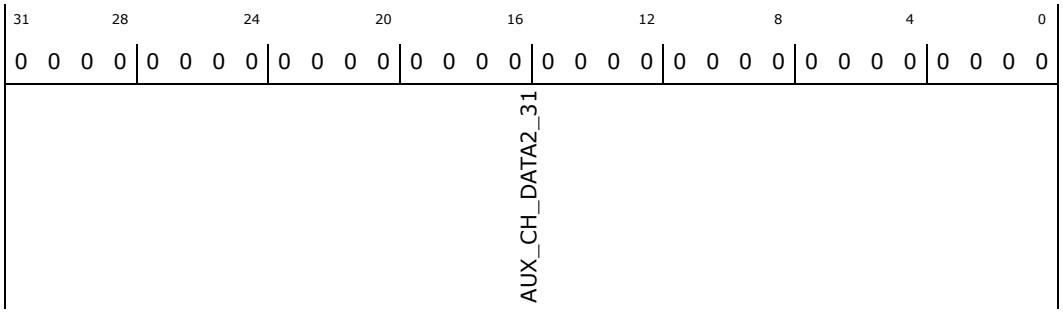
Display Port D AUX Data Register 2 AuxC Data2 (dprrega_b0.v auxc_dpr_data2, ql_auxc_d2)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 64318h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**AUX_CH_DATA2_31:** 0]: The second DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 4. Reads will give the response data after transaction complete.

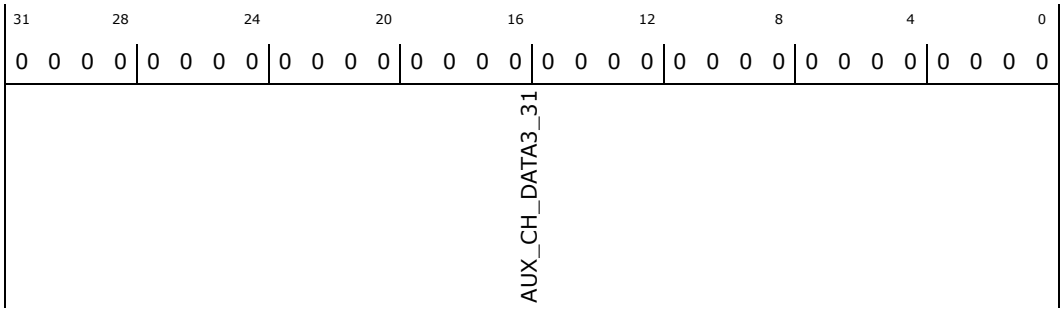
4.3.48 DPD_AUX_CH_DATA3—Offset 6431Ch

Display Port D AUX Data Register 3 AuxC Data3 (dprrega_b0.v auxc_dpr_data3, ql_auxc_d3)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6431Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**AUX_CH_DATA3_31:** 0]: The third DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 8. Reads will give the response data after transaction complete.

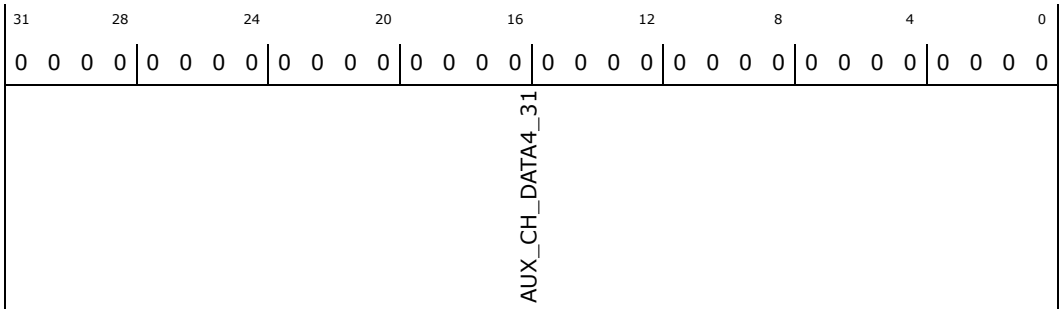
4.3.49 DPD_AUX_CH_DATA4—Offset 64320h

Display Port D AUX Data Register 4 AuxC Data4 (dprrega_b0.v auxc_dpr_data4, ql_auxc_d4)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 64320h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**AUX_CH_DATA4_31:** 0]: The fourth DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 12. Reads will give the response data after transaction complete.

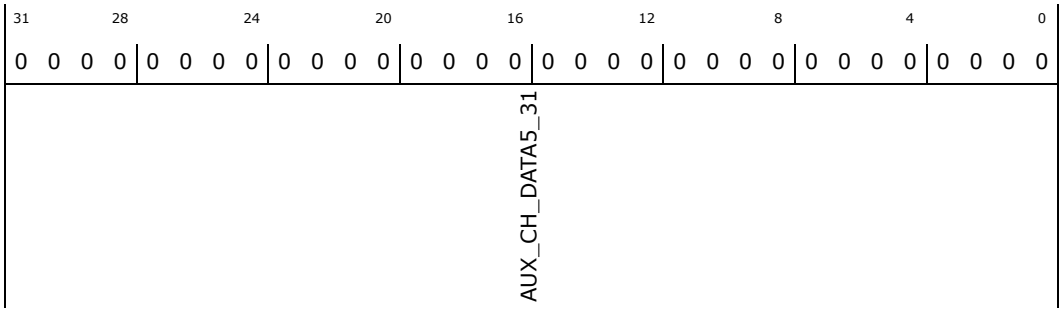
4.3.50 DPD_AUX_CH_DATA5—Offset 64324h

Display Port D AUX Data Register 5 AuxC Data5 (dprrega_b0.v auxc_dpr_data5, ql_auxc_d5)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 64324h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**AUX_CH_DATA5_31:** 0]: The fifth DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 16. Reads will give the response data after transaction complete.

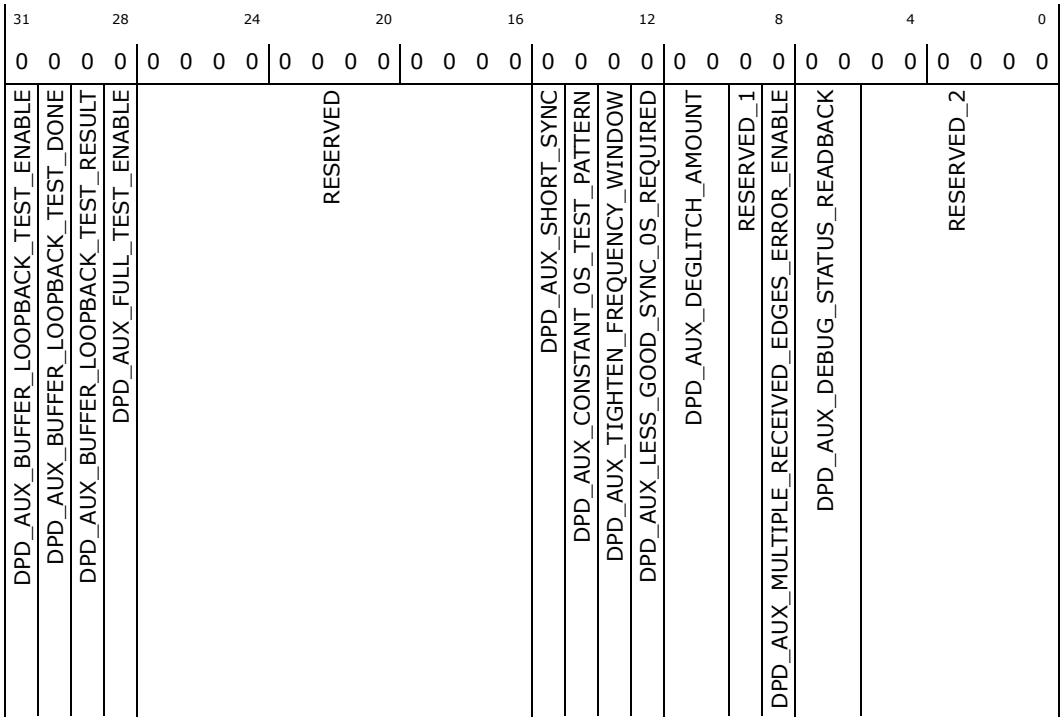
4.3.51 DPD_AUX_TST—Offset 64328h

Display Port D AUX Test Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 64328h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**DPD_AUX_BUFFER_LOOPBACK_TEST_ENABLE:** Project: All Default Value: ;0b Refer DPB description. Value Name Description Project 0b Disable Test disabled All 1b Enable Enable test. All
30	0x0 RO	**DPD_AUX_BUFFER_LOOPBACK_TEST_DONE:** Project: All Default Value: ;0b AccessType: Read Only Refer DPB description. Value Name Description Project 0b Not Done Test not done. DP-AUX Buffer Loopback Test Result is not valid All 1b Done Test done. DP-AUX Buffer Loopback Test Result is now valid All
29	0x0 RO	**DPD_AUX_BUFFER_LOOPBACK_TEST_RESULT:** Project: All Default Value: ;0b AccessType: Read Only Refer description for DPB-AUX Buffer Loopback Test Result Value Name Description Project 0b Pass Pass All 1b Fail Fail All

Bit Range	Default & Access	Field Name (ID): Description
28	0x0 RW	**DPD_AUX_FULL_TEST_ENABLE:** Project: All Default Value: ;0b Refer DPB description. Value Name Description Project 0b Disable Test disabled All 1b Enable Enable test All
27:16	0x0 RO	**RESERVED:** Project: All Format:
15	0x0 RW	**DPD_AUX_SHORT_SYNC:** Project: All Refer DPB description.
14	0x0 RW	**DPD_AUX_CONSTANT_0S_TEST_PATTERN:** Project: All Refer DPB description.
13	0x0 RW	**DPD_AUX_TIGHTEN_FREQUENCY_WINDOW:** Project: All Refer DPB description.
12	0x0 RW	**DPD_AUX_LESS_GOOD_SYNC_0S_REQUIRED:** Project: All Refer DPB description.
11:10	0x0 RW	**DPD_AUX_DEGLITCH_AMOUNT:** Project: All Default Value: ;0b Refer DPB description. Value Name Description Project 00b 50 ns 25 clocks - GMBUS type - 50ns at 500MHz cdclk All 01b 125 ns 1/4 2X bit clock divider value - 125ns All 10b 62.5 ns 1/8 2X bit clock divider value - 62.5ns All 11b 31.125 ns 1/16 2X bit clock divider value - 31.125ns All
9	0x0 RO	**RESERVED_1:** Project: All Format:
8	0x0 RW	**DPD_AUX_MULTIPLE_RECEIVED_EDGES_ERROR_ENABLE:** Project: All Default Value: ;0b Value Name Description Project 0b Okay Multiple edges in window is okay All 1b Error Multiple edges in window is an error All
7:6	0x0 RW	**DPD_AUX_DEBUG_STATUS_READBACK:** Project: All Default Value: ;0b Value Name Description Project 00b Program Readback of bit clock divide field gives the programmed clock frequency All 01b Recover Readback of bit clock divide field gives the recovered clock frequency All 10b Error Type Readback of bit clock divide field gives the error type All
5:0	0x0 RO	**RESERVED_2:** Project: All Format:

4.3.52 STREAM_A_LPE_AUD_CONFIG—Offset 65000h

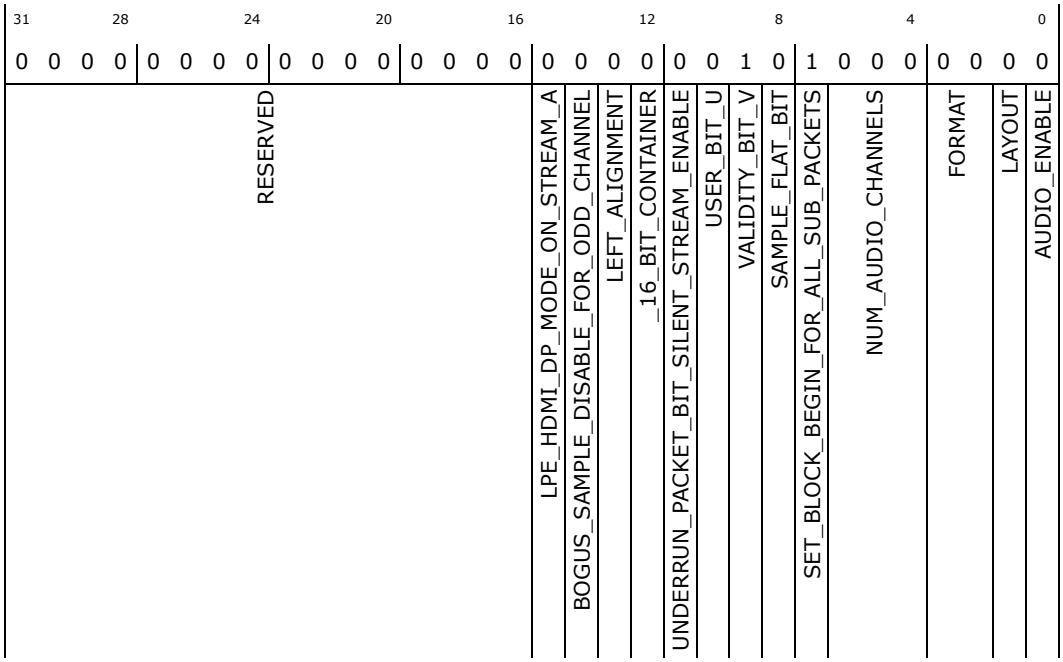
LPE Audio Configuration

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65000h

Default: 00000280h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15	0x0 RW	**LPE_HDMI_DP_MODE_ON_STREAM_A:** 1 = DP mode 0 = HDMI mode (default)
14	0x0 RW	**BOGUS_SAMPLE_DISABLE_FOR_ODD_CHANNEL:** When number of channels in a sample is odd (3, 5, or 7) source application may pad a bogus sample to the next even number of channels. If this bit is set there is no padding in input buffer1= No bogus sample present in buffer for odd number of channels 0= Bogus sample present in buffer for odd number of channels (default)
13	0x0 RW	**LEFT_ALIGNMENT:** When input buffer is in 32-bit container mode. If this bit is set the MSB of audio sample is aligned bit 31 of the container if this bit is clear MSB of audio sample is aligned with bit 23 of the container.1= MSB is bit 31 of 32-bit container 0= MSB is bit 23 of 32-bit container (default)
12	0x0 RW	**_16_BIT_CONTAINER:** When this bit is set 16-bit sample is stored in 16-bit container format. When it is clear container is 32-bit for each sample regardless of valid bits (default)1= 16-bit container 0= 32-bit container

Bit Range	Default & Access	Field Name (ID): Description
11	0x0 RW	**UNDERRUN_PACKET_BIT_SILENT_STREAM_ENABLE:** Set this bit will enable HW to send valid zero-filled packet with Sample flat bit set when no sample buffer is available, NCTS packets (or Timesstamp packet) are sent to keep sink in sync even no audio sound will heard.1= send underrun packets (silent stream) 0= send null packets (default)
10	0x0 RW	**USER_BIT_U:** HW will clear this bit in each sub-frames it sends, But this bit allows to overwrite hardware setting for special operation like debug or testing for compliance 1= sey U bit in sub-frame 0= clear U bit in sub-frame (default)
9	0x1 RW	**VALIDITY_BIT_V:** HW will set this bit in both each sub-frames it sends. But this bit allows to overwrite hardware setting for special operation like debug or testing for compliance 1= Set V bit in sub-frame (default) 0= clear V bit in sub-frame. For debug or testing
8	0x0 RW	**SAMPLE_FLAT_BIT:** When set the sample flat bit will be set in all HDMI sub-packets. 1= flat bit is set for valid sample 0= flat bit is not set for valid sample (default)
7	0x1 RW	**SET_BLOCK_BEGIN_FOR_ALL_SUB_PACKETS:** Controls the B bit in the header of only the first Audio Packet /frame of a 192 frame 60958 block in Layout 1 mode. This bit only applies to LPE HDMI mode. 0: The B bit will be set only for sub-packet 0 1: The B bit in the Audio sample packet header will be set for all valid sub-packets. (default)
6:4	0x0 RW	**NUM_AUDIO_CHANNELS:** 000: 2 channels (stereo) 001: 3 channels 010: 4 channels 011: 5 channels 100: 6 channels 101: 7 channels 110: 8 channels Note: When disable_bogus sample bit is clear HW will always treat odd number of channels similar to the next higher even number. Thus 3 is similar to 4, 5 to 6 and 7 to 8. This is because SW ensures that an even number of samples are packed in the audio buffers.
3:2	0x0 RW	**FORMAT:** 00: L-PCM or IEC 61937 01: High Bit Rate IEC 61937 stream packet (not supported) 10: One Bit Audio Sample packet (not supported) 11: DST Audio Sample packet (not supported)
1	0x0 RW	**LAYOUT:** 0: Layout 0 (2-ch) 1: Layout 1 (3-8 ch) Note: Layout bit doesn’t matter for HBR

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**AUDIO_ENABLE:** Controls generation of N/CTS and transmission of audio sample packets. 0: Audio sample packets are not transmitted, CTS calculation/transmission is disabled 1: Audio sample packets are transmitted and CTS calculation is enabled When enable audio unit will wait until the next vertical blank period before sending out the audio packets. When disable, audio unit may continue to send audio packet until the end of current active video frame before stopping.

4.3.53 STREAM_A_LPE_AUD_CH_STATUS_0—Offset 65008h

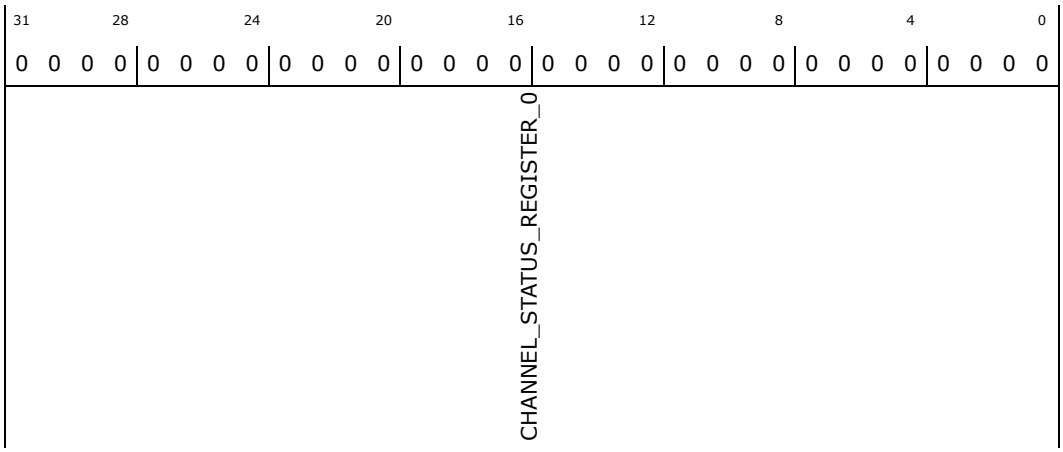
Audio Channel Status Attributes 0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65008h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**CHANNEL_STATUS_REGISTER_0:** . These bits are transmitted as attributes of audio packets

4.3.54 STREAM_A_LPE_AUD_CH_STATUS_1—Offset 6500Ch

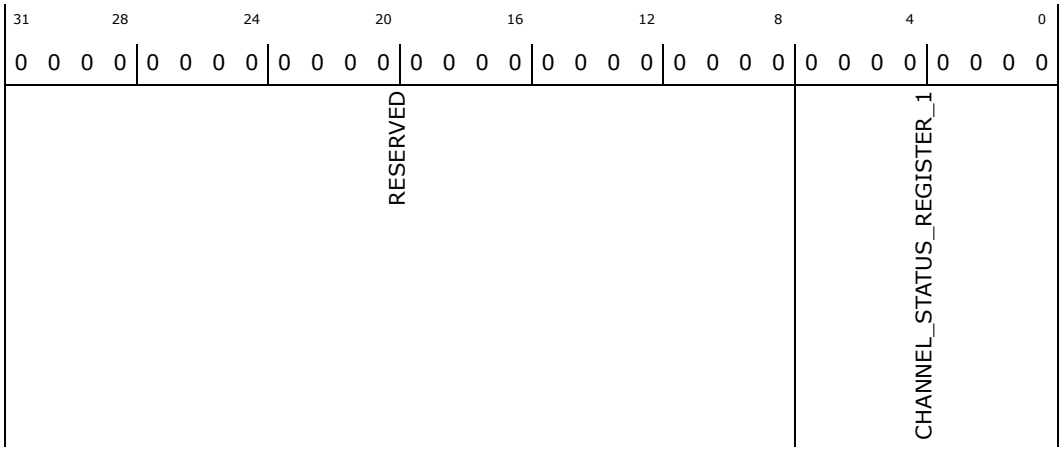
Audio Channel Status Attributes 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6500Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED:** Reserved.
7:0	0x0 RW	**CHANNEL_STATUS_REGISTER_1:** . These bits are transmitted as attributes of audio packets. There is only 8 bits valid in this register.

4.3.55 STREAM_A_LPE_AUD_HDMI_CTS_DP_MAUD—Offset 65010h

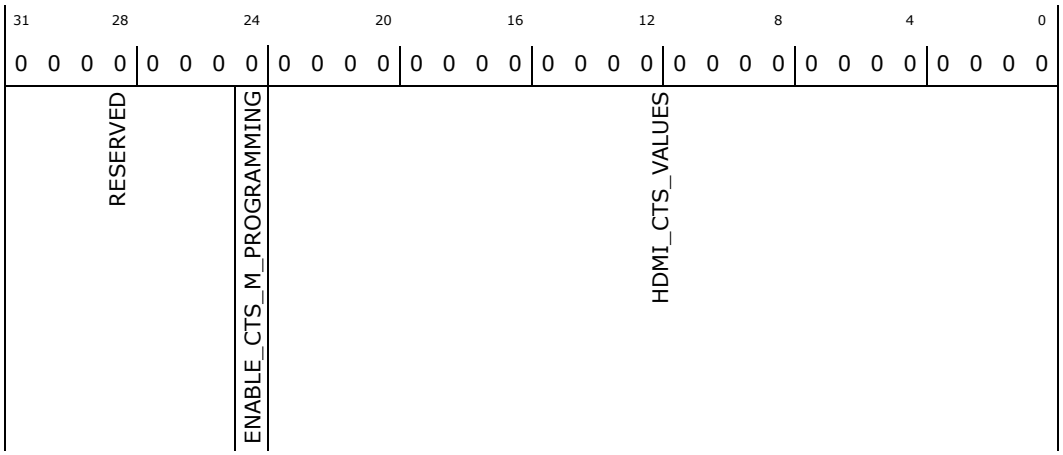
Audio HDMI CTS Register (DP Maud)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65010h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RESERVED:** Reserved.
24	0x0 RW	**ENABLE_CTS_M_PROGRAMMING:** 1 = Enable CTS/M programming 0 = Disable CTS/M programming
23:0	0x0 RW	**HDMI_CTS_VALUES:** These are bits [23:0] of programmable HDMI CTS values (or DP Maud) that is pre-calculated to achieve desired audio sample rates with a particular pixel clocks configuration. Audio function must be disabled when changing this field. Bit 24 also need to write to 1 to enable this field.

4.3.56 STREAM_A_LPE_AUD_HDMI_N_DP_NAUD—Offset 65014h

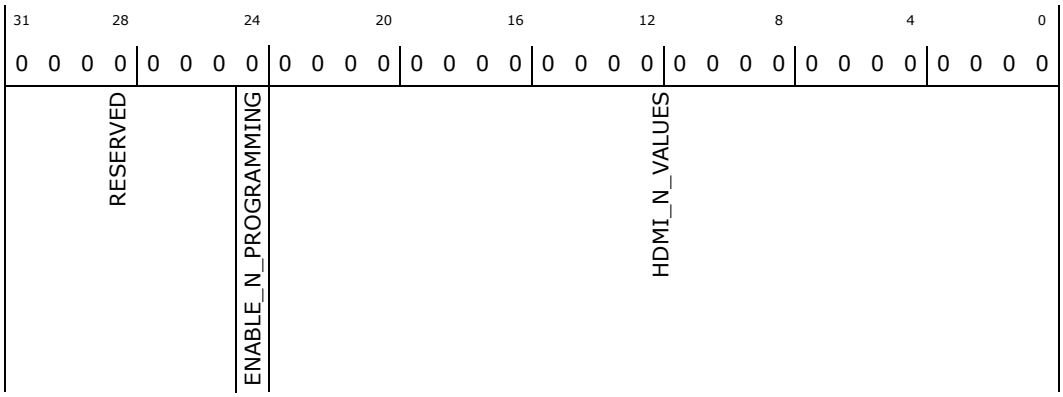
Audio HDMI N Register (DP Naud)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65014h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RESERVED:** Reserved.
24	0x0 RW	**ENABLE_N_PROGRAMMING:** 1 = Enable N programming 0 = Disable N programming
23:0	0x0 RW	**HDMI_N_VALUES:** These are bits [23:0] of programmable HDMI N (or DP Naud) values that is pre-calculated to achieve desired audio sample rates with a particular pixel clocks configuration. Audio function must be disabled when changing this field. Bit 24 also need to write to 1 to enable this field.

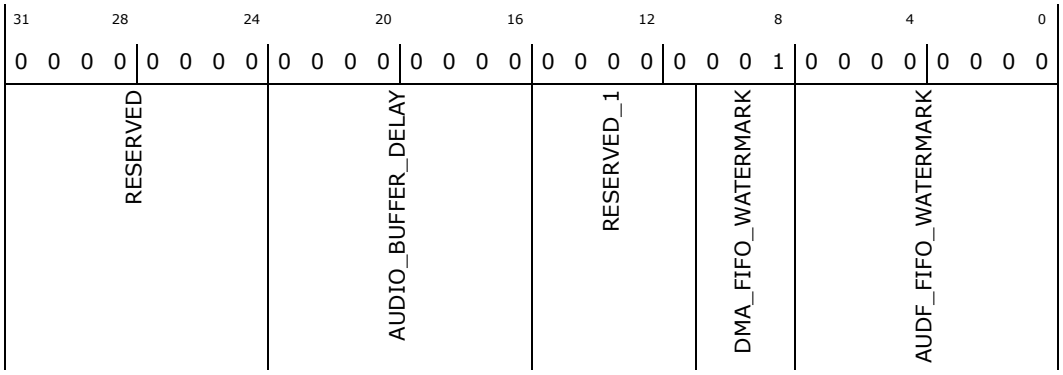
4.3.57 STREAM_A_LPE_AUD_BUFFER_CONFIG—Offset 65020h

LPE Audio buffer config

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65020h

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:16	0x0 RO	**AUDIO_BUFFER_DELAY:** This field specifies a delay in number of video frames that the audio controller will count off when audio enable bit is set before start transmitting audio sample.
15:11	0x0 RO	**RESERVED_1:** Reserved.
10:8	0x1 RO	**DMA_FIFO_WATERMARK:** Audio unit has a 8x64 bytes fifo for pre-fetching and staging audio samples. This register provides a watermark value in SWORDs (64B). When enable and sample buffer is available audio unit will fetch samples until this FIFO is full then it waits until HDMI/DP packet assembler drains the samples to a level less or equal the watermark setting then it will start fetching the samples again. Default value is 1 cacheline (SW).
7:0	0x0 RO	**AUDF_FIFO_WATERMARK:** Audio unit has a 8x96 bytes fifo for pre-fetching and staging audio samples. This register provides a watermark value in DWORDs. When enable and sample buffer is available audio unit will fetch samples until this FIFO is full then it waits until HDMI packet assembler drains the samples to a level less or equal the watermark setting then it will start fetching the samples again

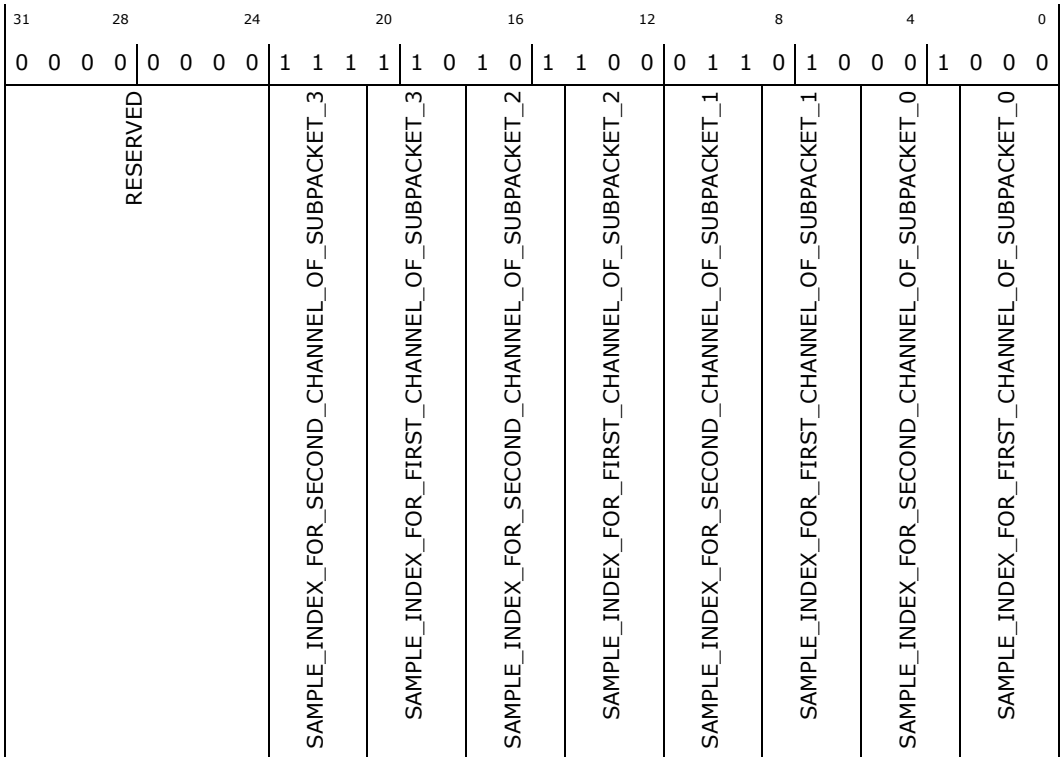
4.3.58 STREAM_A_LPE_AUD_BUF_CH_SWP—Offset 65024h

Audio Sample Swapping

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65024h

Default: 00FAC688h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:21	0x7 RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_3:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 3 in a HDMI audio packet
20:18	0x6 RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_3:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 1 in a HDMI audio packet
17:15	0x5 RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_2:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 0 in a HDMI audio packet
14:12	0x4 RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_2:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 0 in a HDMI audio packet
11:9	0x3 RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_1:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 1 in a HDMI audio packet
8:6	0x2 RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_1:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 1 in a HDMI audio packet

Bit Range	Default & Access	Field Name (ID): Description
5:3	0x1 RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_0:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 0 in a HDMI audio packet
2:0	0x0 RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_0:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 0 in a HDMI audio packet

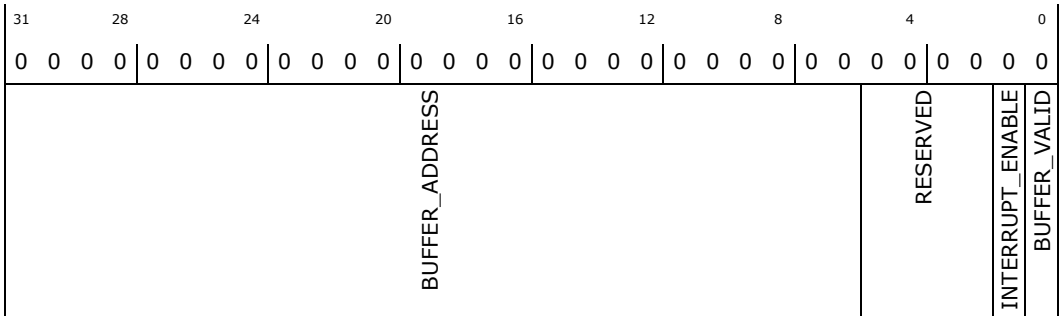
4.3.59 STREAM_A_LPE_AUD_BUF_A_ADDR—Offset 65040h

Address for Audio Buffer A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65040h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0x0 RO	**RESERVED:** Reserved.
1	0x0 RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0x0 RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

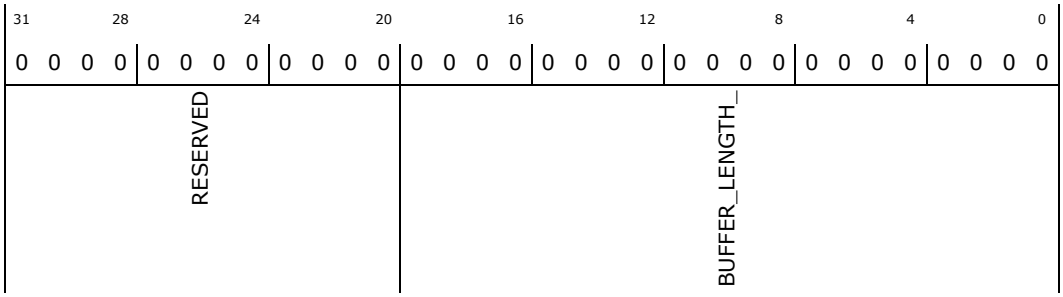
4.3.60 STREAM_A_LPE_AUD_BUF_A_LENGTH—Offset 65044h

Length for Audio Buffer A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65044h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RESERVED:** Reserved.
19:0	0x0 RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

4.3.61 STREAM_A_LPE_AUD_BUF_B_ADDR—Offset 65048h

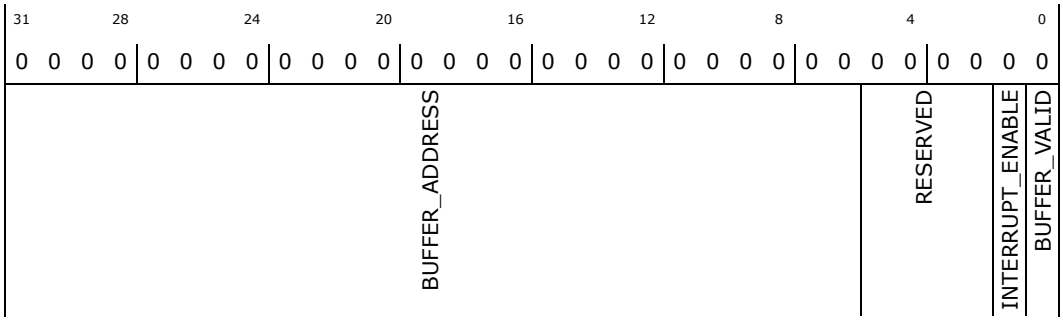
Address for Audio Buffer B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65048h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0x0 RO	**RESERVED:** Reserved.
1	0x0 RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

4.3.62 STREAM_A_LPE_AUD_BUF_B_LENGTH—Offset 6504Ch

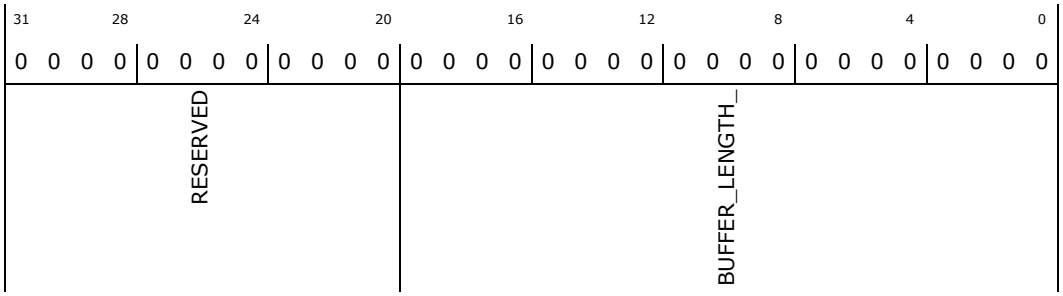
Length for Audio Buffer B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6504Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RESERVED:** Reserved.
19:0	0x0 RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

4.3.63 STREAM_A_LPE_AUD_BUF_C_ADDR—Offset 65050h

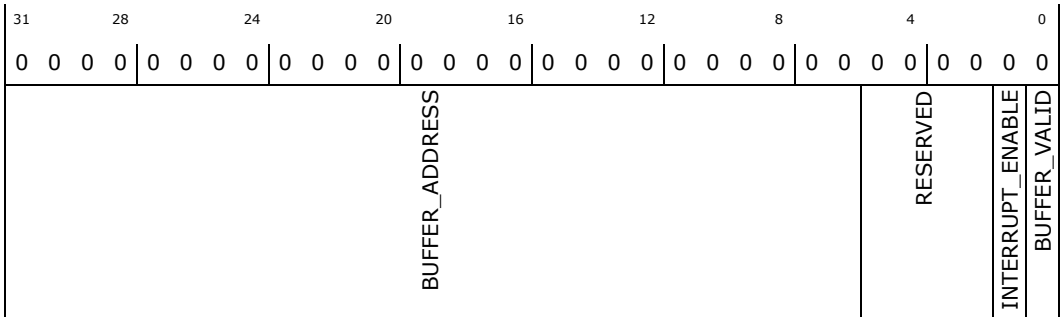
Address for Audio Buffer C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65050h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0x0 RO	**RESERVED:** Reserved.
1	0x0 RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0x0 RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

4.3.64 STREAM_A_LPE_AUD_BUF_C_LENGTH—Offset 65054h

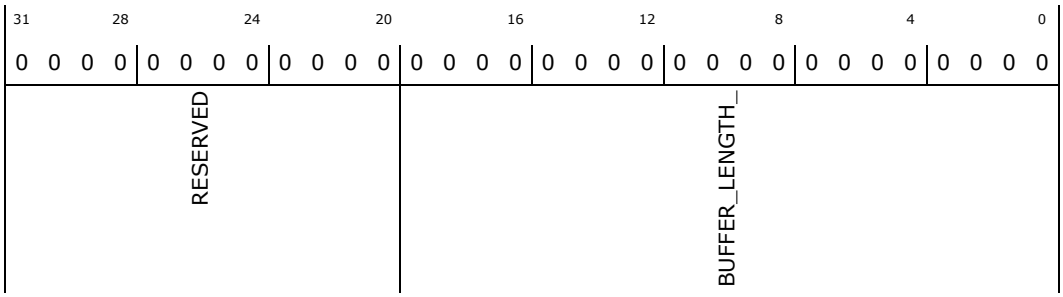
Length for Audio Buffer C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65054h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
19:0	0x0 RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

4.3.65 STREAM_A_LPE_AUD_BUF_D_ADDR—Offset 65058h

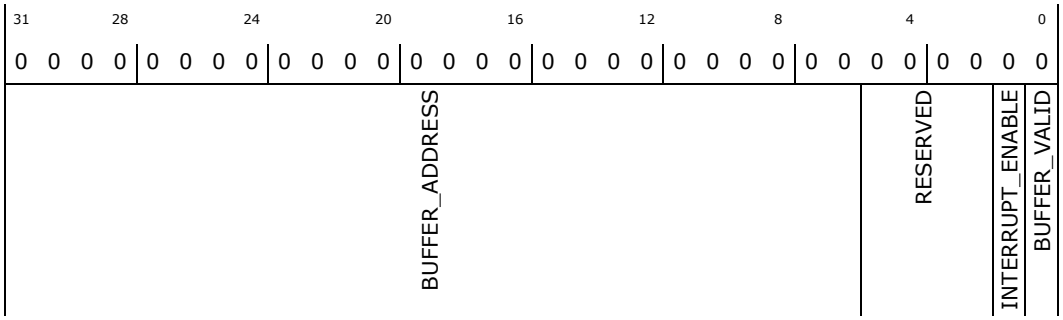
Address for Audio Buffer D

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65058h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0x0 RO	**RESERVED:** Reserved.
1	0x0 RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0x0 RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

4.3.66 STREAM_A_LPE_AUD_BUF_D_LENGTH—Offset 6505Ch

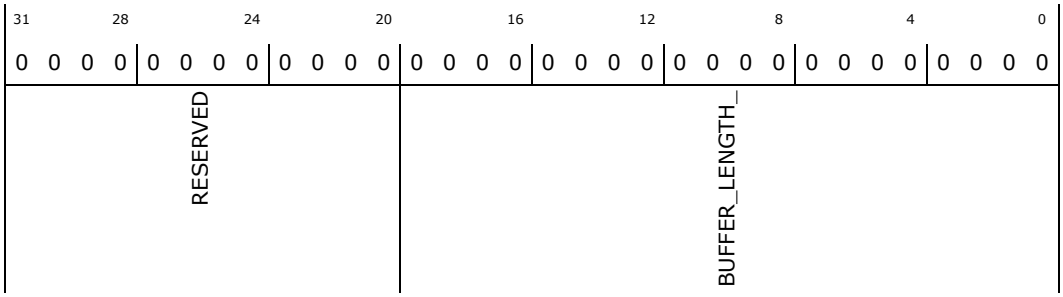
Length for Audio Buffer D

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6505Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RESERVED:** Reserved.
19:0	0x0 RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

4.3.67 STREAM_A_LPE_AUD_CNTL_ST—Offset 65060h

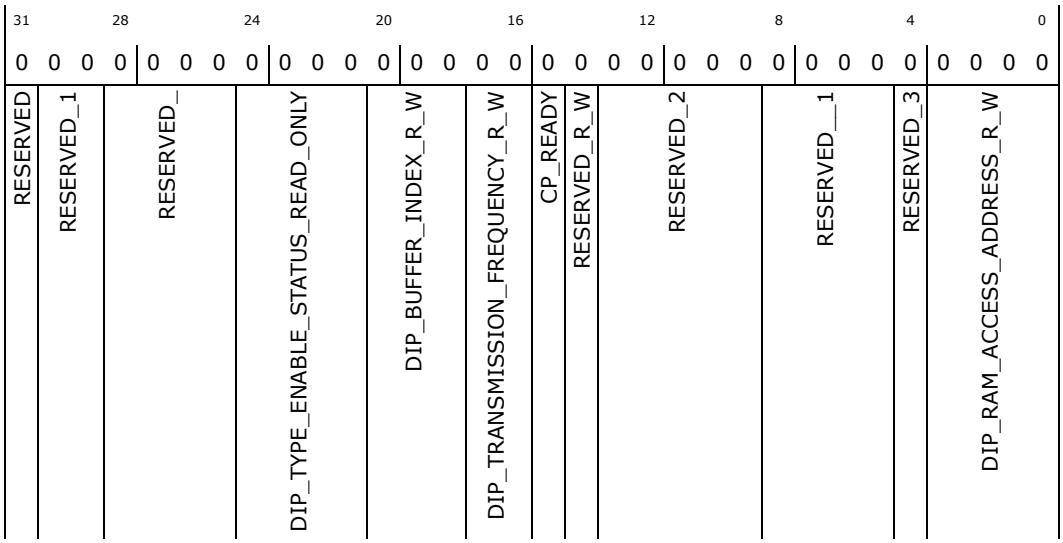
LPE Audio Control State Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65060h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** Reserved.
30:29	0x0 RO	**RESERVED_1:** Reserved.
28:25	0x0 RO	**RESERVED_:** for later DIP type if needed: Must be 0.
24:21	0x0 RO	**DIP_TYPE_ENABLE_STATUS_READ_ONLY:** These bits reflects the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling an DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP. XXX1 = Audio DIP enable status (Default = disabled) XX1X = Generic 1 (ACP) DIP enable status (Default = disabled) X1XX = Generic 2 DIP enable status, can be used by ISRC1 or ISRC2 (Default = disabled) 1XXX = Reserved
20:18	0x0 RW	**DIP_BUFFER_INDEX_R_W:** This field is used during read or write of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0 s. 000 = (Default) Audio DIP (31 bytes of address space, 13 bytes of data) 001 = Generic 1 (ACP) Data Island Packet (31 bytes of address space, 11 bytes of data) 010 = Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data) 011 = Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data) 1XX = reserved
17:16	0x0 RW	**DIP_TRANSMISSION_FREQUENCY_R_W:** These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written.When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18. 00 = Disabled (Default) 01 = once per frame 10 = Send once 11 = Best effort (Send at least every other vsync)
15	0x0 RW	**CP_READY:** This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. 0 = CP request pending or not ready to receive requests (default) 1 = CP request ready CP_ready bit is programmable through Bit 14 for [DevCL, DevBLC]. CP_ready bit is programmable through Bit 15 for [DevCTG]. Bit 15 Reserved for [DevCL, DevBLC].

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RO	**RESERVED_R_W:** ELD valid: This bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit.0 = ELD data invalid (default, when writing ELD data, set 0 by software) 1 = ELD data valid (Set by video software only) ELD bit is programmable through Bit 13 for [DevCL, DevBLC]. ELD bit is programmable through Bit 14 for [DevCTG].
13:9	0x0 RO	**RESERVED_2:** ELD buffer size (read only)10000 = This field reflects the size of the ELD buffer in DWORDs 13:9 reflects ELD buffer size for [DevCTG]. 12:9 reflects ELD buffer size for [DevCL, DevBLC].
8:5	0x0 RO	**RESERVED__1:** ELD access address (R/W): Selects the DWORD address for access to the ELD buffer (48 bytes). The value wraps back to zero when incremented past the max addressing value 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.
4	0x0 RO	**RESERVED_3:** ELD ACK: Acknowledgement from the audio driver that ELD read has been completed
3:0	0x0 RW	**DIP_RAM_ACCESS_ADDRESS_R_W:** Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

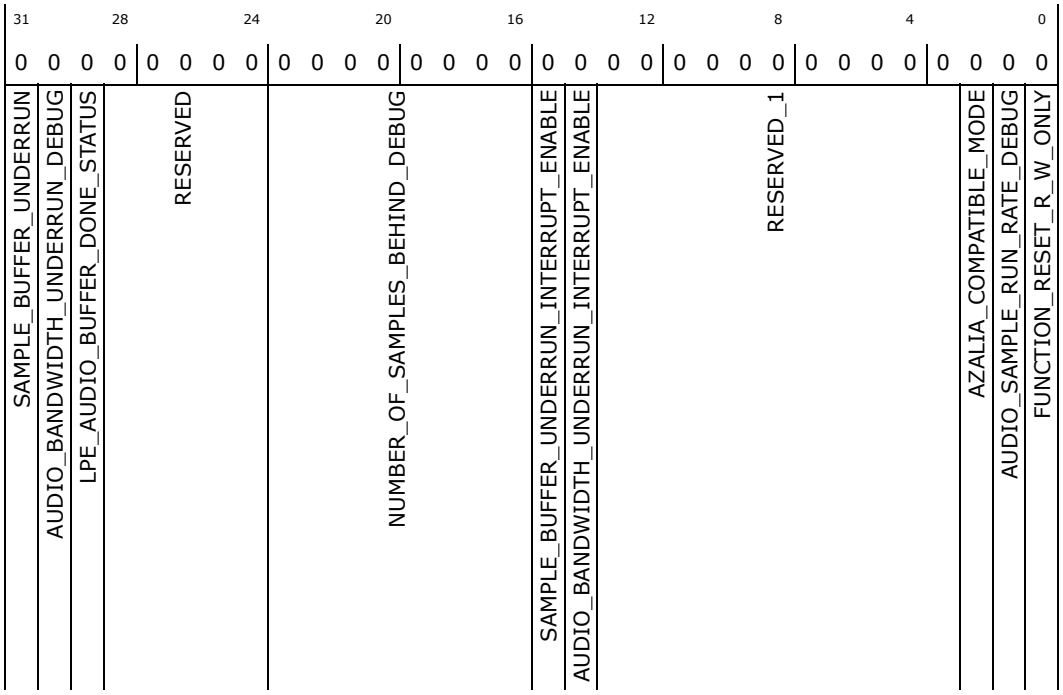
4.3.68 STREAM_A_LPE_AUD_HDMI_STATUS—Offset 65064h

LPE Audio Status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65064h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C	**SAMPLE_BUFFER_UNDERRUN:** This bit indicates an underrun in the sample buffer to HDMI controller when it needs to send. This bit is set at the last line of active video when there are no more sample in any valid buffers and HDMI audio unit has not satisfied number of audio samples intended in that video frame. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. AccessType: One to Clear
30	0x0 RW/1C	**AUDIO_BANDWIDTH_UNDERRUN_DEBUG:** This bit indicates an underrun of audio samples at HDMI audio packet assembly even there is still available sample buffers. Audio bandwidth underrun should not happen in normal functionality but it may happen when audio setting is unappropriate and/or memory bus was blocked by other clients, etc... This bit is set at the last line of active video when there is valid samples in a valid buffer and HDMI audio unit has not satisfied number of audio samples intended in that video frame Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. AccessType: One to Clear
29	0x0 RW/1C	**LPE_AUDIO_BUFFER_DONE_STATUS:** This bit is set when a LPE audio buffer is completed transferred all of its data to LPE audio unit. This bit is clear when write 1 to it AccessType: One to Clear
28:24	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0x0 RO	**NUMBER_OF_SAMPLES_BEHIND_DEBUG:** This field is read only to get the number of audio samples that controller needs to load and send at the time of reading. AccessType: Read Only
15	0x0 RW	**SAMPLE_BUFFER_UNDERRUN_INTERRUPT_ENABLE:** This bit is to enable the first line buffer underrun interrupt when sample buffer underrun status is detected 0 = LPE sample Buffer Underrun Interrupt Disabled 1 = LPE sample Buffer Underrun Interrupt Enabled
14	0x0 RW	**AUDIO_BANDWIDTH_UNDERRUN_INTERRUPT_ENABLE:** This bit is to enable the first line bandwidth underrun interrupt when bandwidth underrun status is detected 0 = LPE Bandwidth Underrun Interrupt Disabled 1 = LPE Bandwidth Underrun Interrupt Enabled
13:3	0x0 RO	**RESERVED_1:** Reserved.
2	0x0 RW	**AZALIA_COMPATIBLE_MODE:** This bit is to enable the vucp, PR, ECC to be generated in the Azalia way 0 = Disable Azalia compatible mode on vucp, PR, ECC 1 = Enable Azalia compatible mode on vucp, PR, ECC
1	0x0 RW	**AUDIO_SAMPLE_RUN_RATE_DEBUG:** When set it allows to fetch sample 128 times than the real sample rate to allow a faster drain of sample buffers.
0	0x0 RW	**FUNCTION_RESET_R_W_ONLY:** Write 1 to this bit will reset hardware within audio unit without needs of reset the full display controller. The FIFO and pointers will be reset and audio registers will be reset to default values. Write 0 will put the unit back to idle and ready to be programmed again.

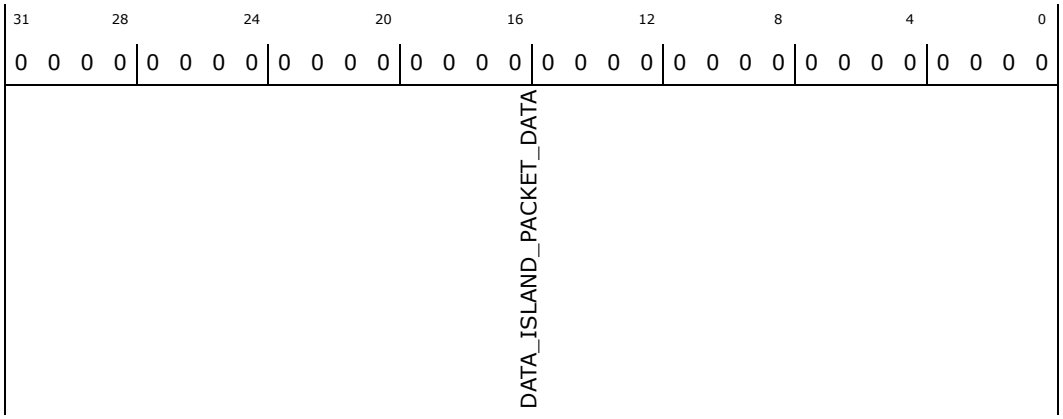
4.3.69 STREAM_A_LPE_AUD_HDMIW_INFOFR—Offset 65068h

Audio HDMI Data Island Packet Data

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65068h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DATA_ISLAND_PACKET_DATA:** When read, this returns the current value at the location specified in the Video DIP buffer index select and Video DIP RAM access address fields. The index used to address the RAM is incremented after each read or write of this register. DIP data can be read at any time. Data should be loaded into the RAM before enabling the transmission through the DIP type enable bit. Accesses to this register are on a per-DWORD basis

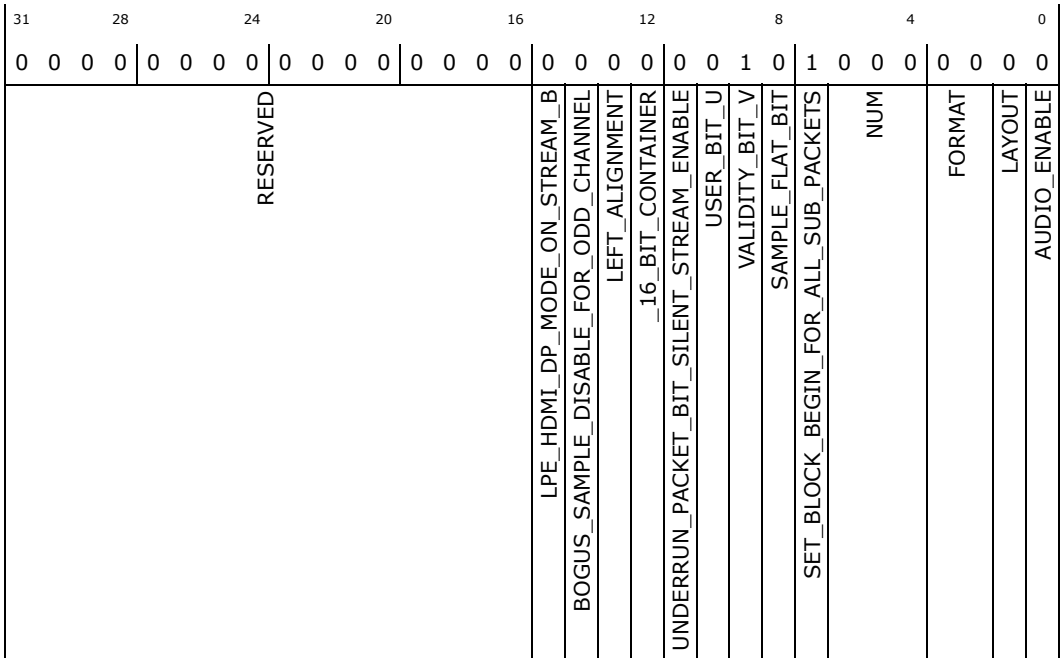
4.3.70 STREAM_B_LPE_AUD_CONFIG—Offset 65800h

LPE Audio Configuration

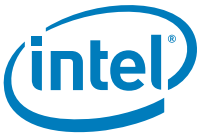
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65800h

Default: 00000280h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15	0x0 RW	**LPE_HDMI_DP_MODE_ON_STREAM_B:** 1= DP mode 0 = HDMI mode (default)
14	0x0 RW	**BOGUS_SAMPLE_DISABLE_FOR_ODD_CHANNEL:** When number of channels in a sample is odd (3, 5, or 7) source application may pad a bogus sample to the next even number of channels. If this bit is set there is no padding in input buffer1= No bogus sample present in buffer for odd number of channels 0= Bogus sample present in buffer for odd number of channels (default)
13	0x0 RW	**LEFT_ALIGNMENT:** When input buffer is in 32-bit container mode. If this bit is set the MSB of audio sample is aligned bit 31 of the container if this bit is clear MSB of audio sample is aligned with bit 23 of the container.1= MSB is bit 31 of 32-bit container 0= MSB is bit 23 of 32-bit container (default)
12	0x0 RW	**_16_BIT_CONTAINER:** When this bit is set 16-bit sample is stored in 16-bit container format. When it is clear container is 32-bit for each sample regardless of valid bits (default)1= 16-bit container 0= 32-bit container
11	0x0 RW	**UNDERRUN_PACKET_BIT_SILENT_STREAM_ENABLE:** Set this bit will enble HW to send valid zero-filled packet with Sample flat bit set when no sample buffer is available, NCTS packets (or Timesstamp packet) are sent to keep sink in sync even no audio sound will heard.1= send underrun packets (silent stream) 0= send null packets (default)



Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RW	**USER_BIT_U:** HW will clear this bit in each sub-frames it sends, But this bit allows to overwrite hardware setting for special operation like debug or testing for compliance 1= sey U bit in sub-frame 0= clear U bit in sub-frame (default)
9	0x1 RW	**VALIDITY_BIT_V:** HW will set this bit in both each sub-frames it sends. But this bit allows to overwrite hardware setting for special operation like debug or testing for compliance 1= Set V bit in sub-frame (default) 0= clear V bit in sub-frame. For debug or testing
8	0x0 RW	**SAMPLE_FLAT_BIT:** When set the sample flat bit will be set in all HDMI sub-packets. 1= flat bit is set for valid sample 0= flat bit is not set for valid sample (default)
7	0x1 RW	**SET_BLOCK_BEGIN_FOR_ALL_SUB_PACKETS:** Controls the B bit in the header of only the first Audio Packet /frame of a 192 frame 60958 block in Layout 1 mode. This bit only applies to LPE HDMI mode. 0: The B bit will be set only for sub-packet 0 1: The B bit in the Audio sample packet header will be set for all valid sub-packets. (default)
6:4	0x0 RW	**NUM:** audio Channels 000: 2 channels (stereo) 001: 3 channels 010: 4 channels 011: 5 channels 100: 6 channels 101: 7 channels 110: 8 channels Note: When disable_bogus sample bit is clear HW will always treat odd number of channels similar to the next higher even number. Thus 3 is similar to 4, 5 to 6 and 7 to 8. This is because SW ensures that an even number of samples are packed in the audio buffers.
3:2	0x0 RW	**FORMAT:** 00: L-PCM or IEC 61937 01: High Bit Rate IEC 61937 stream packet (not supported) 10: One Bit Audio Sample packet (not supported) 11: DST Audio Sample packet (not supported)
1	0x0 RW	**LAYOUT:** 0: Layout 0 (2-ch) 1: Layout 1 (3-8 ch) Note: Layout bit does not matter for HBR
0	0x0 RW	**AUDIO_ENABLE:** Controls generation of N/CTS and transmission of audio sample packets. 0: Audio sample packets are not transmitted, CTS calculation/transmission is disabled 1: Audio sample packets are transmitted and CTS calculation is enabled When enable audio unit will wait until the next vertical blank period before sending out the audio packets. When disable, audio unit may continue to send audio packet until the end of current active video frame before stopping.

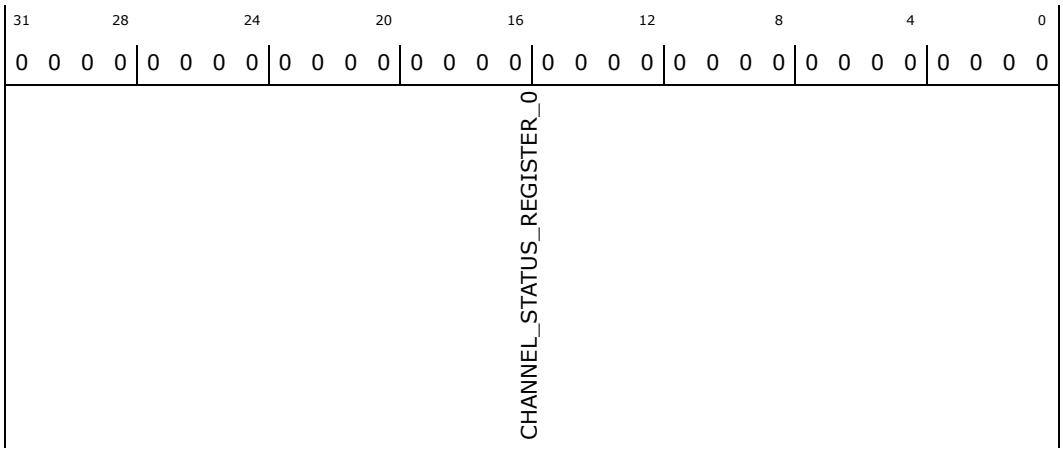
4.3.71 STREAM_B_LPE_AUD_CH_STATUS_0—Offset 65808h

Audio Channel Status Attributes 0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65808h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**CHANNEL_STATUS_REGISTER_0:** . These bits are transmitted as attributes of audio packets

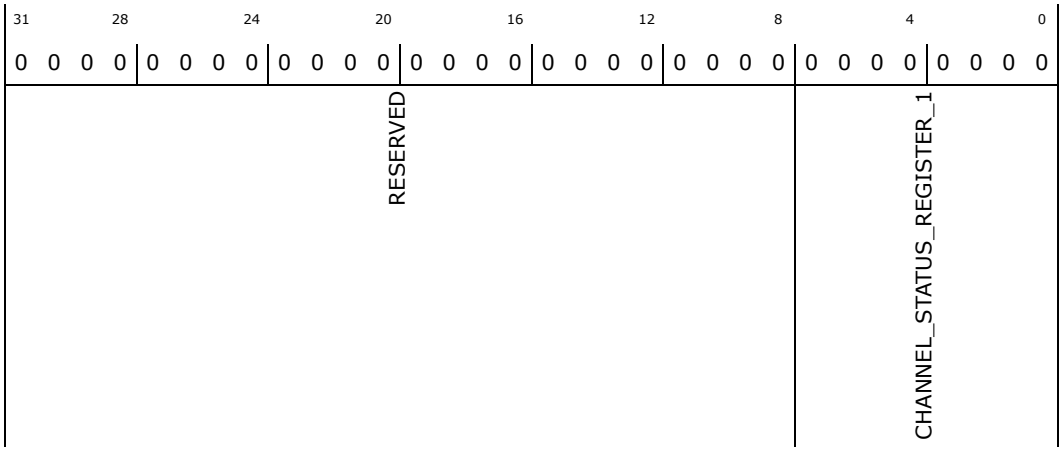
4.3.72 STREAM_B_LPE_AUD_CH_STATUS_1—Offset 6580Ch

Audio Channel Status Attributes 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6580Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED:** Reserved.
7:0	0x0 RW	**CHANNEL_STATUS_REGISTER_1:** . These bits are transmitted as attributes of audio packets. There is only 8 bits valid in this register.

4.3.73 STREAM_B_LPE_AUD_HDMI_CTS_DP_MAUD—Offset 65810h

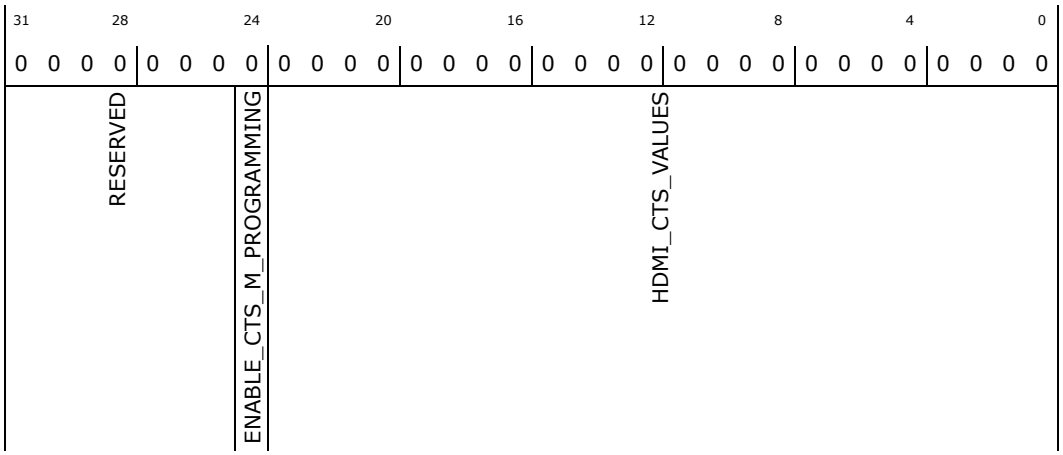
Audio HDMI CTS Register (DP Maud)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65810h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RESERVED:** Reserved.
24	0x0 RW	**ENABLE_CTS_M_PROGRAMMING:** 1 = Enable CTS/M programming 0 = Disable CTS/M programming
23:0	0x0 RW	**HDMI_CTS_VALUES:** These are bits [23:0] of programmable HDMI CTS values (or DP Maud) that is pre-calculated to achieve desired audio sample rates with a particular pixel clocks configuration. Audio function must be disabled when changing this field. Bit 24 also need to write to 1 to enable this field.

4.3.74 STREAM_B_LPE_AUD_HDMI_N_DP_NAUD—Offset 65814h

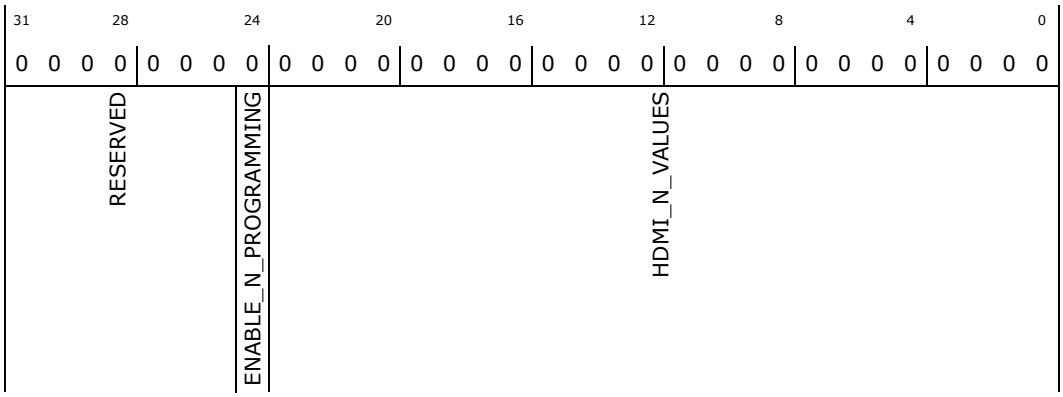
Audio HDMI N Register (DP Naud)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65814h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RESERVED:** Reserved.
24	0x0 RW	**ENABLE_N_PROGRAMMING:** 1 = Enable N programming 0 = Disable N programming
23:0	0x0 RW	**HDMI_N_VALUES:** These are bits [23:0] of programmable HDMI N (or DP Naud) values that is pre-calculated to achieve desired audio sample rates with a particular pixel clocks configuration. Audio function must be disabled when changing this field. Bit 24 also need to write to 1 to enable this field.

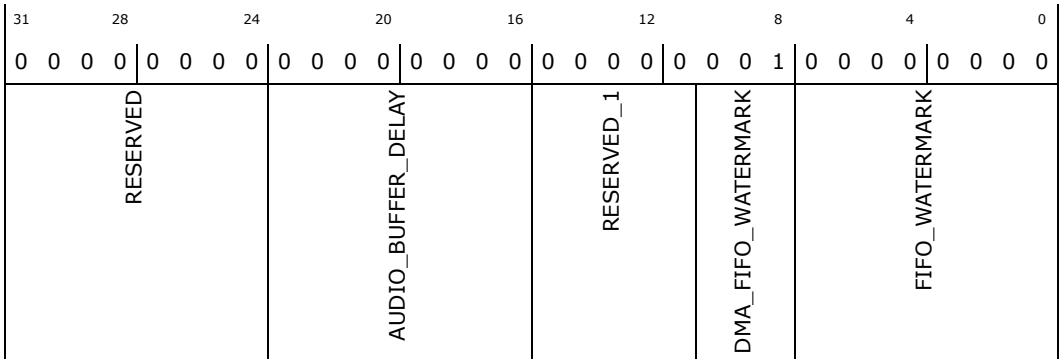
4.3.75 STREAM_B_LPE_AUD_BUFFER_CONFIG—Offset 65820h

LPE Audio buffer config

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65820h

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:16	0x0 RW	**AUDIO_BUFFER_DELAY:** This field specifies a delay in number of video frames that the audio controller will count off when audio enable bit is set before start transmitting audio sample.
15:11	0x0 RO	**RESERVED_1:** .
10:8	0x1 RW	**DMA_FIFO_WATERMARK:** Audio unit has a 8x64 bytes fifo for pre-fetching and staging audio samples. This register provides a watermark value in SWORDs (64B). When enable and sample buffer is available audio unit will fetch samples until this FIFO is full then it waits until HDMI/DP packet assembler drains the samples to a level less or equal the watermark setting then it will start fetching the samples again. Default value is 1 cacheline (SW).
7:0	0x0 RW	**FIFO_WATERMARK:** Audio unit has a 8x96 bytes fifo for pre-fetching and staging audio samples. This register provides a watermark value in DWORDs. When enable and sample buffer is available audio unit will fetch samples until this FIFO is full then it waits until HDMI packet assembler drains the samples to a level less or equal the watermark setting then it will start fetching the samples again

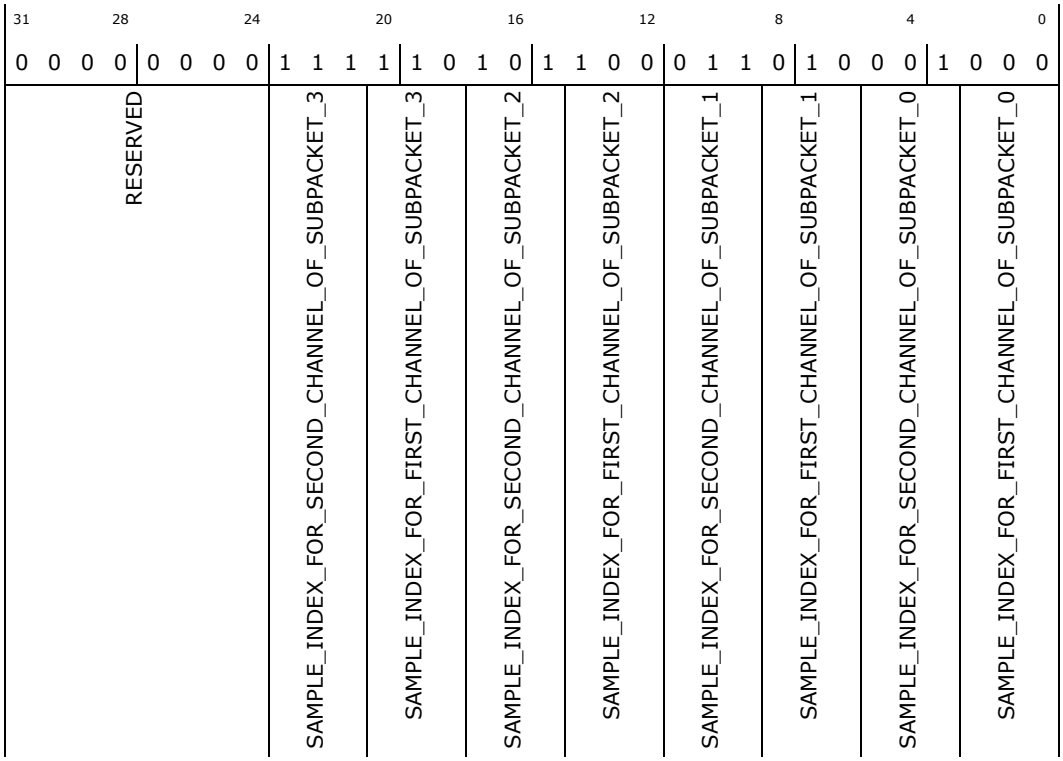
4.3.76 STREAM_B_LPE_AUD_BUF_CH_SWP—Offset 65824h

Audio Sample Swapping

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65824h

Default: 00FAC688h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:21	0x7 RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_3:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 3 in a HDMI audio packet
20:18	0x6 RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_3:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 1 in a HDMI audio packet
17:15	0x5 RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_2:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 0 in a HDMI audio packet
14:12	0x4 RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_2:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 0 in a HDMI audio packet
11:9	0x3 RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_1:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 1 in a HDMI audio packet
8:6	0x2 RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_1:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 1 in a HDMI audio packet

Bit Range	Default & Access	Field Name (ID): Description
5:3	0x1 RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_0:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 0 in a HDMI audio packet
2:0	0x0 RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_0:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 0 in a HDMI audio packet

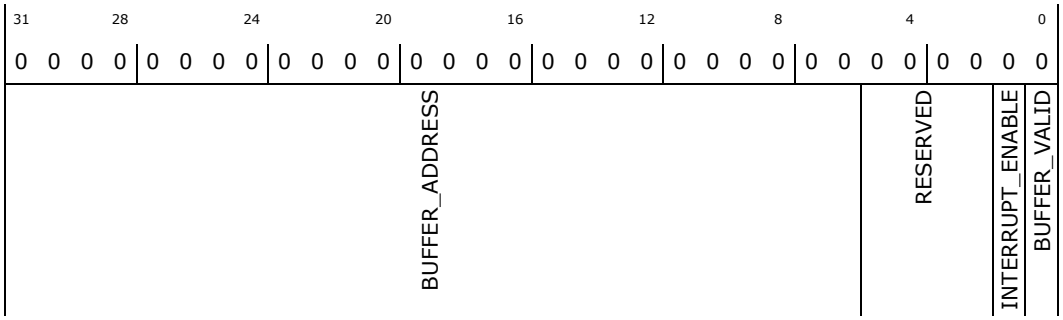
4.3.77 STREAM_B_LPE_AUD_BUF_A_ADDR—Offset 65840h

Address for Audio Buffer A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65840h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0x0 RO	**RESERVED:** Reserved.
1	0x0 RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0x0 RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

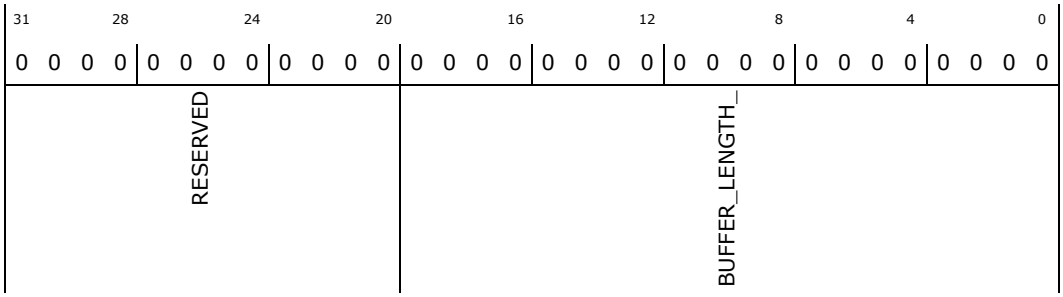
4.3.78 STREAM_B_LPE_AUD_BUF_A_LENGTH—Offset 65844h

Length for Audio Buffer A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65844h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RESERVED:** Reserved.
19:0	0x0 RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

4.3.79 STREAM_B_LPE_AUD_BUF_B_ADDR—Offset 65848h

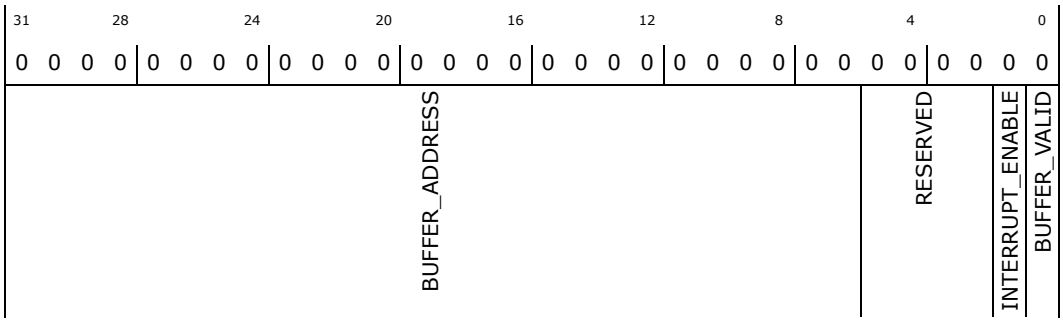
Address for Audio Buffer B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65848h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0x0 RO	**RESERVED:** Reserved.
1	0x0 RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

4.3.80 STREAM_B_LPE_AUD_BUF_B_LENGTH—Offset 6584Ch

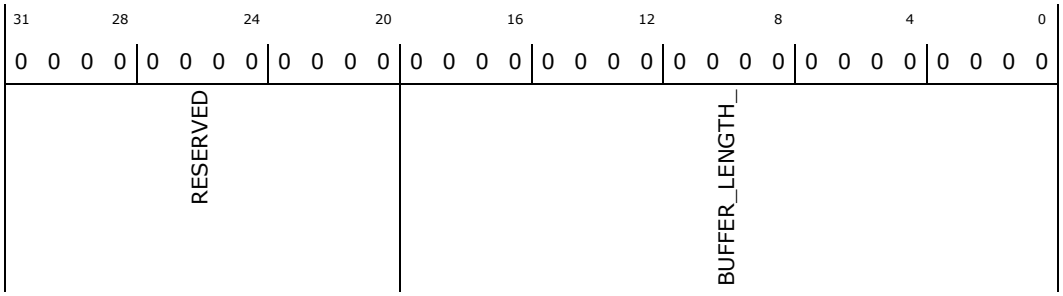
Length for Audio Buffer B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6584Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RESERVED:** Reserved.
19:0	0x0 RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

4.3.81 STREAM_B_LPE_AUD_BUF_C_ADDR—Offset 65850h

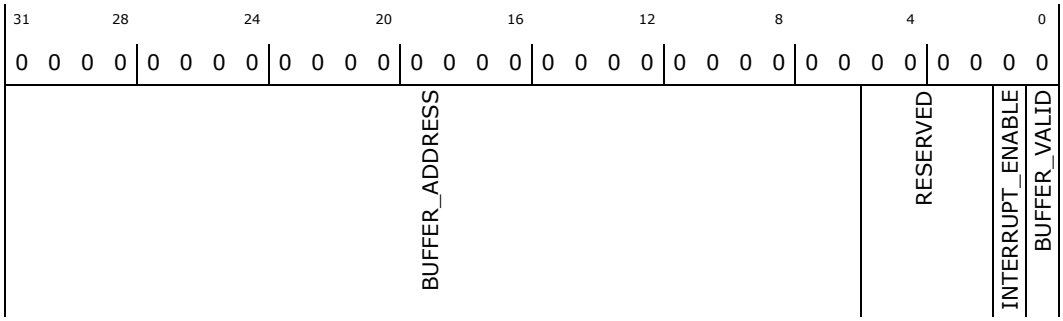
Address for Audio Buffer C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65850h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0x0 RO	**RESERVED:** Reserved.
1	0x0 RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0x0 RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

4.3.82 STREAM_B_LPE_AUD_BUF_C_LENGTH—Offset 65854h

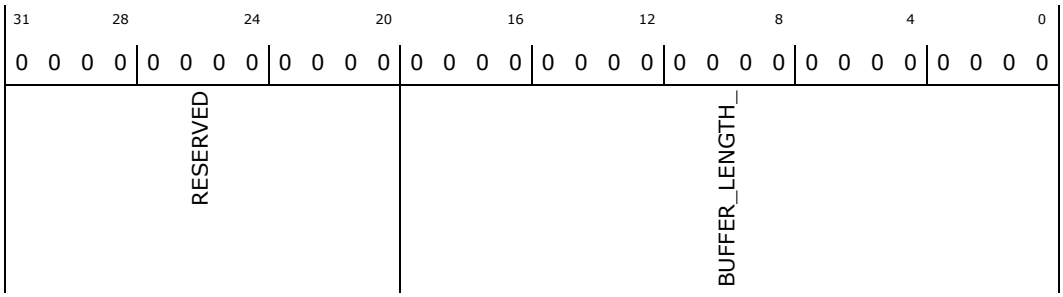
Length for Audio Buffer C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65854h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
19:0	0x0 RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

4.3.83 STREAM_B_LPE_AUD_BUF_D_ADDR—Offset 65858h

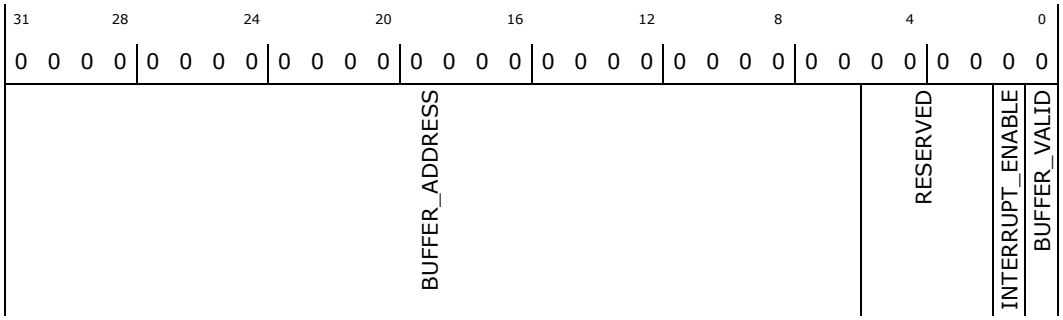
Address for Audio Buffer D

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65858h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0x0 RO	**RESERVED:** Reserved.
1	0x0 RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0x0 RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

4.3.84 STREAM_B_LPE_AUD_BUF_D_LENGTH—Offset 6585Ch

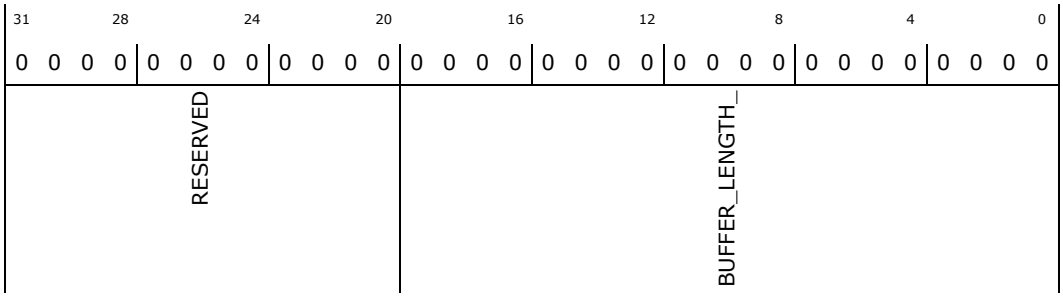
Length for Audio Buffer D

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6585Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RESERVED:** Reserved.
19:0	0x0 RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

4.3.85 STREAM_B_LPE_AUD_CNTL_ST—Offset 65860h

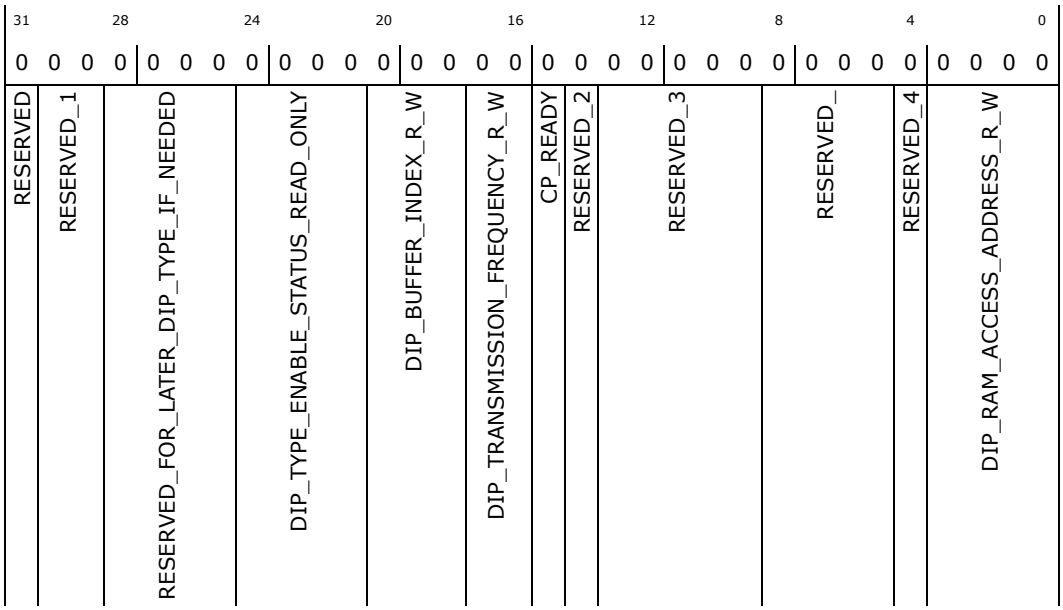
LPE Audio Control State Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65860h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** Reserved.
30:29	0x0 RO	**RESERVED_1:**
28:25	0x0 RO	**RESERVED_FOR_LATER_DIP_TYPE_IF_NEEDED:** Must be 0.
24:21	0x0 RO	**DIP_TYPE_ENABLE_STATUS_READ_ONLY:** These bits reflects the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling an DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP. XXX1 = Audio DIP enable status (Default = disabled) XX1X = Generic 1 (ACP) DIP enable status (Default = disabled) X1XX = Generic 2 DIP enable status, can be used by ISRC1 or ISRC2 (Default = disabled) 1XXX = Reserved AccessType: Read Only
20:18	0x0 RW	**DIP_BUFFER_INDEX_R_W:** This field is used during read or write of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0 s. 000 = (Default) Audio DIP (31 bytes of address space, 13 bytes of data) 001 = Generic 1 (ACP) Data Island Packet (31 bytes of address space, 11 bytes of data) 010 = Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data) 011 = Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data) 1XX = reserved
17:16	0x0 RW	**DIP_TRANSMISSION_FREQUENCY_R_W:** These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written.When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18. 00 = Disabled (Default) 01 = once per frame 10 = Send once 11 = Best effort (Send at least every other vsync)
15	0x0 RW	**CP_READY:** This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. 0 = CP request pending or not ready to receive requests (default) 1 = CP request ready CP_ready bit is programmable through Bit 14 for [DevCL, DevBLC]. CP_ready bit is programmable through Bit 15 for [DevCTG]. Bit 15 Reserved for [DevCL, DevBLC].

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RO	**RESERVED_2:** ELD valid: This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit. 0 = ELD data invalid (default, when writing ELD data, set 0 by software) 1 = ELD data valid (Set by video software only) ELD bit is programmable through Bit 13 for [DevCL, DevBLC]. ELD bit is programmable through Bit 14 for [DevCTG].
13:9	0x0 RO	**RESERVED_3:** ELD buffer size (read only)10000 = This field reflects the size of the ELD buffer in DWORDs 13:9 reflects ELD buffer size for [DevCTG]. 12:9 reflects ELD buffer size for [DevCL, DevBLC].
8:5	0x0 RO	**RESERVED_:** ELD access address (R/W): Selects the DWORD address for access to the ELD buffer (48 bytes). The value wraps back to zero when incremented past the max addressing value 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.
4	0x0 RO	**RESERVED_4:** ELD ACK: Acknowledgement from the audio driver that ELD read has been completed
3:0	0x0 RW	**DIP_RAM_ACCESS_ADDRESS_R_W:** Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

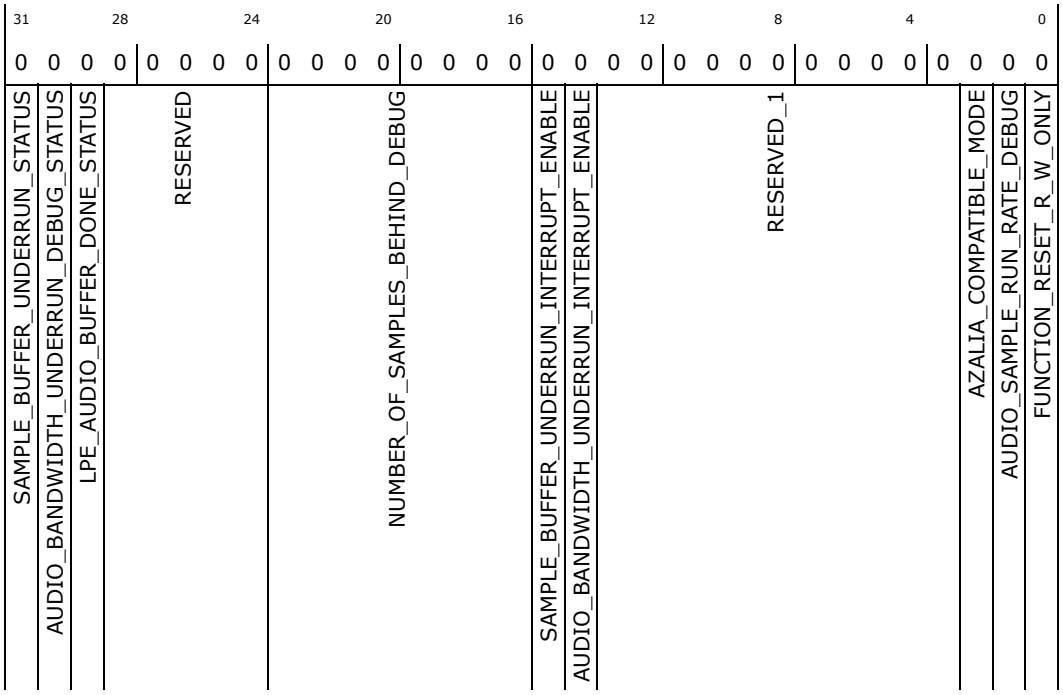
4.3.86 STREAM_B_LPE_AUD_HDMI_STATUS—Offset 65864h

LPE Audio Status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65864h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C	**SAMPLE_BUFFER_UNDERRUN_STATUS:** This bit indicates an underrun in the sample buffer to HDMI/DP controller when it needs to send. This bit is set at the last line of active video when there are no more sample in any valid buffers and HDMI/DP audio unit has not satisfied number of audio samples intended in that video frame. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. AccessType: One to Clear
30	0x0 RW/1C	**AUDIO_BANDWIDTH_UNDERRUN_DEBUG_STATUS:** This bit indicates an underrun of audio samples at HDMI audio packet assembly even there is still available sample buffers. Audio bandwidth underrun should not happen in normal functionality but it may happen when audio setting is unappropriate and/or memory bus was blocked by other clients, etc... This bit is set at the last line of active video when there is valid samples in a valid buffer and HDMI audio unit has not satisfied number of audio samples intended in that video frame Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. AccessType: One to Clear
29	0x0 RW/1C	**LPE_AUDIO_BUFFER_DONE_STATUS:** This bit is set when a LPE audio buffer is completed transferred all of its data to LPE audio unit. This bit is clear when write 1 to it AccessType: One to Clear
28:24	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0x0 RO	**NUMBER_OF_SAMPLES_BEHIND_DEBUG:** This field is read only to get the number of audio samples that controller needs to load and send at the time of reading. AccessType: Read Only
15	0x0 RW	**SAMPLE_BUFFER_UNDERRUN_INTERRUPT_ENABLE:** This bit is to enable the first line buffer underrun interrupt when sample buffer underrun status is detected 0 = LPE sample Buffer Underrun Interrupt Disabled 1 = LPE sample Buffer Underrun Interrupt Enabled
14	0x0 RW	**AUDIO_BANDWIDTH_UNDERRUN_INTERRUPT_ENABLE:** This bit is to enable the first line bandwidth underrun interrupt when bandwidth underrun status is detected 0 = LPE Bandwidth Underrun Interrupt Disabled 1 = LPE Bandwidth Underrun Interrupt Enabled
13:3	0x0 RO	**RESERVED_1:** Reserved.
2	0x0 RW	**AZALIA_COMPATIBLE_MODE:** This bit is to enable the vucp, PR, ECC to be generated in the Azalia way 0 = Disable Azalia compatible mode on vucp, PR, ECC 1 = Enable Azalia compatible mode on vucp, PR, ECC
1	0x0 RW	**AUDIO_SAMPLE_RUN_RATE_DEBUG:** When set it allows to fetch sample 128 times than the real sample rate to allow a faster drain of sample buffers.
0	0x0 RW	**FUNCTION_RESET_R_W_ONLY:** Write 1 to this bit will reset hardware within audio unit without needs of reset the full display controller. The FIFO and pointers will be reset and audio registers will be reset to default values. Write 0 will put the unit back to idle and ready to be programmed again.

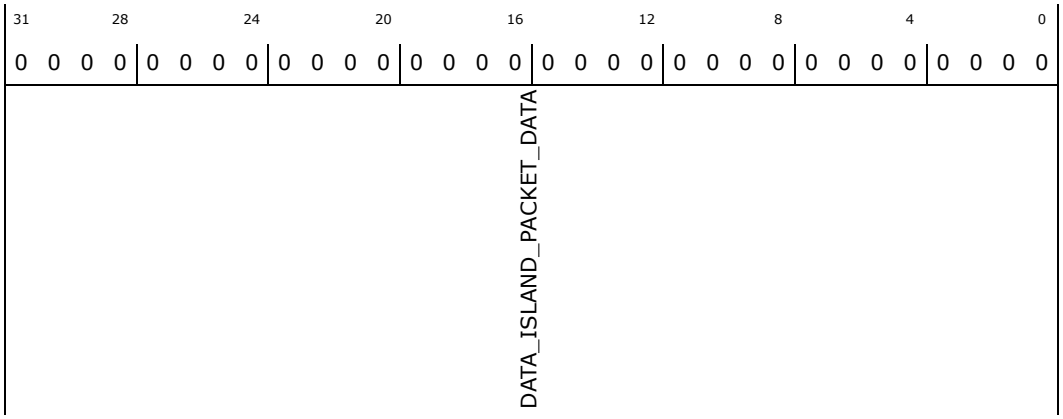
4.3.87 STREAM_B_LPE_AUD_HDMIW_INFOFR—Offset 65868h

Audio HDMI Data Island Packet Data

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65868h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DATA_ISLAND_PACKET_DATA:** When read, this returns the current value at the location specified in the Video DIP buffer index select and Video DIP RAM access address fields. The index used to address the RAM is incremented after each read or write of this register. DIP data can be read at any time. Data should be loaded into the RAM before enabling the transmission through the DIP type enable bit. Accesses to this register are on a per-DWORD basis

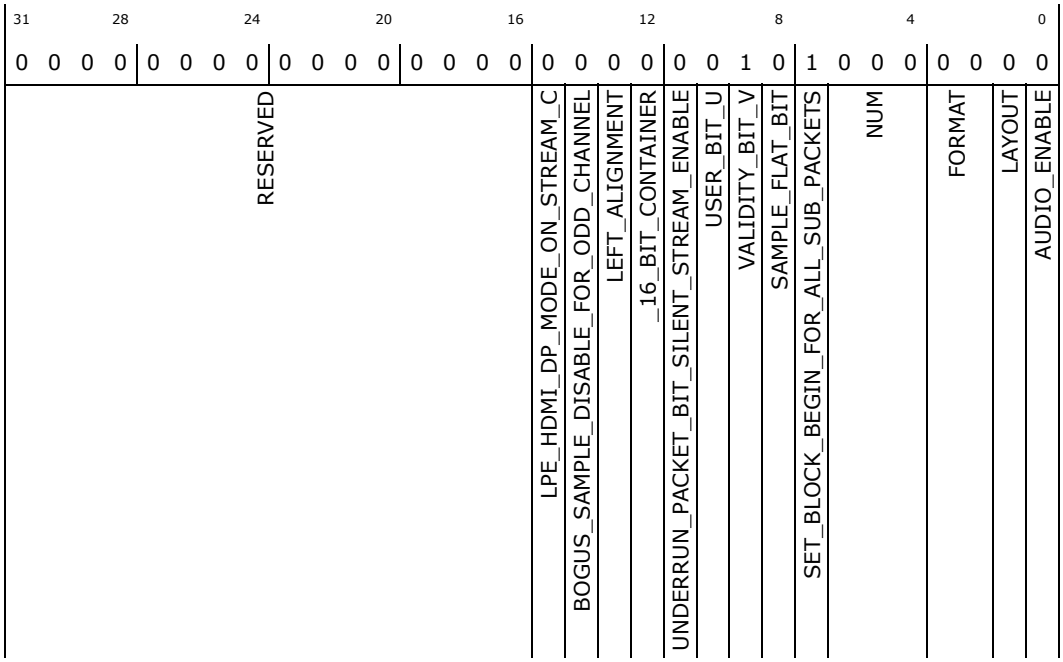
4.3.88 STREAM_C_LPE_AUD_CONFIG—Offset 65900h

LPE Audio Configuration

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65900h

Default: 00000280h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Reserved.
15	0x0 RW	**LPE_HDMI_DP_MODE_ON_STREAM_C:** 1= DP mode 0 = HDMI mode (default)
14	0x0 RW	**BOGUS_SAMPLE_DISABLE_FOR_ODD_CHANNEL:** When number of channels in a sample is odd (3, 5, or 7) source application may pad a bogus sample to the next even number of channels. If this bit is set there is no padding in input buffer1= No bogus sample present in buffer for odd number of channels 0= Bogus sample present in buffer for odd number of channels (default)
13	0x0 RW	**LEFT_ALIGNMENT:** When input buffer is in 32-bit container mode. If this bit is set the MSB of audio sample is aligned bit 31 of the container if this bit is clear MSB of audio sample is aligned with bit 23 of the container.1= MSB is bit 31 of 32-bit container 0= MSB is bit 23 of 32-bit container (default)
12	0x0 RW	**_16_BIT_CONTAINER:** When this bit is set 16-bit sample is stored in 16-bit container format. When it is clear container is 32-bit for each sample regardless of valid bits (default)1= 16-bit container 0= 32-bit container
11	0x0 RW	**UNDERRUN_PACKET_BIT_SILENT_STREAM_ENABLE:** Set this bit will enble HW to send valid zero-filled packet with Sample flat bit set when no sample buffer is available, NCTS packets (or Timesstamp packet) are sent to keep sink in sync even no audio sound will heard.1= send underrun packets (silent stream) 0= send null packets (default)

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RW	**USER_BIT_U:** HW will clear this bit in each sub-frames it sends, But this bit allows to overwrite hardware setting for special operation like debug or testing for compliance 1= sey U bit in sub-frame 0= clear U bit in sub-frame (default)
9	0x1 RW	**VALIDITY_BIT_V:** HW will set this bit in both each sub-frames it sends. But this bit allows to overwrite hardware setting for special operation like debug or testing for compliance 1= Set V bit in sub-frame (default) 0= clear V bit in sub-frame. For debug or testing
8	0x0 RW	**SAMPLE_FLAT_BIT:** When set the sample flat bit will be set in all HDMI sub-packets. 1= flat bit is set for valid sample 0= flat bit is not set for valid sample (default)
7	0x1 RW	**SET_BLOCK_BEGIN_FOR_ALL_SUB_PACKETS:** Controls the B bit in the header of only the first Audio Packet /frame of a 192 frame 60958 block in Layout 1 mode. This bit only applies to LPE HDMI mode. 0: The B bit will be set only for sub-packet 0 1: The B bit in the Audio sample packet header will be set for all valid sub-packets. (default)
6:4	0x0 RW	**NUM:** audio Channels 000: 2 channels (stereo) 001: 3 channels 010: 4 channels 011: 5 channels 100: 6 channels 101: 7 channels 110: 8 channels Note: When disable_bogus sample bit is clear HW will always treat odd number of channels similar to the next higher even number. Thus 3 is similar to 4, 5 to 6 and 7 to 8. This is because SW ensures that an even number of samples are packed in the audio buffers.
3:2	0x0 RW	**FORMAT:** 00: L-PCM or IEC 61937 01: High Bit Rate IEC 61937 stream packet (not supported) 10: One Bit Audio Sample packet (not supported) 11: DST Audio Sample packet (not supported)
1	0x0 RW	**LAYOUT:** 0: Layout 0 (2-ch) 1: Layout 1 (3-8 ch) Note: Layout bit does not matter for HBR
0	0x0 RW	**AUDIO_ENABLE:** Controls generation of N/CTS and transmission of audio sample packets. 0: Audio sample packets are not transmitted, CTS calculation/transmission is disabled 1: Audio sample packets are transmitted and CTS calculation is enabled When enable audio unit will wait until the next vertical blank period before sending out the audio packets. When disable, audio unit may continue to send audio packet until the end of current active video frame before stopping.

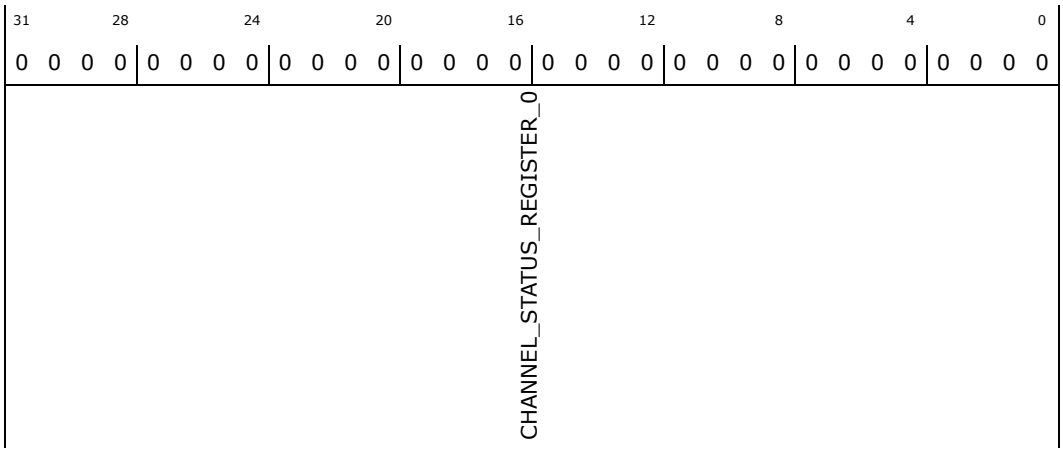
4.3.89 STREAM_C_LPE_AUD_CH_STATUS_0—Offset 65908h

Audio Channel Status Attributes 0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65908h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**CHANNEL_STATUS_REGISTER_0:** . These bits are transmitted as attributes of audio packets

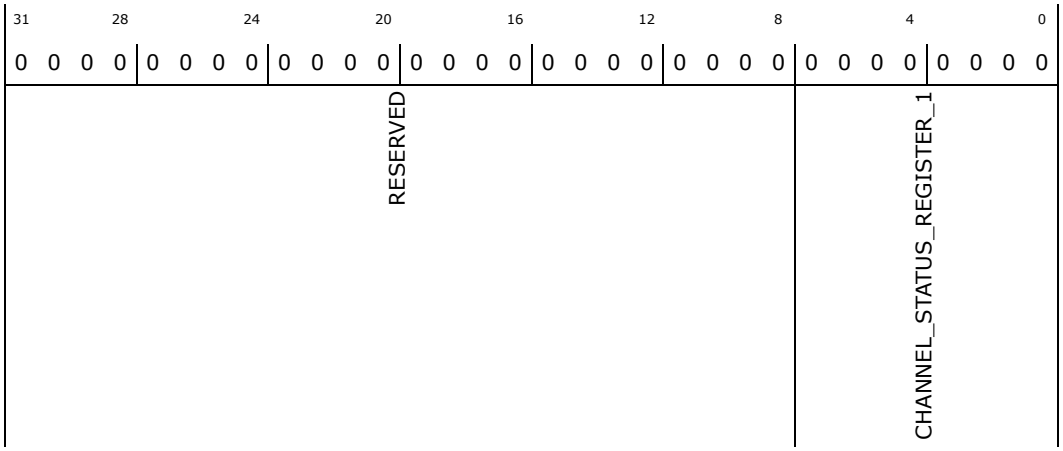
4.3.90 STREAM_C_LPE_AUD_CH_STATUS_1—Offset 6590Ch

Audio Channel Status Attributes 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6590Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED:** Reserved.
7:0	0x0 RW	**CHANNEL_STATUS_REGISTER_1:** . These bits are transmitted as attributes of audio packets. There is only 8 bits valid in this register.

4.3.91 STREAM_C_LPE_AUD_HDMI_CTS_DP_MAUD—Offset 65910h

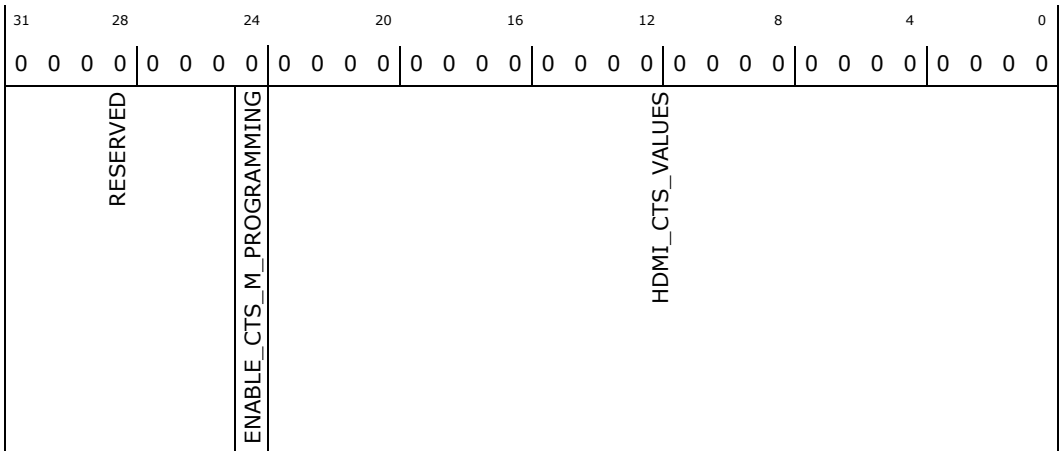
Audio HDMI CTS Register (DP Maud)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65910h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RESERVED:** Reserved.
24	0x0 RW	**ENABLE_CTS_M_PROGRAMMING:** 1 = Enable CTS/M programming 0 = Disable CTS/M programming
23:0	0x0 RW	**HDMI_CTS_VALUES:** These are bits [23:0] of programmable HDMI CTS values (or DP Maud) that is pre-calculated to achieve desired audio sample rates with a particular pixel clocks configuration. Audio function must be disabled when changing this field. Bit 24 also need to write to 1 to enable this field.

4.3.92 STREAM_C_LPE_AUD_HDMI_N_DP_NAUD—Offset 65914h

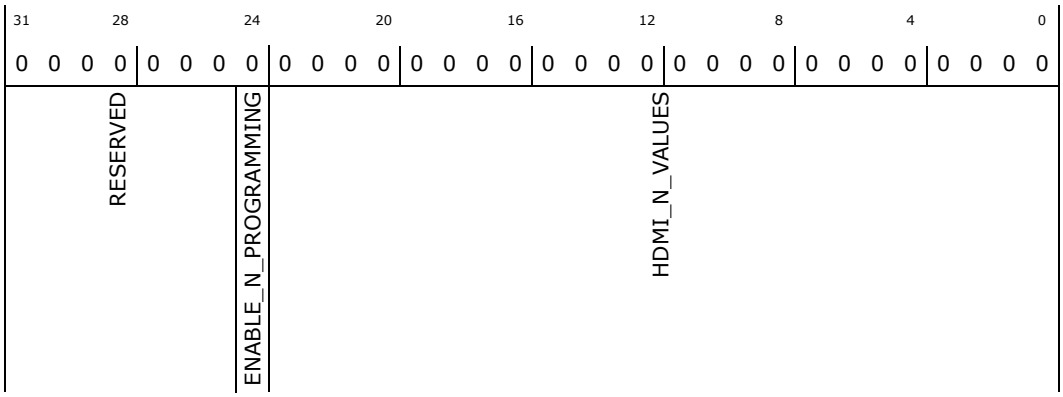
Audio HDMI N Register (DP Naud)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65914h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RESERVED:** Reserved.
24	0x0 RW	**ENABLE_N_PROGRAMMING:** 1 = Enable N programming 0 = Disable N programming
23:0	0x0 RW	**HDMI_N_VALUES:** These are bits [23:0] of programmable HDMI N (or DP Naud) values that is pre-calculated to achieve desired audio sample rates with a particular pixel clocks configuration. Audio function must be disabled when changing this field. Bit 24 also need to write to 1 to enable this field.

4.3.93 STREAM_C_LPE_AUD_BUFFER_CONFIG—Offset 65920h

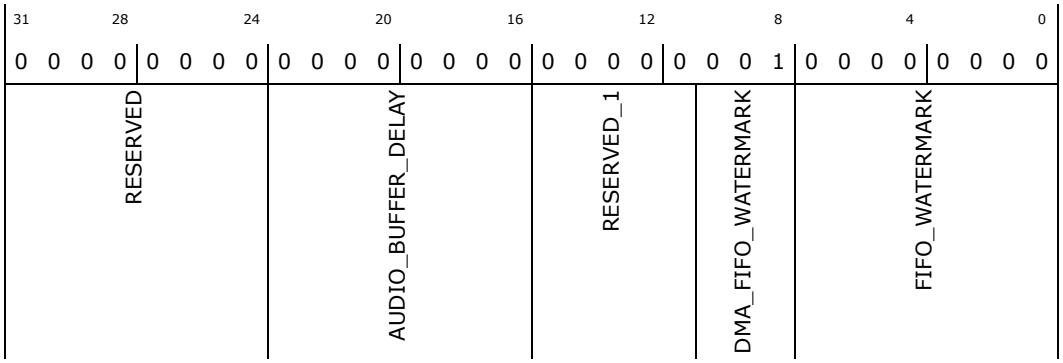
LPE Audio buffer config

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65920h

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:16	0x0 RW	**AUDIO_BUFFER_DELAY:** This field specifies a delay in number of video frames that the audio controller will count off when audio enable bit is set before start transmitting audio sample.
15:11	0x0 RO	**RESERVED_1:** .
10:8	0x1 RW	**DMA_FIFO_WATERMARK:** Audio unit has a 8x64 bytes fifo for pre-fetching and staging audio samples. This register provides a watermark value in SWORDs (64B). When enable and sample buffer is available audio unit will fetch samples until this FIFO is full then it waits until HDMI/DP packet assembler drains the samples to a level less or equal the watermark setting then it will start fetching the samples again. Default value is 1 cacheline (SW).
7:0	0x0 RW	**FIFO_WATERMARK:** Audio unit has a 8x96 bytes fifo for pre-fetching and staging audio samples. This register provides a watermark value in DWORDs. When enable and sample buffer is available audio unit will fetch samples until this FIFO is full then it waits until HDMI packet assembler drains the samples to a level less or equal the watermark setting then it will start fetching the samples again

4.3.94 STREAM_B_LPE_AUD_BUF_CH_SWP (STREAM_C_LPE_AUD_BUF_CH_SWP)—Offset 65924h

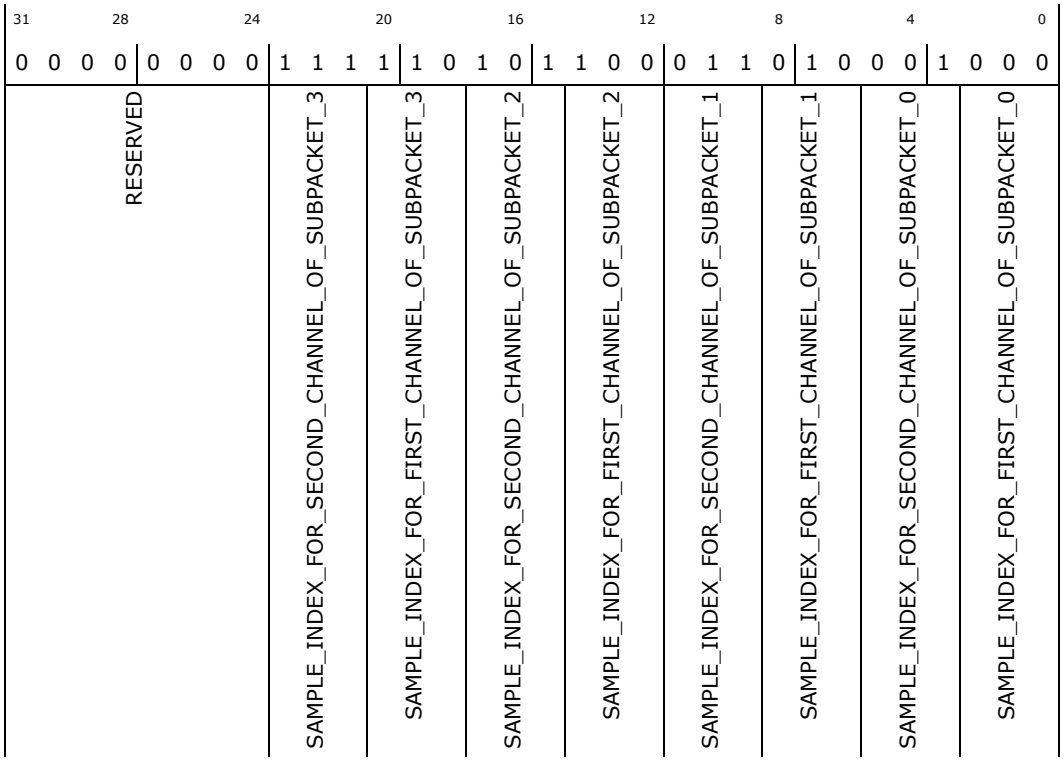
Audio Sample Swapping

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65924h

Default: 00FAC688h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:21	0x7 RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_3:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 3 in a HDMI audio packet
20:18	0x6 RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_3:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 1 in a HDMI audio packet
17:15	0x5 RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_2:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 0 in a HDMI audio packet
14:12	0x4 RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_2:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 0 in a HDMI audio packet
11:9	0x3 RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_1:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 1 in a HDMI audio packet
8:6	0x2 RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_1:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 1 in a HDMI audio packet

Bit Range	Default & Access	Field Name (ID): Description
5:3	0x1 RO	**SAMPLE_INDEX_FOR_SECOND_CHANNEL_OF_SUBPACKET_0:** This field has the index of 32-byte buffer block that will be send out as the second channel sample of subpacket 0 in a HDMI audio packet
2:0	0x0 RO	**SAMPLE_INDEX_FOR_FIRST_CHANNEL_OF_SUBPACKET_0:** This field has the index of 32-byte buffer block that will be send out as the first channel sample of subpacket 0 in a HDMI audio packet

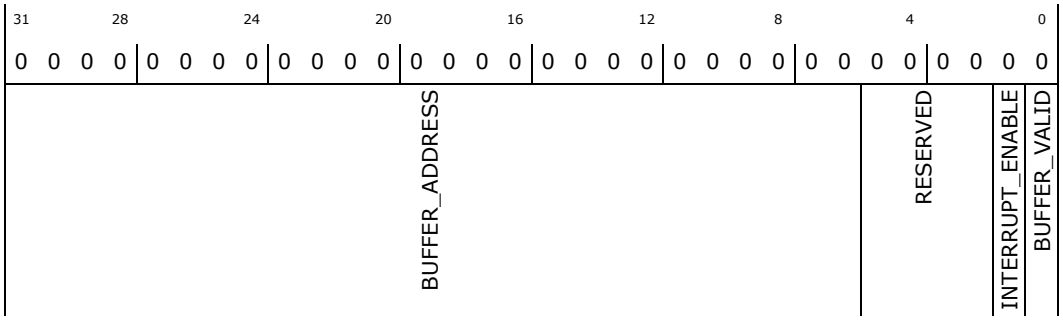
4.3.95 STREAM_C_LPE_AUD_BUF_A_ADDR—Offset 65940h

Address for Audio Buffer A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65940h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0x0 RO	**RESERVED:** Reserved.
1	0x0 RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0x0 RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

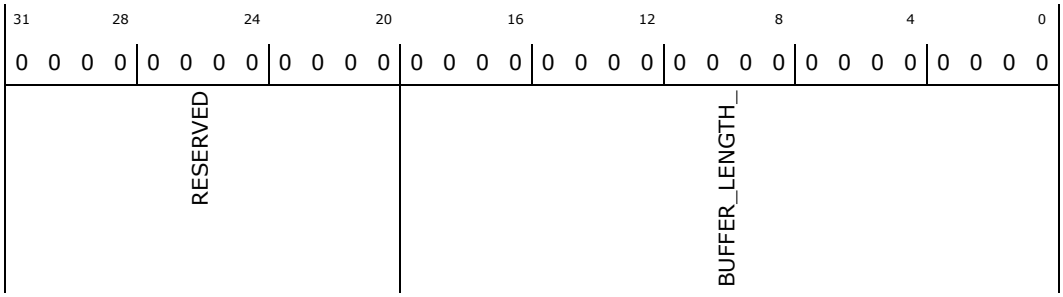
4.3.96 STREAM_C_LPE_AUD_BUF_A_LENGTH—Offset 65944h

Length for Audio Buffer A

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65944h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RESERVED:** Reserved.
19:0	0x0 RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

4.3.97 STREAM_C_LPE_AUD_BUF_B_ADDR—Offset 65948h

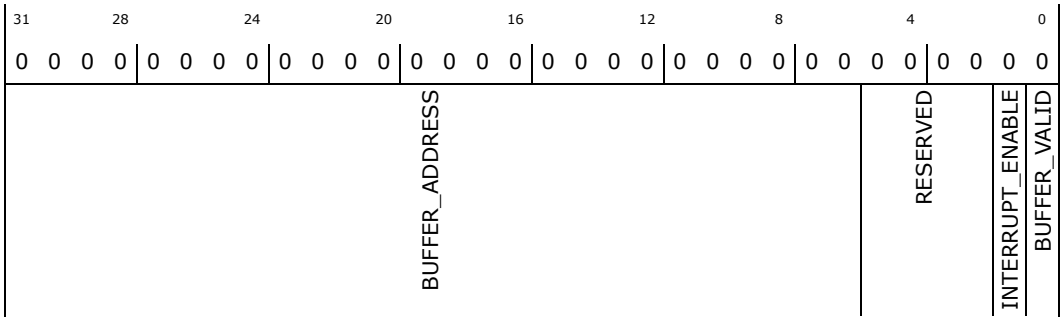
Address for Audio Buffer B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65948h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0x0 RO	**RESERVED:** Reserved.
1	0x0 RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

4.3.98 STREAM_C_LPE_AUD_BUF_B_LENGTH—Offset 6594Ch

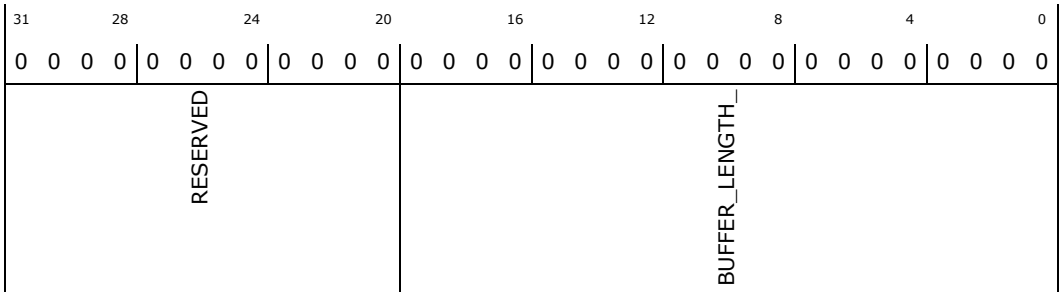
Length for Audio Buffer B

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6594Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RESERVED:** Reserved.
19:0	0x0 RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

4.3.99 STREAM_C_LPE_AUD_BUF_C_ADDR—Offset 65950h

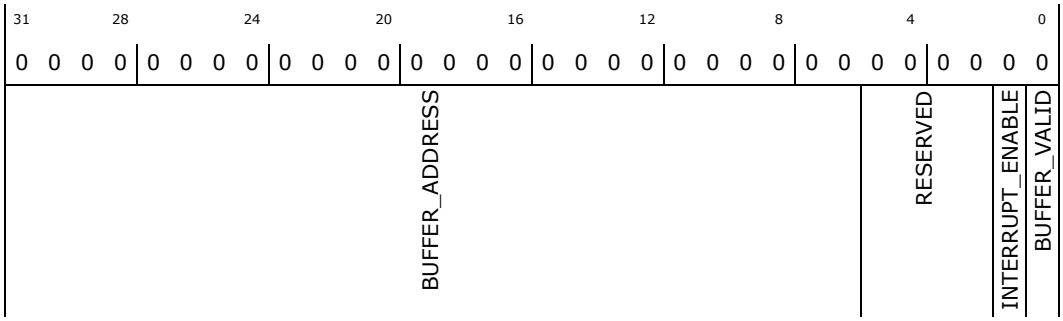
Address for Audio Buffer C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65950h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0x0 RO	**RESERVED:** Reserved.
1	0x0 RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0x0 RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

4.3.100 STREAM_C_LPE_AUD_BUF_C_LENGTH—Offset 65954h

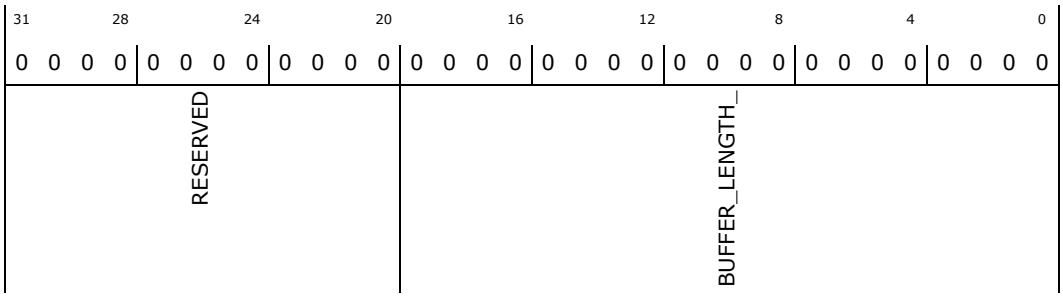
Length for Audio Buffer C

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65954h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
19:0	0x0 RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

4.3.101 STREAM_C_LPE_AUD_BUF_D_ADDR—Offset 65958h

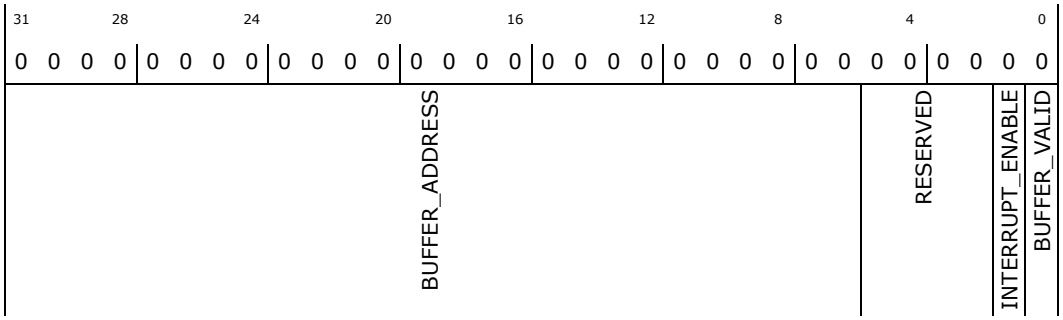
Address for Audio Buffer D

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 65958h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**BUFFER_ADDRESS:** . This is physical address of audio sample buffer A, need to 64-byte aligned.
5:2	0x0 RO	**RESERVED:** Reserved.
1	0x0 RW	**INTERRUPT_ENABLE:** If enable hardware will generate an interrupt when it is done fetching this buffer
0	0x0 RW	**BUFFER_VALID:** . This bit is set by S/W when the mem_addr is written and is cleared by H/W when done reading the data from memory

4.3.102 STREAM_C_LPE_AUD_BUF_D_LENGTH—Offset 6595Ch

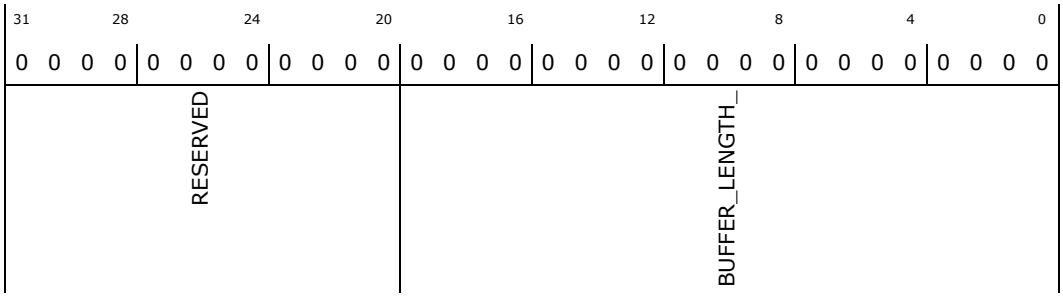
Length for Audio Buffer D

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6595Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RESERVED:** Reserved.
19:0	0x0 RW	**BUFFER_LENGTH_:** This field shows the remaining length of data that needs to be read from memory; Initially set by S/W for total of bytes that are valid and is decremented by H/W as reads are issued. Software must end buffer at the boundary of a audio sample with all of channel values of that sample are valid.

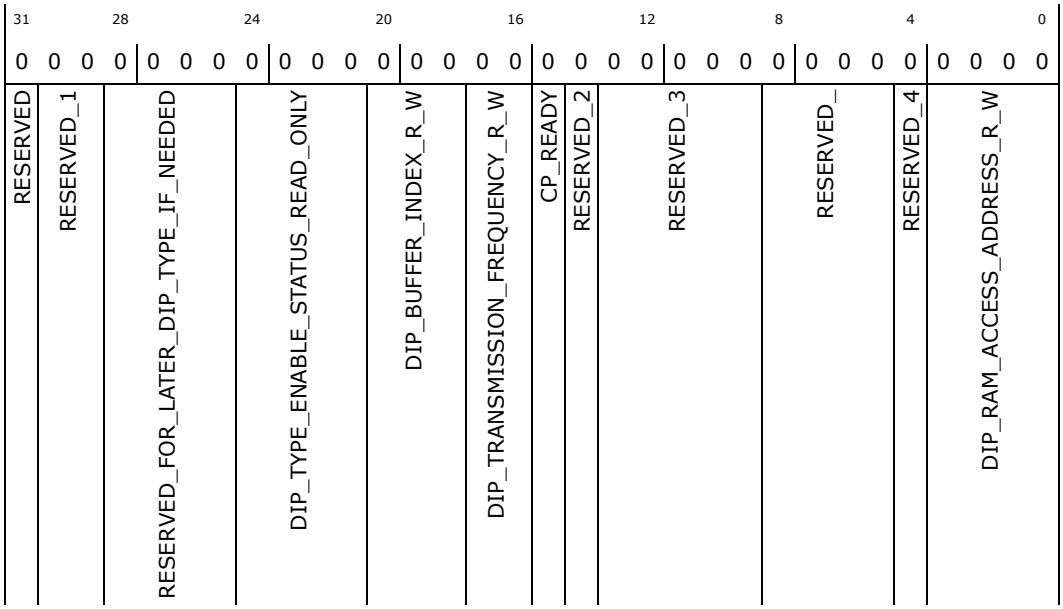
4.3.103 STREAM_C_LPE_AUD_CNTL_ST—Offset 65960h

LPE Audio Control State Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65960h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** Reserved.
30:29	0x0 RO	**RESERVED_1:**
28:25	0x0 RO	**RESERVED_FOR_LATER_DIP_TYPE_IF_NEEDED:** Must be 0.
24:21	0x0 RO	**DIP_TYPE_ENABLE_STATUS_READ_ONLY:** These bits reflects the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling an DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP. XXX1 = Audio DIP enable status (Default = disabled) XX1X = Generic 1 (ACP) DIP enable status (Default = disabled) X1XX = Generic 2 DIP enable status, can be used by ISRC1 or ISRC2 (Default = disabled) 1XXX = Reserved AccessType: Read Only
20:18	0x0 RW	**DIP_BUFFER_INDEX_R_W:** This field is used during read or write of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0 s. 000 = (Default) Audio DIP (31 bytes of address space, 13 bytes of data) 001 = Generic 1 (ACP) Data Island Packet (31 bytes of address space, 11 bytes of data) 010 = Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data) 011 = Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data) 1XX = reserved
17:16	0x0 RW	**DIP_TRANSMISSION_FREQUENCY_R_W:** These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written.When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18. 00 = Disabled (Default) 01 = once per frame 10 = Send once 11 = Best effort (Send at least every other vsync)
15	0x0 RW	**CP_READY:** This R/W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced. 0 = CP request pending or not ready to receive requests (default) 1 = CP request ready CP_ready bit is programmable through Bit 14 for [DevCL, DevBLC]. CP_ready bit is programmable through Bit 15 for [DevCTG]. Bit 15 Reserved for [DevCL, DevBLC].

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RO	**RESERVED_2:** ELD valid: This R/W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit. 0 = ELD data invalid (default, when writing ELD data, set 0 by software) 1 = ELD data valid (Set by video software only) ELD bit is programmable through Bit 13 for [DevCL, DevBLC]. ELD bit is programmable through Bit 14 for [DevCTG].
13:9	0x0 RO	**RESERVED_3:** ELD buffer size (read only)10000 = This field reflects the size of the ELD buffer in DWORDs 13:9 reflects ELD buffer size for [DevCTG]. 12:9 reflects ELD buffer size for [DevCL, DevBLC].
8:5	0x0 RO	**RESERVED_:** ELD access address (R/W): Selects the DWORD address for access to the ELD buffer (48 bytes). The value wraps back to zero when incremented past the max addressing value 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.
4	0x0 RO	**RESERVED_4:** ELD ACK: Acknowledgement from the audio driver that ELD read has been completed
3:0	0x0 RW	**DIP_RAM_ACCESS_ADDRESS_R_W:** Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

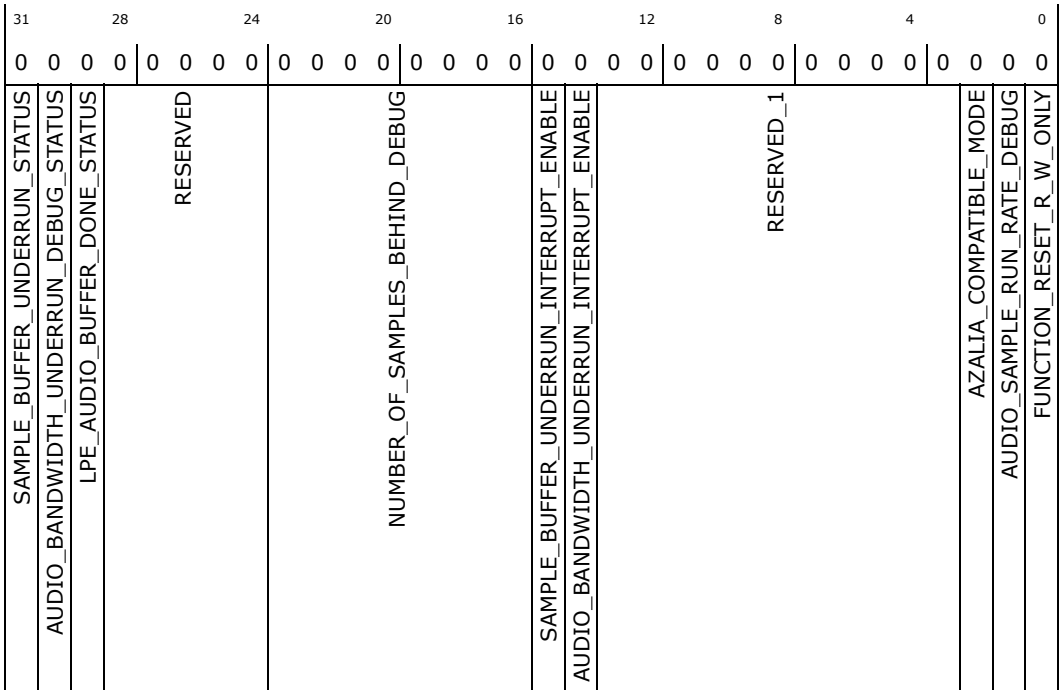
4.3.104 STREAM_C_LPE_AUD_HDMI_STATUS—Offset 65964h

LPE Audio Status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65964h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C	**SAMPLE_BUFFER_UNDERRUN_STATUS:** This bit indicates an underrun in the sample buffer to HDMI/DP controller when it needs to send. This bit is set at the last line of active video when there are no more sample in any valid buffers and HDMI/DP audio unit has not satisfied number of audio samples intended in that video frame. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. AccessType: One to Clear
30	0x0 RW/1C	**AUDIO_BANDWIDTH_UNDERRUN_DEBUG_STATUS:** This bit indicates an underrun of audio samples at HDMI audio packet assembly even there is still available sample buffers. Audio bandwidth underrun should not happen in normal functionality but it may happen when audio setting is unappropriate and/or memory bus was blocked by other clients, etc... This bit is set at the last line of active video when there is valid samples in a valid buffer and HDMI audio unit has not satisfied number of audio samples intended in that video frame Clearing this status bit is accomplished by writing a 1 to this bit through MMIO. AccessType: One to Clear
29	0x0 RW/1C	**LPE_AUDIO_BUFFER_DONE_STATUS:** This bit is set when a LPE audio buffer is completed transferred all of its data to LPE audio unit. This bit is clear when write 1 to it AccessType: One to Clear
28:24	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0x0 RO	**NUMBER_OF_SAMPLES_BEHIND_DEBUG:** This field is read only to get the number of audio samples that controller needs to load and send at the time of reading. AccessType: Read Only
15	0x0 RW	**SAMPLE_BUFFER_UNDERRUN_INTERRUPT_ENABLE:** This bit is to enable the first line buffer underrun interrupt when sample buffer underrun status is detected 0 = LPE sample Buffer Underrun Interrupt Disabled 1 = LPE sample Buffer Underrun Interrupt Enabled
14	0x0 RW	**AUDIO_BANDWIDTH_UNDERRUN_INTERRUPT_ENABLE:** This bit is to enable the first line bandwidth underrun interrupt when bandwidth underrun status is detected 0 = LPE Bandwidth Underrun Interrupt Disabled 1 = LPE Bandwidth Underrun Interrupt Enabled
13:3	0x0 RO	**RESERVED_1:** Reserved.
2	0x0 RW	**AZALIA_COMPATIBLE_MODE:** This bit is to enable the vucp, PR, ECC to be generated in the Azalia way 0 = Disable Azalia compatible mode on vucp, PR, ECC 1 = Enable Azalia compatible mode on vucp, PR, ECC
1	0x0 RW	**AUDIO_SAMPLE_RUN_RATE_DEBUG:** When set it allows to fetch sample 128 times than the real sample rate to allow a faster drain of sample buffers.
0	0x0 RW	**FUNCTION_RESET_R_W_ONLY:** Write 1 to this bit will reset hardware within audio unit without needs of reset the full display controller. The FIFO and pointers will be reset and audio registers will be reset to default values. Write 0 will put the unit back to idle and ready to be programmed again.

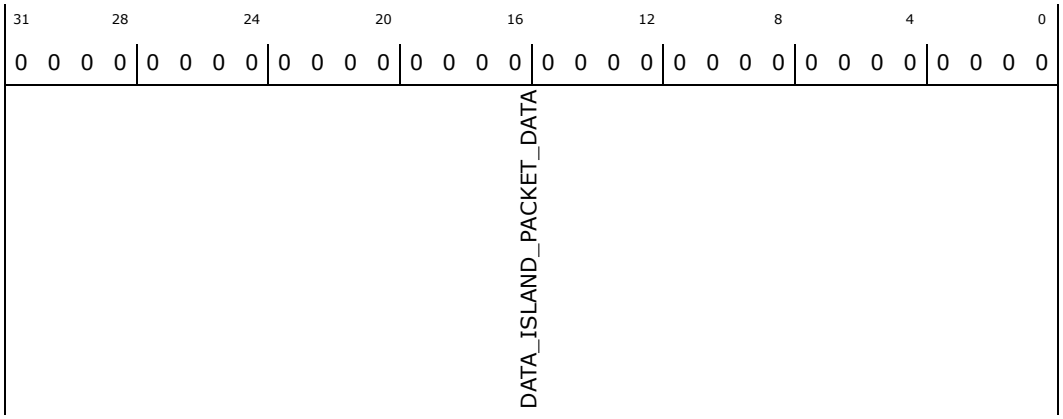
4.3.105 STREAM_C_LPE_AUD_HDMIW_INFOFR—Offset 65968h

Audio HDMI Data Island Packet Data

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 65968h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DATA_ISLAND_PACKET_DATA:** When read, this returns the current value at the location specified in the Video DIP buffer index select and Video DIP RAM access address fields. The index used to address the RAM is incremented after each read or write of this register. DIP data can be read at any time. Data should be loaded into the RAM before enabling the transmission through the DIP type enable bit. Accesses to this register are on a per-DWORD basis

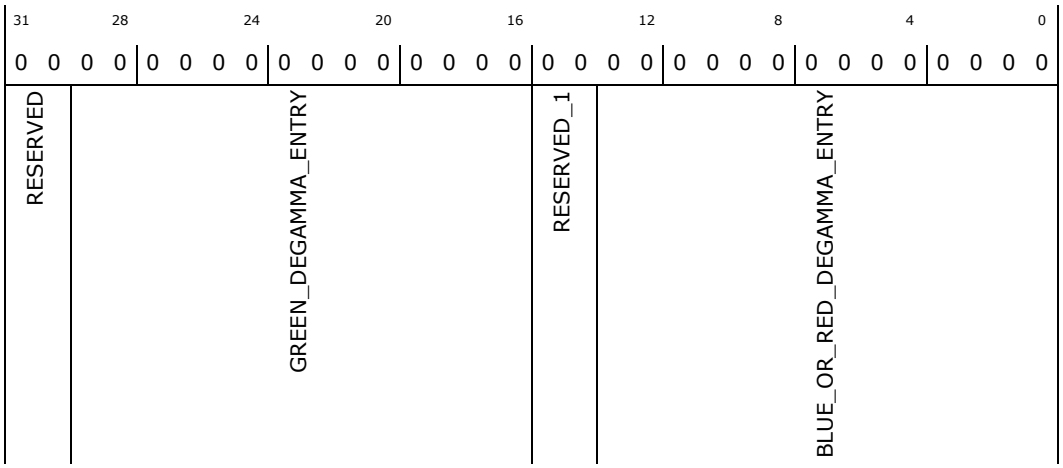
4.3.106 PIPEX_CGM_DEGAMME (PIPEX_CGM_DEGAMMA)—Offset 66000h

Pipe X Color Mapping DeGamma Table. The table has 65 logical entries which is 2 DWORDS as shown below:

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 66000h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RESERVED:** (read only).
29:16	0x0 RW	**GREEN_DEGAMMA_ENTRY:** Green DeGamma Entry is taken into consideration in DWORD0. For DWORD1, The entire 29:16 bits are in reserved section
15:14	0x0 RO	**RESERVED_1:** Reserved.
13:0	0x0 RW	**BLUE_OR_RED_DEGAMMA_ENTRY:** BLUE Entry for DWORD0 and RED Entry for DWORD0

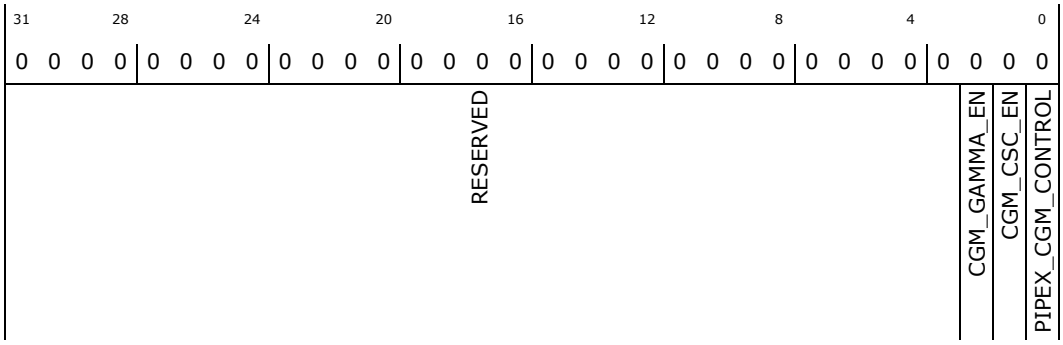
4.3.107 PIPEX_CGM_CONTROL—Offset 67A00h

Pipe X Color Mapping Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 67A00h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**RESERVED:** (read only).
2	0x0 RW	**CGM_GAMMA_EN:** 0=gamma disabled. 1=gamma enabled
1	0x0 RW	**CGM_CSC_EN:** 0=CSC IS DISABLED. 1=CSC IS ENABLED
0	0x0 RW	**CGM_DEGAMMA_EN (PIPEX_CGM_CONTROL):** 0=DEGAMMA IS DISABLED. 1=DEGAMMA IS ENABLED

4.3.108 PCPSXCONFIG—Offset 6D000h

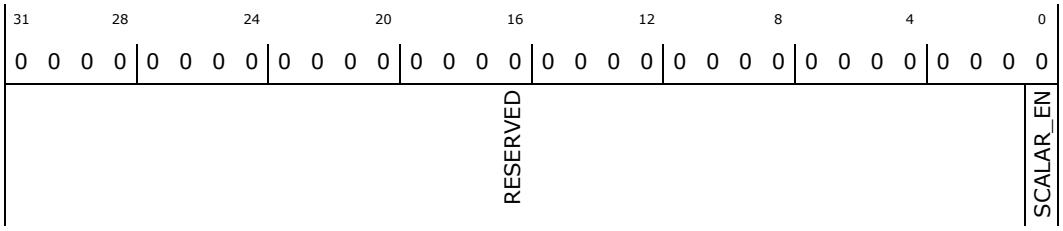
Config Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D000h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RESERVED:** (read only).
0	0x0 RW	**SCALAR_EN:** 0=Perform Scaling per programmed parameters. 1=bypass horizontal and vertical scalers. Other programmed parameters have no effect in this case

4.3.109 PCPSXHS_H—Offset 6D104h

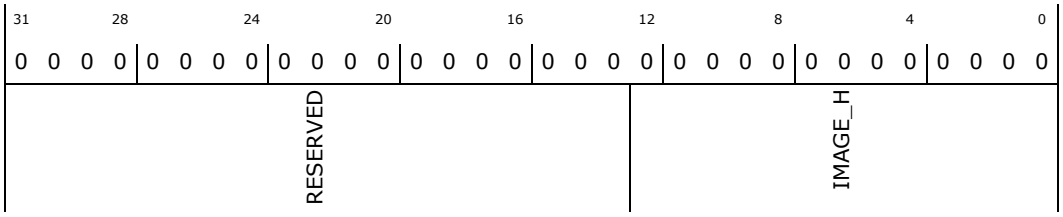
HSC Height Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D104h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RESERVED:** (read only).
12:0	0x0 RW	**IMAGE_H:** Image Height in terms of pixels. This must match the source height specified for the plane

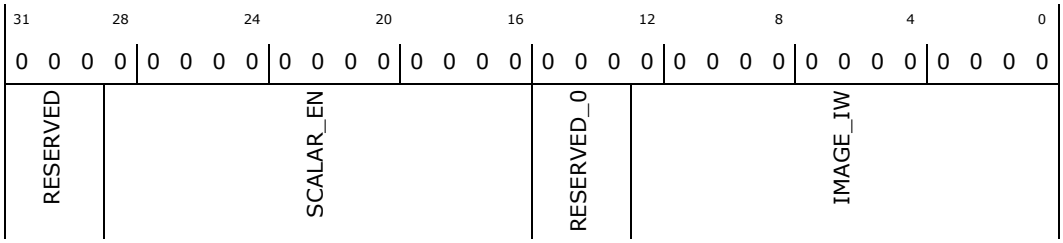
4.3.110 PCPSXHS_W—Offset 6D108h

HSC Width Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6D108h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** (read only).
28:16	0x0 RW	**IMAGE_OW (SCALAR_EN):** Image Output Width in terms of pixels.
15:13	0x0 RO	**RESERVED_0:** (read only).
12:0	0x0 RW	**IMAGE_IW:** Image input width

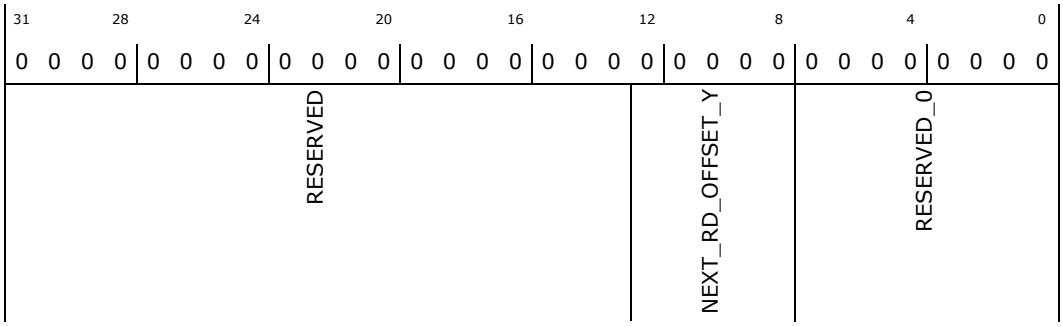
4.3.111 PCPSXHS_NBP—Offset 6D10Ch

Next Block Params Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6D10Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RESERVED:** (read only).

Bit Range	Default & Access	Field Name (ID): Description
12:8	0x0 RW	**Next_RD_OFFSET_Y (NEXT_RD_OFFSET_Y):** 1: Offset(mag) should be subtracted. 0:offset(mag) should be added
7:0	0x0 RO	**RESERVED_0:** (read only).

4.3.112 PCPSXHS_ISF—Offset 6D110h

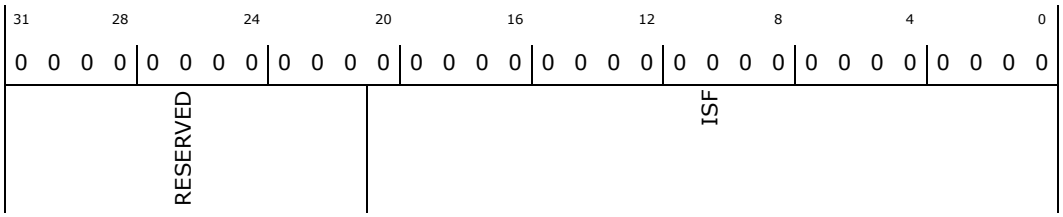
Inverse Scale Factor Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D110h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RO	**RESERVED:** (read only).
20:0	0x0 RW	**ISF:** Inverse Scale Factor. The format is 5.16 For Example, If the scaling Ratio is 4/7, the inverse scale factor is 7/4.

4.3.113 PCPSXHS_PC—Offset 6D114h

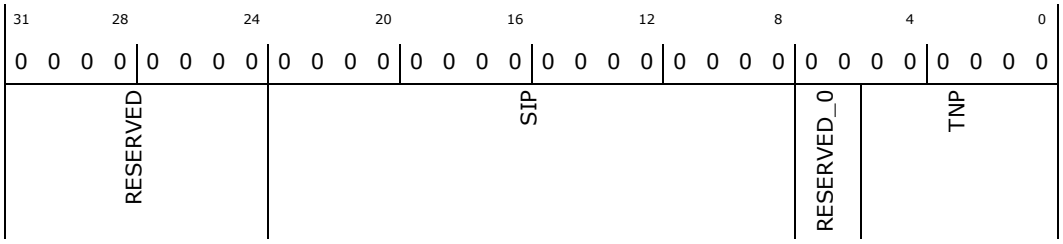
Phase Configuration Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D114h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** (read only).
23:8	0x0 RW	**SIP:** Scaled Initial Phase for the first pixel of every frame. This needs to be programmed to initial phase. The format of the SIP field is 0.16. Usage NOTE: While this field is technically programmable, the horizontal SIP does not change during regular usage. To Reduce validation overhead the only value of SIP tested is 0x7c00. This is the only value that should be programmed by SW.
7:6	0x0 RO	**RESERVED_0:** (read only).
5:0	0x0 RW	**TNP:** Total number of phases used in the filter bank. The horizontal scaler provides a max of 32 phases.

4.3.114 PCPSX HSC PolyPhase YCbCr Co efficient Memory (PCPSXHS_PM)—Offset 6D200h

Config Register

Access Method

Type: Memory Mapped I/O Register (Size: 128 bits) **Offset:** 6D200h

Default: 00000000000000000000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
127:108	0x0 RO	**RESERVED:** Reserved.
107:96	0x0 RO	**C8:** Co efficient 8
95:84	0x0 RO	**C7:** Co efficient 7
83:72	0x0 RO	**C6:** Co efficient 6
71:60	0x0 RO	**C5:** Co efficient 5-First 4 bits
59:48	0x0 RO	**C4:** Co efficient 4
47:36	0x0 RO	**C3:** Co efficient 3
35:24	0x0 RO	**C2:** Co efficient 2-First Half
23:12	0x0 RO	**C1:** Co efficient 1
11:0	0x0 RO	**C0:** Co efficient 0

4.3.115 PCPSX HSC PolyPhase YCbCr Co efficient Memory (PCPSXHS_APM)—Offset 6D300h

Config Register

Access Method

Type: Memory Mapped I/O Register (Size: 128 bits) **Offset:** 6D300h

Default: 00000000000000000000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
127:108	0x0 RO	**RESERVED:** Reserved.
107:96	0x0 RO	**C8:** Co efficient 8
95:84	0x0 RO	**C7:** Co efficient 7
83:72	0x0 RO	**C6:** Co efficient 6
71:60	0x0 RO	**C5:** Co efficient 5-First 4 bits
59:48	0x0 RO	**C4:** Co efficient 4
47:36	0x0 RO	**C3:** Co efficient 3
35:24	0x0 RO	**C2:** Co efficient 2-First Half
23:12	0x0 RO	**C1:** Co efficient 1
11:0	0x0 RO	**C0:** Co efficient 0

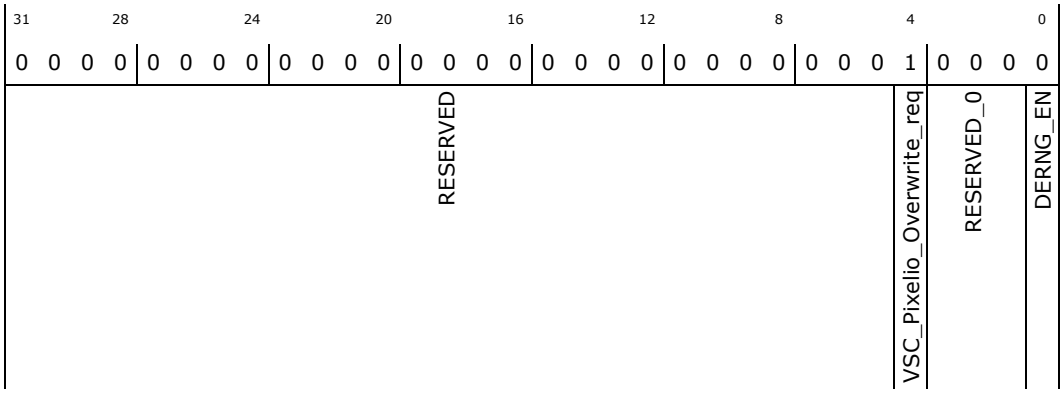
4.3.116 PCPSXVS_CTRL—Offset 6D500h

VSC Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6D500h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RO	**RESERVED:** (read only).
4	0x1 RW	**VSC_Pixelio_Overwrite_req:** Chicken bit: When this bit is set to 1, logic for controlling row incremental information update timing inside pixelio will overwrite pixel request signal.
3:1	0x0 RO	**RESERVED_0:** (read only).
0	0x0 RW	**DERNG_EN:** 1: Enable check and removal ringing pixels. 0:disable checking and removing pixels.

4.3.117 PCPSXVS_H—Offset 6D504h

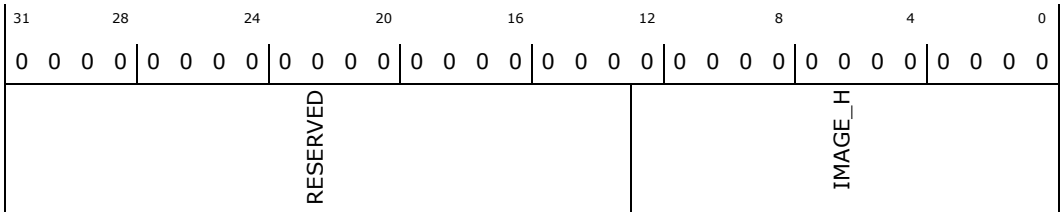
VSC Height Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D504h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RESERVED:** (read only).
12:0	0x0 RW	**IMAGE_H:** Image Height in terms of pixels. This must match the source height specified for the plane

4.3.118 PCPSXVS_W—Offset 6D508h

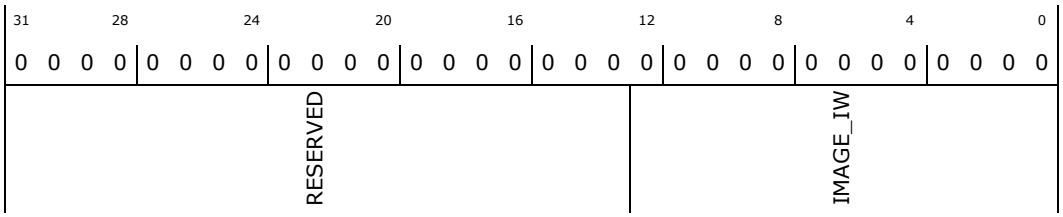
VSC Width Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D508h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RESERVED:** (read only).
12:0	0x0 RW	**IMAGE_IW:** Image input width

4.3.119 PCPSXVS_ISF—Offset 6D510h

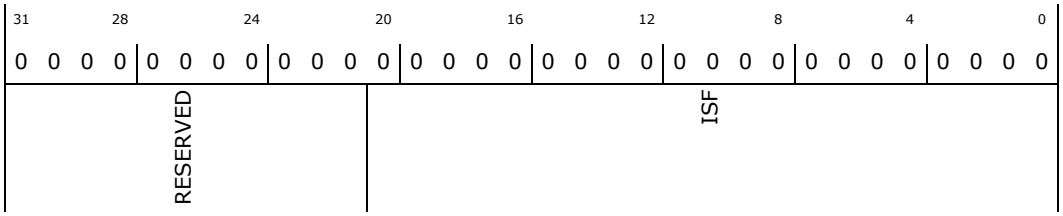
Inverse Scale Factor Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D510h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RO	**RESERVED:** (read only).
20:0	0x0 RW	**ISF:** Inverse Scale Factor. The format is 5.16 For Example, If the scaling Ratio is 4/7, the inverse scale factor is 7/4.

4.3.120 PCPSXVS_PC—Offset 6D514h

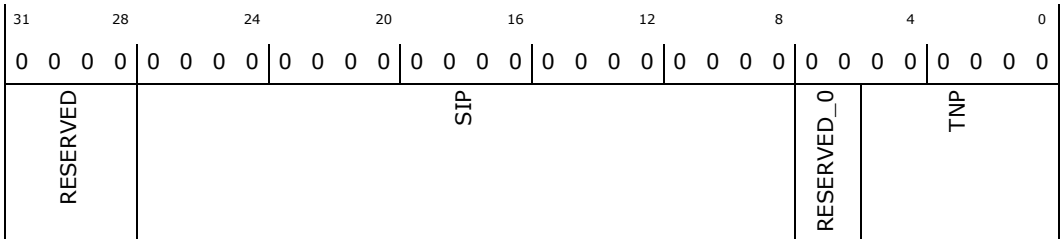
Phase Configuration Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D514h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** (read only).
27:8	0x0 RW	**SIP:** Scaled Initial Phase for the first pixel of every frame. This needs to be programmed to initial phase. The format of the SIP field is 4.16. For up scaling case, SIP should be smaller than 0x10000, for downscaling case to reduce validation overhead SIP is limited smaller than 0x40000.
7:6	0x0 RO	**RESERVED_0:** (read only).
5:0	0x0 RW	**TNP:** Total number of phases used in the filter bank. The vertical scaler provides a max of 32 phases.

4.3.121 PCPSX HSC PolyPhase YCbCr Co efficient Memory (PCPSXVS_PM)—Offset 6D600h

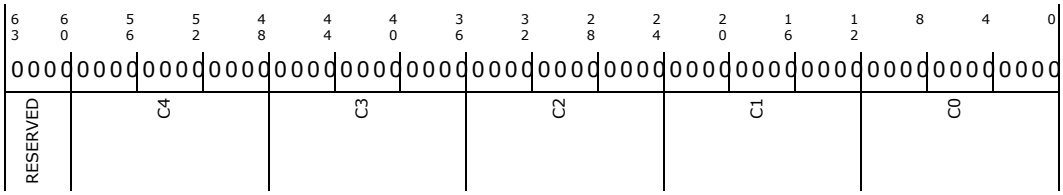
Config Register

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: 6D600h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:60	0x0 RO	**C5 (RESERVED):** RESERVED
59:48	0x0 RO	**C4:** Co efficient 4

Bit Range	Default & Access	Field Name (ID): Description
47:36	0x0 RO	**C3:** Co efficient 3
35:24	0x0 RO	**C2:** Co efficient 2-First Half
23:12	0x0 RO	**C1:** Co efficient 1
11:0	0x0 RO	**C0:** Co efficient 0

4.3.122 PCPSX HSC PolyPhase YCbCr Co efficient Memory (PCPSXVS_APM)—Offset 6D700h

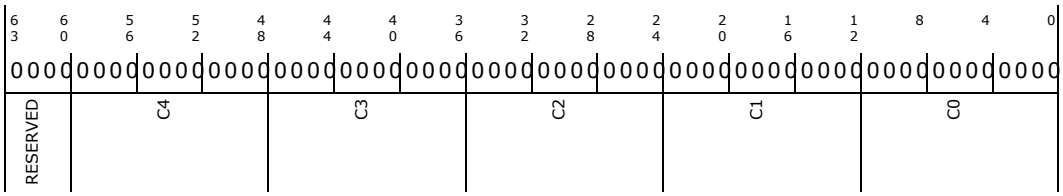
Config Register

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: 6D700h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:60	0x0 RO	**C5 (RESERVED):** RESERVED
59:48	0x0 RO	**C4:** Co efficient 4
47:36	0x0 RO	**C3:** Co efficient 3
35:24	0x0 RO	**C2:** Co efficient 2-First Half
23:12	0x0 RO	**C1:** Co efficient 1
11:0	0x0 RO	**C0:** Co efficient 0

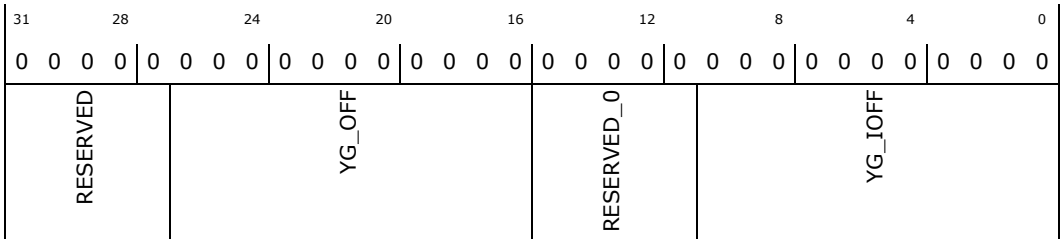
4.3.123 SPCSCYGOFF_C—Offset 6D900h

Sprite C CSC Y/G Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6D900h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** (read only).
26:16	0x0 RW	**YG_OFF:** 2's Complement output offset for Y/G
15:11	0x0 RW	**RESERVED_0:** Reserved.
10:0	0x0 RW	**YG_IOFF:** 2's Complement signed input offset for Y/G

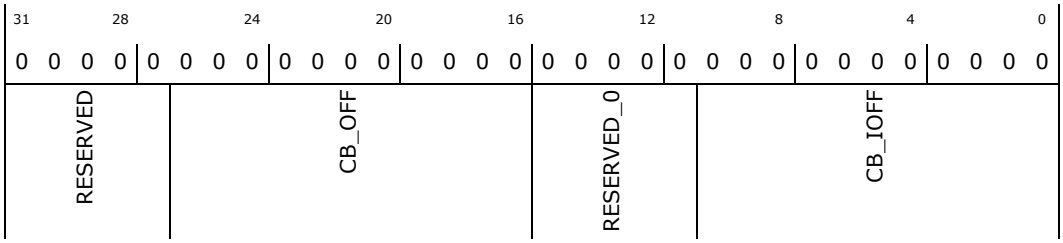
4.3.124 SPCSCCBOFF_C—Offset 6D904h

Sprite C CSC cb/B Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6D904h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** (read only).
26:16	0x0 RW	**CB_OFF:** 2's Complement signed output offset for Cb/B
15:11	0x0 RW	**RESERVED_0:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
10:0	0x0 RW	**CB_IOFF:** 2's Complement signed input offset for Cb/B

4.3.125 SPCSCCROFF_C—Offset 6D908h

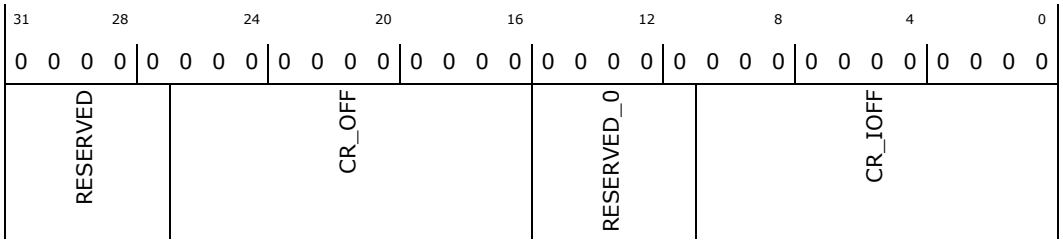
Sprite C CSC Cr/R Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D908h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** (read only).
26:16	0x0 RW	**CR_OFF:** 2's Complement output offset for Cr/R
15:11	0x0 RO	**RESERVED_0:** Reserved.
10:0	0x0 RW	**CR_IOFF:** 2's Complement signed input offset for Cr/R

4.3.126 SPCSCC01_C—Offset 6D90Ch

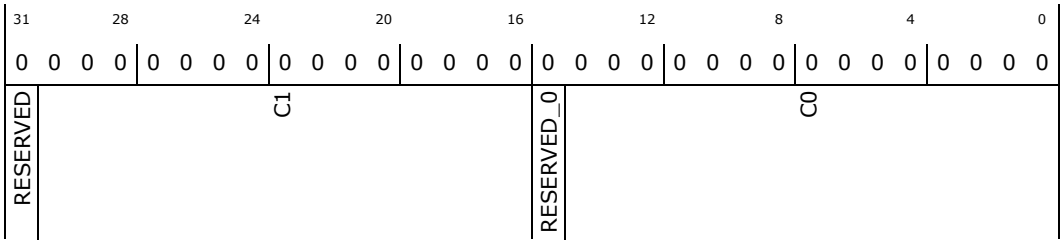
Sprite C CSC Coefficient01 Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D90Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** (read only).
30:16	0x0 RW	**C1:** 2's Complement output offset for C1
15	0x0 RO	**RESERVED_0:** Reserved.
14:0	0x0 RW	**C0:** 2's Complement signed input offset for C0

4.3.127 SPCSCC23_C—Offset 6D910h

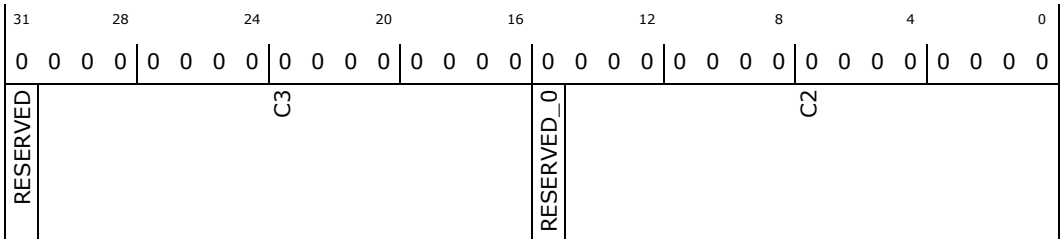
Sprite C CSC Coefficient23 Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D910h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** (read only).
30:16	0x0 RW	**C3:** 2's Complement output offset for C3
15	0x0 RO	**RESERVED_0:** Reserved.
14:0	0x0 RW	**C2:** 2's Complement signed input offset for C2

4.3.128 SPCSCC45_C—Offset 6D914h

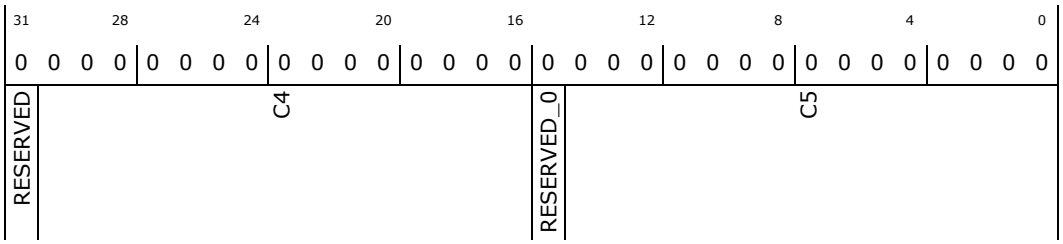
Sprite C CSC Coefficient45 Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D914h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** (read only).
30:16	0x0 RW	**C4:** 2's Complement output offset for C4
15	0x0 RO	**RESERVED_0:** Reserved.
14:0	0x0 RW	**C5:** 2's Complement signed input offset for C5

4.3.129 SPCSCC67_C—Offset 6D918h

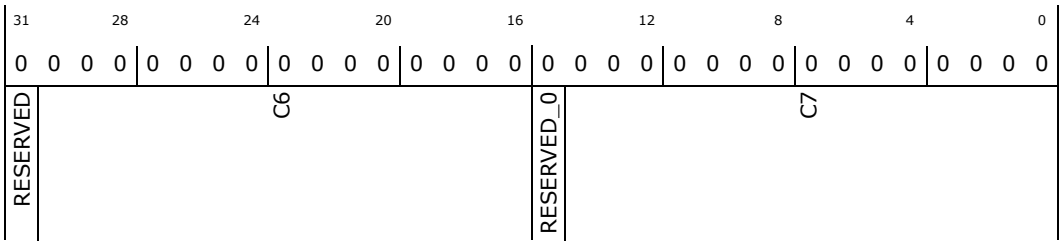
Sprite C CSC Coefficient67 Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D918h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** (read only).

Bit Range	Default & Access	Field Name (ID): Description
30:16	0x0 RW	**C6:** 2's Complement output offset for C6
15	0x0 RO	**RESERVED_0:** Reserved.
14:0	0x0 RW	**C7:** 2's Complement signed input offset for C7

4.3.130 SPCSCC8_C—Offset 6D91Ch

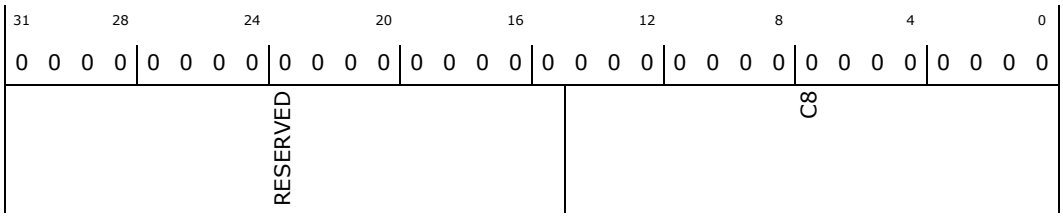
Sprite C CSC Coefficient8 Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D91Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RO	**RESERVED:** (read only).
14:0	0x0 RW	**C8:** 2's Complement output offset for C1

4.3.131 SPCSCYGICLAMP_C—Offset 6D920h

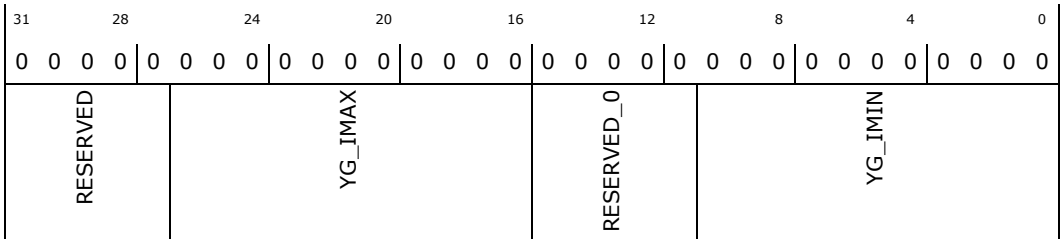
Sprite C CSC Y/G input clamping Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D920h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** (read only).
26:16	0x0 RW	**YG_IMAX:** 2's Complement signed output offset for Y/G Input Max Value
15:11	0x0 RW	**RESERVED_0:** Reserved.
10:0	0x0 RW	**YG_IMIN:** 2's Complement signed input offset for YG_IMIN

4.3.132 SPCSCCBICLAMP_C—Offset 6D924h

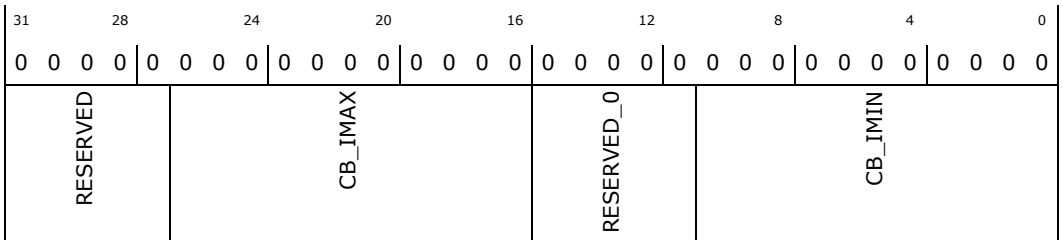
Sprite C CSC Cb/B Input Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D924h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** (read only).
26:16	0x0 RW	**CB_IMAX:** 2's Complement signed output offset for CbIMAN
15:11	0x0 RO	**RESERVED_0:** Reserved.
10:0	0x0 RW	**CB_IMIN:** 2's Complement signed input offset for Cb/B

4.3.133 SPCSCCRICLAMP_C—Offset 6D928h

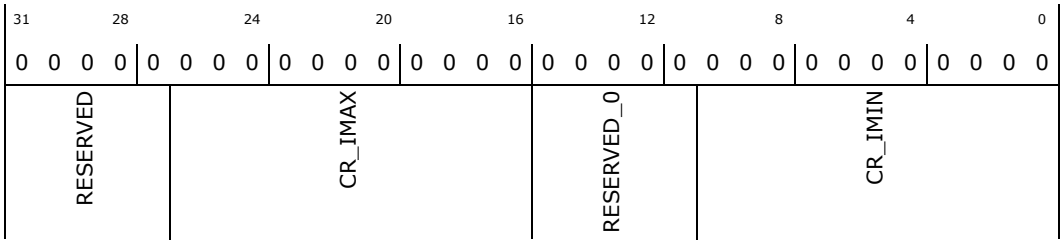
Sprite C CSC Cr/R Input Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D928h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** (read only).
26:16	0x0 RW	**CR_IMAX:** 2's Complement signed output offset for CrIMAN
15:11	0x0 RO	**RESERVED_0:** Reserved.
10:0	0x0 RW	**CR_IMIN:** 2's Complement signed input offset for Cr/R

4.3.134 SPCSCYGOCLAMP_C—Offset 6D92Ch

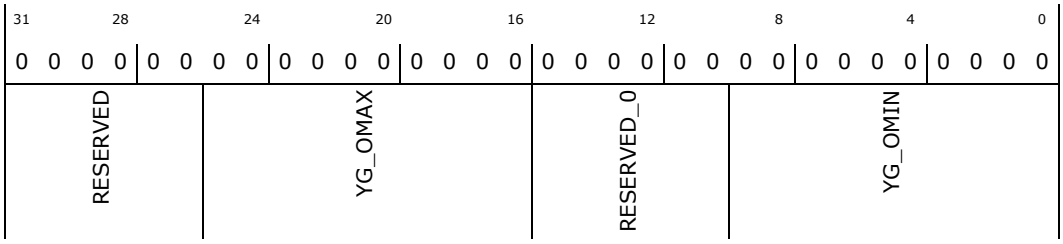
Sprite C CSC Y/G output Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D92Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RESERVED:** (read only).
25:16	0x0 RW	**YG_OMAX:** unsigned output offset for YGOMAX
15:10	0x0 RO	**RESERVED_0:** Reserved.
9:0	0x0 RW	**YG_OMIN:** unsigned output offset for YG

4.3.135 SPCSCCBOCLAMP_C—Offset 6D930h

Sprite C CSC Cb/B output Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D930h

Default: 00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RESERVED:** (read only).
25:16	0x0 RW	**CB_OMAX:** unsigned output offset for CbOMAN
15:10	0x0 RO	**RESERVED_0:** Reserved.
9:0	0x0 RW	**CB_OMIN:** unsigned input offset for CbOMIN

4.3.136 SPCSCCROCLAMP_C—Offset 6D934h

Sprite C CSC Cr/R output Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6D934h

Default: 00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RESERVED:** (read only).

Bit Range	Default & Access	Field Name (ID): Description
25:16	0x0 RW	**CR_OMAX:** unsigned output offset for CrOMAN
15:10	0x0 RO	**RESERVED_0:** Reserved.
9:0	0x0 RW	**CR_OMIN:** unsigned input offset for CrOMIN

4.3.137 PCPSXCONFIG (PCPSXCONFIG_SPR)—Offset 6E000h

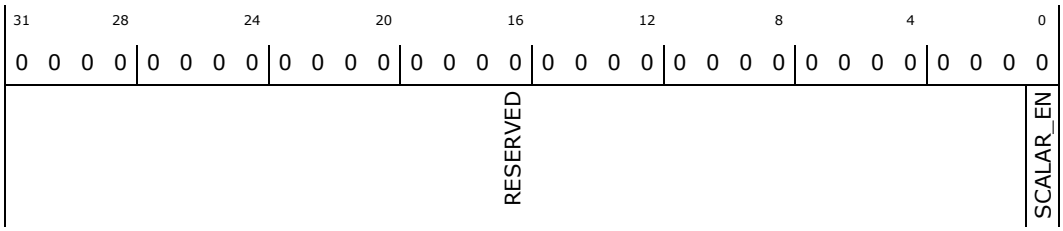
Config Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6E000h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RESERVED:** (read only).
0	0x0 RW	**SCALAR_EN:** 0=Perform Scaling per programmed parameters. 1=bypass horizontal and vertical scalers. Other programmed parameters have no effect in this case

4.3.138 PCPSXHS_H (PCPSXHS_SPR_H)—Offset 6E104h

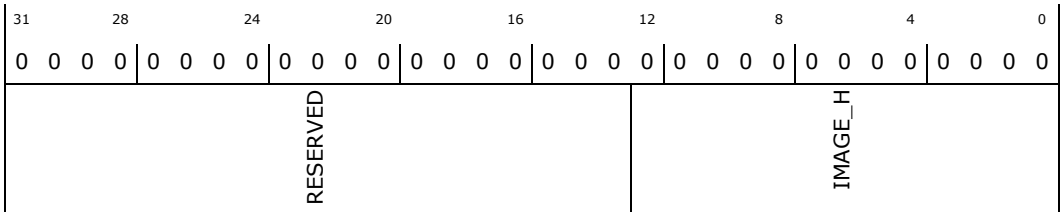
HSC Height Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6E104h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RESERVED:** (read only).
12:0	0x0 RW	**IMAGE_H:** Image Height in terms of pixels. This must match the source height specified for the plane

4.3.139 PCPSXHS_W (PCPSXHS_SPR_W)—Offset 6E108h

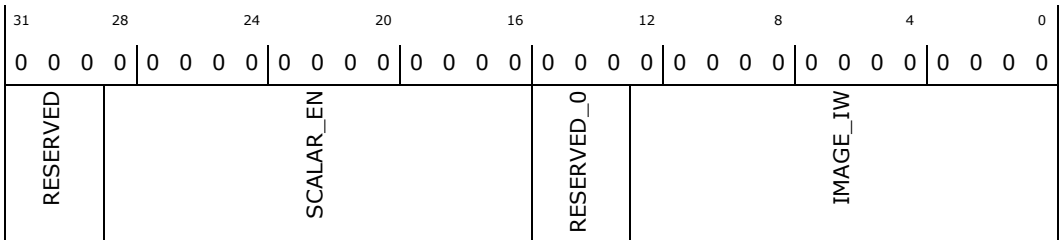
HSC Width Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6E108h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RESERVED:** (read only).
28:16	0x0 RW	**IMAGE_OW (SCALAR_EN):** Image Output Width in terms of pixels.
15:13	0x0 RO	**RESERVED_0:** (read only).
12:0	0x0 RW	**IMAGE_IW:** Image input width

4.3.140 PCPSXHS_NBP (PCPSXHS_SPR_NBP)—Offset 6E10Ch

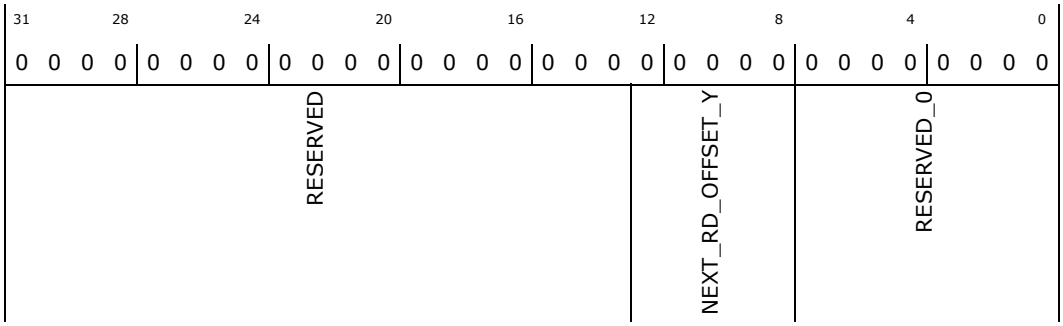
Next Block Params Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6E10Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RESERVED:** (read only).
12:8	0x0 RW	**Next_RD_OFFSET_Y (NEXT_RD_OFFSET_Y):** 1: Offset(mag) should be subtracted. 0:offset(mag) should be added
7:0	0x0 RO	**RESERVED_0:** (read only).

4.3.141 PCPSXHS_ISF (PCPSXHS_SPR_ISF)—Offset 6E110h

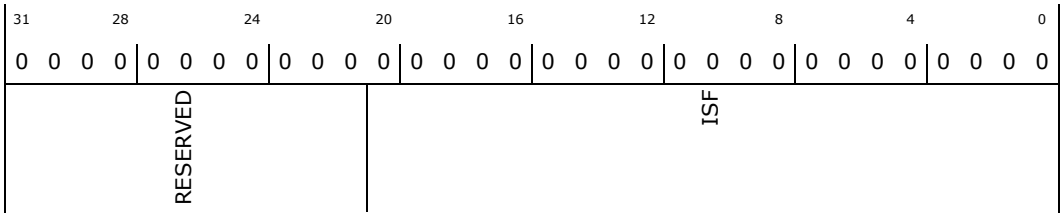
Inverse Scale Factor Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6E110h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RO	**RESERVED:** (read only).
20:0	0x0 RW	**ISF:** Inverse Scale Factor. The format is 5.16 For Example, If the scaling Ratio is 4/7, the inverse scale factor is 7/4.

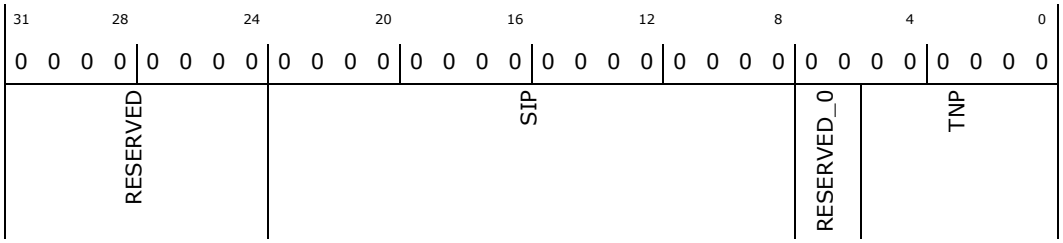
4.3.142 PCPSXHS_PC (PCPSXHS_SPR_PC)—Offset 6E114h

Phase Configuration Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6E114h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** (read only).
23:8	0x0 RW	**SIP:** Scaled Initial Phase for the first pixel of every frame. This needs to be programmed to initial phase. The format of the SIP field is 0.16. Usage NOTE: While this field is technically programmable, the horizontal SIP does not change during regular usage. To Reduce validation overhead the only value of SIP tested is 0x7c00. This is the only value that should be programmed by SW.
7:6	0x0 RO	**RESERVED_0:** (read only).
5:0	0x0 RW	**TNP:** Total number of phases used in the filter bank. The horizontal scaler provides a max of 32 phases.

4.3.143 PCPSX HSC PolyPhase YCbCr Co efficient Memory (PCPSXHS_SPR_PM)—Offset 6E200h

Config Register

Access Method

Type: Memory Mapped I/O Register (Size: 128 bits) **Offset:** 6E200h

Default: 00000000000000000000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
127:108	0x0 RO	**RESERVED:** Reserved.
107:96	0x0 RO	**C8:** Co efficient 8
95:84	0x0 RO	**C7:** Co efficient 7
83:72	0x0 RO	**C6:** Co efficient 6
71:60	0x0 RO	**C5:** Co efficient 5-First 4 bits

Bit Range	Default & Access	Field Name (ID): Description
59:48	0x0 RO	**C4:** Co efficient 4
47:36	0x0 RO	**C3:** Co efficient 3
35:24	0x0 RO	**C2:** Co efficient 2-First Half
23:12	0x0 RO	**C1:** Co efficient 1
11:0	0x0 RO	**C0:** Co efficient 0

4.3.144 PCPSX HSC PolyPhase YCbCr Co efficient Memory (PCPSXHS_SPR_APM)—Offset 6E300h

Config Register

Access Method

Type: Memory Mapped I/O Register (Size: 128 bits)

Offset: 6E300h

Default: 00000000000000000000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
127:108	0x0 RO	**RESERVED:** Reserved.
107:96	0x0 RO	**C8:** Co efficient 8
95:84	0x0 RO	**C7:** Co efficient 7
83:72	0x0 RO	**C6:** Co efficient 6
71:60	0x0 RO	**C5:** Co efficient 5-First 4 bits
59:48	0x0 RO	**C4:** Co efficient 4
47:36	0x0 RO	**C3:** Co efficient 3
35:24	0x0 RO	**C2:** Co efficient 2-First Half
23:12	0x0 RO	**C1:** Co efficient 1
11:0	0x0 RO	**C0:** Co efficient 0

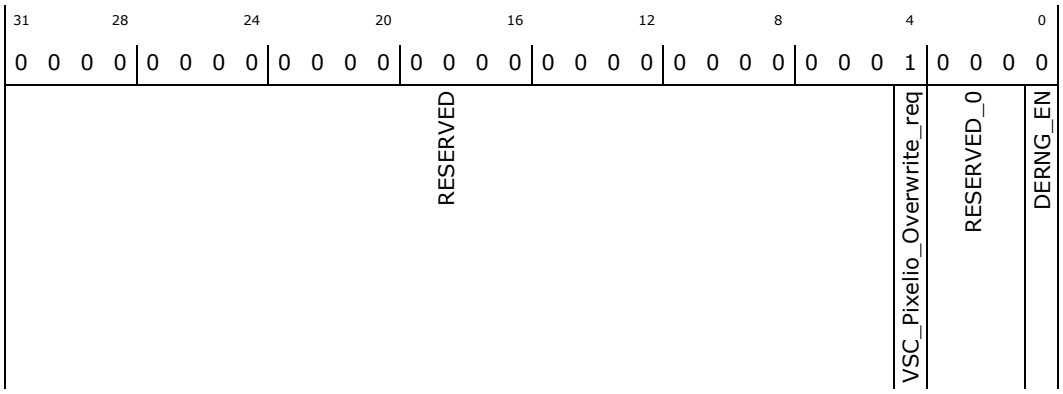
4.3.145 PCPSXVS_SPR_CTRL—Offset 6E500h

VSC Control Register FOR SPRITE

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6E500h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RO	**RESERVED:** (read only).
4	0x1 RW	**VSC_Pixelio_Overwrite_req:** Chicken bit: When this bit is set to 1, logic for controlling row incremental information update timing inside pixelio will overwrite pixel request signal.
3:1	0x0 RO	**RESERVED_0:** (read only).
0	0x0 RW	**DERNG_EN:** 1: Enable check and removal ringing pixels. 0:disable checking and removing pixels.

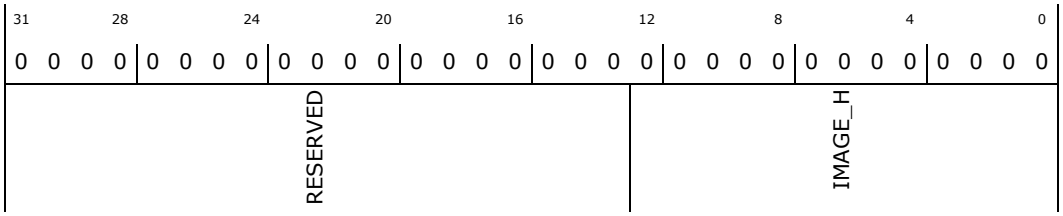
4.3.146 PCPSXVS_H (PCPSXVS_SPR_H)—Offset 6E504h

VSC Height Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6E504h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RESERVED:** (read only).
12:0	0x0 RW	**IMAGE_H:** Image Height in terms of pixels. This must match the source height specified for the plane

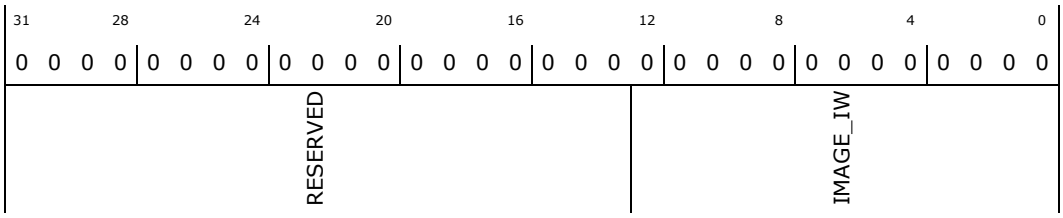
4.3.147 PCPSXVS_W (PCPSXVS_SPR_W)—Offset 6E508h

VSC Width Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6E508h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RESERVED:** (read only).
12:0	0x0 RW	**IMAGE_IW:** Image input width

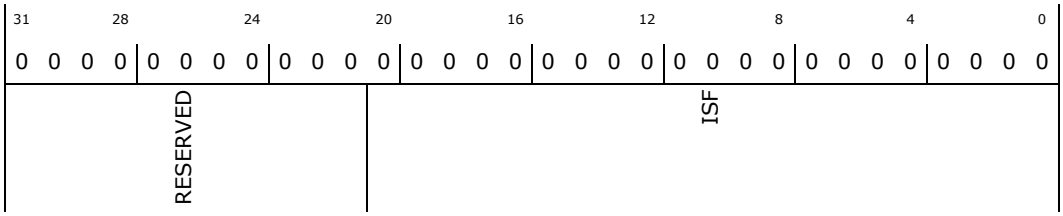
4.3.148 PCPSXVS_ISF (PCPSXVS_SPR_ISF)—Offset 6E510h

Inverse Scale Factor Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6E510h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RO	**RESERVED:** (read only).
20:0	0x0 RW	**ISF:** Inverse Scale Factor. The format is 5.16 For Example, If the scaling Ratio is 4/7, the inverse scale factor is 7/4.

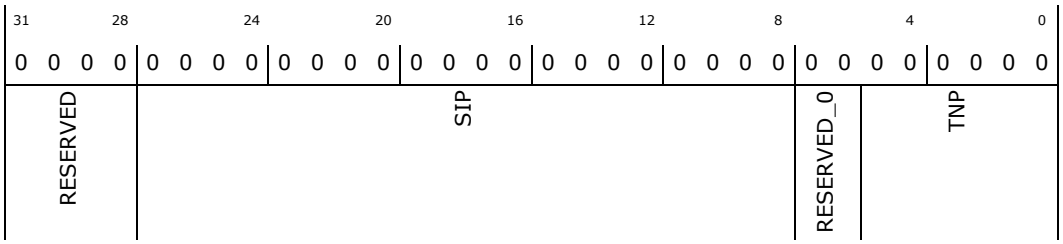
4.3.149 PCPSXVS_PC (PCPSXVS_SPR_PC)—Offset 6E514h

Phase Configuration Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6E514h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** (read only).
27:8	0x0 RW	**SIP:** Scaled Initial Phase for the first pixel of every frame. This needs to be programmed to initial phase. The format of the SIP field is 4.16. For up scaling case, SIP should be smaller than 0x10000, for downscaling case to reduce validation overhead SIP is limited smaller than 0x40000.
7:6	0x0 RO	**RESERVED_0:** (read only).
5:0	0x0 RW	**TNP:** Total number of phases used in the filter bank. The vertical scaler provides a max of 32 phases.

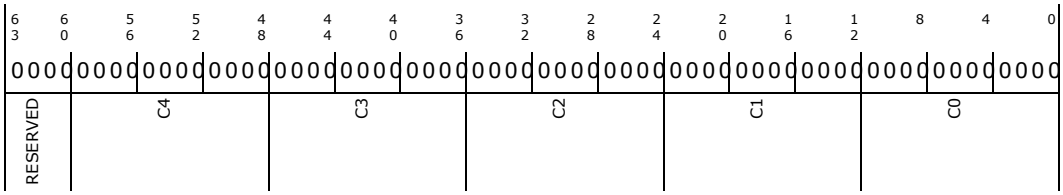
4.3.150 PCPSX HSC PolyPhase YCbCr Co efficient Memory (PCPSXVS_SPR_PM)—Offset 6E600h

Config Register

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits) **Offset:** 6E600h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:60	0x0 RO	**C5 (RESERVED):** RESERVED
59:48	0x0 RO	**C4:** Co efficient 4
47:36	0x0 RO	**C3:** Co efficient 3
35:24	0x0 RO	**C2:** Co efficient 2-First Half
23:12	0x0 RO	**C1:** Co efficient 1
11:0	0x0 RO	**C0:** Co efficient 0

4.3.151 PCPSX HSC PolyPhase YCbCr Co efficient Memory (PCPSXVS_SPR_APM)—Offset 6E700h

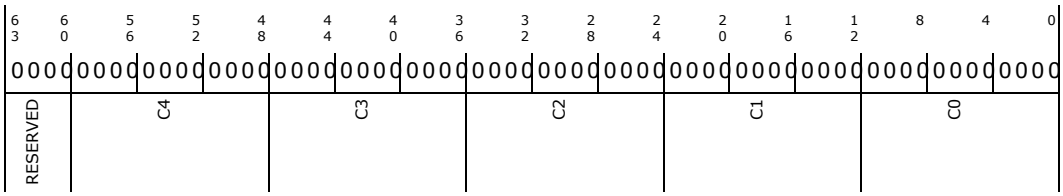
Config Register

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: 6E700h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:60	0x0 RO	**C5 (RESERVED):** RESERVED
59:48	0x0 RO	**C4:** Co efficient 4
47:36	0x0 RO	**C3:** Co efficient 3
35:24	0x0 RO	**C2:** Co efficient 2-First Half

Bit Range	Default & Access	Field Name (ID): Description
23:12	0x0 RO	**C1:** Co efficient 1
11:0	0x0 RO	**C0:** Co efficient 0

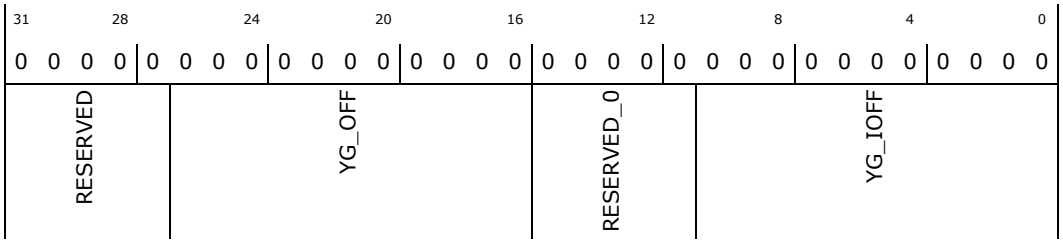
4.3.152 SPCSCYGOFF_D—Offset 6E900h

Sprite D CSC Y/G Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6E900h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** (read only).
26:16	0x0 RW	**YG_OFF:** 2's Complement output offset for Y/G
15:11	0x0 RO	**RESERVED_0:** Reserved.
10:0	0x0 RW	**YG_IOFF:** 2's Complement signed input offset for Y/G

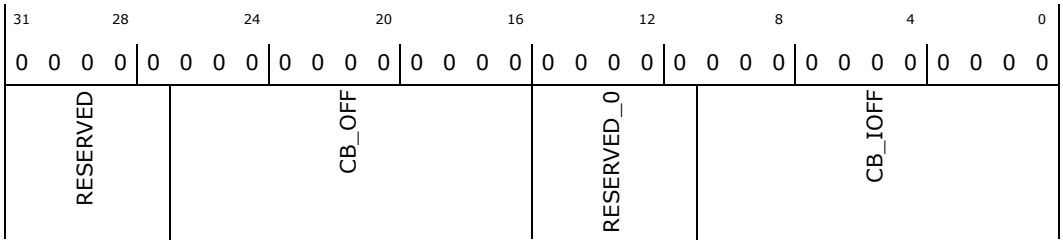
4.3.153 SPCSCCBOFF_D—Offset 6E904h

Sprite D CSC cb/B Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6E904h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** (read only).
26:16	0x0 RW	**CB_OFF:** 2's Complement signed output offset for Cb/B
15:11	0x0 RO	**RESERVED_0:** Reserved.
10:0	0x0 RW	**CB_IOFF:** 2's Complement signed input offset for Cb/B

4.3.154 SPCSCCROFF_D—Offset 6E908h

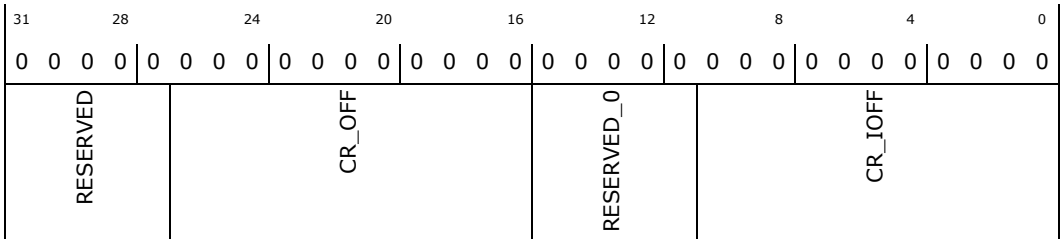
Sprite D CSC Cr/R Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6E908h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** (read only).
26:16	0x0 RW	**CR_OFF:** 2's Complement output offset for Cr/R
15:11	0x0 RO	**RESERVED_0:** Reserved.
10:0	0x0 RW	**CR_IOFF:** 2's Complement signed input offset for Cr/R

4.3.155 SPCSCC01_D—Offset 6E90Ch

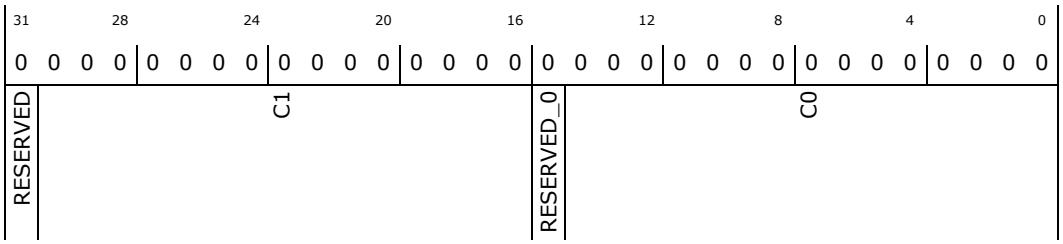
Sprite D CSC Coefficient01 Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6E90Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** (read only).
30:16	0x0 RW	**C1:** 2's Complement output offset for C1
15	0x0 RO	**RESERVED_0:** Reserved.
14:0	0x0 RW	**C0:** 2's Complement signed input offset for C0

4.3.156 SPCSCC23_D—Offset 6E910h

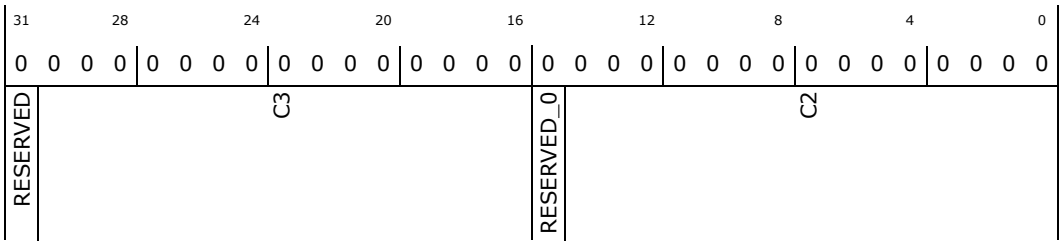
Sprite D CSC Coefficient23 Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6E910h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** (read only).

Bit Range	Default & Access	Field Name (ID): Description
30:16	0x0 RW	**C3:** 2's Complement output offset for C3
15	0x0 RO	**RESERVED_0:** Reserved.
14:0	0x0 RW	**C2:** 2's Complement signed input offset for C2

4.3.157 SPCSCC45_D—Offset 6E914h

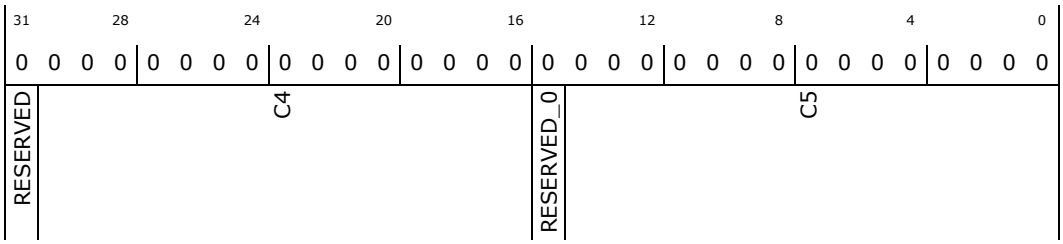
Sprite D CSC Coefficient45 Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6E914h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** (read only).
30:16	0x0 RW	**C4:** 2's Complement output offset for C4
15	0x0 RO	**RESERVED_0:** Reserved.
14:0	0x0 RW	**C5:** 2's Complement signed input offset for C5

4.3.158 SPCSCC67_D—Offset 6E918h

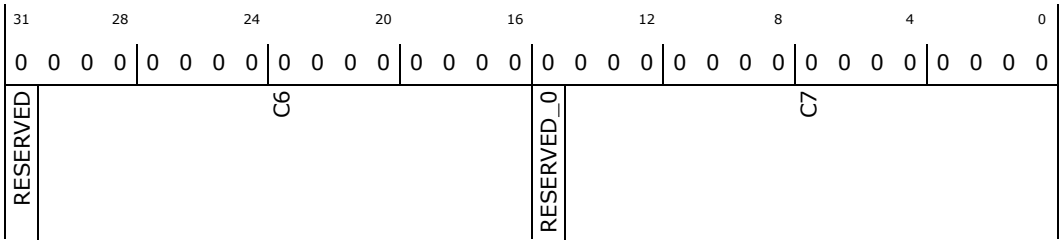
Sprite D CSC Coefficient67 Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6E918h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** (read only).
30:16	0x0 RW	**C6:** 2's Complement output offset for C6
15	0x0 RO	**RESERVED_0:** Reserved.
14:0	0x0 RW	**C7:** 2's Complement signed input offset for C7

4.3.159 SPCSCC8_D—Offset 6E91Ch

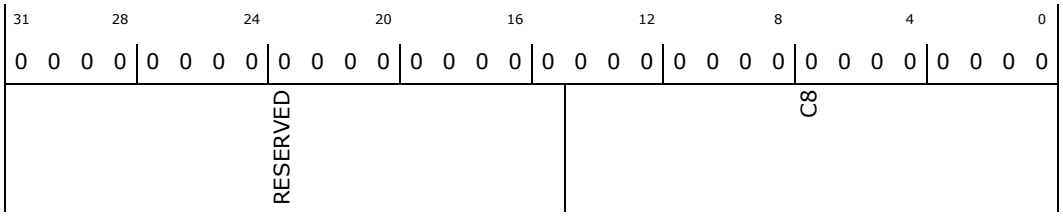
Sprite D CSC Coefficient8 Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6E91Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RO	**RESERVED:** (read only).
14:0	0x0 RW	**C8:** 2's Complement output offset for C1

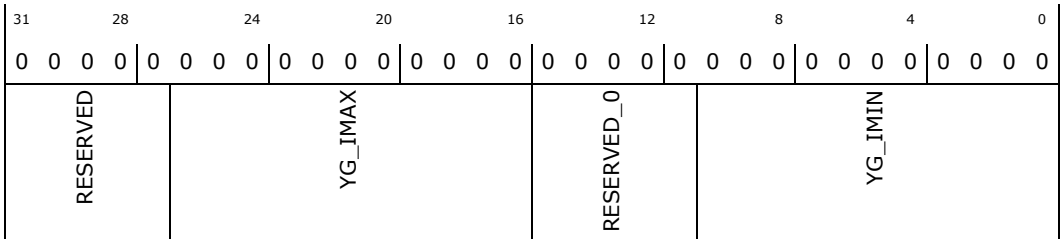
4.3.160 SPCSCYGICLAMP_D—Offset 6E920h

Sprite D CSC Y/G input clamping Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6E920h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** (read only).
26:16	0x0 RW	**YG_IMAX:** 2's Complement signed output offset for Y/G Input Max Value
15:11	0x0 RO	**RESERVED_0:** Reserved.
10:0	0x0 RW	**YG_IMIN:** 2's Complement signed input offset for YG_IMIN

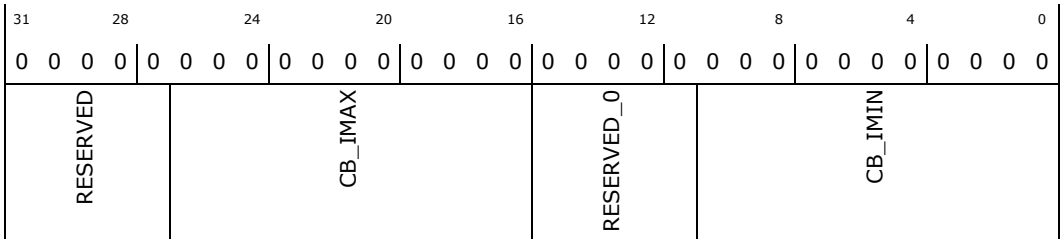
4.3.161 SPCSCCBICLAMP_D—Offset 6E924h

Sprite D CSC Cb/B Input Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 6E924h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** (read only).
26:16	0x0 RW	**CB_IMAX:** 2's Complement signed output offset for CbIMAN
15:11	0x0 RO	**RESERVED_0:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
10:0	0x0 RW	**CB_IMIN:** 2's Complement signed input offset for Cb/B

4.3.162 SPCSCCRICLAMP_D—Offset 6E928h

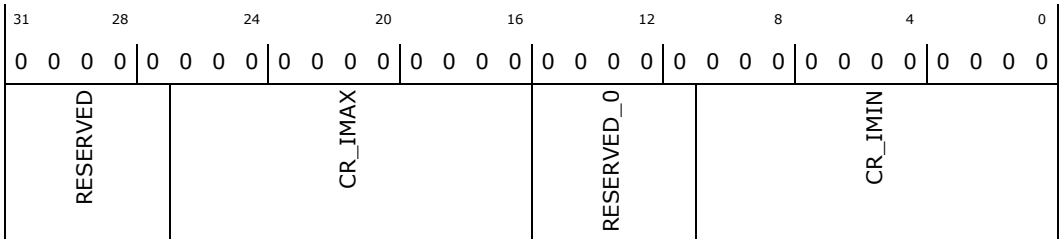
Sprite D CSC Cr/R Input Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6E928h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** (read only).
26:16	0x0 RW	**CR_IMAX:** 2's Complement signed output offset for CrIMAN
15:11	0x0 RO	**RESERVED_0:** Reserved.
10:0	0x0 RW	**CR_IMIN:** 2's Complement signed input offset for Cr/R

4.3.163 SPCSCYGOCLAMP_D—Offset 6E92Ch

Sprite D CSC Y/G output Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6E92Ch

Default: 00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RESERVED:** (read only).
25:16	0x0 RW	**YG_OMAX:** unsigned output offset for YGOMAX
15:10	0x0 RO	**RESERVED_0:** Reserved.
9:0	0x0 RW	**YG_OMIN:** unsigned output offset for YG

4.3.164 SPCSCCBOCLAMP_D—Offset 6E930h

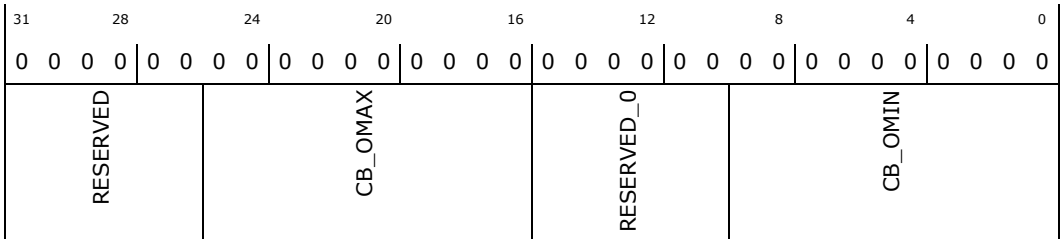
Sprite D CSC Cb/B output Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6E930h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RESERVED:** (read only).
25:16	0x0 RW	**CB_OMAX:** unsigned output offset for CbOMAN
15:10	0x0 RO	**RESERVED_0:** Reserved.
9:0	0x0 RW	**CB_OMIN:** unsigned input offset for CbOMIN

4.3.165 SPCSCCROCLAMP_D—Offset 6E934h

Sprite D CSC Cr/R output Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 6E934h

Default: 00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RESERVED:** (read only).
25:16	0x0 RW	**CR_OMAX:** unsigned output offset for CrOMAN
15:10	0x0 RO	**RESERVED_0:** Reserved.
9:0	0x0 RW	**CR_OMIN:** unsigned input offset for CrOMIN

4.3.166 PIPEA_DSL—Offset 70000h

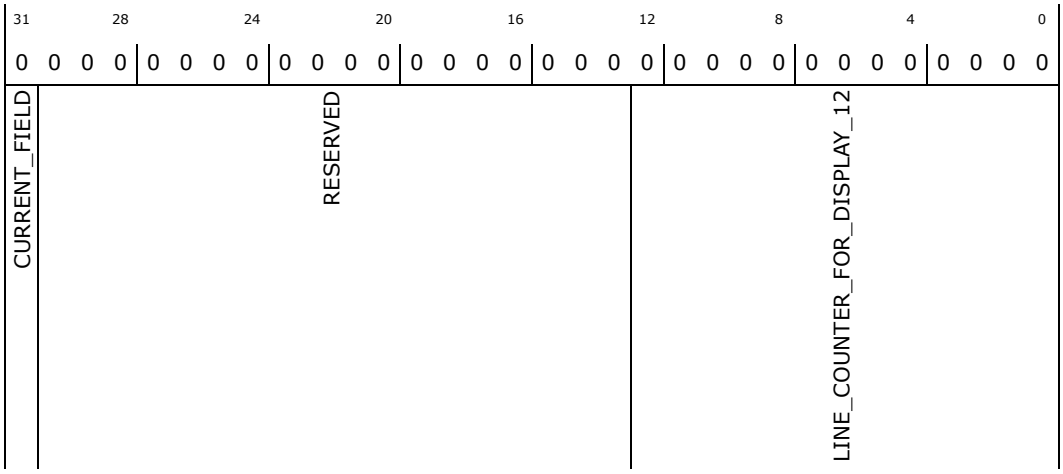
Pipe A Display Scan Line

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70000h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**CURRENT_FIELD:** Provides read back of the current field being displayed on display pipe A. Non-TV mode: 0 = first field (odd field) 1 = second field (even field) TV mode: 1 = first field (odd field) 0 = second field (even field) [DevBW] and [DevCL] Reserved: Read only.
30:13	0x0 RO	**RESERVED:** Read only.
12:0	0x0 RO	**LINE_COUNTER_FOR_DISPLAY_12:** 0]: Provides read back of the display pipe A vertical line counter. This is an indication of the current display scan line to be used by software to synchronize with the display.

4.3.167 PIPEA_SLC—Offset 70004h

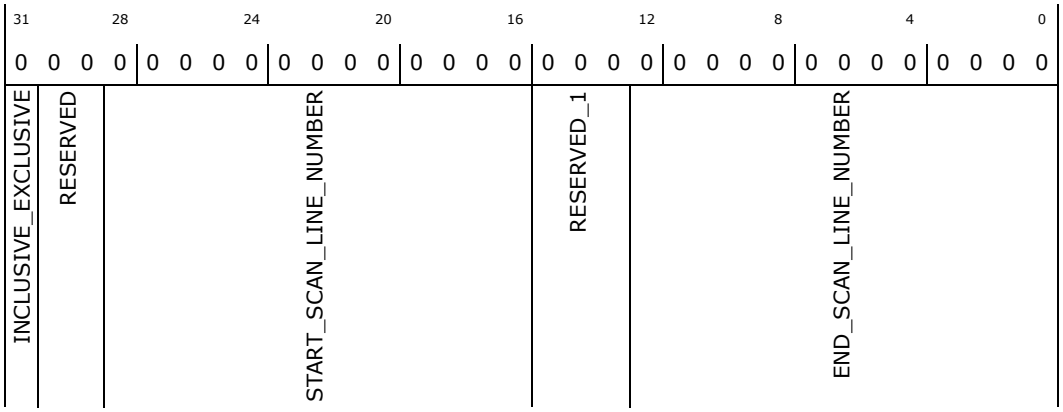
Pipe A Display Scan Line Count Range Compare

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70004h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**INCLUSIVE_EXCLUSIVE:** 1 = Inclusive: within the range. 0 = Exclusive: outside of the range.
30:29	0x0 RO	**RESERVED:** Read only.
28:16	0x0 RW	**START_SCAN_LINE_NUMBER:** This field specifies the starting scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0,Display Buffer height in lines-1]. [DevBW, DevCL] End Scan Line Number: This field specifies the ending scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0, Display Buffer height in lines-1].
15:13	0x0 RO	**RESERVED_1:** Read only.
12:0	0x0 RW	**END_SCAN_LINE_NUMBER:** This field specifies the ending scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0, Display Buffer height in lines-1]. [DevBW] and [DevCL] Start Scan Line Number: This field specifies the starting scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0,Display Buffer height in lines-1].

4.3.168 PIPEACONF—Offset 70008h

Pipe A Configuration Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70008h

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PIPE_A_ENABLE	PIPE_STATE	DSI_PLL_LOCK_LOCK	FRAME_START_DELAY				DISPLAY_PORT_AUDIO_ONLY_MODE			FORCE_BORDER	PIPE_A_GAMMA_UNIT_MODE			INTERLACED_MODE			MIPI_DISPLAY_SELF_REFRESH_MODE_FOR_MIPI_A_REFRESH	DISPLAY_OVERLAY_PLANES_OFF		CURSOR_PLANES_OFF	REFRESH_RATE_CXSR_MODE_ASSOCIATION		COLOR_CORRECTION_MATRIX_ENABLE_ON_PIPE_A_1_COLOR_CORRECTION_COEFFICIENTS_ARE_ENABLED_TO_PERFORM_COLOR_CORRECTION_0_COLOR_CORRECTION_COEFFICIENTS_ARE_DISABLED_		DISPLAYPORT_POWER_MODE_SWITCH_DEVVLVP	COLOR_RANGE_SELECT	S3D_SPRITE_ORDER	S3D_SPRITE_INTERLEAVING_FORMAT		RESERVED		BITS_PER_COLOR			DITHERING_ENABLE	DITHERING_TYPE		DDA_RESET_TEST_MODE	RESERVED_1

Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**PIPE_A_ENABLE:** Setting this bit to the value of one, turns on pipe A. This must be done before any planes are enabled on this pipe. Changing it to a zero should only be done when all planes that are assigned to this pipe have been disabled. Turning the pipe enable bit off disables the timing generator in this pipe. Plane disable occurs after the next VBLANK event after the plane is disabled. Synchronization pulses to the display are not maintained if the timing generator is disabled. Power consumption will be at it s lowest state when disabled. A separate bit controls the DPLL enable for this pipe. Pipe timing registers should contain valid values before this bit is enabled. 0 = Disable 1 = Enable
30	0x0 RO	**PIPE_STATE:** This bit indicates the actual state of the pipe. Since there can be some delay between disabling the pipe and the pipe actually shutting off, this bit indicates the true current state of the pipe. 0 = Disabled 1 = Enabled AccessType: Read Only
29	0x0 RO	**DSI_PLL_LOCK_LOCK:** This bit indicates the clocks from DSI PLL are locked. 0 = Unlocked 1 = Locked AccessType: Read only
28:27	0x0 RW	**FRAME_START_DELAY:** (TEST MODE) Used to delay the frame start signal that is sent to the display planes. Normal operation uses the default 00 value and test modes can use the delayed frame start to shorten the test time. Care must be taken to insure that there are enough lines during VBLANK to support this setting. 00 = Frame Start occurs on the first HBLANK after the start of VBLANK 01 = Frame Start occurs on the second HBLANK after the start of VBLANK 10 = Frame Start occurs on the third HBLANK after the start of VBLANK 11 = Frame Start occurs on the forth HBLANK after the start of VBLANK
26	0x0 RW	**DISPLAY_PORT_AUDIO_ONLY_MODE:** Setting this bit to 1 indicates the DisplayPort will output audio only. 0 = DisplayPort will output Video or Video and Audio 1 = DisplayPort will output Audio only
25	0x0 RW	**FORCE_BORDER:** (TEST MODE)0 = Normal Operation 1 = Color information is ignored and border color is substituted during active region
24	0x0 RW	**PIPE_A_GAMMA_UNIT_MODE:** This bit selects which mode the pipe gamma correction logic works in. In the palette mode, it behaves as a 3X256x8 RAM lookup. Indexed mode operation should use the palette in 8-bit mode. In the 10-bit gamma mode, it will act as a piecewise linear interpolation. Other gamma units such as in the overlay or sprite are unaffected by this bit. 0 = 8-bit Palette Mode 1 = 10-bit Gamma Mode

Bit Range	Default & Access	Field Name (ID): Description
23:21	0x0 RW	**INTERLACED_MODE:** These bits are used for software control of interlaced behavior. They are updated immediately if the pipe is off, or in the vertical blank after programming if pipe is enabled. 0xx = Progressive 100 = Interlaced embedded panel using programmable vertical sync shift. (2x) 101 = Interlaced using vertical sync shift. Backup option to 110 setting. (2x) 110 = Interlaced with VSYNC/HSYNC Field Indication using legacy vertical sync shift. Used for SDVO. 111 = Interlaced with Field 0 Only using legacy vertical sync shift. Not used Setting the Interlaced embedded panel mode causes hardware to automatically modify the output to match the specifications of panels that support interlaced mode.
20	0x0 RW	**MIPI_DISPLAY_SELF_REFRESH_MODE_FOR_MIPI_A_REFRESH:** 0 = Normal Operation, display controller generate timing and refresh display panel at refresh rate 1 = Display self-refresh mode. Display controller update frame buffer in display module on demand only
19	0x0 RW	**DISPLAY_OVERLAY_PLANES_OFF:** This bit when set will cause all enabled Display and overlay planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit, at the next VBLANK. Timing signals continue as they were but the screen becomes blank. Setting the bit back to a zero will then allow the display and overlay planes to resume on the following VBLANK. 0 = Normal Operation 1 = Planes assigned to this pipe are disabled.
18	0x0 RW	**CURSOR_PLANES_OFF:** This bit when set will cause all enabled cursor planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit, at the next VBLANK. Timing signals continue as they were but the cursor(s) no longer appear on the screen. Setting the bit back to a zero will then allow the cursor planes to resume on the following VBLANK. 0 = Normal Operation 1 = Planes assigned to this pipe are disabled.
17:16	0x0 RW	**REFRESH_RATE_CXSR_MODE_ASSOCIATION:** These bits select how refresh rates are tied to big FIFO mode on pipe A. When they are set to anything other than 00, bits 23:21 of this register must be programmed to 0xx. Switching between 01 and 10 settings directly is not allowed. Software must program this field to 00 before switching. Software is responsible for enabling this mode only for integrated display panels that support corresponding mode. 00 Default no dynamic refresh rate change enabled. Software control only. 01 Progressive-to-progressive refresh rate change enabled and tied to big FIFO mode. Pixel clock values set in FPA0/FPA1 settings in the DPLLA control register and FPA0/FPA1 divider registers. FPA0 is tied to non-big-FIFO mode 10 Progressive-to-interlaced refresh rate change enabled and tied to big FIFO mode. Pixel clock value does not change in this case. Scaling must be disabled in this mode. Uses programmable VS shift 11 Reserved

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**COLOR_CORRECTION_MATRIX_ENABLE_ON_PIPE_A_1_COLOR_CORRECTION_COEFFICIENTS_ARE_ENABLED_TO_PERFORM_COLOR_CORRECTION_0_COLOR_CORRECTION_COEFFICIENTS_ARE_DISABLED_:** Reserved.
14	0x0 RW	**DISPLAYPORT_POWER_MODE_SWITCH_DEVVLVP:** This bit selects the software controlled progressive to progressive power saving mode (software controlled DRRS). Hardware Controlled Refresh Rate Select must be disabled when enabling this. Link and data M/N 1 values are used for normal settings, M/N 2 values are used for low power settings. 0 Normal progressive refresh rate (default) 1 Low Power progressive refresh rate
13	0x0 RW	**COLOR_RANGE_SELECT:** : This bit is used to select the color range of RBG outputs. 0 = Apply full 0-255 color range to the output (Default) 1 = Apply 16-235 color range to the output
12	0x0 RW	**S3D_SPRITE_ORDER:** This bit controls the blending order of the sprite planes for S3D support: 0 = Sprite A first. The first line or pixel comes from Sprite A (default) 1 = Sprite B first. The first line or pixel comes from Sprite B
11:10	0x0 RW	**S3D_SPRITE_INTERLEAVING_FORMAT:** These bits control the Sprite A/B interleaving format in S3D mode 00 = No interleaving 01 = Line interleaving 10 = Pixel interleaving 11 = Reserved
9:8	0x0 RO	**RESERVED:** MBZ Scrambling enable [DevCTG]: This bit enables scrambling for DisplayPort. Software must set this bit appropriately when enabling a DisplayPort output. 00 = Scrambling disabled (Default) 01 = Scrambling enabled, no SR after initialization at loop 2 of training 10 - RESERVED 11 = Scrambling and SR enabled. Scrambling is reset every 512 BS symbols.
7:5	0x0 RW	**BITS_PER_COLOR:** This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change can be done independent of a pixel clock change in DisplayPort. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. For further details on Display Port fixed frequency programming to accommodate these formats refer to DP Frequency Programming in DPLL section of Bspec. 000 = 8 bits per color (Default) 001 = 10 bits per color 010 = 6 bits per color 011 = RESERVED 1xx = RESERVED
4	0x0 RW	**DITHERING_ENABLE:** This bit enables dithering for DisplayPort 6bpc or 8bpc modes 0 Dithering disabled (Default) 1 Dithering enabled Programming note: Dithering should only be enabled for 8 bpc or 6 bpc.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0x0 RW	**DITHERING_TYPE:** This bit selects dithering type for DisplayPort 6bpc or 8bpc modes 00 - Spatial only (default) 01- Spatio-Temporal 1 10- Spatio-Temporal 2 (testmode) 11- Temporal only (testmode)
1	0x0 RW	**DDA_RESET_TEST_MODE:** 0 Do not reset DDA 1 Reset DDA every 8th display frame
0	0x0 RO	**RESERVED_1:** Write as zero

4.3.169 PIPEAGCMAXRED—Offset 70010h

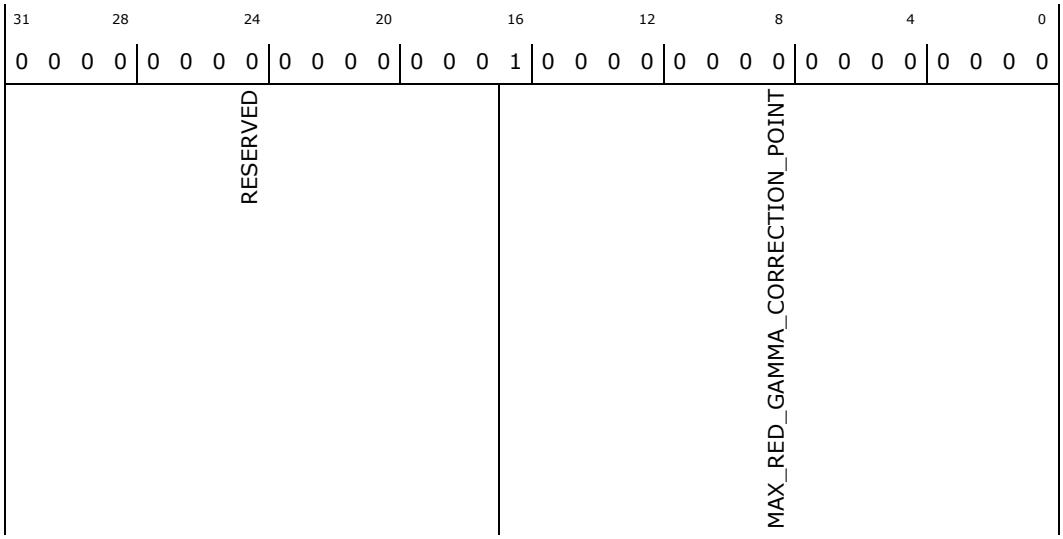
Pipe A Gamma Correction Max Red

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70010h

Default: 00010000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RESERVED:** Reserved.
16:0	0x10000 RW	**MAX_RED_GAMMA_CORRECTION_POINT:** 129th reference point for red channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0. Format: 11.6 Default: 0x10000

4.3.170 PIPEAGCMAXGREEN—Offset 70014h

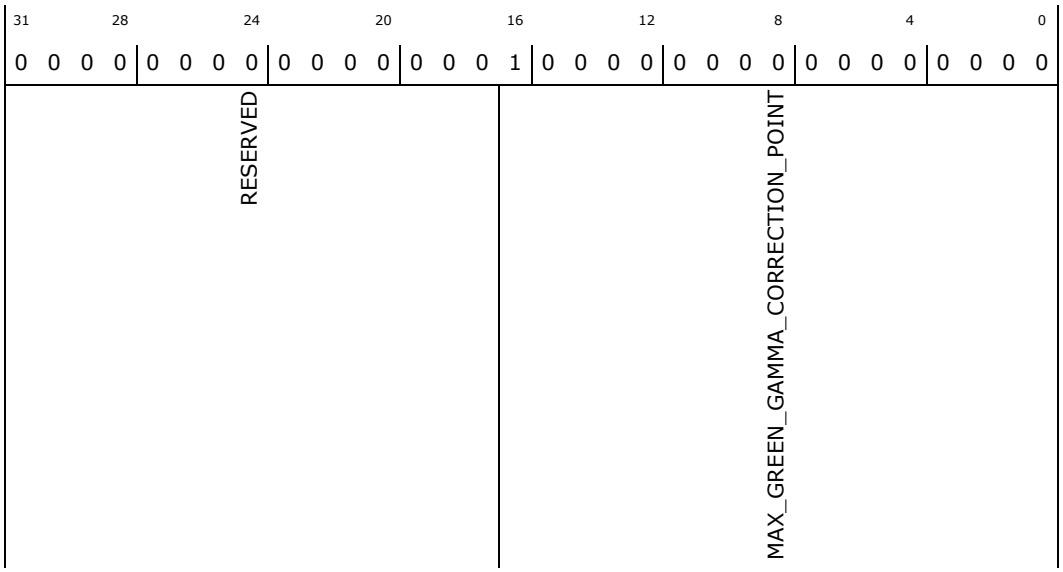
Pipe A Gamma Correction Max Green

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70014h

Default: 00010000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RESERVED:** Reserved.
16:0	0x10000 RW	**MAX_GREEN_GAMMA_CORRECTION_POINT:** 129th reference point for green channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0. Format: 11.6 Default: 0x10000

4.3.171 PIPEAGCMAXBLUE—Offset 70018h

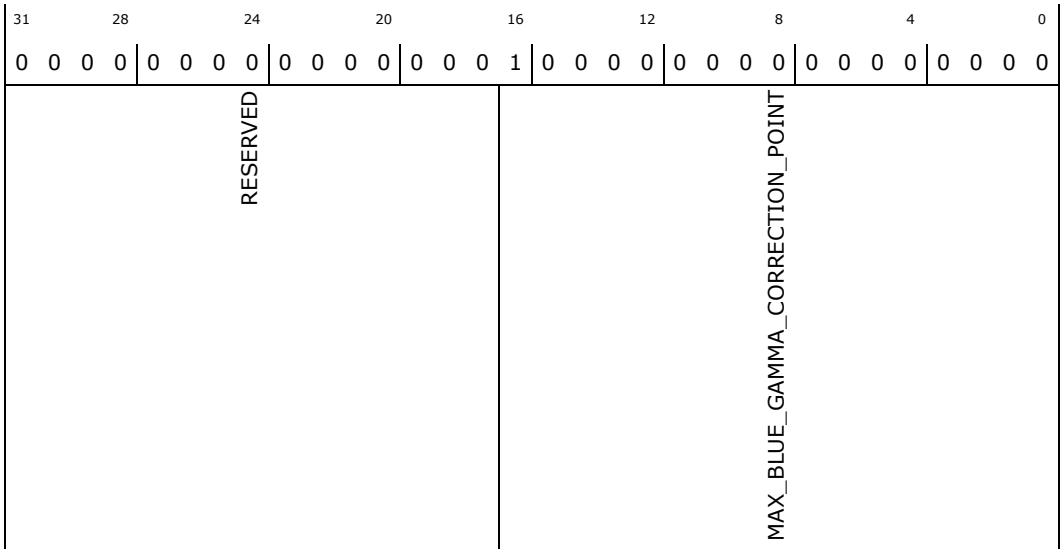
Pipe A Gamma Correction Max Blue

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70018h

Default: 00010000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RESERVED:** Reserved.
16:0	0x10000 RW	**MAX_BLUE_GAMMA_CORRECTION_POINT:** 129th reference point for blue channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0. Format: 11.6 Default: 0x10000

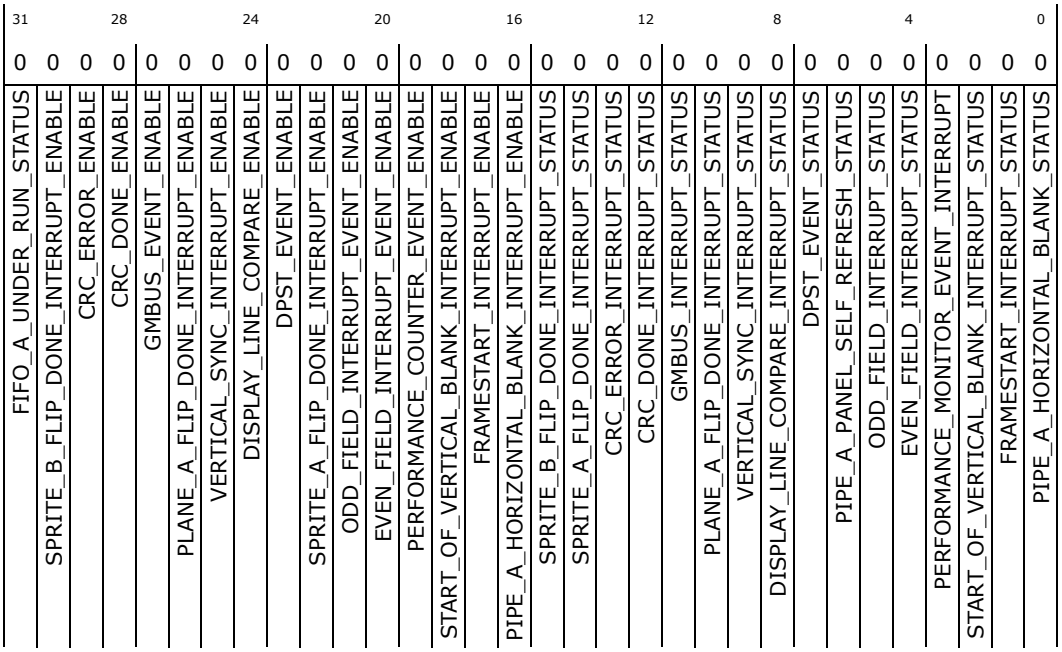
4.3.172 PIPEASTAT—Offset 70024h

Pipe A Display Status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70024h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C	**FIFO_A_UNDER_RUN_STATUS:** Set when a pipe A FIFO under-run occurs, cleared by a write of a 1. An underrun has occurred on an attempt to pop an empty FIFO. This does not feed into the first line interrupt status register. This will occur naturally during mode changes, to be useful, it should be cleared after a mode change has occurred. This bit is only valid after Pipe A has been completely configured. 1 = FIFO A Underflow occurred 0 = FIFO A Underflow did not occur AccessType: One to Clear
30	0x0 RW	**SPRITE_B_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Sprite B flip done interrupt status bit in the first line interrupt logic 0 = Sprite B Flip Done Interrupt Disabled 1 = Sprite B Flip Done Interrupt Enabled
29	0x0 RW	**CRC_ERROR_ENABLE:** This will enable the consideration of the CRC error status bit in the first line interrupt/status logic. 0 = CRC Error Detect Disabled 1 = CRC Error Detect Enabled
28	0x0 RW	**CRC_DONE_ENABLE:** This will enable the consideration of the CRC error status bit in the first line interrupt/status logic. 0 = CRC Done Detect Disabled 1 = CRC Done Detect Enabled
27	0x0 RW	**GMBUS_EVENT_ENABLE:** This will enable the use of the GMBUS interrupt status bit in the first line interrupt/status logic. 0 = No GMBUS event enabled 1 = GMBUS event enabled

Bit Range	Default & Access	Field Name (ID): Description
26	0x0 RW	**PLANE_A_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Plane A flip done interrupt status bit in the first line interrupt logic 0 = Plane A flip done Interrupt/Status Disabled 1 = Plane A flip done Interrupt/Status Enabled
25	0x0 RW	**VERTICAL_SYNC_INTERRUPT_ENABLE:** This will enable the consideration of the vertical sync interrupt status bit in the first line interrupt logic. 0 = Vertical Sync Interrupt/Status Disabled 1 = Vertical Sync Interrupt/Status Enabled
24	0x0 RW	**DISPLAY_LINE_COMPARE_ENABLE:** This will enable the consideration of the line compare interrupt status bit in the first line interrupt/status logic. 0 = Display Line Compare Interrupt/Status Disabled 1 = Display Line Compare Interrupt/Status Enabled
23	0x0 RW	**DPST_EVENT_ENABLE:** This interrupt is generated by the DPST logic. 0 = No DPST event enabled 1 = DPST event enabled
22	0x0 RW	**SPRITE_A_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Sprite A flip done interrupt status bit in the first line interrupt logic 0 = Sprite A Flip Done Interrupt Disabled 1 = Sprite A Flip Done Interrupt Enabled
21	0x0 RW	**ODD_FIELD_INTERRUPT_EVENT_ENABLE:** This bit should only be used when this pipe is in an interlaced display timing. 0 = Odd Field Event disable 1 = Odd Field Event enable
20	0x0 RW	**EVEN_FIELD_INTERRUPT_EVENT_ENABLE:** This bit should only be used when this pipe is in an interlaced display timing. 0 = Even field Event disable 1 = Even field Event enable
19	0x0 RW	**PERFORMANCE_COUNTER_EVENT_ENABLE:** Reserved.
18	0x0 RW	**START_OF_VERTICAL_BLANK_INTERRUPT_ENABLE:** This will enable the consideration of the start of vertical blank interrupt status bit in the first line interrupt/status logic. 0 = Start of Vertical Blank Interrupt/Status Disabled 1 = Start of Vertical Blank Interrupt/Status Enabled
17	0x0 RW	**FRAMESTART_INTERRUPT_ENABLE:** This will enable the consideration of the vertical blank interrupt status bit in the first line interrupt/status logic. 0 = Vertical Blank Interrupt/Status Disabled 1 = Vertical Blank Interrupt/Status Enabled
16	0x0 RW	**PIPE_A_HORIZONTAL_BLANK_INTERRUPT_ENABLE:** This will enable the consideration of the start of horizontal blank interrupt status bit in the first line interrupt/status logic0 = Start of Horizontal Blank Interrupt/Status Disabled 1 = Start of Horizontal Blank Interrupt/Status Enabled

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW/1C	**SPRITE_B_FLIP_DONE_INTERRUPT_STATUS:** MMIO Flip Event is completed on Sprite B 0 = Sprite B Flip Not Done 1 = Sprite B Flip Done AccessType: One to Clear
14	0x0 RW/1C	**SPRITE_A_FLIP_DONE_INTERRUPT_STATUS:** MMIO Flip Event is completed on Sprite A 0 = Sprite A Flip Not Done 1 = Sprite A Flip Done AccessType: One to Clear
13	0x0 RW/1C	**CRC_ERROR_INTERRUPT_STATUS:** This sticky status bit is set when a Pipe A CRC error is detected. It is cleared by a write of a one. For this bit to be meaningful, the pipe and pixel clock should be enabled and running. 0 = No CRC error has occurred 1 = CRC Error Detected AccessType: One to Clear
12	0x0 RW/1C	**CRC_DONE_INTERRUPT_STATUS:** This sticky status bit is set when Pipe A CRC calculation and compare are complete. It is cleared by a write of a one. For this bit to be meaningful, the pipe and pixel clock should be enabled and running. 0 = CRC Not Done 1 = CRC Done AccessType: One to Clear
11	0x0 RW/1C	**GMBUS_INTERRUPT_STATUS:** This status bit will be set on a GMBUS event. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. 0 = GMBUS event has not occurred 1 = GMBUS event has occurred AccessType: One to Clear
10	0x0 RW/1C	**PLANE_A_FLIP_DONE_INTERRUPT_STATUS:** Async/Sync Flip Event is completed on Display Plane A 0 = Plane A Flip Not Done 1 = Plane A Flip Done AccessType: One to Clear
9	0x0 RW/1C	**VERTICAL_SYNC_INTERRUPT_STATUS:** This bit provides a sticky status that is set when a pipe A vertical sync occurs, cleared by a write of a 1. For interlaced timing modes, this occurs once per field, when in progressive, it occurs once per frame. For this bit to be meaningful, the pipe and pixel clock should be enabled and running. 0 = Vertical Sync has not occurred 1 = Vertical Sync has occurred AccessType: One to Clear
8	0x0 RW/1C	**DISPLAY_LINE_COMPARE_INTERRUPT_STATUS:** Set when a pipe A compare match occurs, cleared by a write of a 1. 0 = Display Line Compare has not been satisfied 1 = Display Line Compare has been satisfied AccessType: One to Clear

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW/1C	**DPST_EVENT_STATUS:** This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the value of the bit. Multiple DPST events (Histogram or Phase In) can cause this bit to be asserted, determination of which event occurred is done in the DPST registers. 0 = DPST Interrupt has not occurred on pipe A 1 = DPST Interrupt has occurred on pipe A AccessType: One to Clear
6	0x0 RW/1C	**PIPE_A_PANEL_SELF_REFRESH_STATUS:** This bit indicates interrupt is generated by the PSR controller and intends to send interrupt to SW driver when the PSR interrupt enable bit (70028h bit 22) is set. This is cleared when a write to this register occurs with this bit as a one. Write with this bit as a zero has no effect on the value of the bit. 0 = PSR Interrupt has not occurred on pipe A 1 = PSR interrupt has occurred on pipe A AccessType: One to Clear
5	0x0 RW/1C	**ODD_FIELD_INTERRUPT_STATUS:** This status bit will be set on a Odd field VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates, the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. Note: This bit will not be set when pipe is in Interlaced with Field 0 Only using legacy vertical sync shift mode. 0 = Odd Field Vertical Blank has not occurred 1 = Odd Field Vertical Blank has occurred AccessType: One to Clear
4	0x0 RW/1C	**EVEN_FIELD_INTERRUPT_STATUS:** This status bit will be set on a even field VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates, the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. Note: This bit will not be set when pipe is in Interlaced with Field 0 Only using legacy vertical sync shift mode. 0 = Even Field Vertical Blank has not occurred 1 = Even Field Vertical Blank has occurred AccessType: One to Clear
3	0x0 RW/1C	**PERFORMANCE_MONITOR_EVENT_INTERRUPT:** AccessType: One to Clear
2	0x0 RW/1C	**START_OF_VERTICAL_BLANK_INTERRUPT_STATUS:** This status bit will be set at the beginning of a VBLANK event. At this point, the double buffered display registers flip, taking their new values. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. In MIPI DSR mode, GPIO TE trigger sets the Vblank Interrupt status 0 = Start of Vertical Blank has not occurred 1 = Start of Vertical Blank has occurred AccessType: One to Clear

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW/1C	**FRAMESTART_INTERRUPT_STATUS:** This status bit will be set on a VBLANK event, when the frame start occurs. The display registers are updated at the start of vertical blank, but the new register data is not utilized by the display pipeline until the point in the vertical blank period when the frame start occurs, which is the event that triggers this bit. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. 0 = Vertical Blank has not occurred 1 = Vertical Blank has occurred AccessType: One to Clear
0	0x0 RW/1C	**PIPE_A_HORIZONTAL_BLANK_STATUS:** 0 = Pipe A Horizontal Blank has not occurred 1 = Pipe A Horizontal Blank has occurred AccessType: One to Clear

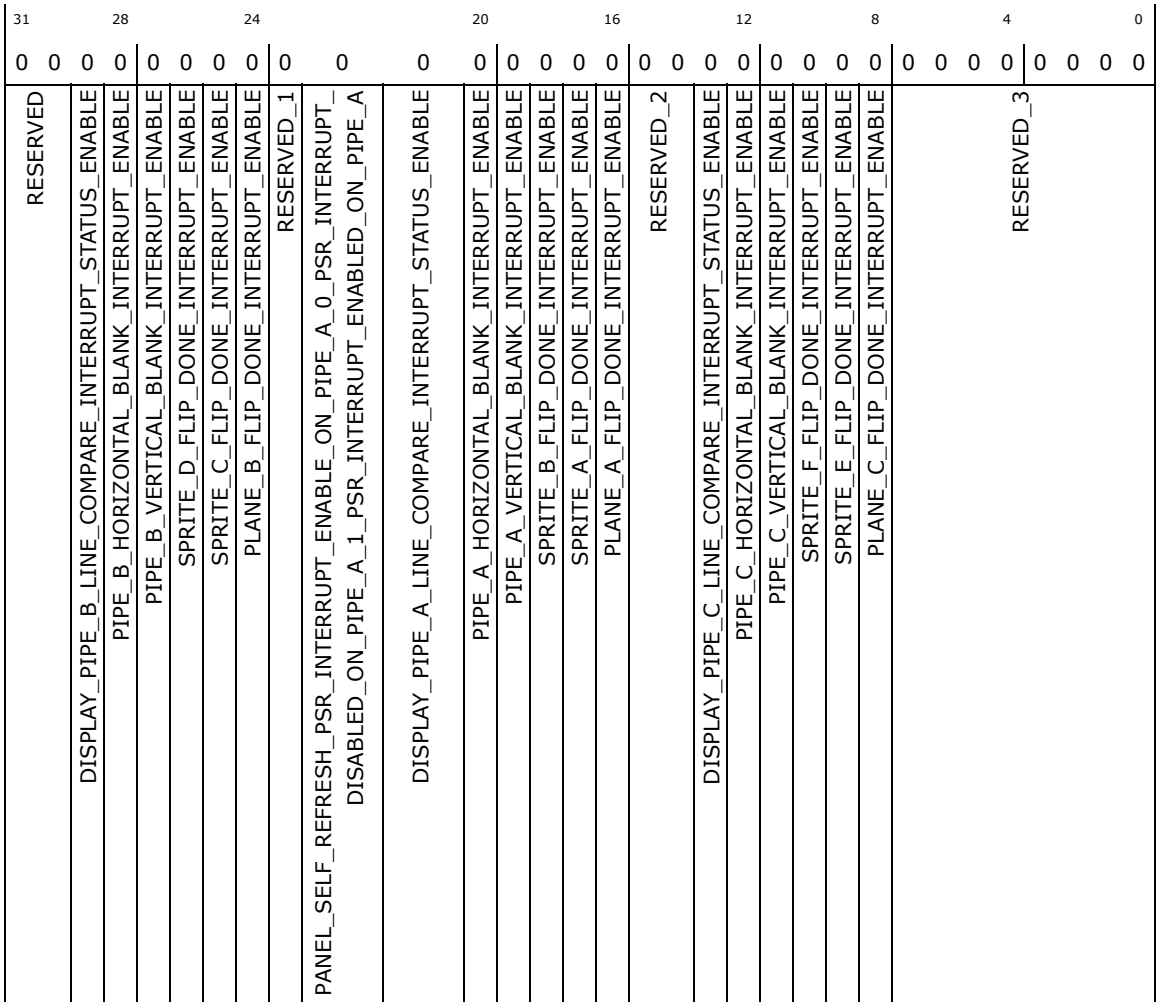
4.3.173 DPFLIPSTAT—Offset 70028h

Display FLIP Status Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70028h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RESERVED:** MBZ
29	0x0 RW	**DISPLAY_PIPE_B_LINE_COMPARE_INTERRUPT_STATUS_ENABLE:** 0 = Display Pipe B Line Compare Interrupt Disabled 1 = Display Pipe B Line Compare Interrupt Enabled
28	0x0 RW	**PIPE_B_HORIZONTAL_BLANK_INTERRUPT_ENABLE:** 0 = Pipe B Horizontal Blank Interrupt Disabled 1 = Pipe B Horizontal Blank Interrupt Enabled
27	0x0 RW	**PIPE_B_VERTICAL_BLANK_INTERRUPT_ENABLE:** 0 = Pipe B Vertical Blank Interrupt Disabled 1 = Pipe B Vertical Blank Interrupt Enabled
26	0x0 RW	**SPRITE_D_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Sprite D Flip Done Interrupt Disabled 1 = Sprite D Flip Done Interrupt Enabled

Bit Range	Default & Access	Field Name (ID): Description
25	0x0 RW	**SPRITE_C_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Sprite C Flip Done Interrupt Disabled 1 = Sprite C Flip Done Interrupt Enabled
24	0x0 RW	**PLANE_B_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Plane B Flip Done Interrupt Disabled 1 = Plane B Flip Done Interrupt Enabled
23	0x0 RO	**RESERVED_1:** Reserved.
22	0x0 RW	**PANEL_SELF_REFRESH_PSR_INTERRUPT_ENABLE_ON_PIPE_A_0_PSR_INTERRUPT_DISABLED_ON_PIPE_A_1_PSR_INTERRUPT_ENABLED_ON_PIPE_A:** Reserved.
21	0x0 RW	**DISPLAY_PIPE_A_LINE_COMPARE_INTERRUPT_STATUS_ENABLE:** 0 = Display Pipe A Line Compare Interrupt Disabled 1 = Display Pipe A Line Compare Interrupt Enabled
20	0x0 RW	**PIPE_A_HORIZONTAL_BLANK_INTERRUPT_ENABLE:** 0 = Pipe A Horizontal Blank Interrupt Disabled 1 = Pipe A Horizontal Blank Interrupt Enabled
19	0x0 RW	**PIPE_A_VERTICAL_BLANK_INTERRUPT_ENABLE:** 0 = Pipe A Vertical Blank Interrupt Disabled 1 = Pipe A Vertical Blank Interrupt Enabled
18	0x0 RW	**SPRITE_B_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Sprite B Flip Done Interrupt Disabled 1 = Sprite B Flip Done Interrupt Enabled
17	0x0 RW	**SPRITE_A_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Sprite A Flip Done Interrupt Disabled 1 = Sprite A Flip Done Interrupt Enabled
16	0x0 RW	**PLANE_A_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Plane A Flip Done Interrupt Disabled 1 = Plane A Flip Done Interrupt Enabled
15:14	0x0 RO	**RESERVED_2:** MBZ
13	0x0 RW	**DISPLAY_PIPE_C_LINE_COMPARE_INTERRUPT_STATUS_ENABLE:** 0 = Display Pipe C Line Compare Interrupt Disabled 1 = Display Pipe A Line Compare Interrupt Enabled
12	0x0 RW	**PIPE_C_HORIZONTAL_BLANK_INTERRUPT_ENABLE:** 0 = Pipe C Horizontal Blank Interrupt Disabled 1 = Pipe A Horizontal Blank Interrupt Enabled
11	0x0 RW	**PIPE_C_VERTICAL_BLANK_INTERRUPT_ENABLE:** 0 = Pipe C Vertical Blank Interrupt Disabled 1 = Pipe A Vertical Blank Interrupt Enabled
10	0x0 RW	**SPRITE_F_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Sprite F Flip Done Interrupt Disabled 1 = Sprite B Flip Done Interrupt Enabled
9	0x0 RW	**SPRITE_E_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Sprite E Flip Done Interrupt Disabled 1 = Sprite A Flip Done Interrupt Enabled

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**PLANE_C_FLIP_DONE_INTERRUPT_ENABLE:** 0 = Plane C Flip Done Interrupt Disabled 1 = Plane A Flip Done Interrupt Enabled
7:0	0x0 RO	**RESERVED_3:** MBZ

4.3.174 DPINVGTT—Offset 7002Ch

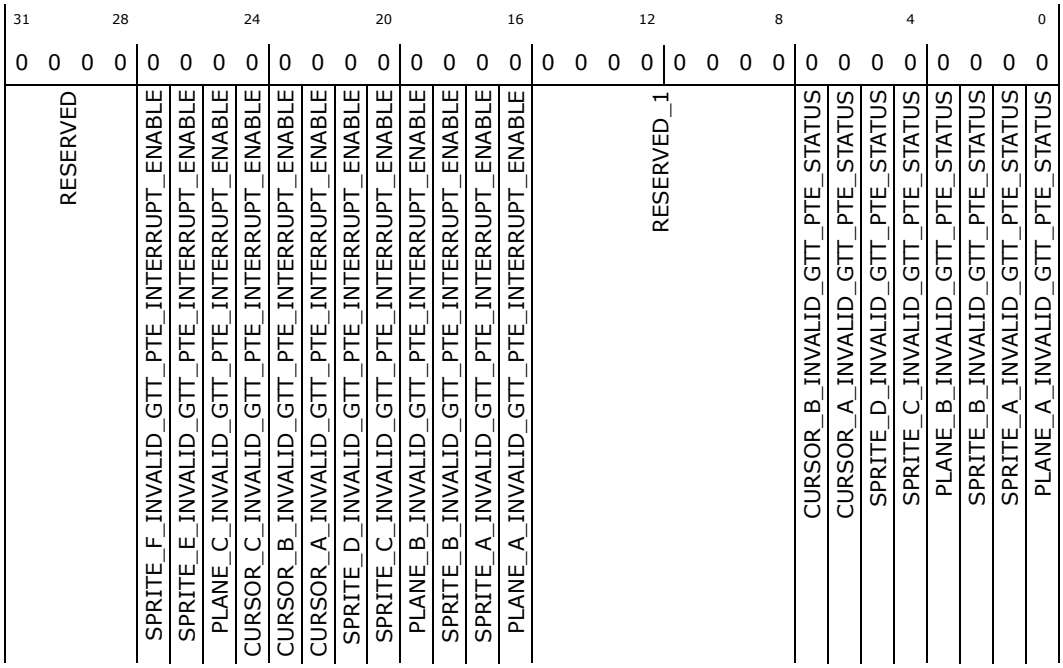
Display Invalid GTT PTE Status Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 7002Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** MBZ
27	0x0 RW	**SPRITE_F_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Sprite F Invalid GTT PTE Interrupt Disabled 1 = Sprite F Invalid GTT PTE Interrupt Enabled
26	0x0 RW	**SPRITE_E_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Sprite E Invalid GTT PTE Interrupt Disabled 1 = Sprite E Invalid GTT PTE Interrupt Enabled

Bit Range	Default & Access	Field Name (ID): Description
25	0x0 RW	**PLANE_C_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Plane C Invalid GTT PTE Interrupt Disabled 1 = Plane C Invalid GTT PTE Interrupt Enabled
24	0x0 RW	**CURSOR_C_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Cursor C Invalid GTT PTE Interrupt Disabled 1 = Cursor C Invalid GTT PTE Interrupt Enabled
23	0x0 RW	**CURSOR_B_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Cursor B Invalid GTT PTE Interrupt Disabled 1 = Cursor B Invalid GTT PTE Interrupt Enabled
22	0x0 RW	**CURSOR_A_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Cursor A Invalid GTT PTE Interrupt Disabled 1 = Cursor A Invalid GTT PTE Interrupt Enabled
21	0x0 RW	**SPRITE_D_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Sprite D Invalid GTT PTE Interrupt Disabled 1 = Sprite D Invalid GTT PTE Interrupt Enabled
20	0x0 RW	**SPRITE_C_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Sprite C Invalid GTT PTE Interrupt Disabled 1 = Sprite C Invalid GTT PTE Interrupt Enabled
19	0x0 RW	**PLANE_B_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Plane B Invalid GTT PTE Interrupt Disabled 1 = Plane B Invalid GTT PTE Interrupt Enabled
18	0x0 RW	**SPRITE_B_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Sprite B Invalid GTT PTE Interrupt Disabled 1 = Sprite B Invalid GTT PTE Interrupt Enabled
17	0x0 RW	**SPRITE_A_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Sprite A Invalid GTT PTE Interrupt Disabled 1 = Sprite A Invalid GTT PTE Interrupt Enabled
16	0x0 RW	**PLANE_A_INVALID_GTT_PTE_INTERRUPT_ENABLE:** 0 = Plane A Invalid GTT PTE Interrupt Disabled 1 = Plane A Invalid GTT PTE Interrupt Enabled
15:8	0x0 RO	**RESERVED_1:** MBZ
7	0x0 RW/1C	**CURSOR_B_INVALID_GTT_PTE_STATUS:** 0 = Cursor B encountered an invalid GTT PTE has not occurred 1 = Cursor B encountered an invalid GTT PTE has occurred AccessType: One to Clear
6	0x0 RW/1C	**CURSOR_A_INVALID_GTT_PTE_STATUS:** 0 = Cursor A encountered an invalid GTT PTE has not occurred 1 = Cursor A encountered an invalid GTT PTE has occurred AccessType: One to Clear
5	0x0 RW/1C	**SPRITE_D_INVALID_GTT_PTE_STATUS:** 0 = Sprite D encountered an invalid GTT PTE has not occurred 1 = Sprite D encountered an invalid GTT PTE has occurred. AccessType: One to Clear
4	0x0 RW/1C	**SPRITE_C_INVALID_GTT_PTE_STATUS:** 0 = Sprite C encountered an invalid GTT PTE has not occurred 1 = Sprite C encountered an invalid GTT PTE has occurred. AccessType: One to Clear

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW/1C	**PLANE_B_INVALID_GTT_PTE_STATUS:** 0 = Plane B encountered an invalid GTT PTE has not occurred 1 = Plane B encountered an invalid GTT PTE has occurred. AccessType: One to Clear
2	0x0 RW/1C	**SPRITE_B_INVALID_GTT_PTE_STATUS:** 0 = Sprite B encountered an invalid GTT PTE has not occurred 1 = Sprite B encountered an invalid GTT PTE has occurred. AccessType: One to Clear
1	0x0 RW/1C	**SPRITE_A_INVALID_GTT_PTE_STATUS:** 0 = Sprite A encountered an invalid GTT PTE has not occurred 1 = Sprite A encountered an invalid GTT PTE has occurred. AccessType: One to Clear
0	0x0 RW/1C	**PLANE_A_INVALID_GTT_PTE_STATUS:** 0 = Plane A encountered an invalid GTT PTE has not occurred 1 = Plane A encountered an invalid GTT PTE has occurred. AccessType: One to Clear

4.3.175 DSPARB—Offset 70030h

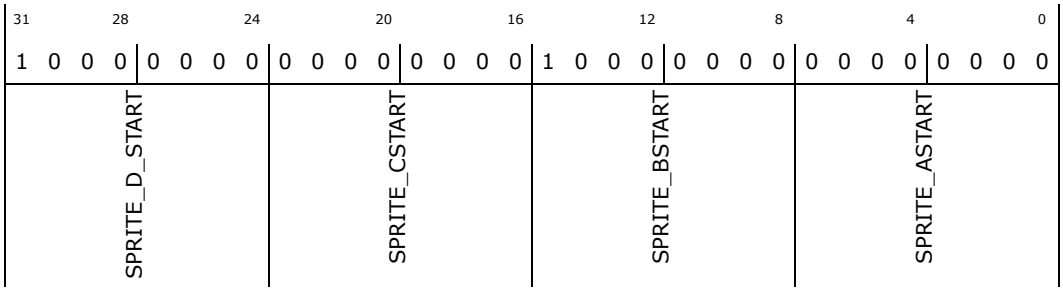
Display Arbitration Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70030h

Default: 80008000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x80 RW	**SPRITE_D_START:** This field selects the end of the ram used for Sprite C and the start of the RAM for Sprite D. If sprite C is unused, this field can be set to the same value as Sprite C START. If Sprite D is unused, this field can be set to TOTALSIZE-1. It must be programmed to a number greater than or equal to the value in Sprite C START and less than the total size of the RAM (TOTALSIZE). The size of the Sprite C FIFO will be (Sprite D START-Sprite C START)*64. The size of the Sprite D FIFO will be (TOTALSIZE-Sprite D START-1) *64 bytes. [DevBLC and DevCTG]: Reserved: Write as zero.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0x0 RW	**SPRITE_CSTART:** This field selects the end of the ram used for display B and the start of the RAM for Sprite C. If display B is unused, this field can be set to zero. The value should never exceed the size of the RAM (TOTALSIZE). The size of the display B FIFO will be (Sprite C START)*64 bytes.
15:8	0x80 RW	**SPRITE_BSTART:** This field selects the end of the ram used for Sprite A and the start of the RAM for Sprite B. If sprite A is unused, this field can be set to the same value as Sprite A START. If Sprite B is unused, this field can be set to TOTALSIZE-1. It must be programmed to a number greater than or equal to the value in Sprite A START and less than the total size of the RAM (TOTALSIZE). The size of the Sprite A FIFO will be (Sprite B START-Sprite A START)*64. The size of the Sprite B FIFO will be (TOTALSIZE-Sprite B START-1) *64 bytes. [DevBLC and DevCTG]: Reserved: Write as zero.
7:0	0x0 RW	**SPRITE_ASTART:** This field selects the end of the ram used for display A and the start of the RAM for Sprite A. If display A is unused, this field can be set to zero. The value should never exceed the size of the RAM (TOTALSIZE). The size of the display A FIFO will be (Sprite A START)*64 bytes.

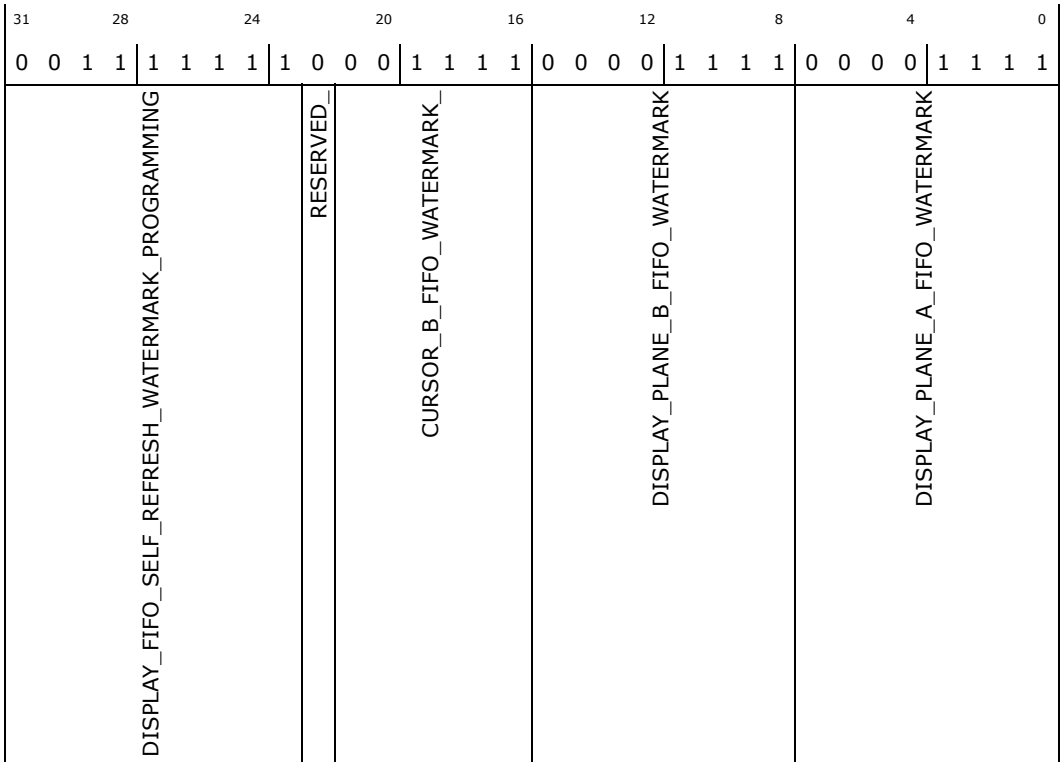
4.3.176 FW1—Offset 70034h

Display FIFO Watermark Control 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70034h

Default: 3F8F0F0Fh



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x7f RW	**DISPLAY_FIFO_SELF_REFRESH_WATERMARK_PROGRAMMING:** This register defines the value of the watermark used by the Display streamer in case the CPU is in C2/C3/C4 and the memory has entered self refresh. Number in 64Bs of space in FIFO above which the Display Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).Note: When calculating watermark values for 15/16bpp display formats, assume 32bpp for purposes of calculation using the high priority bandwidth analysis spreadsheet.
22	0x0 RO	**RESERVED_:** MBZ
21:16	0xf RW	**CURSOR_B_FIFO_WATERMARK_:** Number in 64Bs of space in the Cursor B FIFO above which the Cursor B Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet). Always program to 8.
15:8	0xf RW	**DISPLAY_PLANE_B_FIFO_WATERMARK:** Number in 64Bs of space in FIFO above which the Display B Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet). Always program to 8.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0xf RW	**DISPLAY_PLANE_A_FIFO_WATERMARK:** Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet). Always program to 8.

4.3.177 FW2—Offset 70038h

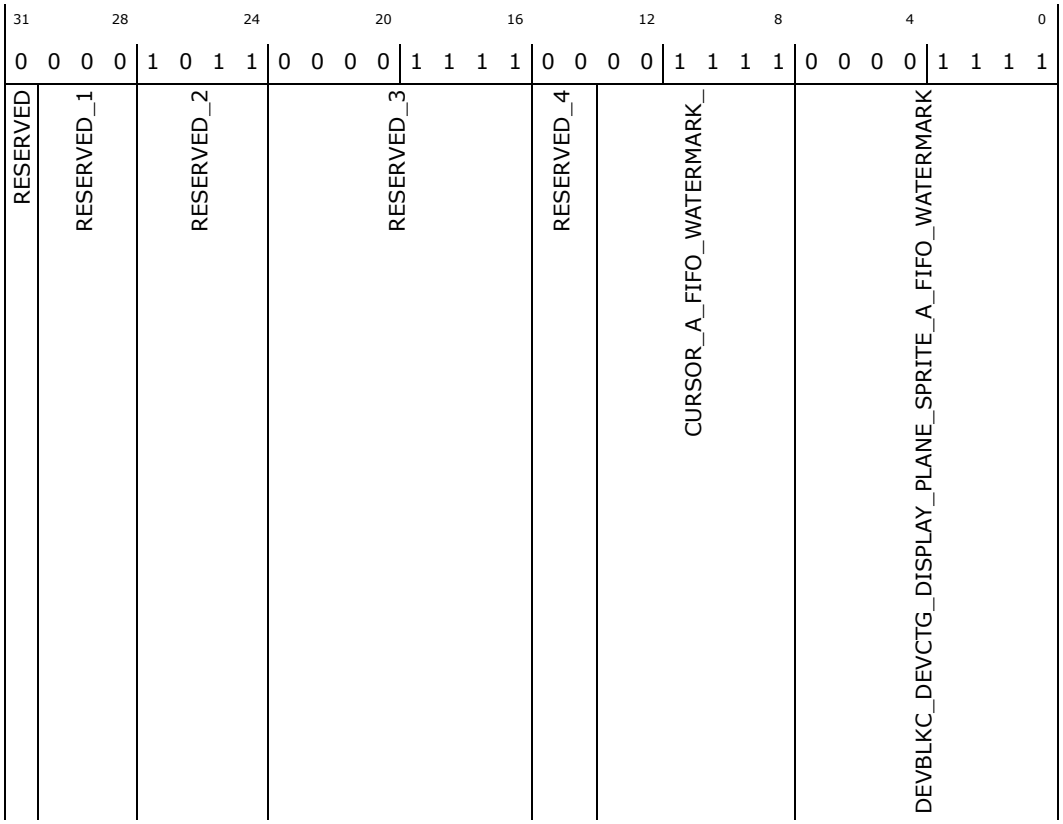
Display FIFO Watermark Control 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70038h

Default: 0B0F0F0Fh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** [DevCTG] FBC SR Watermark Enable: Enables the FBC watermarks to be used in the fetch calculation 0: disabled 1: enabled
30:28	0x0 RO	**RESERVED_1:** [DevCTG] FBC SR Watermark: Number of equivalent lines of the primary display SR watermark
27:24	0xb RO	**RESERVED_2:** [DevCTG] FBC SR HPLL Watermark: Number of equivalent lines of the primary display SR HPLL watermark.
23:16	0xf RO	**RESERVED_3:** [DevBLKC, DevCTG] Display Plane Sprite B FIFO Watermark Number in 64Bs of space in FIFO above which the Display Sprite B Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
15:14	0x0 RO	**RESERVED_4:** MBZ
13:8	0xf RW	**CURSOR_A_FIFO_WATERMARK_:** Number in 64Bs of space in the Cursor A FIFO above which the Cursor A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet). Always program to 8.
7:0	0xf RW	**DEVBLKC_DEVCTG_DISPLAY_PLANE_SPRITE_A_FIFO_WATERMARK:** Number in 64Bs of space in FIFO above which the Display Sprite A Stream will generate requests to Memory DevBW, DevCL] Display Plane C FIFO Watermark. Number in 64Bs of space in FIFO above which the Display C Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet). Always program to 8.

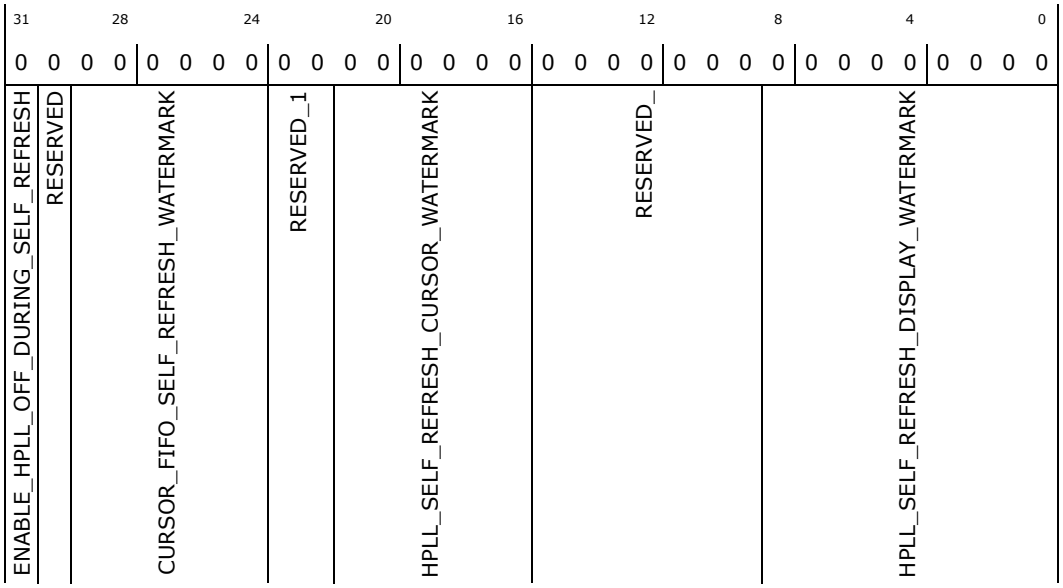
4.3.178 FW3—Offset 7003Ch

Display FIFO Watermark Control 3

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7003Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**ENABLE_HPLL_OFF_DURING_SELF_REFRESH:** . 0 = Disabled 1 = Enabled [DevCL] This bit may be enabled only if the BLC_PWM_CTL duty cycle register offset (0x61254) is programmed to 100% and non-legacy backlight is enabled. This restriction does not apply when I2C is used for back light modulation. [DevCL] When one or more display pipes are enabled, this bit should be disabled before accessing the 6XXXh MMIO register address space. Software must follow these steps: disable this bit (if enabled and one display pipe is enabled) wait for next vblank (switch from hrawclk back to cdclk will occur) access the 6XXXh address space as needed re-enable this bit Note that the wait on next vblank step requires an enabled display pipe.
30	0x0 RO	**RESERVED:** MBZ
29:24	0x0 RW	**CURSOR_FIFO_SELF_REFRESH_WATERMARK:** . Number in 64Bs of space in the Cursor FIFO above which the Cursor Stream will generate requests to Memory during self -refresh. (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
23:22	0x0 RO	**RESERVED_1:** MBZ
21:16	0x0 RW	**HPLL_SELF_REFRESH_CURSOR_WATERMARK:** . Number in 64Bs of space in the Cursor FIFO above which the Cursor Stream will generate requests to Memory during HPLL self -refresh. (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
15:9	0x0 RO	**RESERVED_:** MBZ

Bit Range	Default & Access	Field Name (ID): Description
8:0	0x0 RW	**HPLL_SELF_REFRESH_DISPLAY_WATERMARK:** . Number in 64Bs of space in the FIFO above which the Display Stream will generate requests to Memory during HPLL self -refresh. (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

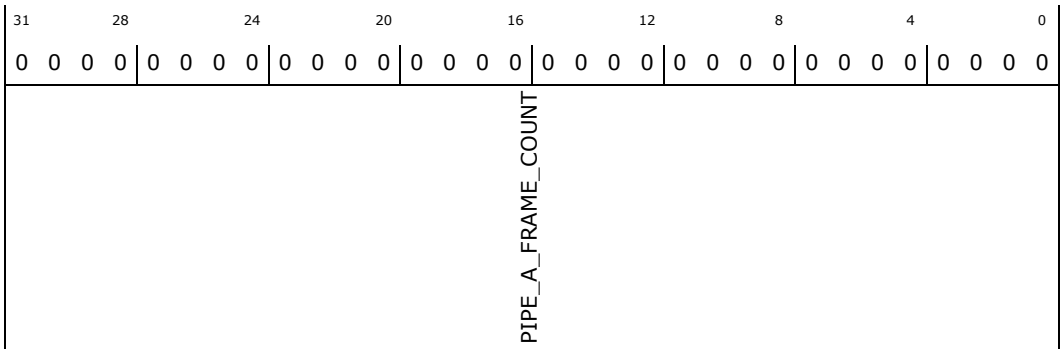
4.3.179 PIPEAFRAMECOUNT—Offset 70040h

Pipe A Frame Count High

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70040h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**PIPE_A_FRAME_COUNT:** Provides read back of the display pipe frame counter. This counter increments on every start of vertical blank and rolls over back to 0 after 2^32 frames

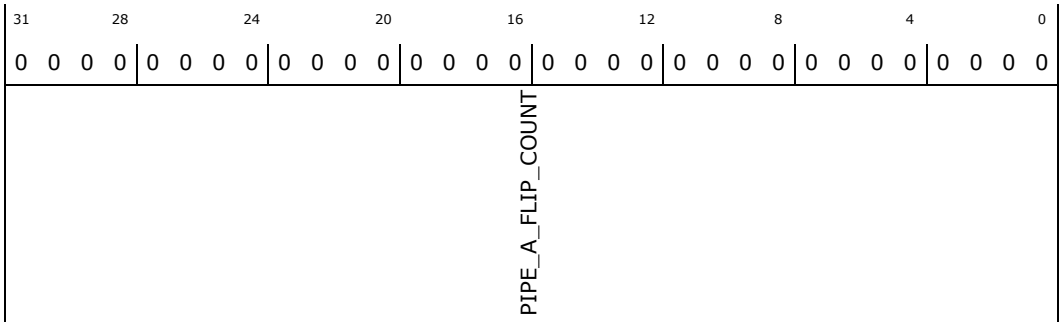
4.3.180 PIPEAFLIPCOUNT—Offset 70044h

Pipe A FLIP COUNTER

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70044h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**PIPE_A_FLIP_COUNT:** Provides read back of the display pipe flip counter. This counter increments on each flip of the surface of the primary plane on this pipe. This includes command streamer asynchronous and synchronous flips and any MMIO writes to the primary plane surface address. It rolls over back to 0 after 2^32 flips.

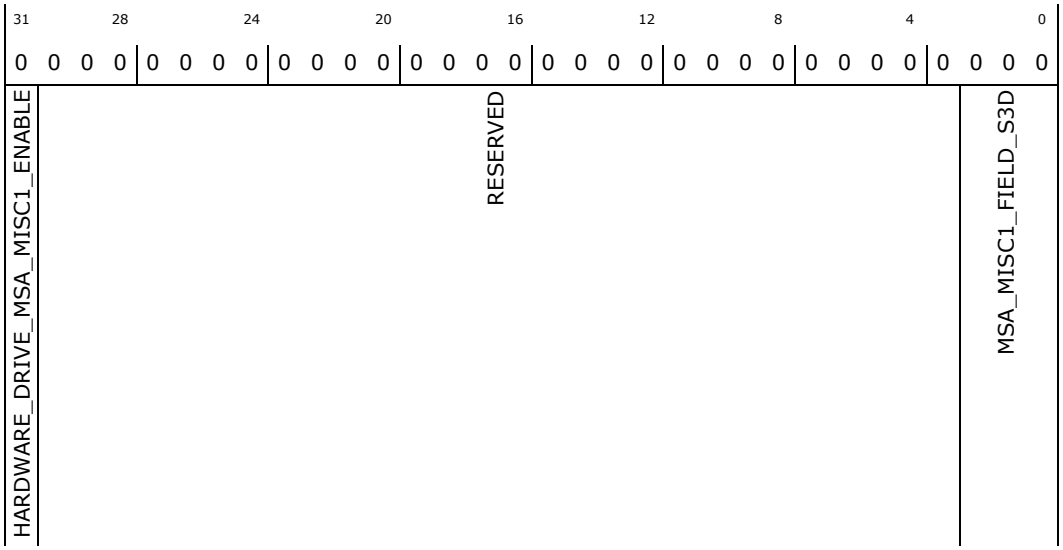
4.3.181 PIPEAMSAMISC—Offset 70048h

Pipe A MSA MISC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70048h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**HARDWARE_DRIVE_MSA_MISC1_ENABLE:** This bit enables hardware to drive MSA MISC1 bit3:1 with the stereo 3D left/right eye field indication. Hardware will drive 000 when S3D mode is disabled, 001 when enabled and the upcoming video frame is right eye, 011 when enabled and the upcoming video frame is left eye. When this bit is disabled, software may manually program the MSA MISC1 Field S3D field in bit 2:0 in this register to set MISC1 bit 3:1 0 = Disable hardware driving MSA MISC1 bit 3:1. Allow software to manually program MSA MISC1 bit3:1 through MSA_MISC1_FIELD_S3D (default) 1 = Enable hardware to drive MSA MISC1 bit3:1 for S3D
30:3	0x0 RO	**RESERVED:** Reserved.
2:0	0x0 RW	**MSA_MISC1_FIELD_S3D:** This field provides software to manually program MSC1 stereo video attribute for DisplayPort: 000 = No stereo video transported 001 = For progressive video, the next (upcoming) video frame is RIGHT eye 010 = Reserved 011 = For progressive video, the next (upcoming) video frame is LEFT eye 100 = Stacked top and bottom top half represents left-eye view and bottom half represents right-eye view 101 = Stacked top and bottom top half represents right-eye view and bottom half represents left-eye view

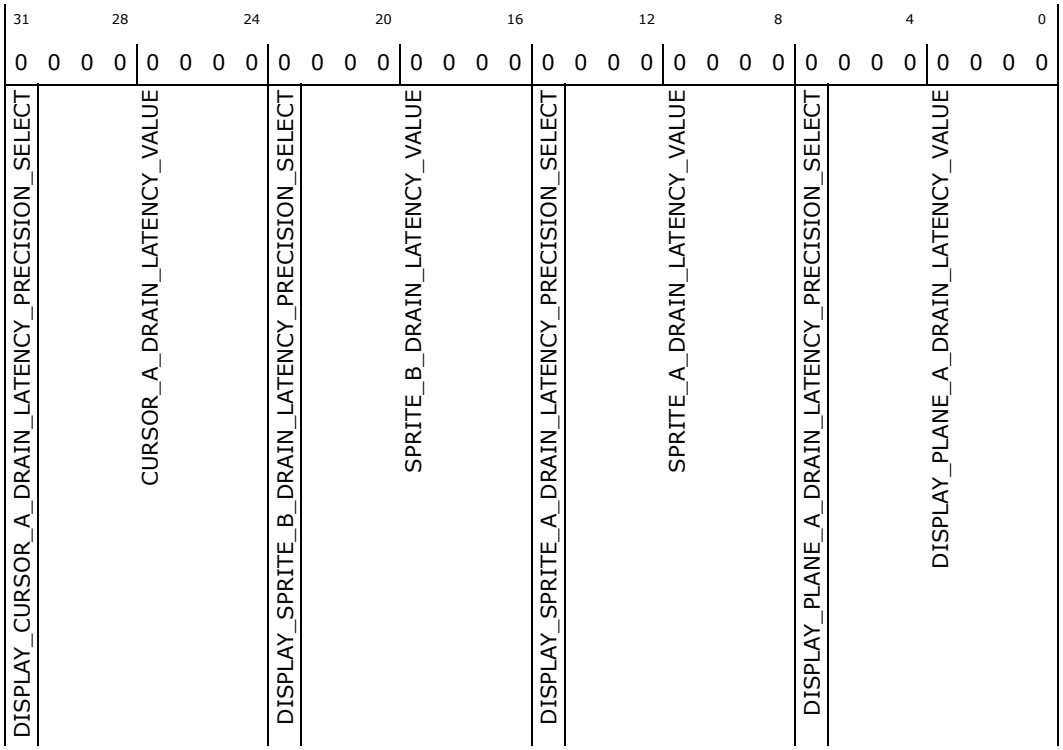
4.3.182 DDL1—Offset 70050h

Display FIFO Drain Latency 1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70050h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**DISPLAY_CURSOR_A_DRAIN_LATENCY_PRECISION_SELECT:** 1 use 32 as precision multiplier to increase precision to be stored in 7-bit Cursor A drain latency value 0 use 16 as precision multiplier to increase precision to be stored in 7-bit Cursor A drain latency value
30:24	0x0 RW	**CURSOR_A_DRAIN_LATENCY_VALUE:** For cursor latency, 4 BPP is assumed for all cursor formats. : Programmable drain latency value in time ticks per 64B FIFO entry
23	0x0 RW	**DISPLAY_SPRITE_B_DRAIN_LATENCY_PRECISION_SELECT:** 1 use 32 as precision multiplier to increase precision to be stored in 7-bit Sprite B drain latency value 0 use 16 as precision multiplier to increase precision to be stored in 7-bit Sprite B drain latency value
22:16	0x0 RW	**SPRITE_B_DRAIN_LATENCY_VALUE:** Programmable drain latency value in time ticks per 64B FIFO entry
15	0x0 RW	**DISPLAY_SPRITE_A_DRAIN_LATENCY_PRECISION_SELECT:** 1 use 32 as precision multiplier to increase precision to be stored in 7-bit Sprite A drain latency value 0 use 16 as precision multiplier to increase precision to be stored in 7-bit Sprite A drain latency value
14:8	0x0 RW	**SPRITE_A_DRAIN_LATENCY_VALUE:** Programmable drain latency value in time ticks per 64B FIFO entry

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW	**DISPLAY_PLANE_A_DRAIN_LATENCY_PRECISION_SELECT:** 1 use 32 as precision multiplier to increase precision to be stored in 7-bit Plane A drain latency value 0 use 16 as precision multiplier to increase precision to be stored in 7-bit Plane A drain latency value
6:0	0x0 RW	**DISPLAY_PLANE_A_DRAIN_LATENCY_VALUE:** Programmable drain latency value in time ticks per 64B FIFO entry

4.3.183 DDL2—Offset 70054h

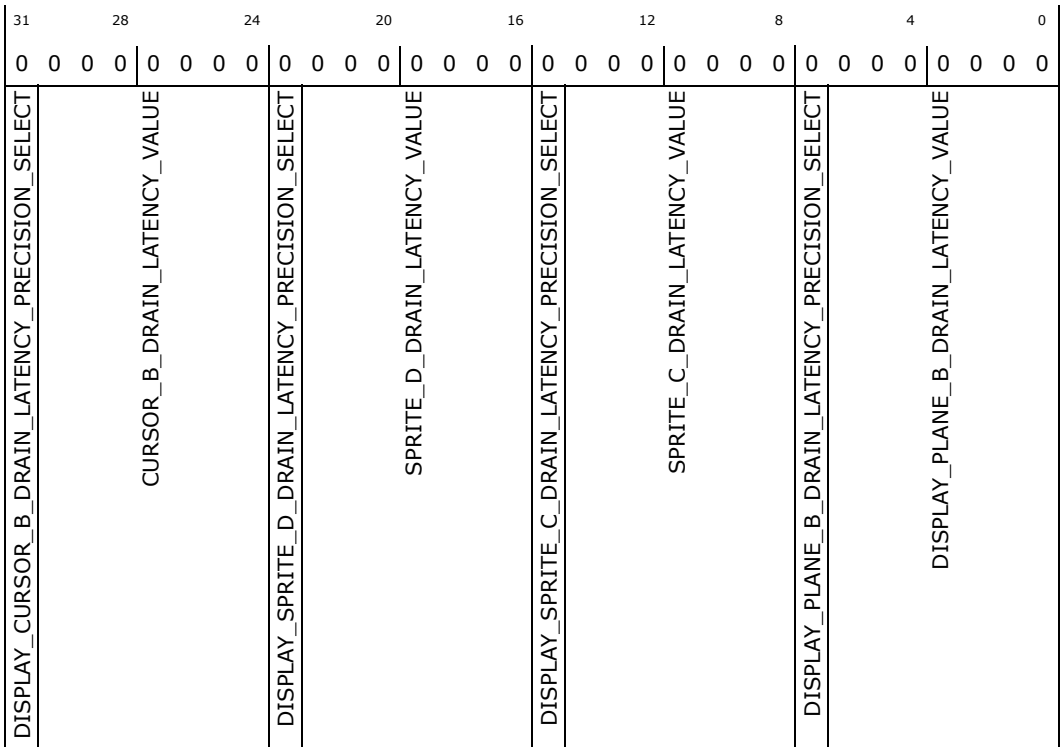
Display FIFO Drain Latency 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70054h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**DISPLAY_CURSOR_B_DRAIN_LATENCY_PRECISION_SELECT:** 1 use 32 as precision multiplier to increase precision to be stored in 7-bit Cursor B drain latency value 0 use 16 as precision multiplier to increase precision to be stored in 7-bit Cursor B drain latency value
30:24	0x0 RW	**CURSOR_B_DRAIN_LATENCY_VALUE:** For cursor latency, 4 BPP is assumed for all cursor formats
23	0x0 RW	**DISPLAY_SPRITE_D_DRAIN_LATENCY_PRECISION_SELECT:** 1 use 32 as precision multiplier to increase precision to be stored in 7-bit Sprite D drain latency value 0 use 16 as precision multiplier to increase precision to be stored in 7-bit Sprite D drain latency value
22:16	0x0 RW	**SPRITE_D_DRAIN_LATENCY_VALUE:**
15	0x0 RW	**DISPLAY_SPRITE_C_DRAIN_LATENCY_PRECISION_SELECT:** 1 use 32 as precision multiplier to increase precision to be stored in 7-bit Sprite C drain latency value 0 use 16 as precision multiplier to increase precision to be stored in 7-bit Sprite C drain latency value
14:8	0x0 RW	**SPRITE_C_DRAIN_LATENCY_VALUE:**
7	0x0 RW	**DISPLAY_PLANE_B_DRAIN_LATENCY_PRECISION_SELECT:** 1 use 32 as precision multiplier to increase precision to be stored in 7-bit Plane B drain latency value 0 use 16 as precision multiplier to increase precision to be stored in 7-bit Plane B drain latency value
6:0	0x0 RW	**DISPLAY_PLANE_B_DRAIN_LATENCY_VALUE:**

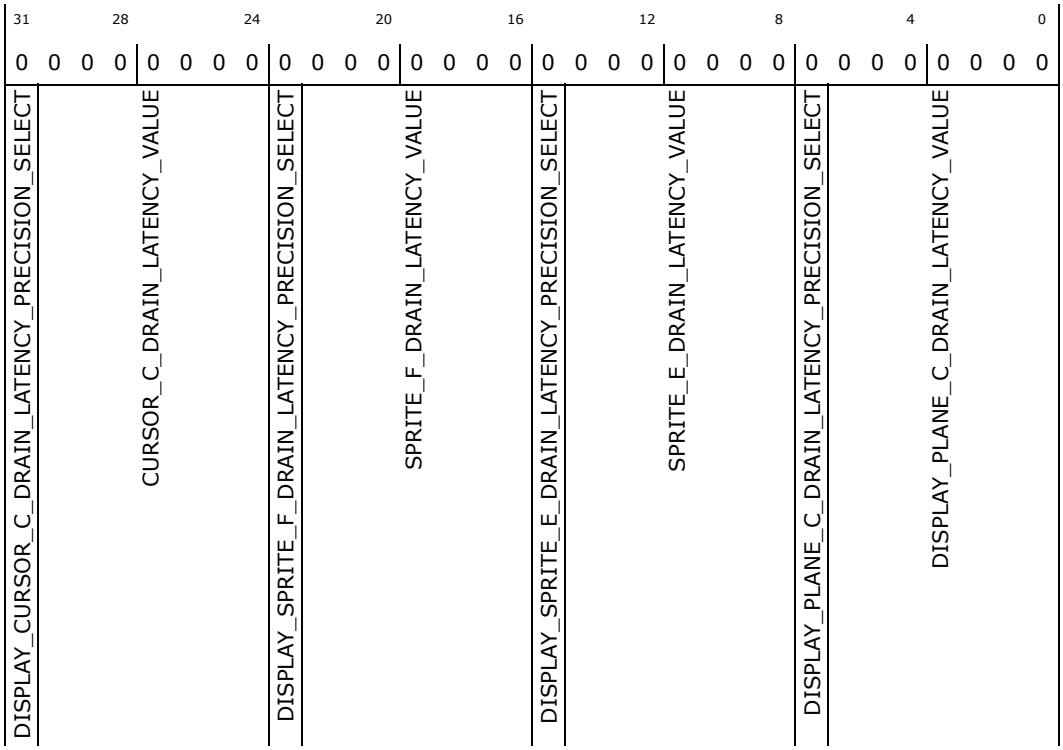
4.3.184 DDL3—Offset 70058h

Display FIFO Drain Latency 3

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70058h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**DISPLAY_CURSOR_C_DRAIN_LATENCY_PRECISION_SELECT:** 1 use 32 as precision multiplier to increase precision to be stored in 7-bit Cursor B drain latency value 0 use 16 as precision multiplier to increase precision to be stored in 7-bit Cursor B drain latency value
30:24	0x0 RW	**CURSOR_C_DRAIN_LATENCY_VALUE:** For cursor latency, 4 BPP is assumed for all cursor formats
23	0x0 RW	**DISPLAY_SPRITE_F_DRAIN_LATENCY_PRECISION_SELECT:** 1 use 32 as precision multiplier to increase precision to be stored in 7-bit Sprite D drain latency value 0 use 16 as precision multiplier to increase precision to be stored in 7-bit Sprite D drain latency value
22:16	0x0 RW	**SPRITE_F_DRAIN_LATENCY_VALUE:**
15	0x0 RW	**DISPLAY_SPRITE_E_DRAIN_LATENCY_PRECISION_SELECT:** 1 use 32 as precision multiplier to increase precision to be stored in 7-bit Sprite C drain latency value 0 use 16 as precision multiplier to increase precision to be stored in 7-bit Sprite C drain latency value
14:8	0x0 RW	**SPRITE_E_DRAIN_LATENCY_VALUE:**

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW	**DISPLAY_PLANE_C_DRAIN_LATENCY_PRECISION_SELECT:** 1 use 32 as precision multiplier to increase precision to be stored in 7-bit Plane B drain latency value 0 use 16 as precision multiplier to increase precision to be stored in 7-bit Plane B drain latency value
6:0	0x0 RW	**DISPLAY_PLANE_C_DRAIN_LATENCY_VALUE:**

4.3.185 DSPARB2—Offset 70060h

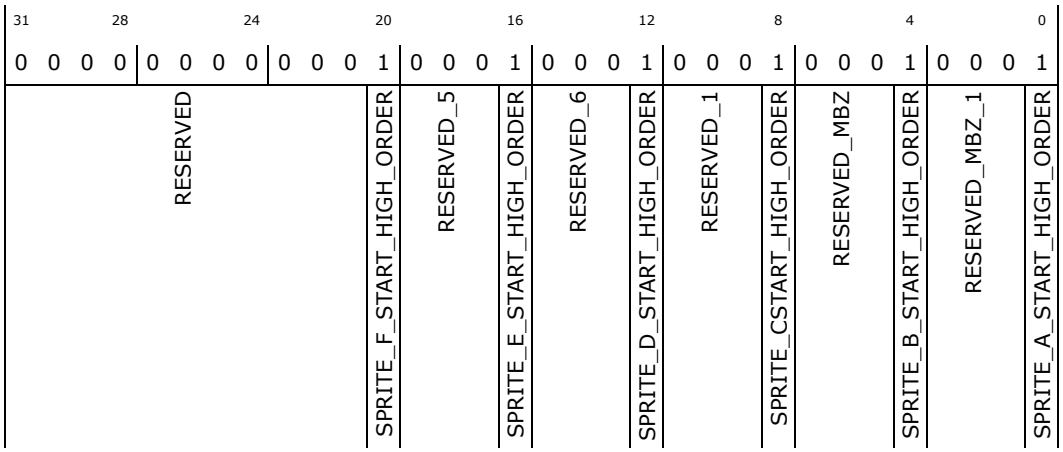
Display Arbitration Control 2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70060h

Default: 00111111h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RO	**RESERVED:** Reserved.
20	0x1 RW	**SPRITE_F_START_HIGH_ORDER:** This field is the high order bits for Sprite D Start pointer. Combined with lower order 8-bit Sprite D Start pointer, this field selects the end of the ram used for Sprite C and the start of the RAM for Sprite D. If sprite C is unused, this field can be set to the same value as Sprite C START. If Sprite D is unused, this field can be set to TOTALSIZE-1. It must be programmed to a number greater than or equal to the value in Sprite C START and less than the total size of the RAM (TOTALSIZE). The size of the Sprite C FIFO will be (Sprite D START-Sprite C START)*64. The size of the Sprite D FIFO will be (TOTALSIZE-Sprite D START-1) *64 bytes. [DevBLC and DevCTG]: Reserved: Write as zero.

Bit Range	Default & Access	Field Name (ID): Description
19:17	0x0 RO	**RESERVED_5:** Reserved.
16	0x1 RW	**SPRITE_E_START_HIGH_ORDER:** This field is the high order bits for Sprite D Start pointer. Combined with lower order 8-bit Sprite D Start pointer, this field selects the end of the ram used for Sprite C and the start of the RAM for Sprite D. If sprite C is unused, this field can be set to the same value as Sprite C START. If Sprite D is unused, this field can be set to TOTALSIZE-1. It must be programmed to a number greater than or equal to the value in Sprite C START and less than the total size of the RAM (TOTALSIZE). The size of the Sprite C FIFO will be (Sprite D START-Sprite C START)*64. The size of the Sprite D FIFO will be (TOTALSIZE-Sprite D START-1) *64 bytes. [DevBLC and DevCTG]: Reserved: Write as zero.
15:13	0x0 RO	**RESERVED_6:** Reserved.
12	0x1 RW	**SPRITE_D_START_HIGH_ORDER:** This field is the high order bits for Sprite D Start pointer. Combined with lower order 8-bit Sprite D Start pointer, this field selects the end of the ram used for Sprite C and the start of the RAM for Sprite D. If sprite C is unused, this field can be set to the same value as Sprite C START. If Sprite D is unused, this field can be set to TOTALSIZE-1. It must be programmed to a number greater than or equal to the value in Sprite C START and less than the total size of the RAM (TOTALSIZE). The size of the Sprite C FIFO will be (Sprite D START-Sprite C START)*64. The size of the Sprite D FIFO will be (TOTALSIZE-Sprite D START-1) *64 bytes. [DevBLC and DevCTG]: Reserved: Write as zero.
11:9	0x0 RO	**RESERVED_1:** Reserved.
8	0x1 RW	**SPRITE_CSTART_HIGH_ORDER:** This field is the high order bits for Sprite C Start pointer. Combined with lower order 8-bit Sprite C Start pointer, this field selects the end of the ram used for display B and the start of the RAM for Sprite C. If display B is unused, this field can be set to zero. The value should never exceed the size of the RAM (TOTALSIZE). The size of the display B FIFO will be (Sprite C START)*64 bytes.
7:5	0x0 RO	**RESERVED_MBZ:** Reserved.
4	0x1 RW	**SPRITE_B_START_HIGH_ORDER:** This field is the high order bits for Sprite B Start pointer. Combined with lower order 8-bit Sprite B Start pointer, this field selects the end of the ram used for Sprite A and the start of the RAM for Sprite B. If sprite A is unused, this field can be set to the same value as Sprite A START. If Sprite B is unused, this field can be set to TOTALSIZE-1. It must be programmed to a number greater than or equal to the value in Sprite A START and less than the total size of the RAM (TOTALSIZE). The size of the Sprite A FIFO will be (Sprite B START-Sprite A START)*64. The size of the Sprite B FIFO will be (TOTALSIZE-Sprite B START-1) *64 bytes. [DevBLC and DevCTG]: Reserved: Write as zero.
3:1	0x0 RO	**RESERVED_MBZ_1:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**SPRITE_A_START_HIGH_ORDER:** This field is the high order bits for Sprite A Start pointer. Combined with lower order 8-bit Sprite A Start pointer, this field selects the end of the ram used for display A and the start of the RAM for Sprite A. If display A is unused, this field can be set to zero. The value should never exceed the size of the RAM (TOTALSIZE). The size of the display A FIFO will be (Sprite A START)*64 bytes.

4.3.186 DSPHOWM—Offset 70064h

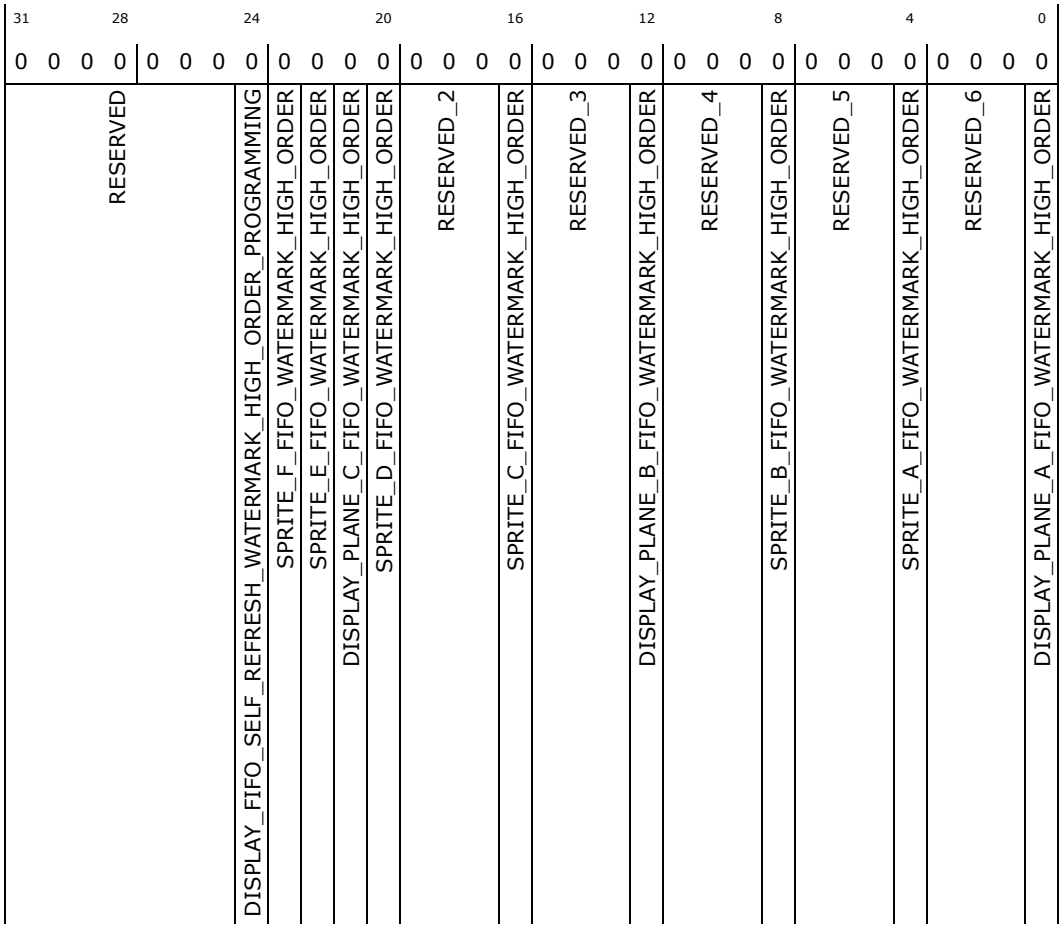
Display FIFO WM High Order

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70064h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RESERVED:** Reserved.
24	0x0 RW	**DISPLAY_FIFO_SELF_REFRESH_WATERMARK_HIGH_ORDER_PROGRAMMING:** This field is the high order bit for the SR WM pointer . Combined with the lower order 9-bit SR FIFO WM pointer, it forms a 10-bit SR FIFO WM pointer. This register defines the value of the watermark used by the Display streamer in case the CPU is in C2/C3/C4 and the memory has entered self refresh. Number in 64Bs of space in FIFO above which the Display Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).Note: When calculating watermark values for 15/16bpp display formats, assume 32bpp for purposes of calculation using the high priority bandwidth analysis spreadsheet.
23	0x0 RW	**SPRITE_F_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Sprite D FIFO WM. Combined with lower order 8-bit Sprite D FIFO WM, it forms a 9-bit Sprite D FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
22	0x0 RW	**SPRITE_E_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Sprite D FIFO WM. Combined with lower order 8-bit Sprite D FIFO WM, it forms a 9-bit Sprite D FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
21	0x0 RW	**DISPLAY_PLANE_C_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Display B FIFO WM. Combined with lower order 8-bit Display B FIFO WM, it forms a 9-bit Display B FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
20	0x0 RW	**SPRITE_D_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Sprite D FIFO WM. Combined with lower order 8-bit Sprite D FIFO WM, it forms a 9-bit Sprite D FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
19:17	0x0 RO	**RESERVED_2:** Reserved.
16	0x0 RW	**SPRITE_C_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Sprite C FIFO WM. Combined with lower order 8-bit Sprite C FIFO WM, it forms a 9-bit Sprite C FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
15:13	0x0 RO	**RESERVED_3:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
12	0x0 RW	**DISPLAY_PLANE_B_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Display B FIFO WM. Combined with lower order 8-bit Display B FIFO WM, it forms a 9-bit Display B FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
11:9	0x0 RO	**RESERVED_4:** Reserved.
8	0x0 RW	**SPRITE_B_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Sprite B FIFO WM. Combined with lower order 8-bit Sprite B FIFO WM, it forms a 9-bit Sprite B FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
7:5	0x0 RO	**RESERVED_5:** MBZ
4	0x0 RW	**SPRITE_A_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Sprite A FIFO WM. Combined with lower order 8-bit Sprite A FIFO WM, it forms a 9-bit Sprite A FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
3:1	0x0 RO	**RESERVED_6:** MBZ
0	0x0 RW	**DISPLAY_PLANE_A_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Display A FIFO WM. Combined with lower order 8-bit Display A FIFO WM, it forms a 9-bit Display A FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

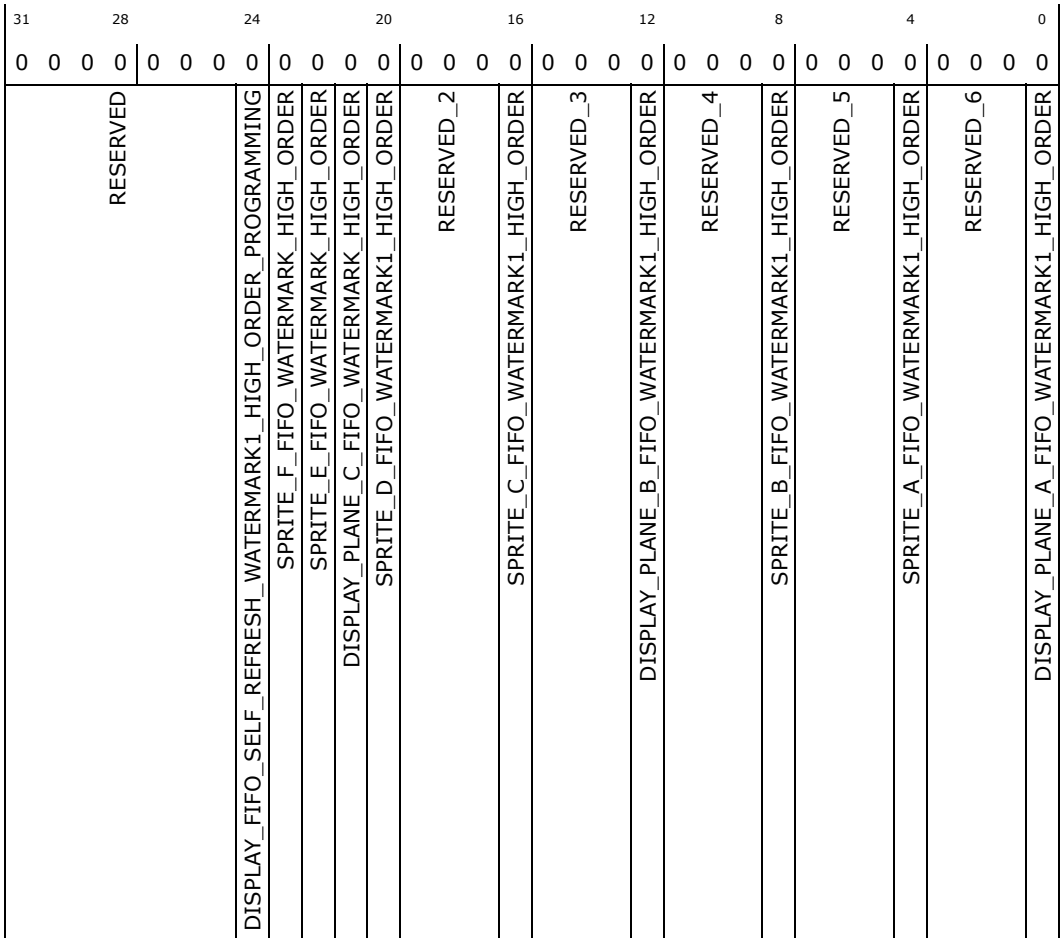
4.3.187 DSPHOWM1—Offset 70068h

Display FIFO WM1 High Order

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70068h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RESERVED:** Reserved.
24	0x0 RW	**DISPLAY_FIFO_SELF_REFRESH_WATERMARK1_HIGH_ORDER_PROGRAMMING:** This field is the high order bit for the SR WM1 pointer . Combined with the lower order 9-bit SR FIFO WM1 pointer, it forms a 10-bit SR FIFO WM1 pointer. This register defines the value of the watermark used by the Display streamer in case the CPU is in C2/C3/C4 and the memory has entered self refresh. Number in 64Bs of space in FIFO above which the Display Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).Note: When calculating watermark values for 15/16bpp display formats, assume 32bpp for purposes of calculation using the high priority bandwidth analysis spreadsheet.

Bit Range	Default & Access	Field Name (ID): Description
23	0x0 RW	**SPRITE_F_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Sprite D FIFO WM. Combined with lower order 8-bit Sprite D FIFO WM, it forms a 9-bit Sprite D FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
22	0x0 RW	**SPRITE_E_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Sprite D FIFO WM. Combined with lower order 8-bit Sprite D FIFO WM, it forms a 9-bit Sprite D FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
21	0x0 RW	**DISPLAY_PLANE_C_FIFO_WATERMARK_HIGH_ORDER:** This field is the high order bit for Display B FIFO WM. Combined with lower order 8-bit Display B FIFO WM, it forms a 9-bit Display B FIFO WM pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
20	0x0 RW	**SPRITE_D_FIFO_WATERMARK1_HIGH_ORDER:** This field is the high order bit for Sprite D FIFO WM1. Combined with lower order 8-bit Sprite D FIFO WM1, it forms a 9-bit Sprite D FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
19:17	0x0 RO	**RESERVED_2:** Reserved.
16	0x0 RW	**SPRITE_C_FIFO_WATERMARK1_HIGH_ORDER:** This field is the high order bit for Sprite C FIFO WM1. Combined with lower order 8-bit Sprite C FIFO WM1, it forms a 9-bit Sprite C FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
15:13	0x0 RO	**RESERVED_3:** Reserved.
12	0x0 RW	**DISPLAY_PLANE_B_FIFO_WATERMARK1_HIGH_ORDER:** This field is the high order bit for Display B FIFO WM1. Combined with lower order 8-bit Display B FIFO WM1, it forms a 9-bit Display B FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
11:9	0x0 RO	**RESERVED_4:** Reserved.
8	0x0 RW	**SPRITE_B_FIFO_WATERMARK1_HIGH_ORDER:** This field is the high order bit for Sprite B FIFO WM1. Combined with lower order 8-bit Sprite B FIFO WM1, it forms a 9-bit Sprite B FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
7:5	0x0 RO	**RESERVED_5:** MBZ

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**SPRITE_A_FIFO_WATERMARK1_HIGH_ORDER:** This field is the high order bit for Sprite A FIFO WM1. Combined with lower order 8-bit Sprite A FIFO WM1, it forms a 9-bit Sprite A FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
3:1	0x0 RO	**RESERVED_6:** MBZ
0	0x0 RW	**DISPLAY_PLANE_A_FIFO_WATERMARK1_HIGH_ORDER:** This field is the high order bit for Display A FIFO WM1. Combined with lower order 8-bit Display A FIFO WM1, it forms a 9-bit Display A FIFO WM1 pointer. Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

4.3.188 FW4—Offset 70070h

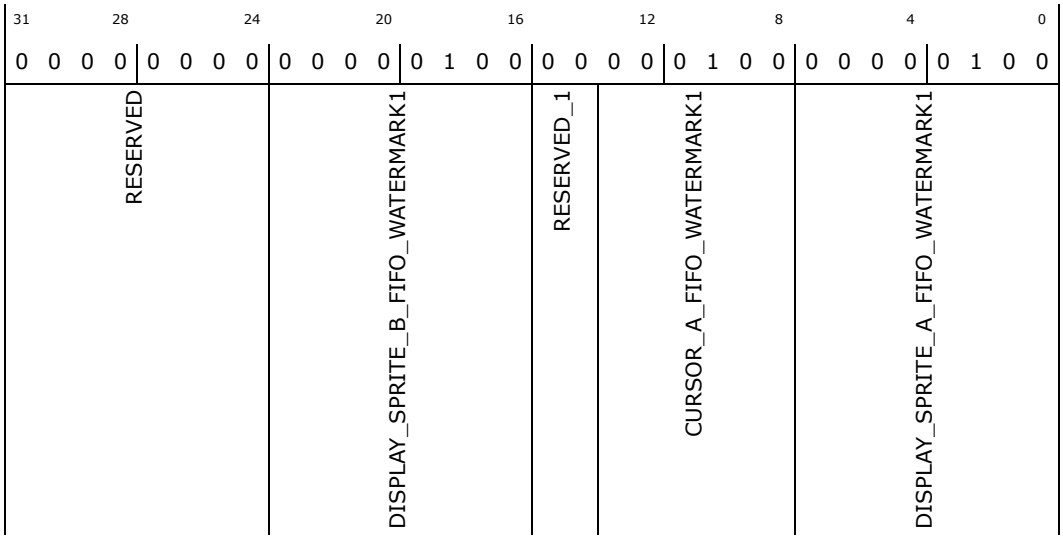
Display FIFO Watermark1 Control 4

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70070h

Default: 00040404h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** MBZ

Bit Range	Default & Access	Field Name (ID): Description
23:16	0x4 RW	**DISPLAY_SPRITE_B_FIFO_WATERMARK1:** Number in 64Bs of space in FIFO above which the Display Sprite B Stream will generate request with status 2
15:14	0x0 RO	**RESERVED_1:** MBZ
13:8	0x4 RW	**CURSOR_A_FIFO_WATERMARK1:** Number in 64Bs of space in the Cursor A FIFO above which the Cursor A Stream will generate requests with status 2 to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
7:0	0x4 RW	**DISPLAY_SPRITE_A_FIFO_WATERMARK1:** Number in 64Bs of space in FIFO above which the Display Sprite A Stream will generate request with status 2 (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

4.3.189 FW5—Offset 70074h

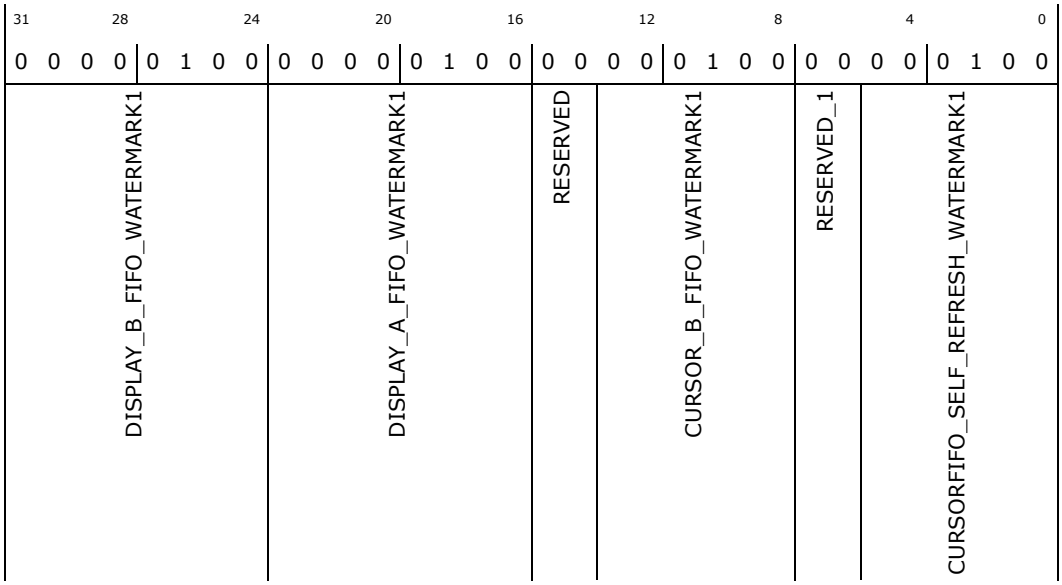
Display FIFO Watermark1 Control 5

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70074h

Default: 04040404h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x4 RW	**DISPLAY_B_FIFO_WATERMARK1:** Number in 64Bs of space in FIFO above which the Display B Stream will generate request with status 2

Bit Range	Default & Access	Field Name (ID): Description
23:16	0x4 RW	**DISPLAY_A_FIFO_WATERMARK1:** Number in 64Bs of space in FIFO above which the Display A Stream will generate request with status 2
15:14	0x0 RO	**RESERVED:** MBZ
13:8	0x4 RW	**CURSOR_B_FIFO_WATERMARK1:** Number in 64Bs of space in the Cursor B FIFO above which the Cursor B Stream will generate requests with status 2 to Memory (Value should be as recommended in the high priority bandwidth analysis spreadsheet).
7:6	0x0 RO	**RESERVED_1:** MBZ
5:0	0x4 RW	**CURSORFIFO_SELF_REFRESH_WATERMARK1:** Number in 64Bs of space in FIFO above which the Display Cursor Stream will generate request with status 2 during memory SR (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

4.3.190 FW6—Offset 70078h

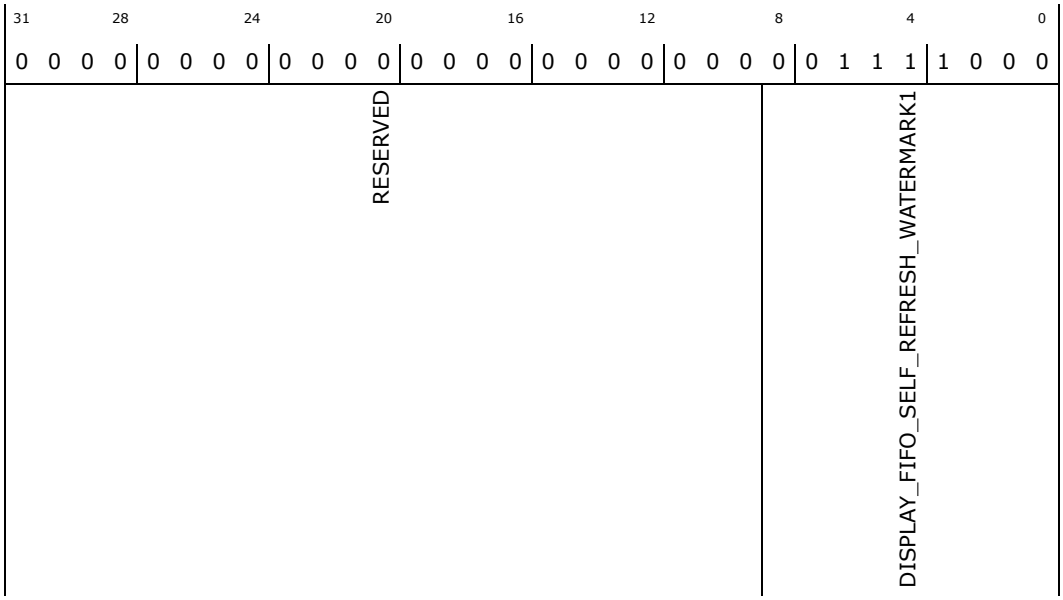
Display FIFO Watermark1 Control 6

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70078h

Default: 00000078h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**RESERVED:** MBZ
8:0	0x78 RW	**DISPLAY_FIFO_SELF_REFRESH_WATERMARK1:** Number in 64Bs of space in FIFO above which the Display A/B Streamer will generate request with status 2 during max fifo mode (Value should be as recommended in the high priority bandwidth analysis spreadsheet).

4.3.191 FW9—Offset 7007Ch

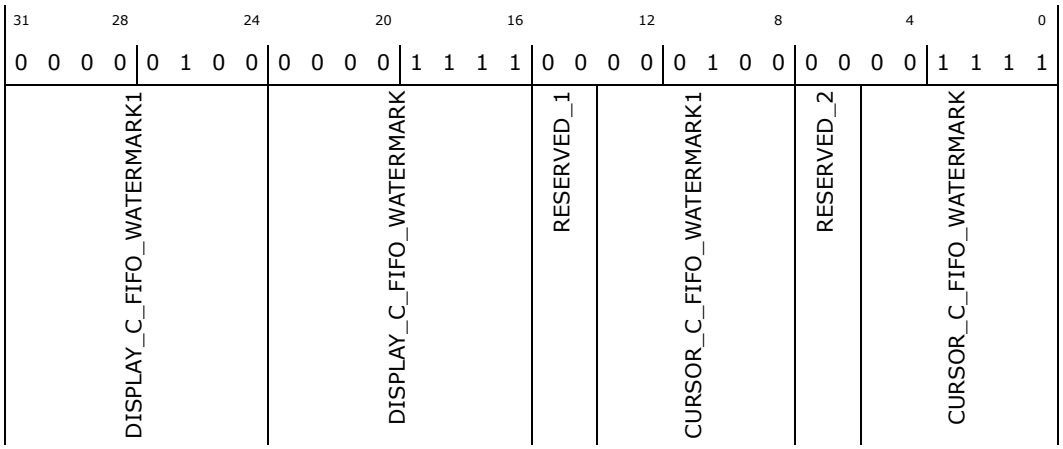
Display FIFO Watermark Control 9

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 7007Ch

Default: 040F040Fh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x4 RW	**DISPLAY_C_FIFO_WATERMARK1:** Number in 64Bs of space in FIFO above which the Display Sprite C Stream will generate request with status 2
23:16	0xf RW	**DISPLAY_C_FIFO_WATERMARK:** Number in 64Bs of space in FIFO above which the Display Sprite C Stream will generate request with status 2
15:14	0x0 RO	**RESERVED_1:** MBZ
13:8	0x4 RW	**CURSOR_C_FIFO_WATERMARK1:** Number in 64Bs of space in FIFO above which the Display CURSOR C Stream will generate request with status 2
7:6	0x0 RO	**RESERVED_2:** MBZ
5:0	0xf RW	**CURSOR_C_FIFO_WATERMARK:** Number in 64Bs of space in FIFO above which the Display CURSOR C Stream will generate request with status 2

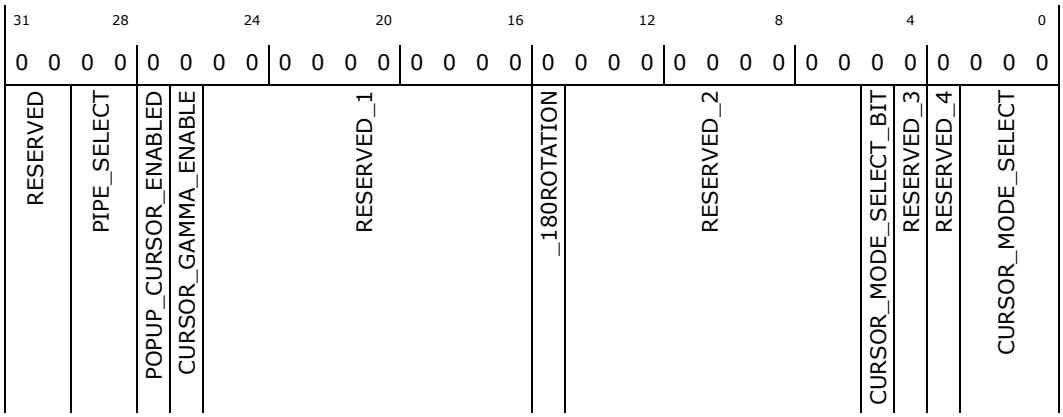
4.3.192 CURACNTR—Offset 70080h

Cursor A Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70080h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RESERVED:** Write as zero.
29:28	0x0 RW	**PIPE_SELECT:**] A state machine handles the synchronization of the switch to both vertical blank signals. So as far as the software is concerned, when both display pipes are being used, it can be switched at any time; the hardware will synchronize the switch. 00 = HW cursor is attached to Display Pipe A. This is the default after reset. 01 = HW cursor is attached to Display Pipe B. 10 = Reserved for pipe C 11 = Reserved for pipe D [DevBLC] and [DevCTG] Reserved: Write as zero.
27	0x0 RW	**POPUP_CURSOR_ENABLED:** . This bit should be turned on when using Cursor A as a popup cursor. When in popup mode, hardware interprets the cursor base address as a physical address instead of a graphics address.0 = Cursor A is hi-res 1 = Cursor A is popup
26	0x0 RW	**CURSOR_GAMMA_ENABLE:** This bit only has an effect when using the cursor in display mode. 0 = Cursor pixel data bypasses gamma correction or palette (default). 1 = Cursor pixel data is gamma to be corrected in the pipe.
25:16	0x0 RO	**RESERVED_1:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**_180ROTATION:** This mode causes the cursor to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image. Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel. 0 = No rotation 1 = 180 Rotation of 32 bit per pixel cursors
14:6	0x0 RO	**RESERVED_2:** Reserved.
5	0x0 RW	**CURSOR_MODE_SELECT_BIT:** Refer following table.
4	0x0 RO	**RESERVED_3:** Reserved.
3	0x0 RO	**RESERVED_4:** Reserved.
2:0	0x0 RW	**CURSOR_MODE_SELECT:** These three bits together with bit 5 select the mode for cursor as shown in the following table.

4.3.193 CURABASE—Offset 70084h

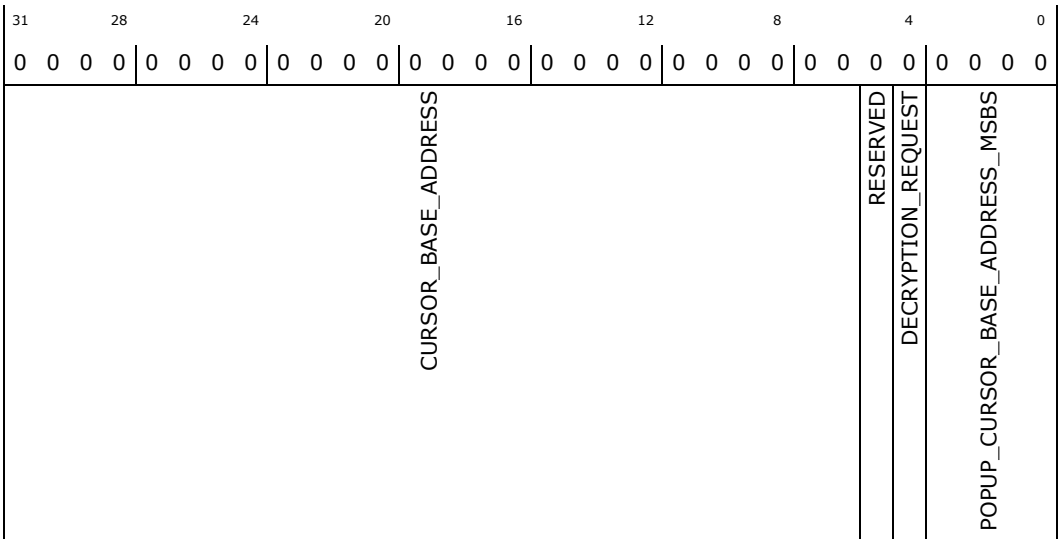
Cursor A Base Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70084h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**CURSOR_BASE_ADDRESS:** . This field specifies bits 31:6 of the graphics address of the base of the cursor. On [DevBW] and [DevCL] if the cursor is a popup, this field specifies bits 31:6 of the physical address of the base of the cursor, and bits 35:32 of the address are specified in the LSBs of this register. Popup cursor mode is selected within the CURACNTR register.The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the cursor data in its unrotated orientation and the cursor surface address. A write to this register also acts as a trigger event to force the update of active registers from the staging registers on the next display event. Each cursor register is double-buffered. The CPU writes to a set of holding registers. The active registers are updated from the holding registers following the leading edge of the vertical blank pulse. The update is postponed until the next vblank if a write cycle is active to any of the cursor registers at the time of the vblank. The update is also postponed if a write sequence is in progress. It is assumed that if the cursor mode is changed, the cursor image will also be changed. To prevent the cursor from appearing when it is only partially programmed, the active registers will not be updated until both the cursor control and base address registers have been programmed. If the cursor control register is written, the cursor base address must also be written before the change will be effective. However, the base address register may be changed (e.g., to change the shape of the cursor) without also writing to the control register. If both are to be written, the control register must be written first.
5	0x0 RO	**RESERVED:** MBZ
4	0x0 RW	**DECRYPTION_REQUEST:** This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. 0 = Decryption request disabled (default) 1 = Decryption request enabled
3:0	0x0 RW	**POPUP_CURSOR_BASE_ADDRESS_MSBS:** ([DevBW] and [DevCL] Only). This field specifies bits 35:32 of the popup cursor physical address. If popup mode is not selected, this field is ignored.

4.3.194 CURAPOS—Offset 70088h

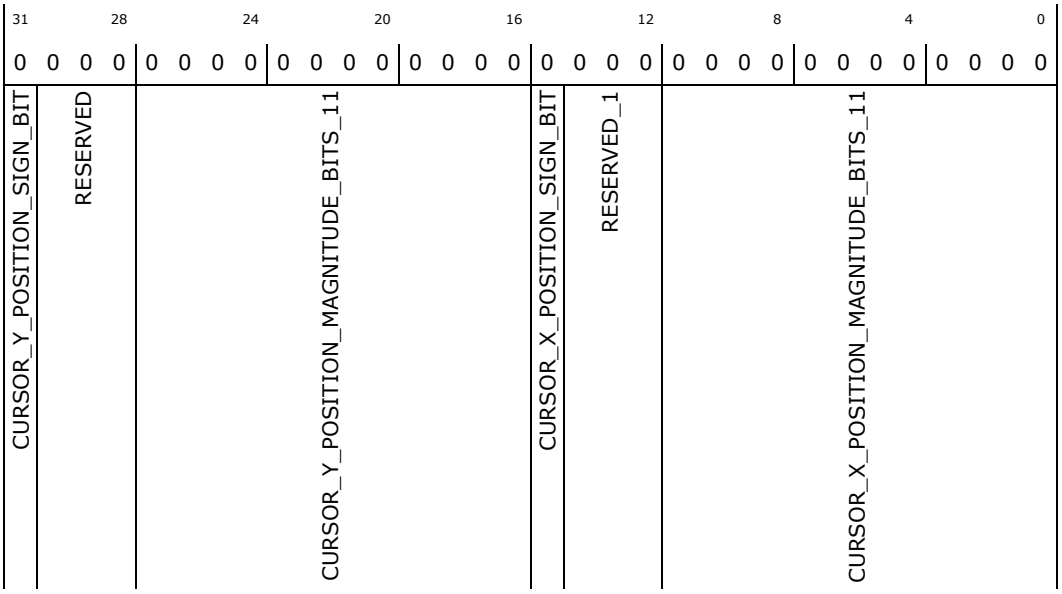
Cursor A Position Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70088h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**CURSOR_Y_POSITION_SIGN_BIT:** This bit provides the sign bit of a signed 13-bit value that specifies the horizontal position of cursor. (default is 0). For normal high resolution display modes, the cursor must have at least a single pixel positioned over the active screen.
30:28	0x0 RO	**RESERVED:** Write as zero.
27:16	0x0 RW	**CURSOR_Y_POSITION_MAGNITUDE_BITS_11:** 0: This register provides the magnitude bits of a signed 12-bit value that specifies the vertical position of cursor. The sign bit of this value is provided by bit 31of this register. (default is 0). For HDMI modes where the vertical zoom is greater than 1x, the position is specified using the zoomed grid. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation.
15	0x0 RW	**CURSOR_X_POSITION_SIGN_BIT:** This bit provides the sign bit of a signed 13-bit value that specifies the horizontal position of cursor. (default is 0).). For normal high resolution display modes, the cursor must have at least a single pixel positioned over the active screen.
14:12	0x0 RO	**RESERVED_1:** Write as zero.
11:0	0x0 RW	**CURSOR_X_POSITION_MAGNITUDE_BITS_11:** 0: These 12 bits provide the signed 13-bit value that specifies the horizontal position of cursor. The sign bit is provided by bit 15 of this register. (default is 0) For HDMI modes where the horizontal zoom is greater than 1x, the position is specified using the zoomed grid. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the end of the active video area in the unrotated orientation.

4.3.195 CURAPALET_0—Offset 70090h

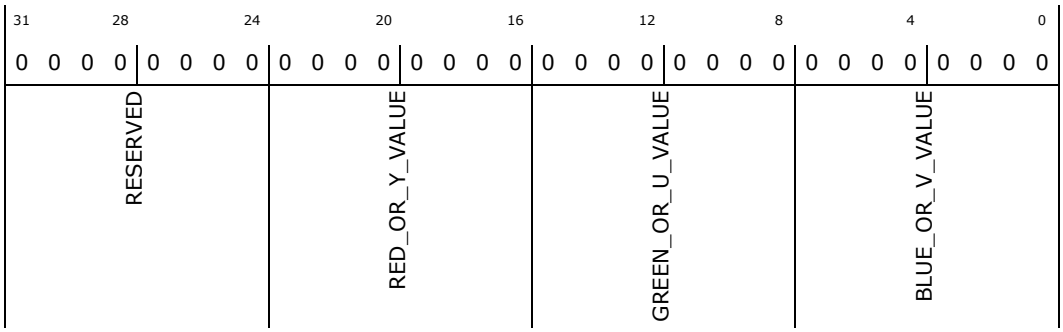
Cursor A Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70090h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero.
23:16	0x0 RW	**RED_OR_Y_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0x0 RW	**GREEN_OR_U_VALUE:**
7:0	0x0 RW	**BLUE_OR_V_VALUE:**

4.3.196 CURAPALET_1—Offset 70094h

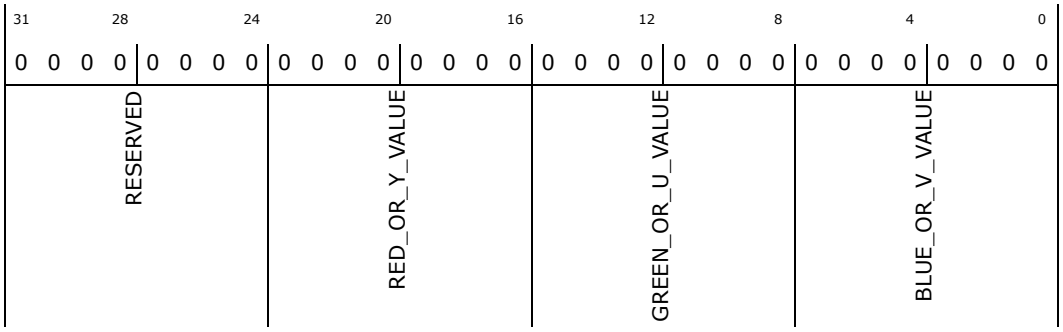
Cursor A Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70094h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero.
23:16	0x0 RW	**RED_OR_Y_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0x0 RW	**GREEN_OR_U_VALUE:**
7:0	0x0 RW	**BLUE_OR_V_VALUE:**

4.3.197 CURAPALET_2—Offset 70098h

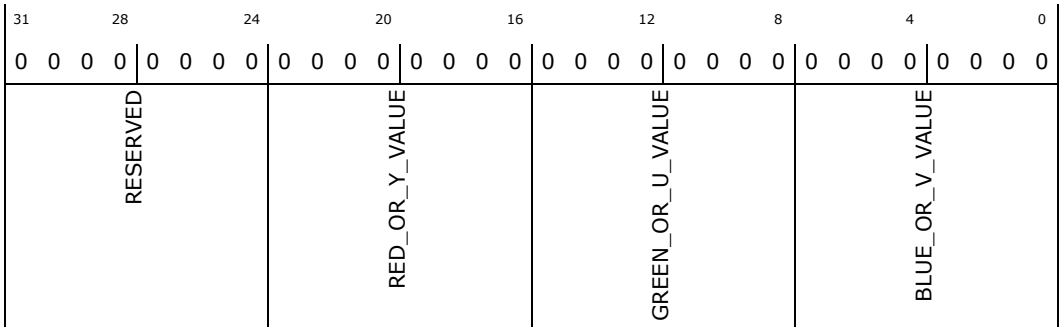
Cursor A Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70098h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0x0 RW	**RED_OR_Y_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0x0 RW	**GREEN_OR_U_VALUE:**
7:0	0x0 RW	**BLUE_OR_V_VALUE:**

4.3.198 CURAPALET_3—Offset 7009Ch

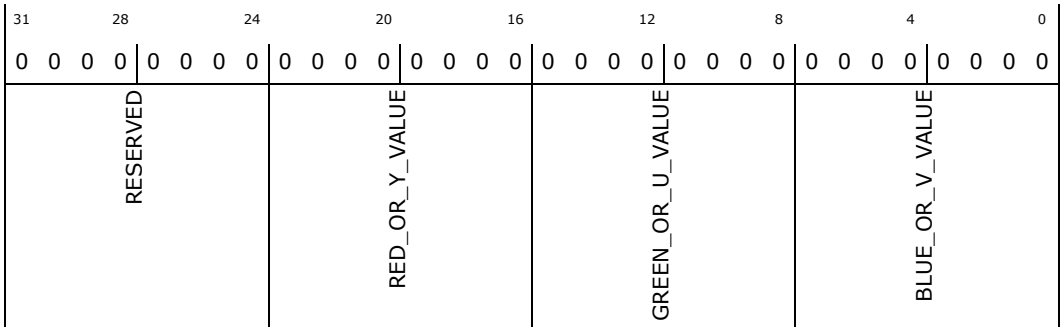
Cursor A Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 7009Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero.
23:16	0x0 RW	**RED_OR_Y_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre-gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	0x0 RW	**GREEN_OR_U_VALUE:**
7:0	0x0 RW	**BLUE_OR_V_VALUE:**

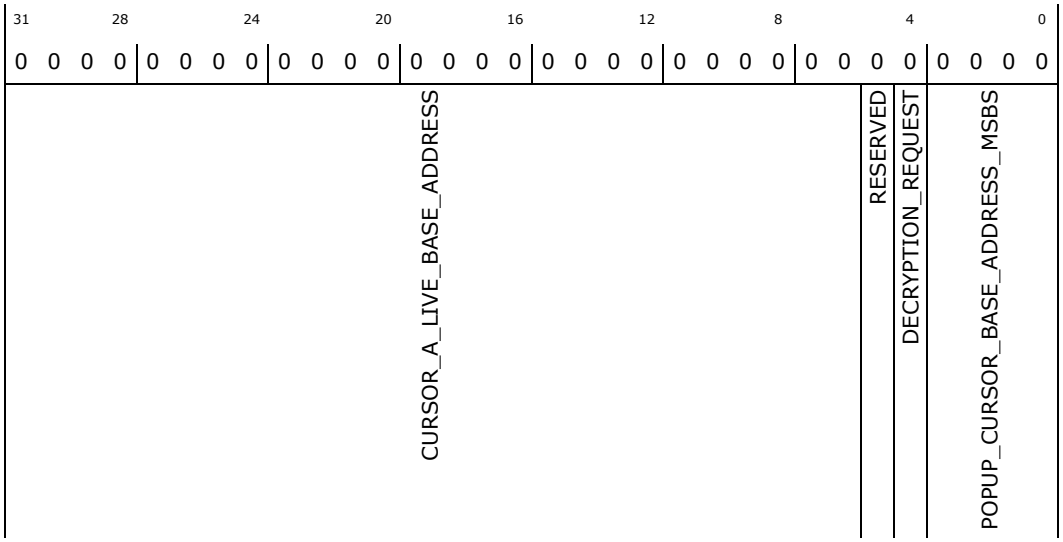
4.3.199 CURALIVEBASE—Offset 700ACh

Cursor A Live Base Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 700ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**CURSOR_A_LIVE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for the plane.
5	0x0 RO	**RESERVED:** MBZ
4	0x0 RO	**DECRYPTION_REQUEST:** This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. 0 = Decryption request disabled (default) 1 = Decryption request enabled
3:0	0x0 RO	**POPUP_CURSOR_BASE_ADDRESS_MSBS:** ([DevBW] and [DevCL] Only). This field specifies bits 35:32 of the popup cursor physical address. If popup mode is not selected, this field is ignored.

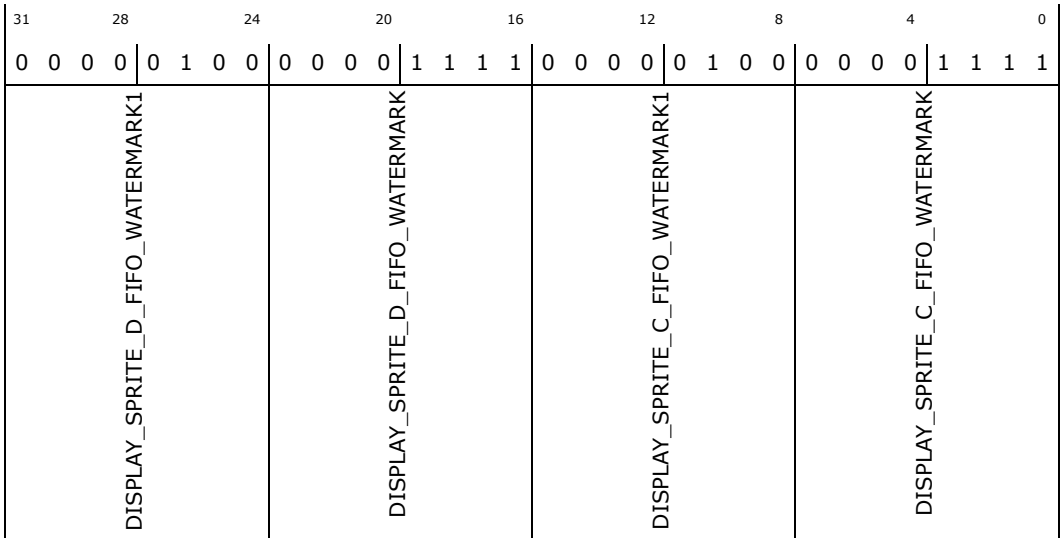
4.3.200 FW7—Offset 700B4h

Display FIFO Watermark Control 7

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 700B4h

Default: 040F040Fh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x4 RW	**DISPLAY_SPRITE_D_FIFO_WATERMARK1:** Number in 64Bs of space in FIFO above which the Display Sprite D Stream will generate request with status 2
23:16	0xf RW	**DISPLAY_SPRITE_D_FIFO_WATERMARK:** Number in 64Bs of space in FIFO above which the Display Sprite D Stream will generate request with status 2
15:8	0x4 RW	**DISPLAY_SPRITE_C_FIFO_WATERMARK1:** Number in 64Bs of space in FIFO above which the Display Sprite C Stream will generate request with status 2
7:0	0xf RW	**DISPLAY_SPRITE_C_FIFO_WATERMARK:** Number in 64Bs of space in FIFO above which the Display Sprite C Stream will generate request with status 2

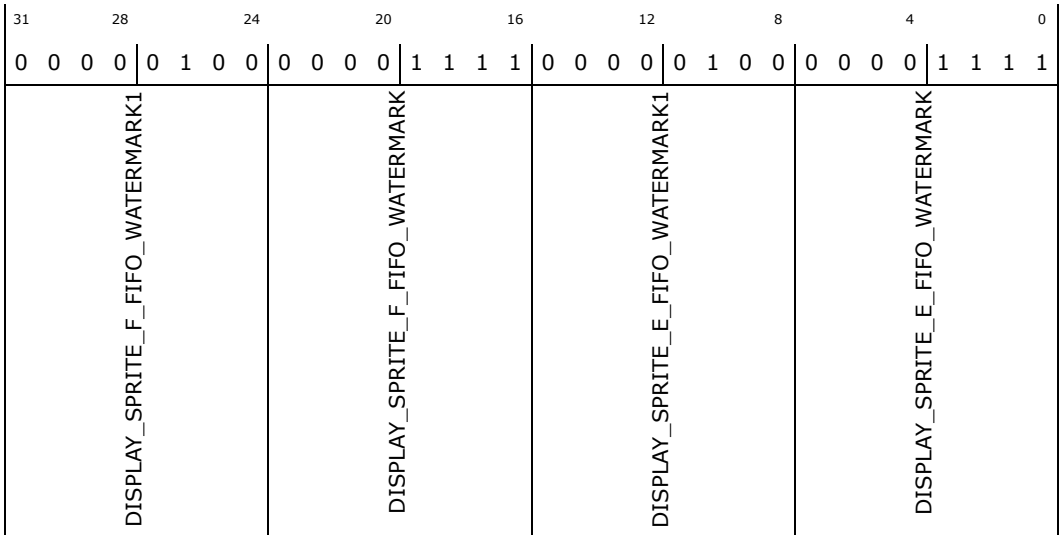
4.3.201 FW8—Offset 700B8h

Display FIFO Watermark Control 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 700B8h

Default: 040F040Fh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x4 RW	**DISPLAY_SPRITE_F_FIFO_WATERMARK1:** Number in 64Bs of space in FIFO above which the Display Sprite F Stream will generate request with status 2
23:16	0xf RW	**DISPLAY_SPRITE_F_FIFO_WATERMARK:** Number in 64Bs of space in FIFO above which the Display Sprite F Stream will generate request with status 2
15:8	0x4 RW	**DISPLAY_SPRITE_E_FIFO_WATERMARK1:** Number in 64Bs of space in FIFO above which the Display Sprite E Stream will generate request with status 2
7:0	0xf RW	**DISPLAY_SPRITE_E_FIFO_WATERMARK:** Number in 64Bs of space in FIFO above which the Display Sprite E Stream will generate request with status 2

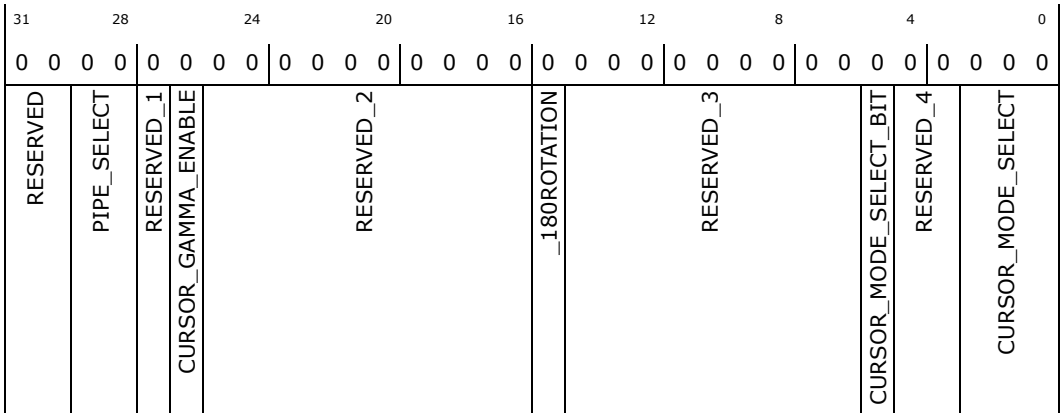
4.3.202 CURBCNTR—Offset 700C0h

Cursor B Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 700C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RESERVED:** Write as zero.
29:28	0x0 RW	**PIPE_SELECT:** A state machine handles the synchronization of the switch to both vertical blank signals. So as far as the software is concerned, when both display pipes are being used, it can be switched at any time; the hardware will synchronize the switch. 00 = HW cursor is attached to Display Pipe A. This is the default after reset. 01 = HW cursor is attached to Display Pipe B. 10 = Reserved for to Display Pipe C. 11 = Reserved for to Display Pipe D. Reserved [DevBLC] and [DevCTG]: Write as zero.
27	0x0 RO	**RESERVED_1:** Write as zero.
26	0x0 RW	**CURSOR_GAMMA_ENABLE:** 0 = Cursor pixel data bypasses gamma correction (default). 1 = Cursor pixel data is gamma to be corrected.
25:16	0x0 RO	**RESERVED_2:** Reserved.
15	0x0 RW	**_180ROTATION:** This mode causes the cursor to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image. Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel. 0 = No rotation 1 = 180 Rotation of 32 bit per pixel cursors
14:6	0x0 RO	**RESERVED_3:** Write as zero
5	0x0 RW	**CURSOR_MODE_SELECT_BIT:** Refer following table.
4:3	0x0 RO	**RESERVED_4:**
2:0	0x0 RW	**CURSOR_MODE_SELECT:** These three bits together with bit 5 select the mode for cursor as shown in the following table.

4.3.203 CURBBASE—Offset 700C4h

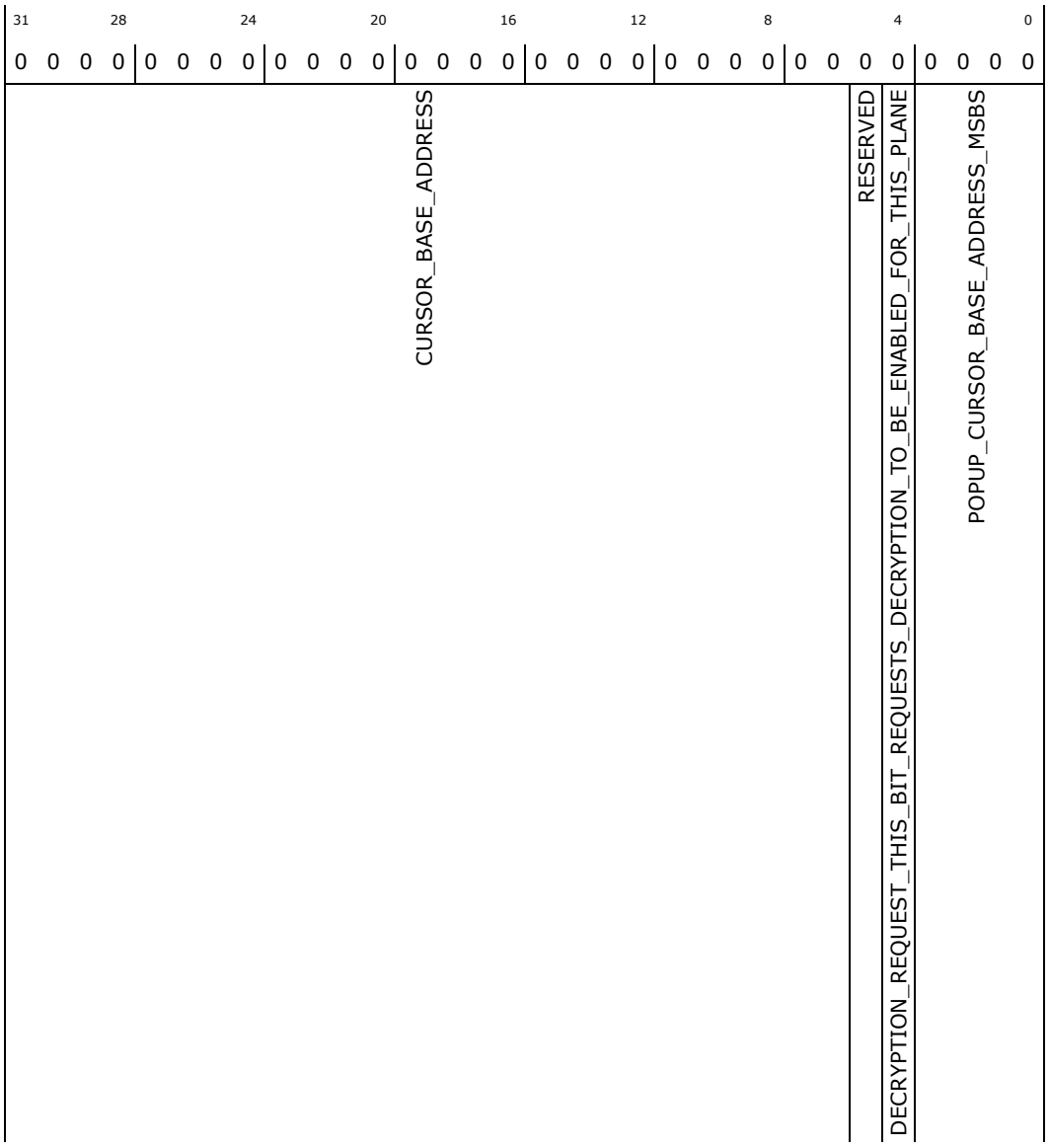
Cursor B Base Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 700C4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**CURSOR_BASE_ADDRESS:** This register specifies the graphics address of the entire cursor. It also acts as a trigger event to force the update of active registers on the next display event. The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the cursor data in its unrotated orientation and the cursor surface address. A write to this register also acts as a trigger event to force the update of active registers from the staging registers on the next display event. Each cursor register is double-buffered. The CPU writes to a set of holding registers. The active registers are updated from the holding registers following the leading edge of the vertical blank pulse. The update is postponed until the next vblank if a write cycle is active to any of the cursor registers at the time of the vblank. The update is also postponed if a write sequence is in progress. It is assumed that if the cursor mode is changed, the cursor image will also be changed. To prevent the cursor from appearing when it is only partially programmed, the active registers will not be updated until both the cursor control and base address registers have been programmed. If the cursor control register is written, the cursor base address must also be written before the change will be effective. However, the base address register may be changed (e.g., to change the shape of the cursor) without also writing to the control register. If both are to be written, the control register must be written first.
5	0x0 RO	**RESERVED:** MBZ
4	0x0 RW	**DECRYPTION_REQUEST_THIS_BIT_REQUESTS_DECRYPTION_TO_BE_ENABLED_FOR_THIS_PLANE:** This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. 0 = Decryption request disabled (default) 1 = Decryption request enabled
3:0	0x0 RW	**POPUP_CURSOR_BASE_ADDRESS_MSBS:** ([DevBW] and [DevCL] Only). This field specifies bits 35:32 of the popup cursor physical address. If popup mode is not selected, this field is ignored.

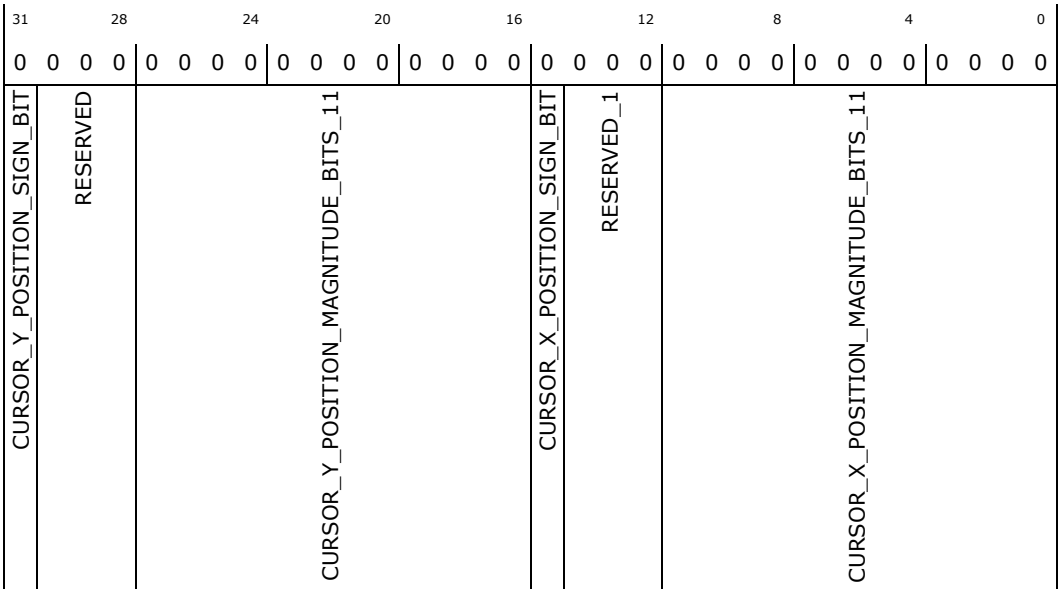
4.3.204 CURBPOS—Offset 700C8h

Cursor B Position Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 700C8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**CURSOR_Y_POSITION_SIGN_BIT:** This bit provides the sign bit of a signed 13-bit value that specifies the horizontal position of cursor. (default is 0).). For normal high resolution display modes, the cursor must have at least a single pixel positioned over the active screen.
30:28	0x0 RO	**RESERVED:** Write as zero.
27:16	0x0 RW	**CURSOR_Y_POSITION_MAGNITUDE_BITS_11:** 0: This register provides the magnitude bits of a signed 13-bit value that specifies the vertical position of cursor. The sign bit of this value is provided by bit 31of this register. (default is 0) When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation.
15	0x0 RW	**CURSOR_X_POSITION_SIGN_BIT:** This bit provides the sign bit of a signed 13-bit value that specifies the horizontal position of cursor. (default is 0).). For normal high resolution display modes, the cursor must have at least a single pixel positioned over the active screen. For HDMI modes where the vertical zoom is greater than 1x, the position is specified using the zoomed grid.
14:12	0x0 RO	**RESERVED_1:** Write as zero.
11:0	0x0 RW	**CURSOR_X_POSITION_MAGNITUDE_BITS_11:** 0: These 12 bits provide the signed 13-bit value that specifies the horizontal position of cursor. The sign bit is provided by bit 15 of this register. (default is 0) For HDMI modes where the horizontal zoom is greater than 1x, the position is specified using the zoomed grid. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation.

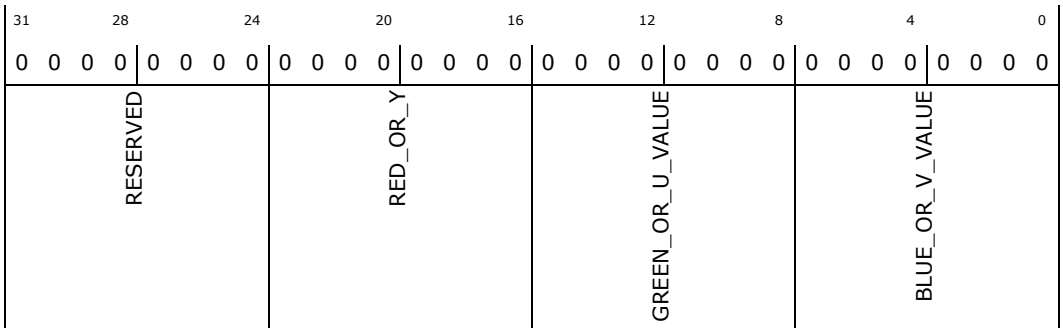
4.3.205 CURBPALET_0—Offset 700D0h

Cursor B Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 700D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero.
23:16	0x0 RW	**RED_OR_Y:**
15:8	0x0 RW	**GREEN_OR_U_VALUE:**
7:0	0x0 RW	**BLUE_OR_V_VALUE:**

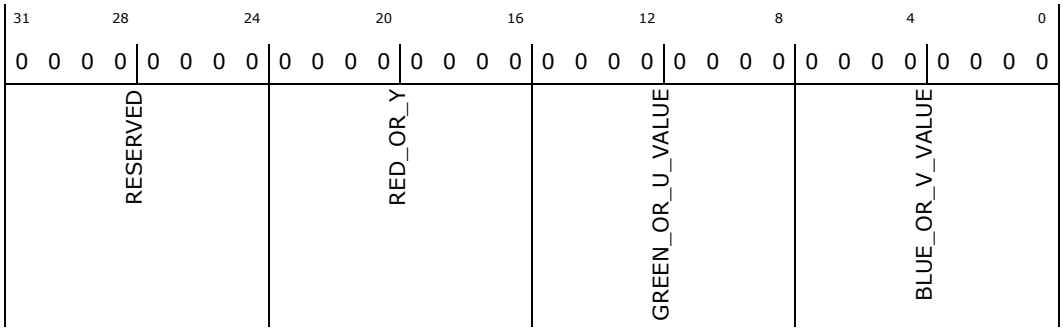
4.3.206 CURBPALET_1—Offset 700D4h

Cursor B Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 700D4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero.
23:16	0x0 RW	**RED_OR_Y:**
15:8	0x0 RW	**GREEN_OR_U_VALUE:**
7:0	0x0 RW	**BLUE_OR_V_VALUE:**

4.3.207 CURBPALET_2—Offset 700D8h

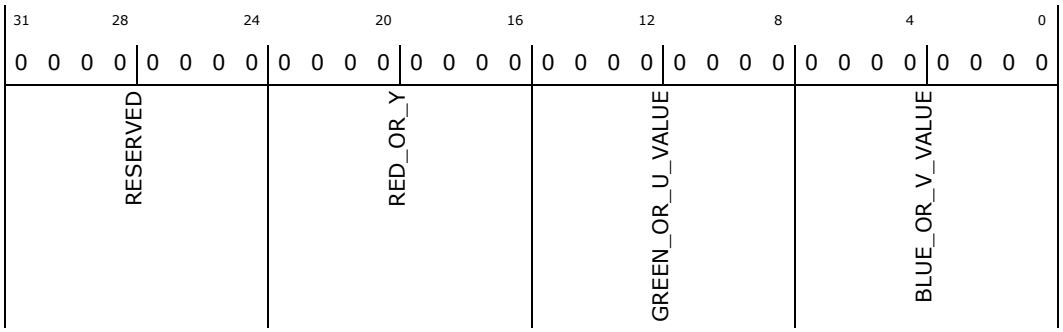
Cursor B Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 700D8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero.
23:16	0x0 RW	**RED_OR_Y:**
15:8	0x0 RW	**GREEN_OR_U_VALUE:**
7:0	0x0 RW	**BLUE_OR_V_VALUE:**

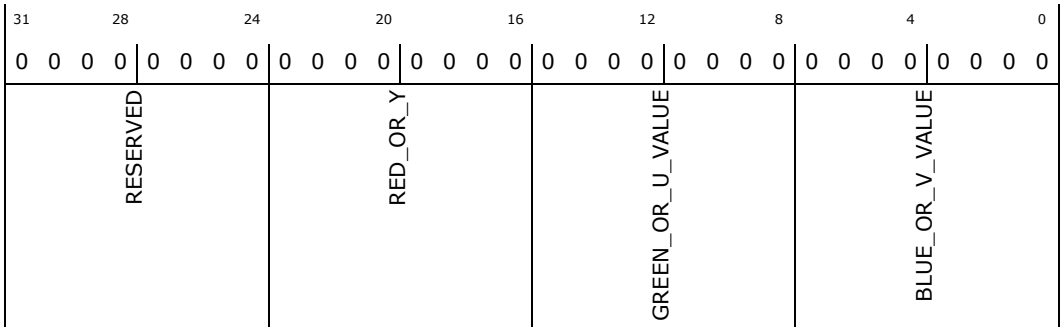
4.3.208 CURBPALET_3—Offset 700DCh

Cursor B Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 700DCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero.
23:16	0x0 RW	**RED_OR_Y:**
15:8	0x0 RW	**GREEN_OR_U_VALUE:**
7:0	0x0 RW	**BLUE_OR_V_VALUE:**

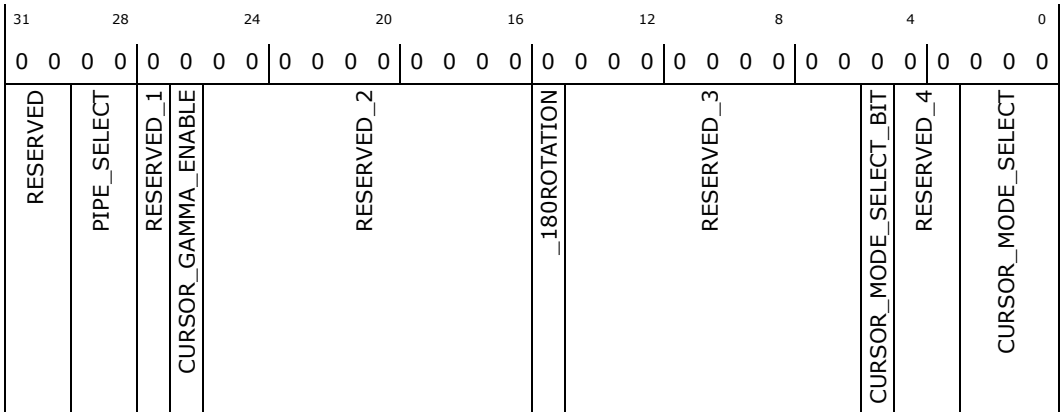
4.3.209 CURCCNTR—Offset 700E0h

Cursor C Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 700E0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RESERVED:** Write as zero.
29:28	0x0 RW	**PIPE_SELECT:** A state machine handles the synchronization of the switch to both vertical blank signals. So as far as the software is concerned, when both display pipes are being used, it can be switched at any time; the hardware will synchronize the switch. 00 = HW cursor is attached to Display Pipe A. This is the default after reset. 01 = HW cursor is attached to Display Pipe B. 10 = Reserved for to Display Pipe C. 11 = Reserved for to Display Pipe D. Reserved [DevBLC] and [DevCTG]: Write as zero.
27	0x0 RO	**RESERVED_1:** Write as zero.
26	0x0 RW	**CURSOR_GAMMA_ENABLE:** 0 = Cursor pixel data bypasses gamma correction (default). 1 = Cursor pixel data is gamma to be corrected.
25:16	0x0 RO	**RESERVED_2:** Reserved.
15	0x0 RW	**_180ROTATION:** This mode causes the cursor to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image. Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel. 0 = No rotation 1 = 180 Rotation of 32 bit per pixel cursors
14:6	0x0 RO	**RESERVED_3:** Write as zero
5	0x0 RW	**CURSOR_MODE_SELECT_BIT:** Refer following table.
4:3	0x0 RO	**RESERVED_4:**
2:0	0x0 RW	**CURSOR_MODE_SELECT:** These three bits together with bit 5 select the mode for cursor as shown in the following table.

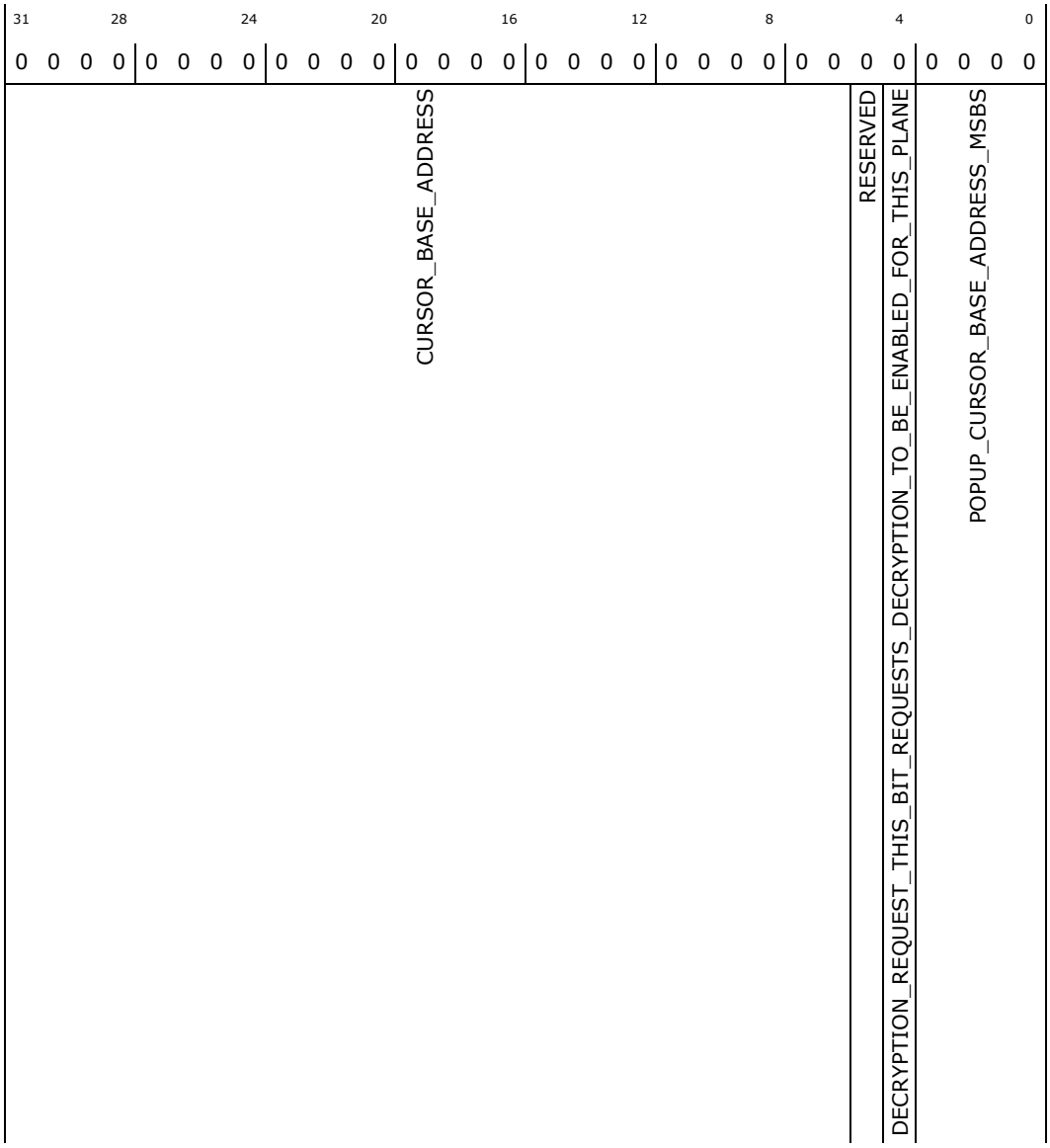
4.3.210 CURCBASE—Offset 700E4h

Cursor C Base Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 700E4h

Default: 00000000h


31 28 24 20 16 12 8 4 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
CURSOR_BASE_ADDRESS
RESERVED
DECRYPTION_REQUEST_THIS_BIT_REQUESTS_DECRYPTION_TO_BE_ENABLED_FOR_THIS_PLANE
POPUP_CURSOR_BASE_ADDRESS_MSBS

Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**CURSOR_BASE_ADDRESS:** This register specifies the graphics address of the entire cursor. It also acts as a trigger event to force the update of active registers on the next display event. The cursor surface address must be 4K byte aligned. The cursor must be in linear memory, it cannot be tiled. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the cursor data in its unrotated orientation and the cursor surface address. A write to this register also acts as a trigger event to force the update of active registers from the staging registers on the next display event. Each cursor register is double-buffered. The CPU writes to a set of holding registers. The active registers are updated from the holding registers following the leading edge of the vertical blank pulse. The update is postponed until the next vblank if a write cycle is active to any of the cursor registers at the time of the vblank. The update is also postponed if a write sequence is in progress. It is assumed that if the cursor mode is changed, the cursor image will also be changed. To prevent the cursor from appearing when it is only partially programmed, the active registers will not be updated until both the cursor control and base address registers have been programmed. If the cursor control register is written, the cursor base address must also be written before the change will be effective. However, the base address register may be changed (e.g., to change the shape of the cursor) without also writing to the control register. If both are to be written, the control register must be written first.
5	0x0 RO	**RESERVED:** MBZ
4	0x0 RW	**DECRYPTION_REQUEST_THIS_BIT_REQUESTS_DECRYPTION_TO_BE_ENABLED_FOR_THIS_PLANE:** This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. 0 = Decryption request disabled (default) 1 = Decryption request enabled
3:0	0x0 RW	**POPUP_CURSOR_BASE_ADDRESS_MSBS:** ([DevBW] and [DevCL] Only). This field specifies bits 35:32 of the popup cursor physical address. If popup mode is not selected, this field is ignored.

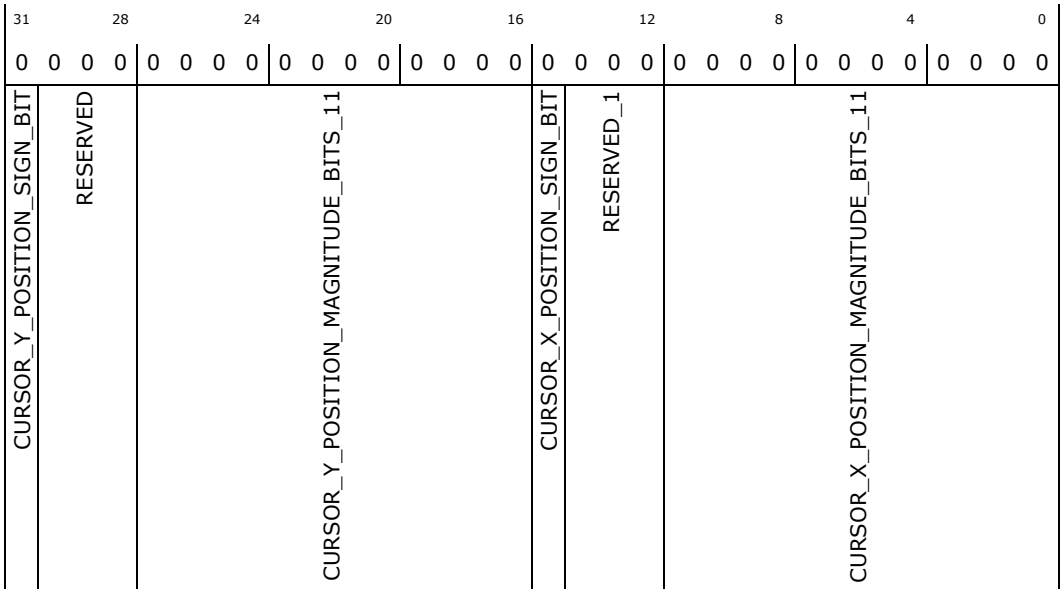
4.3.211 CURCPOS—Offset 700E8h

Cursor C Position Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 700E8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**CURSOR_Y_POSITION_SIGN_BIT:** This bit provides the sign bit of a signed 13-bit value that specifies the horizontal position of cursor. (default is 0).). For normal high resolution display modes, the cursor must have at least a single pixel positioned over the active screen.
30:28	0x0 RO	**RESERVED:** Write as zero.
27:16	0x0 RW	**CURSOR_Y_POSITION_MAGNITUDE_BITS_11:** 0: This register provides the magnitude bits of a signed 13-bit value that specifies the vertical position of cursor. The sign bit of this value is provided by bit 31of this register. (default is 0) When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation.
15	0x0 RW	**CURSOR_X_POSITION_SIGN_BIT:** This bit provides the sign bit of a signed 13-bit value that specifies the horizontal position of cursor. (default is 0).). For normal high resolution display modes, the cursor must have at least a single pixel positioned over the active screen. For HDMI modes where the vertical zoom is greater than 1x, the position is specified using the zoomed grid.
14:12	0x0 RO	**RESERVED_1:** Write as zero.
11:0	0x0 RW	**CURSOR_X_POSITION_MAGNITUDE_BITS_11:** 0: These 12 bits provide the signed 13-bit value that specifies the horizontal position of cursor. The sign bit is provided by bit 15 of this register. (default is 0) For HDMI modes where the horizontal zoom is greater than 1x, the position is specified using the zoomed grid. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation.

4.3.212 CURCLIVEBASE—Offset 700ECh

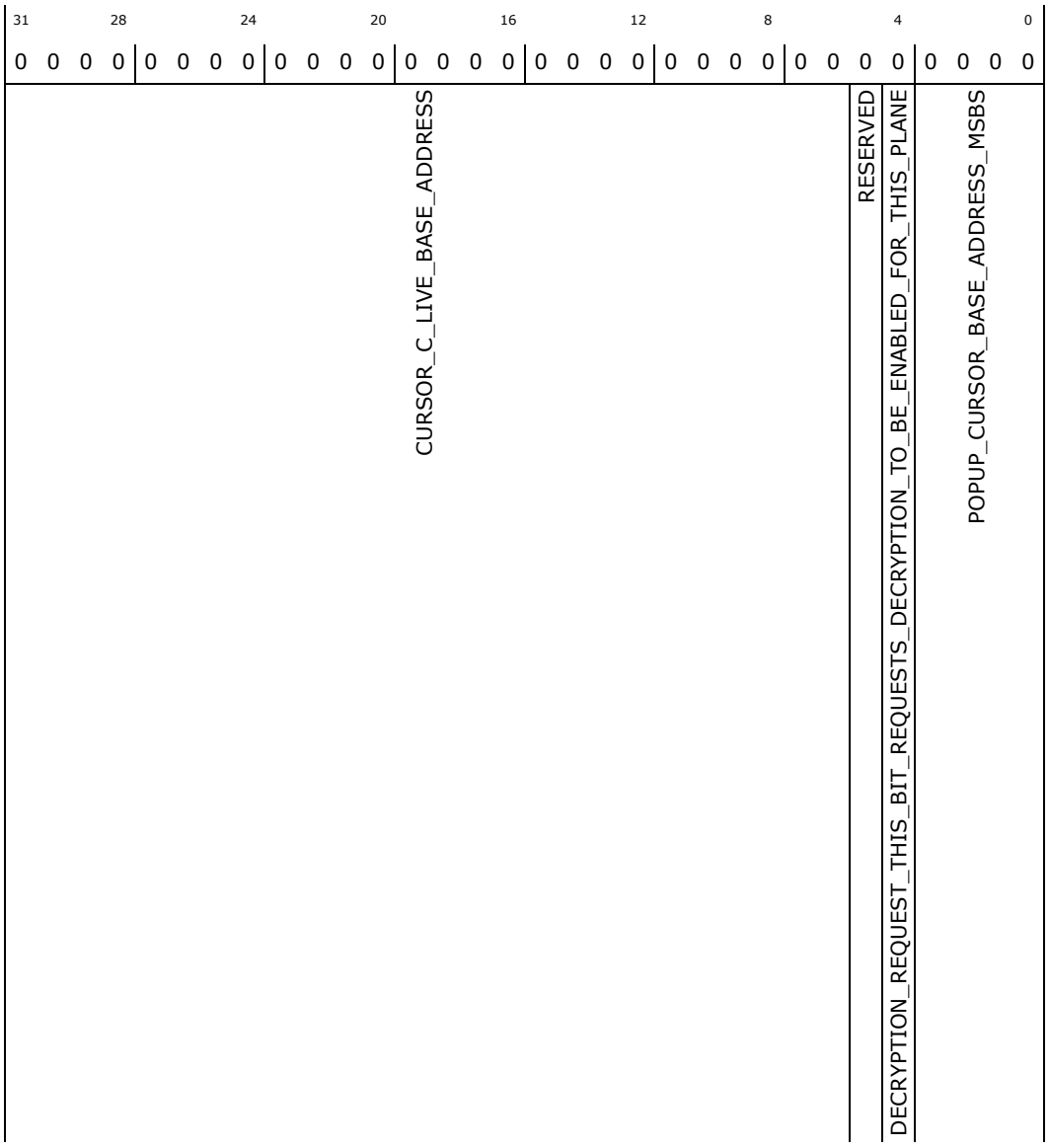
Cursor C Live Base Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 700ECh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**CURSOR_C_LIVE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for Cursor B plane.
5	0x0 RO	**RESERVED:** MBZ
4	0x0 RO	**DECRYPTION_REQUEST_THIS_BIT_REQUESTS_DECRYPTION_TO_BE_ENABLED_FOR_THIS_PLANE:** This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. 0 = Decryption request disabled (default) 1 = Decryption request enabled
3:0	0x0 RO	**POPUP_CURSOR_BASE_ADDRESS_MSBS:** ([DevBW] and [DevCL] Only). This field specifies bits 35:32 of the popup cursor physical address. If popup mode is not selected, this field is ignored.

4.3.213 CURCPALET_0—Offset 700F0h

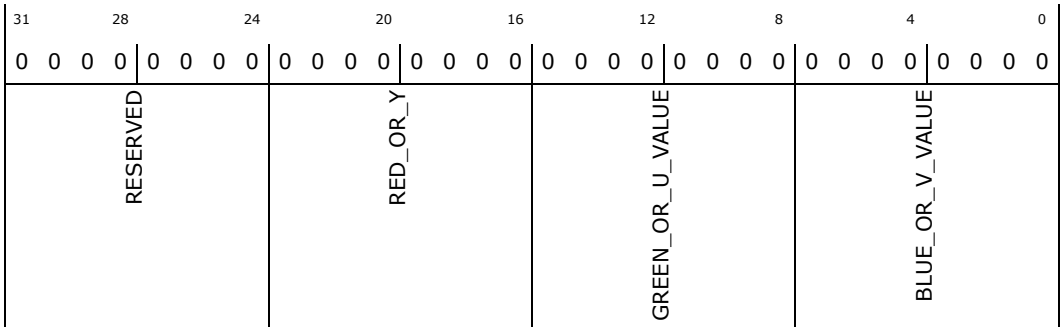
Cursor C Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 700F0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero.
23:16	0x0 RW	**RED_OR_Y:**
15:8	0x0 RW	**GREEN_OR_U_VALUE:**

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**BLUE_OR_V_VALUE:**

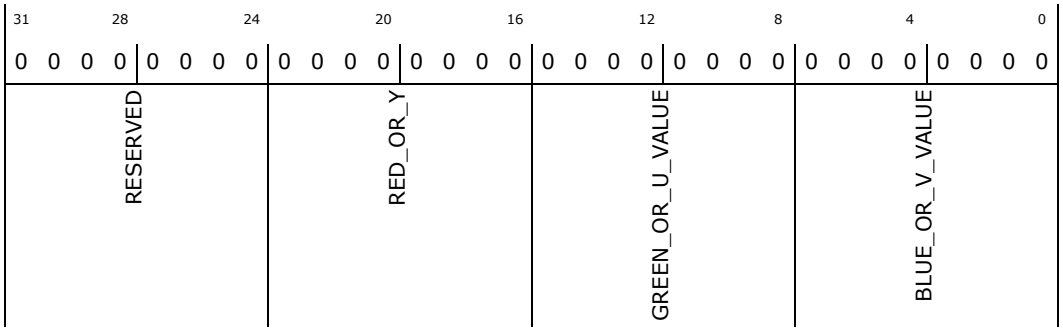
4.3.214 CURCPALET_1—Offset 700F4h

Cursor C Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 700F4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero.
23:16	0x0 RW	**RED_OR_Y:**
15:8	0x0 RW	**GREEN_OR_U_VALUE:**
7:0	0x0 RW	**BLUE_OR_V_VALUE:**

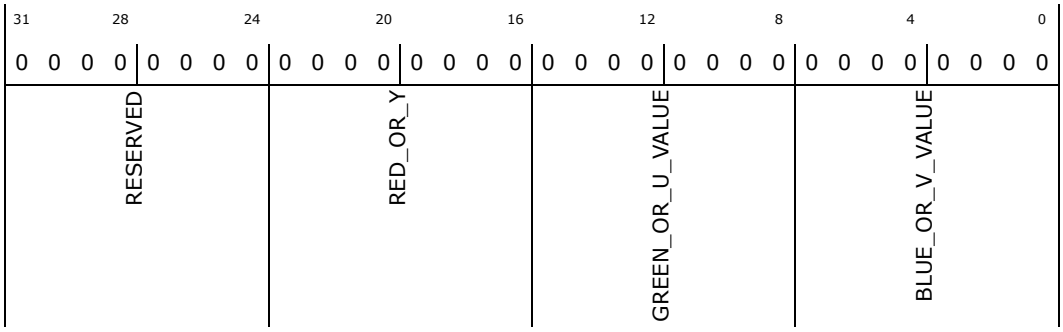
4.3.215 CURCPALET_2—Offset 700F8h

Cursor C Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 700F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero.
23:16	0x0 RW	**RED_OR_Y:**
15:8	0x0 RW	**GREEN_OR_U_VALUE:**
7:0	0x0 RW	**BLUE_OR_V_VALUE:**

4.3.216 CURCPALET_3—Offset 700FCh

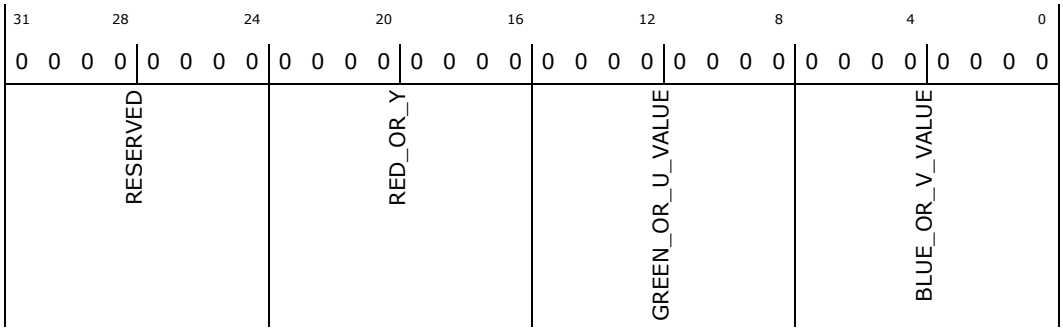
Cursor C Palette registers (4 Registers)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 700FCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero.
23:16	0x0 RW	**RED_OR_Y:**

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RW	**GREEN_OR_U_VALUE:**
7:0	0x0 RW	**BLUE_OR_V_VALUE:**

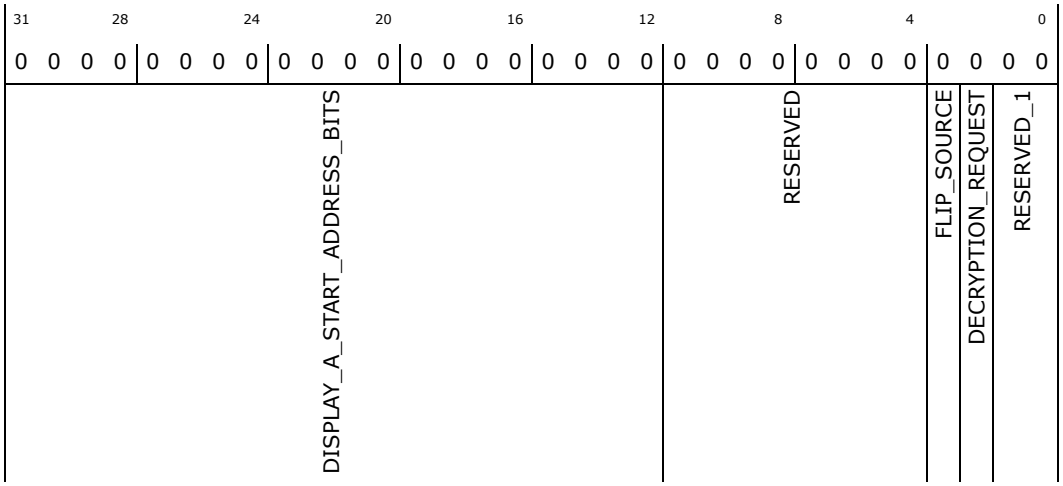
4.3.217 DSPAADDR—Offset 7017Ch

Display A Async flip Start Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7017Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**DISPLAY_A_START_ADDRESS_BITS:** This register provides the start address of the display A plane or the first eye when running in stereo mode. This address must be at least pixel aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . Write to this register triggers async flip. The async flip address is written into the Display A Base Address register 0x7019C

Bit Range	Default & Access	Field Name (ID): Description
11:4	0x0 RO	**RESERVED:** MBZ
3	0x0 RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0x0 RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register.
1:0	0x0 RO	**RESERVED_1:** MBZ

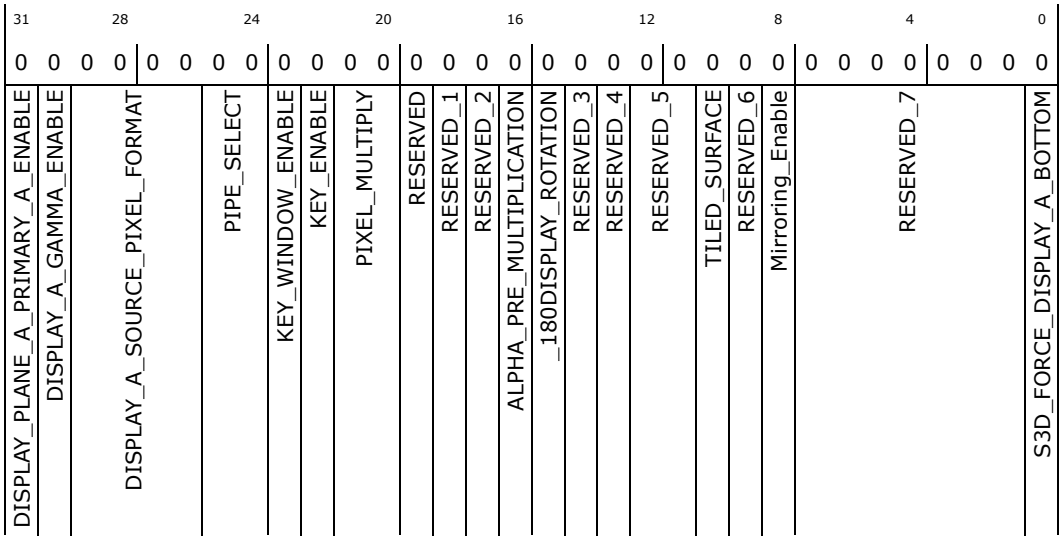
4.3.218 DSPACNTR—Offset 70180h

Display A Plane Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70180h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**DISPLAY_PLANE_A_PRIMARY_A_ENABLE:** When this bit is set, the primary plane will generate pixels for display. When set to zero, display plane A memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that display A is assigned. The display pipe must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. 1 = Enable 0 = Disable
30	0x0 RW	**DISPLAY_A_GAMMA_ENABLE:** This bit should only be changed after the plane has been disabled. It controls the bypassing of the display pipe gamma unit for this display plane s pixel data only. For 8-bit indexed display data, this bit should be set to a one. 0 = Display A pixel data bypasses the display pipe gamma correction logic (default). 1 = Display A pixel data is gamma corrected in the display pipe gamma correction logic.

Bit Range	Default & Access	Field Name (ID): Description
29:26	0x0 RW	**DISPLAY_A_SOURCE_PIXEL_FORMAT:** These bits should only be changed after the plane has been disabled. Pixel formats with an alpha channel (8:8:8:8) should not use source keying. Pixel format of 8-bit indexed uses the palette. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 000x = Reserved. 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format. (with pre-multiplied alpha color format) 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format. (with pre-multiplied alpha color format) 1010 = 32-bit BGRX (10:10:10:2) pixel format Ignore alpha 1011 = 32-bit BGRA (10:10:10:2) pixel format (with pre-multiplied alpha color format) 1100 = 64-bit RGBX (16:16:16:16) 16 bit floating point pixel format. Ignore alpha. 1101 = 64-bit RGBA (16:16:16:16) 16-bit floating point pixel format (with pre-multiplied color format) 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8) pixel format (with pre-multiplied color format)
25:24	0x0 RO	**PIPE_SELECT:** Plane A always ties to Pipe A. AccessType: Read Only Reserved
23	0x0 RW	**KEY_WINDOW_ENABLE:** . This bit applies only to devices with a display plane C. This bit is set to one when the color key is used as a destination key for display C. Display plane C must be enabled on the same pipe and it s Z-order should be programmed to be behind display A for this to be set to a one.0 = Source Key applies to entire display plane A 1 = Source Key applies to only pixels within the intersection between Display A and Display C [DevBLC] and [DevCTG]: Reserved
22	0x0 RW	**KEY_ENABLE:** . This bit enables source keying for display A. Source keying allows a plane that is behind (below) this plane to show through where the display A key matches the display A data. This function is overloaded to provide display C destination keying when combined with the key window enable bit. Setting this bit is not allowed when the display pixel format includes an alpha channel.0 = Source key is disabled 1 = Source key is enabled [DevBLC] and [DevCTG]: Reserved In destination keying, primary plane pixel will be made transparent when blending with sprite pixel as the destination if the primary src key matches with the primary pixel value.

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the pixel multiply mode, the horizontal pixels are doubled and lines are sent twice. Asynchronous flips are not used in this mode. Programming Notes: Asynchronous flips are not permitted when pixel multiply is enabled. 00 = No duplication 01 = Line/pixel Doubling 10 = Reserved 11 = Pixel Doubling only
19	0x0 RO	**RESERVED:** Software must preserve the contents of this bit.
18	0x0 RO	**RESERVED_1:** Write as zero
17	0x0 RO	**RESERVED_2:** Software must preserve the contents of this bit.
16	0x0 RO	**ALPHA_PRE_MULTIPLICATION:** This Bit allows plane logic to alpha multiply ARGB/RGBA pizels if they are not pre multiplied already. 0: RGB Components are pre multiplied with alpha channel of the pixel. 1: RGB components have not been multiplied with alpha channel of the pixel. Plane will performed multiplication before alpha blending.
15	0x0 RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image. [DevCL] Do not enable 180 rotation together with Frame Buffer Compression0 = No rotation 1 = 180 rotation
14	0x0 RO	**RESERVED_3:** [DevBLC] and [DevCTG] Display A Trickle Feed Enable: 0 = Trickle Feed Enabled - Display A data requests are sent whenever there is space in the Display Data Buffer. 1 = Trickle Feed Disabled - Display A data requests are sent in bursts. Note: On mobile products this bit will be ignored such that Trickle Feed is always disabled. [DevELK] Must always be programmed disabled
13	0x0 RO	**RESERVED_4:** [DevBLC] and [DevCTG] Display A Data Buffer Partitioning Control: 0 = Display A Data Buffer will encompass Sprite A buffer space when Sprite A is disabled. 1 = Display A Data Buffer will not use Sprite A buffer space when Sprite A is disabled. Note: When in C3xR Max FIFO mode, this bit will be ignored.
12:11	0x0 RO	**RESERVED_5:** Reserved.
10	0x0 RW	**TILED_SURFACE:** . This bit indicates that the display A surface data is in tiled memory. The tile pitch is specified in bytes in the DSPASTRIDE register. Only X tiling is supported for display surfaces.When this bit is set, it affects the hardware interpretation of the DSPATILEOFF, DSPALINOFF, and DSPASURF registers. 0 = Display A surface uses linear memory 1 = Display A surface uses X-tiled memory

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RO	**RESERVED_6:** Write as zero [DevBLC, DevCTG] Asynchronous Surface Address Update Enable: This bit will enable asynchronous updates of the surface address when written by MMIO. The surface address will change with the next TLB request or when start of vertical blank is reached. Updates during vertical blank may not complete until after the first few active lines are displayed. Restrictions: No command streamer initiated surface address updates are allowed when this bit is enabled. Only one asynchronous update may be made per frame. Must wait for vertical blank before again writing the surface address register. 0 = DSPASURF MMIO writes will update synchronous to start of vertical blank (default) 1 = DSPASURF MMIO writes will update asynchronously
8	0x0 RO	**Mirroring_Enable:** 0: Mirroring is not enabled. 1: Mirroring is enabled.
7:1	0x0 RO	**RESERVED_7:** Write as zero
0	0x0 RW	**S3D_FORCE_DISPLAY_A_BOTTOM:** This bit will force the display A plane to be on the bottom of any sprite planes in the Z order. 0 = Display A Z-order is determined by the other control bits in pipe A 1 = Display A is forced to be on the bottom of any sprite planes in Z-order in pipe A

4.3.219 DSPALINOFF—Offset 70184h

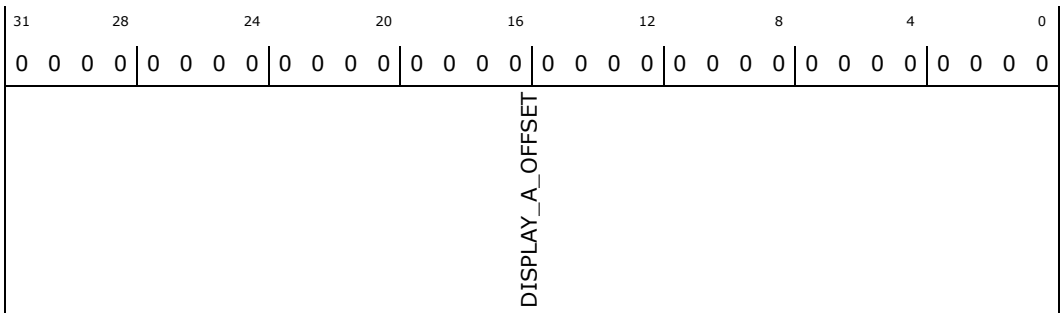
Display A Linear Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70184h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DISPLAY_A_OFFSET:** This register provides the panning offset into the display A plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

4.3.220 DSPASTRIDE—Offset 70188h

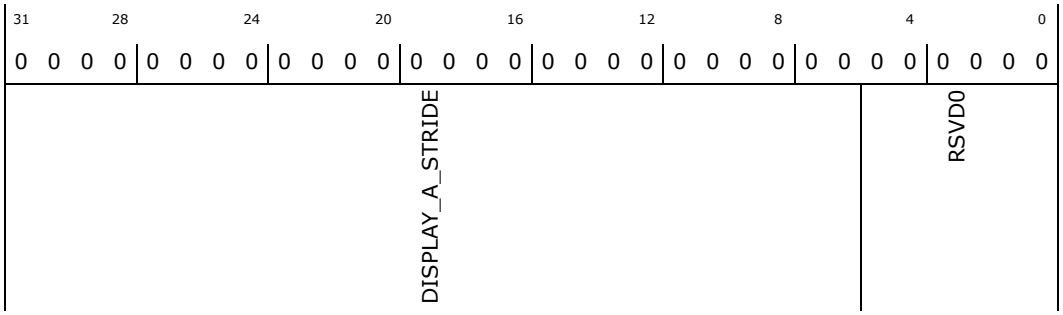
Display A Stride Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70188h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**DISPLAY_A_STRIDE:** This is the stride for display A in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 512 byte aligned. This value is used to determine the line to line increment for the display. This register is updated either through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes. The display stride must be power of 2 when doing Asynch Flips. The display stride must be 8KB or greater when doing Asynch Flips together with 180 rotation. The value in this register is updated through the command streamer during a synchronous flip.
5:0	0x0 RO	**RSVD0:** Reserved

4.3.221 DSPAKEYVAL—Offset 70194h

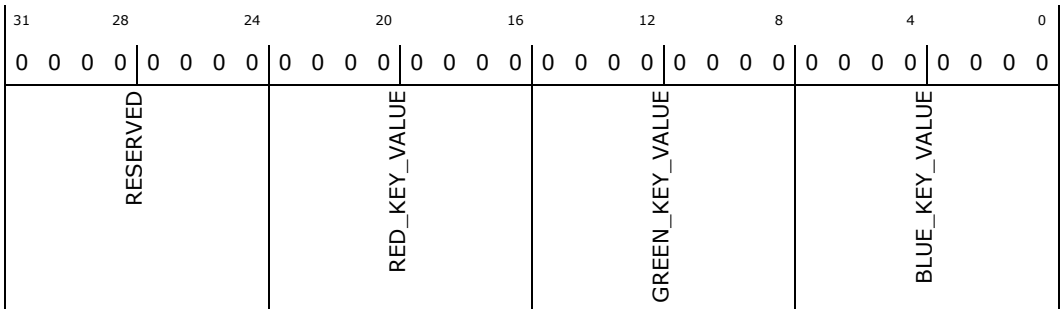
Sprite Color Key Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70194h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Reserved.
23:16	0x0 RW	**RED_KEY_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0x0 RW	**GREEN_KEY_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0x0 RW	**BLUE_KEY_VALUE:** Specifies the color key value for the sprite blue/Cb channel.

4.3.222 DSPAKEYMSK—Offset 70198h

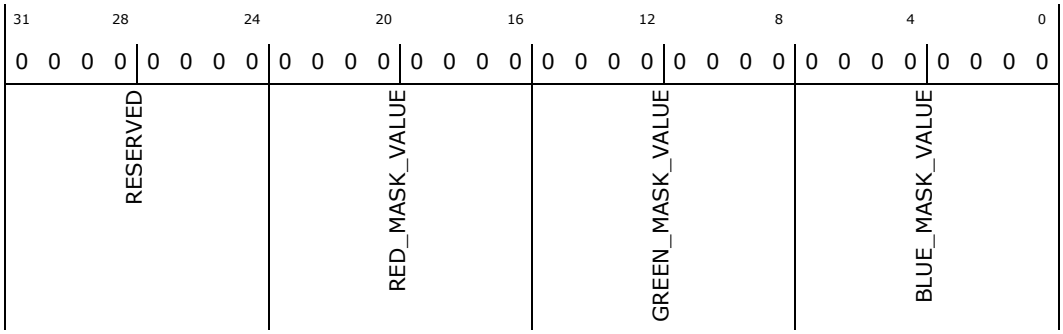
Sprite Color Key Mask Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70198h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x0 RW	**RED_MASK_VALUE:** Specifies the color key mask for the sprite red/Cr channel.
15:8	0x0 RW	**GREEN_MASK_VALUE:** Specifies the color key mask for the sprite green/Y channel.
7:0	0x0 RW	**BLUE_MASK_VALUE:** Specifies the color key mask for the sprite blue/Cb channel.

4.3.223 DSPASURF—Offset 7019Ch

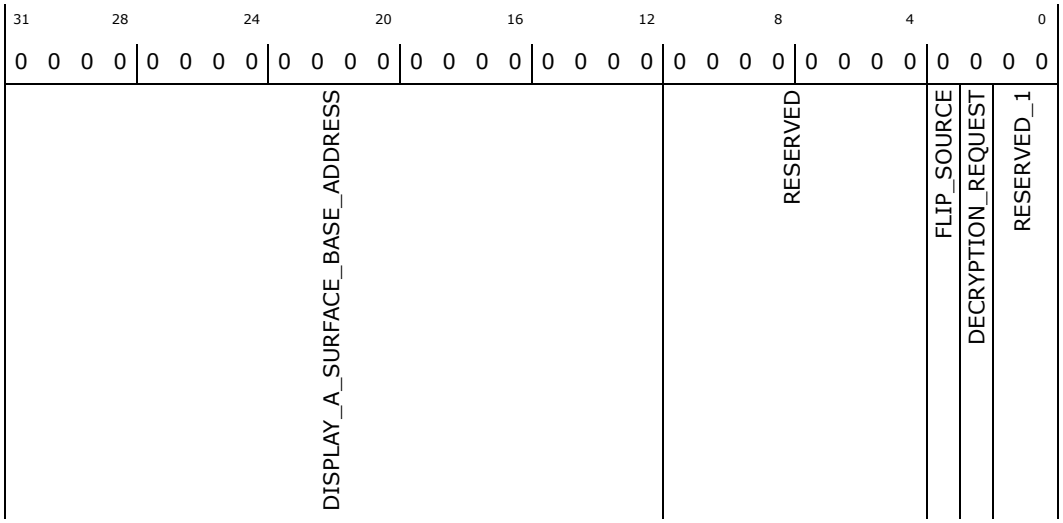
Display A Surface Base Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 7019Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**DISPLAY_A_SURFACE_BASE_ADDRESS:** . This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPATILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPALINOFF register.This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0x0 RO	**RESERVED:** Reserved.
3	0x0 RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0x0 RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register.
1:0	0x0 RO	**RESERVED_1:** MBZ

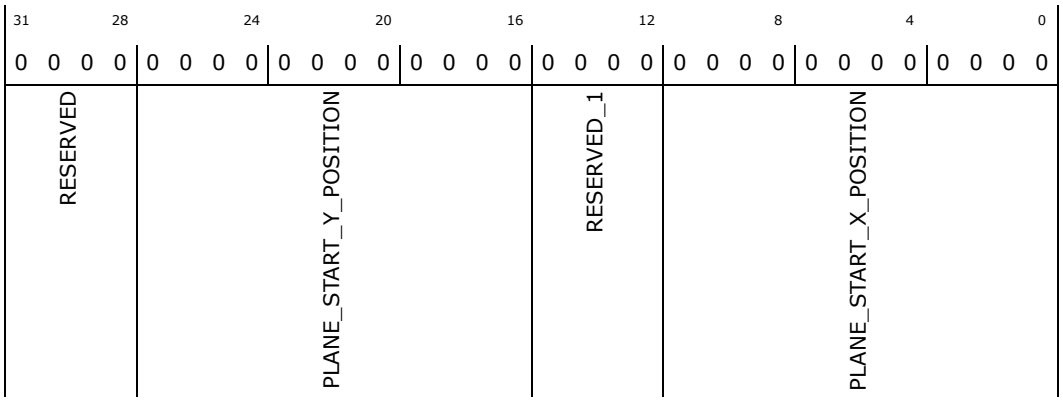
4.3.224 DSPATILEOFF—Offset 701A4h

Display A Tiled Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 701A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation. When display stride is 16KB and doing Asynch Flips, do not program the offset to give pans of 7680 to 8191 bytes.

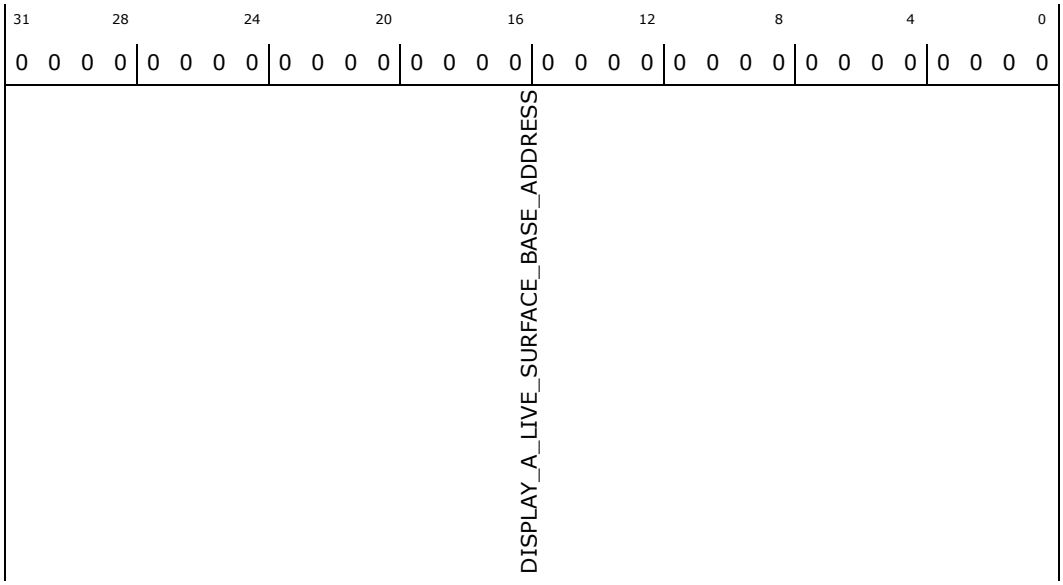
4.3.225 DSPASURFLIVE—Offset 701ACh

Display A Live Surface Base Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 701ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**DISPLAY_A_LIVE_SURFACE_BASE_ADDRESS:** . This gives the live value of the surface base address as being currently used for the plane.

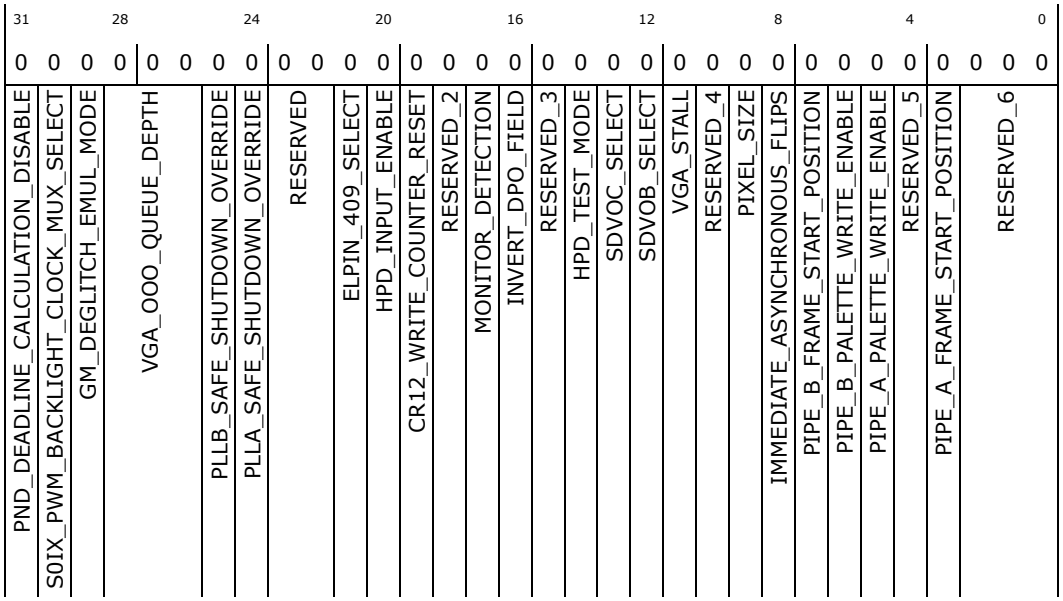
4.3.226 CBR1—Offset 70400h

Chicken Bit Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70400h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**PND_DEADLINE_CALCULATION_DISABLE:** 1 = PND deadline scheme is disabled. Latency deadline calculation is based on the pre-programmed watermark level and the 2-bit FIFO status region. 0 = PND deadline scheme is enabled. Latency deadline calculation is based on actual FIFO level
30	0x0 RW	**S0IX_PWM_BACKLIGHT_CLOCK_MUX_SELECT:** This bit is used to select the new pwm backlight control during s0ix mode 0 = select s0ix pwm backlight control based on 25 MHz oscillator clock (default) 1 = select normal pwm backlight control based on hrawclk Programming note: This bit is programmed to select either 200MHz refclk from CCK or 25MHz refclk from XTAL. This bit cannot be changed on the fly.
29	0x0 RW	**GM_DEGLITCH_EMUL_MODE:** Reserved.
25	0x0 RW	**PLLB_SAFE_SHUTDOWN_OVERRIDE:** This bit disables the dependency for pipe B to be disabled before the PLL is shut down
24	0x0 RW	**PLLA_SAFE_SHUTDOWN_OVERRIDE:** This bit disables the dependency for pipe A to be disabled before the PLL is shut down
23:22	0x0 RO	**RESERVED:** Reserved.
21	0x0 RW	**ELPIN_409_SELECT:** This bit is used to select one of the elpin 409 bug fixes 0 = vrd_ci_rreq 1 = count comparator
20	0x0 RW	**HPD_INPUT_ENABLE:** : this bit is used to enable HPD detection using HPD input pin 0 = HPD Input is disabled (default) 1 = HPD input is enabled

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RW	**CR12_WRITE_COUNTER_RESET:** 0 = Disable CR12 write counter reset 1 = Enable CR12 write counter reset
18	0x0 RO	**RESERVED_2:** Reserved.
17	0x0 RW	**MONITOR_DETECTION:** This bit is used to test the monitor detection. Do not program unless directed.
16	0x0 RW	**INVERT_DPO_FIELD:** Invert DPO interlaced field output. This bit is used to invert the field sense input to the planes from DPO.
15	0x0 RO	**RESERVED_3:** Reserved.
14	0x0 RW	**HPD_TEST_MODE:** load programmable value for filter and long pulse value of HPD register 0x70408.
13	0x0 RW	**SDVOC_SELECT:** sdvoc deglitch logic output select
12	0x0 RW	**SDVOB_SELECT:** sdvob deglitch logic output select
10	0x0 RO	**RESERVED_4:** to prevent async flip failures.
8	0x0 RW	**IMMEDIATE_ASYNCHRONOUS_FLIPS:** This bit causes asynchronous flips to complete immediately upon the start of the vertical blank period. When enabling this feature, frame start should also be moved to the end of the vertical blank period by setting the frame start position bit.
7	0x0 RW	**PIPE_B_FRAME_START_POSITION:** This bit changes the position of frame start on pipe B. This feature is used in conjunction with the immediate asynchronous flips bit to enable fast asynchronous flips during vertical blanking. 0 = frame start occurs at start of the vertical blank period 1 = frame start occurs at end of the vertical blank period Default: 1, causing frame start to occur at the end of vertical blank
6	0x0 RW	**PIPE_B_PALETTE_WRITE_ENABLE:** Disables anti-collision logic in the palette during non-blanking periods on pipe B.
5	0x0 RW	**PIPE_A_PALETTE_WRITE_ENABLE:** Disables anti-collision logic in the palette during non-blanking periods on pipe A
4	0x0 RO	**RESERVED_5:**
3	0x0 RW	**PIPE_A_FRAME_START_POSITION:** This bit changes the position of frame start on pipe A. This feature is used in conjunction with the immediate asynchronous flips bit to enable fast asynchronous flips during vertical blanking. 0 = frame start occurs at start of the vertical blank period 1 = frame start occurs at end of the vertical blank period Default: 1, causing frame start to occur at the end of vertical blank
2:0	0x0 RO	**RESERVED_6:**

4.3.227 CBR2—Offset 70404h

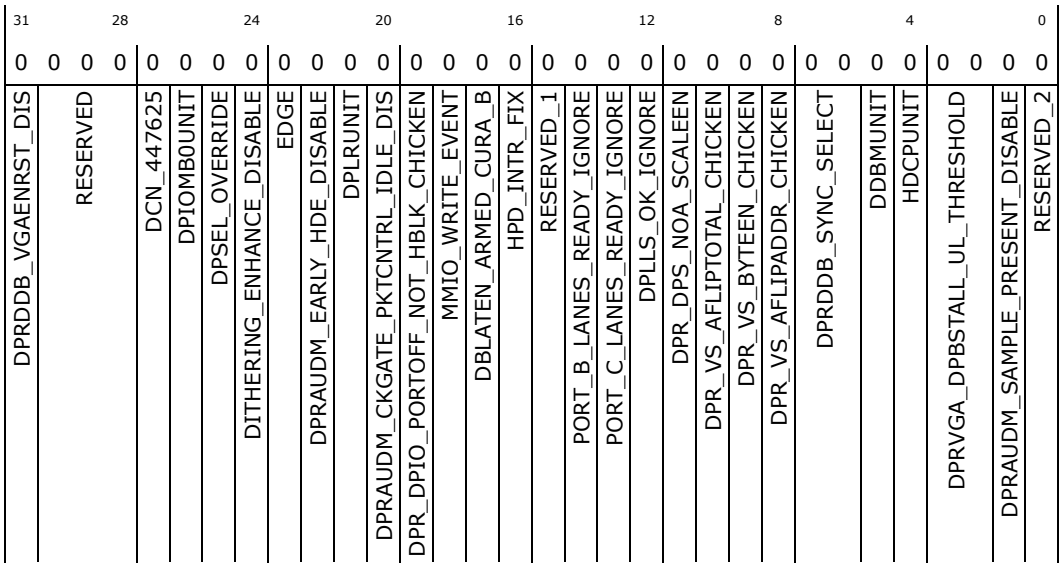
Chicken2 Bit Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70404h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
30:28	0x0 RO	**RESERVED:** Reserved.
27	0x0 RW	**DCN_447625:** - x8 support for hybrid gfx, Kwasi requested (dpr_dpio_x8_conc_sel)
26	0x0 RW	**DPIOMB0UNIT:** ignoring EDP logic when enabling Lanes by the dptc_otxoenb
25	0x0 RW	**DPSEL_OVERRIDE:** when this chicken bit is set override the selects to 0
24	0x0 RW	**DITHERING_ENHANCE_DISABLE:** Anh need for dithering enhance (dithering_enhance_disable)
23	0x0 RW	**EDGE:** edgeA/Bvblank, edgeDPSA/Bvblank, curA/Bedgevblank,
22	0x0 RW	**DPRAUDM_EARLY_HDE_DISABLE:** Chicken bit to Audio unit to disable early RAM FIFO read in 2-channel mode (DPRAUDM_early_hde_disable)
21	0x0 RW	**DPLRUNIT:** Selects cdclk for pwm logic, pwm logic, uses hrawclk by default (select cdclk in scan mode or by setting a chicken bit)
20	0x0 RW	**DPRAUDM_CKGATE_PKTCNTRL_IDLE_DIS:** Chicken bit to disable audclk gating when pktcontrol FSM is idle (DPRAUDM_ckgate_pktcntrl_idle_dis)

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RW	**DPR_DPIO_PORTOFF_NOT_HBLK_CHICKEN:** This bit is needed to qualify the port off with hblank to take care of fragmented audio packet sent off. When chicken bit is enabled, the port off is dependent upon state of hblank, else the legacy behavior rules (dpr_dpio_portoff_not_hblk_chicken)
18	0x0 RW	**MMIO_WRITE_EVENT:** 0: mmio_write_event = RMDecPipeSLC_pre 1: mmio_write_event = 1'b0
17	0x0 RW	**DBLATEN_ARMED_CURA_B:** Reserved.
16	0x0 RW	**HPD_INTR_FIX:** Freezes hpdb_intr_fix, hpdc_intr_fix, hpdd_intr_fix
15	0x0 RO	**RESERVED_1:** Reserved.
14	0x0 RW	**PORT_B_LANES_READY_IGNORE:** 1: Lanes considered as ready for normal operation 0: usual operation: Lanes readiness indications arrived from DPIO SEG outputs
13	0x0 RW	**PORT_C_LANES_READY_IGNORE:** 1: Lanes considered as ready for normal operation 0: usual operation: Lanes readiness indications arrived from DPIO SEG outputs
12	0x0 RW	**DPLLS_OK_IGNORE:** 1: Both mPHY DPLLs considered as OK ('1'). Lanes can be enabled. 0: usual operation: DPLL readiness indications arrived from DPIO SEG outputs
11	0x0 RW	**DPR_DPS_NOA_SCALEEN:** This bit is to enable viewing critical control signals that were added as a result of Cantiga B0 Overlay changes. Default = 0. (dpr_dps_noa_scaleen) 0: Non-scaling signals are sent to NOA bus 1: Scaling signals are sent to the NOA bus
10	0x0 RW	**DPR_VS_AFLIPTOTAL_CHICKEN:** This chicken bit bypasses the current logic used for calculating the number of requests to make for an asynchronous flip. It will be helpful because the current logic is very difficult to validate. (dpr_vs_afliptotal_chicken)
9	0x0 RW	**DPR_VS_BYTEEN_CHICKEN:** This chicken bit bypasses the current logic used for selecting the proper byte enables. It is intended to address byte enables during asynchronous flips, but it was easier to bypass the entire byte-enable circuit instead. HSD bug #1932963. (dpr_vs_byteen_chicken)
8	0x0 RW	**DPR_VS_AFLIPADDR_CHICKEN:** This chicken bit bypasses the current logic used for selecting the starting fetch address of an asynchronous flip. HSD bug #1932964. (dpr_vs_aflipaddr_chicken)

Bit Range	Default & Access	Field Name (ID): Description
7:6	0x0 RW	**DPRDDB_SYNC_SELECT:** When set vsync reset is asserted and when clear no reset is asserted. (dprddb_novsyncreset) This selects between VRVSYNC and hi-res VSYCN when set with dprvrd_novsyncreset also set sync_select novsyncreset. (dprddb_sync_select) X0 = No Vsync reset 01 = vsync or hi-res between Nat and UL mode 11 = vsync reset in both UL and native
5	0x0 RW	**DDBMUNIT:** C0 ECO1 chicken bit defaulted to fix enable
4	0x0 RW	**HDCPUNIT:** EGLK A5 ECO1 Fix. Read Data Fix For RMBus Protocol. vsmunit: Lock Up Issue.
1	0x0 RW	**DPRAUDM_SAMPLE_PRESENT_DISABLE:** When set this bit will disable the sample present bits being set in layout 1 mode of Audio. Default is to enable sample present on Audio. (DPRAUDM_sample_present_disable) vsmunit: FBC/SR Power Fix
0	0x0 RO	**RESERVED_2:** MBZ. This bit si the same as bit 31 in 70450h rega_loadcount_crtdetect

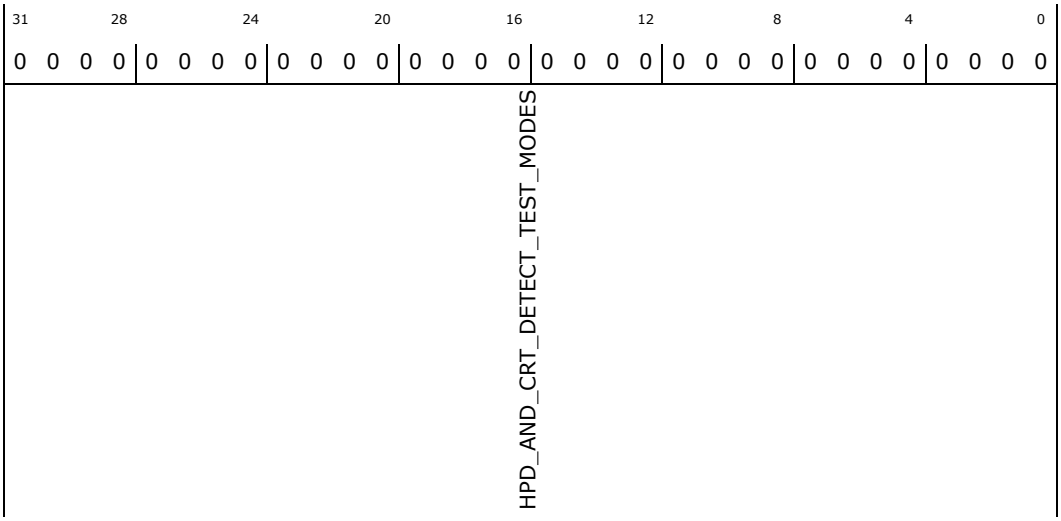
4.3.228 CCBR—Offset 70408h

ChickenCount Bit Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70408h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**HPD_AND_CRT_DETECT_TEST_MODES:** Reserved.

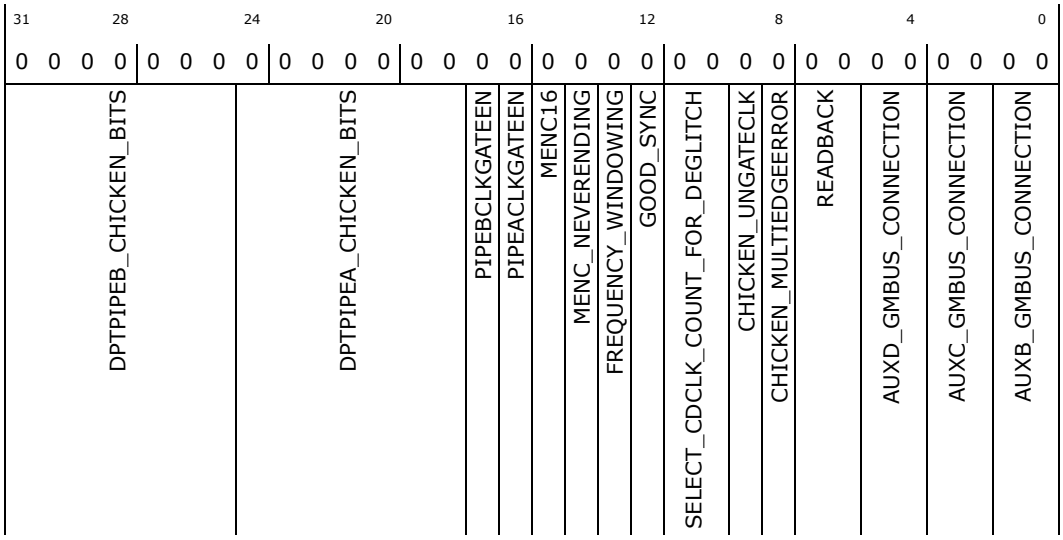
4.3.229 CBR3—Offset 7040Ch

Chicken3 Bit Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7040Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RW	**DPTPIPEB_CHICKEN_BITS:** not used
24:18	0x0 RW	**DPTPIPEA_CHICKEN_BITS:** not used
17	0x0 RW	**PIPEBCLKGATEEN:** Enables reg_pipeBclkgateen_cd reg_pipeBclkgateen_db
16	0x0 RW	**PIPEACLKGATEEN:** Enables reg_pipeAclkgateen_cd reg_pipeAclkgateen_da
15	0x0 RW	**MENC16:** Chicken to cause MENC to output just 16 manchester 0s for sync (otherwise 26)
14	0x0 RW	**MENC_NEVERENDING:** Chicken to cause MENC to output neverending sync 0s for electrical testing
13	0x0 RW	**FREQUENCY_WINDOWING:** Chicken to tighten the frequency windowing

Bit Range	Default & Access	Field Name (ID): Description
12	0x0 RW	**GOOD_SYNC:** Chicken to check for only 8 good sync 0s instead of 12
11:10	0x0 RW	**SELECT_CDCLK_COUNT_FOR_DEGLITCH:** 11 = 1/16 2X bit clock divider value - 31.125ns 10 = 1/8 2X bit clock divider value - 62.5ns 01 = 1/4 2X bit clock divider value - 125ns 00 = 25 - GMBUS type 50ns at 500MHz cdclk
9	0x0 RW	**CHICKEN_UNGATECLK:** 1 = Ungate clock 0 = Automatic clock gating
8	0x0 RW	**CHICKEN_MULTIEDGEERROR:** 1 = Multiple edges in window is an eror 0 = Multiple edges in window is okay
7:6	0x0 RW	**READBACK:** 11 = Readback of bit clock divide field gives the error type 01 = Readback gives the recovered clock frequency 00 = Readback gives the programmed clock frequency
5:4	0x0 RW	**AUXD_GMBUS_CONNECTION:** Selects gmbus connection for AUXD
3:2	0x0 RW	**AUXC_GMBUS_CONNECTION:** Selects gmbus connection for AUXC
1:0	0x0 RW	**AUXB_GMBUS_CONNECTION:** Selects gmbus connection for AUXB

4.3.230 SWF00—Offset 70410h

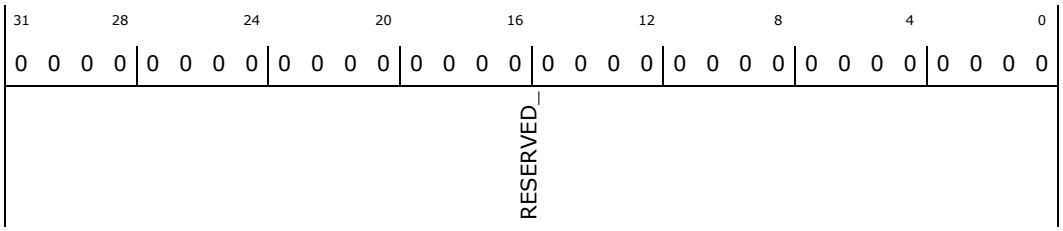
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70410h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

4.3.231 SWF01—Offset 70414h

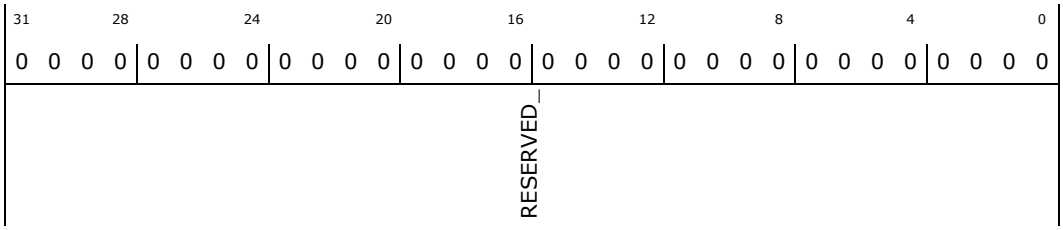
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70414h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

4.3.232 SWF02—Offset 70418h

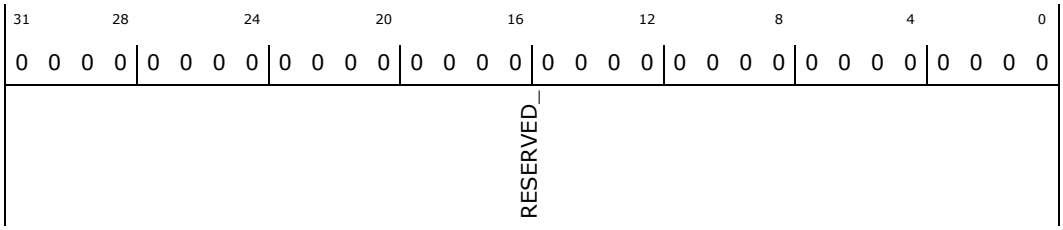
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70418h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

4.3.233 SWF03—Offset 7041Ch

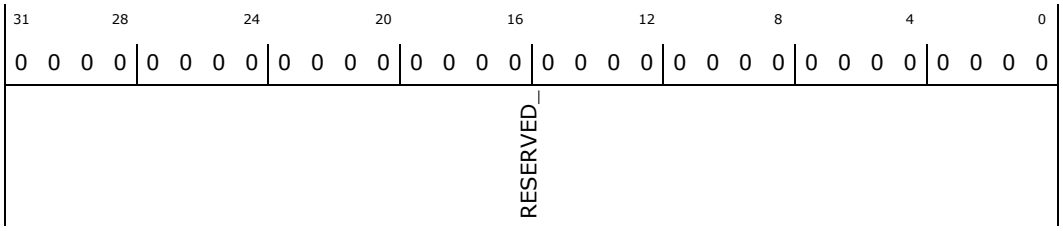
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 7041Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

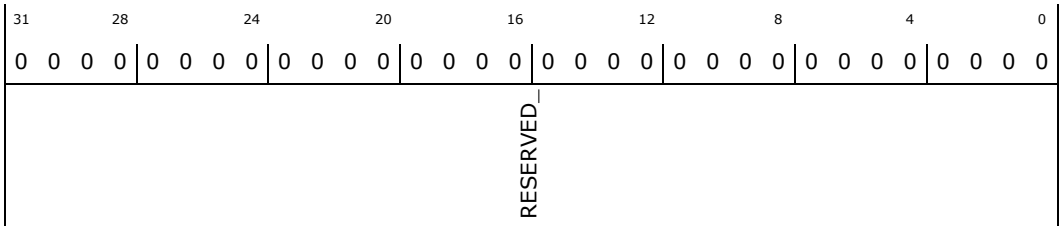
4.3.234 SWF04—Offset 70420h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70420h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

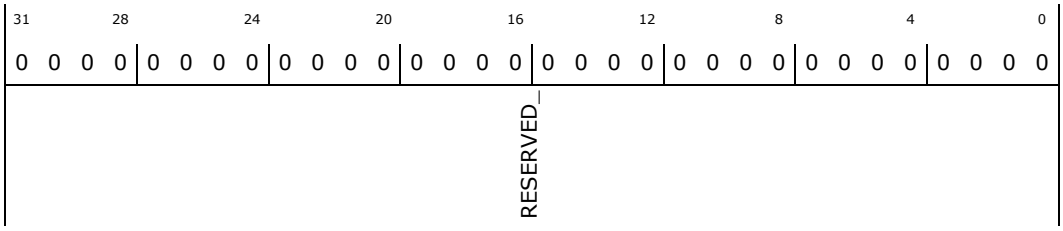
4.3.235 SWF05—Offset 70424h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70424h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

4.3.236 SWF06—Offset 70428h

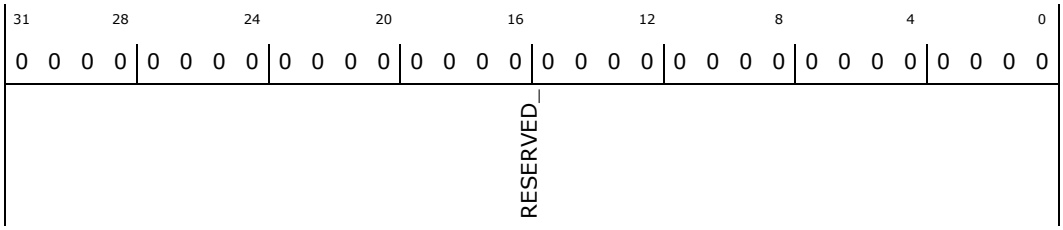
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70428h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

4.3.237 SWF07—Offset 7042Ch

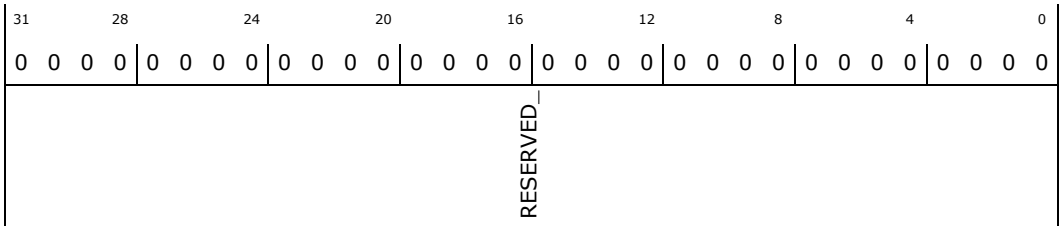
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 7042Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

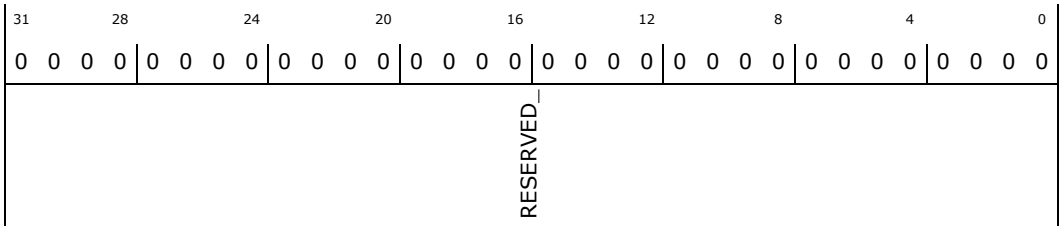
4.3.238 SWF08—Offset 70430h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70430h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

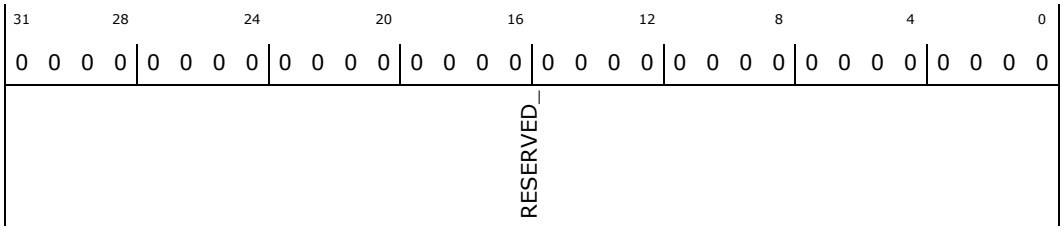
4.3.239 SWF09—Offset 70434h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70434h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

4.3.240 SWF0A—Offset 70438h

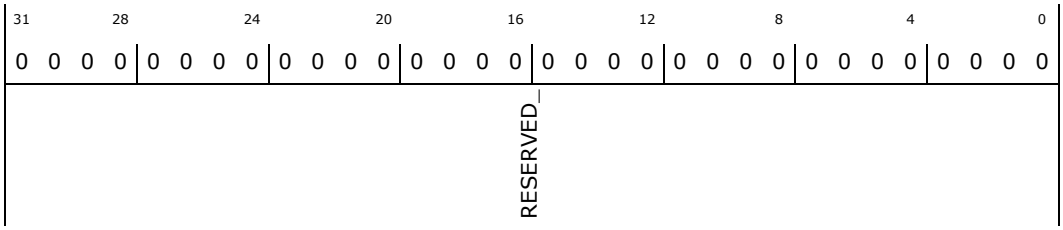
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70438h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

4.3.241 SWF0B—Offset 7043Ch

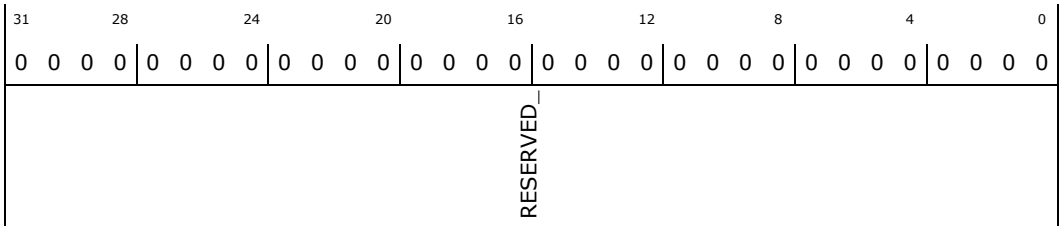
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 7043Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

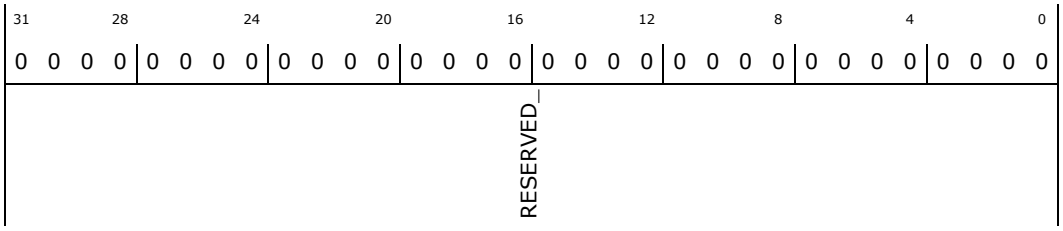
4.3.242 SWF0C—Offset 70440h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70440h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

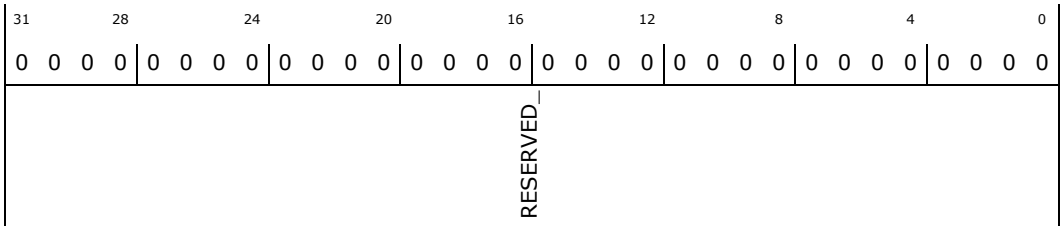
4.3.243 SWF0D—Offset 70444h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70444h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

4.3.244 SWF0E—Offset 70448h

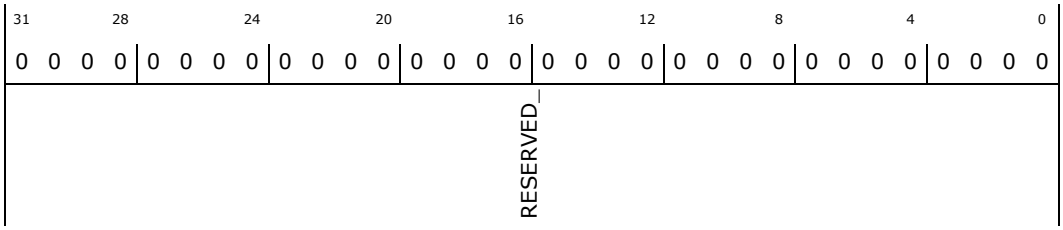
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 70448h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

4.3.245 SWF0F—Offset 7044Ch

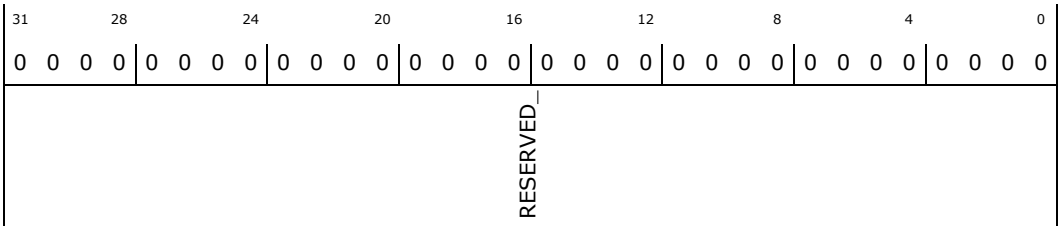
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 7044Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

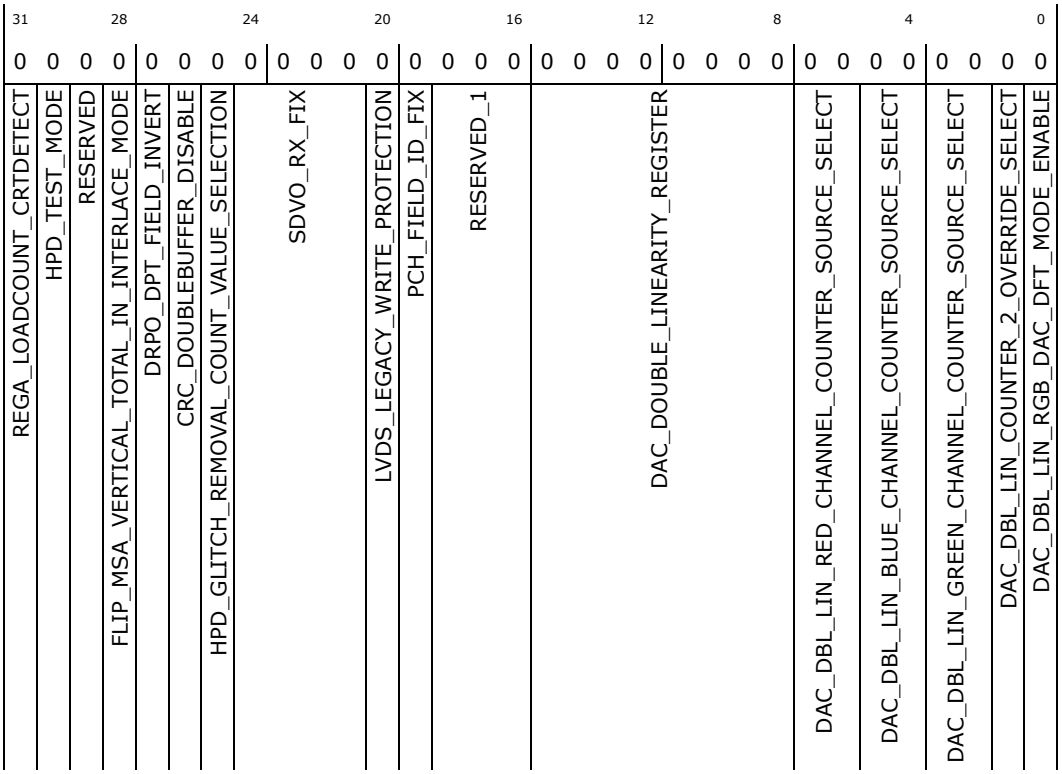
4.3.246 CBR4—Offset 70450h

Display Chicken Bits 4 ;

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 70450h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**REGA_LOADCOUNT_CRTDETECT:** Project: All Format: Load initial value to crtdetect counter
30	0x0 RW	**HPD_TEST_MODE:** Project: All Default Value: ;0b Load programmable value for filter and long pulse value of HPD Value Name Description Project 0b Short Pulse Short Pulse All 1b Long Pulse Long Pulse All
29	0x0 RO	**RESERVED:** Project: All Format: PBC
28	0x0 RW	**FLIP_MSA_VERTICAL_TOTAL_IN_INTERLACE_MODE:** Project: All Format: Set to 1 to flip MSA vtotal
27	0x0 RW	**DRPO_DPT_FIELD_INVERT:** Project: All Format: Invert interlaced field ID output from dptunit.
26	0x0 RW	**CRC_DOUBLEBUFFER_DISABLE:** Project: All Format: Disable doublebuffering on CRCs so enable/disable and source select will happen immediately.
25	0x0 RW	**HPD_GLITCH_REMOVAL_COUNT_VALUE_SELECTION:** Project: All Default Value: ;0b Value Name Description Project 0b 500us 500us glitch removal All 1b 50us 50us glitch removal All
24:21	0x0 RW	**SDVO_RX_FIX:** Project: All Format: Program SDVO receiver fix values
20	0x0 RW	**LVDS_LEGACY_WRITE_PROTECTION:** Project: All Format:
19	0x0 RW	**PCH_FIELD_ID_FIX:** Project: All Format: 1: CPU and PCH field IDs are independent 0: CPU field ID is tied to PCH field ID
18:16	0x0 RO	**RESERVED_1:** Project: All Format: MBZ
15:8	0x0 RW	**DAC_DOUBLE_LINEARITY_REGISTER:** Project: All Format: Project: DevIBX-B Value Name Description Project 00b Disable Normal RGB operation, no test mode enabled All 01b Counter 1 Counter 1 All 10b Inverse Counter 1 Inverse of counter 1 All 11b Counter 2 Counter 2 All

Bit Range	Default & Access	Field Name (ID): Description
7:6	0x0 RW	**DAC_DBL_LIN_RED_CHANNEL_COUNTER_SOURCE_SELECT:** Project: DevIBX-B Default Value: ;00b DefaultVaueDesc BitFieldDesc Value Name Description Project 00b Disable Normal RGB operation, no test mode enabled All 01b Counter 1 Counter 1 All 10b Inverse Counter 1 Inverse of Counter 1 All 11b Counter 2 Counter 2 All Programming Notes Notes Errata Description Project # Desc All
5:4	0x0 RW	**DAC_DBL_LIN_BLUE_CHANNEL_COUNTER_SOURCE_SELECT:** Project: DevIBX-B Default Value: ;00b Value Name Description Project 00b Disable Normal RGB operation, no test mode enabled All 01b Counter 1 Counter 1 All 10b Inverse Counter 1 Inverse of counter 1 All 11b Counter 2 Counter 2 All
3:2	0x0 RW	**DAC_DBL_LIN_GREEN_CHANNEL_COUNTER_SOURCE_SELECT:** Project: DevIBX-B Default Value: ;00b Value Name Description Project 00b Disable Normal RGB operation, no test mode enabled All 01b Counter 1 Counter 1 All 10b Inverse Counter 1 Inverse of counter 1 All 11b Counter 2 Counter 2 All
1	0x0 RW	**DAC_DBL_LIN_COUNTER_2_OVERRIDE_SELECT:** Project: DevIBX-B Default Value: ;0b Value Name Description Project 0b No override No override, count value is from counter 2 All 1b Override Override mode enabled, count value is from 8-bit override value All
0	0x0 RW	**DAC_DBL_LIN_RGB_DAC_DFT_MODE_ENABLE:** Project: DevIBX-B Default Value: ;0b Value Name Description Project 0b Disable Normal operation, no test mode enabled All 1b Enable RGB DAC DFT mode enabled All

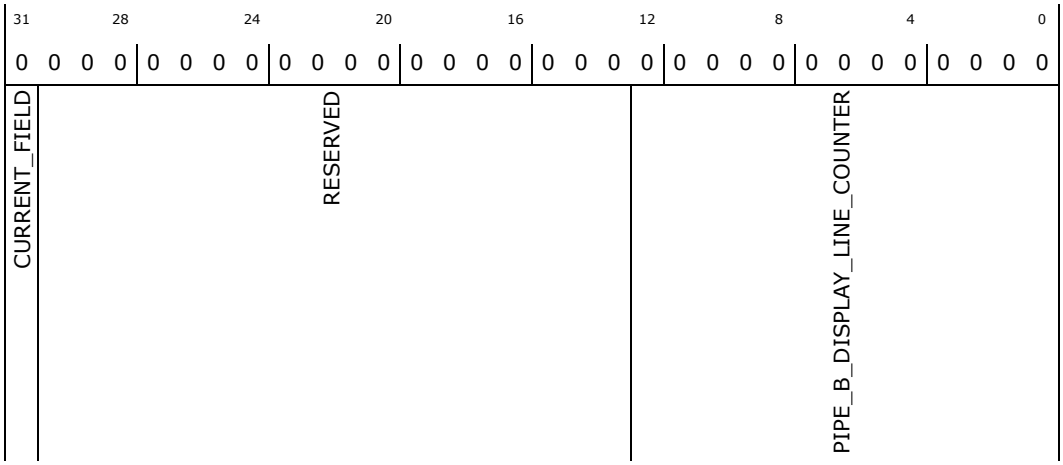
4.3.247 PIPEB_DSL—Offset 71000h

Display Scan Line

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 71000h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**CURRENT_FIELD:** Provides read back of the current field being displayed on display pipe B. Non-TV mode: 0 = first field (odd field) 1 = second field (even field) TV mode: 1 = first field (odd field) 0 = second field (even field) [DevBW and DevCL] Reserved: Read only.
30:13	0x0 RO	**RESERVED:** Read only.
12:0	0x0 RO	**PIPE_B_DISPLAY_LINE_COUNTER:** This register enables the read back of the display vertical line counter . The display line values are from the pipe B timing generator. They change at the leading edge of HSYNC, and can be safely read at any time.

4.3.248 PIPEB_SLC—Offset 71004h

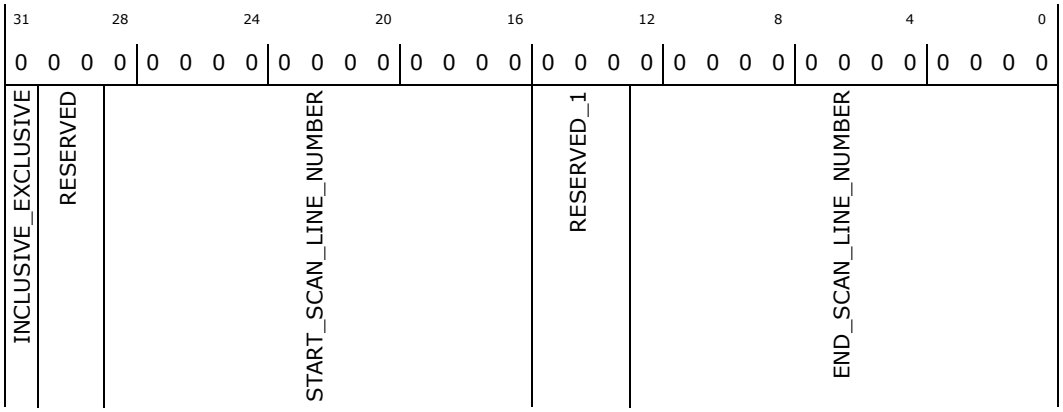
Pipe B Display Scan Line Range Compare Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 71004h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**INCLUSIVE_EXCLUSIVE:** 1 = Inclusive Within Range, 0 = Exclusive Out of Range
30:29	0x0 RO	**RESERVED:** Read only.
28:16	0x0 RW	**START_SCAN_LINE_NUMBER:** This field specifies the starting scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0,Display Buffer height in lines-1]. [DevBW] and [DevCL] End Scan Line Number: This field specifies the ending scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0, Display Buffer height in lines-1].
15:13	0x0 RO	**RESERVED_1:** Read only.
12:0	0x0 RW	**END_SCAN_LINE_NUMBER:** This field specifies the ending scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0, Display Buffer height in lines-1]. [DevBW] and [DevCL] Start Scan Line Number: This field specifies the starting scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0,Display Buffer height in lines-1].

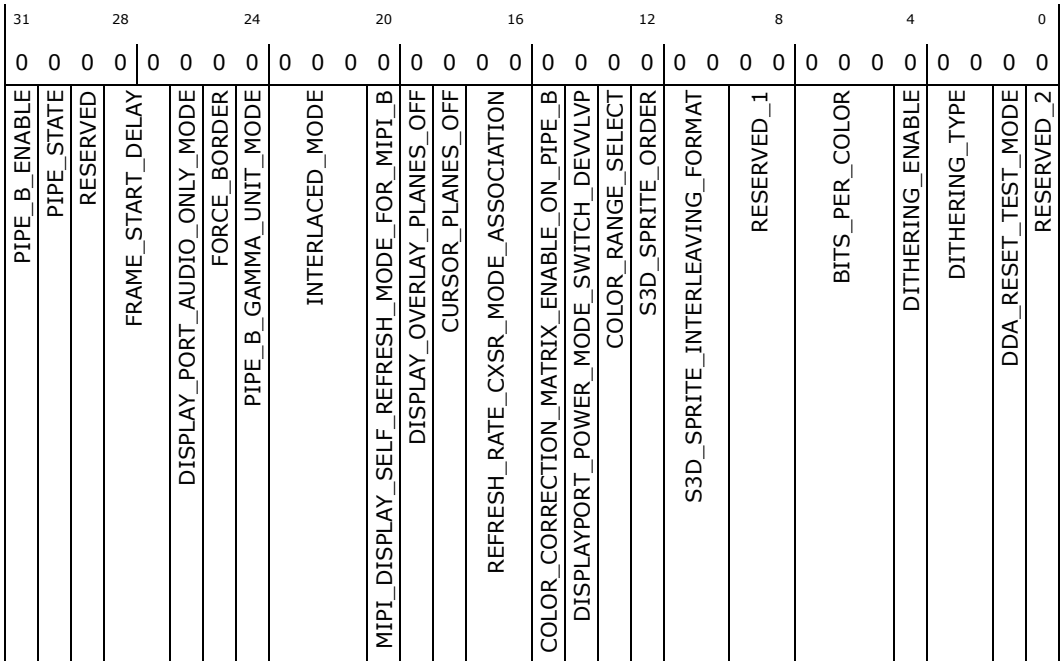
4.3.249 PIPEBCONF—Offset 71008h

Pipe B Configuration Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 71008h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**PIPE_B_ENABLE:** Setting this bit to the value of one, turns on pipe B. This must be done before any planes are enabled on this pipe. Changing it to a zero should only be done when all planes that are assigned to this pipe have been disabled. Turning the pipe enable bit off disables the timing generator in this pipe. Plane disable occurs after the next VBLANK event after the plane is disabled. Synchronization pulses to the display are not maintained if the timing generator is disabled. Power consumption will be at its lowest state when disabled. A separate bit controls the DPLL enable for this pipe. Pipe timing registers should contain valid values before this bit is enabled. Disabling the Pipe and changing the timing registers and re-enabling the pipe before the next VBLANK will cause the mode change to occur at the end of the current frame. This requires no wait on the software s part. On the other hand, if this is the disabling of the pipe, that does require a software wait for VBLANK to occur. Synchronization pulses to the display are not maintained if the timing generator is disabled. Power consumption is at it s lowest state. 1 = Enable 0 = Disable
30	0x0 RO	**PIPE_STATE:** This bit indicates the actual state of the pipe. Since there can be some delay between disabling the pipe and the pipe actually shutting off, this bit indicates the true current state of the pipe. 0 = Disabled 1 = Enabled AccessType: Read Only
29	0x0 RO	**RESERVED:** Write as zero.

Bit Range	Default & Access	Field Name (ID): Description
28:27	0x0 RW	**FRAME_START_DELAY:** Used to delay the frame start signal that is sent to the display planes. Normal operation uses the default 00 value and test modes can use the delayed frame start to shorten the test time. This would be set to 00 for normal operation. 00 = Frame Start occurs on the first HBLANK after the start of VBLANK 01 = Frame Start occurs on the second HBLANK after the start of VBLANK 10 = Frame Start occurs on the third HBLANK after the start of VBLANK 11 = Frame Start occurs on the forth HBLANK after the start of VBLANK
26	0x0 RW	**DISPLAY_PORT_AUDIO_ONLY_MODE:** Setting this bit to 1 indicates the DisplayPort will output audio only. 0 = DisplayPort will output Video or Video and Audio 1 = DisplayPort will output Audio only
25	0x0 RW	**FORCE_BORDER:** (TEST MODE)0 = Normal Operation 1 = Color information is ignored and border color is substituted during active region
24	0x0 RW	**PIPE_B_GAMMA_UNIT_MODE:** . This bit selects which mode the pipe gamma correction logic works in. In the palette mode, it behaves as a 3X256x8 RAM lookup. Indexed mode operation should use the palette in 8-bit mode. In the 10-bit gamma mode, it will act as a piecewise linear interpolation. Other gamma units such as in the overlay and sprite are unaffected by this bit.0 = 8-bit Palette Mode 1 = 10-bit Gamma Mode
23:21	0x0 RW	**INTERLACED_MODE:** These bits are used for software control of interlaced behavior. They are updated immediately if the pipe is off, or in the vertical blank after programming if pipe is enabled. 0xx = Progressive 100 = Interlaced embedded panel using programmable vertical sync shift (2x) 101 = Interlaced using vertical sync shift. Backup option to setting 110. (2x) 110 = Interlaced with VSYNC/HSYNC Field Indication using legacy vertical sync shift. Used for SDVO. 111 = Interlaced with Field 0 Only using legacy vertical sync shift. Not used. Setting the Interlaced embedded panel mode causes hardware to automatically modify the output to match the specifications of panels that support interlaced mode.
20	0x0 RW	**MIPI_DISPLAY_SELF_REFRESH_MODE_FOR_MIPI_B:** .0 = Normal Operation, display controller generate timing and refresh display panel at refresh rate 1 = Display self-refresh mode. Display controller update frame buffer in display module on demand only
19	0x0 RW	**DISPLAY_OVERLAY_PLANES_OFF:** . This bit when set will cause all enabled Display and overlay planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit, at the next VBLANK. Timing signals continue as they were but the screen becomes blank. Setting the bit back to a zero will then allow the display and overlay planes to resume on the following VBLANK.0 = Normal Operation 1 = Planes assigned to this pipe are disabled.

Bit Range	Default & Access	Field Name (ID): Description
18	0x0 RW	**CURSOR_PLANES_OFF:** . This bit when set will cause all enabled cursor planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit, at the next VBLANK. Timing signals continue as they were but the screen becomes blank. Setting the bit back to a zero will then allow the cursor planes to resume on the following VBLANK. 0 = Normal Operation 1 = Planes assigned to this pipe are disabled.
17:16	0x0 RW	**REFRESH_RATE_CXSR_MODE_ASSOCIATION:** These bits select how refresh rates are tied to CxSR on pipe B. When they are set to anything other than 00, bits 23:21 of this register must be programmed to 0xx. Switching between 01 and 10 settings directly is not allowed. Software must program this field to 00 before switching. Software is responsible for enabling this mode only for integrated display panels that support corresponding mode. 00 Default no dynamic refresh rate change enabled. Software control only. 01 Progressive-to-progressive refresh rate change enabled and tied to CxSR. Pixel clock values set in FPB0/FPB1 settings in the DPLLB control register and FPB0/FPB1 divider registers. 10 Progressive-to-interlaced refresh rate change enabled and tied to CxSR. Pixel clock value does not change in this case. Scaling must be disabled in this mode. Uses programmable VS shift 11 Reserved
15	0x0 RW	**COLOR_CORRECTION_MATRIX_ENABLE_ON_PIPE_B:** 1 = Color Correction Coefficients are enabled to perform color correction 0 = Color Correction Coefficients are disabled
14	0x0 RW	**DISPLAYPORT_POWER_MODE_SWITCH_DEVVLVP:** This bit selects the software controlled progressive to progressive power saving mode (software controlled DRRS). Hardware Controlled Refresh Rate Select must be disabled when enabling this. Link and data M/N 1 values are used for normal settings, M/N 2 values are used for low power settings. 0 Normal progressive refresh rate (default) 1 Low Power progressive refresh rate
13	0x0 RW	**COLOR_RANGE_SELECT:** This bit is used to select the color range of RBG outputs. 0 = Apply full 0-255 color range to the output (Default) 1 = Apply 16-235 color range to the output
12	0x0 RW	**S3D_SPRITE_ORDER:** This bit controls the blending order of the sprite planes for S3D support: 0 = Sprite C first. The first line or pixel comes from Sprite C (default) 1 = Sprite D first. The first line or pixel comes from Sprite D
11:10	0x0 RW	**S3D_SPRITE_INTERLEAVING_FORMAT:** These bits control the Sprite C/D interleaving format in S3D mode 00 = No interleaving 01 = Line interleaving 10 = Pixel interleaving 11 = Reserved

Bit Range	Default & Access	Field Name (ID): Description
9:8	0x0 RO	**RESERVED_1:** MBZ Scrambling enable [DevCTG]: This bit enables scrambling for DisplayPort. Software must set this bit appropriately when enabling a DisplayPort output. 00 = Scrambling disabled (Default) 01 = Scrambling enabled, no SR after initialization at loop 2 of training 10 - RESERVED 11 = Scrambling and SR enabled. Scrambling is reset every 512 BS symbols.
7:5	0x0 RW	**BITS_PER_COLOR:** : This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change can be done independent of a pixel clock change. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. For further details on Display Port fixed frequency programming to accommodate these formats refer to DP Frequency Programming in DPLL section of Bspec. 000 = 8 bits per color (Default) 001 = 10 bits per color 010 = 6 bits per color 011 = RESERVED 1xx = RESERVED
4	0x0 RW	**DITHERING_ENABLE:** This bit enables dithering for DisplayPort 6bpc or 8bpc modes 0 Dithering disabled (Default) 1 Dithering enabled Programming Note: Dithering should only be enabled for 8bpc or 6bpc.
3:2	0x0 RW	**DITHERING_TYPE:** This bit selects dithering type for DisplayPort 6bpc or 8bpc modes 00 - Spatial only (default) 01- Spatio-Temporal 1 10- Spatio-Temporal 2 (testmode) 11- Temporal only (testmode)
1	0x0 RW	**DDA_RESET_TEST_MODE:** 0 Do not reset DDA 1 Reset DDA every 8th display frame
0	0x0 RO	**RESERVED_2:** Write as zero

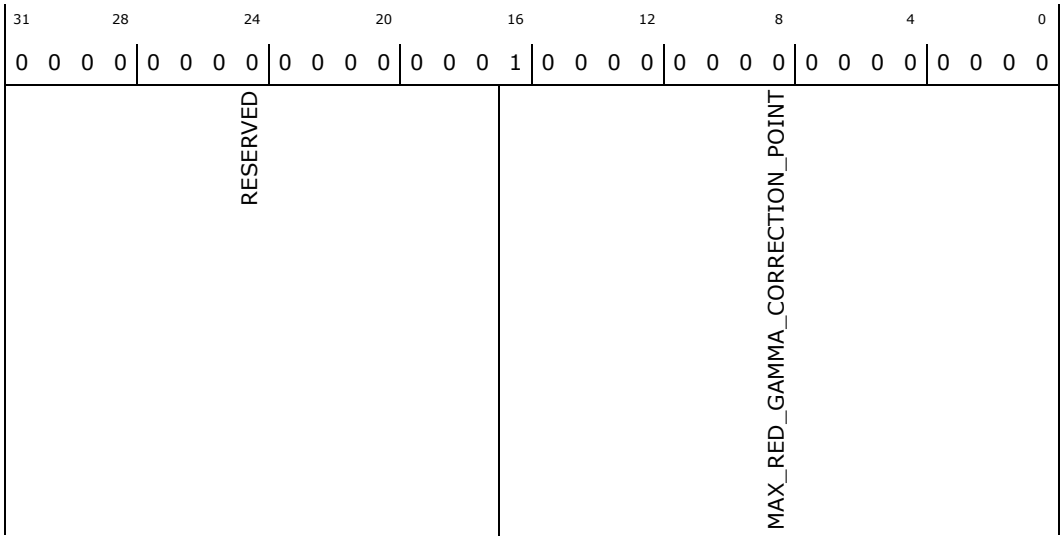
4.3.250 PIPEBGCMAXRED—Offset 71010h

Pipe B Gamma Correction Max Red

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 71010h

Default: 00010000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RESERVED:** Reserved.
16:0	0x10000 RW	**MAX_RED_GAMMA_CORRECTION_POINT:** . 129th reference point for red channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0.Format: 11.6 Default: 0x10000

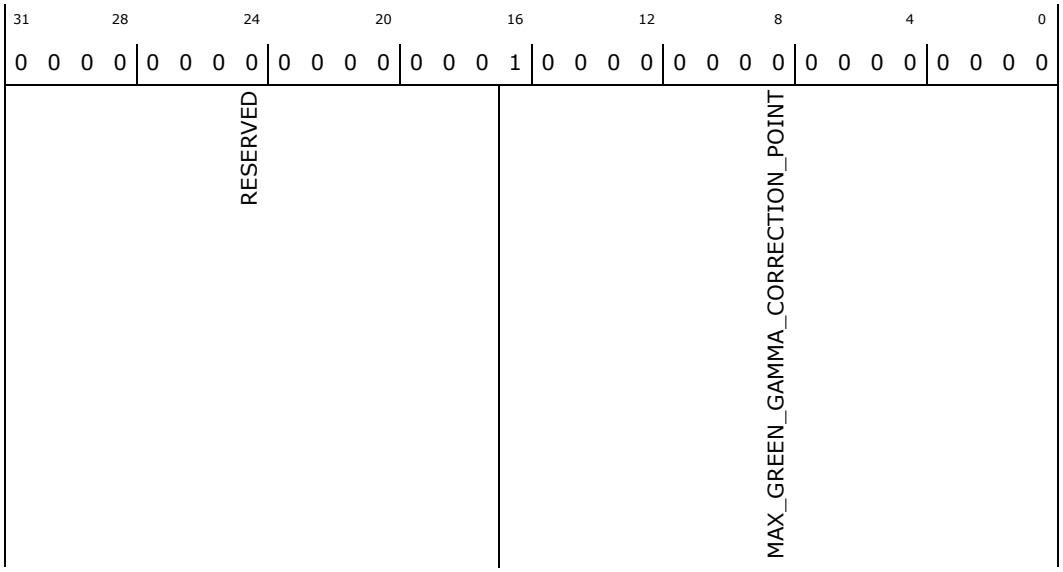
4.3.251 PIPEBGCMAXGREEN—Offset 71014h

Pipe B Gamma Correction Max Green

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 71014h

Default: 00010000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RESERVED:** Reserved.
16:0	0x10000 RW	**MAX_GREEN_GAMMA_CORRECTION_POINT:** . 129th reference point for green channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0.Format: 11.6 Default: 0x10000

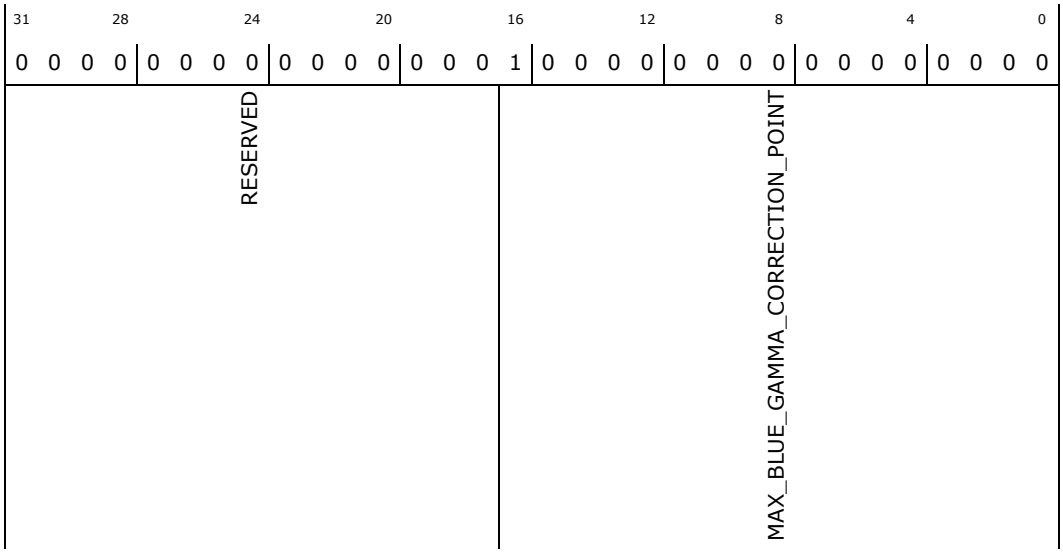
4.3.252 PIPEBGCMAXBLUE—Offset 71018h

Pipe B Gamma Correction Max Blue

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 71018h

Default: 00010000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RESERVED:** Reserved.
16:0	0x10000 RW	**MAX_BLUE_GAMMA_CORRECTION_POINT:** . 129th reference point for blue channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0.Format: 11.6 Default: 0x10000

4.3.253 PIPEBSTAT—Offset 71024h

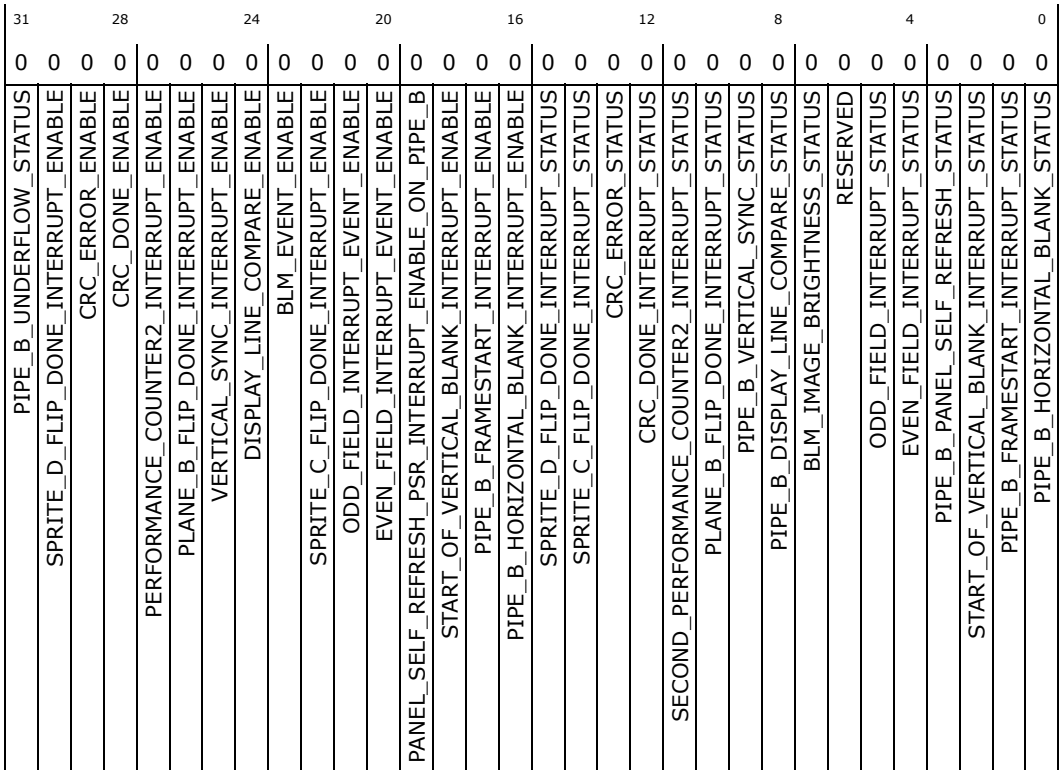
Pipe B Status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

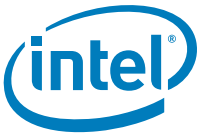
Offset: 71024h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C	**PIPE_B_UNDERFLOW_STATUS:** This bit is set when an underflow occurs at the display pipe B. It is cleared by writing a one to this bit. This event will occur naturally during mode changes, to be effective, it should be cleared after a mode change. This bit is only valid after Pipe B has been completely configured. 1 = FIFO B Underflow occurred 0 = FIFO B Underflow did not occur AccessType: One to Clear
30	0x0 RW	**SPRITE_D_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Sprite D flip done interrupt status bit in the first line interrupt logic 0 = Sprite D Flip Done Interrupt Disabled 1 = Sprite D Flip Done Interrupt Enabled
29	0x0 RW	**CRC_ERROR_ENABLE:** This will enable the consideration of the CRC error status bit in the first line interrupt/status logic. 0 = CRC Error Detect Disabled 1 = CRC Error Detect Enabled
28	0x0 RW	**CRC_DONE_ENABLE:** This will enable the consideration of the CRC done status bit in the first line interrupt/status logic. 0 = CRC Done Detect Disabled 1 = CRC Done Detect Enabled

Bit Range	Default & Access	Field Name (ID): Description
27	0x0 RW	**PERFORMANCE_COUNTER2_INTERRUPT_ENABLE:** This bit enables the second performance counter interrupt. 0 = Second Performance Counter2 Interrupt Status Disabled 1 = Second Performance Counter2 interrupt Status Enabled
26	0x0 RW	**PLANE_B_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Plane B flip done interrupt status bit in the first line interrupt logic 0 = Plane B flip done Interrupt/Status Disabled 1 = Plane B flip done Interrupt/Status Enabled
25	0x0 RW	**VERTICAL_SYNC_INTERRUPT_ENABLE:** 0 = Vertical Sync Interrupt/ Status Disabled 1 = Vertical Sync Interrupt/Status Enabled
24	0x0 RW	**DISPLAY_LINE_COMPARE_ENABLE:** 0 = Pipe B Display Line Compare Status Report Disabled 1 = Pipe B Display Line Compare Status report Enabled
23	0x0 RW	**BLM_EVENT_ENABLE:** This interrupt is generated by the image brightness segment comparators. Which segment cause an interrupt are controlled by the BLM Histogram control register. 0 = No BLM event enabled 1 = BLM event enabled
22	0x0 RW	**SPRITE_C_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Sprite C flip done interrupt status bit in the first line interrupt logic 0 = Sprite C Flip Done Interrupt Disabled 1 = Sprite C Flip Done Interrupt Enabled
21	0x0 RW	**ODD_FIELD_INTERRUPT_EVENT_ENABLE:** . This bit should only be used when this pipe is in an interlaced display timing.0 = Odd Field Event disable 1 = Odd Field Event enable
20	0x0 RW	**EVEN_FIELD_INTERRUPT_EVENT_ENABLE:** . This bit should only be used when this pipe is in an interlaced display timing.0 = Even field Event disable 1 = Even field Event enable
19	0x0 RW	**PANEL_SELF_REFRESH_PSR_INTERRUPT_ENABLE_ON_PIPE_B:** 0 = PSR interrupt Disabled on Pipe B 1 = PSR Interrupt Enabled on Pipe B
18	0x0 RW	**START_OF_VERTICAL_BLANK_INTERRUPT_ENABLE:** This will enable the consideration of the start of vertical blank interrupt status bit in the first line interrupt/status logic. 0 = Start of Vertical Blank Interrupt/Status Disabled 1 = Start of Vertical Blank Interrupt/Status Enabled
17	0x0 RW	**PIPE_B_FRAMESTART_INTERRUPT_ENABLE:** This will enable the consideration of the vertical blank interrupt status bit in the first line interrupt/status logic. 0 = Pipe B Framestart Interrupt/Status Disabled 1 = Pipe B Framestart Interrupt/Status Enabled



Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW	**PIPE_B_HORIZONTAL_BLANK_INTERRUPT_ENABLE:** This will enable the consideration of the start of horizontal blank interrupt status bit in the first line interrupt/status logic0 = Start of Horizontal Blank Interrupt/Status Disabled 1 = Start of Horizontal Blank Interrupt/Status Enabled
15	0x0 RW/1C	**SPRITE_D_FLIP_DONE_INTERRUPT_STATUS:** MMIO Flip Event is completed on Sprite D 0 = Sprite D Flip Not Done 1 = Sprite D Flip Done AccessType: One to Clear
14	0x0 RW/1C	**SPRITE_C_FLIP_DONE_INTERRUPT_STATUS:** MMIO Flip Event is completed on Sprite C 0 = Sprite C Flip Not Done 1 = Sprite C Flip Done AccessType: One to Clear
13	0x0 RW/1C	**CRC_ERROR_STATUS:** This bit is set when a Pipe B CRC error is detected. It is cleared by a write of a one. 0 = No CRC Error 1 = CRC Error detected AccessType: One to Clear
12	0x0 RW/1C	**CRC_DONE_INTERRUPT_STATUS:** This bit is set when Pipe B CRC calculation and compare are complete. It is cleared by a write of a one. 0 = CRC Not Done 1 = CRC Done AccessType: One to Clear
11	0x0 RW/1C	**SECOND_PERFORMANCE_COUNTER2_INTERRUPT_STATUS:** This bit is set when the second performance counter2 generates an interrupt. It is cleared by a write of a one. 0 = Second performance counter interrupt event not asserted 1 = Second performance counter interrupt event asserted AccessType: One to Clear
10	0x0 RW/1C	**PLANE_B_FLIP_DONE_INTERRUPT_STATUS:** Async/Sync Flip Event is completed on Display Plane B 0 = Plane B Flip Not Done 1 = Plane B Flip Done AccessType: One to Clear
9	0x0 RW/1C	**PIPE_B_VERTICAL_SYNC_STATUS:** 0 = Vertical Sync not asserted 1 = Vertical Sync asserted AccessType: One to Clear
8	0x0 RW/1C	**PIPE_B_DISPLAY_LINE_COMPARE_STATUS:** This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the value of the bit. 0 = Display Line Compare Status not asserted 1 = Display Line Compare Status asserted AccessType: One to Clear

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW/1C	**BLM_IMAGE_BRIGHTNESS_STATUS:** This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the value of the bit. 0 =DPST Interrupt has not occurred on pipe B 1 = DPST Interrupt has occurred on pipe B AccessType: One to Clear
6	0x0 RO	**RESERVED:** MBZ
5	0x0 RW/1C	**ODD_FIELD_INTERRUPT_STATUS:** . This status bit will be set on a Odd field VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates, the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set.Note: This bit will not be set when pipe is in Interlaced with Field 0 Only using legacy vertical sync shift mode. 0 = Odd Field Vertical Blank has not occurred 1 = Odd Field Vertical Blank has occurred AccessType: One to Clear
4	0x0 RW/1C	**EVEN_FIELD_INTERRUPT_STATUS:** . This status bit will be set on a even filed VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates, the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set.Note: This bit will not be set when pipe is in Interlaced with Field 0 Only using legacy vertical sync shift mode. 0 = Even Field Vertical Blank has not occurred 1 = Even Field Vertical Blank has occurred AccessType: One to Clear
3	0x0 RW/1C	**PIPE_B_PANEL_SELF_REFRESH_STATUS:** This bit indicates interrupt is generated by the PSR controller and intends to send interrupt to SW driver when the PSR interrupt enable bit (70028h bit 22) is set. This is cleared when a write to this register occurs with this bit as a one. Write with this bit as a zero has no effect on the value of the bit. 0 = PSR Interrupt has not occurred on pipe B 1 = PSR interrupt has occurred on pipe B AccessType: One to Clear
2	0x0 RW/1C	**START_OF_VERTICAL_BLANK_INTERRUPT_STATUS:** This status bit will be set at the beginning of a VBLANK event. At this point, the double buffered display registers flip, taking their new values. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. In MIPI DSR mode, GPIO TE trigger sets the Vblank Interrupt status 0 = Start of Vertical Blank has not occurred 1 = Start of Vertical Blank has occurred AccessType: One to Clear

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW/1C	**PIPE_B_FRAMESTART_INTERRUPT_STATUS:** This status bit will be set on a VBLANK event, when the frame start occurs. The display registers are updated at the start of vertical blank, but the new register data is not utilized by the display pipeline until the point in the vertical blank period when the frame start occurs, which is the event that triggers this bit. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. 0 = Pipe B Framestart Status has not occurred 1 = Pipe B Framestart Status has occurred AccessType: One to Clear
0	0x0 RW/1C	**PIPE_B_HORIZONTAL_BLANK_STATUS:** 0 = Pipe B Horizontal Blank has not occurred 1 = Pipe B Horizontal Blank has occurred AccessType: One to Clear

4.3.254 PIPEBFRAMECOUNT—Offset 71040h

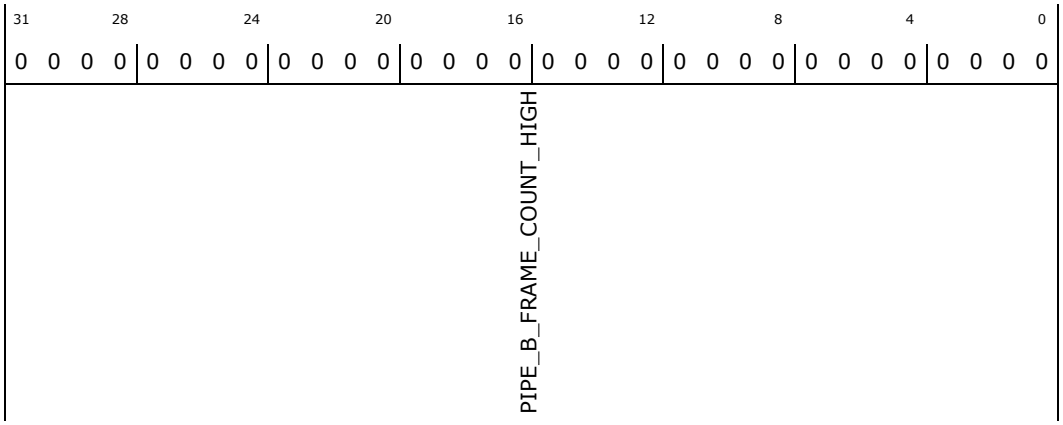
Pipe B Frame Count High

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 71040h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**PIPE_B_FRAME_COUNT_HIGH:** Refer PipeAFrameHigh description.

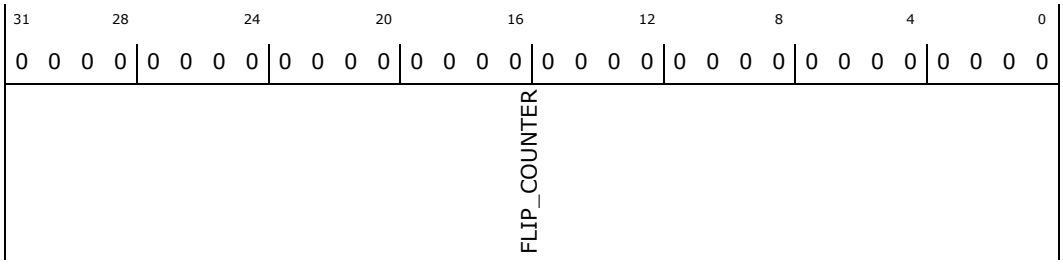
4.3.255 PIPEBFLIPCOUNT—Offset 71044h

Pipe B Flip count

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 71044h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**FLIP_COUNTER:** . Refer PipeAFlipCount description.

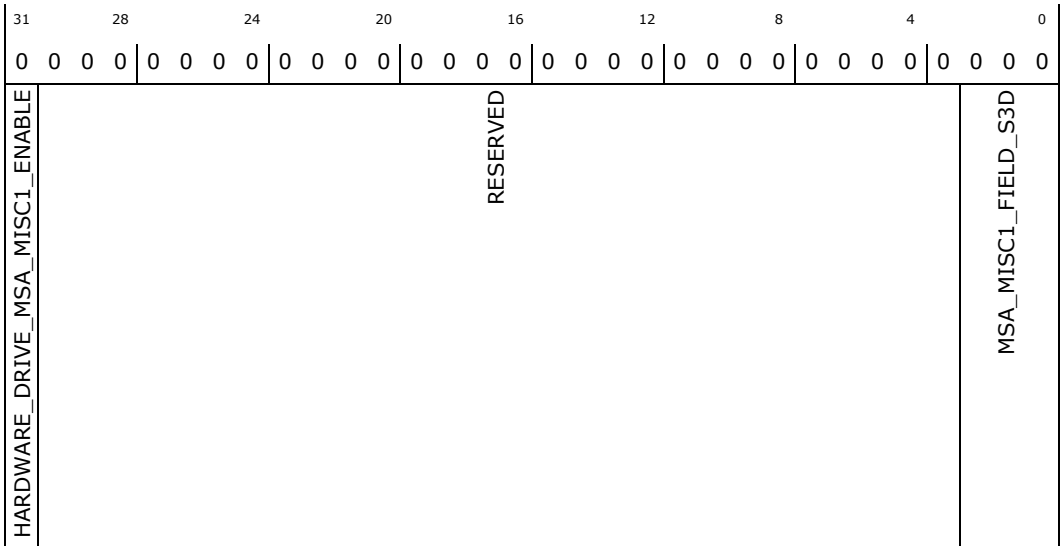
4.3.256 PIPEBMSAMISC—Offset 71048h

Pipe B MSA MISC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 71048h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**HARDWARE_DRIVE_MSA_MISC1_ENABLE:** This bit enables hardware to drive MSA MISC1 bit3:1 with the stereo 3D left/right eye field indication. Hardware will drive 000 when S3D mode is disabled, 001 when enabled and the upcoming video frame is right eye, 011 when enabled and the upcoming video frame is left eye. When this bit is disabled, software may manually program the MSA MISC1 Field S3D field in bit 2:0 in this register to set MISC1 bit 3:1 0 = Disable hardware driving MSA MISC1 bit 3:1. Allow software to manually program MSA MISC1 bit3:1 through MSA_MISC1_FIELD_S3D (default) 1 = Enable hardware to drive MSA MISC1 bit3:1 for S3D
30:3	0x0 RO	**RESERVED:** Reserved.
2:0	0x0 RW	**MSA_MISC1_FIELD_S3D:** This field provides software to manually program MSC1 stereo video attribute for DisplayPort: 000 = No stereo video transported 001 = For progressive video, the next (upcoming) video frame is RIGHT eye 010 = Reserved 011 = For progressive video, the next (upcoming) video frame is LEFT eye 100 = Stacked top and bottom top half represents left-eye view and bottom half represents right-eye view 101 = Stacked top and bottom top half represents right-eye view and bottom half represents left-eye view

4.3.257 DSPBADDR—Offset 7117Ch

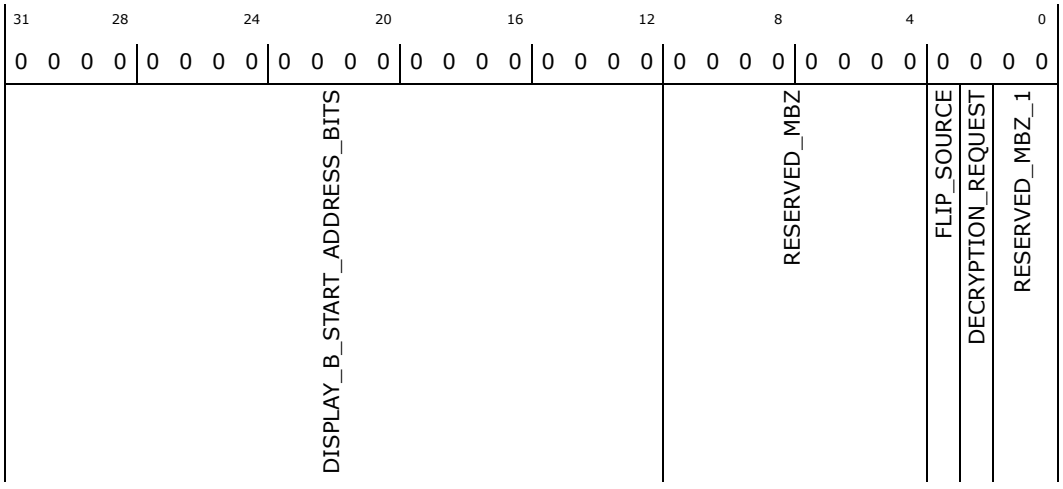
Display B Async flip Start Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 7117Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**DISPLAY_B_START_ADDRESS_BITS:** This register provides the start address of the display B plane or the first eye when running in stereo mode. This address must be at least pixel aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . Write to this register triggers async flip The async flip address is written into the Display B Base Address register 0x7119C
11:4	0x0 RO	**RESERVED_MBZ:** Reserved.
3	0x0 RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register.
1:0	0x0 RO	**RESERVED_MBZ_1:** Reserved.

4.3.258 DSPBCNTR—Offset 71180h

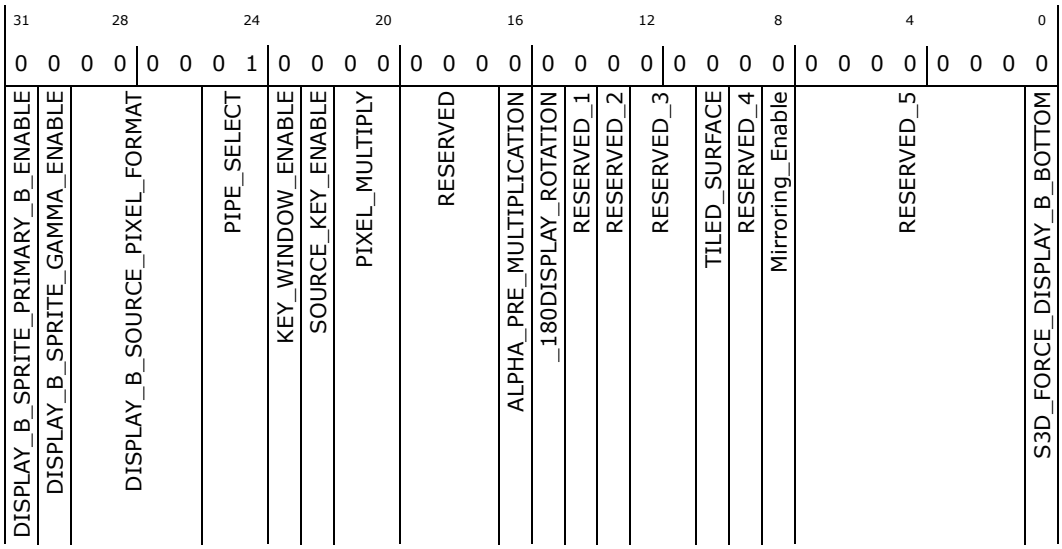
Display B/Sprite Plane Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 71180h

Default: 01000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**DISPLAY_B_SPRITE_PRIMARY_B_ENABLE:** This bit will enable or disable the display B/sprite. When this bit is set, the plane will generate pixels for display. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. 1 = Enable 0 = Disable
30	0x0 RW	**DISPLAY_B_SPRITE_GAMMA_ENABLE:** This bit should only be changed after the plane has been disabled. It controls the bypassing of the display pipe gamma unit for this display plane pixel data only. For 8-bit indexed display data, this bit should be set to a one. 0 = Display B pixel data bypasses the pipe gamma correction logic (default). 1 = Display B pixel data is gamma corrected in the pipe gamma correction logic
29:26	0x0 RW	**DISPLAY_B_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite/display B. Pixel formats with an alpha channel (8:8:8:8) should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 000x = Reserved. 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format. (with pre-multiplied alpha color format) 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format. (with pre-multiplied alpha color format) 1010 = 32-bit BGRX (10:10:10:2) pixel format Ignore alpha 1011 = 32-bit BGRA (10:10:10:2) pixel format (with pre-multiplied alpha color format) 1100 = 64-bit RGBX (16:16:16:16) 16 bit floating point pixel format. Ignore alpha. 1101 = 64-bit RGBA (16:16:16:16) 16-bit floating point pixel format (with pre-multiplied color format) 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8) pixel format (with pre-multiplied color format)
25:24	0x1 RO	**PIPE_SELECT:** Plane B always ties to Pipe B. Reserved AccessType: Read Only

Bit Range	Default & Access	Field Name (ID): Description
23	0x0 RW	**KEY_WINDOW_ENABLE:** This applies only to devices with a Display Plane C. It determines what area of the screen the source key compare should be applied. This bit is set to one when the color key is used as a destination key for display C. Display plane C must be enabled on the same pipe and display A should not be enabled on this pipe for this to be used. The function is only effective when display C is enabled and defined by Z-order to be behind display B. 0 = If keying is enabled, it applies to the entire display B plane 1 = If keying is enabled, it applies only to the intersection between display B and display C [DevBLC] and [DevCTG]: Reserved
22	0x0 RW	**SOURCE_KEY_ENABLE:** When used as a sprite or a secondary this enables source color keying. Sprite pixel values that match the key will become transparent. Source keying allows a plane that is behind (below) this plane to show through where the display B data matches the display B key. This function is overloaded to provide display C destination keying when combined with the key window enable bit.. Setting this bit is not allowed when the display pixel format includes an alpha channel. 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled. [DevBLC] and [DevCTG]: Reserved In destination keying, primary plane pixel will be made transparent when blending with sprite pixel as the destination if the primary src key matches with the primary pixel value.
21:20	0x0 RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. Asynchronous flips are not used in this mode. Programming Notes: Asynchronous flips are not permitted when pixel multiply is enabled. 00 = No duplication 01 = Line/pixel Doubling 10 = Reserved 11 = Pixel Doubling only
19:17	0x0 RO	**RESERVED:** Write as zero
16	0x0 RO	**ALPHA_PRE_MULTIPLICATION:** This Bit allows plane logic to alpha multiply ARGB/RGBA pizels if they are not pre multiplied already. 0: RGB Components are pre multiplied with alpha channel of the pixel. 1: RGB components have not been multiplied with alpha channel of the pixel. Plane will performed multiplication before alpha blending.
15	0x0 RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image. [DevCL] Do not enable 180 rotation together with Frame Buffer Compression 0 = No rotation 1 = 180 rotation

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RO	**RESERVED_1:** [DevBLC, DevCTG] Display B Trickle Feed Enable: 0 = Trickle Feed Enabled - Display B data requests are sent whenever there is space in the Display Data Buffer. 1 = Trickle Feed Disabled - Display B data requests are sent in bursts. Note: On mobile products this bit will be ignored such that Trickle Feed is always disabled. [DevELK] Must always be programmed disabled
13	0x0 RO	**RESERVED_2:** [DevBLC, DevCTG] Display B Data Buffer Partitioning Control: 0 = Display B Data Buffer will encompass Sprite B buffer space when Sprite B is disabled. 1 = Display B Data Buffer will not use Sprite B buffer space when Sprite B is disabled. Note: When in C3xR Max FIFO mode, this bit will be ignored.
12:11	0x0 RO	**RESERVED_3:** Reserved.
10	0x0 RW	**TILED_SURFACE:** This bit indicates that the display B surface data is in tiled memory. The tile pitch is specified in bytes in the DSPBSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPBLINOFF, DSPBTILEOFF, and DSPBSURF registers. 0 = Display B surface uses linear memory 1 = Display B surface uses X-tiled memory
9	0x0 RO	**RESERVED_4:** Write as zero [DevBLC, DevCTG] Asynchronous Surface Address Update Enable: This bit will enable asynchronous updates of the surface address when written by MMIO. The surface address will change with the next TLB request or when start of vertical blank is reached. Updates during vertical blank may not complete until after the first few active lines are displayed. Restrictions: No command streamer initiated surface address updates are allowed when this bit is enabled. Only one asynchronous update may be made per frame. Must wait for vertical blank before again writing the surface address register. 0 = DSPBSURF MMIO writes will update synchronous to start of vertical blank (default) 1 = DSPBSURF MMIO writes will update asynchronously
8	0x0 RO	**Mirroring_Enable:** 0: Mirroring is not enabled. 1: Mirroring is enabled.
7:1	0x0 RO	**RESERVED_5:** Write as zero
0	0x0 RW	**S3D_FORCE_DISPLAY_B_BOTTOM:** This bit will force the display B plane to be on the bottom of any sprite planes in the Z order. 0 = Display B Z-order is determined by the other control bits in pipe B 1 = Display B is forced to be on the bottom of any sprite planes in Z-order in pipe B

4.3.259 DSPBLINOFFSET—Offset 71184h

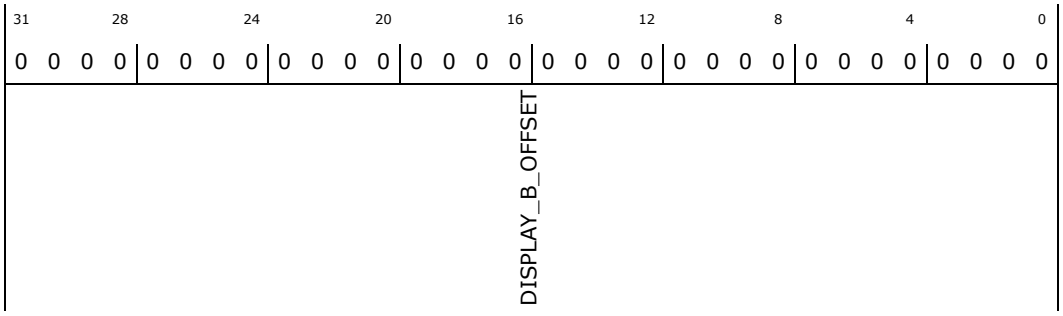
Display B/Sprite Linear Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 71184h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DISPLAY_B_OFFSET:** This register provides the panning offset into the display B plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

4.3.260 DSPBSTRIDE—Offset 71188h

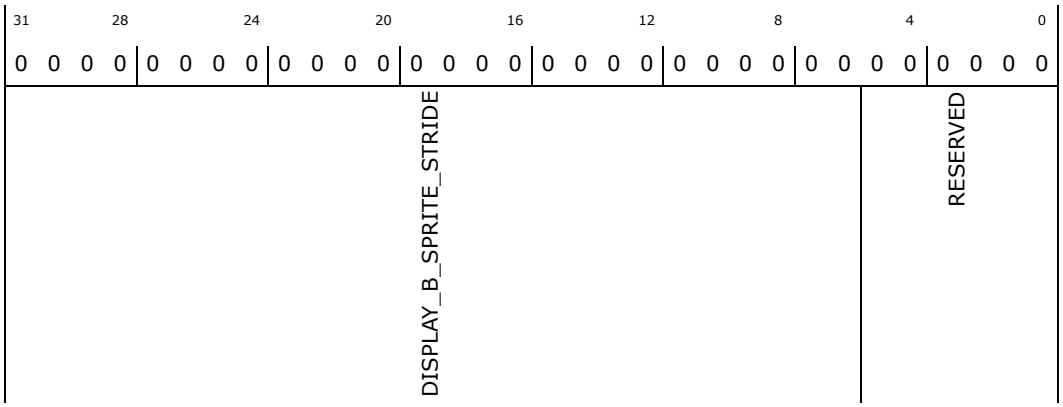
Display B/Sprite Stride Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 71188h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**DISPLAY_B_SPRITE_STRIDE:** This is the stride for display B/Sprite in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 512 byte aligned. The maximum value for this register is fixed. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes. The display stride must be power of 2 when doing Asynch Flips. The display stride must be 8KB or greater when doing Asynch Flips together with 180 rotation. The value in this register is updated through the command streamer during a synchronous flip.
5:0	0x0 RO	**RESERVED:** Reserved.

4.3.261 DSPBKEYVAL—Offset 71194h

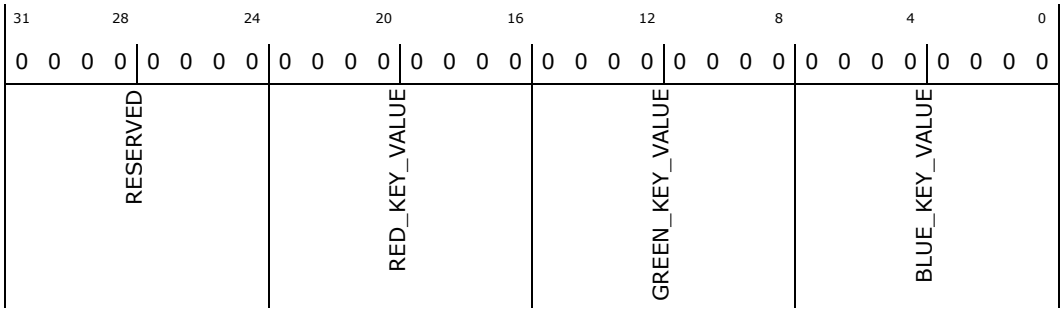
Sprite Color Key Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 71194h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x0 RW	**RED_KEY_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0x0 RW	**GREEN_KEY_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0x0 RW	**BLUE_KEY_VALUE:** Specifies the color key value for the sprite blue/Cb channel.

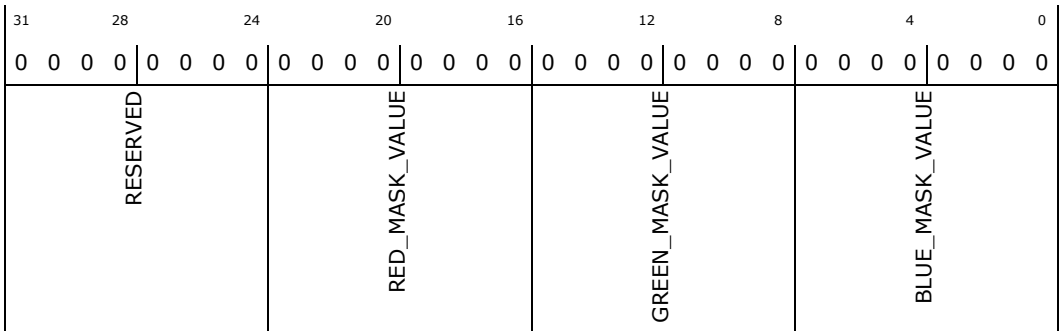
4.3.262 DSPBKEYMSK—Offset 71198h

Sprite Color Key Mask Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 71198h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x0 RW	**RED_MASK_VALUE:** Specifies the color key mask for the sprite red/Cr channel.
15:8	0x0 RW	**GREEN_MASK_VALUE:** Specifies the color key mask for the sprite green/Y channel.
7:0	0x0 RW	**BLUE_MASK_VALUE:** Specifies the color key mask for the sprite blue/Cb channel.

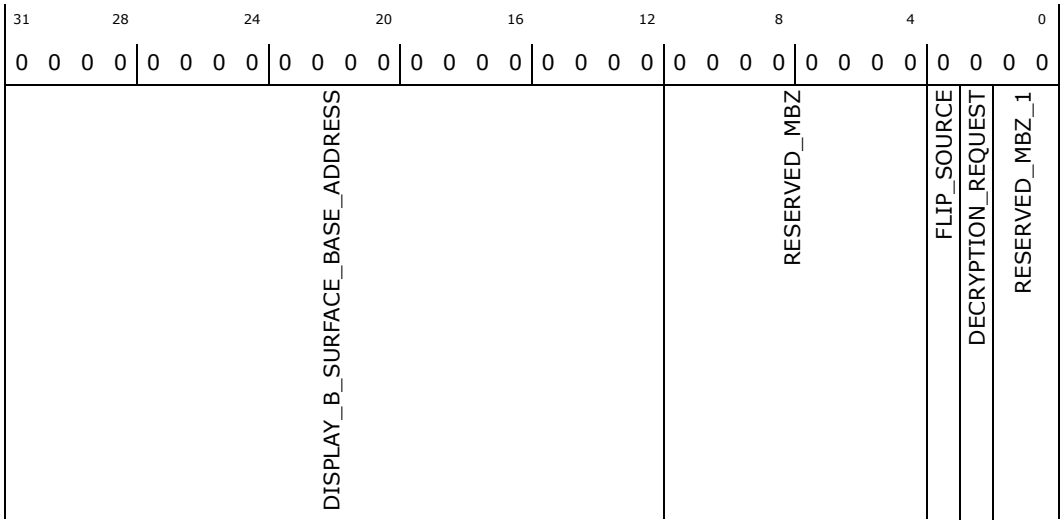
4.3.263 DSPBSURF—Offset 7119Ch

Display B Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7119Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**DISPLAY_B_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPBTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPBLINOFF register. This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0x0 RO	**RESERVED_MBZ:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0x0 RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register.
1:0	0x0 RO	**RESERVED_MBZ_1:** Reserved.

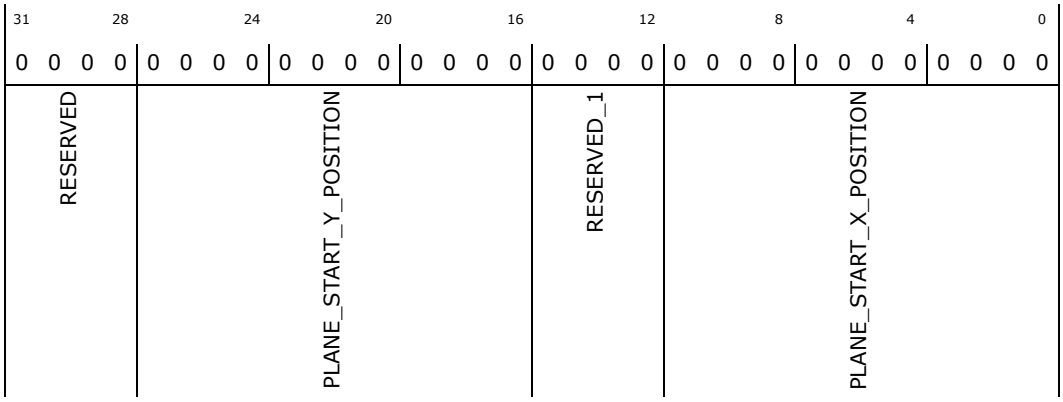
4.3.264 DSPBTILEOFF—Offset 711A4h

Display B Tiled Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 711A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation. When display stride is 16KB and doing Asynch Flips, do not program the offset to give pans of 7680 to 8191 bytes.

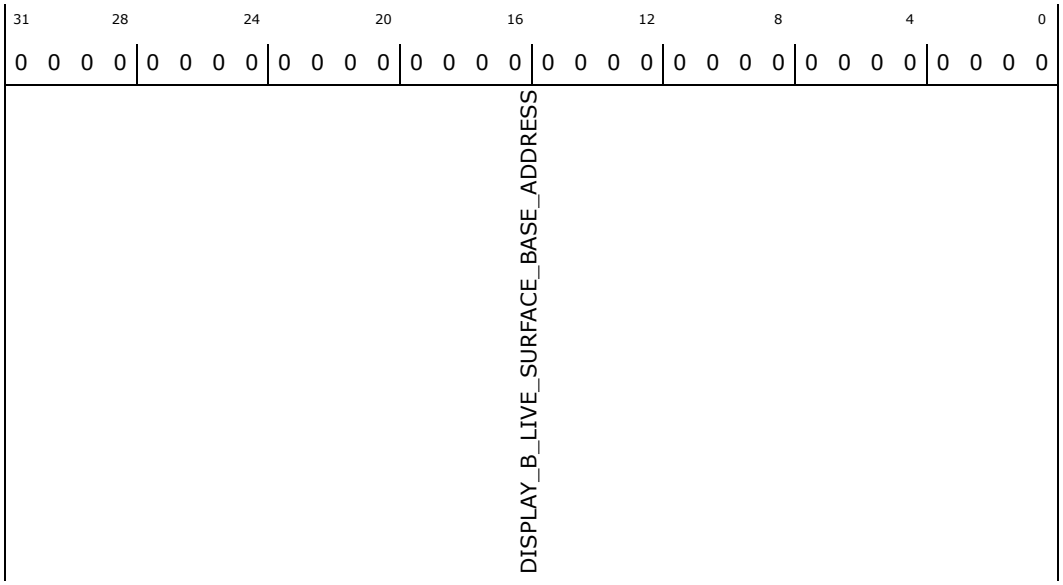
4.3.265 DSPBSURFLIVE—Offset 711ACh

Display B Live Surface Base Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 711ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**DISPLAY_B_LIVE_SURFACE_BASE_ADDRESS:** . This gives the live value of the surface base address as being currently used for the plane.

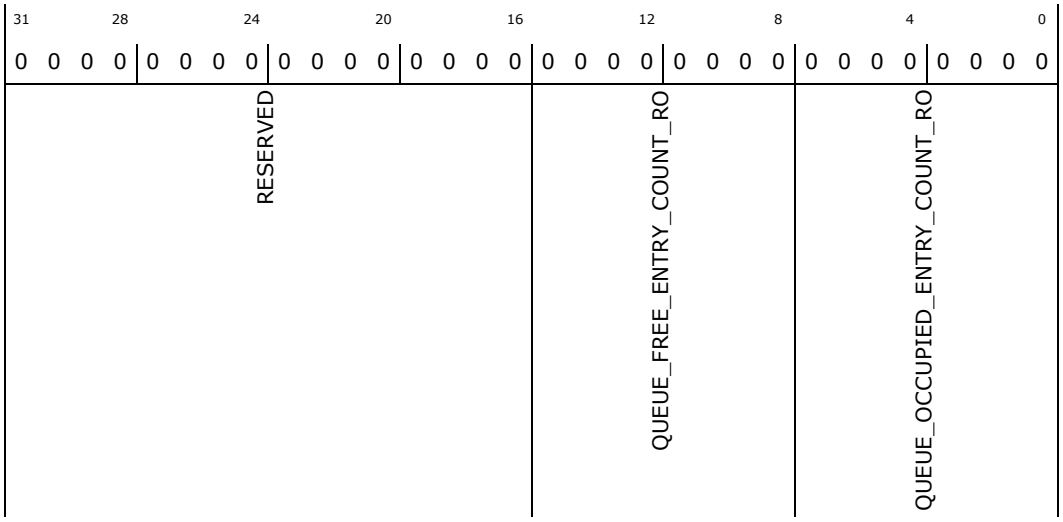
4.3.266 DSPBFLPQSTAT—Offset 71200h

Flip Queue Status Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 71200h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Write as zero (RO)
15:8	0x0 RO	**QUEUE_FREE_ENTRY_COUNT_RO:** This value indicates the number of free entries in the queue at the time that the register was read. The total number of entries in the queue is the sum of the occupied entry count and the free entry count.
7:0	0x0 RO	**QUEUE_OCCUPIED_ENTRY_COUNT_RO:** This value indicates the number of occupied entries in the queue at the time that the register was read. The total number of entries in the queue is the sum of the occupied entry count and the free entry count.

4.3.267 SWF10—Offset 71410h

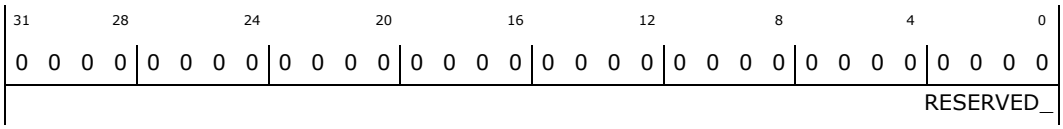
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 71410h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

4.3.268 SWF11—Offset 71414h

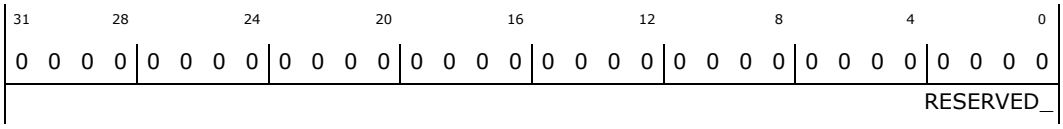
Software Flag Registers

Access Method

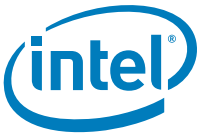
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 71414h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers



4.3.269 SWF12—Offset 71418h

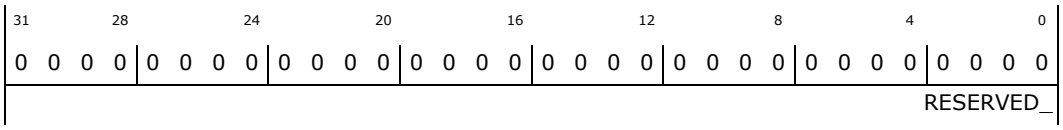
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 71418h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

4.3.270 SWF13—Offset 7141Ch

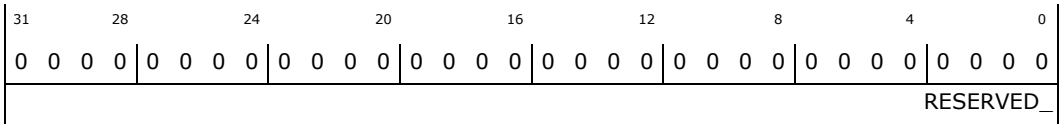
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 7141Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

4.3.271 SWF14—Offset 71420h

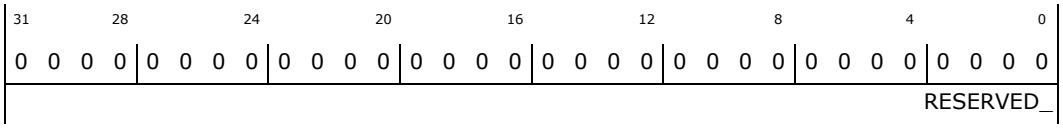
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 71420h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

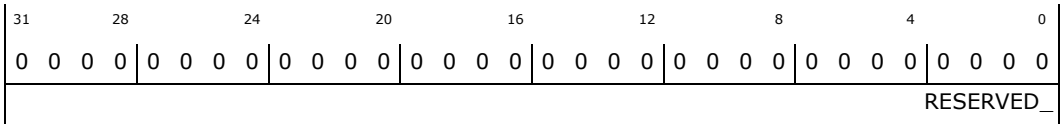
4.3.272 SWF15—Offset 71424h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 71424h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

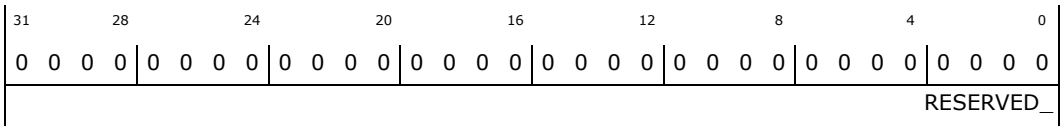
4.3.273 SWF16—Offset 71428h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 71428h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

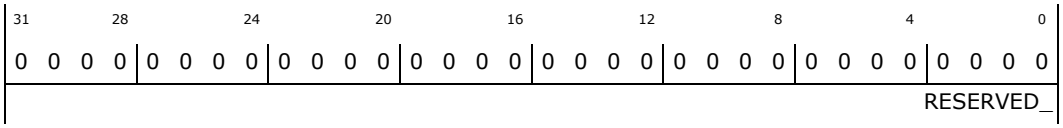
4.3.274 SWF17—Offset 7142Ch

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7142Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

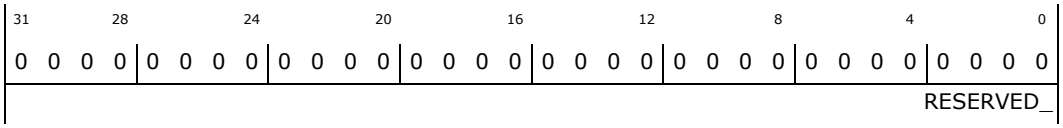
4.3.275 SWF18—Offset 71430h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 71430h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

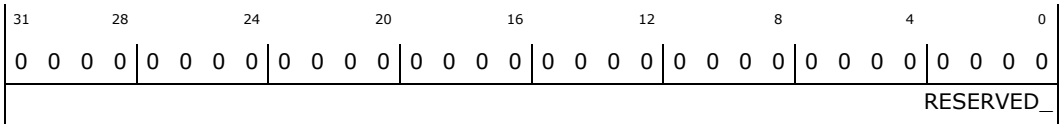
4.3.276 SWF19—Offset 71434h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 71434h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

4.3.277 SWF1A—Offset 71438h

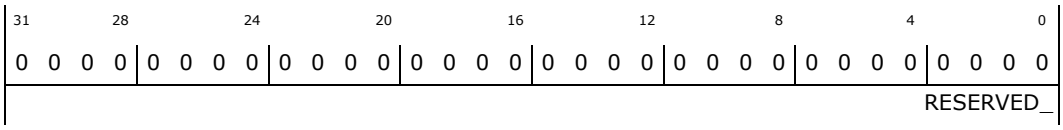
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 71438h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

4.3.278 SWF1B—Offset 7143Ch

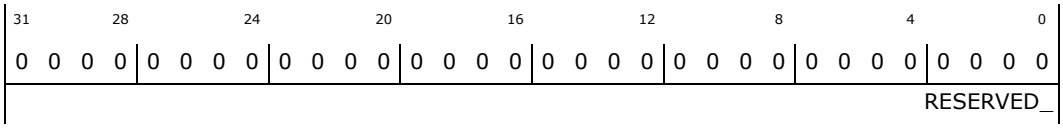
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 7143Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

4.3.279 SWF1C—Offset 71440h

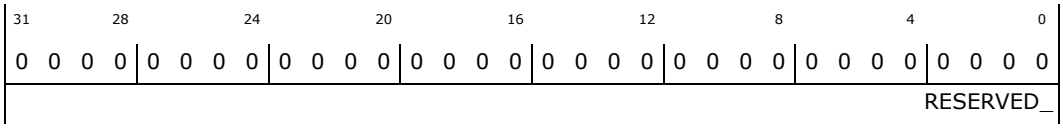
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 71440h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

4.3.280 SWF1D—Offset 71444h

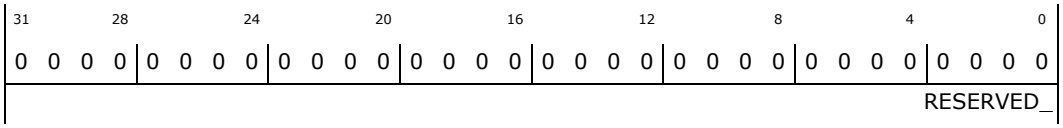
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 71444h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

4.3.281 SWF1E—Offset 71448h

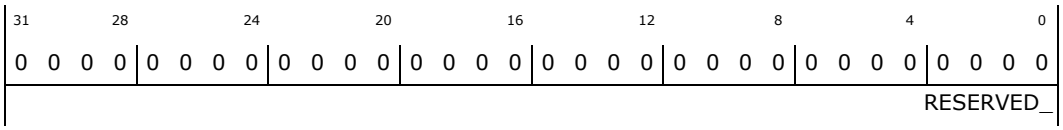
Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 71448h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

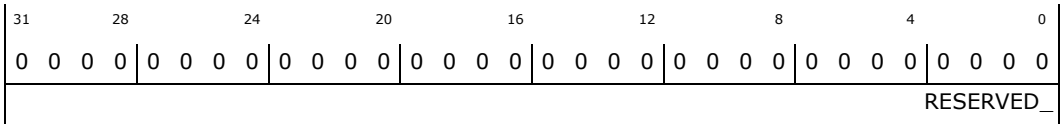
4.3.282 SWF1F—Offset 7144Ch

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7144Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

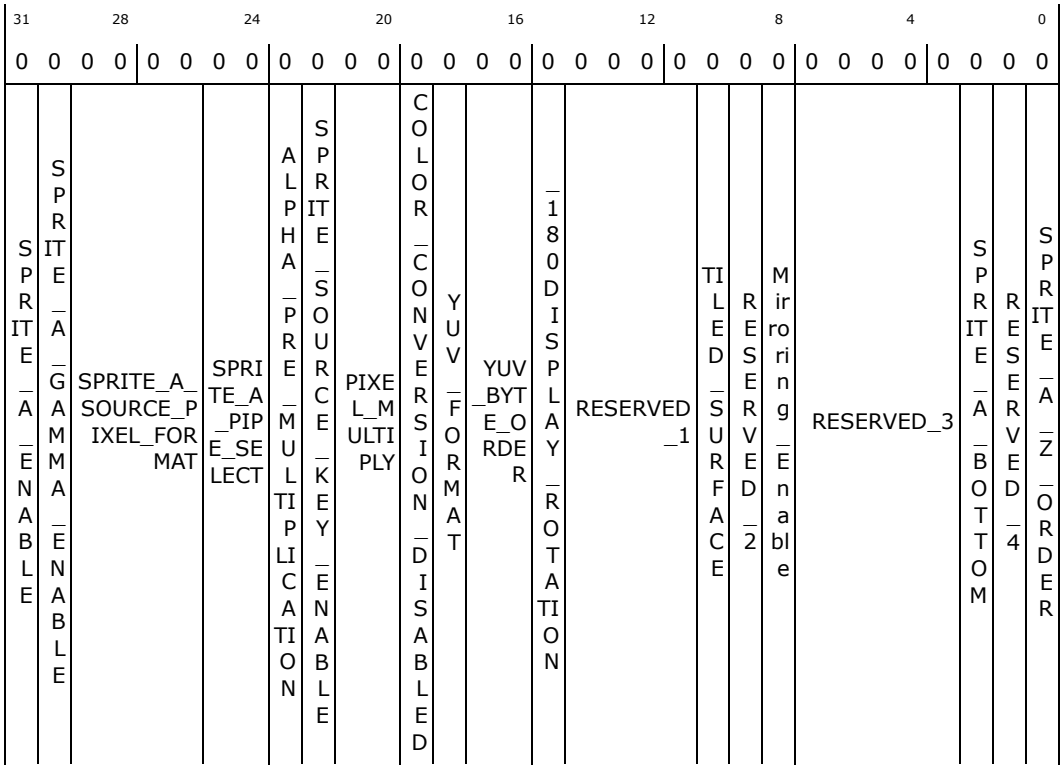
4.3.283 SPACNTR—Offset 72180h

Sprite A Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72180h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SPRITE_A_ENABLE:** This bit will enable or disable the Sprite A. When this bit is set, the plane will generate pixels for display to be combined by the blender for the target pipe. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted, this bit will be overridden and the display disabled when the registers are unlocked. 1 = Enable 0 = Disable
30	0x0 RW	**SPRITE_A_GAMMA_ENABLE:** There are two gamma adjustments possible in the Sprite A data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8-bit indexed, this bit should be set to a one. Gamma correction logic that is contained in the Sprite A logic is disabled by loading the default values into those registers. When this plane is marked as trusted, this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 = Sprite A pixel data bypasses the display pipe gamma correction logic (default). 1 = Sprite A pixel data is gamma corrected in the pipe gamma correction logic
29:26	0x0 RW	**SPRITE_A_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite/Sprite A. Pixel formats with an alpha channel should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 0000 = YUV 4:2:2 packed (see byte order below). 0001 = Reserved 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format with pre-multiplied alpha channel. 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format 1010 = Reserved. 1011 = Reserved. 1100 = Reserved. 1101 = Reserved. 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8)
25:24	0x0 RW	**SPRITE_A_PIPE_SELECT:** Sprite A always ties to pipe A. Reserved.
23	0x0 RO	**ALPHA_PRE_MULTIPLICATION:** This Bit allows plane logic to alpha multiply ARGB/RGBA pizels if they are not pre multiplied already. 0: RGB Components are pre multiplied with alpha channel of the pixel. 1: RGB components have not been multiplied with alpha channel of the pixel. Plane will performed multiplication before alpha blending.

Bit Range	Default & Access	Field Name (ID): Description
22	0x0 RW	**SPRITE_SOURCE_KEY_ENABLE:** When used as a sprite in the 16/32-bpp modes without alpha this enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Setting this bit is not allowed when the Sprite A pixel format includes an alpha channel. [DevBW] Erratum: This bit must always be set to 0 when Sprite A pixel format is YUV 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled. Each sprite has built in source keying enabled/disabled. If the source keying is disabled and no alpha blending is enabled, the pixels are tagged as opaque. If sprite source keying is enabled and no alpha blending is enabled, it works as follows: For YUV sprite data, each yuv channel data is compared with the corresponding channel s key color Low and High (each channel inrange can be masked out). If all three channels are in range between the low and high key values, it is considered source compared. For RGB sprite data, each 24-bit RGB pixel data is compared with the 24-bit key value (note it only uses the 24-bit Low key value for comparison). Each 24-bit has to be equal (each bit comparison can also be masked out) for the source compared. If the sprite source data compare and matches, then the sprite data will be tagged as transparent when blending with its destination pixel. If the sprite source data does not compare, then the sprite data will be tagged as opaque when blending with its destination pixel.
21:20	0x0 RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two (both H and V). 00 = No line/Pixel duplication 01 = Line/Pixel Doubling 10 = Line Doubling only 11 = Pixel Doubling only
19	0x0 RW	**COLOR_CONVERSION_DISABLED:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4:2:2 packed format and x:8:8:8 and 8:8:8:8 formats. Formats such as RGB5:5:5 and 5:6:5 do not have YUV versions. 0 = Pixel data is sent through the conversion logic (only applies to YUV formats) 1 = Pixel data is not sent through the YUV-)RGB conversion logic.
18	0x0 RW	**YUV_FORMAT:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 = ITU-R Recommendation BT.601 1 = ITU-R Recommendation BT.709
17:16	0x0 RW	**YUV_BYTE_ORDER:** This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored. 00 = YUYV 01 = UYVY 10 = YVYU 11 = VYUY

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner. 0 = No rotation 1 = 180 rotation
14:11	0x0 RO	**RESERVED_1:** Reserved.
10	0x0 RW	**TILED_SURFACE:** This bit indicates that the Sprite A surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPCTILEOFF, DSPCLINOFF, and DSPCSURFADDR registers. 0 = Sprite A surface uses linear memory 1 = Sprite A surface uses X-tiled memory
9	0x0 RO	**RESERVED_2:** Write as zero
8	0x0 RO	**Mirroring_Enable:** 0: Mirroring is not enabled. 1: Mirroring is enabled.
7:3	0x0 RO	**RESERVED_3:** Write as zero
2	0x0 RW	**SPRITE_A_BOTTOM:** This bit will force the Sprite A plane to be on the bottom of the Z order. If the plane is marked as trusted, it only applies to the Z order of the trusted planes. 0 = Sprite A Z order is determined by the other control bits 1 = Sprite A is forced to be on the bottom of the Z order.
1	0x0 RO	**RESERVED_4:** Reserved.
0	0x0 RW	**SPRITE_A_Z_ORDER:** With Sprite A and B z-order, bottom control bits, Sprite A plane is placed in a specific z-order among other planes. Display Pipe A Z-orders SA zorderSA bottomSB zorderSB bottomResulting Pipe Z-order (from bottom to top)Source Keying 0000PA SA SB CAPA in Black 1000PA SB SA CAPA in Black 0001SB PA SA CAuse src keying on SB 0011SB PA SA CAuse src keying on SB 1001SB SA PA CAuse src keying on SA 1011SB SA PA CAuse src keying on SA 0100SA PA SB CAuse src keying on SA 1100SA PA SB CAuse src keying on SA 0110SA SB PA CAuse src keying on SB 1110SA SB PA CAuse src keying on SB 0: Sprite A z-order is disabled 1: Sprite A z-order is enabled

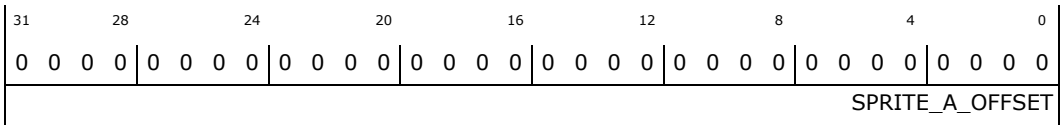
4.3.284 SPALINOFF—Offset 72184h

Sprite A Linear Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72184h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SPRITE_A_OFFSET:** This register provides the panning offset into the Sprite A plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

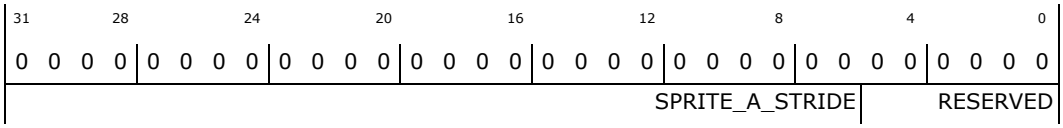
4.3.285 SPASTRIDE—Offset 72188h

Sprite A Stride Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72188h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**SPRITE_A_STRIDE:** This is the stride for Sprite A in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.
5:0	0x0 RO	**RESERVED:** Reserved.

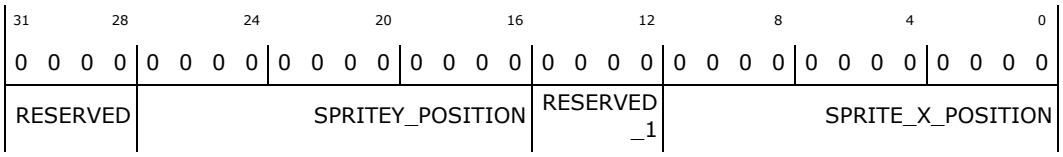
4.3.286 SPAPOS—Offset 7218Ch

Sprite A Position Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7218Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**SPRITEY_POSITION:** These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**SPRITE_X_POSITION:** These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180 rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

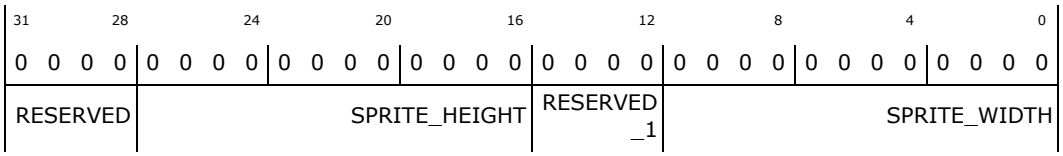
4.3.287 SPASIZE—Offset 72190h

Sprite A Height and Width Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72190h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**SPRITE_HEIGHT:** This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**SPRITE_WIDTH:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values when YUV source pixel format is used (actual width, not the width minus one value).

4.3.288 SPAKEYMINVAL—Offset 72194h

Sprite A Color Key Min Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 72194h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0 | 0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RESERVED	RED_KEY_MIN_VALUE			GREEN_KEY_MIN_VALUE		BLUE_KEY_MIN_VALUE	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero
23:16	0x0 RW	**RED_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite red/Cr channel.
15:8	0x0 RW	**GREEN_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite green/Y channel.
7:0	0x0 RW	**BLUE_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite blue/Cb channel.

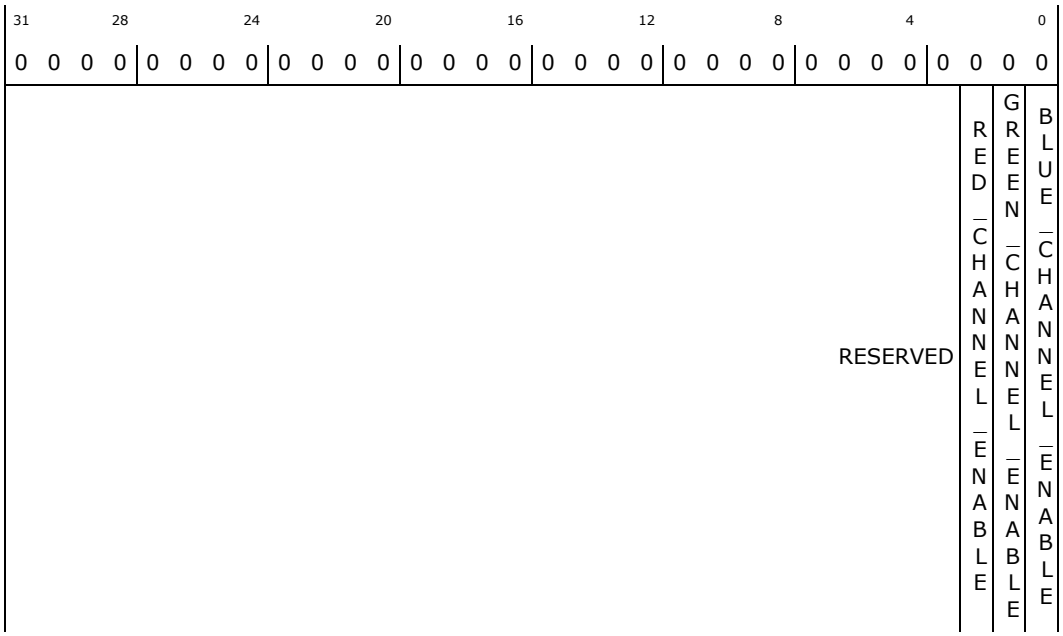
4.3.289 SPAKEYMSK—Offset 72198h

Sprite A Color Key Mask Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72198h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**RESERVED:** Write as zero
2	0x0 RW	**RED_CHANNEL_ENABLE:** Specifies the source color key enable for the red/Cr channel.
1	0x0 RW	**GREEN_CHANNEL_ENABLE:** Specifies the source color key enable for the green/Y channel.
0	0x0 RW	**BLUE_CHANNEL_ENABLE:** Specifies the source color key enable for the blue/Cb channel

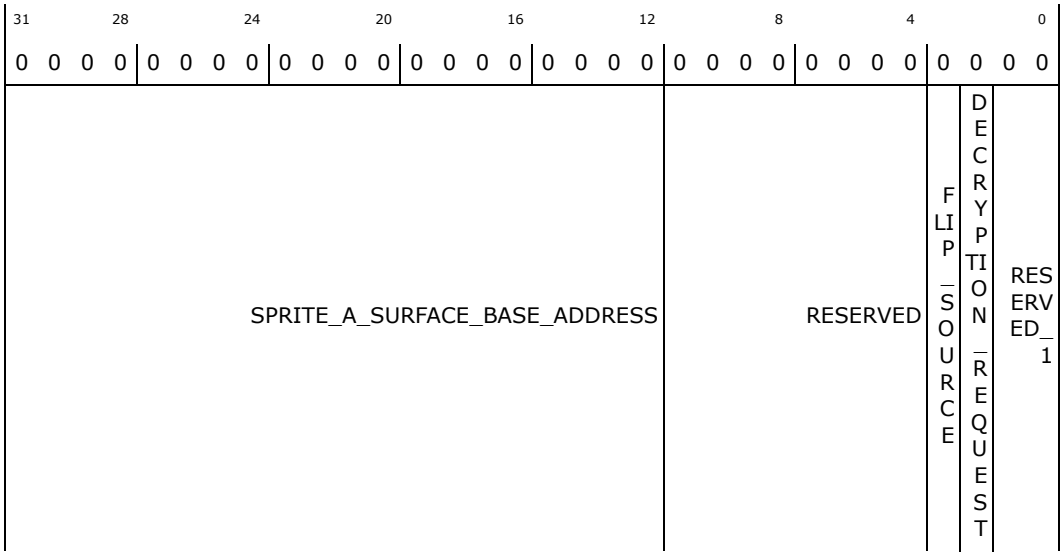
4.3.290 SPASURF—Offset 7219Ch

Sprite A Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7219Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**SPRITE_A_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register. This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . The value in this register is updated through the command streamer during synchronous flips. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0x0 RO	**RESERVED:** MBZ

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0x0 RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0x0 RO	**RESERVED_1:** MBZ

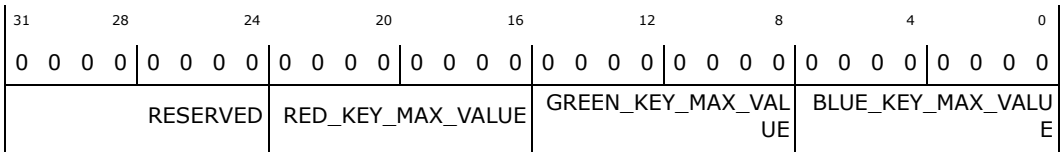
4.3.291 SPAKEYMAXVAL—Offset 721A0h

Sprite A Color Key Max Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 721A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero
23:16	0x0 RW	**RED_KEY_MAX_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0x0 RW	**GREEN_KEY_MAX_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0x0 RW	**BLUE_KEY_MAX_VALUE:** Specifies the color key value for the sprite blue/Cb channel.

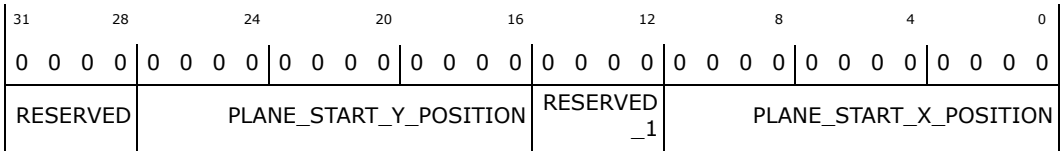
4.3.292 SPATILEOFF—Offset 721A4h

Sprite A Tiled Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 721A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

4.3.293 SPACONTALPHA—Offset 721A8h

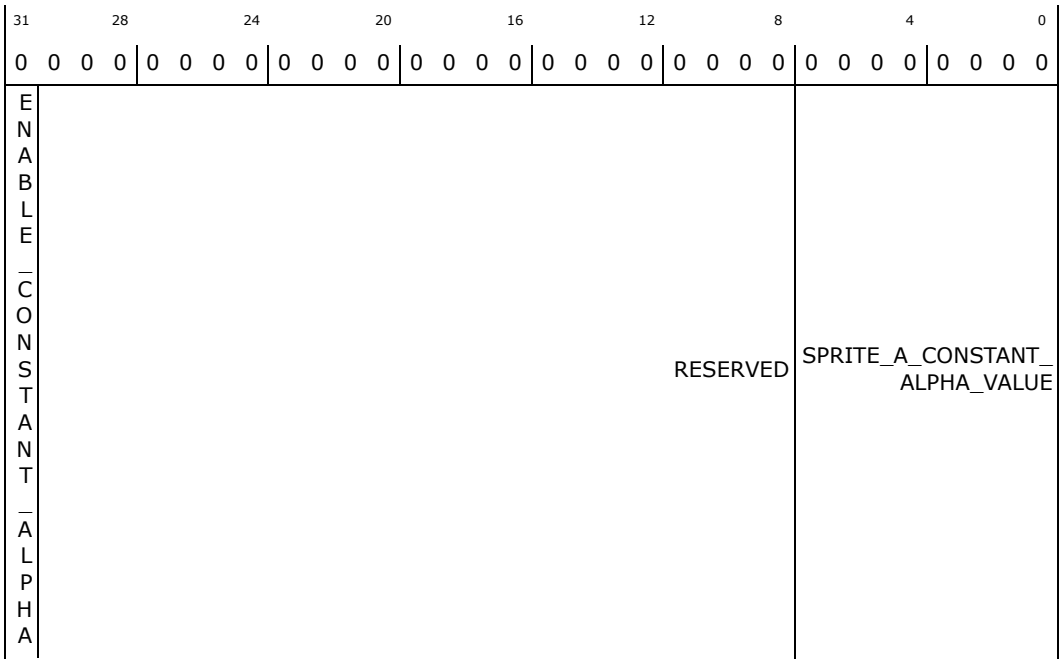
Sprite A Constant Alpha Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 721A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**ENABLE_CONSTANT_ALPHA:** Sprite A Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 Sprite A Sprite Constant Alpha is disabled 1 Sprite A Sprite Constant Alpha is enabled

Bit Range	Default & Access	Field Name (ID): Description
30:8	0x0 RO	**RESERVED:** MBZ
7:0	0x0 RW	**SPRITE_A_CONSTANT_ALPHA_VALUE:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

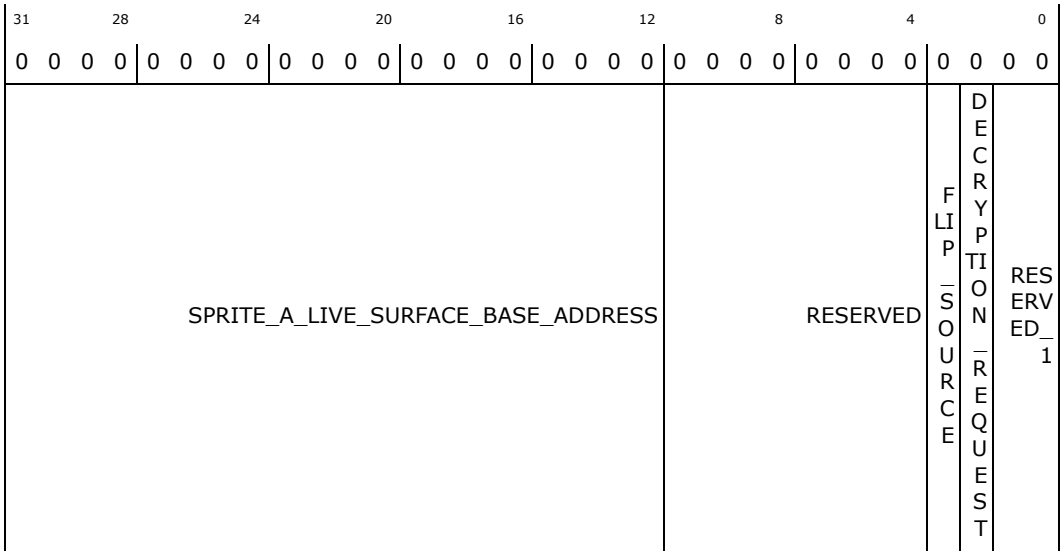
4.3.294 SPALIVESURF—Offset 721ACh

Sprite A Live Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 721ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**SPRITE_A_LIVE_SURFACE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for the Sprite A plane.
11:4	0x0 RO	**RESERVED:** MBZ

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RO	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0x0 RO	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0x0 RO	**RESERVED_1:** MBZ

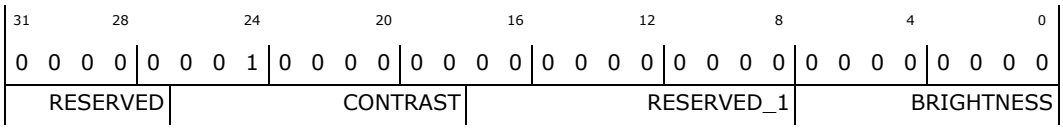
4.3.295 SPACLRC0—Offset 721D0h

Sprite A Color Correction 0 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 721D0h

Default: 01000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** Reserved.
26:18	0x40 RW	**CONTRAST:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed-point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast, for YUV modes and for source data in RGB format, is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	0x0 RO	**RESERVED_1:** Reserved.
7:0	0x0 RW	**BRIGHTNESS:** This field provides the brightness adjustment with a 8-bit 2 s compliment value ranging [-128, +127]. This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8-bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of [-255, +255]. Bypassing Brightness for YUV formats and for source data in RGB format, is accomplished by programming this field to 0.

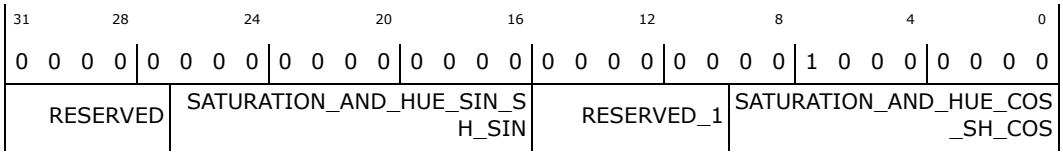
4.3.296 SPACLRC1—Offset 721D4h

Sprite A Color Correction 1 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 721D4h

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** Reserved.
26:16	0x0 RW	**SATURATION_AND_HUE_SIN_SH_SIN:** This 11-bit signed fixed-point number is in 2 s compliment (s3i.7f) format with the MSB as the sign, next 3 MSBs as the integer value and the last 7 LSBs as the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Hue, even for source data in RGB format, is accomplished by programming this field to 0.0.
15:10	0x0 RO	**RESERVED_1:** Reserved.
9:0	0x80 RW	**SATURATION_AND_HUE_COS_SH_COS:** This unsigned fixed-point number is in 3i.7f format with the first 3 MSBs be the integer value and the last 7 LSBs be the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Saturation, even for source data in RGB format, is accomplished by programming this field to 1.0.

4.3.297 SPAGAMC5—Offset 721E0h

Sprite A Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 721E0h

Default: 00C0C0C0h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	1 1 0 0	0 0 0 0	1 1 0 0	0 0 0 0	1 1 0 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0xc0 RW	**RED_V_CR:** Reserved.
15:8	0xc0 RW	**GREEN_Y:** Reserved.
7:0	0xc0 RW	**BLUE_U_CB:**

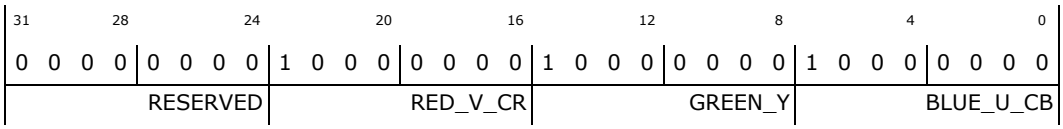
4.3.298 SPAGAMC4—Offset 721E4h

Sprite A Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 721E4h

Default: 00808080h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x80 RW	**RED_V_CR:** Reserved.
15:8	0x80 RW	**GREEN_Y:** Reserved.
7:0	0x80 RW	**BLUE_U_CB:**

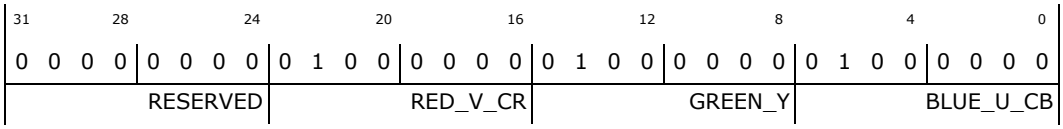
4.3.299 SPAGAMC3—Offset 721E8h

Sprite A Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 721E8h

Default: 00404040h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x40 RW	**RED_V_CR:** Reserved.
15:8	0x40 RW	**GREEN_Y:** Reserved.
7:0	0x40 RW	**BLUE_U_CB:**

4.3.300 SPAGAMC2—Offset 721ECh

Sprite A Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 721ECh

Default: 00202020h

31 28	24	20	16	12	8	4 0
0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 1 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x20 RW	**RED_V_CR:** Reserved.
15:8	0x20 RW	**GREEN_Y:** Reserved.
7:0	0x20 RW	**BLUE_U_CB:**

4.3.301 SPAGAMC1—Offset 721F0h

Sprite A Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 721F0h

Default: 00101010h

31 28	24	20	16	12	8	4 0
0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x10 RW	**RED_V_CR:** Reserved.
15:8	0x10 RW	**GREEN_Y:** Reserved.
7:0	0x10 RW	**BLUE_U_CB:**

4.3.302 SPAGAMC0—Offset 721F4h

Sprite A Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 721F4h

Default: 00080808h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	1 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x8 RW	**RED_V_CR:** Reserved.
15:8	0x8 RW	**GREEN_Y:** Reserved.
7:0	0x8 RW	**BLUE_U_CB:**

4.3.303 SPBCNTR—Offset 72280h

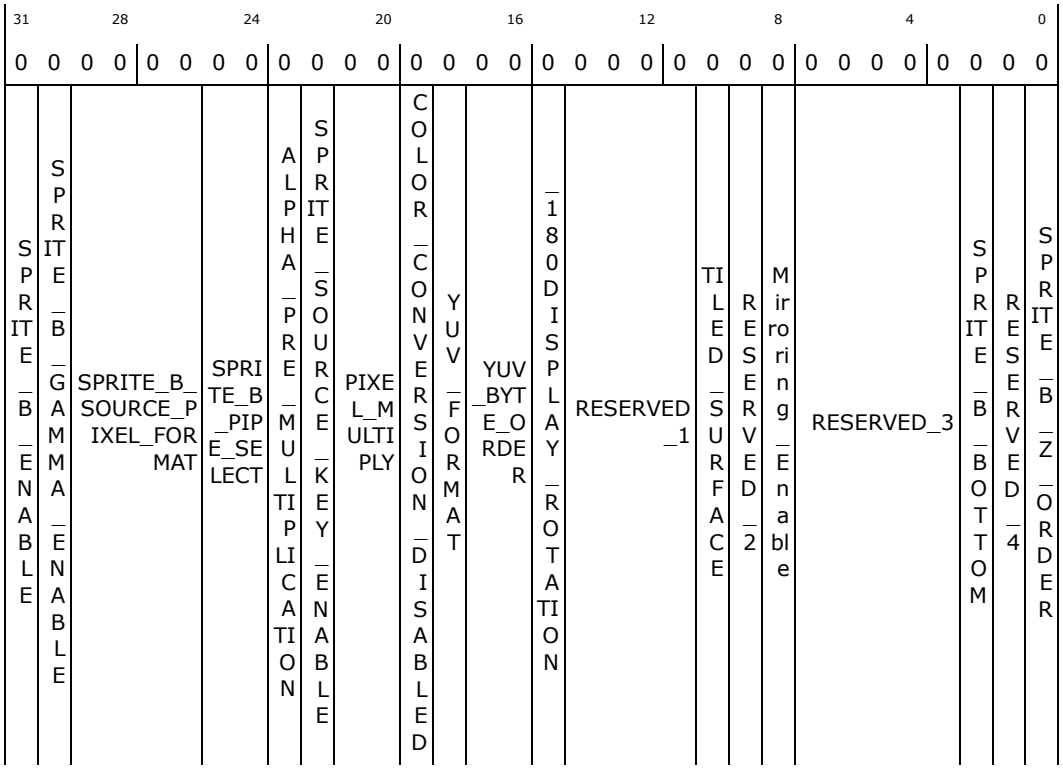
Sprite B Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 72280h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SPRITE_B_ENABLE:** This bit will enable or disable the Sprite B. When this bit is set, the plane will generate pixels for display to be combined by the blender for the target pipe. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted, this bit will be overridden and the display disabled when the registers are unlocked. 1 = Enable 0 = Disable
30	0x0 RW	**SPRITE_B_GAMMA_ENABLE:** There are two gamma adjustments possible in the Sprite B data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8-bit indexed, this bit should be set to a one. Gamma correction logic that is contained in the Sprite B logic is disabled by loading the default values into those registers. When this plane is marked as trusted, this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 = Sprite B pixel data bypasses the display pipe gamma correction logic (default). 1 = Sprite B pixel data is gamma corrected in the pipe gamma correction logic

Bit Range	Default & Access	Field Name (ID): Description
29:26	0x0 RW	**SPRITE_B_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite/Sprite B. Pixel formats with an alpha channel should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 0000 = YUV 4:2:2 packed (see byte order below). 0001 = Reserved 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format with pre-multiplied alpha channel. 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format 1010 = Reserved. 1011 = Reserved. 1100 = Reserved. 1101 = Reserved. 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8)
25:24	0x0 RW	**SPRITE_B_PIPE_SELECT:** Sprite B always ties to Pipe A. Reserved
23	0x0 RO	**ALPHA_PRE_MULTIPLICATION:** This Bit allows plane logic to alpha multiply ARGB/RGBA pizels if they are not pre multiplied already. 0: RGB Components are pre multiplied with alpha channel of the pixel. 1: RGB components have not been multiplied with alpha channel of the pixel. Plane will performed multiplication before alpha blending.
22	0x0 RW	**SPRITE_SOURCE_KEY_ENABLE:** When used as a sprite in the 16/32-bpp modes without alpha this enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Setting this bit is not allowed when the Sprite B pixel format includes an alpha channel. [DevBW] Erratum: This bit must always be set to 0 when Sprite B pixel format is YUV 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled.
21:20	0x0 RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two (both H and V). 00 = No line/Pixel duplication 01 = Line/Pixel Doubling 10 = Line Doubling only 11 = Pixel Doubling only

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RW	**COLOR_CONVERSION_DISABLED:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4:2:2 packed format and x:8:8:8 and 8:8:8:8 formats. Formats such as RGB5:5:5 and 5:6:5 do not have YUV versions. 0 = Pixel data is sent through the conversion logic (only applies to YUV formats) 1 = Pixel data is not sent through the YUV-)RGB conversion logic.
18	0x0 RW	**YUV_FORMAT:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 = ITU-R Recommendation BT.601 1 = ITU-R Recommendation BT.709
17:16	0x0 RW	**YUV_BYTE_ORDER:** This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored. 00 = YUYV 01 = UYVY 10 = YVYU 11 = VYUY
15	0x0 RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner. 0 = No rotation 1 = 180 rotation
14:11	0x0 RO	**RESERVED_1:** Reserved.
10	0x0 RW	**TILED_SURFACE:** This bit indicates that the Sprite B surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPCTILEOFF, DSPCLINOFF, and DSPCSURFADDR registers. 0 = Sprite B surface uses linear memory 1 = Sprite B surface uses X-tiled memory
9	0x0 RO	**RESERVED_2:** Write as zero
8	0x0 RO	**Mirroring_Enable:** 0: Mirroring is not enabled. 1: Mirroring is enabled.
7:3	0x0 RO	**RESERVED_3:** Write as zero
2	0x0 RW	**SPRITE_B_BOTTOM:** This bit will force the Sprite B plane to be on the bottom of the Z order. If the plane is marked as trusted, it only applies to the Z order of the trusted planes. 0 = Sprite B Z order is determined by the other control bits 1 = Sprite B is forced to be on the bottom of the Z order.
1	0x0 RO	**RESERVED_4:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**SPRITE_B_Z_ORDER:** With Sprite A and B z-order, bottom control bits, Sprite B plane is placed in a specific z-order among other planes in pipe A. Display Pipe A Z-orders SA zorderSA bottomSB zorderSB bottomResulting Pipe Z-order (from bottom to top)Source Keying 0000PA SA SB CAPA in Black 1000PA SB SA CAPA in Black 0001SB PA SA CAuse src keying on SB 0011SB PA SA CAuse src keying on SB 1001SB SA PA CAuse src keying on SA 1011SB SA PA CAuse src keying on SA 0100SA PA SB CAuse src keying on SA 1100SA PA SB CAuse src keying on SA 0110SA SB PA CAuse src keying on SB 1110SA SB PA CAuse src keying on SB 0: Sprite B z-order is disabled 1: Sprite B z-order is enabled

4.3.304 SPBLINOFF—Offset 72284h

Sprite B Linear Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72284h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
SPRITE_B_OFFSET							

Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SPRITE_B_OFFSET:** This register provides the panning offset into the Sprite B plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

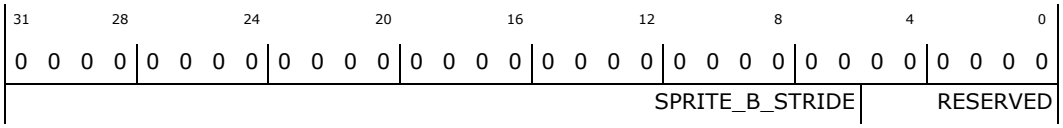
4.3.305 SPBSTRIDE—Offset 72288h

Sprite B Stride Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72288h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**SPRITE_B_STRIDE:** This is the stride for Sprite B in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.
5:0	0x0 RO	**RESERVED:** Reserved.

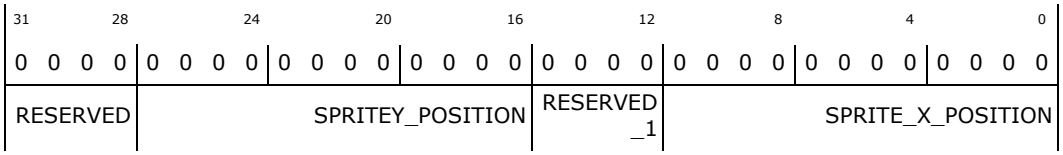
4.3.306 SPBPOS—Offset 7228Ch

Sprite B Position Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7228Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**SPRITEY_POSITION:** These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0x0 RO	**RESERVED_1:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
11:0	0x0 RW	**SPRITE_X_POSITION:** These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180 rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

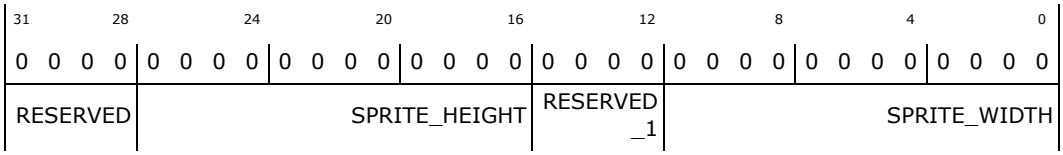
4.3.307 SPBSIZE—Offset 72290h

Sprite B Height and Width Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72290h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**SPRITE_HEIGHT:** This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**SPRITE_WIDTH:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values when YUV source pixel format is used (actual width, not the width minus one value).

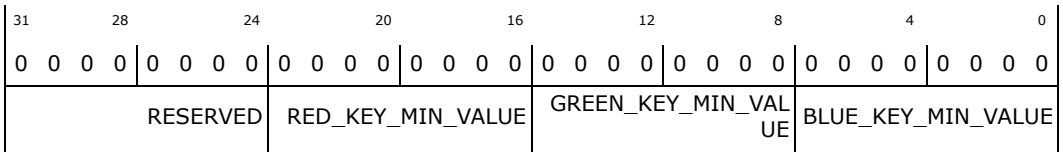
4.3.308 SPBKEYMINVAL—Offset 72294h

Sprite B Color Key Min Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72294h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero
23:16	0x0 RW	**RED_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite red/Cr channel.
15:8	0x0 RW	**GREEN_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite green/Y channel.
7:0	0x0 RW	**BLUE_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite blue/Cb channel.

4.3.309 SPBKEYMSK—Offset 72298h

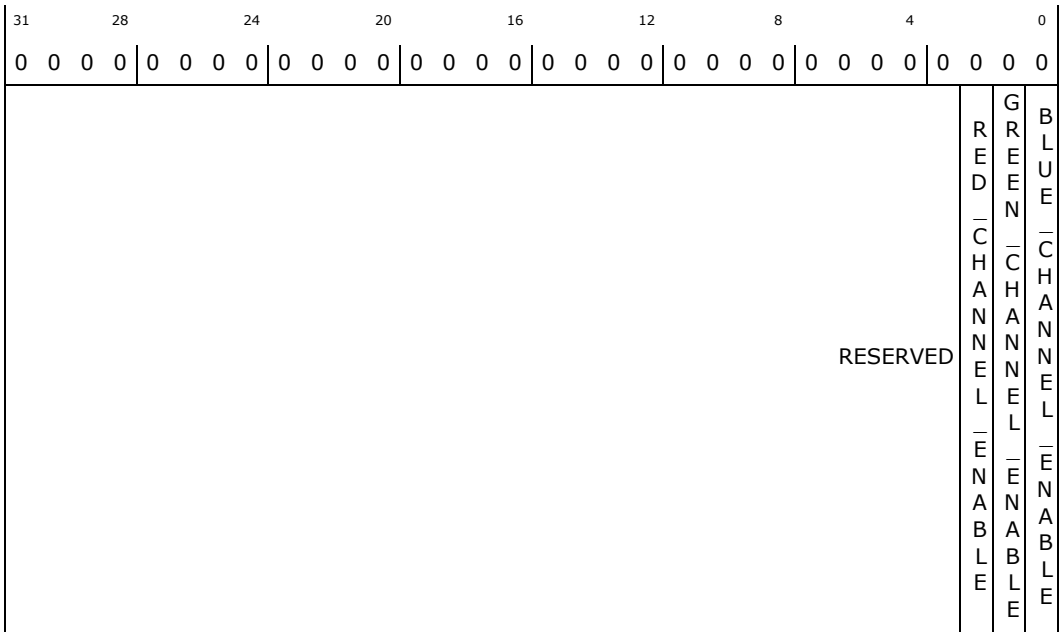
Sprite B Color Key Mask Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 72298h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**RESERVED:** Write as zero
2	0x0 RW	**RED_CHANNEL_ENABLE:** Specifies the source color key enable for the red/Cr channel.
1	0x0 RW	**GREEN_CHANNEL_ENABLE:** Specifies the source color key enable for the green/Y channel.
0	0x0 RW	**BLUE_CHANNEL_ENABLE:** Specifies the source color key enable for the blue/Cb channel

4.3.310 SPBSURF—Offset 7229Ch

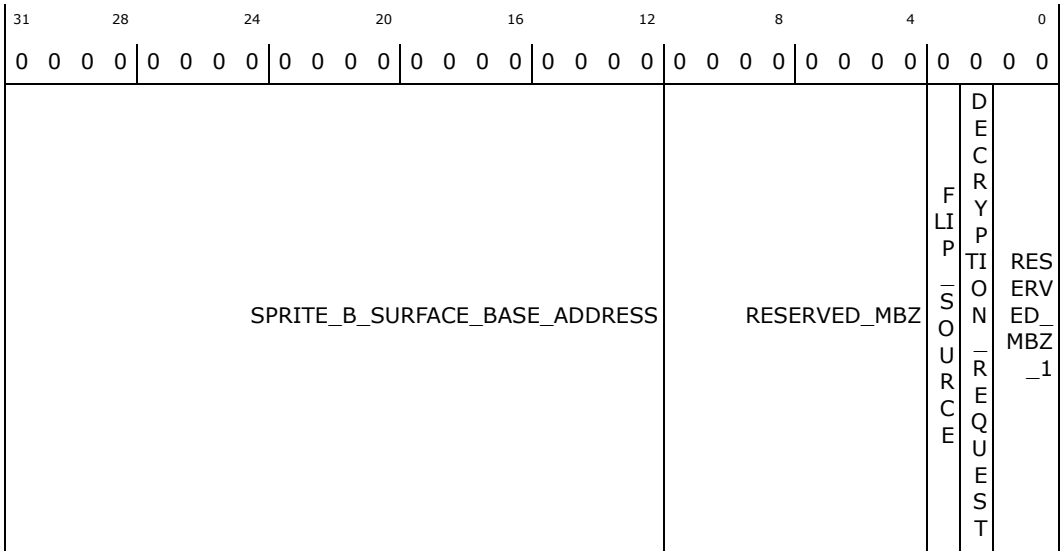
Sprite B Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 7229Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**SPRITE_B_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register. This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . The value in this register is updated through the command streamer during synchronous flips. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0x0 RO	**RESERVED_MBZ:** Reserved.
3	0x0 RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0x0 RO	**RESERVED_MBZ_1:** Reserved.

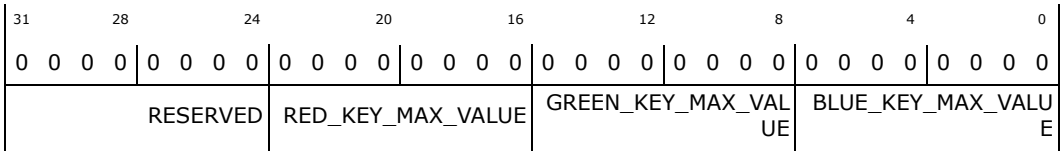
4.3.311 SPBKEYMAXVAL—Offset 722A0h

Sprite B Color Key Max Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 722A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero
23:16	0x0 RW	**RED_KEY_MAX_VALUE:** Specifies the color key value for the sprite red/Cr channel.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RW	**GREEN_KEY_MAX_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0x0 RW	**BLUE_KEY_MAX_VALUE:** Specifies the color key value for the sprite blue/Cb channel.

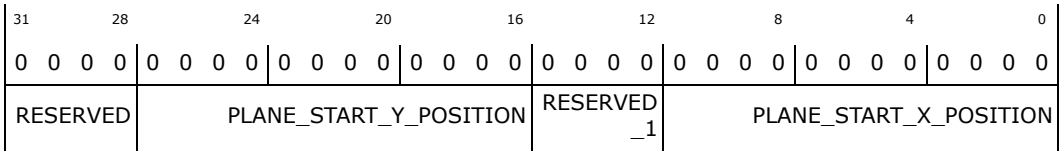
4.3.312 SPBTILEOFF—Offset 722A4h

Sprite B Tiled Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 722A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

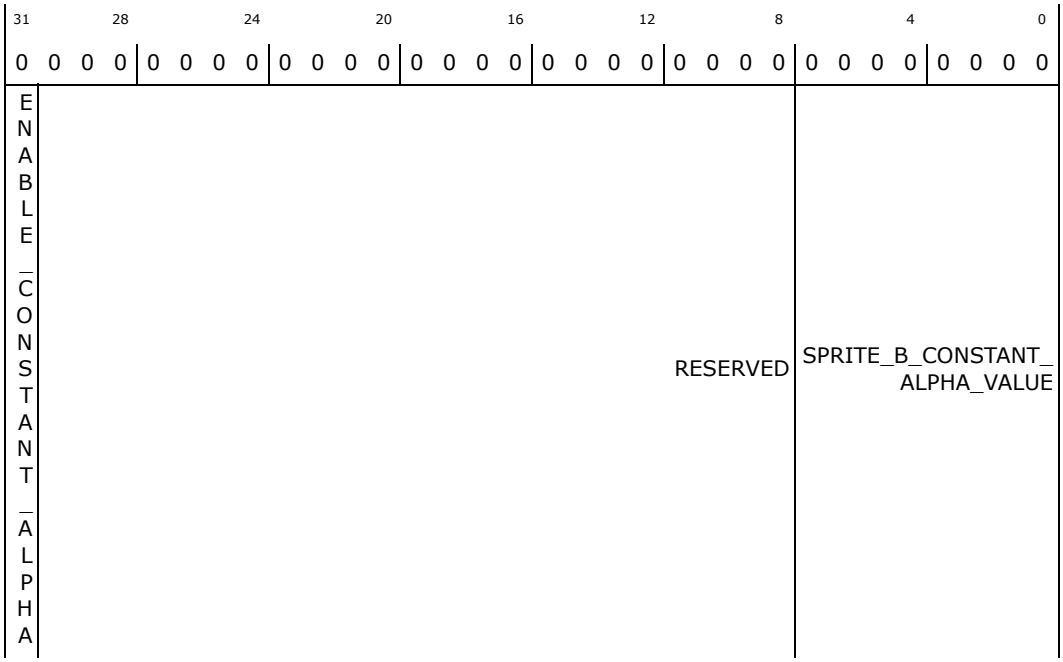
4.3.313 SPBCONTALPHA—Offset 722A8h

Sprite B Constant Alpha Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 722A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**ENABLE_CONSTANT_ALPHA:** Sprite B Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 Sprite B Sprite Constant Alpha is disabled 1 Sprite B Sprite Constant Alpha is enabled
30:8	0x0 RO	**RESERVED:** MBZ
7:0	0x0 RW	**SPRITE_B_CONSTANT_ALPHA_VALUE:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

4.3.314 SPBLIVESURF—Offset 722ACh

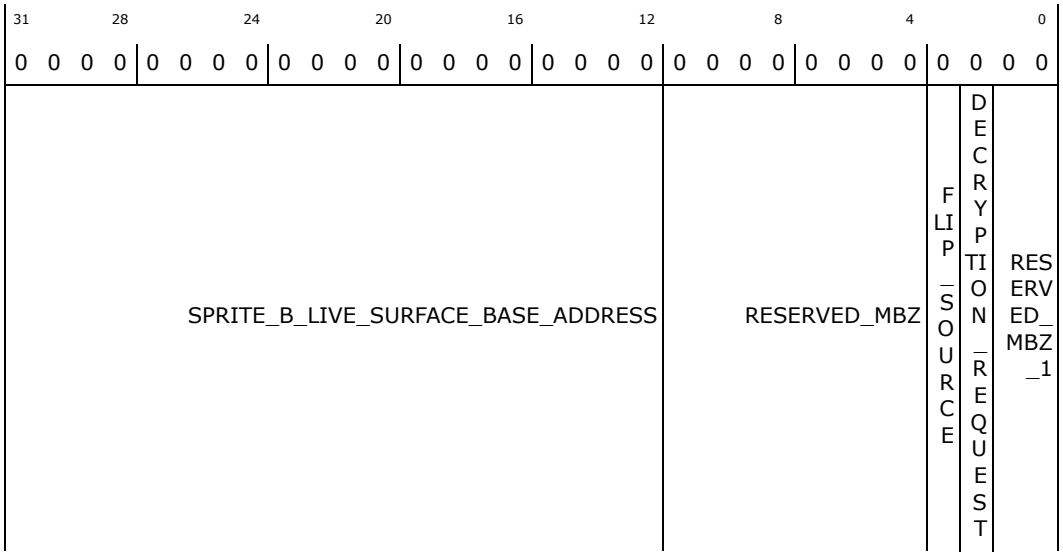
Sprite B Live Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 722ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**SPRITE_B_LIVE_SURFACE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for Sprite B plane.
11:4	0x0 RO	**RESERVED_MBZ:** Reserved.
3	0x0 RO	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RO	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0x0 RO	**RESERVED_MBZ_1:** Reserved.

4.3.315 SPBCLRC0—Offset 722D0h

Sprite B Color Correction 0 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 722D0h

Default: 01000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
RESERVED	CONTRAST	RESERVED_1	BRIGHTNESS					

Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
26:18	0x40 RW	**CONTRAST:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed-point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast, for YUV modes and for source data in RGB format, is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	0x0 RO	**RESERVED_1:** Reserved.
7:0	0x0 RW	**BRIGHTNESS:** This field provides the brightness adjustment with a 8-bit 2 s compliment value ranging [-128, +127]. This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8-bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of [-255, +255]. Bypassing Brightness for YUV formats and for source data in RGB format, is accomplished by programming this field to 0.

4.3.316 SPBCLRC1—Offset 722D4h

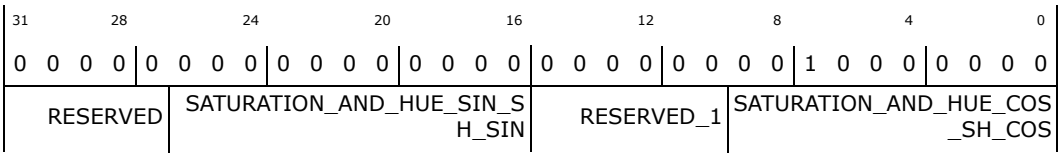
Sprite B Color Correction 1 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 722D4h

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
26:16	0x0 RW	**SATURATION_AND_HUE_SIN_SH_SIN:** This 11-bit signed fixed-point number is in 2 s compliment (s3i.7f) format with the MSB as the sign, next 3 MSBs as the integer value and the last 7 LSBs as the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Hue, even for source data in RGB format, is accomplished by programming this field to 0.0.
15:10	0x0 RO	**RESERVED_1:** Reserved.
9:0	0x80 RW	**SATURATION_AND_HUE_COS_SH_COS:** This unsigned fixed-point number is in 3i.7f format with the first 3 MSBs be the integer value and the last 7 LSBs be the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Saturation, even for source data in RGB format, is accomplished by programming this field to 1.0.

4.3.317 SPBGAMC5—Offset 722E0h

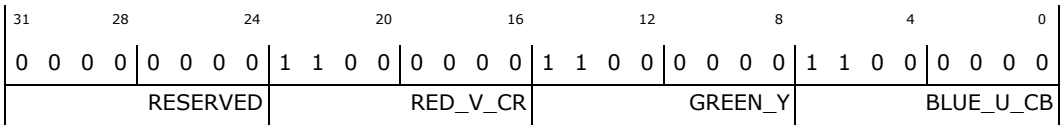
Sprite B Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 722E0h

Default: 00C0C0C0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**

Bit Range	Default & Access	Field Name (ID): Description
23:16	0xc0 RW	**RED_V_CR:** Reserved.
15:8	0xc0 RW	**GREEN_Y:** Reserved.
7:0	0xc0 RW	**BLUE_U_CB:**

4.3.318 SPBGAMC4—Offset 722E4h

Sprite B Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 722E4h

Default: 00808080h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x80 RW	**RED_V_CR:** Reserved.
15:8	0x80 RW	**GREEN_Y:** Reserved.
7:0	0x80 RW	**BLUE_U_CB:**

4.3.319 SPBGAMC3—Offset 722E8h

Sprite B Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 722E8h

Default: 00404040h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 1 0 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x40 RW	**RED_V_CR:** Reserved.
15:8	0x40 RW	**GREEN_Y:** Reserved.
7:0	0x40 RW	**BLUE_U_CB:**

4.3.320 SPBGAMC2—Offset 722ECh

Sprite B Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 722ECh

Default: 00202020h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 1 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x20 RW	**RED_V_CR:** Reserved.
15:8	0x20 RW	**GREEN_Y:** Reserved.
7:0	0x20 RW	**BLUE_U_CB:**

4.3.321 SPBGAMC1—Offset 722F0h

Sprite B Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 722F0h

Default: 00101010h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x10 RW	**RED_V_CR:** Reserved.
15:8	0x10 RW	**GREEN_Y:** Reserved.
7:0	0x10 RW	**BLUE_U_CB:**

4.3.322 SPBGAMC0—Offset 722F4h

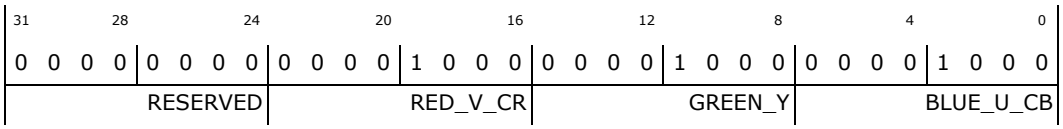
Sprite B Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 722F4h

Default: 00080808h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x8 RW	**RED_V_CR:** Reserved.
15:8	0x8 RW	**GREEN_Y:** Reserved.
7:0	0x8 RW	**BLUE_U_CB:**

4.3.323 SPCCNTR—Offset 72380h

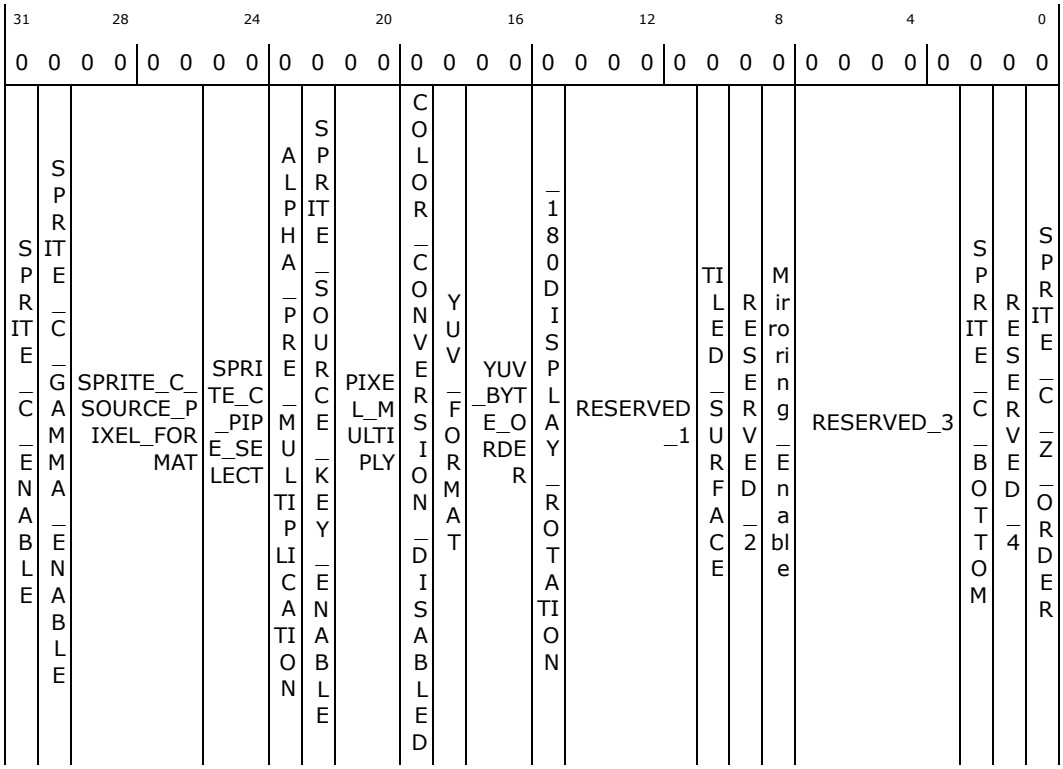
Sprite C Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 72380h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SPRITE_C_ENABLE:** This bit will enable or disable the Sprite C. When this bit is set, the plane will generate pixels for display to be combined by the blender for the target pipe. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted, this bit will be overridden and the display disabled when the registers are unlocked. 1 = Enable 0 = Disable
30	0x0 RW	**SPRITE_C_GAMMA_ENABLE:** There are two gamma adjustments possible in the Sprite C data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8-bit indexed, this bit should be set to a one. Gamma correction logic that is contained in the Sprite C logic is disabled by loading the default values into those registers. When this plane is marked as trusted, this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 = Sprite C pixel data bypasses the display pipe gamma correction logic (default). 1 = Sprite C pixel data is gamma corrected in the pipe gamma correction logic

Bit Range	Default & Access	Field Name (ID): Description
29:26	0x0 RW	**SPRITE_C_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite/Sprite C. Pixel formats with an alpha channel should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 0000 = YUV 4:2:2 packed (see byte order below). 0001 = Reserved 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format with pre-multiplied alpha channel. 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format 1010 = 32-bitBGRX(10:10:10:2)pixel format alpha. 1011 = 32-bit BGRA(10:10:10:2)pixel format(with pre multiplied alpha color format). 1100 = Reserved. 1101 = Reserved. 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8)
25:24	0x0 RW	**SPRITE_C_PIPE_SELECT:** Sprite C always ties to Pipe B Reserved.
23	0x0 RO	**ALPHA_PRE_MULTIPLICATION:** This Bit allows plane logic to alpha multiply ARGB/RGBA pizels if they are not pre multiplied already. 0: RGB Components are pre multiplied with alpha channel of the pixel. 1: RGB components have not been multiplied with alpha channel of the pixel. Plane will performed multiplication before alpha blending.
22	0x0 RW	**SPRITE_SOURCE_KEY_ENABLE:** When used as a sprite in the 16/32-bpp modes without alpha this enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Setting this bit is not allowed when the Sprite C pixel format includes an alpha channel. [DevBW] Erratum: This bit must always be set to 0 when Sprite C pixel format is YUV 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled.
21:20	0x0 RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two (both H and V). 00 = No line/Pixel duplication 01 = Line/Pixel Doubling 10 = Line Doubling only 11 = Pixel Doubling only

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RW	**COLOR_CONVERSION_DISABLED:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4:2:2 packed format and x:8:8:8 and 8:8:8:8 formats. Formats such as RGB5:5:5 and 5:6:5 do not have YUV versions. 0 = Pixel data is sent through the conversion logic (only applies to YUV formats) 1 = Pixel data is not sent through the YUV-)RGB conversion logic.
18	0x0 RW	**YUV_FORMAT:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 = ITU-R Recommendation BT.601 1 = ITU-R Recommendation BT.709
17:16	0x0 RW	**YUV_BYTE_ORDER:** This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored. 00 = YUYV 01 = UYVY 10 = YVYU 11 = VYUY
15	0x0 RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner. 0 = No rotation 1 = 180 rotation
14:11	0x0 RO	**RESERVED_1:** Reserved.
10	0x0 RW	**TILED_SURFACE:** This bit indicates that the Sprite C surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPCTILEOFF, DSPCLINOFF, and DSPCSURFADDR registers. 0 = Sprite C surface uses linear memory 1 = Sprite C surface uses X-tiled memory
9	0x0 RO	**RESERVED_2:** Write as zero
8	0x0 RW	**Mirroring_Enable:** 0: Mirroring is not enabled. 1: Mirroring is enabled.
7:3	0x0 RO	**RESERVED_3:** Write as zero
2	0x0 RW	**SPRITE_C_BOTTOM:** This bit will force the Sprite C plane to be on the bottom of the Z order. If the plane is marked as trusted, it only applies to the Z order of the trusted planes. 0 = Sprite C Z order is determined by the other control bits 1 = Sprite C is forced to be on the bottom of the Z order.
1	0x0 RO	**RESERVED_4:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**SPRITE_C_Z_ORDER:** With Sprite C and D z-order, bottom control bits, Sprite C plane is placed in a specific z-order among other planes in pipe B. Display Pipe B Z-orders SC zorderSC bottomSD zorderSD bottomResulting Pipe Z-order (from bottom to top)Source Keying 0000PB SC SD CBPB in Black 1000PB SD SC CBPB in Black 0001SD PB SC CBuse src keying on SD 0011SD PB SC CBuse src keying on SD 1001SD SC PB CBuse src keying on SC 1011SD SC PB CBuse src keying on SC 0100SC PB SD CBuse src keying on SC 1100SC PB SD CBuse src keying on SC 0110SC SD PB CBuse src keying on SD 1110SC SD PB CBuse src keying on SD 0101Not Allowed 0111Not Allowed 1101Not Allowed 1111Not Allowed 1010Not Allowed 1011Not Allowed 0: Sprite C z-order is disabled 1: Sprite C z-order is enabled

4.3.324 SPCLINOFF—Offset 72384h

Sprite C Linear Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 72384h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
SPRITE_C_OFFSET								

Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SPRITE_C_OFFSET:** This register provides the panning offset into the Sprite C plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

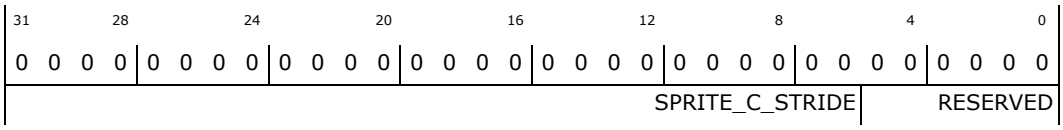
4.3.325 SPCSTRIDE—Offset 72388h

Sprite C Stride Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72388h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**SPRITE_C_STRIDE:** This is the stride for Sprite C in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.
5:0	0x0 RO	**RESERVED:** Reserved.

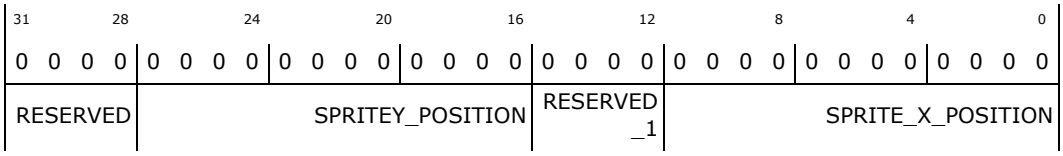
4.3.326 SPCPOS—Offset 7238Ch

Sprite C Position Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7238Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
27:16	0x0 RW	**SPRITEY_POSITION:** These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**SPRITE_X_POSITION:** These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180 rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

4.3.327 SPCSIZE—Offset 72390h

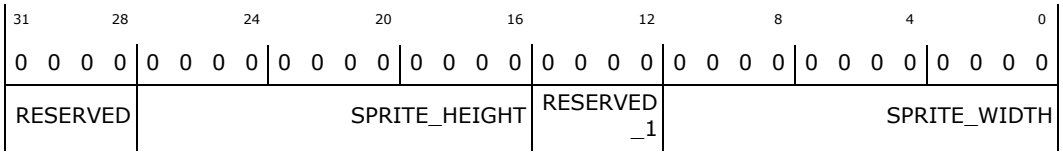
Sprite C Height and Width Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 72390h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**SPRITE_HEIGHT:** This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**SPRITE_WIDTH:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values when YUV source pixel format is used (actual width, not the width minus one value).

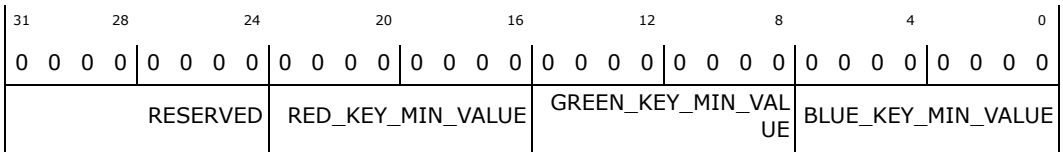
4.3.328 SPCKEYMINVAL—Offset 72394h

Sprite C Color Key Min Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72394h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero
23:16	0x0 RW	**RED_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite red/Cr channel.
15:8	0x0 RW	**GREEN_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite green/Y channel.
7:0	0x0 RW	**BLUE_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite blue/Cb channel.

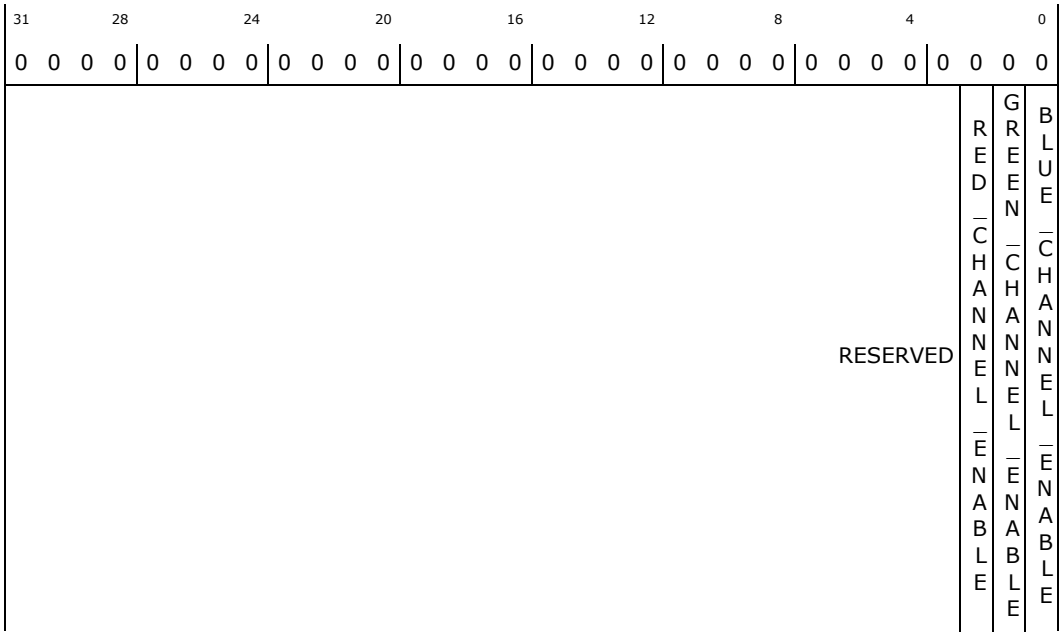
4.3.329 SPCKEYMSK—Offset 72398h

Sprite C Color Key Mask Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72398h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**RESERVED:** Write as zero
2	0x0 RW	**RED_CHANNEL_ENABLE:** Specifies the source color key enable for the red/Cr channel.
1	0x0 RW	**GREEN_CHANNEL_ENABLE:** Specifies the source color key enable for the green/Y channel.
0	0x0 RW	**BLUE_CHANNEL_ENABLE:** Specifies the source color key enable for the blue/Cb channel

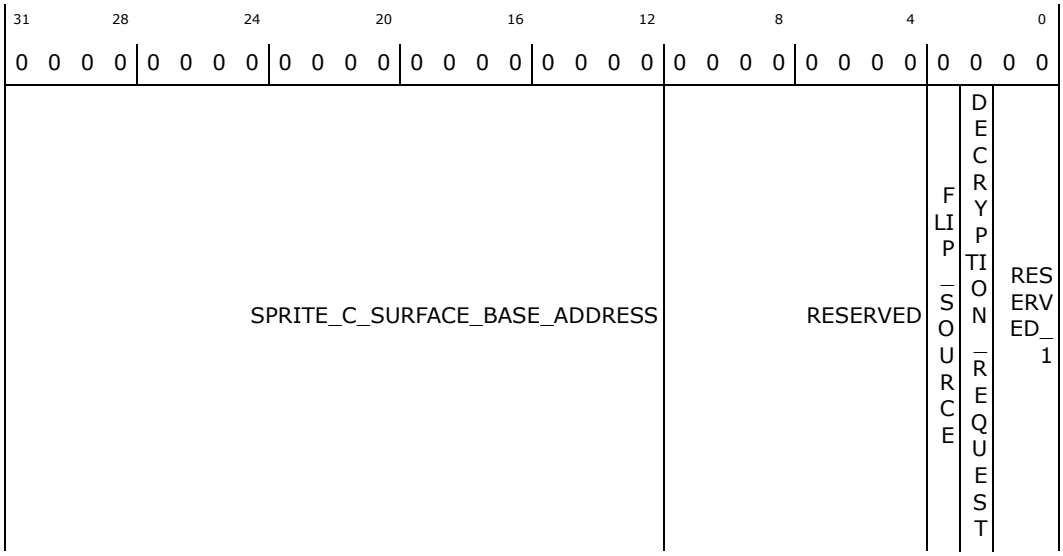
4.3.330 SPCSURF—Offset 7239Ch

Sprite C Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7239Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**SPRITE_C_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register. This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . The value in this register is updated through the command streamer during synchronous flips. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0x0 RO	**RESERVED:** MBZ

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0x0 RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0x0 RO	**RESERVED_1:** MBZ

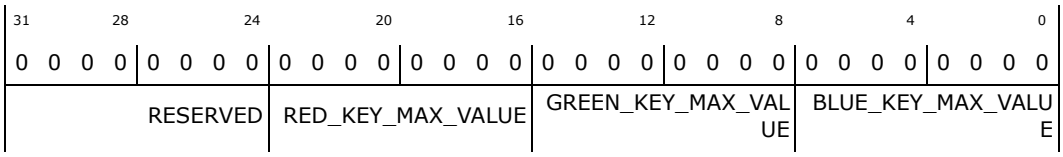
4.3.331 SPCKEYMAXVAL—Offset 723A0h

Sprite C Color Key Max Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 723A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero
23:16	0x0 RW	**RED_KEY_MAX_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0x0 RW	**GREEN_KEY_MAX_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0x0 RW	**BLUE_KEY_MAX_VALUE:** Specifies the color key value for the Sprite Clue/Cb channel.

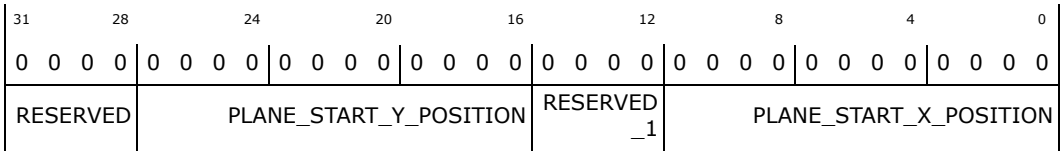
4.3.332 SPCTILEOFF—Offset 723A4h

Sprite C Tiled Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 723A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

4.3.333 SPCCONTALPHA—Offset 723A8h

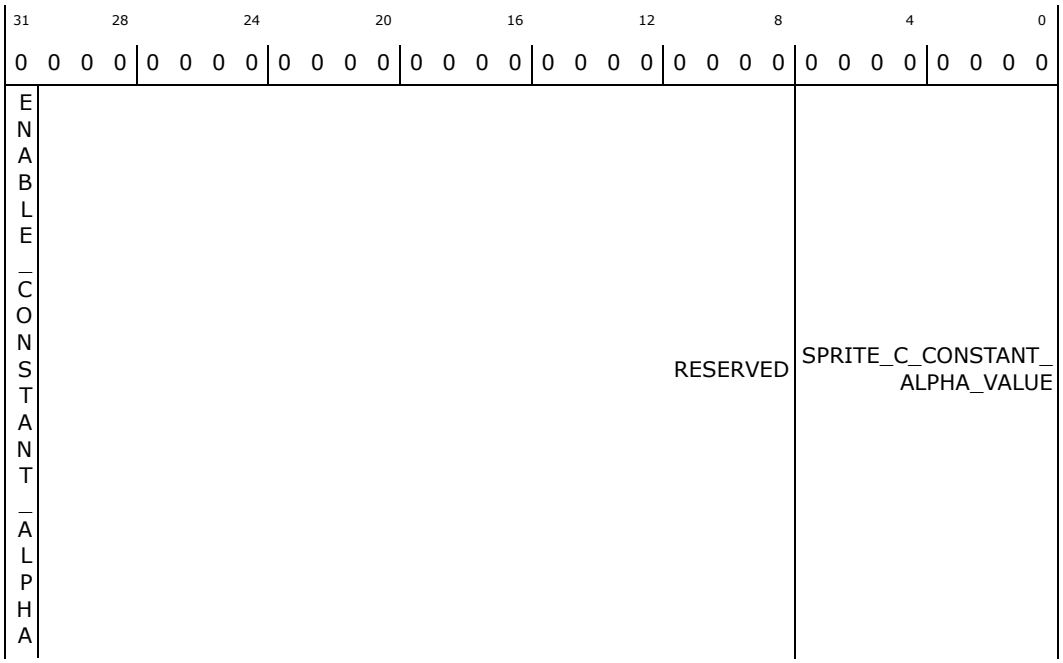
Sprite C Constant Alpha Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 723A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**ENABLE_CONSTANT_ALPHA:** Sprite C Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 Sprite C Sprite Constant Alpha is disabled 1 Sprite C Sprite Constant Alpha is enabled

Bit Range	Default & Access	Field Name (ID): Description
30:8	0x0 RO	**RESERVED:** MBZ
7:0	0x0 RW	**SPRITE_C_CONSTANT_ALPHA_VALUE:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

4.3.334 SPCLIVESURF—Offset 723ACh

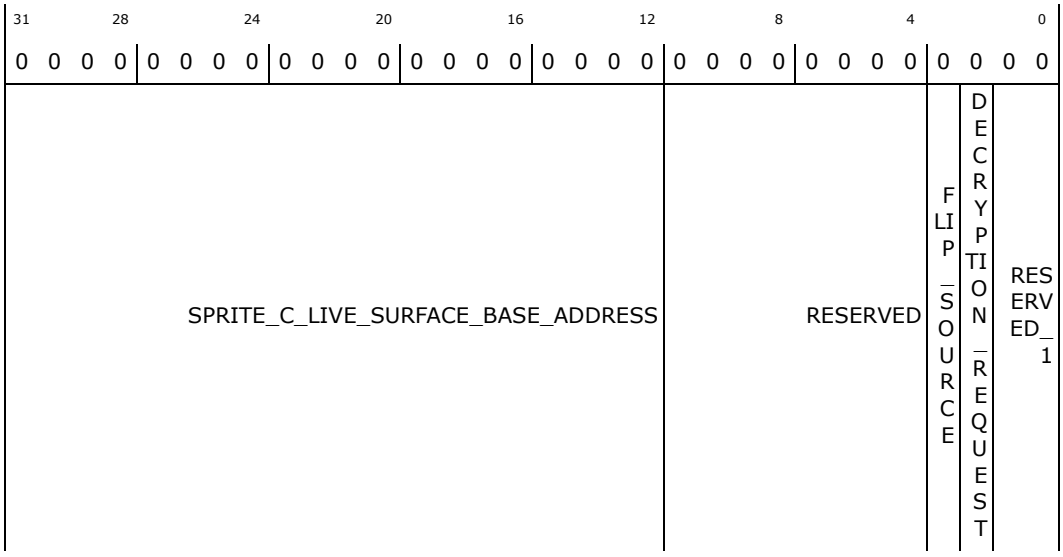
Sprite C Live Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 723ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**SPRITE_C_LIVE_SURFACE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for Sprite C.
11:4	0x0 RO	**RESERVED:** MBZ

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RO	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0x0 RO	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0x0 RO	**RESERVED_1:** MBZ

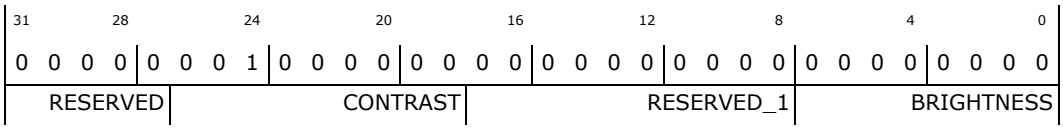
4.3.335 SPCCLRC0—Offset 723D0h

Sprite C Color Correction 0 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 723D0h

Default: 01000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** Reserved.
26:18	0x40 RW	**CONTRAST:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed-point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast, for YUV modes and for source data in RGB format, is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	0x0 RO	**RESERVED_1:** Reserved.
7:0	0x0 RW	**BRIGHTNESS:** This field provides the brightness adjustment with a 8-bit 2 s compliment value ranging [-128, +127]. This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8-bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of [-255, +255]. Bypassing Brightness for YUV formats and for source data in RGB format, is accomplished by programming this field to 0.

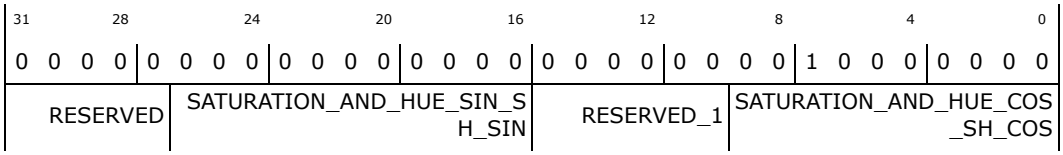
4.3.336 SPCCLRC1—Offset 723D4h

Sprite C Color Correction 1 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 723D4h

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** Reserved.
26:16	0x0 RW	**SATURATION_AND_HUE_SIN_SH_SIN:** This 11-bit signed fixed-point number is in 2 s compliment (s3i.7f) format with the MSB as the sign, next 3 MSBs as the integer value and the last 7 LSBs as the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Hue, even for source data in RGB format, is accomplished by programming this field to 0.0.
15:10	0x0 RO	**RESERVED_1:** Reserved.
9:0	0x80 RW	**SATURATION_AND_HUE_COS_SH_COS:** This unsigned fixed-point number is in 3i.7f format with the first 3 MSBs be the integer value and the last 7 LSBs be the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Saturation, even for source data in RGB format, is accomplished by programming this field to 1.0.

4.3.337 SPCGAMC5—Offset 723E0h

Sprite C Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 723E0h

Default: 00C0C0C0h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	1 1 0 0	0 0 0 0	1 1 0 0	0 0 0 0	1 1 0 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0xc0 RW	**RED_V_CR:** Reserved.
15:8	0xc0 RW	**GREEN_Y:** Reserved.
7:0	0xc0 RW	**BLUE_U_CB:**

4.3.338 SPCGAMC4—Offset 723E4h

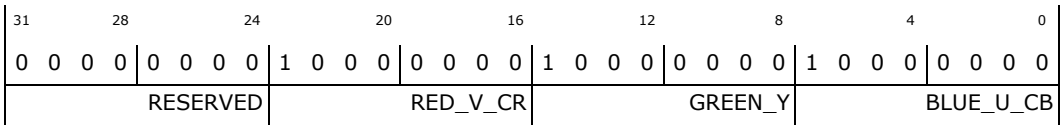
Sprite C Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 723E4h

Default: 00808080h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x80 RW	**RED_V_CR:** Reserved.
15:8	0x80 RW	**GREEN_Y:** Reserved.
7:0	0x80 RW	**BLUE_U_CB:**

4.3.339 SPCGAMC3—Offset 723E8h

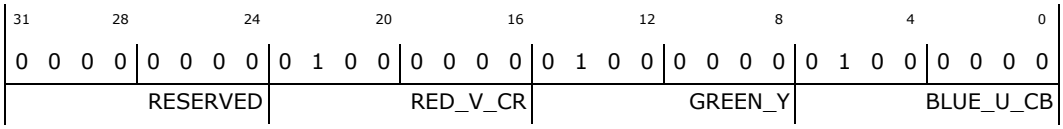
Sprite C Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 723E8h

Default: 00404040h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x40 RW	**RED_V_CR:** Reserved.
15:8	0x40 RW	**GREEN_Y:** Reserved.
7:0	0x40 RW	**BLUE_U_CB:**

4.3.340 SPCGAMC2—Offset 723ECh

Sprite C Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 723ECh

Default: 00202020h

31 28	24	20	16	12	8	4 0
0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 1 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x20 RW	**RED_V_CR:** Reserved.
15:8	0x20 RW	**GREEN_Y:** Reserved.
7:0	0x20 RW	**BLUE_U_CB:**

4.3.341 SPCGAMC1—Offset 723F0h

Sprite C Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 723F0h

Default: 00101010h

31 28	24	20	16	12	8	4 0
0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x10 RW	**RED_V_CR:** Reserved.
15:8	0x10 RW	**GREEN_Y:** Reserved.
7:0	0x10 RW	**BLUE_U_CB:**

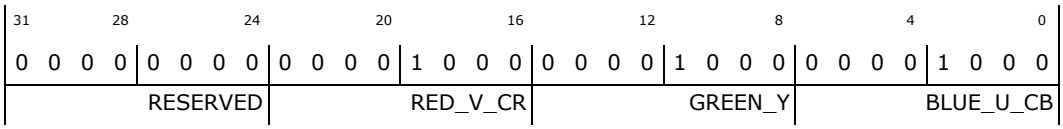
4.3.342 SPCGAMC0—Offset 723F4h

Sprite C Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 723F4h

Default: 00080808h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x8 RW	**RED_V_CR:** Reserved.
15:8	0x8 RW	**GREEN_Y:** Reserved.
7:0	0x8 RW	**BLUE_U_CB:**

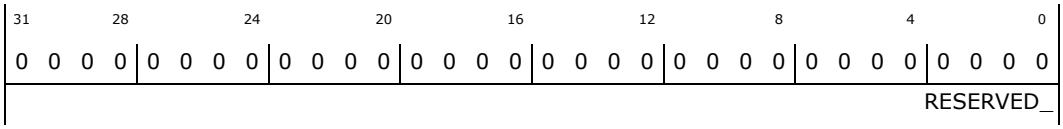
4.3.343 SWF30—Offset 72414h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72414h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

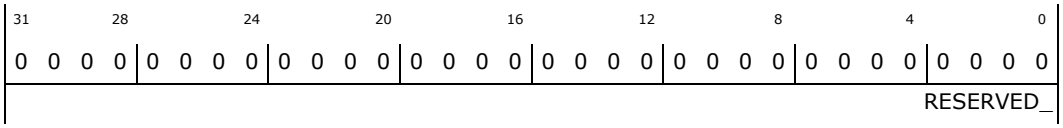
4.3.344 SWF31—Offset 72418h

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72418h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

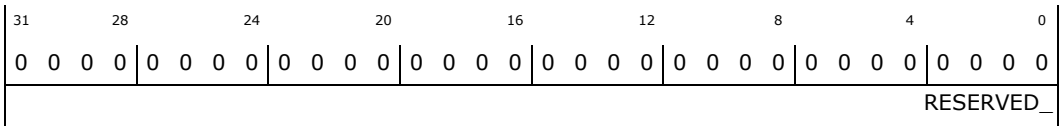
4.3.345 SWF32—Offset 7241Ch

Software Flag Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7241Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RESERVED_:** for Video BIOS and Drivers

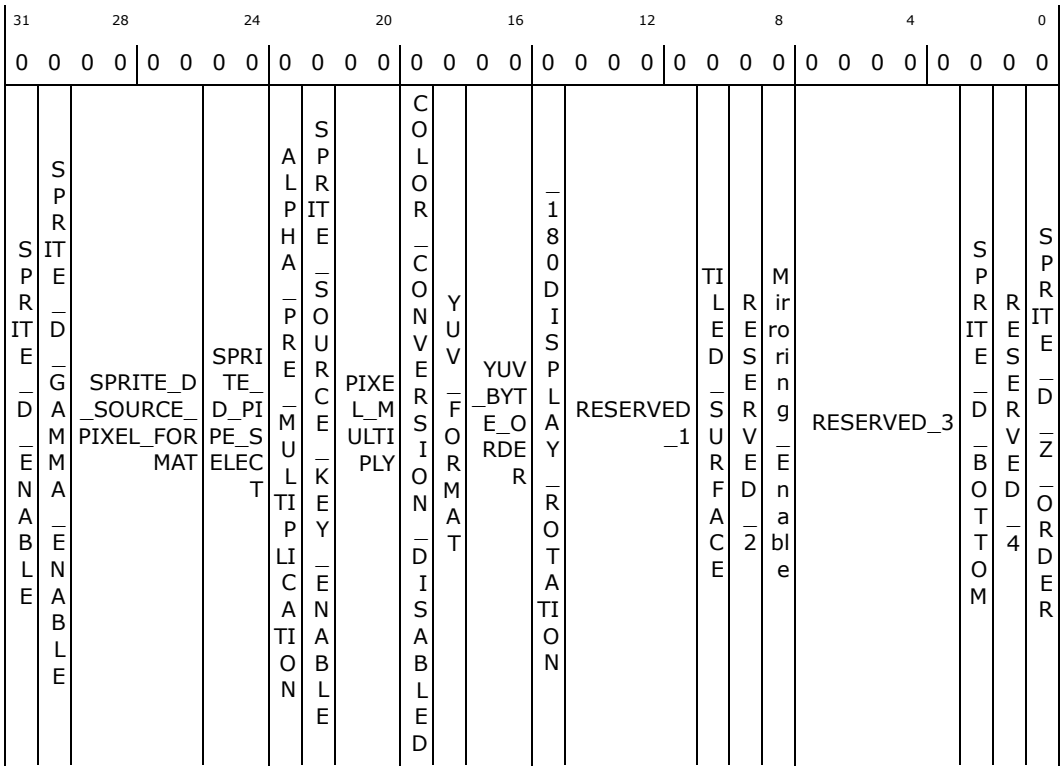
4.3.346 SPDCNTR—Offset 72480h

Sprite D Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72480h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SPRITE_D_ENABLE:** This bit will enable or disable the Sprite D. When this bit is set, the plane will generate pixels for display to be combined by the blender for the target pipe. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted, this bit will be overridden and the display disabled when the registers are unlocked. 1 = Enable 0 = Disable

Bit Range	Default & Access	Field Name (ID): Description
30	0x0 RW	**SPRITE_D_GAMMA_ENABLE:** There are two gamma adjustments possible in the Sprite D data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8-bit indexed, this bit should be set to a one. Gamma correction logic that is contained in the Sprite D logic is disabled by loading the default values into those registers. When this plane is marked as trusted, this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 = Sprite D pixel data bypasses the display pipe gamma correction logic (default). 1 = Sprite D pixel data is gamma corrected in the pipe gamma correction logic
29:26	0x0 RW	**SPRITE_D_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite/Sprite D. Pixel formats with an alpha channel should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 0000 = YUV 4:2:2 packed (see byte order below). 0001 = Reserved 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format with pre-multiplied alpha channel. 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format 1010 = 32-bit BGRX(10:10:10:2)pixel format Ignore alpha. 1011 = 32-bit BRGA(10:10:10:2)pixel format(with pre-multiplied alpha color format). 1100 = Reserved. 1101 = Reserved. 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8)
25:24	0x0 RW	**SPRITE_D_PIPE_SELECT:** Sprite D always ties to Pipe B. Reserved.
23	0x0 RW	**ALPHA_PRE_MULTIPLICATION:** This Bit allows plane logic to alpha multiply ARGB/RGBA pizels if they are not pre multiplied already. 0: RGB Components are pre multiplied with alpha channel of the pixel. 1: RGB components have not been multiplied with alpha channel of the pixel. Plane will performed multiplication before alpha blending.
22	0x0 RW	**SPRITE_SOURCE_KEY_ENABLE:** When used as a sprite in the 16/32-bpp modes without alpha this enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Setting this bit is not allowed when the Sprite D pixel format includes an alpha channel. [DevBW] Erratum: This bit must always be set to 0 when Sprite D pixel format is YUV 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled.

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two (both H and V). 00 = No line/Pixel duplication 01 = Line/Pixel Doubling 10 = Line Doubling only 11 = Pixel Doubling only
19	0x0 RW	**COLOR_CONVERSION_DISABLED:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4:2:2 packed format and x:8:8:8 and 8:8:8:8 formats. Formats such as RGB5:5:5 and 5:6:5 do not have YUV versions. 0 = Pixel data is sent through the conversion logic (only applies to YUV formats) 1 = Pixel data is not sent through the YUV-)RGB conversion logic.
18	0x0 RW	**YUV_FORMAT:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 = ITU-R Recommendation BT.601 1 = ITU-R Recommendation BT.709
17:16	0x0 RW	**YUV_BYTE_ORDER:** This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored. 00 = YUYV 01 = UYVY 10 = YVYU 11 = VYUY
15	0x0 RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner. 0 = No rotation 1 = 180 rotation
14:11	0x0 RO	**RESERVED_1:** Reserved.
10	0x0 RW	**TILED_SURFACE:** This bit indicates that the Sprite D surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPCTILEOFF, DSPCLINOFF, and DSPCSURFADDR registers. 0 = Sprite D surface uses linear memory 1 = Sprite D surface uses X-tiled memory
9	0x0 RO	**RESERVED_2:** Write as zero
8	0x0 RW	**Mirroring_Enable:** 0: Mirroring is not enabled. 1: Mirroring is enabled.
7:3	0x0 RO	**RESERVED_3:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**SPRITE_D_BOTTOM:** This bit will force the Sprite D plane to be on the bottom of the Z order. If the plane is marked as trusted, it only applies to the Z order of the trusted planes. 0 = Sprite D Z order is determined by the other control bits 1 = Sprite D is forced to be on the bottom of the Z order.
1	0x0 RO	**RESERVED_4:** Reserved.
0	0x0 RW	**SPRITE_D_Z_ORDER:** With Sprite C and D z-order, bottom control bits, Sprite D plane is placed in a specific z-order among other planes in pipe B. Display Pipe B Z-orders SC zorderSC bottomSD zorderSD bottomResulting Pipe Z-order (from bottom to top)Source Keying 0000PB SC SD CBPB in Black 1000PB SD SC CBPB in Black 0001SD PB SC CBuse src keying on SD 0011SD PB SC CBuse src keying on SD 1001SD SC PB CBuse src keying on SC 1011SD SC PB CBuse src keying on SC 0100SC PB SD CBuse src keying on SC 1100SC PB SD CBuse src keying on SC 0110SC SD PB CBuse src keying on SD 1110SC SD PB CBuse src keying on SD 0101Not Allowed 0111Not Allowed 1101Not Allowed 1111Not Allowed 1010Not Allowed 1011Not Allowed 0: Sprite D z-order is disabled 1: Sprite D z-order is enabled

4.3.347 SPDLINOFF—Offset 72484h

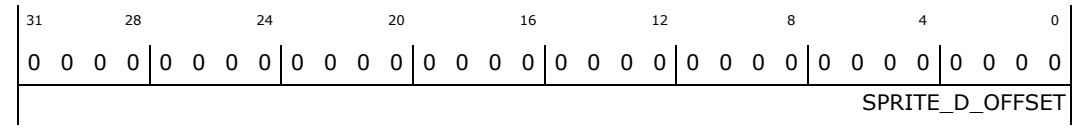
Sprite D Linear Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 72484h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SPRITE_D_OFFSET:** This register provides the panning offset into the Sprite D plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

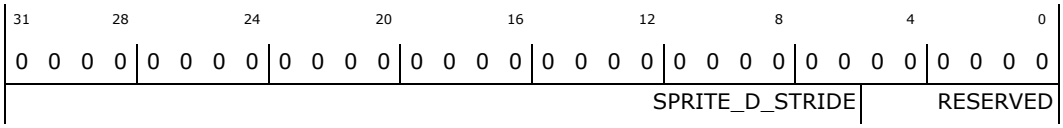
4.3.348 SPDSTRIDE—Offset 72488h

Sprite D Stride Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72488h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**SPRITE_D_STRIDE:** This is the stride for Sprite D in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.
5:0	0x0 RO	**RESERVED:** Reserved.

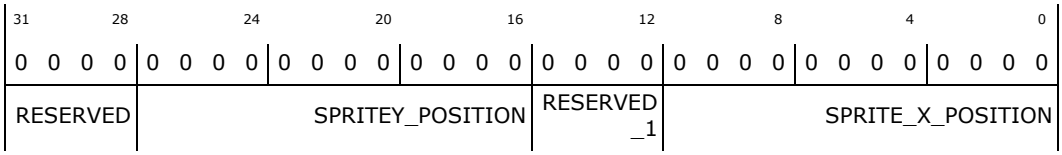
4.3.349 SPDPOS—Offset 7248Ch

Sprite D Position Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7248Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**SPRITEY_POSITION:** These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**SPRITE_X_POSITION:** These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180 rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

4.3.350 SPDSIZE—Offset 72490h

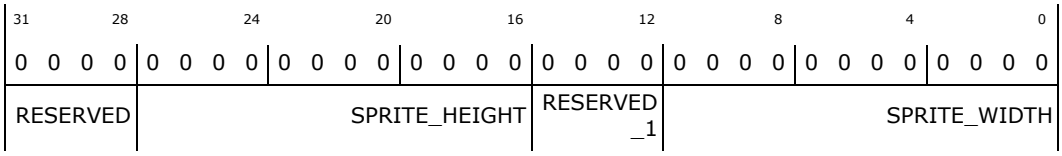
Sprite D Height and Width Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 72490h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**SPRITE_HEIGHT:** This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0x0 RO	**RESERVED_1:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
11:0	0x0 RW	**SPRITE_WIDTH:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values when YUV source pixel format is used (actual width, not the width minus one value).

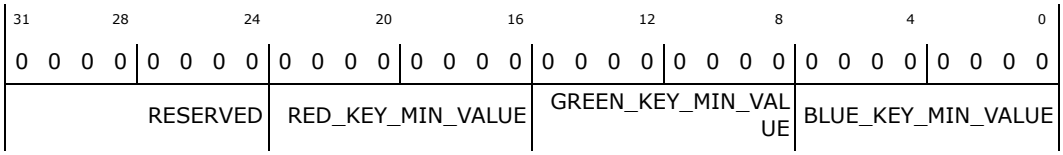
4.3.351 SPDKEYMINVAL—Offset 72494h

Sprite D Color Key Min Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72494h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero
23:16	0x0 RW	**RED_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite red/Cr channel.
15:8	0x0 RW	**GREEN_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite green/Y channel.
7:0	0x0 RW	**BLUE_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite blue/Cb channel.

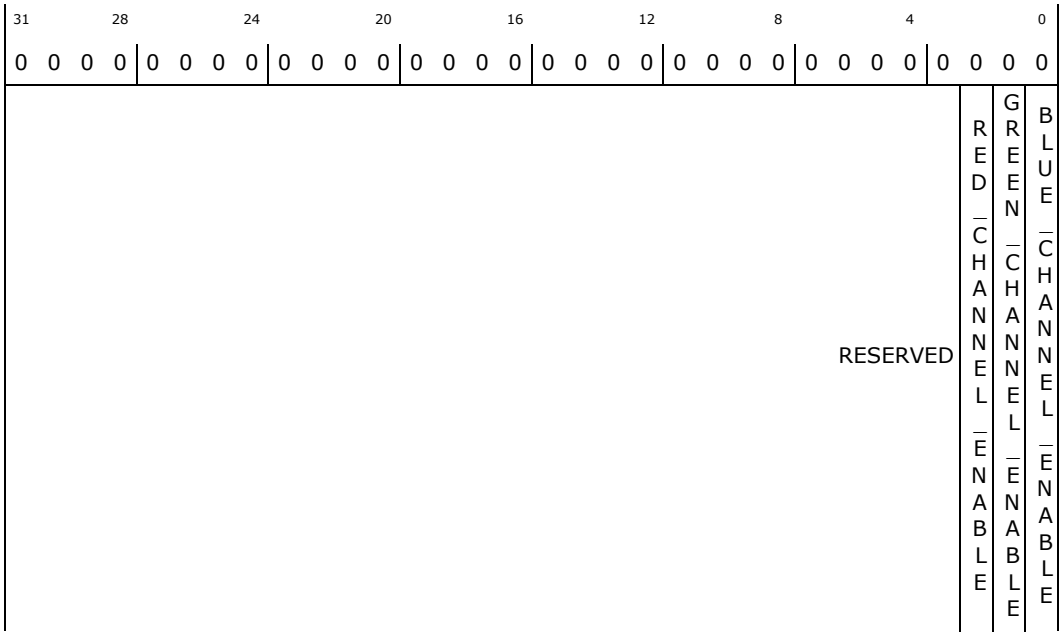
4.3.352 SPDKEYMSK—Offset 72498h

Sprite D Color Key Mask Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72498h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**RESERVED:** Write as zero
2	0x0 RW	**RED_CHANNEL_ENABLE:** Specifies the source color key enable for the red/Cr channel.
1	0x0 RW	**GREEN_CHANNEL_ENABLE:** Specifies the source color key enable for the green/Y channel.
0	0x0 RW	**BLUE_CHANNEL_ENABLE:** Specifies the source color key enable for the blue/Cb channel

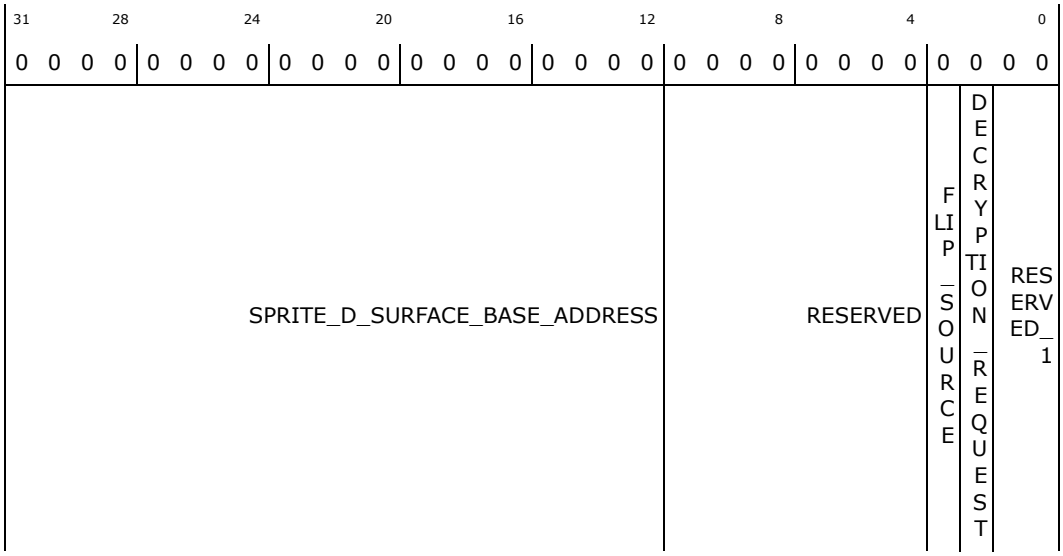
4.3.353 SPDSURF—Offset 7249Ch

Sprite D Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7249Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**SPRITE_D_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register. This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . The value in this register is updated through the command streamer during synchronous flips. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0x0 RO	**RESERVED:** MBZ

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0x0 RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0x0 RO	**RESERVED_1:** MBZ

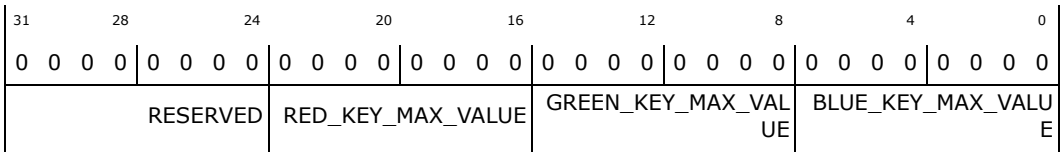
4.3.354 SPDKEYMAXVAL—Offset 724A0h

Sprite D Color Key Max Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 724A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero
23:16	0x0 RW	**RED_KEY_MAX_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0x0 RW	**GREEN_KEY_MAX_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0x0 RW	**BLUE_KEY_MAX_VALUE:** Specifies the color key value for the Sprite blue/Cb channel.

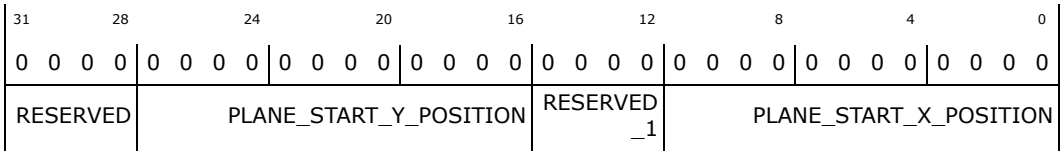
4.3.355 SPDTILEOFF—Offset 724A4h

Sprite D Tiled Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 724A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

4.3.356 SPDCONTALPHA—Offset 724A8h

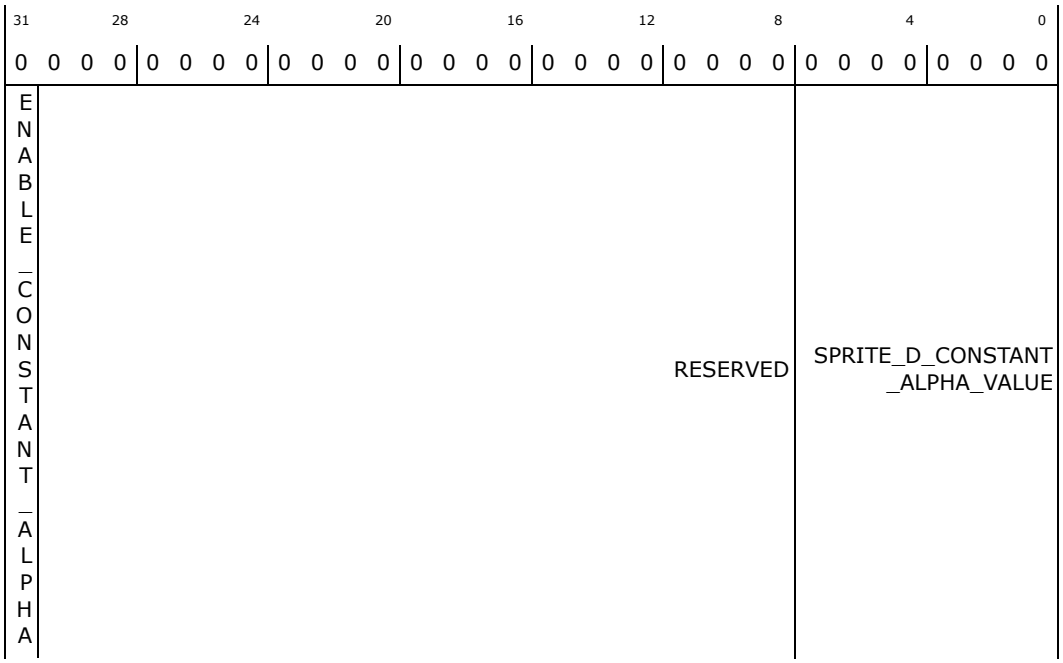
Sprite D Constant Alpha Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 724A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**ENABLE_CONSTANT_ALPHA:** Sprite D Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 Sprite D Constant Alpha is disabled 1 Sprite D Constant Alpha is enabled

Bit Range	Default & Access	Field Name (ID): Description
30:8	0x0 RO	**RESERVED:** MBZ
7:0	0x0 RW	**SPRITE_D_CONSTANT_ALPHA_VALUE:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

4.3.357 SPDLIVESURF—Offset 724ACh

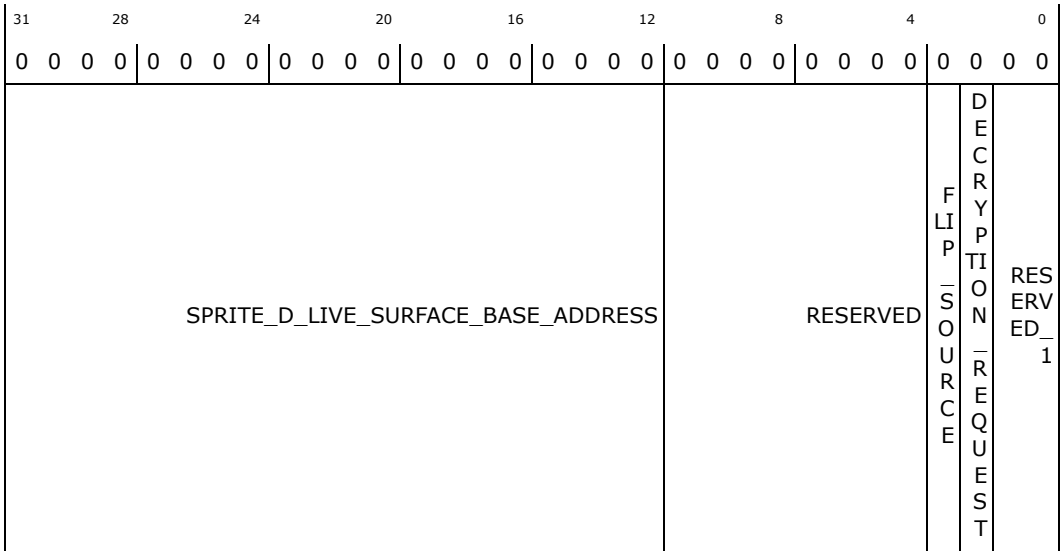
Sprite D Live Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 724ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**SPRITE_D_LIVE_SURFACE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for Sprite D
11:4	0x0 RO	**RESERVED:** MBZ

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RO	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0x0 RO	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0x0 RO	**RESERVED_1:** MBZ

4.3.358 SPDCLRC0—Offset 724D0h

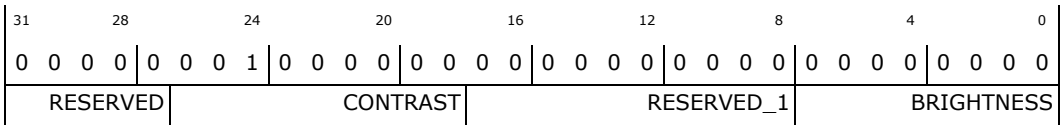
Sprite D Color Correction 0 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 724D0h

Default: 01000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** Reserved.
26:18	0x40 RW	**CONTRAST:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed-point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast, for YUV modes and for source data in RGB format, is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	0x0 RO	**RESERVED_1:** Reserved.
7:0	0x0 RW	**BRIGHTNESS:** This field provides the brightness adjustment with a 8-bit 2 s compliment value ranging [-128, +127]. This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8-bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of [-255, +255]. Bypassing Brightness for YUV formats and for source data in RGB format, is accomplished by programming this field to 0.

4.3.359 SPDCLRC1—Offset 724D4h

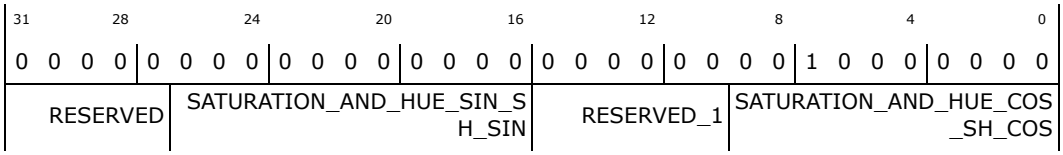
Sprite D Color Correction 1 Register

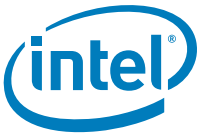
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 724D4h

Default: 00000080h





Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** Reserved.
26:16	0x0 RW	**SATURATION_AND_HUE_SIN_SH_SIN:** This 11-bit signed fixed-point number is in 2 s compliment (s3i.7f) format with the MSB as the sign, next 3 MSBs as the integer value and the last 7 LSBs as the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Hue, even for source data in RGB format, is accomplished by programming this field to 0.0.
15:10	0x0 RO	**RESERVED_1:** Reserved.
9:0	0x80 RW	**SATURATION_AND_HUE_COS_SH_COS:** This unsigned fixed-point number is in 3i.7f format with the first 3 MSBs be the integer value and the last 7 LSBs be the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Saturation, even for source data in RGB format, is accomplished by programming this field to 1.0.

4.3.360 SPDGAMC5—Offset 724E0h

Sprite D Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 724E0h

Default: 00C0C0C0h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	1 1 0 0	0 0 0 0	1 1 0 0	0 0 0 0	1 1 0 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0xc0 RW	**RED_V_CR:** Reserved.
15:8	0xc0 RW	**GREEN_Y:** Reserved.
7:0	0xc0 RW	**BLUE_U_CB:**

4.3.361 SPDGAMC4—Offset 724E4h

Sprite D Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 724E4h

Default: 00808080h

31 28	24	20	16	12	8	4 0
0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x80 RW	**RED_V_CR:** Reserved.
15:8	0x80 RW	**GREEN_Y:** Reserved.
7:0	0x80 RW	**BLUE_U_CB:**

4.3.362 SPDGAMC3—Offset 724E8h

Sprite D Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 724E8h

Default: 00404040h

31 28	24	20	16	12	8	4 0
0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 1 0 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x40 RW	**RED_V_CR:** Reserved.
15:8	0x40 RW	**GREEN_Y:** Reserved.
7:0	0x40 RW	**BLUE_U_CB:**

4.3.363 SPDGAMC2—Offset 724ECh

Sprite D Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 724ECh

Default: 00202020h

31 28	24	20	16	12	8	4 0
0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 1 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x20 RW	**RED_V_CR:** Reserved.
15:8	0x20 RW	**GREEN_Y:** Reserved.
7:0	0x20 RW	**BLUE_U_CB:**

4.3.364 SPDGAMC1—Offset 724F0h

Sprite D Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 724F0h

Default: 00101010h

31 28	24	20	16	12	8	4 0
0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x10 RW	**RED_V_CR:** Reserved.
15:8	0x10 RW	**GREEN_Y:** Reserved.
7:0	0x10 RW	**BLUE_U_CB:**

4.3.365 SPDGAMC0—Offset 724F4h

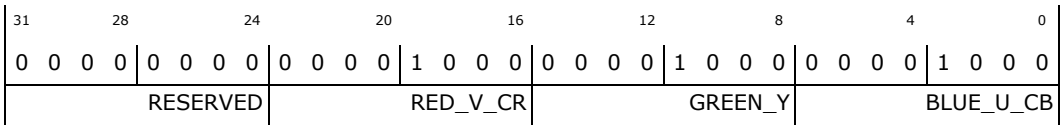
Sprite D Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 724F4h

Default: 00080808h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x8 RW	**RED_V_CR:** Reserved.
15:8	0x8 RW	**GREEN_Y:** Reserved.
7:0	0x8 RW	**BLUE_U_CB:**

4.3.366 SPECNTR—Offset 72580h

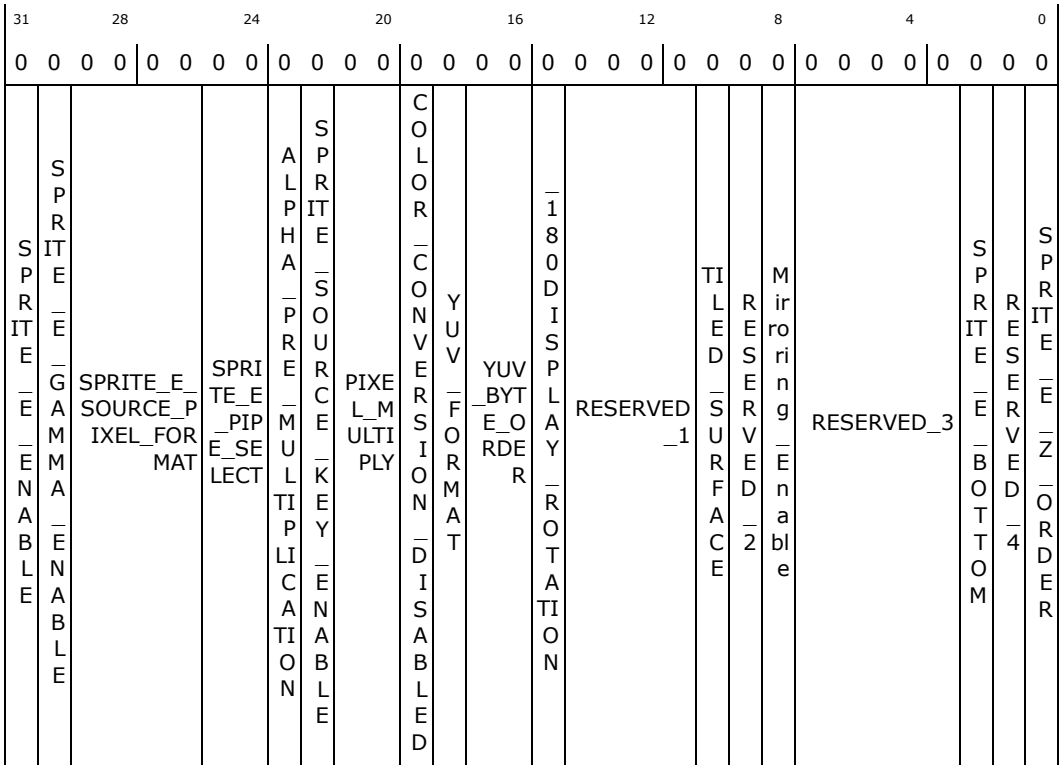
Sprite E Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 72580h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SPRITE_E_ENABLE:** This bit will enable or disable the Sprite E. When this bit is set, the plane will generate pixels for display to be combined by the blender for the target pipe. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted, this bit will be overridden and the display disabled when the registers are unlocked. 1 = Enable 0 = Disable
30	0x0 RW	**SPRITE_E_GAMMA_ENABLE:** There are two gamma adjustments possible in the Sprite E data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8-bit indexed, this bit should be set to a one. Gamma correction logic that is contained in the Sprite E logic is disabled by loading the default values into those registers. When this plane is marked as trusted, this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 = Sprite E pixel data bypasses the display pipe gamma correction logic (default). 1 = Sprite E pixel data is gamma corrected in the pipe gamma correction logic

Bit Range	Default & Access	Field Name (ID): Description
29:26	0x0 RW	**SPRITE_E_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite/Sprite E. Pixel formats with an alpha channel should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 0000 = YUV 4:2:2 packed (see byte order below). 0001 = Reserved 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format with pre-multiplied alpha channel. 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format 1010 = Reserved. 1011 = Reserved. 1100 = Reserved. 1101 = Reserved. 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8)
25:24	0x0 RW	**SPRITE_E_PIPE_SELECT:** Sprite E always ties to Pipe C. Reserved.
23	0x0 RO	**ALPHA_PRE_MULTIPLICATION:** This Bit allows plane logic to alpha multiply ARGB/RGBA pizels if they are not pre multiplied already. 0: RGB Components are pre multiplied with alpha channel of the pixel. 1: RGB components have not been multiplied with alpha channel of the pixel. Plane will performed multiplication before alpha blending.
22	0x0 RW	**SPRITE_SOURCE_KEY_ENABLE:** When used as a sprite in the 16/32-bpp modes without alpha this enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Setting this bit is not allowed when the Sprite E pixel format includes an alpha channel. [DevBW] Erratum: This bit must always be set to 0 when Sprite E pixel format is YUV 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled.
21:20	0x0 RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two (both H and V). 00 = No line/Pixel duplication 01 = Line/Pixel Doubling 10 = Line Doubling only 11 = Pixel Doubling only

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RW	**COLOR_CONVERSION_DISABLED:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4:2:2 packed format and x:8:8:8 and 8:8:8:8 formats. Formats such as RGB5:5:5 and 5:6:5 do not have YUV versions. 0 = Pixel data is sent through the conversion logic (only applies to YUV formats) 1 = Pixel data is not sent through the YUV-)RGB conversion logic.
18	0x0 RW	**YUV_FORMAT:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 = ITU-R Recommendation BT.601 1 = ITU-R Recommendation BT.709
17:16	0x0 RW	**YUV_BYTE_ORDER:** This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored. 00 = YUYV 01 = UYVY 10 = YVYU 11 = VYUY
15	0x0 RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner. 0 = No rotation 1 = 180 rotation
14:11	0x0 RO	**RESERVED_1:** Reserved.
10	0x0 RW	**TILED_SURFACE:** This bit indicates that the Sprite E surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPCTILEOFF, DSPCLINOFF, and DSPCSURFADDR registers. 0 = Sprite E surface uses linear memory 1 = Sprite E surface uses X-tiled memory
9	0x0 RO	**RESERVED_2:** Write as zero
8	0x0 RO	**Mirroring_Enable:** 0: Mirroring is not enabled. 1: Mirroring is enabled.
7:3	0x0 RO	**RESERVED_3:** Write as zero
2	0x0 RW	**SPRITE_E_BOTTOM:** This bit will force the Sprite E plane to be on the bottom of the Z order. If the plane is marked as trusted, it only applies to the Z order of the trusted planes. 0 = Sprite E Z order is determined by the other control bits 1 = Sprite E is forced to be on the bottom of the Z order.
1	0x0 RO	**RESERVED_4:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**SPRITE_E_Z_ORDER:** With Sprite C and D z-order, bottom control bits, Sprite E plane is placed in a specific z-order among other planes in pipe B. Display Pipe B Z-orders SC zorderSC bottomSD zorderSD bottomResulting Pipe Z-order (from bottom to top)Source Keying 0000PB SC SD CBPB in Black 1000PB SD SC CBPB in Black 0001SD PB SC CBuse src keying on SD 0011SD PB SC CBuse src keying on SD 1001SD SC PB CBuse src keying on SC 1011SD SC PB CBuse src keying on SC 0100SC PB SD CBuse src keying on SC 1100SC PB SD CBuse src keying on SC 0110SC SD PB CBuse src keying on SD 1110SC SD PB CBuse src keying on SD 0101Not Allowed 0111Not Allowed 1101Not Allowed 1111Not Allowed 1010Not Allowed 1011Not Allowed 0: Sprite E z-order is disabled 1: Sprite E z-order is enabled

4.3.367 SPELINOFF—Offset 72584h

Sprite E Linear Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72584h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
SPRITE_E_OFFSET								

Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SPRITE_E_OFFSET:** This register provides the panning offset into the Sprite E plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

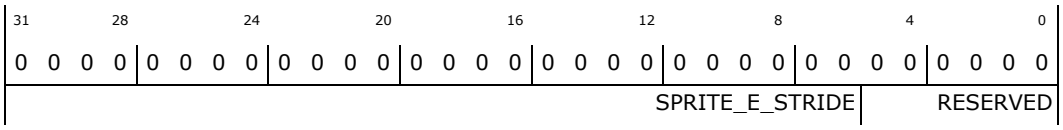
4.3.368 SPESTRIDE—Offset 72588h

Sprite E Stride Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72588h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**SPRITE_E_STRIDE:** This is the stride for Sprite E in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.
5:0	0x0 RO	**RESERVED:** Reserved.

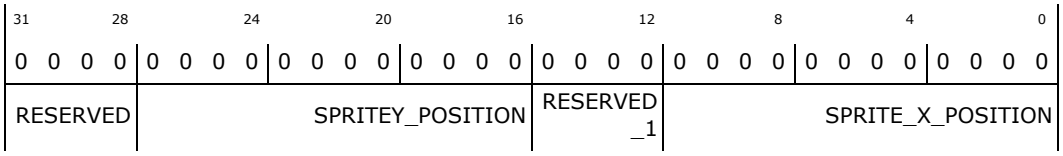
4.3.369 SPEPOS—Offset 7258Ch

Sprite E Position Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7258Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
27:16	0x0 RW	**SPRITEY_POSITION:** These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**SPRITE_X_POSITION:** These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180 rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

4.3.370 SPESIZE—Offset 72590h

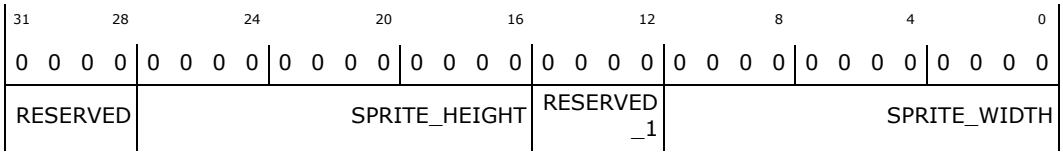
Sprite E Height and Width Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 72590h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**SPRITE_HEIGHT:** This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**SPRITE_WIDTH:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values when YUV source pixel format is used (actual width, not the width minus one value).

4.3.371 SPEKEYMINVAL—Offset 72594h

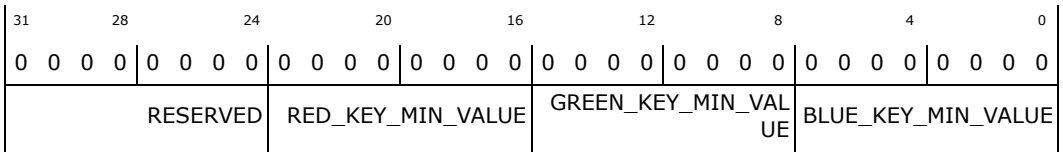
Sprite E Color Key Min Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 72594h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero
23:16	0x0 RW	**RED_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite red/Cr channel.
15:8	0x0 RW	**GREEN_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite green/Y channel.
7:0	0x0 RW	**BLUE_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite blue/Cb channel.

4.3.372 SPEKEYMSK—Offset 72598h

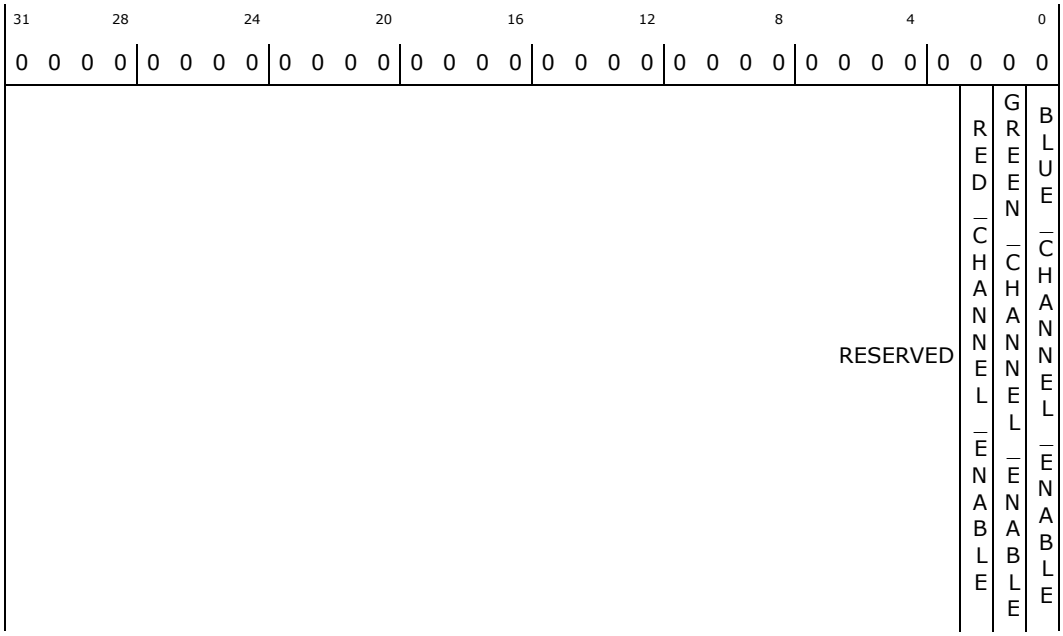
Sprite E Color Key Mask Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 72598h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**RESERVED:** Write as zero
2	0x0 RW	**RED_CHANNEL_ENABLE:** Specifies the source color key enable for the red/Cr channel.
1	0x0 RW	**GREEN_CHANNEL_ENABLE:** Specifies the source color key enable for the green/Y channel.
0	0x0 RW	**BLUE_CHANNEL_ENABLE:** Specifies the source color key enable for the blue/Cb channel

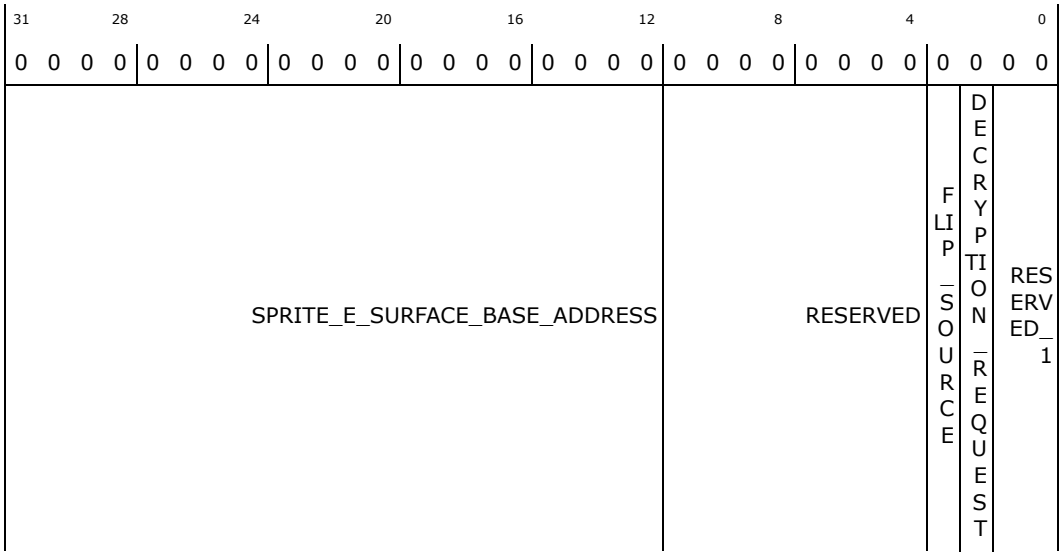
4.3.373 SPESURF—Offset 7259Ch

Sprite E Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7259Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**SPRITE_E_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register. This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . The value in this register is updated through the command streamer during synchronous flips. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0x0 RO	**RESERVED:** MBZ

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0x0 RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0x0 RO	**RESERVED_1:** MBZ

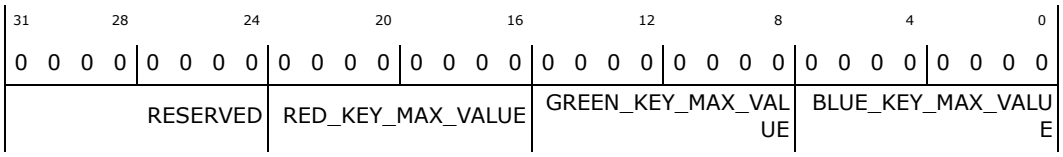
4.3.374 SPEKEYMAXVAL—Offset 725A0h

Sprite E Color Key Max Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 725A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero
23:16	0x0 RW	**RED_KEY_MAX_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0x0 RW	**GREEN_KEY_MAX_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0x0 RW	**BLUE_KEY_MAX_VALUE:** Specifies the color key value for the Sprite blue/Cb channel.

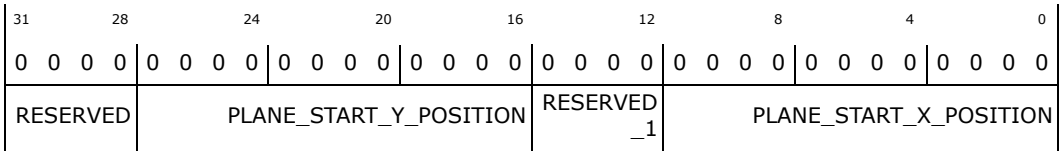
4.3.375 SPETILEOFF—Offset 725A4h

Sprite E Tiled Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 725A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

4.3.376 SPECONTALPHA—Offset 725A8h

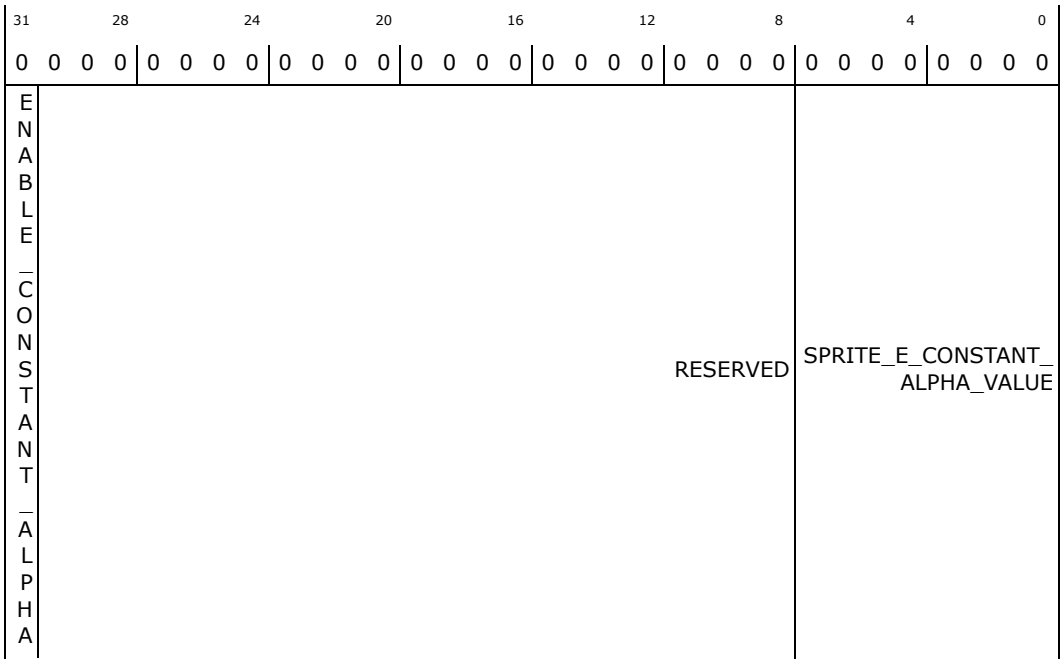
Sprite E Constant Alpha Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 725A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**ENABLE_CONSTANT_ALPHA:** Sprite E Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 Sprite E Constant Alpha is disabled 1 Sprite E Constant Alpha is enabled

Bit Range	Default & Access	Field Name (ID): Description
30:8	0x0 RO	**RESERVED:** MBZ
7:0	0x0 RW	**SPRITE_E_CONSTANT_ALPHA_VALUE:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

4.3.377 SPELIVESURF—Offset 725ACh

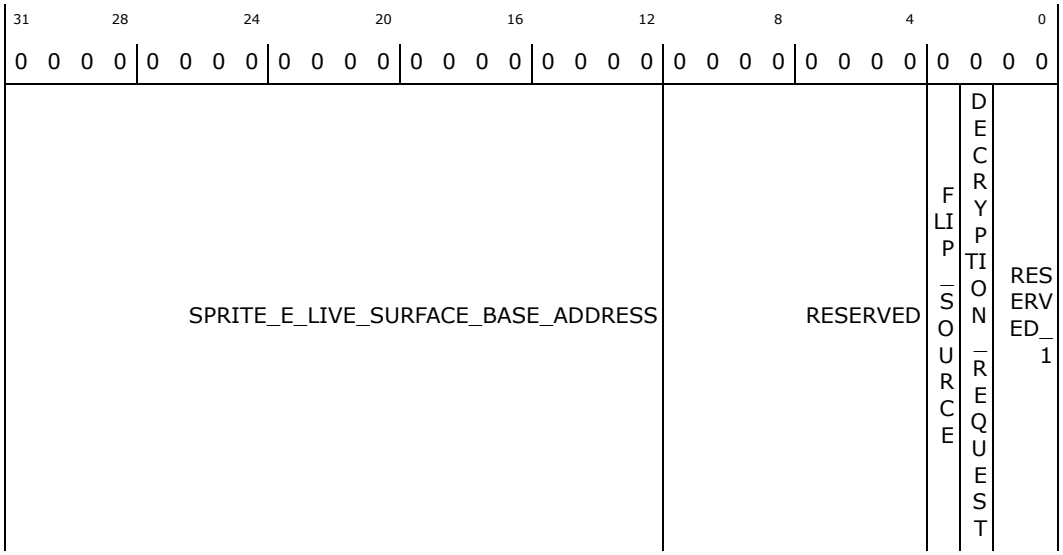
Sprite E Live Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 725ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**SPRITE_E_LIVE_SURFACE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for Sprite E
11:4	0x0 RO	**RESERVED:** MBZ

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RO	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0x0 RO	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0x0 RO	**RESERVED_1:** MBZ

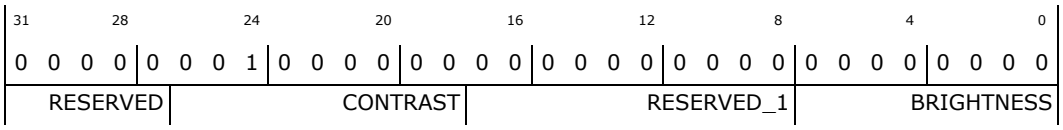
4.3.378 SPECLRC0—Offset 725D0h

Sprite E Color Correction 0 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 725D0h

Default: 01000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** Reserved.
26:18	0x40 RW	**CONTRAST:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed-point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast, for YUV modes and for source data in RGB format, is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	0x0 RO	**RESERVED_1:** Reserved.
7:0	0x0 RW	**BRIGHTNESS:** This field provides the brightness adjustment with a 8-bit 2 s compliment value ranging [-128, +127]. This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8-bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of [-255, +255]. Bypassing Brightness for YUV formats and for source data in RGB format, is accomplished by programming this field to 0.

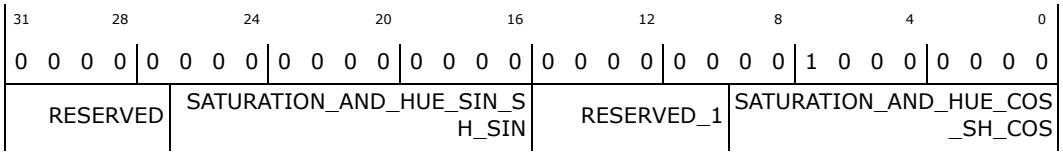
4.3.379 SPECLRC1—Offset 725D4h

Sprite E Color Correction 1 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 725D4h

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** Reserved.
26:16	0x0 RW	**SATURATION_AND_HUE_SIN_SH_SIN:** This 11-bit signed fixed-point number is in 2 s compliment (s3i.7f) format with the MSB as the sign, next 3 MSBs as the integer value and the last 7 LSBs as the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Hue, even for source data in RGB format, is accomplished by programming this field to 0.0.
15:10	0x0 RO	**RESERVED_1:** Reserved.
9:0	0x80 RW	**SATURATION_AND_HUE_COS_SH_COS:** This unsigned fixed-point number is in 3i.7f format with the first 3 MSBs be the integer value and the last 7 LSBs be the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Saturation, even for source data in RGB format, is accomplished by programming this field to 1.0.

4.3.380 SPEGAMC5—Offset 725E0h

Sprite E Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 725E0h

Default: 00C0C0C0h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	1 1 0 0	0 0 0 0	1 1 0 0	0 0 0 0	1 1 0 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0xc0 RW	**RED_V_CR:** Reserved.
15:8	0xc0 RW	**GREEN_Y:** Reserved.
7:0	0xc0 RW	**BLUE_U_CB:**

4.3.381 SPEGAMC4—Offset 725E4h

Sprite E Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 725E4h

Default: 00808080h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x80 RW	**RED_V_CR:** Reserved.
15:8	0x80 RW	**GREEN_Y:** Reserved.
7:0	0x80 RW	**BLUE_U_CB:**

4.3.382 SPEGAMC3—Offset 725E8h

Sprite E Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 725E8h

Default: 00404040h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 1 0 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x40 RW	**RED_V_CR:** Reserved.
15:8	0x40 RW	**GREEN_Y:** Reserved.
7:0	0x40 RW	**BLUE_U_CB:**

4.3.383 SPEGAMC2—Offset 725ECh

Sprite E Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 725ECh

Default: 00202020h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 1 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x20 RW	**RED_V_CR:** Reserved.
15:8	0x20 RW	**GREEN_Y:** Reserved.
7:0	0x20 RW	**BLUE_U_CB:**

4.3.384 SPEGAMC1—Offset 725F0h

Sprite E Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 725F0h

Default: 00101010h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x10 RW	**RED_V_CR:** Reserved.
15:8	0x10 RW	**GREEN_Y:** Reserved.
7:0	0x10 RW	**BLUE_U_CB:**

4.3.385 SPEGAMC0—Offset 725F4h

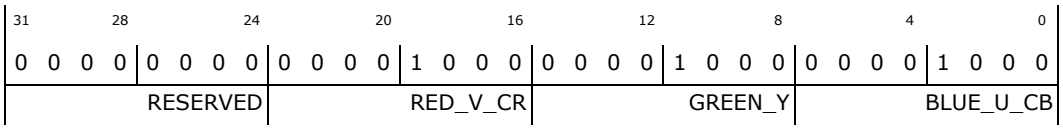
Sprite E Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 725F4h

Default: 00080808h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x8 RW	**RED_V_CR:** Reserved.
15:8	0x8 RW	**GREEN_Y:** Reserved.
7:0	0x8 RW	**BLUE_U_CB:**

4.3.386 SPFCNTR—Offset 72680h

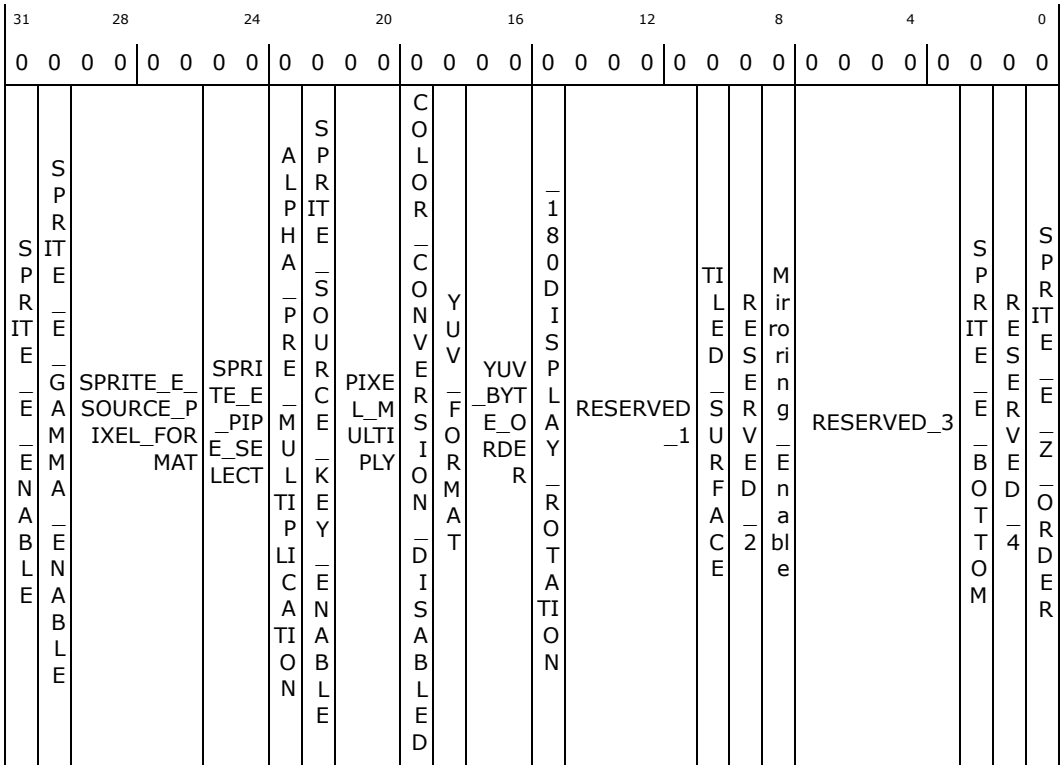
Sprite F Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 72680h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SPRITE_E_ENABLE:** This bit will enable or disable the Sprite F. When this bit is set, the plane will generate pixels for display to be combined by the blender for the target pipe. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted, this bit will be overridden and the display disabled when the registers are unlocked. 1 = Enable 0 = Disable
30	0x0 RW	**SPRITE_E_GAMMA_ENABLE:** There are two gamma adjustments possible in the Sprite F data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8-bit indexed, this bit should be set to a one. Gamma correction logic that is contained in the Sprite F logic is disabled by loading the default values into those registers. When this plane is marked as trusted, this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 = Sprite F pixel data bypasses the display pipe gamma correction logic (default). 1 = Sprite F pixel data is gamma corrected in the pipe gamma correction logic

Bit Range	Default & Access	Field Name (ID): Description
29:26	0x0 RW	**SPRITE_E_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite/Sprite F. Pixel formats with an alpha channel should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 0000 = YUV 4:2:2 packed (see byte order below). 0001 = Reserved 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format with pre-multiplied alpha channel. 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format 1010 = Reserved. 1011 = Reserved. 1100 = Reserved. 1101 = Reserved. 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8)
25:24	0x0 RW	**SPRITE_E_PIPE_SELECT:** Sprite F always ties to Pipe C. Reserved.
23	0x0 RO	**ALPHA_PRE_MULTIPLICATION:** This Bit allows plane logic to alpha multiply ARGB/RGBA pizels if they are not pre multiplied already. 0: RGB Components are pre multiplied with alpha channel of the pixel. 1: RGB components have not been multiplied with alpha channel of the pixel. Plane will performed multiplication before alpha blending.
22	0x0 RW	**SPRITE_SOURCE_KEY_ENABLE:** When used as a sprite in the 16/32-bpp modes without alpha this enables source color keying. Sprite pixel values that match (within range) the key will become transparent. Setting this bit is not allowed when the Sprite F pixel format includes an alpha channel. [DevBW] Erratum: This bit must always be set to 0 when Sprite F pixel format is YUV 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled.
21:20	0x0 RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two (both H and V). 00 = No line/Pixel duplication 01 = Line/Pixel Doubling 10 = Line Doubling only 11 = Pixel Doubling only

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RW	**COLOR_CONVERSION_DISABLED:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4:2:2 packed format and x:8:8:8 and 8:8:8:8 formats. Formats such as RGB5:5:5 and 5:6:5 do not have YUV versions. 0 = Pixel data is sent through the conversion logic (only applies to YUV formats) 1 = Pixel data is not sent through the YUV-)RGB conversion logic.
18	0x0 RW	**YUV_FORMAT:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 = ITU-R Recommendation BT.601 1 = ITU-R Recommendation BT.709
17:16	0x0 RW	**YUV_BYTE_ORDER:** This field is used to select the byte order when using YUV 4:2:2 data formats. For other formats, this field is ignored. 00 = YUYV 01 = UYVY 10 = YVYU 11 = VYUY
15	0x0 RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image and calculate the x, y offset as relative to the lower right corner. 0 = No rotation 1 = 180 rotation
14:11	0x0 RO	**RESERVED_1:** Reserved.
10	0x0 RW	**TILED_SURFACE:** This bit indicates that the Sprite F surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPCTILEOFF, DSPCLINOFF, and DSPCSURFADDR registers. 0 = Sprite F surface uses linear memory 1 = Sprite F surface uses X-tiled memory
9	0x0 RO	**RESERVED_2:** Write as zero
8	0x0 RO	**Mirroring_Enable:** 0: Mirroring is not enabled. 1: Mirroring is enabled.
7:3	0x0 RO	**RESERVED_3:** Write as zero
2	0x0 RW	**SPRITE_E_BOTTOM:** This bit will force the Sprite F plane to be on the bottom of the Z order. If the plane is marked as trusted, it only applies to the Z order of the trusted planes. 0 = Sprite F Z order is determined by the other control bits 1 = Sprite F is forced to be on the bottom of the Z order.
1	0x0 RO	**RESERVED_4:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**SPRITE_E_Z_ORDER:** With Sprite C and D z-order, bottom control bits, Sprite F plane is placed in a specific z-order among other planes in Pipe C. Display Pipe C Z-orders SC zorderSC bottomSD zorderSD bottomResulting Pipe Z-order (from bottom to top)Source Keying 0000PB SC SD CBPB in Black 1000PB SD SC CBPB in Black 0001SD PB SC CBuse src keying on SD 0011SD PB SC CBuse src keying on SD 1001SD SC PB CBuse src keying on SC 1011SD SC PB CBuse src keying on SC 0100SC PB SD CBuse src keying on SC 1100SC PB SD CBuse src keying on SC 0110SC SD PB CBuse src keying on SD 1110SC SD PB CBuse src keying on SD 0101Not Allowed 0111Not Allowed 1101Not Allowed 1111Not Allowed 1010Not Allowed 1011Not Allowed 0: Sprite F z-order is disabled 1: Sprite F z-order is enabled

4.3.387 SPFLINOFF—Offset 72684h

Sprite F Linear Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 72684h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	
SPRITE_E_OFFSET								

Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SPRITE_E_OFFSET:** This register provides the panning offset into the Sprite F plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

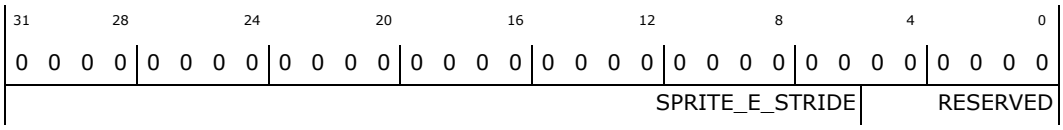
4.3.388 SPFSTRIDE—Offset 72688h

Sprite F Stride Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72688h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**SPRITE_E_STRIDE:** This is the stride for Sprite F in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes.
5:0	0x0 RO	**RESERVED:** Reserved.

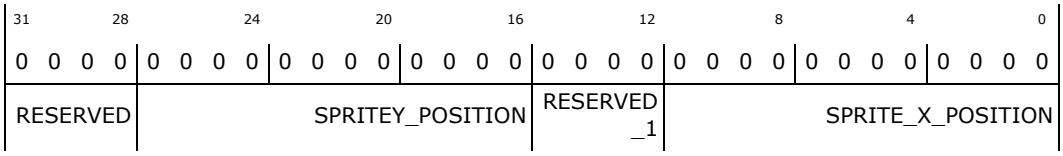
4.3.389 SPFPOS—Offset 7268Ch

Sprite F Position Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7268Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero

Bit Range	Default & Access	Field Name (ID): Description
27:16	0x0 RW	**SPRITEY_POSITION:** These 12 bits specify the vertical position in lines of the sprite (upper left corner) relative to the beginning of the active video area. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**SPRITE_X_POSITION:** These 12 bits specify the horizontal position in pixels of the sprite (upper left corner) relative the beginning of the active video area. When performing 180 rotation, this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the unrotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

4.3.390 SPFSIZE—Offset 72690h

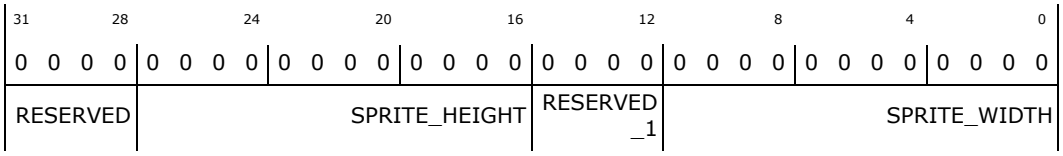
Sprite F Height and Width Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 72690h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**SPRITE_HEIGHT:** This register field is used to SPFcify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**SPRITE_WIDTH:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride (converted to pixels). The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values when YUV source pixel format is used (actual width, not the width minus one value).

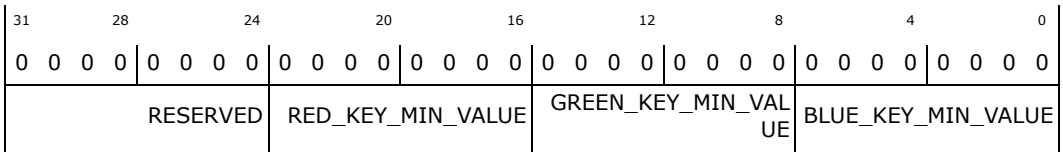
4.3.391 SPFKEYMINVAL—Offset 72694h

Sprite F Color Key Min Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72694h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero
23:16	0x0 RW	**RED_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite red/Cr channel.
15:8	0x0 RW	**GREEN_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite green/Y channel.
7:0	0x0 RW	**BLUE_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite blue/Cb channel.

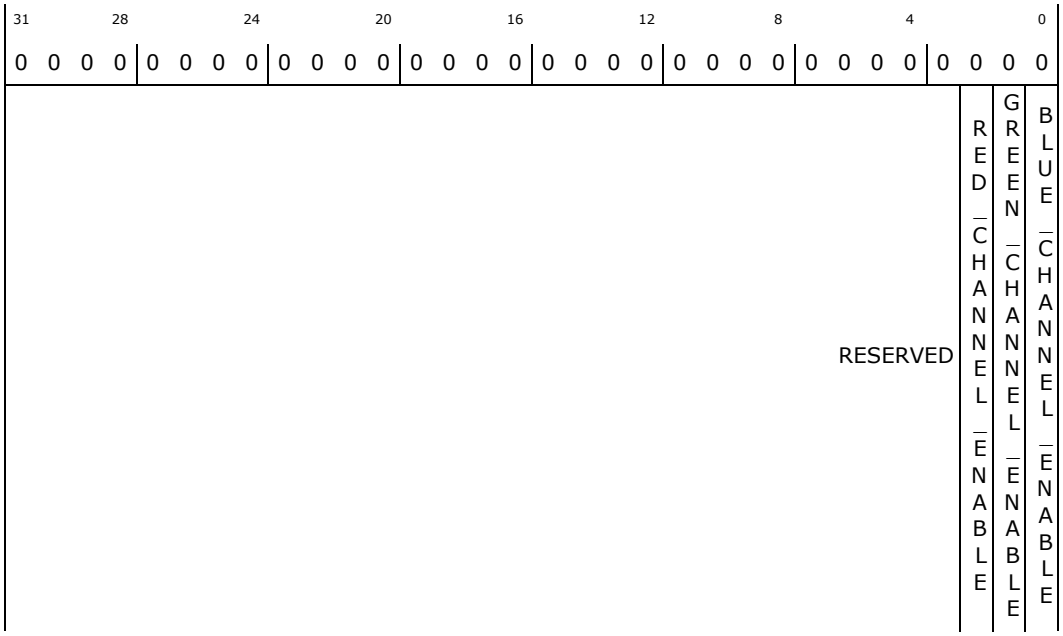
4.3.392 SPFKEYMSK—Offset 72698h

Sprite F Color Key Mask Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 72698h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**RESERVED:** Write as zero
2	0x0 RW	**RED_CHANNEL_ENABLE:** Specifies the source color key enable for the red/Cr channel.
1	0x0 RW	**GREEN_CHANNEL_ENABLE:** Specifies the source color key enable for the green/Y channel.
0	0x0 RW	**BLUE_CHANNEL_ENABLE:** Specifies the source color key enable for the blue/Cb channel

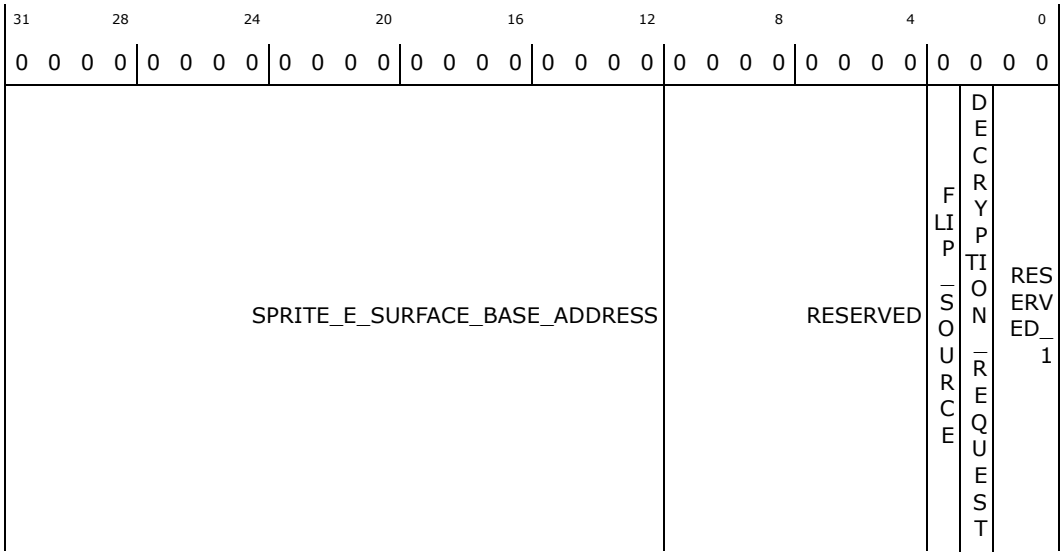
4.3.393 SPFSURF—Offset 7269Ch

Sprite F Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7269Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**SPRITE_E_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register. This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . The value in this register is updated through the command streamer during synchronous flips. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0x0 RO	**RESERVED:** MBZ

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0x0 RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0x0 RO	**RESERVED_1:** MBZ

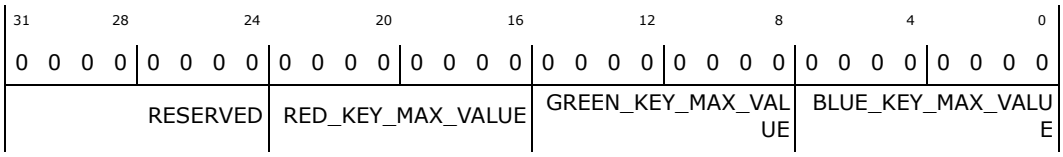
4.3.394 SPFKEYMAXVAL—Offset 726A0h

Sprite F Color Key Max Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 726A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:** Write as zero
23:16	0x0 RW	**RED_KEY_MAX_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0x0 RW	**GREEN_KEY_MAX_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0x0 RW	**BLUE_KEY_MAX_VALUE:** Specifies the color key value for the Sprite blue/Cb channel.

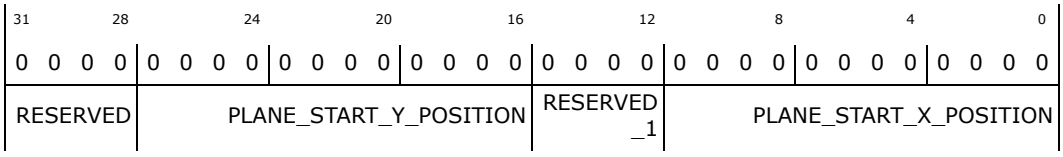
4.3.395 SPFTILEOFF—Offset 726A4h

Sprite F Tiled Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 726A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation.

4.3.396 SPFCONTALPHA—Offset 726A8h

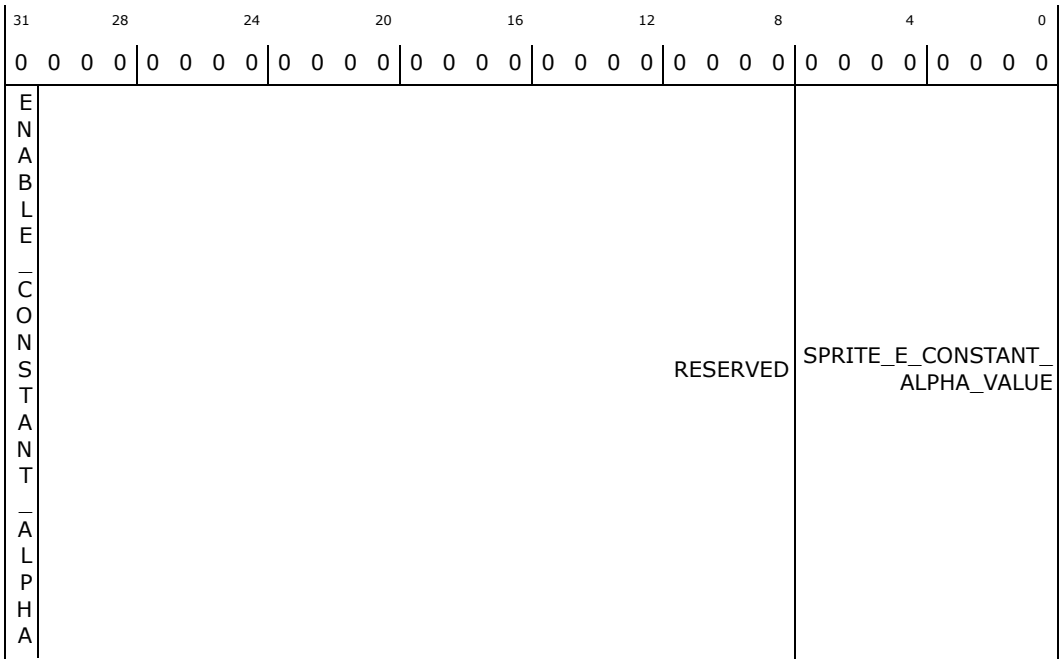
Sprite F Constant Alpha Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 726A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**ENABLE_CONSTANT_ALPHA:** Sprite F Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 Sprite F Constant Alpha is disabled 1 Sprite F Constant Alpha is enabled

Bit Range	Default & Access	Field Name (ID): Description
30:8	0x0 RO	**RESERVED:** MBZ
7:0	0x0 RW	**SPRITE_E_CONSTANT_ALPHA_VALUE:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

4.3.397 SPFLIVESURF—Offset 726ACh

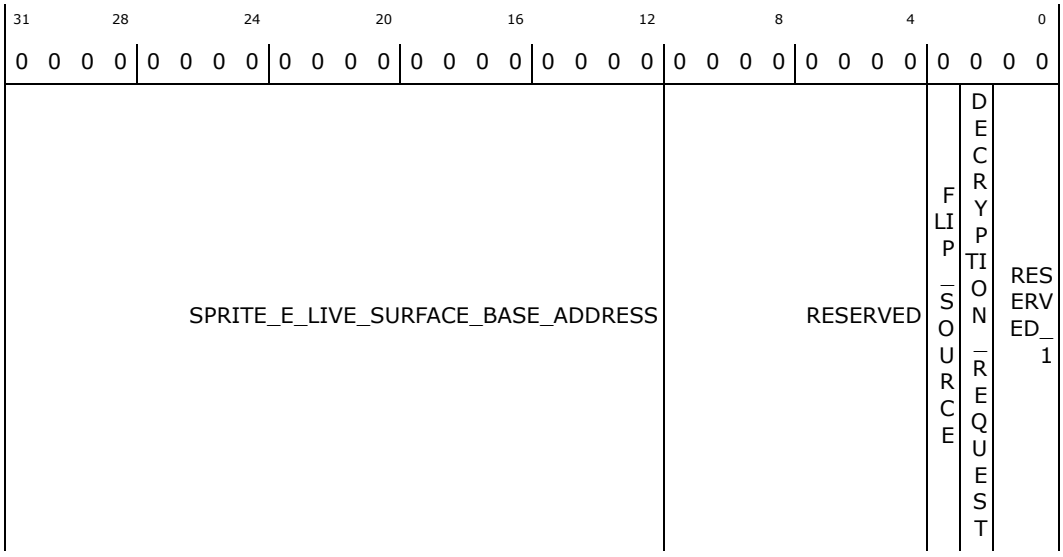
Sprite F Live Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 726ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**SPRITE_E_LIVE_SURFACE_BASE_ADDRESS:** This gives the live value of the surface base address as being currently used for Sprite F
11:4	0x0 RO	**RESERVED:** MBZ

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RO	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0x0 RO	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register. ValueNameDescriptionProject 0b Not requested Decrytpion not requested All 1b Requested Decryption requested All
1:0	0x0 RO	**RESERVED_1:** MBZ

4.3.398 SPFCLRC0—Offset 726D0h

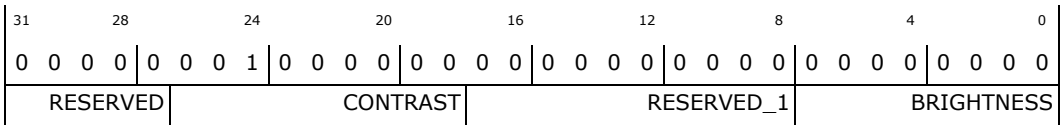
Sprite F Color Correction 0 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 726D0h

Default: 01000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** Reserved.
26:18	0x40 RW	**CONTRAST:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed-point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast, for YUV modes and for source data in RGB format, is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	0x0 RO	**RESERVED_1:** Reserved.
7:0	0x0 RW	**BRIGHTNESS:** This field provides the brightness adjustment with a 8-bit 2 s compliment value ranging [-128, +127]. This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8-bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of [-255, +255]. Bypassing Brightness for YUV formats and for source data in RGB format, is accomplished by programming this field to 0.

4.3.399 SPFCLRC1—Offset 726D4h

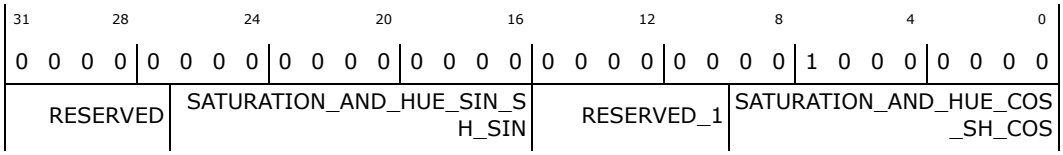
Sprite F Color Correction 1 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 726D4h

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED:** Reserved.
26:16	0x0 RW	**SATURATION_AND_HUE_SIN_SH_SIN:** This 11-bit signed fixed-point number is in 2 s compliment (s3i.7f) format with the MSB as the sign, next 3 MSBs as the integer value and the last 7 LSBs as the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Hue, even for source data in RGB format, is accomplished by programming this field to 0.0.
15:10	0x0 RO	**RESERVED_1:** Reserved.
9:0	0x80 RW	**SATURATION_AND_HUE_COS_SH_COS:** This unsigned fixed-point number is in 3i.7f format with the first 3 MSBs be the integer value and the last 7 LSBs be the fraction value. This field can be used in two modes. When full range YUV data is operated on, this field contains the saturation value. When the range-limited YCbCr data is used, software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor (=128/112). Similar to the contrast field, there is no limit for saturation reduction saturation = 0 means all pixels become the same value. However, increasing contrast can only be increased by a factor less than 8. For example, the largest contrast with value of 0x7.7F can bring input range [0, 32] to a full display color range of [0, 255]. Bypassing Saturation, even for source data in RGB format, is accomplished by programming this field to 1.0.

4.3.400 SPFGAMC5—Offset 726E0h

Sprite F Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 726E0h

Default: 00C0C0C0h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	1 1 0 0	0 0 0 0	1 1 0 0	0 0 0 0	1 1 0 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0xc0 RW	**RED_V_CR:** Reserved.
15:8	0xc0 RW	**GREEN_Y:** Reserved.
7:0	0xc0 RW	**BLUE_U_CB:**

4.3.401 SPFGAMC4—Offset 726E4h

Sprite F Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 726E4h

Default: 00808080h

31 28	24	20	16	12	8	4 0
0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x80 RW	**RED_V_CR:** Reserved.
15:8	0x80 RW	**GREEN_Y:** Reserved.
7:0	0x80 RW	**BLUE_U_CB:**

4.3.402 SPFGAMC3—Offset 726E8h

Sprite F Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 726E8h

Default: 00404040h

31 28	24	20	16	12	8	4 0
0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 1 0 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB	

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x40 RW	**RED_V_CR:** Reserved.
15:8	0x40 RW	**GREEN_Y:** Reserved.
7:0	0x40 RW	**BLUE_U_CB:**

4.3.403 SPFGAMC2—Offset 726ECh

Sprite F Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 726ECh

Default: 00202020h

31 28	24	20	16	12	8	4 0
0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 1 0	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x20 RW	**RED_V_CR:** Reserved.
15:8	0x20 RW	**GREEN_Y:** Reserved.
7:0	0x20 RW	**BLUE_U_CB:**

4.3.404 SPFGAMC1—Offset 726F0h

Sprite F Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 726F0h

Default: 00101010h

31 28	24	20	16	12	8	4 0
0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 0
RESERVED		RED_V_CR		GREEN_Y		BLUE_U_CB

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x10 RW	**RED_V_CR:** Reserved.
15:8	0x10 RW	**GREEN_Y:** Reserved.
7:0	0x10 RW	**BLUE_U_CB:**

4.3.405 SPFGAMC0—Offset 726F4h

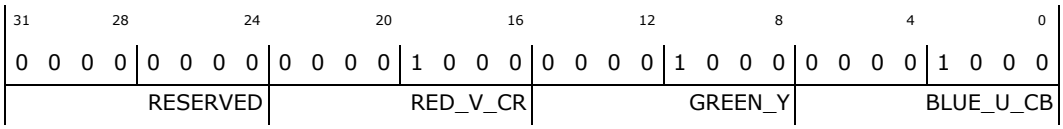
Sprite F Gamma Correction Registers

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 726F4h

Default: 00080808h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x8 RW	**RED_V_CR:** Reserved.
15:8	0x8 RW	**GREEN_Y:** Reserved.
7:0	0x8 RW	**BLUE_U_CB:**

4.3.406 PCSRC—Offset 73000h

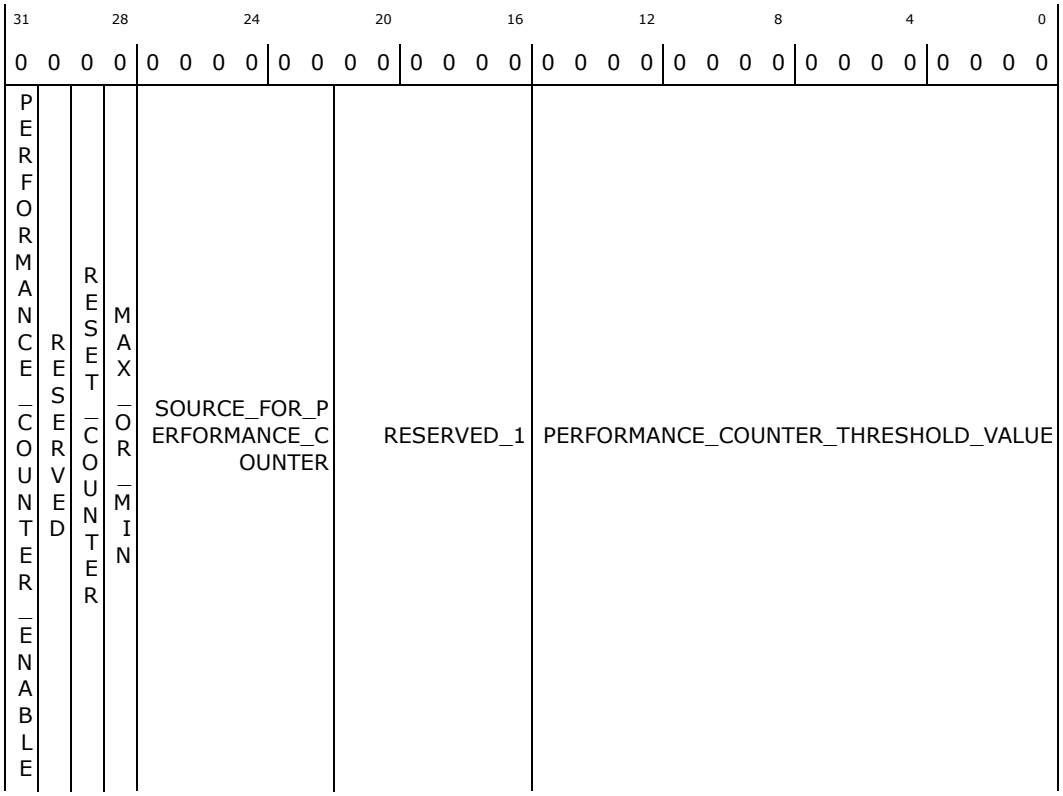
Performance Counter Source Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 73000h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**PERFORMANCE_COUNTER_ENABLE:** This bit enables the performance counter. 0 = Performance counter is disabled 1 = Performance counter is enabled.
30	0x0 RO	**RESERVED:** Reserved.
29	0x0 RW	**RESET_COUNTER:** This bit indicates when the counter will be reset. 1 = Reset after each frame, summing all events in the frame 0 = Reset after each event within the frame
28	0x0 RW	**MAX_OR_MIN:** This bit tells whether the stored counter value for an event is the maximum or the minimum value. The previous value is used to do the compare. 0 = Stored value is the maximum latency 1 = Stored value is the minimum latency

Bit Range	Default & Access	Field Name (ID): Description
27:22	0x0 RW	**SOURCE_FOR_PERFORMANCE_COUNTER:** These bits indicate the source for the performance counter. 000000 = Overlay Register Request Latency [DevBW] and [DevCL] 000001 = Font Request Latency 000010 = Character Request Latency 000011 = Display A FIFO Status 000100 = Display B FIFO Status 000101 = Sprite A FIFO Status 000110 = Cursor A FIFO Status 000111 = Cursor B FIFO Status 001000 = Display Steamer A TLB Latency 001001 = Display Streamer B TLB Latency 001010 = Sprite Streamer A TLB Latency 001011 = Cursor Streamer A TLB Latency 001100 = Cursor Streamer B TLB Latency 001101 = Overlay Streamer TLB Latency [DevBW] and [DevCL] 001110 = Display Steamer A Request Latency 001111 = Display Streamer B Request Latency 010000 = Sprite Streamer A Request Latency 010001 = Cursor Streamer A Request Latency 010010 = Cursor Streamer B Request Latency 010011 = Overlay Streamer Request Latency [DevBW] and [DevCL] 010100 = Display A Command Request Latency 010101 = Display B Command Request Latency 010110 = Sprite A Command Request Latency 010111 = Cursor A Command Request Latency 011000 = Cursor B Command Request Latency 011001 = Overlay Command Request Latency [DevBW] and [DevCL] 011010 = DPFC Dummy Read [DevCTG] 011011 = DPFC Self Refresh [DevCTG] 011100 = Sprite B FIFO status 011101 = Sprite C FIFO status 011110 = Sprite D FIFO status 011111 = Sprite B TLB Request Latency 100000 = Sprite C TLB Request Latency 100001 = Sprite D TLB Request Latency 100010 = Sprite B Request Latency 100011 = Sprite C Request Latency 100100 = Sprite D Request Latency 100101 = Sprite B Command Request Latency 100110 = Sprite C Command Request Latency 100111 = Sprite D Command Request Latency 101000 = SR exit to data HP Put (measure the latency from the SRexit failing edge to the first data HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA) 101001 = InSR to data HP Put (measure the latency from any data request made during inSR is active to the first data HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA) 101010 = SR exit to TLB HP Put (measure the latency from the SRexit failing edge to the first TLB HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA) 101011 = InSR to TLB HP Put (measure the latency from any TLB request made during inSR is active to the first TLB HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA)

Bit Range	Default & Access	Field Name (ID): Description
21:16	0x0 RO	**RESERVED_1:** Write as zero.
15:0	0x0 RW	**PERFORMANCE_COUNTER_THRESHOLD_VALUE:** This value is used to compare against the performance counter. If the performance counter matches this value, an interrupt is generated if the interrupt bit is enabled. When the source selected is DDB FIFO status, the threshold value is used to program the value needed to monitor in the DDB FIFO. No interrupt is generated in this condition.

4.3.407 PCSTAT—Offset 73004h

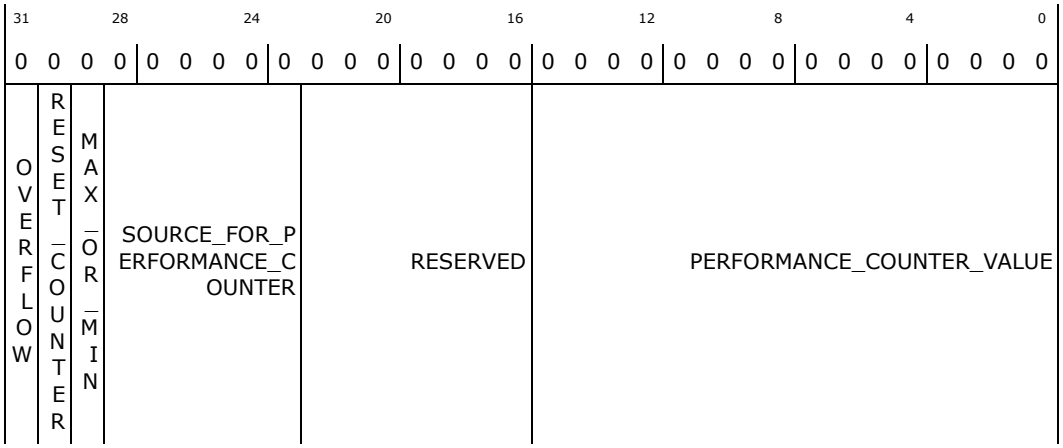
Performance Counter Status Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 73004h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**OVERFLOW:** This bit indicates weather the 16 bit counter overflowed or not. 0 = Counter is valid 1 = Counter is invalid since it overflowed
30	0x0 RO	**RESET_COUNTER:** This bit indicates when the counter will be reset. 1 = Reset after each frame, sum of all event in the frame 0 = Reset after each event within the frame
29	0x0 RO	**MAX_OR_MIN:** This bit tells whether the stored counter value for an event is the maximum or the minimum value of the previous event. 0 = Stored value is the maximum latency 1 = Stored value is the minimum latency

Bit Range	Default & Access	Field Name (ID): Description
28:23	0x0 RO	**SOURCE_FOR_PERFORMANCE_COUNTER:** These bits indicate the source for the performance counter. 000000 = Overlay Register Request Latency [DevBW] and [DevCL] 000001 = Font Request Latency 000010 = Character Request Latency 000011 = Display A FIFO Status 000100 = Display B FIFO Status 000101 = Sprite A FIFO Status 000110 = Cursor A FIFO Status 000111 = Cursor B FIFO Status 001000 = Display Steamer A TLB Latency 001001 = Display Streamer B TLB Latency 001010 = Sprite Streamer A TLB Latency 001011 = Cursor Streamer A TLB Latency 001100 = Cursor Streamer B TLB Latency 001101 = Overlay Streamer TLB Latency [DevBW] and [DevCL] 001110 = Display Steamer A Request Latency 001111 = Display Streamer B Request Latency 010000 = Sprite Streamer A Request Latency 010001 = Cursor Streamer A Request Latency 010010 = Cursor Streamer B Request Latency 010011 = Overlay Streamer Request Latency [DevBW] and [DevCL] 010100 = Display A Command Request Latency 010101 = Display B Command Request Latency 010110 = Sprite A Command Request Latency 010111 = Cursor A Command Request Latency 011000 = Cursor B Command Request Latency 011001 = Overlay Command Request Latency [DevBW] and [DevCL] 011010 = DPFC Dummy Read [DevCTG] 011011 = DPFC Self Refresh [DevCTG] 011100 = Sprite B FIFO status 011101 = Sprite C FIFO status 011110 = Sprite D FIFO status 011111 = Sprite B TLB Request Latency 100000 = Sprite C TLB Request Latency 100001 = Sprite D TLB Request Latency 100010 = Sprite B Request Latency 100011 = Sprite C Request Latency 100100 = Sprite D Request Latency 100101 = Sprite B Command Request Latency 100110 = Sprite C Command Request Latency 100111 = Sprite D Command Request Latency 101000 = SR exit to data HP Put (measure the latency from the SRexit failing edge to the first data HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA) 101001 = InSR to data HP Put (measure the latency from any data request made during inSR is active to the first data HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA) 101010 = SR exit to TLB HP Put (measure the latency from the SRexit failing edge to the first TLB HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA) 101011 = InSR to TLB HP Put (measure the latency from any TLB request made during inSR is active to the first TLB HP Put. This event shall be measured by either planeA, SpriteA, SpriteB, or CurA in pipeA)

Bit Range	Default & Access	Field Name (ID): Description
22:16	0x0 RO	**RESERVED:** Write as zero.
15:0	0x0 RO	**PERFORMANCE_COUNTER_VALUE:** This is the value of the performance counter for the source indicated in the source field.

4.3.408 PCSRC2—Offset 73008h

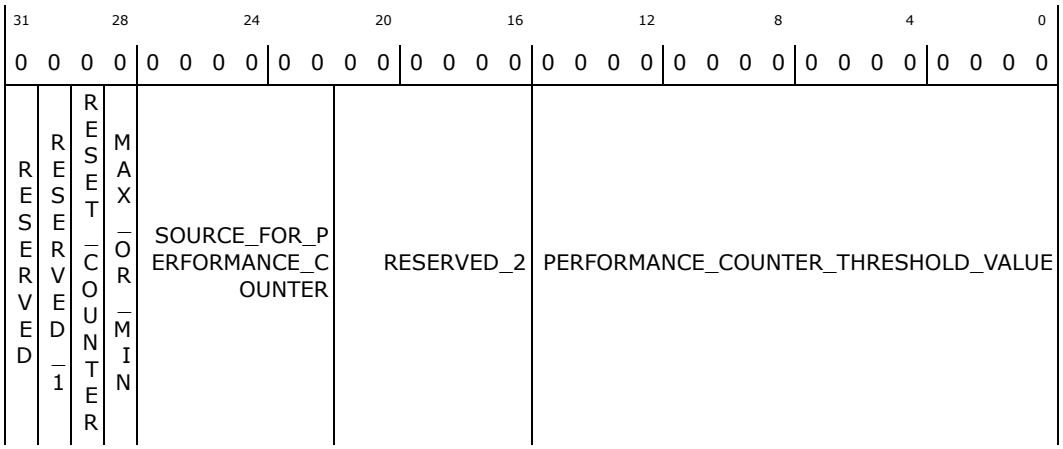
Performance Counter Source2 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 73008h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** Programming note: This second performance counter is enabled by the enable bit in the PCSRC1 bit 31.
30	0x0 RO	**RESERVED_1:** Reserved.
29	0x0 RW	**RESET_COUNTER:** This bit indicates when the counter will be reset. 1 = Reset after each frame, summing all events in the frame 0 = Reset after each event within the frame
28	0x0 RW	**MAX_OR_MIN:** This bit tells whether the stored counter value for an event is the maximum or the minimum value. The previous value is used to do the compare. 0 = Stored value is the maximum latency 1 = Stored value is the minimum latency

Bit Range	Default & Access	Field Name (ID): Description
27:22	0x0 RW	**SOURCE_FOR_PERFORMANCE_COUNTER:** These bits indicate the source for the performance counter. 000000 = Overlay Register Request Latency [DevBW] and [DevCL] 000001 = Font Request Latency 000010 = Character Request Latency 000011 = Display A FIFO Status 000100 = Display B FIFO Status 000101 = Sprite A FIFO Status 000110 = Cursor A FIFO Status 000111 = Cursor B FIFO Status 001000 = Display Streamer A TLB Latency 001001 = Display Streamer B TLB Latency 001010 = Sprite Streamer A TLB Latency 001011 = Cursor Streamer A TLB Latency 001100 = Cursor Streamer B TLB Latency 001101 = Overlay Streamer TLB Latency [DevBW] and [DevCL] 001110 = Display Streamer A Request Latency 001111 = Display Streamer B Request Latency 010000 = Sprite Streamer A Request Latency 010001 = Cursor Streamer A Request Latency 010010 = Cursor Streamer B Request Latency 010011 = Overlay Streamer Request Latency [DevBW] and [DevCL] 010100 = Display A Command Request Latency 010101 = Display B Command Request Latency 010110 = Sprite A Command Request Latency 010111 = Cursor A Command Request Latency 011000 = Cursor B Command Request Latency 011001 = Overlay Command Request Latency [DevBW] and [DevCL] 011010 = DPFC Dummy Read [DevCTG] 011011 = DPFC Self Refresh [DevCTG] 011100 = Sprite B FIFO status 011101 = Sprite C FIFO status 011110 = Sprite D FIFO status 011111 = Sprite B TLB Request Latency 100000 = Sprite C TLB Request Latency 100001 = Sprite D TLB Request Latency 100010 = Sprite B Request Latency 100011 = Sprite C Request Latency 100100 = Sprite D Request Latency 100101 = Sprite B Command Request Latency 100110 = Sprite C Command Request Latency 100111 = Sprite D Command Request Latency 101000 = SR exit to data HP Put (measure the latency from the SRexit failing edge to the first data HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101001 = InSR to data HP Put (measure the latency from any data request made during inSR is active to the first data HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101010 = SR exit to TLB HP Put (measure the latency from the SRexit failing edge to the first TLB HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101011 = InSR to TLB HP Put (measure the latency from any TLB request made during inSR is active to the first TLB HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB)

Bit Range	Default & Access	Field Name (ID): Description
21:16	0x0 RO	**RESERVED_2:** Write as zero.
15:0	0x0 RW	**PERFORMANCE_COUNTER_THRESHOLD_VALUE:** This value is used to compare against the performance counter. If the performance counter matches this value, an interrupt is generated if the interrupt bit is enabled. When the source selected is DDB FIFO status, the threshold value is used to program the value needed to monitor in the DDB FIFO. No interrupt is generated in this condition.

4.3.409 PCSTAT2—Offset 7300Ch

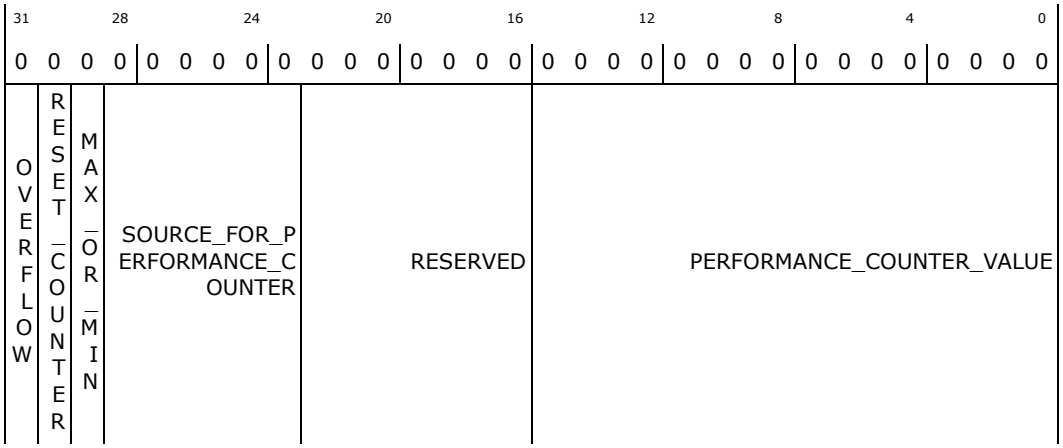
Performance Counter Status2 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 7300Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**OVERFLOW:** This bit indicates weather the 16 bit counter overflowed or not. 0 = Counter is valid 1 = Counter is invalid since it overflowed
30	0x0 RO	**RESET_COUNTER:** This bit indicates when the counter will be reset. 1 = Reset after each frame, sum of all event in the frame 0 = Reset after each event within the frame
29	0x0 RO	**MAX_OR_MIN:** This bit tells whether the stored counter value for an event is the maximum or the minimum value of the previous event. 0 = Stored value is the maximum latency 1 = Stored value is the minimum latency

Bit Range	Default & Access	Field Name (ID): Description
28:23	0x0 RO	**SOURCE_FOR_PERFORMANCE_COUNTER:** These bits indicate the source for the performance counter. 000000 = Overlay Register Request Latency [DevBW] and [DevCL] 000001 = Font Request Latency 000010 = Character Request Latency 000011 = Display A FIFO Status 000100 = Display B FIFO Status 000101 = Sprite A FIFO Status 000110 = Cursor A FIFO Status 000111 = Cursor B FIFO Status 001000 = Display Steamer A TLB Latency 001001 = Display Streamer B TLB Latency 001010 = Sprite Streamer A TLB Latency 001011 = Cursor Streamer A TLB Latency 001100 = Cursor Streamer B TLB Latency 001101 = Overlay Streamer TLB Latency [DevBW] and [DevCL] 001110 = Display Steamer A Request Latency 001111 = Display Streamer B Request Latency 010000 = Sprite Streamer A Request Latency 010001 = Cursor Streamer A Request Latency 010010 = Cursor Streamer B Request Latency 010011 = Overlay Streamer Request Latency [DevBW] and [DevCL] 010100 = Display A Command Request Latency 010101 = Display B Command Request Latency 010110 = Sprite A Command Request Latency 010111 = Cursor A Command Request Latency 011000 = Cursor B Command Request Latency 011001 = Overlay Command Request Latency [DevBW] and [DevCL] 011010 = DPFC Dummy Read [DevCTG] 011011 = DPFC Self Refresh [DevCTG] 011100 = Sprite B FIFO status 011101 = Sprite C FIFO status 011110 = Sprite D FIFO status 011111 = Sprite B TLB Request Latency 100000 = Sprite C TLB Request Latency 100001 = Sprite D TLB Request Latency 100010 = Sprite B Request Latency 100011 = Sprite C Request Latency 100100 = Sprite D Request Latency 100101 = Sprite B Command Request Latency 100110 = Sprite C Command Request Latency 101001 = InSR to HP Put (first put after inSR failing edge) 101000 = SR exit to data HP Put (measure the latency from the SRexit failing edge to the first data HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101001 = InSR to data HP Put (measure the latency from any data request made during inSR is active to the first data HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101010 = SR exit to TLB HP Put (measure the latency from the SRexit failing edge to the first TLB HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101011 = InSR to TLB HP Put (measure the latency from any TLB request made during inSR is active to the first TLB HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB)

Bit Range	Default & Access	Field Name (ID): Description
22:16	0x0 RO	**RESERVED:** Write as zero.
15:0	0x0 RO	**PERFORMANCE_COUNTER_VALUE:** This is the value of the performance counter for the source indicated in the source field.

4.3.410 PCSRC3—Offset 73010h

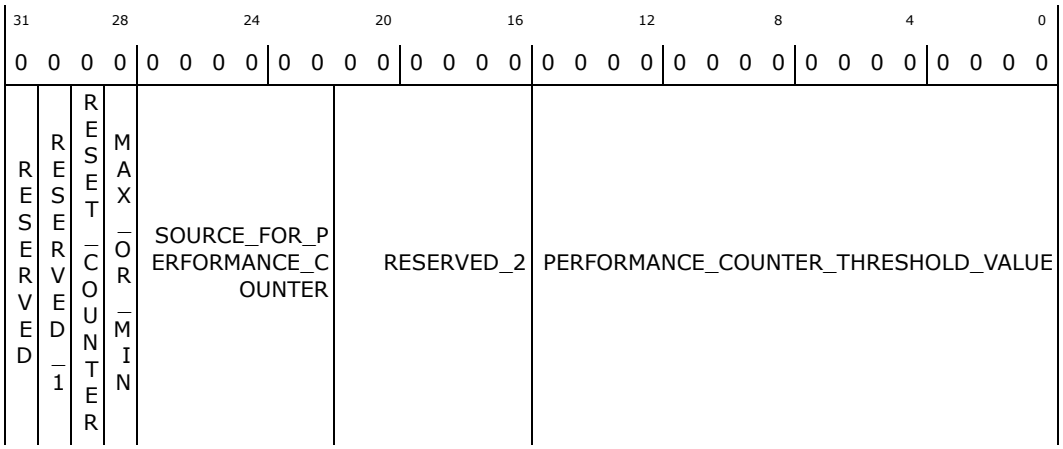
Performance Counter Source2 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 73010h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RESERVED:** Programming note: This third performance counter is enabled by the enable bit in the PCSRC1 bit 31.
30	0x0 RO	**RESERVED_1:** Reserved.
29	0x0 RW	**RESET_COUNTER:** This bit indicates when the counter will be reset. 1 = Reset after each frame, summing all events in the frame 0 = Reset after each event within the frame
28	0x0 RW	**MAX_OR_MIN:** This bit tells whether the stored counter value for an event is the maximum or the minimum value. The previous value is used to do the compare. 0 = Stored value is the maximum latency 1 = Stored value is the minimum latency

Bit Range	Default & Access	Field Name (ID): Description
27:22	0x0 RW	**SOURCE_FOR_PERFORMANCE_COUNTER:** These bits indicate the source for the performance counter. 000000 = Overlay Register Request Latency [DevBW] and [DevCL] 000001 = Font Request Latency 000010 = Character Request Latency 000011 = Display A FIFO Status 000100 = Display B FIFO Status 000101 = Sprite A FIFO Status 000110 = Cursor A FIFO Status 000111 = Cursor B FIFO Status 001000 = Display Streamer A TLB Latency 001001 = Display Streamer B TLB Latency 001010 = Sprite Streamer A TLB Latency 001011 = Cursor Streamer A TLB Latency 001100 = Cursor Streamer B TLB Latency 001101 = Overlay Streamer TLB Latency [DevBW] and [DevCL] 001110 = Display Streamer A Request Latency 001111 = Display Streamer B Request Latency 010000 = Sprite Streamer A Request Latency 010001 = Cursor Streamer A Request Latency 010010 = Cursor Streamer B Request Latency 010011 = Overlay Streamer Request Latency [DevBW] and [DevCL] 010100 = Display A Command Request Latency 010101 = Display B Command Request Latency 010110 = Sprite A Command Request Latency 010111 = Cursor A Command Request Latency 011000 = Cursor B Command Request Latency 011001 = Overlay Command Request Latency [DevBW] and [DevCL] 011010 = DPFC Dummy Read [DevCTG] 011011 = DPFC Self Refresh [DevCTG] 011100 = Sprite B FIFO status 011101 = Sprite C FIFO status 011110 = Sprite D FIFO status 011111 = Sprite B TLB Request Latency 100000 = Sprite C TLB Request Latency 100001 = Sprite D TLB Request Latency 100010 = Sprite B Request Latency 100011 = Sprite C Request Latency 100100 = Sprite D Request Latency 100101 = Sprite B Command Request Latency 100110 = Sprite C Command Request Latency 100111 = Sprite D Command Request Latency 101000 = SR exit to data HP Put (measure the latency from the SRexit failing edge to the first data HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101001 = InSR to data HP Put (measure the latency from any data request made during inSR is active to the first data HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101010 = SR exit to TLB HP Put (measure the latency from the SRexit failing edge to the first TLB HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101011 = InSR to TLB HP Put (measure the latency from any TLB request made during inSR is active to the first TLB HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB)

Bit Range	Default & Access	Field Name (ID): Description
21:16	0x0 RO	**RESERVED_2:** Write as zero.
15:0	0x0 RW	**PERFORMANCE_COUNTER_THRESHOLD_VALUE:** This value is used to compare against the performance counter. If the performance counter matches this value, an interrupt is generated if the interrupt bit is enabled. When the source selected is DDB FIFO status, the threshold value is used to program the value needed to monitor in the DDB FIFO. No interrupt is generated in this condition.

4.3.411 PCSTAT3—Offset 73014h

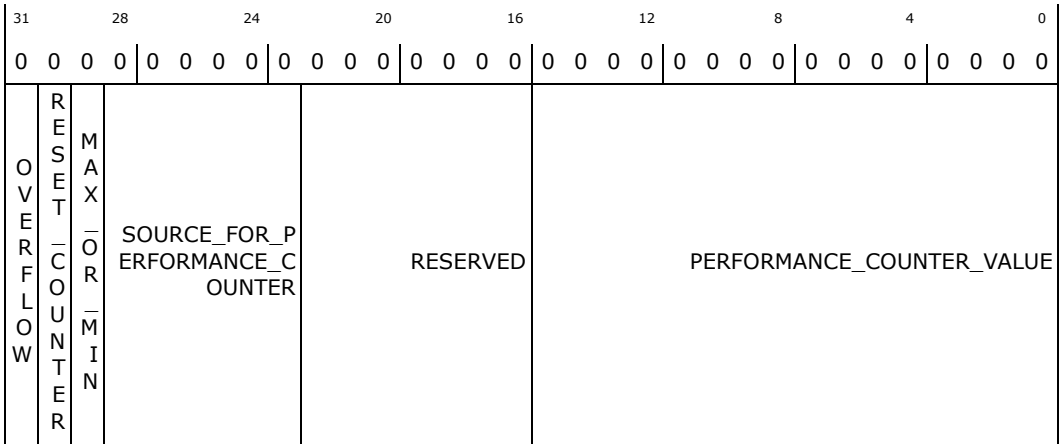
Performance Counter Status3 Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 73014h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**OVERFLOW:** This bit indicates weather the 16 bit counter overflowed or not. 0 = Counter is valid 1 = Counter is invalid since it overflowed
30	0x0 RO	**RESET_COUNTER:** This bit indicates when the counter will be reset. 1 = Reset after each frame, sum of all event in the frame 0 = Reset after each event within the frame
29	0x0 RO	**MAX_OR_MIN:** This bit tells whether the stored counter value for an event is the maximum or the minimum value of the previous event. 0 = Stored value is the maximum latency 1 = Stored value is the minimum latency

Bit Range	Default & Access	Field Name (ID): Description
28:23	0x0 RO	**SOURCE_FOR_PERFORMANCE_COUNTER:** These bits indicate the source for the performance counter. 000000 = Overlay Register Request Latency [DevBW] and [DevCL] 000001 = Font Request Latency 000010 = Character Request Latency 000011 = Display A FIFO Status 000100 = Display B FIFO Status 000101 = Sprite A FIFO Status 000110 = Cursor A FIFO Status 000111 = Cursor B FIFO Status 001000 = Display Steamer A TLB Latency 001001 = Display Streamer B TLB Latency 001010 = Sprite Streamer A TLB Latency 001011 = Cursor Streamer A TLB Latency 001100 = Cursor Streamer B TLB Latency 001101 = Overlay Streamer TLB Latency [DevBW] and [DevCL] 001110 = Display Steamer A Request Latency 001111 = Display Streamer B Request Latency 010000 = Sprite Streamer A Request Latency 010001 = Cursor Streamer A Request Latency 010010 = Cursor Streamer B Request Latency 010011 = Overlay Streamer Request Latency [DevBW] and [DevCL] 010100 = Display A Command Request Latency 010101 = Display B Command Request Latency 010110 = Sprite A Command Request Latency 010111 = Cursor A Command Request Latency 011000 = Cursor B Command Request Latency 011001 = Overlay Command Request Latency [DevBW] and [DevCL] 011010 = DPFC Dummy Read [DevCTG] 011011 = DPFC Self Refresh [DevCTG] 011100 = Sprite B FIFO status 011101 = Sprite C FIFO status 011110 = Sprite D FIFO status 011111 = Sprite B TLB Request Latency 100000 = Sprite C TLB Request Latency 100001 = Sprite D TLB Request Latency 100010 = Sprite B Request Latency 100011 = Sprite C Request Latency 100100 = Sprite D Request Latency 100101 = Sprite B Command Request Latency 100110 = Sprite C Command Request Latency 101001 = InSR to HP Put (first put after inSR failing edge) 101000 = SR exit to data HP Put (measure the latency from the SRexit failing edge to the first data HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101001 = InSR to data HP Put (measure the latency from any data request made during inSR is active to the first data HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101010 = SR exit to TLB HP Put (measure the latency from the SRexit failing edge to the first TLB HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB) 101011 = InSR to TLB HP Put (measure the latency from any TLB request made during inSR is active to the first TLB HP Put. This event shall be measured by either planeB, SpriteC, SpriteD, or CurB in pipeB)

Bit Range	Default & Access	Field Name (ID): Description
22:16	0x0 RO	**RESERVED:** Write as zero.
15:0	0x0 RO	**PERFORMANCE_COUNTER_VALUE:** This is the value of the performance counter for the source indicated in the source field.

4.3.412 PIPEC_DSL—Offset 74000h

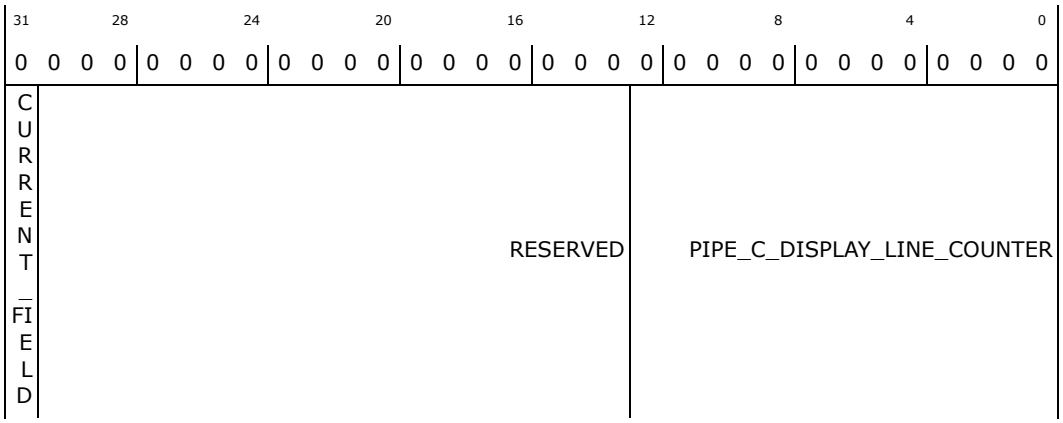
Display Scan Line

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 74000h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**CURRENT_FIELD:** Provides read back of the current field being displayed on display pipe B. Non-TV mode: 0 = first field (odd field) 1 = second field (even field) TV mode: 1 = first field (odd field) 0 = second field (even field) [DevBW and DevCL] Reserved: Read only.
30:13	0x0 RO	**RESERVED:** Read only.
12:0	0x0 RO	**PIPE_C_DISPLAY_LINE_COUNTER:** This register enables the read back of the display vertical line counter . The display line values are from the pipe B timing generator. They change at the leading edge of HSYNC, and can be safely read at any time.

4.3.413 PIPEC_SLC—Offset 74004h

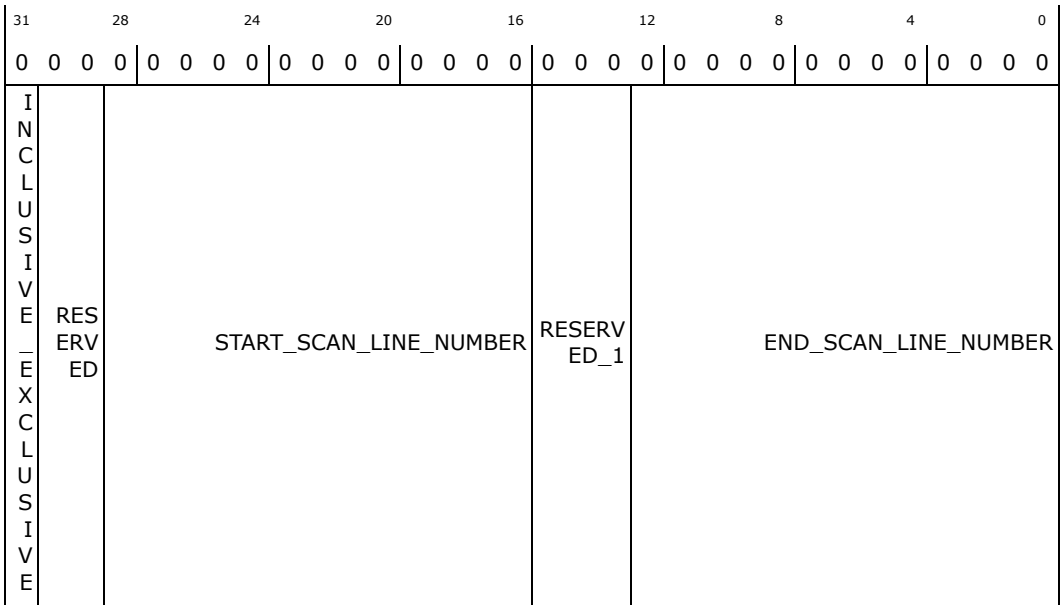
Pipe C Display Scan Line Range Compare Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 74004h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**INCLUSIVE_EXCLUSIVE:** 1 = Inclusive Within Range, 0 = Exclusive Out of Range
30:29	0x0 RO	**RESERVED:** Read only.
28:16	0x0 RW	**START_SCAN_LINE_NUMBER:** This field specifies the starting scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0,Display Buffer height in lines-1]. [DevBW] and [DevCL] End Scan Line Number: This field specifies the ending scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0, Display Buffer height in lines-1].
15:13	0x0 RO	**RESERVED_1:** Read only.

Bit Range	Default & Access	Field Name (ID): Description
12:0	0x0 RW	**END_SCAN_LINE_NUMBER:** This field specifies the ending scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0, Display Buffer height in lines-1]. [DevBW] and [DevCL] Start Scan Line Number: This field specifies the starting scan line number of the Scan Line Window. Format = U16 in scan lines, where scan line 0 is the first line of the display frame. Range = [0,Display Buffer height in lines-1].

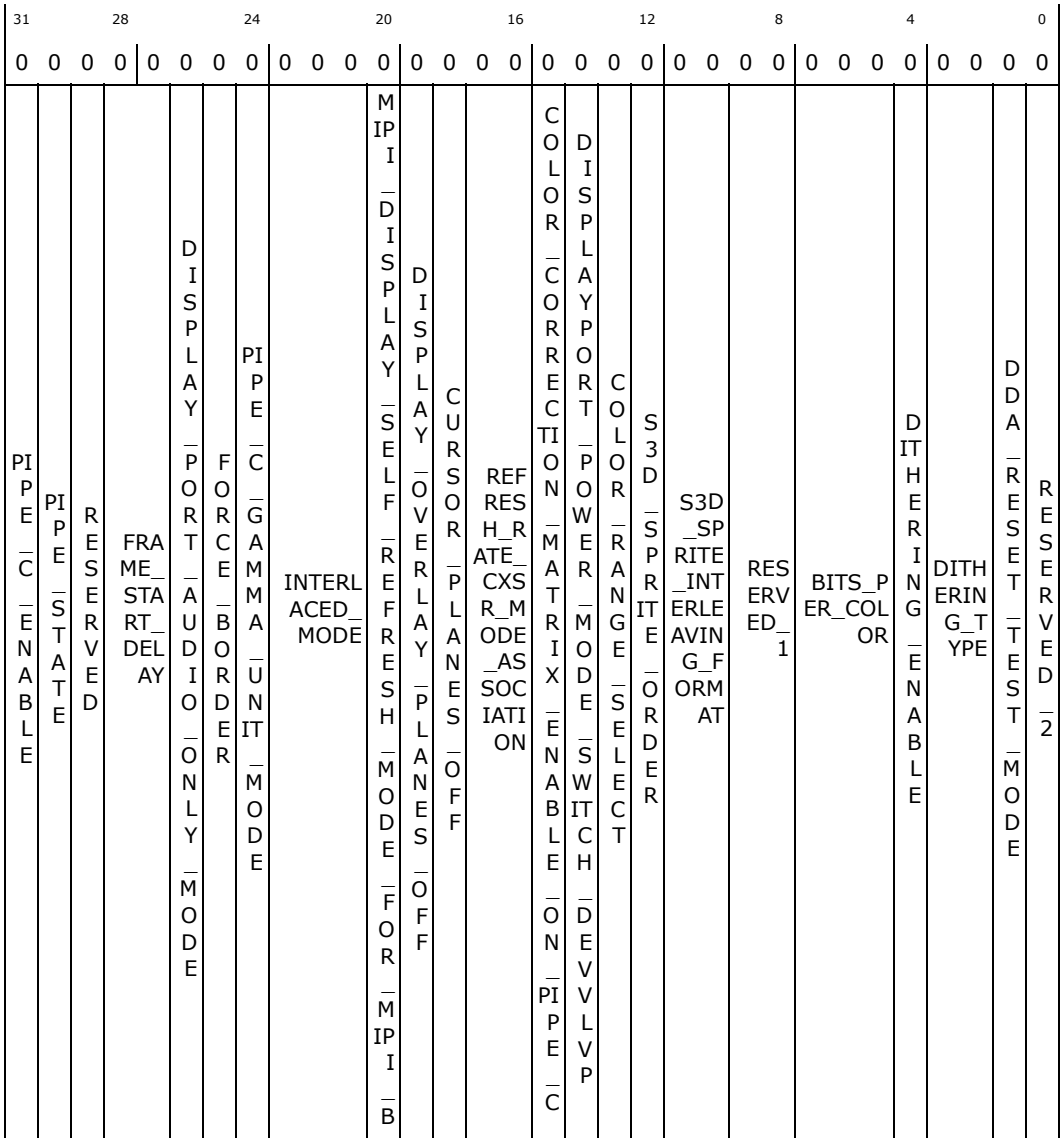
4.3.414 PIPECCONF—Offset 74008h

Pipe C Configuration Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 74008h

Default: 00000000h


31 28 24 20 16 12 8 4 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
PIPE_C_ENABLE
PIPE_STATE
RESERVED
FRAME_START_DELAY
DISPLAY_PORT_AUDIO_ONLY_MODE
FORCE_BORDER
PIPE_C_GAMMA_UNIT_MODE
INTERLACED_MODE
MIPI_DISPLAY_SELF_REFRESH_MODE_FOR_MIPI_B
DISPLAY_OVERLAY_PLANES_OFF
CURSOR_PLANES_OFF
REFRESH_RATE_CXSR_MODE_ASSOCIATION
COLOR_CORRECTION_MATRIX_ENABLE_ON_PIPE_C
DISPLAYPORT_POWER_MODE_SWITCH_DEVVLVP
COLOR_RANGE_SELECT
S3D_SPRITE_ORDER
S3D_SPRITE_INTERLEAVING_FORMAT
RESERVED_1
BITS_PER_COLOR
DITHERING_ENABLE
DITHERING_TYPE
DDA_RESET_TEST_MODE
RESERVED_2

Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**PIPE_C_ENABLE:** Setting this bit to the value of one, turns on pipe B. This must be done before any planes are enabled on this pipe. Changing it to a zero should only be done when all planes that are assigned to this pipe have been disabled. Turning the pipe enable bit off disables the timing generator in this pipe. Plane disable occurs after the next VBLANK event after the plane is disabled. Synchronization pulses to the display are not maintained if the timing generator is disabled. Power consumption will be at its lowest state when disabled. A separate bit controls the DPLL enable for this pipe. Pipe timing registers should contain valid values before this bit is enabled. Disabling the Pipe and changing the timing registers and re-enabling the pipe before the next VBLANK will cause the mode change to occur at the end of the current frame. This requires no wait on the software s part. On the other hand, if this is the disabling of the pipe, that does require a software wait for VBLANK to occur. Synchronization pulses to the display are not maintained if the timing generator is disabled. Power consumption is at it s lowest state. 1 = Enable 0 = Disable
30	0x0 RO	**PIPE_STATE:** This bit indicates the actual state of the pipe. Since there can be some delay between disabling the pipe and the pipe actually shutting off, this bit indicates the true current state of the pipe. 0 = Disabled 1 = Enabled AccessType: Read Only
29	0x0 RO	**RESERVED:** Write as zero.
28:27	0x0 RW	**FRAME_START_DELAY:** Used to delay the frame start signal that is sent to the display planes. Normal operation uses the default 00 value and test modes can use the delayed frame start to shorten the test time. This would be set to 00 for normal operation. 00 = Frame Start occurs on the first HBLANK after the start of VBLANK 01 = Frame Start occurs on the second HBLANK after the start of VBLANK 10 = Frame Start occurs on the third HBLANK after the start of VBLANK 11 = Frame Start occurs on the forth HBLANK after the start of VBLANK
26	0x0 RW	**DISPLAY_PORT_AUDIO_ONLY_MODE:** Setting this bit to 1 indicates the DisplayPort will output audio only. 0 = DisplayPort will output Video or Video and Audio 1 = DisplayPort will output Audio only
25	0x0 RW	**FORCE_BORDER:** (TEST MODE)0 = Normal Operation 1 = Color information is ignored and border color is substituted during active region
24	0x0 RW	**PIPE_C_GAMMA_UNIT_MODE:** . This bit selects which mode the pipe gamma correction logic works in. In the palette mode, it behaves as a 3X256x8 RAM lookup. Indexed mode operation should use the palette in 8-bit mode. In the 10-bit gamma mode, it will act as a piecewise linear interpolation. Other gamma units such as in the overlay and sprite are unaffected by this bit.0 = 8-bit Palette Mode 1 = 10-bit Gamma Mode

Bit Range	Default & Access	Field Name (ID): Description
23:21	0x0 RW	**INTERLACED_MODE:** These bits are used for software control of interlaced behavior. They are updated immediately if the pipe is off, or in the vertical blank after programming if pipe is enabled. 0xx = Progressive 100 = Interlaced embedded panel using programmable vertical sync shift (2x) 101 = Interlaced using vertical sync shift. Backup option to setting 110. (2x) 110 = Interlaced with VSYNC/HSYNC Field Indication using legacy vertical sync shift. Used for SDVO. 111 = Interlaced with Field 0 Only using legacy vertical sync shift. Not used. Setting the Interlaced embedded panel mode causes hardware to automatically modify the output to match the specifications of panels that support interlaced mode.
20	0x0 RW	**MIPI_DISPLAY_SELF_REFRESH_MODE_FOR_MIPI_B:** .0 = Normal Operation, display controller generate timing and refresh display panel at refresh rate 1 = Display self-refresh mode. Display controller update frame buffer in display module on demand only
19	0x0 RW	**DISPLAY_OVERLAY_PLANES_OFF:** . This bit when set will cause all enabled Display and overlay planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit, at the next VBLANK. Timing signals continue as they were but the screen becomes blank. Setting the bit back to a zero will then allow the display and overlay planes to resume on the following VBLANK.0 = Normal Operation 1 = Planes assigned to this pipe are disabled.
18	0x0 RW	**CURSOR_PLANES_OFF:** . This bit when set will cause all enabled cursor planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit, at the next VBLANK. Timing signals continue as they were but the screen becomes blank. Setting the bit back to a zero will then allow the cursor planes to resume on the following VBLANK. 0 = Normal Operation 1 = Planes assigned to this pipe are disabled.
17:16	0x0 RW	**REFRESH_RATE_CXSR_MODE_ASSOCIATION:** These bits select how refresh rates are tied to CxSR on pipe B. When they are set to anything other than 00, bits 23:21 of this register must be programmed to 0xx. Switching between 01 and 10 settings directly is not allowed. Software must program this field to 00 before switching. Software is responsible for enabling this mode only for integrated display panels that support corresponding mode. 00 Default no dynamic refresh rate change enabled. Software control only. 01 Progressive-to-progressive refresh rate change enabled and tied to CxSR. Pixel clock values set in FPB0/FPB1 settings in the DPLLB control register and FPB0/FPB1 divider registers. 10 Progressive-to-interlaced refresh rate change enabled and tied to CxSR. Pixel clock value does not change in this case. Scaling must be disabled in this mode. Uses programmable VS shift 11 Reserved
15	0x0 RW	**COLOR_CORRECTION_MATRIX_ENABLE_ON_PIPE_C:** 1 = Color Correction Coefficients are enabled to perform color correction 0 = Color Correction Coefficients are disabled

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**DISPLAYPORT_POWER_MODE_SWITCH_DEVVLVP:** This bit selects the software controlled progressive to progressive power saving mode (software controlled DRRS). Hardware Controlled Refresh Rate Select must be disabled when enabling this. Link and data M/N 1 values are used for normal settings, M/N 2 values are used for low power settings. 0 Normal progressive refresh rate (default) 1 Low Power progressive refresh rate
13	0x0 RW	**COLOR_RANGE_SELECT:** : This bit is used to select the color range of RBG outputs. 0 = Apply full 0-255 color range to the output (Default) 1 = Apply 16-235 color range to the output
12	0x0 RW	**S3D_SPRITE_ORDER:** This bit controls the blending order of the sprite planes for S3D support: 0 = Sprite C first. The first line or pixel comes from Sprite C (default) 1 = Sprite D first. The first line or pixel comes from Sprite D
11:10	0x0 RW	**S3D_SPRITE_INTERLEAVING_FORMAT:** These bits control the Sprite C/D interleaving format in S3D mode 00 = No interleaving 01 = Line interleaving 10 = Pixel interleaving 11 = Reserved
9:8	0x0 RO	**RESERVED_1:** MBZ Scrambling enable [DevCTG]: This bit enables scrambling for DisplayPort. Software must set this bit appropriately when enabling a DisplayPort output. 00 = Scrambling disabled (Default) 01 = Scrambling enabled, no SR after initialization at loop 2 of training 10 - RESERVED 11 = Scrambling and SR enabled. Scrambling is reset every 512 BS symbols.
7:5	0x0 RW	**BITS_PER_COLOR:** This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change can be done independent of a pixel clock change. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. For further details on Display Port fixed frequency programming to accommodate these formats refer to DP Frequency Programming in DPLL section of Bspec. 000 = 8 bits per color (Default) 001 = 10 bits per color 010 = 6 bits per color 011 = RESERVED 1xx = RESERVED
4	0x0 RW	**DITHERING_ENABLE:** This bit enables dithering for DisplayPort 6bpc or 8bpc modes 0 Dithering disabled (Default) 1 Dithering enabled Programming Note: Dithering should only be enabled for 8bpc or 6bpc.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0x0 RW	**DITHERING_TYPE:** This bit selects dithering type for DisplayPort 6bpc or 8bpc modes 00 - Spatial only (default) 01- Spatio-Temporal 1 10- Spatio-Temporal 2 (testmode) 11- Temporal only (testmode)
1	0x0 RW	**DDA_RESET_TEST_MODE::** 0 Do not reset DDA 1 Reset DDA every 8th display frame
0	0x0 RO	**RESERVED_2:** Write as zero

4.3.415 PIPECGCMAXRED—Offset 74010h

Pipe C Gamma Correction Max Red

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 74010h

Default: 00010000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																MAX_RED_GAMMA_CORRECTION_POINT															

Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RESERVED:** Reserved.
16:0	0x10000 RW	**MAX_RED_GAMMA_CORRECTION_POINT:** . 129th reference point for red channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0.Format: 11.6 Default: 0x10000

4.3.416 PIPECGCMAXGREEN—Offset 74014h

Pipe C Gamma Correction Max Green

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 74014h

Default: 00010000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED																MAX_GREEN_GAMMA_CORRECTION_POINT															

Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RESERVED:** Reserved.
16:0	0x10000 RW	**MAX_GREEN_GAMMA_CORRECTION_POINT:** . 129th reference point for green channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0.Format: 11.6 Default: 0x10000

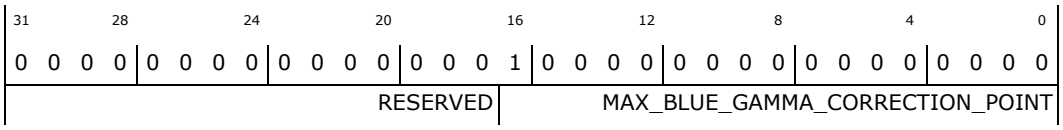
4.3.417 PIPECGCMAXBLUE—Offset 74018h

Pipe C Gamma Correction Max Blue

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 74018h

Default: 00010000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RESERVED:** Reserved.
16:0	0x10000 RW	**MAX_BLUE_GAMMA_CORRECTION_POINT:** . 129th reference point for blue channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0.Format: 11.6 Default: 0x10000

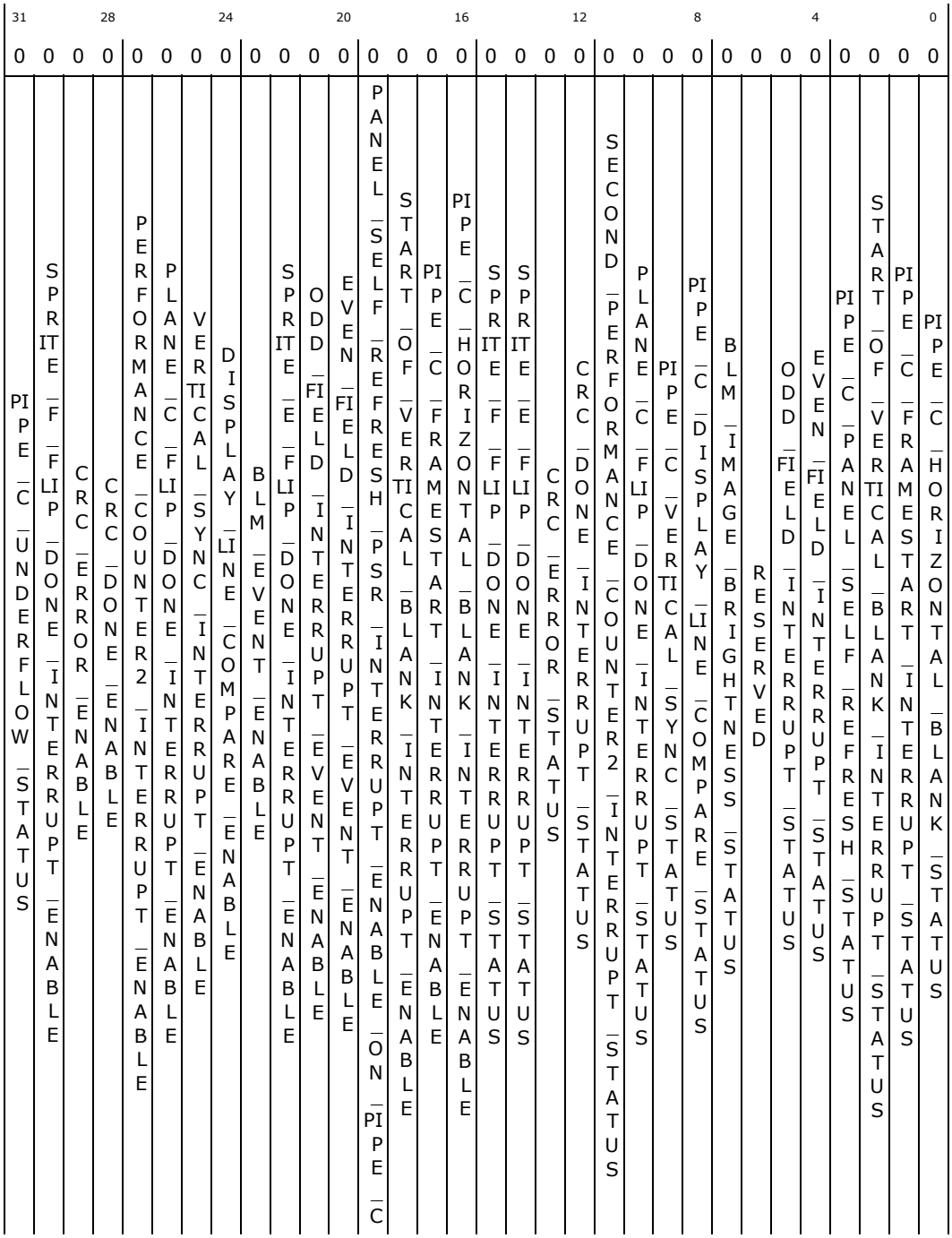
4.3.418 PIPECSTAT—Offset 74024h

Pipe C Status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 74024h

Default: 00000000h


31 28 24 20 16 12 8 4 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
PIPE_C_UNDERFLOW_STATUS
SPRITE_F_FLIP_DONE_INTERRUPT_ENABLE
CRC_ERROR_ENABLE
CRC_DONE_ENABLE
PERFORMANCE_COUNTER2_INTERRUPT_ENABLE
PLANE_C_FLIP_DONE_INTERRUPT_ENABLE
VERTICAL_SYNC_INTERRUPT_ENABLE
DISPLAY_LINE_COMPARE_ENABLE
BLM_EVENT_ENABLE
SPRITE_E_FLIP_DONE_INTERRUPT_ENABLE
ODD_FIELD_INTERRUPT_EVENT_ENABLE
EVEN_FIELD_INTERRUPT_EVENT_ENABLE
PANEL_SELF_REFRESH_PSR_INTERRUPT_ENABLE_ON_PIPE_C
START_OF_VERTICAL_BLANK_INTERRUPT_ENABLE
PIPE_C_FRAMESTART_INTERRUPT_ENABLE
PIPE_C_HORIZONTAL_BLANK_INTERRUPT_ENABLE
SPRITE_F_FLIP_DONE_INTERRUPT_STATUS
SPRITE_E_FLIP_DONE_INTERRUPT_STATUS
CRC_ERROR_STATUS
CRC_DONE_INTERRUPT_STATUS
SECOND_PERFORMANCE_COUNTER2_INTERRUPT_STATUS
PLANE_C_FLIP_DONE_INTERRUPT_STATUS
PIPE_C_VERTICAL_SYNC_STATUS
PIPE_C_DISPLAY_LINE_COMPARE_STATUS
BLM_IMAGE_BRIGHTNESS_STATUS
RESERVED
ODD_FIELD_INTERRUPT_STATUS
EVEN_FIELD_INTERRUPT_STATUS
PIPE_C_PANEL_SELF_REFRESH_STATUS
START_OF_VERTICAL_BLANK_INTERRUPT_STATUS
PIPE_C_FRAMESTART_INTERRUPT_STATUS
PIPE_C_HORIZONTAL_BLANK_STATUS

Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C	**PIPE_C_UNDERFLOW_STATUS:** This bit is set when an underflow occurs at the display pipe B. It is cleared by writing a one to this bit. This event will occur naturally during mode changes, to be effective, it should be cleared after a mode change. This bit is only valid after Pipe B has been completely configured. 1 = FIFO B Underflow occurred 0 = FIFO B Underflow did not occur AccessType: One to Clear
30	0x0 RW	**SPRITE_F_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Sprite F flip done interrupt status bit in the first line interrupt logic 0 = Sprite F Flip Done Interrupt Disabled 1 = Sprite F Flip Done Interrupt Enabled
29	0x0 RW	**CRC_ERROR_ENABLE:** This will enable the consideration of the CRC error status bit in the first line interrupt/status logic. 0 = CRC Error Detect Disabled 1 = CRC Error Detect Enabled
28	0x0 RW	**CRC_DONE_ENABLE:** This will enable the consideration of the CRC done status bit in the first line interrupt/status logic. 0 = CRC Done Detect Disabled 1 = CRC Done Detect Enabled
27	0x0 RW	**PERFORMANCE_COUNTER2_INTERRUPT_ENABLE:** This bit enables the second performance counter interrupt. 0 = Second Performance Counter2 Interrupt Status Disabled 1 = Second Performance Counter2 interrupt Status Enabled
26	0x0 RW	**PLANE_C_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Plane C flip done interrupt status bit in the first line interrupt logic 0 = Plane C flip done Interrupt/Status Disabled 1 = Plane C flip done Interrupt/Status Enabled
25	0x0 RW	**VERTICAL_SYNC_INTERRUPT_ENABLE:** 0 = Vertical Sync Interrupt/ Status Disabled 1 = Vertical Sync Interrupt/Status Enabled
24	0x0 RW	**DISPLAY_LINE_COMPARE_ENABLE:** 0 = Pipe C Display Line Compare Status Report Disabled 1 = Pipe C Display Line Compare Status report Enabled
23	0x0 RW	**BLM_EVENT_ENABLE:** This interrupt is generated by the image brightness segment comparators. Which segment cause an interrupt are controlled by the BLM Histogram control register. 0 = No BLM event enabled 1 = BLM event enabled
22	0x0 RW	**SPRITE_E_FLIP_DONE_INTERRUPT_ENABLE:** This will enable the consideration of the Sprite E flip done interrupt status bit in the first line interrupt logic 0 = Sprite E Flip Done Interrupt Disabled 1 = Sprite E Flip Done Interrupt Enabled
21	0x0 RW	**ODD_FIELD_INTERRUPT_EVENT_ENABLE:** . This bit should only be used when this pipe is in an interlaced display timing.0 = Odd Field Event disable 1 = Odd Field Event enable

Bit Range	Default & Access	Field Name (ID): Description
20	0x0 RW	**EVEN_FIELD_INTERRUPT_EVENT_ENABLE:** . This bit should only be used when this pipe is in an interlaced display timing.0 = Even field Event disable 1 = Even field Event enable
19	0x0 RW	**PANEL_SELF_REFRESH_PSR_INTERRUPT_ENABLE_ON_PIPE_C:** 0 = PSR interrupt Disabled on Pipe C 1 = PSR Interrupt Enabled on Pipe C
18	0x0 RW	**START_OF_VERTICAL_BLANK_INTERRUPT_ENABLE:** This will enable the consideration of the start of vertical blank interrupt status bit in the first line interrupt/status logic. 0 = Start of Vertical Blank Interrupt/Status Disabled 1 = Start of Vertical Blank Interrupt/Status Enabled
17	0x0 RW	**PIPE_C_FRAMESTART_INTERRUPT_ENABLE:** This will enable the consideration of the vertical blank interrupt status bit in the first line interrupt/status logic. 0 = Pipe C Framestart Interrupt/Status Disabled 1 = Pipe C Framestart Interrupt/Status Enabled
16	0x0 RW	**PIPE_C_HORIZONTAL_BLANK_INTERRUPT_ENABLE:** This will enable the consideration of the start of horizontal blank interrupt status bit in the first line interrupt/status logic0 = Start of Horizontal Blank Interrupt/Status Disabled 1 = Start of Horizontal Blank Interrupt/Status Enabled
15	0x0 RW/1C	**SPRITE_F_FLIP_DONE_INTERRUPT_STATUS:** MMIO Flip Event is completed on Sprite F 0 = Sprite F Flip Not Done 1 = Sprite F Flip Done AccessType: One to Clear
14	0x0 RW/1C	**SPRITE_E_FLIP_DONE_INTERRUPT_STATUS:** MMIO Flip Event is completed on Sprite E 0 = Sprite E Flip Not Done 1 = Sprite E Flip Done AccessType: One to Clear
13	0x0 RW/1C	**CRC_ERROR_STATUS:** This bit is set when a Pipe C CRC error is detected. It is cleared by a write of a one. 0 = No CRC Error 1 = CRC Error detected AccessType: One to Clear
12	0x0 RW/1C	**CRC_DONE_INTERRUPT_STATUS:** This bit is set when Pipe C CRC calculation and compare are complete. It is cleared by a write of a one. 0 = CRC Not Done 1 = CRC Done AccessType: One to Clear
11	0x0 RW/1C	**SECOND_PERFORMANCE_COUNTER2_INTERRUPT_STATUS:** This bit is set when the second performance counter2 generates an interrupt. It is cleared by a write of a one. 0 = Second performance counter interrupt event not asserted 1 = Second performance counter interrupt event asserted AccessType: One to Clear

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RW/1C	**PLANE_C_FLIP_DONE_INTERRUPT_STATUS:** Async/Sync Flip Event is completed on Display Plane C 0 = Plane C Flip Not Done 1 = Plane C Flip Done AccessType: One to Clear
9	0x0 RW/1C	**PIPE_C_VERTICAL_SYNC_STATUS:** 0 = Vertical Sync not asserted 1 = Vertical Sync asserted AccessType: One to Clear
8	0x0 RW/1C	**PIPE_C_DISPLAY_LINE_COMPARE_STATUS:** This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the value of the bit. 0 = Display Line Compare Status not asserted 1 = Display Line Compare Status asserted AccessType: One to Clear
7	0x0 RW/1C	**BLM_IMAGE_BRIGHTNESS_STATUS:** This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the value of the bit. 0 =DPST Interrupt has not occurred on pipe C 1 = DPST Interrupt has occurred on pipe C AccessType: One to Clear
6	0x0 RO	**RESERVED:** MBZ
5	0x0 RW/1C	**ODD_FIELD_INTERRUPT_STATUS:** . This status bit will be set on a Odd field VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates, the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set.Note: This bit will not be set when pipe is in Interlaced with Field 0 Only using legacy vertical sync shift mode. 0 = Odd Field Vertical Blank has not occurred 1 = Odd Field Vertical Blank has occurred AccessType: One to Clear
4	0x0 RW/1C	**EVEN_FIELD_INTERRUPT_STATUS:** . This status bit will be set on a even filed VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates, the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set.Note: This bit will not be set when pipe is in Interlaced with Field 0 Only using legacy vertical sync shift mode. 0 = Even Field Vertical Blank has not occurred 1 = Even Field Vertical Blank has occurred AccessType: One to Clear
3	0x0 RW/1C	**PIPE_C_PANEL_SELF_REFRESH_STATUS:** This bit indicates interrupt is generated by the PSR controller and intends to send interrupt to SW driver when the PSR interrupt enable bit (70028h bit 22) is set. This is cleared when a write to this register occurs with this bit as a one. Write with this bit as a zero has no effect on the value of the bit. 0 = PSR Interrupt has not occurred on pipe C 1 = PSR interrupt has occurred on pipe C AccessType: One to Clear

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW/1C	**START_OF_VERTICAL_BLANK_INTERRUPT_STATUS:** This status bit will be set at the beginning of a VBLANK event. At this point, the double buffered display registers flip, taking their new values. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. In MIPI DSR mode, GPIO TE trigger sets the Vblank Interrupt status 0 = Start of Vertical Blank has not occurred 1 = Start of Vertical Blank has occurred AccessType: One to Clear
1	0x0 RW/1C	**PIPE_C_FRAMESTART_INTERRUPT_STATUS:** This status bit will be set on a VBLANK event, when the frame start occurs. The display registers are updated at the start of vertical blank, but the new register data is not utilized by the display pipeline until the point in the vertical blank period when the frame start occurs, which is the event that triggers this bit. To use this bit in a polling manner, clear the bit by writing a one to it followed by the polling loop waiting for it to become set. 0 = Pipe C Framestart Status has not occurred 1 = Pipe C Framestart Status has occurred AccessType: One to Clear
0	0x0 RW/1C	**PIPE_C_HORIZONTAL_BLANK_STATUS:** 0 = Pipe C Horizontal Blank has not occurred 1 = Pipe C Horizontal Blank has occurred AccessType: One to Clear

4.3.419 PIPECFRAMECOUNT—Offset 74040h

Pipe C Frame Count High

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 74040h

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
PIPE_C_FRAME_COUNT								

Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**PIPE_C_FRAME_COUNT:** Refer PipeAFrameHigh description.

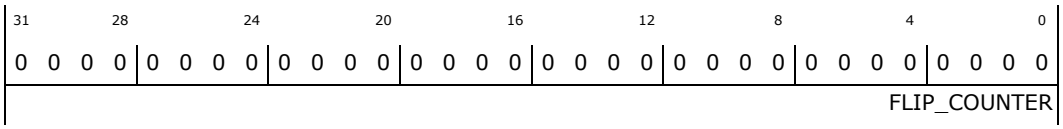
4.3.420 PIPECFLIPCOUNT—Offset 74044h

Pipe C Flip count

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 74044h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**FLIP_COUNTER:** . Refer PipeAFlipCount description.

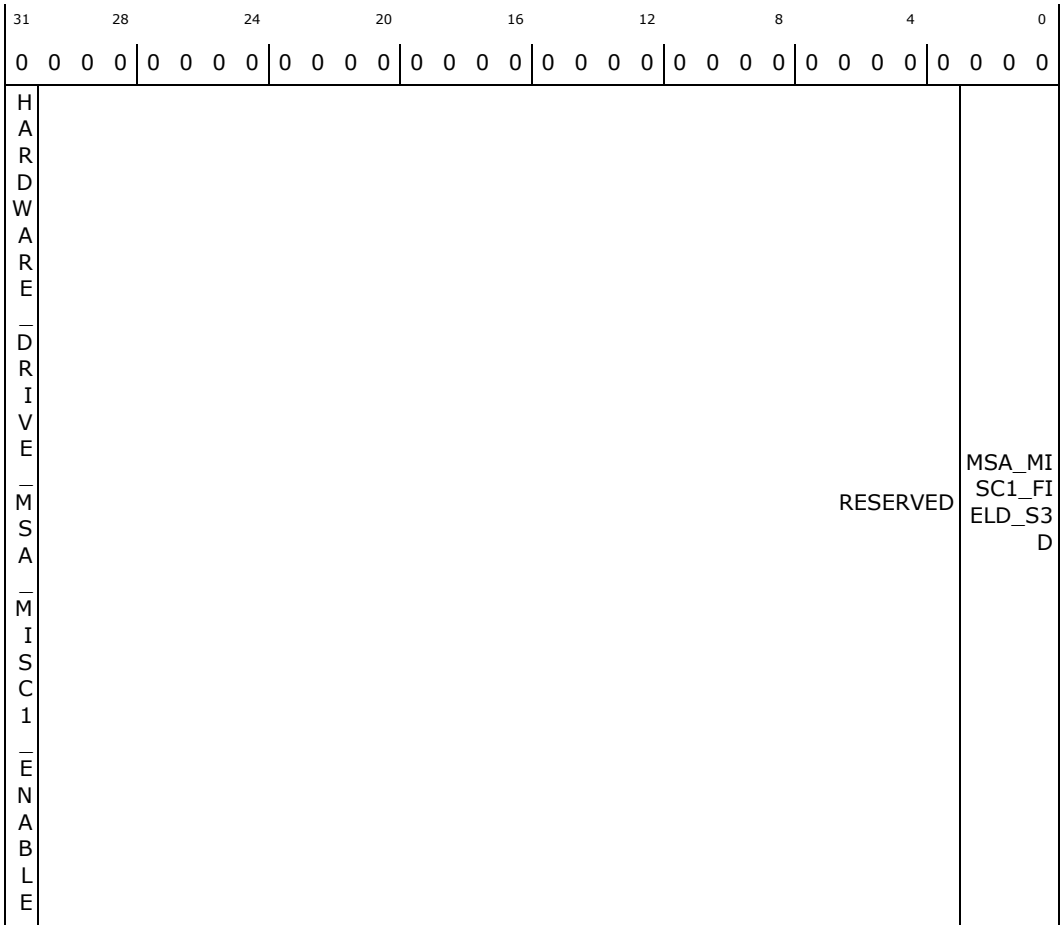
4.3.421 PIPECMSAMISC—Offset 74048h

Pipe C MSA MISC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 74048h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**HARDWARE_DRIVE_MSA_MISC1_ENABLE:** This bit enables hardware to drive MSA MISC1 bit3:1 with the stereo 3D left/right eye field indication. Hardware will drive 000 when S3D mode is disabled, 001 when enabled and the upcoming video frame is right eye, 011 when enabled and the upcoming video frame is left eye. When this bit is disabled, software may manually program the MSA MISC1 Field S3D field in bit 2:0 in this register to set MISC1 bit 3:1 0 = Disable hardware driving MSA MISC1 bit 3:1. Allow software to manually program MSA MISC1 bit3:1 through MSA_MISC1_FIELD_S3D (default) 1 = Enable hardware to drive MSA MISC1 bit3:1 for S3D
30:3	0x0 RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2:0	0x0 RW	**MSA_MISC1_FIELD_S3D:** This field provides software to manually program MSC1 stereo video attribute for DisplayPort: 000 = No stereo video transported 001 = For progressive video, the next (upcoming) video frame is RIGHT eye 010 = Reserved 011 = For progressive video, the next (upcoming) video frame is LEFT eye 100 = Stacked top and bottom top half represents left-eye view and bottom half represents right-eye view 101 = Stacked top and bottom top half represents right-eye view and bottom half represents left-eye view

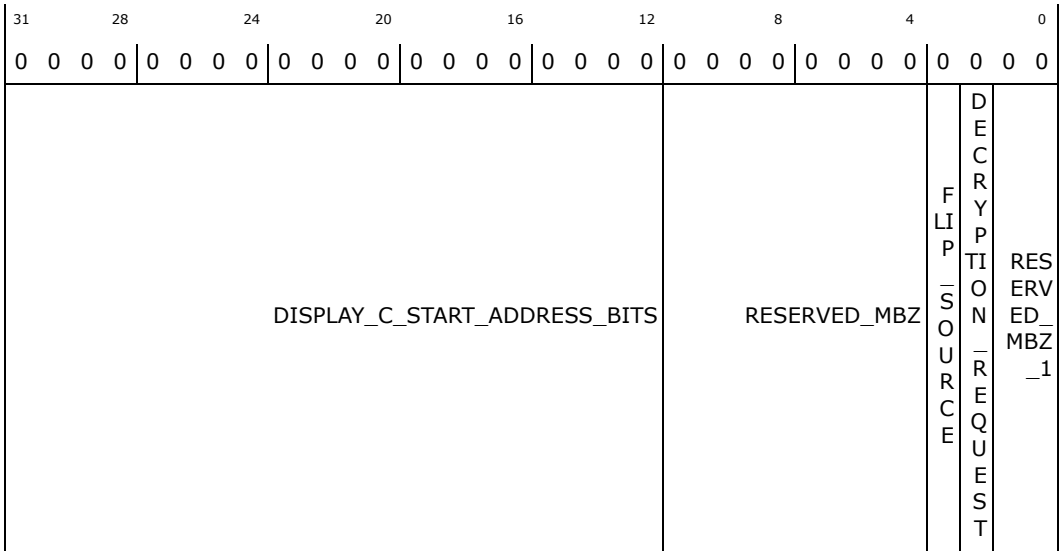
4.3.422 DSPCADDR—Offset 7417Ch

Display C Async flip Start Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7417Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**DISPLAY_C_START_ADDRESS_BITS:** This register provides the start address of the display C plane or the first eye when running in stereo mode. This address must be at least pixel aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted, the memory pages must not be marked NoDMA . Write to this register triggers async flip The async flip address is written into the Display C Base Address register 0x7119C
11:4	0x0 RO	**RESERVED_MBZ:** Reserved.
3	0x0 RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register.
1:0	0x0 RO	**RESERVED_MBZ_1:** Reserved.

4.3.423 DSPCCNTR—Offset 74180h

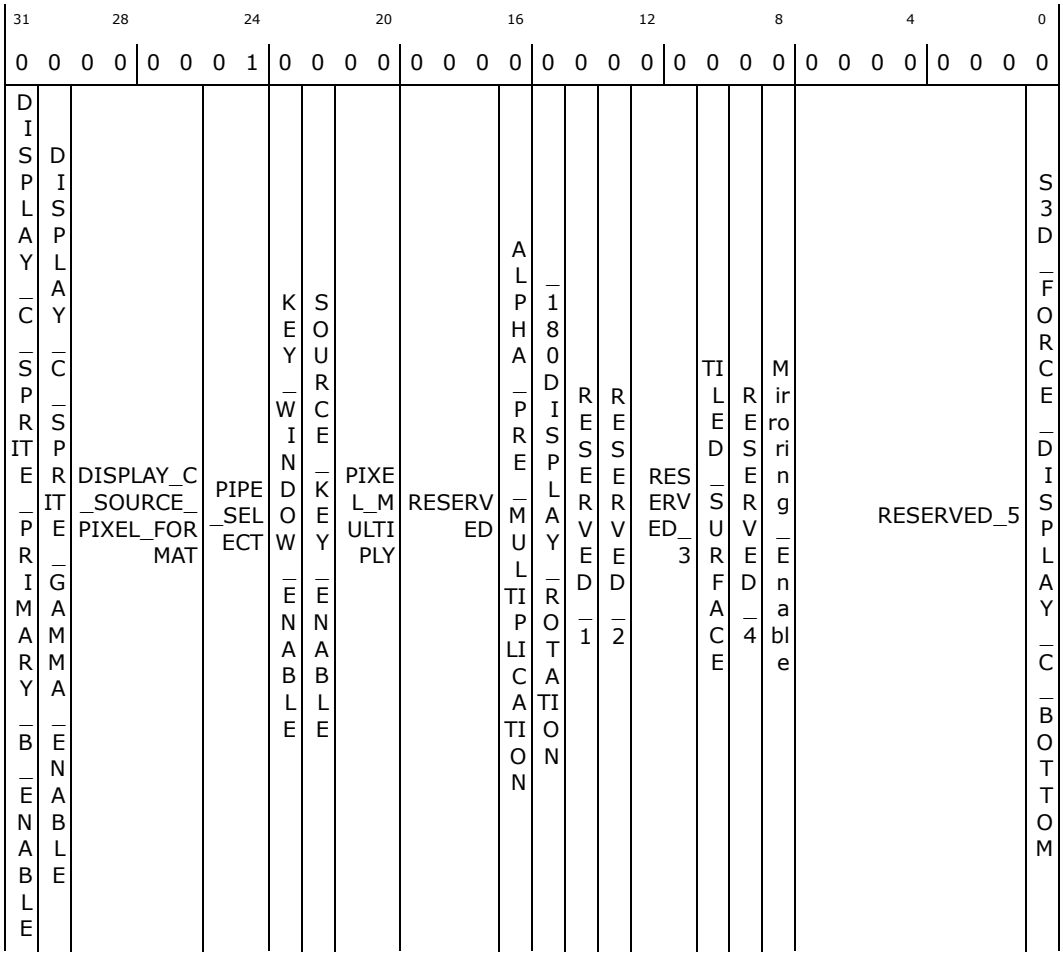
Display C/Sprite Plane Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 74180h

Default: 01000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**DISPLAY_C_SPRITE_PRIMARY_B_ENABLE:** This bit will enable or disable the display C/sprite. When this bit is set, the plane will generate pixels for display. When set to zero, memory fetches cease and display is blanked (from this plane) at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. 1 = Enable 0 = Disable
30	0x0 RW	**DISPLAY_C_SPRITE_GAMMA_ENABLE:** This bit should only be changed after the plane has been disabled. It controls the bypassing of the display pipe gamma unit for this display plane pixel data only. For 8-bit indexed display data, this bit should be set to a one. 0 = Display C pixel data bypasses the pipe gamma correction logic (default). 1 = Display C pixel data is gamma corrected in the pipe gamma correction logic

Bit Range	Default & Access	Field Name (ID): Description
29:26	0x0 RW	**DISPLAY_C_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite/display C. Pixel formats with an alpha channel (8:8:8:8) should not use source keying. Before entering the blender, each source format is converted to 10 bits per pixel (details are described in the intermediate precision for the blender section of the Display Functions chapter). 000x = Reserved. 0010 = 8-bpp Indexed. 0011 = Reserved. 0100 = Reserved. 0101 = 16-bit BGRX (5:6:5:0) pixel format (XGA compatible). 0110 = 32-bit BGRX (8:8:8:8) pixel format. Ignore alpha. 0111 = 32-bit BGRA (8:8:8:8) pixel format. (with pre-multiplied alpha color format) 1000 = 32-bit RGBX (10:10:10:2) pixel format. Ignore alpha. 1001 = 32-bit RGBA (10:10:10:2) pixel format. (with pre-multiplied alpha color format) 1010 = 32-bit BGRX (10:10:10:2) pixel format Ignore alpha 1011 = 32-bit BGRA (10:10:10:2) pixel format (with pre-multiplied alpha color format) 1100 = 64-bit RGBX (16:16:16:16) 16 bit floating point pixel format. Ignore alpha. 1101 = 64-bit RGBA (16:16:16:16) 16-bit floating point pixel format (with pre-multiplied color format) 1110 = 32-bit RGBX (8:8:8:8) pixel format. Ignore alpha. 1111 = 32-bit RGBA (8:8:8:8) pixel format (with pre-multiplied color format)
25:24	0x1 RO	**PIPE_SELECT:** Plane C always ties to Pipe C. Reserved AccessType: Read Only
23	0x0 RW	**KEY_WINDOW_ENABLE:** This applies only to devices with a Display Plane C. It determines what area of the screen the source key compare should be applied. This bit is set to one when the color key is used as a destination key for display C. Display plane C must be enabled on the same pipe and display A should not be enabled on this pipe for this to be used. The function is only effective when display C is enabled and defined by Z-order to be behind display C. 0 = If keying is enabled, it applies to the entire display C plane 1 = If keying is enabled, it applies only to the intersection between display B and display C [DevBLC] and [DevCTG]: Reserved
22	0x0 RW	**SOURCE_KEY_ENABLE:** When used as a sprite or a secondary this enables source color keying. Sprite pixel values that match the key will become transparent. Source keying allows a plane that is behind (below) this plane to show through where the display B data matches the display B key. This function is overloaded to provide display C destination keying when combined with the key window enable bit.. Setting this bit is not allowed when the display pixel format includes an alpha channel. 0 = Sprite source key is disabled (default) 1 = Sprite source key is enabled. [DevBLC] and [DevCTG]: Reserved In destination keying, primary plane pixel will be made transparent when blending with sprite pixel as the destination if the primary src key matches with the primary pixel value.

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line/pixel doubling mode, the horizontal pixels are doubled and lines are sent twice. Asynchronous flips are not used in this mode. Programming Notes: Asynchronous flips are not permitted when pixel multiply is enabled. 00 = No duplication 01 = Line/pixel Doubling 10 = Reserved 11 = Pixel Doubling only
19:17	0x0 RO	**RESERVED:** Write as zero
16	0x0 RO	**ALPHA_PRE_MULTIPLICATION:** This Bit allows plane logic to alpha multiply ARGB/RGBA pizels if they are not pre multiplied already. 0: RGB Components are pre multiplied with alpha channel of the pixel. 1: RGB components have not been multiplied with alpha channel of the pixel. Plane will performed multiplication before alpha blending.
15	0x0 RW	**_180DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit, software must also set the base address to the lower right corner of the unrotated image. [DevCL] Do not enable 180 rotation together with Frame Buffer Compression 0 = No rotation 1 = 180 rotation
14	0x0 RO	**RESERVED_1:** [DevBLC, DevCTG] Display C Trickle Feed Enable: 0 = Trickle Feed Enabled - Display B data requests are sent whenever there is space in the Display Data Buffer. 1 = Trickle Feed Disabled - Display C data requests are sent in bursts. Note: On mobile products this bit will be ignored such that Trickle Feed is always disabled. [DevELK] Must always be programmed disabled
13	0x0 RO	**RESERVED_2:** [DevBLC, DevCTG] Display C Data Buffer Partitioning Control: 0 = Display C Data Buffer will encompass Sprite C buffer space when Sprite B is disabled. 1 = Display C Data Buffer will not use Sprite B buffer space when Sprite B is disabled. Note: When in C3xR Max FIFO mode, this bit will be ignored.
12:11	0x0 RO	**RESERVED_3:** Reserved.
10	0x0 RW	**TILED_SURFACE:** This bit indicates that the display C surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set, it affects the hardware interpretation of the DSPCLINOFF, DSPCTILEOFF, and DSPCSURF registers. 0 = Display C surface uses linear memory 1 = Display C surface uses X-tiled memory

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RO	**RESERVED_4:** Write as zero [DevBLC, DevCTG] Asynchronous Surface Address Update Enable: This bit will enable asynchronous updates of the surface address when written by MMIO. The surface address will change with the next TLB request or when start of vertical blank is reached. Updates during vertical blank may not complete until after the first few active lines are displayed. Restrictions: No command streamer initiated surface address updates are allowed when this bit is enabled. Only one asynchronous update may be made per frame. Must wait for vertical blank before again writing the surface address register. 0 = DSPCSURF MMIO writes will update synchronous to start of vertical blank (default) 1 = DSPCSURF MMIO writes will update asynchronously
8	0x0 RO	**Mirroring_Enable:** 0: Mirroring is not enabled. 1: Mirroring is enabled.
7:1	0x0 RO	**RESERVED_5:** Write as zero
0	0x0 RW	**S3D_FORCE_DISPLAY_B_BOTTOM (S3D_FORCE_DISPLAY_C_BOTTOM):** This bit will force the display C plane to be on the bottom of any sprite planes in the Z order. 0 = Display C Z-order is determined by the other control bits in pipe C 1 = Display C is forced to be on the bottom of any sprite planes in Z-order in pipe C

4.3.424 DSPCLINOFFSET—Offset 74184h

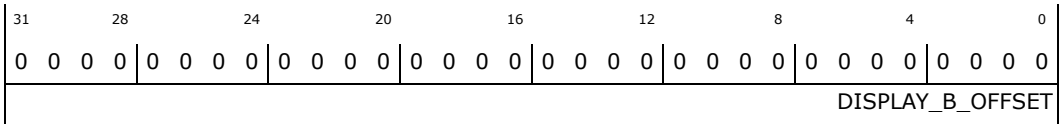
Display C/Sprite Linear Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 74184h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DISPLAY_C_OFFSET (DISPLAY_B_OFFSET):** This register provides the panning offset into the display B plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation, this offset must be the difference between the last pixel of the last line of the display data in its unrotated orientation and the display surface address.

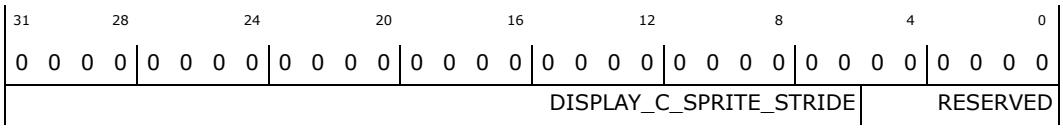
4.3.425 DSPCSTRIDE—Offset 74188h

Display C/Sprite Stride Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 74188h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**DISPLAY_C_SPRITE_STRIDE:** This is the stride for display C/Sprite in bytes. When using linear memory, this must be 64 byte aligned. When using tiled memory, this must be 512 byte aligned. The maximum value for this register is fixed. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register, the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory, the actual memory buffer stride is limited to a maximum of 16K bytes. The display stride must be power of 2 when doing Asynch Flips. The display stride must be 8KB or greater when doing Asynch Flips together with 180 rotation. The value in this register is updated through the command streamer during a synchronous flip.
5:0	0x0 RO	**RESERVED:** Reserved.

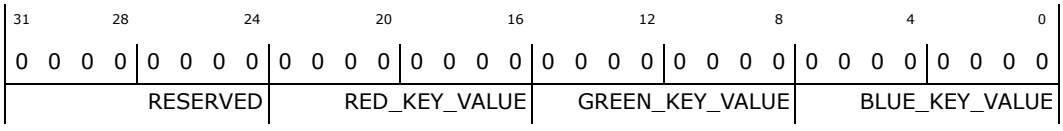
4.3.426 DSPCKEYVAL—Offset 74194h

Sprite Color Key Value Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 74194h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**

Bit Range	Default & Access	Field Name (ID): Description
23:16	0x0 RW	**RED_KEY_VALUE:** Specifies the color key value for the sprite red/Cr channel.
15:8	0x0 RW	**GREEN_KEY_VALUE:** Specifies the color key value for the sprite green/Y channel.
7:0	0x0 RW	**BLUE_KEY_VALUE:** Specifies the color key value for the sprite blue/Cb channel.

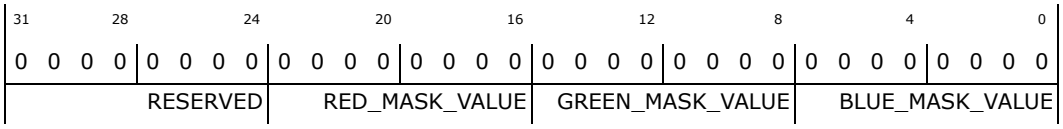
4.3.427 DSPCKEYMSK—Offset 74198h

Sprite Color Key Mask Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 74198h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED:**
23:16	0x0 RW	**RED_MASK_VALUE:** Specifies the color key mask for the sprite red/Cr channel.
15:8	0x0 RW	**GREEN_MASK_VALUE:** Specifies the color key mask for the sprite green/Y channel.
7:0	0x0 RW	**BLUE_MASK_VALUE:** Specifies the color key mask for the sprite blue/Cb channel.

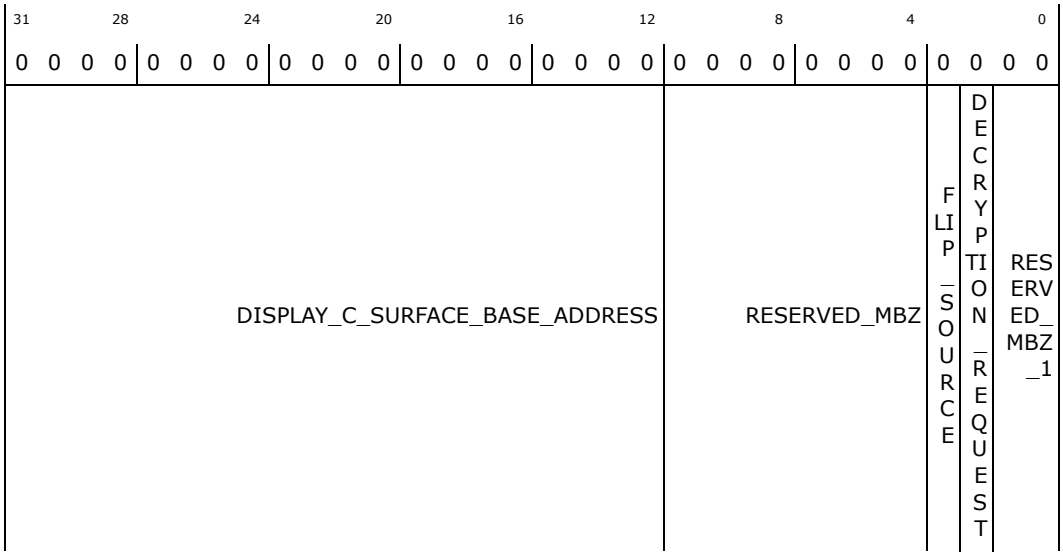
4.3.428 DSPCSURF—Offset 7419Ch

Display C Surface Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 7419Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**DISPLAY_C_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled, panning is specified using (x, y) offsets in the DSPCTILEOFF register. When the surface is in linear memory, panning is specified using a linear offset in the DSPCLINOFF register. This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory, this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. [DevBW] and [DevCL]: This address must be 128K aligned for linear memory.
11:4	0x0 RO	**RESERVED_MBZ:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**FLIP_SOURCE:** Project: All Default Value: 0b This bit indicates if the source of the flip is CS or BCS so display can send the flip done response to the appropriate destination. ValueNameDescriptionProject 0b CS Flip source is CS All 1b BCS Flip source is BCS All
2	0x0 RW	**DECRYPTION_REQUEST:** Project: All Default Value: 0b This bit requests decryption to be enabled for this plane. This request will be qualified with the separate decryption allow message in order to create the decryption enable. This bit is only allowed to change on a synchronous flip, but once set with a synchronous flip, the bit can remain set while using asynchronous flips. This value is loaded into the surface base address register of the associated plane. Usage must conform to the rules outlined in the plane surface base address register.
1:0	0x0 RO	**RESERVED_MBZ_1:** Reserved.

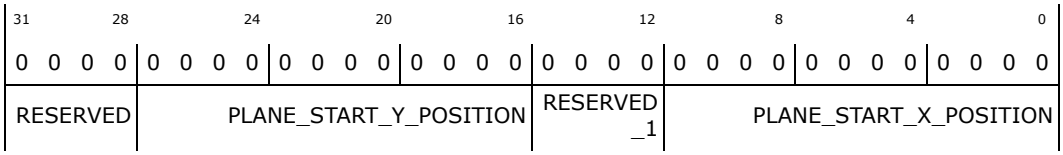
4.3.429 DSPCTILEOFF—Offset 741A4h

Display C Tiled Offset Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** 741A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED:** Write as zero
27:16	0x0 RW	**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the unrotated orientation.
15:12	0x0 RO	**RESERVED_1:** Write as zero
11:0	0x0 RW	**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation, this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the unrotated orientation. When display stride is 16KB and doing Asynch Flips, do not program the offset to give pans of 7680 to 8191 bytes.

4.3.430 DSPCSURFLIVE—Offset 741ACh

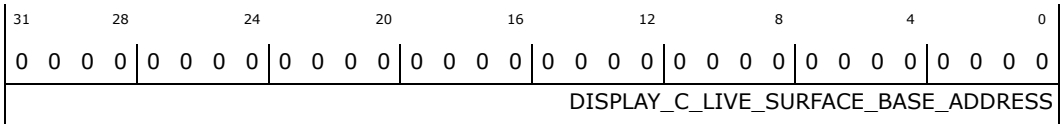
Display C Live Surface Base Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 741ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**DISPLAY_C_LIVE_SURFACE_BASE_ADDRESS:** . This gives the live value of the surface base address as being currently used for the plane.

4.3.431 DSPCFLPQSTAT—Offset 74200h

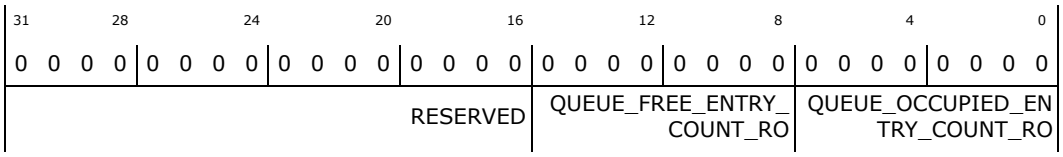
Flip Queue Status Register

Access Method

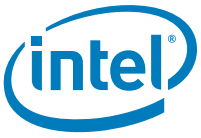
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: 74200h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RESERVED:** Write as zero (RO)
15:8	0x0 RO	**QUEUE_FREE_ENTRY_COUNT_RO:** This value indicates the number of free entries in the queue at the time that the register was read. The total number of entries in the queue is the sum of the occupied entry count and the free entry count.
7:0	0x0 RO	**QUEUE_OCCUPIED_ENTRY_COUNT_RO:** This value indicates the number of occupied entries in the queue at the time that the register was read. The total number of entries in the queue is the sum of the occupied entry count and the free entry count.



4.4 READ Address Map (Read Only)

Table 24. Summary of Display Memory Mapped I/O Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3BA–3BAh	1	"ST01 (ST01_MDA)—Offset 3BAh" on page 961	00h
3C2–3C2h	1	"ST00—Offset 3C2h" on page 962	00h
3C7–3C7h	1	"DACSTATE—Offset 3C7h" on page 963	00h
3DA–3DAh	1	"ST01 (ST01_CGA)—Offset 3DAh" on page 964	00h

4.4.1 ST01 (ST01_MDA)—Offset 3BAh

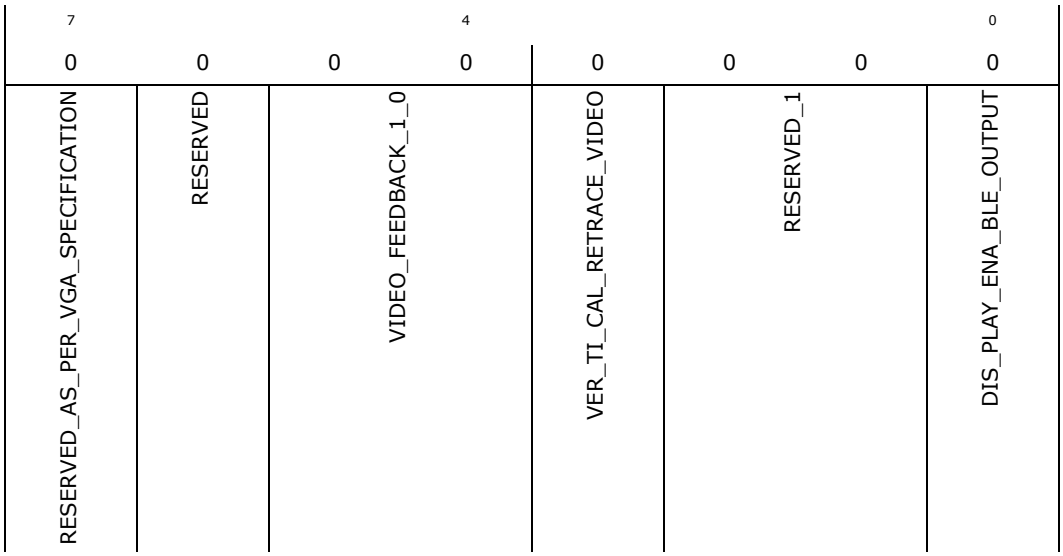
Input Status 1

Access Method

Type: ??? Register
(Size: 8 bits)

Offset: 3BAh

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
6	0x0 RO	**RESERVED:** Read as 0.
5:4	0x0 RO	**VIDEO_FEEDBACK_1_0:** These are diagnostic video bits that are selected by the Color Plane Enable Register. These bits that are programmable connected to 2 of the 8 color bits sent to the palette. Bits 4 and 5 of the Color Plane Enable Register (AR12) selects which two of the 8 possible color bits become connected to these 2 bits of this register. The current software normally does not use these 2 bits. They exist for EGA compatibility.
3	0x0 RO	**VER_TI_CAL_RETRACE_VIDEO:** 0 = VSYNC inactive (Indicates that a vertical retrace interval is not taking place). 1 = VSYNC active (Indicates that a vertical retrace interval is taking place).
2:1	0x0 RO	**RESERVED_1:** Read as 0s.

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RO	**DIS_PLAY_ENA_BLE_OUTPUT:** Display Enable is a status bit (bit 0) in Input Status Register 1 that indicates when either a horizontal retrace interval or a vertical retrace interval is taking place. This was used with the IBM* EGA graphics system (and the ones that preceded it, including MDA and CGA). In those cases, it was important to check the status of this bit to ensure that one or the other retrace intervals was taking place before reading from or writing to the frame buffer. In these earlier systems, reading from or writing to frame buffer at times outside the retrace intervals meant that the CRT controller would be denied access to the frame buffer. This resulted in either snow or a flickering display. This bit provides compatibility with software designed for those early graphics controllers. This bit is currently used in DOS applications that access the palette to prevent the sparkle associated with read and write accesses to the palette ram with the same address on the same clock cycle. 0 = Active display data is being sent to the display. Neither a horizontal retrace interval or a vertical retrace interval is currently taking place. 1 = Either a horizontal retrace interval (horizontal blanking) or a vertical retrace interval (vertical blanking) is currently taking place.

4.4.2 ST00—Offset 3C2h

Input Status 0

Access Method

Type: ??? Register
(Size: 8 bits)

Offset: 3C2h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CRT_INTER_RUPT_PENDING	RESERVED		RGB_COMPARATOR_SENSE	RESERVED_1			

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**CRT_INTER_RUPT_PENDING:** This bit is here for EGA compatibility and will always return zero. Note that the generation of interrupts was originally enabled, through bits [4,5] of the Vertical Retrace End Register (CR11). This ability to generate interrupts at the start of the vertical retrace interval is a feature that is typically unused by DOS software and therefore is only supported through other means for use under a operating system support. 0 = CRT (vertical retrace interval) interrupt is not pending. 1 = CRT (vertical retrace interval) interrupt is pending
6:5	0x0 RO	**RESERVED:** Read as 0s.
4	0x0 RO	**RGB_COMPARATOR_SENSE:** This bit returns the state of the output of the RGB output comparator(s). Video BIOS uses this bit during POST to determine whether the display is connected and if it is a color or monochrome CRT. BIOS blanks the screen or clears the frame buffer to display only black. Next, BIOS outputs a ramp to the D-to-A converters to test for the presence of a color display by determining which code cause the comparator to switch. Finally, if the BIOS does not detect any termination resistors on Red or Blue, it tests for the presence of a display using the Green signal. The result of each such test is read via this bit. 0 = Below threshold 1 = Above threshold
3:0	0x0 RO	**RESERVED_1:** Read as 0s.

4.4.3 DACSTATE—Offset 3C7h

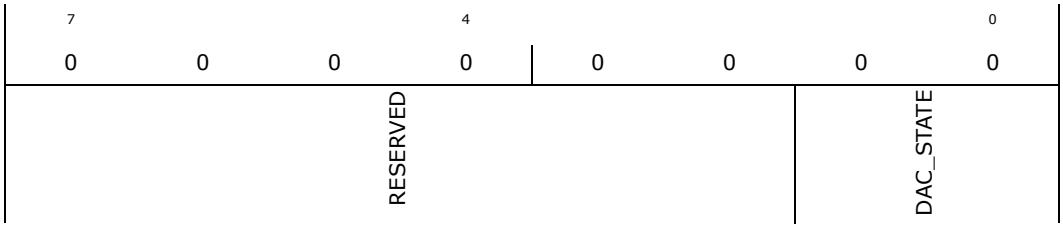
DAC State Register

Access Method

Type: ??? Register
(Size: 8 bits)

Offset: 3C7h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:2	0x0 RO	**RESERVED:** Read as 0.

Bit Range	Default & Access	Field Name (ID): Description
1:0	0x0 RO	**DAC_STATE:** This field indicates which of the two index registers was most recently written. Bits [1:0] Index Register Indicated 00 Palette Write Index Register at I/O Address 3C7h (default) 01 Reserved 10 Reserved 11 Palette Read Index Register at I/O Address 3C8h

4.4.4 ST01 (ST01_CGA)—Offset 3DAh

Input Status 1

Access Method

Type: ??? Register
(Size: 8 bits)

Offset: 3DAh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RESERVED_AS_PER_VGA_SPECIFICATION	RESERVED	VIDEO_FEEDBACK_1_0		VER_TI_CAL_RETRACE_VIDEO	RESERVED_1		DIS_PLAY_ENA_BLE_OUTPUT

Bit Range	Default & Access	Field Name (ID): Description
6	0x0 RO	**RESERVED:** Read as 0.
5:4	0x0 RO	**VIDEO_FEEDBACK_1_0:** These are diagnostic video bits that are selected by the Color Plane Enable Register. These bits that are programmably connected to 2 of the 8 color bits sent to the palette. Bits 4 and 5 of the Color Plane Enable Register (AR12) selects which two of the 8 possible color bits become connected to these 2 bits of this register. The current software normally does not use these 2 bits. They exist for EGA compatibility.
3	0x0 RO	**VER_TI_CAL_RETRACE_VIDEO:** 0 = VSYNC inactive (Indicates that a vertical retrace interval is not taking place). 1 = VSYNC active (Indicates that a vertical retrace interval is taking place).

Bit Range	Default & Access	Field Name (ID): Description
2:1	0x0 RO	**RESERVED_1:** Read as 0s.
0	0x0 RO	**DIS_PLAY_ENA_BLE_OUTPUT:** Display Enable is a status bit (bit 0) in Input Status Register 1 that indicates when either a horizontal retrace interval or a vertical retrace interval is taking place. This was used with the IBM* EGA graphics system (and the ones that preceded it, including MDA and CGA). In those cases, it was important to check the status of this bit to ensure that one or the other retrace intervals was taking place before reading from or writing to the frame buffer. In these earlier systems, reading from or writing to frame buffer at times outside the retrace intervals meant that the CRT controller would be denied access to the frame buffer. This resulted in either snow or a flickering display. This bit provides compatibility with software designed for those early graphics controllers. This bit is currently used in DOS applications that access the palette to prevent the sparkle associated with read and write accesses to the palette ram with the same address on the same clock cycle.

4.5 WRITE Address Map (Read Only)

Table 25. Summary of Display Memory Mapped I/O Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3BA–3BAh	1	"FCR (FCR_MDA_Write)—Offset 3BAh" on page 967	00h
3C2–3C2h	1	"MSR (MSR_Write)—Offset 3C2h" on page 967	00h
3C7–3C7h	1	"DACRX—Offset 3C7h" on page 968	00h
3DA–3DAh	1	"FCR (FCR_CGA_Write)—Offset 3DAh" on page 969	00h

4.5.1 FCR (FCR_MDA_Write)—Offset 3BAh

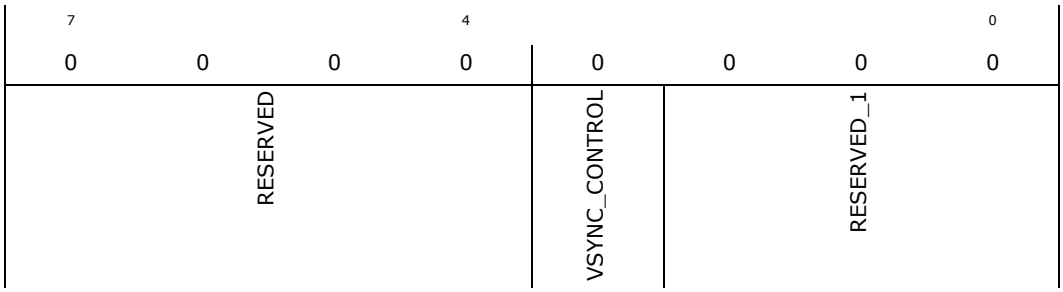
Feature Control

Access Method

Type: ??? Register
(Size: 8 bits)

Offset: 3BAh

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RO	**RESERVED:** Read as 0.
3	0x0 RW	**VSYNC_CONTROL:** This bit is provided for compatibility only and has no other function. Reads and writes to this bit have no effect other than to change the value of this bit. The previous definition of this bit selected the output on the VSYNC pin. 0 = Was used to set VSYNC out put on the VSYNC pin (default). 1 = Was used to set the log i cal 'OR' of VSYNC and Display Enable output on the VSYNC pin. This capability was not typically very useful..
2:0	0x0 RO	**RESERVED_1:** Read as 0.

4.5.2 MSR (MSR_Write)—Offset 3C2h

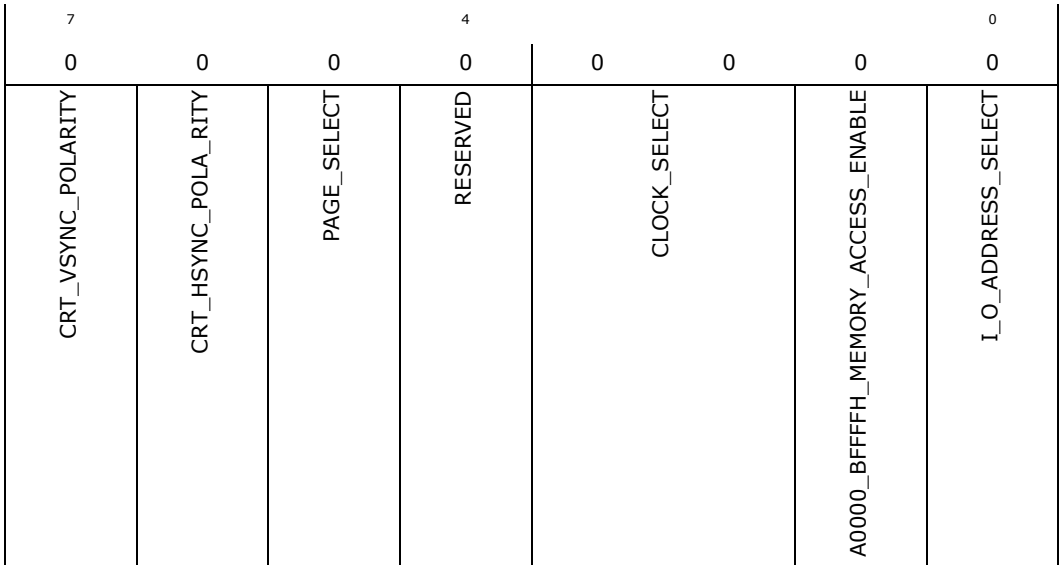
Miscellaneous Output

Access Method

Type: ??? Register
(Size: 8 bits)

Offset: 3C2h

Default: 00h



7			4				0
0	0	0	0	0	0	0	0
CRT_VSYNC_POLARITY	CRT_HSYNC_POLA_RITY	PAGE_SELECT	RESERVED	CLOCK_SELECT		A0000_BFFFFH_MEMORY_ACCESS_ENABLE	I_O_ADDRESS_SELECT

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**PAGE_SELECT:** In Odd/Even Memory Map Mode 1 (GR6), this bit selects the upper or lower 64 KB page in dis play memory for CPU access: 0 = Upper page (default) 1 = Lower page. Selects between two 64KB pages of frame buffer memory during standard odd/even modes (modes 0h through 5h). Bit 1 of register GR06 can also program this bit in other modes. Note that this bit is would normally set to 1 by the software.
4	0x0 RO	**RESERVED:** Read as 0.
0	0x0 RW	**I_O_ADDRESS_SELECT:** This bit selects 3Bxh or 3Dxh as the I/O address for the CRT Controller registers, the Feature Control Register (FCR), and Input Status Register 1 (ST01). Presently ignored (whole range is claimed), but will ignore 3Bx for color configuration or 3Dx for monochrome. Note that it is typical in AGP chipsets to shadow this bit and properly steer I/O cycles to the proper bus for operation where a MDA exists on another bus such as ISA. 0 = Select 3Bxh I/O address (MDA emulation) (default). 1 = Select 3Dxh I/O address (CGA emulation).

4.5.3 DACRX—Offset 3C7h

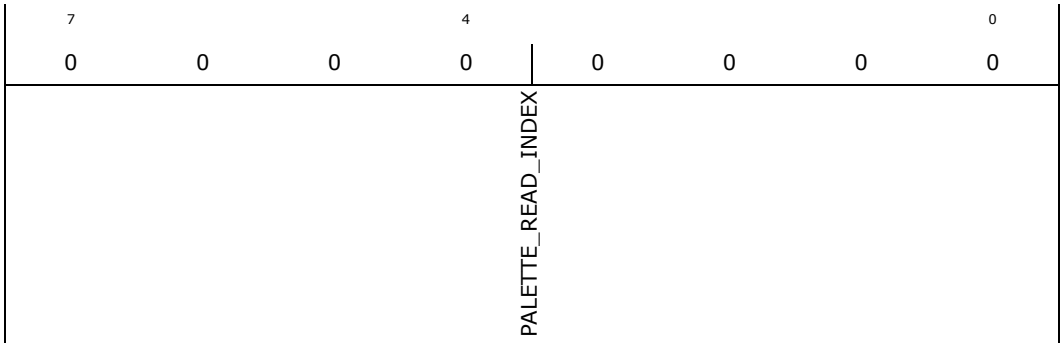
Palette Read Index Register

Access Method

Type: ??? Register
(Size: 8 bits)

Offset: 3C7h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 WO	**PALETTE_READ_INDEX:** The 8-bit index value programmed into this register chooses which of 256 standard color data positions within the palette are to be made accessible for being read from via the Palette Data Register (DACDATA). The index value held in this register is automatically incremented when all three bytes of the color data position selected by the current index have been read. A write to this register will abort a uncompleted palette write sequence. This register allows access to the palette even when running display modes.

4.5.4 FCR (FCR_CGA_Write)—Offset 3DAh

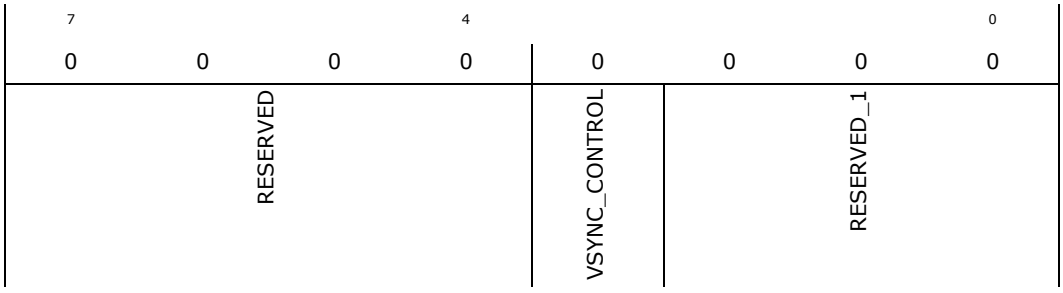
Feature Control

Access Method

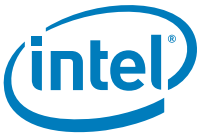
Type: ??? Register
(Size: 8 bits)

Offset: 3DAh

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RO	**RESERVED:** Read as 0.



Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**VSYNC_CONTROL:** This bit is provided for compatibility only and has no other function. Reads and writes to this bit have no effect other than to change the value of this bit. The previous definition of this bit selected the output on the VSYNC pin. 0 = Was used to set VSYNC out put on the VSYNC pin (default). 1 = Was used to set the log i cal 'OR' of VSYNC and Display Enable output on the VSYNC pin. This capability was not typically very useful..
2:0	0x0 RO	**RESERVED_1:** Read as 0.

5 MIPI*- CSI (Camera Serial Interface) and ISP Registers

5.1 Image Signal Processor PCI Configuration Registers

Table 26. Summary of Image Signal Processor PCI Configuration Registers—0/3/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"iunit_ID_type (ID)—Offset 0h" on page 974	22B88086h
4–7h	4	"iunit_PCICMDSTS_type (PCICMDSTS)—Offset 4h" on page 974	00100000h
8–Bh	4	"iunit_RIDCC_type (RIDCC)—Offset 8h" on page 975	04800000h
C–Fh	4	"iunit_HDR_type (HDR)—Offset Ch" on page 976	00000000h
10–13h	4	"iunit_ISPMMADR_type (ISPMMADR)—Offset 10h" on page 976	00000000h
2C–2Fh	4	"iunit_SSID_type (SSID)—Offset 2Ch" on page 977	00000000h
34–37h	4	"iunit_CAPPOINT_type (CAPPOINT)—Offset 34h" on page 978	00000080h
3C–3Fh	4	"iunit_INTR_type (INTR)—Offset 3Ch" on page 978	00000000h
80–83h	4	"iunit_PMCAP_type (PMCAP)—Offset 80h" on page 979	00229001h
84–87h	4	"iunit_PMCS_type (PMCS)—Offset 84h" on page 980	00000000h
90–93h	4	"iunit_MSI_CAPID_type (MSI_CAPID)—Offset 90h" on page 980	00000005h
94–97h	4	"iunit_MSI_ADDRESS_type (MSI_ADDRESS)—Offset 94h" on page 981	00000000h
98–9Bh	4	"iunit_MSI_DATA_type (MSI_DATA)—Offset 98h" on page 982	00000000h
9C–9Fh	4	"iunit_INTERRUPT_CONTROL_type (INTERRUPT_CONTROL)—Offset 9Ch" on page 982	00000100h
B0–B3h	4	"iunit_PERF0_type (PERF0)—Offset B0h" on page 983	00000000h
B4–B7h	4	"iunit_PERF1_type (PERF1)—Offset B4h" on page 984	00000000h
B8–BBh	4	"iunit_PERF2_type (PERF2)—Offset B8h" on page 985	00000000h
BC–BFh	4	"iunit_PERF3_type (PERF3)—Offset BCh" on page 985	00000000h
C0–C3h	4	"iunit_MISR0_type (MISR0)—Offset C0h" on page 986	FFFFFFFFh
C4–C7h	4	"iunit_MISR1_type (MISR1)—Offset C4h" on page 987	FFFFFFFFh
C8–CBh	4	"iunit_MISR2_type (MISR2)—Offset C8h" on page 987	FFFFFFFFh
CC–CFh	4	"iunit_MISR3_type (MISR3)—Offset CCh" on page 988	FFFFFFFFh
D0–D3h	4	"iunit_MANUFACTURING_ID_type (MANUFACTURING_ID)—Offset D0h" on page 988	00000000h
D4–D7h	4	"iunit_IUNIT_ACCESS_CTRL_VIOL_type (IUNIT_ACCESS_CTRL_VIOL)—Offset D4h" on page 989	00000000h
D8–DBh	4	"iunit_IUNIT_DEADLINE_STATUS_type (IUNIT_DEADLINE_STATUS)—Offset D8h" on page 990	00000000h

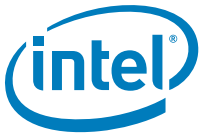


Table 26. Summary of Image Signal Processor PCI Configuration Registers—0/3/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
DC–DFh	4	"iunit_IUNIT_AFE_HS_CONTROL_type (IUNIT_AFE_HS_CONTROL)—Offset DCh" on page 991	64000A00h
E0–E3h	4	"iunit_IUNIT_AFE_RCOMP_CONTROL_type (IUNIT_AFE_RCOMP_CONTROL)—Offset E0h" on page 992	00000000h
E8–EBh	4	"iunit_IUNIT_CSI_CONTROL_type (IUNIT_CSI_CONTROL)—Offset E8h" on page 993	000007F8h
EC–EFh	4	"iunit_IUNIT_DEADLINE_CONTROL_type (IUNIT_DEADLINE_CONTROL)—Offset ECh" on page 994	040A0100h
F0–F3h	4	"iunit_IUNIT_RCOMP_STATUS_type (IUNIT_RCOMP_STATUS)—Offset F0h" on page 995	0C0C0C0Ch
F4–F7h	4	"iunit_IUNIT_RCOMP_CONTROL_type (IUNIT_RCOMP_CONTROL)—Offset F4h" on page 997	00200001h
F8–FBh	4	"iunit_IUNIT_STATUS_type (IUNIT_STATUS)—Offset F8h" on page 998	0000EB01h
FC–FFh	4	"iunit_IUNIT_CONTROL_type (IUNIT_CONTROL)—Offset FCh" on page 999	00000103h

5.1.1 iunit_ID_type (ID)—Offset 0h

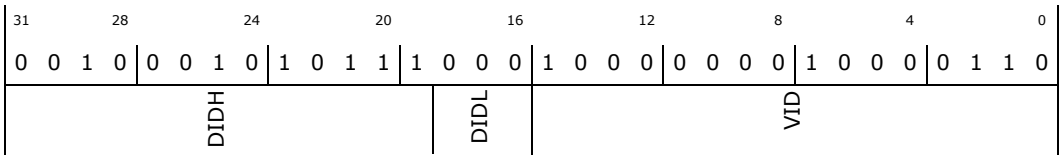
PCI Device and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 0h

Default: 22B88086h



Bit Range	Default and Access	Field Name (ID): Description
31:19	0x457 RO	**DIDH:** DEVICE_IDENTIFICATION_NUMBER_HIGH: Upper bits of ISP Device ID. Connected to straps at I-unit top level.
18:16	0x0 RO	**DIDL:** DEVICE_IDENTIFICATION_NUMBER_LOW: Lower bits of ISP Device ID. Connected to fuse FB_isp_device_id.
15:0	0x8086 RO	**VID:** VENDOR_IDENTIFICATION_NUMBER: PCI standard identification for Intel.

5.1.2 iunit_PCICMDSTS_type (PCICMDSTS)—Offset 4h

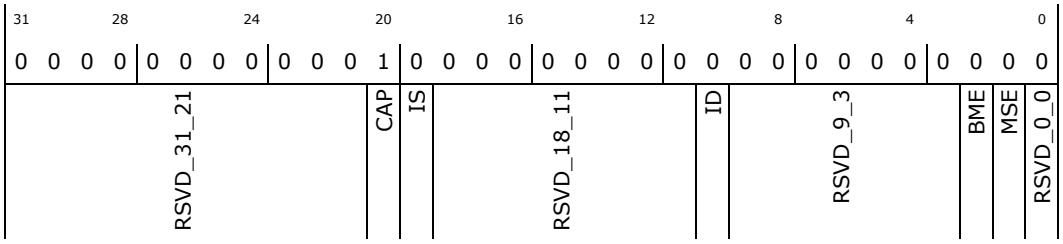
PCI Command and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 4h

Default: 00100000h



Bit Range	Default and Access	Field Name (ID): Description
31:21	0x0 RO	**RSVD_31_21:** Reserved
20	0x1 RO	**CAP:** CAPABILITY_LIST: Indicates that the CAPPOINT register at 34h provides an offset into PCI Configuration Space containing a pointer to the location of the first item in the list.

Bit Range	Default and Access	Field Name (ID): Description
19	0x0 RO	**IS:** INTERRUPT_STATUS: Reflects the state of the interrupt in the camera device. Is set to 1 if IER and IIR are both set. Otherwise is set to 0.
18:11	0x0 RO	**RSVD_18_11:** Reserved
10	0x0 RW	**ID:** INTERRUPT_DISABLE: When 1, blocks the sending of ASSERT_INTA and DEASSERT_INTA messages to the Intel Legacy Block (ILB). The interrupt status is not blocked from being reflected in PCICMDSTS.IS. When 0, permits the sending of ASSERT_INTA and DEASSERT_INTA messages to the ILB.
9:3	0x0 RO	**RSVD_9_3:** Reserved
2	0x0 RW	**BME:** BUS_MASTER_ENABLE: Enables ISP to function as a PCI compliant master. When 0, blocks the sending of MSI interrupts. When 1, permits the sending of MSI interrupts.
1	0x0 RW	**MSE:** MEMORY_SPACE_ENABLE: When set, accesses to this device's memory space is enabled. When 1, the ISP will compare the incoming address on the IOSF bus with ISPMMADR(31:22). If there is a match and if the IOSF command is either a MEMRD or MEMWR, the ISP will select the command and present it on the AHB bus. When 0, the ISP will not claim MEMRD or MEMWR IOSF commands.
0	0x0 RO	**RSVD_0_0:** Reserved

5.1.3 iunit_RIDCC_type (RIDCC)—Offset 8h

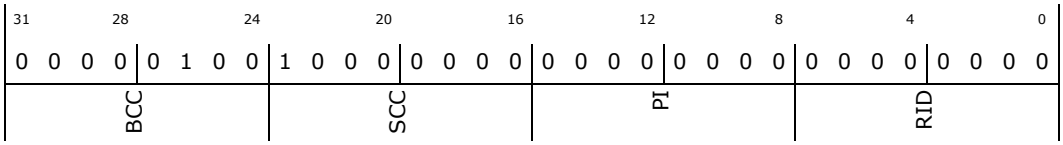
Revision Identification and Class Codes

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 8h

Default: 04800000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x4 RO	**BCC:** BASE_CLASS_CODE: Indicates a multimedia device.
23:16	0x80 RO	**SCC:** SUB_CLASS_CODE: Indicates other multimedia device.
15:8	0x0 RO	**PI:** PROGRAMMING_INTERFACE: Default programming interface.

Bit Range	Default and Access	Field Name (ID): Description
7:0	0x0 RO	**RID:** REVISION_ID: The value in this field reflects the value of strapRID(7:0) (which is an input pin of ISP) and can be changed with each stepping of the silicon.

5.1.4 iunit_HDR_type (HDR)—Offset Ch

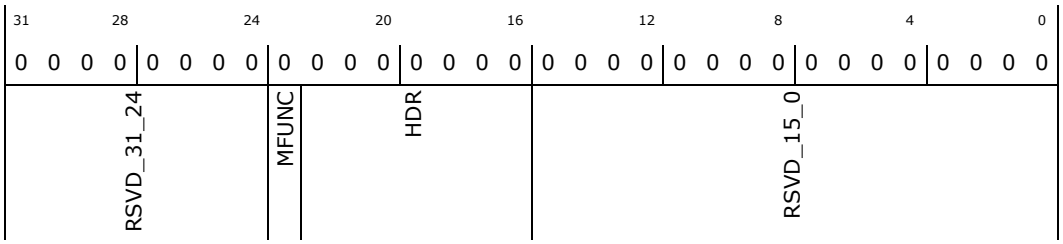
Header Type

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + Ch

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD_31_24:** Reserved
23	0x0 RO	**MFUNC:** MULTI_FUNCTION_STATUS: I-unit is a single function.
22:16	0x0 RO	**HDR:** HEADER_CODE: Indicates a type 0 header format.
15:0	0x0 RO	**RSVD_15_0:** Reserved

5.1.5 iunit_ISPMMADR_type (ISPMMADR)—Offset 10h

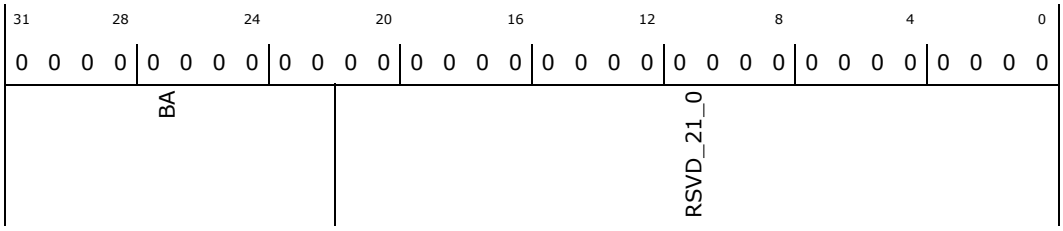
Memory Mapped Address Range. This is the base address for all memory mapped registers.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:22	0x0 RW	**BA:** BASE_ADDRESS: Set by the OS, these bits correspond to address signals (31:22). The ISP will compare the IOSF address (31:22) with ISPMMADR(31:22). If there is a match, and PCICMDSTS(1) = MSE = 1 and the IOSF command is either a MEMRD or MEMWR, the ISP will select the command and present it on the AHB bus to the vendor IP.
21:0	0x0 RO	**RSVD_21_0:** Reserved

5.1.6 iunit_SSID_type (SSID)—Offset 2Ch

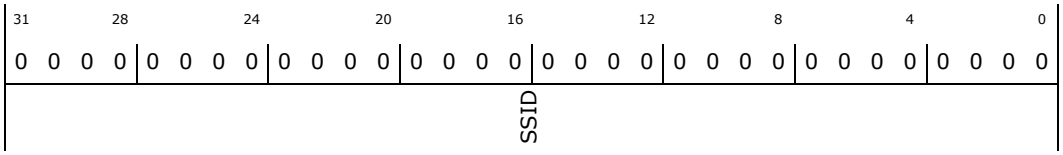
Subsystem Identifiers

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 2Ch

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**SSID:** SUBSYSTEM_IDENTIFIERS: The value in this field is a copy of the SSID register programmed by the graphics device driver or BIOS in the Device 0/2/0 PCI header. To change the subsystem ID, write to Device 0/2/0 SSID instead of to this SSID.

5.1.7 iunit_CAPPOINT_type (CAPPOINT)—Offset 34h

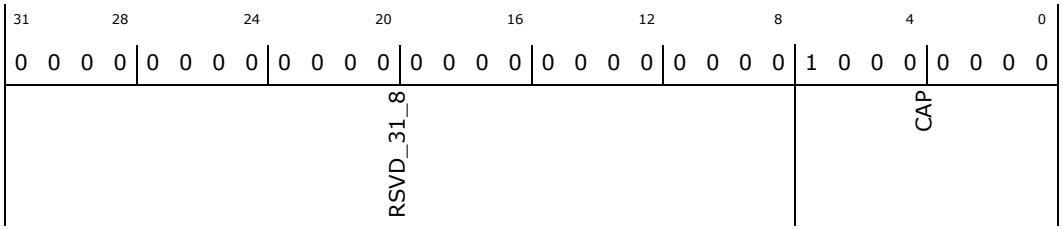
Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 34h

Default: 00000080h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD_31_8:** Reserved
7:0	0x80 RO	**CAP:** CAPABILITIES_POINTER: The first item in the capabilities list is at address 80h.

5.1.8 iunit_INTR_type (INTR)—Offset 3Ch

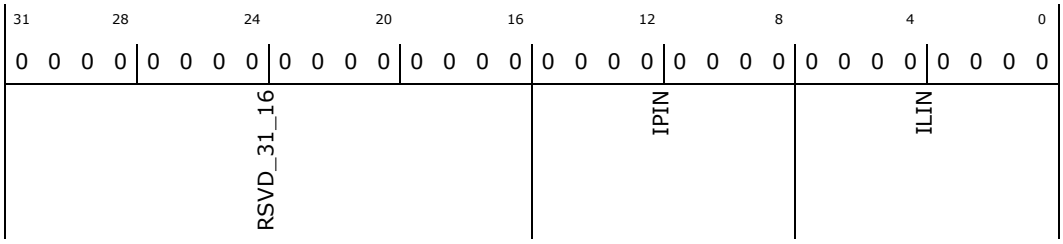
Interrupt—This register is programmed by SBIOS.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 3Ch

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD_31_16:** Reserved
15:8	0x0 RO	**IPIN:** INTERRUPT_PIN: PCI Device 0/3/0 (I-unit) is a single function device. If INTx is used, the PCI spec requires that it use INTA#. If INTx is used (FB_intx_supported fuse is 1), then this field is hard coded to 01h. If INTx is not used (FB_intx_supported fuse is 0), this field is hard coded to 00h.
7:0	0x0 RW	**ILIN:** INTERRUPT_LINE: BIOS written value to communicate interrupt line routing information to the ISP device driver.

5.1.9 iunit_PMCAP_type (PMCAP)—Offset 80h

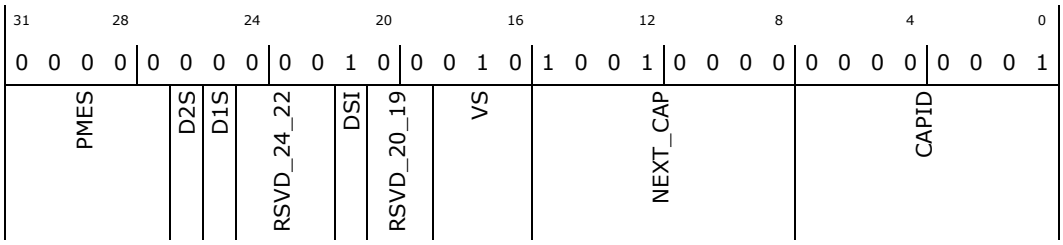
Power Management Capabilities

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 80h

Default: 00229001h



Bit Range	Default and Access	Field Name (ID): Description
31:27	0x0 RO	**PMES:** PME_SUPPORT: The camera controller does not generate PME#.
26	0x0 RO	**D2S:** D2_SUPPORT: The D2 power management state is not supported.

Bit Range	Default and Access	Field Name (ID): Description
25	0x0 RO	**D1S:** D1_SUPPORT: The D1 power management state is not supported.
24:22	0x0 RO	**RSVD_24_22:** Reserved
21	0x1 RO	**DSI:** DEVICE_SPECIFIC_INITIALIZATION: Hardwired to 1 to indicate that special initialization of the camera controller is required before generic class device driver is to use it.
20:19	0x0 RO	**RSVD_20_19:** Reserved
18:16	0x2 RO	**VS:** VERSION: Indicates compliance with revision 1.1 of the PCI Power Management Specification.
15:8	0x90 RO	**NEXT_CAP:** POINTER_TO_NEXT_CAPABILITY: Indicates the next item in the capabilities list.
7:0	0x1 RO	**CAPID:** CAPABILITIES: SIG defines this ID is 01h for power management.

5.1.10 iunit_PMCS_type (PMCS)—Offset 84h

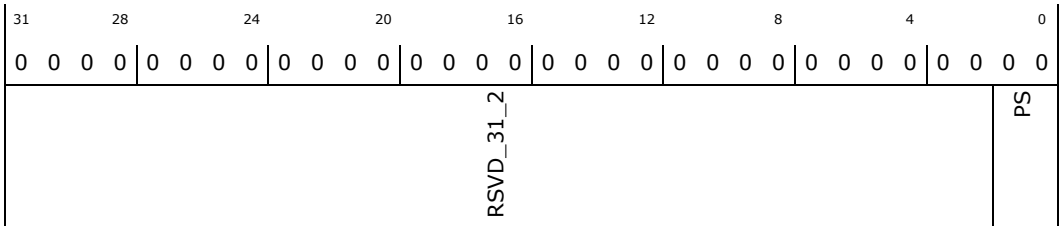
Power Management Control/Status.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 84h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RO	**RSVD_31_2:** Reserved
1:0	0x0 RW	**PS:** POWER_STATE: Power management is implemented by writing to control registers in the P-unit. This field may be programmed by the software driver, but no action is taken based on writing to this field.

5.1.11 iunit_MSI_CAPID_type (MSI_CAPID)—Offset 90h

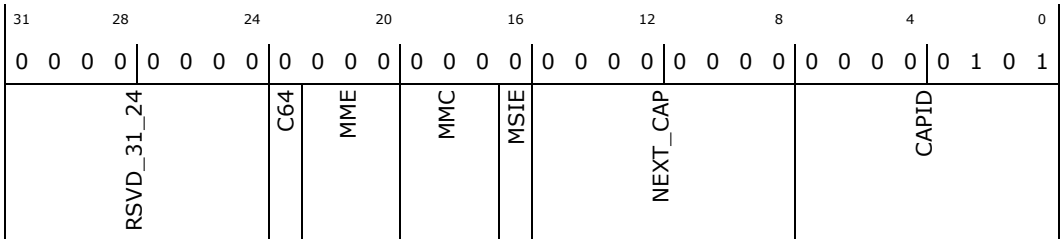
Message Signaled Interrupts Capability ID and Control Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 90h

Default: 00000005h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD_31_24:** Reserved
23	0x0 RO	**C64:** 64_BIT_ADDRESS_CAPABLE: 32-bit capable only.
22:20	0x0 RW	**MME:** MULTIPLE_MESSAGE_ENABLE: This field is RW for software compatibility, but only a single message is ever generated.
19:17	0x0 RO	**MMC:** MULTIPLE_MESSAGE_CAPABLE: This device is only single message capable.
16	0x0 RW	**MSIE:** MSI_ENABLE: If set, MSI is enabled. PCICMDSTS.BME must be set for an MSI to be generated.When 0, blocks the sending of a MSI interrupt. The interrupt status is not blocked from being reflected in the PCICMDSTS.IS bit. When 1, permits sending of a MSI interrupt.
15:8	0x0 RO	**NEXT_CAP:** POINTER_TO_NEXT_CAPABILITY: Indicates this is the last item in the list.
7:0	0x5 RO	**CAPID:** CAPABILITY_ID: Indicates an MSI capability.

5.1.12 iunit_MSI_ADDRESS_type (MSI_ADDRESS)—Offset 94h

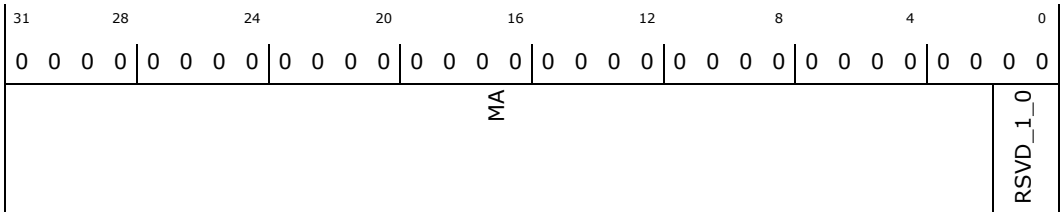
MSI Message Address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 94h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**MA:** MSI_ADDRESS: System specified message address, always DW aligned. When the ISP issues an MSI interrupt as a MEMWR on the IOSF, the memory address used is 12xFEE, MSI_ADDRESS[19:0].
1:0	0x0 RO	**RSVD_1_0:** Reserved

5.1.13 iunit_MSI_DATA_type (MSI_DATA)—Offset 98h

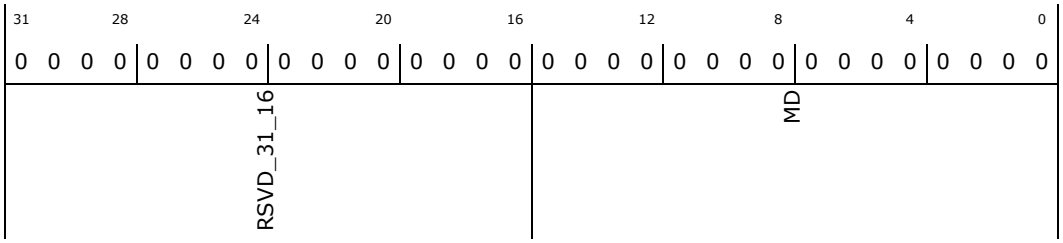
MSI Message Data

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 98h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD_31_16:** Reserved
15:0	0x0 RW	**MD:** MSI_DATA: This 16-bit field is programmed by system software and is driven onto the lower word of data during the data phase of the MSI write transaction. When the ISP issues an MSI interrupt as a MEMWR on the IOSF, the write data corresponds to the value of this field.

5.1.14 iunit_INTERRUPT_CONTROL_type (INTERRUPT_CONTROL)—Offset 9Ch

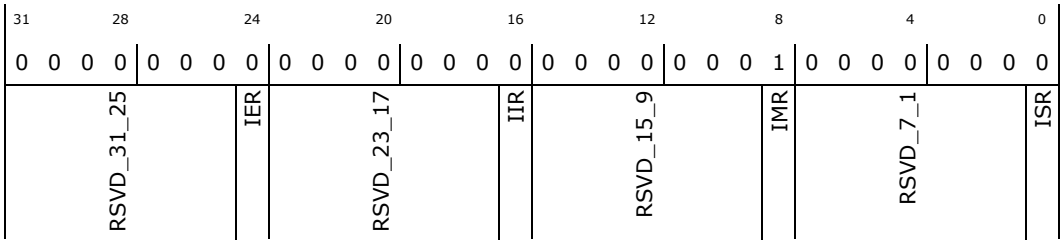
INTERRUPT_CONTROL

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 9Ch

Default: 00000100h



Bit Range	Default and Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD_31_25:** Reserved
24	0x0 RW	**IER:** IER: This is an enable bit that allows the sending of an interrupt to the CPU using either MSI or INTR mechanisms. The interrupt is sent immediately to the CPU. The firmware running on the ISP guarantees ordering by reading the last data write from memory before raising the interrupt. 1 = If MSI_ENABLE is set, then an MSI is sent to the CPU when the IIR bit is set, or if the IIR bit remains set after software writes to this register. If INTERRUPT_DISABLE is not set, then an ASSERT_INTA message is sent to the Intel Legacy Block (ILB) when the IIR bit is set by hardware, or if the IIR bit remains set after software writes to this register. If software clears the IIR bit, and INTERRUPT_DISABLE is not set then a DEASSERT_INTA message is sent to the ILB. 0 = Do not generate an MSI even if the MSI_ENABLE bit is set. Do not send ASSERT_INTA or DEASSERT_INTA messages to the ILB even if the INTERRUPT_DISABLE bit is not set.
23:17	0x0 RO	**RSVD_23_17:** Reserved
16	0x0 RW/1C	**IIR:** IIR: This is the persistent value of the interrupt bit. It is set by hardware, and cleared by software. Software must write a 1 to clear this bit. Writing a 0 is a NOP. If both software and hardware attempt to write to this field in the same clock cycle, hardware wins. 1 = An interrupt was received from the vendor IP when the IMR bit was not set, and software has not yet cleared it. 0 = There is no pending interrupt.
15:9	0x0 RO	**RSVD_15_9:** Reserved
8	0x1 RW	**IMR:** IMR: Interrupt Mask bit. 1 = IIR bit will not be set when the ISR bit is set. 0 = IIR bit will be set when the ISR bit is set.
7:1	0x0 RO	**RSVD_7_1:** Reserved
0	0x0 RO	**ISR:** ISR: Reflects the state of the interrupt line from the vendor IP, after it is synchronized to the czclk domain.

5.1.15 iunit_PERF0_type (PERF0)—Offset B0h

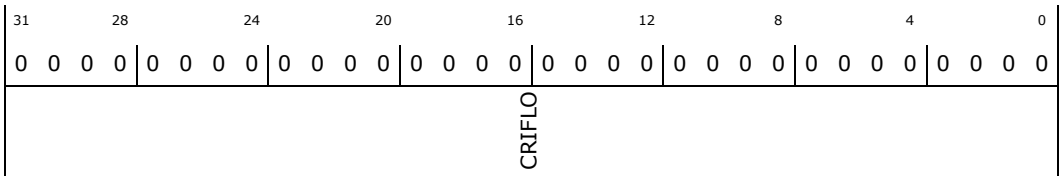
Performance

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + B0h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW/SE	**CRIFLO:** The I-unit has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 31:0 of the cumulative_reads_in_flight counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will enable all four counters.

5.1.16 iunit_PERF1_type (PERF1)—Offset B4h

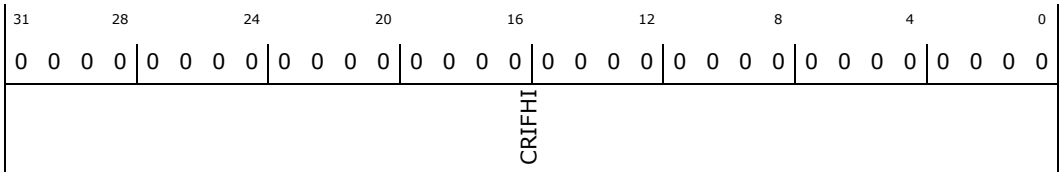
Performance

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + B4h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW/SE	**CRIFHI:** I-unit has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 63:32 of the cumulative_reads_in_flight counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will disable all four counters.

5.1.17 iunit_PERF2_type (PERF2)—Offset B8h

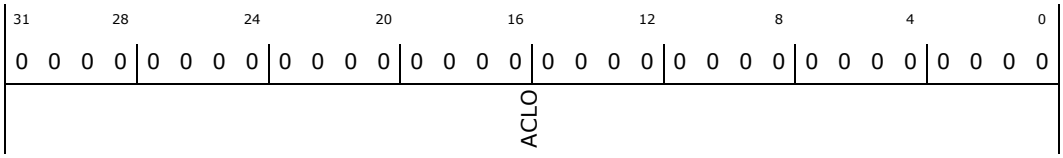
Performance

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + B8h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW/SE	**ACLO:** I-unit has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 31:0 of the active_cycles counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will clear all four counters. The counters should only be cleared after they are disabled.

5.1.18 iunit_PERF3_type (PERF3)—Offset BCh

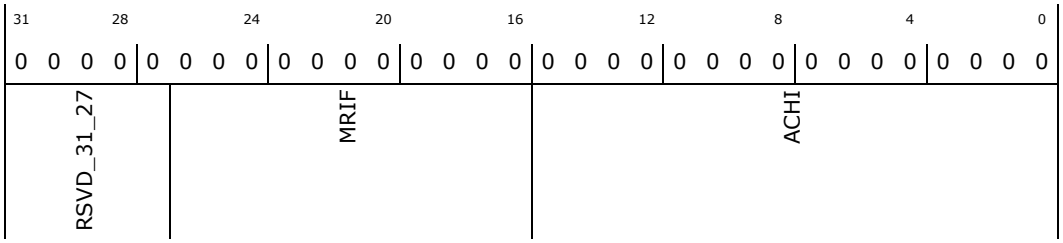
Performance

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + BCh

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:27	0x0 RO	**RSVD_31_27:** Reserved
26:16	0x0 RW/SE	**MRIF:** I-unit has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 11:0 of the max_reads_in_flight counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will clear the max_reads_in_flight counters only. The counters should only be cleared after they are disabled.
15:0	0x0 RW/SE	**ACHI:** I-unit has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 47:32 of the active_cycles counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will clear the max_reads_in_flight counters only. The counters should only be cleared after they are disabled.

5.1.19 iunit_MISR0_type (MISR0)—Offset C0h

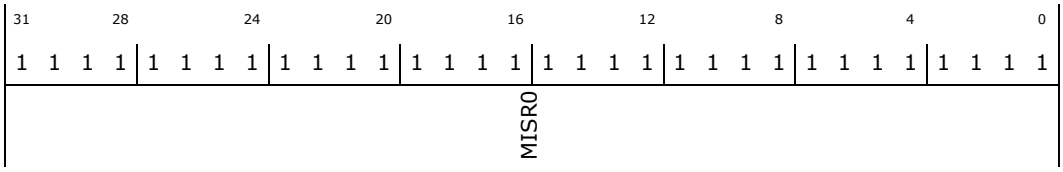
OCP Master Write Data

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + C0h

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW/C	**MISR0:** MISR0: Write to this register address clears this MISR. This is a 8:1 compression MISR capturing the 256-bit write data on the OCP interface between ISP_CSS and I-unit wrapper.

5.1.20 iunit_MISR1_type (MISR1)—Offset C4h

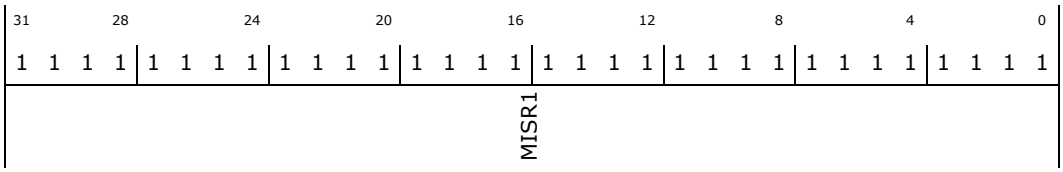
OCP Master Read Data

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + C4h

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW/C	**MISR1:** MISR1: Write to this register address clears this MISR. This is a 8:1 compression MISR capturing the 256-bit read return data on the OCP interface between ISP_CSS and I-unit wrapper.

5.1.21 iunit_MISR2_type (MISR2)—Offset C8h

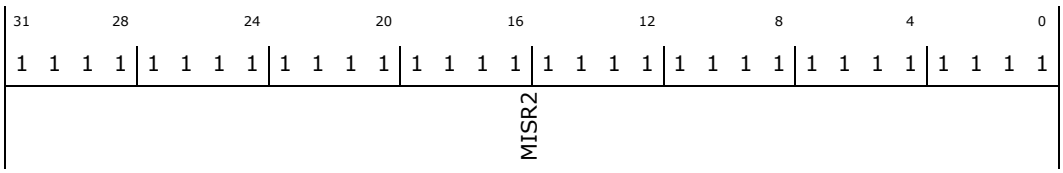
OCP Master Address and Control

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + C8h

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW/C	**MISR2:** MISR2: Write to this register address clears this MISR. This is a 4:1 compression MISR capturing the control signals on the OCP Master port in the I-unit.

5.1.22 iunit_MISR3_type (MISR3)—Offset CCh

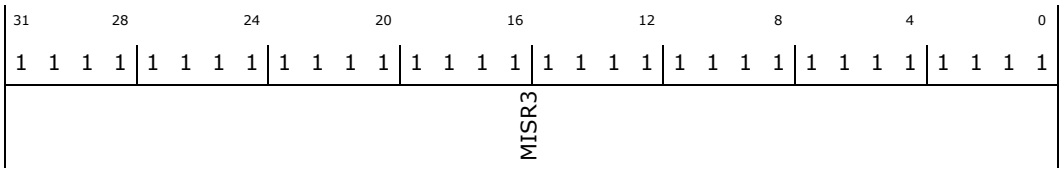
Scalar Processor Output

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + CCh

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW/C	**MISR3:** MISR3: Write to this register address clears this MISR. This is a 4:1 compression MISR capturing the output signals of the Scalar Processor.

5.1.23 iunit_MANUFACTURING_ID_type (MANUFACTURING_ID)—Offset D0h

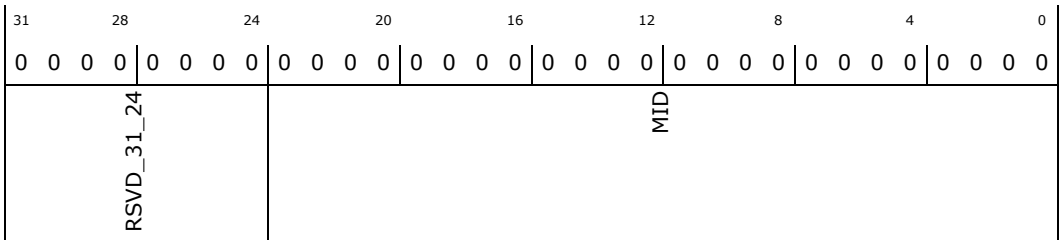
Manufacturing ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + D0h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD_31_24:** Reserved
23:0	0x0 RO	**MID:** MANUFACTURING_ID: Hardwired to strapMANID (23:0).

5.1.24 iunit_IUNIT_ACCESS_CTRL_VIOL_type (IUNIT_ACCESS_CTRL_VIOL)—Offset D4h

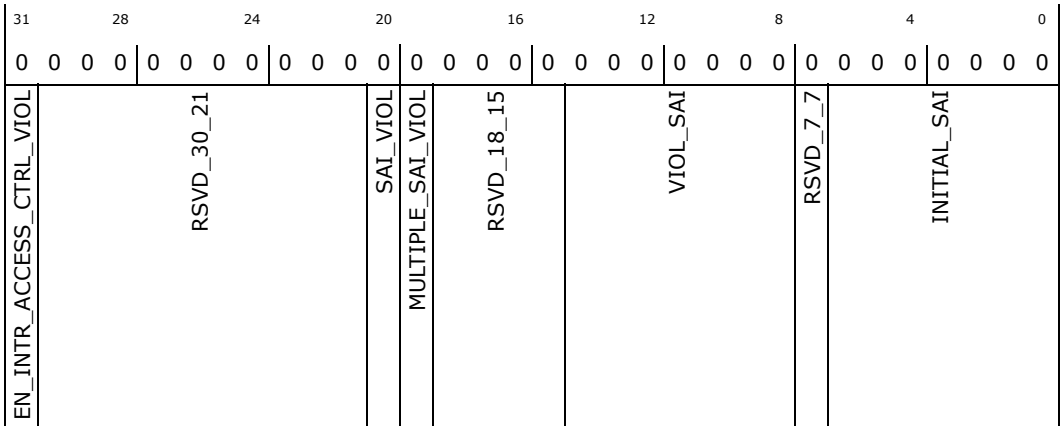
I-unit Access Control Violation Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + D4h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**EN_INTR_ACCESS_CTRL_VIOL:** Enable Interrupt on access control violation: When set, the I-unit will latch violation information into this register and send an interrupt request (opcode 0XEE) and (port 0x04) to the P-unit.
30:21	0x0 RO	**RSVD_30_21:** Reserved
20	0x0 RW	**SAI_VIOL:** SAI_VIOL: If set, the I-unit has detected an SAI violation and has captured the status in this register. This bit must be cleared by software in order for I-unit to capture the next violation.
19	0x0 RW	**MULTIPLE_SAI_VIOL:** If set, more than one SAI violation has been detected in the I-unit. Status for the 1st violation has been captured in this register. It is recommend that software clear this bit whenever it clears bit[20] of this register.

Bit Range	Default and Access	Field Name (ID): Description
18:15	0x0 RO	**RSVD_18_15:** Reserved
14:8	0x0 RW	**VIOL_SAI:** VIOL_SAI: SAI bits that triggered the violation: This 7-bit value indicates the SAI of the subsequent transaction which caused the violation.
7	0x0 RO	**RSVD_7_7:** Reserved
6:0	0x0 RW	**INITIAL_SAI:** INITIAL_SAI: This 7-bit value indicates the SAI of the initial transaction for SAI mismatch error codes.

5.1.25 iunit_IUNIT_DEADLINE_STATUS_type (IUNIT_DEADLINE_STATUS)—Offset D8h

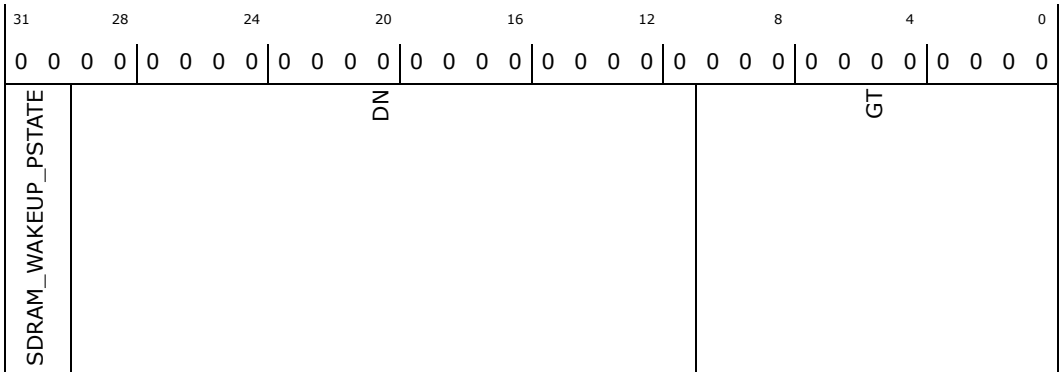
I-unit Deadline Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + D8h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RO	**SDRAM_WAKEUP_PSTATE:** SDRAM_WAKEUP_PSTATE: State of the SDRAM_WAKEUP state machine. 00b = State machine is idle; 01b = sdram_wakeup seen, waiting for all memory transactions in flight to complete; 10b = All memory transactions are completed, waiting for acknowledgement from czclk domain before returning to idle state;
29:11	0x0 RO	**DN:** DN: Computed deadline value to be send with the next request on IB PFI bus. This is the internal deadline value. The actual deadline that is sent on the IB PFI bus is the maximum of GT+MDD or DN.
10:0	0x0 RO	**GT:** GT: Current value of Global Timer

5.1.26 iunit_IUNIT_AFE_HS_CONTROL_type (IUNIT_AFE_HS_CONTROL)—Offset DCh

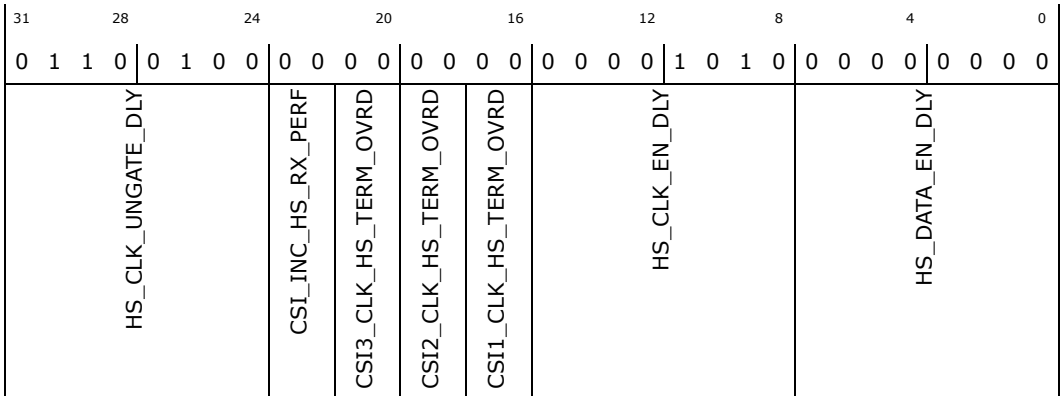
High-speed Termination Control MIPI*-CSI DPHY

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + DCh

Default: 64000A00h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x64 RW	**HS_CLK_UNGATE_DLY:** HS_CLK_UNGATE_DLY: Delay between the assertion of HS enable and the ungating of the HS clocks going to the DPHY logic for all clock lanes. HS clocks are gated by default and are ungated after Tclk-settle time. The range of this field is 0–510 nanoseconds in increments of 2 nanoseconds, with reset value 0x64 indicating 200 nanoseconds. **Note**: Intel uses the czclk to increment the counter, hence the actual delay can be as much as 10 nanoseconds larger than the programmed value.
23:22	0x0 RW	**CSI_INC_HS_RX_PERF:** INC_HS_RX_PERF: Config bits to increase the High-speed Receiver performance; 00 = POR (default), 01 = +10% bias current (Stage 1 adder), 10 = TBD, 11 = TBD
21:20	0x0 RW	**CSI3_CLK_HS_TERM_OVRD:** CSI3_CLK_HS_TERM_OVRD: Override for HS termination enable for CSI3 clock lane. 00b = Use the termination enable output from the DPHY IP and gate XOR clocks in high speed mode; 01b = Keep HS termination (and HS enable) always-on; 10b = Generate HS termination by sampling the CP/CN lines using coreclk and gate XOR clocks in high speed mode; 11b = Use the termination enable output from the DPHY IP;
19:18	0x0 RW	**CSI2_CLK_HS_TERM_OVRD:** CSI2_CLK_HS_TERM_OVRD: Override for HS termination enable for CSI2 clock lane. 00b = Use the termination enable output from the DPHY IP and gate XOR clocks in high speed mode; 01b = Keep HS termination (and HS enable) always-on; 10b = Generate HS termination by sampling the CP/CN lines using coreclk and gate XOR clocks in high speed mode; 11b = Use the termination enable output from the DPHY IP;

Bit Range	Default and Access	Field Name (ID): Description
17:16	0x0 RW	**CSI1_CLK_HS_TERM_OVRD:** CSI1_CLK_HS_TERM_OVRD: Override for HS termination enable for CSI1 clock lane. 00b = Use the termination enable output from the DPHY IP and gate XOR clocks in high speed mode; 01b = Keep HS termination (and HS enable) always-on; 10b = Generate HS termination by sampling the CP/CN lines using coreclk and gate XOR clocks in high speed mode; 11b = Use the termination enable output from the DPHY IP;
15:8	0xa RW	**HS_CLK_EN_DLY:** HS_CLK_EN_DLY: Delay between the assertion of HS termination enable and the assertion of HS enable for all clock lanes. The range of this field is 0 nanoseconds to 510 nanoseconds in increments of 2 nanoseconds, with reset value 0x0A indicating 20 nanoseconds. **Note**: that we use czclk to increment the counter, hence the actual delay can be as much as 10 nanoseconds larger than the programmed value.
7:0	0x0 RW	**HS_DATA_EN_DLY:** HS_DATA_EN_DLY: Delay between the assertion of HS termination enable and the assertion of HS enable for all data lanes. The range of this field is 0 nanoseconds to 510 nanoseconds in increments of 2 nanoseconds, with reset value 0x0 indicating 0 nanoseconds. **Note**: Use czclk to increment the counter, hence the actual delay can be as much as 10 nanoseconds larger than the programmed value.

5.1.27 iunit_IUNIT_AFE_RCOMP_CONTROL_type (IUNIT_AFE_RCOMP_CONTROL)—Offset E0h

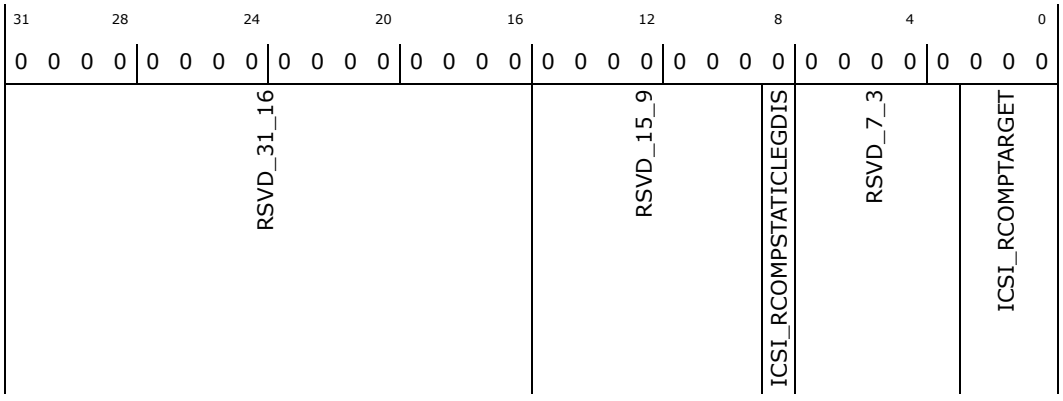
AFE RCOMP control

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + E0h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD_31_16:** Reserved
15:9	0x0 RW	**RSVD_15_9:** Reserved
8	0x0 RW	**ICSI_RCOMPSTATICLEGDIS:** ICSI_RCOMPSTATICLEGDIS: Disable RCOMP static leg in AFE
7:3	0x0 RW	**RSVD_7_3:** Reserved
2:0	0x0 RW	**ICSI_RCOMPTARGET:** ICSI_RCOMPTARGET: RCOMP target level range is 90 Ohms or 100 Ohms differential impedance. 000b = 50 Ohms; 001b = 45 Ohms; other values = reserved

5.1.28 iunit_IUNIT_CSI_CONTROL_type (IUNIT_CSI_CONTROL)—Offset E8h

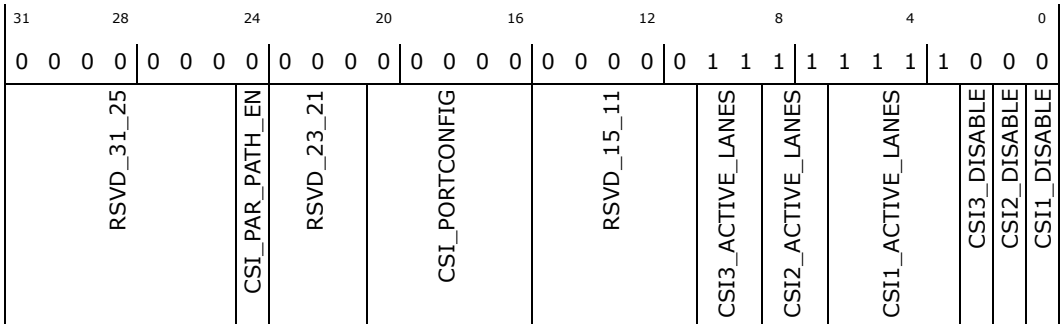
Control Register for MIPI*-CSI

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + E8h

Default: 000007F8h



Bit Range	Default and Access	Field Name (ID): Description
31:25	0x0 RW	**RSVD_31_25:** Reserved
24	0x0 RW	**CSI_PAR_PATH_EN:** PAR_PATH_EN: Selection between Arasan DPHY and VIED DPHY; 0b = Arasan DPHY supporting up to 1.0Gbps (default), 1b = VIED DPHY supporting up to 1.5Gbps
23:21	0x0 RW	**RSVD_23_21:** Reserved
20:16	0x0 RW	**CSI_PORTCONFIG:** CSI_PORTCONFIG: Used to enable the CSI data lanes to CSI ports if FB_csi_portconfig_override fuse is set. This field is ignored if FB_csi_portconfig_override fuse is clear.

Bit Range	Default and Access	Field Name (ID): Description
15:11	0x0 RW	**RSVD_15_11:** Reserved
10:9	0x3 RW	**CSI3_ACTIVE_LANES:** Used to determine which of the lanes that are enabled by the FB_csi_portconfig fuses or the CSI_PORTCONFIG field, are currently being used on the MIPI*-CSI-3 interface. 1=active, 0=inactive.
8:7	0x3 RW	**CSI2_ACTIVE_LANES:** Used to determine which of the lanes that are enabled by the FB_csi_portconfig fuses or the CSI_PORTCONFIG field, are currently being used on the MIPI*-CSI-2 interface. 1=active, 0=inactive.
6:3	0xf RW	**CSI1_ACTIVE_LANES:** Used to determine which of the lanes that are enabled by the FB_csi_portconfig fuses or the CSI_PORTCONFIG field, are currently being used on the MIPI*-CSI-1 interface. 1=active, 0=inactive.
2	0x0 RW	**CSI3_DISABLE:** 1 = Disable MIPI*-CSI-3 interface. 0 = Enable MIPI*-CSI-3 interface if FB_csi_portdisable[2] fuse is cleared
1	0x0 RW	**CSI2_DISABLE:** 1 = Disable MIPI*-CSI-2 interface. 0 = Enable MIPI*-CSI-2 interface if FB_csi_portdisable[1] fuse is cleared
0	0x0 RW	**CSI1_DISABLE:** 1 = Disable MIPI*-CSI-1 interface. 0 = Enable MIPI*-CSI-1 interface if FB_csi_portdisable[0] fuse is cleared

5.1.29 iunit_IUNIT_DEADLINE_CONTROL_type (IUNIT_DEADLINE_CONTROL)—Offset ECh

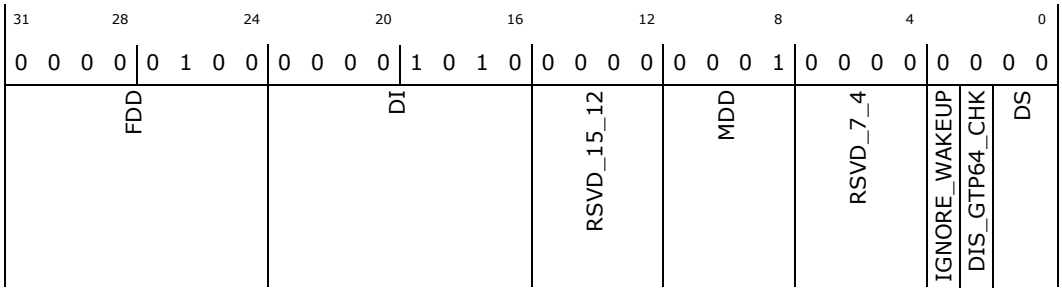
I-unit Deadline Control Register

Access Method

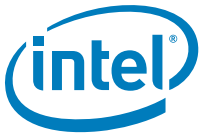
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + ECh

Default: 040A0100h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x4 RW	**FDD:** FIRST_DEADLINE_DELAY: Delay between the rising edge of WAKEUP signal and the fake deadline that will be specified for the first request of that line. Unit in 250 nanoseconds. Reset value of 8'h04 indicates FDD = 1 µsec.



Bit Range	Default and Access	Field Name (ID): Description
23:16	0xa RW	**DI:** DEADLINE_INCREMENT: Difference in deadline times between adjacent requests. If the current request is for 32B, the next deadline will be DI more than the current deadline. If the current request is for 64B, the next deadline will be 2*DI more than the current deadline. Unit in 1/1024 µsec. Reset value of 8'h0A indicates DI = 9.765625 nanoseconds.
15:12	0x0 RW	**RSVD_15_12:** Reserved
11:8	0x1 RW	**MDD:** MINIMUM_DEADLINE_DELAY: Minimum separation between current Global Timer value and the deadline specified with any request on the PFI interface. Unit is 250 nanoseconds. Reset value of 4'h1 indicates MDD = 250 nanoseconds.
7:4	0x0 RW	**RSVD_7_4:** Reserved
3	0x0 RW	**IGNORE_WAKEUP:** If clear, then after each rising edge of sdram_wakeup, the OCP master interface is stalled until all reads in flight and all FIFOs are empty and then the next deadline is set to GT + FDD. If set, the sdram_wakeup signal from ISP_CSS is ignored.
2	0x0 RW	**DIS_GTP64_CHK:** If clear, then the PFI interface is stalled whenever the next deadline value exceeds GT + 64 µsec. This check is a safety measure to make sure that deadline does not drift too far into the future. If set, this check is not performed.
1:0	0x0 RW	**DS:** DEADLINE_SCHEME: 11b = Reserved; 10b = Reserved; 01b = When WAKEUP is asserted, FDD is added to the current global timer to compute DN. With each request, the deadline sent to System Agent is either DN, or the sum of the global timer and MDD, whichever is larger. After each request is sent, DN is computed by adding DI for each 32Byte request sent to either DN or the sum of the global timer and MDD, whichever is larger. Each clock cycle, DN is checked to make sure it is greater than the current global timer, else it is set to the global timer.; 00b = When WAKEUP is asserted, FDD is added to the current global timer to compute DN. With each request, the deadline sent to System Agent is either DN, or the sum of the global timer and MDD, whichever is larger. After each request is sent, DN is computed by adding DI for each 32Byte request sent to DN. Each cycle, DN is checked to make sure that it is either greater than the current global timer, or is less than the global timer by no more than 64 µsec, else it is set to the global timer minus 64 µsec.

5.1.30 iunit_IUNIT_RCOMP_STATUS_type (IUNIT_RCOMP_STATUS)—Offset F0h

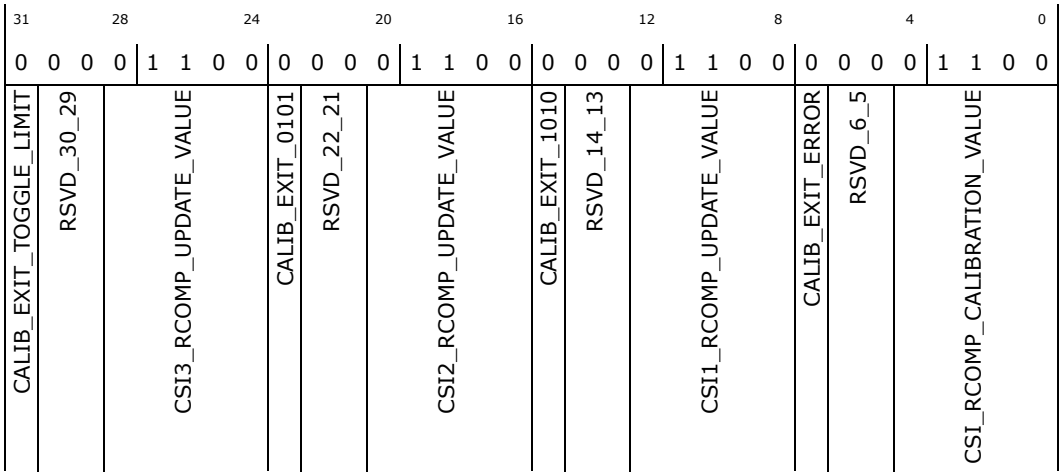
I-unit RCOMP Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + F0h

Default: 0C0C0C0Ch



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RO	**CALIB_EXIT_TOGGLE_LIMIT:** CALIB_EXIT_TOGGLE_LIMIT: If set, indicates that the last calibration cycle exited because the number of toggles matched the value specified by the CSI_HS_ROGGLE_LIMIT_CREG_ENC field of the IUNIT_RCOMP_CONTROL register.
30:29	0x0 RO	**RSVD_30_29:** Reserved
28:24	0xc RO	**CSI3_RCOMP_UPDATE_VALUE:** MIPI*-CSI-3 RCOMP value: Current RCOMP value on MIPI*-CSI-3 port
23	0x0 RO	**CALIB_EXIT_0101:** CALIB_EXIT_0101: If set, indicates that the last calibration cycle exited because the last four states of rcompcountup were 0101
22:21	0x0 RO	**RSVD_22_21:** Reserved
20:16	0xc RO	**CSI2_RCOMP_UPDATE_VALUE:** MIPI*-CSI-2 RCOMP value: Current RCOMP value on MIPI*-CSI-2 port
15	0x0 RO	**CALIB_EXIT_1010:** CALIB_EXIT_1010: If set, indicates that the last calibration cycle exited because the last four states of rcompcountup were 1010
14:13	0x0 RO	**RSVD_14_13:** Reserved
12:8	0xc RO	**CSI1_RCOMP_UPDATE_VALUE:** MIPI*-CSI-1 RCOMP value: Current RCOMP value on MIPI*-CSI-1 port
7	0x0 RO	**CALIB_EXIT_ERROR:** CALIB_EXIT_ERROR: If set, indicates that the last calibration cycle exited due to an error condition.
6:5	0x0 RO	**RSVD_6_5:** Reserved
4:0	0xc RO	**CSI_RCOMP_CALIBRATION_VALUE:** MIPI*-CSI RCOMP value from last calibration cycle

5.1.31 iunit_IUNIT_RCOMP_CONTROL_type (IUNIT_RCOMP_CONTROL)—Offset F4h

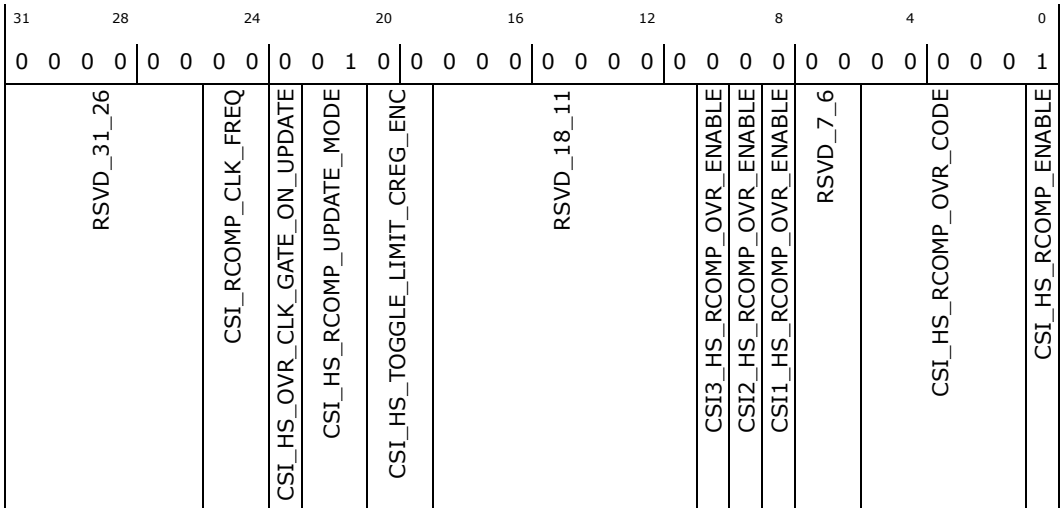
MIPI*-CSI RCOMP Control Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + F4h

Default: 00200001h



Bit Range	Default and Access	Field Name (ID): Description
31:26	0x0 RW	**RSVD_31_26:** Reserved
25:24	0x0 RW	**CSI_RCOMP_CLK_FREQ:** CSI_RCOMP_CLK_FREQ: Bandgap/RCOMP clock frequency. 0h=)20 MHz; 1h=)15 MHz; 2h=)10 MHz; 3h=)reserved. At the start of each RCOMP calibration cycle, the state machine waits for 8 clock cycles before starting to sample the count up/down signal.
23	0x0 RW	**CSI_HS_OVR_CLK_GATE_ON_UPDATE:** CSI_HS_OVR_CLK_GATE_ON_UPDATE: If cleared, the high speed clock going to the digital logic is gated when RCOMP update is happening. The clock is gated for a minimum of 100 nanoseconds. If this bit is set, then the high speed clock is not gated during the update cycle.
22:21	0x1 RW	**CSI_HS_RCOMP_UPDATE_MODE:** CSI_HS_RCOMP_UPDATE_MODE: 00b = RCOMP is updated if the clock lane is in LP11 state. 01b = RCOMP is updated if all the data lanes are in LP11 state. 10b = RCOMP is updated immediately after calibration is completed, or the CSI[1-3]_HS_RCOMP_OVR_ENABLE bits are written to 1 by software. 11b = Reserved.
20:19	0x0 RW	**CSI_HS_TOGGLE_LIMIT_CREG_ENC:** CSI_HS_TOGGLE_LIMIT_CREG_ENC: HS state machine toggle limit. Number of times RCOMP state machine will toggle before exiting. 2'b00: 6 toggles; 2'b01: 4 toggles; 2'b10: 8 toggles; 2'b11: 10 toggles;

Bit Range	Default and Access	Field Name (ID): Description
18:11	0x0 RW	**RSVD_18_11:** Reserved
10	0x0 RW	**CSI3_HS_RCOMP_OVR_ENABLE:** CSI3_HS_RCOMP_OVR_ENABLE: If set, then the CSI_HS_RCOMP_OVRD field is used as the RCOMP value during the update cycle for CSI port 3. If clear, then the output of the RCOMP calibration engine (stored in CSI_RCOMP_CALIBRATION_VALUE field of IUNIT_RCOMP_STATUS register) is used as the RCOMP value during the update cycle for CSI port 3.
9	0x0 RW	**CSI2_HS_RCOMP_OVR_ENABLE:** CSI2_HS_RCOMP_OVR_ENABLE: If set, then the CSI_HS_RCOMP_OVRD field is used as the RCOMP value during the update cycle for CSI port 2. If clear, then the output of the RCOMP calibration engine (stored in CSI_RCOMP_CALIBRATION_VALUE field of IUNIT_RCOMP_STATUS register) is used as the RCOMP value during the update cycle for CSI port 2.
8	0x0 RW	**CSI1_HS_RCOMP_OVR_ENABLE:** CSI1_HS_RCOMP_OVR_ENABLE: If set, then the CSI_HS_RCOMP_OVRD field is used as the RCOMP value during the update cycle for CSI port 1. If clear, then the output of the RCOMP calibration engine (stored in CSI_RCOMP_CALIBRATION_VALUE field of IUNIT_RCOMP_STATUS register) is used as the RCOMP value during the update cycle for CSI port 1.
7:6	0x0 RW	**RSVD_7_6:** Reserved
5:1	0x0 RW	**CSI_HS_RCOMP_OVR_CODE:** CSI_HS_RCOMP_OVR_CODE: Software defined value to use as the RCOMP value for CSI[1-3] ports if the CSI[1-3]_HS_RCOMP_OVR_ENABLE fields are set.
0	0x1 RW	**CSI_HS_RCOMP_ENABLE:** CSI_HS_RCOMP_ENABLE: Enable CSI HS RCOMP. **Note**: This bit does not affect the initial RCOMP at the de-assertion of reset which is controlled by the fuse FB_disable_initial_RCOMP.)

5.1.32 iunit_IUNIT_STATUS_type (IUNIT_STATUS)—Offset F8h

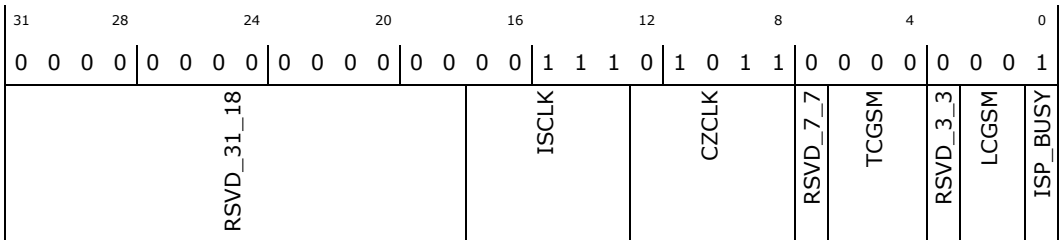
I-unit Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + F8h

Default: 0000EB01h



Bit Range	Default and Access	Field Name (ID): Description
31:18	0x0 RO	**RSVD_31_18:** Reserved
17:13	0x7 RO	**ISCLK:** Reflects the value of cck_isp_isclk_ratio_zcznfwh input pin.
12:8	0xb RO	**CZCLK:** Reflects the value of cck_xxx_czclk_ratio_zcznfwh input pin.
7	0x0 RO	**RSVD_7_7:** Reserved
6:4	0x0 RO	**TCGSM:** ISP trunk clock gating state machine. 0h = RUN_TRUNK_CLK; 1h = STOP_TRUNK_CLK; 2h = WAIT_FOR_RESUME; 3h = START_TRUNK_CLK; 4h = WAIT_FOR_LOCAL_CLK_TO_START. The reset value will be RUN_TRUNK_CLK. If the FB_override_initial_clock_gating fuse is not set, then shortly after reset, the value of this register will automatically change to STOP_TRUNK_CLK.
3	0x0 RO	**RSVD_3_3:** Reserved
2:1	0x0 RO	**LCGSM:** ISP local clock gating state machine. 0h = RUN_LOCAL_CLK; 1h = WAIT_FOR_FIFO_EMPTY; 2h = STOP_LOCAL_CLK. The reset value will be RUN_LOCAL_CLK. If the FB_override_initial_clock_gating fuse is not set, then shortly after reset, the value of this register will automatically change to STOP_LOCAL_CLK.
0	0x1 RO	**ISP_BUSY:** ISP_BUSY: 1 = ISP is busy; 0 = ISP is idle.

5.1.33 iunit_IUNIT_CONTROL_type (IUNIT_CONTROL)—Offset FCh

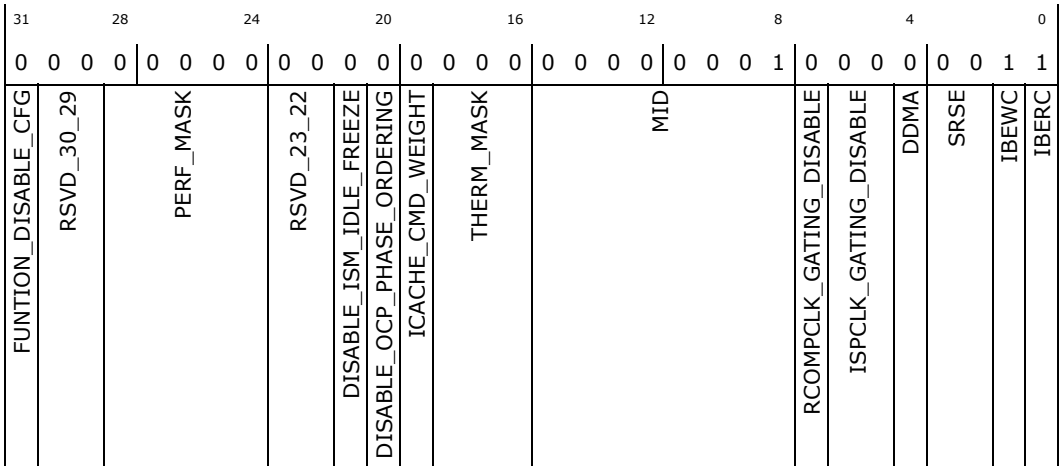
I-unit Control Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + FCh

Default: 00000103h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**FUNTION_DISABLE_CFG:** FUNCTION_DISABLE_INT: When set, both legacy and MSI interrupts are disabled.
30:29	0x0 RW	**RSVD_30_29:** Reserved
28:24	0x0 RW	**PERF_MASK:** PERF_MASK: This field determines the amount of performance throttling applied to ispclk. The value of this field determines how many beat periods of ispclk are killed, where a beat period is defined as 16 ispclk cycles. A 16 cycle period was chosen to make the throttling independent of the actual clock ratio between ispclk and coreclk. **Note**: Clock gating should be enabled when thermal throttling is enabled.
23:22	0x0 RW	**RSVD_23_22:** Reserved
21	0x0 RW	**DISABLE_ISM_IDLE_FREEZE:** DISABLE_ISM_IDLE_FREEZE: When the I-unit receives a RESET_WARN message from P-unit, it will freeze the IOSF primary Idle State Machine (among other things), before sending an OK_TO_RESET message to P-unit. If the DISABLE_ISM_IDLE_FREEZE bit is set, I-unit will not freeze the ISM in the IDLE state as part of this reset sequence.
20	0x0 RW	**DISABLE_OCP_PHASE_ORDERING:** DISABLE_OCP_PHASE_ORDERING: By default the I-unit will follow the OCP phase ordering protocol and wait until a write command is accepted before accepting the write data corresponding to that command. If the DISABLE_OCP_PHASE_ORDERING bit is set, the I-unit wrapper will accept the write data independent of the write command.
19	0x0 RW	**ICACHE_CMD_WEIGHT:** ICACHE_CMD_WEIGHT: 0b = Requests from the OCP master port sending Icache miss traffic will win arbitration over requests from the OCP master port that sends pixel data traffic. 1b = Requests from the two OCP master interfaces will be accepted in a round robin fashion.

Bit Range	Default and Access	Field Name (ID): Description
18:16	0x0 RW	**THERM_MASK:** THERM_MASK: This field determines the amount of thermal throttling applied to ispclk. The value of this field determines how many beat periods of ispclk are killed, where a beat period is defined as 16 ispclk cycles. A 16 cycle period was chosen to make the throttling independent of the actual clock ratio between ispclk and coreclk. 000 = No throttling; 001 = 12.5% throttling; 010 = 25% throttling; 011 = 37.5% throttling; 100 = 50% throttling; 101 = 62.5% throttling; 110 = 75% throttling; 111 = 87.5% throttling;
15:8	0x1 RW	**MID:** MIN_IDLE_DELAY: Minimum wait time after the rising edge of idle, before the clock gating state machine will start the sequence to gate ispclk. Range is 0–130 µsec. Unit is 0.512 µsec. Reset value of 8'h1 indicates MID = 0.512 µsec.
7	0x0 RW	**RCOMPCLK_GATING_DISABLE:** 1 = Disable clock gating for rcompclk. 0 = Enable clock gating for rcompclk. **Note**: All clock gating is disabled by hardware while reset is asserted, regardless of the state of this field.
6:5	0x0 RW	**ISPCLK_GATING_DISABLE:** ISPCLK_GATING_DISABLE: 11 = Disable local clock gating and trunk clock gating for ispclk.; 10 = Enable local clock gating for ispclk, but disable trunk clock gating.; 01 = Reserved; 00 = Enable local clock gating and trunk clock gating for ispclk. **Note**: All clock gating is disabled by hardware while reset is asserted, regardless of the state of this field.
4	0x0 RW	**DDMA:** 1 = Disable DMA. Stop sending any requests on the IB PFI port. 0 = Enable DMA. IB PFI port operates normally.
3:2	0x0 RW	**SRSE:** SOFT_RESET_SEQUENCE_ENABLE: If SRSE=2b00: When an IUNIT_RESET_WARN message is received from P-unit, I-unit will a) stop accepting requests on the IOSF primary interface, b) stop accepting new requests from the OCP master interface, c) wait until read data from all earlier read requests received from the OCP master interface have been returned by SSA, d) wait until SSA reads data for all earlier PFI write requests, and e) wait for all DPHY lanes to enter stop state (LP11), and then f) send an IUNIT_OK_TO_RESET posted message to P-unit. If SRSE=2b01: When an IUNIT_RESET_WARN message is received from P-unit, I-unit will a) stop accepting requests on the IOSF primary interface, b) stop accepting new requests from the OCP master interface, c) wait until read data from all earlier read requests received from the OCP master interface have been returned by SSA, d) wait until SSA reads data for all earlier PFI write requests, and then e) send an IUNIT_OK_TO_RESET posted message to P-unit. If SRSE=2b10: When an IUNIT_RESET_WARN message is received from P-unit, I-unit will wait for all DPHY lanes to enter stop state (LP11), and then send an IUNIT_OK_TO_RESET posted message to P-unit. If SRSE=2b11: When an IUNIT_RESET_WARN message is received from P-unit, I-unit will immediately send an IUINT_OK_TO_RESET posted message to P-unit.
1	0x1 RW	**IBEWC:** IB_ENABLE_WRITE_COMBINING: When set, enables the combining of adjacent 32-byte write requests to the same cache line. When cleared, each 32-byte write request is sent as a separate request on the IB interface.

Bit Range	Default and Access	Field Name (ID): Description
0	0x1 RW	**IBERC:** IB_ENABLE_READ_COMBINING: When set, enables the combining of adjacent 32-byte read requests to the same cache line. When cleared, each 32-byte read request is sent as a separate request on the IB interface.

5.2 Image Signal Processor Memory Mapped I/O Registers

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"reg_gp_sdram_wakeup (gpd_gp_reg_reg_gp_sdram_wakeup)—Offset 0h" on page 1040	00000000h
4–7h	4	"reg_gp_idle (gpd_gp_reg_reg_gp_idle)—Offset 4h" on page 1040	00000000h
8–Bh	4	"reg_gp_irq_req0 (gpd_gp_reg_reg_gp_irq_req0)—Offset 8h" on page 1041	00000000h
C–Fh	4	"reg_gp_irq_req1 (gpd_gp_reg_reg_gp_irq_req1)—Offset Ch" on page 1042	00000000h
10–13h	4	"reg_gp_sp_stream_stat (gpd_gp_reg_reg_gp_sp_stream_stat)—Offset 10h" on page 1042	00222222h
14–17h	4	"reg_gp_sp_stream_stat_b (gpd_gp_reg_reg_gp_sp_stream_stat_b)—Offset 14h" on page 1046	00000000h
18–1Bh	4	"reg_gp_isp_stream_stat (gpd_gp_reg_reg_gp_isp_stream_stat)—Offset 18h" on page 1047	02222222h
1C–1Fh	4	"reg_gp_mod_stream_stat (gpd_gp_reg_reg_gp_mod_stream_stat)—Offset 1Ch" on page 1050	AAAA2222h
20–23h	4	"reg_gp_sp_stream_stat_irq_cond (gpd_gp_reg_reg_gp_sp_stream_stat_irq_cond)—Offset 20h" on page 1053	00000000h
24–27h	4	"reg_gp_sp_stream_stat_b_irq_cond (gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_cond)—Offset 24h" on page 1054	00000000h
28–2Bh	4	"reg_gp_isp_stream_stat_irq_cond (gpd_gp_reg_reg_gp_isp_stream_stat_irq_cond)—Offset 28h" on page 1055	00000000h
2C–2Fh	4	"reg_gp_mod_stream_stat_irq_cond (gpd_gp_reg_reg_gp_mod_stream_stat_irq_cond)—Offset 2Ch" on page 1056	00000000h
30–33h	4	"reg_gp_sp_stream_stat_irq_enable (gpd_gp_reg_reg_gp_sp_stream_stat_irq_enable)—Offset 30h" on page 1057	00000000h

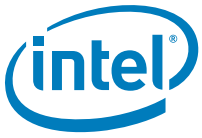


Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
34–37h	4	"reg_gp_sp_stream_stat_b_irq_enable (gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_enable)—Offset 34h" on page 1058	00000000h
38–3Bh	4	"reg_gp_isp_stream_stat_irq_enable (gpd_gp_reg_reg_gp_isp_stream_stat_irq_enable)—Offset 38h" on page 1060	00000000h
3C–3Fh	4	"reg_gp_mod_stream_stat_irq_enable (gpd_gp_reg_reg_gp_mod_stream_stat_irq_enable)—Offset 3Ch" on page 1060	00000000h
40–43h	4	"reg_gp_switch_if (gpd_gp_reg_reg_gp_switch_if)—Offset 40h" on page 1061	00000000h
44–47h	4	"reg_gp_switch_gdc1 (gpd_gp_reg_reg_gp_switch_gdc1)—Offset 44h" on page 1062	00000000h
48–4Bh	4	"reg_gp_switch_gdc2 (gpd_gp_reg_reg_gp_switch_gdc2)—Offset 48h" on page 1063	00000000h
4C–4Fh	4	"reg_gp_srst (gpd_gp_reg_reg_gp_srst)—Offset 4Ch" on page 1064	00000000h
50–53h	4	"reg_gp_slv_reg_srst (gpd_gp_reg_reg_gp_slv_reg_srst)—Offset 50h" on page 1066	00000000h
54–57h	4	"reg_gpd_gp_reg_reg_gp_isel_switch_type (gpd_gp_reg_reg_gp_isel_switch)—Offset 54h" on page 1067	00000000h
100–103h	4	"FifoWriteCmd (gpd_tc_FifoWriteCmd)—Offset 100h" on page 1068	00000000h
400–403h	4	"reg_gpio_doe (gpd_c_gpio_reg_gpio_doe)—Offset 400h" on page 1068	00000000h
404–407h	4	"reg_gpio_do_select (gpd_c_gpio_reg_gpio_do_select)—Offset 404h" on page 1069	00000000h
408–40Bh	4	"reg_gpio_do_0 (gpd_c_gpio_reg_gpio_do_0)—Offset 408h" on page 1070	00000000h
40C–40Fh	4	"reg_gpio_do_1 (gpd_c_gpio_reg_gpio_do_1)—Offset 40Ch" on page 1071	00000000h
410–413h	4	"reg_gpio_do_pwm_cnt_0 (gpd_c_gpio_reg_gpio_do_pwm_cnt_0)—Offset 410h" on page 1072	00000000h
414–417h	4	"reg_gpio_do_pwm_cnt_1 (gpd_c_gpio_reg_gpio_do_pwm_cnt_1)—Offset 414h" on page 1072	00000000h
418–41Bh	4	"reg_gpio_do_pwm_cnt_2 (gpd_c_gpio_reg_gpio_do_pwm_cnt_2)—Offset 418h" on page 1073	00000000h
41C–41Fh	4	"reg_gpio_do_pwm_cnt_3 (gpd_c_gpio_reg_gpio_do_pwm_cnt_3)—Offset 41Ch" on page 1074	00000000h
420–423h	4	"reg_gpio_do_pwm_main_cnt (gpd_c_gpio_reg_gpio_do_pwm_main_cnt)—Offset 420h" on page 1075	00000000h
424–427h	4	"reg_gpio_do_pwm_enable (gpd_c_gpio_reg_gpio_do_pwm_enable)—Offset 424h" on page 1076	00000000h

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
428–42Bh	4	"reg_gpio_di_debouncemethod (gpd_c_gpio_reg_gpio_di_debouncemethod)—Offset 428h" on page 1077	00000000h
42C–42Fh	4	"reg_gpio_di_debounce_cnt0 (gpd_c_gpio_reg_gpio_di_debounce_cnt0)—Offset 42Ch" on page 1078	00000000h
430–433h	4	"reg_gpio_di_debounce_cnt1 (gpd_c_gpio_reg_gpio_di_debounce_cnt1)—Offset 430h" on page 1079	00000000h
434–437h	4	"reg_gpio_di_debounce_cnt2 (gpd_c_gpio_reg_gpio_di_debounce_cnt2)—Offset 434h" on page 1080	00000000h
438–43Bh	4	"reg_gpio_di_debounce_cnt3 (gpd_c_gpio_reg_gpio_di_debounce_cnt3)—Offset 438h" on page 1080	00000000h
43C–43Fh	4	"reg_gpio_di_activelevel (gpd_c_gpio_reg_gpio_di_activelevel)—Offset 43Ch" on page 1081	00000FFFh
440–443h	4	"reg_gpio_di_debouncemethod (gpd_c_gpio_reg_gpio_di_debouncemethod)—Offset 428h" on page 1077	00000FFFh
500–503h	4	"reg_irq_edge (gpd_irq_ctrl_reg_irq_edge)—Offset 500h" on page 1082	00000000h
504–507h	4	"reg_irq_mask (gpd_irq_ctrl_reg_irq_mask)—Offset 504h" on page 1083	00000000h
508–50Bh	4	"reg_irq_status (gpd_irq_ctrl_reg_irq_status)—Offset 508h" on page 1083	00000000h
50C–50Fh	4	"reg_irq_clear (gpd_irq_ctrl_reg_irq_clear)—Offset 50Ch" on page 1085	00000000h
510–513h	4	"reg_irq_enable (gpd_irq_ctrl_reg_irq_enable)—Offset 510h" on page 1086	00000000h
514–517h	4	"reg_irq_level_not_pulse (gpd_irq_ctrl_reg_irq_level_not_pulse)—Offset 514h" on page 1086	00000000h
518–51Bh	4	"reg_irq_str_out_enable (gpd_irq_ctrl_reg_irq_str_out_enable)—Offset 518h" on page 1087	00000000h
600–603h	4	"reg_reset (gpd_gptimer_reg_reset)—Offset 600h" on page 1088	00000000h
604–607h	4	"overall_enable (gpd_gptimer_overall_enable)—Offset 604h" on page 1088	00000000h
608–60Bh	4	"enable_timer_0 (gpd_gptimer_enable_timer_0)—Offset 608h" on page 1089	00000000h
60C–60Fh	4	"enable_timer_1 (gpd_gptimer_enable_timer_1)—Offset 60Ch" on page 1090	00000000h
610–613h	4	"enable_timer_2 (gpd_gptimer_enable_timer_2)—Offset 610h" on page 1090	00000000h

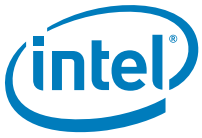


Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
614–617h	4	"enable_timer_3 (gpd_gptimer_enable_timer_3)—Offset 614h" on page 1091	00000000h
618–61Bh	4	"enable_timer_4 (gpd_gptimer_enable_timer_4)—Offset 618h" on page 1092	00000000h
61C–61Fh	4	"enable_timer_5 (gpd_gptimer_enable_timer_5)—Offset 61Ch" on page 1092	00000000h
620–623h	4	"enable_timer_6 (gpd_gptimer_enable_timer_6)—Offset 620h" on page 1093	00000000h
624–627h	4	"enable_timer_7 (gpd_gptimer_enable_timer_7)—Offset 624h" on page 1094	00000000h
628–62Bh	4	"value_timer_0 (gpd_gptimer_value_timer_0)—Offset 628h" on page 1094	00000000h
62C–62Fh	4	"value_timer_1 (gpd_gptimer_value_timer_1)—Offset 62Ch" on page 1095	00000000h
630–633h	4	"value_timer_2 (gpd_gptimer_value_timer_2)—Offset 630h" on page 1096	00000000h
634–637h	4	"value_timer_3 (gpd_gptimer_value_timer_3)—Offset 634h" on page 1096	00000000h
638–63Bh	4	"value_timer_4 (gpd_gptimer_value_timer_4)—Offset 638h" on page 1097	00000000h
63C–63Fh	4	"value_timer_5 (gpd_gptimer_value_timer_5)—Offset 63Ch" on page 1097	00000000h
640–643h	4	"value_timer_6 (gpd_gptimer_value_timer_6)—Offset 640h" on page 1098	00000000h
644–647h	4	"value_timer_7 (gpd_gptimer_value_timer_7)—Offset 644h" on page 1098	00000000h
648–64Bh	4	"count_type_timer_0 (gpd_gptimer_count_type_timer_0)—Offset 648h" on page 1099	00000000h
64C–64Fh	4	"count_type_timer_1 (gpd_gptimer_count_type_timer_1)—Offset 64Ch" on page 1100	00000000h
650–653h	4	"count_type_timer_2 (gpd_gptimer_count_type_timer_2)—Offset 650h" on page 1101	00000000h
654–657h	4	"count_type_timer_3 (gpd_gptimer_count_type_timer_3)—Offset 654h" on page 1101	00000000h
658–65Bh	4	"count_type_timer_4 (gpd_gptimer_count_type_timer_4)—Offset 658h" on page 1102	00000000h
65C–65Fh	4	"count_type_timer_5 (gpd_gptimer_count_type_timer_5)—Offset 65Ch" on page 1103	00000000h
660–663h	4	"count_type_timer_6 (gpd_gptimer_count_type_timer_6)—Offset 660h" on page 1104	00000000h
664–667h	4	"count_type_timer_7 (gpd_gptimer_count_type_timer_7)—Offset 664h" on page 1105	00000000h

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
668–66Bh	4	"signal_select_timer_0 (gpd_gptimer_signal_select_timer_0)—Offset 668h" on page 1106	00000000h
66C–66Fh	4	"signal_select_timer_1 (gpd_gptimer_signal_select_timer_1)—Offset 66Ch" on page 1107	00000000h
670–673h	4	"signal_select_timer_2 (gpd_gptimer_signal_select_timer_2)—Offset 670h" on page 1108	00000000h
674–677h	4	"signal_select_timer_3 (gpd_gptimer_signal_select_timer_3)—Offset 674h" on page 1108	00000000h
678–67Bh	4	"signal_select_timer_4 (gpd_gptimer_signal_select_timer_4)—Offset 678h" on page 1109	00000000h
67C–67Fh	4	"signal_select_timer_5 (gpd_gptimer_signal_select_timer_5)—Offset 67Ch" on page 1110	00000000h
680–683h	4	"signal_select_timer_6 (gpd_gptimer_signal_select_timer_6)—Offset 680h" on page 1111	00000000h
684–687h	4	"signal_select_timer_7 (gpd_gptimer_signal_select_timer_7)—Offset 684h" on page 1111	00000000h
688–68Bh	4	"irq_trigger_value_0 (gpd_gptimer_irq_trigger_value_0)—Offset 688h" on page 1112	00000000h
68C–68Fh	4	"irq_trigger_value_1 (gpd_gptimer_irq_trigger_value_1)—Offset 68Ch" on page 1113	00000000h
690–693h	4	"irq_timer_select_0 (gpd_gptimer_irq_timer_select_0)—Offset 690h" on page 1114	00000000h
694–697h	4	"irq_timer_select_1 (gpd_gptimer_irq_timer_select_1)—Offset 694h" on page 1114	00000000h
698–69Bh	4	"irq_enable_0 (gpd_gptimer_irq_enable_0)—Offset 698h" on page 1115	00000000h
69C–69Fh	4	"irq_enable_1 (gpd_gptimer_irq_enable_1)—Offset 69Ch" on page 1116	00000000h
10000–10003h	4	"scalar_processor_2400_processor processor status and control register (scp_stat_and_ctrl)—Offset 10000h" on page 1116	000000A0h
10004–10007h	4	"scalar_processor_2400_processor processor base address register (scp_base_address)—Offset 10004h" on page 1118	00000000h
10008–1000Bh	4	"Reserved (scp_unused_2)—Offset 10008h" on page 1119	00000000h
10010–10013h	4	"scalar_processor_2400_processor processor base address for segment 0 of master interface xmem_master_int (scp_base_addr_seg_0_MI_xmem_master_int)—Offset 10010h" on page 1119	00000000h
10014–10017h	4	"scalar_processor_2400_processor processor base address for segment 0 of master interface config_ilm_conf_ilm_master (scp_base_addr_seg_0_MI_config_ilm_conf_ilm_master)—Offset 10014h" on page 1120	00000000h
10018–1001Bh	4	"Reserved (scp_unused_6)—Offset 10018h" on page 1121	00000000h
1001C–1001Fh	4	"Reserved (scp_unused_7)—Offset 1001Ch" on page 1122	00000000h

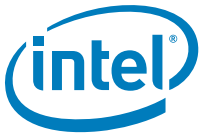


Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
10024–10027h	4	"scalar_processor_2400_processor processor debug program counter (scp_debug_pc)—Offset 10024h" on page 1122	00000000h
10028–1002Bh	4	"scalar_processor_2400_processor processor stalling flags (scp_stall_stat_fifo_loc_mt_am_inst_0_op0)—Offset 10028h" on page 1123	00000000h
1002C–1002Fh	4	"Reserved (scp_unused_11)—Offset 1002Ch" on page 1125	00000000h
10030–10033h	4	"scalar_processor_2400_processor processor program memory slave access (scp_pmem_slave_access)—Offset 10030h" on page 1125	00000000h
20000–20003h	4	"isp2401_mamoiada_processor processor status and control register (isp_stat_and_ctrl)—Offset 20000h" on page 1126	000000A0h
20004–20007h	4	"isp2401_mamoiada_processor processor base address register (isp_base_address)—Offset 20004h" on page 1128	00000000h
20008–2000Bh	4	"Reserved (isp_unused_2)—Offset 20008h" on page 1129	00000000h
20010–20013h	4	"isp2401_mamoiada_processor processor base address for segment 0 of master interface base_config_mem_master (isp_base_addr_seg_0_MI_base_config_mem_master)—Offset 20010h" on page 1129	00000000h
20014–20017h	4	"Reserved (isp_unused_5)—Offset 20014h" on page 1130	00000000h
2001C–2001Fh	4	"isp2401_mamoiada_processor processor debug program counter (isp_debug_pc)—Offset 2001Ch" on page 1131	00000000h
20020–20023h	4	"isp2401_mamoiada_processor processor stalling flags (isp_stall_stat_base_config_mem_iam_op0)—Offset 20020h" on page 1131	00000000h
20024–20027h	4	"Reserved (isp_unused_9)—Offset 20024h" on page 1133	00000000h
20028–2002Bh	4	"isp2401_mamoiada_processor processor program memory slave access (isp_pmem_slave_access)—Offset 20028h" on page 1134	00000000h
30000–30003h	4	"IF_sw_rst (is_2400_ifmt_ift_prim_IF_sw_rst)—Offset 30000h" on page 1135	00000000h
30004–30007h	4	"IF_start_line (is_2400_ifmt_ift_prim_IF_start_line)—Offset 30004h" on page 1136	00000000h
30008–3000Bh	4	"IF_start_column (is_2400_ifmt_ift_prim_IF_start_column)—Offset 30008h" on page 1137	00000000h
3000C–3000Fh	4	"IF_Cropped_height (is_2400_ifmt_ift_prim_IF_Cropped_height)—Offset 3000Ch" on page 1137	00000000h
30010–30013h	4	"IF_Cropped_width (is_2400_ifmt_ift_prim_IF_Cropped_width)—Offset 30010h" on page 1138	00000000h
30014–30017h	4	"IF_Vert_Decim (is_2400_ifmt_ift_prim_IF_Vert_Decim)—Offset 30014h" on page 1139	00000000h
30018–3001Bh	4	"IF_Horiz_Decim (is_2400_ifmt_ift_prim_IF_Horiz_Decim)—Offset 30018h" on page 1140	00000000h
3001C–3001Fh	4	"IF_Horiz_Deinter (is_2400_ifmt_ift_prim_IF_Horiz_Deinter)—Offset 3001Ch" on page 1141	00000000h

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
30020–30023h	4	"IF_Left_Pad (is_2400_ifmt_ift_prim_IF_Left_Pad)—Offset 30020h" on page 1142	00000000h
30024–30027h	4	"IF_EOF_Offset (is_2400_ifmt_ift_prim_IF_EOF_Offset)—Offset 30024h" on page 1142	00000000h
30028–3002Bh	4	"IF_Start_addr (is_2400_ifmt_ift_prim_IF_Start_addr)—Offset 30028h" on page 1143	00000000h
3002C–3002Fh	4	"IF_End_addr (is_2400_ifmt_ift_prim_IF_End_addr)—Offset 3002Ch" on page 1144	00000000h
30030–30033h	4	"IF_incr (is_2400_ifmt_ift_prim_IF_incr)—Offset 30030h" on page 1144	00000000h
30034–30037h	4	"IF_YUV_420_format (is_2400_ifmt_ift_prim_IF_YUV_420_format)—Offset 30034h" on page 1145	00000000h
30038–3003Bh	4	"IF_Vsynch_active_low (is_2400_ifmt_ift_prim_IF_Vsynch_active_low)—Offset 30038h" on page 1146	00000000h
3003C–3003Fh	4	"IF_Hsynch_active_low (is_2400_ifmt_ift_prim_IF_Hsynch_active_low)—Offset 3003Ch" on page 1146	00000000h
30040–30043h	4	"IF_ReEnable (is_2400_ifmt_ift_prim_IF_ReEnable)—Offset 30040h" on page 1147	00000000h
30044–30047h	4	"IF_block_input (is_2400_ifmt_ift_prim_IF_block_input)—Offset 30044h" on page 1148	00000000h
30048–3004Bh	4	"IF_Vert_Deinter (is_2400_ifmt_ift_prim_IF_Vert_Deinter)—Offset 30048h" on page 1149	00000000h
30100–30103h	4	"IF_FSM_Sync_status (is_2400_ifmt_ift_prim_IF_FSM_Sync_status)—Offset 30100h" on page 1149	00000000h
30104–30107h	4	"FSM_Sync_counter (is_2400_ifmt_ift_prim_FSM_Sync_counter)—Offset 30104h" on page 1150	00000000h
30108–3010Bh	4	"FSM_Crop_status (is_2400_ifmt_ift_prim_FSM_Crop_status)—Offset 30108h" on page 1151	00000000h
3010C–3010Fh	4	"FSM_Crop_line_counter (is_2400_ifmt_ift_prim_FSM_Crop_line_counter)—Offset 3010Ch" on page 1152	00000000h
30110–30113h	4	"FSM_Crop_pixel_counter (is_2400_ifmt_ift_prim_FSM_Crop_pixel_counter)—Offset 30110h" on page 1153	00000000h
30114–30117h	4	"FSM_Deinterl_idx_buffer (is_2400_ifmt_ift_prim_FSM_Deinterl_idx_buffer)—Offset 30114h" on page 1154	00000000h
30118–3011Bh	4	"FSM_Horiz_Decim_cnt (is_2400_ifmt_ift_prim_FSM_Horiz_Decim_cnt)—Offset 30118h" on page 1155	00000000h

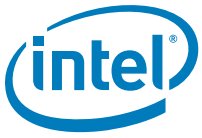


Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3011C–3011Fh	4	"FSM_Vertic_Decim_cnt (is_2400_ifmt_ift_prim_FSM_Vertic_Decim_cnt)—Offset 3011Ch" on page 1156	00000000h
30120–30123h	4	"FSM_Vertic_Block_Decim_cnt (is_2400_ifmt_ift_prim_FSM_Vertic_Block_Decim_cnt)—Offset 30120h" on page 1157	00000000h
30124–30127h	4	"IF_FSM_Padding_status (is_2400_ifmt_ift_prim_IF_FSM_Padding_status)—Offset 30124h" on page 1158	00000000h
30128–3012Bh	4	"IF_FSM_Padding_elem_idx (is_2400_ifmt_ift_prim_IF_FSM_Padding_elem_idx)—Offset 30128h" on page 1159	00000000h
3012C–3012Fh	4	"IF_FSM_Vec_Sup (is_2400_ifmt_ift_prim_IF_FSM_Vec_Sup)—Offset 3012Ch" on page 1160	00000000h
30130–30133h	4	"IF_FSM_Vec_Sup_Buf_full (is_2400_ifmt_ift_prim_IF_FSM_Vec_Sup_Buf_full)—Offset 30130h" on page 1161	00000000h
30134–30137h	4	"IF_FSM_Vec_Sup_rd_accept (is_2400_ifmt_ift_prim_IF_FSM_Vec_Sup_rd_accept)—Offset 30134h" on page 1162	00000001h
30138–3013Bh	4	"IF_Pixel_Fifo_status (is_2400_ifmt_ift_prim_IF_Pixel_Fifo_status)—Offset 30138h" on page 1162	00000001h
30200–30203h	4	"IF_sw_rst (is_2400_ifmt_ift_prim_b_IF_sw_rst)—Offset 30200h" on page 1163	00000000h
30204–30207h	4	"IF_start_line (is_2400_ifmt_ift_prim_b_IF_start_line)—Offset 30204h" on page 1164	00000000h
30208–3020Bh	4	"IF_start_column (is_2400_ifmt_ift_prim_b_IF_start_column)—Offset 30208h" on page 1164	00000000h
3020C–3020Fh	4	"IF_Cropped_height (is_2400_ifmt_ift_prim_b_IF_Cropped_height)—Offset 3020Ch" on page 1165	00000000h
30210–30213h	4	"IF_Cropped_width (is_2400_ifmt_ift_prim_b_IF_Cropped_width)—Offset 30210h" on page 1166	00000000h
30214–30217h	4	"IF_Vert_Decim (is_2400_ifmt_ift_prim_b_IF_Vert_Decim)—Offset 30214h" on page 1167	00000000h
30218–3021Bh	4	"IF_Horiz_Decim (is_2400_ifmt_ift_prim_b_IF_Horiz_Decim)—Offset 30218h" on page 1168	00000000h
3021C–3021Fh	4	"IF_Horiz_Deinter (is_2400_ifmt_ift_prim_b_IF_Horiz_Deinter)—Offset 3021Ch" on page 1168	00000000h
30220–30223h	4	"IF_Left_Pad (is_2400_ifmt_ift_prim_b_IF_Left_Pad)—Offset 30220h" on page 1169	00000000h
30224–30227h	4	"IF_EOF_Offset (is_2400_ifmt_ift_prim_b_IF_EOF_Offset)—Offset 30224h" on page 1170	00000000h

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
30228–3022Bh	4	"IF_Start_addr (is_2400_ifmt_ift_prim_b_IF_Start_addr)—Offset 30228h" on page 1170	00000000h
3022C–3022Fh	4	"IF_End_addr (is_2400_ifmt_ift_prim_b_IF_End_addr)—Offset 3022Ch" on page 1171	00000000h
30230–30233h	4	"IF_incr (is_2400_ifmt_ift_prim_b_IF_incr)—Offset 30230h" on page 1172	00000000h
30234–30237h	4	"IF_YUV_420_format (is_2400_ifmt_ift_prim_b_IF_YUV_420_format)—Offset 30234h" on page 1172	00000000h
30238–3023Bh	4	"IF_Vsynch_active_low (is_2400_ifmt_ift_prim_b_IF_Vsynch_active_low)—Offset 30238h" on page 1173	00000000h
3023C–3023Fh	4	"IF_Hsynch_active_low (is_2400_ifmt_ift_prim_b_IF_Hsynch_active_low)—Offset 3023Ch" on page 1174	00000000h
30240–30243h	4	"IF_ReEnable (is_2400_ifmt_ift_prim_b_IF_ReEnable)—Offset 30240h" on page 1175	00000000h
30244–30247h	4	"IF_block_input (is_2400_ifmt_ift_prim_b_IF_block_input)—Offset 30244h" on page 1176	00000000h
30248–3024Bh	4	"IF_Vert_Deinter (is_2400_ifmt_ift_prim_b_IF_Vert_Deinter)—Offset 30248h" on page 1176	00000000h
30300–30303h	4	"IF_FSM_Sync_status (is_2400_ifmt_ift_prim_b_IF_FSM_Sync_status)—Offset 30300h" on page 1177	00000000h
30304–30307h	4	"FSM_Sync_counter (is_2400_ifmt_ift_prim_b_FSM_Sync_counter)—Offset 30304h" on page 1178	00000000h
30308–3030Bh	4	"FSM_Crop_status (is_2400_ifmt_ift_prim_b_FSM_Crop_status)—Offset 30308h" on page 1179	00000000h
3030C–3030Fh	4	"FSM_Crop_line_counter (is_2400_ifmt_ift_prim_b_FSM_Crop_line_counter)—Offset 3030Ch" on page 1180	00000000h
30310–30313h	4	"FSM_Crop_pixel_counter (is_2400_ifmt_ift_prim_b_FSM_Crop_pixel_counter)—Offset 30310h" on page 1181	00000000h
30314–30317h	4	"FSM_Deinterl_idx_buffer (is_2400_ifmt_ift_prim_b_FSM_Deinterl_idx_buffer)—Offset 30314h" on page 1181	00000000h
30318–3031Bh	4	"FSM_Horiz_Decim_cnt (is_2400_ifmt_ift_prim_b_FSM_Horiz_Decim_cnt)—Offset 30318h" on page 1182	00000000h
3031C–3031Fh	4	"FSM_Vertic_Decim_cnt (is_2400_ifmt_ift_prim_b_FSM_Vertic_Decim_cnt)—Offset 3031Ch" on page 1183	00000000h

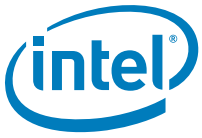


Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
30320–30323h	4	"FSM_Vertic_Block_Decim_cnt (is_2400_ifmt_ift_prim_b_FSM_Vertic_Block_Decim_cnt)—Offset 30320h" on page 1184	00000000h
30324–30327h	4	"IF_FSM_Padding_status (is_2400_ifmt_ift_prim_b_IF_FSM_Padding_status)—Offset 30324h" on page 1185	00000000h
30328–3032Bh	4	"IF_FSM_Padding_elem_idx (is_2400_ifmt_ift_prim_b_IF_FSM_Padding_elem_idx)—Offset 30328h" on page 1186	00000000h
3032C–3032Fh	4	"IF_FSM_Vec_Sup (is_2400_ifmt_ift_prim_b_IF_FSM_Vec_Sup)—Offset 3032Ch" on page 1187	00000000h
30330–30333h	4	"IF_FSM_Vec_Sup_Buf_full (is_2400_ifmt_ift_prim_b_IF_FSM_Vec_Sup_Buf_full)—Offset 30330h" on page 1188	00000000h
30334–30337h	4	"IF_FSM_Vec_Sup_rd_accept (is_2400_ifmt_ift_prim_b_IF_FSM_Vec_Sup_rd_accept)—Offset 30334h" on page 1189	00000001h
30338–3033Bh	4	"IF_Pixel_Fifo_status (is_2400_ifmt_ift_prim_b_IF_Pixel_Fifo_status)—Offset 30338h" on page 1189	00000001h
30400–30403h	4	"IF_sw_rst (is_2400_ifmt_ift_sec_IF_sw_rst)—Offset 30400h" on page 1190	00000000h
30404–30407h	4	"IF_start_line (is_2400_ifmt_ift_sec_IF_start_line)—Offset 30404h" on page 1191	00000000h
30408–3040Bh	4	"IF_start_column (is_2400_ifmt_ift_sec_IF_start_column)—Offset 30408h" on page 1192	00000000h
3040C–3040Fh	4	"IF_Cropped_height (is_2400_ifmt_ift_sec_IF_Cropped_height)—Offset 3040Ch" on page 1192	00000000h
30410–30413h	4	"IF_Cropped_width (is_2400_ifmt_ift_sec_IF_Cropped_width)—Offset 30410h" on page 1193	00000000h
30414–30417h	4	"IF_Vert_Decim (is_2400_ifmt_ift_sec_IF_Vert_Decim)—Offset 30414h" on page 1194	00000000h
30418–3041Bh	4	"IF_Horiz_Decim (is_2400_ifmt_ift_sec_IF_Horiz_Decim)—Offset 30418h" on page 1195	00000000h
3041C–3041Fh	4	"IF_Horiz_Deinter (is_2400_ifmt_ift_sec_IF_Horiz_Deinter)—Offset 3041Ch" on page 1196	00000000h
30420–30423h	4	"IF_Left_Pad (is_2400_ifmt_ift_sec_IF_Left_Pad)—Offset 30420h" on page 1197	00000000h
30424–30427h	4	"IF_EOF_Offset (is_2400_ifmt_ift_sec_IF_EOF_Offset)—Offset 30424h" on page 1197	00000000h
30428–3042Bh	4	"IF_Start_addr (is_2400_ifmt_ift_sec_IF_Start_addr)—Offset 30428h" on page 1198	00000000h
3042C–3042Fh	4	"IF_End_addr (is_2400_ifmt_ift_sec_IF_End_addr)—Offset 3042Ch" on page 1199	00000000h

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
30430–30433h	4	"IF_incr (is_2400_ifmt_ift_sec_IF_incr)—Offset 30430h" on page 1199	00000000h
30434–30437h	4	"IF_YUV_420_format (is_2400_ifmt_ift_sec_IF_YUV_420_format)—Offset 30434h" on page 1200	00000000h
30438–3043Bh	4	"IF_Vsynch_active_low (is_2400_ifmt_ift_sec_IF_Vsynch_active_low)—Offset 30438h" on page 1201	00000000h
3043C–3043Fh	4	"IF_Hsynch_active_low (is_2400_ifmt_ift_sec_IF_Hsynch_active_low)—Offset 3043Ch" on page 1201	00000000h
30440–30443h	4	"IF_ReEnable (is_2400_ifmt_ift_sec_IF_ReEnable)—Offset 30440h" on page 1202	00000000h
30444–30447h	4	"IF_block_input (is_2400_ifmt_ift_sec_IF_block_input)—Offset 30444h" on page 1203	00000000h
30448–3044Bh	4	"IF_Vert_Deinter (is_2400_ifmt_ift_sec_IF_Vert_Deinter)—Offset 30448h" on page 1204	00000000h
30500–30503h	4	"IF_FSM_Sync_status (is_2400_ifmt_ift_sec_IF_FSM_Sync_status)—Offset 30500h" on page 1204	00000000h
30504–30507h	4	"FSM_Sync_counter (is_2400_ifmt_ift_sec_FSM_Sync_counter)—Offset 30504h" on page 1205	00000000h
30508–3050Bh	4	"FSM_Crop_status (is_2400_ifmt_ift_sec_FSM_Crop_status)—Offset 30508h" on page 1206	00000000h
3050C–3050Fh	4	"FSM_Crop_line_counter (is_2400_ifmt_ift_sec_FSM_Crop_line_counter)—Offset 3050Ch" on page 1207	00000000h
30510–30513h	4	"FSM_Crop_pixel_counter (is_2400_ifmt_ift_sec_FSM_Crop_pixel_counter)—Offset 30510h" on page 1208	00000000h
30514–30517h	4	"FSM_Deinterl_idx_buffer (is_2400_ifmt_ift_sec_FSM_Deinterl_idx_buffer)—Offset 30514h" on page 1208	00000000h
30518–3051Bh	4	"FSM_Horiz_Decim_cnt (is_2400_ifmt_ift_sec_FSM_Horiz_Decim_cnt)—Offset 30518h" on page 1209	00000000h
3051C–3051Fh	4	"FSM_Vertic_Decim_cnt (is_2400_ifmt_ift_sec_FSM_Vertic_Decim_cnt)—Offset 3051Ch" on page 1210	00000000h
30520–30523h	4	"FSM_Vertic_Block_Decim_cnt (is_2400_ifmt_ift_sec_FSM_Vertic_Block_Decim_cnt)—Offset 30520h" on page 1211	00000000h
30524–30527h	4	"IF_FSM_Padding_status (is_2400_ifmt_ift_sec_IF_FSM_Padding_status)—Offset 30524h" on page 1212	00000000h

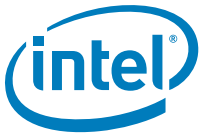


Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
30528–3052Bh	4	"IF_FSM_Padding_elem_idx (is_2400_ifmt_ift_sec_IF_FSM_Padding_elem_idx)—Offset 30528h" on page 1212	00000000h
3052C–3052Fh	4	"IF_FSM_Vec_Sup (is_2400_ifmt_ift_sec_IF_FSM_Vec_Sup)—Offset 3052Ch" on page 1213	00000000h
30530–30533h	4	"IF_FSM_Vec_Sup_Buf_full (is_2400_ifmt_ift_sec_IF_FSM_Vec_Sup_Buf_full)—Offset 30530h" on page 1214	00000000h
30534–30537h	4	"IF_FSM_Vec_Sup_rd_accept (is_2400_ifmt_ift_sec_IF_FSM_Vec_Sup_rd_accept)—Offset 30534h" on page 1215	00000001h
30538–3053Bh	4	"IF_Pixel_Fifo_status (is_2400_ifmt_ift_sec_IF_Pixel_Fifo_status)—Offset 30538h" on page 1216	00000001h
30600–30603h	4	"MemCopy_sw_rst (is_2400_ifmt_mem_cpy_MemCopy_sw_rst)—Offset 30600h" on page 1216	00000000h
30604–30607h	4	"MemCopy_in_endian (is_2400_ifmt_mem_cpy_MemCopy_in_endian)—Offset 30604h" on page 1217	00000000h
30608–3060Bh	4	"MemCopy_out_endian (is_2400_ifmt_mem_cpy_MemCopy_out_endian)—Offset 30608h" on page 1218	00000000h
3060C–3060Fh	4	"MemCopy_bit_swap (is_2400_ifmt_mem_cpy_MemCopy_bit_swap)—Offset 3060Ch" on page 1219	00000000h
30610–30613h	4	"MemCopy_block_synch (is_2400_ifmt_mem_cpy_MemCopy_block_synch)—Offset 30610h" on page 1219	00000000h
30614–30617h	4	"MemCopy_packet_synch (is_2400_ifmt_mem_cpy_MemCopy_packet_synch)—Offset 30614h" on page 1220	00000000h
30618–3061Bh	4	"MemCopy_rd_post_wr_sync (is_2400_ifmt_mem_cpy_MemCopy_rd_post_wr_sync)—Offset 30618h" on page 1221	00000000h
3061C–3061Fh	4	"MemCopy_dual_input (is_2400_ifmt_mem_cpy_MemCopy_dual_input)—Offset 3061Ch" on page 1222	00000000h
30620–30623h	4	"MemCopy_ReEnable (is_2400_ifmt_mem_cpy_MemCopy_ReEnable)—Offset 30620h" on page 1223	00000000h
30700–30703h	4	"MemCopy_token_data (is_2400_ifmt_mem_cpy_MemCopy_token_data)—Offset 30700h" on page 1224	00000000h
30704–30707h	4	"MemCopy_FSM_Sync_status (is_2400_ifmt_mem_cpy_MemCopy_FSM_Sync_status)—Offset 30704h" on page 1224	00000000h

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
30708–3070Bh	4	"MemCopy_FSM_Sync_bytes_cnt (is_2400_ifmt_mem_cpy_MemCopy_FSM_Sync_bytes_cnt)—Offset 30708h" on page 1225	00000000h
3070C–3070Fh	4	"MemCopy_FSM_Sync_token_cnt (is_2400_ifmt_mem_cpy_MemCopy_FSM_Sync_token_cnt)—Offset 3070Ch" on page 1226	00000000h
30710–30713h	4	"MemCopy_FSM_Pack_idx_cnt (is_2400_ifmt_mem_cpy_MemCopy_FSM_Pack_idx_cnt)—Offset 30710h" on page 1227	00000000h
30714–30717h	4	"MemCopy_FSM_Buf_Sup_status (is_2400_ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_status)—Offset 30714h" on page 1228	00000000h
30718–3071Bh	4	"MemCopy_FSM_Buf_Sup_cnt (is_2400_ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_cnt)—Offset 30718h" on page 1229	00000000h
3071C–3071Fh	4	"MemCopy_FSM_CioWr_status (is_2400_ifmt_mem_cpy_MemCopy_FSM_CioWr_status)—Offset 3071Ch" on page 1230	00000004h
30720–30723h	4	"MemCopy_FSM_CioWr_addr (is_2400_ifmt_mem_cpy_MemCopy_FSM_CioWr_addr)—Offset 30720h" on page 1231	00000000h
30800–30803h	4	"IFMT_input_switch__reg0 (is_2400_ifmt_gp_reg_IFMT_input_switch__reg0)—Offset 30800h" on page 1232	00000000h
30804–30807h	4	"IFMT_input_switch__reg1 (is_2400_ifmt_gp_reg_IFMT_input_switch__reg1)—Offset 30804h" on page 1234	00000000h
30808–3080Bh	4	"IFMT_input_switch__reg2 (is_2400_ifmt_gp_reg_IFMT_input_switch__reg2)—Offset 30808h" on page 1235	00000000h
3080C–3080Fh	4	"IFMT_input_switch__reg3 (is_2400_ifmt_gp_reg_IFMT_input_switch__reg3)—Offset 3080Ch" on page 1237	00000000h
30810–30813h	4	"IFMT_input_switch__reg4 (is_2400_ifmt_gp_reg_IFMT_input_switch__reg4)—Offset 30810h" on page 1239	00000000h
30814–30817h	4	"IFMT_input_switch__reg5 (is_2400_ifmt_gp_reg_IFMT_input_switch__reg5)—Offset 30814h" on page 1240	00000000h
30818–3081Bh	4	"IFMT_input_switch__reg6 (is_2400_ifmt_gp_reg_IFMT_input_switch__reg6)—Offset 30818h" on page 1242	00000000h
3081C–3081Fh	4	"IFMT_input_switch__reg7 (is_2400_ifmt_gp_reg_IFMT_input_switch__reg7)—Offset 3081Ch" on page 1244	00000000h

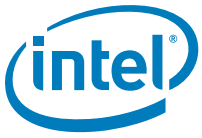


Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
30820–30823h	4	"IFMT_input_switch_fsync_ (is_2400_ifmt_gp_reg_IFMT_input_switch_fsync_)—Offset 30820h" on page 1245	00000000h
30824–30827h	4	"IFMT_srst (is_2400_ifmt_gp_reg_IFMT_srst)—Offset 30824h" on page 1247	00000000h
30828–3082Bh	4	"IFMT_slv_reg_srst (is_2400_ifmt_gp_reg_IFMT_slv_reg_srst)—Offset 30828h" on page 1247	00000000h
3082C–3082Fh	4	"IFMT_input_switch_ch_id_fmt_type (is_2400_ifmt_gp_reg_IFMT_input_switch_ch_id_fmt_type)—Offset 3082Ch" on page 1248	00000000h
30A00–30A03h	4	"IFMT_IRQ_ctrl_edge (is_2400_ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge)—Offset 30A00h" on page 1249	00000000h
30A04–30A07h	4	"IFMT_IRQ_ctrl_mask (is_2400_ifmt_irq_ctrl_IFMT_IRQ_ctrl_mask)—Offset 30A04h" on page 1250	00000000h
30A08–30A0Bh	4	"IFMT_IRQ_ctrl_status (is_2400_ifmt_irq_ctrl_IFMT_IRQ_ctrl_status)—Offset 30A08h" on page 1251	00000000h
30A0C–30A0Fh	4	"IFMT_IRQ_ctrl_clear (is_2400_ifmt_irq_ctrl_IFMT_IRQ_ctrl_clear)—Offset 30A0Ch" on page 1252	00000000h
30A10–30A13h	4	"IFMT_IRQ_ctrl_enable (is_2400_ifmt_irq_ctrl_IFMT_IRQ_ctrl_enable)—Offset 30A10h" on page 1253	00000000h
30A14–30A17h	4	"IFMT_IRQ_ctrl_edge_pulse (is_2400_ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge_pulse)—Offset 30A14h" on page 1254	00000000h
40000–40003h	4	"DMA_FSM_Command (isp_dma_DMA_FSM_Command)—Offset 40000h" on page 1254	00000001h
41000–41003h	4	"DMA_CH0_ConnectionID_sgnzext (isp_dma_DMA_CH0_ConnectionID_sgnzext)—Offset 41000h" on page 1255	00000000h
41004–41007h	4	"DMA_CH1_ConnectionID_sgnzext (isp_dma_DMA_CH1_ConnectionID_sgnzext)—Offset 41004h" on page 1256	00000000h
41008–4100Bh	4	"DMA_CH2_ConnectionID_sgnzext (isp_dma_DMA_CH2_ConnectionID_sgnzext)—Offset 41008h" on page 1257	00000000h
4100C–4100Fh	4	"DMA_CH3_ConnectionID_sgnzext (isp_dma_DMA_CH3_ConnectionID_sgnzext)—Offset 4100Ch" on page 1258	00000000h
41010–41013h	4	"DMA_CH4_ConnectionID_sgnzext (isp_dma_DMA_CH4_ConnectionID_sgnzext)—Offset 41010h" on page 1259	00000000h

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
41014–41017h	4	"DMA_CH5_ConnectionID_sgnzext (isp_dma_DMA_CH5_ConnectionID_sgnzext)—Offset 41014h" on page 1260	00000000h
41018–4101Bh	4	"DMA_CH6_ConnectionID_sgnzext (isp_dma_DMA_CH6_ConnectionID_sgnzext)—Offset 41018h" on page 1261	00000000h
4101C–4101Fh	4	"DMA_CH7_ConnectionID_sgnzext (isp_dma_DMA_CH7_ConnectionID_sgnzext)—Offset 4101Ch" on page 1262	00000000h
41020–41023h	4	"DMA_CH8_ConnectionID_sgnzext (isp_dma_DMA_CH8_ConnectionID_sgnzext)—Offset 41020h" on page 1263	00000000h
41024–41027h	4	"DMA_CH9_ConnectionID_sgnzext (isp_dma_DMA_CH9_ConnectionID_sgnzext)—Offset 41024h" on page 1264	00000000h
41028–4102Bh	4	"DMA_CH10_ConnectionID_sgnzext (isp_dma_DMA_CH10_ConnectionID_sgnzext)—Offset 41028h" on page 1265	00000000h
4102C–4102Fh	4	"DMA_CH11_ConnectionID_sgnzext (isp_dma_DMA_CH11_ConnectionID_sgnzext)—Offset 4102Ch" on page 1266	00000000h
41030–41033h	4	"DMA_CH12_ConnectionID_sgnzext (isp_dma_DMA_CH12_ConnectionID_sgnzext)—Offset 41030h" on page 1267	00000000h
41034–41037h	4	"DMA_CH13_ConnectionID_sgnzext (isp_dma_DMA_CH13_ConnectionID_sgnzext)—Offset 41034h" on page 1268	00000000h
41038–4103Bh	4	"DMA_CH14_ConnectionID_sgnzext (isp_dma_DMA_CH14_ConnectionID_sgnzext)—Offset 41038h" on page 1269	00000000h
4103C–4103Fh	4	"DMA_CH15_ConnectionID_sgnzext (isp_dma_DMA_CH15_ConnectionID_sgnzext)—Offset 4103Ch" on page 1270	00000000h
41040–41043h	4	"DMA_CH16_ConnectionID_sgnzext (isp_dma_DMA_CH16_ConnectionID_sgnzext)—Offset 41040h" on page 1271	00000000h
41044–41047h	4	"DMA_CH17_ConnectionID_sgnzext (isp_dma_DMA_CH17_ConnectionID_sgnzext)—Offset 41044h" on page 1272	00000000h
41048–4104Bh	4	"DMA_CH18_ConnectionID_sgnzext (isp_dma_DMA_CH18_ConnectionID_sgnzext)—Offset 41048h" on page 1273	00000000h
4104C–4104Fh	4	"DMA_CH19_ConnectionID_sgnzext (isp_dma_DMA_CH19_ConnectionID_sgnzext)—Offset 4104Ch" on page 1274	00000000h

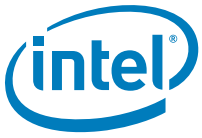


Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
41050–41053h	4	"DMA_CH20_ConnectionID_sgnzext (isp_dma_DMA_CH20_ConnectionID_sgnzext)—Offset 41050h" on page 1275	00000000h
41054–41057h	4	"DMA_CH21_ConnectionID_sgnzext (isp_dma_DMA_CH21_ConnectionID_sgnzext)—Offset 41054h" on page 1276	00000000h
41058–4105Bh	4	"DMA_CH22_ConnectionID_sgnzext (isp_dma_DMA_CH22_ConnectionID_sgnzext)—Offset 41058h" on page 1277	00000000h
4105C–4105Fh	4	"DMA_CH23_ConnectionID_sgnzext (isp_dma_DMA_CH23_ConnectionID_sgnzext)—Offset 4105Ch" on page 1278	00000000h
41060–41063h	4	"DMA_CH24_ConnectionID_sgnzext (isp_dma_DMA_CH24_ConnectionID_sgnzext)—Offset 41060h" on page 1279	00000000h
41064–41067h	4	"DMA_CH25_ConnectionID_sgnzext (isp_dma_DMA_CH25_ConnectionID_sgnzext)—Offset 41064h" on page 1280	00000000h
41068–4106Bh	4	"DMA_CH26_ConnectionID_sgnzext (isp_dma_DMA_CH26_ConnectionID_sgnzext)—Offset 41068h" on page 1281	00000000h
4106C–4106Fh	4	"DMA_CH27_ConnectionID_sgnzext (isp_dma_DMA_CH27_ConnectionID_sgnzext)—Offset 4106Ch" on page 1282	00000000h
41070–41073h	4	"DMA_CH28_ConnectionID_sgnzext (isp_dma_DMA_CH28_ConnectionID_sgnzext)—Offset 41070h" on page 1283	00000000h
41074–41077h	4	"DMA_CH29_ConnectionID_sgnzext (isp_dma_DMA_CH29_ConnectionID_sgnzext)—Offset 41074h" on page 1284	00000000h
41078–4107Bh	4	"DMA_CH30_ConnectionID_sgnzext (isp_dma_DMA_CH30_ConnectionID_sgnzext)—Offset 41078h" on page 1285	00000000h
4107C–4107Fh	4	"DMA_CH31_ConnectionID_sgnzext (isp_dma_DMA_CH31_ConnectionID_sgnzext)—Offset 4107Ch" on page 1286	00000000h
41100–41103h	4	"DMA_CH0_Stride_Addr_Space_A (isp_dma_DMA_CH0_Stride_Addr_Space_A)—Offset 41100h" on page 1287	00000000h
41104–41107h	4	"DMA_CH1_Stride_Addr_Space_A (isp_dma_DMA_CH1_Stride_Addr_Space_A)—Offset 41104h" on page 1288	00000000h
41108–4110Bh	4	"DMA_CH2_Stride_Addr_Space_A (isp_dma_DMA_CH2_Stride_Addr_Space_A)—Offset 41108h" on page 1289	00000000h

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4110C–4110Fh	4	"DMA_CH3_Stride_Addr_Space_A (isp_dma_DMA_CH3_Stride_Addr_Space_A)—Offset 4110Ch" on page 1289	00000000h
41110–41113h	4	"DMA_CH4_Stride_Addr_Space_A (isp_dma_DMA_CH4_Stride_Addr_Space_A)—Offset 41110h" on page 1290	00000000h
41114–41117h	4	"DMA_CH5_Stride_Addr_Space_A (isp_dma_DMA_CH5_Stride_Addr_Space_A)—Offset 41114h" on page 1291	00000000h
41118–4111Bh	4	"DMA_CH6_Stride_Addr_Space_A (isp_dma_DMA_CH6_Stride_Addr_Space_A)—Offset 41118h" on page 1292	00000000h
4111C–4111Fh	4	"DMA_CH7_Stride_Addr_Space_A (isp_dma_DMA_CH7_Stride_Addr_Space_A)—Offset 4111Ch" on page 1292	00000000h
41120–41123h	4	"DMA_CH8_Stride_Addr_Space_A (isp_dma_DMA_CH8_Stride_Addr_Space_A)—Offset 41120h" on page 1293	00000000h
41124–41127h	4	"DMA_CH9_Stride_Addr_Space_A (isp_dma_DMA_CH9_Stride_Addr_Space_A)—Offset 41124h" on page 1294	00000000h
41128–4112Bh	4	"DMA_CH10_Stride_Addr_Space_A (isp_dma_DMA_CH10_Stride_Addr_Space_A)—Offset 41128h" on page 1295	00000000h
4112C–4112Fh	4	"DMA_CH11_Stride_Addr_Space_A (isp_dma_DMA_CH11_Stride_Addr_Space_A)—Offset 4112Ch" on page 1295	00000000h
41130–41133h	4	"DMA_CH12_Stride_Addr_Space_A (isp_dma_DMA_CH12_Stride_Addr_Space_A)—Offset 41130h" on page 1296	00000000h
41134–41137h	4	"DMA_CH13_Stride_Addr_Space_A (isp_dma_DMA_CH13_Stride_Addr_Space_A)—Offset 41134h" on page 1297	00000000h
41138–4113Bh	4	"DMA_CH14_Stride_Addr_Space_A (isp_dma_DMA_CH14_Stride_Addr_Space_A)—Offset 41138h" on page 1298	00000000h
4113C–4113Fh	4	"DMA_CH15_Stride_Addr_Space_A (isp_dma_DMA_CH15_Stride_Addr_Space_A)—Offset 4113Ch" on page 1298	00000000h
41140–41143h	4	"DMA_CH16_Stride_Addr_Space_A (isp_dma_DMA_CH16_Stride_Addr_Space_A)—Offset 41140h" on page 1299	00000000h
41144–41147h	4	"DMA_CH17_Stride_Addr_Space_A (isp_dma_DMA_CH17_Stride_Addr_Space_A)—Offset 41144h" on page 1300	00000000h

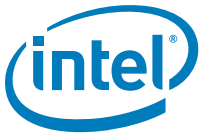


Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
41148–4114Bh	4	"DMA_CH18_Stride_Addr_Space_A (isp_dma_DMA_CH18_Stride_Addr_Space_A)—Offset 41148h" on page 1301	00000000h
4114C–4114Fh	4	"DMA_CH19_Stride_Addr_Space_A (isp_dma_DMA_CH19_Stride_Addr_Space_A)—Offset 4114Ch" on page 1301	00000000h
41150–41153h	4	"DMA_CH20_Stride_Addr_Space_A (isp_dma_DMA_CH20_Stride_Addr_Space_A)—Offset 41150h" on page 1302	00000000h
41154–41157h	4	"DMA_CH21_Stride_Addr_Space_A (isp_dma_DMA_CH21_Stride_Addr_Space_A)—Offset 41154h" on page 1303	00000000h
41200–41203h	4	"DMA_CH0_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH0_Left_Crop_and_Elem_Addr_Space_A)—Offset 41200h" on page 1304	00000000h
41204–41207h	4	"DMA_CH1_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH1_Left_Crop_and_Elem_Addr_Space_A)—Offset 41204h" on page 1305	00000000h
41208–4120Bh	4	"DMA_CH2_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH2_Left_Crop_and_Elem_Addr_Space_A)—Offset 41208h" on page 1306	00000000h
4120C–4120Fh	4	"DMA_CH3_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH3_Left_Crop_and_Elem_Addr_Space_A)—Offset 4120Ch" on page 1307	00000000h
41210–41213h	4	"DMA_CH4_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH4_Left_Crop_and_Elem_Addr_Space_A)—Offset 41210h" on page 1308	00000000h
41214–41217h	4	"DMA_CH5_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH5_Left_Crop_and_Elem_Addr_Space_A)—Offset 41214h" on page 1309	00000000h
41218–4121Bh	4	"DMA_CH6_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH6_Left_Crop_and_Elem_Addr_Space_A)—Offset 41218h" on page 1310	00000000h
4121C–4121Fh	4	"DMA_CH7_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH7_Left_Crop_and_Elem_Addr_Space_A)—Offset 4121Ch" on page 1311	00000000h
41220–41223h	4	"DMA_CH8_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH8_Left_Crop_and_Elem_Addr_Space_A)—Offset 41220h" on page 1312	00000000h
41224–41227h	4	"DMA_CH9_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH9_Left_Crop_and_Elem_Addr_Space_A)—Offset 41224h" on page 1313	00000000h
41228–4122Bh	4	"DMA_CH10_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH10_Left_Crop_and_Elem_Addr_Space_A)—Offset 41228h" on page 1314	00000000h

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4122C–4122Fh	4	"DMA_CH11_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH11_Left_Crop_and_Elem_Addr_Space_A)—Offset 4122Ch" on page 1315	00000000h
41230–41233h	4	"DMA_CH12_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH12_Left_Crop_and_Elem_Addr_Space_A)—Offset 41230h" on page 1316	00000000h
41234–41237h	4	"DMA_CH13_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH13_Left_Crop_and_Elem_Addr_Space_A)—Offset 41234h" on page 1317	00000000h
41238–4123Bh	4	"DMA_CH14_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH14_Left_Crop_and_Elem_Addr_Space_A)—Offset 41238h" on page 1318	00000000h
4123C–4123Fh	4	"DMA_CH15_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH15_Left_Crop_and_Elem_Addr_Space_A)—Offset 4123Ch" on page 1319	00000000h
41240–41243h	4	"DMA_CH16_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH16_Left_Crop_and_Elem_Addr_Space_A)—Offset 41240h" on page 1320	00000000h
41244–41247h	4	"DMA_CH17_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH17_Left_Crop_and_Elem_Addr_Space_A)—Offset 41244h" on page 1321	00000000h
41248–4124Bh	4	"DMA_CH18_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH18_Left_Crop_and_Elem_Addr_Space_A)—Offset 41248h" on page 1322	00000000h
4124C–4124Fh	4	"DMA_CH19_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH19_Left_Crop_and_Elem_Addr_Space_A)—Offset 4124Ch" on page 1323	00000000h
41250–41253h	4	"DMA_CH20_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH20_Left_Crop_and_Elem_Addr_Space_A)—Offset 41250h" on page 1324	00000000h
41254–41257h	4	"DMA_CH21_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH21_Left_Crop_and_Elem_Addr_Space_A)—Offset 41254h" on page 1325	00000000h
41258–4125Bh	4	"DMA_CH22_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH22_Left_Crop_and_Elem_Addr_Space_A)—Offset 41258h" on page 1326	00000000h
4125C–4125Fh	4	"DMA_CH23_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH23_Left_Crop_and_Elem_Addr_Space_A)—Offset 4125Ch" on page 1327	00000000h
41260–41263h	4	"DMA_CH24_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH24_Left_Crop_and_Elem_Addr_Space_A)—Offset 41260h" on page 1328	00000000h
41264–41267h	4	"DMA_CH25_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH25_Left_Crop_and_Elem_Addr_Space_A)—Offset 41264h" on page 1329	00000000h

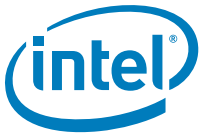


Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
41268–4126Bh	4	"DMA_CH26_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH26_Left_Crop_and_Elem_Addr_Space_A)—Offset 41268h" on page 1330	00000000h
4126C–4126Fh	4	"DMA_CH27_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH27_Left_Crop_and_Elem_Addr_Space_A)—Offset 4126Ch" on page 1331	00000000h
41270–41273h	4	"DMA_CH28_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH28_Left_Crop_and_Elem_Addr_Space_A)—Offset 41270h" on page 1332	00000000h
41274–41277h	4	"DMA_CH29_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH29_Left_Crop_and_Elem_Addr_Space_A)—Offset 41274h" on page 1333	00000000h
41278–4127Bh	4	"DMA_CH30_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH30_Left_Crop_and_Elem_Addr_Space_A)—Offset 41278h" on page 1334	00000000h
4127C–4127Fh	4	"DMA_CH31_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH31_Left_Crop_and_Elem_Addr_Space_A)—Offset 4127Ch" on page 1335	00000000h
412C0–412C3h	4	"DMA_CH22_Stride_Addr_Space_A (isp_dma_DMA_CH22_Stride_Addr_Space_A)—Offset 412C0h" on page 1336	00000000h
412C4–412C7h	4	"DMA_CH23_Stride_Addr_Space_A (isp_dma_DMA_CH23_Stride_Addr_Space_A)—Offset 412C4h" on page 1337	00000000h
412C8–412CBh	4	"DMA_CH24_Stride_Addr_Space_A (isp_dma_DMA_CH24_Stride_Addr_Space_A)—Offset 412C8h" on page 1337	00000000h
412CC–412CFh	4	"DMA_CH25_Stride_Addr_Space_A (isp_dma_DMA_CH25_Stride_Addr_Space_A)—Offset 412CCh" on page 1338	00000000h
412D0–412D3h	4	"DMA_CH26_Stride_Addr_Space_A (isp_dma_DMA_CH26_Stride_Addr_Space_A)—Offset 412D0h" on page 1339	00000000h
412D4–412D7h	4	"DMA_CH27_Stride_Addr_Space_A (isp_dma_DMA_CH27_Stride_Addr_Space_A)—Offset 412D4h" on page 1339	00000000h
412D8–412DBh	4	"DMA_CH28_Stride_Addr_Space_A (isp_dma_DMA_CH28_Stride_Addr_Space_A)—Offset 412D8h" on page 1340	00000000h
412DC–412DFh	4	"DMA_CH29_Stride_Addr_Space_A (isp_dma_DMA_CH29_Stride_Addr_Space_A)—Offset 412DCh" on page 1341	00000000h
412E0–412E3h	4	"DMA_CH30_Stride_Addr_Space_A (isp_dma_DMA_CH30_Stride_Addr_Space_A)—Offset 412E0h" on page 1342	00000000h

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
412E4–412E7h	4	"DMA_CH31_Stride_Addr_Space_A (isp_dma_DMA_CH31_Stride_Addr_Space_A)—Offset 412E4h" on page 1342	00000000h
41300–41303h	4	"DMA_CH0_Block_Width_Addr_Space_A (isp_dma_DMA_CH0_Block_Width_Addr_Space_A)—Offset 41300h" on page 1343	00000000h
41304–41307h	4	"DMA_CH1_Block_Width_Addr_Space_A (isp_dma_DMA_CH1_Block_Width_Addr_Space_A)—Offset 41304h" on page 1344	00000000h
41308–4130Bh	4	"DMA_CH2_Block_Width_Addr_Space_A (isp_dma_DMA_CH2_Block_Width_Addr_Space_A)—Offset 41308h" on page 1345	00000000h
4130C–4130Fh	4	"DMA_CH3_Block_Width_Addr_Space_A (isp_dma_DMA_CH3_Block_Width_Addr_Space_A)—Offset 4130Ch" on page 1346	00000000h
41310–41313h	4	"DMA_CH4_Block_Width_Addr_Space_A (isp_dma_DMA_CH4_Block_Width_Addr_Space_A)—Offset 41310h" on page 1347	00000000h
41314–41317h	4	"DMA_CH5_Block_Width_Addr_Space_A (isp_dma_DMA_CH5_Block_Width_Addr_Space_A)—Offset 41314h" on page 1348	00000000h
41318–4131Bh	4	"DMA_CH6_Block_Width_Addr_Space_A (isp_dma_DMA_CH6_Block_Width_Addr_Space_A)—Offset 41318h" on page 1349	00000000h
4131C–4131Fh	4	"DMA_CH7_Block_Width_Addr_Space_A (isp_dma_DMA_CH7_Block_Width_Addr_Space_A)—Offset 4131Ch" on page 1350	00000000h
41320–41323h	4	"DMA_CH8_Block_Width_Addr_Space_A (isp_dma_DMA_CH8_Block_Width_Addr_Space_A)—Offset 41320h" on page 1351	00000000h
41324–41327h	4	"DMA_CH9_Block_Width_Addr_Space_A (isp_dma_DMA_CH9_Block_Width_Addr_Space_A)—Offset 41324h" on page 1352	00000000h
41328–4132Bh	4	"DMA_CH10_Block_Width_Addr_Space_A (isp_dma_DMA_CH10_Block_Width_Addr_Space_A)—Offset 41328h" on page 1353	00000000h
4132C–4132Fh	4	"DMA_CH11_Block_Width_Addr_Space_A (isp_dma_DMA_CH11_Block_Width_Addr_Space_A)—Offset 4132Ch" on page 1354	00000000h
41330–41333h	4	"DMA_CH12_Block_Width_Addr_Space_A (isp_dma_DMA_CH12_Block_Width_Addr_Space_A)—Offset 41330h" on page 1355	00000000h
41334–41337h	4	"DMA_CH13_Block_Width_Addr_Space_A (isp_dma_DMA_CH13_Block_Width_Addr_Space_A)—Offset 41334h" on page 1356	00000000h

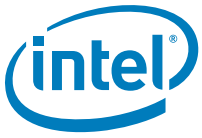


Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
41338–4133Bh	4	"DMA_CH14_Block_Width_Addr_Space_A (isp_dma_DMA_CH14_Block_Width_Addr_Space_A)—Offset 41338h" on page 1357	00000000h
4133C–4133Fh	4	"DMA_CH15_Block_Width_Addr_Space_A (isp_dma_DMA_CH15_Block_Width_Addr_Space_A)—Offset 4133Ch" on page 1358	00000000h
41340–41343h	4	"DMA_CH16_Block_Width_Addr_Space_A (isp_dma_DMA_CH16_Block_Width_Addr_Space_A)—Offset 41340h" on page 1359	00000000h
41344–41347h	4	"DMA_CH17_Block_Width_Addr_Space_A (isp_dma_DMA_CH17_Block_Width_Addr_Space_A)—Offset 41344h" on page 1360	00000000h
41348–4134Bh	4	"DMA_CH18_Block_Width_Addr_Space_A (isp_dma_DMA_CH18_Block_Width_Addr_Space_A)—Offset 41348h" on page 1361	00000000h
4134C–4134Fh	4	"DMA_CH19_Block_Width_Addr_Space_A (isp_dma_DMA_CH19_Block_Width_Addr_Space_A)—Offset 4134Ch" on page 1362	00000000h
41350–41353h	4	"DMA_CH20_Block_Width_Addr_Space_A (isp_dma_DMA_CH20_Block_Width_Addr_Space_A)—Offset 41350h" on page 1363	00000000h
41354–41357h	4	"DMA_CH21_Block_Width_Addr_Space_A (isp_dma_DMA_CH21_Block_Width_Addr_Space_A)—Offset 41354h" on page 1364	00000000h
41358–4135Bh	4	"DMA_CH22_Block_Width_Addr_Space_A (isp_dma_DMA_CH22_Block_Width_Addr_Space_A)—Offset 41358h" on page 1365	00000000h
4135C–4135Fh	4	"DMA_CH23_Block_Width_Addr_Space_A (isp_dma_DMA_CH23_Block_Width_Addr_Space_A)—Offset 4135Ch" on page 1366	00000000h
41360–41363h	4	"DMA_CH24_Block_Width_Addr_Space_A (isp_dma_DMA_CH24_Block_Width_Addr_Space_A)—Offset 41360h" on page 1367	00000000h
41364–41367h	4	"DMA_CH25_Block_Width_Addr_Space_A (isp_dma_DMA_CH25_Block_Width_Addr_Space_A)—Offset 41364h" on page 1368	00000000h
41368–4136Bh	4	"DMA_CH26_Block_Width_Addr_Space_A (isp_dma_DMA_CH26_Block_Width_Addr_Space_A)—Offset 41368h" on page 1369	00000000h
4136C–4136Fh	4	"DMA_CH27_Block_Width_Addr_Space_A (isp_dma_DMA_CH27_Block_Width_Addr_Space_A)—Offset 4136Ch" on page 1370	00000000h
41370–41373h	4	"DMA_CH28_Block_Width_Addr_Space_A (isp_dma_DMA_CH28_Block_Width_Addr_Space_A)—Offset 41370h" on page 1371	00000000h

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
41374–41377h	4	"DMA_CH29_Block_Width_Addr_Space_A (isp_dma_DMA_CH29_Block_Width_Addr_Space_A)—Offset 41374h" on page 1372	00000000h
41378–4137Bh	4	"DMA_CH30_Block_Width_Addr_Space_A (isp_dma_DMA_CH30_Block_Width_Addr_Space_A)—Offset 41378h" on page 1373	00000000h
4137C–4137Fh	4	"DMA_CH31_Block_Width_Addr_Space_A (isp_dma_DMA_CH31_Block_Width_Addr_Space_A)—Offset 4137Ch" on page 1374	00000000h
41400–41403h	4	"DMA_CH0_Stride_Addr_Space_B (isp_dma_DMA_CH0_Stride_Addr_Space_B)—Offset 41400h" on page 1375	00000000h
41404–41407h	4	"DMA_CH1_Stride_Addr_Space_B (isp_dma_DMA_CH1_Stride_Addr_Space_B)—Offset 41404h" on page 1376	00000000h
41408–4140Bh	4	"DMA_CH2_Stride_Addr_Space_B (isp_dma_DMA_CH2_Stride_Addr_Space_B)—Offset 41408h" on page 1377	00000000h
4140C–4140Fh	4	"DMA_CH3_Stride_Addr_Space_B (isp_dma_DMA_CH3_Stride_Addr_Space_B)—Offset 4140Ch" on page 1377	00000000h
41410–41413h	4	"DMA_CH4_Stride_Addr_Space_B (isp_dma_DMA_CH4_Stride_Addr_Space_B)—Offset 41410h" on page 1378	00000000h
41414–41417h	4	"DMA_CH5_Stride_Addr_Space_B (isp_dma_DMA_CH5_Stride_Addr_Space_B)—Offset 41414h" on page 1379	00000000h
41418–4141Bh	4	"DMA_CH6_Stride_Addr_Space_B (isp_dma_DMA_CH6_Stride_Addr_Space_B)—Offset 41418h" on page 1380	00000000h
4141C–4141Fh	4	"DMA_CH7_Stride_Addr_Space_B (isp_dma_DMA_CH7_Stride_Addr_Space_B)—Offset 4141Ch" on page 1380	00000000h
41420–41423h	4	"DMA_CH8_Stride_Addr_Space_B (isp_dma_DMA_CH8_Stride_Addr_Space_B)—Offset 41420h" on page 1381	00000000h
41424–41427h	4	"DMA_CH9_Stride_Addr_Space_B (isp_dma_DMA_CH9_Stride_Addr_Space_B)—Offset 41424h" on page 1382	00000000h
41428–4142Bh	4	"DMA_CH10_Stride_Addr_Space_B (isp_dma_DMA_CH10_Stride_Addr_Space_B)—Offset 41428h" on page 1383	00000000h
4142C–4142Fh	4	"DMA_CH11_Stride_Addr_Space_B (isp_dma_DMA_CH11_Stride_Addr_Space_B)—Offset 4142Ch" on page 1383	00000000h

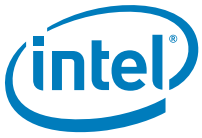


Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
41430–41433h	4	"DMA_CH12_Stride_Addr_Space_B (isp_dma_DMA_CH12_Stride_Addr_Space_B)—Offset 41430h" on page 1384	00000000h
41434–41437h	4	"DMA_CH13_Stride_Addr_Space_B (isp_dma_DMA_CH13_Stride_Addr_Space_B)—Offset 41434h" on page 1385	00000000h
41438–4143Bh	4	"DMA_CH14_Stride_Addr_Space_B (isp_dma_DMA_CH14_Stride_Addr_Space_B)—Offset 41438h" on page 1386	00000000h
4143C–4143Fh	4	"DMA_CH15_Stride_Addr_Space_B (isp_dma_DMA_CH15_Stride_Addr_Space_B)—Offset 4143Ch" on page 1386	00000000h
41440–41443h	4	"DMA_CH16_Stride_Addr_Space_B (isp_dma_DMA_CH16_Stride_Addr_Space_B)—Offset 41440h" on page 1387	00000000h
41444–41447h	4	"DMA_CH17_Stride_Addr_Space_B (isp_dma_DMA_CH17_Stride_Addr_Space_B)—Offset 41444h" on page 1388	00000000h
41448–4144Bh	4	"DMA_CH18_Stride_Addr_Space_B (isp_dma_DMA_CH18_Stride_Addr_Space_B)—Offset 41448h" on page 1389	00000000h
4144C–4144Fh	4	"DMA_CH19_Stride_Addr_Space_B (isp_dma_DMA_CH19_Stride_Addr_Space_B)—Offset 4144Ch" on page 1389	00000000h
41450–41453h	4	"DMA_CH20_Stride_Addr_Space_B (isp_dma_DMA_CH20_Stride_Addr_Space_B)—Offset 41450h" on page 1390	00000000h
41454–41457h	4	"DMA_CH21_Stride_Addr_Space_B (isp_dma_DMA_CH21_Stride_Addr_Space_B)—Offset 41454h" on page 1391	00000000h
41458–4145Bh	4	"DMA_CH22_Stride_Addr_Space_B (isp_dma_DMA_CH22_Stride_Addr_Space_B)—Offset 41458h" on page 1392	00000000h
4145C–4145Fh	4	"DMA_CH23_Stride_Addr_Space_B (isp_dma_DMA_CH23_Stride_Addr_Space_B)—Offset 4145Ch" on page 1392	00000000h
41460–41463h	4	"DMA_CH24_Stride_Addr_Space_B (isp_dma_DMA_CH24_Stride_Addr_Space_B)—Offset 41460h" on page 1393	00000000h
41464–41467h	4	"DMA_CH25_Stride_Addr_Space_B (isp_dma_DMA_CH25_Stride_Addr_Space_B)—Offset 41464h" on page 1394	00000000h
41468–4146Bh	4	"DMA_CH26_Stride_Addr_Space_B (isp_dma_DMA_CH26_Stride_Addr_Space_B)—Offset 41468h" on page 1395	00000000h

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4146C–4146Fh	4	"DMA_CH27_Stride_Addr_Space_B (isp_dma_DMA_CH27_Stride_Addr_Space_B)—Offset 4146Ch" on page 1395	00000000h
41470–41473h	4	"DMA_CH28_Stride_Addr_Space_B (isp_dma_DMA_CH28_Stride_Addr_Space_B)—Offset 41470h" on page 1396	00000000h
41474–41477h	4	"DMA_CH29_Stride_Addr_Space_B (isp_dma_DMA_CH29_Stride_Addr_Space_B)—Offset 41474h" on page 1397	00000000h
41478–4147Bh	4	"DMA_CH30_Stride_Addr_Space_B (isp_dma_DMA_CH30_Stride_Addr_Space_B)—Offset 41478h" on page 1398	00000000h
4147C–4147Fh	4	"DMA_CH31_Stride_Addr_Space_B (isp_dma_DMA_CH31_Stride_Addr_Space_B)—Offset 4147Ch" on page 1398	00000000h
41500–41503h	4	"DMA_CH0_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH0_Left_Crop_and_Elem_Addr_Space_B)—Offset 41500h" on page 1399	00000000h
41504–41507h	4	"DMA_CH1_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH1_Left_Crop_and_Elem_Addr_Space_B)—Offset 41504h" on page 1400	00000000h
41508–4150Bh	4	"DMA_CH2_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH2_Left_Crop_and_Elem_Addr_Space_B)—Offset 41508h" on page 1401	00000000h
4150C–4150Fh	4	"DMA_CH3_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH3_Left_Crop_and_Elem_Addr_Space_B)—Offset 4150Ch" on page 1402	00000000h
41510–41513h	4	"DMA_CH4_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH4_Left_Crop_and_Elem_Addr_Space_B)—Offset 41510h" on page 1403	00000000h
41514–41517h	4	"DMA_CH5_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH5_Left_Crop_and_Elem_Addr_Space_B)—Offset 41514h" on page 1404	00000000h
41518–4151Bh	4	"DMA_CH6_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH6_Left_Crop_and_Elem_Addr_Space_B)—Offset 41518h" on page 1405	00000000h
4151C–4151Fh	4	"DMA_CH7_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH7_Left_Crop_and_Elem_Addr_Space_B)—Offset 4151Ch" on page 1406	00000000h
41520–41523h	4	"DMA_CH8_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH8_Left_Crop_and_Elem_Addr_Space_B)—Offset 41520h" on page 1407	00000000h
41524–41527h	4	"DMA_CH9_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH9_Left_Crop_and_Elem_Addr_Space_B)—Offset 41524h" on page 1408	00000000h

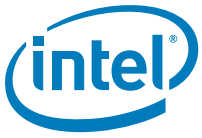


Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
41528–4152Bh	4	"DMA_CH10_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH10_Left_Crop_and_Elem_Addr_Space_B)—Offset 41528h" on page 1409	00000000h
4152C–4152Fh	4	"DMA_CH11_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH11_Left_Crop_and_Elem_Addr_Space_B)—Offset 4152Ch" on page 1410	00000000h
41530–41533h	4	"DMA_CH12_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH12_Left_Crop_and_Elem_Addr_Space_B)—Offset 41530h" on page 1411	00000000h
41534–41537h	4	"DMA_CH13_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH13_Left_Crop_and_Elem_Addr_Space_B)—Offset 41534h" on page 1412	00000000h
41538–4153Bh	4	"DMA_CH14_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH14_Left_Crop_and_Elem_Addr_Space_B)—Offset 41538h" on page 1413	00000000h
4153C–4153Fh	4	"DMA_CH15_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH15_Left_Crop_and_Elem_Addr_Space_B)—Offset 4153Ch" on page 1414	00000000h
41540–41543h	4	"DMA_CH16_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH16_Left_Crop_and_Elem_Addr_Space_B)—Offset 41540h" on page 1415	00000000h
41544–41547h	4	"DMA_CH17_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH17_Left_Crop_and_Elem_Addr_Space_B)—Offset 41544h" on page 1416	00000000h
41548–4154Bh	4	"DMA_CH18_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH18_Left_Crop_and_Elem_Addr_Space_B)—Offset 41548h" on page 1417	00000000h
4154C–4154Fh	4	"DMA_CH19_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH19_Left_Crop_and_Elem_Addr_Space_B)—Offset 4154Ch" on page 1418	00000000h
41550–41553h	4	"DMA_CH20_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH20_Left_Crop_and_Elem_Addr_Space_B)—Offset 41550h" on page 1419	00000000h
41554–41557h	4	"DMA_CH21_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH21_Left_Crop_and_Elem_Addr_Space_B)—Offset 41554h" on page 1420	00000000h
41558–4155Bh	4	"DMA_CH22_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH22_Left_Crop_and_Elem_Addr_Space_B)—Offset 41558h" on page 1421	00000000h
4155C–4155Fh	4	"DMA_CH23_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH23_Left_Crop_and_Elem_Addr_Space_B)—Offset 4155Ch" on page 1422	00000000h
41560–41563h	4	"DMA_CH24_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH24_Left_Crop_and_Elem_Addr_Space_B)—Offset 41560h" on page 1423	00000000h

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
41564–41567h	4	"DMA_CH25_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH25_Left_Crop_and_Elem_Addr_Space_B)—Offset 41564h" on page 1424	00000000h
41568–4156Bh	4	"DMA_CH26_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH26_Left_Crop_and_Elem_Addr_Space_B)—Offset 41568h" on page 1425	00000000h
4156C–4156Fh	4	"DMA_CH27_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH27_Left_Crop_and_Elem_Addr_Space_B)—Offset 4156Ch" on page 1426	00000000h
41570–41573h	4	"DMA_CH28_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH28_Left_Crop_and_Elem_Addr_Space_B)—Offset 41570h" on page 1427	00000000h
41574–41577h	4	"DMA_CH29_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH29_Left_Crop_and_Elem_Addr_Space_B)—Offset 41574h" on page 1428	00000000h
41578–4157Bh	4	"DMA_CH30_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH30_Left_Crop_and_Elem_Addr_Space_B)—Offset 41578h" on page 1429	00000000h
4157C–4157Fh	4	"DMA_CH31_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH31_Left_Crop_and_Elem_Addr_Space_B)—Offset 4157Ch" on page 1430	00000000h
41600–41603h	4	"DMA_CH0_Block_Width_Addr_Space_B (isp_dma_DMA_CH0_Block_Width_Addr_Space_B)—Offset 41600h" on page 1431	00000000h
41604–41607h	4	"DMA_CH1_Block_Width_Addr_Space_B (isp_dma_DMA_CH1_Block_Width_Addr_Space_B)—Offset 41604h" on page 1432	00000000h
41608–4160Bh	4	"DMA_CH2_Block_Width_Addr_Space_B (isp_dma_DMA_CH2_Block_Width_Addr_Space_B)—Offset 41608h" on page 1433	00000000h
4160C–4160Fh	4	"DMA_CH3_Block_Width_Addr_Space_B (isp_dma_DMA_CH3_Block_Width_Addr_Space_B)—Offset 4160Ch" on page 1434	00000000h
41610–41613h	4	"DMA_CH4_Block_Width_Addr_Space_B (isp_dma_DMA_CH4_Block_Width_Addr_Space_B)—Offset 41610h" on page 1435	00000000h
41614–41617h	4	"DMA_CH5_Block_Width_Addr_Space_B (isp_dma_DMA_CH5_Block_Width_Addr_Space_B)—Offset 41614h" on page 1436	00000000h
41618–4161Bh	4	"DMA_CH6_Block_Width_Addr_Space_B (isp_dma_DMA_CH6_Block_Width_Addr_Space_B)—Offset 41618h" on page 1437	00000000h
4161C–4161Fh	4	"DMA_CH7_Block_Width_Addr_Space_B (isp_dma_DMA_CH7_Block_Width_Addr_Space_B)—Offset 4161Ch" on page 1438	00000000h

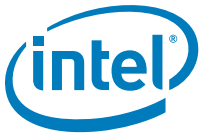


Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
41620–41623h	4	"DMA_CH8_Block_Width_Addr_Space_B (isp_dma_DMA_CH8_Block_Width_Addr_Space_B)—Offset 41620h" on page 1439	00000000h
41624–41627h	4	"DMA_CH9_Block_Width_Addr_Space_B (isp_dma_DMA_CH9_Block_Width_Addr_Space_B)—Offset 41624h" on page 1440	00000000h
41628–4162Bh	4	"DMA_CH10_Block_Width_Addr_Space_B (isp_dma_DMA_CH10_Block_Width_Addr_Space_B)—Offset 41628h" on page 1441	00000000h
4162C–4162Fh	4	"DMA_CH11_Block_Width_Addr_Space_B (isp_dma_DMA_CH11_Block_Width_Addr_Space_B)—Offset 4162Ch" on page 1442	00000000h
41630–41633h	4	"DMA_CH12_Block_Width_Addr_Space_B (isp_dma_DMA_CH12_Block_Width_Addr_Space_B)—Offset 41630h" on page 1443	00000000h
41634–41637h	4	"DMA_CH13_Block_Width_Addr_Space_B (isp_dma_DMA_CH13_Block_Width_Addr_Space_B)—Offset 41634h" on page 1444	00000000h
41638–4163Bh	4	"DMA_CH14_Block_Width_Addr_Space_B (isp_dma_DMA_CH14_Block_Width_Addr_Space_B)—Offset 41638h" on page 1445	00000000h
4163C–4163Fh	4	"DMA_CH15_Block_Width_Addr_Space_B (isp_dma_DMA_CH15_Block_Width_Addr_Space_B)—Offset 4163Ch" on page 1446	00000000h
41640–41643h	4	"DMA_CH16_Block_Width_Addr_Space_B (isp_dma_DMA_CH16_Block_Width_Addr_Space_B)—Offset 41640h" on page 1447	00000000h
41644–41647h	4	"DMA_CH17_Block_Width_Addr_Space_B (isp_dma_DMA_CH17_Block_Width_Addr_Space_B)—Offset 41644h" on page 1448	00000000h
41648–4164Bh	4	"DMA_CH18_Block_Width_Addr_Space_B (isp_dma_DMA_CH18_Block_Width_Addr_Space_B)—Offset 41648h" on page 1449	00000000h
4164C–4164Fh	4	"DMA_CH19_Block_Width_Addr_Space_B (isp_dma_DMA_CH19_Block_Width_Addr_Space_B)—Offset 4164Ch" on page 1450	00000000h
41650–41653h	4	"DMA_CH20_Block_Width_Addr_Space_B (isp_dma_DMA_CH20_Block_Width_Addr_Space_B)—Offset 41650h" on page 1451	00000000h
41654–41657h	4	"DMA_CH21_Block_Width_Addr_Space_B (isp_dma_DMA_CH21_Block_Width_Addr_Space_B)—Offset 41654h" on page 1452	00000000h
41658–4165Bh	4	"DMA_CH22_Block_Width_Addr_Space_B (isp_dma_DMA_CH22_Block_Width_Addr_Space_B)—Offset 41658h" on page 1453	00000000h

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4165C–4165Fh	4	"DMA_CH23_Block_Width_Addr_Space_B (isp_dma_DMA_CH23_Block_Width_Addr_Space_B)—Offset 4165Ch" on page 1454	00000000h
41660–41663h	4	"DMA_CH24_Block_Width_Addr_Space_B (isp_dma_DMA_CH24_Block_Width_Addr_Space_B)—Offset 41660h" on page 1455	00000000h
41664–41667h	4	"DMA_CH25_Block_Width_Addr_Space_B (isp_dma_DMA_CH25_Block_Width_Addr_Space_B)—Offset 41664h" on page 1456	00000000h
41668–4166Bh	4	"DMA_CH26_Block_Width_Addr_Space_B (isp_dma_DMA_CH26_Block_Width_Addr_Space_B)—Offset 41668h" on page 1457	00000000h
4166C–4166Fh	4	"DMA_CH27_Block_Width_Addr_Space_B (isp_dma_DMA_CH27_Block_Width_Addr_Space_B)—Offset 4166Ch" on page 1458	00000000h
41670–41673h	4	"DMA_CH28_Block_Width_Addr_Space_B (isp_dma_DMA_CH28_Block_Width_Addr_Space_B)—Offset 41670h" on page 1459	00000000h
41674–41677h	4	"DMA_CH29_Block_Width_Addr_Space_B (isp_dma_DMA_CH29_Block_Width_Addr_Space_B)—Offset 41674h" on page 1460	00000000h
41678–4167Bh	4	"DMA_CH30_Block_Width_Addr_Space_B (isp_dma_DMA_CH30_Block_Width_Addr_Space_B)—Offset 41678h" on page 1461	00000000h
4167C–4167Fh	4	"DMA_CH31_Block_Width_Addr_Space_B (isp_dma_DMA_CH31_Block_Width_Addr_Space_B)—Offset 4167Ch" on page 1462	00000000h
41700–41703h	4	"DMA_CH0_Block_Height (isp_dma_DMA_CH0_Block_Height)—Offset 41700h" on page 1463	00000000h
41704–41707h	4	"DMA_CH1_Block_Height (isp_dma_DMA_CH1_Block_Height)—Offset 41704h" on page 1464	00000000h
41708–4170Bh	4	"DMA_CH2_Block_Height (isp_dma_DMA_CH2_Block_Height)—Offset 41708h" on page 1465	00000000h
4170C–4170Fh	4	"DMA_CH3_Block_Height (isp_dma_DMA_CH3_Block_Height)—Offset 4170Ch" on page 1465	00000000h
41710–41713h	4	"DMA_CH4_Block_Height (isp_dma_DMA_CH4_Block_Height)—Offset 41710h" on page 1466	00000000h
41714–41717h	4	"DMA_CH5_Block_Height (isp_dma_DMA_CH5_Block_Height)—Offset 41714h" on page 1467	00000000h
41718–4171Bh	4	"DMA_CH6_Block_Height (isp_dma_DMA_CH6_Block_Height)—Offset 41718h" on page 1468	00000000h
4171C–4171Fh	4	"DMA_CH7_Block_Height (isp_dma_DMA_CH7_Block_Height)—Offset 4171Ch" on page 1468	00000000h
41720–41723h	4	"DMA_CH8_Block_Height (isp_dma_DMA_CH8_Block_Height)—Offset 41720h" on page 1469	00000000h

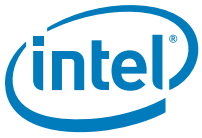


Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
41724–41727h	4	"DMA_CH9_Block_Height (isp_dma_DMA_CH9_Block_Height)—Offset 41724h" on page 1470	00000000h
41728–4172Bh	4	"DMA_CH10_Block_Height (isp_dma_DMA_CH10_Block_Height)—Offset 41728h" on page 1471	00000000h
4172C–4172Fh	4	"DMA_CH11_Block_Height (isp_dma_DMA_CH11_Block_Height)—Offset 4172Ch" on page 1471	00000000h
41730–41733h	4	"DMA_CH12_Block_Height (isp_dma_DMA_CH12_Block_Height)—Offset 41730h" on page 1472	00000000h
41734–41737h	4	"DMA_CH13_Block_Height (isp_dma_DMA_CH13_Block_Height)—Offset 41734h" on page 1473	00000000h
41738–4173Bh	4	"DMA_CH14_Block_Height (isp_dma_DMA_CH14_Block_Height)—Offset 41738h" on page 1474	00000000h
4173C–4173Fh	4	"DMA_CH15_Block_Height (isp_dma_DMA_CH15_Block_Height)—Offset 4173Ch" on page 1475	00000000h
41740–41743h	4	"DMA_CH16_Block_Height (isp_dma_DMA_CH16_Block_Height)—Offset 41740h" on page 1476	00000000h
41744–41747h	4	"DMA_CH17_Block_Height (isp_dma_DMA_CH17_Block_Height)—Offset 41744h" on page 1477	00000000h
41748–4174Bh	4	"DMA_CH18_Block_Height (isp_dma_DMA_CH18_Block_Height)—Offset 41748h" on page 1478	00000000h
4174C–4174Fh	4	"DMA_CH19_Block_Height (isp_dma_DMA_CH19_Block_Height)—Offset 4174Ch" on page 1479	00000000h
41750–41753h	4	"DMA_CH20_Block_Height (isp_dma_DMA_CH20_Block_Height)—Offset 41750h" on page 1480	00000000h
41754–41757h	4	"DMA_CH21_Block_Height (isp_dma_DMA_CH21_Block_Height)—Offset 41754h" on page 1481	00000000h
41758–4175Bh	4	"DMA_CH22_Block_Height (isp_dma_DMA_CH22_Block_Height)—Offset 41758h" on page 1482	00000000h
4175C–4175Fh	4	"DMA_CH23_Block_Height (isp_dma_DMA_CH23_Block_Height)—Offset 4175Ch" on page 1483	00000000h
41760–41763h	4	"DMA_CH24_Block_Height (isp_dma_DMA_CH24_Block_Height)—Offset 41760h" on page 1484	00000000h
41764–41767h	4	"DMA_CH25_Block_Height (isp_dma_DMA_CH25_Block_Height)—Offset 41764h" on page 1485	00000000h
41768–4176Bh	4	"DMA_CH26_Block_Height (isp_dma_DMA_CH26_Block_Height)—Offset 41768h" on page 1486	00000000h
4176C–4176Fh	4	"DMA_CH27_Block_Height (isp_dma_DMA_CH27_Block_Height)—Offset 4176Ch" on page 1487	00000000h
41770–41773h	4	"DMA_CH28_Block_Height (isp_dma_DMA_CH28_Block_Height)—Offset 41770h" on page 1488	00000000h
41774–41777h	4	"DMA_CH29_Block_Height (isp_dma_DMA_CH29_Block_Height)—Offset 41774h" on page 1489	00000000h

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
41778–4177Bh	4	"DMA_CH30_Block_Height (isp_dma_DMA_CH30_Block_Height)—Offset 41778h" on page 1490	00000000h
4177C–4177Fh	4	"DMA_CH31_Block_Height (isp_dma_DMA_CH31_Block_Height)—Offset 4177Ch" on page 1491	00000000h
41800–41803h	4	"DMA_CH0_cnt_pending_commands (isp_dma_DMA_CH0_cnt_pending_commands)—Offset 41800h" on page 1492	00000000h
41804–41807h	4	"DMA_CH1_cnt_pending_commands (isp_dma_DMA_CH1_cnt_pending_commands)—Offset 41804h" on page 1493	00000000h
41808–4180Bh	4	"DMA_CH2_cnt_pending_commands (isp_dma_DMA_CH2_cnt_pending_commands)—Offset 41808h" on page 1494	00000000h
4180C–4180Fh	4	"DMA_CH3_cnt_pending_commands (isp_dma_DMA_CH3_cnt_pending_commands)—Offset 4180Ch" on page 1495	00000000h
41810–41813h	4	"DMA_CH4_cnt_pending_commands (isp_dma_DMA_CH4_cnt_pending_commands)—Offset 41810h" on page 1496	00000000h
41814–41817h	4	"DMA_CH5_cnt_pending_commands (isp_dma_DMA_CH5_cnt_pending_commands)—Offset 41814h" on page 1497	00000000h
41818–4181Bh	4	"DMA_CH6_cnt_pending_commands (isp_dma_DMA_CH6_cnt_pending_commands)—Offset 41818h" on page 1498	00000000h
4181C–4181Fh	4	"DMA_CH7_cnt_pending_commands (isp_dma_DMA_CH7_cnt_pending_commands)—Offset 4181Ch" on page 1499	00000000h
41820–41823h	4	"DMA_CH8_cnt_pending_commands (isp_dma_DMA_CH8_cnt_pending_commands)—Offset 41820h" on page 1500	00000000h
41824–41827h	4	"DMA_CH9_cnt_pending_commands (isp_dma_DMA_CH9_cnt_pending_commands)—Offset 41824h" on page 1501	00000000h
41828–4182Bh	4	"DMA_CH10_cnt_pending_commands (isp_dma_DMA_CH10_cnt_pending_commands)—Offset 41828h" on page 1502	00000000h
4182C–4182Fh	4	"DMA_CH11_cnt_pending_commands (isp_dma_DMA_CH11_cnt_pending_commands)—Offset 4182Ch" on page 1503	00000000h
41830–41833h	4	"DMA_CH12_cnt_pending_commands (isp_dma_DMA_CH12_cnt_pending_commands)—Offset 41830h" on page 1504	00000000h
41834–41837h	4	"DMA_CH13_cnt_pending_commands (isp_dma_DMA_CH13_cnt_pending_commands)—Offset 41834h" on page 1505	00000000h

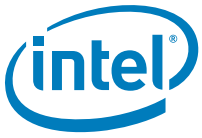


Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
41838–4183Bh	4	"DMA_CH14_cnt_pending_commands (isp_dma_DMA_CH14_cnt_pending_commands)—Offset 41838h" on page 1506	00000000h
4183C–4183Fh	4	"DMA_CH15_cnt_pending_commands (isp_dma_DMA_CH15_cnt_pending_commands)—Offset 4183Ch" on page 1507	00000000h
41840–41843h	4	"DMA_CH16_cnt_pending_commands (isp_dma_DMA_CH16_cnt_pending_commands)—Offset 41840h" on page 1508	00000000h
41844–41847h	4	"DMA_CH17_cnt_pending_commands (isp_dma_DMA_CH17_cnt_pending_commands)—Offset 41844h" on page 1509	00000000h
41848–4184Bh	4	"DMA_CH18_cnt_pending_commands (isp_dma_DMA_CH18_cnt_pending_commands)—Offset 41848h" on page 1510	00000000h
4184C–4184Fh	4	"DMA_CH19_cnt_pending_commands (isp_dma_DMA_CH19_cnt_pending_commands)—Offset 4184Ch" on page 1511	00000000h
41850–41853h	4	"DMA_CH20_cnt_pending_commands (isp_dma_DMA_CH20_cnt_pending_commands)—Offset 41850h" on page 1512	00000000h
41854–41857h	4	"DMA_CH21_cnt_pending_commands (isp_dma_DMA_CH21_cnt_pending_commands)—Offset 41854h" on page 1513	00000000h
41858–4185Bh	4	"DMA_CH22_cnt_pending_commands (isp_dma_DMA_CH22_cnt_pending_commands)—Offset 41858h" on page 1514	00000000h
4185C–4185Fh	4	"DMA_CH23_cnt_pending_commands (isp_dma_DMA_CH23_cnt_pending_commands)—Offset 4185Ch" on page 1515	00000000h
41860–41863h	4	"DMA_CH24_cnt_pending_commands (isp_dma_DMA_CH24_cnt_pending_commands)—Offset 41860h" on page 1516	00000000h
41864–41867h	4	"DMA_CH25_cnt_pending_commands (isp_dma_DMA_CH25_cnt_pending_commands)—Offset 41864h" on page 1517	00000000h
41868–4186Bh	4	"DMA_CH26_cnt_pending_commands (isp_dma_DMA_CH26_cnt_pending_commands)—Offset 41868h" on page 1518	00000000h
4186C–4186Fh	4	"DMA_CH27_cnt_pending_commands (isp_dma_DMA_CH27_cnt_pending_commands)—Offset 4186Ch" on page 1519	00000000h
41870–41873h	4	"DMA_CH28_cnt_pending_commands (isp_dma_DMA_CH28_cnt_pending_commands)—Offset 41870h" on page 1520	00000000h

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
41874–41877h	4	"DMA_CH29_cnt_pending_commands (isp_dma_DMA_CH29_cnt_pending_commands)—Offset 41874h" on page 1521	00000000h
41878–4187Bh	4	"DMA_CH30_cnt_pending_commands (isp_dma_DMA_CH30_cnt_pending_commands)—Offset 41878h" on page 1522	00000000h
4187C–4187Fh	4	"DMA_CH31_cnt_pending_commands (isp_dma_DMA_CH31_cnt_pending_commands)—Offset 4187Ch" on page 1523	00000000h
42000–42003h	4	"DMA_command_token (isp_dma_DMA_command_token)—Offset 42000h" on page 1524	00000000h
42004–42007h	4	"DMA_command_src_addr (isp_dma_DMA_command_src_addr)—Offset 42004h" on page 1525	00000000h
42008–4200Bh	4	"DMA_command_dst_addr (isp_dma_DMA_command_dst_addr)—Offset 42008h" on page 1526	00000000h
4200C–4200Fh	4	"DMA_command_ctrl_idx (isp_dma_DMA_command_ctrl_idx)—Offset 4200Ch" on page 1526	00000000h
42010–42013h	4	"DMA_FSM_Ctrl_status (isp_dma_DMA_FSM_Ctrl_status)—Offset 42010h" on page 1527	00000001h
42014–42017h	4	"DMA_FSM_Pack_status (isp_dma_DMA_FSM_Pack_status)—Offset 42014h" on page 1528	00000001h
42018–4201Bh	4	"DMA_FSM_request_status (isp_dma_DMA_FSM_request_status)—Offset 42018h" on page 1529	00000000h
4201C–4201Fh	4	"DMA_FSM_write_status (isp_dma_DMA_FSM_write_status)—Offset 4201Ch" on page 1530	00000000h
42110–42113h	4	"DMA_FSM_Ctrl_dev_interf_idx (isp_dma_DMA_FSM_Ctrl_dev_interf_idx)—Offset 42110h" on page 1530	00000000h
42114–42117h	4	"DMA_FSM_Pack_cnt_Block_Height (isp_dma_DMA_FSM_Pack_cnt_Block_Height)—Offset 42114h" on page 1531	00000000h
42118–4211Bh	4	"DMA_FSM_Request_cnt_Block_Height (isp_dma_DMA_FSM_Request_cnt_Block_Height)—Offset 42118h" on page 1532	00000000h
4211C–4211Fh	4	"DMA_FSM_Write_cnt_Block_Height (isp_dma_DMA_FSM_Write_cnt_Block_Height)—Offset 4211Ch" on page 1533	00000000h
42210–42213h	4	"DMA_FSM_Ctrl_req_addr (isp_dma_DMA_FSM_Ctrl_req_addr)—Offset 42210h" on page 1534	00000000h
42214–42217h	4	"DMA_FSM_Pack_req_cnt_Block_Width (isp_dma_DMA_FSM_Pack_req_cnt_Block_Width)—Offset 42214h" on page 1535	00000000h
42218–4221Bh	4	"DMA_FSM_Request_cnt_Block_Width (isp_dma_DMA_FSM_Request_cnt_Block_Width)—Offset 42218h" on page 1536	00000000h

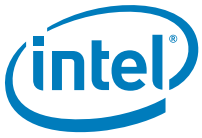


Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4221C–4221Fh	4	"DMA_FSM_Write_cnt_Xb (isp_dma_DMA_FSM_Write_cnt_Xb)—Offset 4221Ch" on page 1537	00000000h
42310–42313h	4	"DMA_FSM_Ctrl_req_stride (isp_dma_DMA_FSM_Ctrl_req_stride)—Offset 42310h" on page 1538	00000000h
42314–42317h	4	"DMA_FSM_Pack_wr_cnt_Block_Width (isp_dma_DMA_FSM_Pack_wr_cnt_Block_Width)—Offset 42314h" on page 1539	00000000h
42318–4231Bh	4	"DMA_FSM_Req_remaining_Block_Width (isp_dma_DMA_FSM_Req_remaining_Block_Width)—Offset 42318h" on page 1540	00000000h
4231C–4231Fh	4	"DMA_FSM_Wr_remaining_Block_Width (isp_dma_DMA_FSM_Wr_remaining_Block_Width)—Offset 4231Ch" on page 1540	00000000h
42410–42413h	4	"DMA_FSM_Ctrl_req_Block_Width (isp_dma_DMA_FSM_Ctrl_req_Block_Width)—Offset 42410h" on page 1541	00000000h
42418–4241Bh	4	"DMA_FSM_Req_burst_cnt (isp_dma_DMA_FSM_Req_burst_cnt)—Offset 42418h" on page 1542	0000FFFFh
4241C–4241Fh	4	"DMA_FSM_Wr_burst_cnt (isp_dma_DMA_FSM_Wr_burst_cnt)—Offset 4241Ch" on page 1543	0000FFFFh
42510–42513h	4	"DMA_FSM_Ctrl_req_Block_Height (isp_dma_DMA_FSM_Ctrl_req_Block_Height)—Offset 42510h" on page 1544	00000000h
42610–42613h	4	"DMA_FSM_Ctrl_Pack_req_dev_interf_idx (isp_dma_DMA_FSM_Ctrl_Pack_req_dev_interf_idx)—Offset 42610h" on page 1545	00000000h
42710–42713h	4	"DMA_FSM_Ctrl_Pack_wr_dev_interf_idx (isp_dma_DMA_FSM_Ctrl_Pack_wr_dev_interf_idx)—Offset 42710h" on page 1546	00000000h
42810–42813h	4	"DMA_FSM_Ctrl_Wr_addr (isp_dma_DMA_FSM_Ctrl_Wr_addr)—Offset 42810h" on page 1547	00000000h
42910–42913h	4	"DMA_FSM_Ctrl_Wr_stride (isp_dma_DMA_FSM_Ctrl_Wr_stride)—Offset 42910h" on page 1548	00000000h
42A10–42A13h	4	"DMA_FSM_Ctrl_pack_req_Block_Width (isp_dma_DMA_FSM_Ctrl_pack_req_Block_Width)—Offset 42A10h" on page 1549	00000000h
42B10–42B13h	4	"DMA_FSM_Ctrl_pack_Block_Height (isp_dma_DMA_FSM_Ctrl_pack_Block_Height)—Offset 42B10h" on page 1549	00000000h
42C10–42C13h	4	"DMA_FSM_Ctrl_pack_wr_Block_Width (isp_dma_DMA_FSM_Ctrl_pack_wr_Block_Width)—Offset 42C10h" on page 1550	00000000h
42D10–42D13h	4	"DMA_FSM_Ctrl_pack_req_elem (isp_dma_DMA_FSM_Ctrl_pack_req_elem)—Offset 42D10h" on page 1551	00000000h

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
42E10–42E13h	4	"DMA_FSM_Ctrl_pack_wr_elem (isp_dma_DMA_FSM_Ctrl_pack_wr_elem)—Offset 42E10h" on page 1552	00000000h
42F10–42F13h	4	"DMA_FSM_Ctrl_pack_sgnzext_ctrl_idx (isp_dma_DMA_FSM_Ctrl_pack_sgnzext_ctrl_idx)—Offset 42F10h" on page 1553	00000000h
43000–43003h	4	"Dev_Interf_0_status_req_side (isp_dma_Dev_Interf_0_status_req_side)—Offset 43000h" on page 1554	00000000h
43004–43007h	4	"Dev_Interf_1_status_req_side (isp_dma_Dev_Interf_1_status_req_side)—Offset 43004h" on page 1555	00000006h
43008–4300Bh	4	"Dev_Interf_2_status_req_side (isp_dma_Dev_Interf_2_status_req_side)—Offset 43008h" on page 1556	00000006h
43100–43103h	4	"Dev_Interf_0_status_send_side (isp_dma_Dev_Interf_0_status_send_side)—Offset 43100h" on page 1557	00000004h
43104–43107h	4	"Dev_Interf_1_status_send_side (isp_dma_Dev_Interf_1_status_send_side)—Offset 43104h" on page 1558	00000006h
43108–4310Bh	4	"Dev_Interf_2_status_send_side (isp_dma_Dev_Interf_2_status_send_side)—Offset 43108h" on page 1559	00000006h
43200–43203h	4	"Dev_Interf_0_Fifo_status (isp_dma_Dev_Interf_0_Fifo_status)—Offset 43200h" on page 1560	00000004h
43204–43207h	4	"Dev_Interf_1_Fifo_status (isp_dma_Dev_Interf_1_Fifo_status)—Offset 43204h" on page 1561	00000004h
43208–4320Bh	4	"Dev_Interf_2_Fifo_status (isp_dma_Dev_Interf_2_Fifo_status)—Offset 43208h" on page 1562	00000004h
43300–43303h	4	"Dev_Interf_0_Req_complete_bust (isp_dma_Dev_Interf_0_Req_complete_bust)—Offset 43300h" on page 1563	00000000h
43304–43307h	4	"Dev_Interf_1_Req_complete_bust (isp_dma_Dev_Interf_1_Req_complete_bust)—Offset 43304h" on page 1564	00000000h
43308–4330Bh	4	"Dev_Interf_2_Req_complete_bust (isp_dma_Dev_Interf_2_Req_complete_bust)—Offset 43308h" on page 1565	00000000h
43408–4340Bh	4	"Dev_Interf_2_Max_Burst_Size (isp_dma_Dev_Interf_2_Max_Burst_Size)—Offset 43408h" on page 1566	0000007Fh
50000–50003h	4	"reg0 (gdc1_reg0)—Offset 50000h" on page 1567	00000000h
50004–50007h	4	"woi_x (gdc1_woi_x)—Offset 50004h" on page 1568	00000000h
50008–5000Bh	4	"woi_y (gdc1_woi_y)—Offset 50008h" on page 1568	00000000h

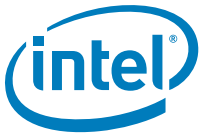


Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
5000C–5000Fh	4	"bpp (gdc1_bpp)—Offset 5000Ch" on page 1569	00000000h
50010–50013h	4	"fryipxfrx_start (gdc1_fryipxfrx_start)—Offset 50010h" on page 1569	00000000h
50014–50017h	4	"oxdim (gdc1_oxdim)—Offset 50014h" on page 1570	00000000h
50018–5001Bh	4	"oydim (gdc1_oydim)—Offset 50018h" on page 1571	00000000h
5001C–5001Fh	4	"src_addr (gdc1_src_addr)—Offset 5001Ch" on page 1571	00000000h
50020–50023h	4	"src_end (gdc1_src_end)—Offset 50020h" on page 1572	00000000h
50024–50027h	4	"src_wrap (gdc1_src_wrap)—Offset 50024h" on page 1572	00000000h
50028–5002Bh	4	"src_stride (gdc1_src_stride)—Offset 50028h" on page 1573	00000000h
5002C–5002Fh	4	"dst_addr (gdc1_dst_addr)—Offset 5002Ch" on page 1574	00000000h
50030–50033h	4	"dst_stride (gdc1_dst_stride)—Offset 50030h" on page 1574	00000000h
50034–50037h	4	"dx (gdc1_dx)—Offset 50034h" on page 1575	00000000h
50038–5003Bh	4	"dy (gdc1_dy)—Offset 50038h" on page 1575	00000000h
5003C–5003Fh	4	"P0_primX_ixdim (gdc1_P0_primX_ixdim)—Offset 5003Ch" on page 1576	00000000h
50040–50043h	4	"P0_primY_iydim (gdc1_P0_primY_iydim)—Offset 50040h" on page 1577	00000000h
50044–50047h	4	"P1_primX (gdc1_P1_primX)—Offset 50044h" on page 1577	00000000h
50048–5004Bh	4	"P1_primY (gdc1_P1_primY)—Offset 50048h" on page 1578	00000000h
5004C–5004Fh	4	"P2_primX (gdc1_P2_primX)—Offset 5004Ch" on page 1579	00000000h
50050–50053h	4	"P2_primY (gdc1_P2_primY)—Offset 50050h" on page 1579	00000000h
50054–50057h	4	"P3_primX (gdc1_P3_primX)—Offset 50054h" on page 1580	00000000h
50058–5005Bh	4	"P3_primY (gdc1_P3_primY)—Offset 50058h" on page 1581	00000000h
5005C–5005Fh	4	"perf_mode (gdc1_perf_mode)—Offset 5005Ch" on page 1581	00000000h
50060–50063h	4	"interp_type (gdc1_interp_type)—Offset 50060h" on page 1582	00000000h
50064–50067h	4	"scan_mode (gdc1_scan_mode)—Offset 50064h" on page 1582	00000000h
50068–5006Bh	4	"proc_mode (gdc1_proc_mode)—Offset 50068h" on page 1583	00000000h
60000–60003h	4	"reg0 (gdc2_reg0)—Offset 60000h" on page 1584	00000000h
60004–60007h	4	"woi_x (gdc2_woi_x)—Offset 60004h" on page 1584	00000000h
60008–6000Bh	4	"woi_y (gdc2_woi_y)—Offset 60008h" on page 1585	00000000h
6000C–6000Fh	4	"bpp (gdc2_bpp)—Offset 6000Ch" on page 1585	00000000h
60010–60013h	4	"fryipxfrx_start (gdc2_fryipxfrx_start)—Offset 60010h" on page 1586	00000000h
60014–60017h	4	"oxdim (gdc2_oxdim)—Offset 60014h" on page 1587	00000000h
60018–6001Bh	4	"oydim (gdc2_oydim)—Offset 60018h" on page 1587	00000000h
6001C–6001Fh	4	"src_addr (gdc2_src_addr)—Offset 6001Ch" on page 1588	00000000h
60020–60023h	4	"src_end (gdc2_src_end)—Offset 60020h" on page 1588	00000000h

Table 27. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
60024–60027h	4	"src_wrap (gdc2_src_wrap)—Offset 60024h" on page 1589	00000000h
60028–6002Bh	4	"src_stride (gdc2_src_stride)—Offset 60028h" on page 1590	00000000h
6002C–6002Fh	4	"dst_addr (gdc2_dst_addr)—Offset 6002Ch" on page 1590	00000000h
60030–60033h	4	"dst_stride (gdc2_dst_stride)—Offset 60030h" on page 1591	00000000h
60034–60037h	4	"dx (gdc2_dx)—Offset 60034h" on page 1592	00000000h
60038–6003Bh	4	"dy (gdc2_dy)—Offset 60038h" on page 1592	00000000h
6003C–6003Fh	4	"P0_primX_ixdim (gdc2_P0_primX_ixdim)—Offset 6003Ch" on page 1593	00000000h
60040–60043h	4	"P0_primY_iydim (gdc2_P0_primY_iydim)—Offset 60040h" on page 1593	00000000h
60044–60047h	4	"P1_primX (gdc2_P1_primX)—Offset 60044h" on page 1594	00000000h
60048–6004Bh	4	"P1_primY (gdc2_P1_primY)—Offset 60048h" on page 1595	00000000h
6004C–6004Fh	4	"P2_primX (gdc2_P2_primX)—Offset 6004Ch" on page 1595	00000000h
60050–60053h	4	"P2_primY (gdc2_P2_primY)—Offset 60050h" on page 1596	00000000h
60054–60057h	4	"P3_primX (gdc2_P3_primX)—Offset 60054h" on page 1596	00000000h
60058–6005Bh	4	"P3_primY (gdc2_P3_primY)—Offset 60058h" on page 1597	00000000h
6005C–6005Fh	4	"perf_mode (gdc2_perf_mode)—Offset 6005Ch" on page 1598	00000000h
60060–60063h	4	"interp_type (gdc2_interp_type)—Offset 60060h" on page 1598	00000000h
60064–60067h	4	"scan_mode (gdc2_scan_mode)—Offset 60064h" on page 1599	00000000h
60068–6006Bh	4	"proc_mode (gdc2_proc_mode)—Offset 60068h" on page 1600	00000000h
70000–70003h	4	"MMU_invalidate_cache (data_out_sys_c_mmu_MMU_invalidate_cache)—Offset 70000h" on page 1600	00000000h
70004–70007h	4	"MMU_page_table_base (data_out_sys_c_mmu_MMU_page_table_base)—Offset 70004h" on page 1601	00000000h

5.2.1 reg_gp_sdram_wakeup (gpd_gp_reg_reg_gp_sdram_wakeup)—Offset 0h

When set to 1, this signal will cause the memory controller to bring the external SDRAM into an active state.

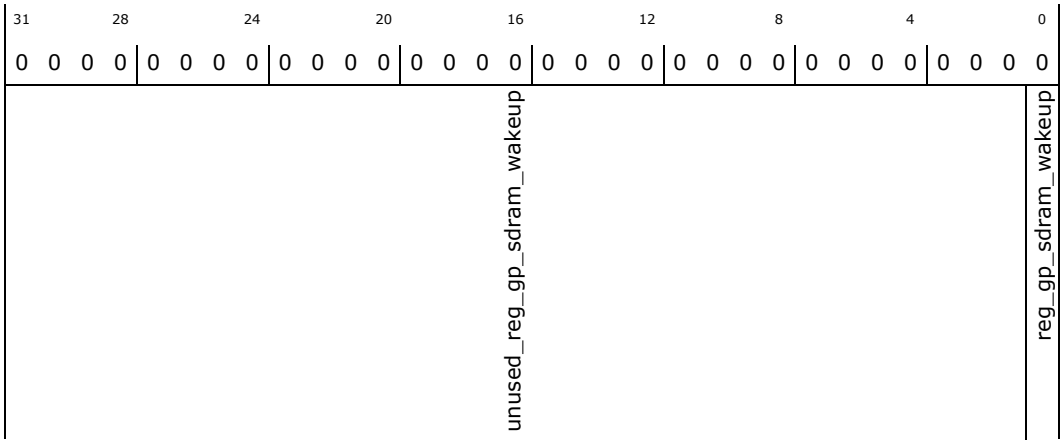
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 0h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_gp_sdram_wakeup):** Unused
0	0x0 RW	**reg_gp_sdram_wakeup:** when set to 1, this signal will cause the memory controller to bring the external SDRAM into an active state.

5.2.2 reg_gp_idle (gpd_gp_reg_reg_gp_idle)—Offset 4h

Should be set to 1 when ISP system is in idle mode.

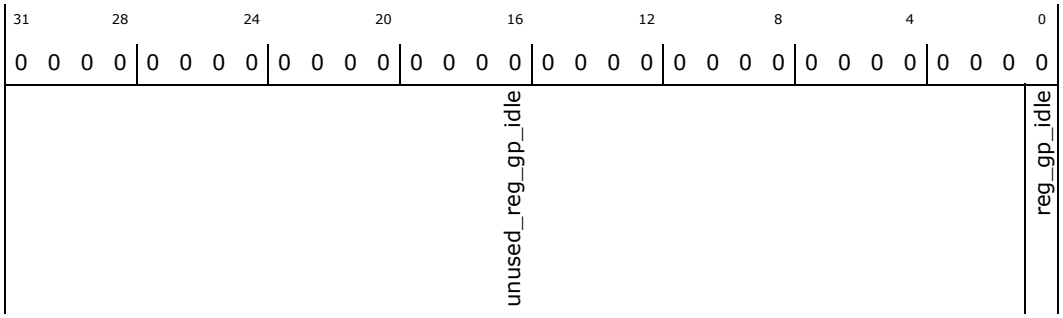
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_gp_idle):** Unused
0	0x0 RW	**reg_gp_idle:** Should be set to 1 when ISP system is in ?idle? mode.

5.2.3 reg_gp_irq_req0 (gpd_gp_reg_reg_gp_irq_req0)—Offset 8h

Possibly causes an interrupt request (if the host interrupt controller is properly configured)

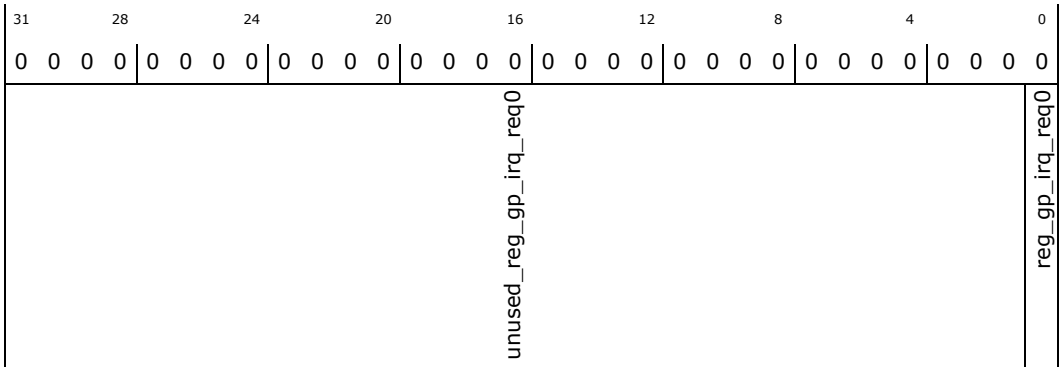
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_gp_irq_req0):** Unused

Bit Range	Default and Access	Field Name (ID): Description
0	0x0 RW	**reg_gp_irq_req0:** possibly causes an interrupt request (if the host interrupt controller is properly configured)

5.2.4 reg_gp_irq_req1 (gpd_gp_reg_reg_gp_irq_req1)—Offset Ch

Possibly causes an interrupt request (if the host interrupt controller is properly configured).

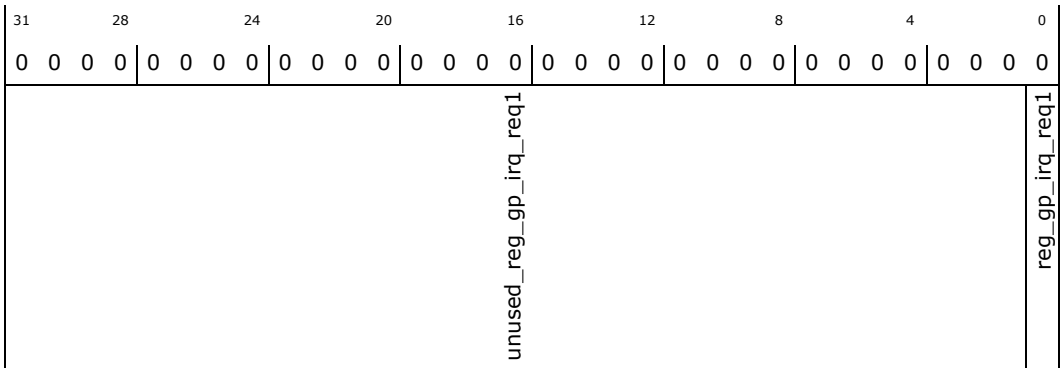
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_gp_irq_req1):** Unused
0	0x0 RW	**reg_gp_irq_req1:** possibly causes an interrupt request (if the host interrupt controller is properly configured)

5.2.5 reg_gp_sp_stream_stat (gpd_gp_reg_reg_gp_sp_stream_stat)—Offset 10h

Indicates the status of the streaming ports of the scalar processor. All valid and accept signals of the scalar processor are reflected in this register and in reg_gp_sp_stream_stat_b.

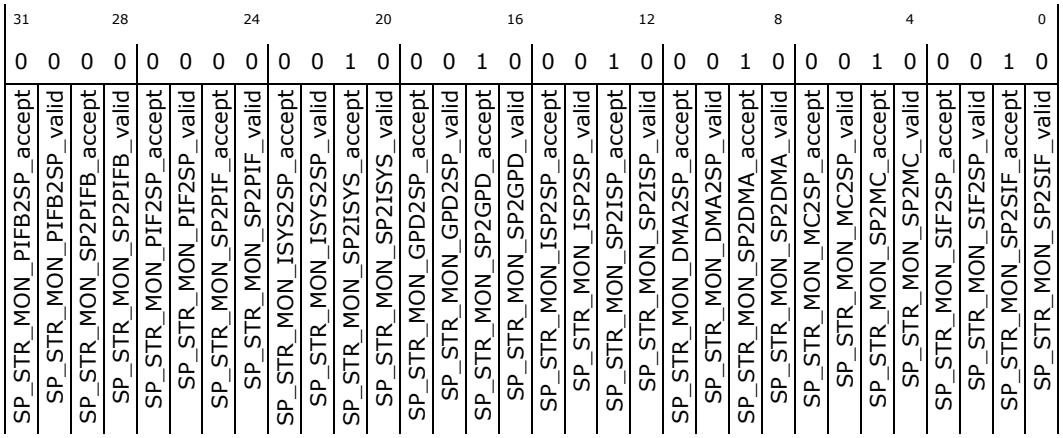
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00222222h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RO	**SP_STR_MON_PIFB2SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the primary input formatter B acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
30	0x0 RO	**SP_STR_MON_PIFB2SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the primary input formatter B acknowledge port and the SP, is present on the primary input formatter B input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
29	0x0 RO	**SP_STR_MON_SP2PIFB_accept:** Returns the value 1 if the command FIFO between SP and the Primary input formatter B can accept a command from the SP. Returns the value 0 if this FIFO cannot accept a token from the SP.
28	0x0 RO	**SP_STR_MON_SP2PIFB_valid:** Returns the value 1 if SP sends a command using the streaming port connected to the Primary Input Formatter B command FIFO. Returns the value 0 if the SP does not send a command to this FIFO
27	0x0 RO	**SP_STR_MON_PIF2SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the primary input formatter acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
26	0x0 RO	**SP_STR_MON_PIF2SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the primary input formatter acknowledge port and the SP, is present on the primary input formatter input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.

Bit Range	Default and Access	Field Name (ID): Description
25	0x0 RO	**SP_STR_MON_SP2PIF_accept:** Returns the value 1 if the command FIFO between SP and the Primary input formatter can accept a command from the SP. Returns the value 0 if this command FIFO cannot accept a command from the SP.
24	0x0 RO	**SP_STR_MON_SP2PIF_valid:** Returns the value 1 if SP sends a command using the streaming port connected to the Primary Input Formatter command FIFO. Returns the value 0 if the SP does not send a command to the Primary Input formatter
23	0x0 RO	**SP_STR_MON_ISYS2SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the input system acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
22	0x0 RO	**SP_STR_MON_ISYS2SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the input system acknowledge port and the SP, is present on the input system input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
21	0x1 RO	**SP_STR_MON_SP2ISYS_accept:** Returns the value 1 if the command FIFO between SP and the input system can accept a command from the SP. Returns the value 0 if this command FIFO cannot accept a command from the SP.
20	0x0 RO	**SP_STR_MON_SP2ISYS_valid:** Returns the value 1 if SP sends a command using the streaming port connected to the input system command FIFO. Returns the value 0 if the SP does not send a command to the input system
19	0x0 RO	**SP_STR_MON_GPD2SP_accept:** Returns the value 1 if the SP can accept a token from the streaming FIFO between the FIFO adapter in GP devices and the SP. Returns 0 if the SP cannot accept a token from this FIFO.
18	0x0 RO	**SP_STR_MON_GPD2SP_valid:** Returns the value 1 if the streaming FIFO between the FIFO adapter in GP devices and the SP has a valid token for the SP. Returns the value 0 if this FIFO is empty.
17	0x1 RO	**SP_STR_MON_SP2GPD_accept:** Returns the value 1 if the token FIFO between SP and FIFO adapter can accept a token from the SP. Returns the value 0 if this token FIFO is full.
16	0x0 RO	**SP_STR_MON_SP2GPD_valid:** Returns the value 1 if SP sends a token using the streaming port connected to the token FIFO between the SP and the FIFO adapter in GP_devices. Returns the value 0 if the SP does not send a token to the FIFO adapter.
15	0x0 RO	**SP_STR_MON_ISP2SP_accept:** Returns the value 1 if the SP can accept a token from the streaming FIFO between the ISP and the SP. Returns 0 if the SP cannot accept a token from this FIFO.
14	0x0 RO	**SP_STR_MON_ISP2SP_valid:** Returns the value 1 if the streaming FIFO between the ISP and the SP has a valid token for the SP. Returns the value 0 if this FIFO is empty
13	0x1 RO	**SP_STR_MON_SP2ISP_accept:** Returns the value 1 if the token FIFO between SP and ISP can accept a token from the SP. Returns the value 0 if this token FIFO is full.

Bit Range	Default and Access	Field Name (ID): Description
12	0x0 RO	**SP_STR_MON_SP2ISP_valid:** Returns the value 1 if SP sends a token using the streaming port connected to the ISP token FIFO. Returns the value 0 if the SP does not send a token to the ISP
11	0x0 RO	**SP_STR_MON_DMA2SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the DMA acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
10	0x0 RO	**SP_STR_MON_DMA2SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the DMA acknowledge port and the SP, is present on the DMA input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
9	0x1 RO	**SP_STR_MON_SP2DMA_accept:** Returns the value 1 if the command FIFO between SP and the DMA can accept a command from the SP. Returns the value 0 if this command FIFO cannot accept a command from the SP.
8	0x0 RO	**SP_STR_MON_SP2DMA_valid:** Returns the value 1 if SP sends a command using the streaming port connected to the DMA command FIFO. Returns the value 0 if the SP does not send a command to the DMA
7	0x0 RO	**SP_STR_MON_MC2SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the stream2mem acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
6	0x0 RO	**SP_STR_MON_MC2SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the stream2mem acknowledge port and the SP, is present on the stream2mem input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
5	0x1 RO	**SP_STR_MON_SP2MC_accept:** Returns the value 1 if the command FIFO between SP and the stream2mem can accept a command from the SP. Returns the value 0 if this command FIFO is full.
4	0x0 RO	**SP_STR_MON_SP2MC_valid:** Returns the value 1 if SP sends a command using the streaming port connected to the stream2mem command FIFO. Returns the value 0 if the SP does not send a command to the stream2mem
3	0x0 RO	**SP_STR_MON_SIF2SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the secondary input formatter acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
2	0x0 RO	**SP_STR_MON_SIF2SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the secondary input formatter acknowledge port and the SP, is present on the secondary input formatter input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
1	0x1 RO	**SP_STR_MON_SP2SIF_accept:** Returns the value 1 if the command FIFO between SP and the secondary input formatter can accept a command from the SP. Returns the value 0 if this command FIFO is full.
0	0x0 RO	**SP_STR_MON_SP2SIF_valid:** Returns the value 1 if SP sends a command using the streaming port connected to the Secondary Input Formatter command FIFO. Returns the value 0 if the SP does not send a command to the Secondary Input formatter

5.2.6 reg_gp_sp_stream_stat_b (gpd_gp_reg_reg_gp_sp_stream_stat_b)—Offset 14h

Indicates the status of the streaming ports of the scalar processor. All valid and accept signals of the scalar processor are reflected in this register and in reg_gp_sp_stream_stat.

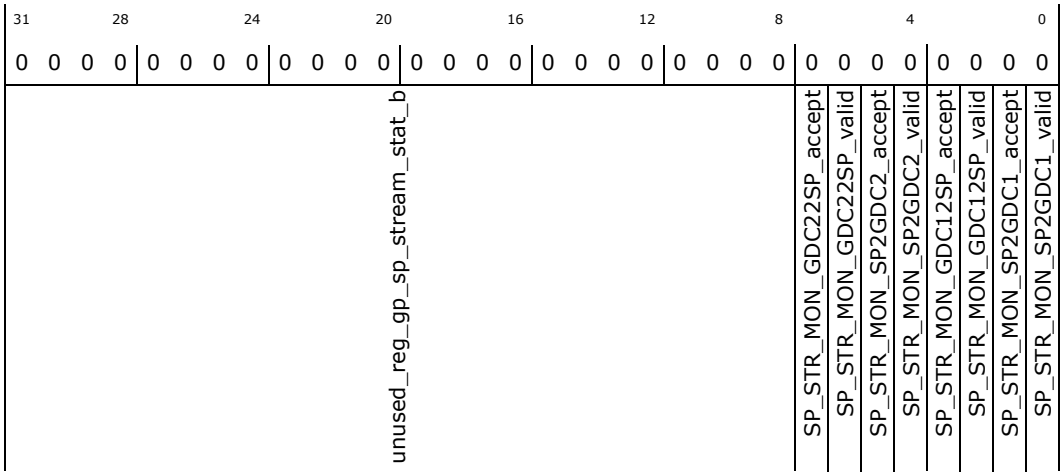
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 14h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (unused_reg_gp_sp_stream_stat_b):** Unused
7	0x0 RO	**SP_STR_MON_GDC22SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the GDC2 acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
6	0x0 RO	**SP_STR_MON_GDC22SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the GDC2 acknowledge port and the SP, is present on the GDC2 input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
5	0x0 RO	**SP_STR_MON_SP2GDC2_accept:** Returns the value 1 if the command FIFO between SP and GDC2 can accept a command from the SP. Returns the value 0 if this command FIFO cannot accept a command from the SP.
4	0x0 RO	**SP_STR_MON_SP2GDC2_valid:** Returns the value 1 if SP sends a command using the streaming port connected to GDC2 command FIFO. Returns the value 0 if the SP does not send a command to GDC2

Bit Range	Default and Access	Field Name (ID): Description
3	0x0 RO	**SP_STR_MON_GDC12SP_accept:** Returns the value 1 if the SP can accept an acknowledge token from the FIFO between the GDC1 acknowledge port and the SP. Returns the value 0 if the SP cannot accept a token on this SP input port.
2	0x0 RO	**SP_STR_MON_GDC12SP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the GDC1 acknowledge port and the SP, is present on the GDC1 input port of the SP. Returns the value 0 if there is no valid acknowledge token available on this SP input port.
1	0x0 RO	**SP_STR_MON_SP2GDC1_accept:** Returns the value 1 if the command FIFO between SP and GDC1 can accept a command from the SP. Returns the value 0 if this command FIFO cannot accept a command from the SP.
0	0x0 RO	**SP_STR_MON_SP2GDC1_valid:** Returns the value 1 if SP sends a command using the streaming port connected to GDC1 command FIFO. Returns the value 0 if the SP does not send a command to GDC1

5.2.7 reg_gp_isp_stream_stat (gpd_gp_reg_reg_gp_isp_stream_stat)—Offset 18h

Indicate the status of the streaming ports of the vector processor. All valid and accept signals of the vector processor are reflected in this register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 18h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 02222222h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
unused_reg_gp_isp_stream_stat				ISP_STR_MON_SP2ISP_accept	ISP_STR_MON_SP2ISP_valid	ISP_STR_MON_ISP2SP_accept	ISP_STR_MON_ISP2SP_valid	ISP_STR_MON_GPD2ISP_accept	ISP_STR_MON_GPD2ISP_valid	ISP_STR_MON_ISP2GPD_accept	ISP_STR_MON_ISP2GPD_valid	ISP_STR_MON_GDC22ISP_accept	ISP_STR_MON_GDC22ISP_valid	ISP_STR_MON_ISP2GDC2_accept	ISP_STR_MON_ISP2GDC2_valid	ISP_STR_MON_GDC12ISP_accept	ISP_STR_MON_GDC12ISP_valid	ISP_STR_MON_ISP2GDC1_accept	ISP_STR_MON_ISP2GDC1_valid	ISP_STR_MON_DMA2ISP_accept	ISP_STR_MON_DMA2ISP_valid	ISP_STR_MON_ISP2DMA_accept	ISP_STR_MON_ISP2DMA_valid	ISP_STR_MON_PIFB2ISP_accept	ISP_STR_MON_PIFB2ISP_valid	ISP_STR_MON_ISP2PIFB_accept	ISP_STR_MON_ISP2PIFB_valid	ISP_STR_MON_PIF2ISP_accept	ISP_STR_MON_PIF2ISP_valid	ISP_STR_MON_ISP2PIF_accept	ISP_STR_MON_ISP2PIF_valid

Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (unused_reg_gp_isp_stream_stat):** Unused
27	0x0 RO	**ISP_STR_MON_SP2ISP_accept:** Returns the value 1 if the ISP can accept a token from the streaming FIFO between the SP and the ISP. Returns 0 if the ISP cannot accept a token from this FIFO.
26	0x0 RO	**ISP_STR_MON_SP2ISP_valid:** Returns the value 1 if the streaming FIFO between the SP and the ISP has a valid token for the ISP. Returns the value 0 if this FIFO is empty
25	0x1 RO	**ISP_STR_MON_ISP2SP_accept:** Returns the value 1 if the token FIFO between ISP and SP can accept a token from the ISP. Returns the value 0 if this token FIFO is full.
24	0x0 RO	**ISP_STR_MON_ISP2SP_valid:** Returns the value 1 if ISP sends a token using the streaming port connected to the SP token FIFO. Returns the value 0 if the ISP does not send a token to the SP
23	0x0 RO	**ISP_STR_MON_GPD2ISP_accept:** Returns the value 1 if the ISP can accept a token from the streaming FIFO between the FIFO adapter in GP devices and the ISP. Returns 0 if the ISP cannot accept a token from this FIFO.
22	0x0 RO	**ISP_STR_MON_GPD2ISP_valid:** Returns the value 1 if the streaming FIFO between the FIFO adapter in GP devices and the ISP has a valid token for the ISP. Returns the value 0 if this FIFO is empty.
21	0x1 RO	**ISP_STR_MON_ISP2GPD_accept:** Returns the value 1 if the token FIFO between ISP and FIFO adapter can accept a token from the ISP. Returns the value 0 if this token FIFO is full.
20	0x0 RO	**ISP_STR_MON_ISP2GPD_valid:** Returns the value 1 if ISP sends a token using the streaming port connected to the token FIFO between the ISP and the FIFO adapter in GP_devices. Returns the value 0 if the ISP does not send a token to the FIFO adapter.
19	0x0 RO	**ISP_STR_MON_GDC22ISP_accept:** Returns the value 1 if the ISP can accept an acknowledge token from the FIFO between the GDC2 acknowledge port and the ISP. Returns the value 0 if the ISP cannot accept a token on this ISP input port.
18	0x0 RO	**ISP_STR_MON_GDC22ISP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the GDC2 acknowledge port and the ISP, is present on the GDC2 input port of the ISP. Returns the value 0 if there is no valid acknowledge token available on this ISP input port.
17	0x1 RO	**ISP_STR_MON_ISP2GDC2_accept:** Returns the value 1 if the command FIFO between ISP and GDC2 can accept a command from the ISP. Returns the value 0 if this command FIFO is full.
16	0x0 RO	**ISP_STR_MON_ISP2GDC2_valid:** Returns the value 1 if ISP sends a command using the streaming port connected to the GDC2 command FIFO. Returns the value 0 if the ISP does not send a command to GDC2
15	0x0 RO	**ISP_STR_MON_GDC12ISP_accept:** Returns the value 1 if the ISP can accept an acknowledge token from the FIFO between the GDC1 acknowledge port and the ISP. Returns the value 0 if the ISP cannot accept a token on this ISP input port.

Bit Range	Default and Access	Field Name (ID): Description
14	0x0 RO	**ISP_STR_MON_GDC12ISP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the GDC1 acknowledge port and the ISP, is present on the GDC1 input port of the ISP. Returns the value 0 if there is no valid acknowledge token available on this ISP input port.
13	0x1 RO	**ISP_STR_MON_ISP2GDC1_accept:** Returns the value 1 if the command FIFO between ISP and GDC1 can accept a command from the ISP. Returns the value 0 if this command FIFO is full.
12	0x0 RO	**ISP_STR_MON_ISP2GDC1_valid:** Returns the value 1 if ISP sends a command using the streaming port connected to the GDC1 command FIFO. Returns the value 0 if the ISP does not send a command to GDC1
11	0x0 RO	**ISP_STR_MON_DMA2ISP_accept:** Returns the value 1 if the ISP can accept an acknowledge token from the FIFO between the DMA acknowledge port and the ISP. Returns the value 0 if the ISP cannot accept a token on this ISP input port.
10	0x0 RO	**ISP_STR_MON_DMA2ISP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the DMA acknowledge port and the ISP, is present on the DMA input port of the ISP. Returns the value 0 if there is no valid acknowledge token available on this ISP input port.
9	0x1 RO	**ISP_STR_MON_ISP2DMA_accept:** Returns the value 1 if the command FIFO between ISP and the DMA can accept a command from the ISP. Returns the value 0 if this command FIFO cannot accept a token from the ISP.
8	0x0 RO	**ISP_STR_MON_ISP2DMA_valid:** Returns the value 1 if ISP sends a command using the streaming port connected to the DMA command FIFO. Returns the value 0 if the ISP does not send a command to the DMA
7	0x0 RO	**ISP_STR_MON_PIFB2ISP_accept:** Returns the value 1 if the ISP can accept an acknowledge token from the FIFO between the primary input formatter B acknowledge port and the ISP. Returns the value 0 if the ISP cannot accept a token on this ISP input port.
6	0x0 RO	**ISP_STR_MON_PIFB2ISP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the primary input formatter B acknowledge port and the ISP, is present on the primary input formatter B input port of the ISP. Returns the value 0 if there is no valid acknowledge token available on this ISP input port.
5	0x1 RO	**ISP_STR_MON_ISP2PIFB_accept:** Returns the value 1 if the command FIFO between ISP and the Primary input formatter B can accept a command from the ISP. Returns the value 0 if this FIFO cannot accept a command from the ISP.
4	0x0 RO	**ISP_STR_MON_ISP2PIFB_valid:** Returns the value 1 if ISP sends a command using the streaming port connected to the Primary Input Formatter B command FIFO. Returns the value 0 if the ISP does not send a command to the Primary Input formatter B
3	0x0 RO	**ISP_STR_MON_PIF2ISP_accept:** Returns the value 1 if the ISP can accept an acknowledge token from the FIFO between the primary input formatter acknowledge port and the ISP. Returns the value 0 if the ISP cannot accept a token on this ISP input port.

Bit Range	Default and Access	Field Name (ID): Description
2	0x0 RO	**ISP_STR_MON_PIF2ISP_valid:** Returns the value 1 if a valid acknowledge token from the FIFO between the primary input formatter acknowledge port and the ISP, is present on the primary input formatter input port of the ISP. Returns the value 0 if there is no valid acknowledge token available on this ISP input port.
1	0x1 RO	**ISP_STR_MON_ISP2PIF_accept:** Returns the value 1 if the command FIFO between ISP and the Primary input formatter can accept a command from the ISP. Returns the value 0 if this command FIFO is full.
0	0x0 RO	**ISP_STR_MON_ISP2PIF_valid:** Returns the value 1 if ISP sends a command using the streaming port connected to the Primary Input Formatter command FIFO. Returns the value 0 if the ISP does not send a command to the Primary Input formatter

5.2.8 reg_gp_mod_stream_stat (gpd_gp_reg_reg_gp_mod_stream_stat)—Offset 1Ch

Indicates the status of the streaming ports of the modules. All modules valid and accept ports used for control are reflected in this register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

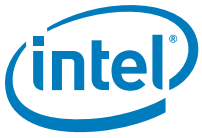
Offset: [ISPMMADR] + 1Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: AAAA2222h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
MOD_STR_MON_CELLS2GDC2_accept	MOD_STR_MON_CELLS2GDC2_valid	MOD_STR_MON_GDC22CELLS_accept	MOD_STR_MON_GDC22CELLS_valid	MOD_STR_MON_CELLS2GDC1_accept	MOD_STR_MON_CELLS2GDC1_valid	MOD_STR_MON_GDC12CELLS_accept	MOD_STR_MON_GDC12CELLS_valid	MOD_STR_MON_SP2DMA_accept	MOD_STR_MON_SP2DMA_valid	MOD_STR_MON_DMA2SP_accept	MOD_STR_MON_DMA2SP_valid	MOD_STR_MON_ISP2DMA_accept	MOD_STR_MON_ISP2DMA_valid	MOD_STR_MON_DMA2ISP_accept	MOD_STR_MON_DMA2ISP_valid	MOD_STR_MON_SP2MC_accept	MOD_STR_MON_SP2MC_valid	MOD_STR_MON_MC2SP_accept	MOD_STR_MON_MC2SP_valid	MOD_STR_MON_SP2SIF_accept	MOD_STR_MON_SP2SIF_valid	MOD_STR_MON_SIF2SP_accept	MOD_STR_MON_SIF2SP_valid	MOD_STR_MON_CELLS2PIFB_accept	MOD_STR_MON_CELLS2PIFB_valid	MOD_STR_MON_PIFB2CELLS_accept	MOD_STR_MON_PIFB2CELLS_valid	MOD_STR_MON_CELLS2PIFA_accept	MOD_STR_MON_CELLS2PIFA_valid	MOD_STR_MON_PIFA2CELLS_accept	MOD_STR_MON_PIFA2CELLS_valid

Bit Range	Default and Access	Field Name (ID): Description
31	0x1 RO	**MOD_STR_MON_CELLS2GDC2_accept:** Returns the value 1 if the acknowledge FIFO between GDC2 and ISP/SP can accept an acknowledge token from GDC2. Returns the value 0 if this FIFO is full.
30	0x0 RO	**MOD_STR_MON_CELLS2GDC2_valid:** Returns the value 1 if GDC2 sends an acknowledge token using the streaming port connected to the acknowledge FIFO to the ISP/SP. Returns the value 0 if GDC2 does not send an acknowledge token to this FIFO.
29	0x1 RO	**MOD_STR_MON_GDC22CELLS_accept:** Returns the value 1 if GDC2 can accept a command token from the command FIFO between the ISP/SP and GDC2. Returns the value 0 if GDC2 cannot accept a command token.
28	0x0 RO	**MOD_STR_MON_GDC22CELLS_valid:** Returns the value 1 if there is a command available on the command FIFO between SP/ISP and GDC2. Returns the value 0 if the command FIFO for GDC2 is empty.
27	0x1 RO	**MOD_STR_MON_CELLS2GDC1_accept:** Returns the value 1 if the acknowledge FIFO between GDC1 and ISP/SP can accept an acknowledge token from GDC1. Returns the value 0 if this FIFO is full.
26	0x0 RO	**MOD_STR_MON_CELLS2GDC1_valid:** Returns the value 1 if GDC1 sends an acknowledge token using the streaming port connected to the acknowledge FIFO to the ISP/SP. Returns the value 0 if GDC1 does not send an acknowledge token to this FIFO.
25	0x1 RO	**MOD_STR_MON_GDC12CELLS_accept:** Returns the value 1 if GDC1 can accept a command token from the command FIFO between the ISP/SP and GDC1. Returns the value 0 if GDC1 cannot accept a command token.
24	0x0 RO	**MOD_STR_MON_GDC12CELLS_valid:** Returns the value 1 if there is a command available on the command FIFO between SP/ISP and GDC1. Returns the value 0 if the command FIFO for GDC1 is empty.
23	0x1 RO	**MOD_STR_MON_SP2DMA_accept:** Returns the value 1 if the acknowledge FIFO between the DMA and SP can accept an acknowledge token from the DMA. Returns the value 0 if this FIFO is full.
22	0x0 RO	**MOD_STR_MON_SP2DMA_valid:** Returns the value 1 if DMA sends an acknowledge token using the streaming port connected to the acknowledge FIFO to the SP. Returns the value 0 if the DMA does not send an acknowledge token to this FIFO.
21	0x1 RO	**MOD_STR_MON_DMA2SP_accept:** Returns the value 1 if the DMA can accept a command token from the command FIFO between the SP and the DMA. Returns the value 0 if the DMA cannot accept a command token.
20	0x0 RO	**MOD_STR_MON_DMA2SP_valid:** Returns the value 1 if there is a command available on the command FIFO between SP and the DMA. Returns the value 0 if the command FIFO for the DMA is empty.
19	0x1 RO	**MOD_STR_MON_ISP2DMA_accept:** Returns the value 1 if the acknowledge FIFO between the DMA and ISP can accept an acknowledge token from the DMA. Returns the value 0 if this FIFO is full.
18	0x0 RO	**MOD_STR_MON_ISP2DMA_valid:** Returns the value 1 if DMA sends an acknowledge token using the streaming port connected to the acknowledge FIFO to the ISP. Returns the value 0 if the DMA does not send an acknowledge token to this FIFO.



Bit Range	Default and Access	Field Name (ID): Description
17	0x1 RO	**MOD_STR_MON_DMA2ISP_accept:** Returns the value 1 if the DMA can accept a command token from the command FIFO between the SP and the DMA. Returns the value 0 if the DMA cannot accept a command token.
16	0x0 RO	**MOD_STR_MON_DMA2ISP_valid:** Returns the value 1 if there is a command available on the command FIFO between ISP and the DMA. Returns the value 0 if the command FIFO for the DMA is empty.
15	0x0 RO	**MOD_STR_MON_SP2MC_accept:** Returns the value 1 if stream2mem can accept a command token from the command FIFO between the SP and the stream2mem. Returns the value 0 if stream2mem cannot accept a command token.
14	0x0 RO	**MOD_STR_MON_SP2MC_valid:** Returns the value 1 if there is a command available on the command FIFO between the SP and the stream2mem. Returns the value 0 if the command FIFO for the stream2mem is empty.
13	0x1 RO	**MOD_STR_MON_MC2SP_accept:** Returns the value 1 if the acknowledge FIFO between the stream2mem and the SP can accept an acknowledge token from the stream2mem. Returns the value 0 if this FIFO is full.
12	0x0 RO	**MOD_STR_MON_MC2SP_valid:** Returns the value 1 if the stream2mem sends an acknowledge token using its acknowledge output port connected to the acknowledge FIFO between the stream2mem and the SP. Returns the value 0 if the stream2mem does not send an acknowledge token to this FIFO.
11	0x0 RO	**MOD_STR_MON_SP2SIF_accept:** Returns the value 1 if secondary input formatter can accept a command token from the command FIFO between the SP and the secondary input formatter. Returns the value 0 if this FIFO is full.
10	0x0 RO	**MOD_STR_MON_SP2SIF_valid:** Returns the value 1 if there is a command available on the command FIFO between the SP and the secondary input formatter. Returns the value 0 if the command FIFO for the secondary input formatter is empty.
9	0x1 RO	**MOD_STR_MON_SIF2SP_accept:** Returns the value 1 if the acknowledge FIFO between the secondary input formatter and the SP can accept an acknowledge token from the secondary input formatter. Returns the value 0 if this FIFO is full.
8	0x0 RO	**MOD_STR_MON_SIF2SP_valid:** Returns the value 1 if the secondary input formatter sends an acknowledge token using its acknowledge output port connected to the acknowledge FIFO between the secondary input formatter and the SP. Returns the value 0 if the secondary input formatter does not send an acknowledge token to this FIFO.
7	0x0 RO	**MOD_STR_MON_CELLS2PIFB_accept:** Returns the value 1 if primary input formatter B can accept a command token from the command FIFO between the ISP/SP and the primary input formatter B. Returns the value 0 if the primary input formatter B cannot accept a command token.
6	0x0 RO	**MOD_STR_MON_CELLS2PIFB_valid:** Returns the value 1 if there is a command available on the command FIFO between SP/ISP and the primary input formatter B. Returns the value 0 if the command FIFO for the primary input formatter B is empty.
5	0x1 RO	**MOD_STR_MON_PIFB2CELLS_accept:** Returns the value 1 if the acknowledge FIFO between the primary input formatter B and the ISP/SP can accept an acknowledge token from the primary input formatter B. Returns the value 0 if this command FIFO is full.

Bit Range	Default and Access	Field Name (ID): Description
4	0x0 RO	**MOD_STR_MON_PIFB2CELLS_valid:** Returns the value 1 if primary input formatter B sends an acknowledge token using the streaming port connected to the acknowledge FIFO to the ISP/SP. Returns the value 0 if the primary input formatter B does not send an acknowledge token to this FIFO.
3	0x0 RO	**MOD_STR_MON_CELLS2PIFA_accept:** Returns the value 1 if primary input formatter A can accept a command token from the command FIFO between the ISP/SP and the primary input formatter A. Returns the value 0 if the primary input formatter A cannot accept a command token.
2	0x0 RO	**MOD_STR_MON_CELLS2PIFA_valid:** Returns the value 1 if there is a command available on the command FIFO between SP/ISP and the primary input formatter A. Returns the value 0 if the command FIFO for the primary input formatter A is empty.
1	0x1 RO	**MOD_STR_MON_PIFA2CELLS_accept:** Returns the value 1 if the acknowledge FIFO between the primary input formatter A and the ISP/SP can accept an acknowledge token from the primary input formatter A. Returns the value 0 if this command FIFO is full.
0	0x0 RO	**MOD_STR_MON_PIFA2CELLS_valid:** Returns the value 1 if primary input formatter A sends an acknowledge token using the streaming port connected to the acknowledge FIFO to the ISP/SP. Returns the value 0 if the primary input formatter A does not send an acknowledge token to this FIFO.

5.2.9 reg_gp_sp_stream_stat_irq_cond (gpd_gp_reg_reg_gp_sp_stream_stat_irq_cond)—Offset 20h

This register indicates which condition of the SP streaming ports will enable the SP streaming stat IRQ output.

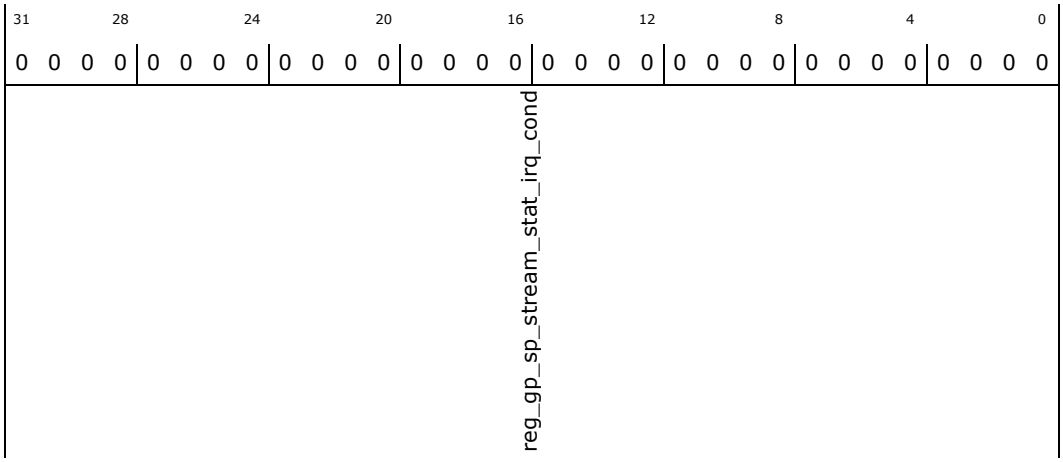
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 20h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**reg_gp_sp_stream_stat_irq_cond:** This register indicates which condition of the SP streaming ports will enable the SP streaming stat IRQ output

5.2.10 reg_gp_sp_stream_stat_b_irq_cond (gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_cond)—Offset 24h

This register indicates which condition of the SP streaming ports b will enable the SP streaming stat b IRQ output

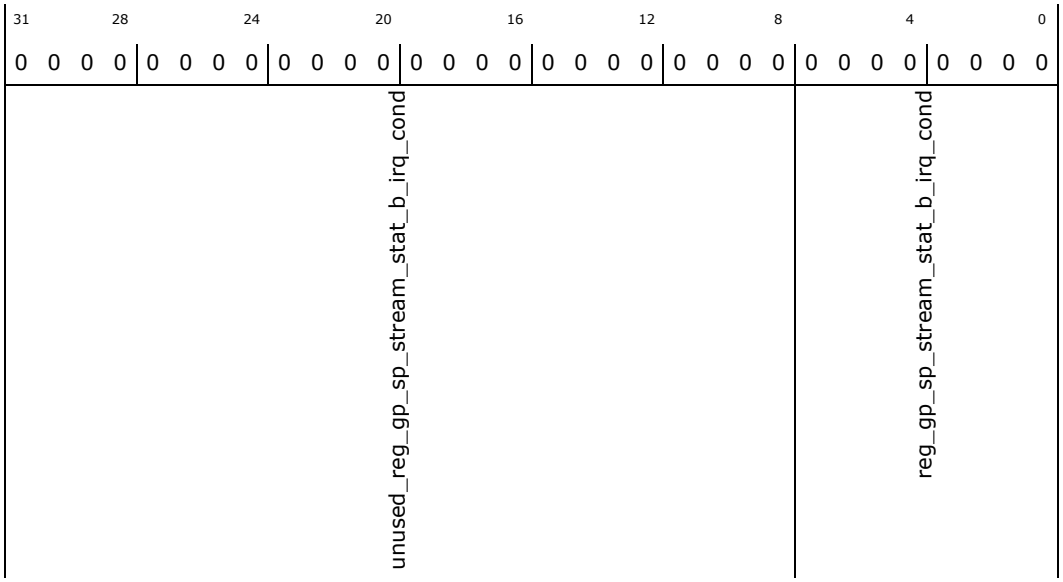
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 24h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved (unused_reg_gp_sp_stream_stat_b_irq_cond):** Unused
7:0	0x0 RW	**reg_gp_sp_stream_stat_b_irq_cond:** This register indicates which condition of the SP streaming ports b will enable the SP streaming stat b IRQ output

5.2.11 reg_gp_isp_stream_stat_irq_cond (gpd_gp_reg_reg_gp_isp_stream_stat_irq_cond)—Offset 28h

This register indicates which condition of the ISP streaming ports will enable the ISP streaming stat IRQ output

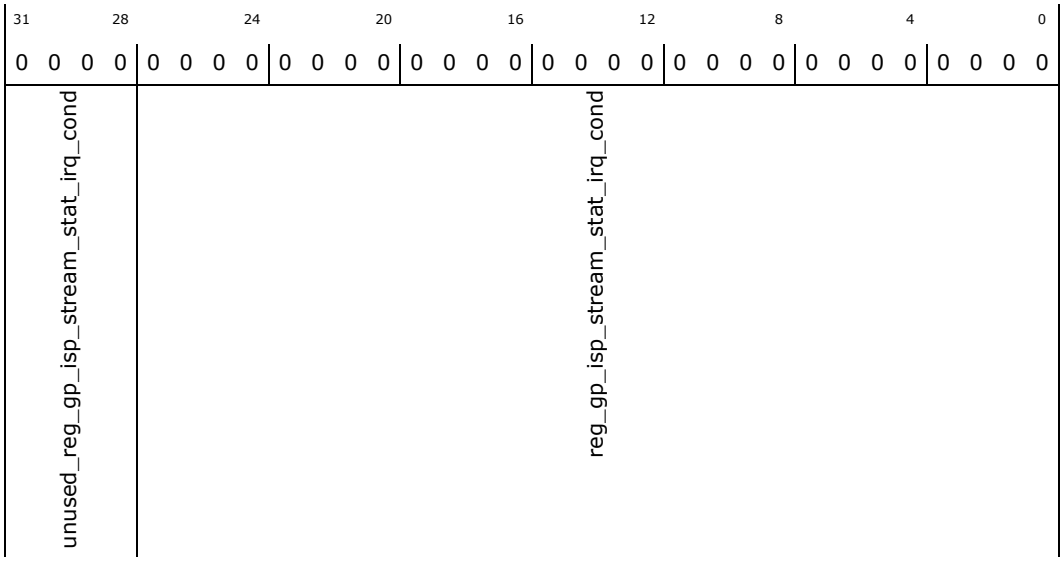
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 28h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Reserved (unused_reg_gp_isp_stream_stat_irq_cond):** Unused
27:0	0x0 RW	**reg_gp_isp_stream_stat_irq_cond:** This register indicates which condition of the ISP streaming ports will enable the ISP streaming stat IRQ output

5.2.12 reg_gp_mod_stream_stat_irq_cond (gpd_gp_reg_reg_gp_mod_stream_stat_irq_cond)—Offset 2Ch

This register indicates which condition of the MOD streaming ports will enable the MOD streaming stat IRQ output

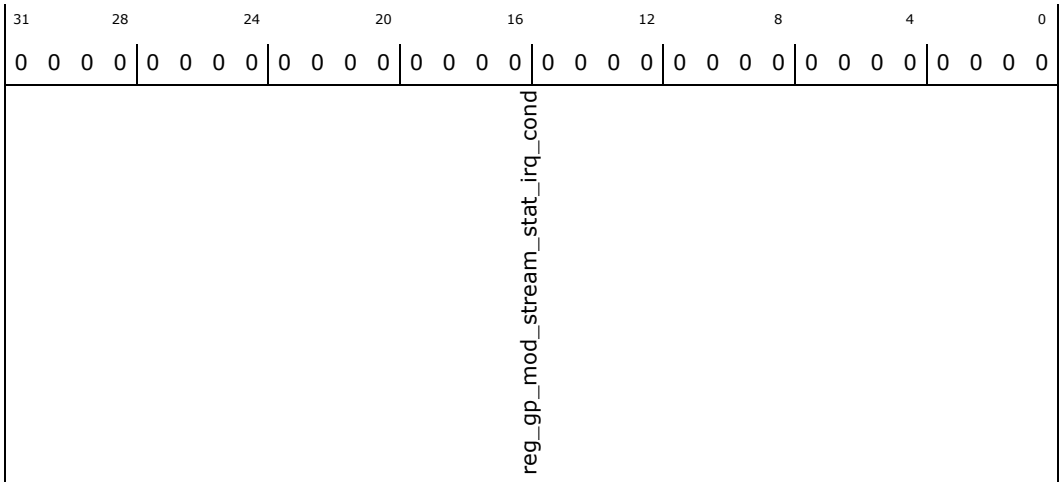
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 2Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**reg_gp_mod_stream_stat_irq_cond:** This register indicates which condition of the MOD streaming ports will enable the MOD streaming stat IRQ output

5.2.13 reg_gp_sp_stream_stat_irq_enable (gpd_gp_reg_reg_gp_sp_stream_stat_irq_enable)—Offset 30h

This register enables the SP streaming stat IRQ output for each of the 16 ports

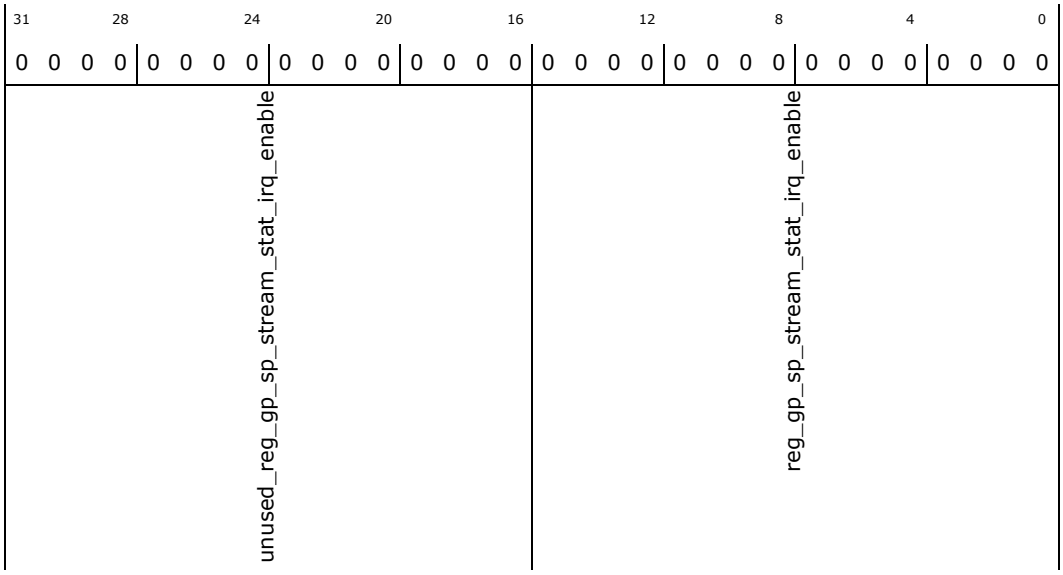
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_reg_gp_sp_stream_stat_irq_enable):** Unused
15:0	0x0 RW	**reg_gp_sp_stream_stat_irq_enable:** This register enables the SP streaming stat IRQ output for each of the 16 ports

5.2.14 reg_gp_sp_stream_stat_b_irq_enable (gpd_gp_reg_reg_gp_sp_stream_stat_b_irq_enable)—Offset 34h

This register enables the SP streaming stat b IRQ output for each of the 4 ports.

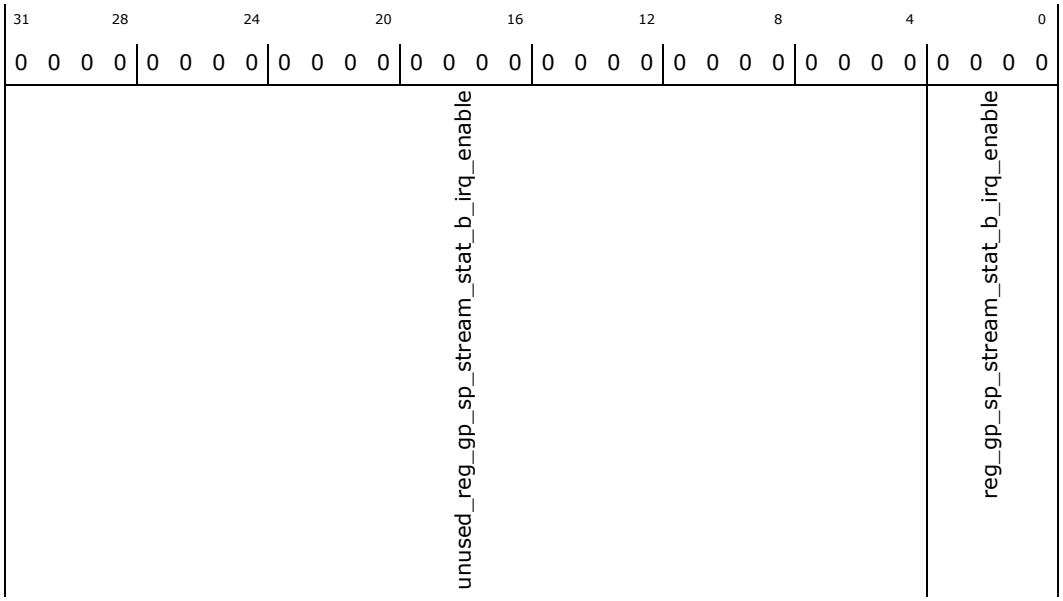
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 34h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RW	**Reserved (unused_reg_gp_sp_stream_stat_b_irq_enable):** Unused
3:0	0x0 RW	**reg_gp_sp_stream_stat_b_irq_enable:** This register enables the SP streaming stat b IRQ output for each of the 4 ports

5.2.15 reg_gp_isp_stream_stat_irq_enable (gpd_gp_reg_reg_gp_isp_stream_stat_irq_enable)—Offset 38h

This register enables the ISP streaming stat IRQ output for each of the 14 ports

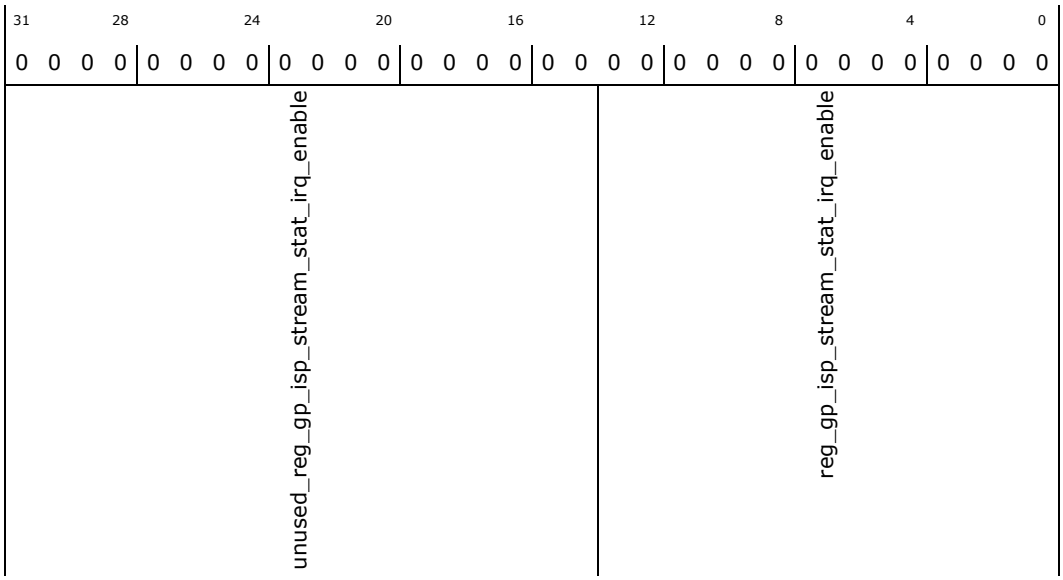
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 38h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RW	**Reserved (unused_reg_gp_isp_stream_stat_irq_enable):** Unused
13:0	0x0 RW	**reg_gp_isp_stream_stat_irq_enable:** This register enables the ISP streaming stat IRQ output for each of the 14 ports

5.2.16 reg_gp_mod_stream_stat_irq_enable (gpd_gp_reg_reg_gp_mod_stream_stat_irq_enable)—Offset 3Ch

This register enables the MOD streaming stat IRQ output for each of the 16 ports.

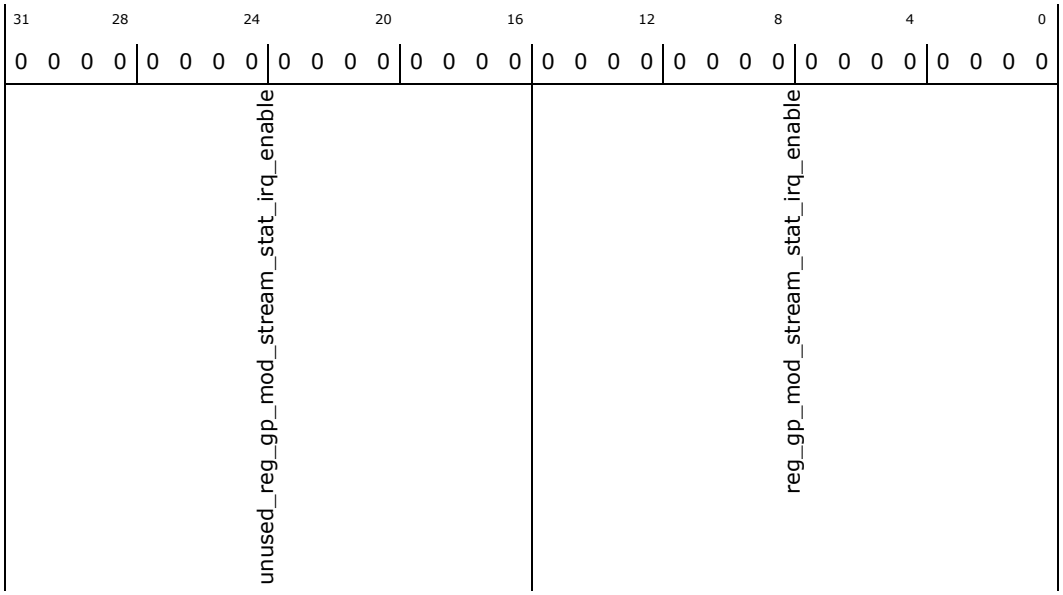
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_reg_gp_mod_stream_stat_irq_enable):** Unused
15:0	0x0 RW	**reg_gp_mod_stream_stat_irq_enable:** This register enables the MOD streaming stat IRQ output for each of the 16 ports

5.2.17 reg_gp_switch_if (gpd_gp_reg_reg_gp_switch_if)—Offset 40h

Selects the control stream switch for the primary input formatter and for primary input formatter b. The input formatters can be controlled by the scalar processor (value=1) or by the ISP (value=0)

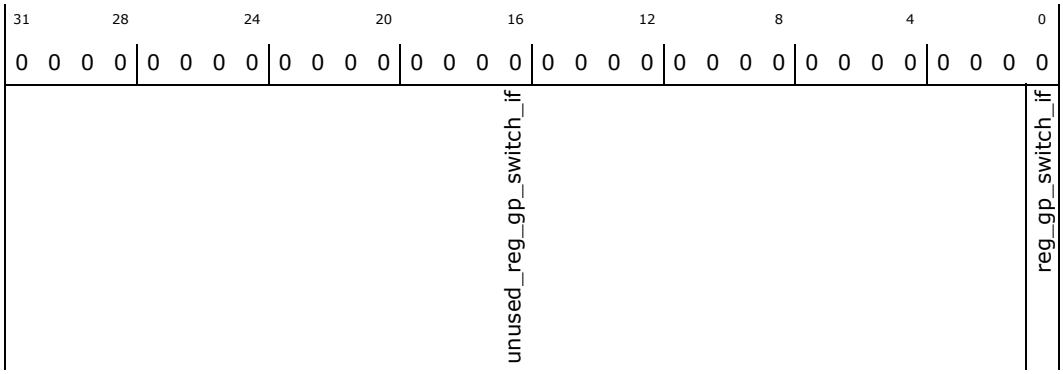
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 40h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_gp_switch_if):** Unused
0	0x0 RW	**reg_gp_switch_if:** Selects the control stream switch for the primary input formatter and for primary input formatter b. The input formatters can be controlled by the scalar processor (value=1) or by the ISP (value=0)

5.2.18 reg_gp_switch_gdc1 (gpd_gp_reg_reg_gp_switch_gdc1)—Offset 44h

Selects the control stream switch for the GDC1. GDC1 can be controlled by the scalar processor (value=1) or the ISP (value=0)

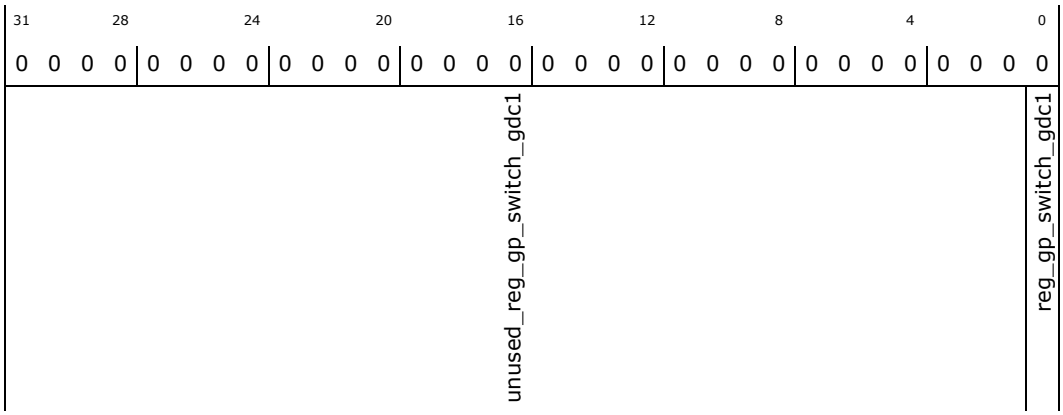
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 44h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_gp_switch_gdc1):** Unused
0	0x0 RW	**reg_gp_switch_gdc1:** Selects the control stream switch for the GDC1. GDC1 can be controlled by the scalar processor (value=1) or the ISP (value=0)

5.2.19 reg_gp_switch_gdc2 (gpd_gp_reg_reg_gp_switch_gdc2)—Offset 48h

Selects the control stream switch for the GDC2. GDC2 can be controlled by the scalar processor (value=1) or the ISP (value=0)

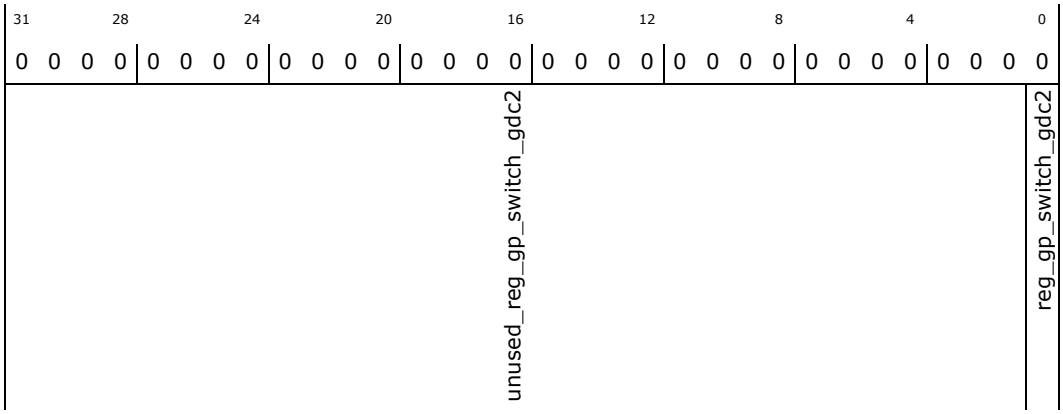
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 48h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_gp_switch_gdc2):** Unused
0	0x0 RW	**reg_gp_switch_gdc2:** Selects the control stream switch for the GDC2. GDC2 can be controlled by the scalar processor (value=1) or the ISP (value=0)

5.2.20 reg_gp_srst (gpd_gp_reg_reg_gp_srst)—Offset 4Ch

Soft reset for several modules in the system. If '1' is written to a bit, the module(s) connected to that bit are held in reset until a '0' is written to that bit.

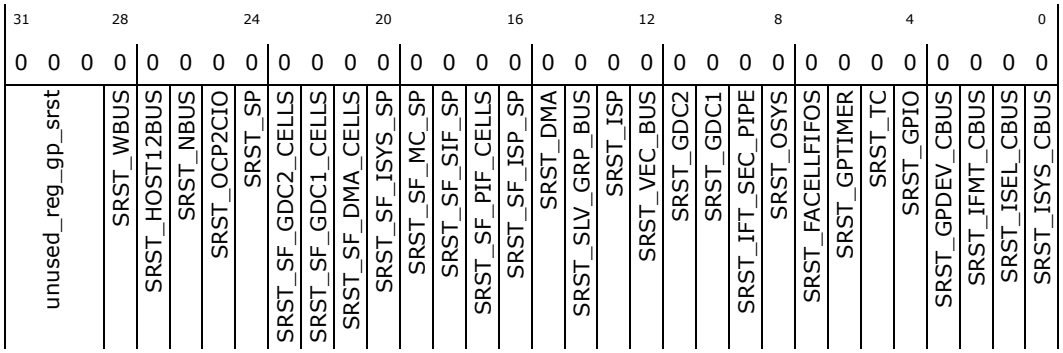
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:29	0x0 RO	**Reserved (unused_reg_gp_srst):** Unused
28	0x0 RW	**SRST_WBUS:** soft reset bit for the wide bus
27	0x0 RW	**SRST_HOST12BUS:** soft reset bit for the bus from host to FIFO adapters
26	0x0 RW	**SRST_NBUS:** soft reset bit for the narrow bus
25	0x0 RW	**SRST_OCP2CIO:** soft reset bit for the OCP2CIO converter
24	0x0 RW	**SRST_SP:** soft reset bit for the SP
23	0x0 RW	**SRST_SF_GDC2_CELLS:** soft reset bit for the FIFOs between the GDC2 and the cells
22	0x0 RW	**SRST_SF_GDC1_CELLS:** soft reset bit for the FIFOs between the GDC1 and the cells
21	0x0 RW	**SRST_SF_DMA_CELLS:** soft reset bit for the FIFOs between the DMA and the cells
20	0x0 RW	**SRST_SF_ISYS_SP:** soft reset bit for the FIFOs between the input system and the SP
19	0x0 RW	**SRST_SF_MC_SP:** soft reset bit for the FIFOs between the stream2memory and the SP
18	0x0 RW	**SRST_SF_SIF_SP:** soft reset bit for the FIFOs between the secondary input formatter and the SP
17	0x0 RW	**SRST_SF_PIF_CELLS:** soft reset bit for the FIFOs between the primary input formatters and the cells
16	0x0 RW	**SRST_SF_ISP_SP:** soft reset bit for the FIFOs between SP and ISP
15	0x0 RW	**SRST_DMA:** soft reset bit for the DMA
14	0x0 RW	**SRST_SLV_GRP_BUS:** soft reset bit for the slave group bus

Bit Range	Default and Access	Field Name (ID): Description
13	0x0 RW	**SRST_ISP:** soft reset bit for the ISP (vector processor)
12	0x0 RW	**SRST_VEC_BUS:** soft reset bit for the vector bus
11	0x0 RW	**SRST_GDC2:** soft reset bit for the GDC2 block
10	0x0 RW	**SRST_GDC1:** soft reset bit for the GDC1 block
9	0x0 RW	**SRST_IFT_SEC_PIPE:** soft reset bit for the CIO pipeline after the secondary input formatter
8	0x0 RW	**SRST_OSYS:** soft reset bit for the blocks in the output system cluster
7	0x0 RW	**SRST_FACELLFIFOS:** soft reset bit for the FIFO's connected to the FIFO adapter between host and cells
6	0x0 RW	**SRST_GPTIMER:** soft reset bit for the GP timer block
5	0x0 RW	**SRST_TC:** soft reset bit for the timed controller block
4	0x0 RW	**SRST_GPIO:** soft reset bit for the GPIO block
3	0x0 RW	**SRST_GPDEV_CBUS:** soft reset bit for the gp devices cluster control bus
2	0x0 RW	**SRST_IFMT_CBUS:** soft reset bit for the input formatting cluster control bus
1	0x0 RW	**SRST_ISEL_CBUS:** soft reset bit for the input selector cluster control bus
0	0x0 RW	**SRST_ISYS_CBUS:** soft reset bit for the input system control bus

5.2.21 reg_gp_slv_reg_srst (gpd_gp_reg_reg_gp_slv_reg_srst)—Offset 50h

Soft reset for the slave accessible registers in some blocks. If '1' is written to a bit, the attached registers get their default value. They can only be overwritten after writing a '0' to this bit

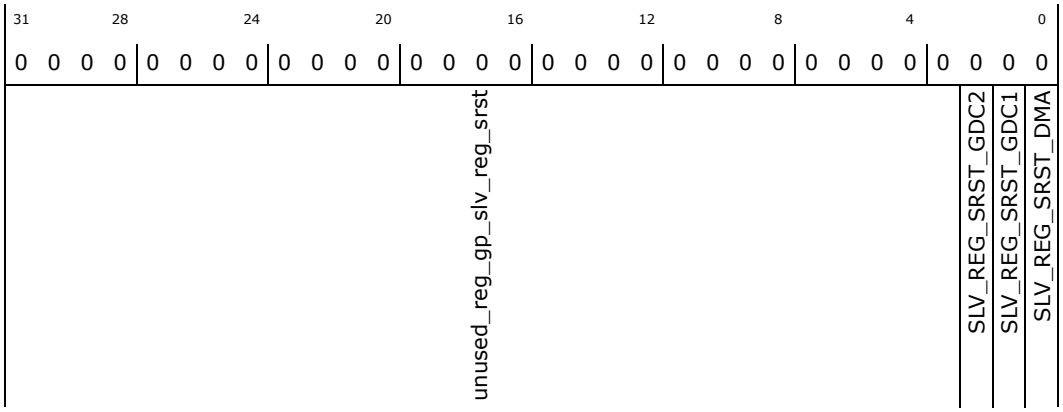
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:3	0x0 RO	**Reserved (unused_reg_gp_slv_reg_srst):** Unused
2	0x0 RW	**SLV_REG_SRST_GDC2:** soft reset bit for the slave registers in the GDC2
1	0x0 RW	**SLV_REG_SRST_GDC1:** soft reset bit for the slave registers in the GDC1
0	0x0 RW	**SLV_REG_SRST_DMA:** soft reset bit for the slave registers in the DMA

5.2.22 reg_gpd_gp_reg_reg_gp_isel_switch_type (gpd_gp_reg_reg_gp_isel_switch)—Offset 54h

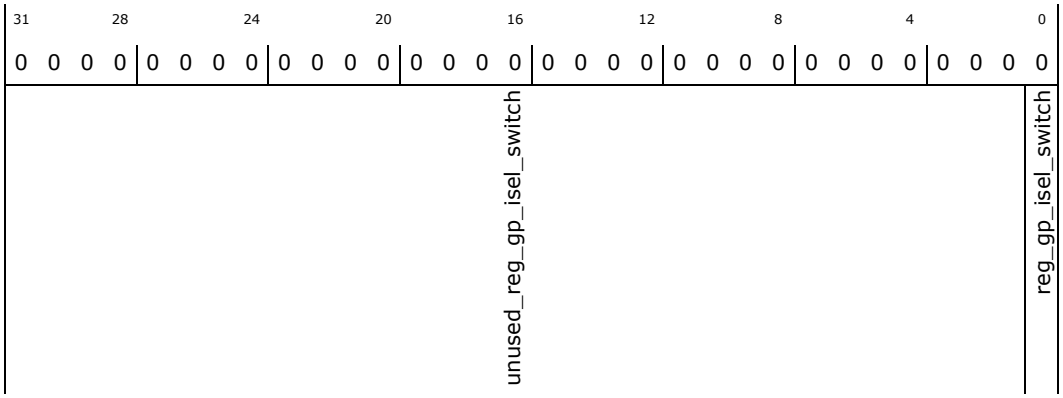
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 54h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**unused_reg_gp_isel_switch:** Unused
0	0x0 RW	**reg_gp_isel_switch:** Selects whether the legacy 2400 input system is used, value=0, or the new 2401 input system, value=1

5.2.23 FifoWriteCmd (gpd_tc_FifoWriteCmd)—Offset 100h

Timed controller Command input. A Timed Controller command consists of 5 32-bit tokens that need to be written sequentially to this register location

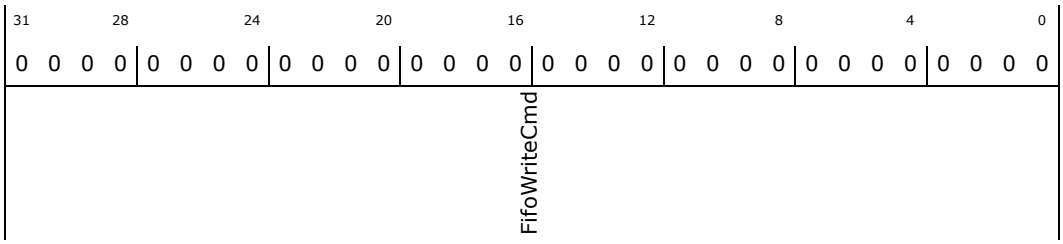
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 WO	**FifoWriteCmd:** Timed controller Command input. A Timed Controller command consists of 5 32-bit tokens that need to be written sequentially to this register location

5.2.24 reg_gpio_doe (gpd_c_gpio_reg_gpio_doe)—Offset 400h

indicates for each bit whether it is intended to be an input (value='0') or an output (value='1')

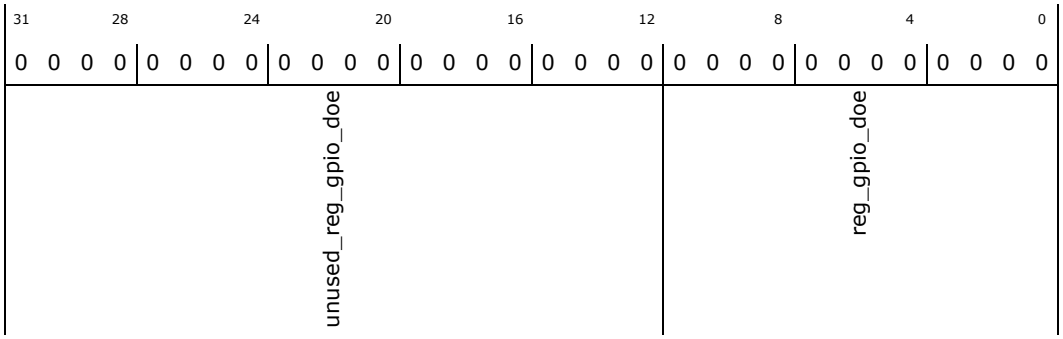
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 400h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_reg_gpio_doe):** Unused
11:0	0x0 RW	**reg_gpio_doe:** indicates for each bit whether it is intended to be an input (value='0') or an output (value='1')

5.2.25 reg_gpio_do_select (gpd_c_gpio_reg_gpio_do_select)—Offset 404h

indicates for each bit of gpio_do whether it should have the value from source 0 (value='0') or source 1 (value='1').

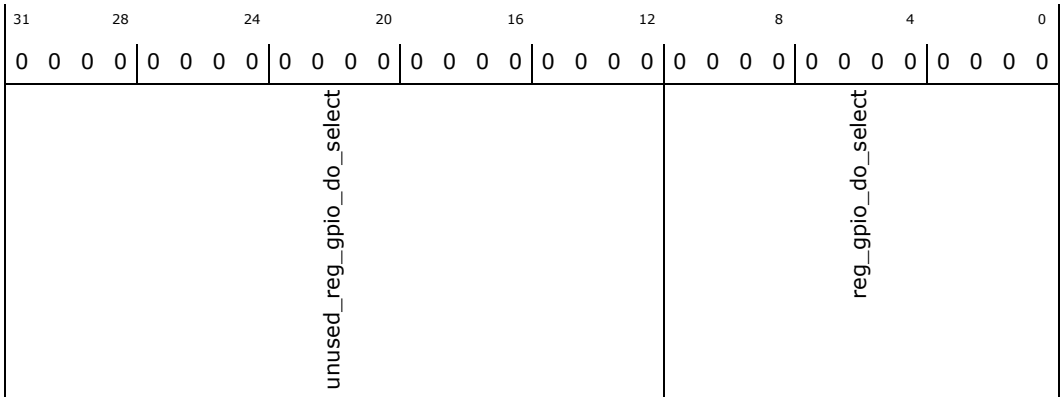
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 404h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_reg_gpio_do_select):** Unused
11:0	0x0 RW	**reg_gpio_do_select:** indicates for each bit of gpio_do whether it should have the value from source 0 (value='0') or source 1 (value='1').

5.2.26 reg_gpio_do_0 (gpd_c_gpio_reg_gpio_do_0)—Offset 408h

Provides the value for each of the output bits (source 0)

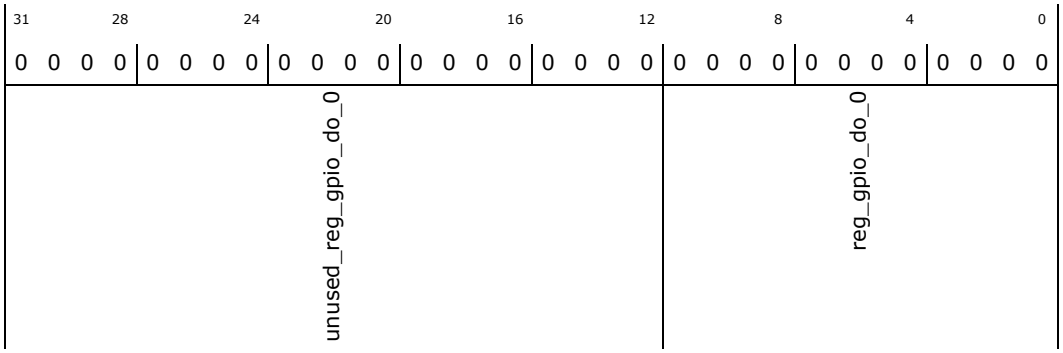
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 408h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_reg_gpio_do_0):** Unused
11:0	0x0 RW	**reg_gpio_do_0:** provides the value for each of the output bits (source 0)

5.2.27 reg_gpio_do_1 (gpd_c_gpio_reg_gpio_do_1)—Offset 40Ch

Provides the value for each of the output bits (source 1)

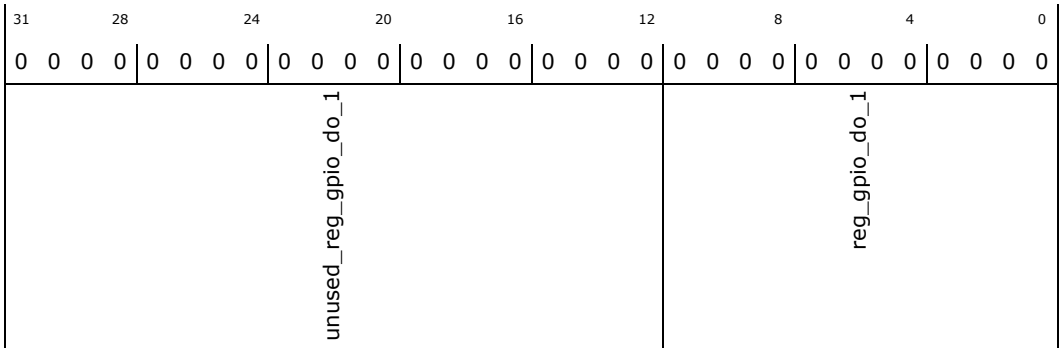
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 40Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_reg_gpio_do_1):** Unused

Bit Range	Default and Access	Field Name (ID): Description
11:0	0x0 RW	**reg_gpio_do_1:** provides the value for each of the output bits (source 1)

5.2.28 reg_gpio_do_pwm_cnt_0 (gpd_c_gpio_reg_gpio_do_pwm_cnt_0)—Offset 410h

indicates duty cycle for PWM output 0. value d means duty cycle d/64

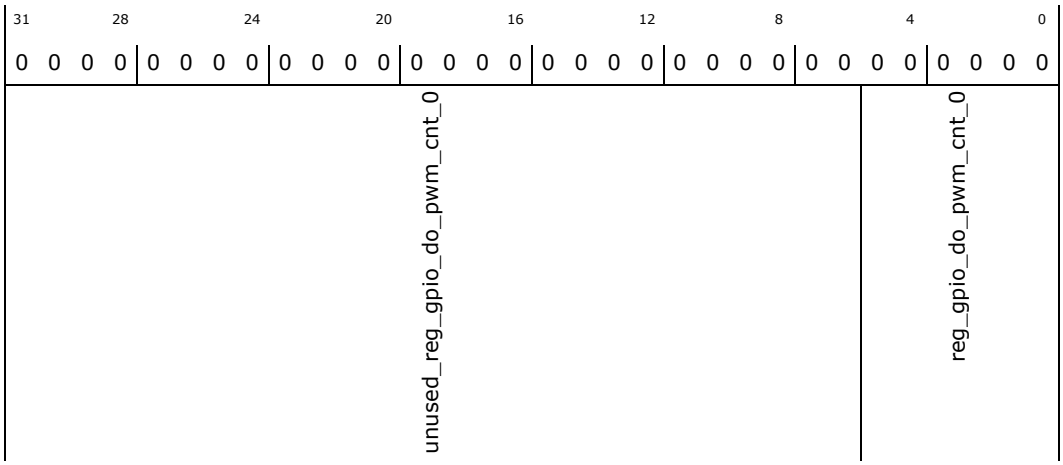
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 410h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_reg_gpio_do_pwm_cnt_0):** Unused
5:0	0x0 RW	**reg_gpio_do_pwm_cnt_0:** indicates duty cycle for PWM output 0. value d means duty cycle d/64

5.2.29 reg_gpio_do_pwm_cnt_1 (gpd_c_gpio_reg_gpio_do_pwm_cnt_1)—Offset 414h

Indicates duty cycle for PWM output 1. Value d means duty cycle d/64.

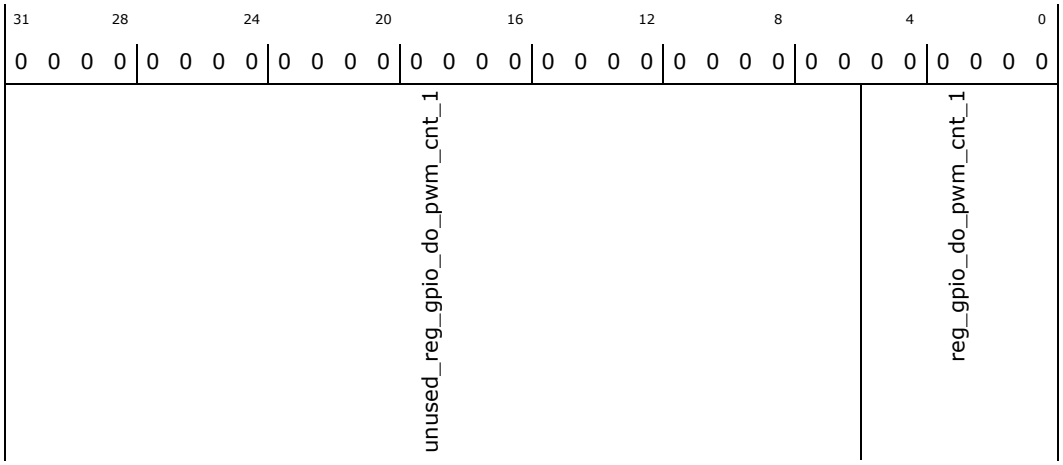
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 414h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_reg_gpio_do_pwm_cnt_1):** Unused
5:0	0x0 RW	**reg_gpio_do_pwm_cnt_1:** indicates duty cycle for PWM output 1. value d means duty cycle d/64

5.2.30 reg_gpio_do_pwm_cnt_2 (gpd_c_gpio_reg_gpio_do_pwm_cnt_2)—Offset 418h

Indicates duty cycle for PWM output 2. Value d means duty cycle d/64.

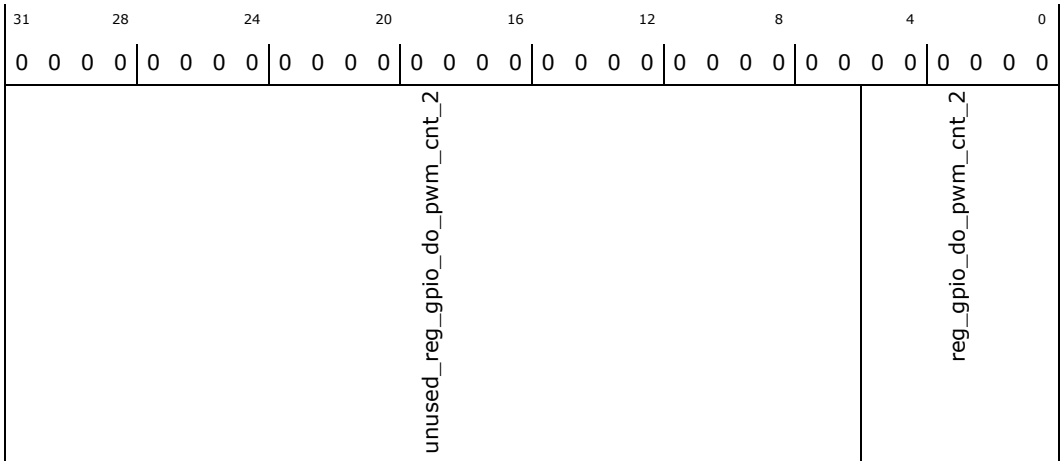
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 418h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_reg_gpio_do_pwm_cnt_2):** Unused
5:0	0x0 RW	**reg_gpio_do_pwm_cnt_2:** indicates duty cycle for PWM output 2. Value d means duty cycle d/64.

5.2.31 reg_gpio_do_pwm_cnt_3 (gpd_c_gpio_reg_gpio_do_pwm_cnt_3)—Offset 41Ch

Indicates duty cycle for PWM output 3. Value d means duty cycle d/64

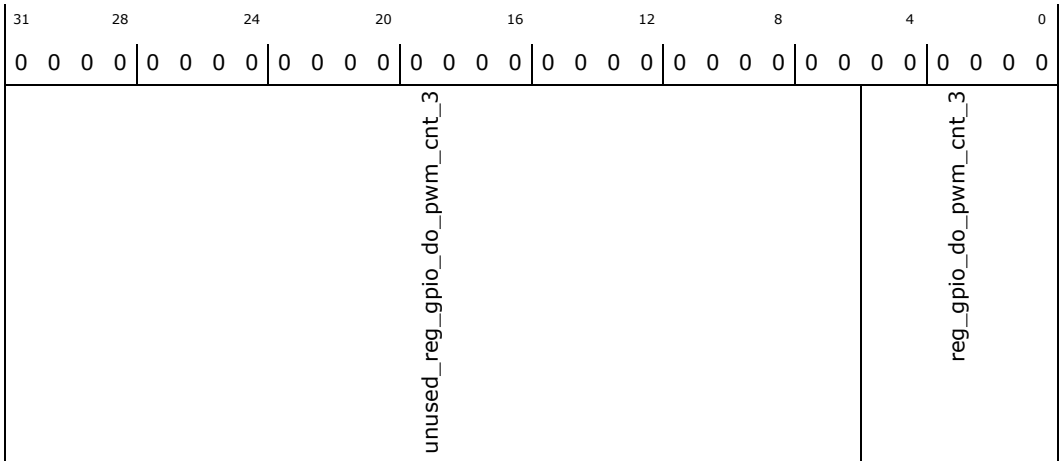
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_reg_gpio_do_pwm_cnt_3):** Unused
5:0	0x0 RW	**reg_gpio_do_pwm_cnt_3:** indicates duty cycle for PWM output 3. value d means duty cycle d/64

5.2.32 reg_gpio_do_pwm_main_cnt (gpd_c_gpio_reg_gpio_do_pwm_main_cnt)—Offset 420h

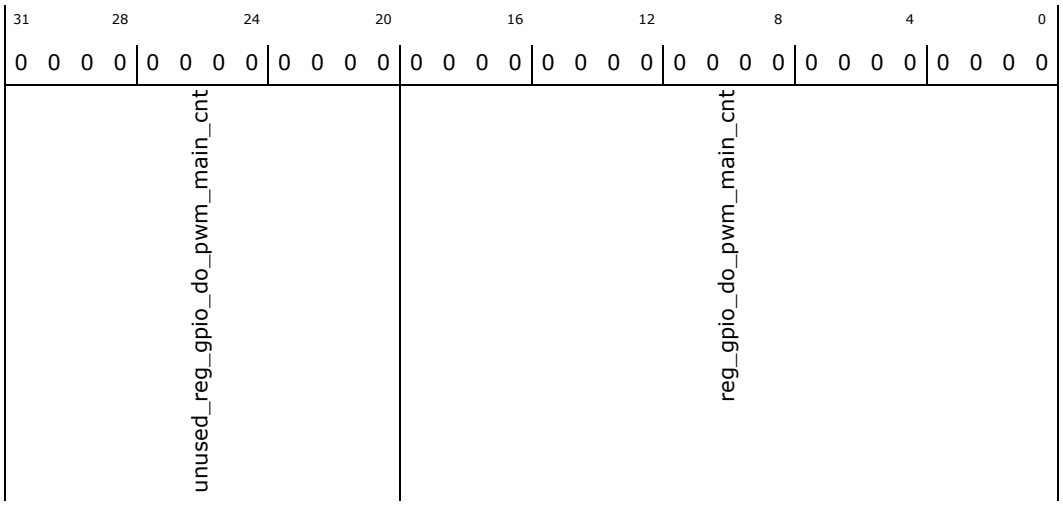
Indicates wrapping value for PWM main counter.**Access Method**

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 420h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:20	0x0 RW	**Reserved (unused_reg_gpio_do_pwm_main_cnt):** Unused
19:0	0x0 RW	**reg_gpio_do_pwm_main_cnt:** indicates wrapping value for PWM main counter

5.2.33 reg_gpio_do_pwm_enable (gpd_c_gpio_reg_gpio_do_pwm_enable)—Offset 424h

Indicates per bit whether PWM is on (value='1') or output is fixed '0' (value='0').

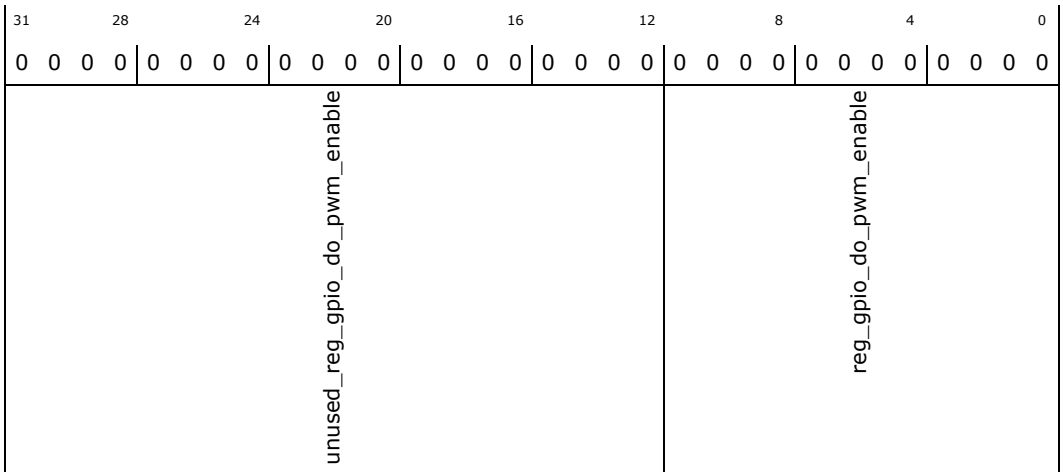
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 424h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_reg_gpio_do_pwm_enable):** Unused
11:0	0x0 RW	**reg_gpio_do_pwm_enable:** indicates per bit whether PWM is on (value='1') or output is fixed '0' (value='0')

5.2.34 reg_gpio_di_debouncemethod (gpd_c_gpio_reg_gpio_di_debouncemethod)—Offset 428h

Indicates for each input bit which debouncing counter value is chosen: '00': debounce_cnt0, '01': debounce_cnt1, '10': debounce_cnt2, '11': debounce_cnt3'

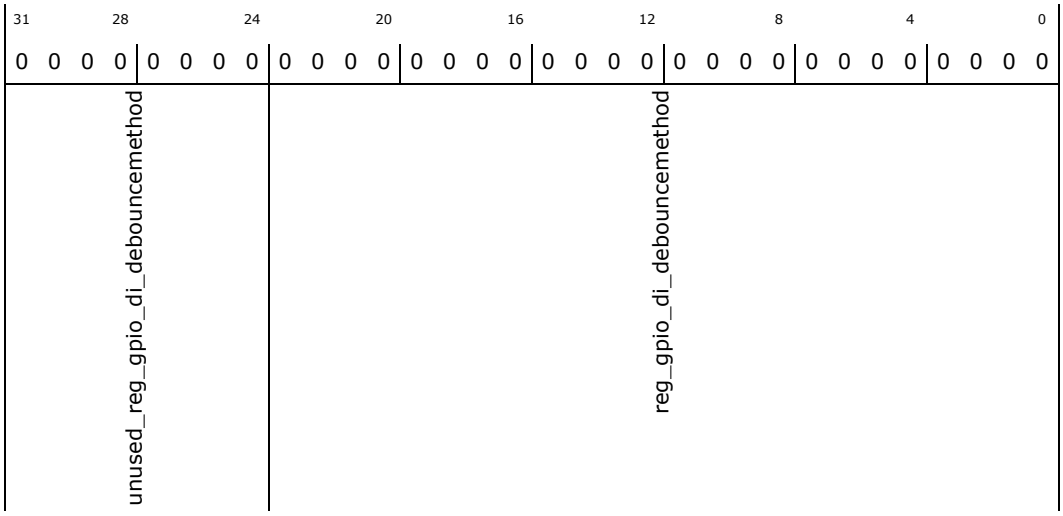
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 428h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved (unused_reg_gpio_di_debouncemethod):** Unused
23:0	0x0 RW	**reg_gpio_di_debouncemethod:** indicates for each input bit which debouncing counter value is chosen: '00': debounce_cnt0, '01': debounce_cnt1, '10': debounce_cnt2, '11': debounce_cnt3'

5.2.35 reg_gpio_di_debounce_cnt0 (gpd_c_gpio_reg_gpio_di_debounce_cnt0)—Offset 42Ch

Indicates the period an input has to be stable before passing its value to the output*.

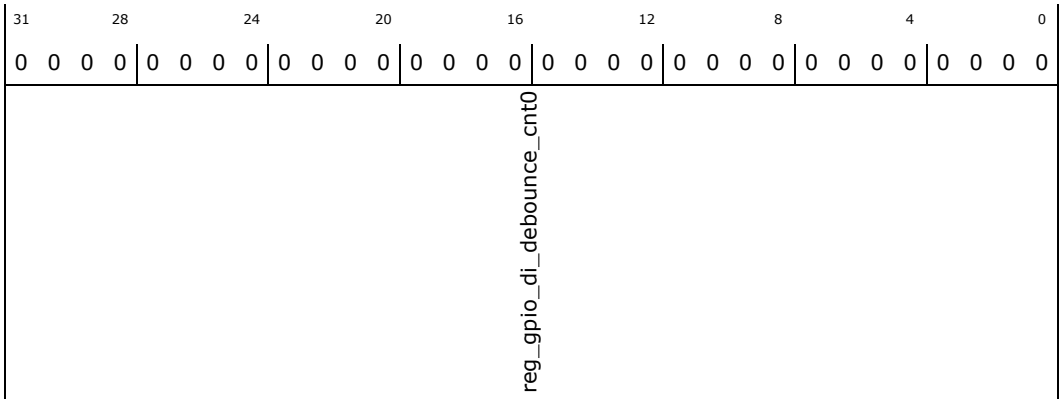
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**reg_gpio_di_debounce_cnt0:** Indicates the period an input has to be stable before passing its value to the output*

5.2.36 reg_gpio_di_debounce_cnt1 (gpd_c_gpio_reg_gpio_di_debounce_cnt1)—Offset 430h

Indicates the period an input has to be stable before passing its value to the output*.

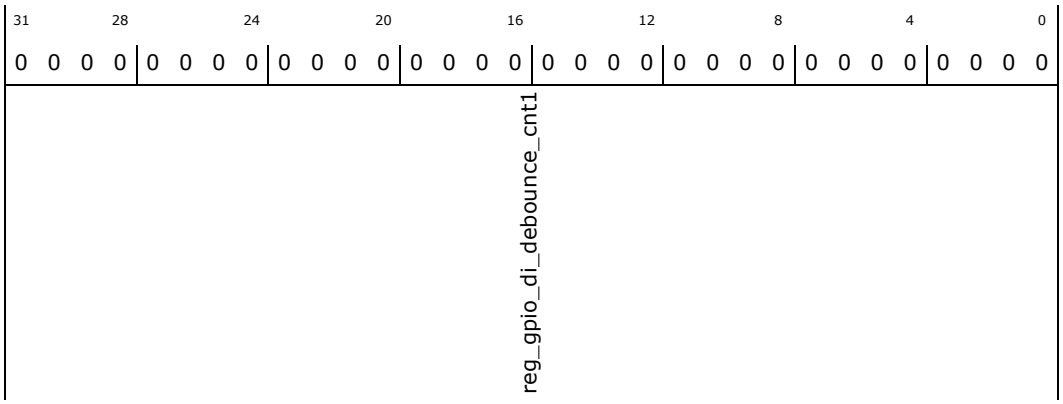
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 430h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**reg_gpio_di_debounce_cnt1:** Indicates the period an input has to be stable before passing its value to the output*

5.2.37 reg_gpio_di_debounce_cnt2 (gpd_c_gpio_reg_gpio_di_debounce_cnt2)—Offset 434h

Indicates the period an input has to be stable before passing its value to the output.

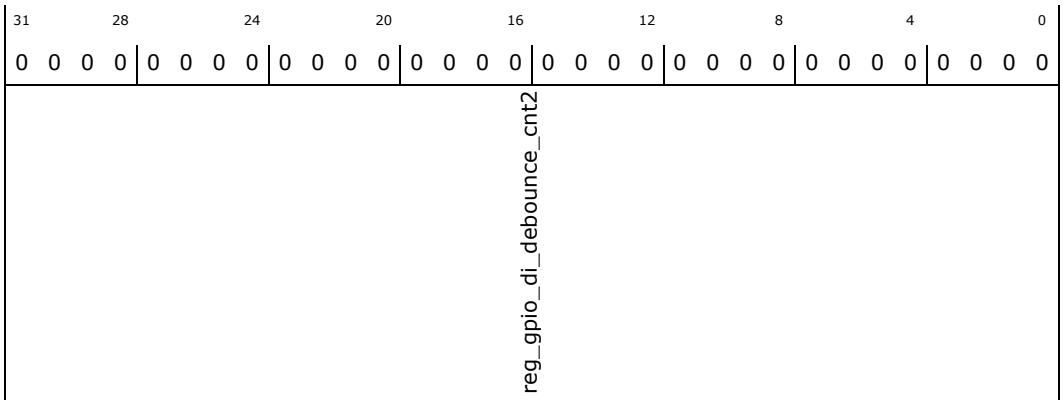
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 434h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**reg_gpio_di_debounce_cnt2:** Indicates the period an input has to be stable before passing its value to the output

5.2.38 reg_gpio_di_debounce_cnt3 (gpd_c_gpio_reg_gpio_di_debounce_cnt3)—Offset 438h

Indicates the period an input has to be stable before passing its value to the output

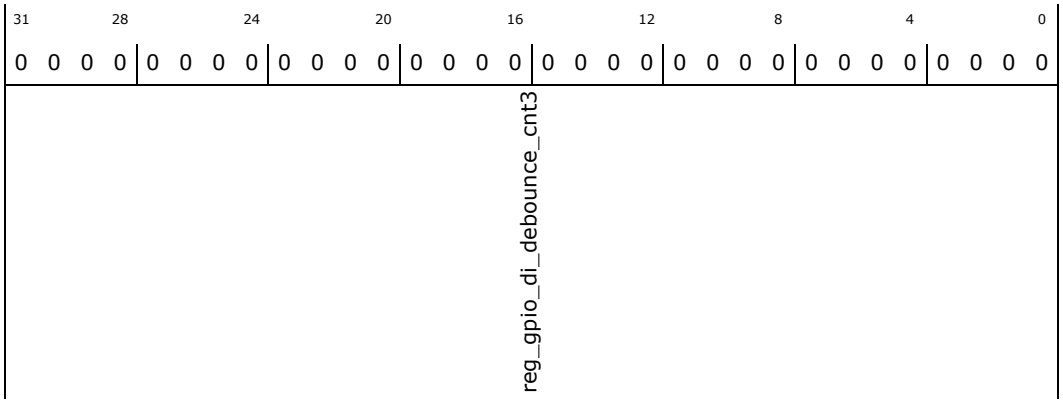
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 438h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**reg_gpio_di_debounce_cnt3:** Indicates the period an input has to be stable before passing its value to the output

5.2.39 reg_gpio_di_activelevel (gpd_c_gpio_reg_gpio_di_activelevel)—Offset 43Ch

Indicates for each bit whether it is intended to be active low (value='0') or active high (value='1').

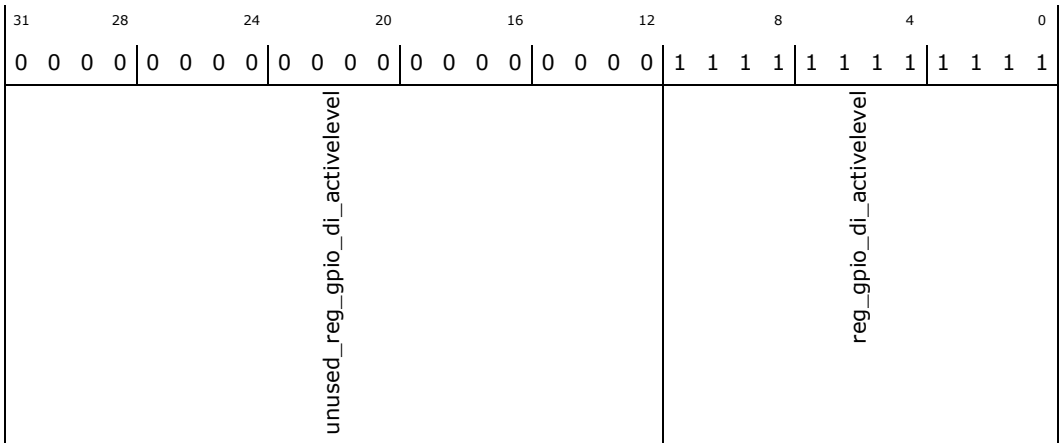
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 43Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000FFFh



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_reg_gpio_di_activelevel):** Unused
11:0	0xfff RW	**reg_gpio_di_activelevel:** indicates for each bit whether it is intended to be active low (value='0') or active high (value='1').

5.2.40 reg_gpio_di (gpd_c_gpio_reg_gpio_di)—Offset 440h

Contains the values of all debounced, active level compensated inputs

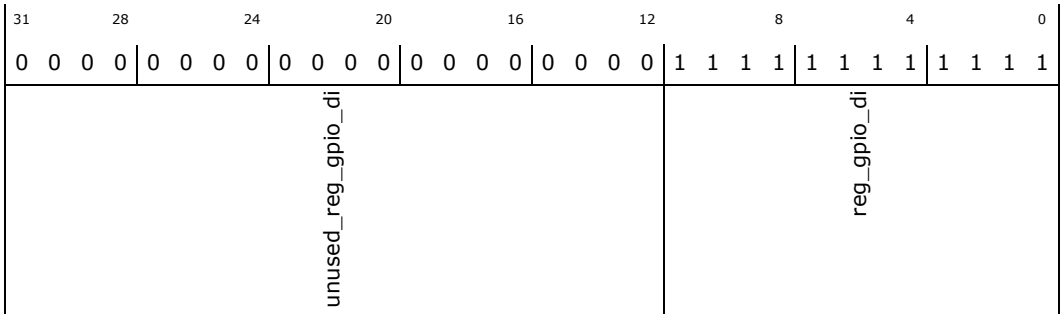
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 440h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000FFFh



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_reg_gpio_di):** Unused
11:0	0xfff RO	**reg_gpio_di:** contains the values of all debounced, active level compensated inputs

5.2.41 reg_irq_edge (gpd_irq_ctrl_reg_irq_edge)—Offset 500h

indicates for each bit whether an interrupt request should be generated on a falling edge (value='0') or a rising edge (value='1').

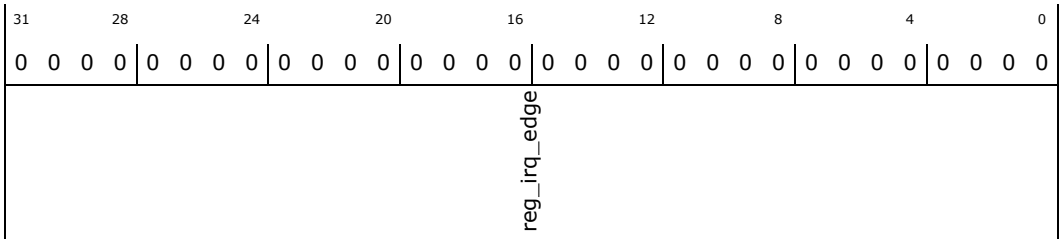
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 500h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**reg_irq_edge:** indicates for each bit whether an interrupt request should be generated on a falling edge (value='0') or a rising edge (value='1').

5.2.42 reg_irq_mask (gpd_irq_ctrl_reg_irq_mask)—Offset 504h

Indicates for each bit of irq_di whether it can generate an interrupt request (value='1') or not (value='0'). Setting will affect reg_irq_value as well as IRQ output pin

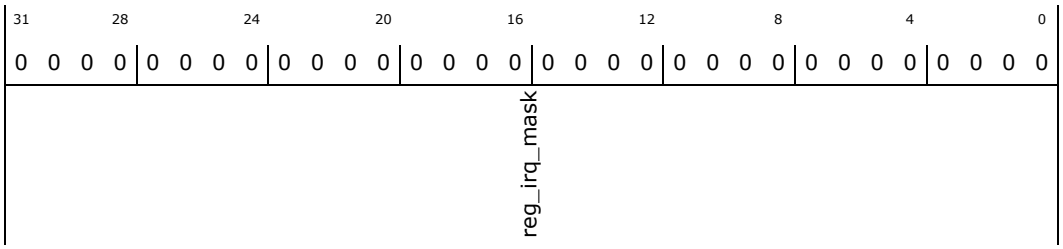
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 504h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**reg_irq_mask:** indicates for each bit of irq_di whether it can generate an interrupt request (value='1') or not (value='0'). Setting will affect reg_irq_value as well as IRQ output pin

5.2.43 reg_irq_status (gpd_irq_ctrl_reg_irq_status)—Offset 508h

Indicates for each bit whether a non-masked interrupt has been generated (value='1'). Can be cleared by writing a '1' into the corresponding bit of the req_irq_clear register.

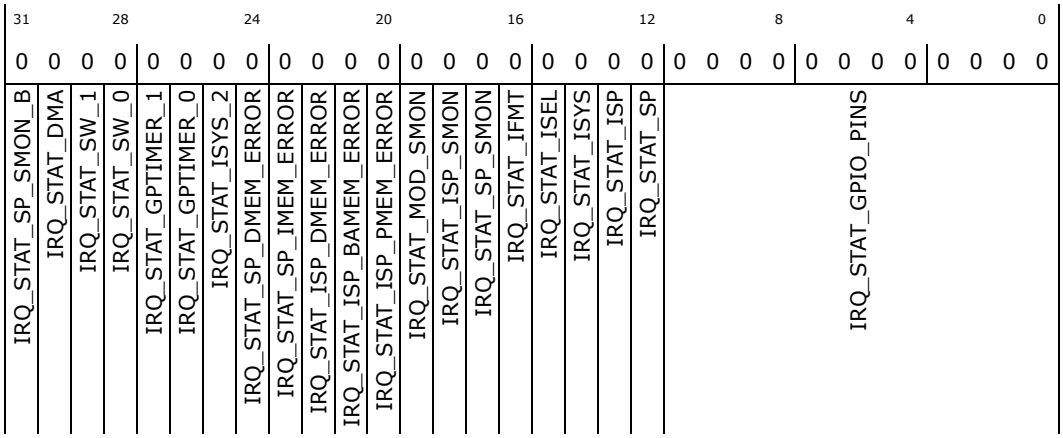
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 508h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RO	**IRQ_STAT_SP_SMON_B:** Represents the IRQ status of the irq_out from the SP streaming monitor b
30	0x0 RO	**IRQ_STAT_DMA:** Represents the IRQ status of the DMA
29	0x0 RO	**IRQ_STAT_SW_1:** Represents the IRQ status of the GP register IRQ SW 1
28	0x0 RO	**IRQ_STAT_SW_0:** Represents the IRQ status of the GP register IRQ SW 0
27	0x0 RO	**IRQ_STAT_GPTIMER_1:** Represents the IRQ status of the IRQ[1] out signal from the GP Timer block
26	0x0 RO	**IRQ_STAT_GPTIMER_0:** Represents the IRQ status of the IRQ[0] out signal from the GP Timer block
25	0x0 RO	**IRQ_STAT_ISYS_2:** Represents the IRQ status of the IRQ out signal from the input system
24	0x0 RO	**IRQ_STAT_SP_DMEM_ERROR:** Represents the IRQ status of the error signal from the SP data memory
23	0x0 RO	**IRQ_STAT_SP_IMEM_ERROR:** Represents the IRQ status of the error signal from the SP instruction cache memory
22	0x0 RO	**IRQ_STAT_ISP_DMEM_ERROR:** Represents the IRQ status of the error signal from the ISP data memory
21	0x0 RO	**IRQ_STAT_ISP_BAMEM_ERROR:** Represents the IRQ status of the error signal from the ISP vector memory
20	0x0 RO	**IRQ_STAT_ISP_PMEM_ERROR:** Represents the IRQ status of the error signal from the ISP program memory

Bit Range	Default and Access	Field Name (ID): Description
19	0x0 RO	**IRQ_STAT_MOD_SMON:** Represents the IRQ status of the irq_out from the MOD streaming monitor
18	0x0 RO	**IRQ_STAT_ISP_SMON:** Represents the IRQ status of the irq_out from the ISP streaming monitor
17	0x0 RO	**IRQ_STAT_SP_SMON:** Represents the IRQ status of the irq_out from the SP streaming monitor
16	0x0 RO	**IRQ_STAT_IFMT:** Represents the IRQ status of the irq_out from the input formatting subsystem
15	0x0 RO	**IRQ_STAT_ISEL:** Represents the IRQ status of the irq_out from the input selector
14	0x0 RO	**IRQ_STAT_ISYS:** Represents the IRQ status of the irq_out from the input system
13	0x0 RO	**IRQ_STAT_ISP:** Represents the IRQ status of the irq_out from isp2300
12	0x0 RO	**IRQ_STAT_SP:** Represents the IRQ status of the irq_out from scalar processor
11:0	0x0 RO	**IRQ_STAT_GPIO_PINS:** Represents the IRQ status of the - potentially debounced - GPIO input pins

5.2.44 reg_irq_clear (gpd_irq_ctrl_reg_irq_clear)—Offset 50Ch

Clears (set to '0') bits in reg_irq_status. When writing a '1' into a bit of this register, the corresponding bit in the req_irq_status is cleared. When writing a '0' into a bit of this register, the corresponding bit in the req_irq_status is not affected.

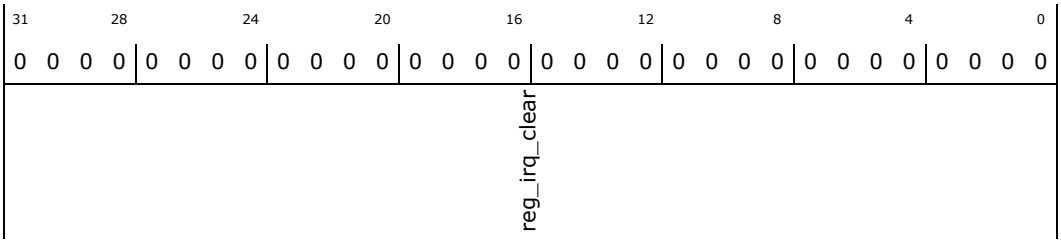
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 WO	**reg_irq_clear:** Clears (set to '0') bits in reg_irq_status. When writing a '1' into a bit of this register, the corresponding bit in the req_irq_status is cleared. When writing a '0' into a bit of this register, the corresponding bit in the req_irq_status is not affected.

5.2.45 reg_irq_enable (gpd_irq_ctrl_reg_irq_enable)—Offset 510h

Indicates for each bit whether an interrupt cause as monitored by the req_irq_status register also affects the IRQ pin (value='1') or not (value='0')

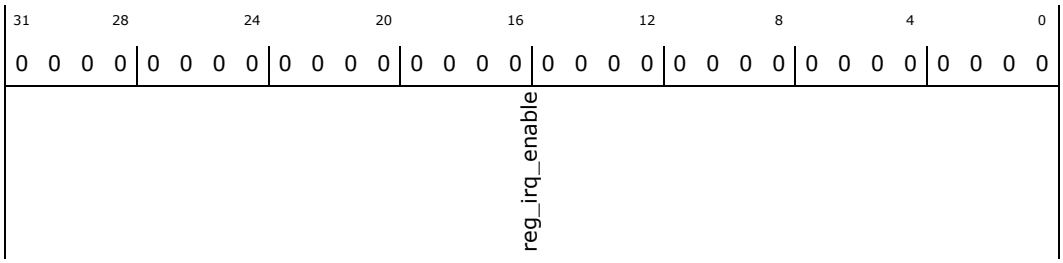
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 510h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**reg_irq_enable:** Indicates for each bit whether an interrupt cause as monitored by the req_irq_status register also affects the IRQ pin (value='1') or not (value='0')

5.2.46 reg_irq_level_not_pulse (gpd_irq_ctrl_reg_irq_level_not_pulse)—Offset 514h

Indicates for each bit whether an interrupt cause is translated into a pulse (value='0') or into a constant level '1' (value='1') on the IRQ pin

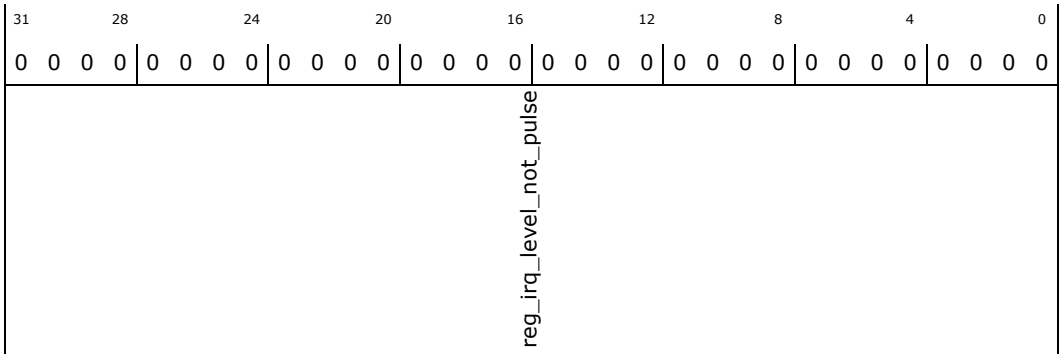
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 514h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**reg_irq_level_not_pulse:** Indicates for each bit whether an interrupt cause is translated into a pulse (value='0') or into a constant level '1' (value='1') on the IRQ pin

5.2.47 reg_irq_str_out_enable (gpd_irq_ctrl_reg_irq_str_out_enable)—Offset 518h

Indicates for each bit whether an interrupt cause as monitored by the req_irq_status register also results in a send token on the irq_str_out port (value='1') or not (value='0')

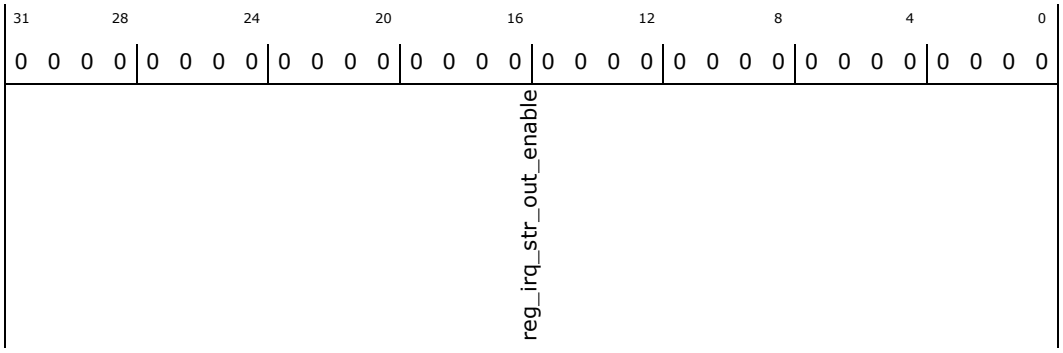
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 518h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**reg_irq_str_out_enable:** Indicates for each bit whether an interrupt cause as monitored by the req_irq_status register also results in a send token on the irq_str_out port (value='1') or not (value='0')

5.2.48 reg_reset (gpd_gptimer_reg_reset)—Offset 600h

GP Timer reset. Write '1' to bit x to reset timer x. Write 0xFF to reset all timers.

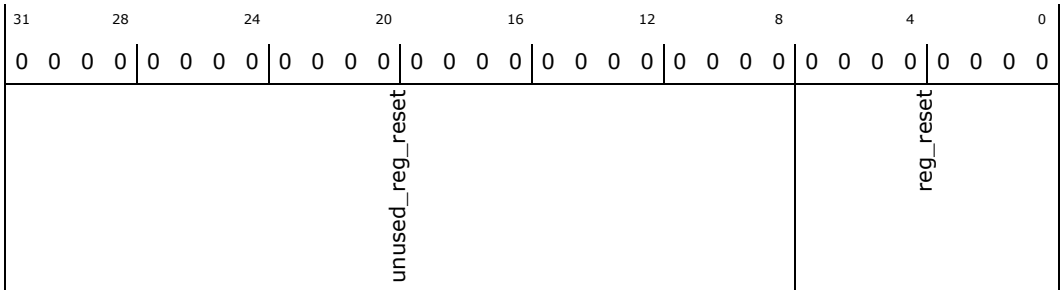
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 600h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved (unused_reg_reset):** Unused
7:0	0x0 WO	**reg_reset:** GP Timer reset. Write '1' to bit x to reset timer x. Write 0xFF to reset all timers.

5.2.49 overall_enable (gpd_gptimer_overall_enable)—Offset 604h

GP Timer enable. Write '1' to enable all enabled timers, write '0' to disable all timers.

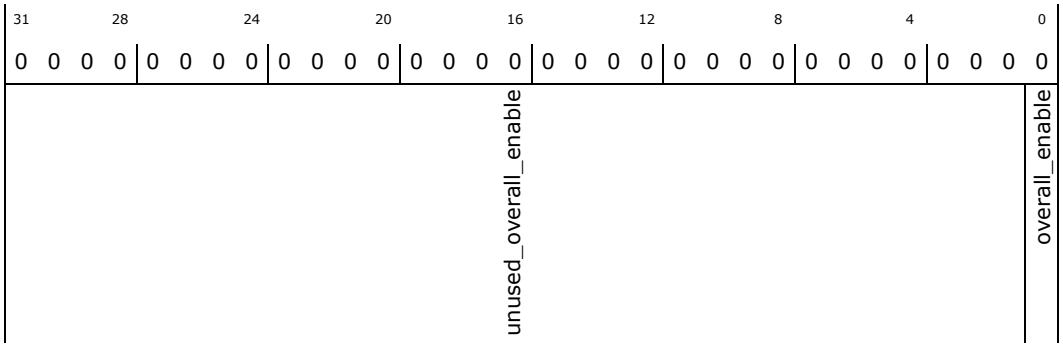
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 604h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_overall_enable):** Unused
0	0x0 RW	**overall_enable:** GP Timer enable. Write '1' to enable all enabled timers, write '0' to disable all timers.

5.2.50 enable_timer_0 (gpd_gptimer_enable_timer_0)—Offset 608h

GP Timer enable. Write '1' to enable timer 0. Write '0' to disable timer 0.

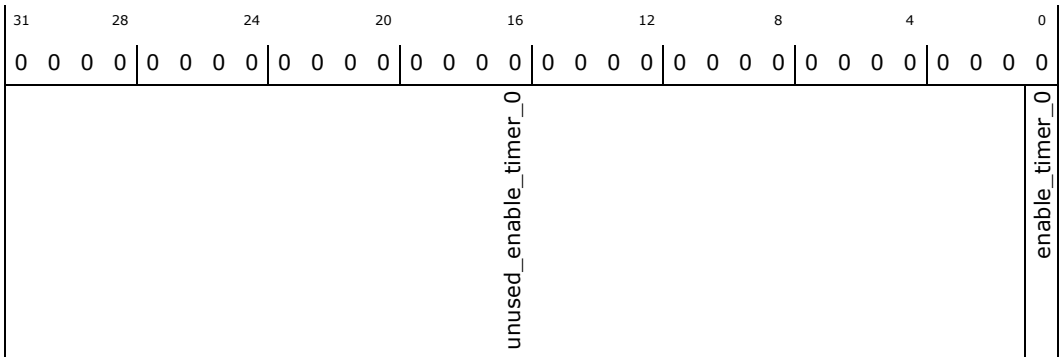
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 608h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_enable_timer_0):** Unused
0	0x0 RW	**enable_timer_0:** GP Timer enable. Write '1' to enable timer 0. Write '0' to disable timer 0

5.2.51 enable_timer_1 (gpd_gptimer_enable_timer_1)—Offset 60Ch

GP Timer enable. Write '1' to enable timer 1. Write '0' to disable timer 1.

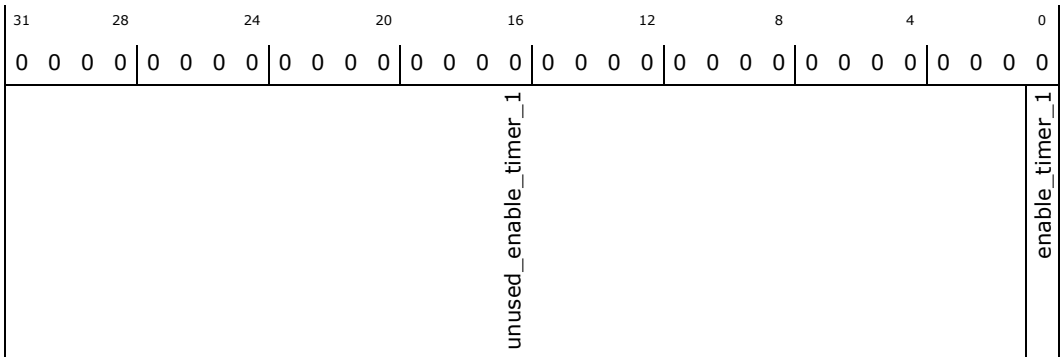
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_enable_timer_1):** Unused
0	0x0 RW	**enable_timer_1:** GP Timer enable. Write '1' to enable timer 1. Write '0' to disable timer 1

5.2.52 enable_timer_2 (gpd_gptimer_enable_timer_2)—Offset 610h

GP Timer enable. Write '1' to enable timer 2. Write '0' to disable timer 2

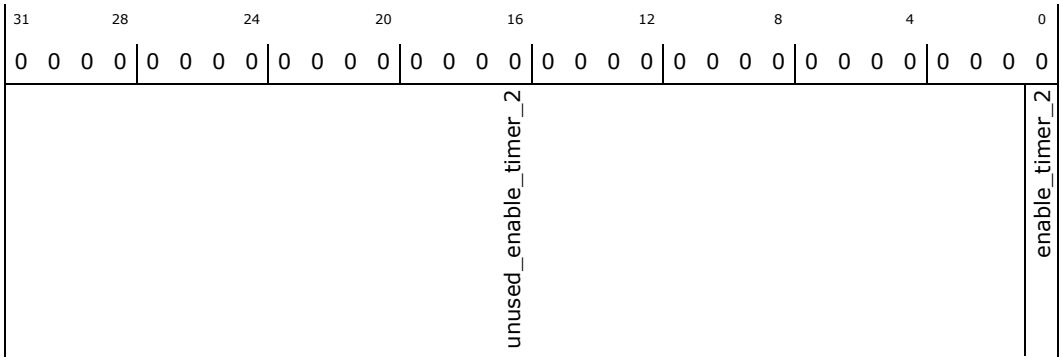
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 610h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_enable_timer_2):** Unused
0	0x0 RW	**enable_timer_2:** GP Timer enable. Write '1' to enable timer 2. Write '0' to disable timer 2

5.2.53 enable_timer_3 (gpd_gptimer_enable_timer_3)—Offset 614h

GP Timer enable. Write '1' to enable timer 3. Write '0' to disable timer 3.

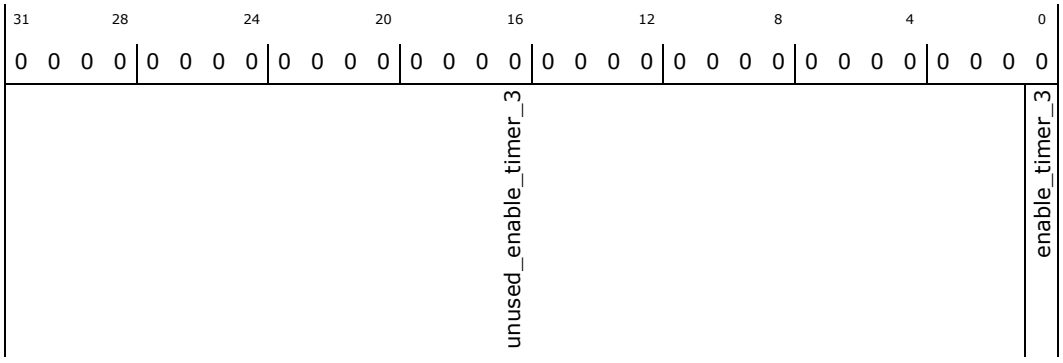
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 614h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_enable_timer_3):** Unused
0	0x0 RW	**enable_timer_3:** GP Timer enable. Write '1' to enable timer 3. Write '0' to disable timer 3

5.2.54 enable_timer_4 (gpd_gptimer_enable_timer_4)—Offset 618h

GP Timer enable. Write '1' to enable timer 4. Write '0' to disable timer 4.

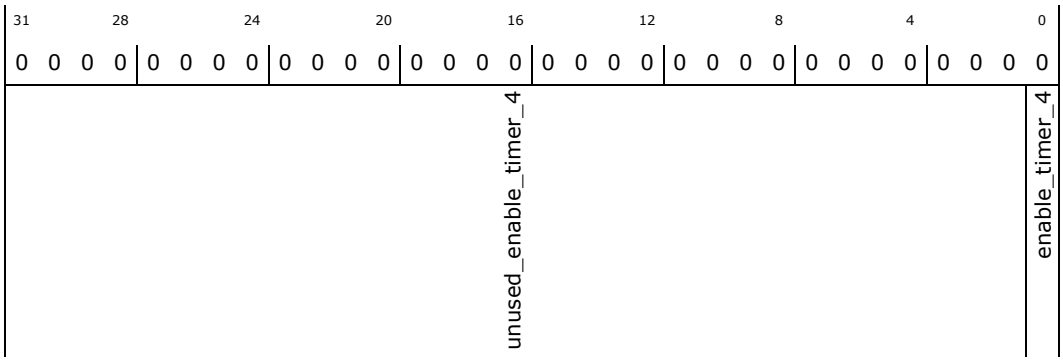
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 618h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_enable_timer_4):** Unused
0	0x0 RW	**enable_timer_4:** GP Timer enable. Write '1' to enable timer 4. Write '0' to disable timer 4

5.2.55 enable_timer_5 (gpd_gptimer_enable_timer_5)—Offset 61Ch

GP Timer enable. Write '1' to enable timer 5. Write '0' to disable timer 5.

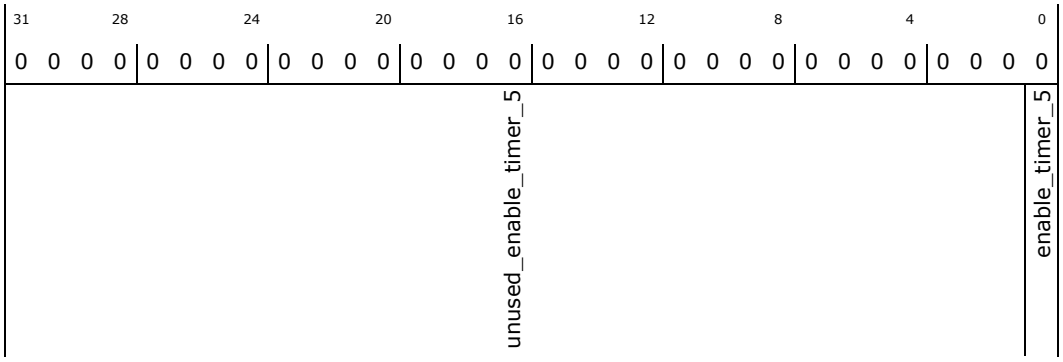
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 61Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_enable_timer_5):** Unused
0	0x0 RW	**enable_timer_5:** GP Timer enable. Write '1' to enable timer 5. Write '0' to disable timer 5

5.2.56 enable_timer_6 (gpd_gptimer_enable_timer_6)—Offset 620h

GP Timer enable. Write '1' to enable timer 6. Write '0' to disable timer 6.

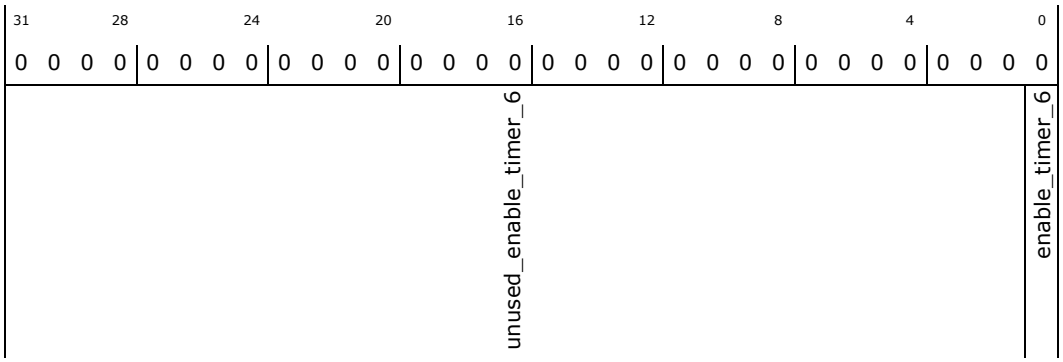
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 620h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_enable_timer_6):** Unused
0	0x0 RW	**enable_timer_6:** GP Timer enable. Write '1' to enable timer 6. Write '0' to disable timer 6

5.2.57 enable_timer_7 (gpd_gptimer_enable_timer_7)—Offset 624h

GP Timer enable. Write '1' to enable timer 7. Write '0' to disable timer 7.

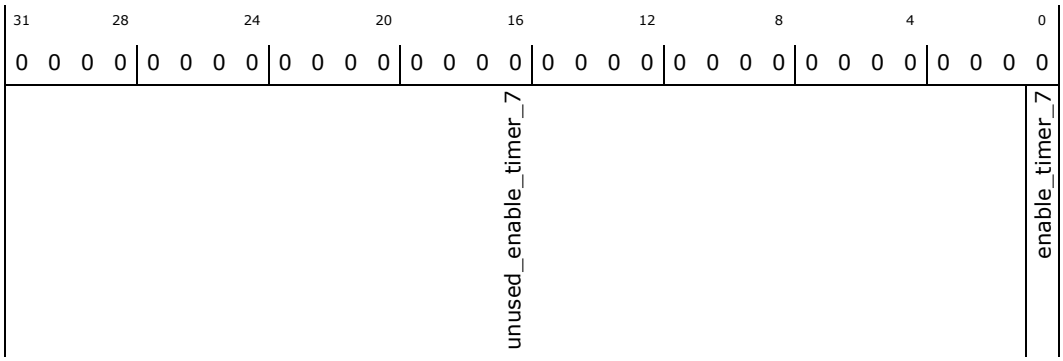
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 624h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_enable_timer_7):** Unused
0	0x0 RW	**enable_timer_7:** GP Timer enable. Write '1' to enable timer 7. Write '0' to disable timer 7

5.2.58 value_timer_0 (gpd_gptimer_value_timer_0)—Offset 628h

Returns the value of timer 0

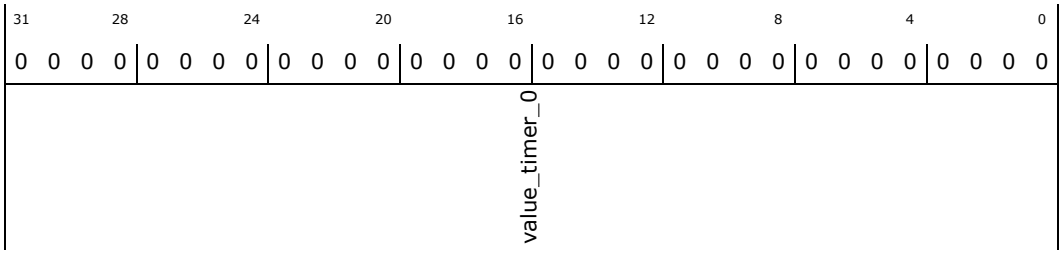
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 628h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**value_timer_0:** Returns the value of timer 0

5.2.59 value_timer_1 (gpd_gptimer_value_timer_1)—Offset 62Ch

Returns the value of timer 1.

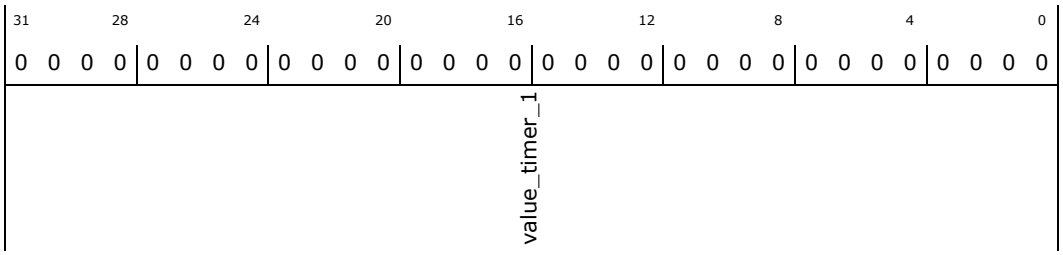
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 62Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**value_timer_1:** Returns the value of timer 1

5.2.60 value_timer_2 (gpd_gptimer_value_timer_2)—Offset 630h

Returns the value of timer 2.

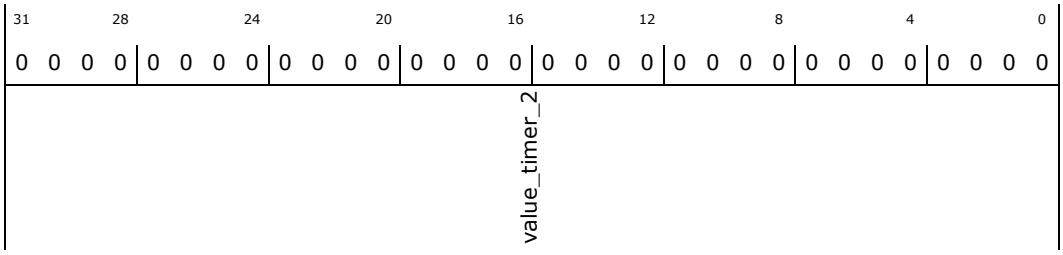
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 630h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**value_timer_2:** Returns the value of timer 2

5.2.61 value_timer_3 (gpd_gptimer_value_timer_3)—Offset 634h

Returns the value of timer 3

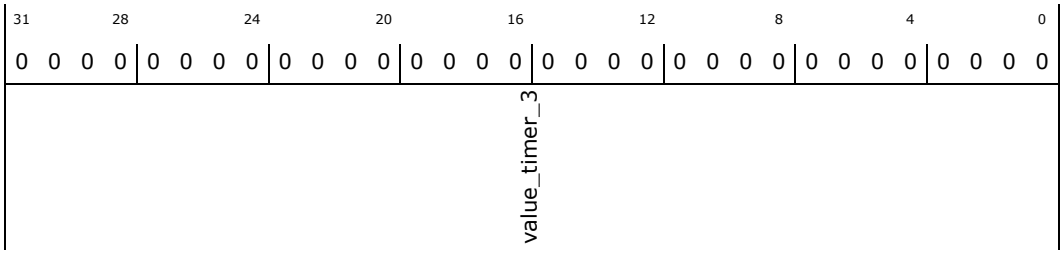
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 634h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**value_timer_3:** Returns the value of timer 3

5.2.62 value_timer_4 (gpd_gptimer_value_timer_4)—Offset 638h

Returns the value of timer 4.

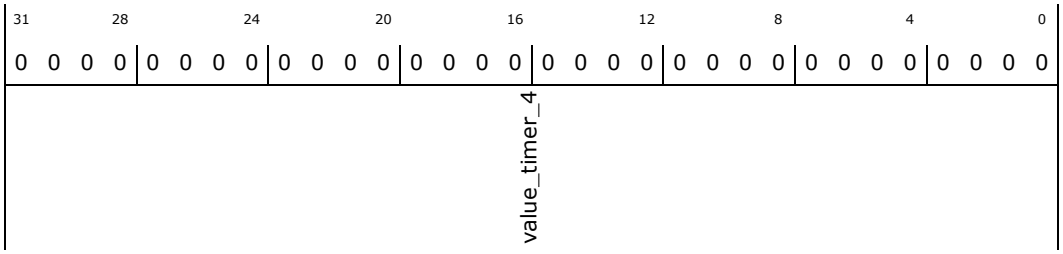
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 638h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**value_timer_4:** Returns the value of timer 4

5.2.63 value_timer_5 (gpd_gptimer_value_timer_5)—Offset 63Ch

Returns the value of timer 5

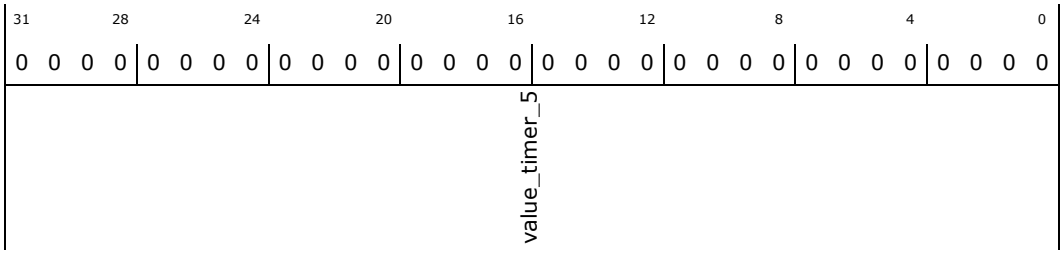
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 63Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**value_timer_5:** Returns the value of timer 5

5.2.64 value_timer_6 (gpd_gptimer_value_timer_6)—Offset 640h

Returns the value of timer 6

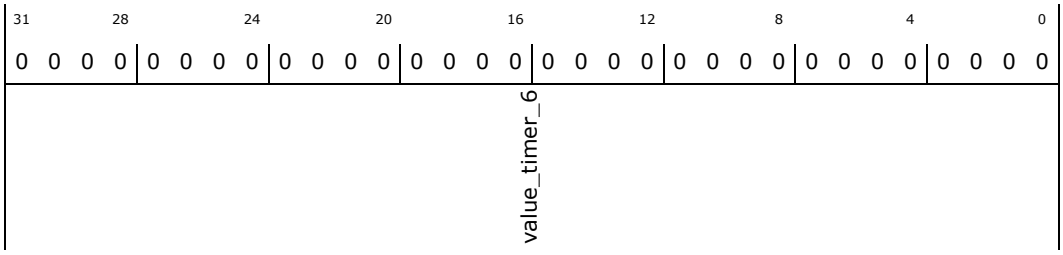
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 640h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**value_timer_6:** Returns the value of timer 6

5.2.65 value_timer_7 (gpd_gptimer_value_timer_7)—Offset 644h

Returns the value of timer 7

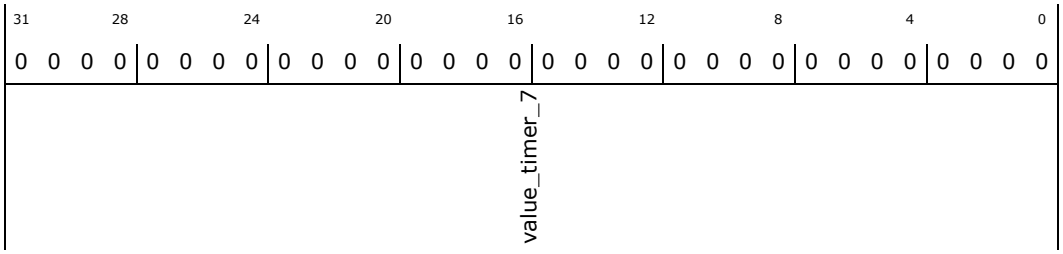
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 644h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**value_timer_7:** Returns the value of timer 7

5.2.66 count_type_timer_0 (gpd_gptimer_count_type_timer_0)—Offset 648h

Indicates what needs to be counted by timer 0, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

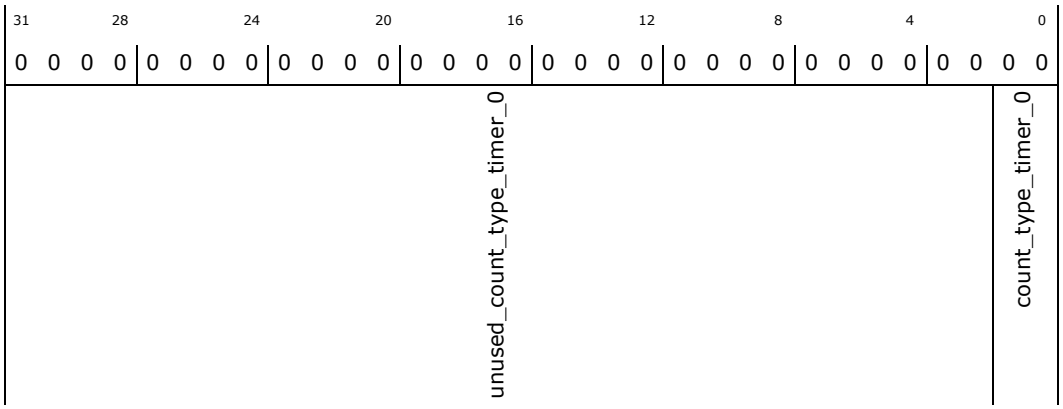
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 648h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_count_type_timer_0):** Unused
1:0	0x0 RW	**count_type_timer_0:** Indicates what needs to be counted by timer 0, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

5.2.67 count_type_timer_1 (gpd_gptimer_count_type_timer_1)—Offset 64Ch

Indicates what needs to be counted by timer 1, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

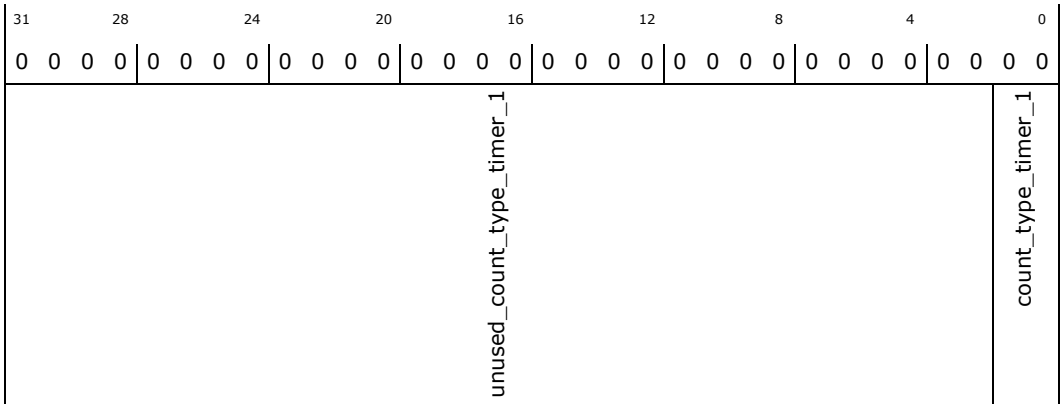
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 64Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_count_type_timer_1):** Unused
1:0	0x0 RW	**count_type_timer_1:** Indicates what needs to be counted by timer 1, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

5.2.68 count_type_timer_2 (gpd_gptimer_count_type_timer_2)—Offset 650h

Indicates what needs to be counted by timer 2, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

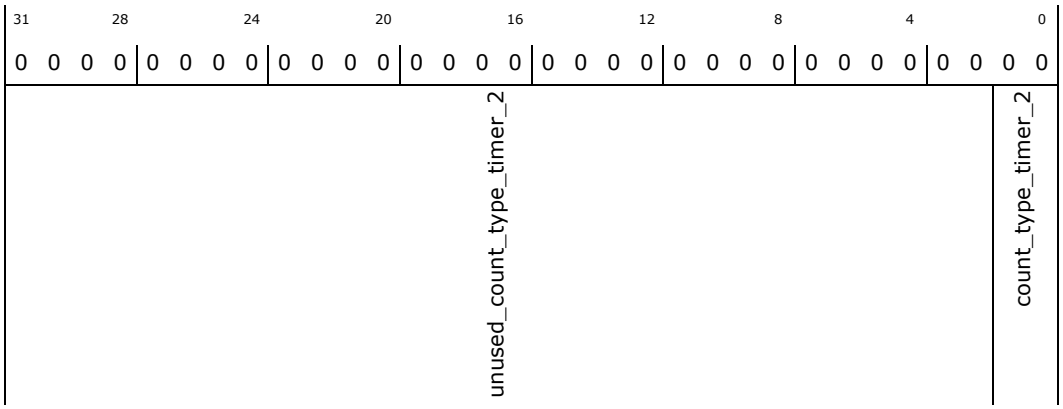
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 650h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_count_type_timer_2):** Unused
1:0	0x0 RW	**count_type_timer_2:** Indicates what needs to be counted by timer 2, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

5.2.69 count_type_timer_3 (gpd_gptimer_count_type_timer_3)—Offset 654h

Indicates what needs to be counted by timer 3, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

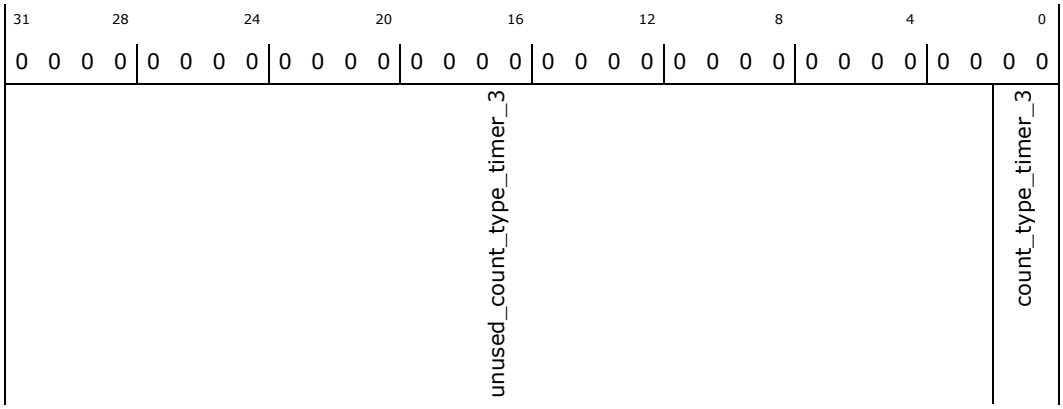
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 654h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_count_type_timer_3):** Unused
1:0	0x0 RW	**count_type_timer_3:** Indicates what needs to be counted by timer 3, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

5.2.70 count_type_timer_4 (gpd_gptimer_count_type_timer_4)—Offset 658h

Indicates what needs to be counted by timer 4, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

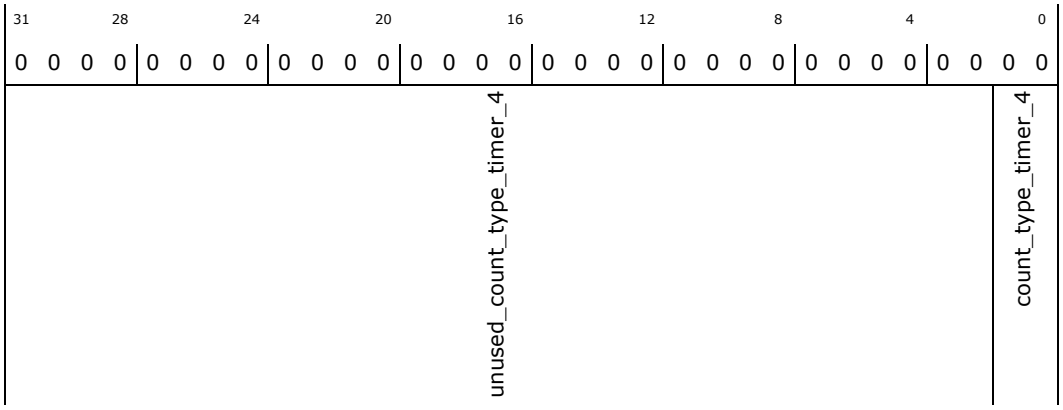
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 658h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_count_type_timer_4):** Unused
1:0	0x0 RW	**count_type_timer_4:** Indicates what needs to be counted by timer 4, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

5.2.71 count_type_timer_5 (gpd_gptimer_count_type_timer_5)—Offset 65Ch

Indicates what needs to be counted by timer 5, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

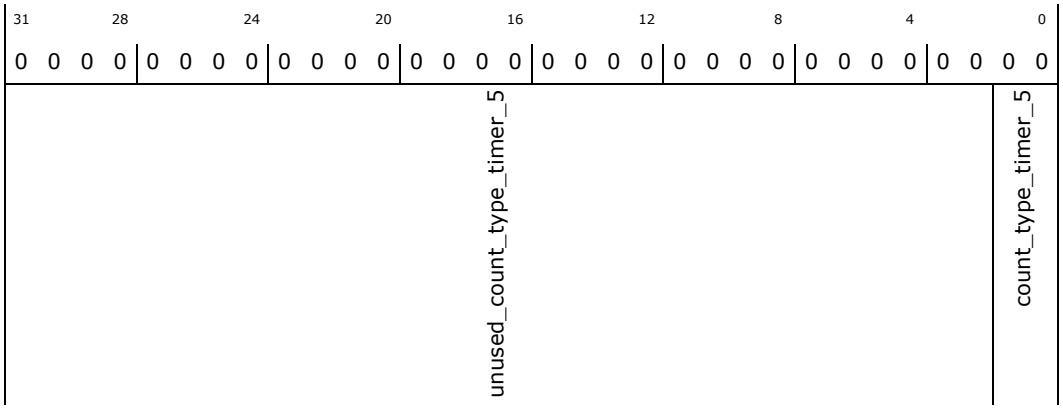
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 65Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_count_type_timer_5):** Unused
1:0	0x0 RW	**count_type_timer_5:** Indicates what needs to be counted by timer 5, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

5.2.72 count_type_timer_6 (gpd_gptimer_count_type_timer_6)—Offset 660h

Indicates what needs to be counted by timer 6, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

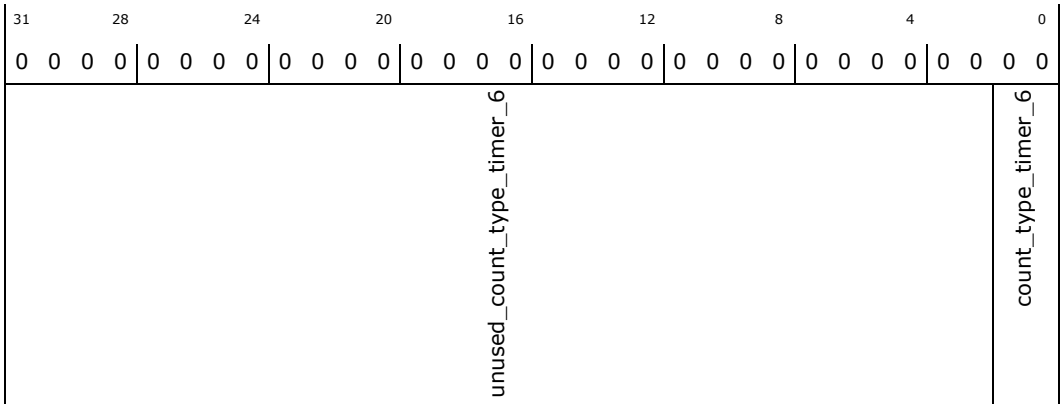
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 660h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_count_type_timer_6):** Unused
1:0	0x0 RW	**count_type_timer_6:** Indicates what needs to be counted by timer 6, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

5.2.73 count_type_timer_7 (gpd_gptimer_count_type_timer_7)—Offset 664h

Indicates what needs to be counted by timer 7, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

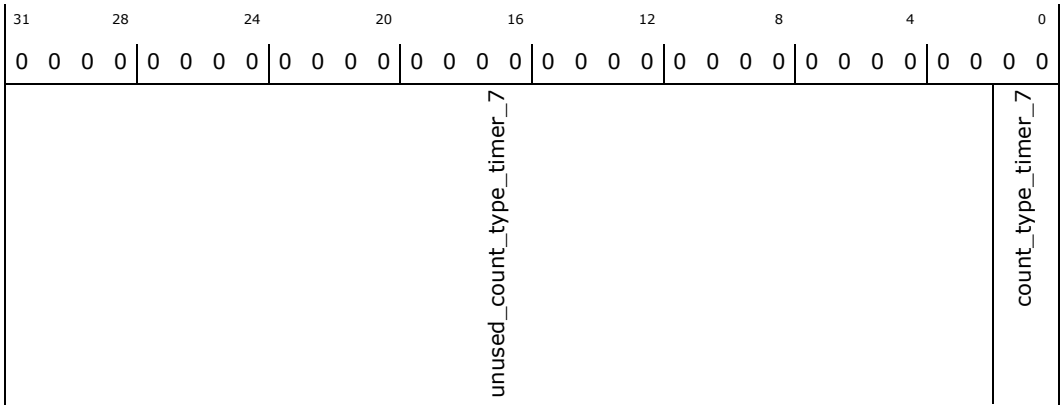
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 664h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_count_type_timer_7):** Unused
1:0	0x0 RW	**count_type_timer_7:** Indicates what needs to be counted by timer 7, 00- # cycles the signal is high (1), 01- # cycles the signal is low (0), 10- # changes from low to high, 11- # changes from high to low

5.2.74 signal_select_timer_0 (gpd_gptimer_signal_select_timer_0)—Offset 668h

Selects which of the 55 input signals are counted by timer 0

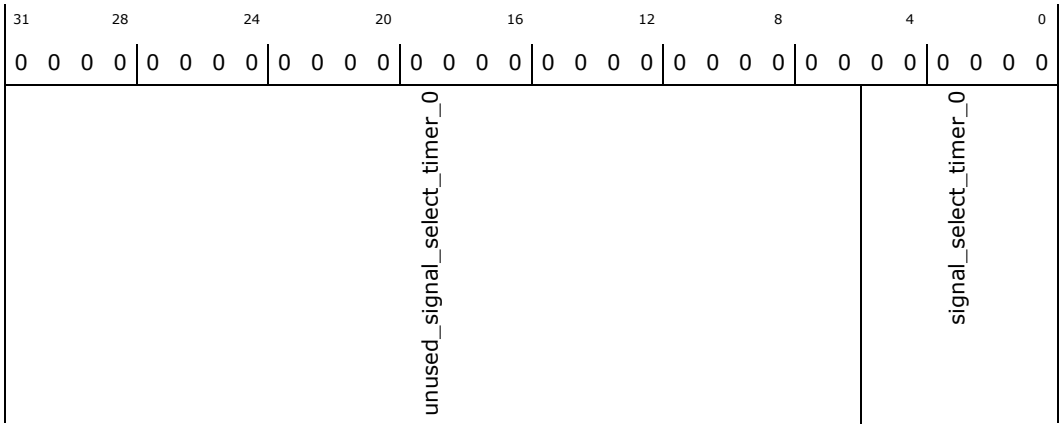
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 668h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_signal_select_timer_0):** Unused
5:0	0x0 RW	**signal_select_timer_0:** Selects which of the 55 input signals are counted by timer 0

5.2.75 signal_select_timer_1 (gpd_gptimer_signal_select_timer_1)—Offset 66Ch

Selects which of the 55 input signals are counted by timer 1

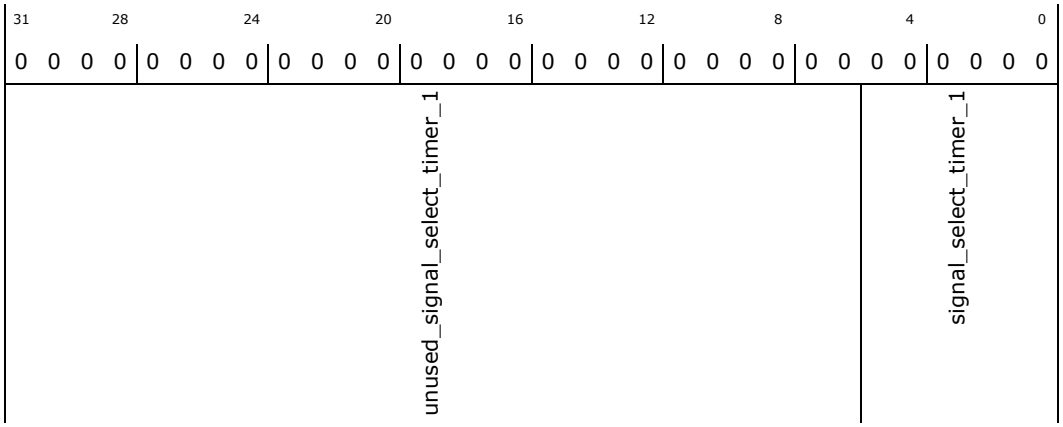
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 66Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_signal_select_timer_1):** Unused
5:0	0x0 RW	**signal_select_timer_1:** Selects which of the 55 input signals are counted by timer 1

5.2.76 signal_select_timer_2 (gpd_gptimer_signal_select_timer_2)—Offset 670h

Selects which of the 55 input signals are counted by timer 2

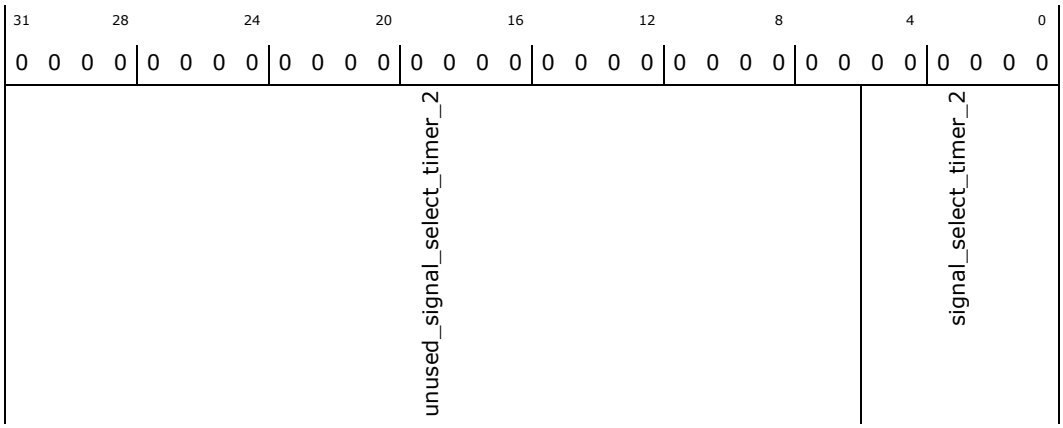
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 670h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_signal_select_timer_2):** Unused
5:0	0x0 RW	**signal_select_timer_2:** Selects which of the 55 input signals are counted by timer 2

5.2.77 signal_select_timer_3 (gpd_gptimer_signal_select_timer_3)—Offset 674h

Selects which of the 55 input signals are counted by timer 3

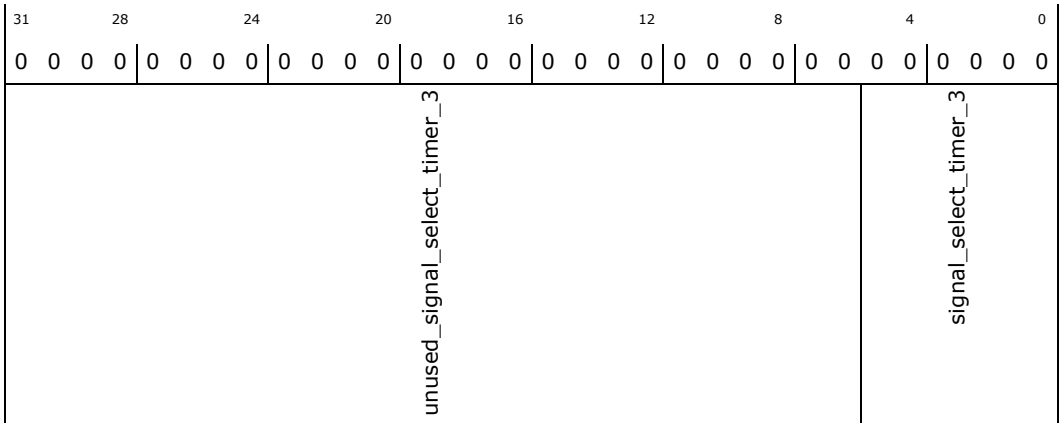
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 674h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_signal_select_timer_3):** Unused
5:0	0x0 RW	**signal_select_timer_3:** Selects which of the 55 input signals are counted by timer 3

5.2.78 signal_select_timer_4 (gpd_gptimer_signal_select_timer_4)—Offset 678h

Selects which of the 55 input signals are counted by timer 4

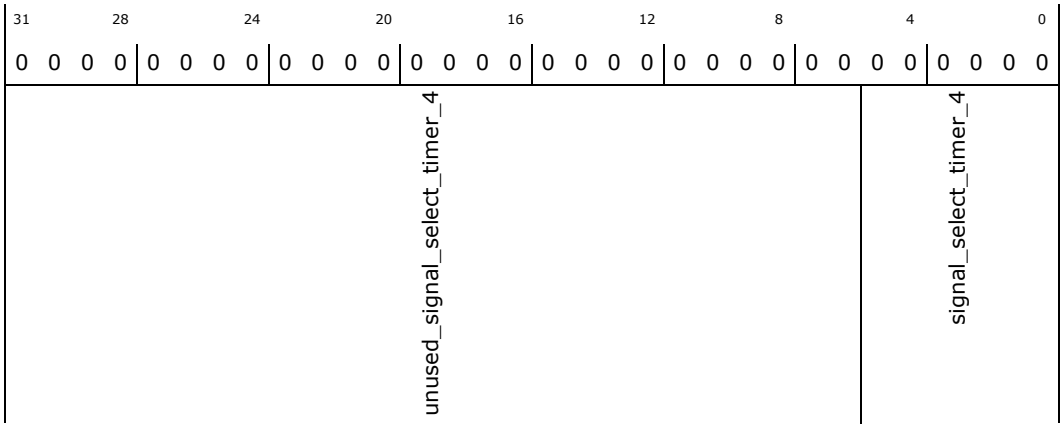
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 678h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_signal_select_timer_4):** Unused
5:0	0x0 RW	**signal_select_timer_4:** Selects which of the 55 input signals are counted by timer 4

5.2.79 signal_select_timer_5 (gpd_gptimer_signal_select_timer_5)—Offset 67Ch

Selects which of the 55 input signals are counted by timer 5

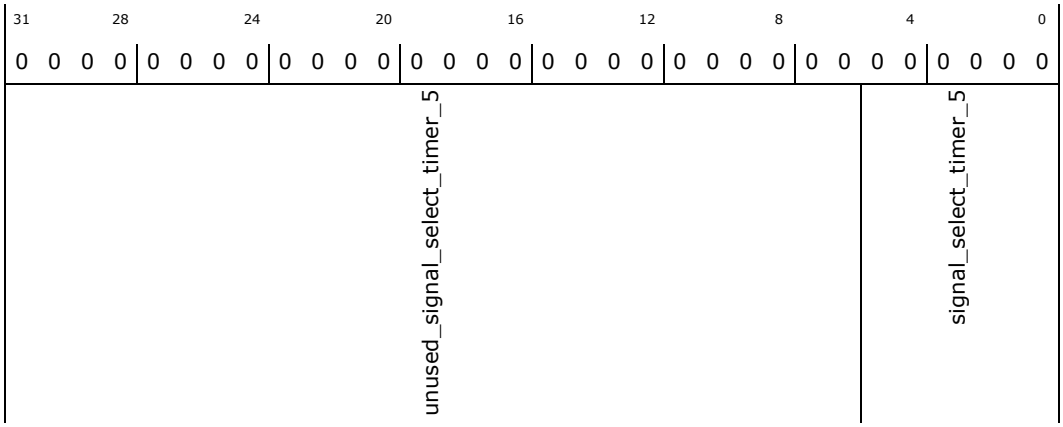
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 67Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_signal_select_timer_5):** Unused
5:0	0x0 RW	**signal_select_timer_5:** Selects which of the 55 input signals are counted by timer 5

5.2.80 signal_select_timer_6 (gpd_gptimer_signal_select_timer_6)—Offset 680h

Selects which of the 55 input signals are counted by timer 6

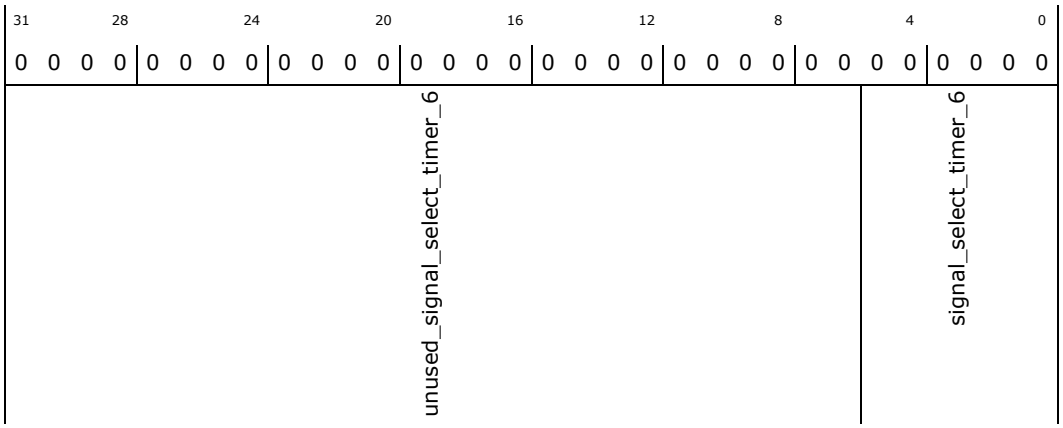
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 680h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_signal_select_timer_6):** Unused
5:0	0x0 RW	**signal_select_timer_6:** Selects which of the 55 input signals are counted by timer 6

5.2.81 signal_select_timer_7 (gpd_gptimer_signal_select_timer_7)—Offset 684h

Selects which of the 55 input signals are counted by timer 7

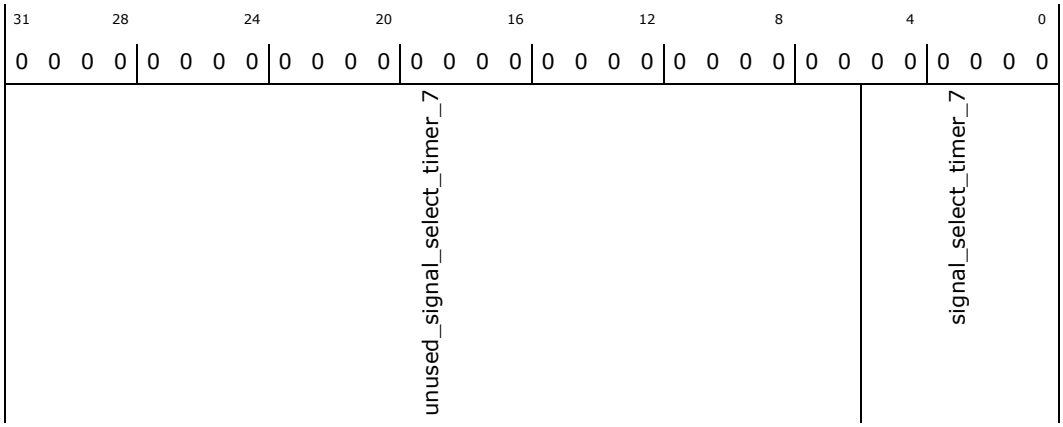
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 684h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_signal_select_timer_7):** Unused
5:0	0x0 RW	**signal_select_timer_7:** Selects which of the 55 input signals are counted by timer 7

5.2.82 irq_trigger_value_0 (gpd_gptimer_irq_trigger_value_0)—Offset 688h

IRQ trigger value for interrupt 0. If the timer selected by irq_timer_select_0 reaches this value, irq_0 will be enabled

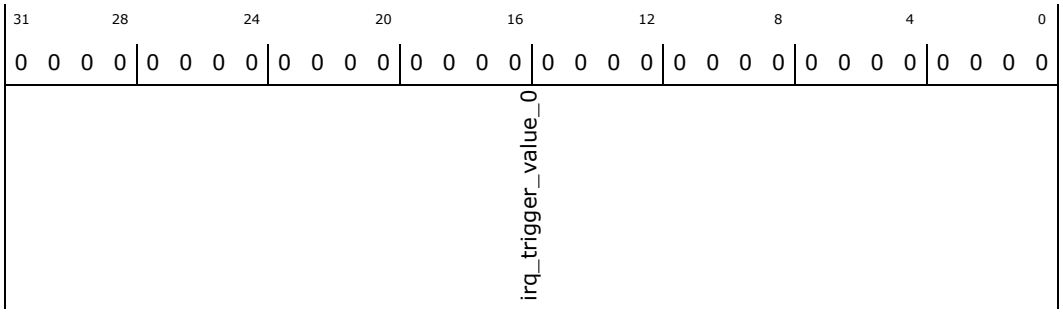
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 688h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**irq_trigger_value_0:** IRQ trigger value for interrupt 0. If the timer selected by irq_timer_select_0 reaches this value, irq_0 will be enabled

5.2.83 irq_trigger_value_1 (gpd_gptimer_irq_trigger_value_1)—Offset 68Ch

IRQ trigger value for interrupt 1. If the timer selected by irq_timer_select_1 reaches this value, irq_1 will be enabled

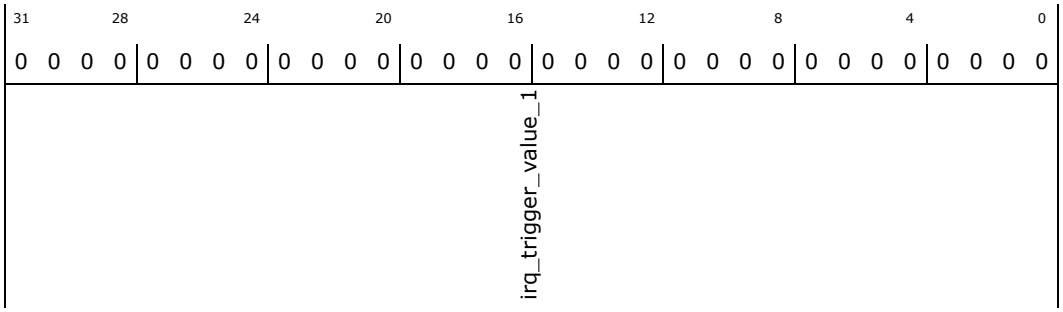
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 68Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**irq_trigger_value_1:** IRQ trigger value for interrupt 1. If the timer selected by irq_timer_select_1 reaches this value, irq_1 will be enabled

5.2.84 irq_timer_select_0 (gpd_gptimer_irq_timer_select_0)—Offset 690h

Indicates which of the 8 timers are used for irq_0 generation

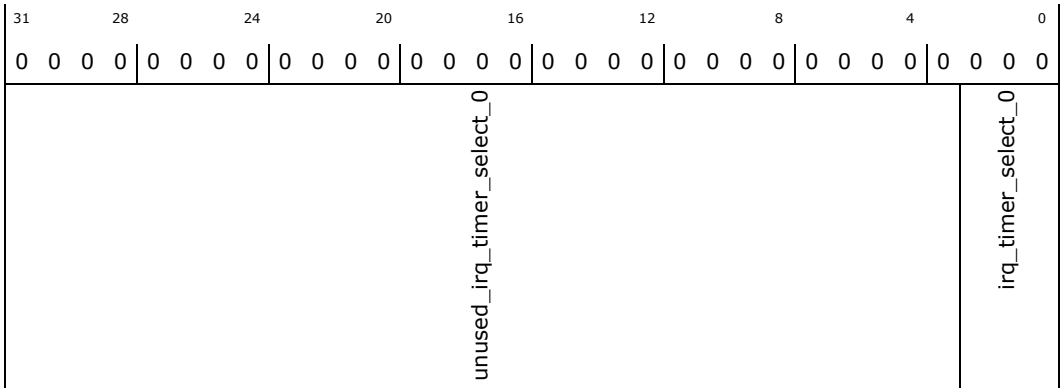
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 690h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved (unused_irq_timer_select_0):** Unused
2:0	0x0 RW	**irq_timer_select_0:** Indicates which of the 8 timers are used for irq_0 generation

5.2.85 irq_timer_select_1 (gpd_gptimer_irq_timer_select_1)—Offset 694h

Indicates which of the 8 timers are used for irq_1 generation

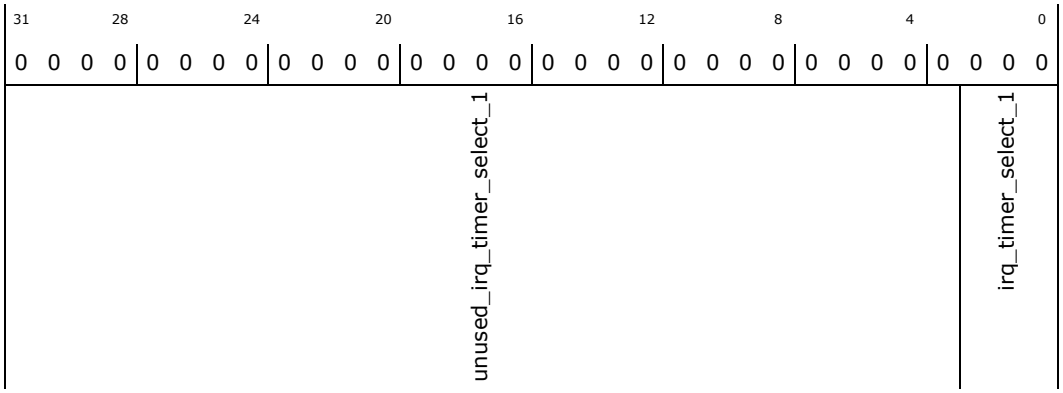
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 694h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved (unused_irq_timer_select_1):** Unused
2:0	0x0 RW	**irq_timer_select_1:** Indicates which of the 8 timers are used for irq_1 generation

5.2.86 irq_enable_0 (gpd_gptimer_irq_enable_0)—Offset 698h

Enable interrupt 0

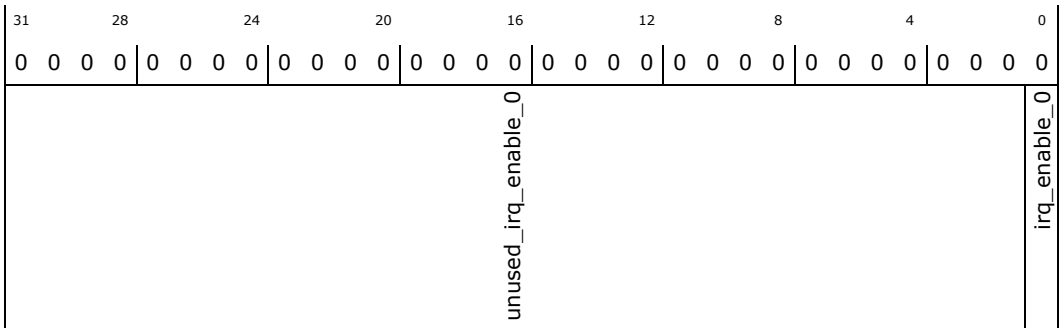
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 698h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_irq_enable_0):** Unused

Bit Range	Default and Access	Field Name (ID): Description
0	0x0 RW	**irq_enable_0:** Enable interrupt 0

5.2.87 irq_enable_1 (gpd_gptimer_irq_enable_1)—Offset 69Ch

Enable interrupt 1

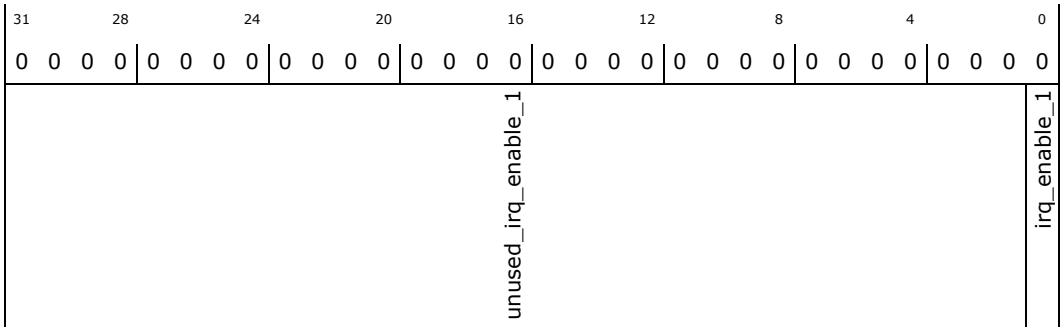
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 69Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_irq_enable_1):** Unused
0	0x0 RW	**irq_enable_1:** Enable interrupt 1

5.2.88 scalar_processor_2400_processor processor status and control register (scp_stat_and_ctrl)—Offset 10000h

Scalar_processor_2400_processor processor status and control register

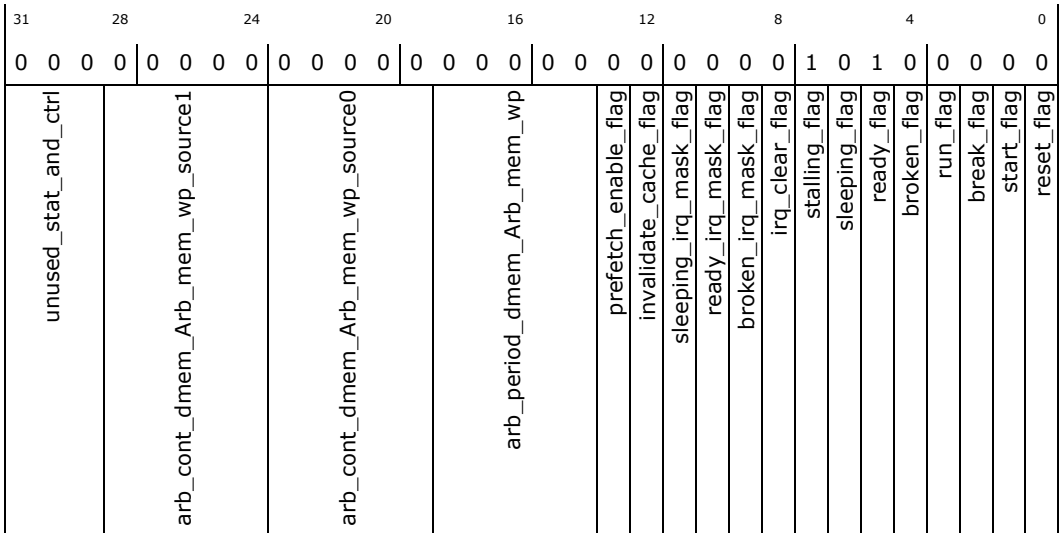
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 10000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 000000A0h



Bit Range	Default and Access	Field Name (ID): Description
31:29	0x0 RO	**Reserved (unused_stat_and_ctrl):** Unused
28:24	0x0 RW	**scalar_processor_2400_processor processor arbiter contender group bandwidth for dmem_Arb_mem_wp_source1 (arb_cont_dmem_Arb_mem_wp_source1):** Arbiter contender group bandwidth for dmem_Arb_mem_wp_source1
23:19	0x0 RW	**scalar_processor_2400_processor processor arbiter contender group bandwidth for dmem_Arb_mem_wp_source0 (arb_cont_dmem_Arb_mem_wp_source0):** Arbiter contender group bandwidth for dmem_Arb_mem_wp_source0
18:14	0x0 RW	**scalar_processor_2400_processor processor arbiter period for dmem_Arb_mem_wp (arb_period_dmem_Arb_mem_wp):** Arbiter period for dmem_Arb_mem_wp
13	0x0 RW	**scalar_processor_2400_processor processor prefetch enable flag (prefetch_enable_flag):** Prefetch enable flag for config_ilm_conf_ilm_icache
12	0x0 RW	**scalar_processor_2400_processor processor invalidate cache flag (invalidate_cache_flag):** Invalidate cache flag for config_ilm_conf_ilm_icache
11	0x0 RW	**scalar_processor_2400_processor processor sleeping interrupt mask (sleeping_irq_mask_flag):** Sleeping IRQ mask flag. Enables (high) or disables (low) IRQ generation when the cell enters the SLEEP state.
10	0x0 RW	**scalar_processor_2400_processor processor ready interrupt mask (ready_irq_mask_flag):** Ready IRQ mask flag. Enables (high) or disables (low) IRQ generation when the cell enters the IDLE state.
9	0x0 RW	**scalar_processor_2400_processor processor broken interrupt mask (broken_irq_mask_flag):** Broken IRQ mask flag. Enables (high) or disables (low) IRQ generation when the cell enters the BROKEN state.

Bit Range	Default and Access	Field Name (ID): Description
8	0x0 RW	**scalar_processor_2400_processor processor clear interrupt flag (irq_clear_flag):** IRQ clear flag. Clears an interrupt request sent by the cell. The cell can generate a level-shaped IRQ when it gets to the BROKEN, IDLE or SLEEP state. Interrupt generation is controlled by mask.
7	0x1 RO	**scalar_processor_2400_processor processor stalling flag (stalling_flag):** Stalling flag. Set to '1' when not executing an instruction. Happens when the run control signal has been set to low, or when an LSU or the CoreIO cannot access data (for example, cache miss, arbitration conflict or FIFO full).
6	0x0 RO	**scalar_processor_2400_processor processor sleeping flag (sleeping_flag):** Sleeping flag. The cell is in sleep mode, that is, when the 'std_sleep' operation has been issued. To resume execution, the start control flag must be set to high.
5	0x1 RO	**scalar_processor_2400_processor processor ready flag (ready_flag):** Ready flag. Set to '1' when not executing a program. This state is entered after a (soft) reset or when the 'std_idle' operation has been issued. To (re)start execution from the start address (in the following register), the start control flag must be set to high.
4	0x0 RO	**scalar_processor_2400_processor processor broken flag (broken_flag):** Broken flag. Unused (obsolete) flag.
3	0x0 RW	**scalar_processor_2400_processor processor run flag (run_flag):** Run flag. Enables program execution (high) or stall the cell, disabling it from continuing program execution (low).
2	0x0 RW	**scalar_processor_2400_processor processor break flag (break_flag):** Break flag. Unused (obsolete) flag.
1	0x0 WO	**scalar_processor_2400_processor processor start flag (start_flag):** Start flag. Starts or continues program execution. The cell automatically resets the bit to '0' after one clock cycle.
0	0x0 WO	**scalar_processor_2400_processor processor reset flag (reset_flag):** Reset flag. Initiates a soft reset for the VLIW core of a processor, the CoreIO part is not reset. This flag must be explicitly cleared by the user to deactivate the soft reset.

5.2.89 scalar_processor_2400_processor processor base address register (scp_base_address)—Offset 10004h

Start address. Specifies the address in the program memory from which the program execution starts when a start signal is issued to the core being in IDLE state.

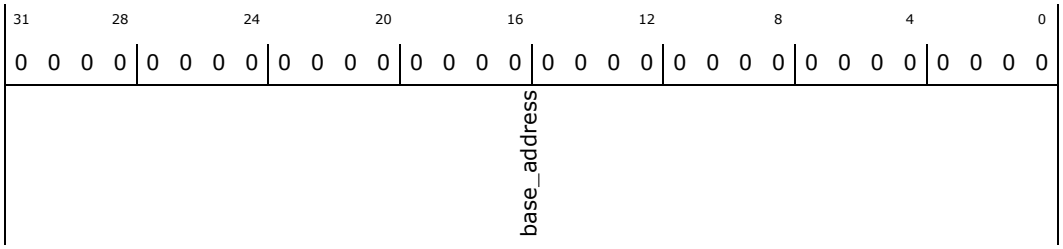
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 10004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**scalar_processor_2400_processor processor base address register (base_address):** Start address. Specifies the address in the program memory from which the program execution starts when a start signal is issued to the core being in IDLE state.

5.2.90 Reserved (scp_unused_2)—Offset 10008h

Unused

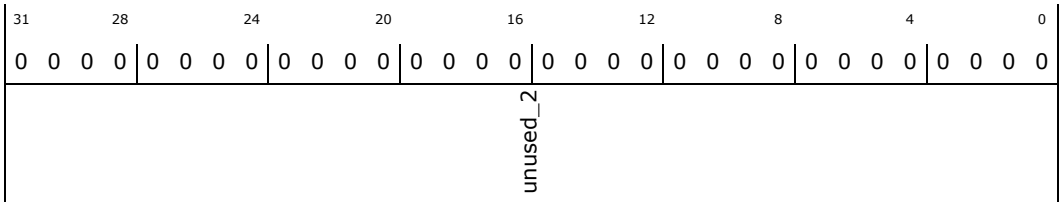
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 10008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**Reserved (unused_2):** Unused

5.2.91 scalar_processor_2400_processor processor base address for segment 0 of master interface xmem_master_int (scp_base_addr_seg_0_MI_xmem_master_int)—Offset 10010h

Base address for segment 0 of master interface xmem_master_int

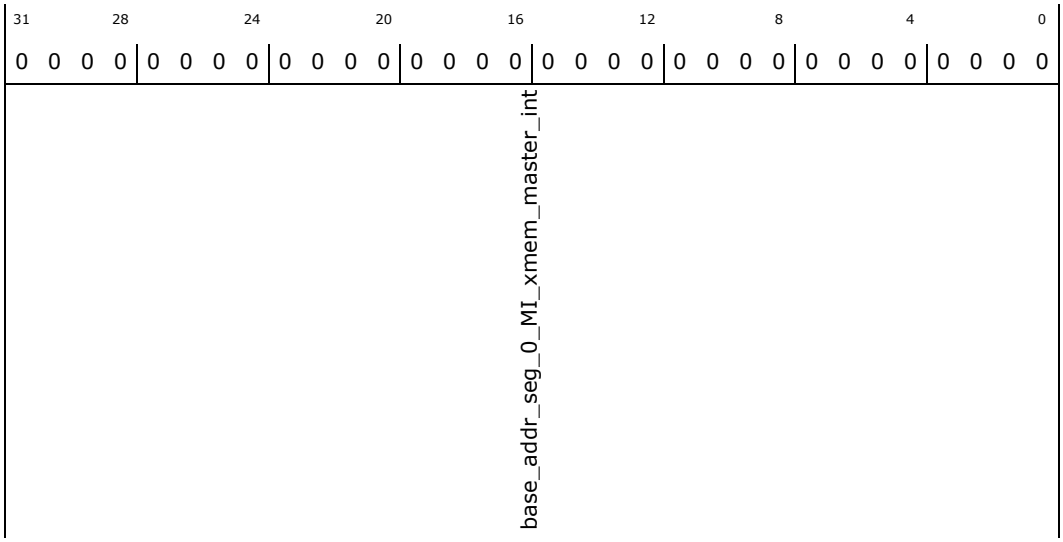
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 10010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**scalar_processor_2400_processor processor base address for segment 0 of master interface xmem_master_int (base_addr_seg_0_MI_xmem_master_int):** Base address for segment 0 of master interface xmem_master_int

5.2.92 scalar_processor_2400_processor processor base address for segment 0 of master interface config_ilm_conf_ilm_master (scp_base_addr_seg_0_MI_config_ilm_conf_ilm_master) —Offset 10014h

Base address for segment 0 of master interface config_ilm_conf_ilm_master

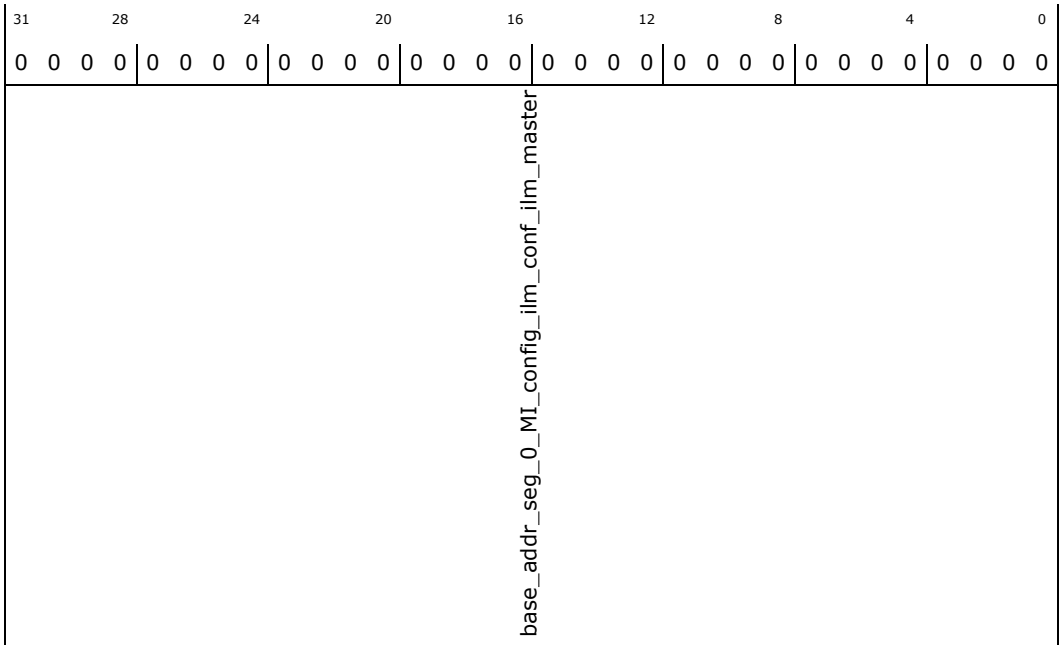
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 10014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**scalar_processor_2400_processor processor base address for segment 0 of master interface config_ilm_conf_ilm_master (base_addr_seg_0_MI_config_ilm_conf_ilm_master):** Base address for segment 0 of master interface config_ilm_conf_ilm_master

5.2.93 Reserved (scp_unused_6)—Offset 10018h

Unused

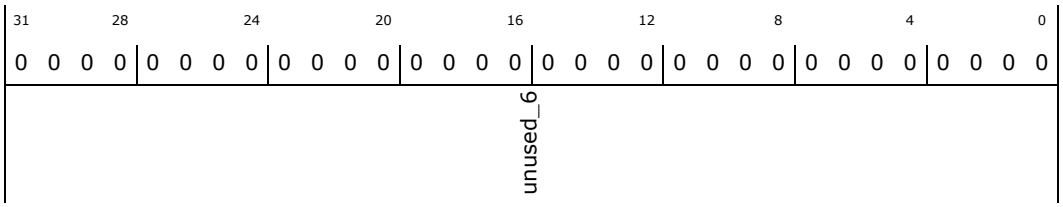
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 10018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**Reserved (unused_6):** Unused

5.2.94 Reserved (scp_unused_7)—Offset 1001Ch

Unused

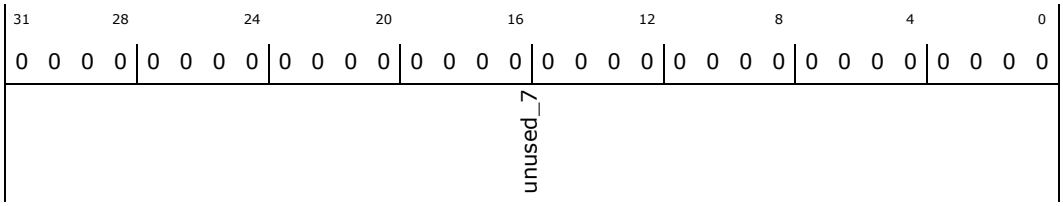
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 1001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**Reserved (unused_7):** Unused

5.2.95 scalar_processor_2400_processor processor debug program counter (scp_debug_pc)—Offset 10024h

Debug program counter. To observe the value of the program counter.

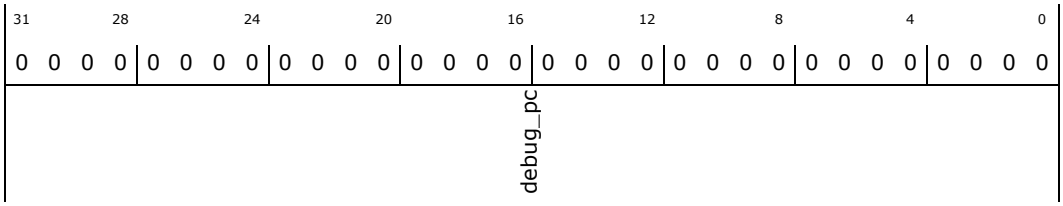
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 10024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**scalar_processor_2400_processor processor debug program counter (debug_pc):** Debug program counter. To observe the value of the program counter.

5.2.96 scalar_processor_2400_processor processor stalling flags (scp_stall_stat_fifo_loc_mt_am_inst_0_op0)—Offset 10028h

Scalar_processor_2400_processor processor stalling flags

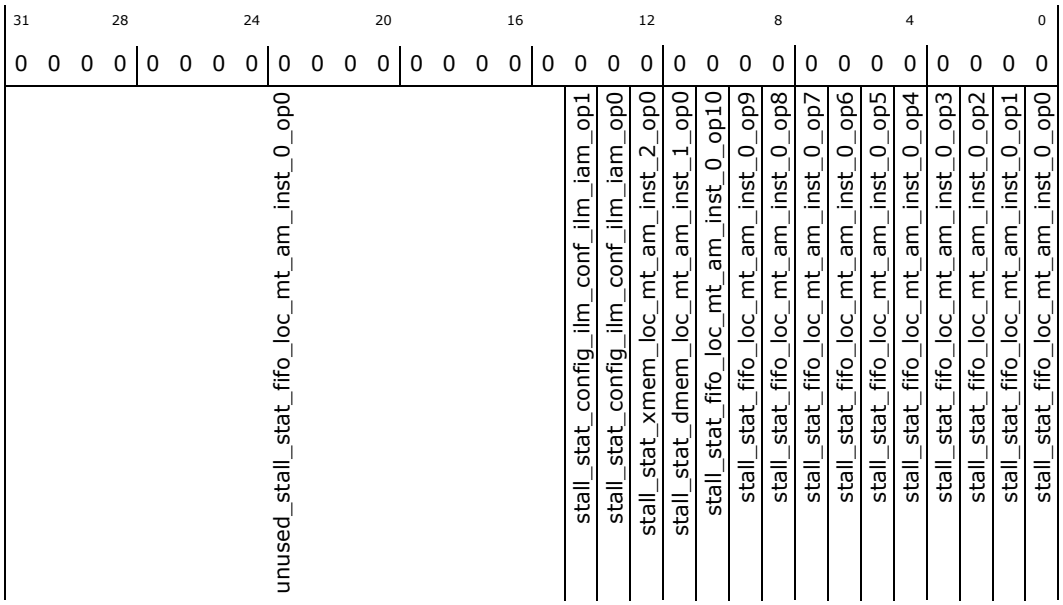
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 10028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:15	0x0 RO	**Reserved (unused_stall_stat_fifo_loc_mt_am_inst_0_op0):** Unused
14	0x0 RO	**scalar_processor_2400_processor processor stalling flag for msink config_ilm_conf_ilm_iam_op1 (stall_stat_config_ilm_conf_ilm_iam_op1):** Stalling flag for msink config_ilm_conf_ilm_iam_op1

Bit Range	Default and Access	Field Name (ID): Description
13	0x0 RO	**scalar_processor_2400_processor processor stalling flag for msink config_ilm_conf_ilm_iam_op0 (stall_stat_config_ilm_conf_ilm_iam_op0):** Stalling flag for msink config_ilm_conf_ilm_iam_op0
12	0x0 RO	**scalar_processor_2400_processor processor stalling flag for msink xmem_loc_mt_am_inst_2_op0 (stall_stat_xmem_loc_mt_am_inst_2_op0):** Stalling flag for msink xmem_loc_mt_am_inst_2_op0
11	0x0 RO	**scalar_processor_2400_processor processor stalling flag for msink dmem_loc_mt_am_inst_1_op0 (stall_stat_dmem_loc_mt_am_inst_1_op0):** Stalling flag for msink dmem_loc_mt_am_inst_1_op0
10	0x0 RO	**scalar_processor_2400_processor processor stalling flag for msink fifo_loc_mt_am_inst_0_op10 (stall_stat_fifo_loc_mt_am_inst_0_op10):** Stalling flag for msink fifo_loc_mt_am_inst_0_op10
9	0x0 RO	**scalar_processor_2400_processor processor stalling flag for msink fifo_loc_mt_am_inst_0_op9 (stall_stat_fifo_loc_mt_am_inst_0_op9):** Stalling flag for msink fifo_loc_mt_am_inst_0_op9
8	0x0 RO	**scalar_processor_2400_processor processor stalling flag for msink fifo_loc_mt_am_inst_0_op8 (stall_stat_fifo_loc_mt_am_inst_0_op8):** Stalling flag for msink fifo_loc_mt_am_inst_0_op8
7	0x0 RO	**scalar_processor_2400_processor processor stalling flag for msink fifo_loc_mt_am_inst_0_op7 (stall_stat_fifo_loc_mt_am_inst_0_op7):** Stalling flag for msink fifo_loc_mt_am_inst_0_op7
6	0x0 RO	**scalar_processor_2400_processor processor stalling flag for msink fifo_loc_mt_am_inst_0_op6 (stall_stat_fifo_loc_mt_am_inst_0_op6):** Stalling flag for msink fifo_loc_mt_am_inst_0_op6
5	0x0 RO	**scalar_processor_2400_processor processor stalling flag for msink fifo_loc_mt_am_inst_0_op5 (stall_stat_fifo_loc_mt_am_inst_0_op5):** Stalling flag for msink fifo_loc_mt_am_inst_0_op5
4	0x0 RO	**scalar_processor_2400_processor processor stalling flag for msink fifo_loc_mt_am_inst_0_op4 (stall_stat_fifo_loc_mt_am_inst_0_op4):** Stalling flag for msink fifo_loc_mt_am_inst_0_op4
3	0x0 RO	**scalar_processor_2400_processor processor stalling flag for msink fifo_loc_mt_am_inst_0_op3 (stall_stat_fifo_loc_mt_am_inst_0_op3):** Stalling flag for msink fifo_loc_mt_am_inst_0_op3
2	0x0 RO	**scalar_processor_2400_processor processor stalling flag for msink fifo_loc_mt_am_inst_0_op2 (stall_stat_fifo_loc_mt_am_inst_0_op2):** Stalling flag for msink fifo_loc_mt_am_inst_0_op2

Bit Range	Default and Access	Field Name (ID): Description
1	0x0 RO	**scalar_processor_2400_processor processor stalling flag for msink fifo_loc_mt_am_inst_0_op1 (stall_stat_fifo_loc_mt_am_inst_0_op1):** Stalling flag for msink fifo_loc_mt_am_inst_0_op1
0	0x0 RO	**scalar_processor_2400_processor processor stalling flag for msink fifo_loc_mt_am_inst_0_op0 (stall_stat_fifo_loc_mt_am_inst_0_op0):** Stalling flag for msink fifo_loc_mt_am_inst_0_op0

5.2.97 Reserved (scp_unused_11)—Offset 1002Ch

Unused

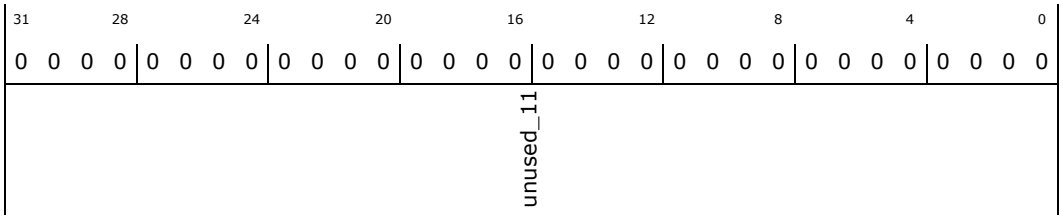
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 1002Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**Reserved (unused_11):** Unused

5.2.98 scalar_processor_2400_processor processor program memory slave access (scp_pmem_slave_access)—Offset 10030h

Pmem slave access flag. By default, the local program memory of the core can only be accessed by a slave interface when the core is idling. While running a program, by default the core has exclusive read access to its local program. Whenever, the slave interface tries to access PMEM in this default mode, it will stall. When setting this flag to '1', this default behavior can be overruled by switching exclusive access to PMEM to the slave interface. Whenever the core tries to access PMEM in this 'PMEM slave access' mode, it will be stalled. The benefit of this feature is that it allows uploading new code to PMEM while the core is running a program, for instance from its instruction cache.

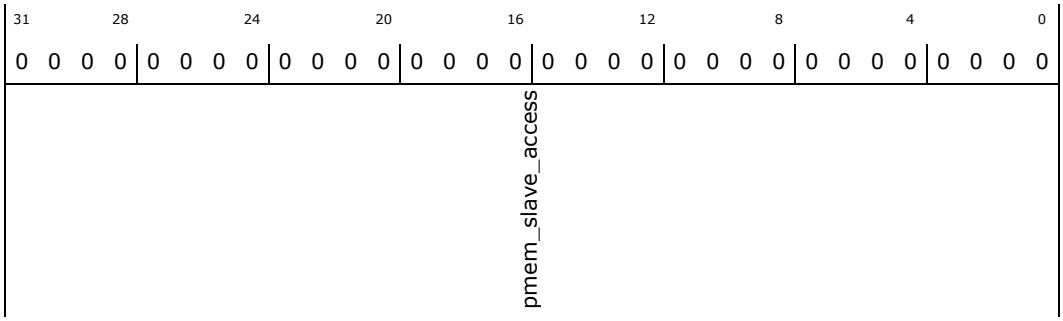
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 10030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**scalar_processor_2400_processor processor program memory slave access (pmem_slave_access):** Pmem slave access flag. By default, the local program memory of the core can only be accessed by a slave interface when the core is idling. While running a program, by default the core has exclusive read access to its local program. Whenever, the slave interface tries to access PMEM in this default mode, it will stall. When setting this flag to '1', this default behavior can be overruled by switching exclusive access to PMEM to the slave interface. Whenever the core tries to access PMEM in this 'PMEM slave access' mode, it will be stalled. The benefit of this feature is that it allows uploading new code to PMEM while the core is running a program, for instance from its instruction cache.

5.2.99 isp2401_mamoiada_processor processor status and control register (isp_stat_and_ctrl)—Offset 20000h

isp2401_mamoiada_processor processor status and control register

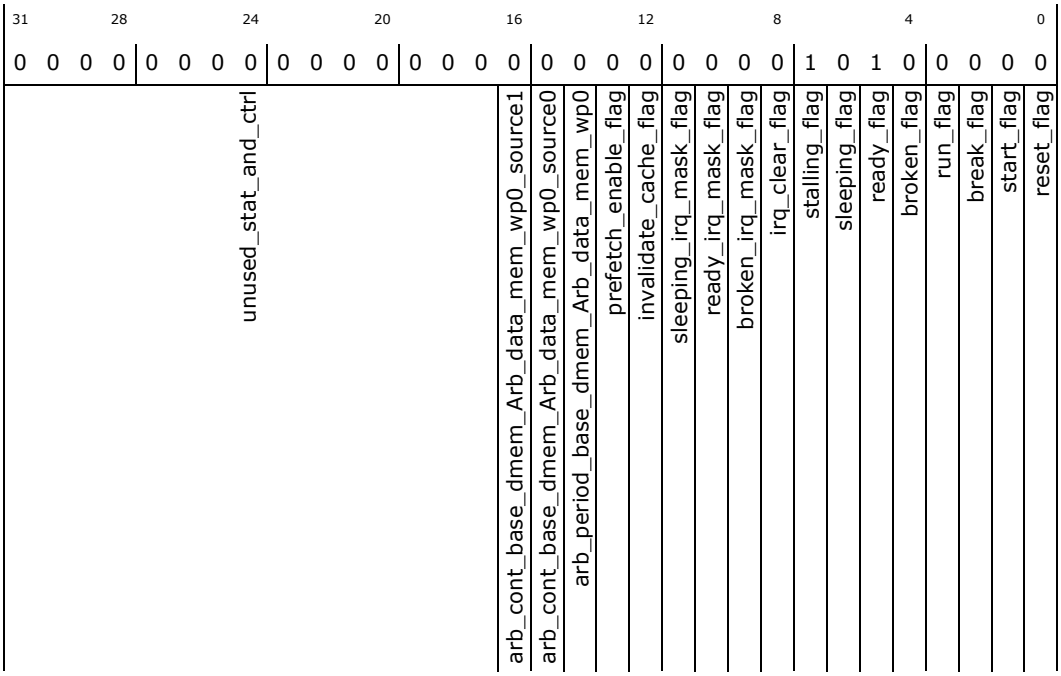
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

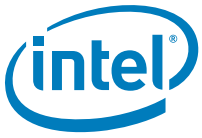
Offset: [ISPMMADR] + 20000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 000000A0h



Bit Range	Default and Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (unused_stat_and_ctrl):** Unused
16	0x0 RW	**isp2401_mamoiada_processor processor arbiter contender group bandwidth for base_dmem_Arb_data_mem_wp0_source1 (arb_cont_base_dmem_Arb_data_mem_wp0_source1):** Arbiter contender group bandwidth for base_dmem_Arb_data_mem_wp0_source1
15	0x0 RW	**isp2401_mamoiada_processor processor arbiter contender group bandwidth for base_dmem_Arb_data_mem_wp0_source0 (arb_cont_base_dmem_Arb_data_mem_wp0_source0):** Arbiter contender group bandwidth for base_dmem_Arb_data_mem_wp0_source0
14	0x0 RW	**isp2401_mamoiada_processor processor arbiter period for base_dmem_Arb_data_mem_wp0 (arb_period_base_dmem_Arb_data_mem_wp0):** Arbiter period for base_dmem_Arb_data_mem_wp0
13	0x0 RW	**isp2401_mamoiada_processor processor prefetch enable flag (prefetch_enable_flag):** Prefetch enable flag for base_config_mem_icache
12	0x0 RW	**isp2401_mamoiada_processor processor invalidate cache flag (invalidate_cache_flag):** Invalidate cache flag for base_config_mem_icache
11	0x0 RW	**isp2401_mamoiada_processor processor sleeping interrupt mask (sleeping_irq_mask_flag):** Sleeping IRQ mask flag. Enables (high) or disables (low) IRQ generation when the cell enters the SLEEP state.



Bit Range	Default and Access	Field Name (ID): Description
10	0x0 RW	**isp2401_mamoiada_processor processor ready interrupt mask (ready_irq_mask_flag):** Ready IRQ mask flag. Enables (high) or disables (low) IRQ generation when the cell enters the IDLE state.
9	0x0 RW	**isp2401_mamoiada_processor processor broken interrupt mask (broken_irq_mask_flag):** Broken IRQ mask flag. Enables (high) or disables (low) IRQ generation when the cell enters the BROKEN state.
8	0x0 RW	**isp2401_mamoiada_processor processor clear interrupt flag (irq_clear_flag):** IRQ clear flag. Clears an interrupt request sent by the cell. The cell can generate a level-shaped IRQ when it gets to the BROKEN, IDLE or SLEEP state. Interrupt generation is controlled by mask.
7	0x1 RO	**isp2401_mamoiada_processor processor stalling flag (stalling_flag):** Stalling flag. Set to '1' when not executing an instruction. Happens when the run control signal has been set to low, or when an LSU or the CoreIO cannot access data (for example, cache miss, arbitration conflict or FIFO full).
6	0x0 RO	**isp2401_mamoiada_processor processor sleeping flag (sleeping_flag):** Sleeping flag. The cell is in sleep mode, that is, when the 'std_sleep' operation has been issued. To resume execution, the start control flag must be set to high.
5	0x1 RO	**isp2401_mamoiada_processor processor ready flag (ready_flag):** Ready flag. Set to '1' when not executing a program. This state is entered after a (soft) reset or when the 'std_idle' operation has been issued. To (re)start execution from the start address (in the following register), the start control flag must be set to high.
4	0x0 RO	**isp2401_mamoiada_processor processor broken flag (broken_flag):** Broken flag. Unused (obsolete) flag.
3	0x0 RW	**isp2401_mamoiada_processor processor run flag (run_flag):** Run flag. Enables program execution (high) or stall the cell, disabling it from continuing program execution (low).
2	0x0 RW	**isp2401_mamoiada_processor processor break flag (break_flag):** Break flag. Unused (obsolete) flag.
1	0x0 WO	**isp2401_mamoiada_processor processor start flag (start_flag):** Start flag. Starts or continues program execution. The cell automatically resets the bit to '0' after one clock cycle.
0	0x0 WO	**isp2401_mamoiada_processor processor reset flag (reset_flag):** Reset flag. Initiates a soft reset for the VLIW core of a processor, the CoreIO part is not reset. This flag must be explicitly cleared by the user to de-activate the soft reset.

5.2.100 isp2401_mamoiada_processor processor base address register (isp_base_address)—Offset 20004h

Start address. Specifies the address in the program memory from which the program execution starts when a start signal is issued to the core being in IDLE state.

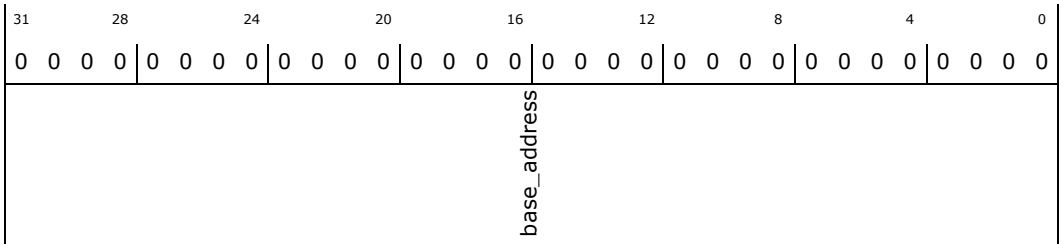
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 20004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**isp2401_mamoiada_processor processor base address register (base_address):** Start address. Specifies the address in the program memory from which the program execution starts when a start signal is issued to the core being in IDLE state.

5.2.101 Reserved (isp_unused_2)—Offset 20008h

Unused

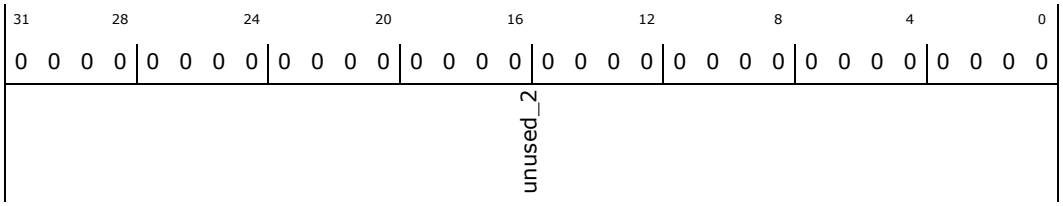
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 20008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**Reserved (unused_2):** Unused

5.2.102 isp2401_mamoiada_processor processor base address for segment 0 of master interface base_config_mem_master

(isp_base_addr_seg_0_MI_base_config_mem_master)—Offset 20010h

Base address for segment 0 of master interface base_config_mem_master

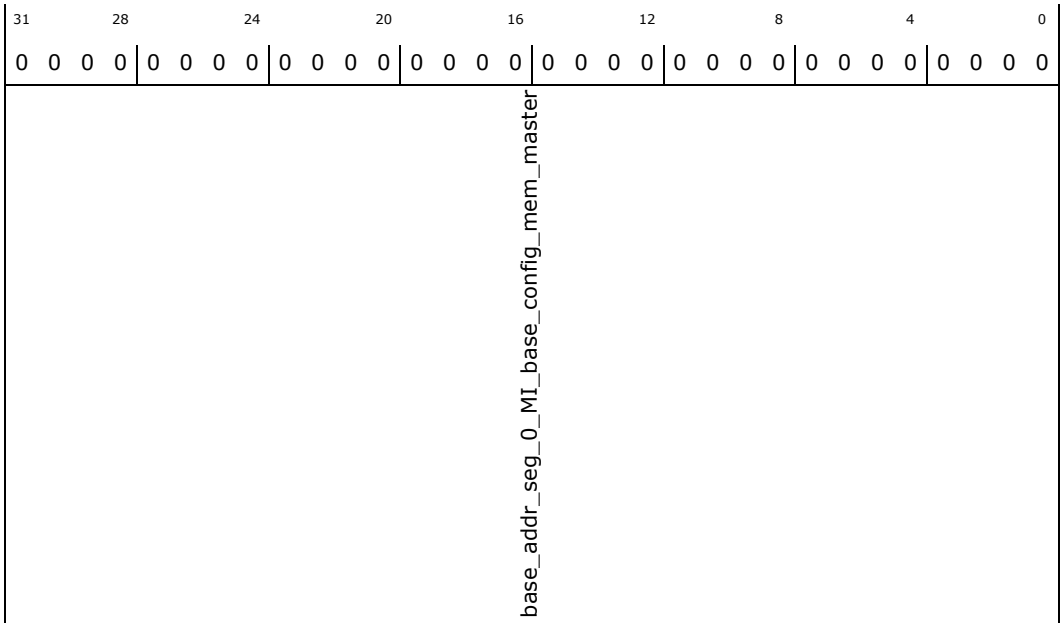
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 20010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**isp2401_mamoiada_processor processor base address for segment 0 of master interface base_config_mem_master (base_addr_seg_0_MI_base_config_mem_master):** Base address for segment 0 of master interface base_config_mem_master

5.2.103 Reserved (isp_unused_5)—Offset 20014h

Unused

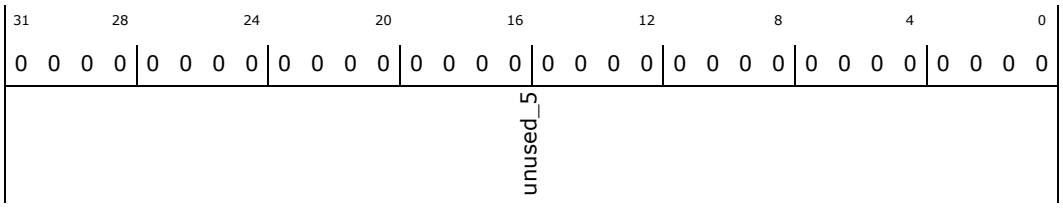
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 20014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**Reserved (unused_5):** Unused

5.2.104 isp2401_mamoiada_processor processor debug program counter (isp_debug_pc)—Offset 2001Ch

Debug program counter. To observe the value of the program counter.

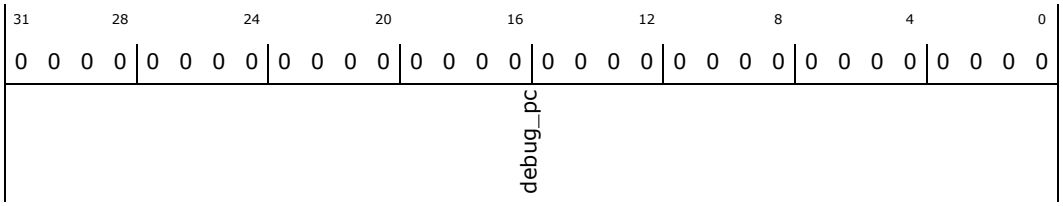
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 2001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**isp2401_mamoiada_processor processor debug program counter (debug_pc):** Debug program counter. To observe the value of the program counter.

5.2.105 isp2401_mamoiada_processor processor stalling flags (isp_stall_stat_base_config_mem_iam_op0)—Offset 20020h

isp2401_mamoiada_processor processor stalling flags

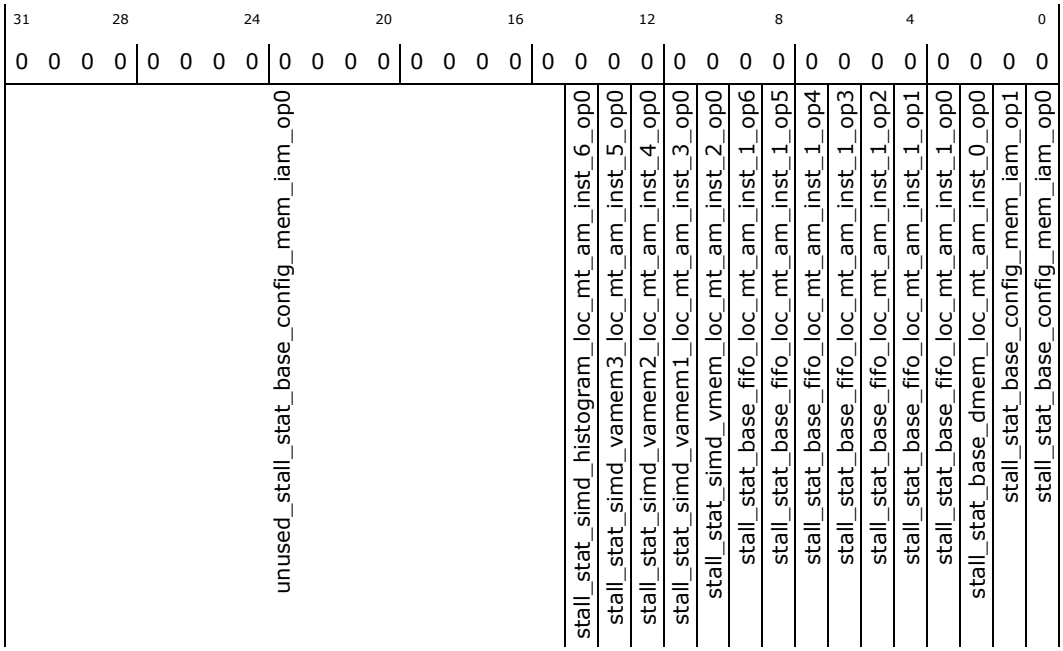
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 20020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:15	0x0 RO	**Reserved (unused_stall_stat_base_config_mem_iam_op0):** Unused
14	0x0 RO	**isp2401_mamoiada_processor processor stalling flag for msink simd_histogram_loc_mt_am_inst_6_op0 (stall_stat_simd_histogram_loc_mt_am_inst_6_op0):** Stalling flag for msink simd_histogram_loc_mt_am_inst_6_op0
13	0x0 RO	**isp2401_mamoiada_processor processor stalling flag for msink simd_vamem3_loc_mt_am_inst_5_op0 (stall_stat_simd_vamem3_loc_mt_am_inst_5_op0):** Stalling flag for msink simd_vamem3_loc_mt_am_inst_5_op0
12	0x0 RO	**isp2401_mamoiada_processor processor stalling flag for msink simd_vamem2_loc_mt_am_inst_4_op0 (stall_stat_simd_vamem2_loc_mt_am_inst_4_op0):** Stalling flag for msink simd_vamem2_loc_mt_am_inst_4_op0
11	0x0 RO	**isp2401_mamoiada_processor processor stalling flag for msink simd_vamem1_loc_mt_am_inst_3_op0 (stall_stat_simd_vamem1_loc_mt_am_inst_3_op0):** Stalling flag for msink simd_vamem1_loc_mt_am_inst_3_op0

Bit Range	Default and Access	Field Name (ID): Description
10	0x0 RO	**isp2401_mamoiada_processor processor stalling flag for msink simd_vmem_loc_mt_am_inst_2_op0 (stall_stat_simd_vmem_loc_mt_am_inst_2_op0):** Stalling flag for msink simd_vmem_loc_mt_am_inst_2_op0
9	0x0 RO	**isp2401_mamoiada_processor processor stalling flag for msink base_fifo_loc_mt_am_inst_1_op6 (stall_stat_base_fifo_loc_mt_am_inst_1_op6):** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op6
8	0x0 RO	**isp2401_mamoiada_processor processor stalling flag for msink base_fifo_loc_mt_am_inst_1_op5 (stall_stat_base_fifo_loc_mt_am_inst_1_op5):** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op5
7	0x0 RO	**isp2401_mamoiada_processor processor stalling flag for msink base_fifo_loc_mt_am_inst_1_op4 (stall_stat_base_fifo_loc_mt_am_inst_1_op4):** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op4
6	0x0 RO	**isp2401_mamoiada_processor processor stalling flag for msink base_fifo_loc_mt_am_inst_1_op3 (stall_stat_base_fifo_loc_mt_am_inst_1_op3):** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op3
5	0x0 RO	**isp2401_mamoiada_processor processor stalling flag for msink base_fifo_loc_mt_am_inst_1_op2 (stall_stat_base_fifo_loc_mt_am_inst_1_op2):** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op2
4	0x0 RO	**isp2401_mamoiada_processor processor stalling flag for msink base_fifo_loc_mt_am_inst_1_op1 (stall_stat_base_fifo_loc_mt_am_inst_1_op1):** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op1
3	0x0 RO	**isp2401_mamoiada_processor processor stalling flag for msink base_fifo_loc_mt_am_inst_1_op0 (stall_stat_base_fifo_loc_mt_am_inst_1_op0):** Stalling flag for msink base_fifo_loc_mt_am_inst_1_op0
2	0x0 RO	**isp2401_mamoiada_processor processor stalling flag for msink base_dmem_loc_mt_am_inst_0_op0 (stall_stat_base_dmem_loc_mt_am_inst_0_op0):** Stalling flag for msink base_dmem_loc_mt_am_inst_0_op0
1	0x0 RO	**isp2401_mamoiada_processor processor stalling flag for msink base_config_mem_iam_op1 (stall_stat_base_config_mem_iam_op1):** Stalling flag for msink base_config_mem_iam_op1
0	0x0 RO	**isp2401_mamoiada_processor processor stalling flag for msink base_config_mem_iam_op0 (stall_stat_base_config_mem_iam_op0):** Stalling flag for msink base_config_mem_iam_op0

5.2.106 Reserved (isp_unused_9)—Offset 20024h

Unused

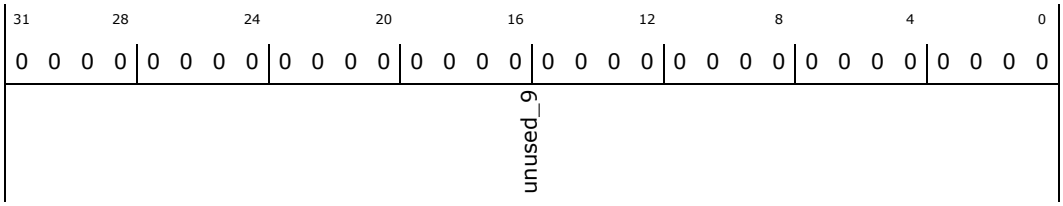
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 20024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**Reserved (unused_9):** Unused

5.2.107 isp2401_mamoiada_processor processor program memory slave access (isp_pmem_slave_access)—Offset 20028h

Pmem slave access flag. By default, the local program memory of the core can only be accessed by a slave interface when the core is idling. While running a program, by default the core has exclusive read access to its local program. Whenever, the slave interface tries to access PMEM in this default mode, it will stall. When setting this flag to '1', this default behavior can be overruled by switching exclusive access to PMEM to the slave interface. Whenever the core tries to access PMEM in this 'PMEM slave access' mode, it will be stalled. The benefit of this feature is that it allows uploading new code to PMEM while the core is running a program, for instance from its instruction cache.

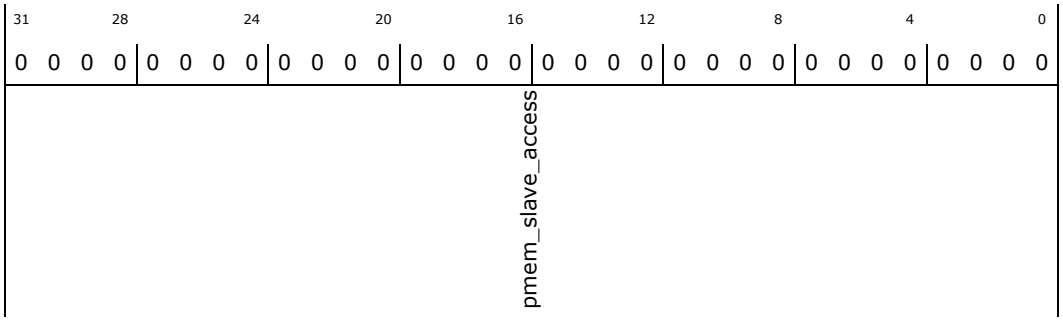
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 20028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**isp2401_mamoiada_processor processor program memory slave access (pmem_slave_access):** Pmem slave access flag. By default, the local program memory of the core can only be accessed by a slave interface when the core is idling. While running a program, by default the core has exclusive read access to its local program. Whenever, the slave interface tries to access PMEM in this default mode, it will stall. When setting this flag to '1', this default behavior can be overruled by switching exclusive access to PMEM to the slave interface. Whenever the core tries to access PMEM in this 'PMEM slave access' mode, it will be stalled. The benefit of this feature is that it allows uploading new code to PMEM while the core is running a program, for instance from its instruction cache.

5.2.108 IF_sw_rst (is_2400_ifmt_ift_prim_IF_sw_rst)—Offset 30000h

Software Reset

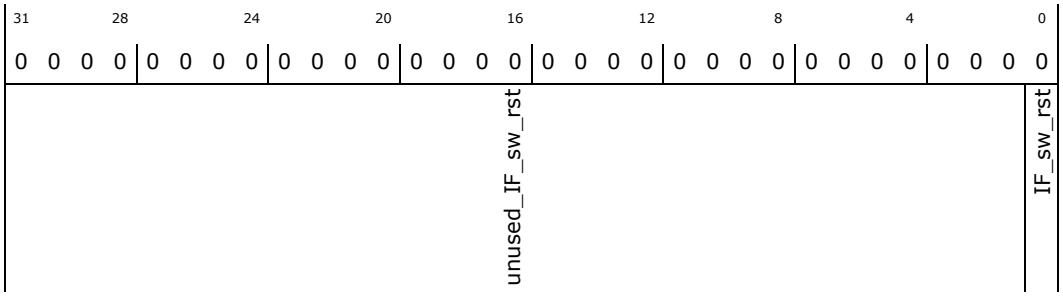
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_sw_rst):** Unused
0	0x0 RW	**IF_sw_rst:** Software Reset

5.2.109 IF_start_line (is_2400_ifmt_ift_prim_IF_start_line)—Offset 30004h

Start line: number of line to skip before passing the 1st line

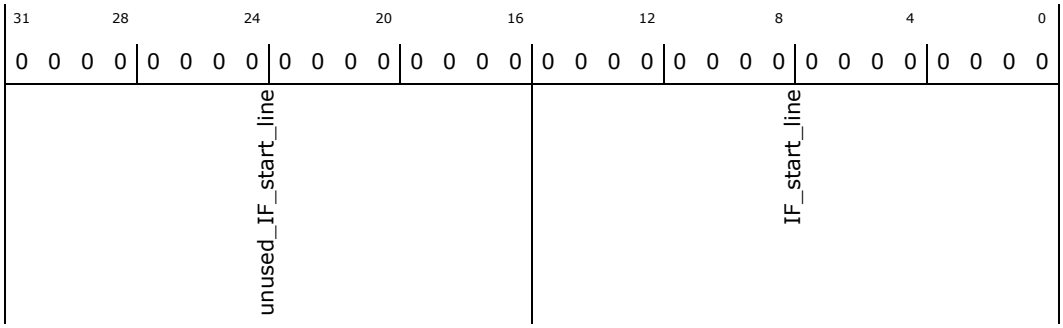
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_IF_start_line):** Unused
15:0	0x0 RW	**IF_start_line:** Start line: number of line to skip before passing the 1st line

5.2.110 IF_start_column (is_2400_ifmt_ift_prim_IF_start_column)—Offset 30008h

Start column: number pixel component to skip before passing the 1st of a line

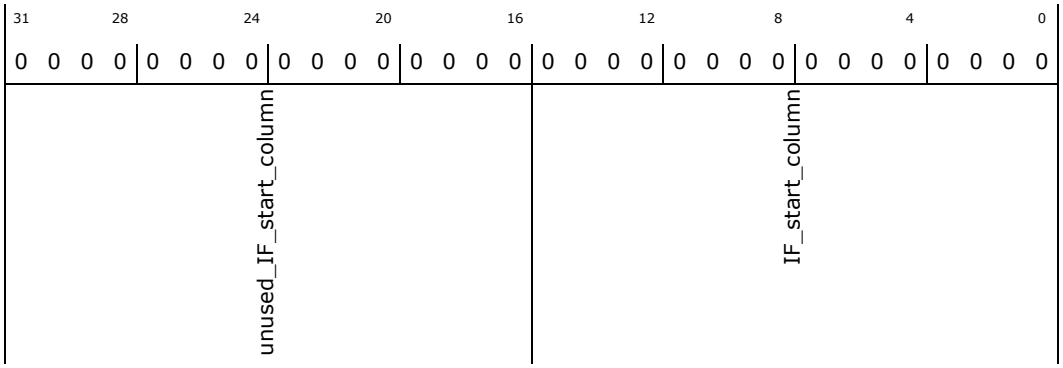
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_IF_start_column):** Unused
15:0	0x0 RW	**IF_start_column:** Start column: number pixel component to skip before passing the 1st of a line

5.2.111 IF_Cropped_height (is_2400_ifmt_ift_prim_IF_Cropped_height)—Offset 3000Ch

Cropped height: number of lines of the cropped image

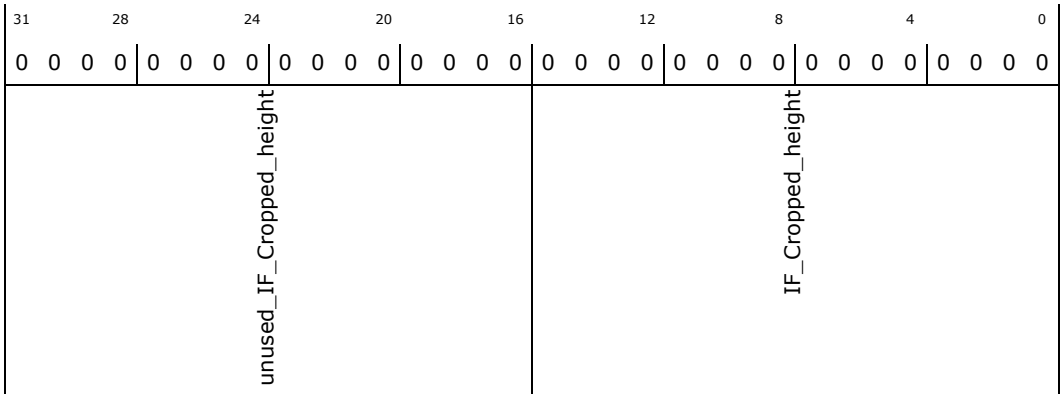
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3000Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_IF_Cropped_height):** Unused
15:0	0x0 RW	**IF_Cropped_height:** Cropped height: number of lines of the cropped image

5.2.112 IF_Cropped_width (is_2400_ifmt_ift_prim_IF_Cropped_width)—Offset 30010h

Cropped width: number of pixel component of the cropped image

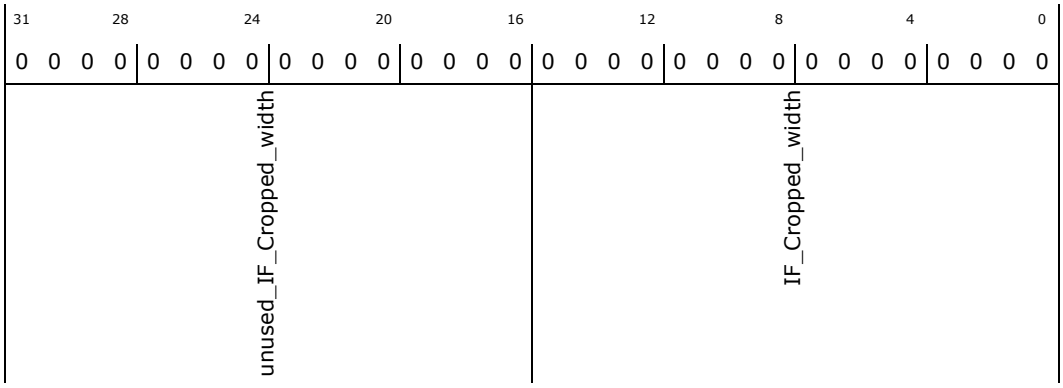
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_IF_Cropped_width):** Unused
15:0	0x0 RW	**IF_Cropped_width:** Cropped width: number of pixel component of the cropped image

5.2.113 IF_Vert_Decim (is_2400_ifmt_ift_prim_IF_Vert_Decim)—Offset 30014h

Vertical Decimation Factor

Vertical decimation factor of N means that only 1 every N lines is processed. When the de-interleaving factor is set to 2 (that is, Bayer), the IF will process 2 consecutive lines avery 2N lines.

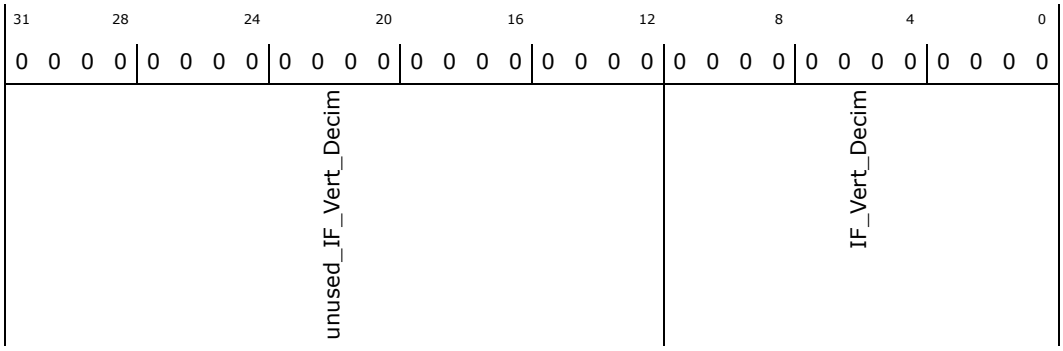
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_IF_Vert_Decim):** Unused
11:0	0x0 RW	**IF_Vert_Decim:** Vertical decimation factor. Vertical decimation factor of N means that only 1 every N lines is processed. When the de-interleaving factor is set to 2 (that is, Bayer), the IF will process 2 consecutive lines avery 2N lines.

5.2.114 IF_Horiz_Decim (is_2400_ifmt_ift_prim_IF_Horiz_Decim)—Offset 30018h

Horizontal decimation factor. Horizontal decimation factor of N means that only 1 every N pixel components is processed. When the de-interleaving factor is set to 2 (that is, Bayer), the IF will process 2 consecutive pixel components avery 2N pixel components.

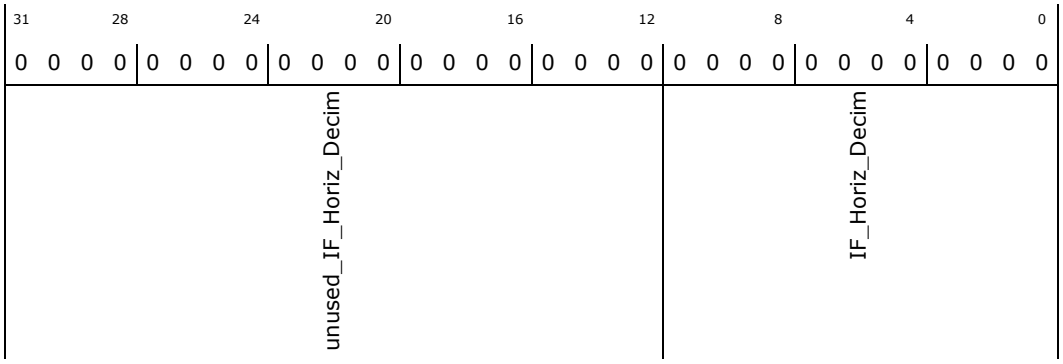
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_IF_Horiz_Decim):** Unused
11:0	0x0 RW	**IF_Horiz_Decim:** Horizontal decimation factor. Horizontal decimation factor of N means that only 1 every N pixel components is processed. When the de-interleaving factor is set to 2 (that is, Bayer), the IF will process 2 consecutive pixel components avery 2N pixel components.

5.2.115 IF_Horiz_Deinter (is_2400_ifmt_ift_prim_IF_Horiz_Deinter)—Offset 3001Ch

Horizontal de-interleaving factor

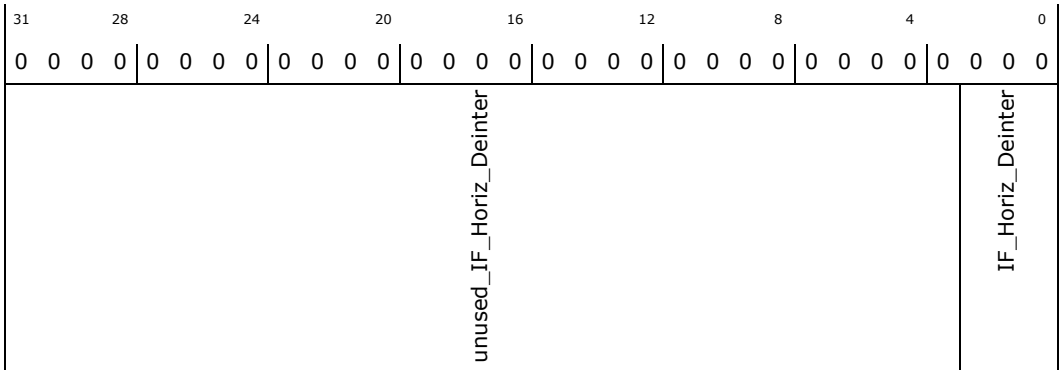
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved (unused_IF_Horiz_Deinter):** Unused
2:0	0x0 RW	**IF_Horiz_Deinter:** Horizontal de-interleaving factor

5.2.116 IF_Left_Pad (is_2400_ifmt_ift_prim_IF_Left_Pad)—Offset 30020h

Left padding: pixel component to be padded at the beginning of each line

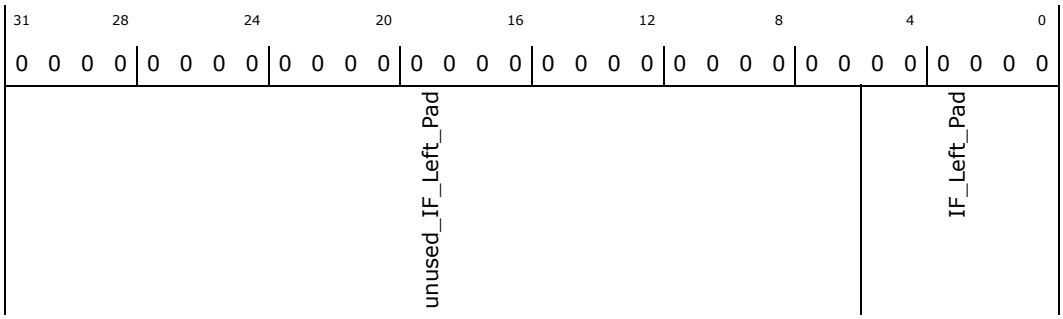
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_IF_Left_Pad):** Unused
5:0	0x0 RW	**IF_Left_Pad:** Left padding: pixel component to be padded at the beginning of each line

5.2.117 IF_EOF_Offset (is_2400_ifmt_ift_prim_IF_EOF_Offset)—Offset 30024h

End of line offset in bytes: number of bytes to add at the address at the end of a line

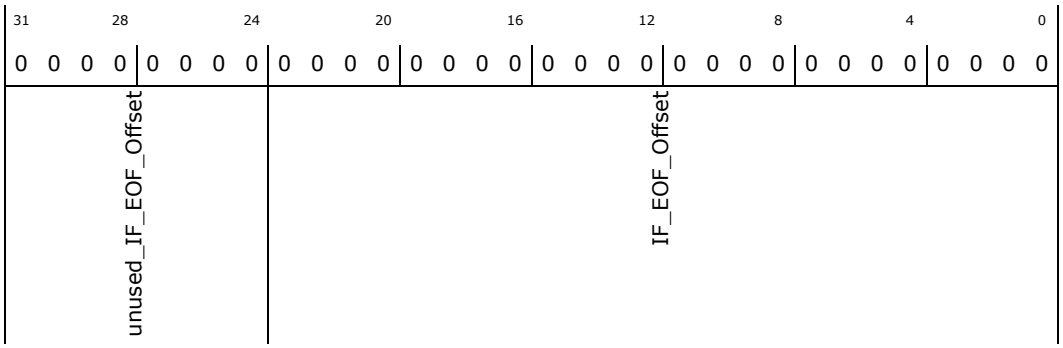
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved (unused_IF_EOF_Offset):** Unused
23:0	0x0 RW	**IF_EOF_Offset:** End of line offset in bytes: number of bytes to add at the address at the end of a line

5.2.118 IF_Start_addr (is_2400_ifmt_ift_prim_IF_Start_addr)—Offset 30028h

Local memory buffer start address (byte aligned)

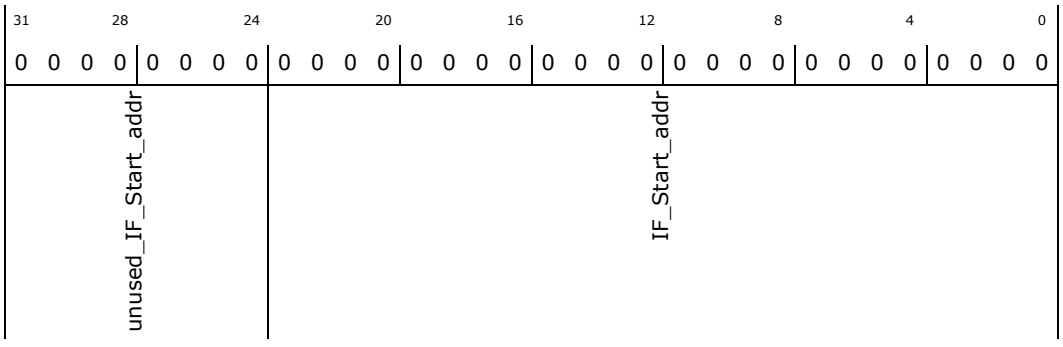
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved (unused_IF_Start_addr):** Unused

Bit Range	Default and Access	Field Name (ID): Description
23:0	0x0 RW	**IF_Start_addr:** Local memory buffer start address (byte aligned)

5.2.119 IF_End_addr (is_2400_ifmt_ift_prim_IF_End_addr)—Offset 3002Ch

Local memory buffer end address (byte aligned)

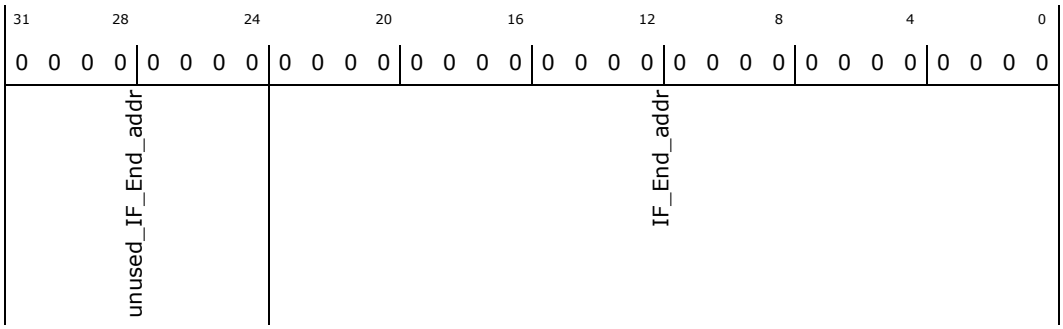
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3002Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved (unused_IF_End_addr):** Unused
23:0	0x0 RW	**IF_End_addr:** Local memory buffer end address (byte aligned)

5.2.120 IF_incr (is_2400_ifmt_ift_prim_IF_incr)—Offset 30030h

Address word increment (word aligned). After every write the address is updated by adding this value times the word alignment.

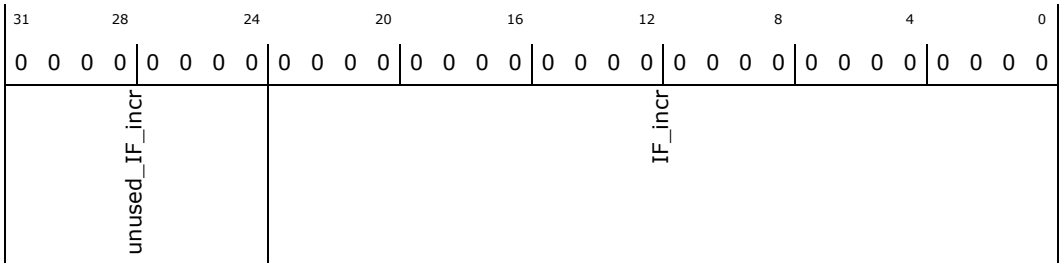
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved (unused_IF_incr):** Unused
23:0	0x0 RW	**IF_incr:** Address word increment (word aligned). After every write the address is updated by adding this value times the word alignment.

5.2.121 IF_YUV_420_format (is_2400_ifmt_ift_prim_IF_YUV_420_format)—Offset 30034h

YUV 420 format: set to work on legacy format YUV420

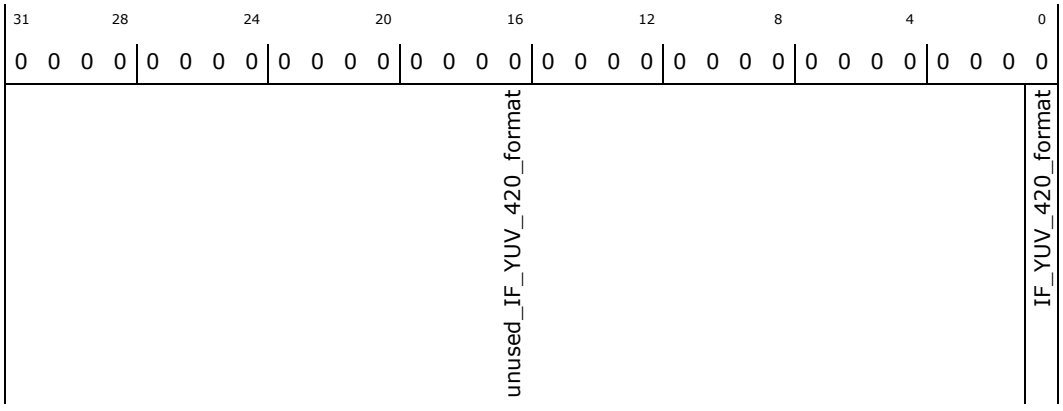
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_YUV_420_format):** Unused

Bit Range	Default and Access	Field Name (ID): Description
0	0x0 RW	**IF_YUV_420_format:** YUV 420 format: set to work on legacy format YUV420

5.2.122 IF_Vsynch_active_low (is_2400_ifmt_ift_prim_IF_Vsynch_active_low)—Offset 30038h

Vertical synch active low: set to 1 if Vsynch and EndOfFrame are active low

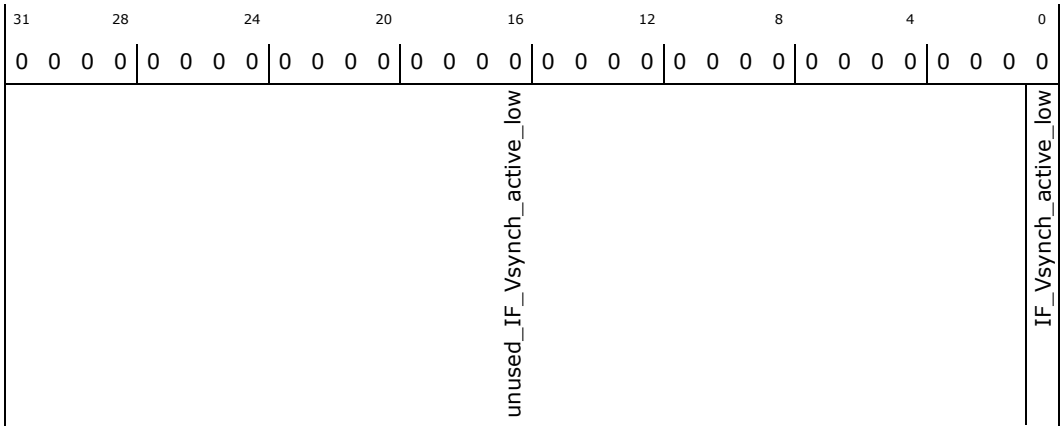
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_Vsynch_active_low):** Unused
0	0x0 RW	**IF_Vsynch_active_low:** Vertical synch active low: set to 1 if Vsynch and EndOfFrame are active low

5.2.123 IF_Hsynch_active_low (is_2400_ifmt_ift_prim_IF_Hsynch_active_low)—Offset 3003Ch

Horizontal synch active low: set to 1 if Hsynch and EndOfLine are active low

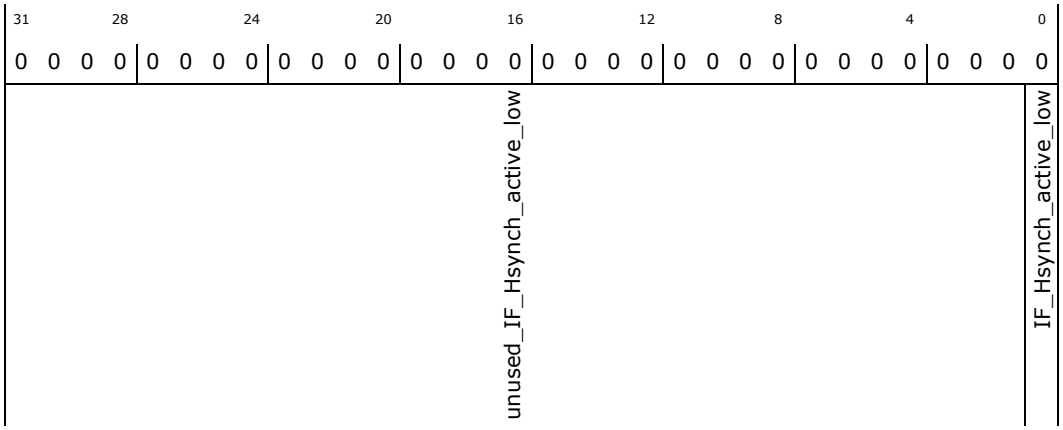
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3003Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_Hsynch_active_low):** Unused
0	0x0 RW	**IF_Hsynch_active_low:** Horizontal synch active low: set to 1 if Hsynch and EndOfLine are active low

5.2.124 IF_ReEnable (is_2400_ifmt_ift_prim_IF_ReEnable)—Offset 30040h

Re-enable status registers. When one of the FSM goes into error state, the status registers keep their value for post-debugging. Setting to 1 will re-enable status register.

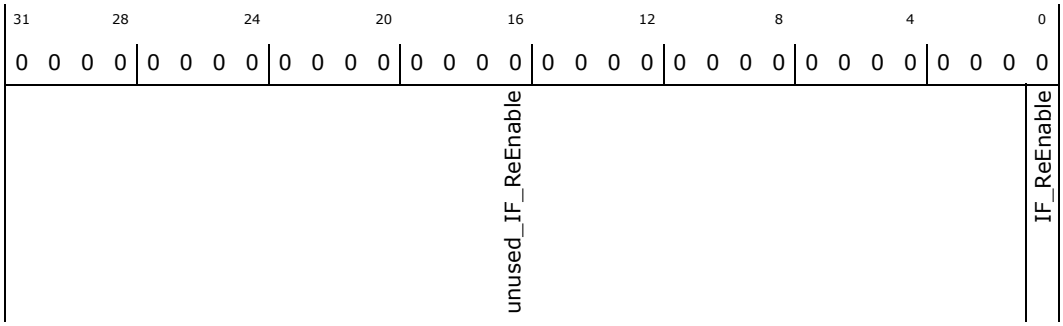
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30040h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_ReEnable):** Unused
0	0x0 RW	**IF_ReEnable:** Re-enable status registers. When one of the FSM goes into error state, the status registers keep their value for post-debugging. Setting to 1 will re-enable status register.

5.2.125 IF_block_input (is_2400_ifmt_ift_prim_IF_block_input)—Offset 30044h

Block input when no req: set to 1 to block data streaming input when no request is received

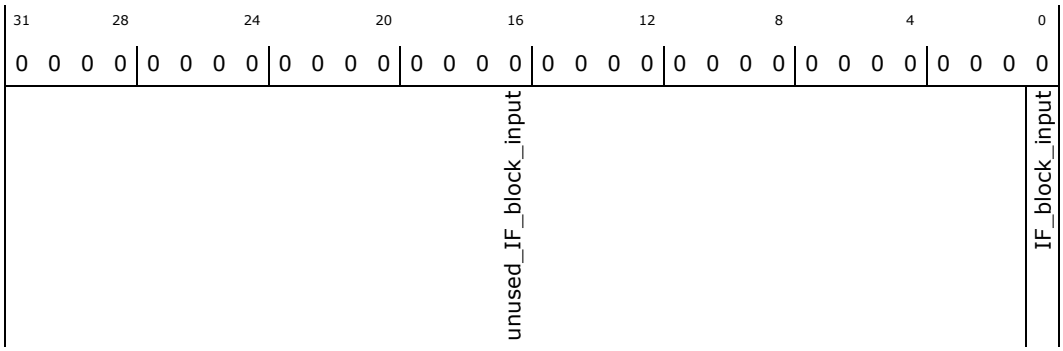
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30044h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_block_input):** Unused
0	0x0 RW	**IF_block_input:** Block input when no req: set to 1 to block data streaming input when no request is received

5.2.126 IF_Vert_Deinter (is_2400_ifmt_ift_prim_IF_Vert_Deinter)—Offset 30048h

Vertical de-interleaving factor

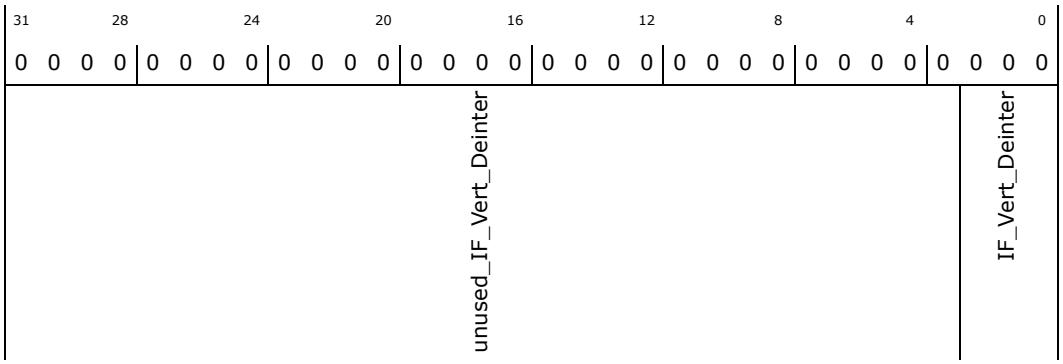
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30048h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved (unused_IF_Vert_Deinter):** Unused
2:0	0x0 RW	**IF_Vert_Deinter:** Vertical de-interleaving factor

5.2.127 IF_FSM_Sync_status (is_2400_ifmt_ift_prim_IF_FSM_Sync_status)—Offset 30100h

FSM Sync status

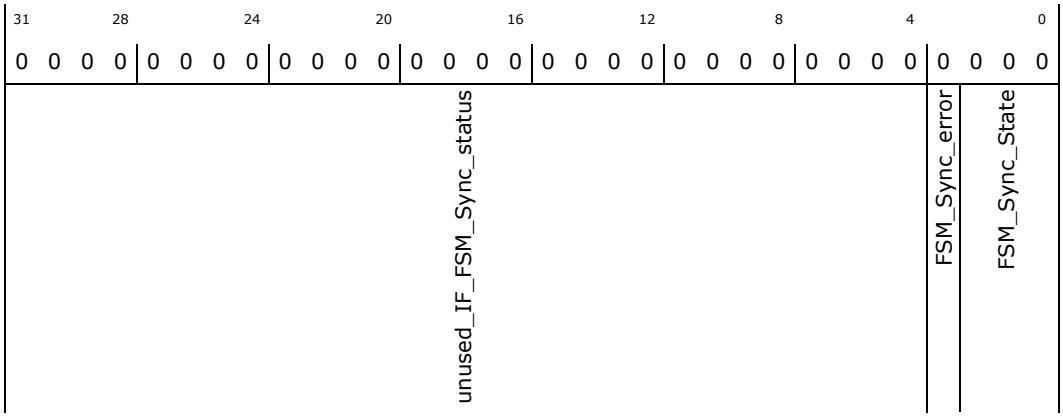
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_IF_FSM_Sync_status):** Unused
3	0x0 RO	**FSM_Sync_error:** Error flag: when set in combination with: Idle state an unknown command has been received; Req. Lines state an unexpected vsynch or eof has been received; Req. Vectors state an unexpected vsynch or eof has been received; another state an illegal state transition has occurred.
2:0	0x0 RO	**FSM_Sync_State:** FSM State: State: 0)Idle -- 1)Req Frame -- 2)Req. Lines -- 3)Req. Vectors -- 4)Send Acknowledge

5.2.128 FSM_Sync_counter (is_2400_ifmt_ift_prim_FSM_Sync_counter)—Offset 30104h

FSM Sync counter: counts the processed items. For Request Frame counts the number of frames processed. For Request lines command counts the number of lines processed. For Request vectors command counts the number of vectors processed. The counter begins at value 1.

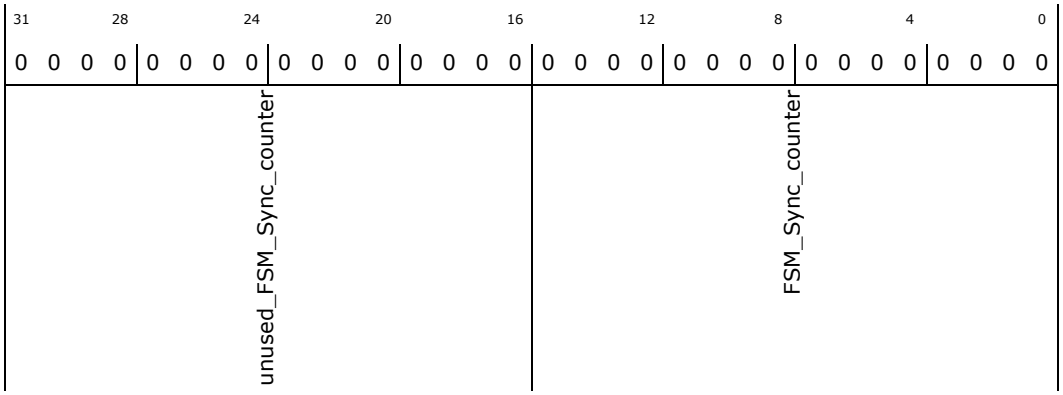
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30104h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_FSM_Sync_counter):** Unused
15:0	0x0 RO	**FSM_Sync_counter:** FSM Sync counter: counts the processed items. For Request Frame counts the number of frames processed. For Request lines command counts the number of lines processed. For Request vectors command counts the number of vectors processed. The counter begins at value 1.

5.2.129 FSM_Crop_status (is_2400_ifmt_ift_prim_FSM_Crop_status)—Offset 30108h

FSM Crop Status

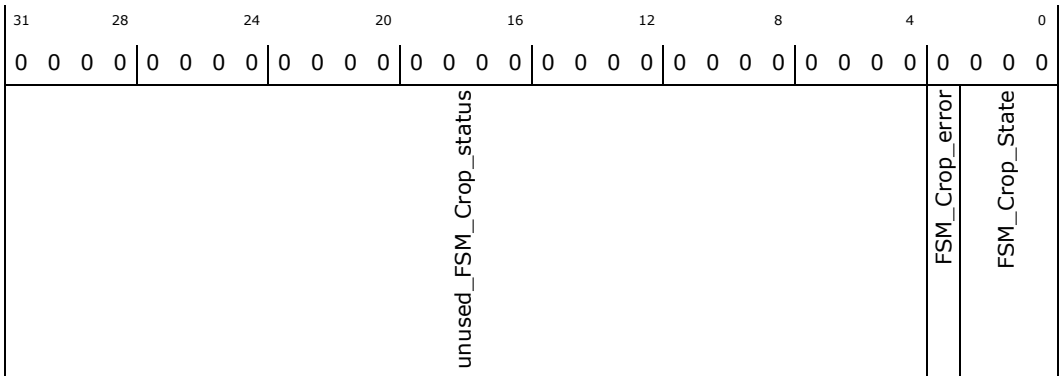
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30108h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_FSM_Crop_status):** Unused
3	0x0 RO	**FSM_Crop_error:** Error flag: when set in combination with: Crop Line state unexpected vsynch or eof has been received; Req. Lines state unexpected vsynch or eof has been received; Req. Vectors state unexpected vsynch or eof has been received; another state an illegal state transition has occurred.
2:0	0x0 RO	**FSM_Crop_State:** FSM State: State: 0)Idle -- 1)Wait Line -- 2)Crop Line -- 3)Crop Pixel -- 4)Pass pixel -- 5) Pass Line

5.2.130 FSM_Crop_line_counter (is_2400_ifmt_ift_prim_FSM_Crop_line_counter)—Offset 3010Ch

FSM Crop line counter

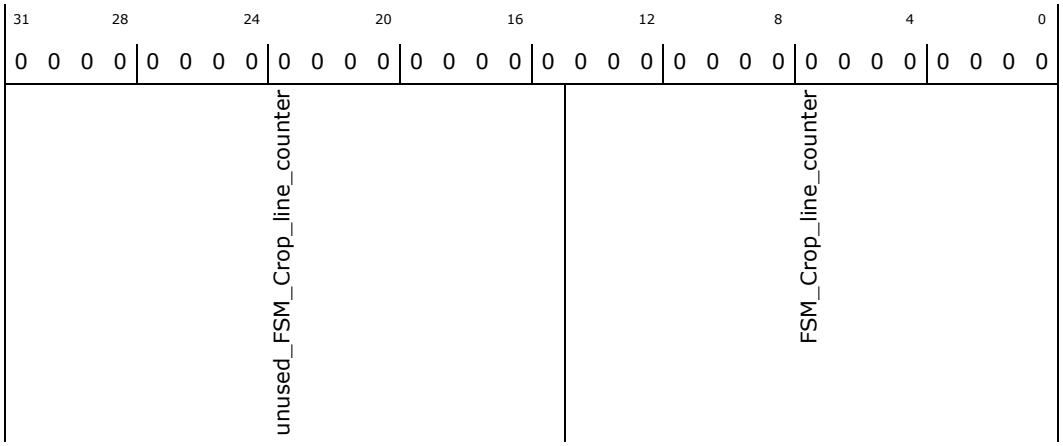
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3010Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:15	0x0 RW	**Reserved (unused_FSM_Crop_line_counter):** Unused
14:0	0x0 RO	**FSM_Crop_line_counter:** FSM Crop line counter

5.2.131 FSM_Crop_pixel_counter (is_2400_ifmt_ift_prim_FSM_Crop_pixel_counter)—Offset 30110h

FSM Crop pixel component counter

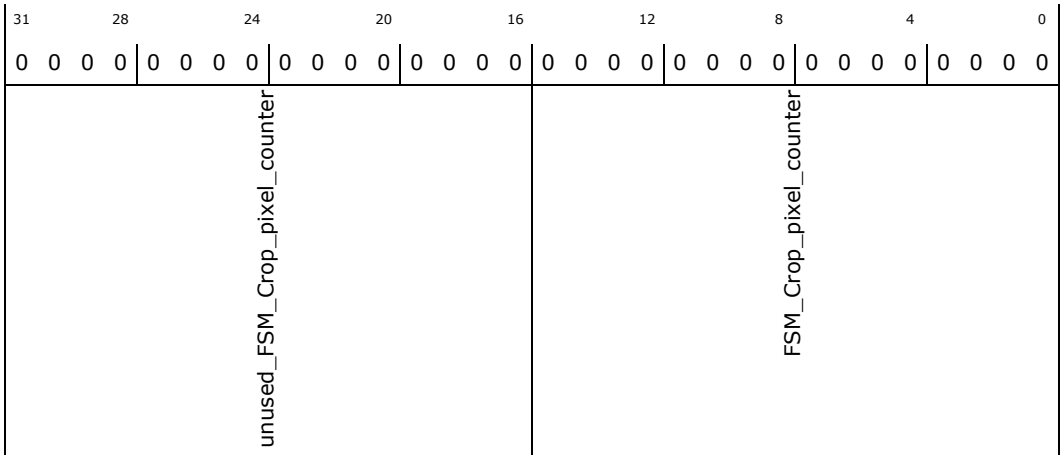
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30110h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_FSM_Crop_pixel_counter):** Unused
15:0	0x0 RO	**FSM_Crop_pixel_counter:** FSM Crop pixel component counter

5.2.132 FSM_Deinterl_idx_buffer (is_2400_ifmt_ift_prim_FSM_Deinterl_idx_buffer)—Offset 30114h

FSM De-interleaving idx Buffer

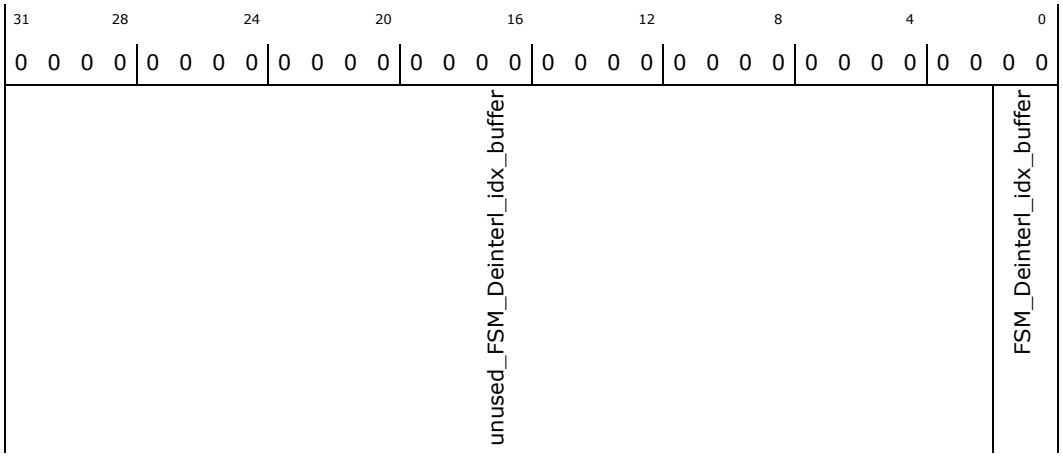
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30114h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_FSM_Deinterl_idx_buffer):** Unused
1:0	0x0 RO	**FSM_Deinterl_idx_buffer:** FSM de-interleaving idx buffer

5.2.133 FSM_Horiz_Decim_cnt (is_2400_ifmt_ift_prim_FSM_Horiz_Decim_cnt)—Offset 30118h

FSM Horizontal Decimation Counter

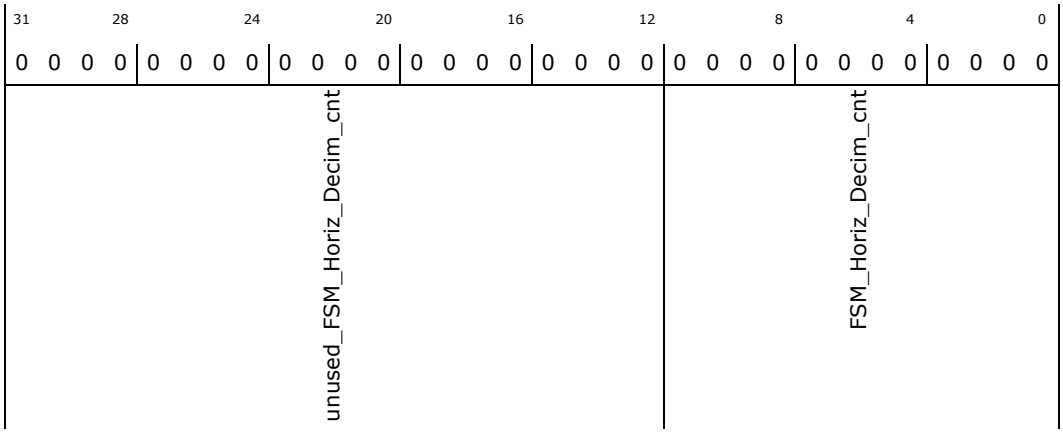
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30118h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_FSM_Horiz_Decim_cnt):** Unused
11:0	0x0 RO	**FSM_Horiz_Decim_cnt:** FSM Horizontal Decimation counter

5.2.134 FSM_Vertic_Decim_cnt (is_2400_ifmt_ift_prim_FSM_Vertic_Decim_cnt)—Offset 3011Ch

FSM Vertical Decimation Counter

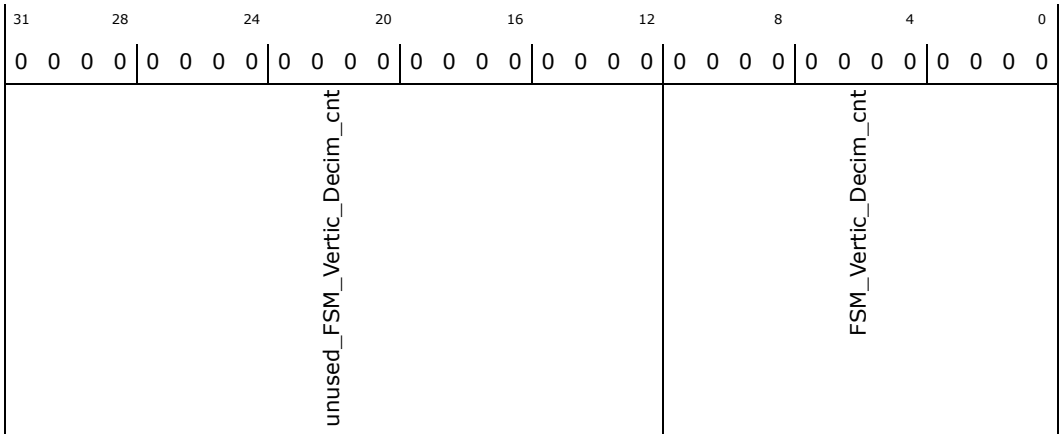
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3011Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_FSM_Vertic_Decim_cnt):** Unused
11:0	0x0 RO	**FSM_Vertic_Decim_cnt:** FSM Vertical decimation counter

5.2.135 FSM_Vertic_Block_Decim_cnt (is_2400_ifmt_ift_prim_FSM_Vertic_Block_Decim_cnt)—Offset 30120h

FSM Vertical Block Decimation Counter

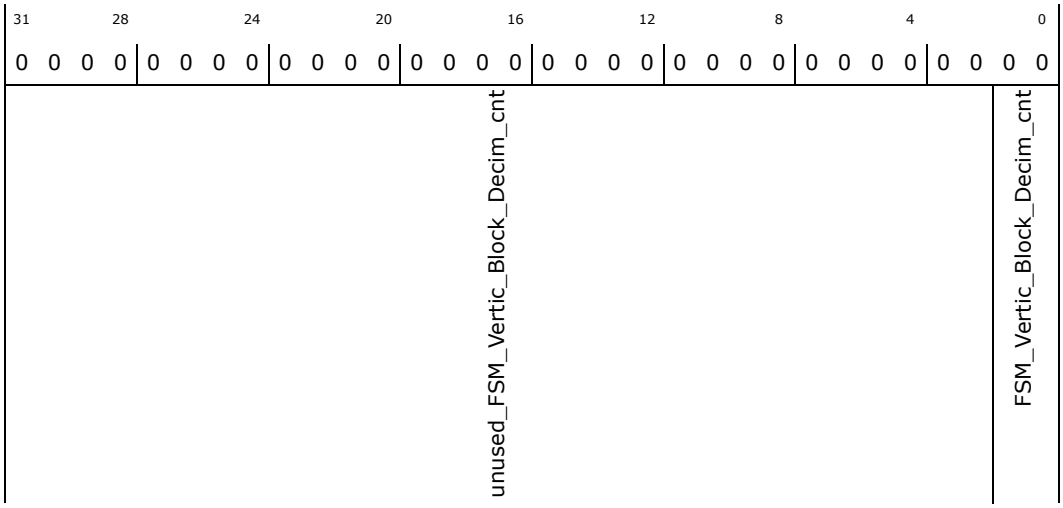
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30120h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_FSM_Vertic_Block_Decim_cnt):** Unused
1:0	0x0 RO	**FSM_Vertic_Block_Decim_cnt:** FSM Vertical block decimation counter

5.2.136 IF_FSM_Padding_status (is_2400_ifmt_ift_prim_IF_FSM_Padding_status)—Offset 30124h

FSM Padding Status

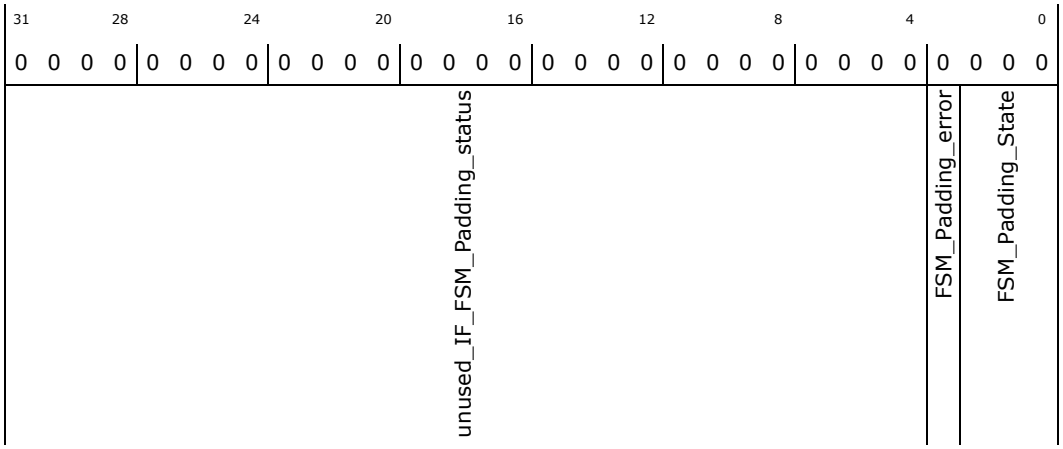
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30124h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_IF_FSM_Padding_status):** Unused
3	0x0 RO	**FSM_Padding_error:** Error flag: when set in combination with: Left Padding state an unexpected vsynch or hsync has been received; Write state an unexpected vsynch or hsync has been received; Right padding state unexpected vsynch has been received; Send EOL state an unexpected vsynch has been received; another state an illegal state transition has occurred.
2:0	0x0 RO	**FSM_Padding_State:** FSM State: State: 0)Idle -- 1)Left Padding -- 2)Write -- 3)Right padding -- 4)Sending EOL

5.2.137 IF_FSM_Padding_elem_idx (is_2400_ifmt_ift_prim_IF_FSM_Padding_elem_idx)—Offset 30128h

FSM Padding Element Index Counter

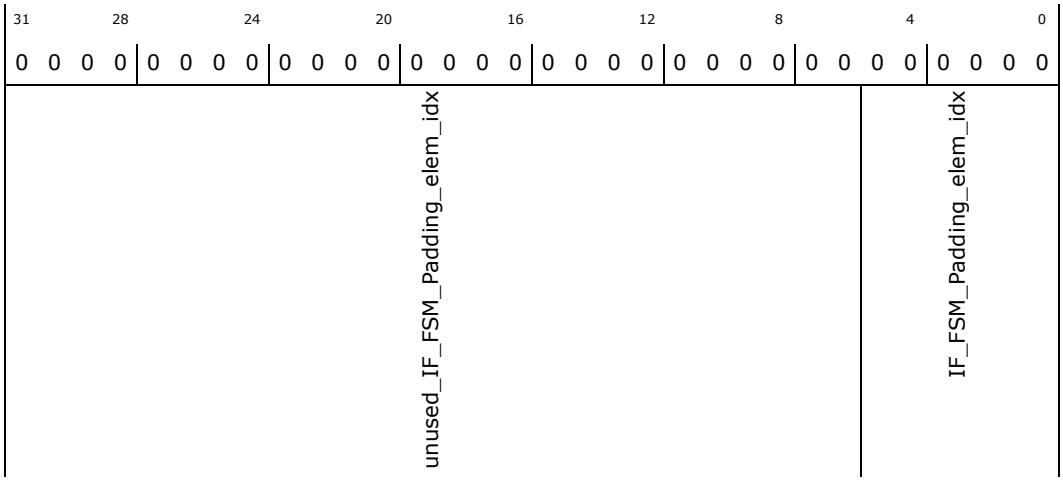
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30128h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_IF_FSM_Padding_elem_idx):** Unused
5:0	0x0 RO	**IF_FSM_Padding_elem_idx:** FSM Padding element index counter

5.2.138 IF_FSM_Vec_Sup (is_2400_ifmt_ift_prim_IF_FSM_Vec_Sup)—Offset 3012Ch

FSM Vector Support Error State: if set the FSM Vector support is in error state

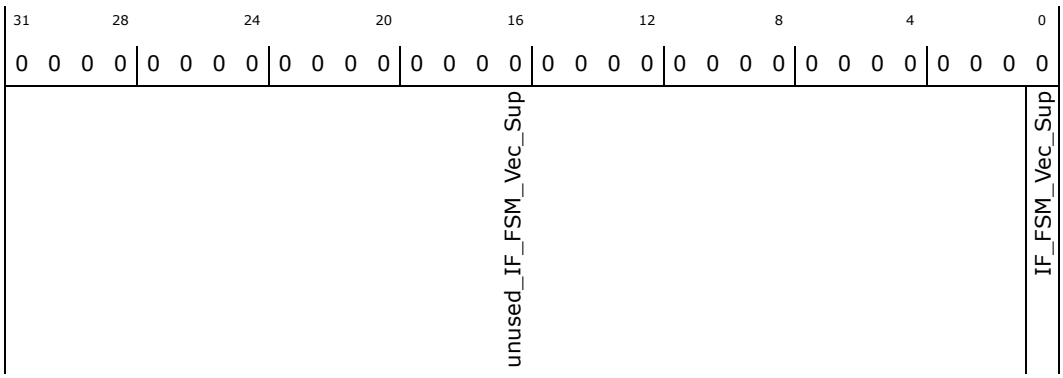
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3012Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_FSM_Vec_Sup):** Unused
0	0x0 RO	**IF_FSM_Vec_Sup:** FSM Vector support error state: if set the FSM Vector support is in error state

5.2.139 IF_FSM_Vec_Sup_Buf_full (is_2400_ifmt_ift_prim_IF_FSM_Vec_Sup_Buf_full)—Offset 30130h

FSM Vector Support Buffer Full: one-hot encoding flag signaling that the correspondent buffer is full

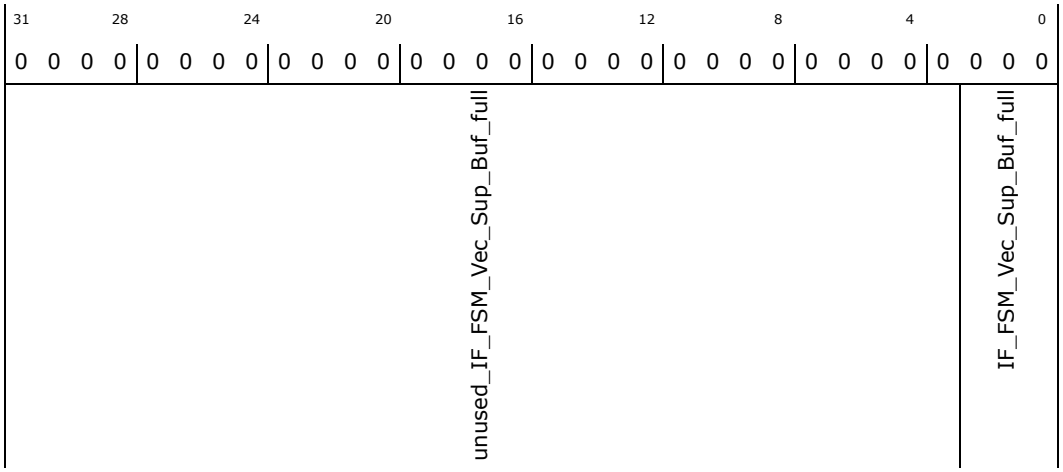
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30130h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved (unused_IF_FSM_Vec_Sup_Buf_full):** Unused
2:0	0x0 RO	**IF_FSM_Vec_Sup_Buf_full:** FSM Vector support buf full: one-hot encoding flag signaling that the correspondent buffer is full

5.2.140 IF_FSM_Vec_Sup_rd_accept (is_2400_ifmt_ift_prim_IF_FSM_Vec_Sup_rd_accept)—Offset 30134h

FSM Vector Support FIFO rd accept flag

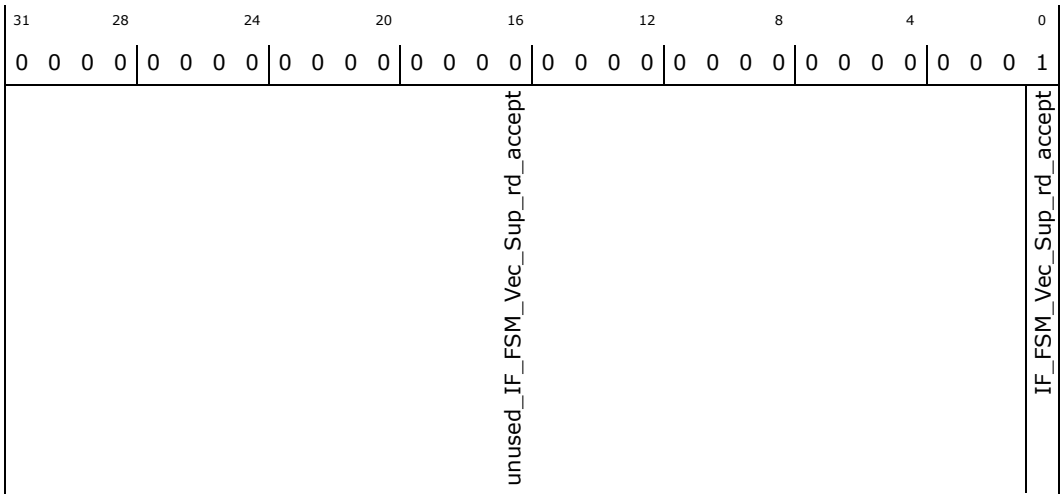
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30134h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_FSM_Vec_Sup_rd_accept):** Unused
0	0x1 RO	**IF_FSM_Vec_Sup_rd_accept:** FSM Vector Support FIFO rd accept flag

5.2.141 IF_Pixel_Fifo_status (is_2400_ifmt_ift_prim_IF_Pixel_Fifo_status)—Offset 30138h

Pixel FIFO Status

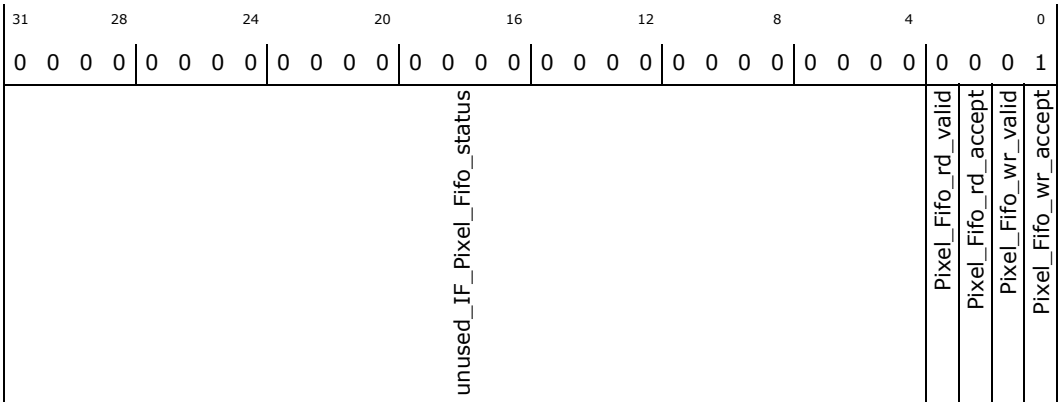
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30138h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_IF_Pixel_Fifo_status):** Unused
3	0x0 RO	**Pixel_Fifo_rd_valid:** Fifo has an element to be read
2	0x0 RO	**Pixel_Fifo_rd_accept:** IF accepts Pixel(s)
1	0x0 RO	**Pixel_Fifo_wr_valid:** There is an element to write into the FIFO
0	0x1 RO	**Pixel_Fifo_wr_accept:** FIFO is not full(1), FIFO is Full(0)

5.2.142 IF_sw_rst (is_2400_ifmt_ift_prim_b_IF_sw_rst)—Offset 30200h

Software Reset

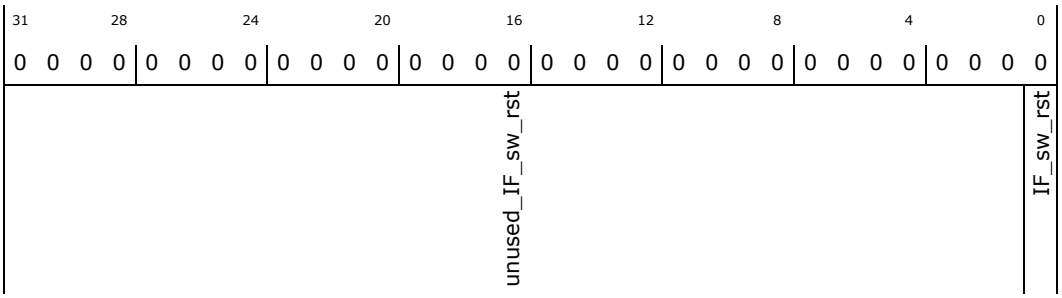
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_sw_rst):** Unused
0	0x0 RW	**IF_sw_rst:** Software Reset

5.2.143 IF_start_line (is_2400_ifmt_ift_prim_b_IF_start_line)—Offset 30204h

Start line: Number of lines to skip before passing the 1st line

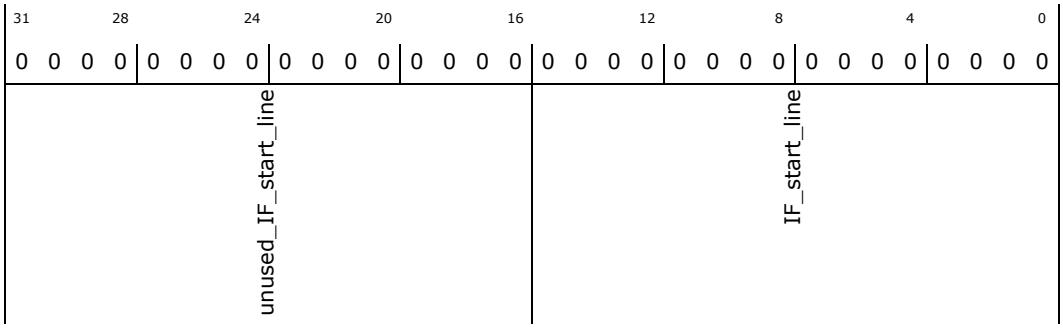
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30204h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_IF_start_line):** Unused
15:0	0x0 RW	**IF_start_line:** Start line: number of line to skip before passing the 1st line

5.2.144 IF_start_column (is_2400_ifmt_ift_prim_b_IF_start_column)—Offset 30208h

Start column: Number pixel component to skip before passing the 1st of a line

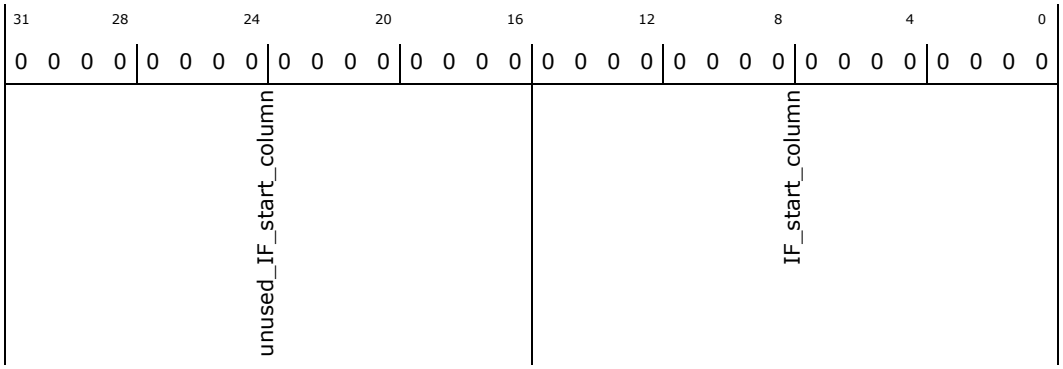
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30208h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_IF_start_column):** Unused
15:0	0x0 RW	**IF_start_column:** Start column: number pixel component to skip before passing the 1st of a line

5.2.145 IF_Cropped_height (is_2400_ifmt_ift_prim_b_IF_Cropped_height)—Offset 3020Ch

Cropped height: number of lines of the cropped image

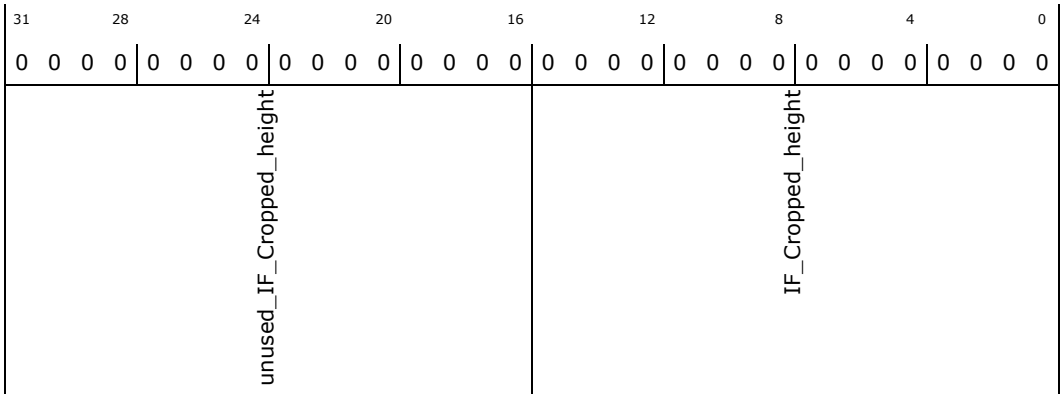
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3020Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_IF_Cropped_height):** Unused
15:0	0x0 RW	**IF_Cropped_height:** Cropped height: number of lines of the cropped image

5.2.146 IF_Cropped_width (is_2400_ifmt_ift_prim_b_IF_Cropped_width)—Offset 30210h

Cropped width: number of pixel component of the cropped image

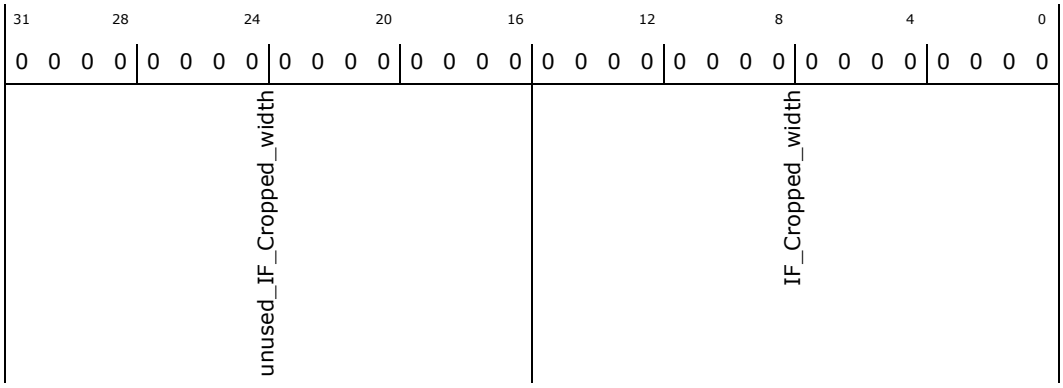
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30210h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_IF_Cropped_width):** Unused
15:0	0x0 RW	**IF_Cropped_width:** Cropped width: number of pixel component of the cropped image

5.2.147 IF_Vert_Decim (is_2400_ifmt_ift_prim_b_IF_Vert_Decim)—Offset 30214h

Vertical Decimation Factor

Vertical decimation factor of N means that only 1 every N lines is processed. When the de-interleaving factor is set to 2 (that is, Bayer), the IF will process 2 consecutive lines avery 2N lines.

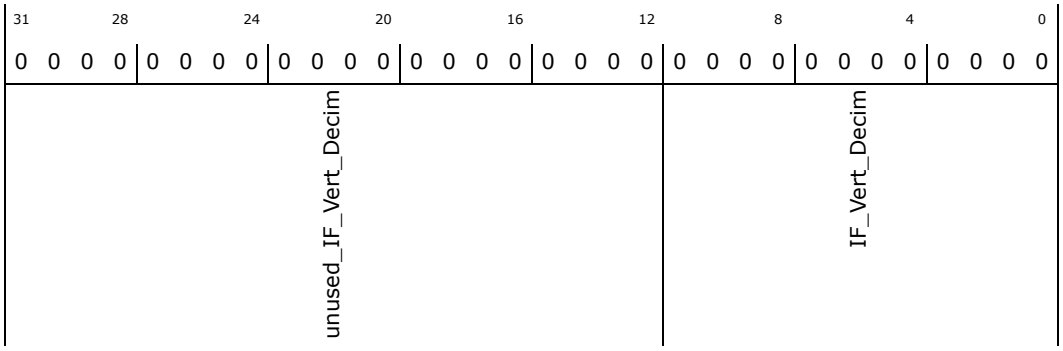
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30214h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_IF_Vert_Decim):** Unused
11:0	0x0 RW	**IF_Vert_Decim:** Vertical decimation factor. Vertical decimation factor of N means that only 1 every N lines is processed. When the de-interleaving factor is set to 2 (that is, Bayer), the IF will process 2 consecutive lines avery 2N lines.

5.2.148 IF_Horiz_Decim (is_2400_ifmt_ift_prim_b_IF_Horiz_Decim)—Offset 30218h

Horizontal decimation factor. Horizontal decimation factor of N means that only 1 every N pixel components is processed. When the de-interleaving factor is set to 2 (that is, Bayer), the IF will process 2 consecutive pixel components avery 2N pixel components.

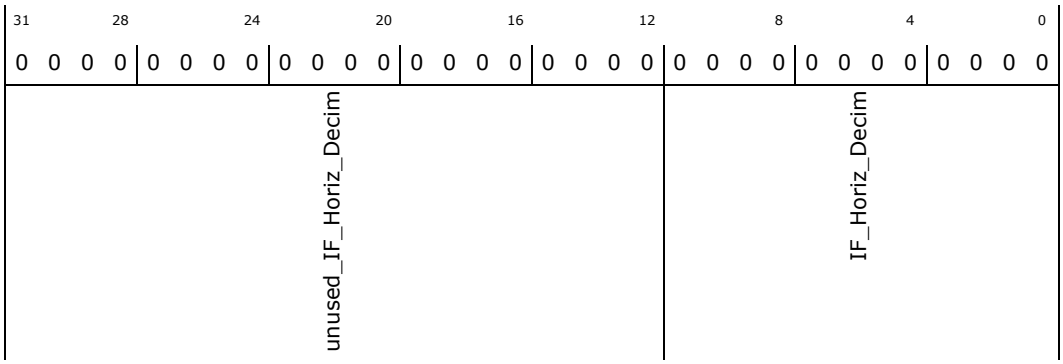
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30218h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_IF_Horiz_Decim):** Unused
11:0	0x0 RW	**IF_Horiz_Decim:** Horizontal decimation factor. Horizontal decimation factor of N means that only 1 every N pixel components is processed. When the de-interleaving factor is set to 2 (that is, Bayer), the IF will process 2 consecutive pixel components avery 2N pixel components.

5.2.149 IF_Horiz_Deinter (is_2400_ifmt_ift_prim_b_IF_Horiz_Deinter)—Offset 3021Ch

Horizontal De-interleaving Factor

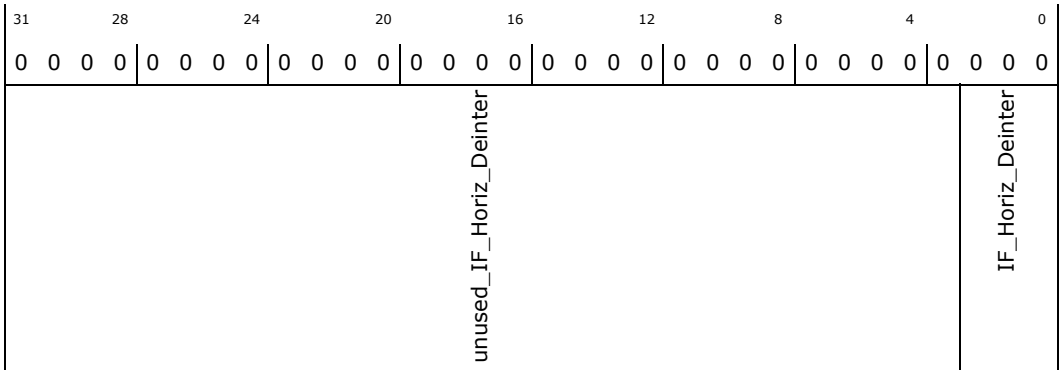
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3021Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved (unused_IF_Horiz_Deinter):** Unused
2:0	0x0 RW	**IF_Horiz_Deinter:** Horizontal de-interleaving factor

5.2.150 IF_Left_Pad (is_2400_ifmt_ift_prim_b_IF_Left_Pad)—Offset 30220h

Left padding: Pixel component to be padded at the beginning of each line

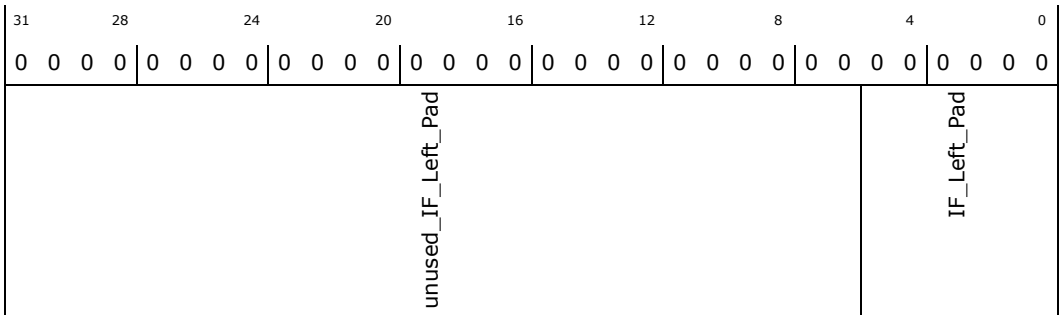
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30220h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_IF_Left_Pad):** Unused

Bit Range	Default and Access	Field Name (ID): Description
5:0	0x0 RW	**IF_Left_Pad:** Left padding: pixel component to be padded at the beginning of each line

5.2.151 IF_EOF_Offset (is_2400_ifmt_ift_prim_b_IF_EOF_Offset)—Offset 30224h

End of line offset in bytes: number of bytes to add at the address at the end of a line

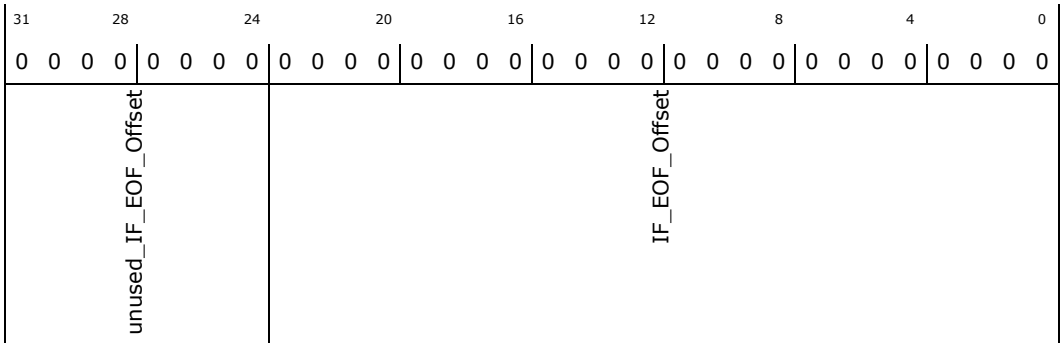
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30224h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved (unused_IF_EOF_Offset):** Unused
23:0	0x0 RW	**IF_EOF_Offset:** End of line offset in bytes: number of bytes to add at the address at the end of a line

5.2.152 IF_Start_addr (is_2400_ifmt_ift_prim_b_IF_Start_addr)—Offset 30228h

Local Memory Buffer Start Address (byte aligned)

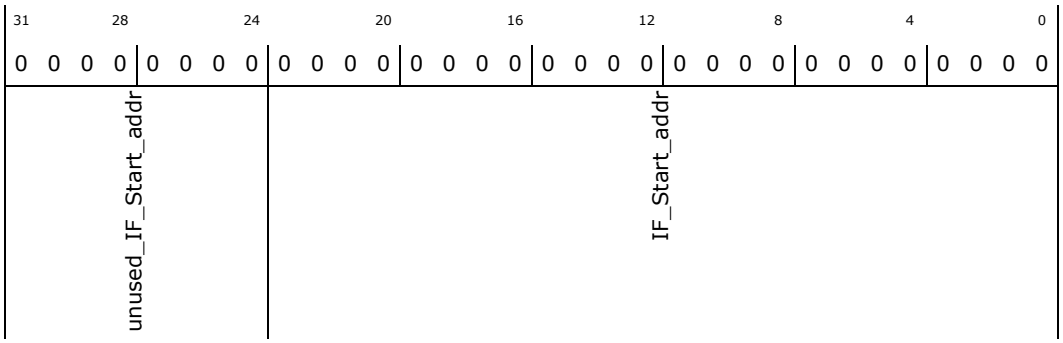
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30228h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved (unused_IF_Start_addr):** Unused
23:0	0x0 RW	**IF_Start_addr:** Local memory buffer start address (byte aligned)

5.2.153 IF_End_addr (is_2400_ifmt_ift_prim_b_IF_End_addr)—Offset 3022Ch

Local Memory Buffer End Address (byte aligned)

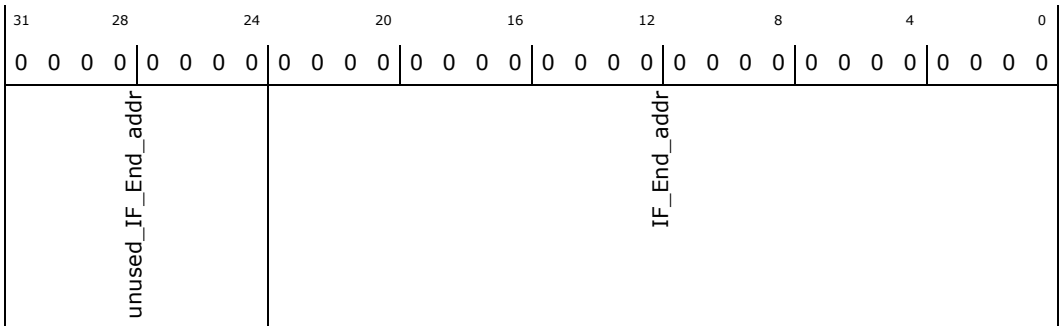
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3022Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved (unused_IF_End_addr):** Unused

Bit Range	Default and Access	Field Name (ID): Description
23:0	0x0 RW	**IF_End_addr:** Local memory buffer end address (byte aligned)

5.2.154 IF_incr (is_2400_ifmt_ift_prim_b_IF_incr)—Offset 30230h

Address word increment (word aligned). After every write the address is updated by adding this value times the word alignment.

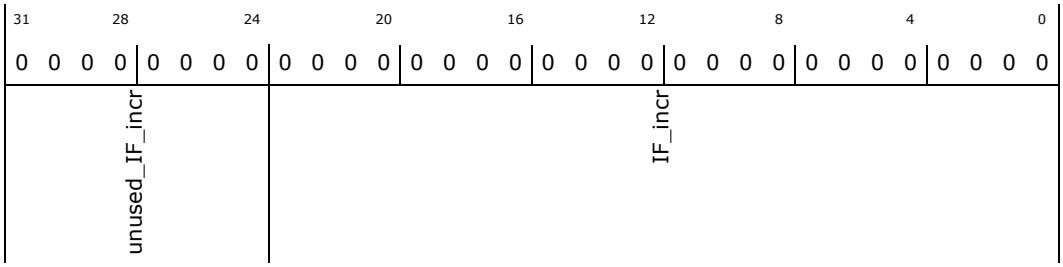
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30230h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved (unused_IF_incr):** Unused
23:0	0x0 RW	**IF_incr:** Address word increment (word aligned). After every write the address is updated by adding this value times the word alignment.

5.2.155 IF_YUV_420_format (is_2400_ifmt_ift_prim_b_IF_YUV_420_format)—Offset 30234h

YUV 420 format: set to work on legacy format YUV420

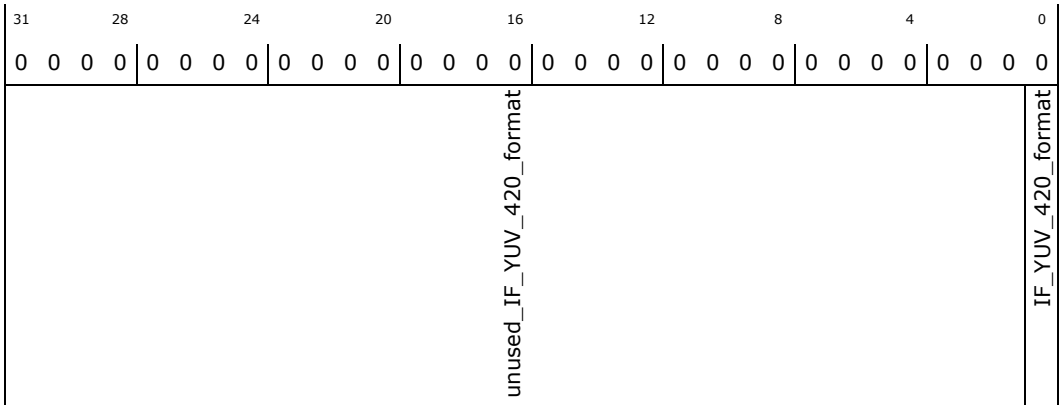
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30234h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_YUV_420_format):** Unused
0	0x0 RW	**IF_YUV_420_format:** YUV 420 format: set to work on legacy format YUV420

5.2.156 IF_Vsynch_active_low (is_2400_ifmt_ift_prim_b_IF_Vsynch_active_low)—Offset 30238h

Vertical Synch Active Low: Set to 1 if Vsynch and EndOfFrame are active low

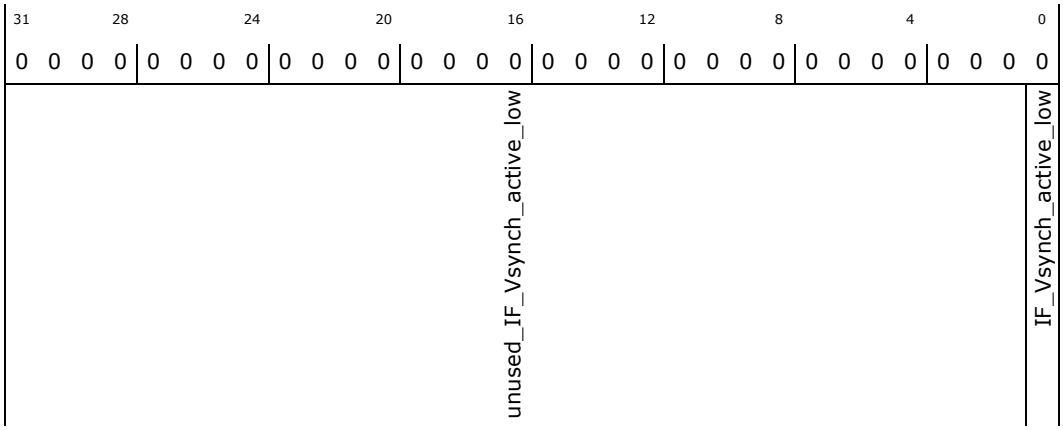
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30238h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_Vsynch_active_low):** Unused
0	0x0 RW	**IF_Vsynch_active_low:** Vertical synch active low: set to 1 if Vsynch and EndOfFrame are active low

5.2.157 IF_Hsynch_active_low (is_2400_ifmt_ift_prim_b_IF_Hsynch_active_low)—Offset 3023Ch

Horizontal Synch Active Low: set to 1 if Hsynch and EndOfLine are active low

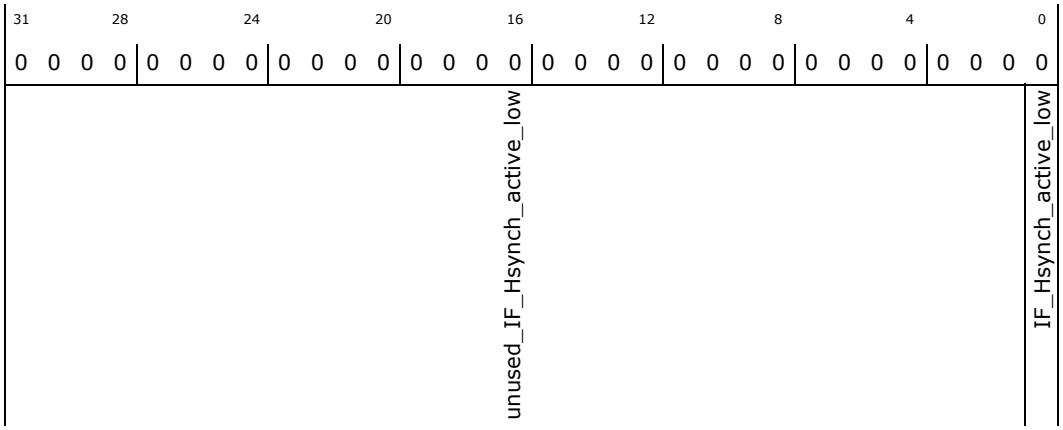
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3023Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_Hsynch_active_low):** Unused
0	0x0 RW	**IF_Hsynch_active_low:** Horizontal synch active low: set to 1 if Hsynch and EndOfLine are active low

5.2.158 IF_ReEnable (is_2400_ifmt_ift_prim_b_IF_ReEnable)—Offset 30240h

Re-enable status registers. When one of the FSM goes into error state, the status registers keep their value for post-debugging. Setting to 1 will re-enable status register.

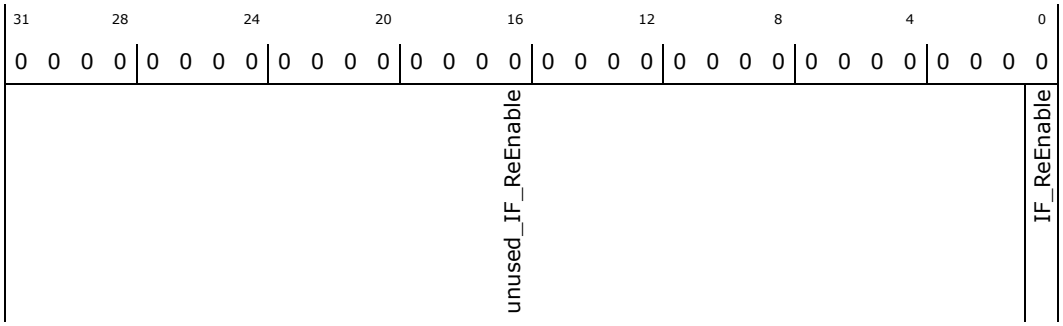
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30240h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_ReEnable):** Unused
0	0x0 RW	**IF_ReEnable:** Re-enable status registers. When one of the FSM goes into error state, the status registers keep their value for post-debugging. Setting to 1 will re-enable status register.

5.2.159 IF_block_input (is_2400_ifmt_ift_prim_b_IF_block_input)—Offset 30244h

Block input when no req: set to 1 to block data streaming input when no request is received

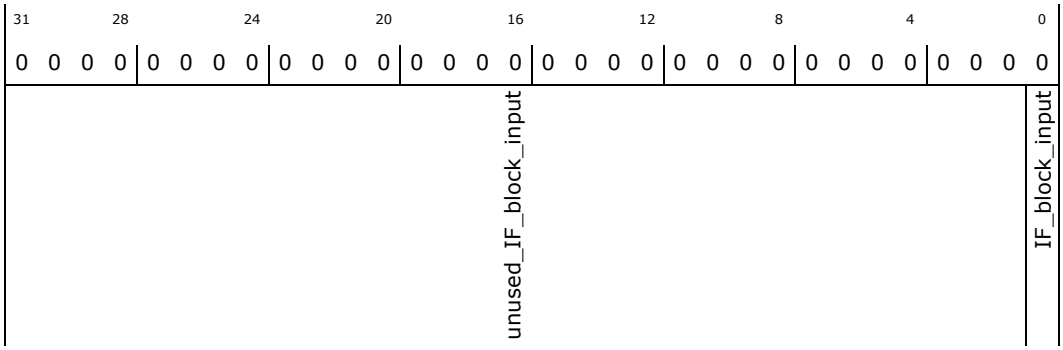
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30244h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_block_input):** Unused
0	0x0 RW	**IF_block_input:** Block input when no req: set to 1 to block data streaming input when no request is received

5.2.160 IF_Vert_Deinter (is_2400_ifmt_ift_prim_b_IF_Vert_Deinter)—Offset 30248h

Vertical De-interleaving Factor

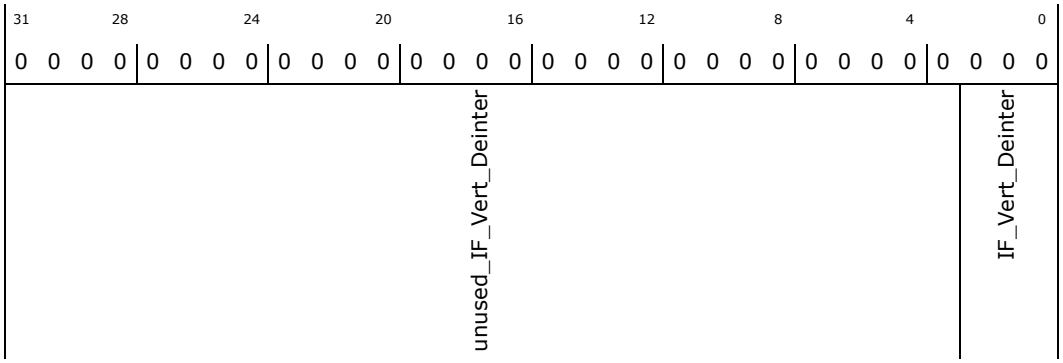
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30248h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved (unused_IF_Vert_Deinter):** Unused
2:0	0x0 RW	**IF_Vert_Deinter:** Vertical de-interleaving factor

5.2.161 IF_FSM_Sync_status (is_2400_ifmt_ift_prim_b_IF_FSM_Sync_status)—Offset 30300h

FSM Sync Status

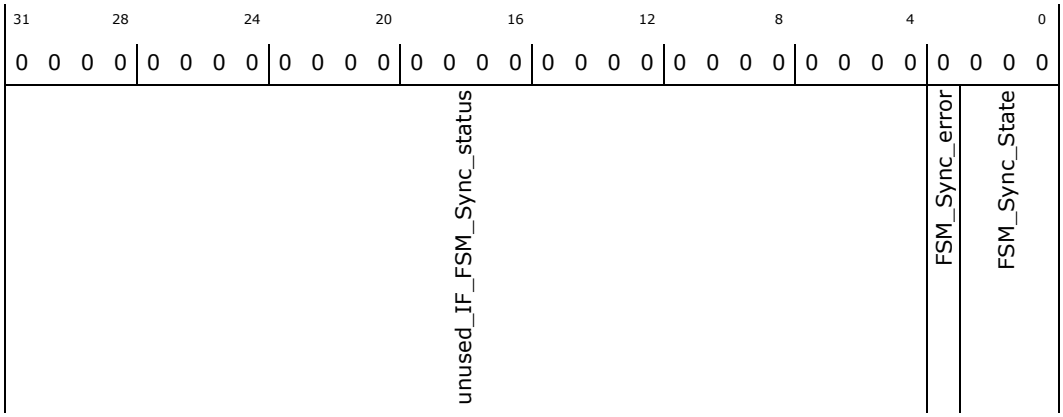
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30300h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_IF_FSM_Sync_status):** Unused
3	0x0 RO	**FSM_Sync_error:** Error flag: when set in combination with: Idle state an unknown command has been received; Req. Lines state an unexpected vsynch or eof has been received; Req. Vectors state an unexpected vsynch or eof has been received; another state an illegal state transition has occurred.
2:0	0x0 RO	**FSM_Sync_State:** FSM State: State: 0)Idle -- 1)Req Frame -- 2)Req. Lines -- 3)Req. Vectors -- 4)Send Acknowledge

5.2.162 FSM_Sync_counter (is_2400_ifmt_ift_prim_b_FSM_Sync_counter)—Offset 30304h

FSM Sync Counter:

Counts the processed items. For Request Frame counts the number of frames processed. For Request lines command counts the number of lines processed. For Request vectors command counts the number of vectors processed. The counter begins at value 1.

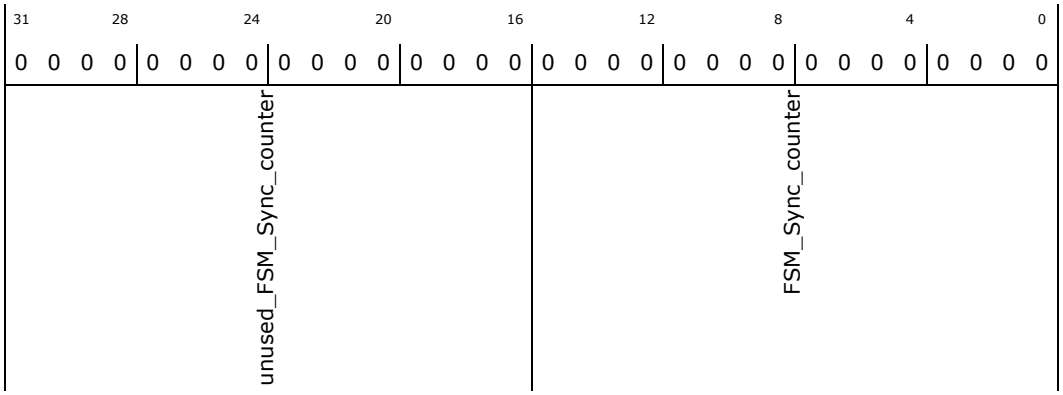
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30304h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_FSM_Sync_counter):** Unused
15:0	0x0 RO	**FSM_Sync_counter:** FSM Sync counter: counts the processed items. For Request Frame counts the number of frames processed. For Request lines command counts the number of lines processed. For Request vectors command counts the number of vectors processed. The counter begins at value 1.

5.2.163 FSM_Crop_status (is_2400_ifmt_ift_prim_b_FSM_Crop_status)—Offset 30308h

FSM Crop Status

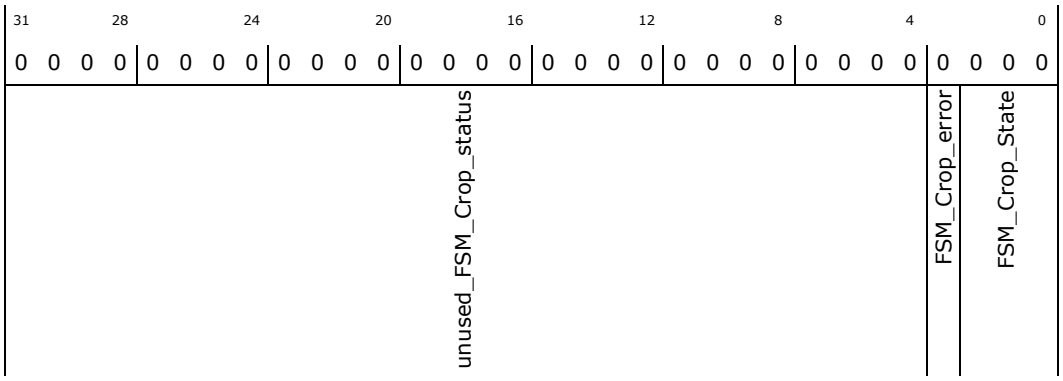
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30308h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_FSM_Crop_status):** Unused
3	0x0 RO	**FSM_Crop_error:** Error flag: when set in combination with: Crop Line state unexpected synch or eof has been received; Req. Lines state unexpected vsynch or eof has been received; Req. Vectors state unexpected vsynch or eof has been received; another state an illegal state transition has occurred.
2:0	0x0 RO	**FSM_Crop_State:** FSM State: State: 0)Idle -- 1)Wait Line -- 2)Crop Line -- 3)Crop Pixel -- 4)Pass pixel -- 5) Pass Line

5.2.164 FSM_Crop_line_counter (is_2400_ifmt_ift_prim_b_FSM_Crop_line_counter)—Offset 3030Ch

FSM Crop Line Counter

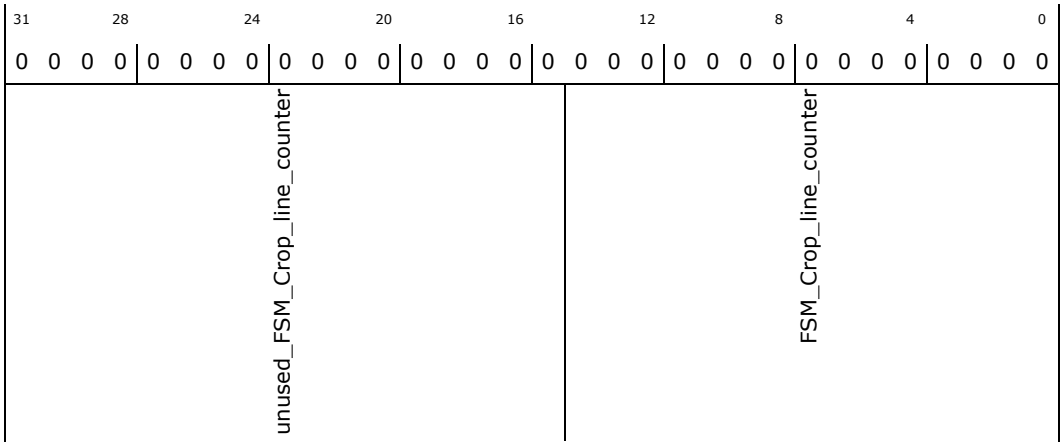
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3030Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:15	0x0 RW	**Reserved (unused_FSM_Crop_line_counter):** Unused
14:0	0x0 RO	**FSM_Crop_line_counter:** FSM Crop line counter

5.2.165 FSM_Crop_pixel_counter (is_2400_ifmt_ift_prim_b_FSM_Crop_pixel_counter)—Offset 30310h

FSM Crop Pixel Component Counter

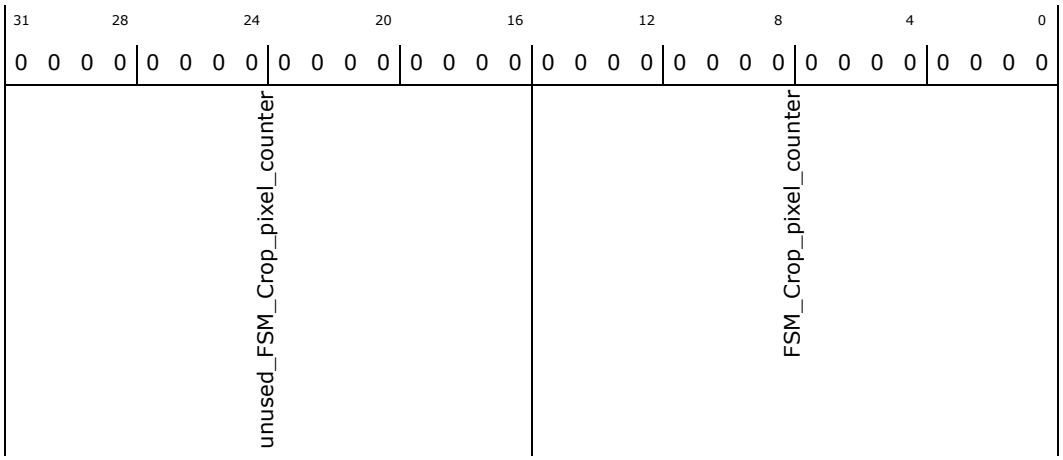
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30310h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_FSM_Crop_pixel_counter):** Unused
15:0	0x0 RO	**FSM_Crop_pixel_counter:** FSM Crop pixel component counter

5.2.166 FSM_Deinterl_idx_buffer (is_2400_ifmt_ift_prim_b_FSM_Deinterl_idx_buffer)—Offset 30314h

FSM De-interleaving idx Buffer

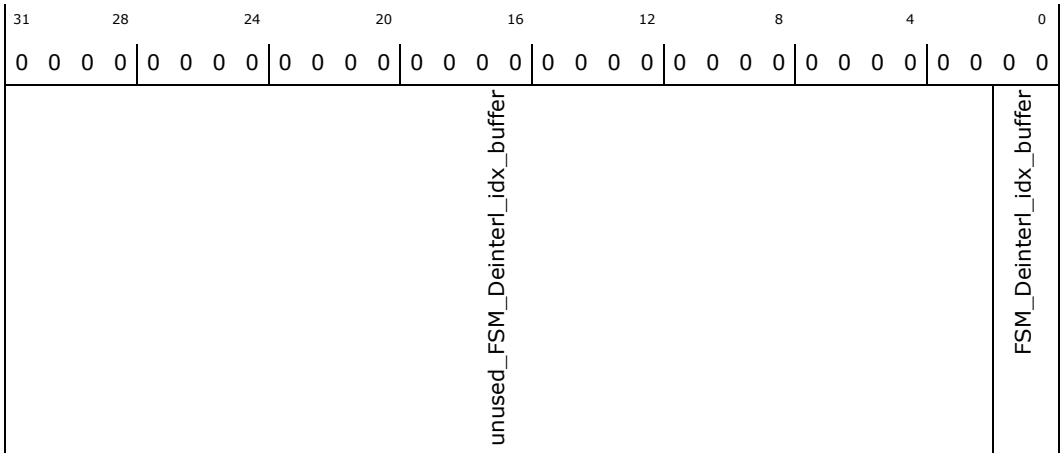
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30314h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_FSM_Deinterl_idx_buffer):** Unused
1:0	0x0 RO	**FSM_Deinterl_idx_buffer:** FSM De-interleaving idx buffer

5.2.167 FSM_Horiz_Decim_cnt (is_2400_ifmt_ift_prim_b_FSM_Horiz_Decim_cnt)—Offset 30318h

FSM Horizontal Decimation Counter

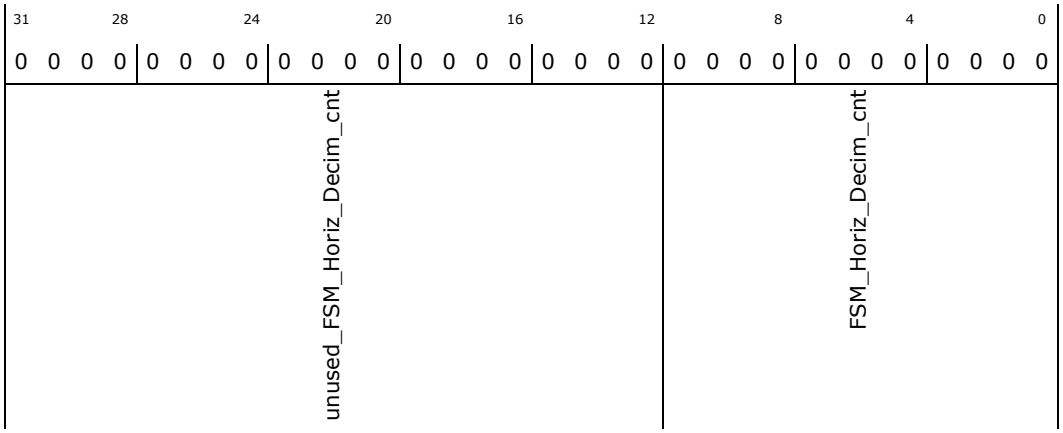
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30318h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_FSM_Horiz_Decim_cnt):** Unused
11:0	0x0 RO	**FSM_Horiz_Decim_cnt:** FSM Horizontal Decimation counter

5.2.168 FSM_Vertic_Decim_cnt (is_2400_ifmt_ift_prim_b_FSM_Vertic_Decim_cnt)—Offset 3031Ch

FSM Vertical Decimation Counter

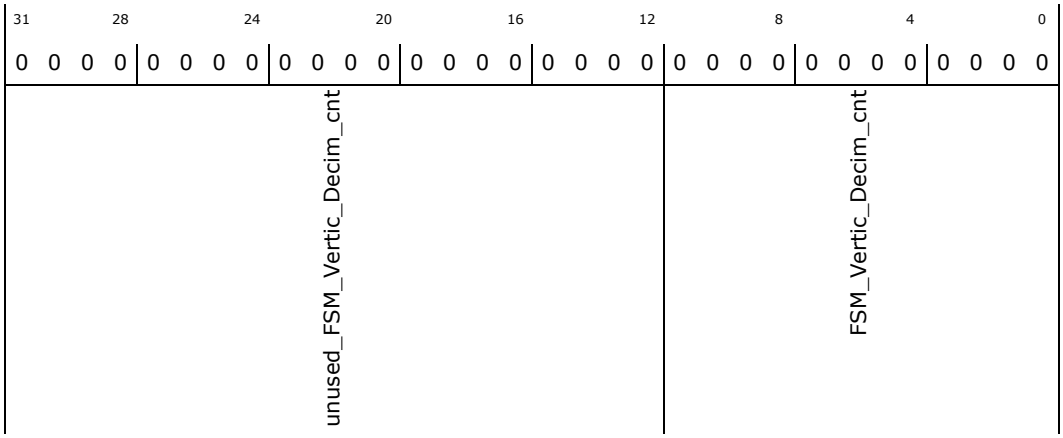
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3031Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_FSM_Vertic_Decim_cnt):** Unused
11:0	0x0 RO	**FSM_Vertic_Decim_cnt:** FSM Vertical decimation counter

5.2.169 FSM_Vertic_Block_Decim_cnt (is_2400_ifmt_ift_prim_b_FSM_Vertic_Block_Decim_cnt) —Offset 30320h

FSM Vertical Block Decimation Counter

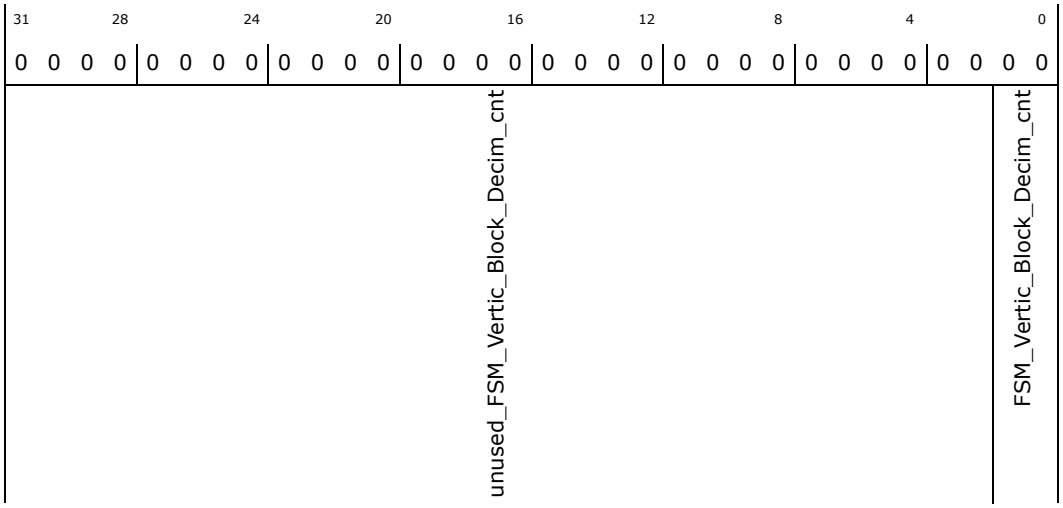
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30320h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_FSM_Vertic_Block_Decim_cnt):** Unused
1:0	0x0 RO	**FSM_Vertic_Block_Decim_cnt:** FSM Vertical block decimation counter

5.2.170 IF_FSM_Padding_status (is_2400_ifmt_ift_prim_b_IF_FSM_Padding_status)—Offset 30324h

FSM Padding Status

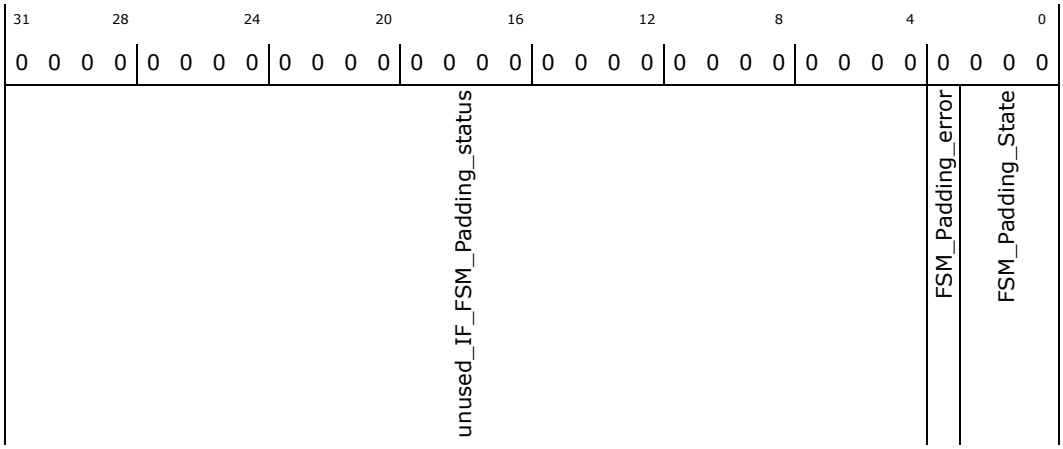
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30324h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_IF_FSM_Padding_status):** Unused
3	0x0 RO	**FSM_Padding_error:** Error flag: when set in combination with: Left Padding state an unexpected vsynch or hsync has been received; Write state an unexpected vsynch or hsync has been received; Right padding state unexpected vsynch has been received; Send EOL state an unexpected vsynch has been received; another state an illegal state transition has occurred.
2:0	0x0 RO	**FSM_Padding_State:** FSM State: State: 0)Idle -- 1)Left Padding -- 2)Write -- 3)Right padding -- 4)Sending EOL

5.2.171 IF_FSM_Padding_elem_idx (is_2400_ifmt_ift_prim_b_IF_FSM_Padding_elem_idx)—Offset 30328h

FSM Padding Element Index Counter

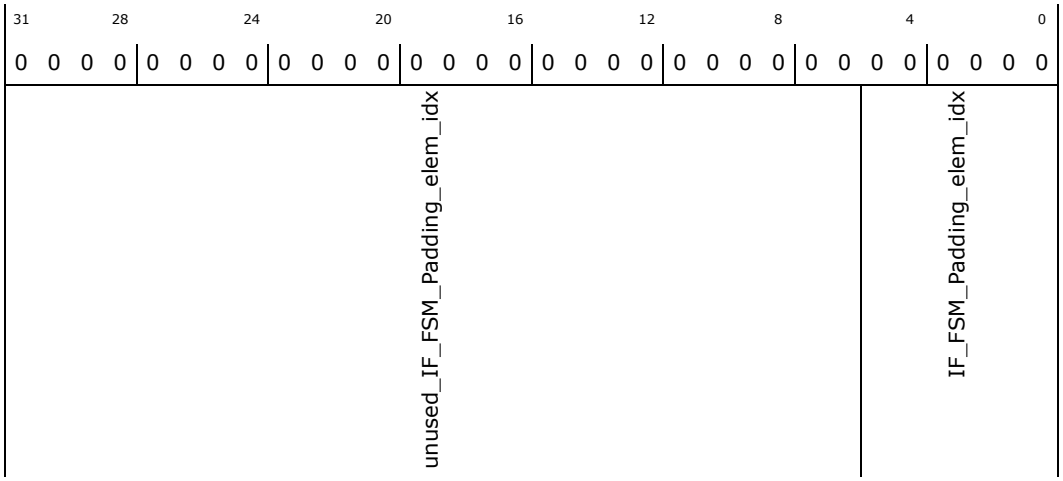
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30328h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_IF_FSM_Padding_elem_idx):** Unused
5:0	0x0 RO	**IF_FSM_Padding_elem_idx:** FSM Padding element index counter

5.2.172 IF_FSM_Vec_Sup (is_2400_ifmt_ift_prim_b_IF_FSM_Vec_Sup)—Offset 3032Ch

FSM Vector Support Error State: if set the FSM Vector support is in error state

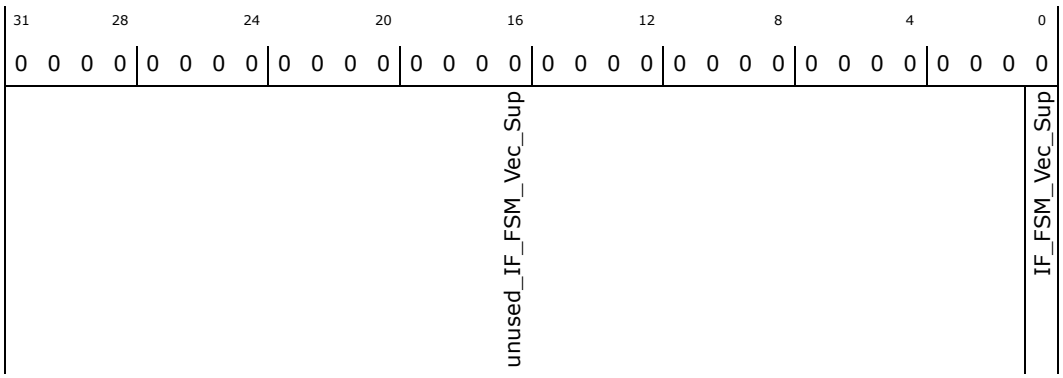
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3032Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_FSM_Vec_Sup):** Unused
0	0x0 RO	**IF_FSM_Vec_Sup:** FSM Vector support error state: if set the FSM Vector support is in error state

5.2.173 IF_FSM_Vec_Sup_Buf_full (is_2400_ifmt_ift_prim_b_IF_FSM_Vec_Sup_Buf_full)—Offset 30330h

FSM Vector Support Buf Full: one-hot encoding flag signaling that the correspondent buffer is full

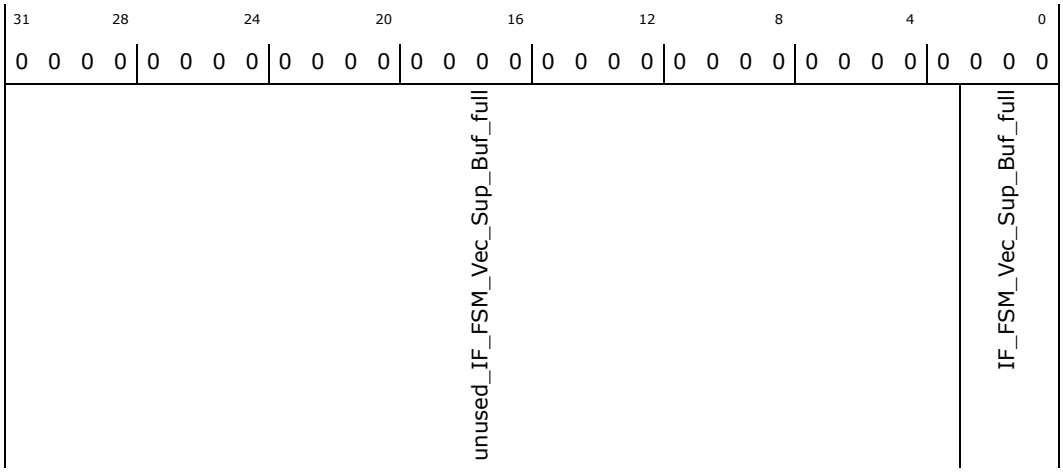
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30330h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved (unused_IF_FSM_Vec_Sup_Buf_full):** Unused
2:0	0x0 RO	**IF_FSM_Vec_Sup_Buf_full:** FSM Vector support buf full: one-hot encoding flag signaling that the correspondent buffer is full

5.2.174 IF_FSM_Vec_Sup_rd_accept (is_2400_ifmt_ift_prim_b_IF_FSM_Vec_Sup_rd_accept)—Offset 30334h

FSM Vector Support FIFO rd accept flag

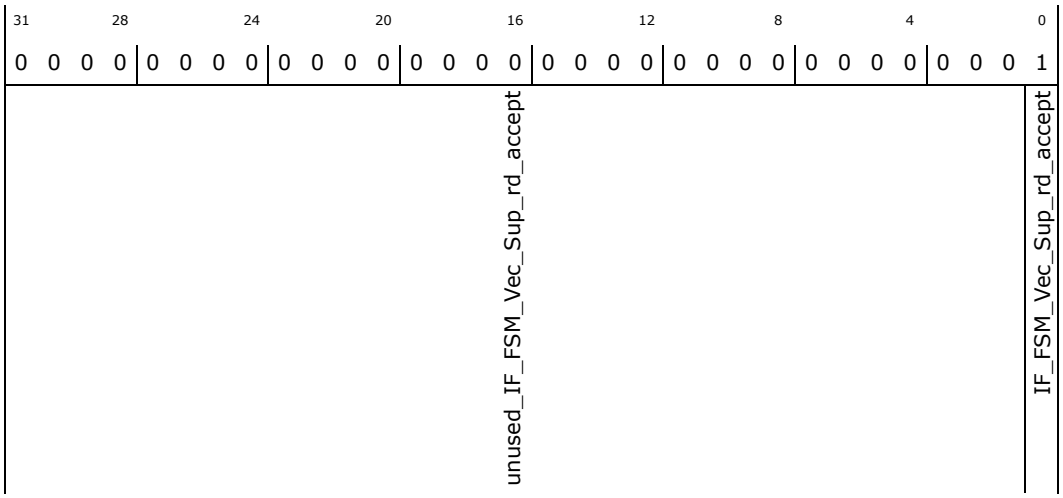
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30334h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_FSM_Vec_Sup_rd_accept):** Unused
0	0x1 RO	**IF_FSM_Vec_Sup_rd_accept:** FSM Vector Support FIFO rd accept flag

5.2.175 IF_Pixel_Fifo_status (is_2400_ifmt_ift_prim_b_IF_Pixel_Fifo_status)—Offset 30338h

Pixel FIFO status

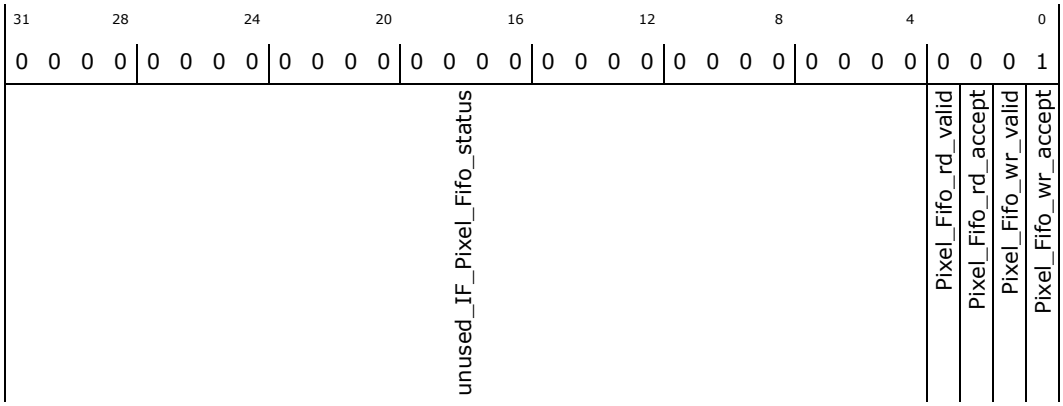
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30338h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_IF_Pixel_Fifo_status):** Unused
3	0x0 RO	**Pixel_Fifo_rd_valid:** Fifo has an element to be read
2	0x0 RO	**Pixel_Fifo_rd_accept:** IF accepts Pixel(s)
1	0x0 RO	**Pixel_Fifo_wr_valid:** There is an element to write into the Fifo
0	0x1 RO	**Pixel_Fifo_wr_accept:** FIFO is not full(1), FIFO is Full(0)

5.2.176 IF_sw_rst (is_2400_ifmt_ift_sec_IF_sw_rst)—Offset 30400h

Software Reset

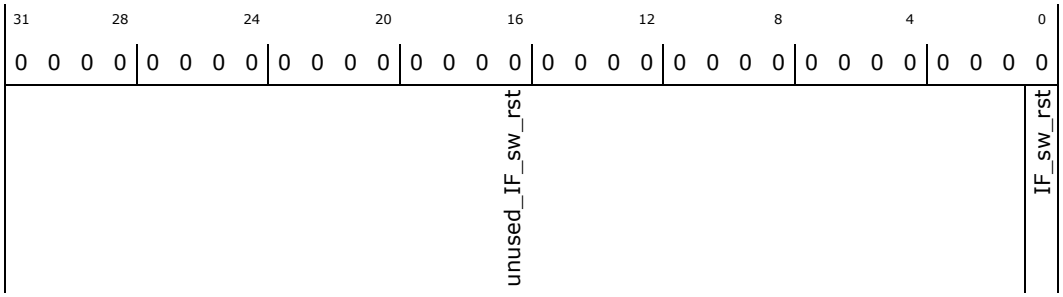
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30400h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_sw_rst):** Unused
0	0x0 RW	**IF_sw_rst:** Software Reset

5.2.177 IF_start_line (is_2400_ifmt_ift_sec_IF_start_line)—Offset 30404h

Start line: number of line to skip before passing the 1st line

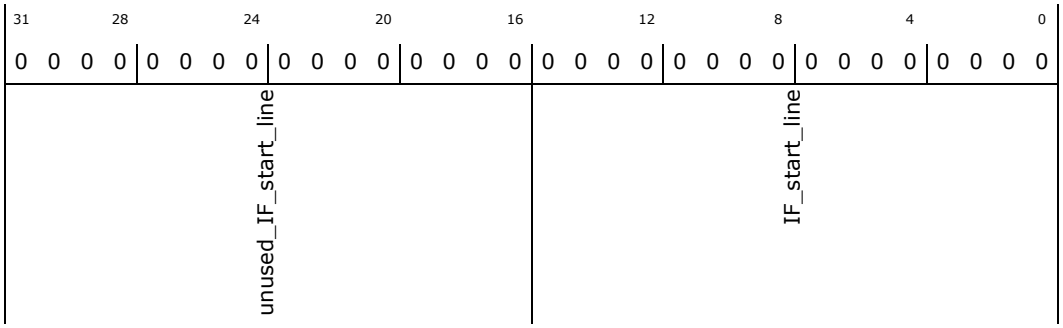
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30404h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_IF_start_line):** Unused
15:0	0x0 RW	**IF_start_line:** Start line: number of line to skip before passing the 1st line

5.2.178 IF_start_column (is_2400_ifmt_ift_sec_IF_start_column)—Offset 30408h

Start column: Number of pixel components to skip before passing the 1st of a line

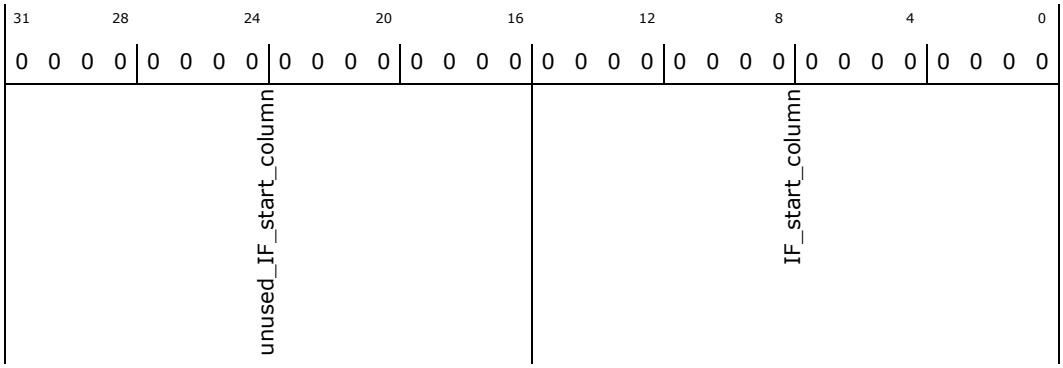
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30408h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_IF_start_column):** Unused
15:0	0x0 RW	**IF_start_column:** Start column: number pixel component to skip before passing the 1st of a line

5.2.179 IF_Cropped_height (is_2400_ifmt_ift_sec_IF_Cropped_height)—Offset 3040Ch

Cropped height: Number of lines of the cropped image

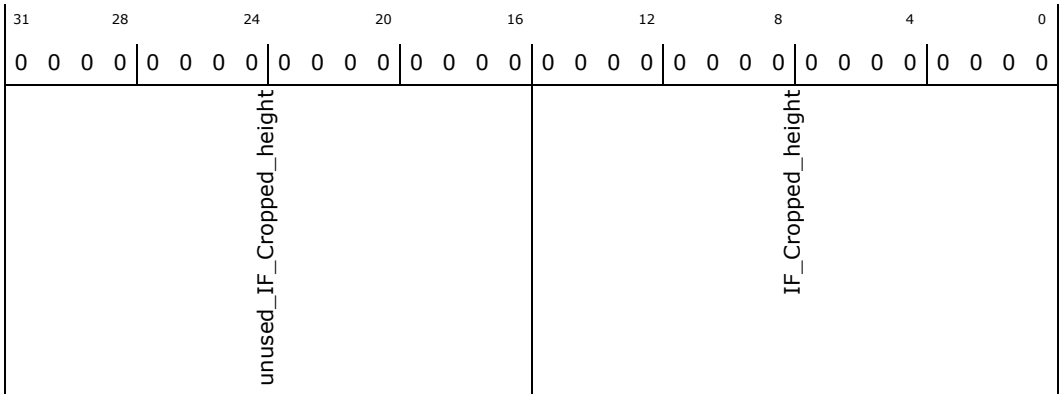
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3040Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_IF_Cropped_height):** Unused
15:0	0x0 RW	**IF_Cropped_height:** Cropped height: number of lines of the cropped image

5.2.180 IF_Cropped_width (is_2400_ifmt_ift_sec_IF_Cropped_width)—Offset 30410h

Cropped width: number of pixel component of the cropped image

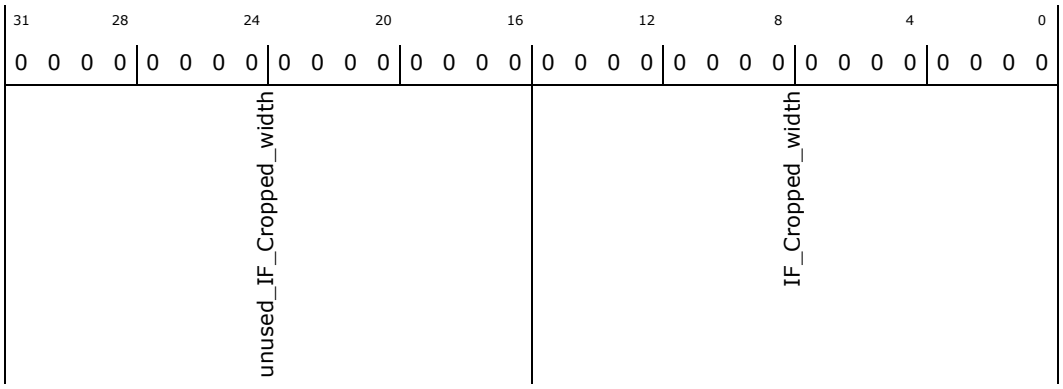
Access Method

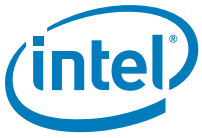
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30410h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h





Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_IF_Cropped_width):** Unused
15:0	0x0 RW	**IF_Cropped_width:** Cropped width: number of pixel component of the cropped image

5.2.181 IF_Vert_Decim (is_2400_ifmt_ift_sec_IF_Vert_Decim)—Offset 30414h

Vertical decimation factor. Vertical decimation factor of N means that only 1 every N lines is processed. When the de-interleaving factor is set to 2 (that is, Bayer), the IF will process 2 consecutive lines avery 2N lines.

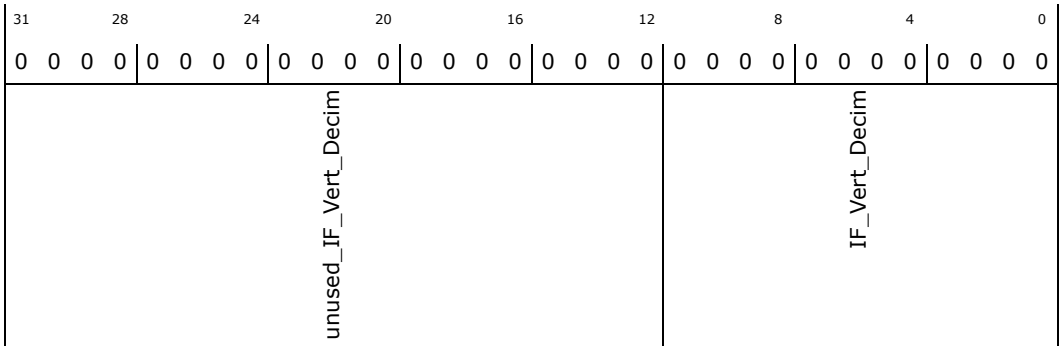
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30414h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_IF_Vert_Decim):** Unused
11:0	0x0 RW	**IF_Vert_Decim:** Vertical decimation factor. Vertical decimation factor of N means that only 1 every N lines is processed. When the de-interleaving factor is set to 2 (that is, Bayer), the IF will process 2 consecutive lines avery 2N lines.

5.2.182 IF_Horiz_Decim (is_2400_ifmt_ift_sec_IF_Horiz_Decim)—Offset 30418h

Horizontal Decimation Factor

Horizontal decimation factor of N means that only 1 every N pixel components is processed. When the de-interleaving factor is set to 2 (that is, Bayer), the IF will process 2 consecutive pixel components avery 2N pixel components.

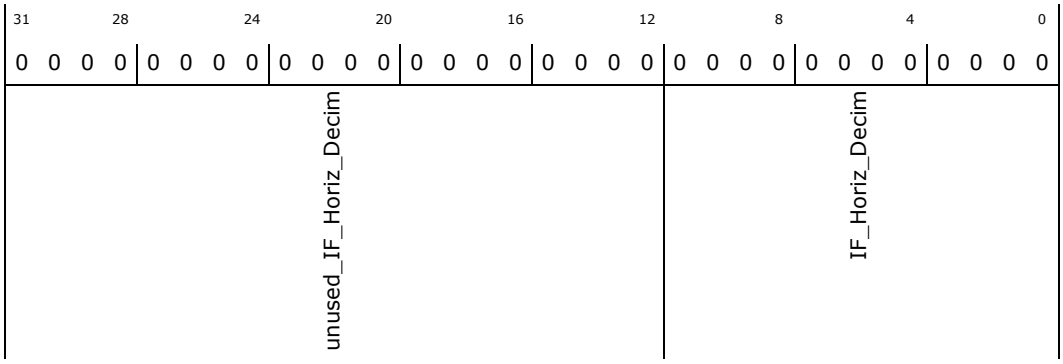
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30418h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_IF_Horiz_Decim):** Unused
11:0	0x0 RW	**IF_Horiz_Decim:** Horizontal decimation factor. Horizontal decimation factor of N means that only 1 every N pixel components is processed. When the de-interleaving factor is set to 2 (that is, Bayer), the IF will process 2 consecutive pixel components avery 2N pixel components.

5.2.183 IF_Horiz_Deinter (is_2400_ifmt_ift_sec_IF_Horiz_Deinter)—Offset 3041Ch

Horizontal De-interleaving Factor

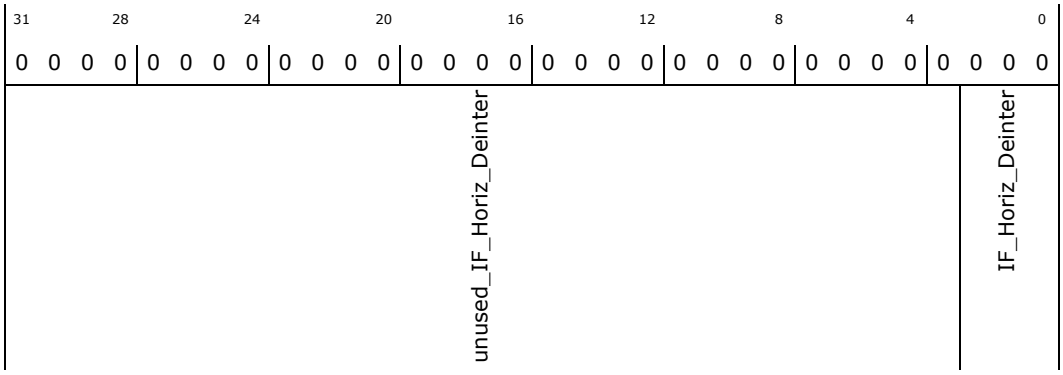
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3041Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved (unused_IF_Horiz_Deinter):** Unused
2:0	0x0 RW	**IF_Horiz_Deinter:** Horizontal de-interleaving factor

5.2.184 IF_Left_Pad (is_2400_ifmt_ift_sec_IF_Left_Pad)—Offset 30420h

Left padding: pixel component to be padded at the beginning of each line

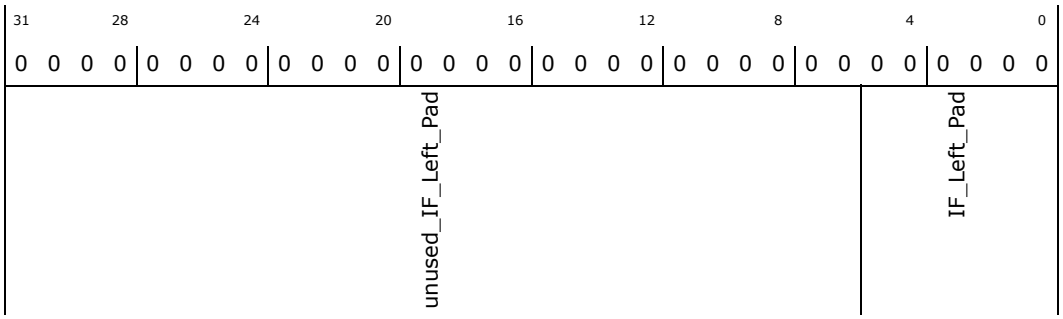
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30420h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_IF_Left_Pad):** Unused
5:0	0x0 RW	**IF_Left_Pad:** Left padding: pixel component to be padded at the beginning of each line

5.2.185 IF_EOF_Offset (is_2400_ifmt_ift_sec_IF_EOF_Offset)—Offset 30424h

End of line offset in bytes: number of bytes to add at the address at the end of a line

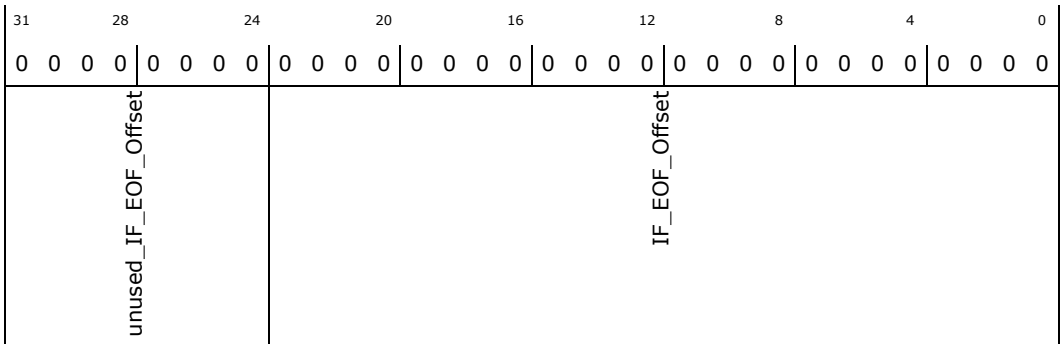
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30424h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved (unused_IF_EOF_Offset):** Unused
23:0	0x0 RW	**IF_EOF_Offset:** End of line offset in bytes: number of bytes to add at the address at the end of a line

5.2.186 IF_Start_addr (is_2400_ifmt_ift_sec_IF_Start_addr)—Offset 30428h

Local Memory Buffer Start Address (byte aligned)

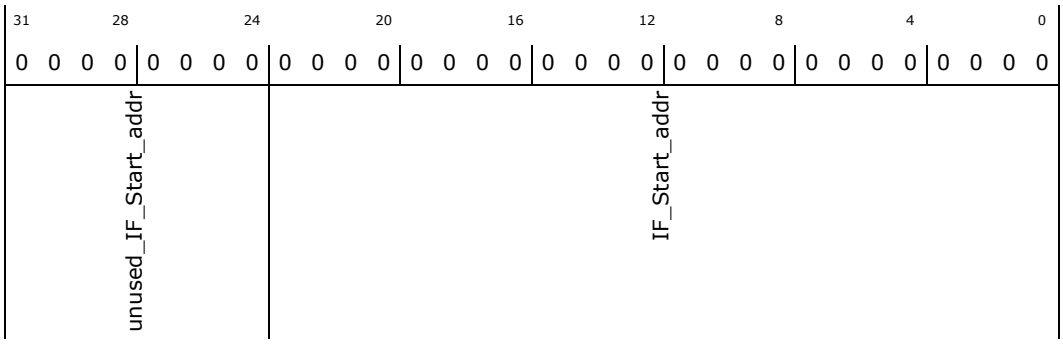
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30428h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved (unused_IF_Start_addr):** Unused

Bit Range	Default and Access	Field Name (ID): Description
23:0	0x0 RW	**IF_Start_addr:** Local memory buffer start address (byte aligned)

5.2.187 IF_End_addr (is_2400_ifmt_ift_sec_IF_End_addr)—Offset 3042Ch

Local memory buffer end address (byte aligned)

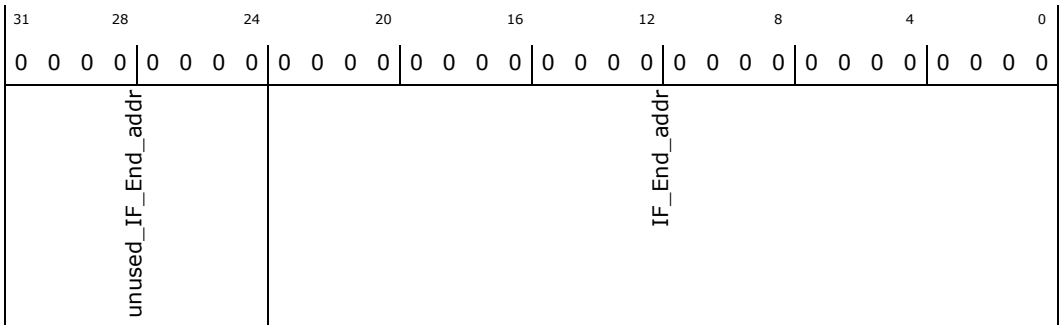
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3042Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved (unused_IF_End_addr):** Unused
23:0	0x0 RW	**IF_End_addr:** Local memory buffer end address (byte aligned)

5.2.188 IF_incr (is_2400_ifmt_ift_sec_IF_incr)—Offset 30430h

Address word increment (word aligned). After every write the address is updated by adding this value times the word alignment.

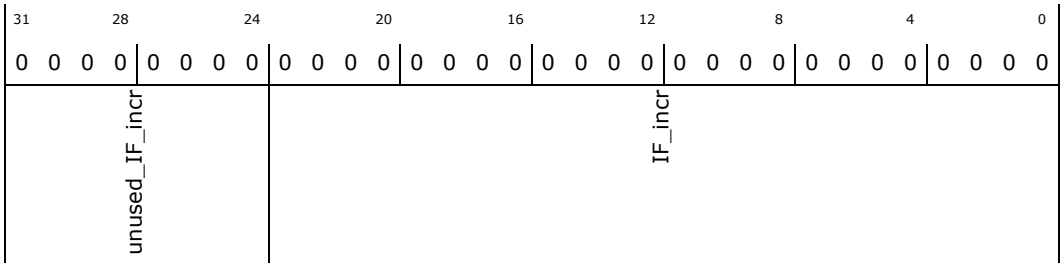
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30430h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved (unused_IF_incr):** Unused
23:0	0x0 RW	**IF_incr:** Address word increment (word aligned). After every write the address is updated by adding this value times the word alignment.

5.2.189 IF_YUV_420_format (is_2400_ifmt_ift_sec_IF_YUV_420_format)—Offset 30434h

YUV 420 format: set to work on legacy format YUV420

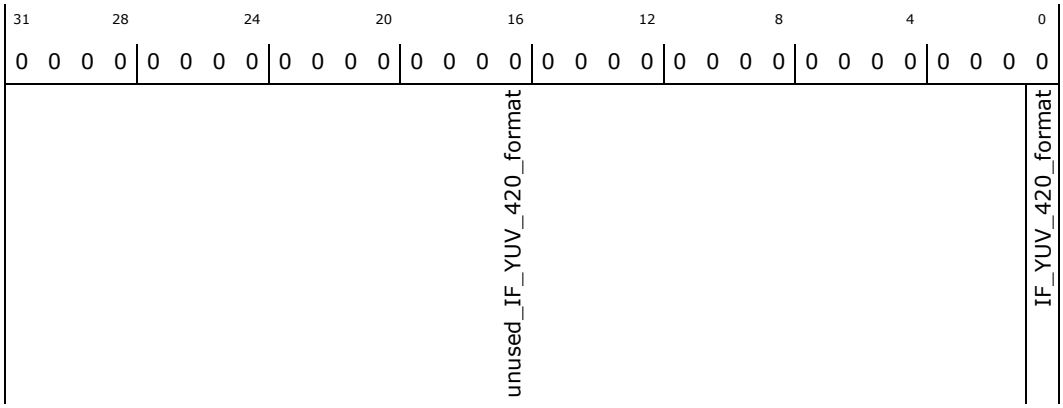
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30434h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_YUV_420_format):** Unused

Bit Range	Default and Access	Field Name (ID): Description
0	0x0 RW	**IF_YUV_420_format:** YUV 420 format: set to work on legacy format YUV420

5.2.190 IF_Vsynch_active_low (is_2400_ifmt_ift_sec_IF_Vsynch_active_low)—Offset 30438h

Vertical synch active low: set to 1 if Vsynch and EndOfFrame are active low

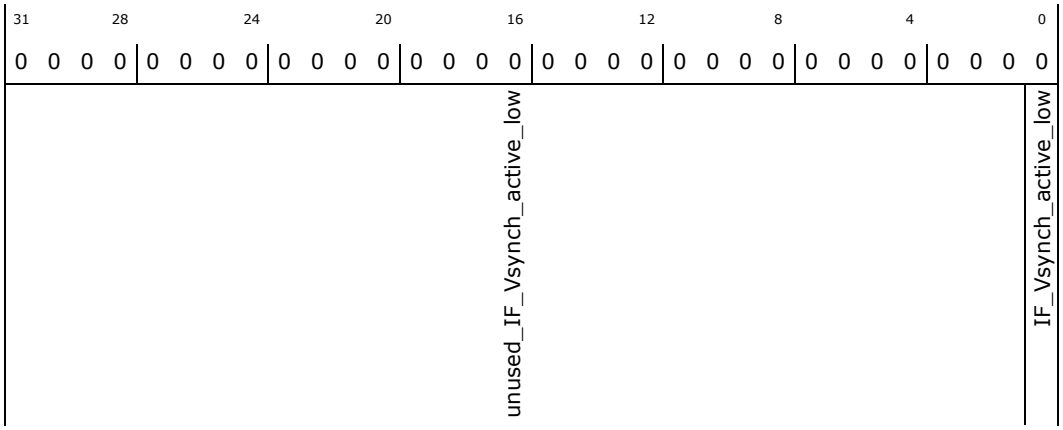
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30438h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_Vsynch_active_low):** Unused
0	0x0 RW	**IF_Vsynch_active_low:** Vertical synch active low: set to 1 if Vsynch and EndOfFrame are active low

5.2.191 IF_Hsynch_active_low (is_2400_ifmt_ift_sec_IF_Hsynch_active_low)—Offset 3043Ch

Horizontal synch active low: set to 1 if Hsynch and EndOfLine are active low

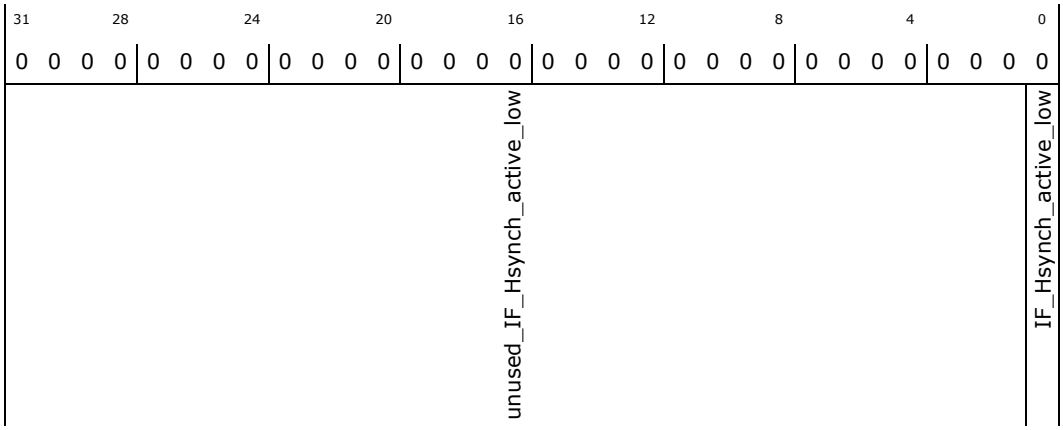
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3043Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_Hsynch_active_low):** Unused
0	0x0 RW	**IF_Hsynch_active_low:** Horizontal synch active low: set to 1 if Hsynch and EndOfLine are active low

5.2.192 IF_ReEnable (is_2400_ifmt_ift_sec_IF_ReEnable)—Offset 30440h

Re-enable status registers. When one of the FSM goes into error state, the status registers keep their value for post-debugging. Setting to 1 will re-enable status register.

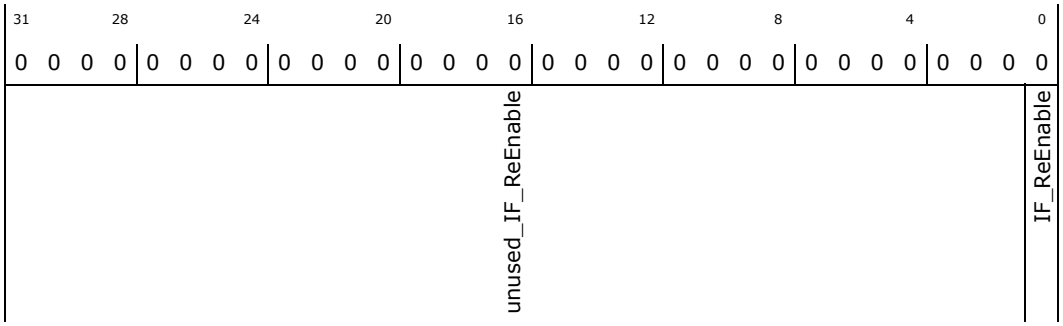
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30440h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_ReEnable):** Unused
0	0x0 RW	**IF_ReEnable:** Re-enable status registers. When one of the FSM goes into error state, the status registers keep their value for post-debugging. Setting to 1 will re-enable status register.

5.2.193 IF_block_input (is_2400_ifmt_ift_sec_IF_block_input)—Offset 30444h

Block input when no req: set to 1 to block data streaming input when no request is received

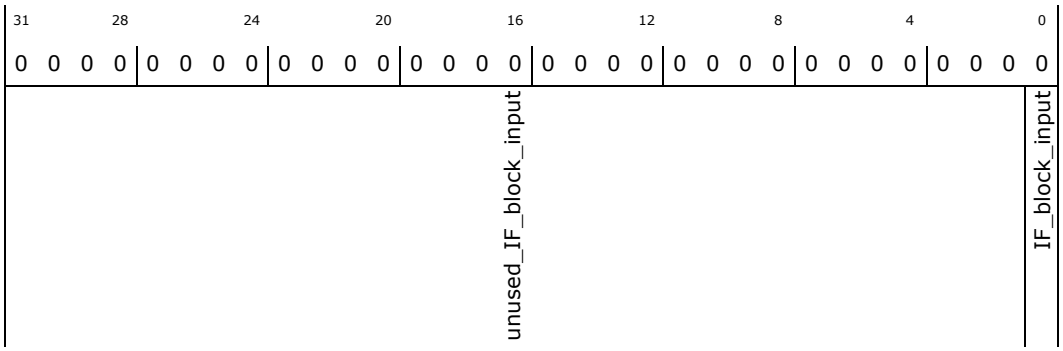
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30444h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_block_input):** Unused
0	0x0 RW	**IF_block_input:** Block input when no req: set to 1 to block data streaming input when no request is received

5.2.194 IF_Vert_Deinter (is_2400_ifmt_ift_sec_IF_Vert_Deinter)—Offset 30448h

Vertical de-interleaving factor

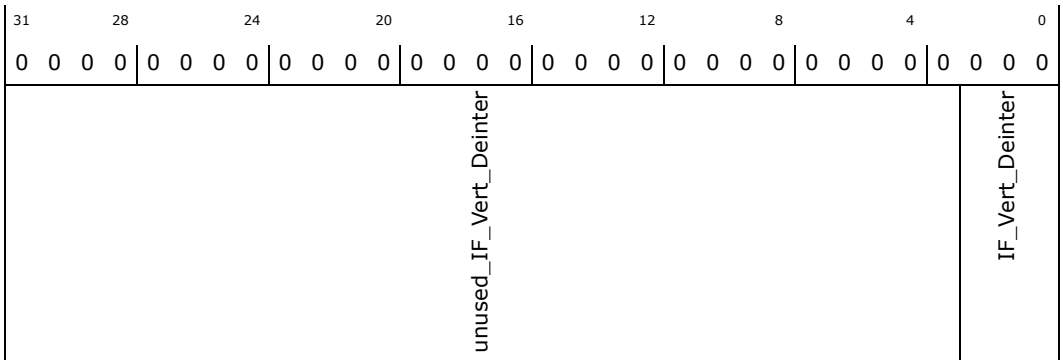
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30448h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved (unused_IF_Vert_Deinter):** Unused
2:0	0x0 RW	**IF_Vert_Deinter:** Vertical de-interleaving factor

5.2.195 IF_FSM_Sync_status (is_2400_ifmt_ift_sec_IF_FSM_Sync_status)—Offset 30500h

FSM Sync status

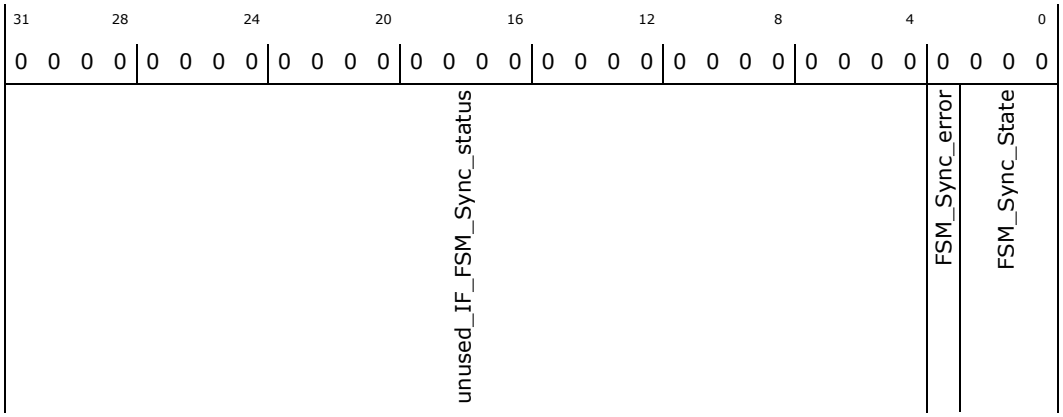
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30500h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_IF_FSM_Sync_status):** Unused
3	0x0 RO	**FSM_Sync_error:** Error flag: when set in combination with: Idle state an unknown command has been received; Req. Lines state an unexpected vsynch or eof has been received; Req. Vectors state an unexpected vsynch or eof has been received; another state an illegal state transition has occurred.
2:0	0x0 RO	**FSM_Sync_State:** FSM State: State: 0)Idle -- 1)Req Frame -- 2)Req. Lines -- 3)Req. Vectors -- 4)Send Acknowledge

5.2.196 FSM_Sync_counter (is_2400_ifmt_ift_sec_FSM_Sync_counter)—Offset 30504h

FSM Sync counter: counts the processed items. For Request Frame counts the number of frames processed. For Request lines command counts the number of lines processed. For Request vectors command counts the number of vectors processed. The counter begins at value 1.

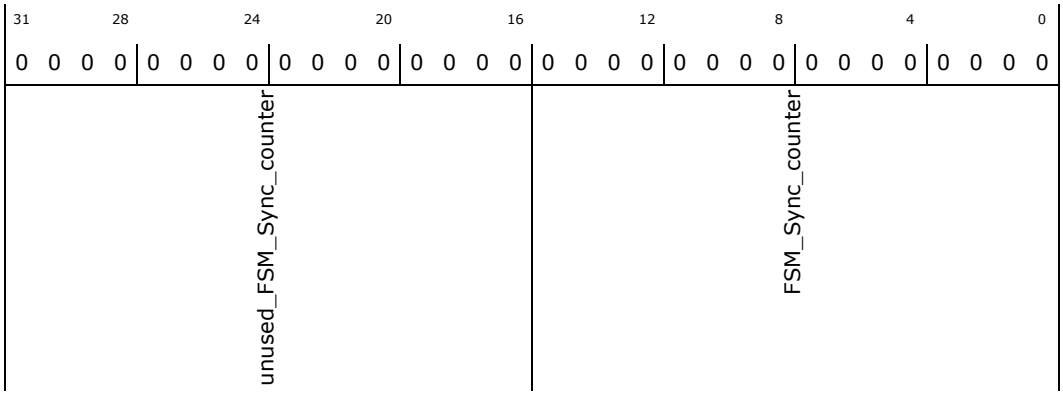
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30504h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_FSM_Sync_counter):** Unused
15:0	0x0 RO	**FSM_Sync_counter:** FSM Sync counter: counts the processed items. For Request Frame counts the number of frames processed. For Request lines command counts the number of lines processed. For Request vectors command counts the number of vectors processed. The counter begins at value 1.

5.2.197 FSM_Crop_status (is_2400_ifmt_ift_sec_FSM_Crop_status)—Offset 30508h

FSM Crop status

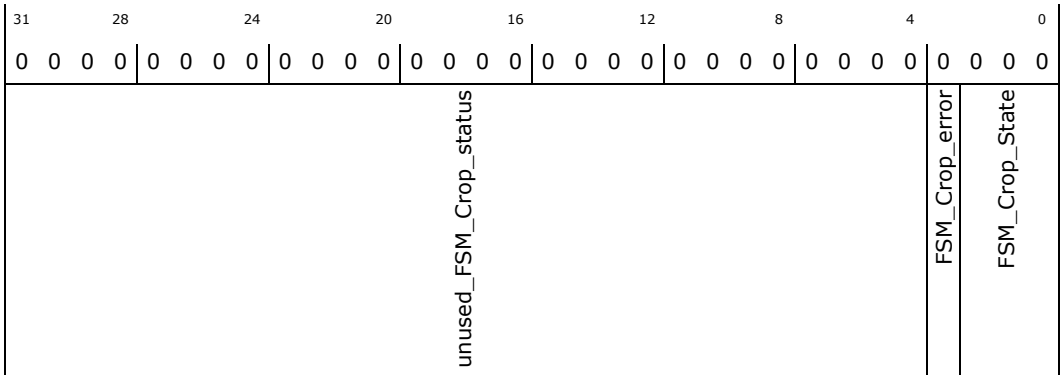
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30508h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_FSM_Crop_status):** Unused
3	0x0 RO	**FSM_Crop_error:** Error flag: when set in combination with: Crop Line state unexpected vsynch or eof has been received; Req. Lines state unexpected vsynch or eof has been received; Req. Vectors state unexpected vsynch or eof has been received; another state an illegal state transition has occurred.
2:0	0x0 RO	**FSM_Crop_State:** FSM State: State: 0)Idle -- 1)Wait Line -- 2)Crop Line -- 3)Crop Pixel -- 4)Pass pixel -- 5) Pass Line

5.2.198 FSM_Crop_line_counter (is_2400_ifmt_ift_sec_FSM_Crop_line_counter)—Offset 3050Ch

FSM Crop line counter

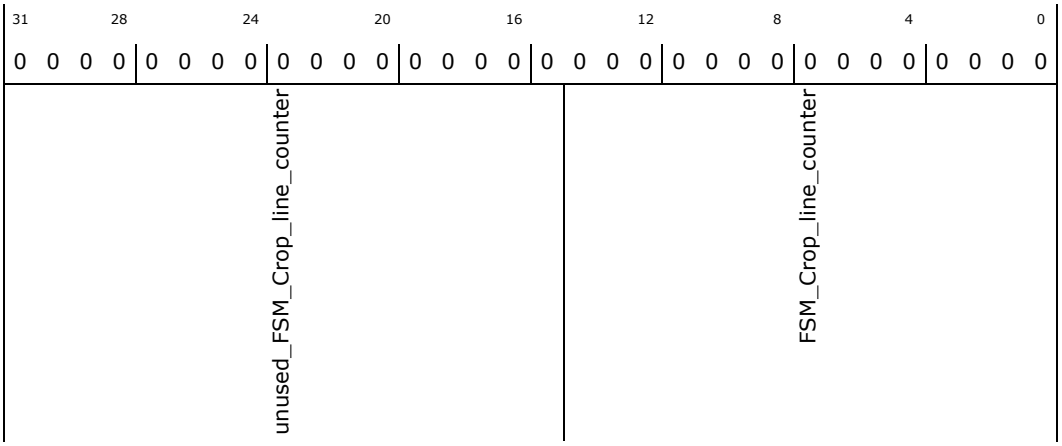
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3050Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:15	0x0 RW	**Reserved (unused_FSM_Crop_line_counter):** Unused
14:0	0x0 RO	**FSM_Crop_line_counter:** FSM Crop line counter

5.2.199 FSM_Crop_pixel_counter (is_2400_ifmt_ift_sec_FSM_Crop_pixel_counter)—Offset 30510h

FSM Crop pixel component counter

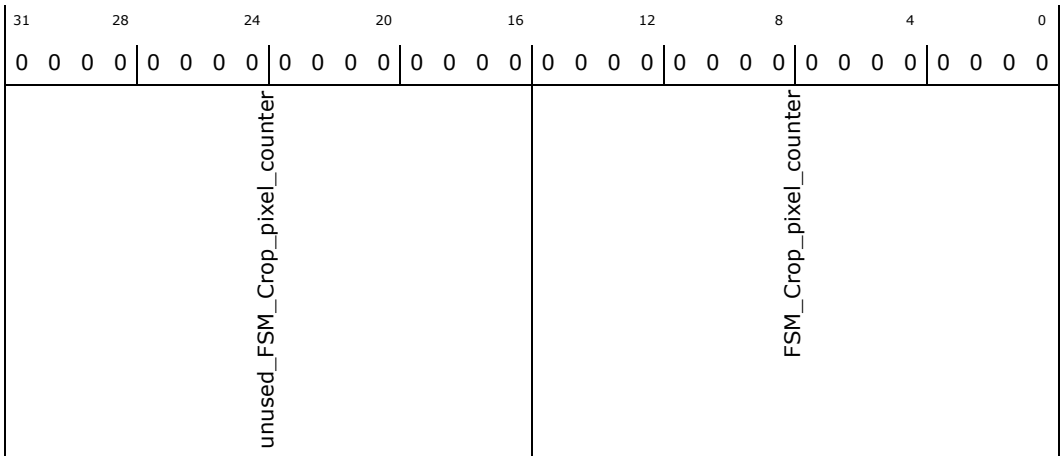
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30510h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_FSM_Crop_pixel_counter):** Unused
15:0	0x0 RO	**FSM_Crop_pixel_counter:** FSM Crop pixel component counter

5.2.200 FSM_Deinterl_idx_buffer (is_2400_ifmt_ift_sec_FSM_Deinterl_idx_buffer)—Offset 30514h

FSM de-interleaving idx buffer

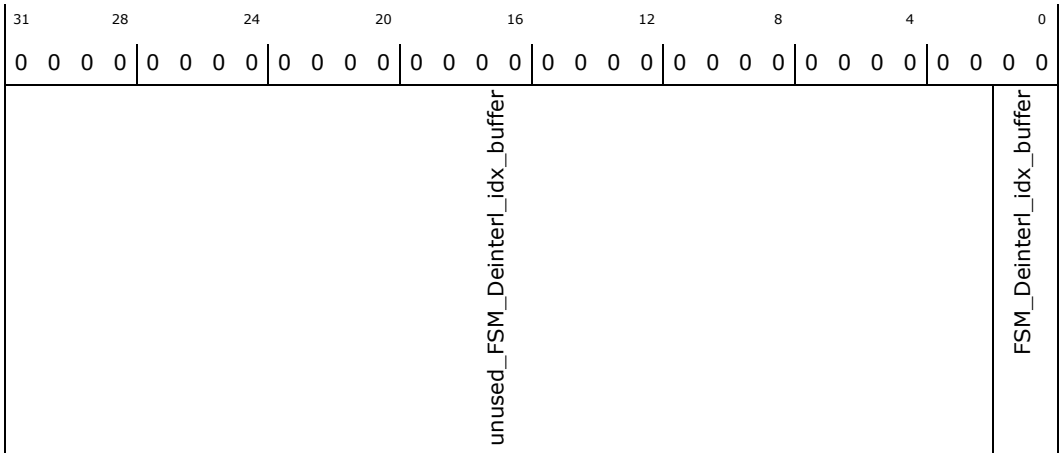
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30514h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_FSM_Deinterl_idx_buffer):** Unused
1:0	0x0 RO	**FSM_Deinterl_idx_buffer:** FSM de-interleaving idx buffer

5.2.201 FSM_Horiz_Decim_cnt (is_2400_ifmt_ift_sec_FSM_Horiz_Decim_cnt)—Offset 30518h

FSM Horizontal Decimation counter

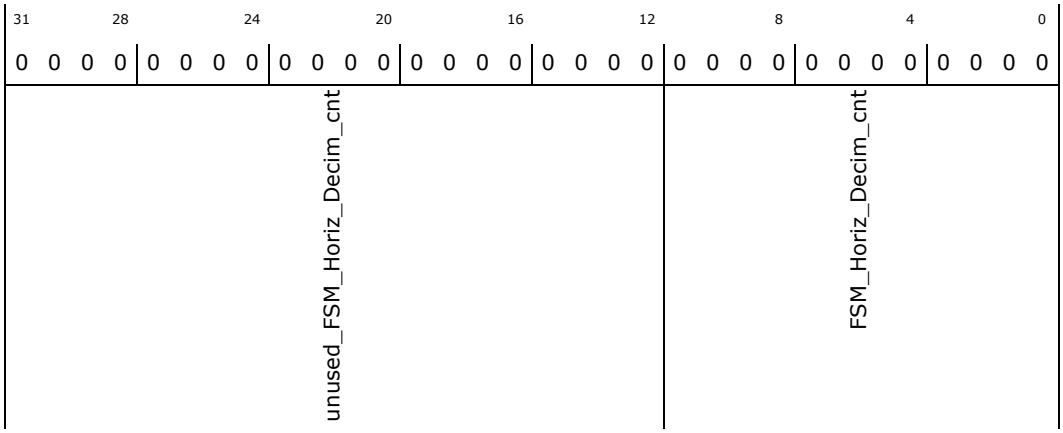
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30518h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_FSM_Horiz_Decim_cnt):** Unused
11:0	0x0 RO	**FSM_Horiz_Decim_cnt:** FSM Horizontal Decimation counter

5.2.202 FSM_Vertic_Decim_cnt (is_2400_ifmt_ift_sec_FSM_Vertic_Decim_cnt)—Offset 3051Ch

FSM Vertical decimation counter

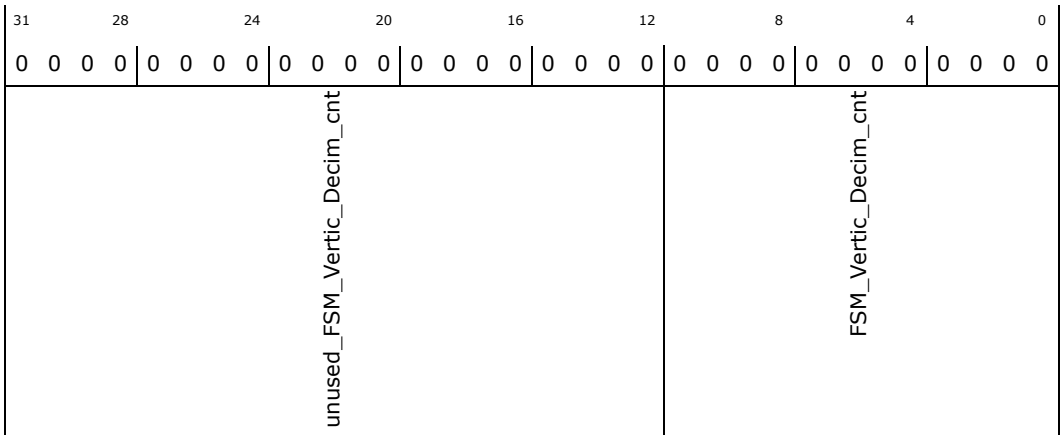
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3051Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_FSM_Vertic_Decim_cnt):** Unused
11:0	0x0 RO	**FSM_Vertic_Decim_cnt:** FSM Vertical decimation counter

5.2.203 FSM_Vertic_Block_Decim_cnt (is_2400_ifmt_ift_sec_FSM_Vertic_Block_Decim_cnt)—Offset 30520h

FSM Vertical block decimation counter

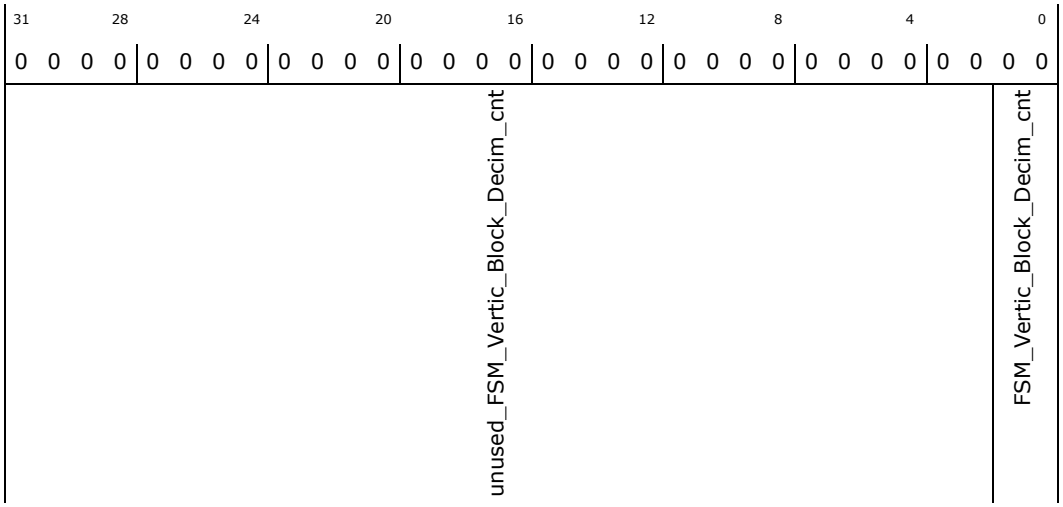
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30520h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_FSM_Vertic_Block_Decim_cnt):** Unused
1:0	0x0 RO	**FSM_Vertic_Block_Decim_cnt:** FSM Vertical block decimation counter

5.2.204 IF_FSM_Padding_status (is_2400_ifmt_ift_sec_IF_FSM_Padding_status)—Offset 30524h

FSM Padding status

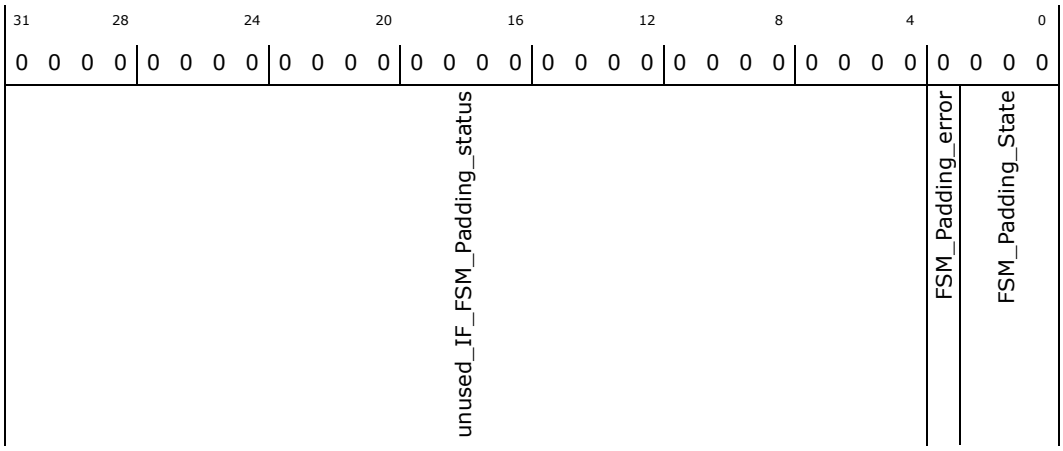
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30524h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_IF_FSM_Padding_status):** Unused
3	0x0 RO	**FSM_Padding_error:** Error flag: when set in combination with: Left Padding state an unexpected vsynch or hsync has been received; Write state an unexpected vsynch or hsync has been received; Right padding state unexpected vsynch has been received; Send EOL state an unexpected vsynch has been received; another state an illegal state transition has occurred.
2:0	0x0 RO	**FSM_Padding_State:** FSM State: State: 0)Idle -- 1)Left Padding -- 2)Write -- 3)Right padding -- 4)Sending EOL

5.2.205 IF_FSM_Padding_elem_idx (is_2400_ifmt_ift_sec_IF_FSM_Padding_elem_idx)—Offset 30528h

FSM Padding element index counter

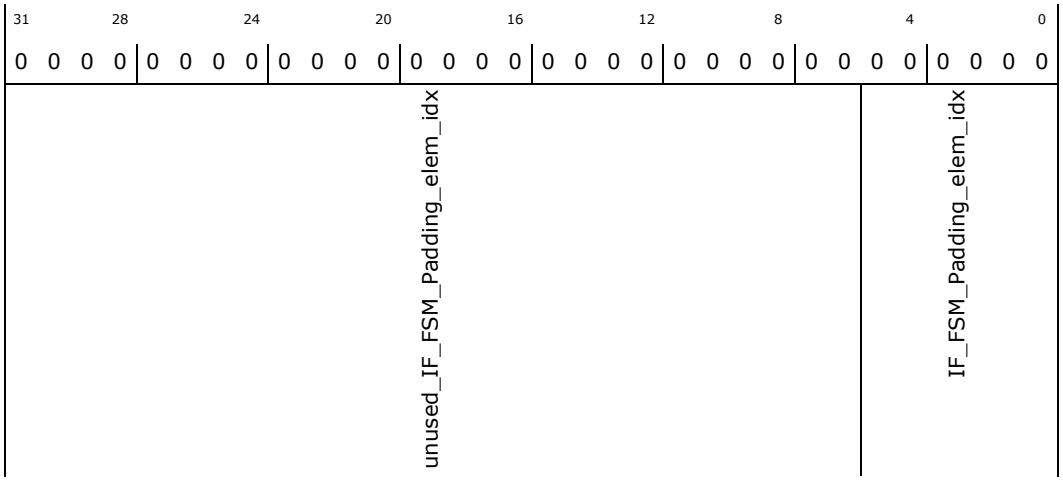
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30528h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_IF_FSM_Padding_elem_idx):** Unused
5:0	0x0 RO	**IF_FSM_Padding_elem_idx:** FSM Padding element index counter

5.2.206 IF_FSM_Vec_Sup (is_2400_ifmt_ift_sec_IF_FSM_Vec_Sup)—Offset 3052Ch

FSM Vector support error state: if set the FSM Vector support is in error state

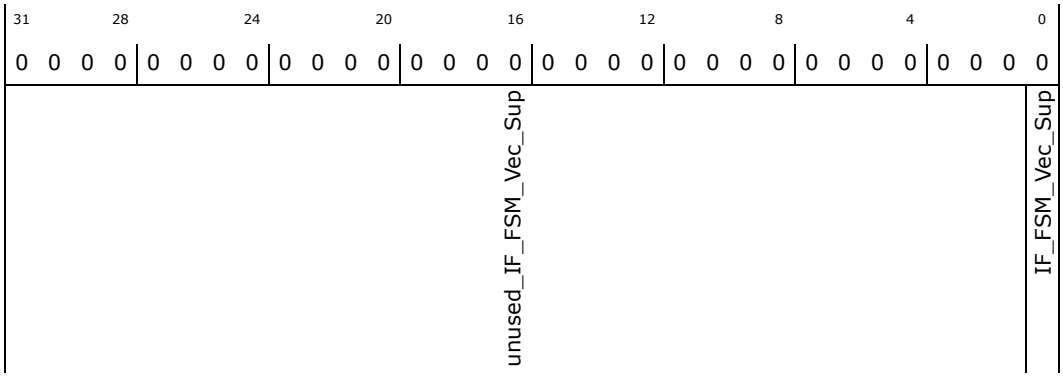
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3052Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_FSM_Vec_Sup):** Unused
0	0x0 RO	**IF_FSM_Vec_Sup:** FSM Vector support error state: if set the FSM Vector support is in error state

5.2.207 IF_FSM_Vec_Sup_Buf_full (is_2400_ifmt_ift_sec_IF_FSM_Vec_Sup_Buf_full)—Offset 30530h

FSM Vector support buf full: one-hot encoding flag signaling that the correspondent buffer is full

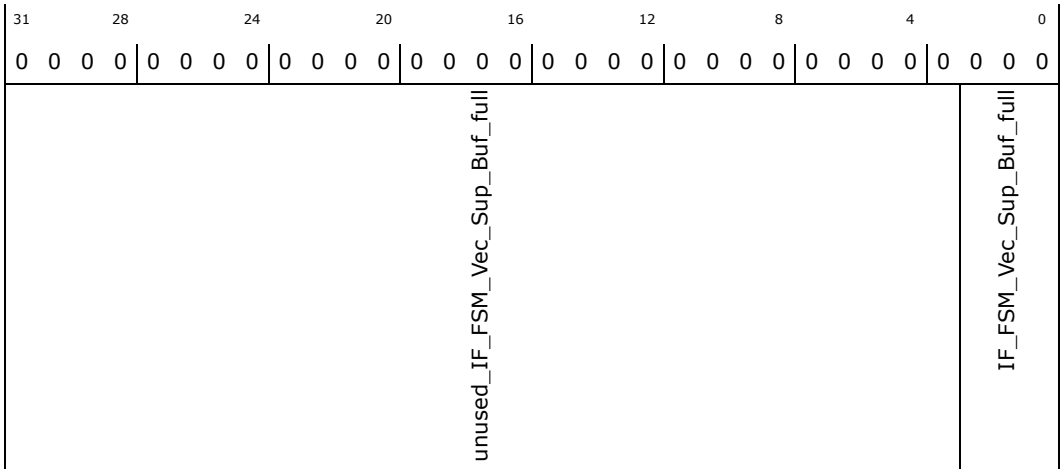
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30530h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved (unused_IF_FSM_Vec_Sup_Buf_full):** Unused
2:0	0x0 RO	**IF_FSM_Vec_Sup_Buf_full:** FSM Vector support buf full: one-hot encoding flag signaling that the correspondent buffer is full

5.2.208 IF_FSM_Vec_Sup_rd_accept (is_2400_ifmt_ift_sec_IF_FSM_Vec_Sup_rd_accept)—Offset 30534h

FSM Vector Support FIFO rd accept flag

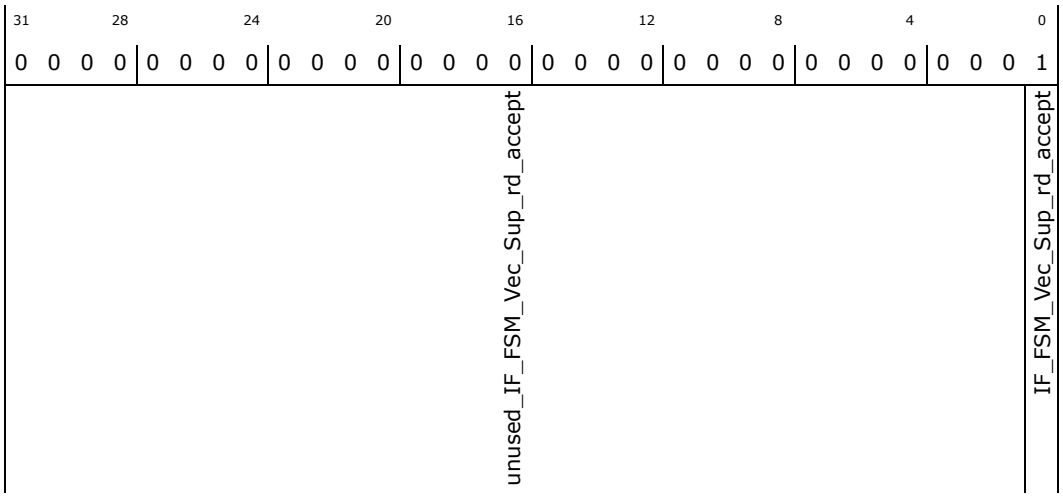
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30534h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_IF_FSM_Vec_Sup_rd_accept):** Unused
0	0x1 RO	**IF_FSM_Vec_Sup_rd_accept:** FSM Vector Support FIFO rd accept flag

5.2.209 IF_Pixel_Fifo_status (is_2400_ifmt_ift_sec_IF_Pixel_Fifo_status)—Offset 30538h

Pixel FIFO status

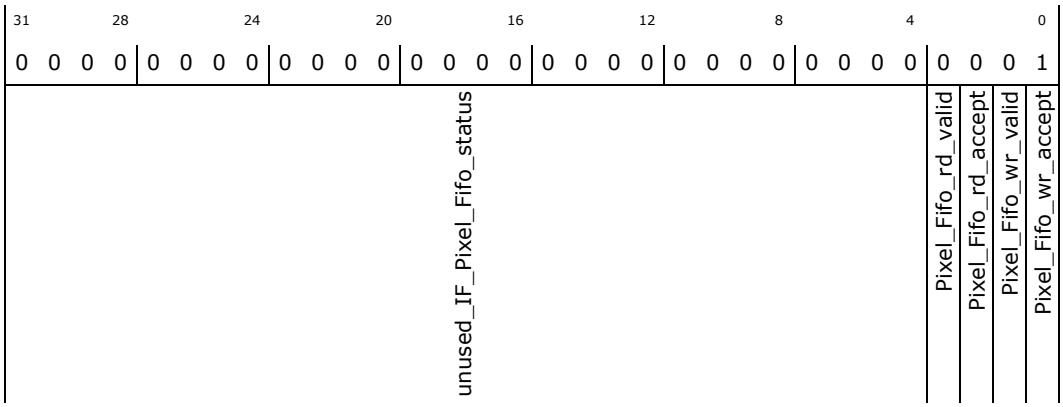
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30538h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_IF_Pixel_Fifo_status):** Unused
3	0x0 RO	**Pixel_Fifo_rd_valid:** FIFO has an element to be read
2	0x0 RO	**Pixel_Fifo_rd_accept:** IF accepts Pixel(s)
1	0x0 RO	**Pixel_Fifo_wr_valid:** There is an element to write into the FIFO
0	0x1 RO	**Pixel_Fifo_wr_accept:** FIFO is not full(1), FIFO is Full(0)

5.2.210 MemCopy_sw_rst (is_2400_ifmt_mem_cpy_MemCopy_sw_rst)—Offset 30600h

Software Reset

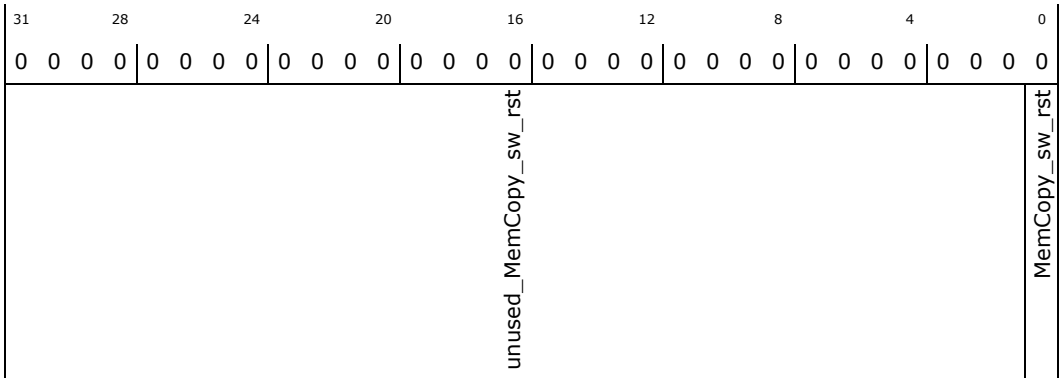
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30600h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_MemCopy_sw_rst):** Unused
0	0x0 RW	**MemCopy_sw_rst:** Software Reset

5.2.211 MemCopy_in_endian (is_2400_ifmt_mem_cpy_MemCopy_in_endian)—Offset 30604h

Input endian set to 1 if input is big endian

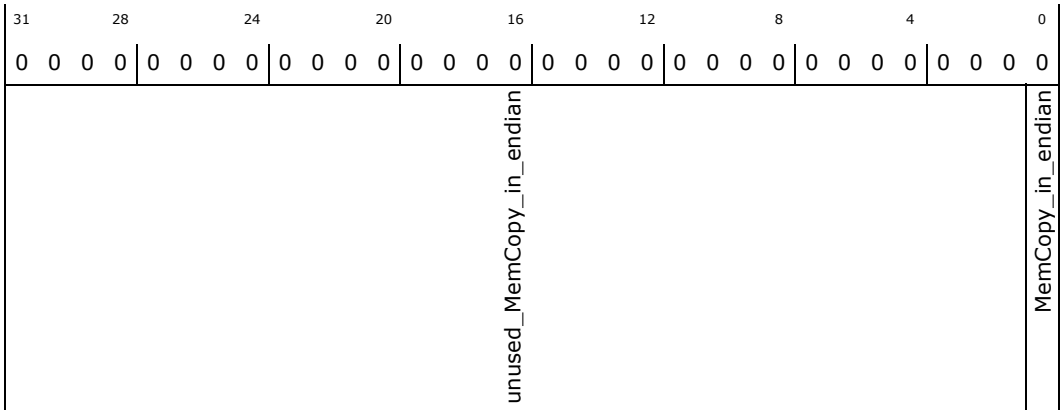
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30604h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_MemCopy_in_endian):** Unused
0	0x0 RW	**MemCopy_in_endian:** Input endian: set to 1 if input is big endian

5.2.212 MemCopy_out_endian (is_2400_ifmt_mem_cpy_MemCopy_out_endian)—Offset 30608h

Output endian: set to 1 to deliver output input in big endian

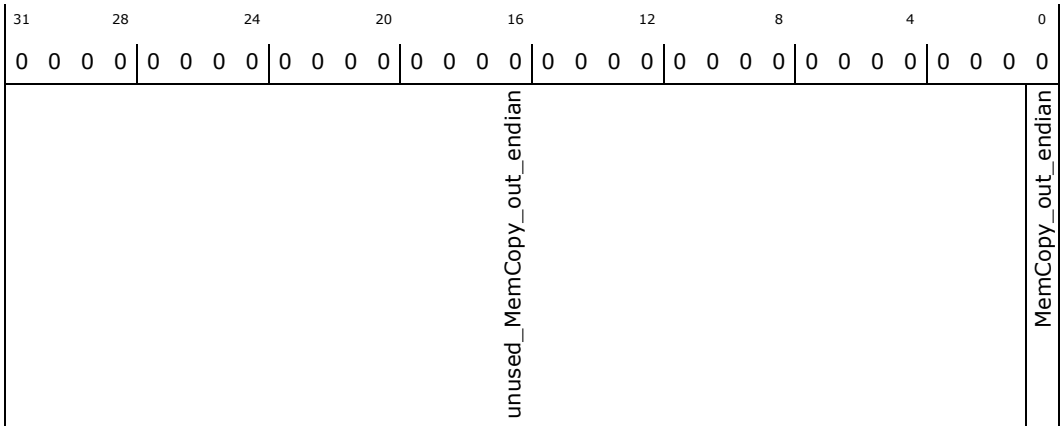
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30608h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_MemCopy_out_endian):** Unused
0	0x0 RW	**MemCopy_out_endian:** Output endian: set to 1 to deliver output input in big endian

5.2.213 MemCopy_bit_swap (is_2400_ifmt_mem_cpy_MemCopy_bit_swap)—Offset 3060Ch

Bit swapping: set to 1 to swap the bit of the incoming byte

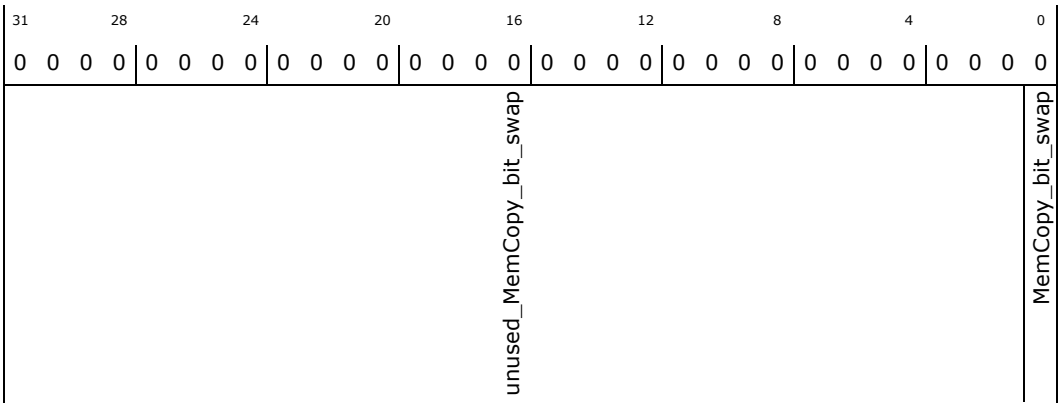
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3060Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_MemCopy_bit_swap):** Unused
0	0x0 RW	**MemCopy_bit_swap:** Bit swapping: set to 1 to swap the bit of the incoming byte

5.2.214 MemCopy_block_synch (is_2400_ifmt_mem_cpy_MemCopy_block_synch)—Offset 30610h

Block synchronization pulse active low: set to 1 if start of block and end of block are active low

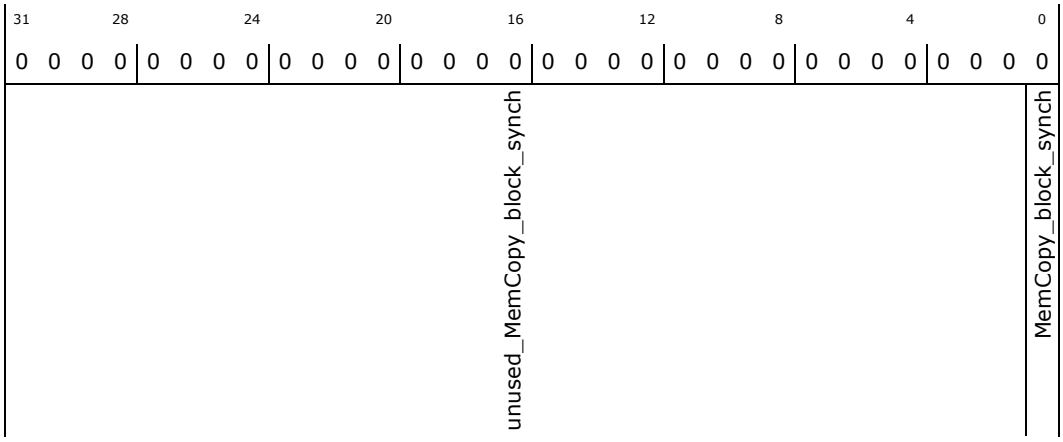
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30610h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_MemCopy_block_synch):** Unused
0	0x0 RW	**MemCopy_block_synch:** Block synchronization pulse active low: set to 1 if start of block and end of block are active low

5.2.215 MemCopy_packet_synch (is_2400_ifmt_mem_cpy_MemCopy_packet_synch)—Offset 30614h

Packet synchronization pulse active low: set to 1 if start of packet and end of packet are active low

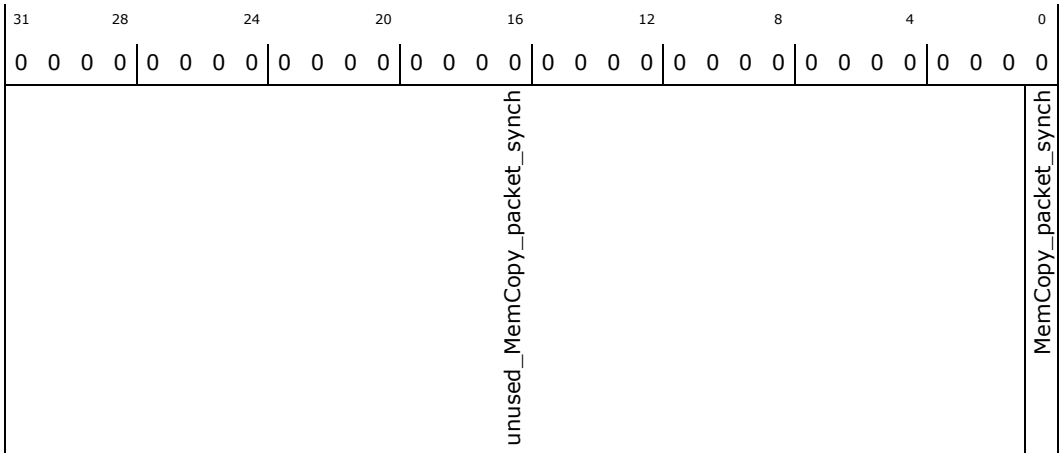
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30614h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_MemCopy_packet_synch):** Unused
0	0x0 RW	**MemCopy_packet_synch:** Packet synchronization pulse active low: set to 1 if start of packet and end of packet are active low

5.2.216 MemCopy_rd_post_wr_sync (is_2400_ifmt_mem_cpy_MemCopy_rd_post_wr_sync)—Offset 30618h

Enable read post write synchronization: set to 1 to enable read post write check before sending acknowledge

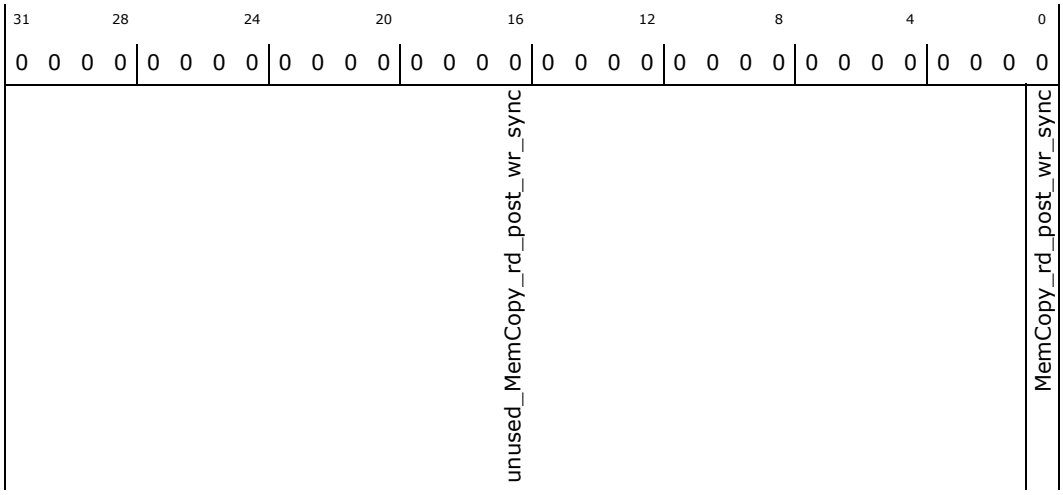
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30618h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_MemCopy_rd_post_wr_sync):** Unused
0	0x0 RW	**MemCopy_rd_post_wr_sync:** Enable read post write synchronization: set to 1 to enable read post write check before sending acknowledge

5.2.217 MemCopy_dual_input (is_2400_ifmt_mem_cpy_MemCopy_dual_input)—Offset 3061Ch

Enable dual byte inputs: set to 1 to enable dual byte input

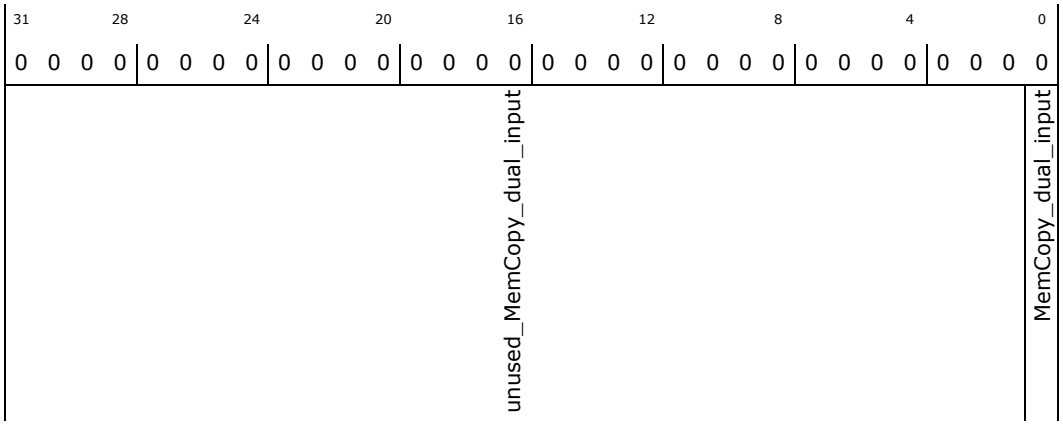
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3061Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_MemCopy_dual_input):** Unused
0	0x0 RW	**MemCopy_dual_input:** Enable dual byte inputs: set to 1 to enable dual byte input

5.2.218 MemCopy_ReEnable (is_2400_ifmt_mem_cpy_MemCopy_ReEnable)—Offset 30620h

Re-enable status update: set to 1 to re-enable status update after an error situation

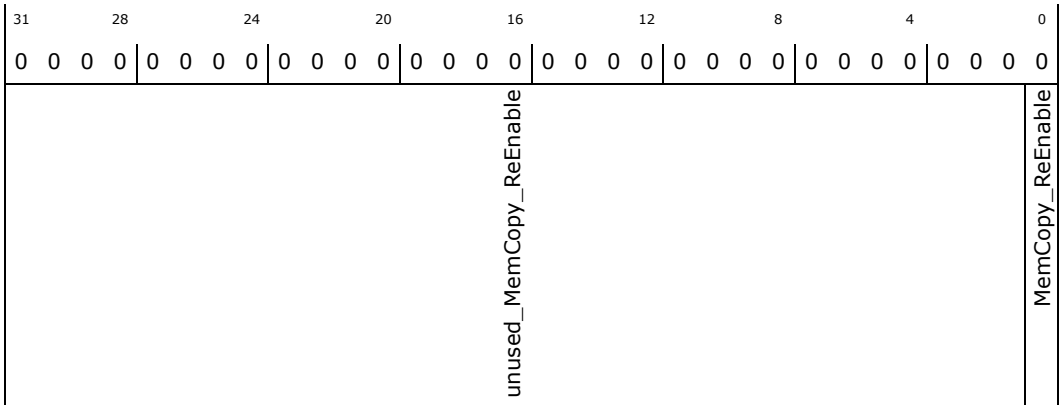
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30620h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_MemCopy_ReEnable):** Unused
0	0x0 RW	**MemCopy_ReEnable:** Re-enable status update: set to 1 to re-enable status update after an error situation

5.2.219 MemCopy_token_data (is_2400_ifmt_mem_cpy_MemCopy_token_data)—Offset 30700h

Token data on command port

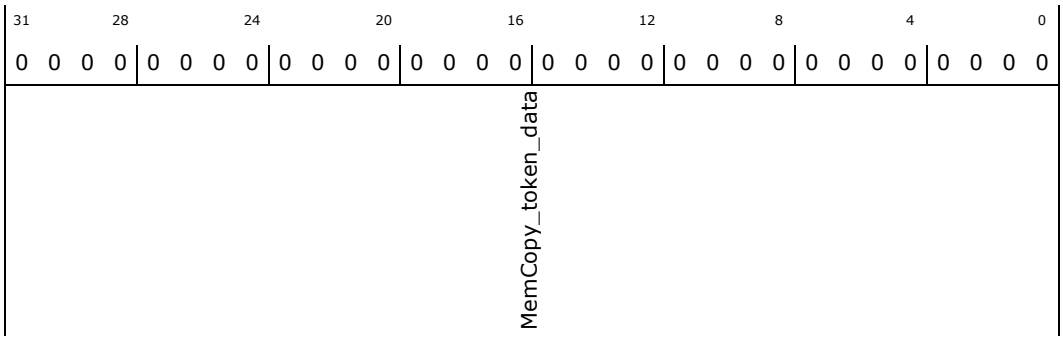
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30700h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**MemCopy_token_data:** Token data on command port

5.2.220 MemCopy_FSM_Sync_status (is_2400_ifmt_mem_cpy_MemCopy_FSM_Sync_status)—Offset 30704h

FSM Synchronization Status: 0)Idle -- 1)Request Blocks -- 2)Request Packets -- 3)Request Bytes -- 4)Send Acknowledge

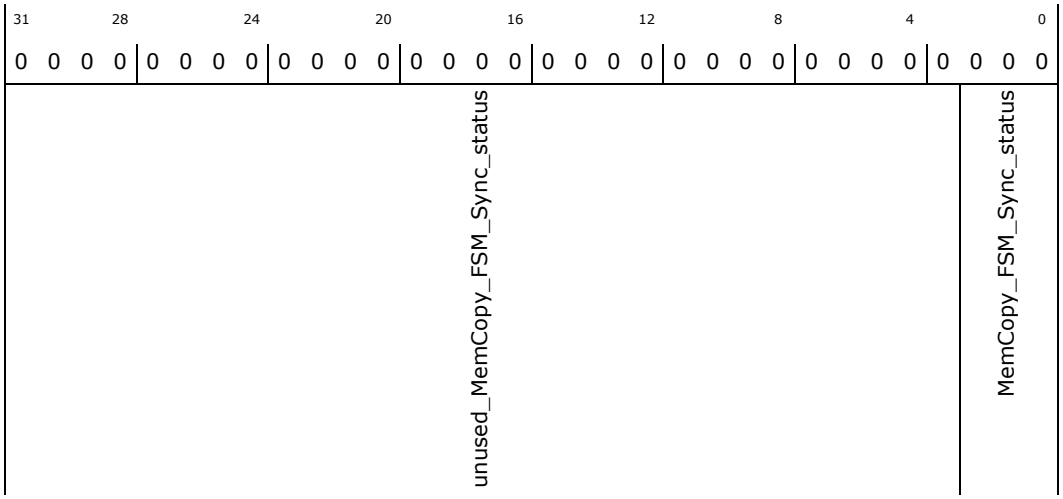
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30704h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved (unused_MemCopy_FSM_Sync_status):** Unused
2:0	0x0 RO	**MemCopy_FSM_Sync_status:** FSM Synchronization Status: 0)Idle -- 1)Request Blocks -- 2)Request Packets -- 3)Request Bytes -- 4)Send Acknowledge

5.2.221 MemCopy_FSM_Sync_bytes_cnt (is_2400_ifmt_mem_cpy_MemCopy_FSM_Sync_bytes_cnt)—Offset 30708h

FSM Synchronization bytes counter: counts the number of bytes received and packed

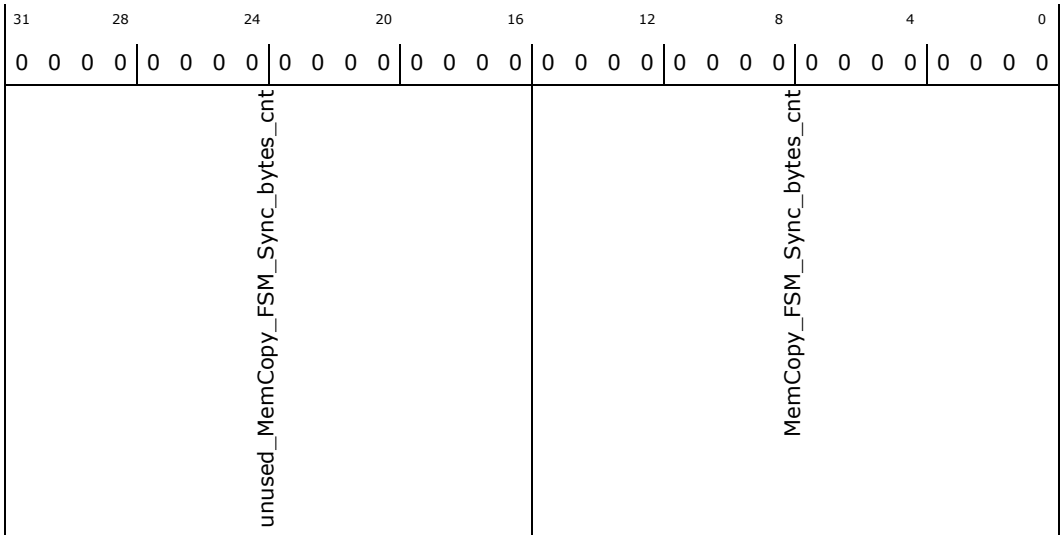
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30708h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_MemCopy_FSM_Sync_bytes_cnt):** Unused
15:0	0x0 RO	**MemCopy_FSM_Sync_bytes_cnt:** FSM Synchronization bytes counter: counts the number of bytes received and packed

5.2.222 MemCopy_FSM_Sync_token_cnt (is_2400_ifmt_mem_cpy_MemCopy_FSM_Sync_token_cnt)—Offset 3070Ch

FSM Synchronization token amount: counts the number of token processed

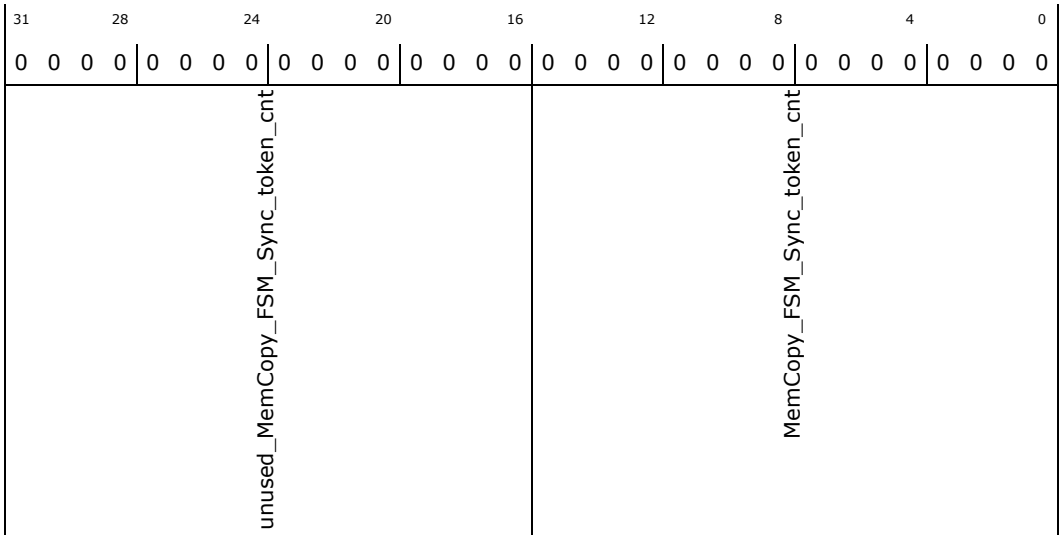
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3070Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_MemCopy_FSM_Sync_token_cnt):** Unused
15:0	0x0 RO	**MemCopy_FSM_Sync_token_cnt:** FSM Synchronization token amount: counts the number of token processed

5.2.223 MemCopy_FSM_Pack_idx_cnt (is_2400_ifmt_mem_cpy_MemCopy_FSM_Pack_idx_cnt) —Offset 30710h

FSM Pack idx counter: element index

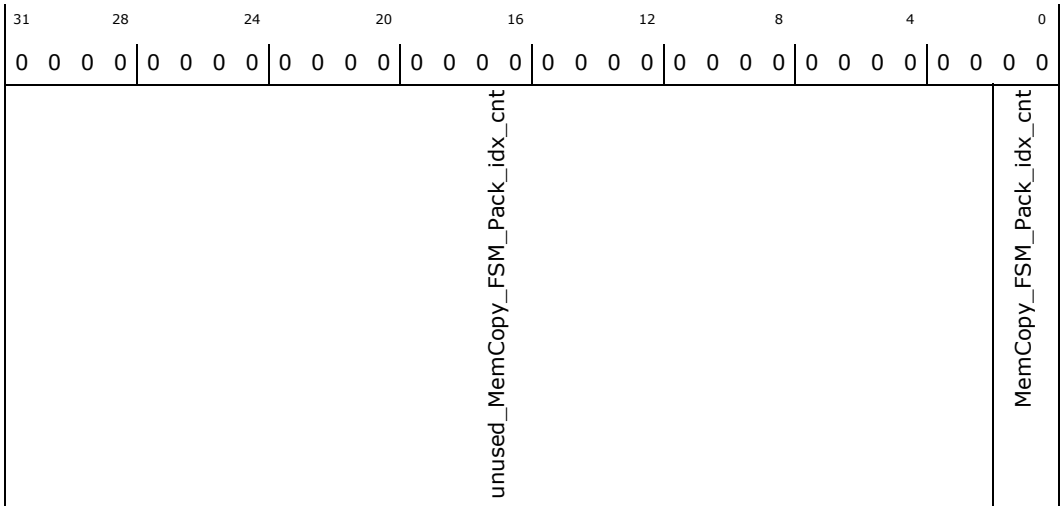
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30710h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_MemCopy_FSM_Pack_idx_cnt):** Unused
1:0	0x0 RO	**MemCopy_FSM_Pack_idx_cnt:** FSM Pack idx counter: element index

5.2.224 MemCopy_FSM_Buf_Sup_status (is_2400_ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_status)—Offset 30714h

Buffer Full and mask

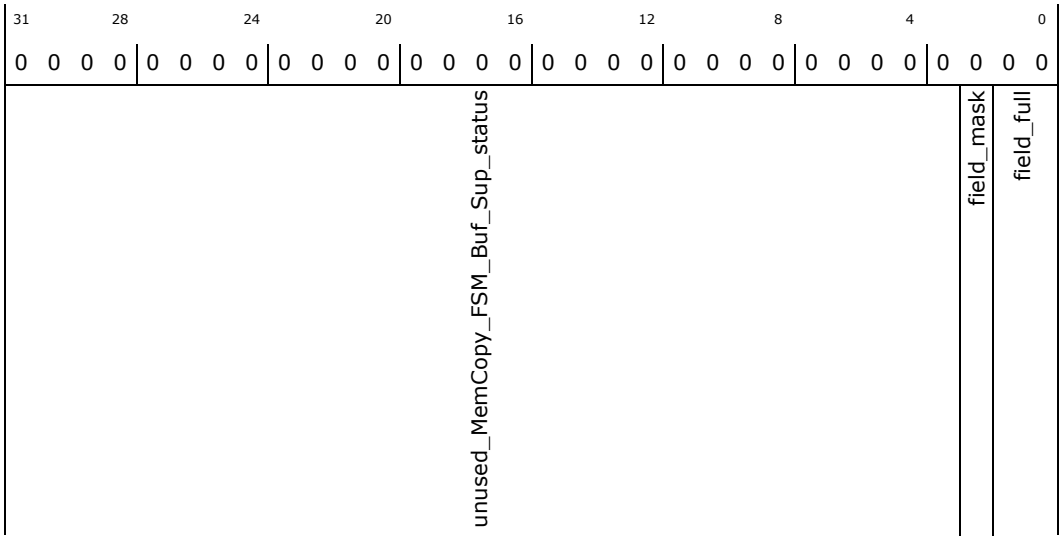
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30714h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:3	0x0 RO	**Reserved (unused_MemCopy_FSM_Buf_Sup_status):** Unused
2	0x0 RO	**field_mask:** FSM Buffer support mask buffers full to the FSM CioWr
1:0	0x0 RO	**field_full:** FSM Buffer support one-hot encoding flagging when the buffer are full

5.2.225 MemCopy_FSM_Buf_Sup_cnt (is_2400_ifmt_mem_cpy_MemCopy_FSM_Buf_Sup_cnt)—Offset 30718h

FSM Buffer support: counter for buffer index

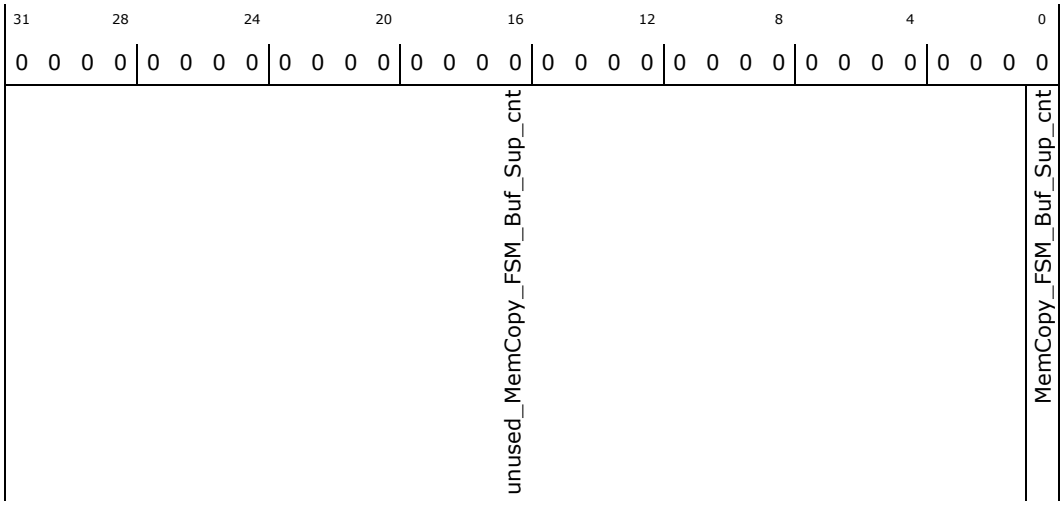
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30718h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_MemCopy_FSM_Buf_Sup_cnt):** Unused
0	0x0 RO	**MemCopy_FSM_Buf_Sup_cnt:** FSM Buffer support: counter for buffer index

5.2.226 MemCopy_FSM_CioWr_status (is_2400_ifmt_mem_cpy_MemCopy_FSM_CioWr_status) —Offset 3071Ch

FSM CioWr Status

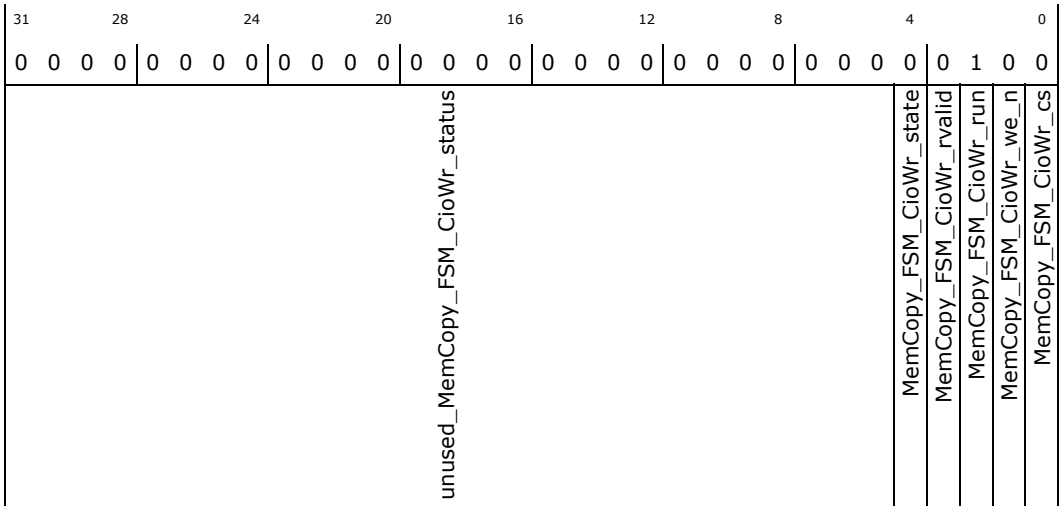
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3071Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_MemCopy_FSM_CioWr_status):** Unused
4	0x0 RO	**MemCopy_FSM_CioWr_state:** 0)Idle - 1)Writing
3	0x0 RO	**MemCopy_FSM_CioWr_rvalid:** Read valid flag
2	0x1 RO	**MemCopy_FSM_CioWr_run:** Run flag
1	0x0 RO	**MemCopy_FSM_CioWr_we_n:** Write enable flag, active low
0	0x0 RO	**MemCopy_FSM_CioWr_cs:** CS flag

5.2.227 MemCopy_FSM_CioWr_addr (is_2400_ifmt_mem_cpy_MemCopy_FSM_CioWr_addr)—Offset 30720h

FSM CioWr: write address in byte

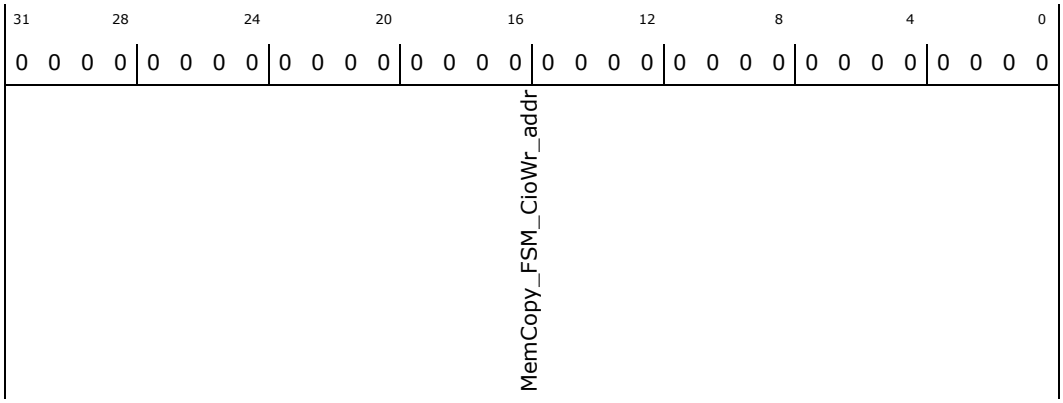
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30720h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**MemCopy_FSM_CioWr_addr:** FSM CioWr: write address in byte

5.2.228 IFMT_input_switch__reg0 (is_2400_ifmt_gp_reg_IFMT_input_switch__reg0)—Offset 30800h

GP reg input switch data and hsync look-up table Register 0

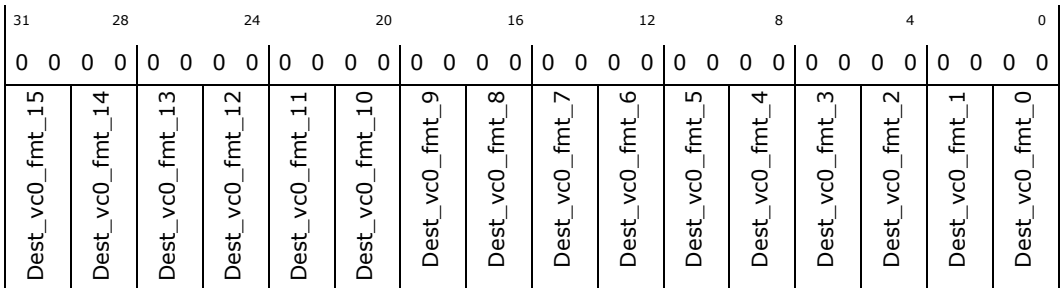
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30800h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**Dest_vc0_fmt_15:** Selects destination of data and hsync for vc=0 fmt=15. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.

Bit Range	Default and Access	Field Name (ID): Description
29:28	0x0 RW	**Dest_vc0_fmt_14:** Selects destination of data and hsync for vc=0 fmt=14. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
27:26	0x0 RW	**Dest_vc0_fmt_13:** Selects destination of data and hsync for vc=0 fmt=13. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
25:24	0x0 RW	**Dest_vc0_fmt_12:** Selects destination of data and hsync for vc=0 fmt=12. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
23:22	0x0 RW	**Dest_vc0_fmt_11:** Selects destination of data and hsync for vc=0 fmt=11. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
21:20	0x0 RW	**Dest_vc0_fmt_10:** Selects destination of data and hsync for vc=0 fmt=10. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
19:18	0x0 RW	**Dest_vc0_fmt_9:** Selects destination of data and hsync for vc=0 fmt=9. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
17:16	0x0 RW	**Dest_vc0_fmt_8:** Selects destination of data and hsync for vc=0 fmt=8. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
15:14	0x0 RW	**Dest_vc0_fmt_7:** Selects destination of data and hsync for vc=0 fmt=7. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
13:12	0x0 RW	**Dest_vc0_fmt_6:** Selects destination of data and hsync for vc=0 fmt=6. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
11:10	0x0 RW	**Dest_vc0_fmt_5:** Selects destination of data and hsync for vc=0 fmt=5. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
9:8	0x0 RW	**Dest_vc0_fmt_4:** Selects destination of data and hsync for vc=0 fmt=4. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
7:6	0x0 RW	**Dest_vc0_fmt_3:** Selects destination of data and hsync for vc=0 fmt=3. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
5:4	0x0 RW	**Dest_vc0_fmt_2:** Selects destination of data and hsync for vc=0 fmt=2. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
3:2	0x0 RW	**Dest_vc0_fmt_1:** Selects destination of data and hsync for vc=0 fmt=1. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
1:0	0x0 RW	**Dest_vc0_fmt_0:** Selects destination of data and hsync for vc=0 fmt=0. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.

5.2.229 IFMT_input_switch__reg1 (is_2400_ifmt_gp_reg_IFMT_input_switch__reg1)— Offset 30804h

GP reg input switch data and hsync look-up table Register 1

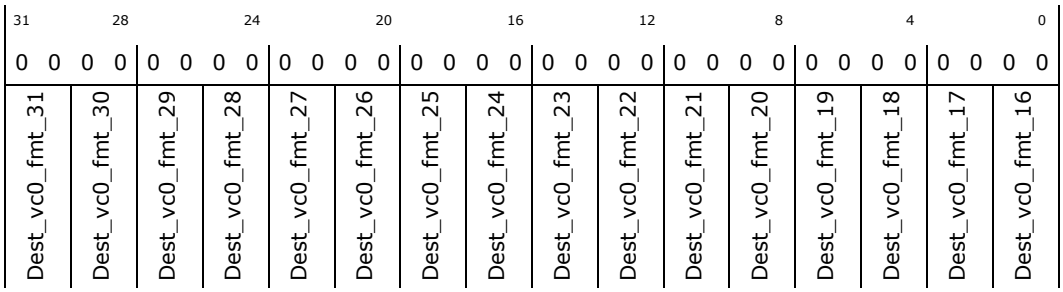
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30804h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**Dest_vc0_fmt_31:** Selects destination of data and hsync for vc=0 fmt=31. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
29:28	0x0 RW	**Dest_vc0_fmt_30:** Selects destination of data and hsync for vc=0 fmt=30. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
27:26	0x0 RW	**Dest_vc0_fmt_29:** Selects destination of data and hsync for vc=0 fmt=29. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
25:24	0x0 RW	**Dest_vc0_fmt_28:** Selects destination of data and hsync for vc=0 fmt=28. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
23:22	0x0 RW	**Dest_vc0_fmt_27:** Selects destination of data and hsync for vc=0 fmt=27. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
21:20	0x0 RW	**Dest_vc0_fmt_26:** Selects destination of data and hsync for vc=0 fmt=26. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
19:18	0x0 RW	**Dest_vc0_fmt_25:** Selects destination of data and hsync for vc=0 fmt=25. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
17:16	0x0 RW	**Dest_vc0_fmt_24:** Selects destination of data and hsync for vc=0 fmt=24. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.

Bit Range	Default and Access	Field Name (ID): Description
15:14	0x0 RW	**Dest_vc0_fmt_23:** Selects destination of data and hsync for vc=0 fmt=23. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
13:12	0x0 RW	**Dest_vc0_fmt_22:** Selects destination of data and hsync for vc=0 fmt=22. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
11:10	0x0 RW	**Dest_vc0_fmt_21:** Selects destination of data and hsync for vc=0 fmt=21. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
9:8	0x0 RW	**Dest_vc0_fmt_20:** Selects destination of data and hsync for vc=0 fmt=20. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
7:6	0x0 RW	**Dest_vc0_fmt_19:** Selects destination of data and hsync for vc=0 fmt=19. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
5:4	0x0 RW	**Dest_vc0_fmt_18:** Selects destination of data and hsync for vc=0 fmt=18. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
3:2	0x0 RW	**Dest_vc0_fmt_17:** Selects destination of data and hsync for vc=0 fmt=17. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
1:0	0x0 RW	**Dest_vc0_fmt_16:** Selects destination of data and hsync for vc=0 fmt=16. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.

5.2.230 IFMT_input_switch__reg2 (is_2400_ifmt_gp_reg_IFMT_input_switch__reg2)—Offset 30808h

GP reg input switch data and hsync look-up table Register 2

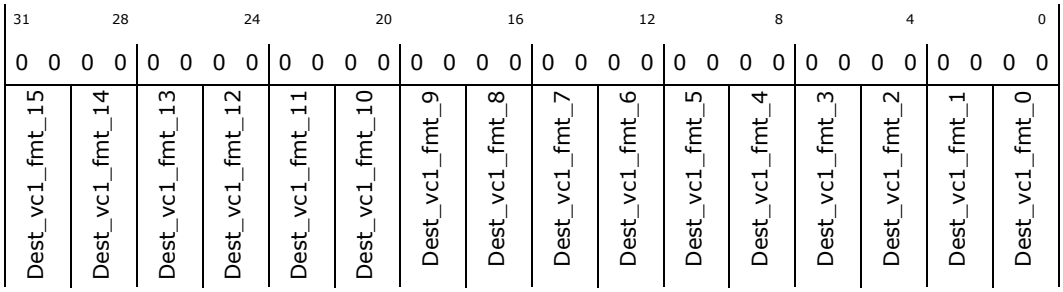
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30808h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**Dest_vc1_fmt_15:** Selects destination of data and hsync for vc=1 fmt=15. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
29:28	0x0 RW	**Dest_vc1_fmt_14:** Selects destination of data and hsync for vc=1 fmt=14. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
27:26	0x0 RW	**Dest_vc1_fmt_13:** Selects destination of data and hsync for vc=1 fmt=13. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
25:24	0x0 RW	**Dest_vc1_fmt_12:** Selects destination of data and hsync for vc=1 fmt=12. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
23:22	0x0 RW	**Dest_vc1_fmt_11:** Selects destination of data and hsync for vc=1 fmt=11. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
21:20	0x0 RW	**Dest_vc1_fmt_10:** Selects destination of data and hsync for vc=1 fmt=10. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
19:18	0x0 RW	**Dest_vc1_fmt_9:** Selects destination of data and hsync for vc=1 fmt=9. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
17:16	0x0 RW	**Dest_vc1_fmt_8:** Selects destination of data and hsync for vc=1 fmt=8. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
15:14	0x0 RW	**Dest_vc1_fmt_7:** Selects destination of data and hsync for vc=1 fmt=7. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
13:12	0x0 RW	**Dest_vc1_fmt_6:** Selects destination of data and hsync for vc=1 fmt=6. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
11:10	0x0 RW	**Dest_vc1_fmt_5:** Selects destination of data and hsync for vc=1 fmt=5. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
9:8	0x0 RW	**Dest_vc1_fmt_4:** Selects destination of data and hsync for vc=1 fmt=4. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.

Bit Range	Default and Access	Field Name (ID): Description
7:6	0x0 RW	**Dest_vc1_fmt_3:** Selects destination of data and hsync for vc=1 fmt=3. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
5:4	0x0 RW	**Dest_vc1_fmt_2:** Selects destination of data and hsync for vc=1 fmt=2. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
3:2	0x0 RW	**Dest_vc1_fmt_1:** Selects destination of data and hsync for vc=1 fmt=1. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
1:0	0x0 RW	**Dest_vc1_fmt_0:** Selects destination of data and hsync for vc=1 fmt=0. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.

5.2.231 IFMT_input_switch__reg3 (is_2400_ifmt_gp_reg_IFMT_input_switch__reg3)—Offset 3080Ch

GP reg input switch data and hsync look-up table Register 3

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

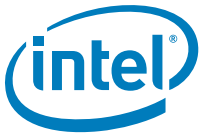
Offset: [ISPMMADR] + 3080Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Dest_vc2_fmt_31 | Dest_vc2_fmt_30	Dest_vc2_fmt_29 | Dest_vc2_fmt_28	Dest_vc2_fmt_27 | Dest_vc2_fmt_26	Dest_vc2_fmt_25 | Dest_vc2_fmt_24	Dest_vc2_fmt_23 | Dest_vc2_fmt_22	Dest_vc2_fmt_21 | Dest_vc2_fmt_20	Dest_vc2_fmt_19 | Dest_vc2_fmt_18	Dest_vc2_fmt_17 | Dest_vc2_fmt_16

Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**Dest_vc2_fmt_31:** Selects destination of data and hsync for vc=1 fmt=31. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
29:28	0x0 RW	**Dest_vc2_fmt_30:** Selects destination of data and hsync for vc=1 fmt=30. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.



Bit Range	Default and Access	Field Name (ID): Description
27:26	0x0 RW	**Dest_vc2_fmt_29:** Selects destination of data and hsync for vc=1 fmt=29. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
25:24	0x0 RW	**Dest_vc2_fmt_28:** Selects destination of data and hsync for vc=1 fmt=28. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
23:22	0x0 RW	**Dest_vc2_fmt_27:** Selects destination of data and hsync for vc=1 fmt=27. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
21:20	0x0 RW	**Dest_vc2_fmt_26:** Selects destination of data and hsync for vc=1 fmt=26. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
19:18	0x0 RW	**Dest_vc2_fmt_25:** Selects destination of data and hsync for vc=1 fmt=25. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
17:16	0x0 RW	**Dest_vc2_fmt_24:** Selects destination of data and hsync for vc=1 fmt=24. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
15:14	0x0 RW	**Dest_vc2_fmt_23:** Selects destination of data and hsync for vc=1 fmt=23. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
13:12	0x0 RW	**Dest_vc2_fmt_22:** Selects destination of data and hsync for vc=1 fmt=22. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
11:10	0x0 RW	**Dest_vc2_fmt_21:** Selects destination of data and hsync for vc=1 fmt=21. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
9:8	0x0 RW	**Dest_vc2_fmt_20:** Selects destination of data and hsync for vc=1 fmt=20. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
7:6	0x0 RW	**Dest_vc2_fmt_19:** Selects destination of data and hsync for vc=1 fmt=19. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
5:4	0x0 RW	**Dest_vc2_fmt_18:** Selects destination of data and hsync for vc=1 fmt=18. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
3:2	0x0 RW	**Dest_vc2_fmt_17:** Selects destination of data and hsync for vc=1 fmt=17. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
1:0	0x0 RW	**Dest_vc2_fmt_16:** Selects destination of data and hsync for vc=1 fmt=16. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.

5.2.232 IFMT_input_switch__reg4 (is_2400_ifmt_gp_reg_IFMT_input_switch__reg4)—Offset 30810h

GP reg input switch data and hsync look-up table Register 4

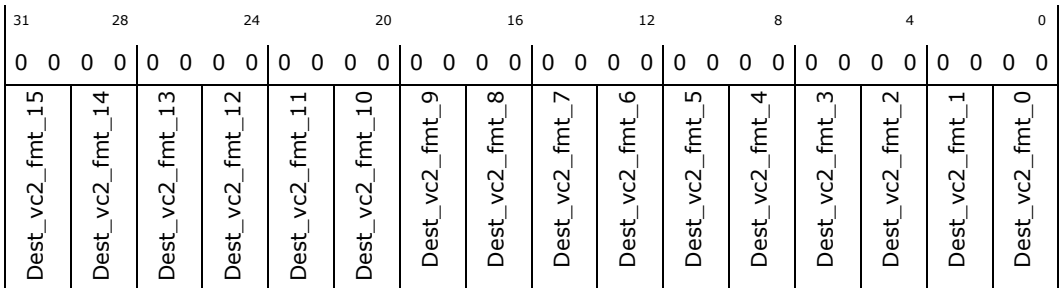
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30810h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**Dest_vc2_fmt_15:** Selects destination of data and hsync for vc=2 fmt=15. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
29:28	0x0 RW	**Dest_vc2_fmt_14:** Selects destination of data and hsync for vc=2 fmt=14. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
27:26	0x0 RW	**Dest_vc2_fmt_13:** Selects destination of data and hsync for vc=2 fmt=13. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
25:24	0x0 RW	**Dest_vc2_fmt_12:** Selects destination of data and hsync for vc=2 fmt=12. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
23:22	0x0 RW	**Dest_vc2_fmt_11:** Selects destination of data and hsync for vc=2 fmt=11. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
21:20	0x0 RW	**Dest_vc2_fmt_10:** Selects destination of data and hsync for vc=2 fmt=10. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
19:18	0x0 RW	**Dest_vc2_fmt_9:** Selects destination of data and hsync for vc=2 fmt=9. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
17:16	0x0 RW	**Dest_vc2_fmt_8:** Selects destination of data and hsync for vc=2 fmt=8. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.

Bit Range	Default and Access	Field Name (ID): Description
15:14	0x0 RW	**Dest_vc2_fmt_7:** Selects destination of data and hsync for vc=2 fmt=7. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
13:12	0x0 RW	**Dest_vc2_fmt_6:** Selects destination of data and hsync for vc=2 fmt=6. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
11:10	0x0 RW	**Dest_vc2_fmt_5:** Selects destination of data and hsync for vc=2 fmt=5. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
9:8	0x0 RW	**Dest_vc2_fmt_4:** Selects destination of data and hsync for vc=2 fmt=4. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
7:6	0x0 RW	**Dest_vc2_fmt_3:** Selects destination of data and hsync for vc=2 fmt=3. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
5:4	0x0 RW	**Dest_vc2_fmt_2:** Selects destination of data and hsync for vc=2 fmt=2. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
3:2	0x0 RW	**Dest_vc2_fmt_1:** Selects destination of data and hsync for vc=2 fmt=1. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
1:0	0x0 RW	**Dest_vc2_fmt_0:** Selects destination of data and hsync for vc=2 fmt=0. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.

5.2.233 IFMT_input_switch__reg5 (is_2400_ifmt_gp_reg_IFMT_input_switch__reg5)—Offset 30814h

GP reg input switch data and hsync look-up table Register 5

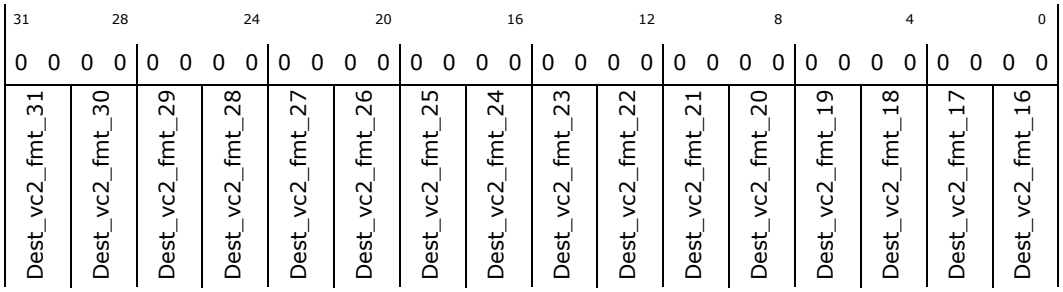
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30814h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**Dest_vc2_fmt_31:** Selects destination of data and hsync for vc=2 fmt=31. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
29:28	0x0 RW	**Dest_vc2_fmt_30:** Selects destination of data and hsync for vc=2 fmt=30. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
27:26	0x0 RW	**Dest_vc2_fmt_29:** Selects destination of data and hsync for vc=2 fmt=29. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
25:24	0x0 RW	**Dest_vc2_fmt_28:** Selects destination of data and hsync for vc=2 fmt=28. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
23:22	0x0 RW	**Dest_vc2_fmt_27:** Selects destination of data and hsync for vc=2 fmt=27. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
21:20	0x0 RW	**Dest_vc2_fmt_26:** Selects destination of data and hsync for vc=2 fmt=26. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
19:18	0x0 RW	**Dest_vc2_fmt_25:** Selects destination of data and hsync for vc=2 fmt=25. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
17:16	0x0 RW	**Dest_vc2_fmt_24:** Selects destination of data and hsync for vc=2 fmt=24. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
15:14	0x0 RW	**Dest_vc2_fmt_23:** Selects destination of data and hsync for vc=2 fmt=23. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
13:12	0x0 RW	**Dest_vc2_fmt_22:** Selects destination of data and hsync for vc=2 fmt=22. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
11:10	0x0 RW	**Dest_vc2_fmt_21:** Selects destination of data and hsync for vc=2 fmt=21. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
9:8	0x0 RW	**Dest_vc2_fmt_20:** Selects destination of data and hsync for vc=2 fmt=20. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.

Bit Range	Default and Access	Field Name (ID): Description
7:6	0x0 RW	**Dest_vc2_fmt_19:** Selects destination of data and hsync for vc=2 fmt=19. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
5:4	0x0 RW	**Dest_vc2_fmt_18:** Selects destination of data and hsync for vc=2 fmt=18. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
3:2	0x0 RW	**Dest_vc2_fmt_17:** Selects destination of data and hsync for vc=2 fmt=17. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
1:0	0x0 RW	**Dest_vc2_fmt_16:** Selects destination of data and hsync for vc=2 fmt=16. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.

5.2.234 IFMT_input_switch__reg6 (is_2400_ifmt_gp_reg_IFMT_input_switch__reg6)—Offset 30818h

GP reg input switch data and hsync look-up table Register 6

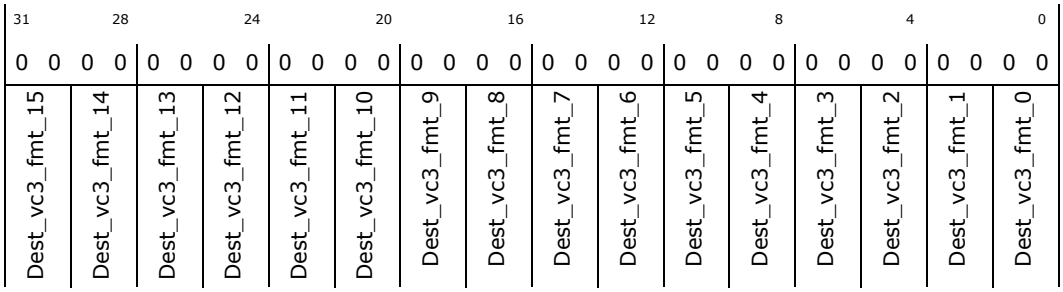
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30818h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**Dest_vc3_fmt_15:** Selects destination of data and hsync for vc=3 fmt=15. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
29:28	0x0 RW	**Dest_vc3_fmt_14:** Selects destination of data and hsync for vc=3 fmt=14. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.

Bit Range	Default and Access	Field Name (ID): Description
27:26	0x0 RW	**Dest_vc3_fmt_13:** Selects destination of data and hsync for vc=3 fmt=13. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
25:24	0x0 RW	**Dest_vc3_fmt_12:** Selects destination of data and hsync for vc=3 fmt=12. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
23:22	0x0 RW	**Dest_vc3_fmt_11:** Selects destination of data and hsync for vc=3 fmt=11. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
21:20	0x0 RW	**Dest_vc3_fmt_10:** Selects destination of data and hsync for vc=3 fmt=10. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
19:18	0x0 RW	**Dest_vc3_fmt_9:** Selects destination of data and hsync for vc=3 fmt=9. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
17:16	0x0 RW	**Dest_vc3_fmt_8:** Selects destination of data and hsync for vc=3 fmt=8. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
15:14	0x0 RW	**Dest_vc3_fmt_7:** Selects destination of data and hsync for vc=3 fmt=7. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
13:12	0x0 RW	**Dest_vc3_fmt_6:** Selects destination of data and hsync for vc=3 fmt=6. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
11:10	0x0 RW	**Dest_vc3_fmt_5:** Selects destination of data and hsync for vc=3 fmt=5. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
9:8	0x0 RW	**Dest_vc3_fmt_4:** Selects destination of data and hsync for vc=3 fmt=4. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
7:6	0x0 RW	**Dest_vc3_fmt_3:** Selects destination of data and hsync for vc=3 fmt=3. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
5:4	0x0 RW	**Dest_vc3_fmt_2:** Selects destination of data and hsync for vc=3 fmt=2. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
3:2	0x0 RW	**Dest_vc3_fmt_1:** Selects destination of data and hsync for vc=3 fmt=1. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
1:0	0x0 RW	**Dest_vc3_fmt_0:** Selects destination of data and hsync for vc=3 fmt=0. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.

5.2.235 IFMT_input_switch__reg7 (is_2400_ifmt_gp_reg_IFMT_input_switch__reg7)— Offset 3081Ch

GP reg input switch data and hsync look-up table Register 7

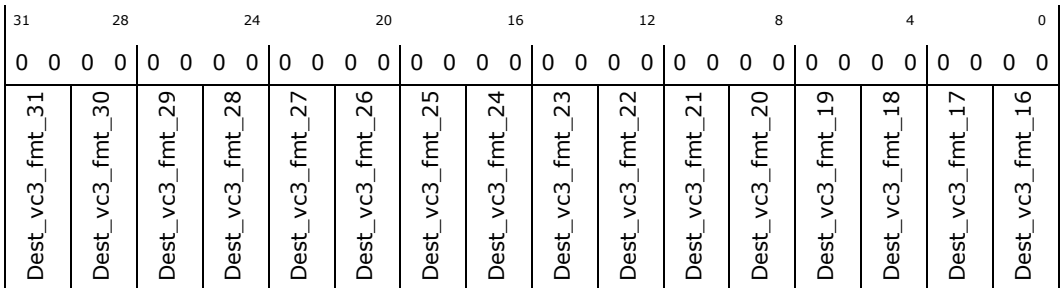
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3081Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**Dest_vc3_fmt_31:** Selects destination of data and hsync for vc=3 fmt=31. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
29:28	0x0 RW	**Dest_vc3_fmt_30:** Selects destination of data and hsync for vc=3 fmt=30. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
27:26	0x0 RW	**Dest_vc3_fmt_29:** Selects destination of data and hsync for vc=3 fmt=29. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
25:24	0x0 RW	**Dest_vc3_fmt_28:** Selects destination of data and hsync for vc=3 fmt=28. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
23:22	0x0 RW	**Dest_vc3_fmt_27:** Selects destination of data and hsync for vc=3 fmt=27. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
21:20	0x0 RW	**Dest_vc3_fmt_26:** Selects destination of data and hsync for vc=3 fmt=26. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
19:18	0x0 RW	**Dest_vc3_fmt_25:** Selects destination of data and hsync for vc=3 fmt=25. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
17:16	0x0 RW	**Dest_vc3_fmt_24:** Selects destination of data and hsync for vc=3 fmt=24. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.

Bit Range	Default and Access	Field Name (ID): Description
15:14	0x0 RW	**Dest_vc3_fmt_23:** Selects destination of data and hsync for vc=3 fmt=23. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
13:12	0x0 RW	**Dest_vc3_fmt_22:** Selects destination of data and hsync for vc=3 fmt=22. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
11:10	0x0 RW	**Dest_vc3_fmt_21:** Selects destination of data and hsync for vc=3 fmt=21. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
9:8	0x0 RW	**Dest_vc3_fmt_20:** Selects destination of data and hsync for vc=3 fmt=20. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
7:6	0x0 RW	**Dest_vc3_fmt_19:** Selects destination of data and hsync for vc=3 fmt=19. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
5:4	0x0 RW	**Dest_vc3_fmt_18:** Selects destination of data and hsync for vc=3 fmt=18. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
3:2	0x0 RW	**Dest_vc3_fmt_17:** Selects destination of data and hsync for vc=3 fmt=17. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.
1:0	0x0 RW	**Dest_vc3_fmt_16:** Selects destination of data and hsync for vc=3 fmt=16. 00-data is discarded, 01-primary input formatter, 10-secondary input formatter, 11-stream2mem.

5.2.236 IFMT_input_switch_fsync_ (is_2400_ifmt_gp_reg_IFMT_input_switch_fsync_)—Offset 30820h

GP reg input switch frame synchronization signal look-up table register

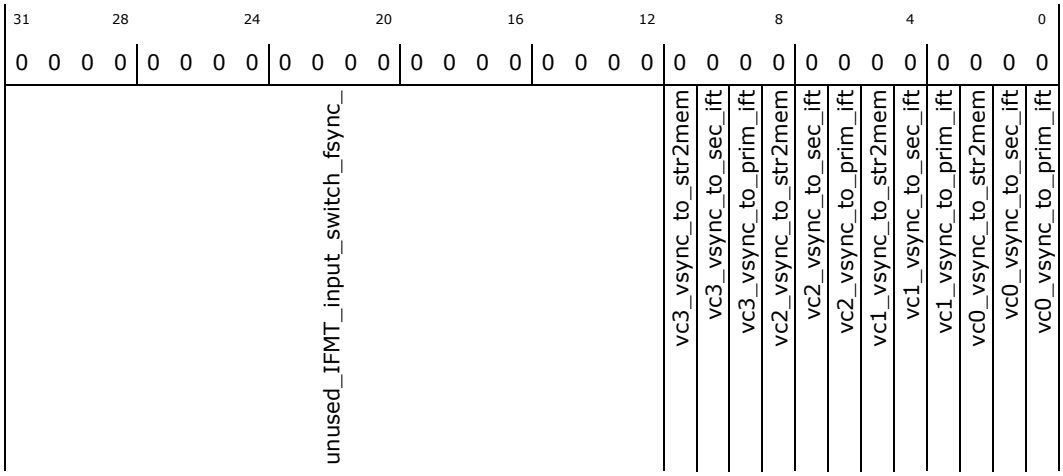
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30820h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved (unused_IFMT_input_switch_fsync_):** Unused
11	0x0 RW	**vc3_vsync_to_str2mem:** If '1', sof and eof on vc3 will be lead to the stream2mem
10	0x0 RW	**vc3_vsync_to_sec_ift:** If '1', sof and eof on vc3 will be lead to the secondary input formatter
9	0x0 RW	**vc3_vsync_to_prim_ift:** If '1', sof and eof on vc3 will be lead to the primary input formatters
8	0x0 RW	**vc2_vsync_to_str2mem:** If '1', sof and eof on vc2 will be lead to the stream2mem
7	0x0 RW	**vc2_vsync_to_sec_ift:** If '1', sof and eof on vc2 will be lead to the secondary input formatter
6	0x0 RW	**vc2_vsync_to_prim_ift:** If '1', sof and eof on vc2 will be lead to the primary input formatters
5	0x0 RW	**vc1_vsync_to_str2mem:** If '1', sof and eof on vc1 will be lead to the stream2mem
4	0x0 RW	**vc1_vsync_to_sec_ift:** If '1', sof and eof on vc1 will be lead to the secondary input formatter
3	0x0 RW	**vc1_vsync_to_prim_ift:** If '1', sof and eof on vc1 will be lead to the primary input formatters
2	0x0 RW	**vc0_vsync_to_str2mem:** If '1', sof and eof on vc0 will be lead to the stream2mem
1	0x0 RW	**vc0_vsync_to_sec_ift:** If '1', sof and eof on vc0 will be lead to the secondary input formatter
0	0x0 RW	**vc0_vsync_to_prim_ift:** If '1', sof and eof on vc0 will be lead to the primary input formatters

5.2.237 IFMT_srst (is_2400_ifmt_gp_reg_IFMT_srst)—Offset 30824h

GP reg soft reset

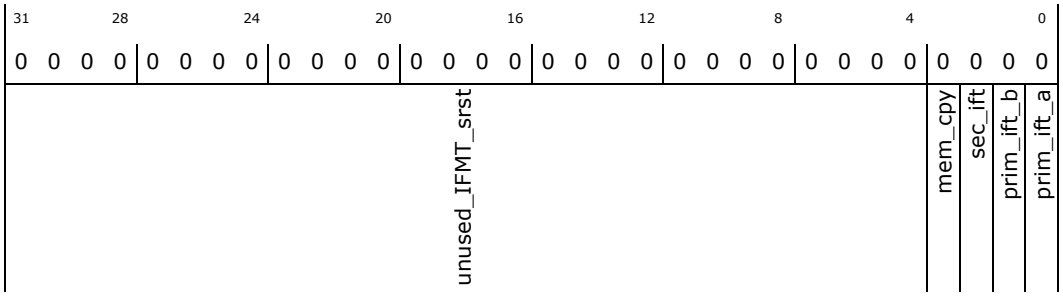
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30824h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_IFMT_srst):** Unused
3	0x0 RW	**mem_cpy:** Soft resets mem copy
2	0x0 RW	**sec_ift:** Soft resets secondary input formatter
1	0x0 RW	**prim_ift_b:** Soft resets primary input formatter B
0	0x0 RW	**prim_ift_a:** Soft resets primary input formatter A

5.2.238 IFMT_slv_reg_srst (is_2400_ifmt_gp_reg_IFMT_slv_reg_srst)—Offset 30828h

GP reg slave register soft reset

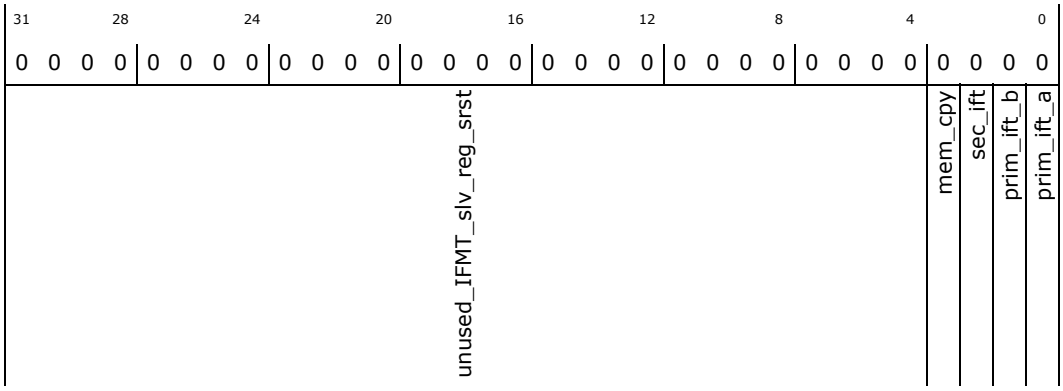
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30828h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_IFMT_slv_reg_srst):** Unused
3	0x0 RW	**mem_cpy:** Soft resets slave registers of mem copy
2	0x0 RW	**sec_ift:** Soft resets slave registers of secondary input formatter
1	0x0 RW	**prim_ift_b:** Soft resets slave registers of primary input formatter B
0	0x0 RW	**prim_ift_a:** Soft resets slave registers of primary input formatter A

5.2.239 IFMT_input_switch_ch_id_fmt_type (is_2400_ifmt_gp_reg_IFMT_input_switch_ch_id_fmt_type)—Offset 3082Ch

GP reg input switch status register

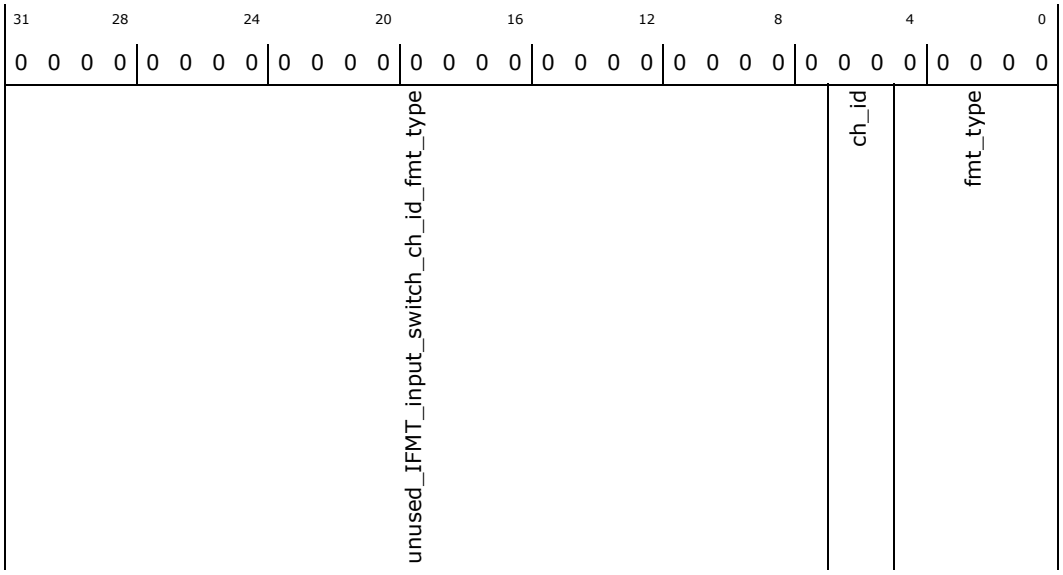
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 3082Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:7	0x0 RO	**Reserved (unused_IFMT_input_switch_ch_id_fmt_type):** Unused
6:5	0x0 RO	**ch_id:** Returns the channel id as it arrives at the input of the input switch
4:0	0x0 RO	**fmt_type:** Returns the format type as it arrives at the input of the input switch

5.2.240 IFMT_IRQ_ctrl_edge (is_2400_ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge)—Offset 30A00h

indicates for each IRQ bit whether an interrupt request should be generated on a falling edge (value='0') or a rising edge (value='1').

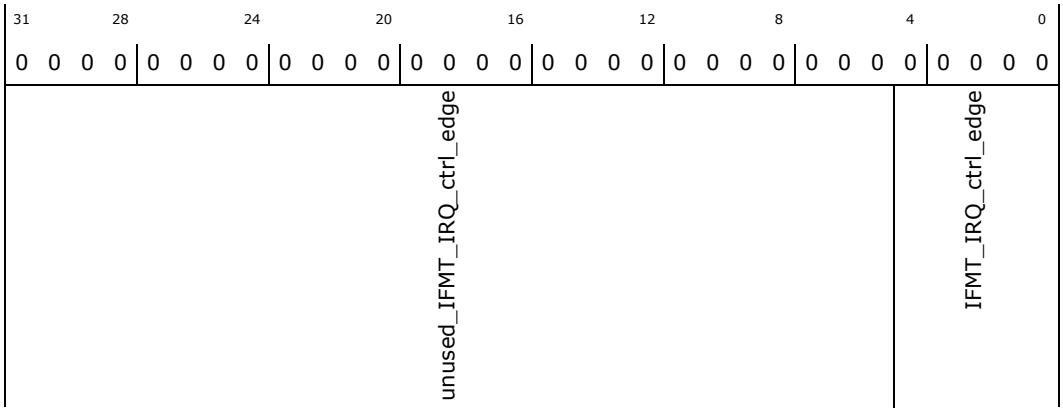
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30A00h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_IFMT_IRQ_ctrl_edge):** Unused
4:0	0x0 RW	**IFMT_IRQ_ctrl_edge:** indicates for each IRQ bit whether an interrupt request should be generated on a falling edge (value='0') or a rising edge (value='1').

5.2.241 IFMT_IRQ_ctrl_mask (is_2400_ifmt_irq_ctrl_IFMT_IRQ_ctrl_mask)—Offset 30A04h

indicates for each IRQ bit whether it can generate an interrupt request (value='1') or not (value='0'). Setting will affect reg_irq_value as well as IRQ output pin

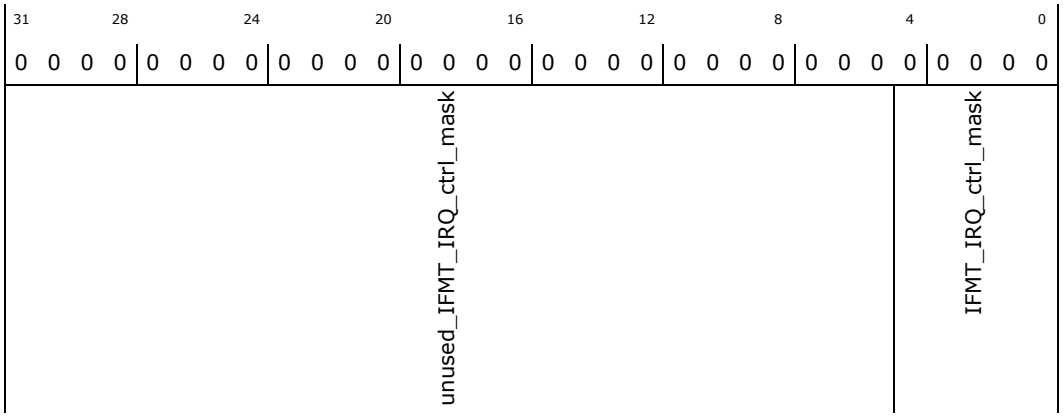
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30A04h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_IFMT_IRQ_ctrl_mask):** Unused
4:0	0x0 RW	**IFMT_IRQ_ctrl_mask:** indicates for each IRQ bit whether it can generate an interrupt request (value='1') or not (value='0'). Setting will affect reg_irq_value as well as IRQ output pin

5.2.242 IFMT_IRQ_ctrl_status (is_2400_ifmt_irq_ctrl_IFMT_IRQ_ctrl_status)—Offset 30A08h

IRQ controller STATUS

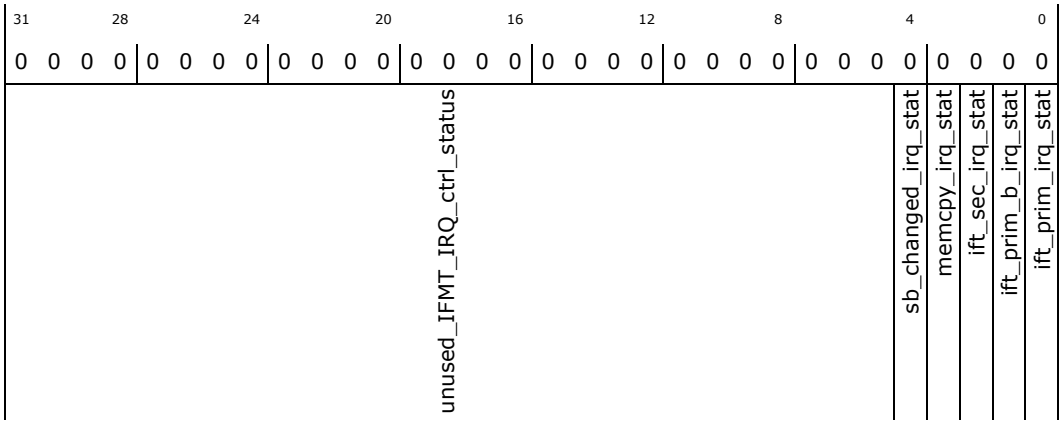
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30A08h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_IFMT_IRQ_ctrl_status):** Unused
4	0x0 RO	**sb_changed_irq_stat:** Returns the status of the IRQ signal indicating a change in either the channel id or the format type
3	0x0 RO	**memcpy_irq_stat:** Returns the status of the IRQ generated by the stream to memory device
2	0x0 RO	**ift_sec_irq_stat:** Returns the status of the IRQ generated by the secondary input formatter
1	0x0 RO	**ift_prim_b_irq_stat:** Returns the status of the IRQ generated by the primary input formatter b
0	0x0 RO	**ift_prim_irq_stat:** Returns the status of the IRQ generated by the primary input formatter

5.2.243 IFMT_IRQ_ctrl_clear (is_2400_ifmt_irq_ctrl_IFMT_IRQ_ctrl_clear)—Offset 30A0Ch

Clears (set to '0') bits in IFMT_IRQ_ctrl_status. When writing a '1' into a bit of this register, the corresponding bit in the IFMT_IRQ_ctrl_status is cleared. When writing a '0' into a bit of this register, the corresponding bit in the IFMT_IRQ_ctrl_status is not affected.

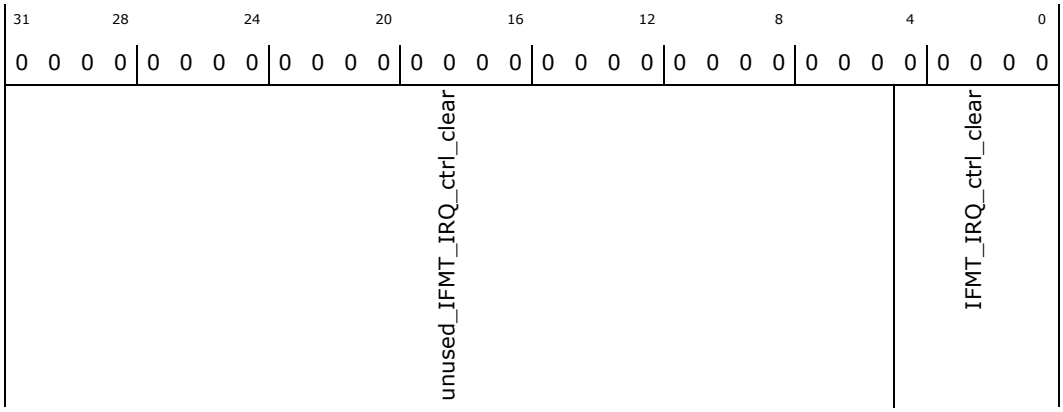
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30A0Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_IFMT_IRQ_ctrl_clear):** Unused
4:0	0x0 WO	**IFMT_IRQ_ctrl_clear:** Clears (set to '0') bits in IFMT_IRQ_ctrl_status. When writing a '1' into a bit of this register, the corresponding bit in the IFMT_IRQ_ctrl_status is cleared. When writing a '0' into a bit of this register, the corresponding bit in the IFMT_IRQ_ctrl_status is not affected.

5.2.244 IFMT_IRQ_ctrl_enable (is_2400_ifmt_irq_ctrl_IFMT_IRQ_ctrl_enable)—Offset 30A10h

Indicates for each bit whether an interrupt cause as monitored by the IFMT_IRQ_ctrl_status register also affects the IRQ pin (value='1') or not (value='0')

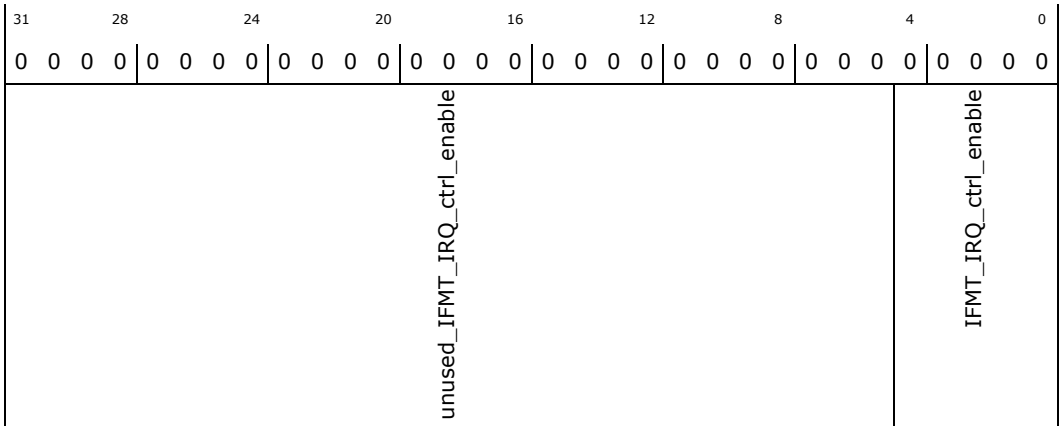
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30A10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_IFMT_IRQ_ctrl_enable):** Unused
4:0	0x0 RW	**IFMT_IRQ_ctrl_enable:** Indicates for each bit whether an interrupt cause as monitored by the IFMT_IRQ_ctrl_status register also affects the IRQ pin (value='1') or not (value='0')

5.2.245 IFMT_IRQ_ctrl_edge_pulse (is_2400_ifmt_irq_ctrl_IFMT_IRQ_ctrl_edge_pulse)—Offset 30A14h

Indicates for each bit whether an interrupt cause is translated into a pulse (value='0') or into a constant level '1' (value='1') on the IRQ pin

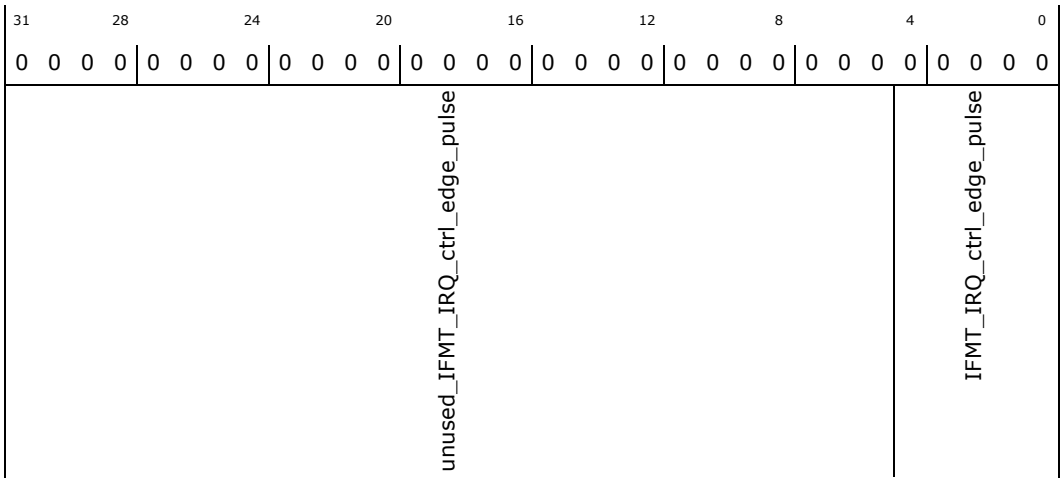
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 30A14h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_IFMT_IRQ_ctrl_edge_pulse):** Unused
4:0	0x0 RW	**IFMT_IRQ_ctrl_edge_pulse:** Indicates for each bit whether an interrupt cause is translated into a pulse (value='0') or into a constant level '1' (value='1') on the IRQ pin

5.2.246 DMA_FSM_Command (isp_dma_DMA_FSM_Command)—Offset 40000h

FSM Command: Last command and State

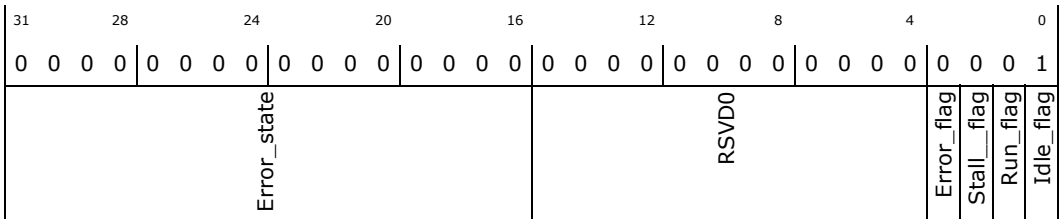
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 40000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RO	**Error_state:** Lower 16 bits of the last command received and processed
15:4	0x0 RO	**RSVD0:** Reserved
3	0x0 RO	**Error_flag:** Error flag
2	0x0 RO	**Stall__flag:** Stall flag
1	0x0 RO	**Run_flag:** Run flag
0	0x1 RO	**Idle_flag:** Idle flag

5.2.247 DMA_CH0_ConnectionID_sgnzext (isp_dma_DMA_CH0_ConnectionID_sgnzext)—Offset 41000h

DMA CH 0 PARAM 0: Connection ID and Zero/Sign extension settings

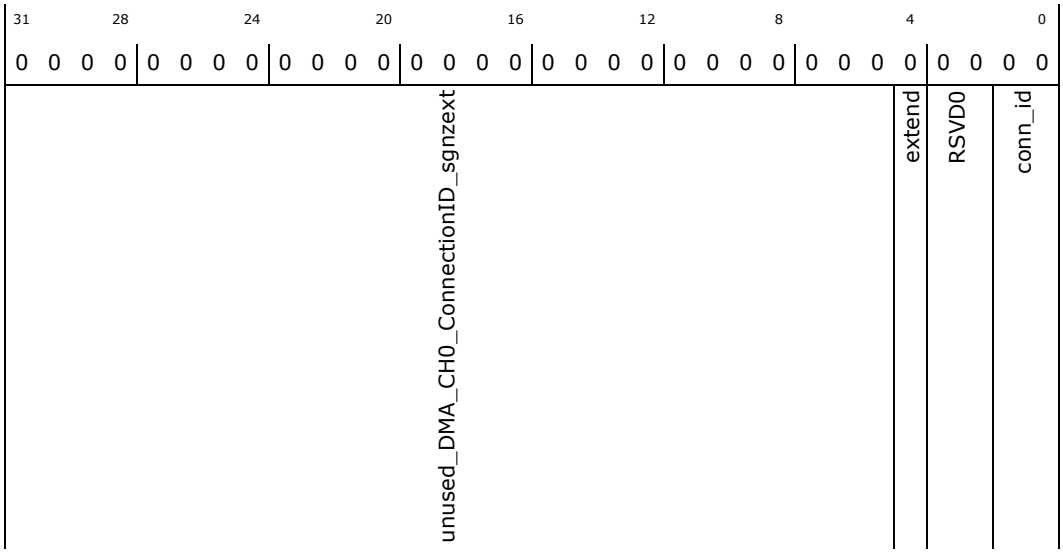
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH0_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.248 DMA_CH1_ConnectionID_sgnzext (isp_dma_DMA_CH1_ConnectionID_sgnzext)—Offset 41004h

DMA CH 1 PARAM 0: Connection ID and Zero/Sign extension settings

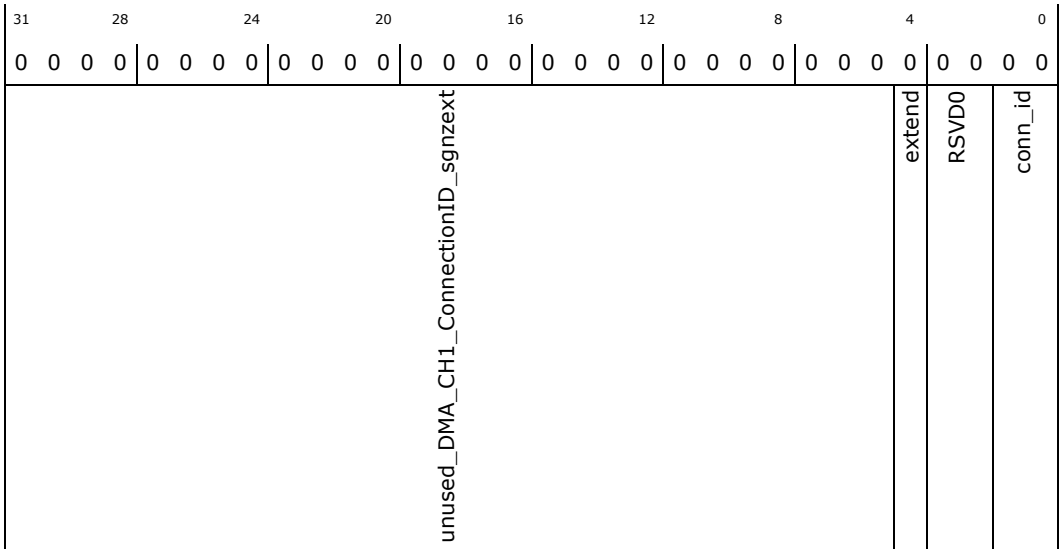
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH1_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.249 DMA_CH2_ConnectionID_sgnzext (isp_dma_DMA_CH2_ConnectionID_sgnzext)—Offset 41008h

DMA CH 2 PARAM 0: Connection ID and Zero/Sign extension settings

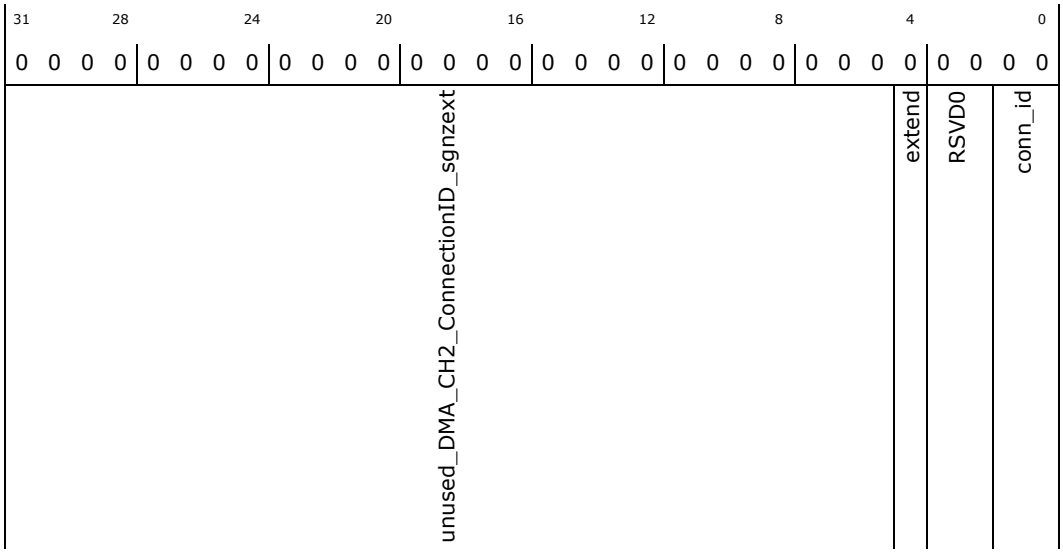
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH2_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.250 DMA_CH3_ConnectionID_sgnzext (isp_dma_DMA_CH3_ConnectionID_sgnzext)—Offset 4100Ch

DMA CH 3 PARAM 0: Connection ID and Zero/Sign extension settings

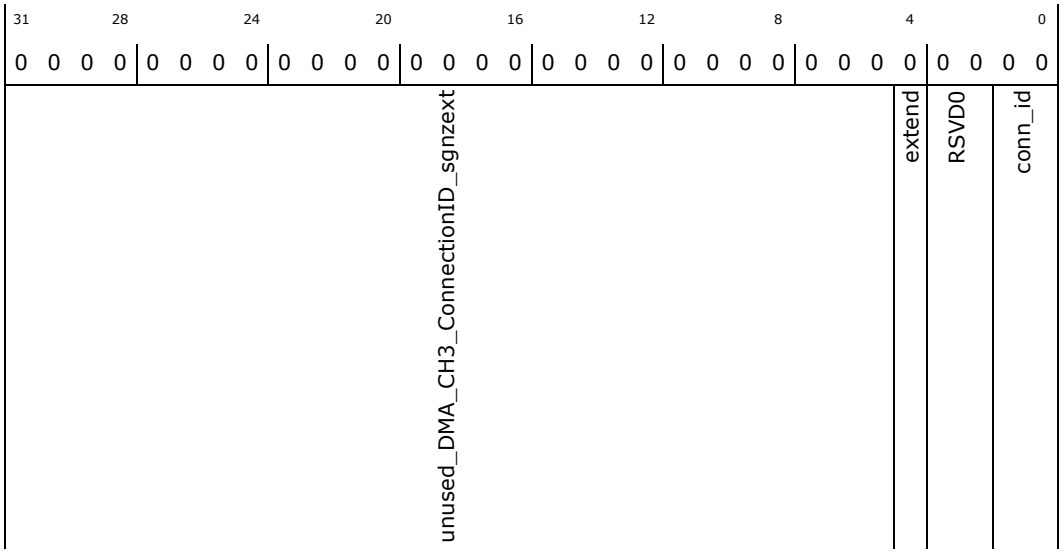
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4100Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH3_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.251 DMA_CH4_ConnectionID_sgnzext (isp_dma_DMA_CH4_ConnectionID_sgnzext)—Offset 41010h

DMA CH 4 PARAM 0: Connection ID and Zero/Sign extension settings

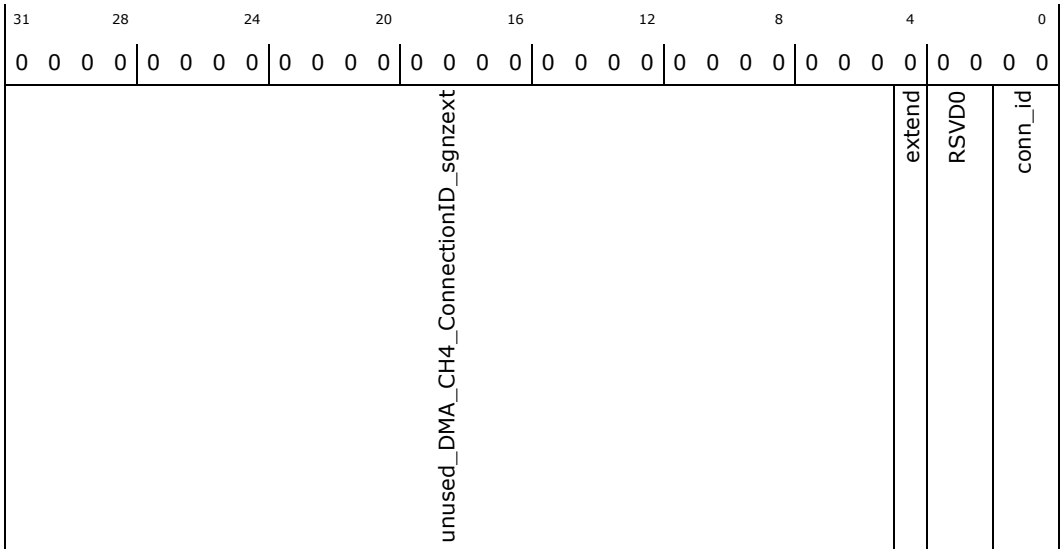
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH4_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.252 DMA_CH5_ConnectionID_sgnzext (isp_dma_DMA_CH5_ConnectionID_sgnzext)—Offset 41014h

DMA CH 5 PARAM 0: Connection ID and Zero/Sign extension settings

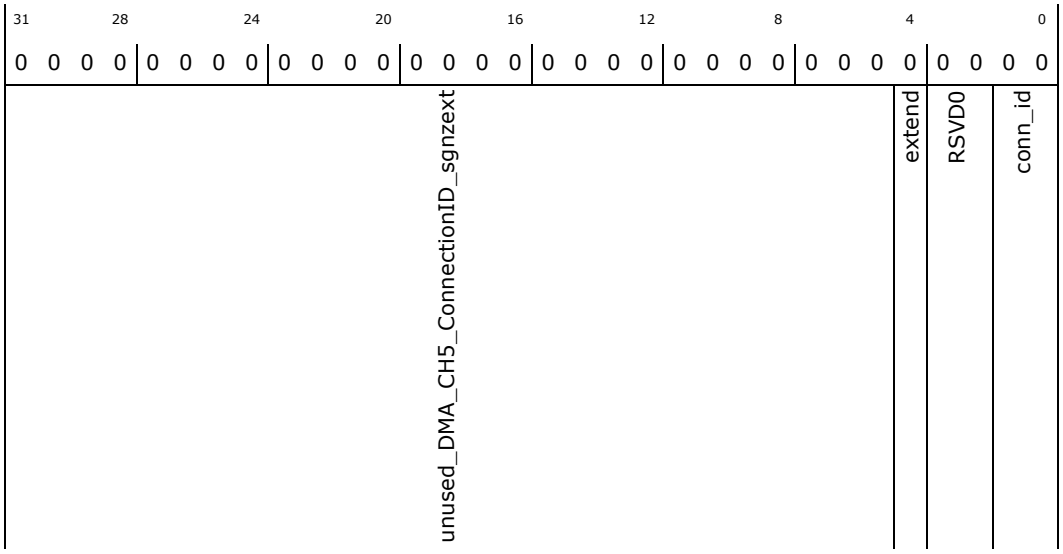
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH5_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.253 DMA_CH6_ConnectionID_sgnzext (isp_dma_DMA_CH6_ConnectionID_sgnzext)—Offset 41018h

DMA CH 6 PARAM 0: Connection ID and Zero/Sign extension settings

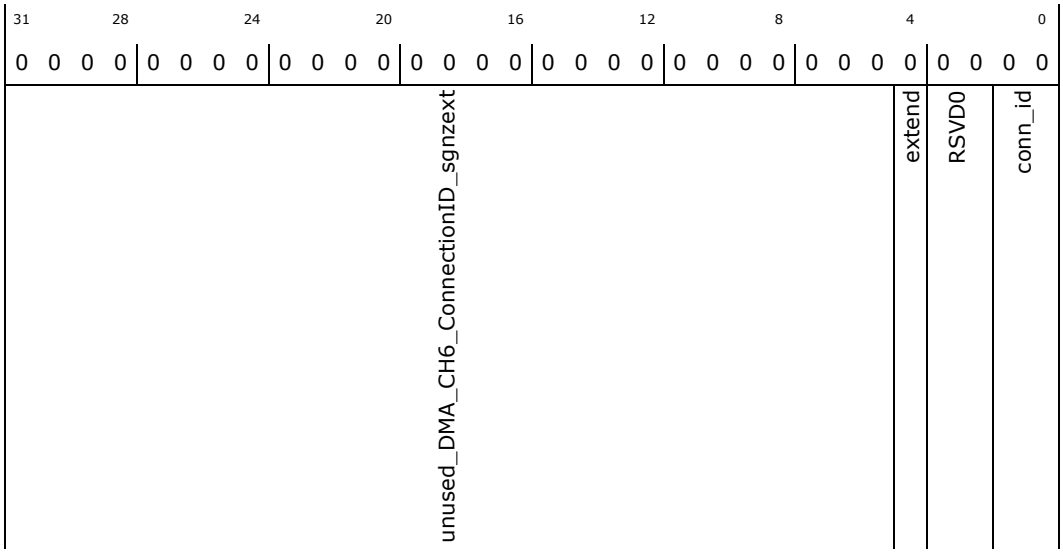
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH6_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.254 DMA_CH7_ConnectionID_sgnzext (isp_dma_DMA_CH7_ConnectionID_sgnzext)—Offset 4101Ch

DMA CH 7 PARAM 0: Connection ID and Zero/Sign extension settings

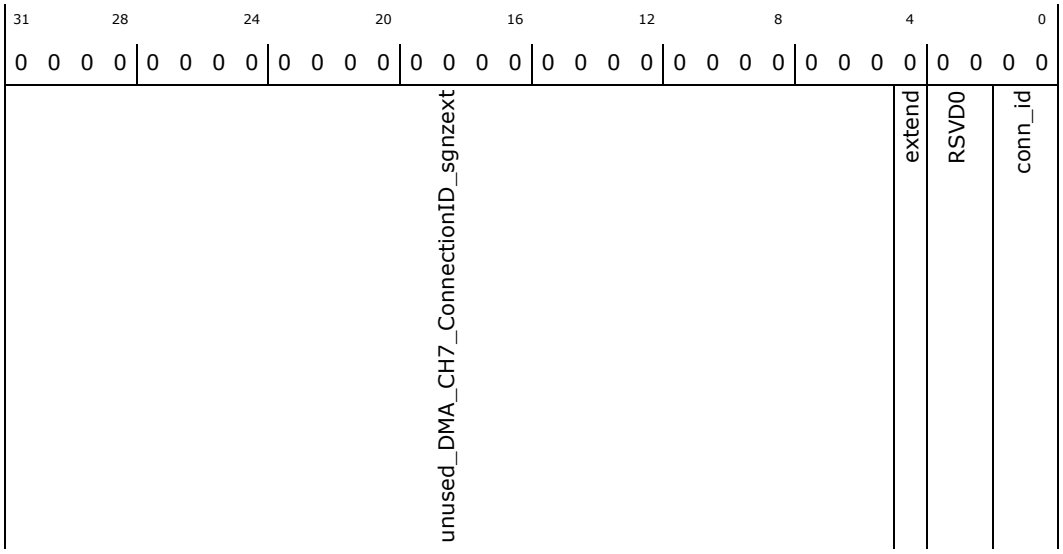
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4101Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH7_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.255 DMA_CH8_ConnectionID_sgnzext (isp_dma_DMA_CH8_ConnectionID_sgnzext)—Offset 41020h

DMA CH 8 PARAM 0: Connection ID and Zero/Sign extension settings

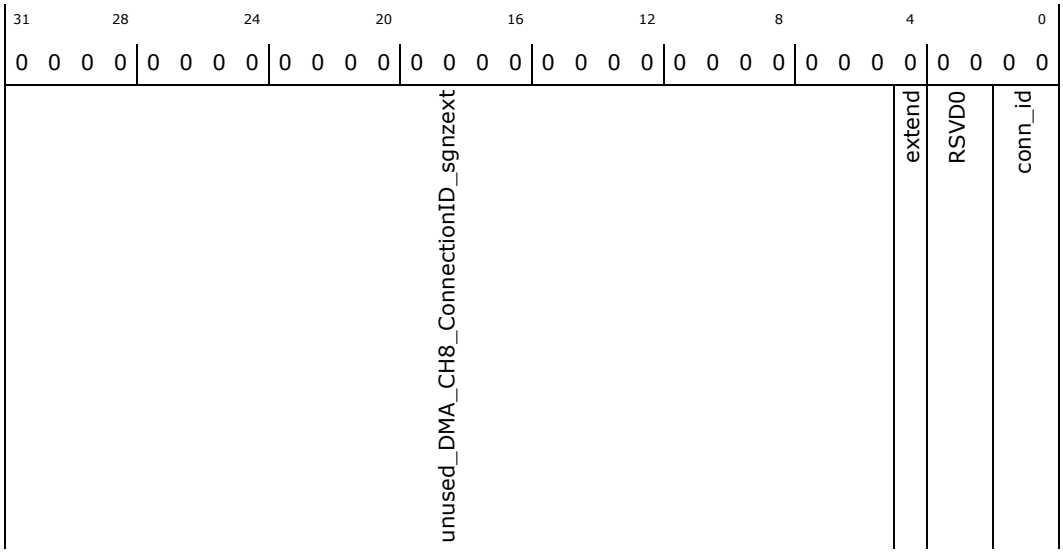
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH8_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.256 DMA_CH9_ConnectionID_sgnzext (isp_dma_DMA_CH9_ConnectionID_sgnzext)—Offset 41024h

DMA CH 9 PARAM 0: Connection ID and Zero/Sign extension settings

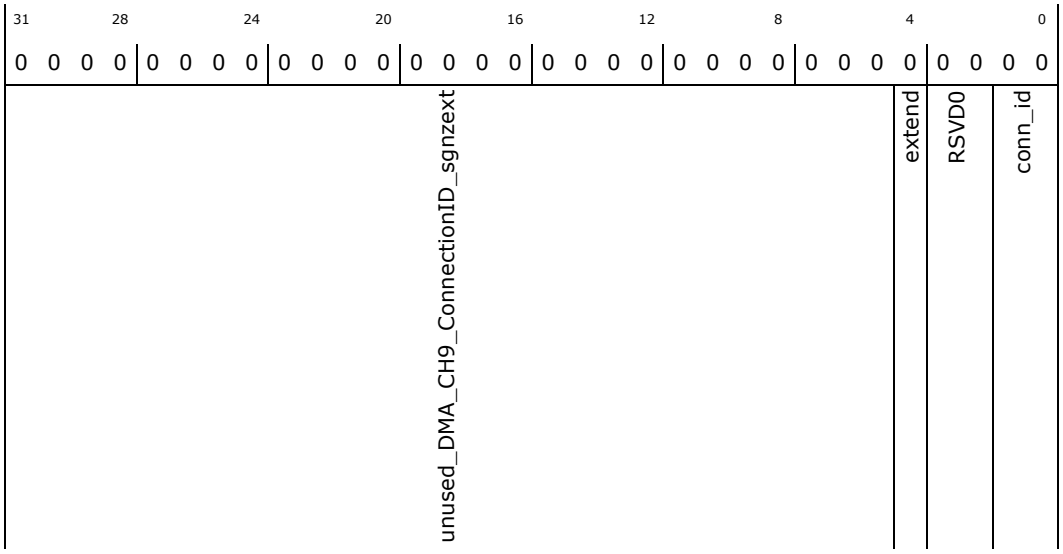
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH9_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.257 DMA_CH10_ConnectionID_sgnzext (isp_dma_DMA_CH10_ConnectionID_sgnzext)—Offset 41028h

DMA CH 10 PARAM 0: Connection ID and Zero/Sign extension settings

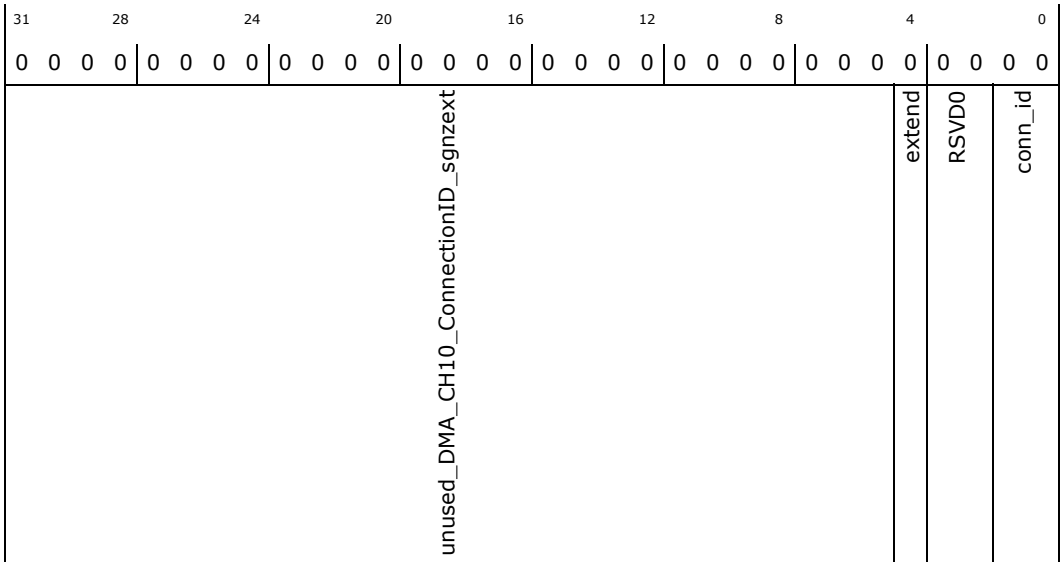
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH10_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.258 DMA_CH11_ConnectionID_sgnzext (isp_dma_DMA_CH11_ConnectionID_sgnzext)—Offset 4102Ch

DMA CH 11 PARAM 0: Connection ID and Zero/Sign extension settings

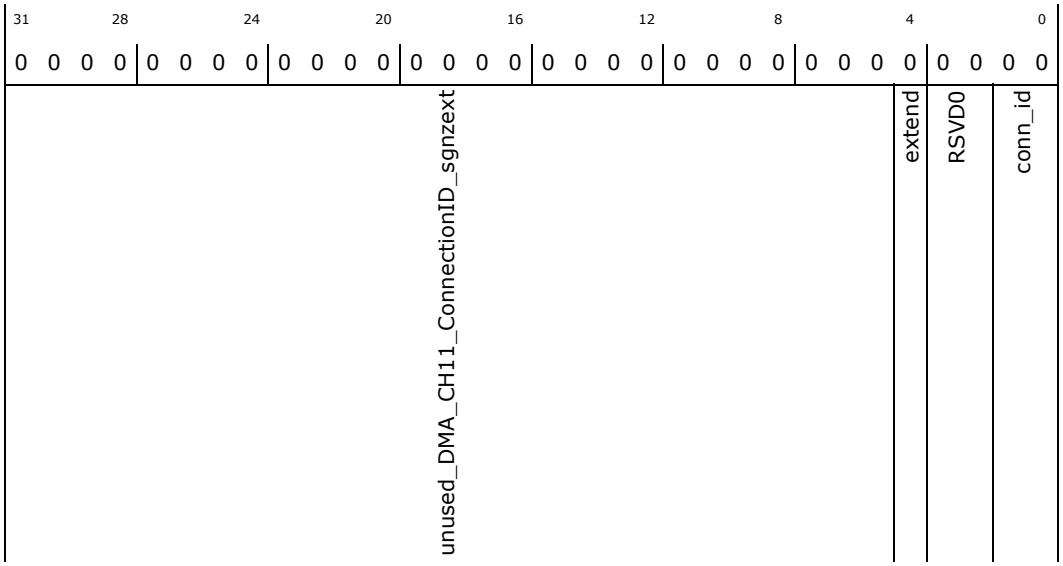
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4102Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH11_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.259 DMA_CH12_ConnectionID_sgnzext (isp_dma_DMA_CH12_ConnectionID_sgnzext)—Offset 41030h

DMA CH 12 PARAM 0: Connection ID and Zero/Sign extension settings

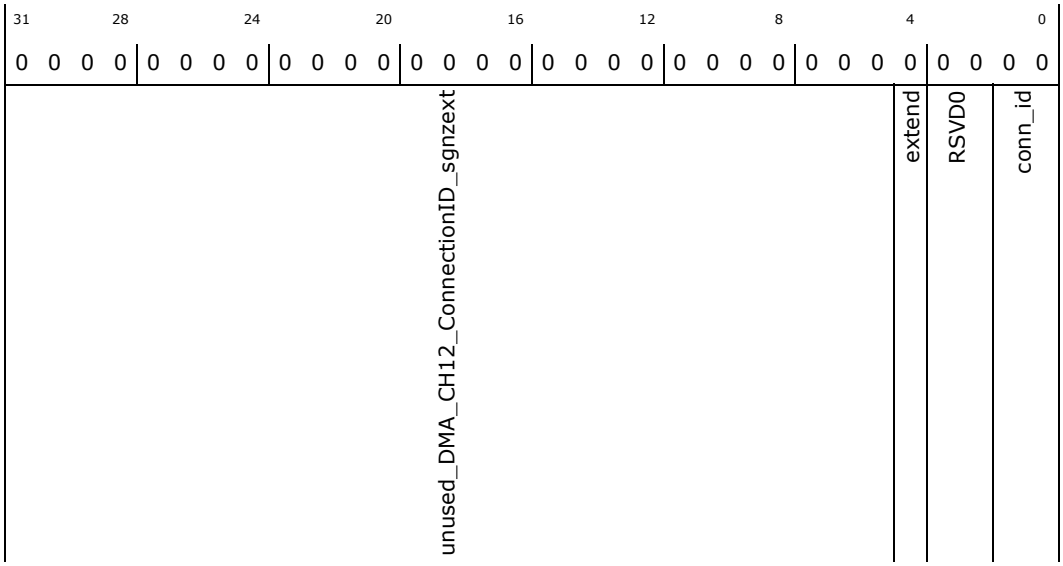
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH12_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.260 DMA_CH13_ConnectionID_sgnzext (isp_dma_DMA_CH13_ConnectionID_sgnzext)—Offset 41034h

DMA CH 13 PARAM 0: Connection ID and Zero/Sign extension settings

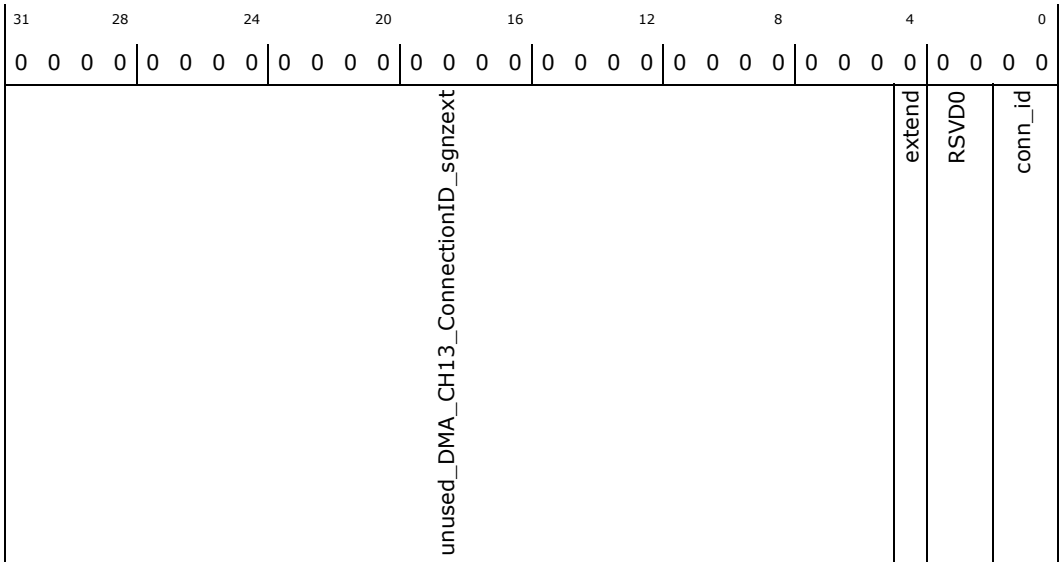
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH13_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.261 DMA_CH14_ConnectionID_sgnzext (isp_dma_DMA_CH14_ConnectionID_sgnzext)—Offset 41038h

DMA CH 14 PARAM 0: Connection ID and Zero/Sign extension settings

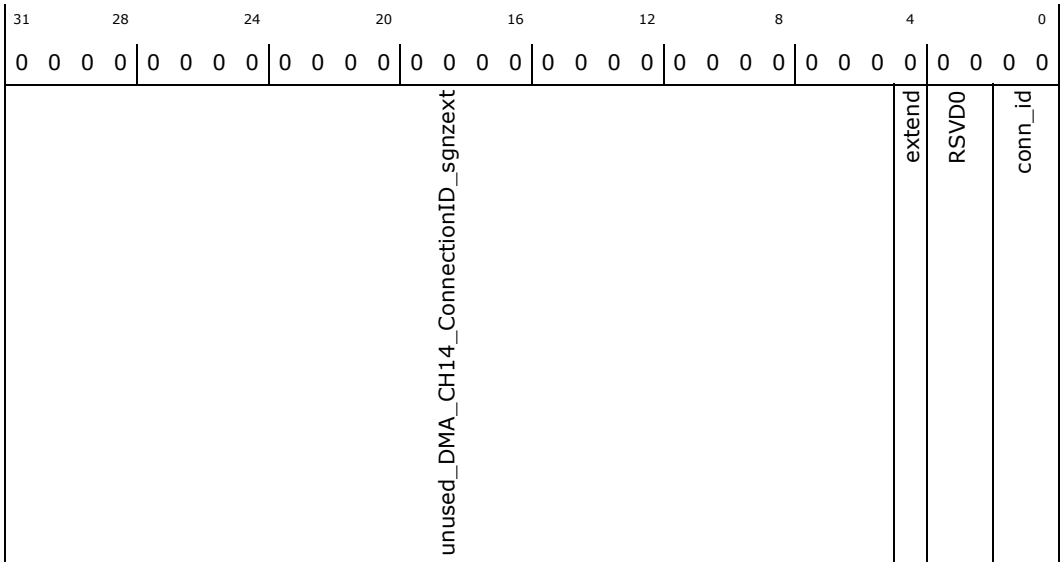
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH14_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.262 DMA_CH15_ConnectionID_sgnzext (isp_dma_DMA_CH15_ConnectionID_sgnzext)—Offset 4103Ch

DMA CH 15 PARAM 0: Connection ID and Zero/Sign extension settings

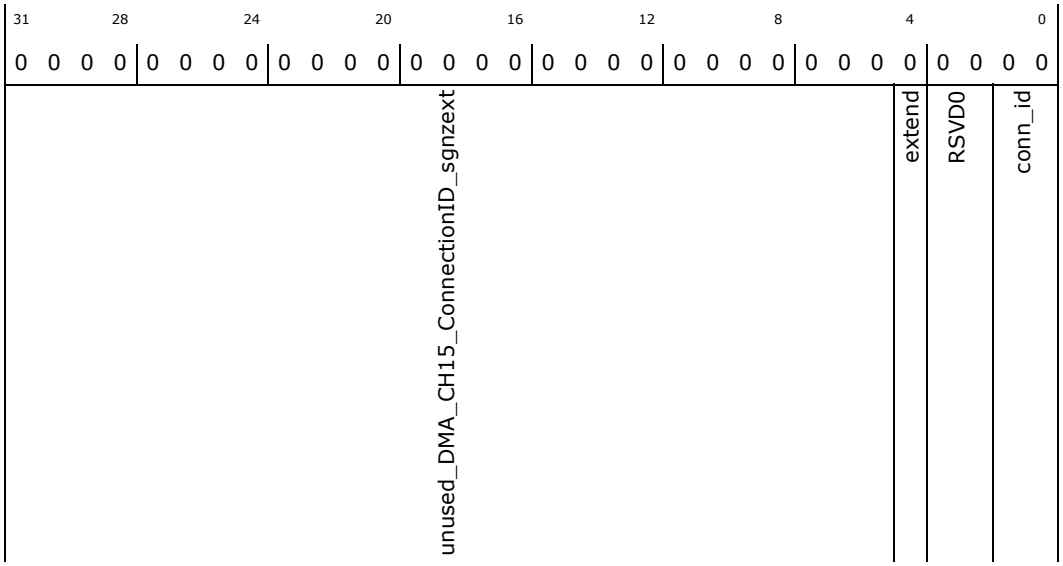
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4103Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH15_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.263 DMA_CH16_ConnectionID_sgnzext (isp_dma_DMA_CH16_ConnectionID_sgnzext)—Offset 41040h

DMA CH 16 PARAM 0: Connection ID and Zero/Sign extension settings

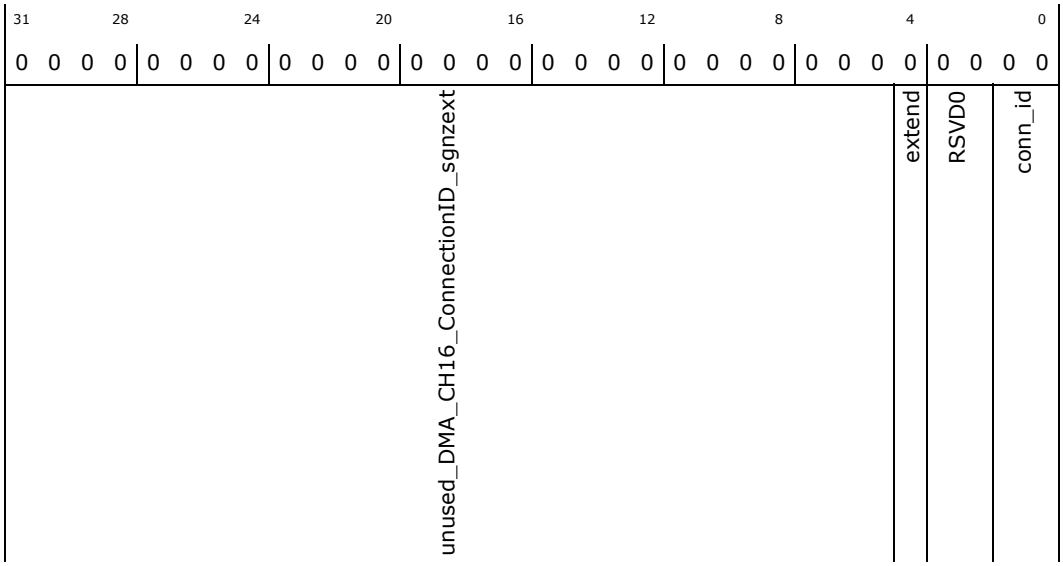
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41040h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH16_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.264 DMA_CH17_ConnectionID_sgnzext (isp_dma_DMA_CH17_ConnectionID_sgnzext)—Offset 41044h

DMA CH 17 PARAM 0: Connection ID and Zero/Sign extension settings

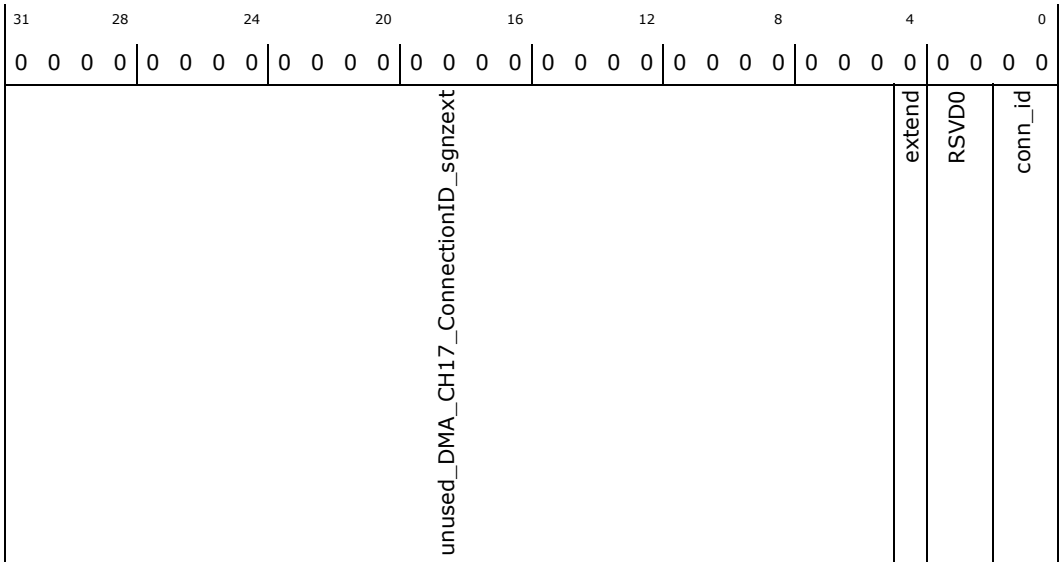
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41044h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH17_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.265 DMA_CH18_ConnectionID_sgnzext (isp_dma_DMA_CH18_ConnectionID_sgnzext)—Offset 41048h

DMA CH 18 PARAM 0: Connection ID and Zero/Sign extension settings

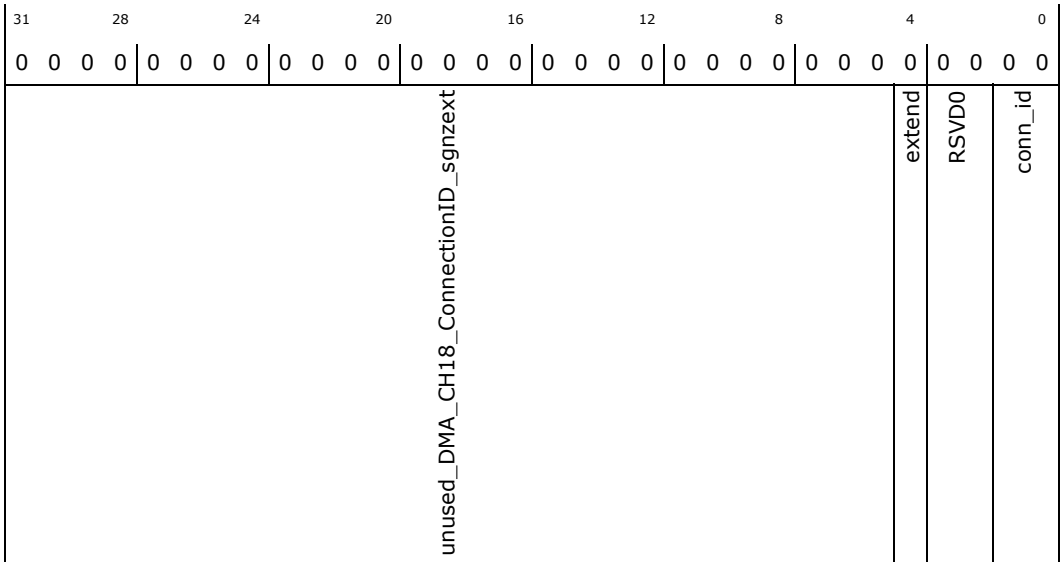
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41048h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH18_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.266 DMA_CH19_ConnectionID_sgnzext (isp_dma_DMA_CH19_ConnectionID_sgnzext)—Offset 4104Ch

DMA CH 19 PARAM 0: Connection ID and Zero/Sign extension settings

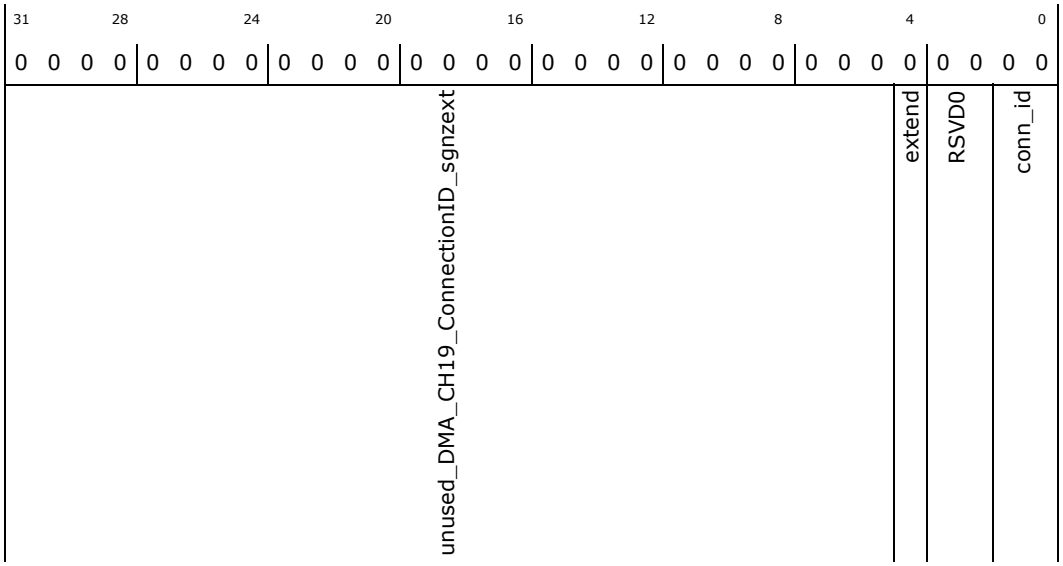
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4104Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH19_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.267 DMA_CH20_ConnectionID_sgnzext (isp_dma_DMA_CH20_ConnectionID_sgnzext)—Offset 41050h

DMA CH 20 PARAM 0: Connection ID and Zero/Sign extension settings

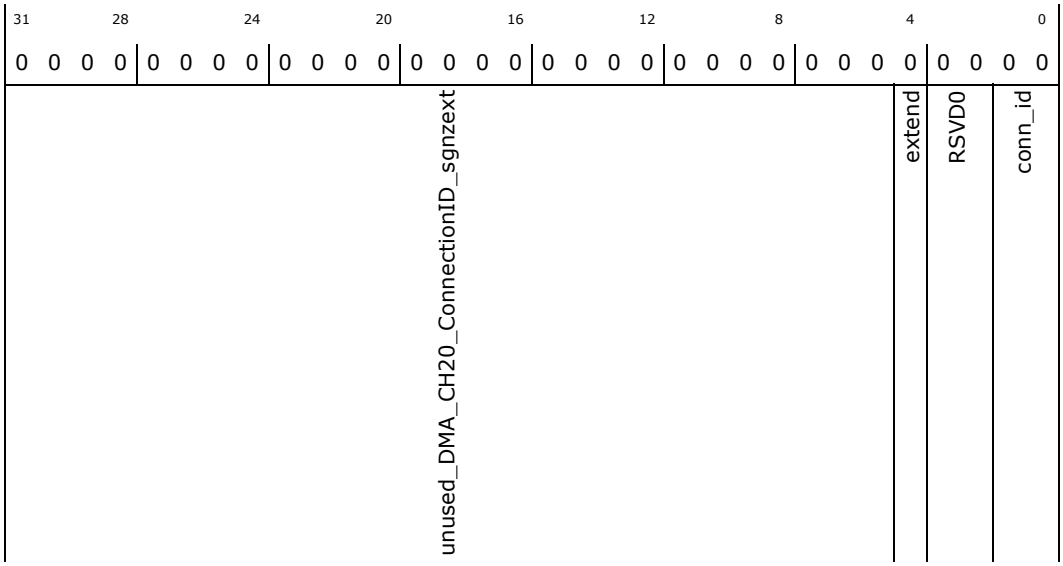
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41050h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH20_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.268 DMA_CH21_ConnectionID_sgnzext (isp_dma_DMA_CH21_ConnectionID_sgnzext)—Offset 41054h

DMA CH 21 PARAM 0: Connection ID and Zero/Sign extension settings

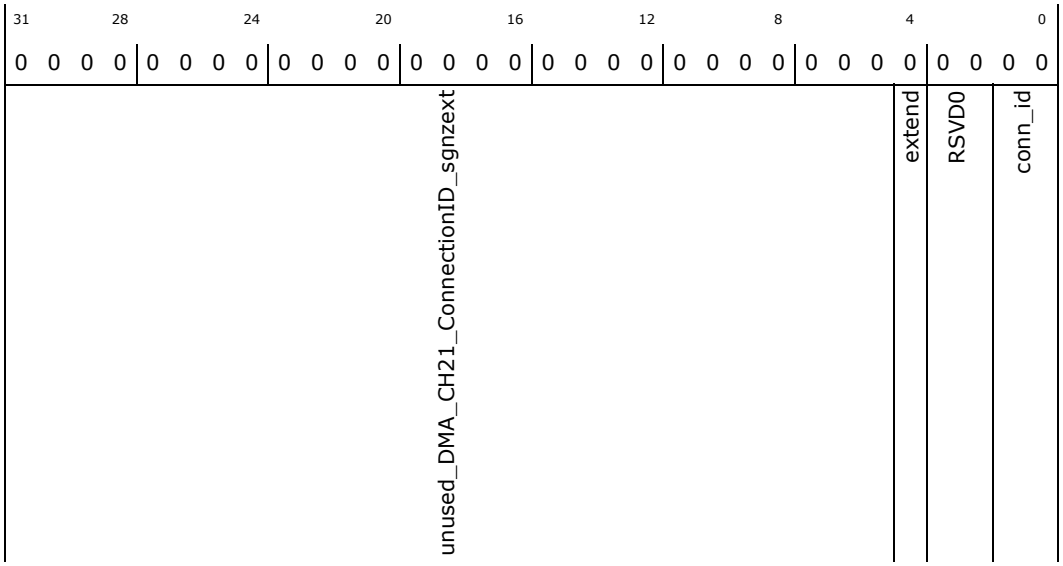
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41054h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH21_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.269 DMA_CH22_ConnectionID_sgnzext (isp_dma_DMA_CH22_ConnectionID_sgnzext)—Offset 41058h

DMA CH 22 PARAM 0: Connection ID and Zero/Sign extension settings

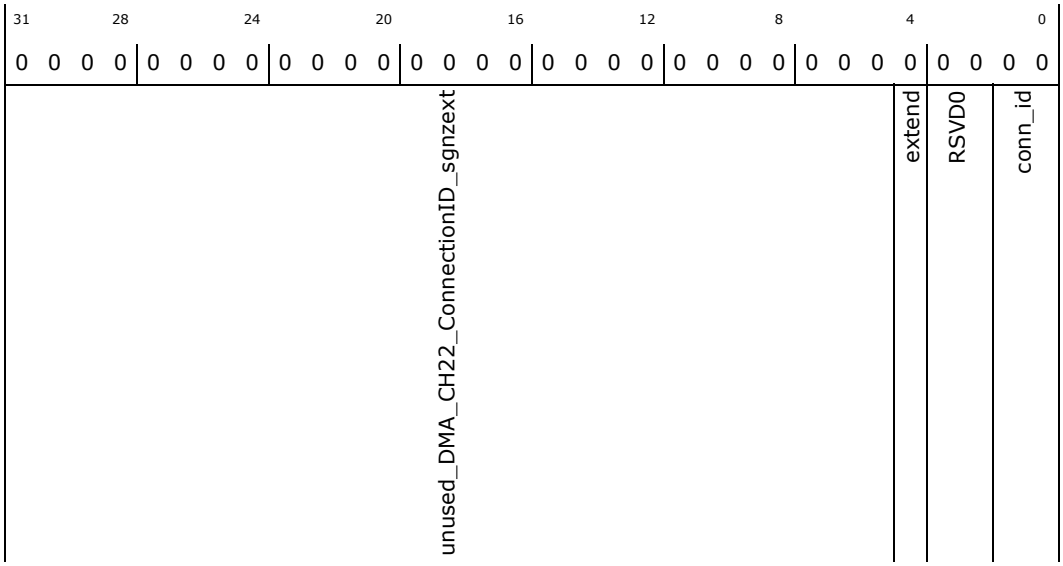
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41058h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH22_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.270 DMA_CH23_ConnectionID_sgnzext (isp_dma_DMA_CH23_ConnectionID_sgnzext)—Offset 4105Ch

DMA CH 23 PARAM 0: Connection ID and Zero/Sign extension settings

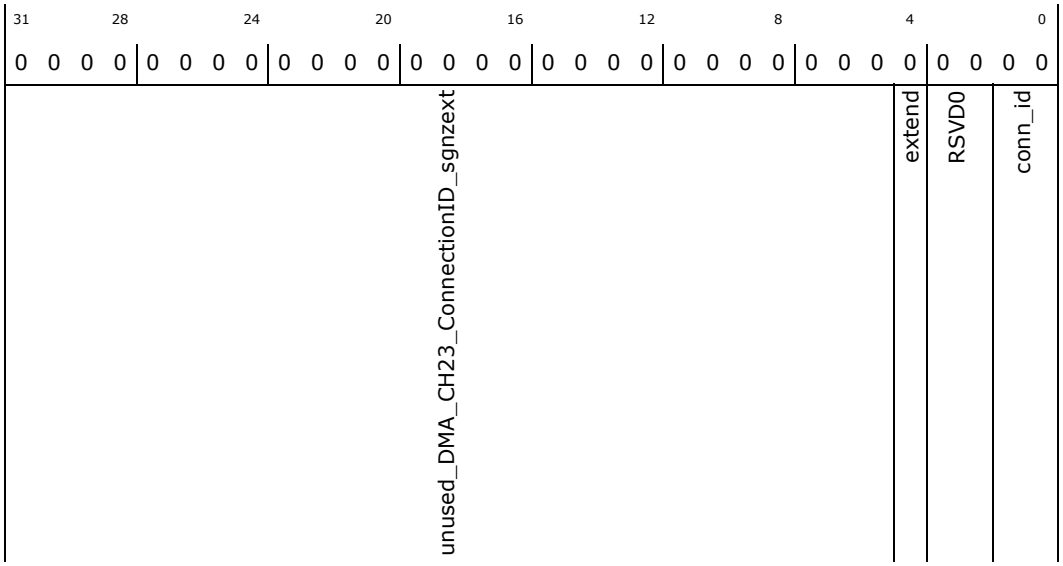
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4105Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH23_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.271 DMA_CH24_ConnectionID_sgnzext (isp_dma_DMA_CH24_ConnectionID_sgnzext)—Offset 41060h

DMA CH 24 PARAM 0: Connection ID and Zero/Sign extension settings

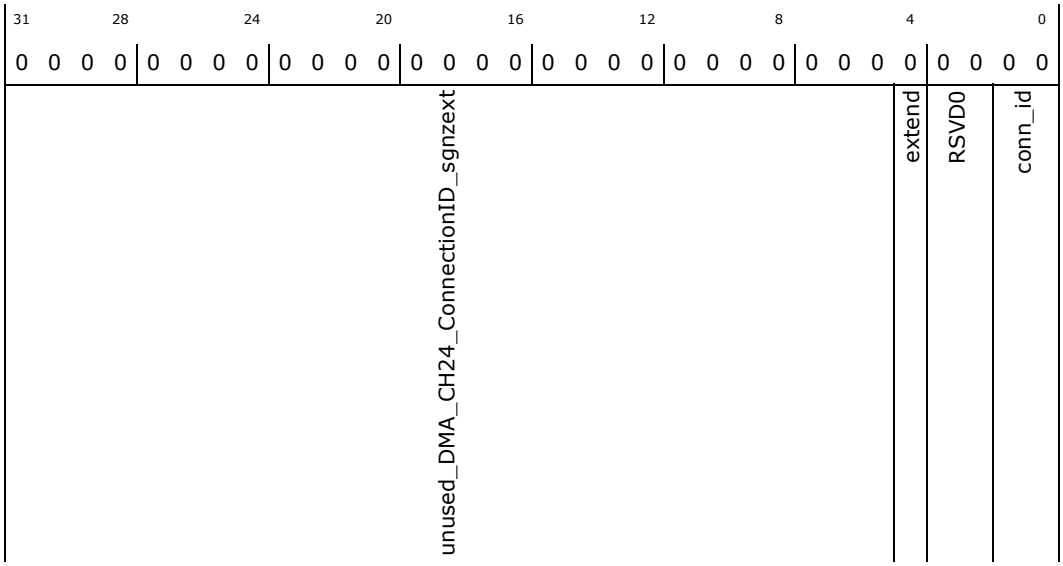
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41060h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH24_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.272 DMA_CH25_ConnectionID_sgnzext (isp_dma_DMA_CH25_ConnectionID_sgnzext)—Offset 41064h

DMA CH 25 PARAM 0: Connection ID and Zero/Sign extension settings

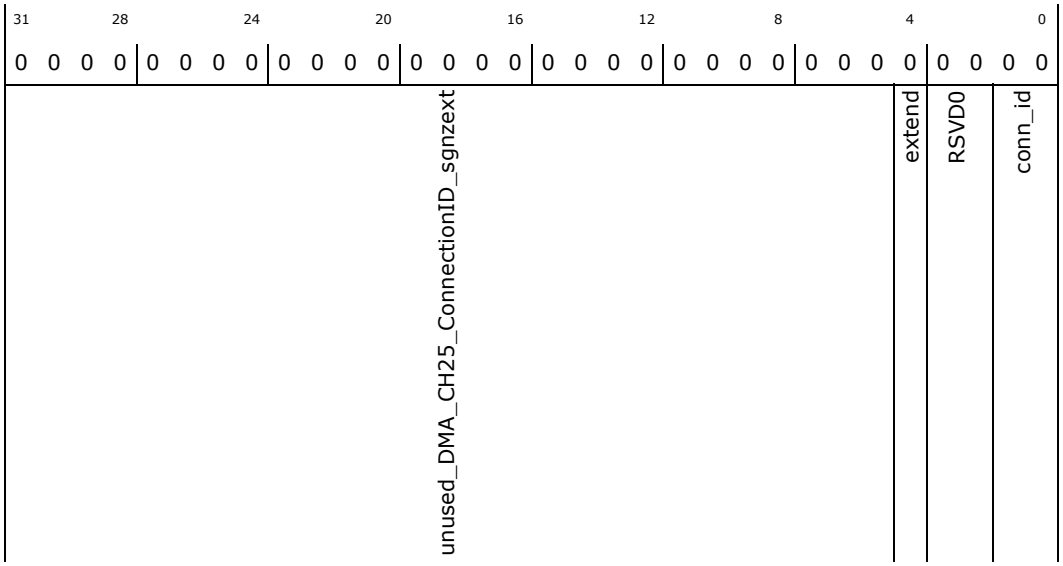
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41064h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH25_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.273 DMA_CH26_ConnectionID_sgnzext (isp_dma_DMA_CH26_ConnectionID_sgnzext)—Offset 41068h

DMA CH 26 PARAM 0: Connection ID and Zero/Sign extension settings

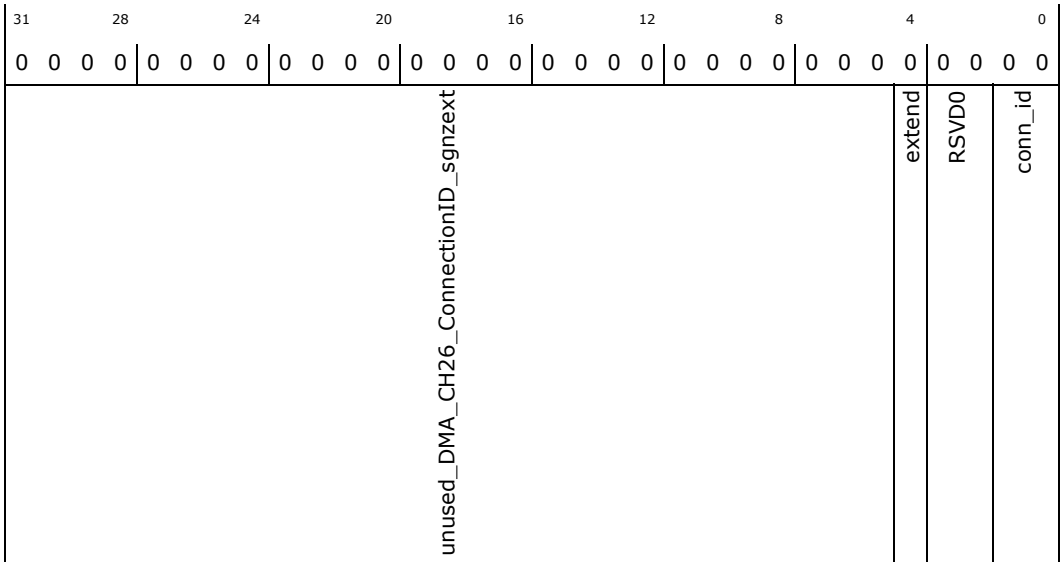
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41068h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH26_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.274 DMA_CH27_ConnectionID_sgnzext (isp_dma_DMA_CH27_ConnectionID_sgnzext)—Offset 4106Ch

DMA CH 27 PARAM 0: Connection ID and Zero/Sign extension settings

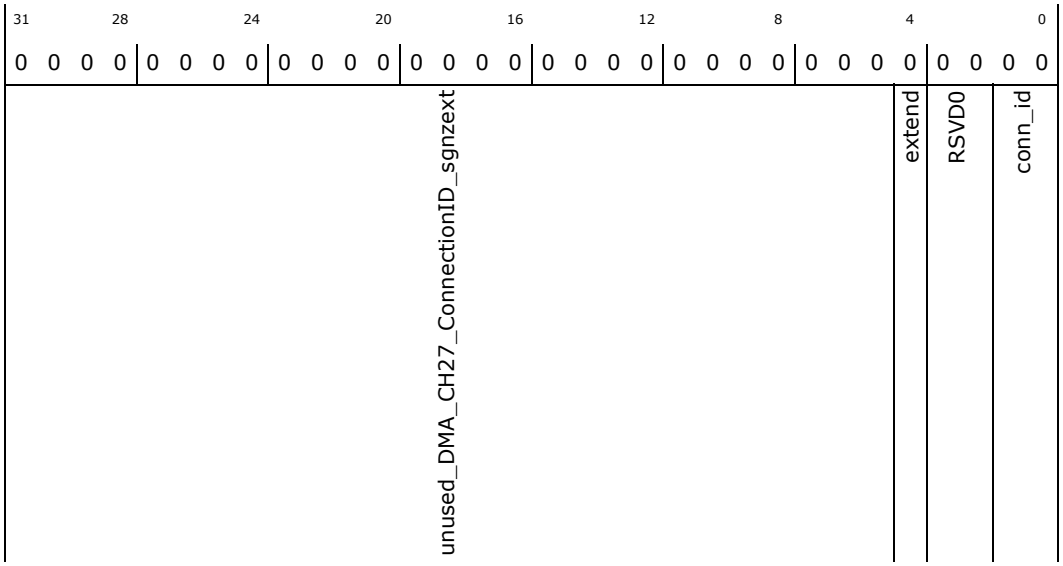
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4106Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH27_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.275 DMA_CH28_ConnectionID_sgnzext (isp_dma_DMA_CH28_ConnectionID_sgnzext)—Offset 41070h

DMA CH 28 PARAM 0: Connection ID and Zero/Sign extension settings

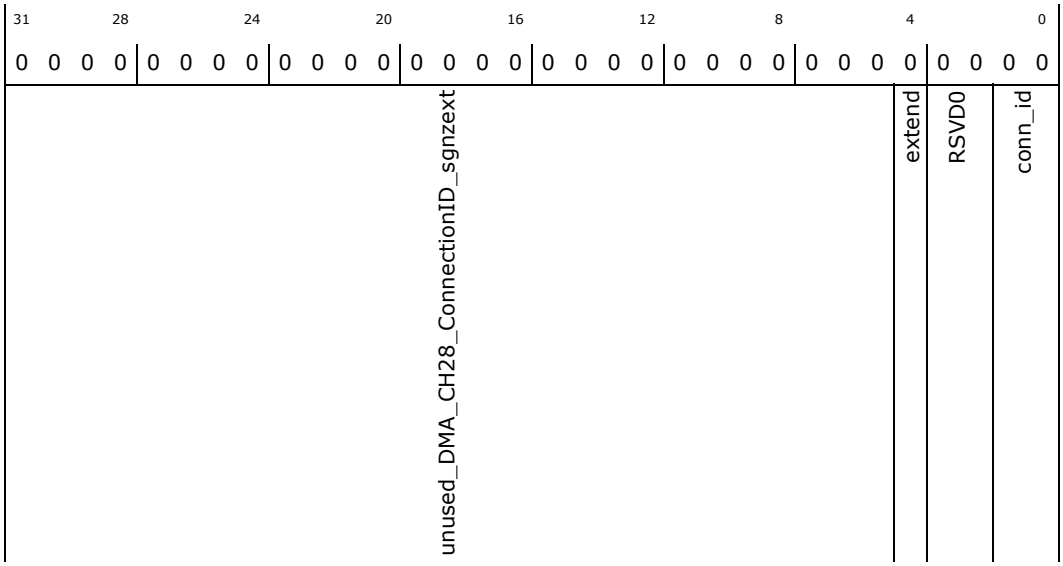
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41070h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH28_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.276 DMA_CH29_ConnectionID_sgnzext (isp_dma_DMA_CH29_ConnectionID_sgnzext)—Offset 41074h

DMA CH 29 PARAM 0: Connection ID and Zero/Sign extension settings

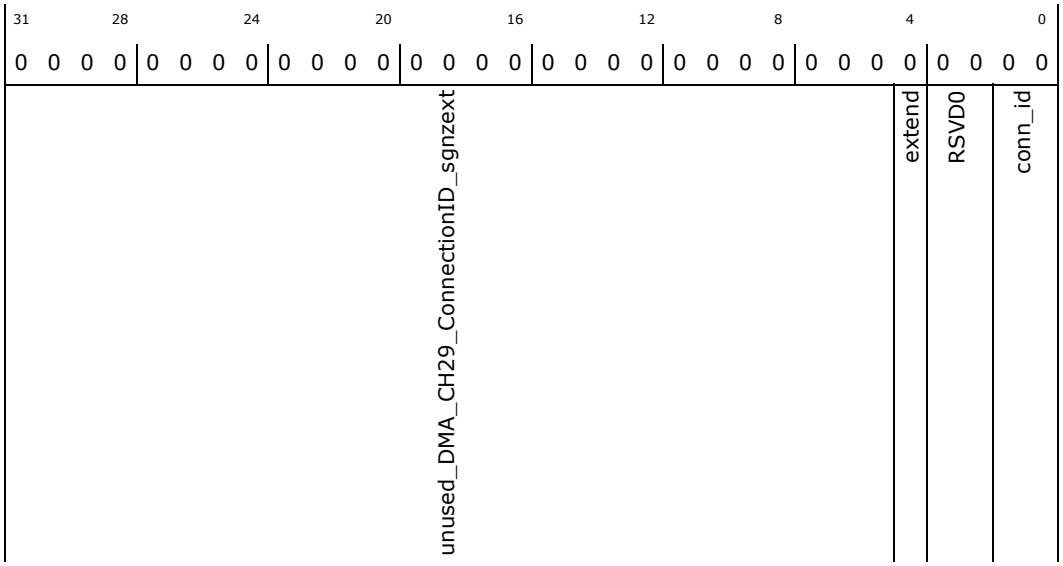
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41074h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH29_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.277 DMA_CH30_ConnectionID_sgnzext (isp_dma_DMA_CH30_ConnectionID_sgnzext)—Offset 41078h

DMA CH 30 PARAM 0: Connection ID and Zero/Sign extension settings

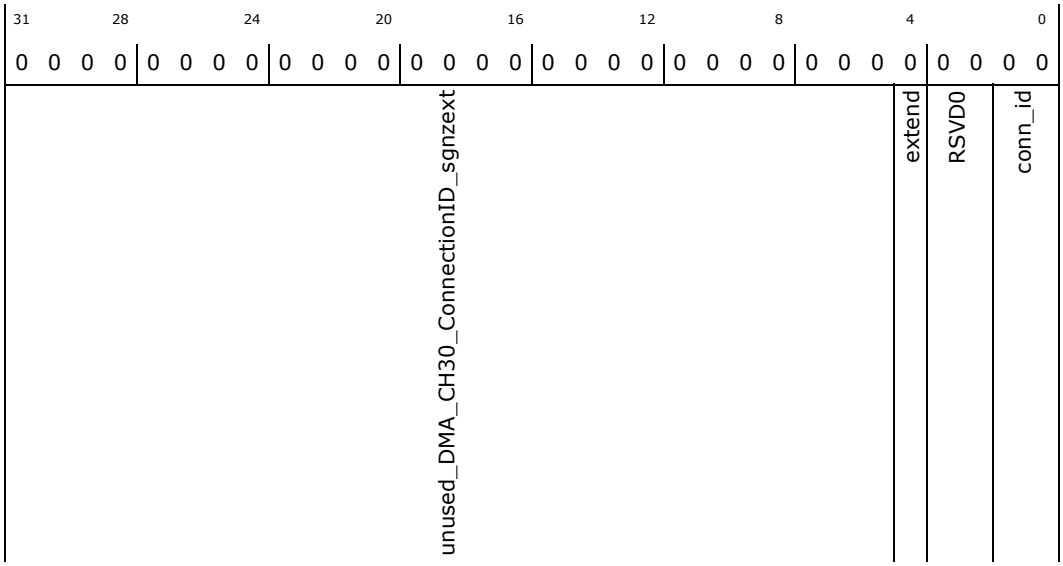
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41078h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH30_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.278 DMA_CH31_ConnectionID_sgnzext (isp_dma_DMA_CH31_ConnectionID_sgnzext)—Offset 4107Ch

DMA CH 31 PARAM 0: Connection ID and Zero/Sign extension settings

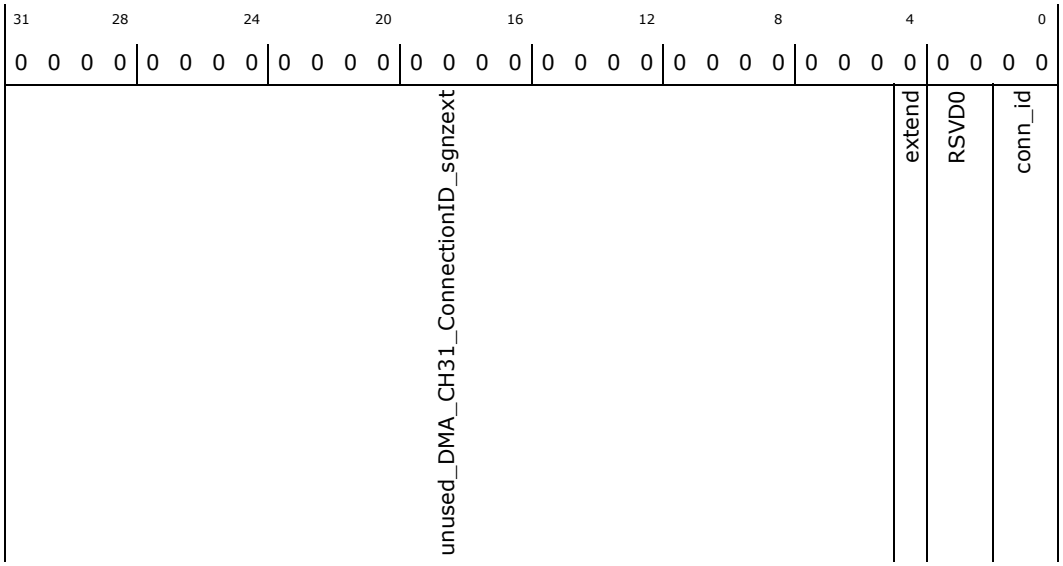
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4107Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH31_ConnectionID_sgnzext):** Unused
4	0x0 RO	**extend:** Zero(0)/Sign(1) extension
3:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RO	**conn_id:** Connection ID

5.2.279 DMA_CH0_Stride_Addr_Space_A (isp_dma_DMA_CH0_Stride_Addr_Space_A)—Offset 41100h

DMA CH 0 PARAM 1: Line Stride for Device A side of the connection.

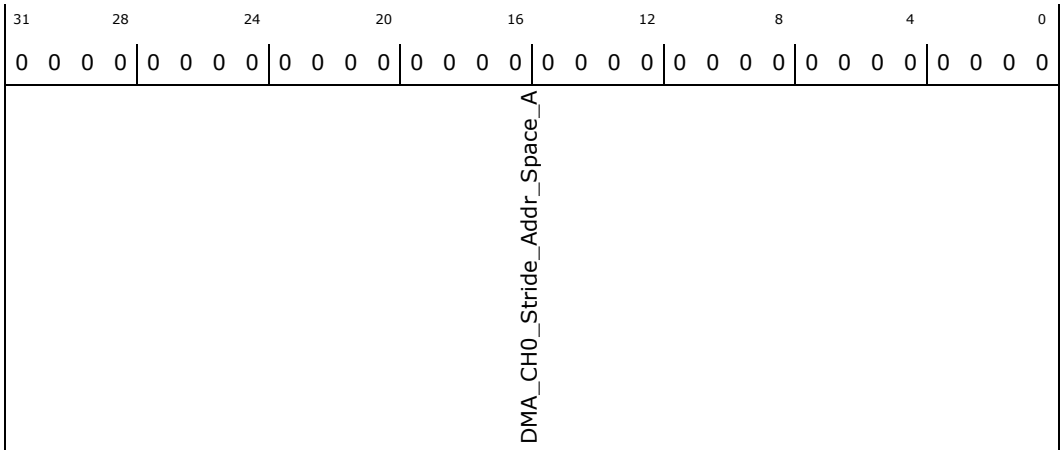
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH0_Stride_Addr_Space_A:** DMA CH 0 PARAM 1: Line Stride for Device A side of the connection.

5.2.280 DMA_CH1_Stride_Addr_Space_A (isp_dma_DMA_CH1_Stride_Addr_Space_A)—Offset 41104h

DMA CH 1 PARAM 1: Line Stride for Device A side of the connection.

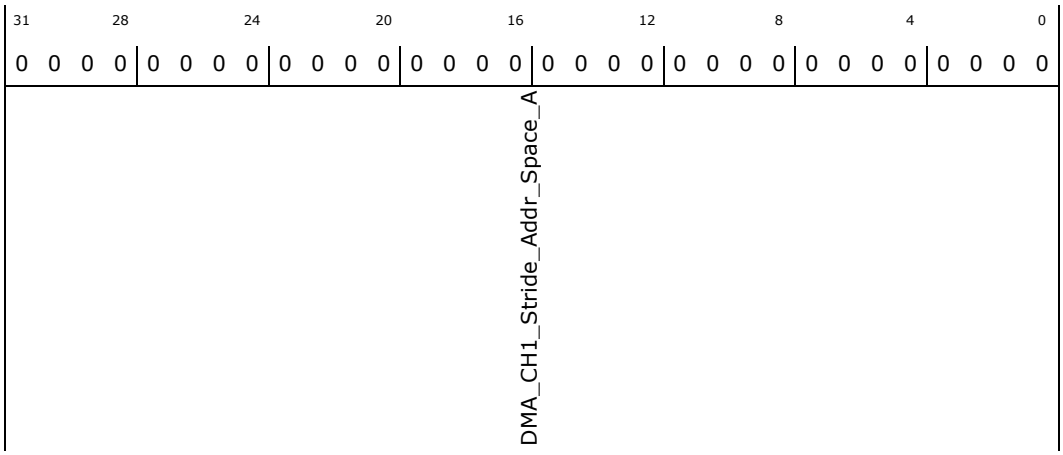
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41104h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH1_Stride_Addr_Space_A:** DMA CH 1 PARAM 1: Line Stride for Device A side of the connection.

5.2.281 DMA_CH2_Stride_Addr_Space_A (isp_dma_DMA_CH2_Stride_Addr_Space_A)—Offset 41108h

DMA CH 2 PARAM 1: Line Stride for Device A side of the connection.

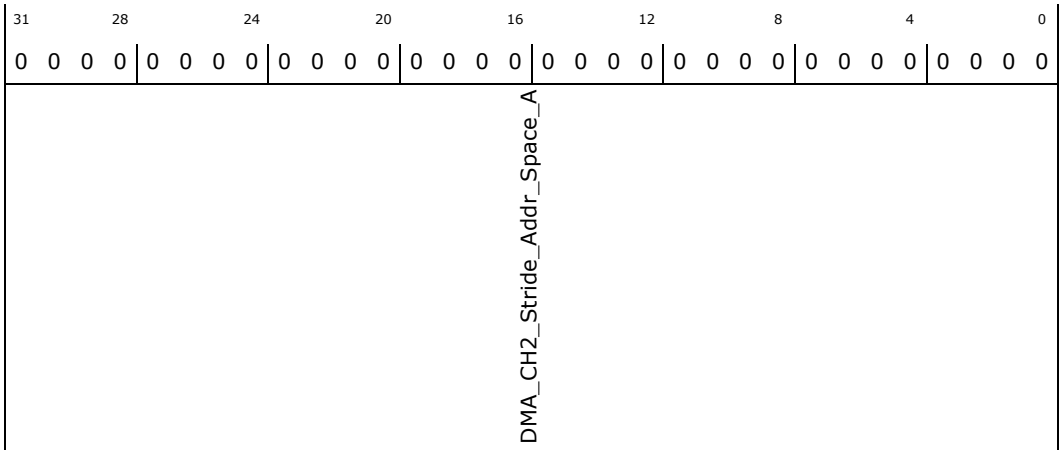
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41108h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH2_Stride_Addr_Space_A:** DMA CH 2 PARAM 1: Line Stride for Device A side of the connection.

5.2.282 DMA_CH3_Stride_Addr_Space_A (isp_dma_DMA_CH3_Stride_Addr_Space_A)—Offset 4110Ch

DMA CH 3 PARAM 1: Line Stride for Device A side of the connection.

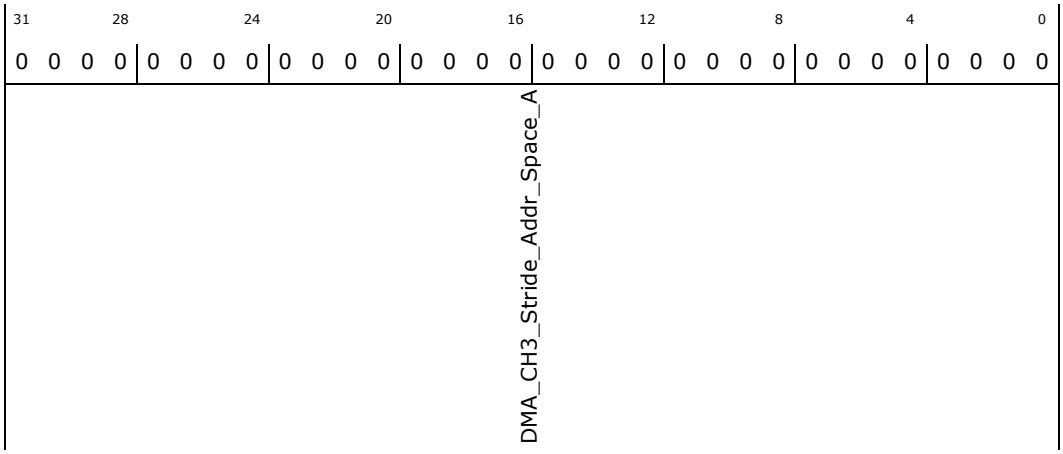
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4110Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH3_Stride_Addr_Space_A:** DMA CH 3 PARAM 1: Line Stride for Device A side of the connection.

5.2.283 DMA_CH4_Stride_Addr_Space_A (isp_dma_DMA_CH4_Stride_Addr_Space_A)—Offset 41110h

DMA CH 4 PARAM 1: Line Stride for Device A side of the connection.

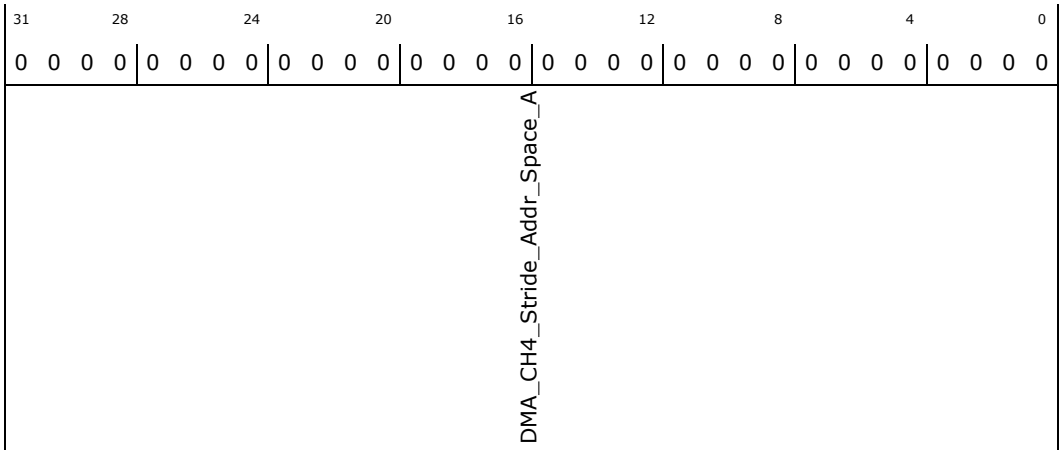
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41110h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH4_Stride_Addr_Space_A:** DMA CH 4 PARAM 1: Line Stride for Device A side of the connection.

5.2.284 DMA_CH5_Stride_Addr_Space_A (isp_dma_DMA_CH5_Stride_Addr_Space_A)—Offset 41114h

DMA CH 5 PARAM 1: Line Stride for Device A side of the connection.

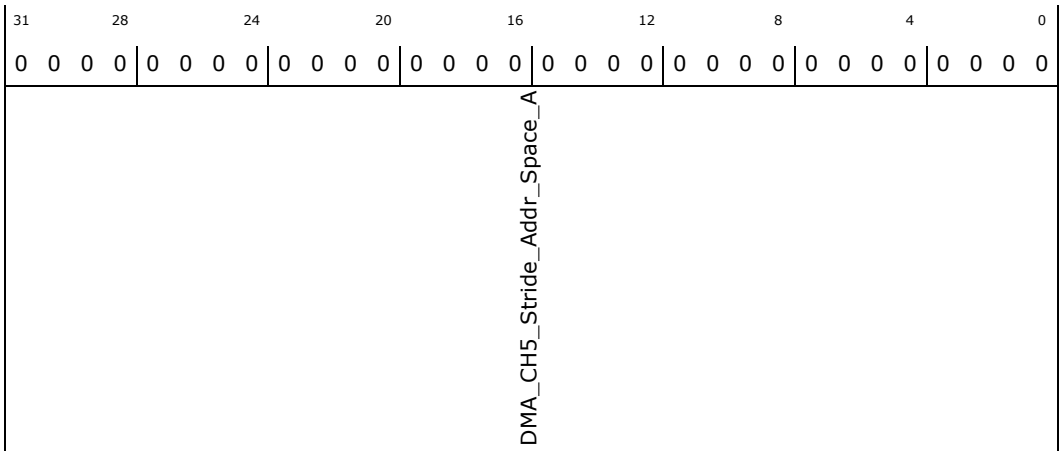
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41114h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH5_Stride_Addr_Space_A:** DMA CH 5 PARAM 1: Line Stride for Device A side of the connection.

5.2.285 DMA_CH6_Stride_Addr_Space_A (isp_dma_DMA_CH6_Stride_Addr_Space_A)—Offset 41118h

DMA CH 6 PARAM 1: Line Stride for Device A side of the connection.

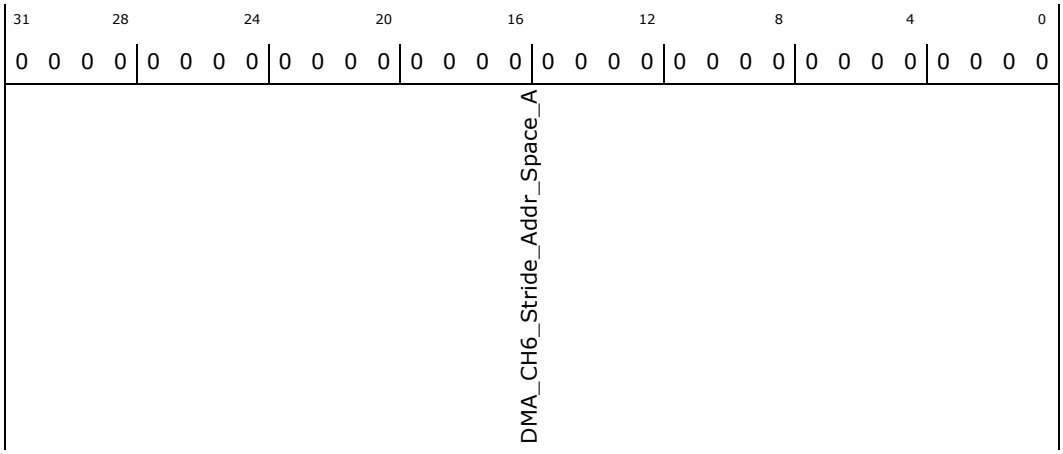
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41118h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH6_Stride_Addr_Space_A:** DMA CH 6 PARAM 1: Line Stride for Device A side of the connection.

5.2.286 DMA_CH7_Stride_Addr_Space_A (isp_dma_DMA_CH7_Stride_Addr_Space_A)—Offset 4111Ch

DMA CH 7 PARAM 1: Line Stride for Device A side of the connection.

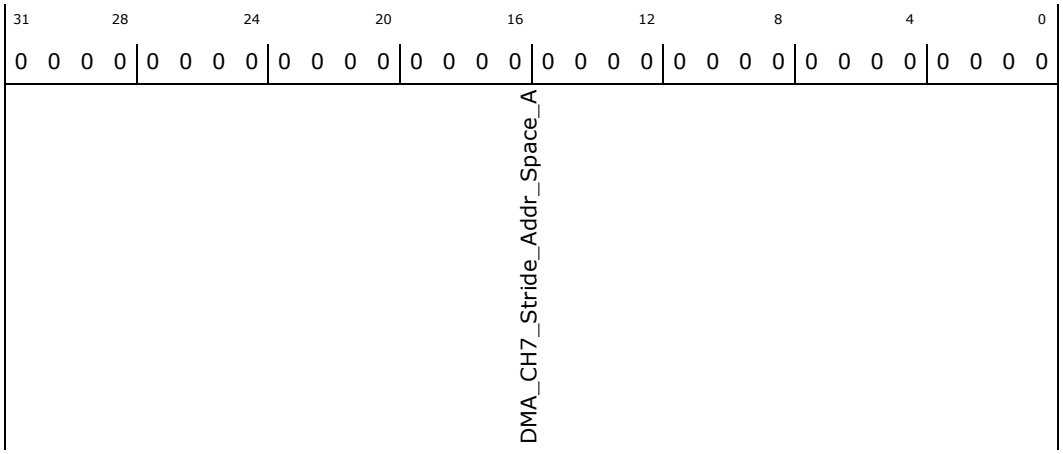
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4111Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH7_Stride_Addr_Space_A:** DMA CH 7 PARAM 1: Line Stride for Device A side of the connection.

5.2.287 DMA_CH8_Stride_Addr_Space_A (isp_dma_DMA_CH8_Stride_Addr_Space_A)—Offset 41120h

DMA CH 8 PARAM 1: Line Stride for Device A side of the connection.

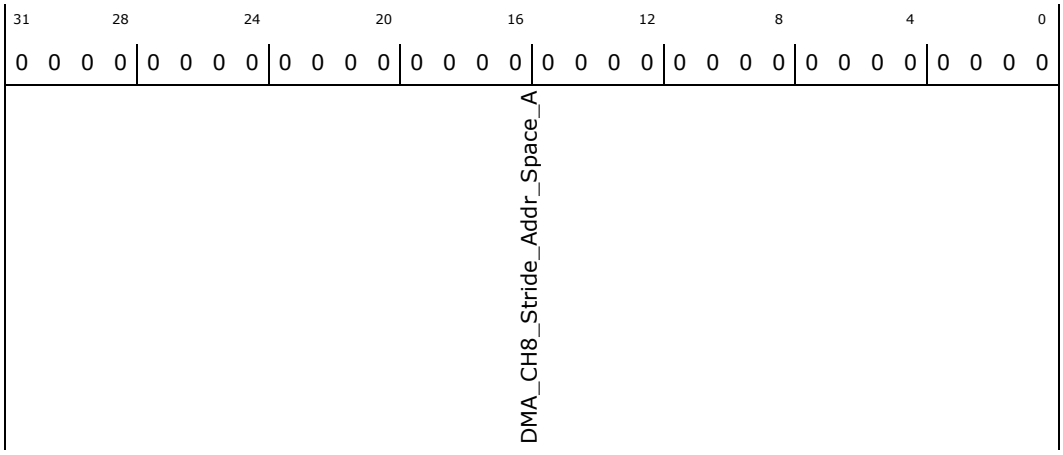
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41120h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH8_Stride_Addr_Space_A:** DMA CH 8 PARAM 1: Line Stride for Device A side of the connection.

5.2.288 DMA_CH9_Stride_Addr_Space_A (isp_dma_DMA_CH9_Stride_Addr_Space_A)—Offset 41124h

DMA CH 9 PARAM 1: Line Stride for Device A side of the connection.

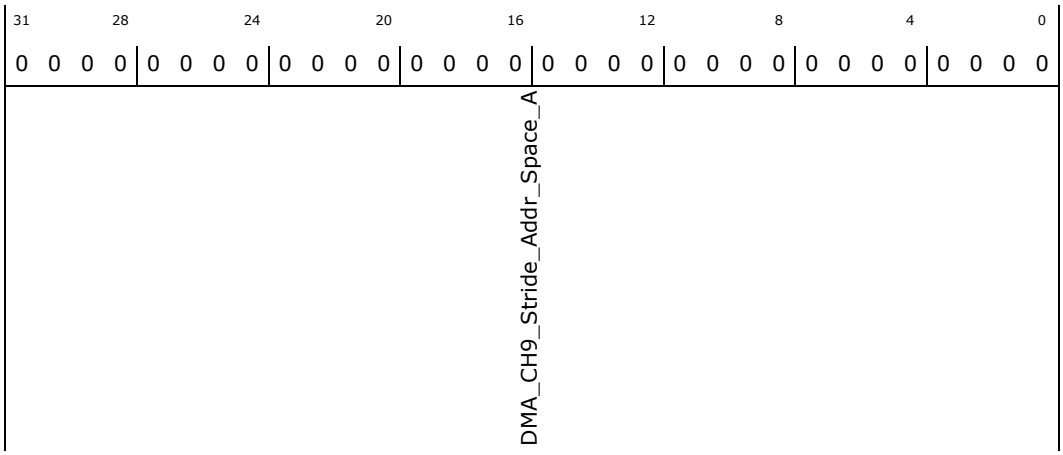
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41124h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH9_Stride_Addr_Space_A:** DMA CH 9 PARAM 1: Line Stride for Device A side of the connection.

5.2.289 DMA_CH10_Stride_Addr_Space_A (isp_dma_DMA_CH10_Stride_Addr_Space_A)—Offset 41128h

DMA CH 10 PARAM 1: Line Stride for Device A side of the connection.

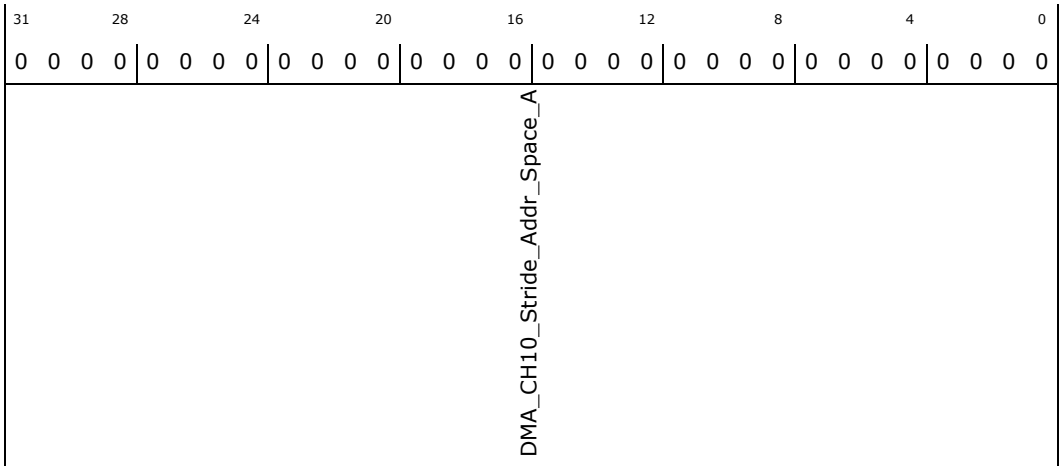
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41128h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH10_Stride_Addr_Space_A:** DMA CH 10 PARAM 1: Line Stride for Device A side of the connection.

5.2.290 DMA_CH11_Stride_Addr_Space_A (isp_dma_DMA_CH11_Stride_Addr_Space_A)—Offset 4112Ch

DMA CH 11 PARAM 1: Line Stride for Device A side of the connection.

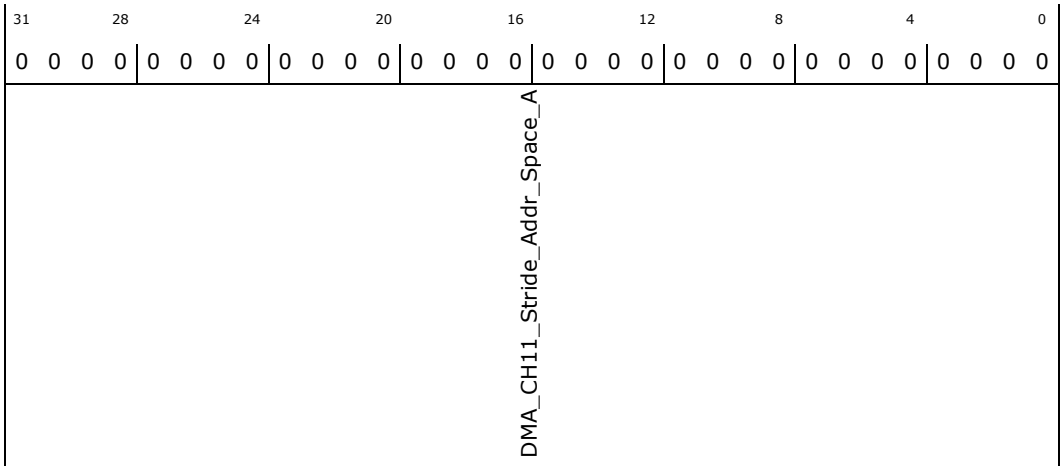
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4112Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH11_Stride_Addr_Space_A:** DMA CH 11 PARAM 1: Line Stride for Device A side of the connection.

5.2.291 DMA_CH12_Stride_Addr_Space_A (isp_dma_DMA_CH12_Stride_Addr_Space_A)—Offset 41130h

DMA CH 12 PARAM 1: Line Stride for Device A side of the connection.

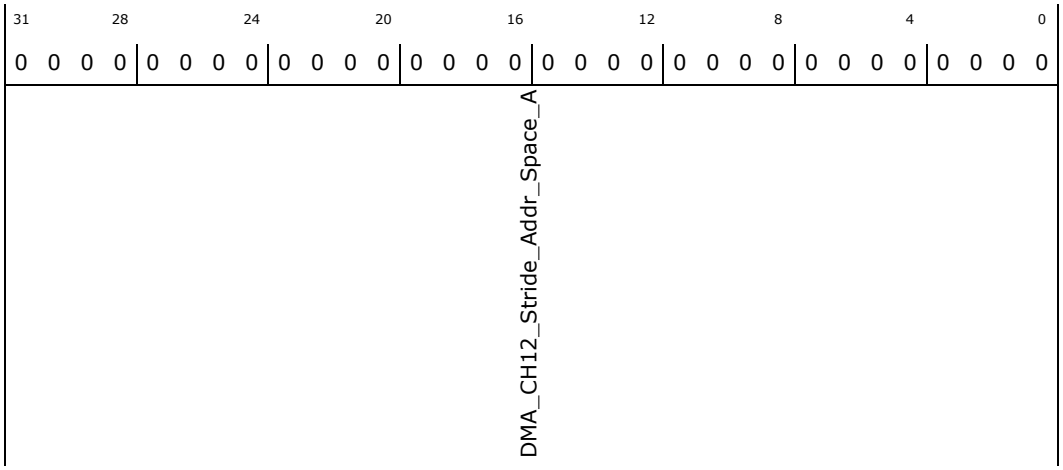
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41130h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH12_Stride_Addr_Space_A:** DMA CH 12 PARAM 1: Line Stride for Device A side of the connection.

5.2.292 DMA_CH13_Stride_Addr_Space_A (isp_dma_DMA_CH13_Stride_Addr_Space_A)—Offset 41134h

DMA CH 13 PARAM 1: Line Stride for Device A side of the connection.

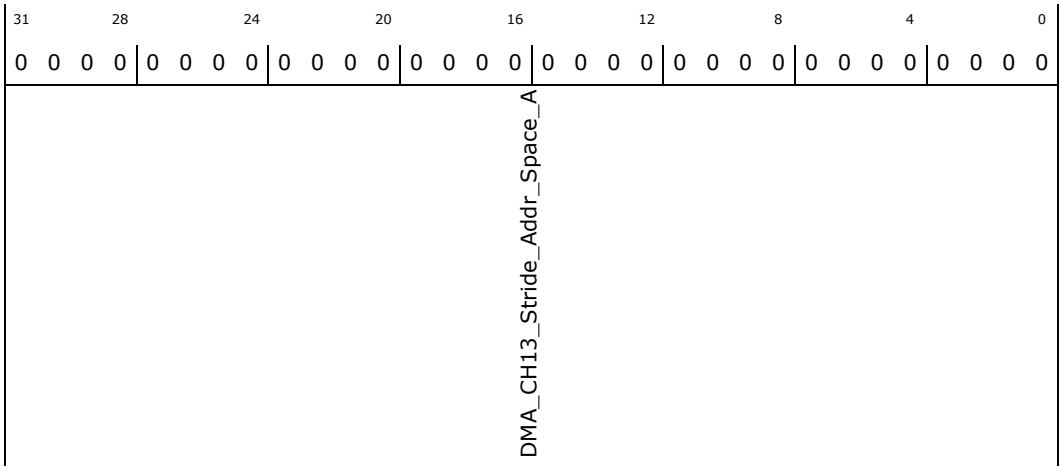
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41134h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH13_Stride_Addr_Space_A:** DMA CH 13 PARAM 1: Line Stride for Device A side of the connection.

5.2.293 DMA_CH14_Stride_Addr_Space_A (isp_dma_DMA_CH14_Stride_Addr_Space_A)—Offset 41138h

DMA CH 14 PARAM 1: Line Stride for Device A side of the connection.

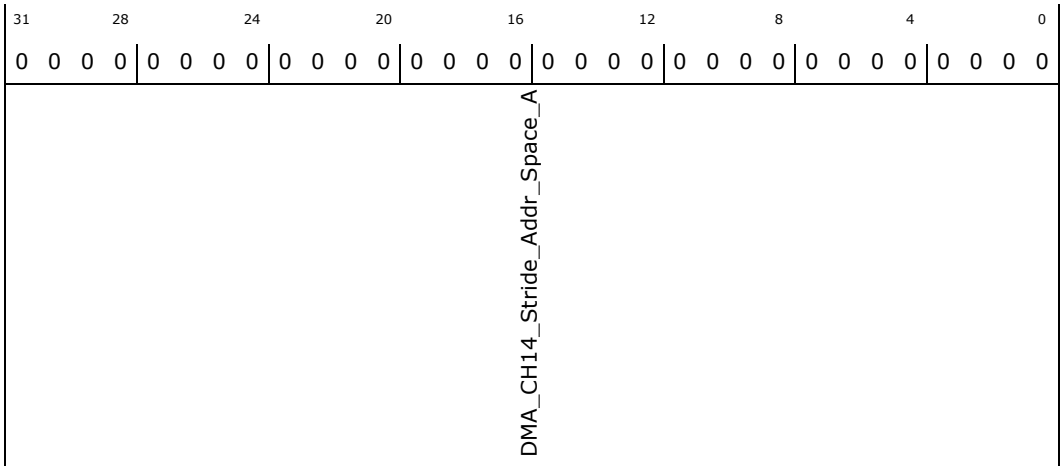
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41138h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH14_Stride_Addr_Space_A:** DMA CH 14 PARAM 1: Line Stride for Device A side of the connection.

5.2.294 DMA_CH15_Stride_Addr_Space_A (isp_dma_DMA_CH15_Stride_Addr_Space_A)—Offset 4113Ch

DMA CH 15 PARAM 1: Line Stride for Device A side of the connection.

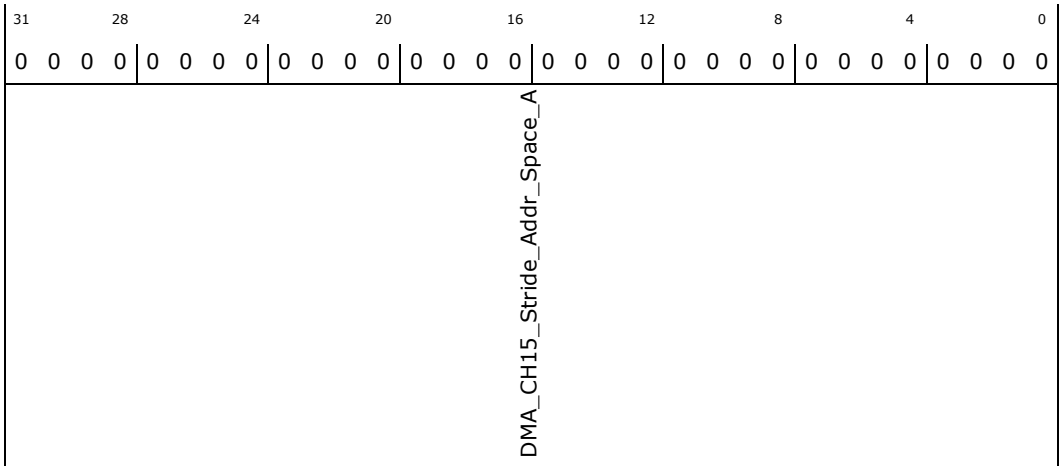
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4113Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH15_Stride_Addr_Space_A:** DMA CH 15 PARAM 1: Line Stride for Device A side of the connection.

5.2.295 DMA_CH16_Stride_Addr_Space_A (isp_dma_DMA_CH16_Stride_Addr_Space_A)—Offset 41140h

DMA CH 16 PARAM 1: Line Stride for Device A side of the connection.

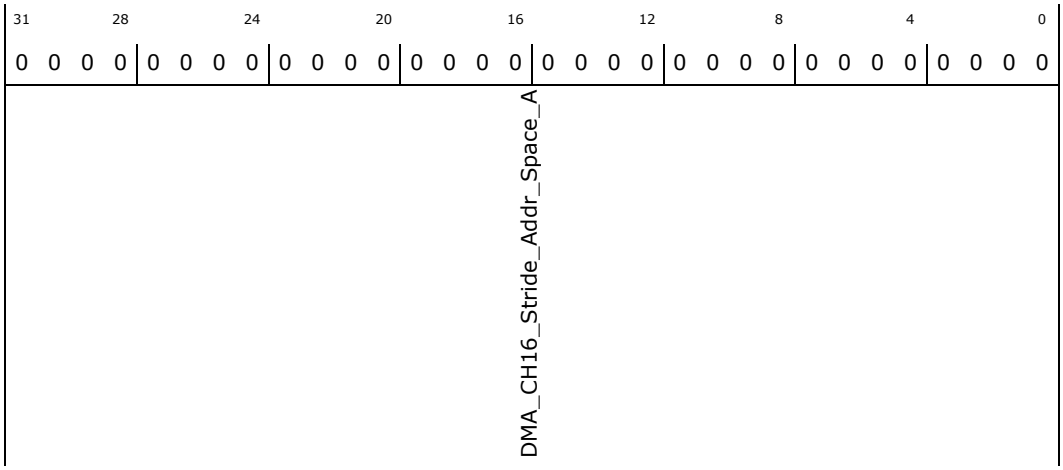
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41140h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH16_Stride_Addr_Space_A:** DMA CH 16 PARAM 1: Line Stride for Device A side of the connection.

5.2.296 DMA_CH17_Stride_Addr_Space_A (isp_dma_DMA_CH17_Stride_Addr_Space_A)—Offset 41144h

DMA CH 17 PARAM 1: Line Stride for Device A side of the connection.

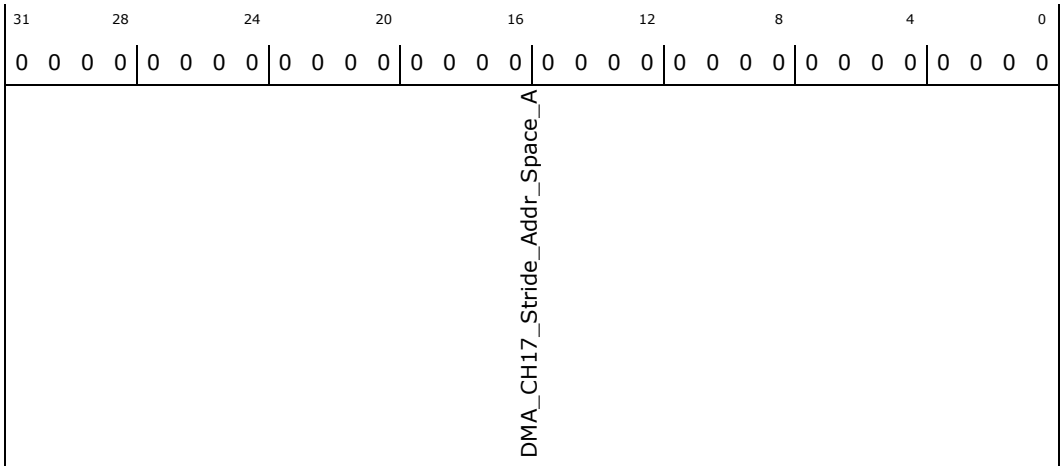
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41144h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH17_Stride_Addr_Space_A:** DMA CH 17 PARAM 1: Line Stride for Device A side of the connection.

5.2.297 DMA_CH18_Stride_Addr_Space_A (isp_dma_DMA_CH18_Stride_Addr_Space_A)—Offset 41148h

DMA CH 18 PARAM 1: Line Stride for Device A side of the connection.

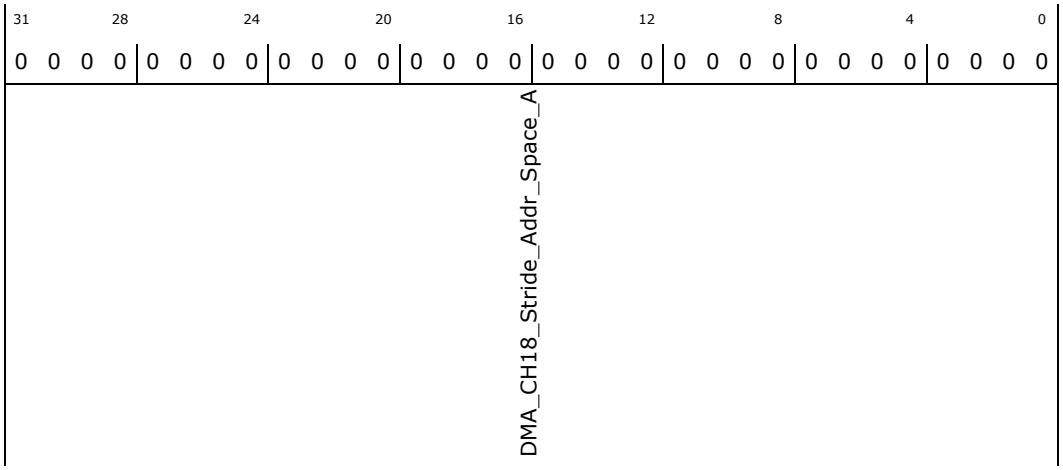
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41148h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH18_Stride_Addr_Space_A:** DMA CH 18 PARAM 1: Line Stride for Device A side of the connection.

5.2.298 DMA_CH19_Stride_Addr_Space_A (isp_dma_DMA_CH19_Stride_Addr_Space_A)—Offset 4114Ch

DMA CH 19 PARAM 1: Line Stride for Device A side of the connection.

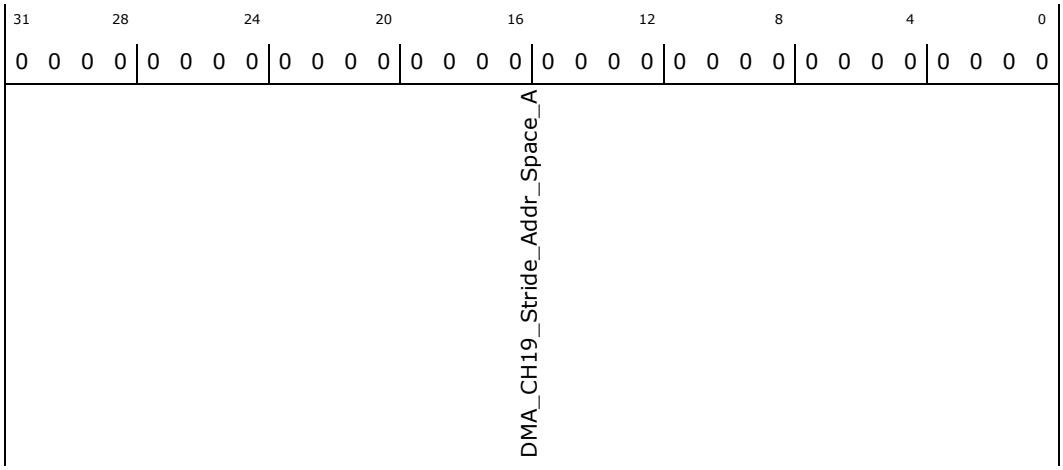
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4114Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH19_Stride_Addr_Space_A:** DMA CH 19 PARAM 1: Line Stride for Device A side of the connection.

5.2.299 DMA_CH20_Stride_Addr_Space_A (isp_dma_DMA_CH20_Stride_Addr_Space_A)—Offset 41150h

DMA CH 20 PARAM 1: Line Stride for Device A side of the connection.

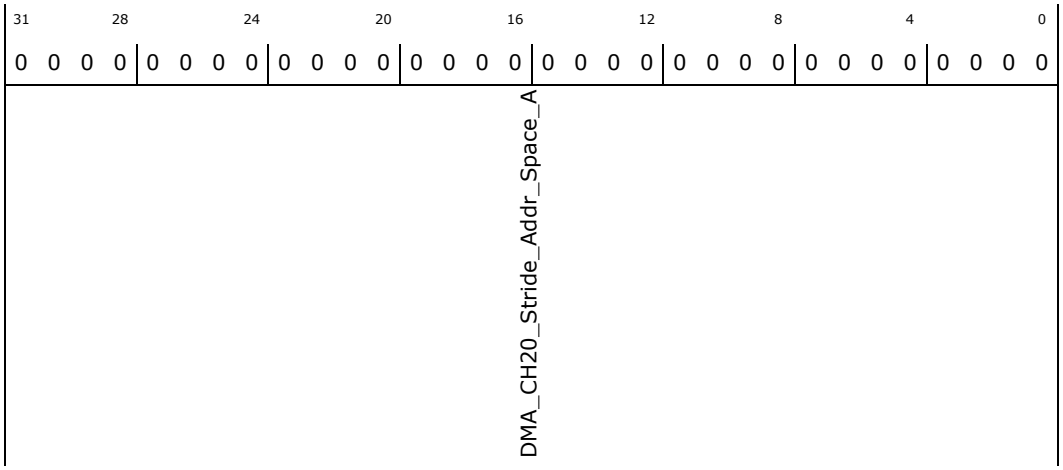
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41150h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH20_Stride_Addr_Space_A:** DMA CH 20 PARAM 1: Line Stride for Device A side of the connection.

5.2.300 DMA_CH21_Stride_Addr_Space_A (isp_dma_DMA_CH21_Stride_Addr_Space_A)—Offset 41154h

DMA CH 21 PARAM 1: Line Stride for Device A side of the connection.

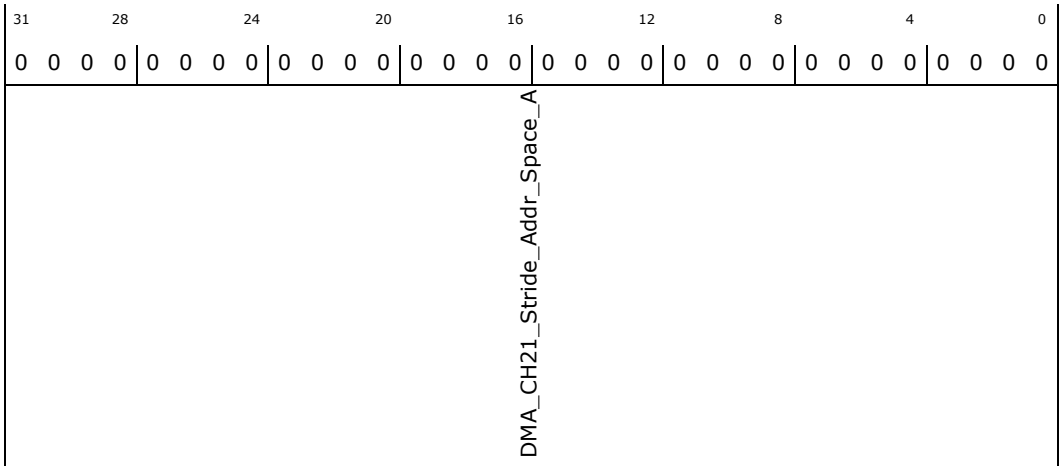
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41154h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH21_Stride_Addr_Space_A:** DMA CH 21 PARAM 1: Line Stride for Device A side of the connection.

5.2.301 DMA_CH0_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH0_Left_Crop_and_Elem_Addr_Space_A)—Offset 41200h

DMA CH 0 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

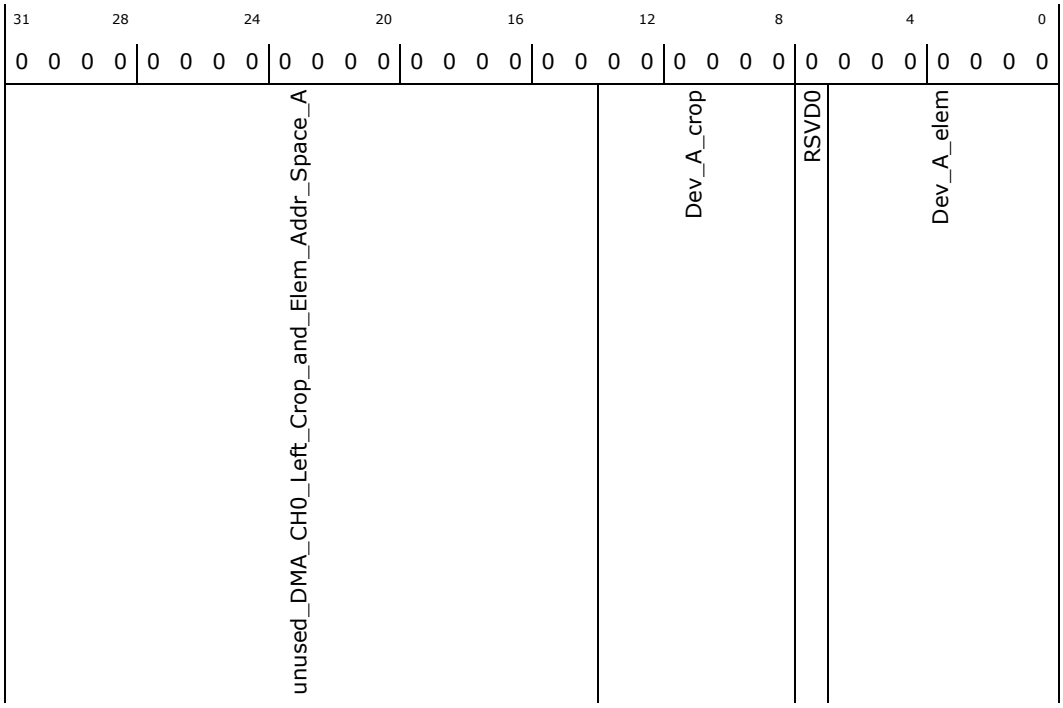
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH0_Left_Crop_and_Elem_Addr_Space_A):** Unused

Bit Range	Default and Access	Field Name (ID): Description
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.302 DMA_CH1_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH1_Left_Crop_and_Elem_Addr_Space_A)—Offset 41204h

DMA CH 1 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

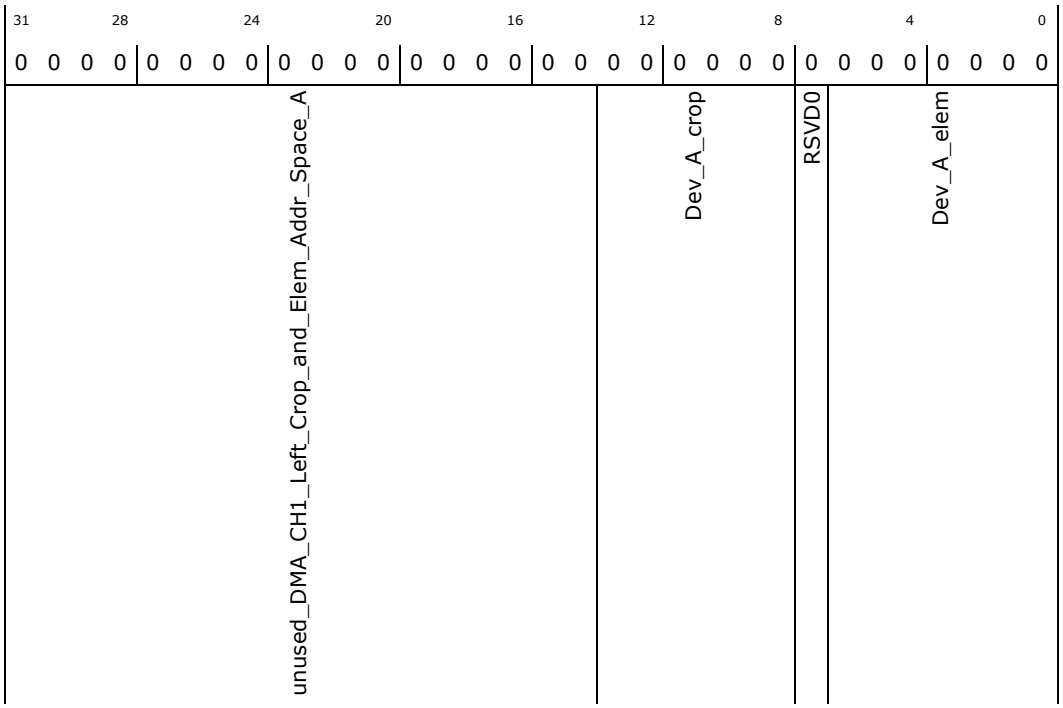
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41204h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH1_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.303 DMA_CH2_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH2_Left_Crop_and_Elem_Addr_Space_A)—Offset 41208h

DMA CH 2 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

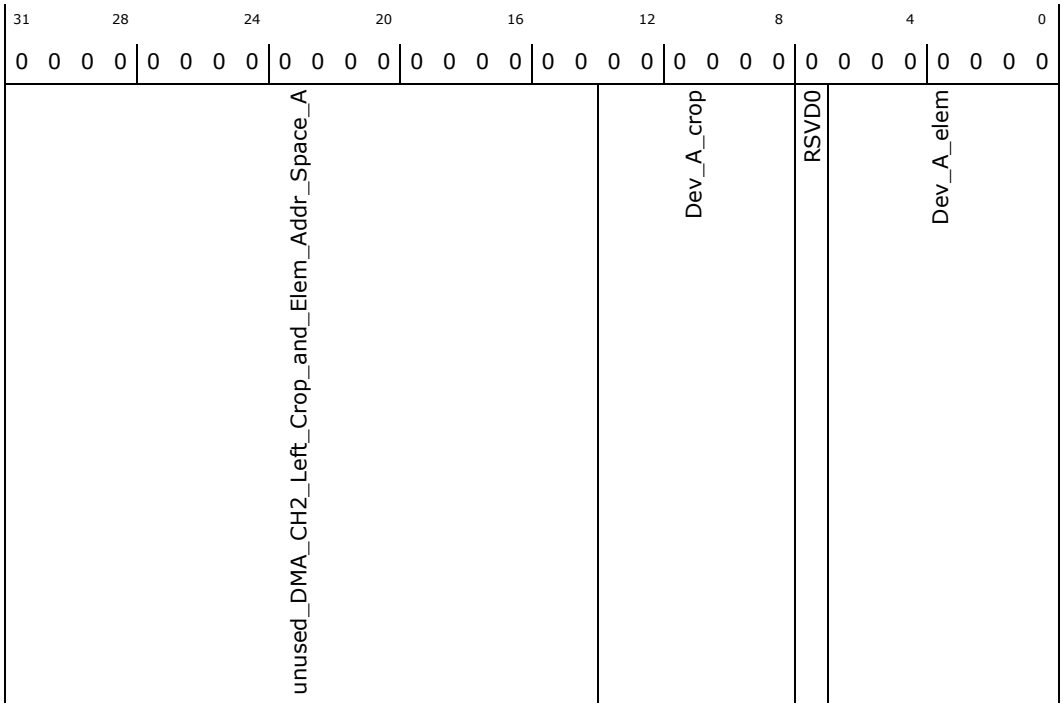
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41208h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH2_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.304 DMA_CH3_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH3_Left_Crop_and_Elem_Addr_Space_A)—Offset 4120Ch

DMA CH 3 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

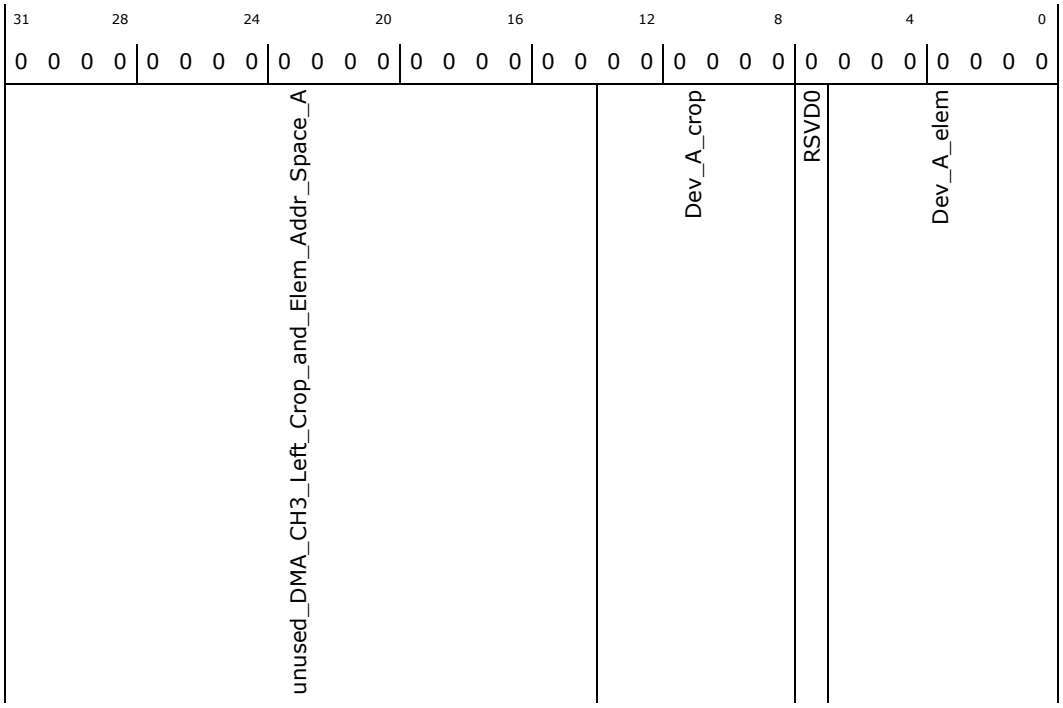
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4120Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH3_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.305 DMA_CH4_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH4_Left_Crop_and_Elem_Addr_Space_A)—Offset 41210h

DMA CH 4 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

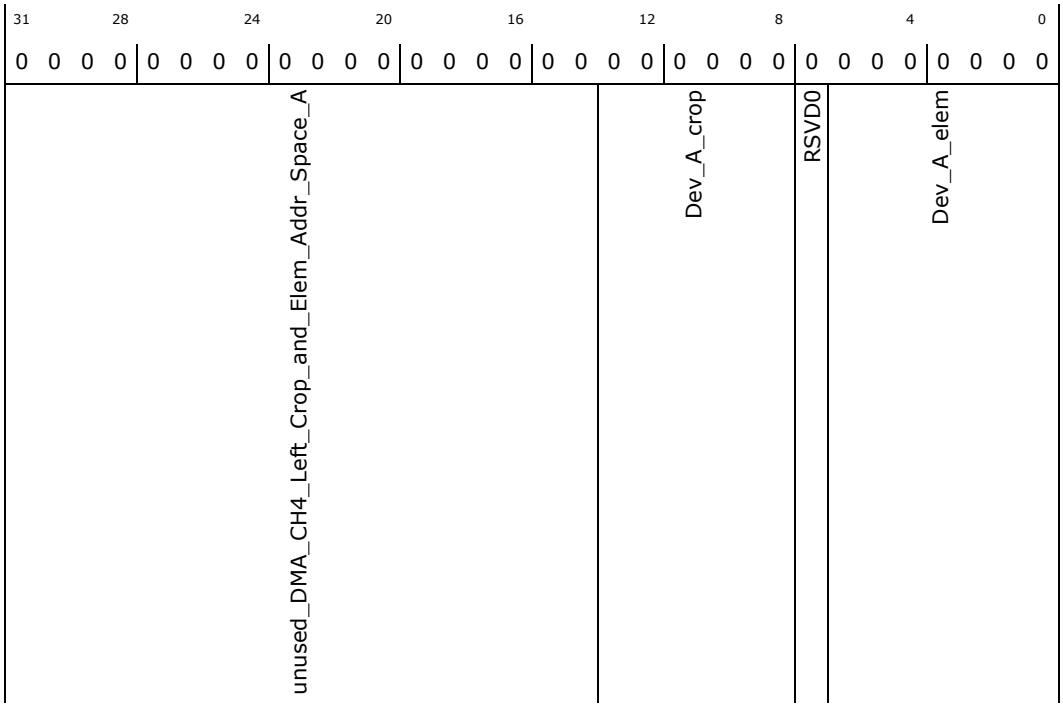
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41210h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH4_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.306 DMA_CH5_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH5_Left_Crop_and_Elem_Addr_Space_A)—Offset 41214h

DMA CH 5 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

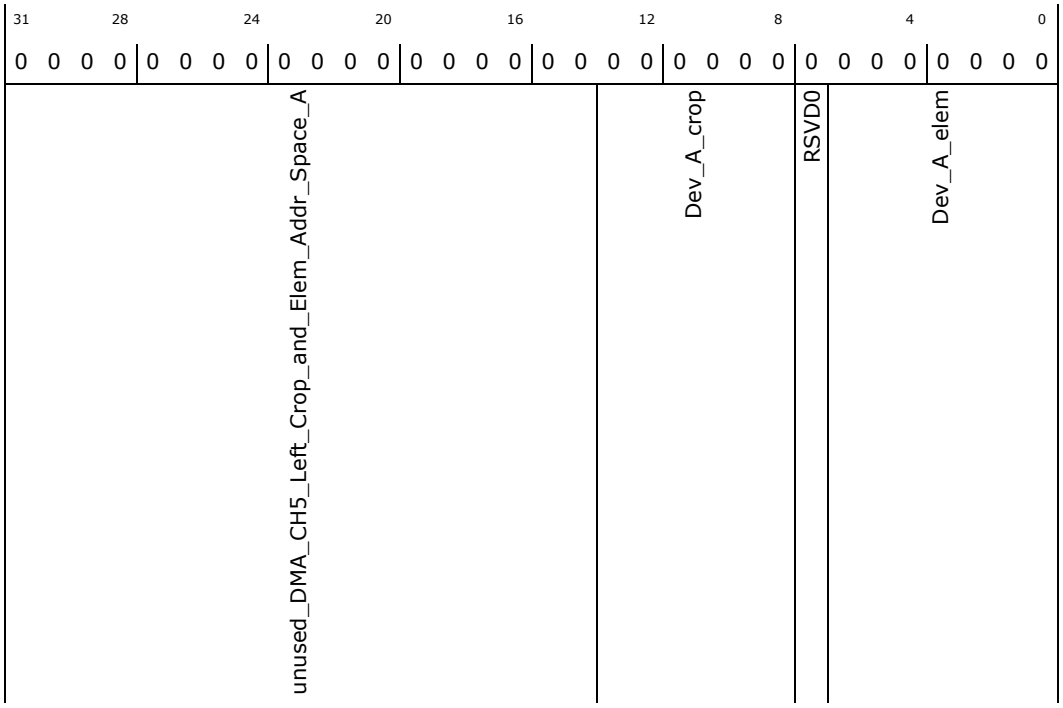
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41214h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH5_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.307 DMA_CH6_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH6_Left_Crop_and_Elem_Addr_Space_A)—Offset 41218h

DMA CH 6 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

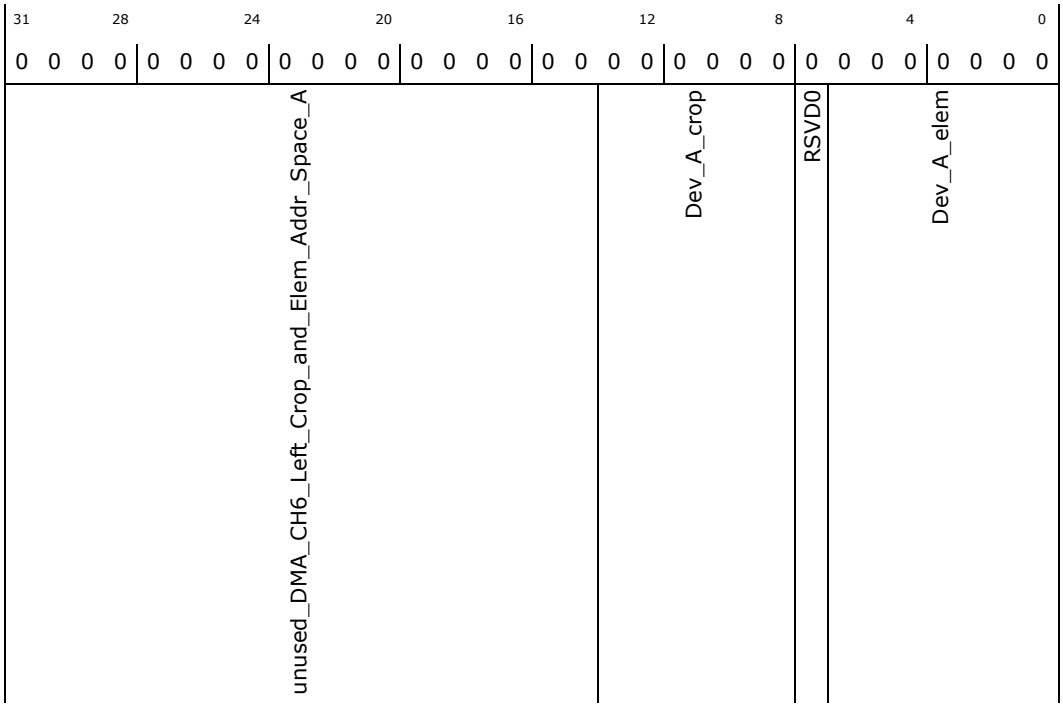
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41218h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH6_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.308 DMA_CH7_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH7_Left_Crop_and_Elem_Addr_Space_A)—Offset 4121Ch

DMA CH 7 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

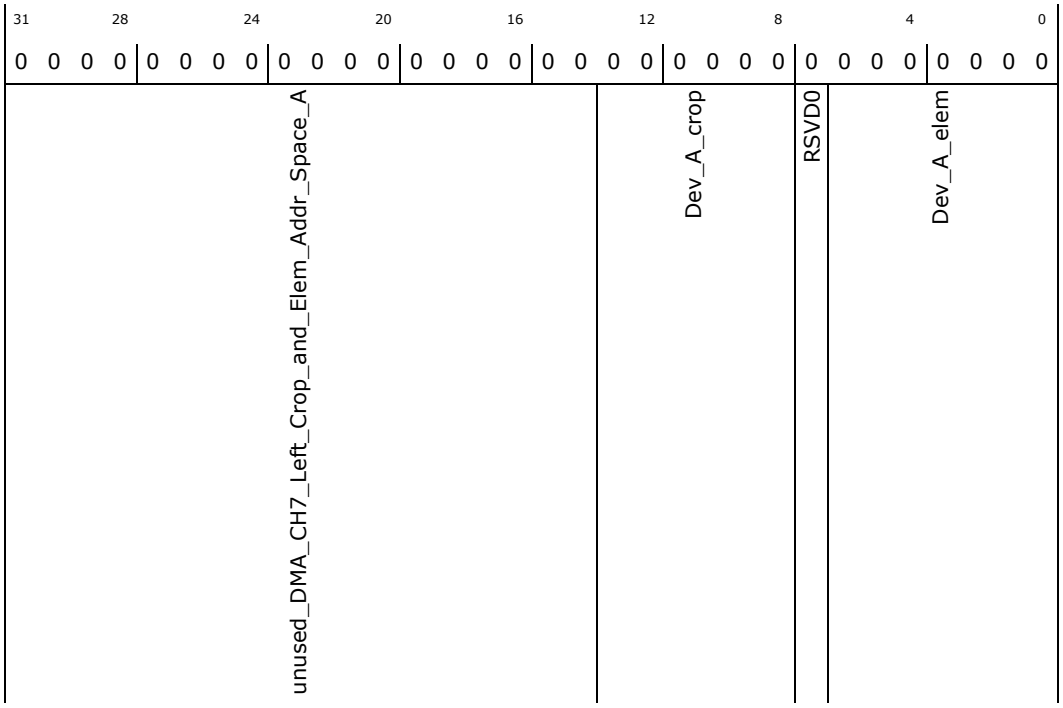
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4121Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH7_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.309 DMA_CH8_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH8_Left_Crop_and_Elem_Addr_Space_A)—Offset 41220h

DMA CH 8 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

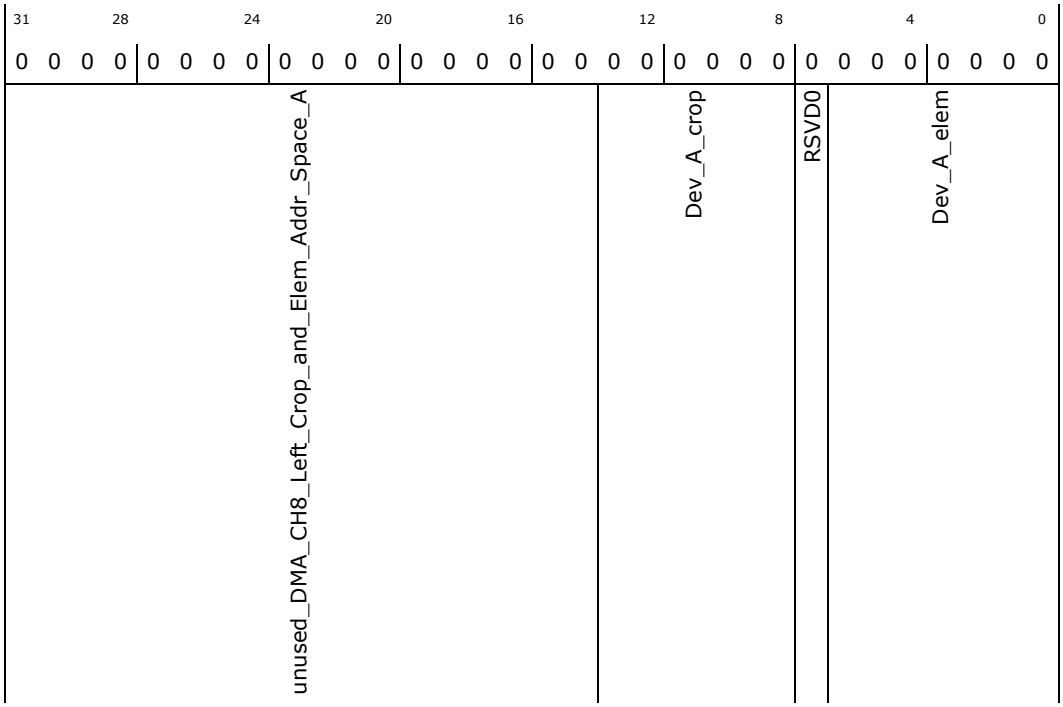
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41220h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH8_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.310 DMA_CH9_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH9_Left_Crop_and_Elem_Addr_Space_A)—Offset 41224h

DMA CH 9 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

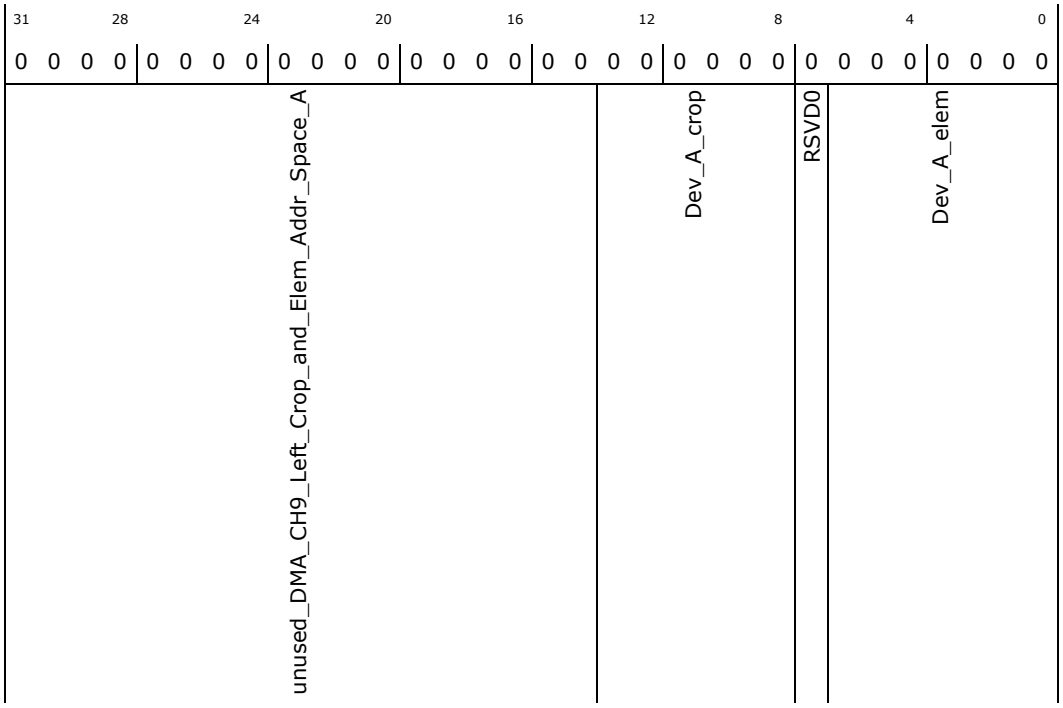
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41224h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH9_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.311 DMA_CH10_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH10_Left_Crop_and_Elem_Addr_Space_A)—Offset 41228h

DMA CH 10 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

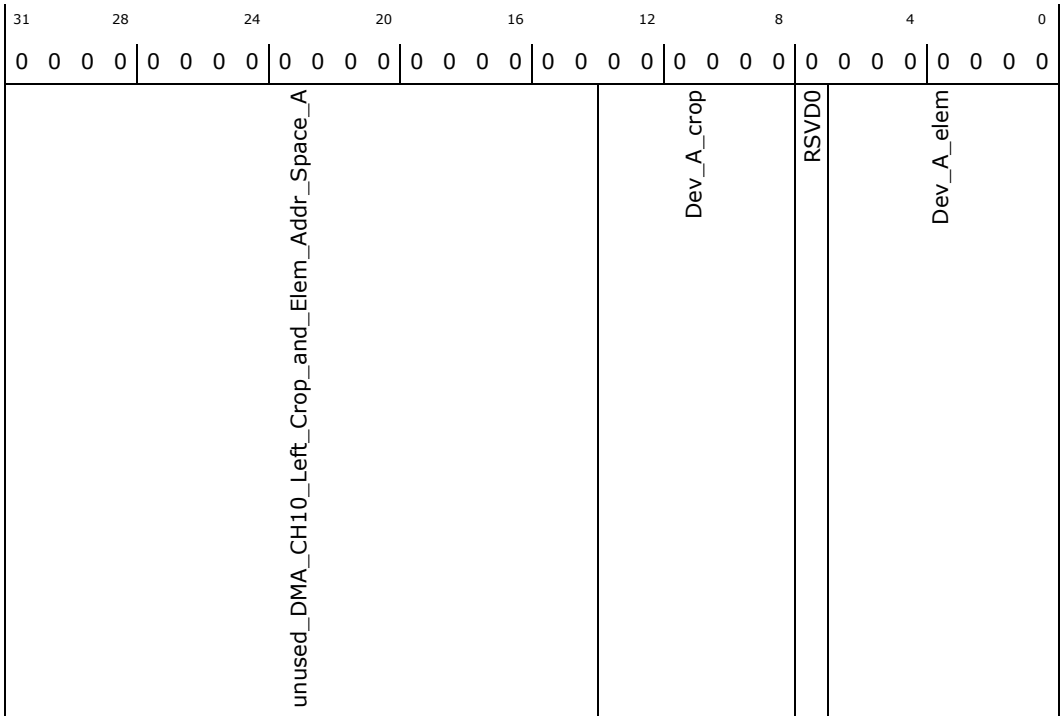
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41228h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH10_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.312 DMA_CH11_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH11_Left_Crop_and_Elem_Addr_Space_A)—Offset 4122Ch

DMA CH 11 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

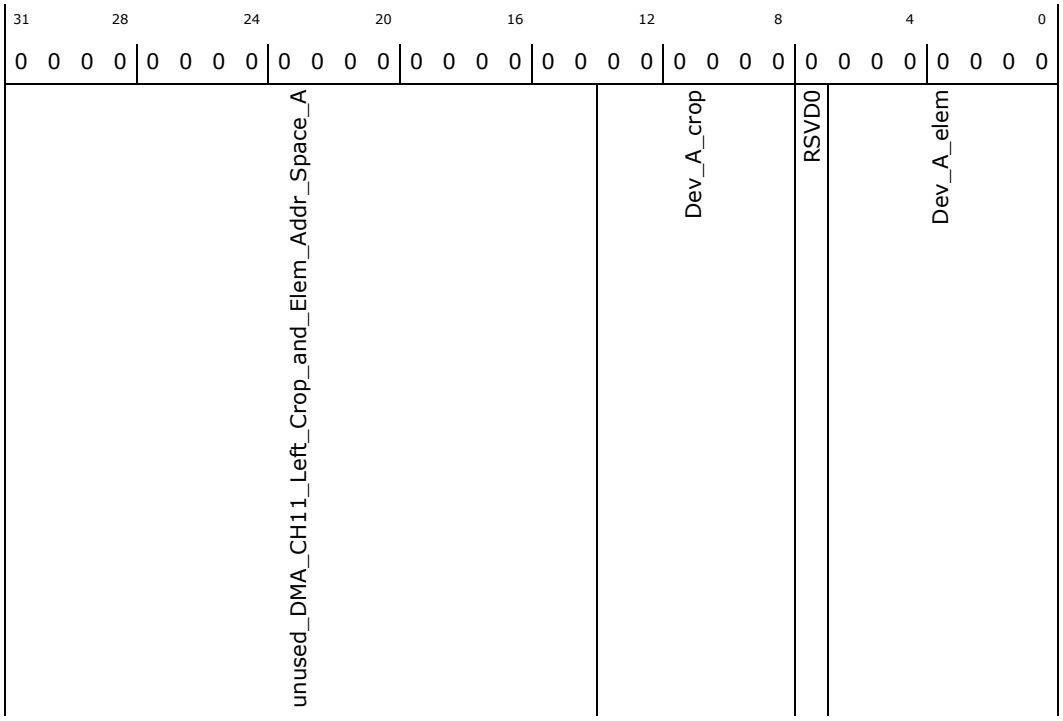
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4122Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH11_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.313 DMA_CH12_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH12_Left_Crop_and_Elem_Addr_Space_A)—Offset 41230h

DMA CH 12 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

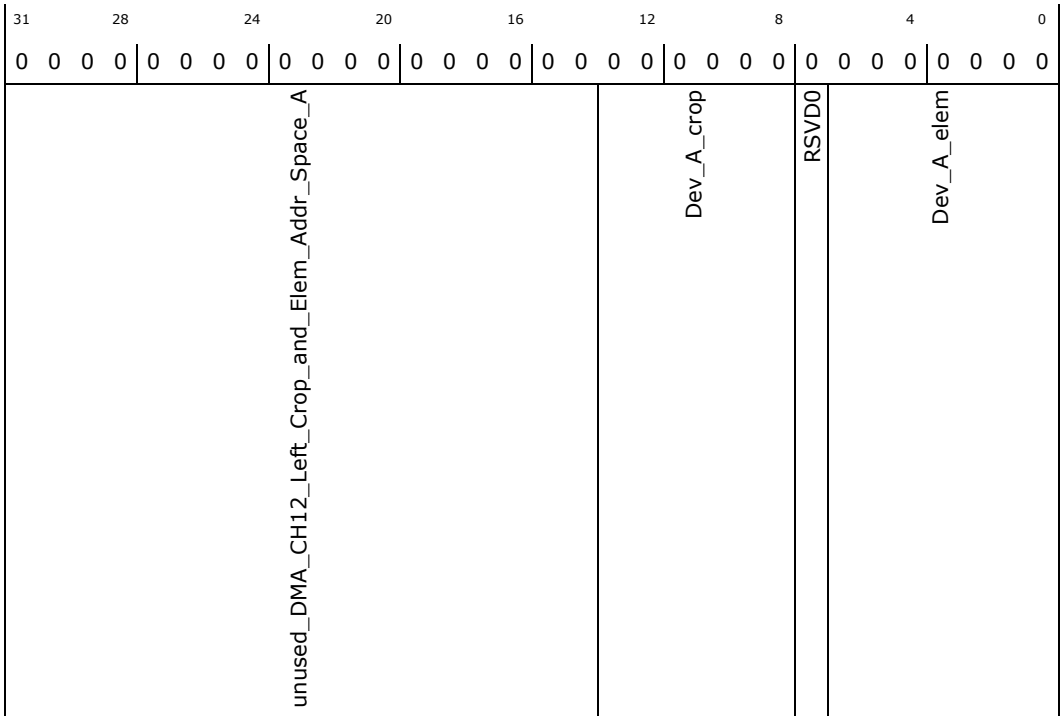
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41230h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH12_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.314 DMA_CH13_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH13_Left_Crop_and_Elem_Addr_Space_A)—Offset 41234h

DMA CH 13 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

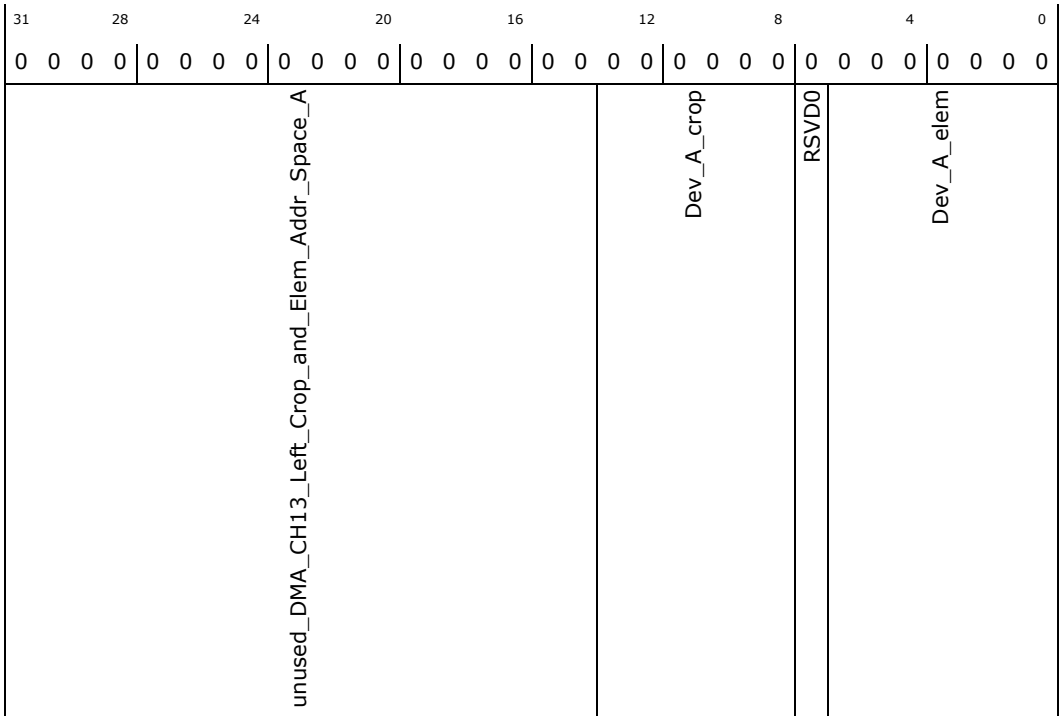
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41234h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH13_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.315 DMA_CH14_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH14_Left_Crop_and_Elem_Addr_Space_A)—Offset 41238h

DMA CH 14 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

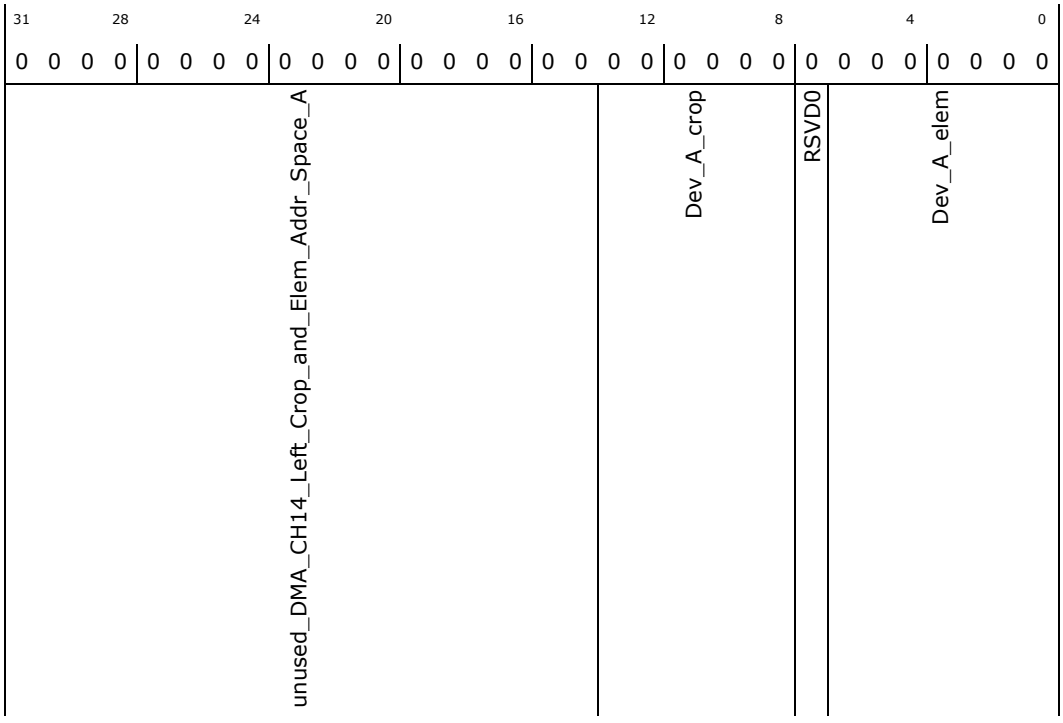
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41238h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH14_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.316 DMA_CH15_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH15_Left_Crop_and_Elem_Addr_Space_A)—Offset 4123Ch

DMA CH 15 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

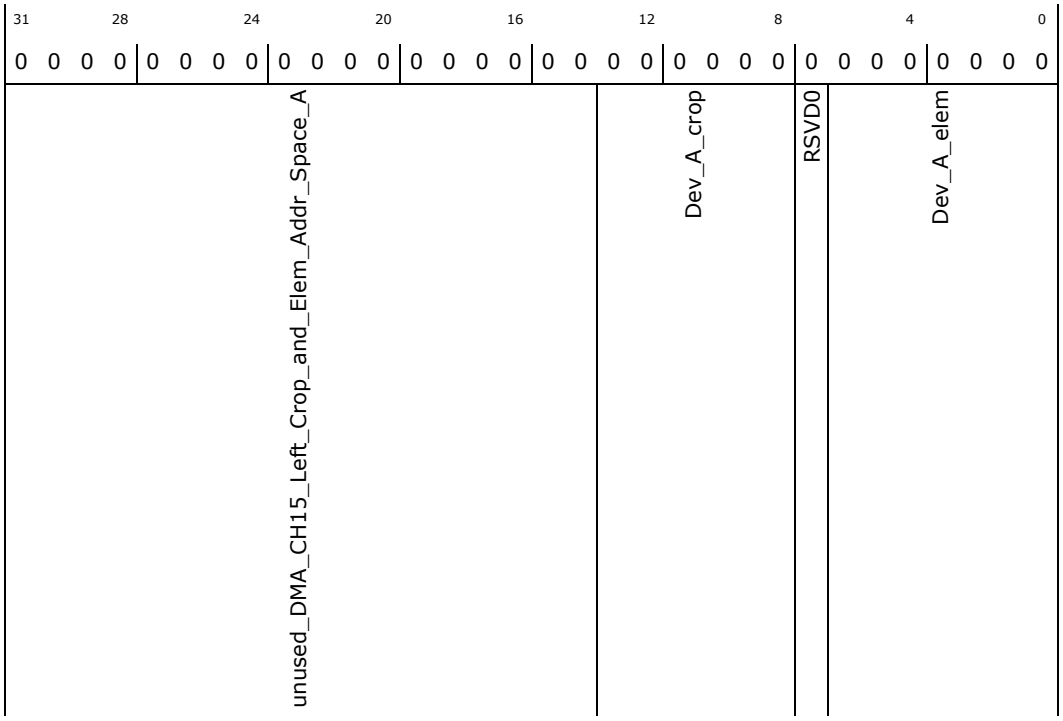
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4123Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH15_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.317 DMA_CH16_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH16_Left_Crop_and_Elem_Addr_Space_A)—Offset 41240h

DMA CH 16 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

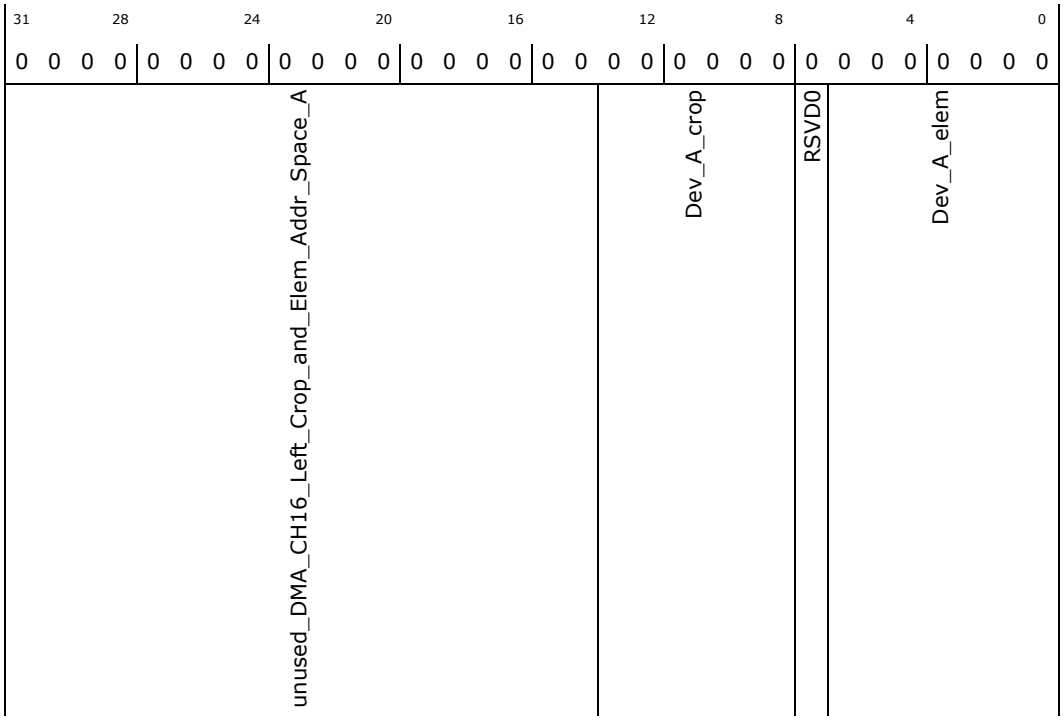
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41240h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH16_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.318 DMA_CH17_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH17_Left_Crop_and_Elem_Addr_Space_A)—Offset 41244h

DMA CH 17 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

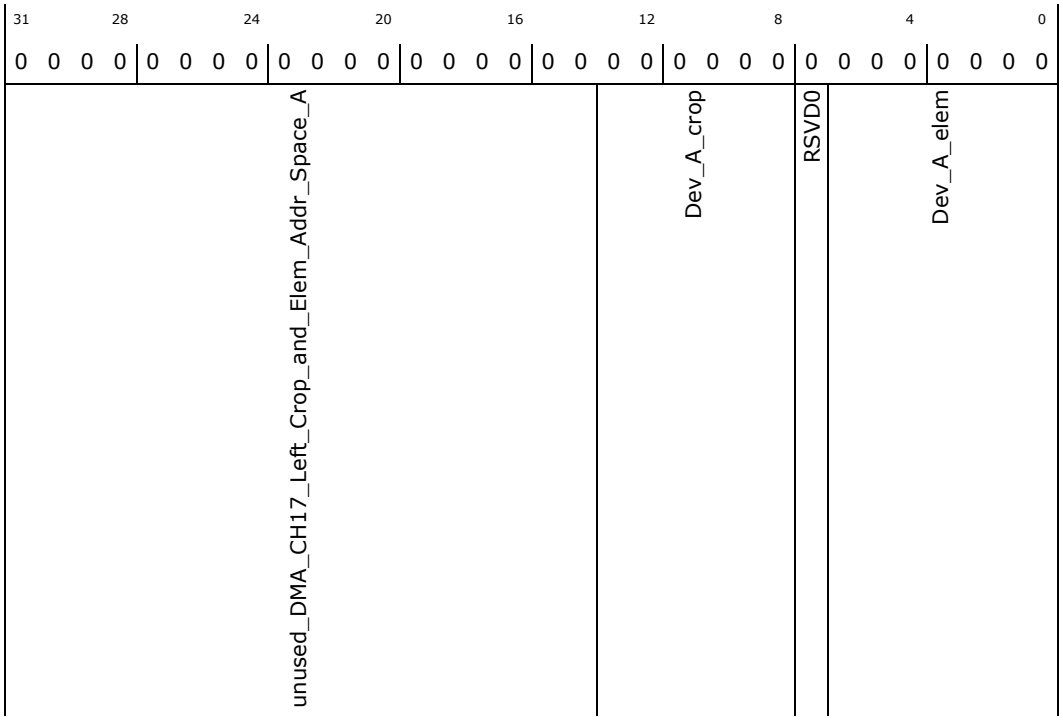
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41244h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH17_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.319 DMA_CH18_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH18_Left_Crop_and_Elem_Addr_Space_A)—Offset 41248h

DMA CH 18 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

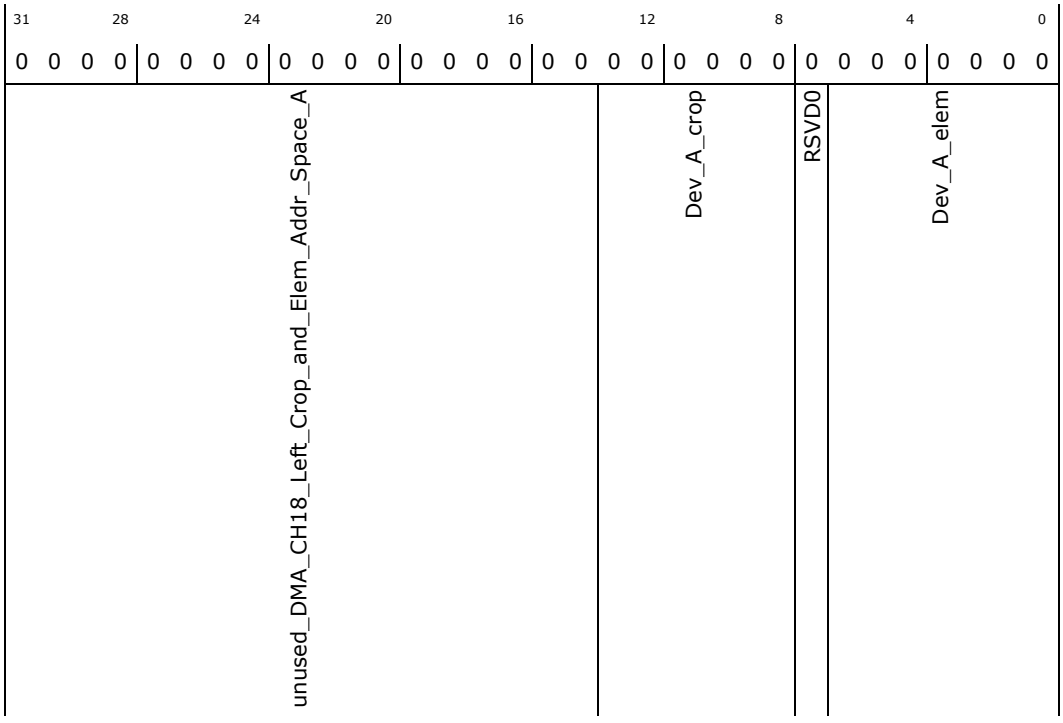
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41248h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH18_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.320 DMA_CH19_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH19_Left_Crop_and_Elem_Addr_Space_A)—Offset 4124Ch

DMA CH 19 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

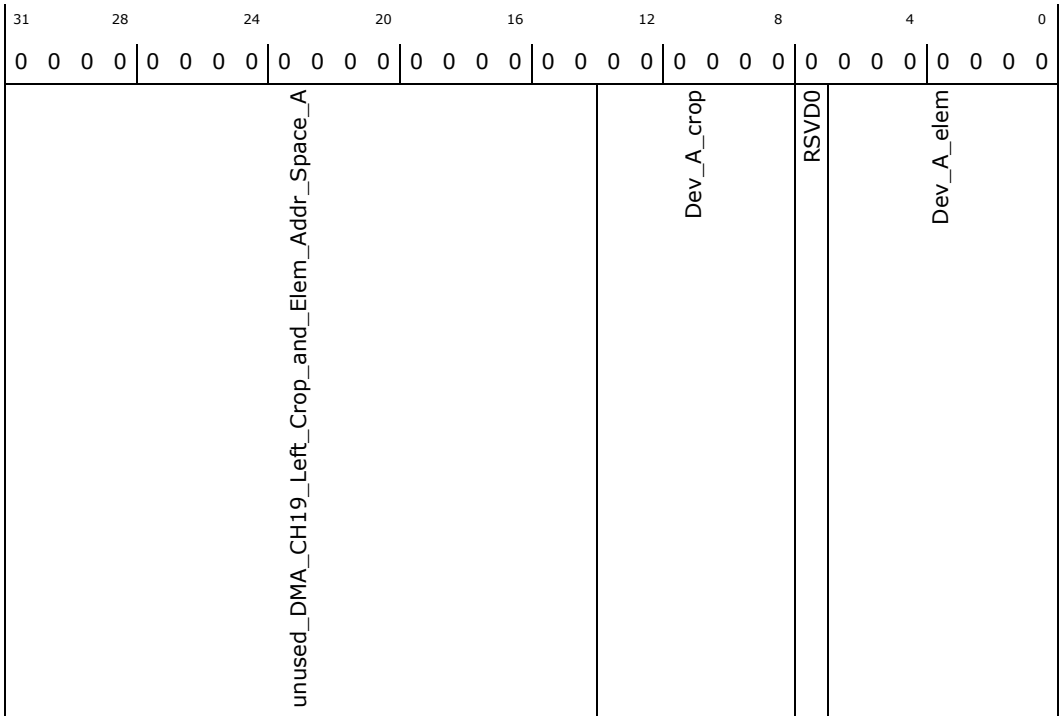
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4124Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH19_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.321 DMA_CH20_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH20_Left_Crop_and_Elem_Addr_Space_A)—Offset 41250h

DMA CH 20 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

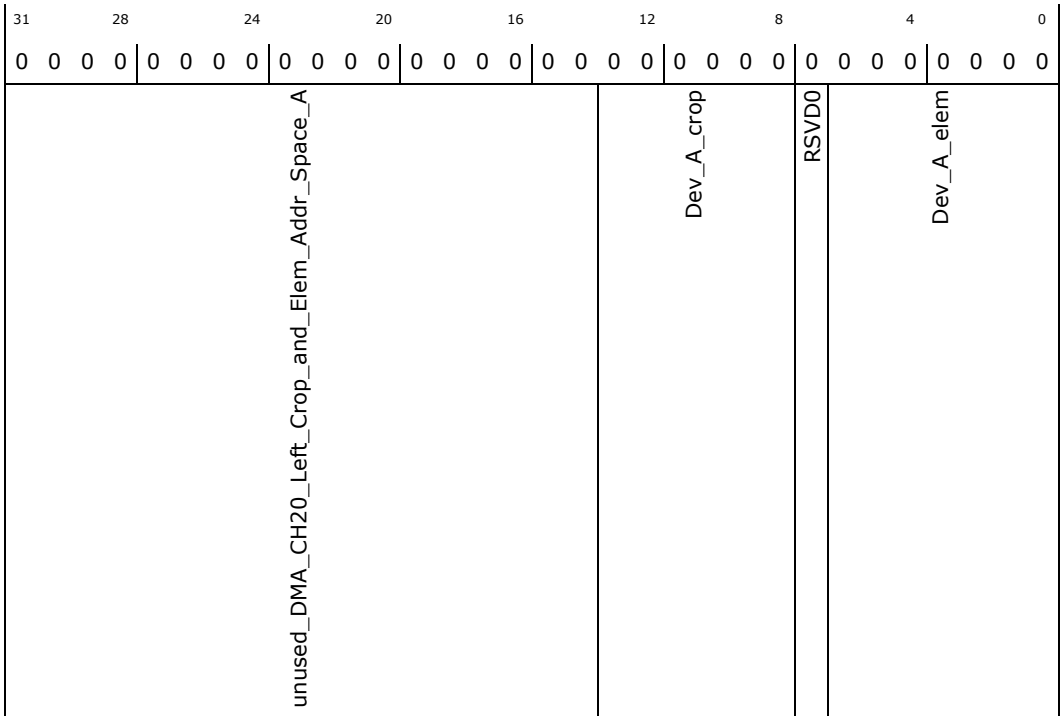
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41250h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH20_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.322 DMA_CH21_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH21_Left_Crop_and_Elem_Addr_Space_A)—Offset 41254h

DMA CH 21 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

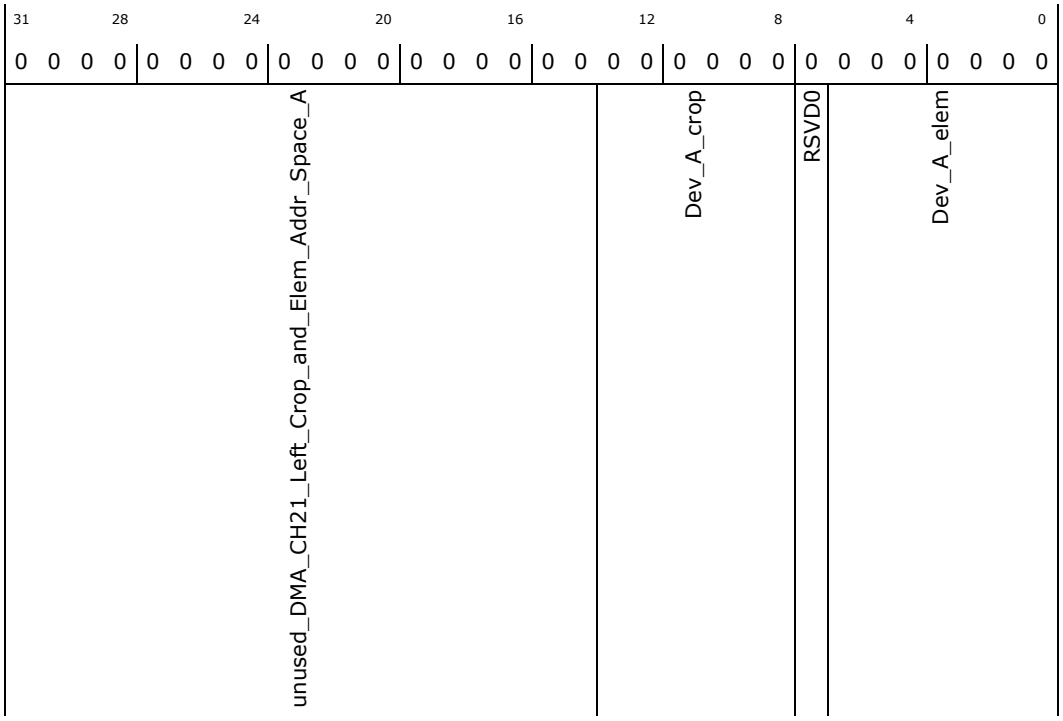
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41254h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH21_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.323 DMA_CH22_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH22_Left_Crop_and_Elem_Addr_Space_A)—Offset 41258h

DMA CH 22 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

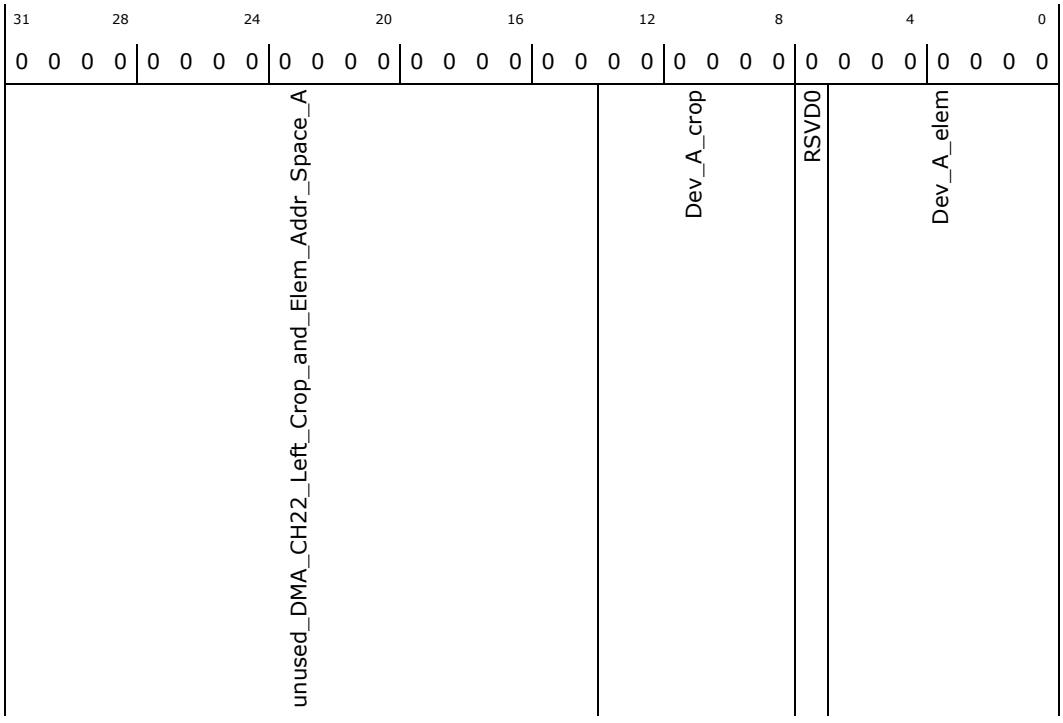
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41258h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH22_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.324 DMA_CH23_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH23_Left_Crop_and_Elem_Addr_Space_A)—Offset 4125Ch

DMA CH 23 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

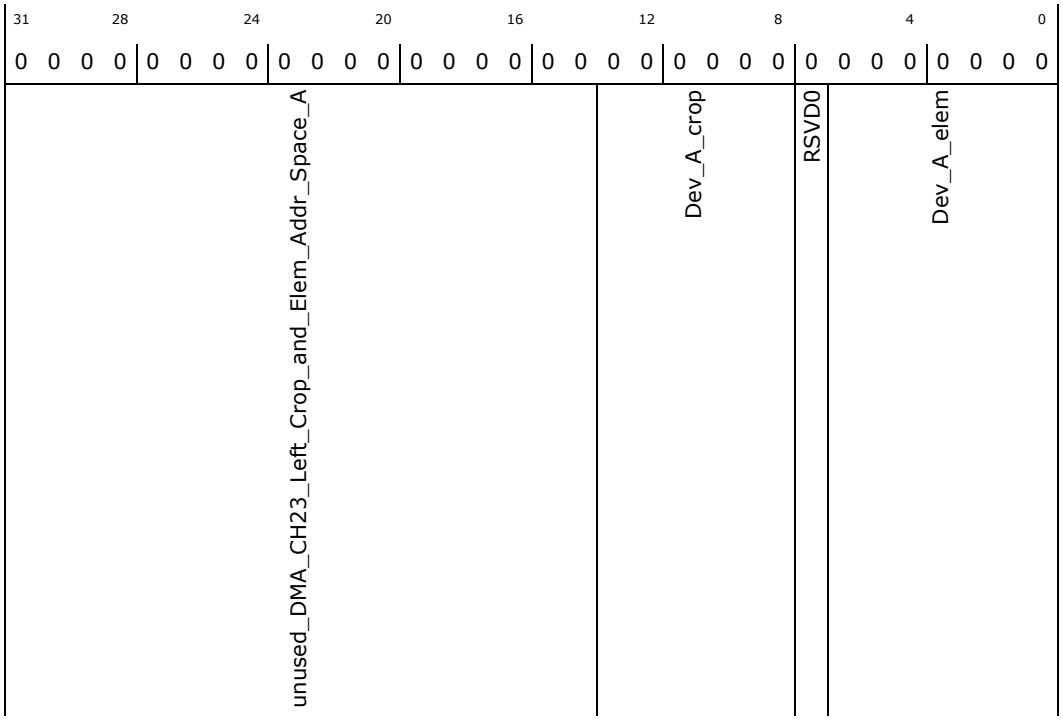
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4125Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH23_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.325 DMA_CH24_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH24_Left_Crop_and_Elem_Addr_Space_A)—Offset 41260h

DMA CH 24 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

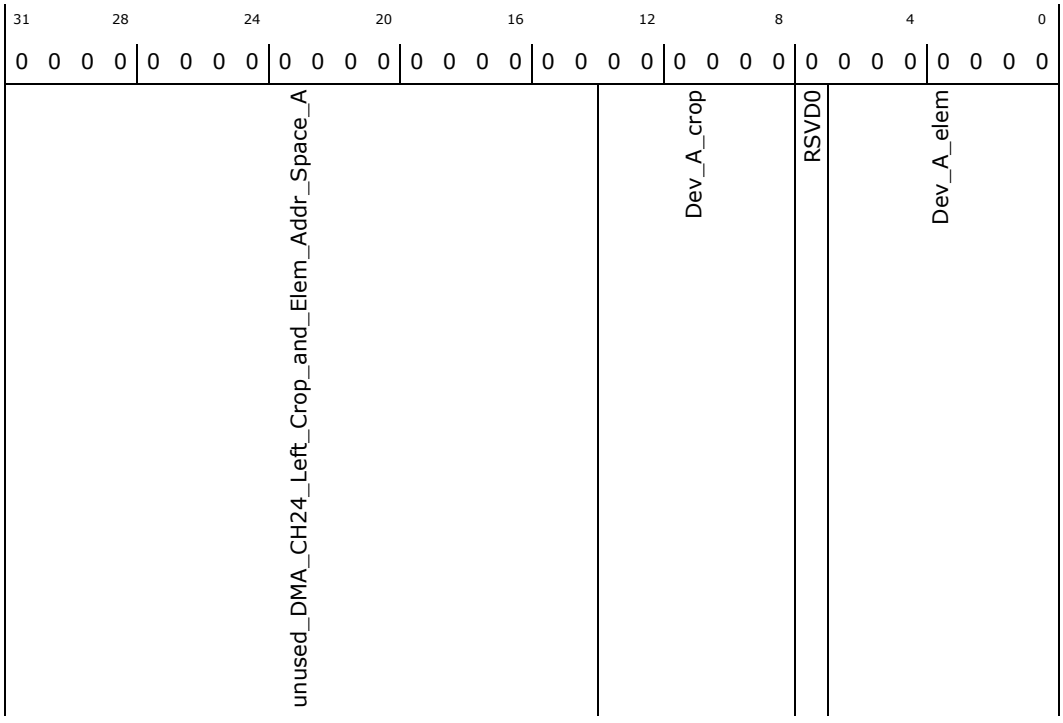
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41260h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH24_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.326 DMA_CH25_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH25_Left_Crop_and_Elem_Addr_Space_A)—Offset 41264h

DMA CH 25 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

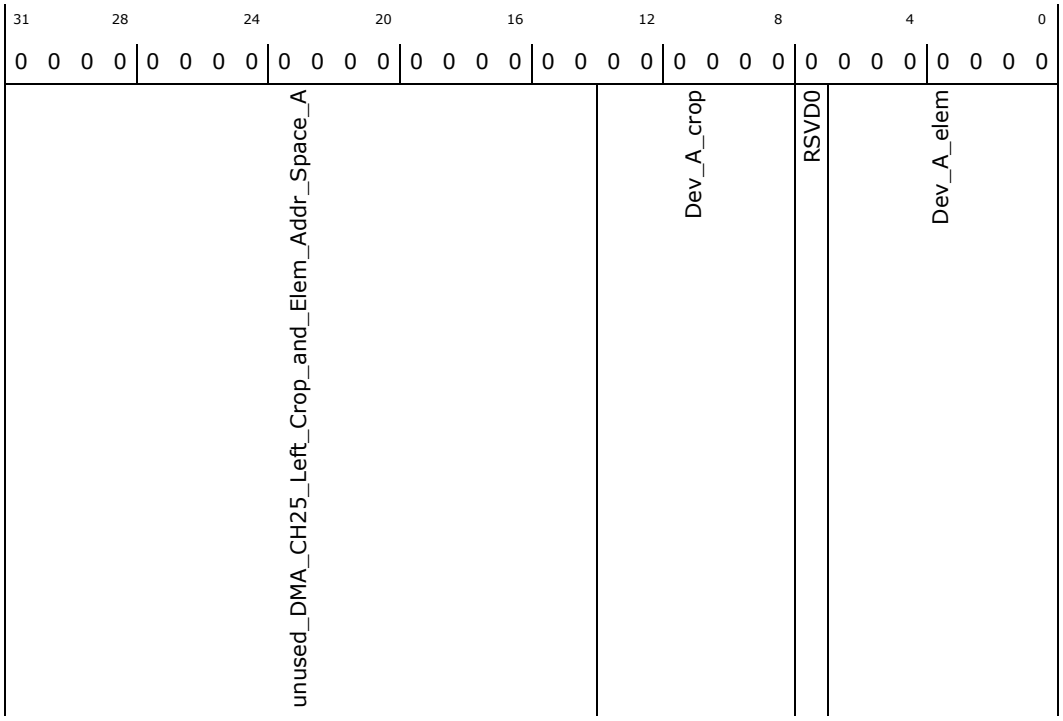
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41264h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH25_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.327 DMA_CH26_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH26_Left_Crop_and_Elem_Addr_Space_A)—Offset 41268h

DMA CH 26 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

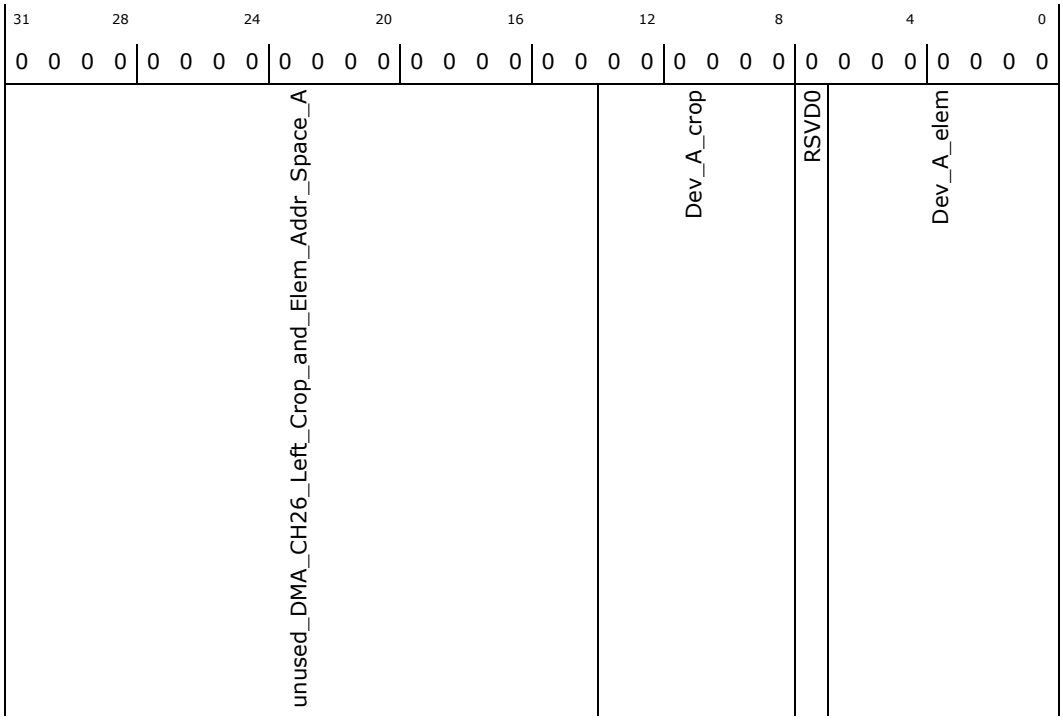
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41268h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH26_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.328 DMA_CH27_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH27_Left_Crop_and_Elem_Addr_Space_A)—Offset 4126Ch

DMA CH 27 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

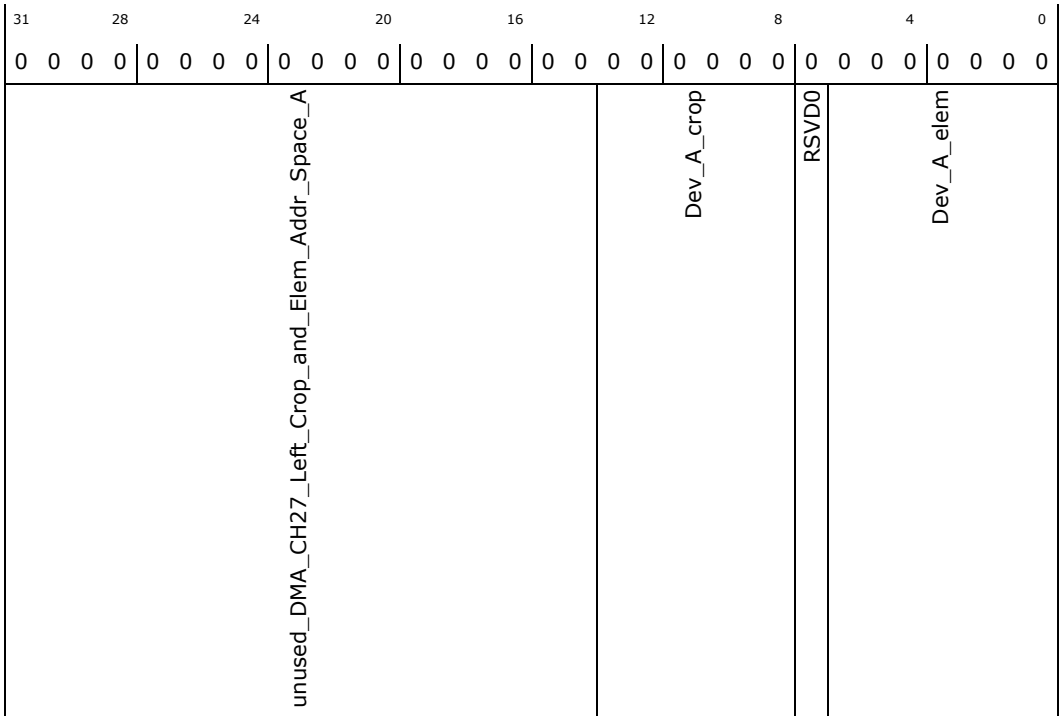
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4126Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH27_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.329 DMA_CH28_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH28_Left_Crop_and_Elem_Addr_Space_A)—Offset 41270h

DMA CH 28 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

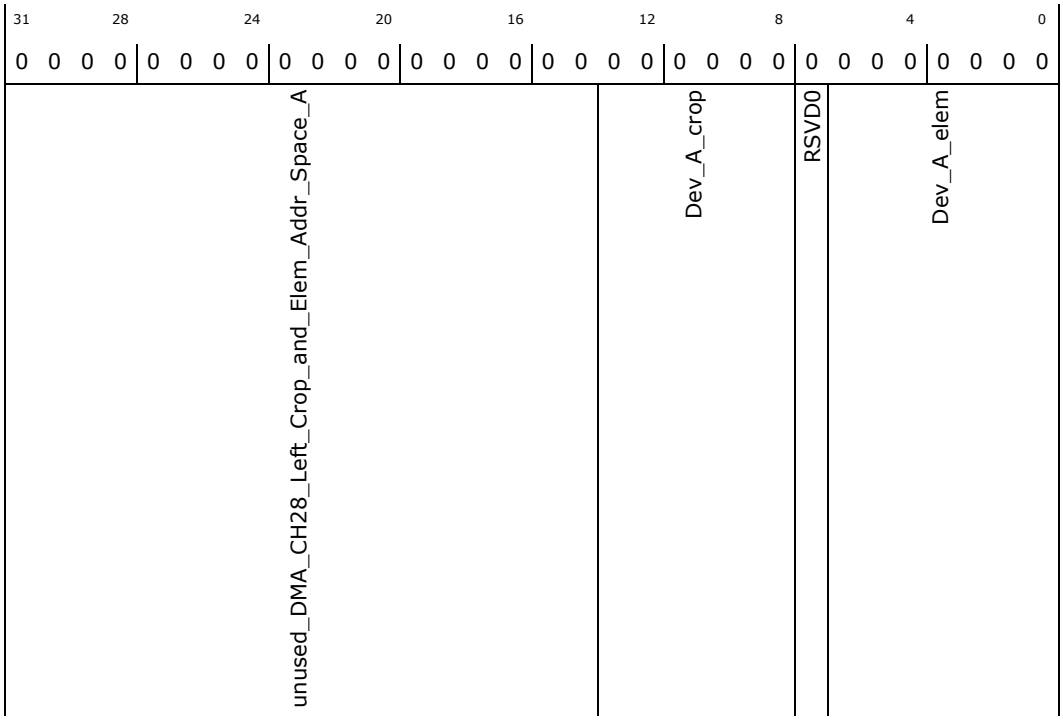
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41270h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH28_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.330 DMA_CH29_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH29_Left_Crop_and_Elem_Addr_Space_A)—Offset 41274h

DMA CH 29 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

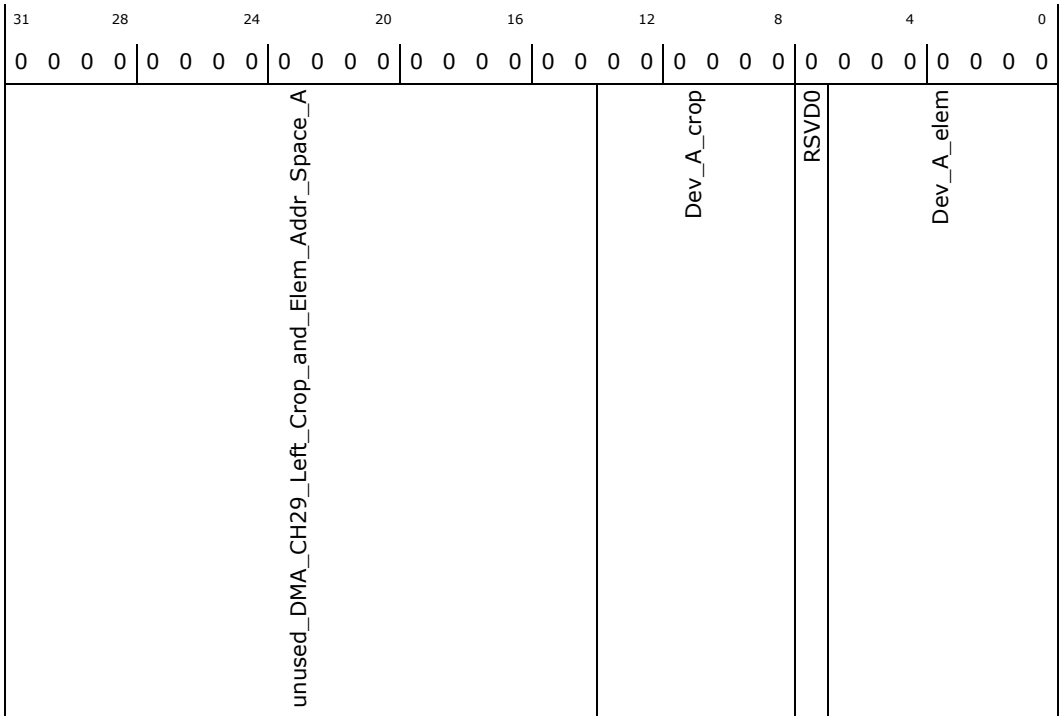
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41274h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH29_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.331 DMA_CH30_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH30_Left_Crop_and_Elem_Addr_Space_A)—Offset 41278h

DMA CH 30 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

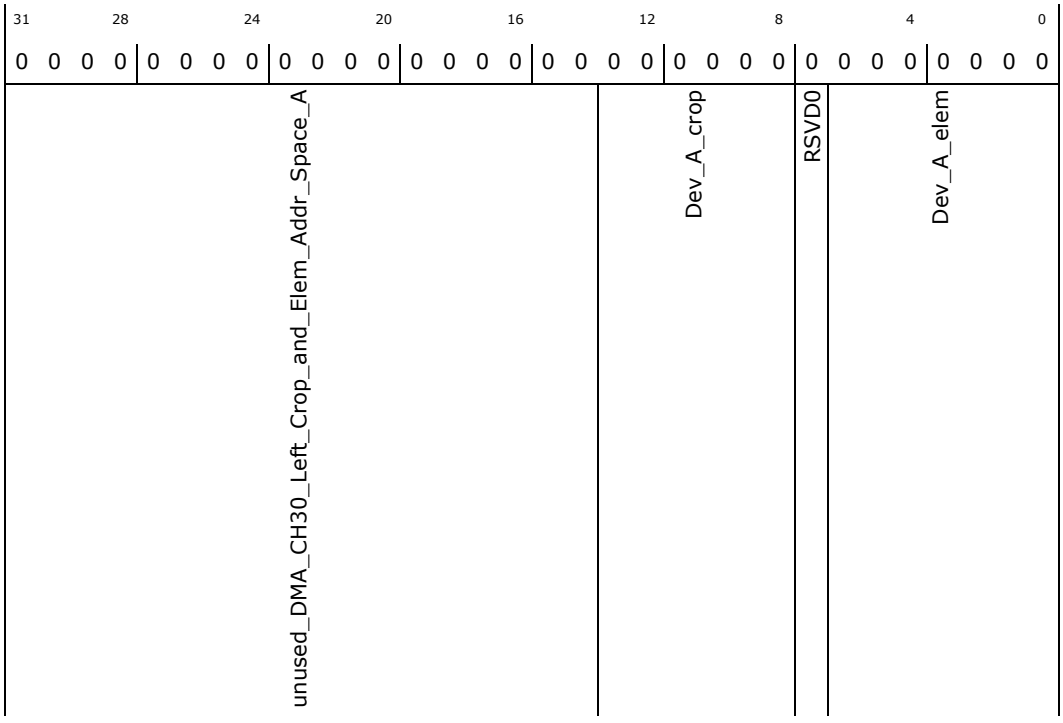
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41278h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH30_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.332 DMA_CH31_Left_Crop_and_Elem_Addr_Space_A (isp_dma_DMA_CH31_Left_Crop_and_Elem_Addr_Space_A)—Offset 4127Ch

DMA CH 31 PARAM 2: Setting value of cropped pixels for each line and number of elements in a word for Device A side of the connection.

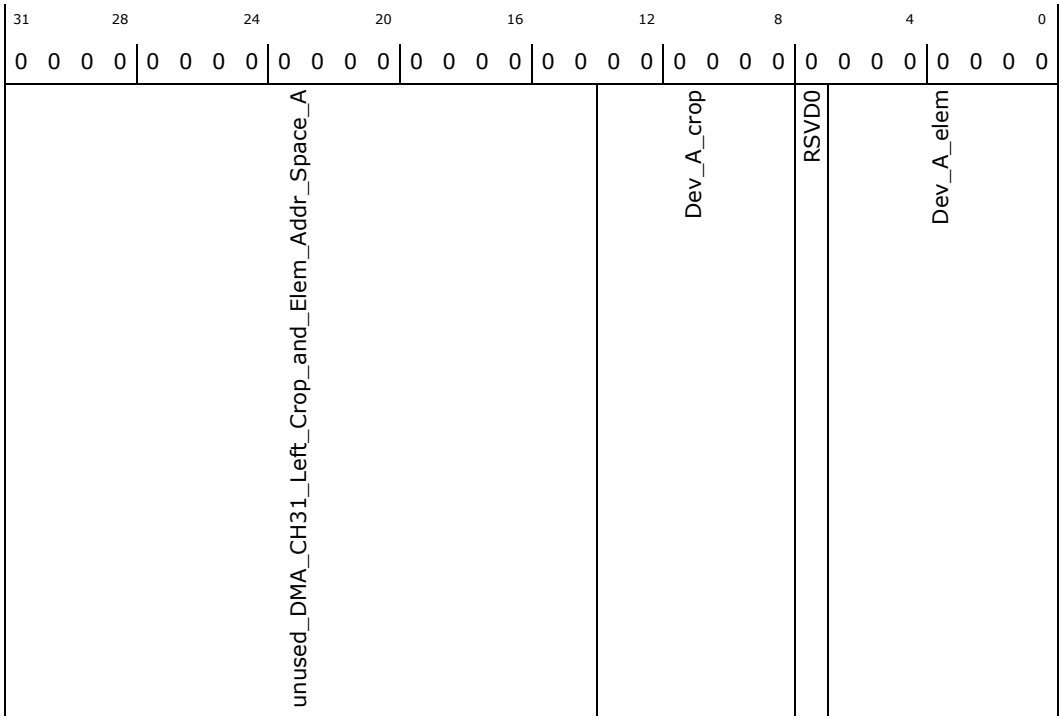
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4127Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH31_Left_Crop_and_Elem_Addr_Space_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.2.333 DMA_CH22_Stride_Addr_Space_A (isp_dma_DMA_CH22_Stride_Addr_Space_A)—Offset 412C0h

DMA CH 22 PARAM 1: Line Stride for Device A side of the connection.

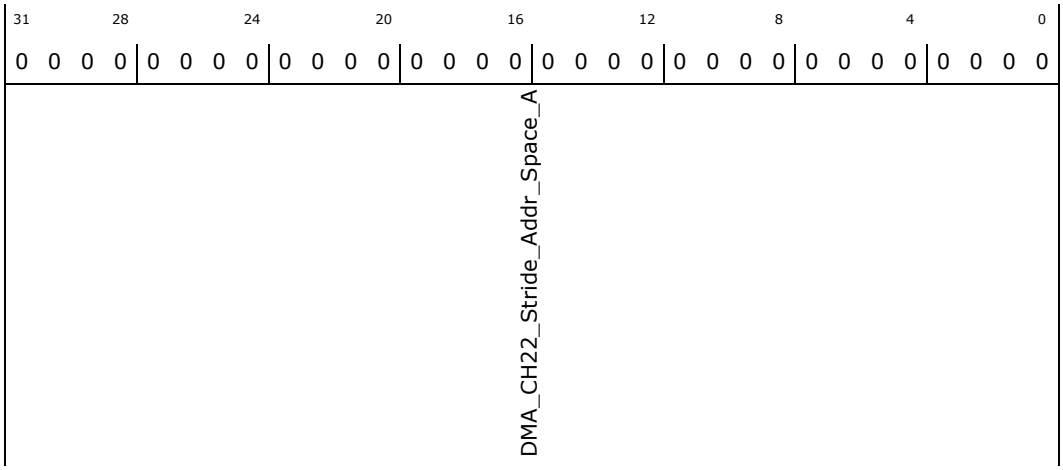
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 412C0h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH22_Stride_Addr_Space_A:** DMA CH 22 PARAM 1: Line Stride for Device A side of the connection.

5.2.334 DMA_CH23_Stride_Addr_Space_A (isp_dma_DMA_CH23_Stride_Addr_Space_A)—Offset 412C4h

DMA CH 23 PARAM 1: Line Stride for Device A side of the connection.

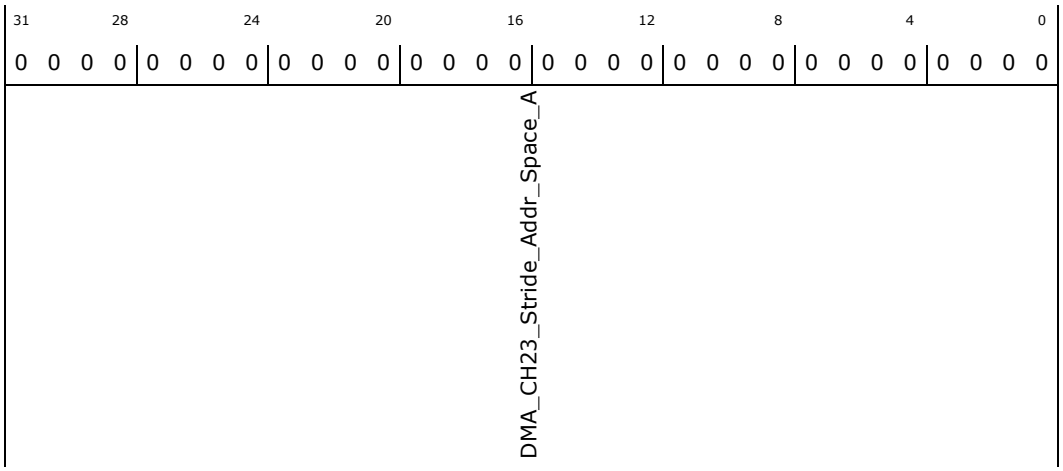
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 412C4h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH23_Stride_Addr_Space_A:** DMA CH 23 PARAM 1: Line Stride for Device A side of the connection.

5.2.335 DMA_CH24_Stride_Addr_Space_A (isp_dma_DMA_CH24_Stride_Addr_Space_A)—Offset 412C8h

DMA CH 24 PARAM 1: Line Stride for Device A side of the connection.

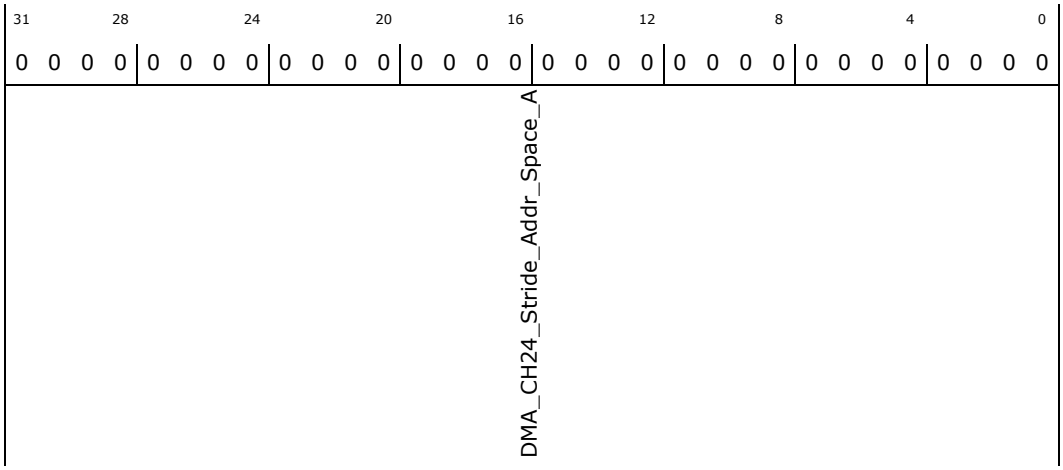
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 412C8h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH24_Stride_Addr_Space_A:** DMA CH 24 PARAM 1: Line Stride for Device A side of the connection.

5.2.336 DMA_CH25_Stride_Addr_Space_A (isp_dma_DMA_CH25_Stride_Addr_Space_A)—Offset 412CCh

DMA CH 25 PARAM 1: Line Stride for Device A side of the connection.

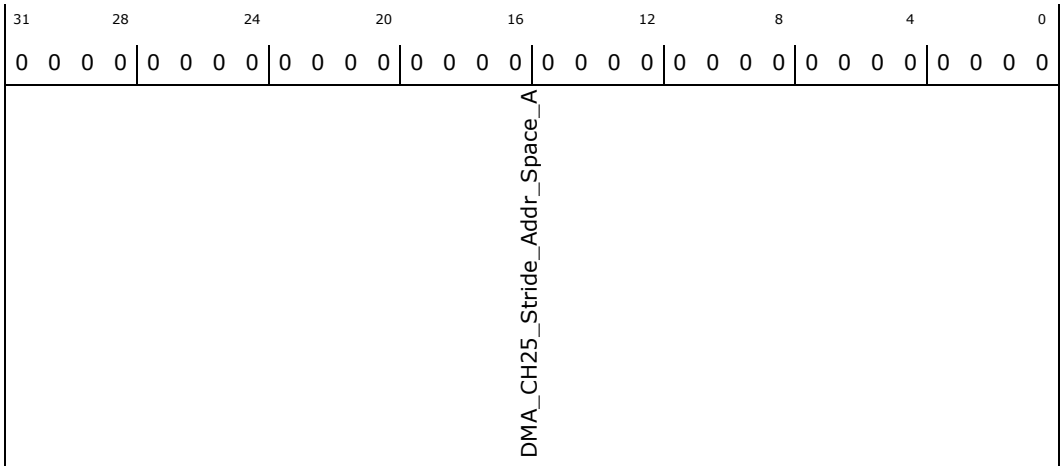
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 412CCh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH25_Stride_Addr_Space_A:** DMA CH 25 PARAM 1: Line Stride for Device A side of the connection.

5.2.337 DMA_CH26_Stride_Addr_Space_A (isp_dma_DMA_CH26_Stride_Addr_Space_A)—Offset 412D0h

DMA CH 26 PARAM 1: Line Stride for Device A side of the connection.

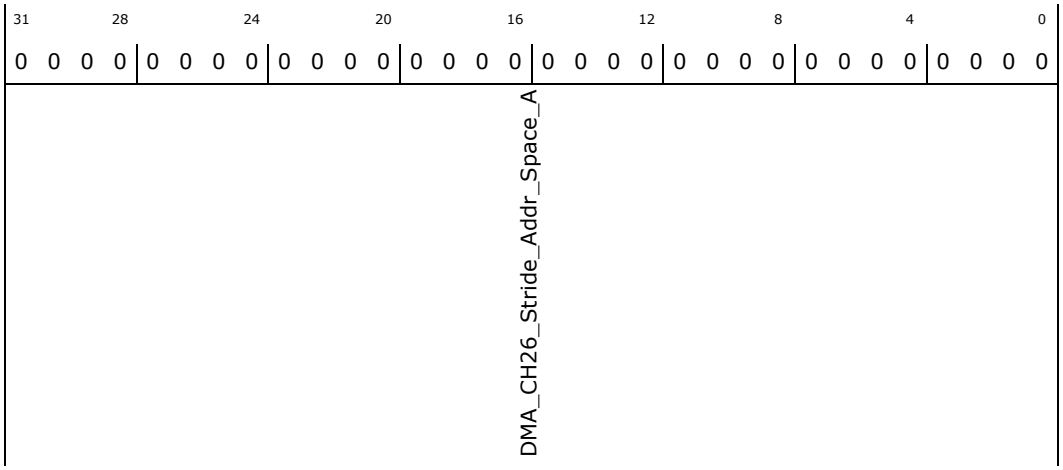
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 412D0h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH26_Stride_Addr_Space_A:** DMA CH 26 PARAM 1: Line Stride for Device A side of the connection.

5.2.338 DMA_CH27_Stride_Addr_Space_A (isp_dma_DMA_CH27_Stride_Addr_Space_A)—Offset 412D4h

DMA CH 27 PARAM 1: Line Stride for Device A side of the connection.

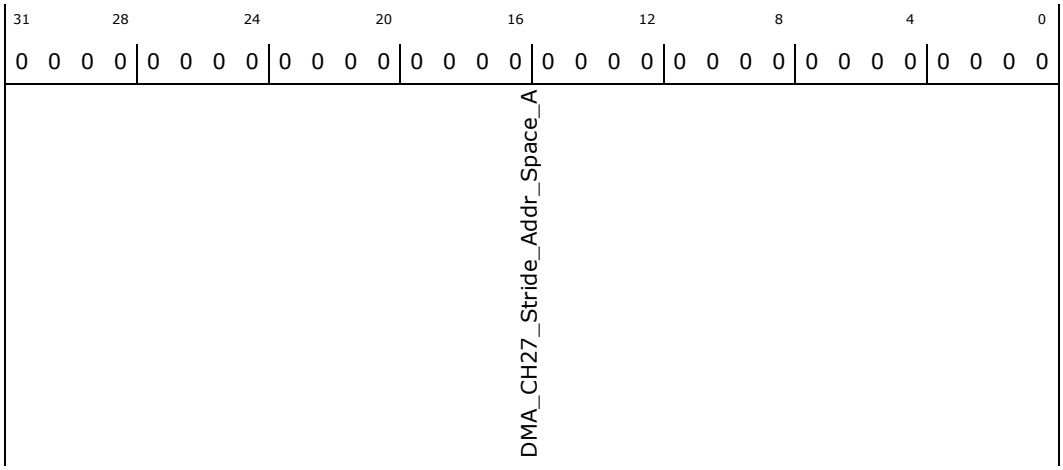
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 412D4h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH27_Stride_Addr_Space_A:** DMA CH 27 PARAM 1: Line Stride for Device A side of the connection.

5.2.339 DMA_CH28_Stride_Addr_Space_A (isp_dma_DMA_CH28_Stride_Addr_Space_A)—Offset 412D8h

DMA CH 28 PARAM 1: Line Stride for Device A side of the connection.

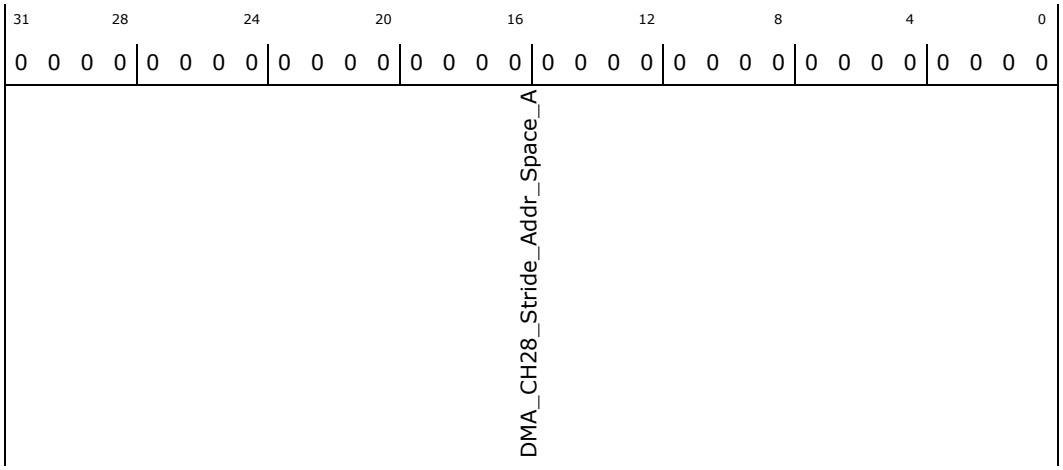
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 412D8h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH28_Stride_Addr_Space_A:** DMA CH 28 PARAM 1: Line Stride for Device A side of the connection.

5.2.340 DMA_CH29_Stride_Addr_Space_A (isp_dma_DMA_CH29_Stride_Addr_Space_A)—Offset 412DCh

DMA CH 29 PARAM 1: Line Stride for Device A side of the connection.

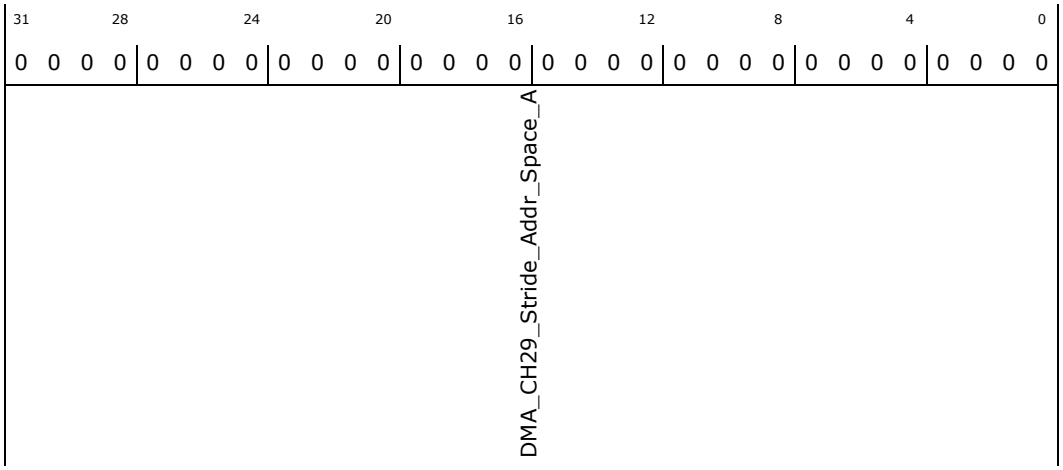
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 412DCh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH29_Stride_Addr_Space_A:** DMA CH 29 PARAM 1: Line Stride for Device A side of the connection.

5.2.341 DMA_CH30_Stride_Addr_Space_A (isp_dma_DMA_CH30_Stride_Addr_Space_A)—Offset 412E0h

DMA CH 30 PARAM 1: Line Stride for Device A side of the connection.

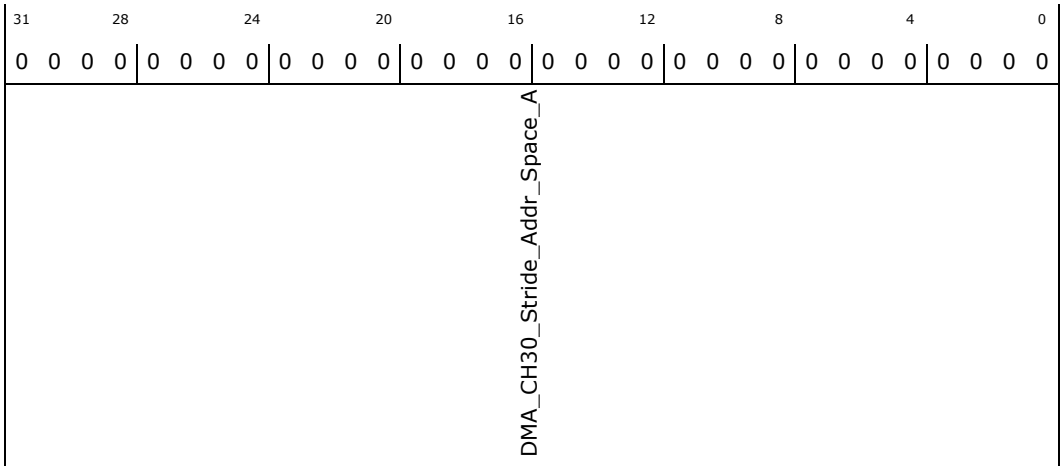
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 412E0h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH30_Stride_Addr_Space_A:** DMA CH 30 PARAM 1: Line Stride for Device A side of the connection.

5.2.342 DMA_CH31_Stride_Addr_Space_A (isp_dma_DMA_CH31_Stride_Addr_Space_A)—Offset 412E4h

DMA CH 31 PARAM 1: Line Stride for Device A side of the connection.

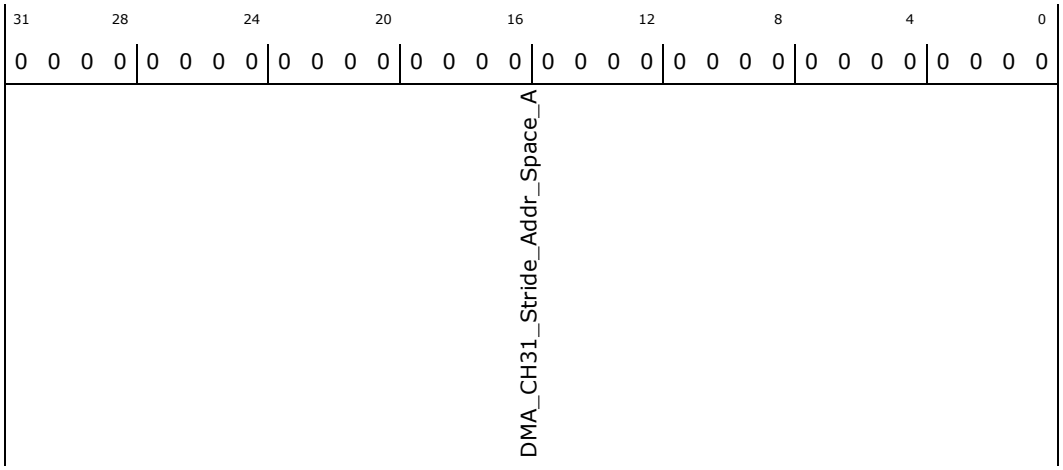
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 412E4h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH31_Stride_Addr_Space_A:** DMA CH 31 PARAM 1: Line Stride for Device A side of the connection.

5.2.343 DMA_CH0_Block_Width_Addr_Space_A (isp_dma_DMA_CH0_Block_Width_Addr_Space_A)—Offset 41300h

DMA CH 0 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

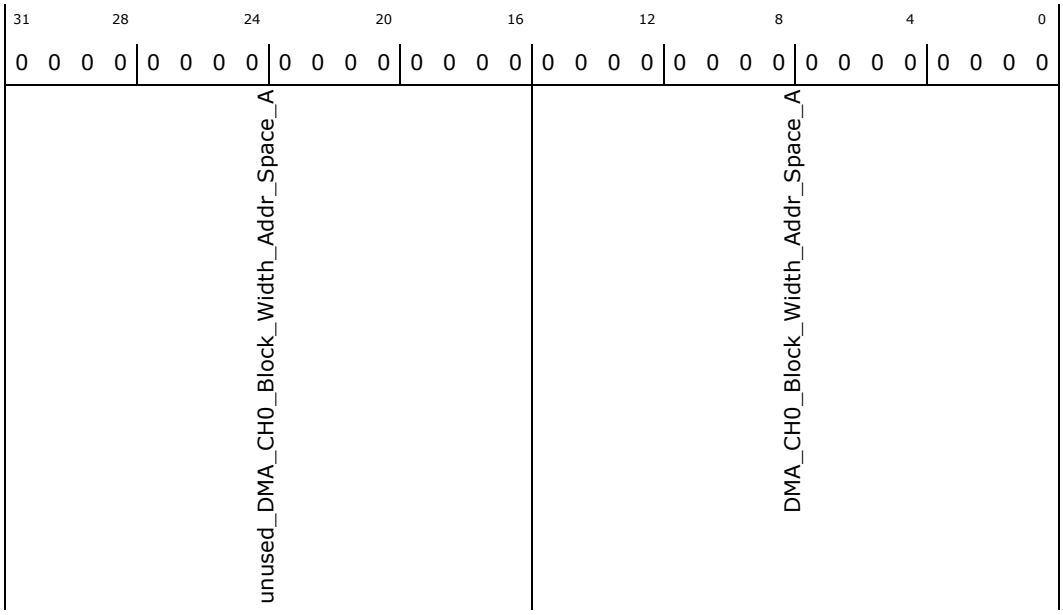
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41300h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH0_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH0_Block_Width_Addr_Space_A:** DMA CH 0 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.344 DMA_CH1_Block_Width_Addr_Space_A (isp_dma_DMA_CH1_Block_Width_Addr_Space_A)—Offset 41304h

DMA CH 1 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

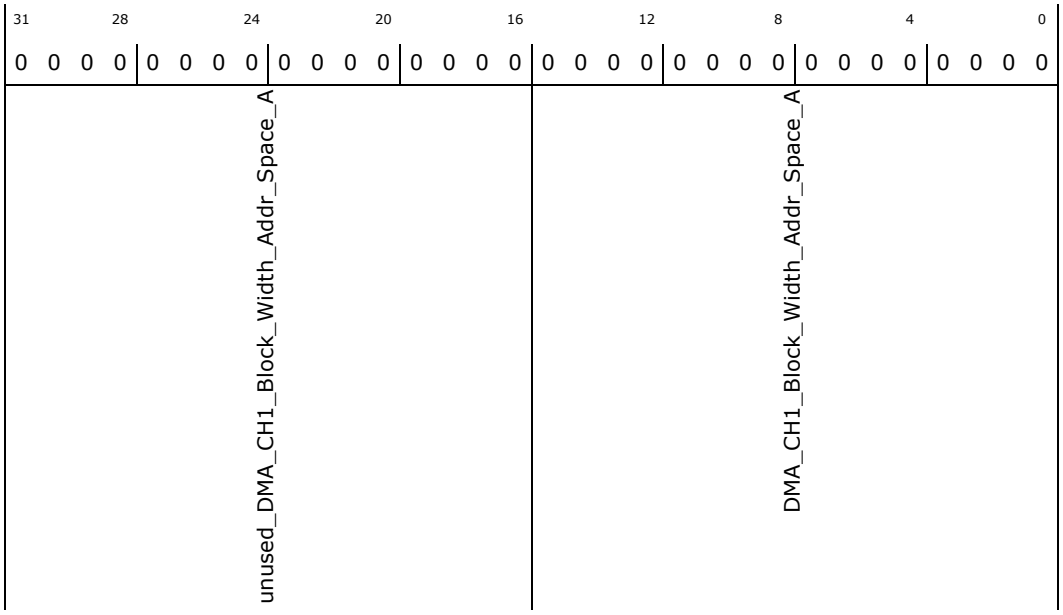
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41304h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH1_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH1_Block_Width_Addr_Space_A:** DMA CH 1 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.345 DMA_CH2_Block_Width_Addr_Space_A (isp_dma_DMA_CH2_Block_Width_Addr_Space_A)—Offset 41308h

DMA CH 2 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

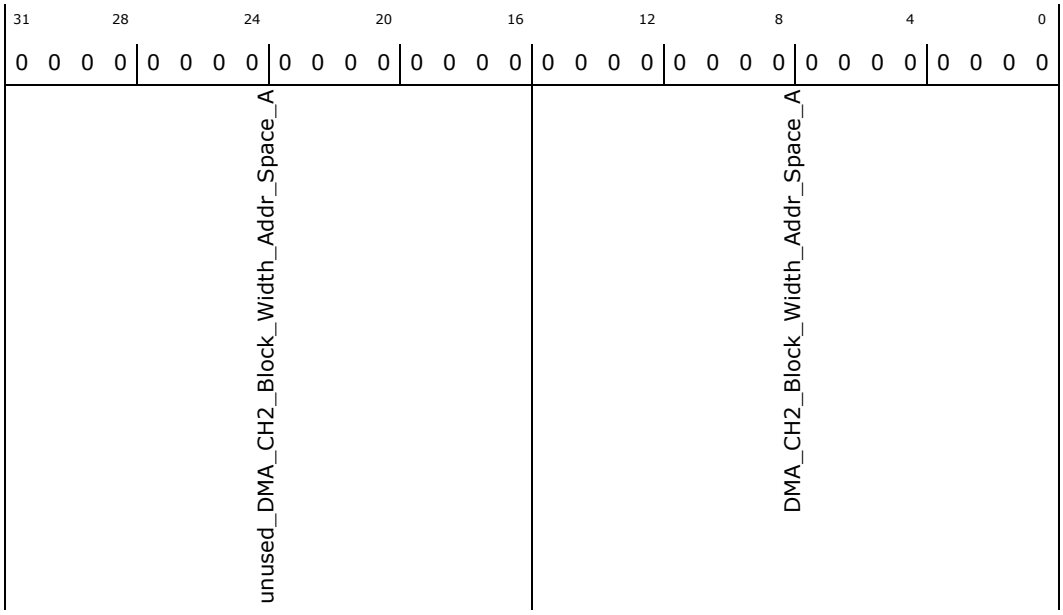
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41308h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH2_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH2_Block_Width_Addr_Space_A:** DMA CH 2 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.346 DMA_CH3_Block_Width_Addr_Space_A (isp_dma_DMA_CH3_Block_Width_Addr_Space_A)—Offset 4130Ch

DMA CH 3 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

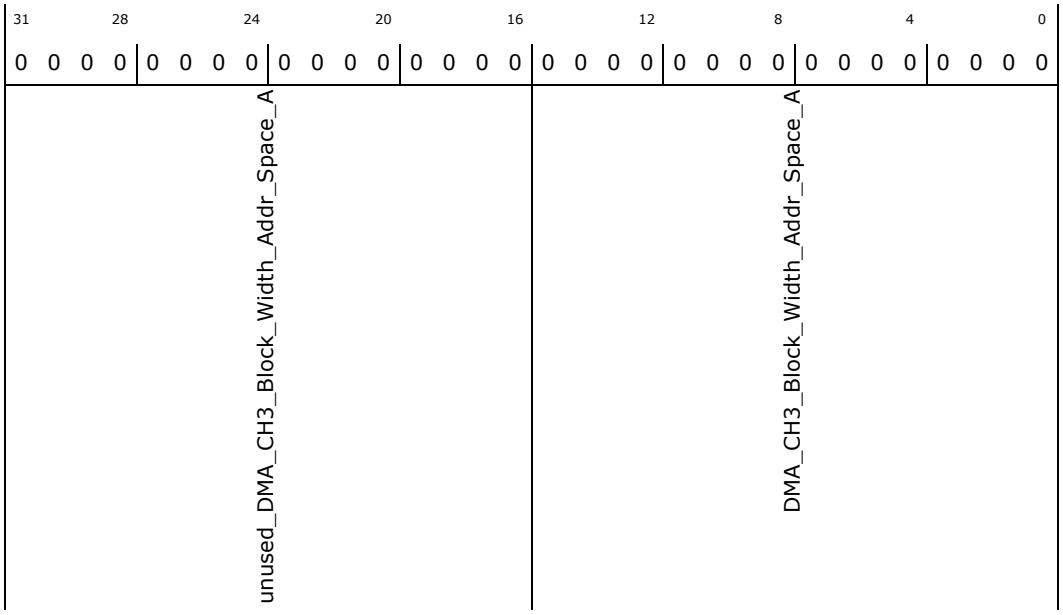
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4130Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH3_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH3_Block_Width_Addr_Space_A:** DMA CH 3 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.347 DMA_CH4_Block_Width_Addr_Space_A (isp_dma_DMA_CH4_Block_Width_Addr_Space_A)—Offset 41310h

DMA CH 4 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

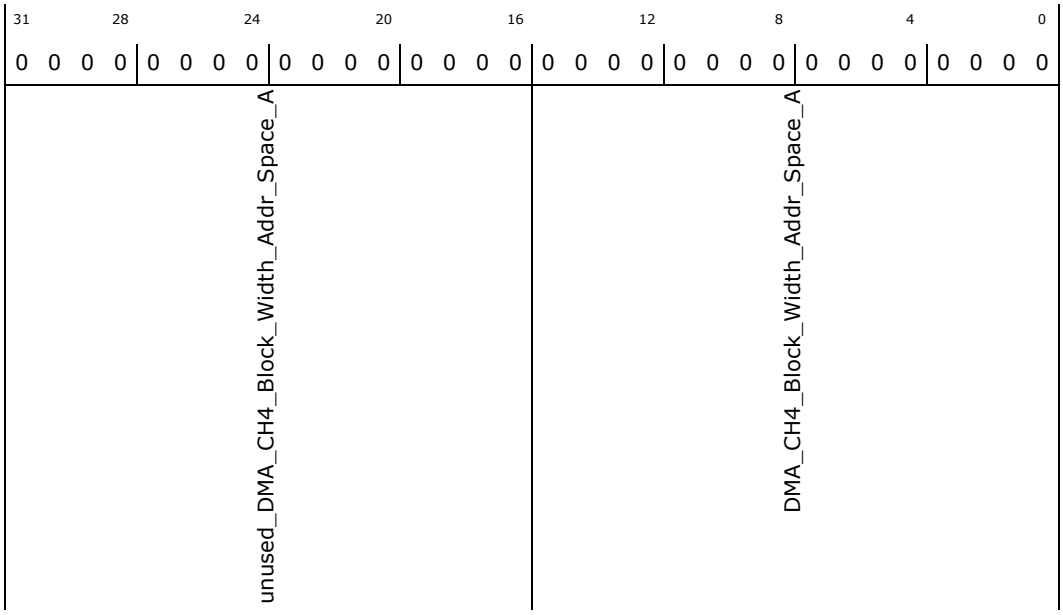
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41310h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH4_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH4_Block_Width_Addr_Space_A:** DMA CH 4 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.348 DMA_CH5_Block_Width_Addr_Space_A (isp_dma_DMA_CH5_Block_Width_Addr_Space_A)—Offset 41314h

DMA CH 5 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

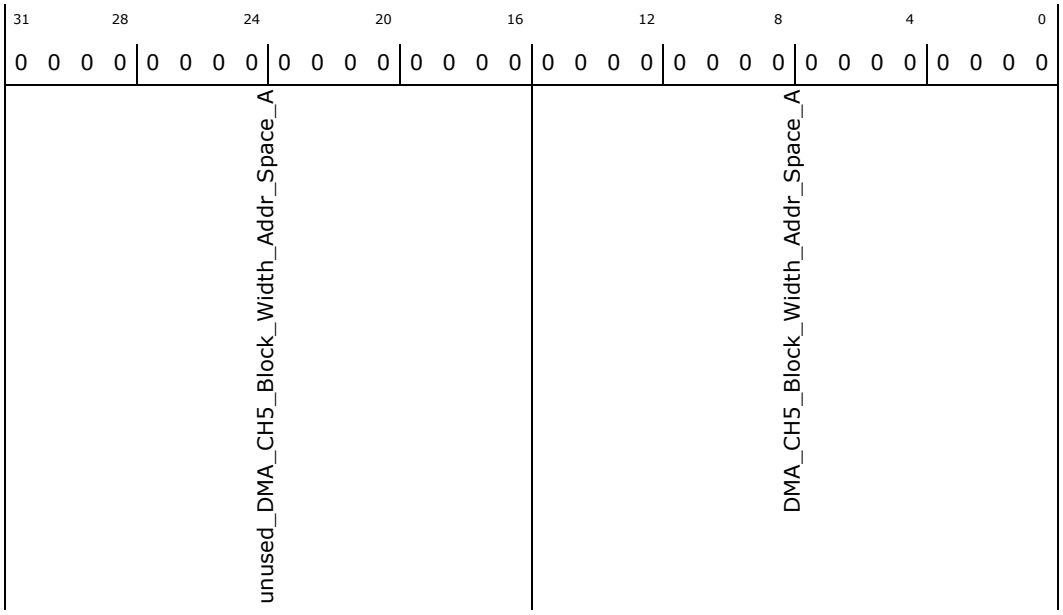
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41314h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH5_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH5_Block_Width_Addr_Space_A:** DMA CH 5 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.349 DMA_CH6_Block_Width_Addr_Space_A (isp_dma_DMA_CH6_Block_Width_Addr_Space_A)—Offset 41318h

DMA CH 6 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

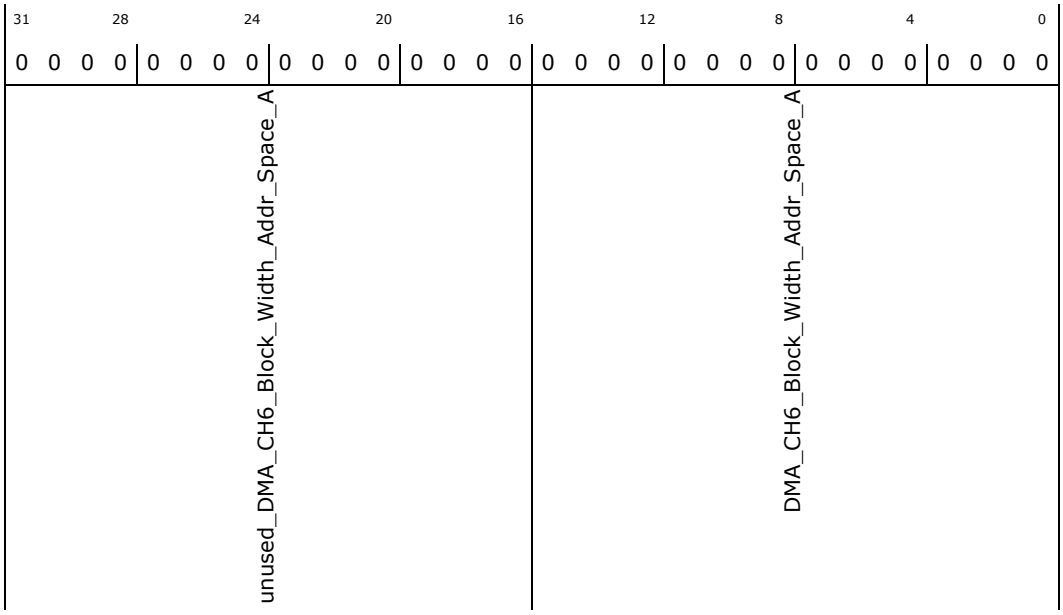
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41318h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH6_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH6_Block_Width_Addr_Space_A:** DMA CH 6 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.350 DMA_CH7_Block_Width_Addr_Space_A (isp_dma_DMA_CH7_Block_Width_Addr_Space_A)—Offset 4131Ch

DMA CH 7 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

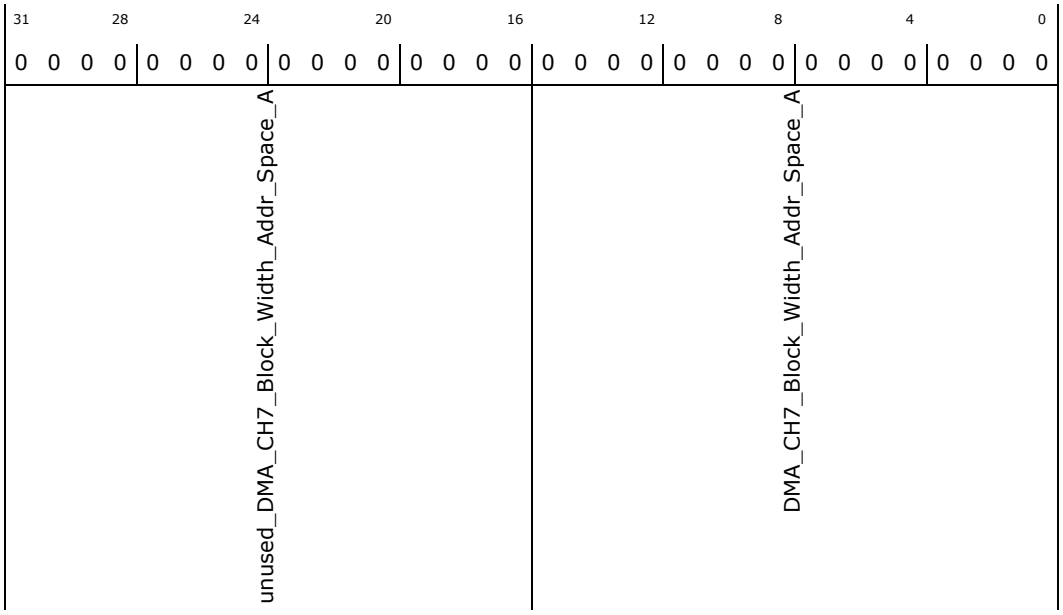
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4131Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH7_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH7_Block_Width_Addr_Space_A:** DMA CH 7 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.351 DMA_CH8_Block_Width_Addr_Space_A (isp_dma_DMA_CH8_Block_Width_Addr_Space_A)—Offset 41320h

DMA CH 8 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

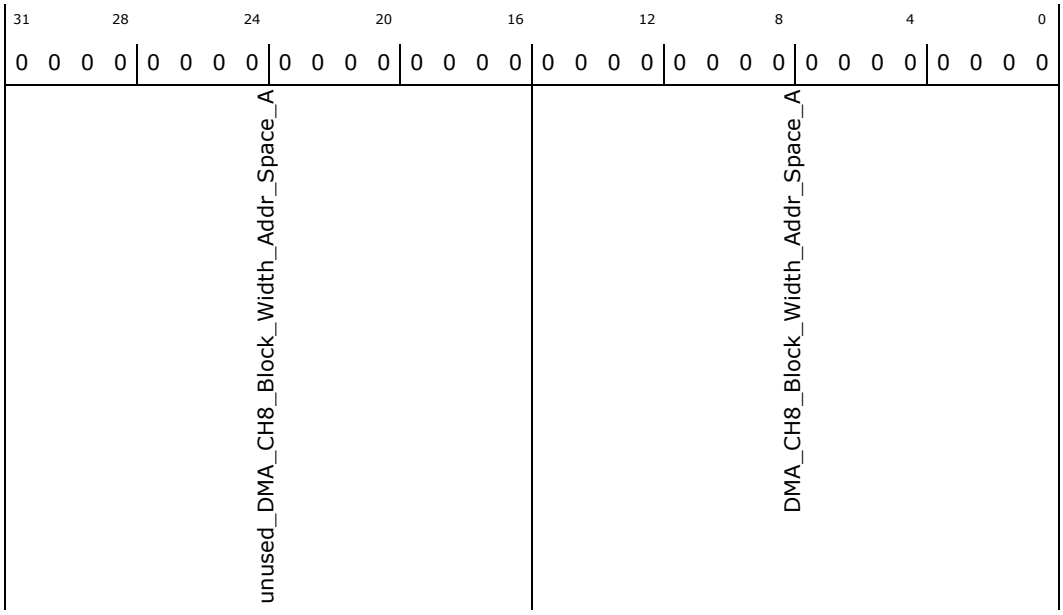
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41320h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH8_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH8_Block_Width_Addr_Space_A:** DMA CH 8 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.352 DMA_CH9_Block_Width_Addr_Space_A (isp_dma_DMA_CH9_Block_Width_Addr_Space_A)—Offset 41324h

DMA CH 9 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

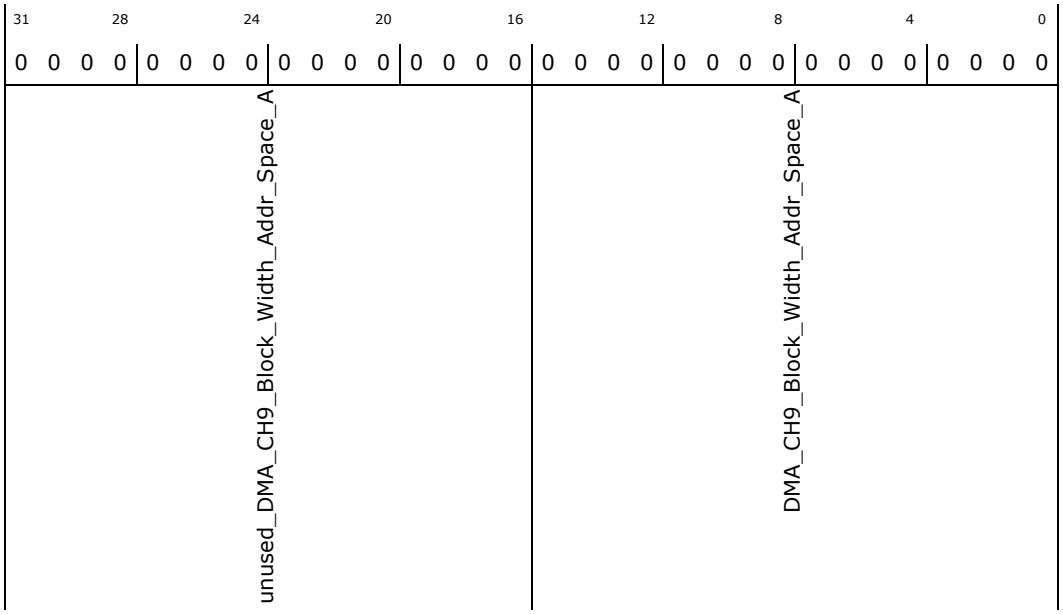
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41324h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH9_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH9_Block_Width_Addr_Space_A:** DMA CH 9 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.353 DMA_CH10_Block_Width_Addr_Space_A (isp_dma_DMA_CH10_Block_Width_Addr_Space_A)—Offset 41328h

DMA CH 10 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

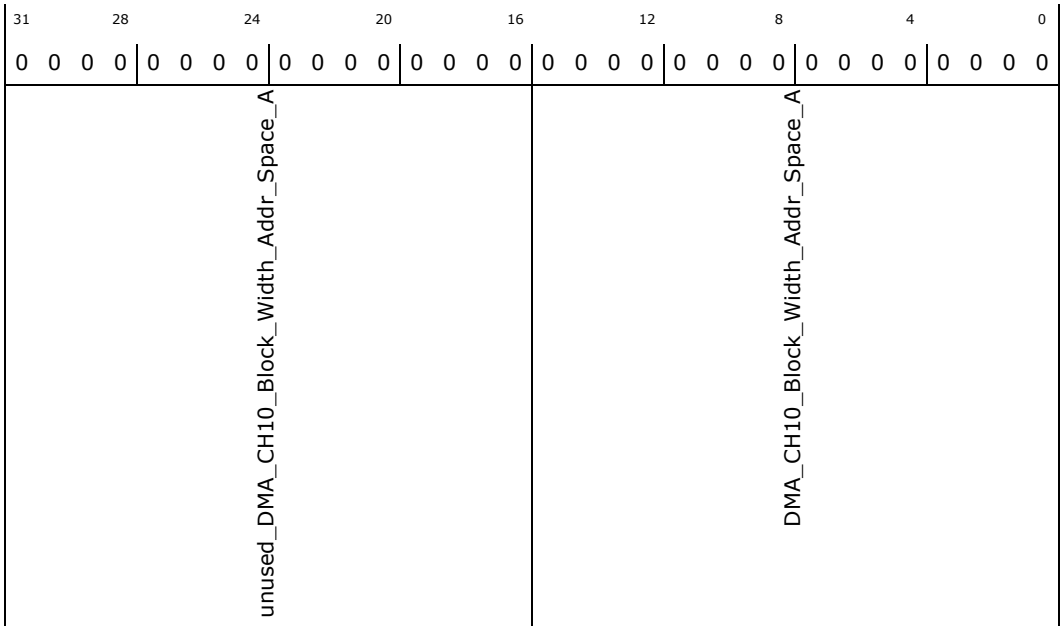
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41328h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH10_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH10_Block_Width_Addr_Space_A:** DMA CH 10 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.354 DMA_CH11_Block_Width_Addr_Space_A (isp_dma_DMA_CH11_Block_Width_Addr_Space_A)—Offset 4132Ch

DMA CH 11 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

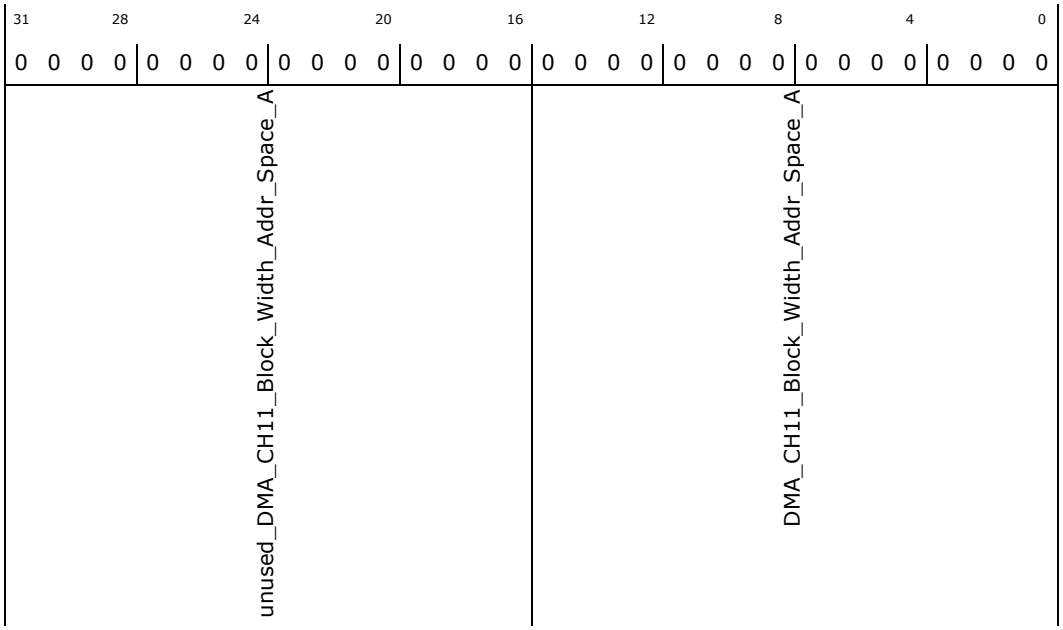
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4132Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH11_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH11_Block_Width_Addr_Space_A:** DMA CH 11 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.355 DMA_CH12_Block_Width_Addr_Space_A (isp_dma_DMA_CH12_Block_Width_Addr_Space_A)—Offset 41330h

DMA CH 12 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

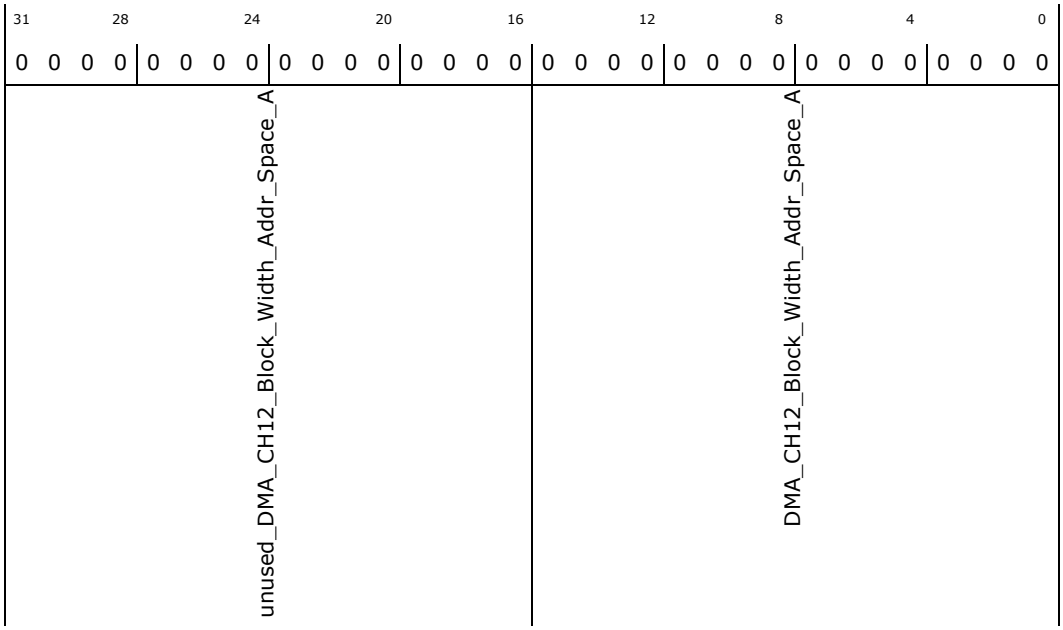
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41330h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH12_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH12_Block_Width_Addr_Space_A:** DMA CH 12 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.356 DMA_CH13_Block_Width_Addr_Space_A (isp_dma_DMA_CH13_Block_Width_Addr_Space_A)—Offset 41334h

DMA CH 13 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

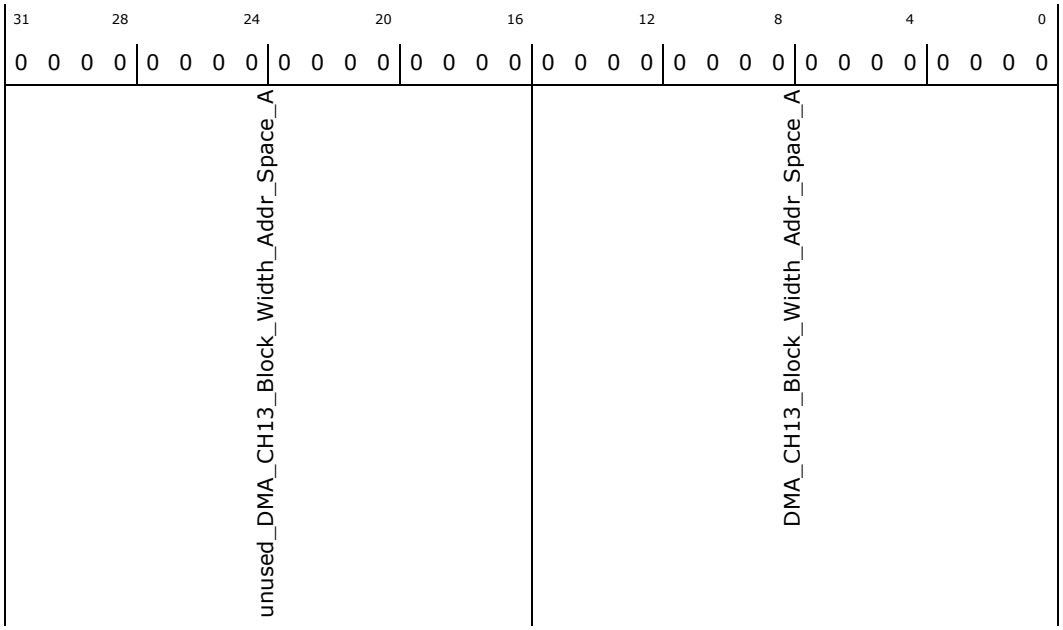
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41334h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH13_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH13_Block_Width_Addr_Space_A:** DMA CH 13 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.357 DMA_CH14_Block_Width_Addr_Space_A (isp_dma_DMA_CH14_Block_Width_Addr_Space_A)—Offset 41338h

DMA CH 14 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

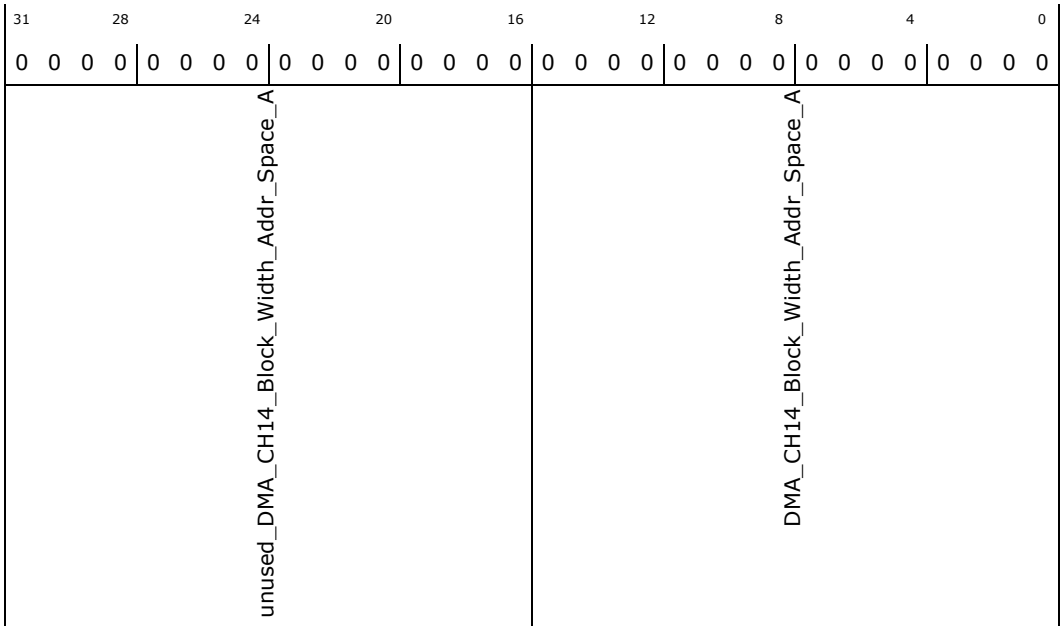
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41338h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH14_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH14_Block_Width_Addr_Space_A:** DMA CH 14 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.358 DMA_CH15_Block_Width_Addr_Space_A (isp_dma_DMA_CH15_Block_Width_Addr_Space_A)—Offset 4133Ch

DMA CH 15 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

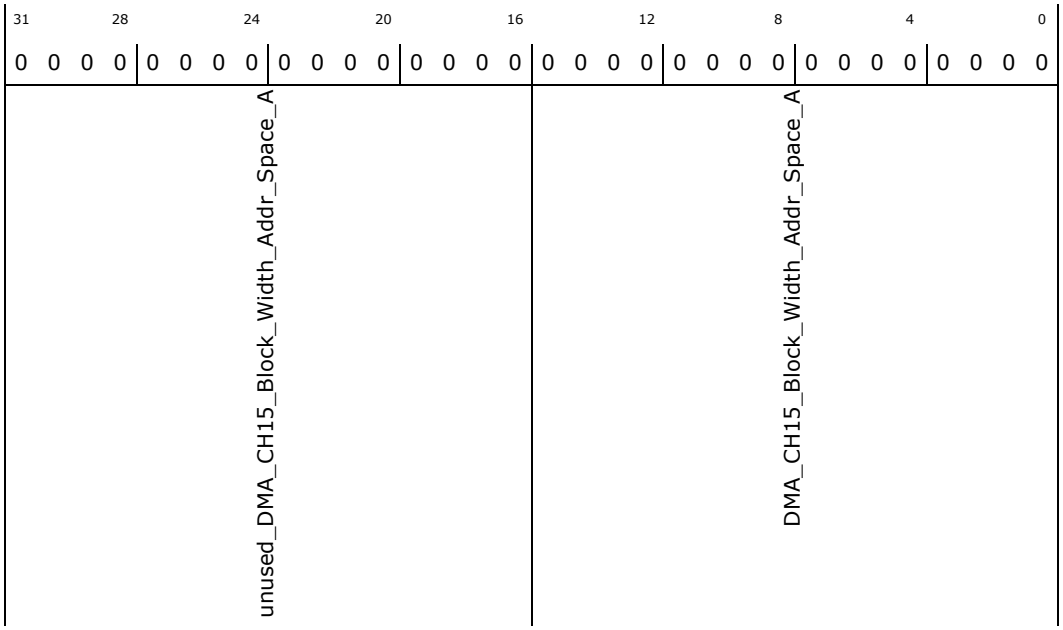
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4133Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH15_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH15_Block_Width_Addr_Space_A:** DMA CH 15 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.359 DMA_CH16_Block_Width_Addr_Space_A (isp_dma_DMA_CH16_Block_Width_Addr_Space_A)—Offset 41340h

DMA CH 16 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

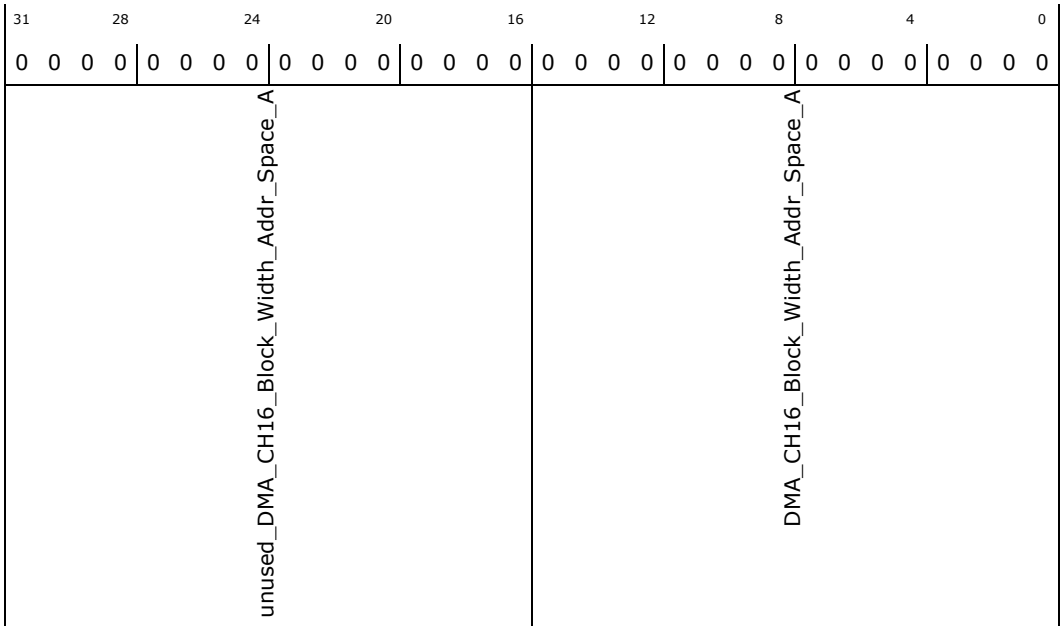
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41340h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH16_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH16_Block_Width_Addr_Space_A:** DMA CH 16 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.360 DMA_CH17_Block_Width_Addr_Space_A (isp_dma_DMA_CH17_Block_Width_Addr_Space_A)—Offset 41344h

DMA CH 17 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

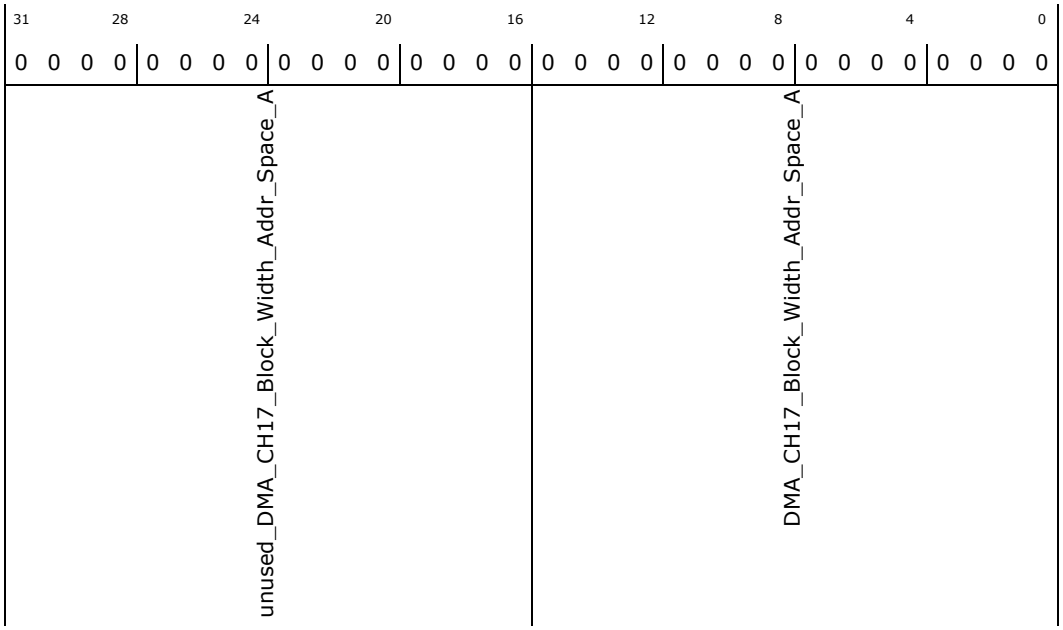
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41344h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH17_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH17_Block_Width_Addr_Space_A:** DMA CH 17 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.361 DMA_CH18_Block_Width_Addr_Space_A (isp_dma_DMA_CH18_Block_Width_Addr_Space_A)—Offset 41348h

DMA CH 18 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

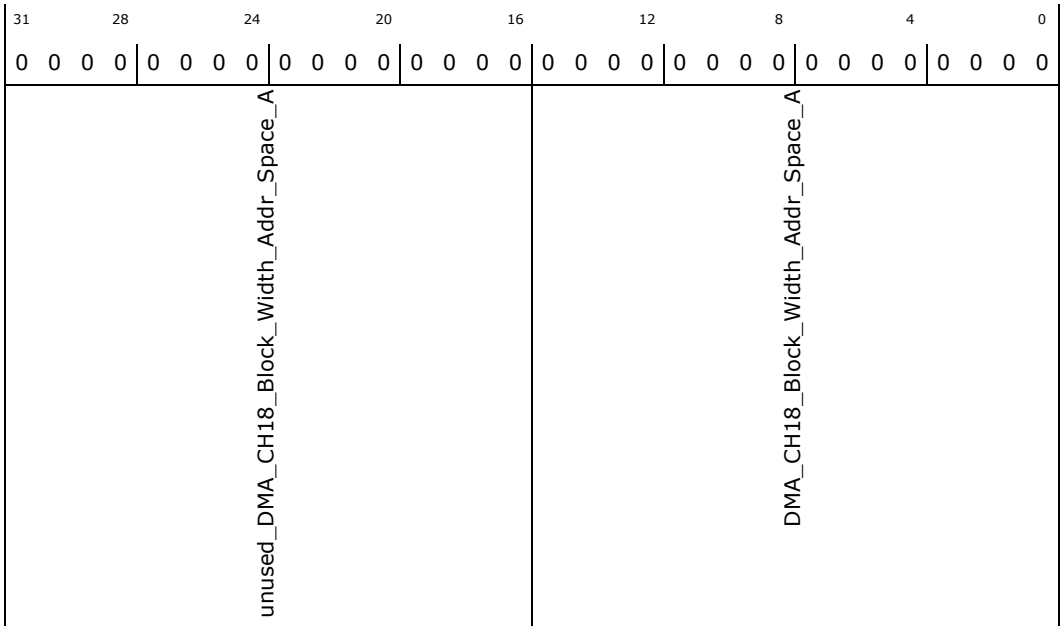
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41348h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH18_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH18_Block_Width_Addr_Space_A:** DMA CH 18 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.362 DMA_CH19_Block_Width_Addr_Space_A (isp_dma_DMA_CH19_Block_Width_Addr_Space_A)—Offset 4134Ch

DMA CH 19 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

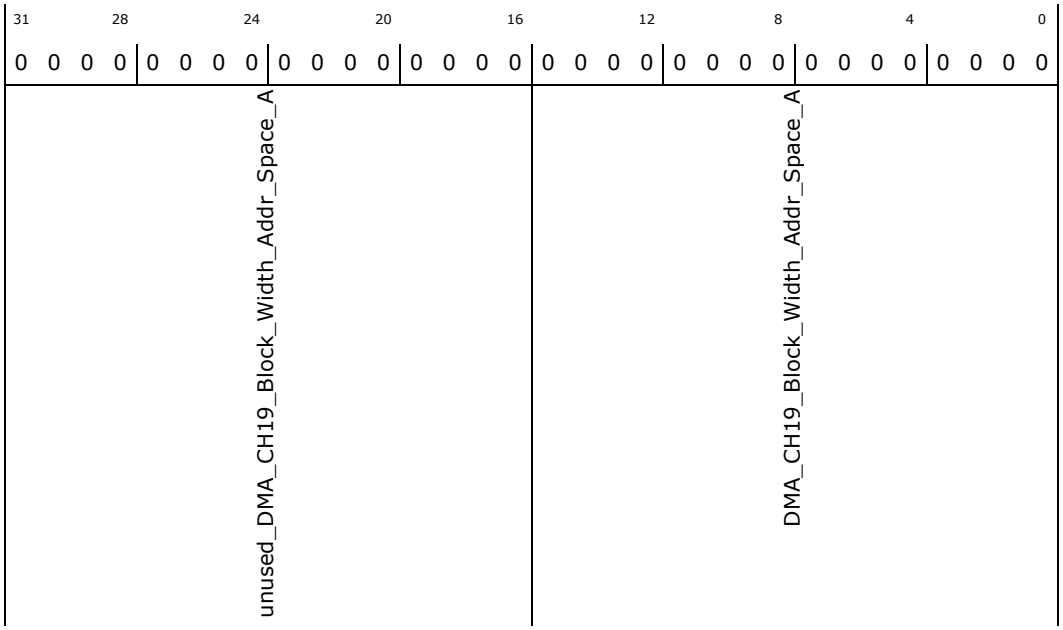
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4134Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH19_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH19_Block_Width_Addr_Space_A:** DMA CH 19 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.363 DMA_CH20_Block_Width_Addr_Space_A (isp_dma_DMA_CH20_Block_Width_Addr_Space_A)—Offset 41350h

DMA CH 20 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

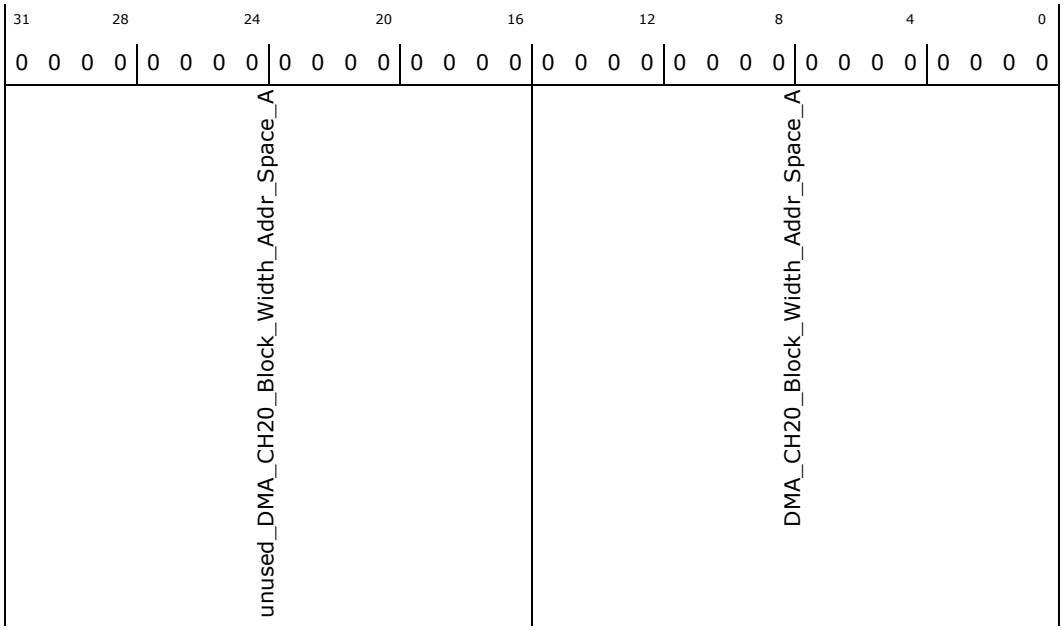
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41350h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH20_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH20_Block_Width_Addr_Space_A:** DMA CH 20 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.364 DMA_CH21_Block_Width_Addr_Space_A (isp_dma_DMA_CH21_Block_Width_Addr_Space_A)—Offset 41354h

DMA CH 21 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

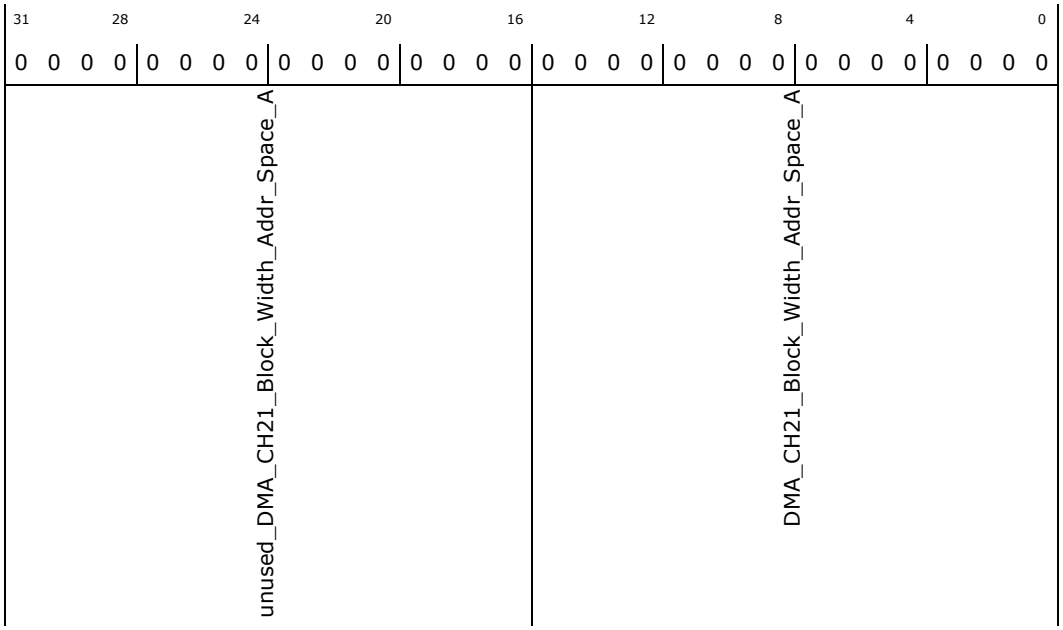
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41354h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH21_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH21_Block_Width_Addr_Space_A:** DMA CH 21 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.365 DMA_CH22_Block_Width_Addr_Space_A (isp_dma_DMA_CH22_Block_Width_Addr_Space_A)—Offset 41358h

DMA CH 22 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

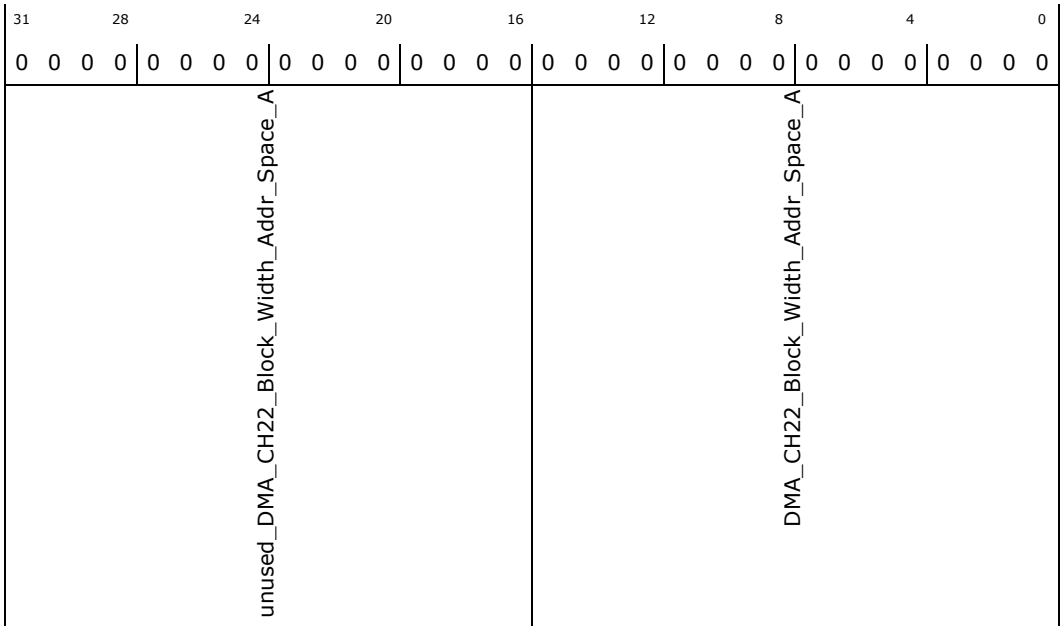
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41358h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH22_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH22_Block_Width_Addr_Space_A:** DMA CH 22 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.366 DMA_CH23_Block_Width_Addr_Space_A (isp_dma_DMA_CH23_Block_Width_Addr_Space_A)—Offset 4135Ch

DMA CH 23 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

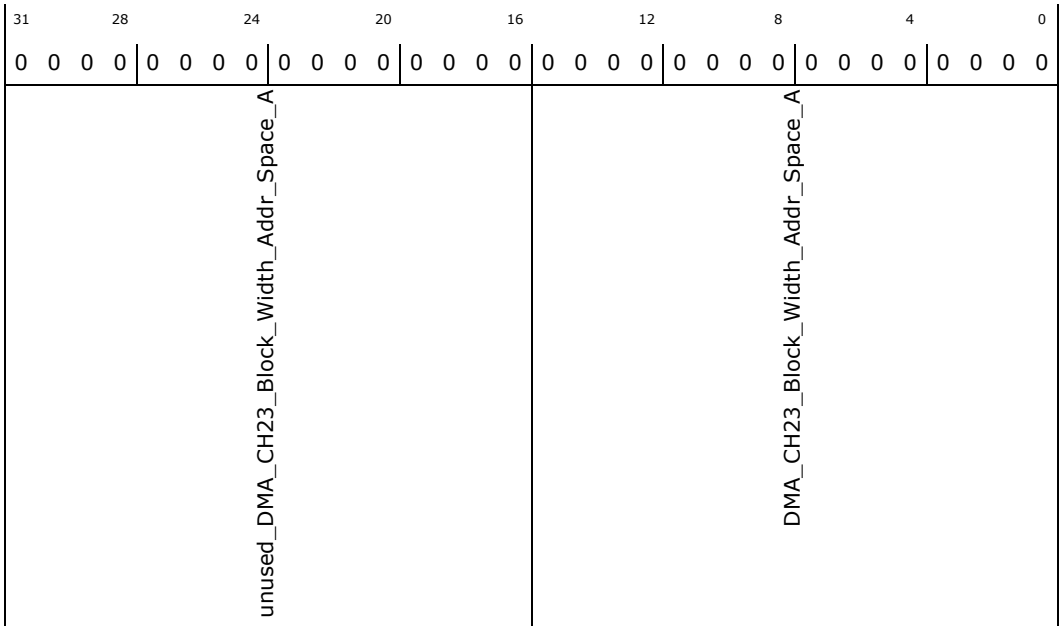
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4135Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH23_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH23_Block_Width_Addr_Space_A:** DMA CH 23 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.367 DMA_CH24_Block_Width_Addr_Space_A (isp_dma_DMA_CH24_Block_Width_Addr_Space_A)—Offset 41360h

DMA CH 24 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

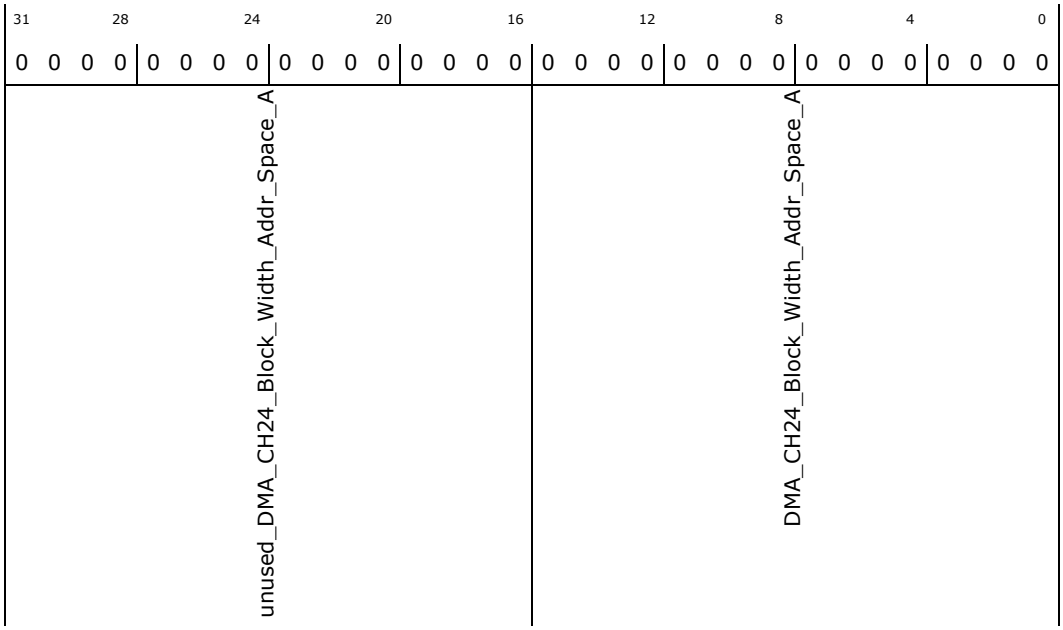
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41360h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH24_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH24_Block_Width_Addr_Space_A:** DMA CH 24 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.368 DMA_CH25_Block_Width_Addr_Space_A (isp_dma_DMA_CH25_Block_Width_Addr_Space_A)—Offset 41364h

DMA CH 25 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

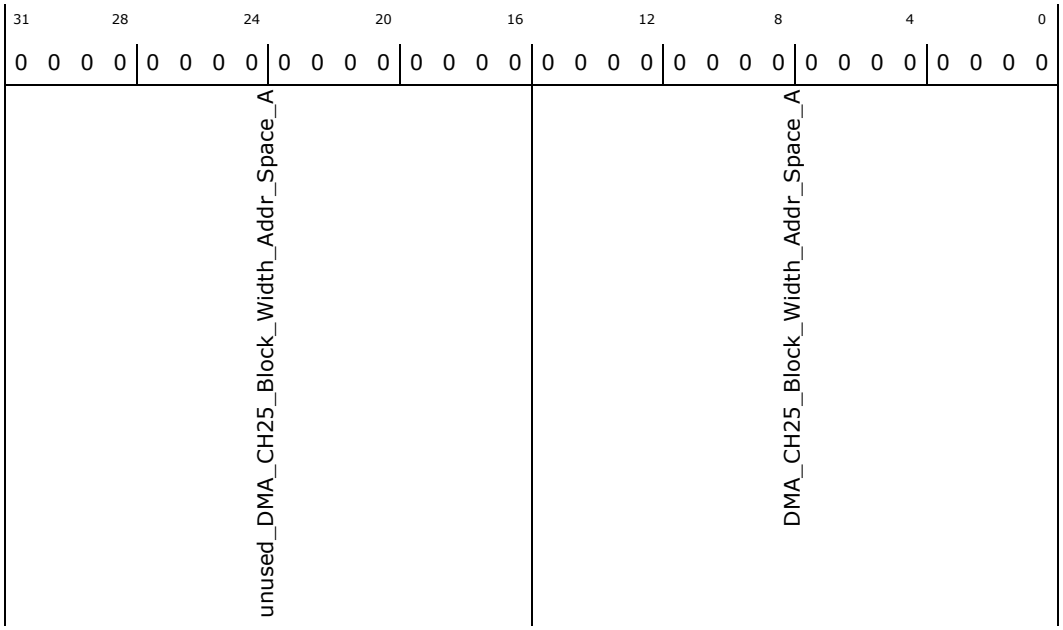
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41364h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH25_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH25_Block_Width_Addr_Space_A:** DMA CH 25 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.369 DMA_CH26_Block_Width_Addr_Space_A (isp_dma_DMA_CH26_Block_Width_Addr_Space_A)—Offset 41368h

DMA CH 26 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

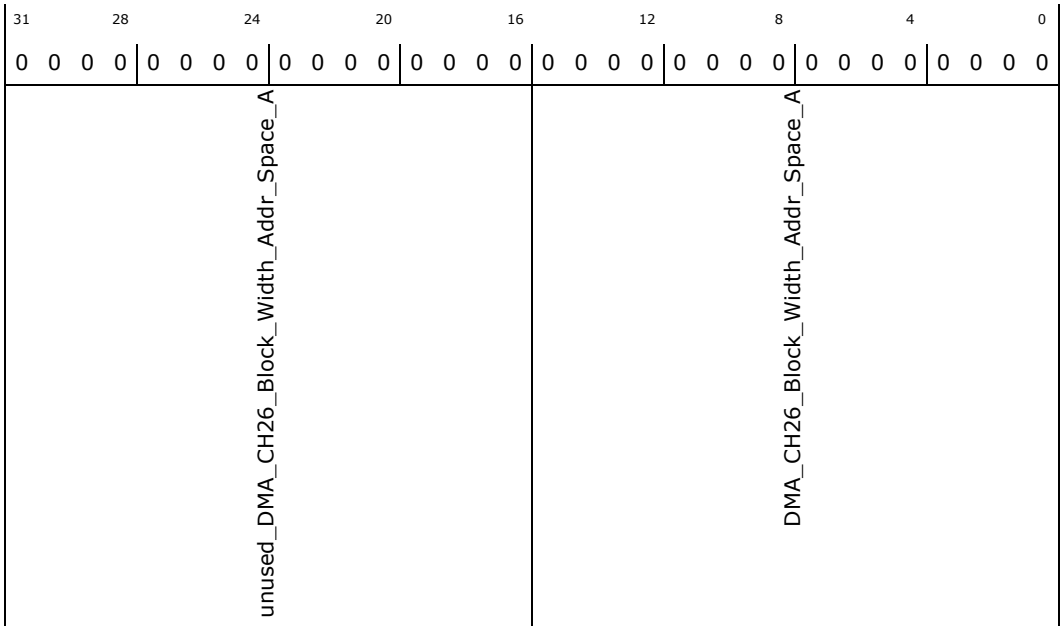
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41368h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH26_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH26_Block_Width_Addr_Space_A:** DMA CH 26 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.370 DMA_CH27_Block_Width_Addr_Space_A (isp_dma_DMA_CH27_Block_Width_Addr_Space_A)—Offset 4136Ch

DMA CH 27 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

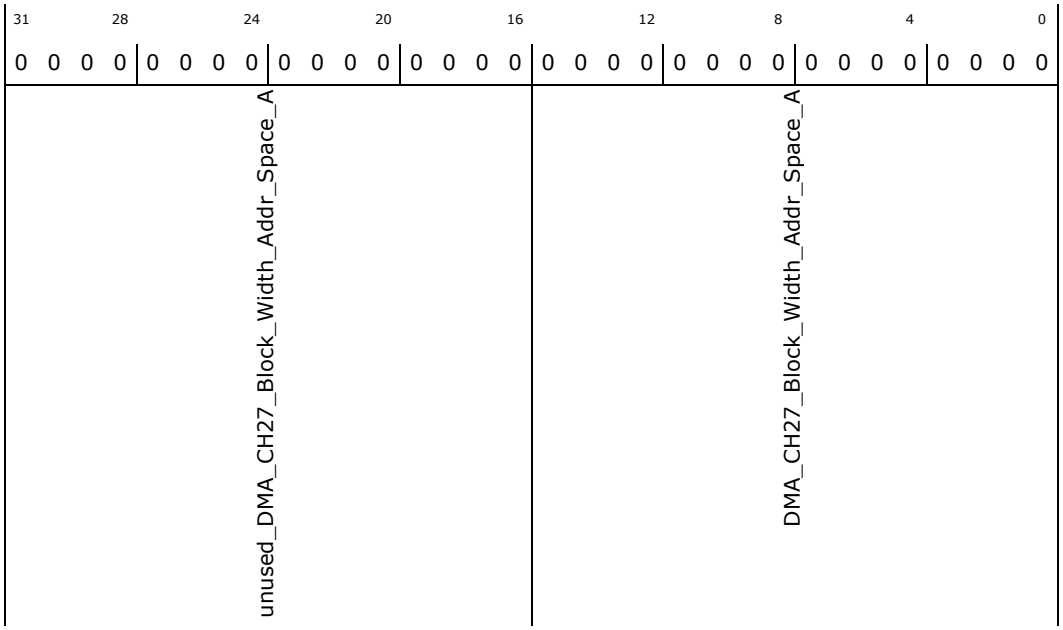
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4136Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH27_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH27_Block_Width_Addr_Space_A:** DMA CH 27 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.371 DMA_CH28_Block_Width_Addr_Space_A (isp_dma_DMA_CH28_Block_Width_Addr_Space_A)—Offset 41370h

DMA CH 28 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

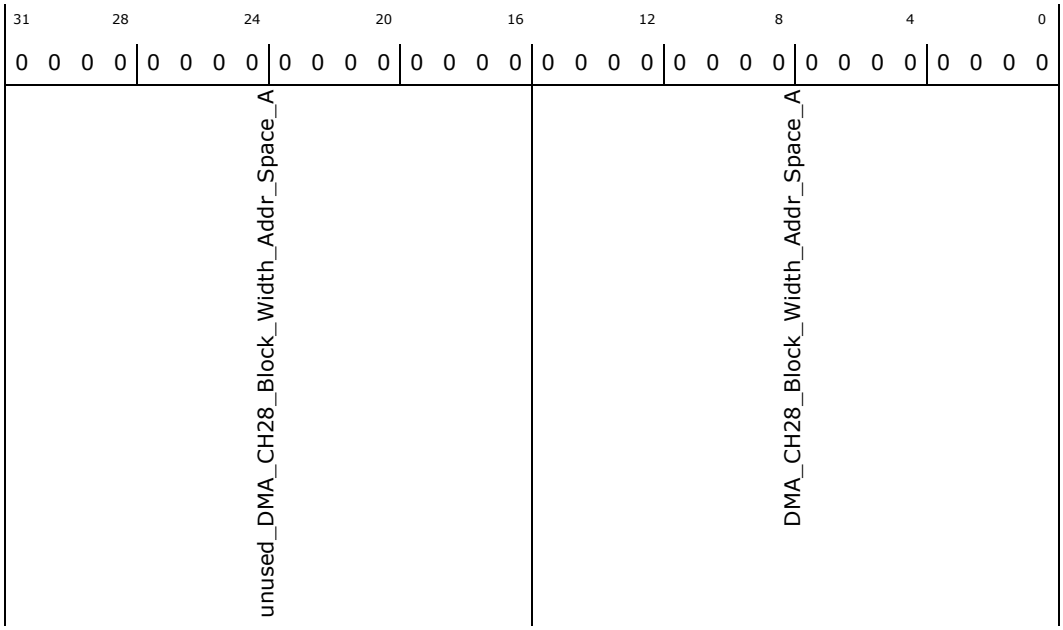
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41370h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH28_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH28_Block_Width_Addr_Space_A:** DMA CH 28 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.372 DMA_CH29_Block_Width_Addr_Space_A (isp_dma_DMA_CH29_Block_Width_Addr_Space_A)—Offset 41374h

DMA CH 29 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

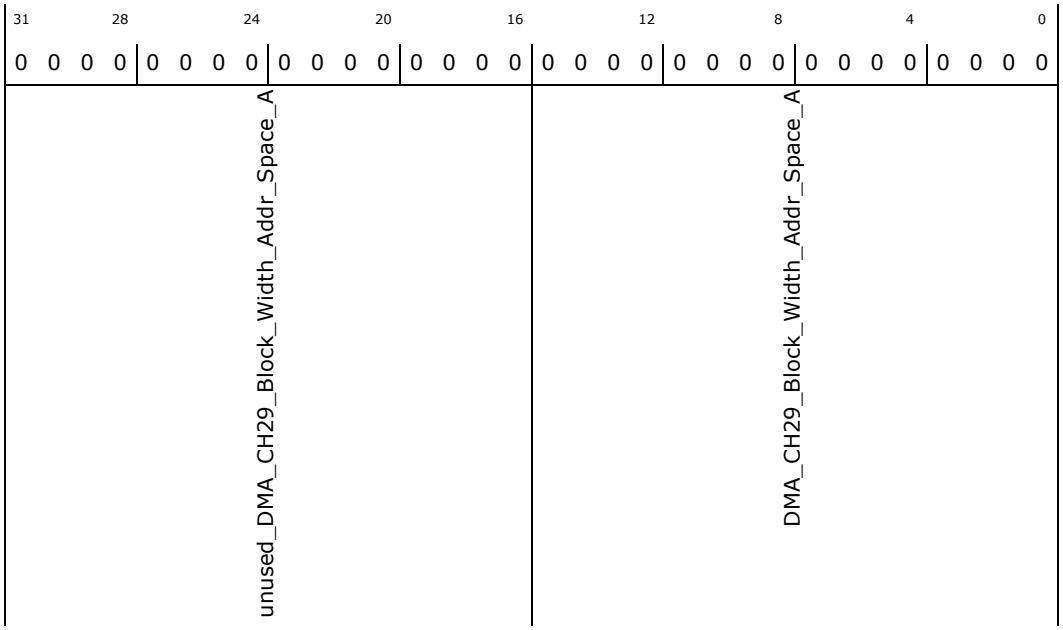
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41374h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH29_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH29_Block_Width_Addr_Space_A:** DMA CH 29 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.373 DMA_CH30_Block_Width_Addr_Space_A (isp_dma_DMA_CH30_Block_Width_Addr_Space_A)—Offset 41378h

DMA CH 30 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

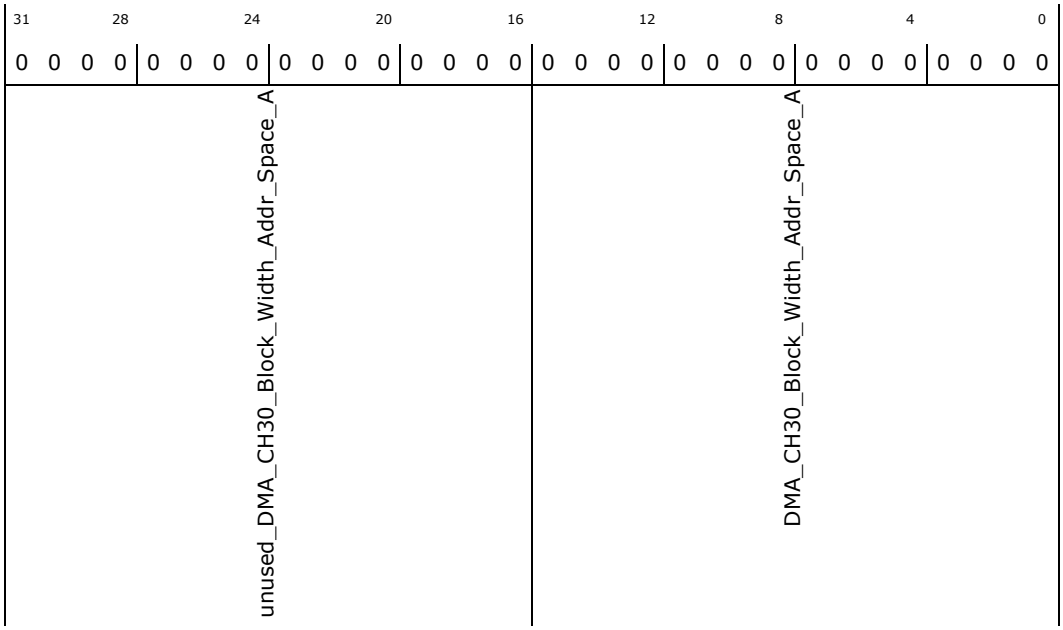
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41378h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH30_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH30_Block_Width_Addr_Space_A:** DMA CH 30 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.374 DMA_CH31_Block_Width_Addr_Space_A (isp_dma_DMA_CH31_Block_Width_Addr_Space_A)—Offset 4137Ch

DMA CH 31 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

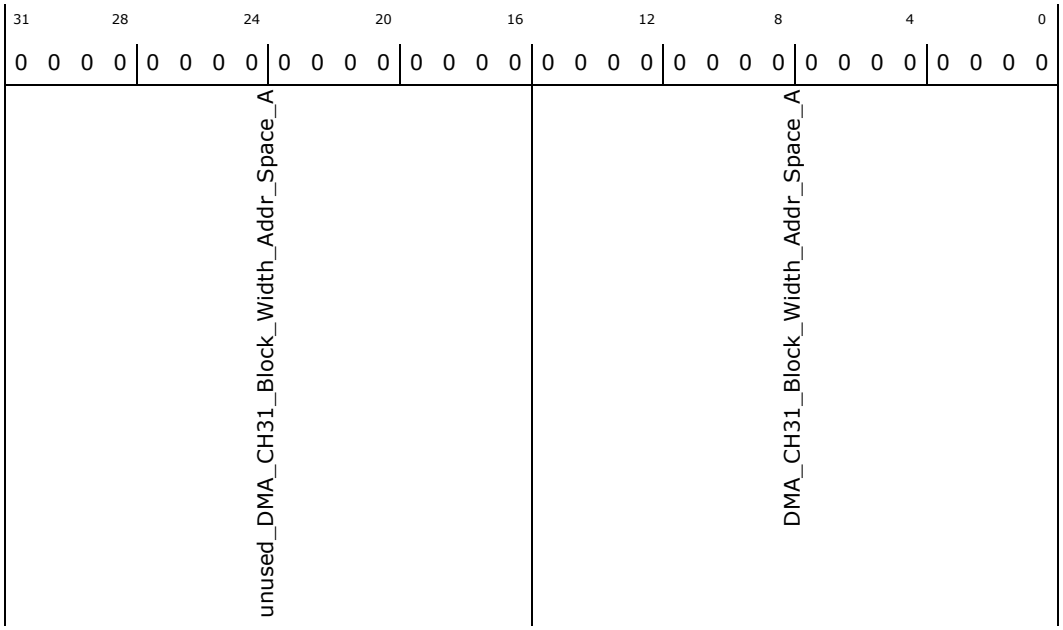
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4137Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH31_Block_Width_Addr_Space_A):** Unused
15:0	0x0 RO	**DMA_CH31_Block_Width_Addr_Space_A:** DMA CH 31 PARAM 3: Block Width (Xb) for Device A side of the connection in terms of Device A words.

5.2.375 DMA_CH0_Stride_Addr_Space_B (isp_dma_DMA_CH0_Stride_Addr_Space_B)—Offset 41400h

DMA CH 0 PARAM 4: Line Stride for Device B side of the connection.

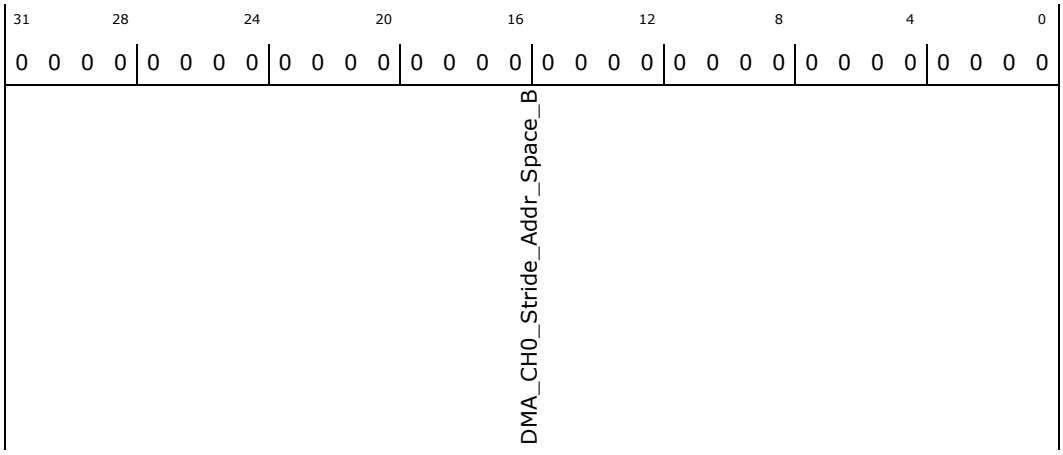
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41400h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH0_Stride_Addr_Space_B:** DMA CH 0 PARAM 4: Line Stride for Device B side of the connection.

5.2.376 DMA_CH1_Stride_Addr_Space_B (isp_dma_DMA_CH1_Stride_Addr_Space_B)—Offset 41404h

DMA CH 1 PARAM 4: Line Stride for Device B side of the connection.

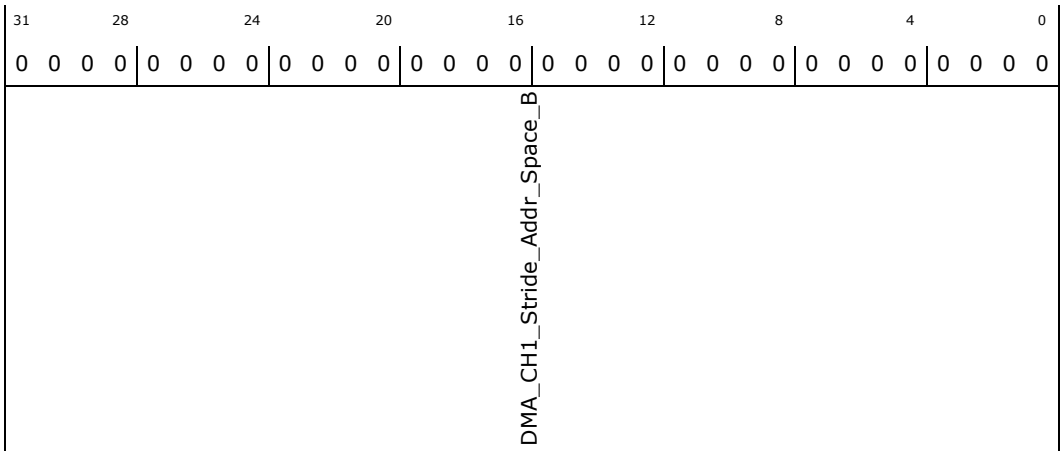
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41404h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH1_Stride_Addr_Space_B:** DMA CH 1 PARAM 4: Line Stride for Device B side of the connection.

5.2.377 DMA_CH2_Stride_Addr_Space_B (isp_dma_DMA_CH2_Stride_Addr_Space_B)—Offset 41408h

DMA CH 2 PARAM 4: Line Stride for Device B side of the connection.

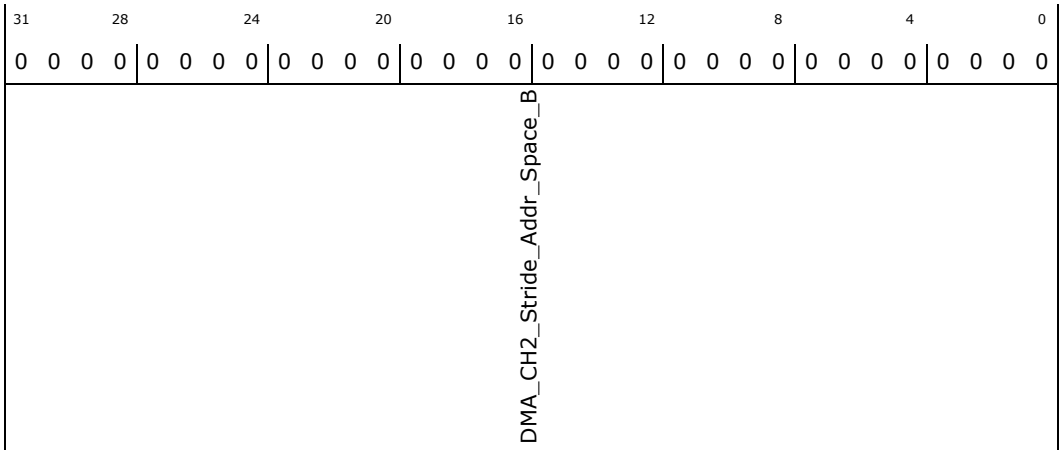
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41408h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH2_Stride_Addr_Space_B:** DMA CH 2 PARAM 4: Line Stride for Device B side of the connection.

5.2.378 DMA_CH3_Stride_Addr_Space_B (isp_dma_DMA_CH3_Stride_Addr_Space_B)—Offset 4140Ch

DMA CH 3 PARAM 4: Line Stride for Device B side of the connection.

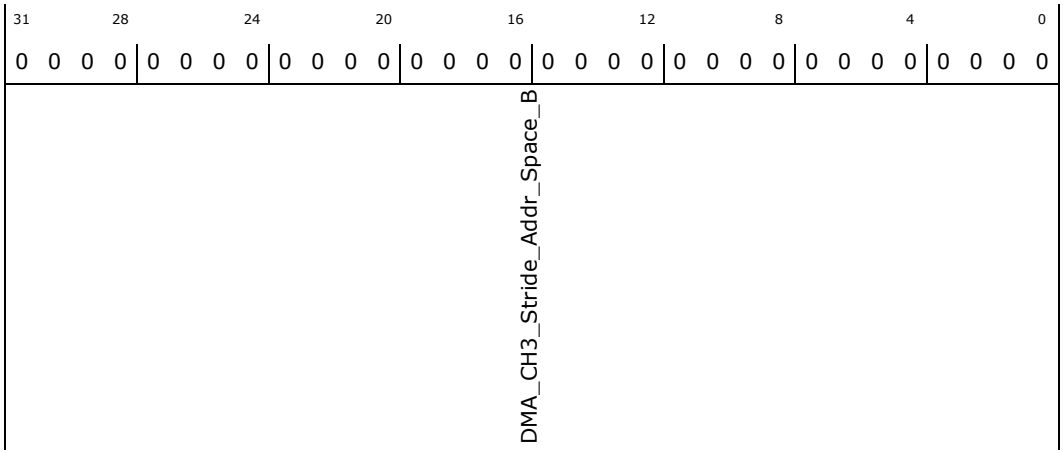
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4140Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH3_Stride_Addr_Space_B:** DMA CH 3 PARAM 4: Line Stride for Device B side of the connection.

5.2.379 DMA_CH4_Stride_Addr_Space_B (isp_dma_DMA_CH4_Stride_Addr_Space_B)—Offset 41410h

DMA CH 4 PARAM 4: Line Stride for Device B side of the connection.

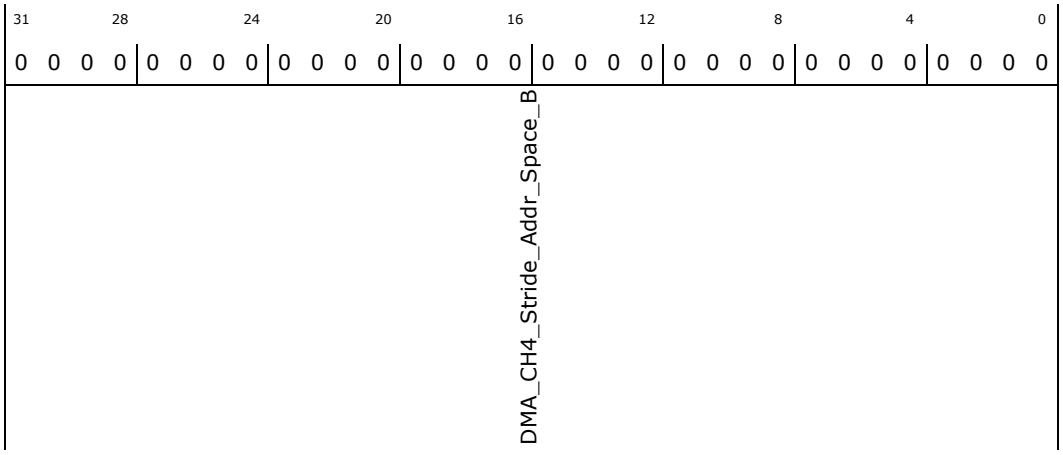
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41410h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH4_Stride_Addr_Space_B:** DMA CH 4 PARAM 4: Line Stride for Device B side of the connection.

5.2.380 DMA_CH5_Stride_Addr_Space_B (isp_dma_DMA_CH5_Stride_Addr_Space_B)—Offset 41414h

DMA CH 5 PARAM 4: Line Stride for Device B side of the connection.

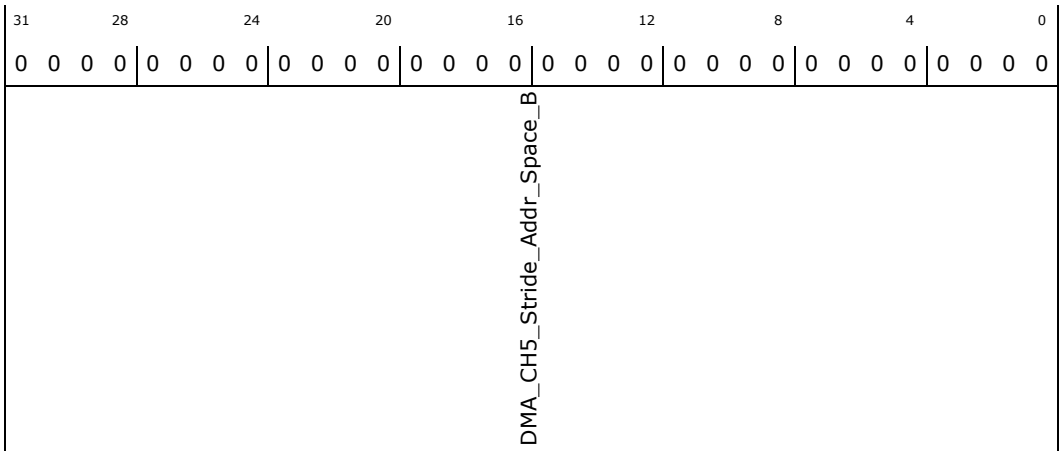
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41414h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH5_Stride_Addr_Space_B:** DMA CH 5 PARAM 4: Line Stride for Device B side of the connection.

5.2.381 DMA_CH6_Stride_Addr_Space_B (isp_dma_DMA_CH6_Stride_Addr_Space_B)—Offset 41418h

DMA CH 6 PARAM 4: Line Stride for Device B side of the connection.

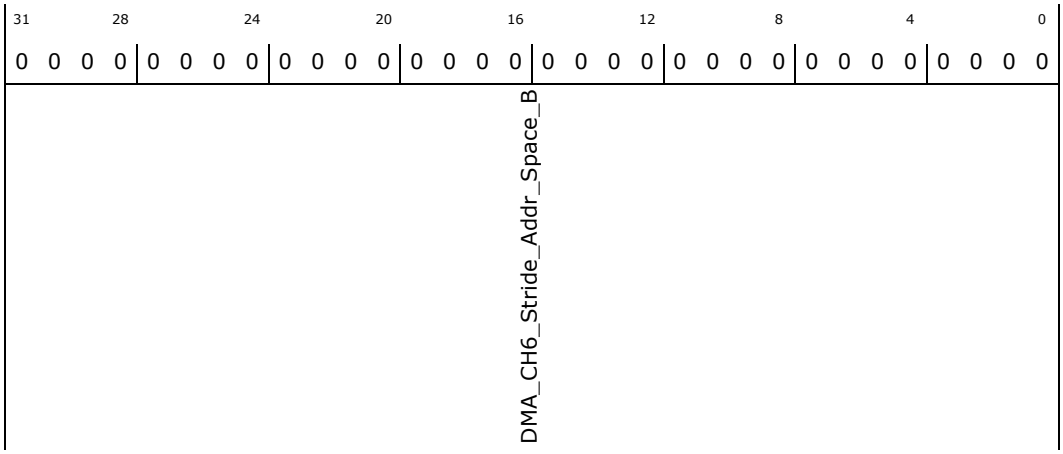
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41418h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH6_Stride_Addr_Space_B:** DMA CH 6 PARAM 4: Line Stride for Device B side of the connection.

5.2.382 DMA_CH7_Stride_Addr_Space_B (isp_dma_DMA_CH7_Stride_Addr_Space_B)—Offset 4141Ch

DMA CH 7 PARAM 4: Line Stride for Device B side of the connection.

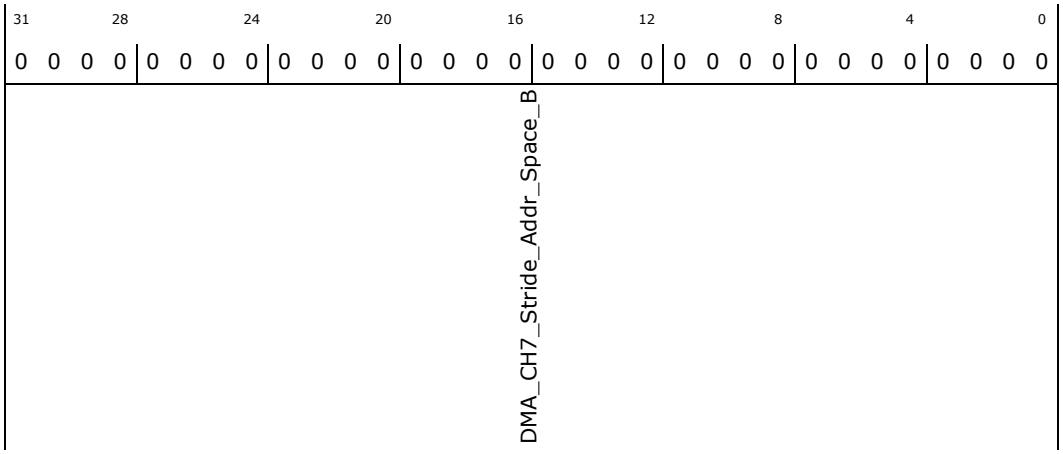
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4141Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH7_Stride_Addr_Space_B:** DMA CH 7 PARAM 4: Line Stride for Device B side of the connection.

5.2.383 DMA_CH8_Stride_Addr_Space_B (isp_dma_DMA_CH8_Stride_Addr_Space_B)—Offset 41420h

DMA CH 8 PARAM 4: Line Stride for Device B side of the connection.

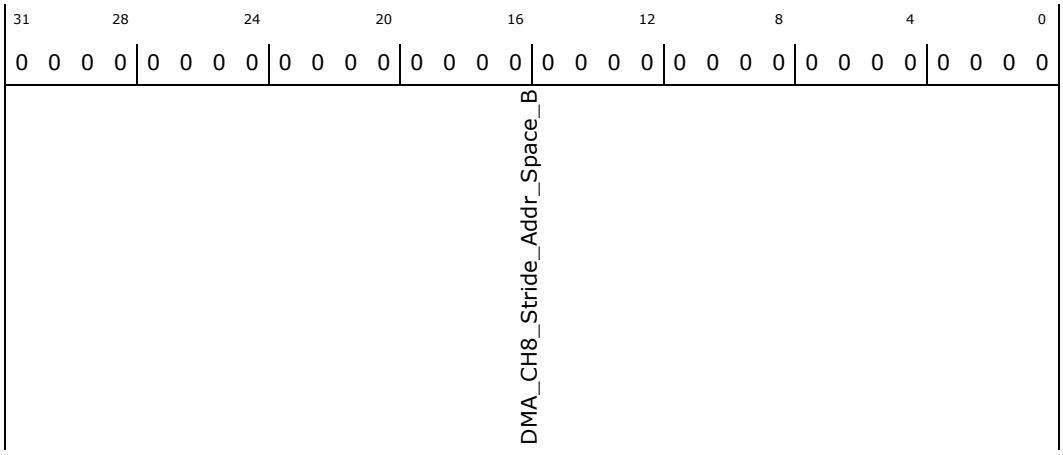
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41420h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH8_Stride_Addr_Space_B:** DMA CH 8 PARAM 4: Line Stride for Device B side of the connection.

5.2.384 DMA_CH9_Stride_Addr_Space_B (isp_dma_DMA_CH9_Stride_Addr_Space_B)—Offset 41424h

DMA CH 9 PARAM 4: Line Stride for Device B side of the connection.

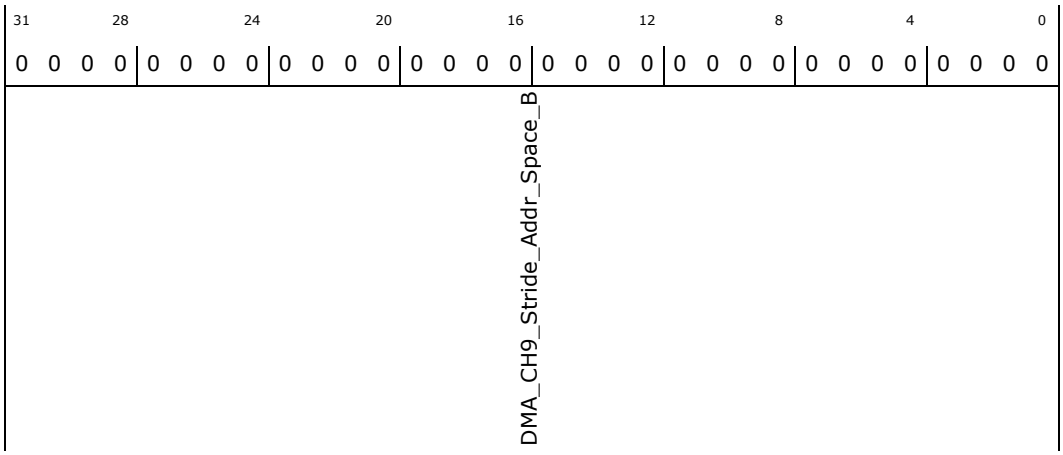
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41424h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH9_Stride_Addr_Space_B:** DMA CH 9 PARAM 4: Line Stride for Device B side of the connection.

5.2.385 DMA_CH10_Stride_Addr_Space_B (isp_dma_DMA_CH10_Stride_Addr_Space_B)—Offset 41428h

DMA CH 10 PARAM 4: Line Stride for Device B side of the connection.

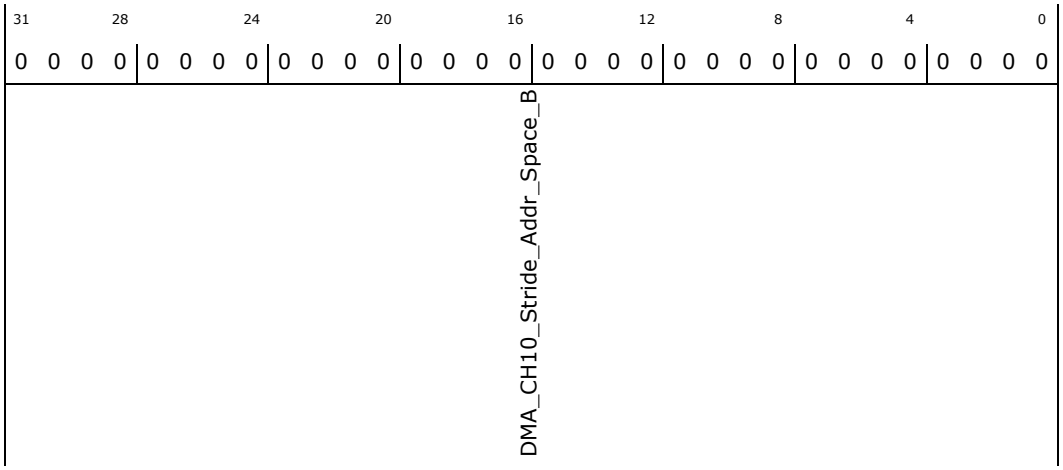
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41428h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH10_Stride_Addr_Space_B:** DMA CH 10 PARAM 4: Line Stride for Device B side of the connection.

5.2.386 DMA_CH11_Stride_Addr_Space_B (isp_dma_DMA_CH11_Stride_Addr_Space_B)—Offset 4142Ch

DMA CH 11 PARAM 4: Line Stride for Device B side of the connection.

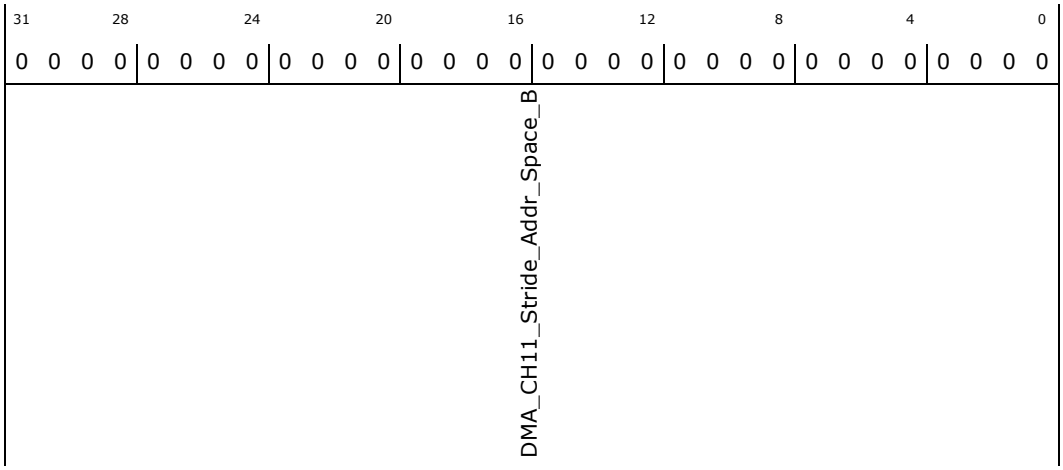
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4142Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH11_Stride_Addr_Space_B:** DMA CH 11 PARAM 4: Line Stride for Device B side of the connection.

5.2.387 DMA_CH12_Stride_Addr_Space_B (isp_dma_DMA_CH12_Stride_Addr_Space_B)—Offset 41430h

DMA CH 12 PARAM 4: Line Stride for Device B side of the connection.

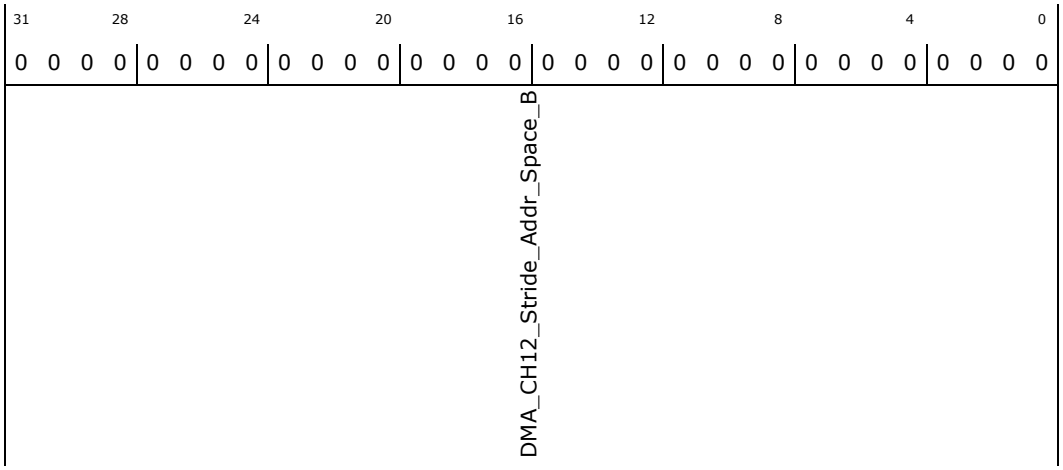
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41430h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH12_Stride_Addr_Space_B:** DMA CH 12 PARAM 4: Line Stride for Device B side of the connection.

5.2.388 DMA_CH13_Stride_Addr_Space_B (isp_dma_DMA_CH13_Stride_Addr_Space_B)—Offset 41434h

DMA CH 13 PARAM 4: Line Stride for Device B side of the connection.

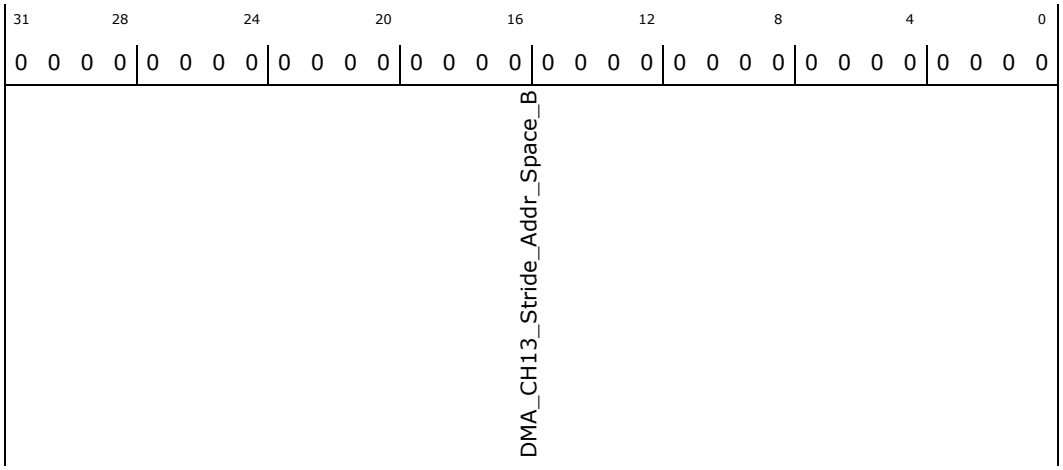
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41434h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH13_Stride_Addr_Space_B:** DMA CH 13 PARAM 4: Line Stride for Device B side of the connection.

5.2.389 DMA_CH14_Stride_Addr_Space_B (isp_dma_DMA_CH14_Stride_Addr_Space_B)—Offset 41438h

DMA CH 14 PARAM 4: Line Stride for Device B side of the connection.

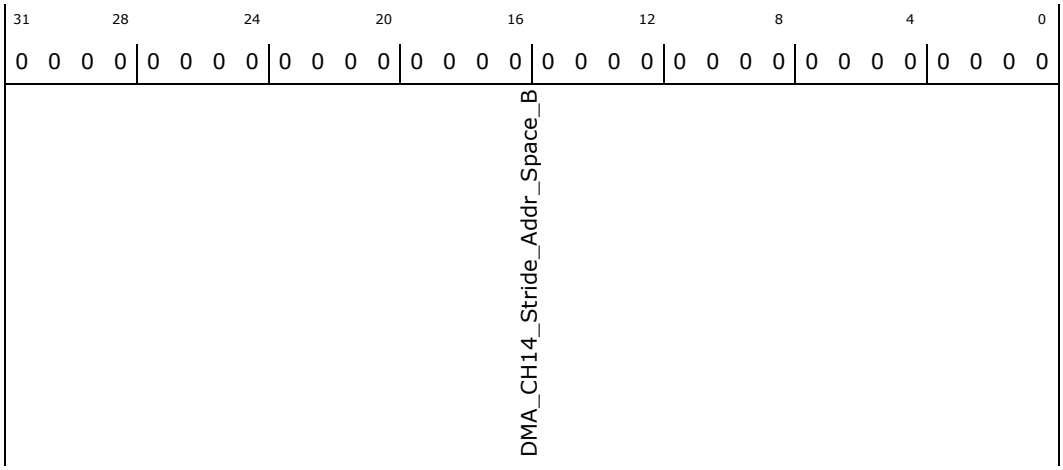
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41438h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH14_Stride_Addr_Space_B:** DMA CH 14 PARAM 4: Line Stride for Device B side of the connection.

5.2.390 DMA_CH15_Stride_Addr_Space_B (isp_dma_DMA_CH15_Stride_Addr_Space_B)—Offset 4143Ch

DMA CH 15 PARAM 4: Line Stride for Device B side of the connection.

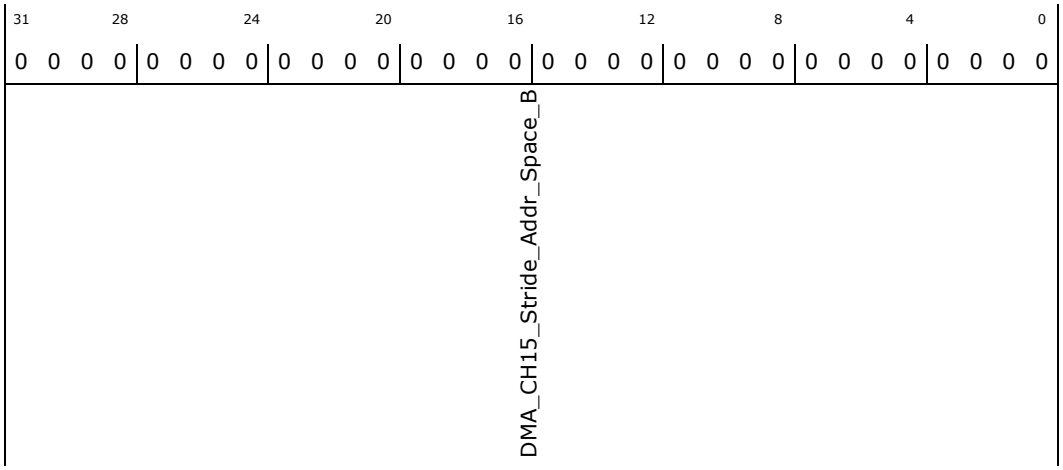
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4143Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH15_Stride_Addr_Space_B:** DMA CH 15 PARAM 4: Line Stride for Device B side of the connection.

5.2.391 DMA_CH16_Stride_Addr_Space_B (isp_dma_DMA_CH16_Stride_Addr_Space_B)—Offset 41440h

DMA CH 16 PARAM 4: Line Stride for Device B side of the connection.

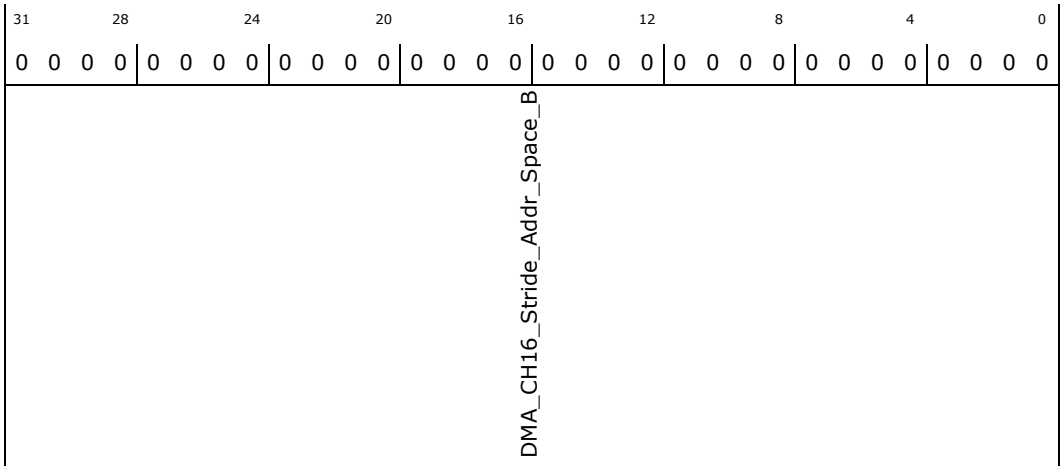
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41440h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH16_Stride_Addr_Space_B:** DMA CH 16 PARAM 4: Line Stride for Device B side of the connection.

5.2.392 DMA_CH17_Stride_Addr_Space_B (isp_dma_DMA_CH17_Stride_Addr_Space_B)—Offset 41444h

DMA CH 17 PARAM 4: Line Stride for Device B side of the connection.

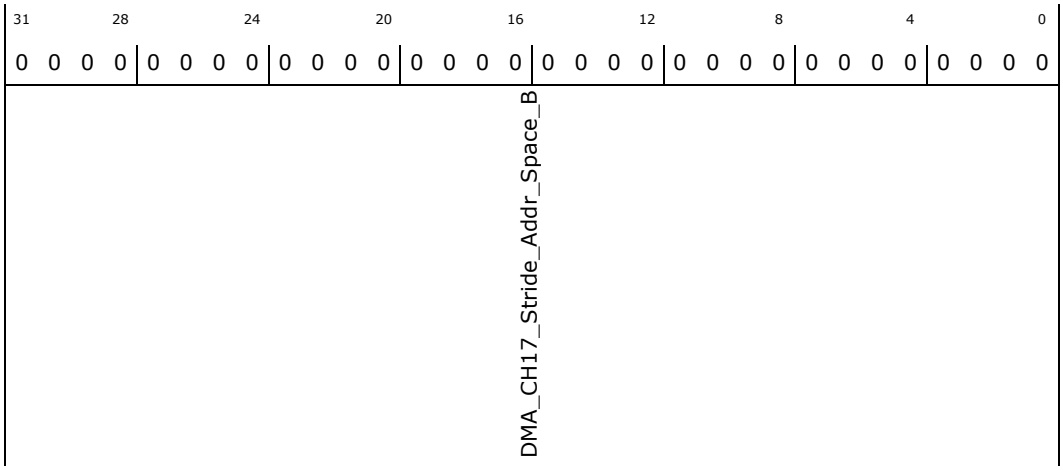
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41444h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH17_Stride_Addr_Space_B:** DMA CH 17 PARAM 4: Line Stride for Device B side of the connection.

5.2.393 DMA_CH18_Stride_Addr_Space_B (isp_dma_DMA_CH18_Stride_Addr_Space_B)—Offset 41448h

DMA CH 18 PARAM 4: Line Stride for Device B side of the connection.

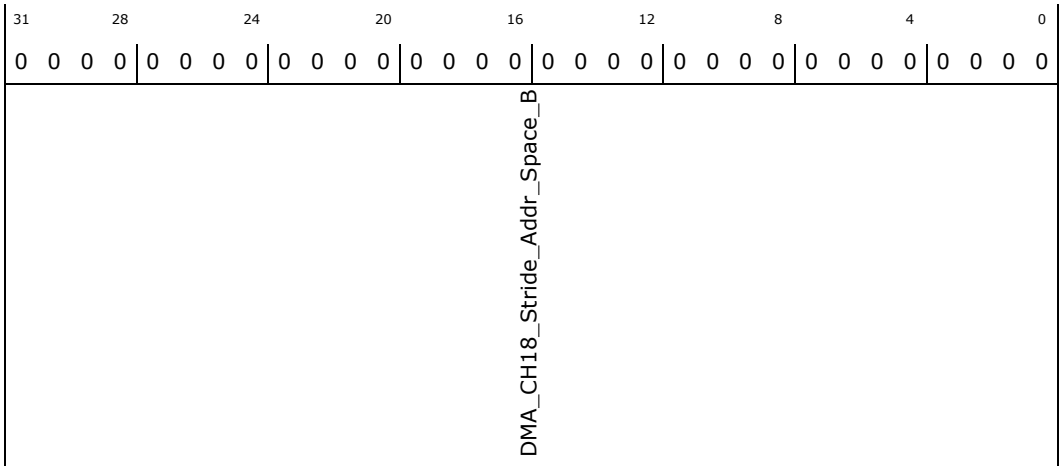
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41448h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH18_Stride_Addr_Space_B:** DMA CH 18 PARAM 4: Line Stride for Device B side of the connection.

5.2.394 DMA_CH19_Stride_Addr_Space_B (isp_dma_DMA_CH19_Stride_Addr_Space_B)—Offset 4144Ch

DMA CH 19 PARAM 4: Line Stride for Device B side of the connection.

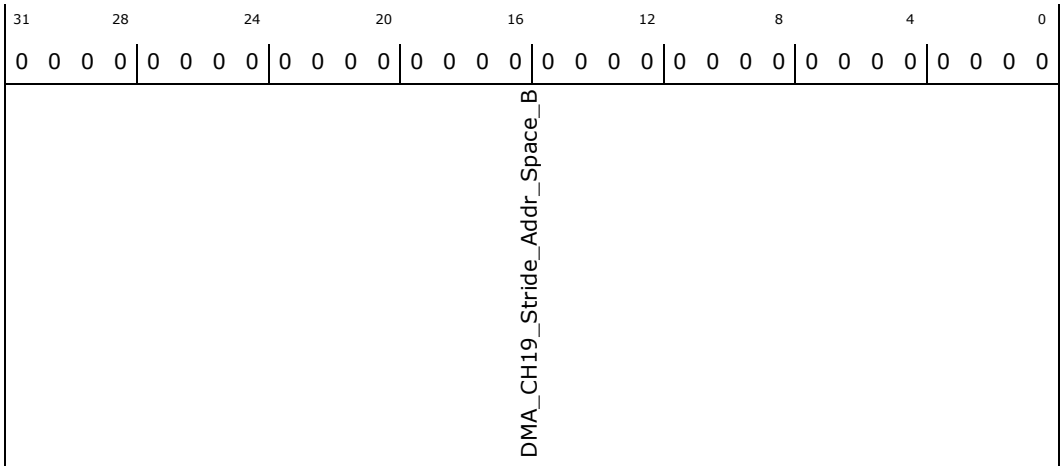
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4144Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH19_Stride_Addr_Space_B:** DMA CH 19 PARAM 4: Line Stride for Device B side of the connection.

5.2.395 DMA_CH20_Stride_Addr_Space_B (isp_dma_DMA_CH20_Stride_Addr_Space_B)—Offset 41450h

DMA CH 20 PARAM 4: Line Stride for Device B side of the connection.

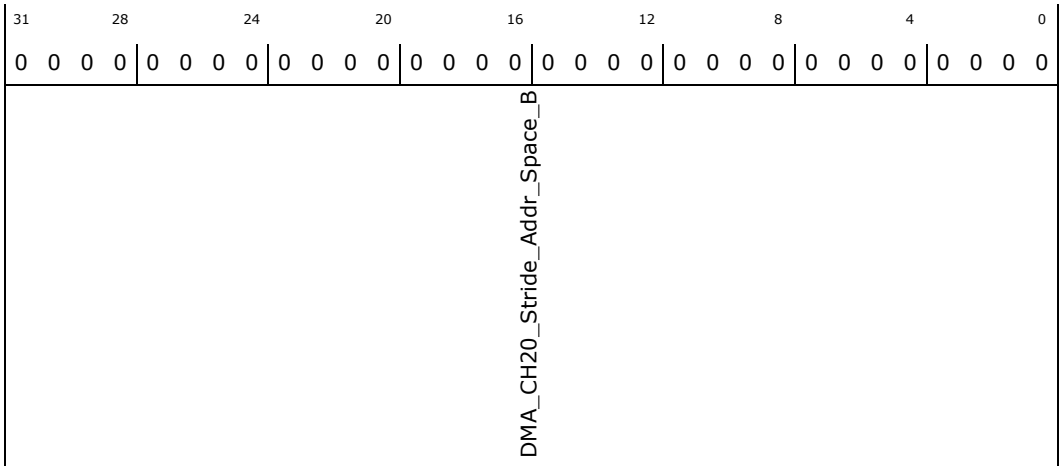
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41450h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH20_Stride_Addr_Space_B:** DMA CH 20 PARAM 4: Line Stride for Device B side of the connection.

5.2.396 DMA_CH21_Stride_Addr_Space_B (isp_dma_DMA_CH21_Stride_Addr_Space_B)—Offset 41454h

DMA CH 21 PARAM 4: Line Stride for Device B side of the connection.

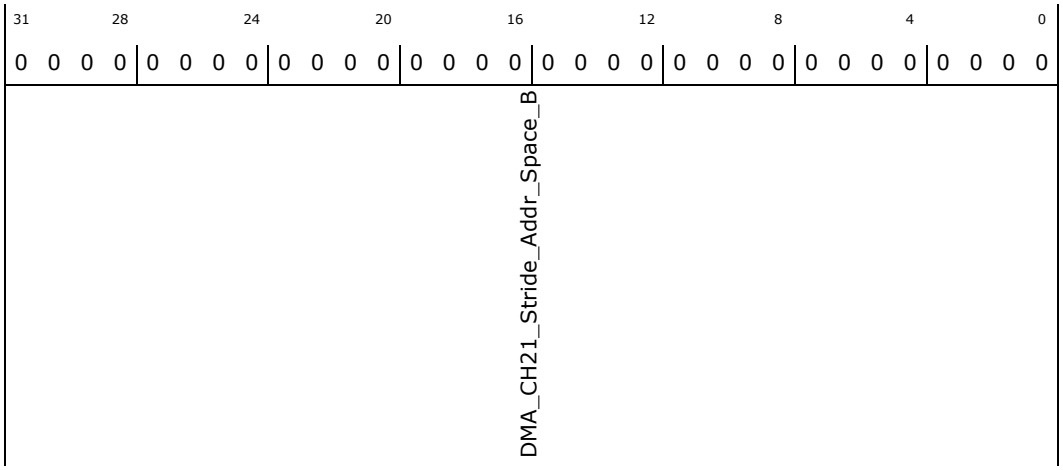
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41454h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH21_Stride_Addr_Space_B:** DMA CH 21 PARAM 4: Line Stride for Device B side of the connection.

5.2.397 DMA_CH22_Stride_Addr_Space_B (isp_dma_DMA_CH22_Stride_Addr_Space_B)—Offset 41458h

DMA CH 22 PARAM 4: Line Stride for Device B side of the connection.

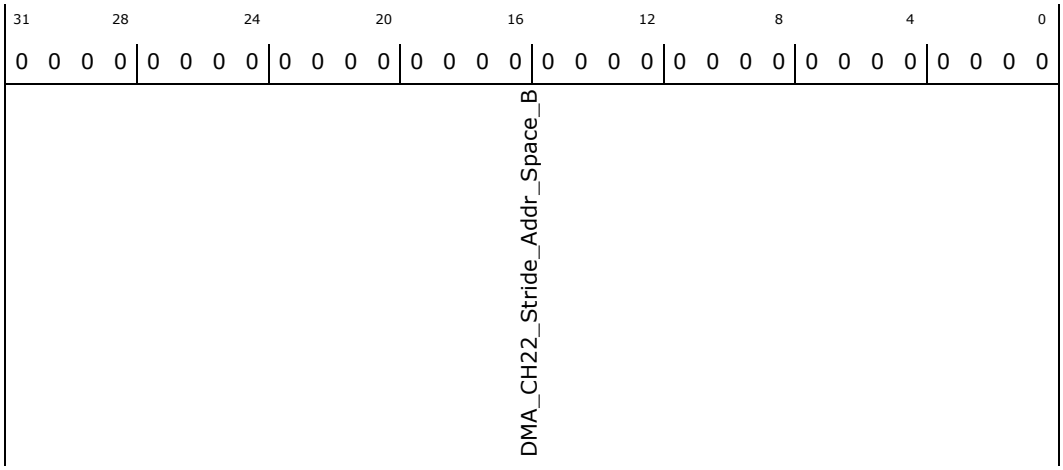
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41458h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH22_Stride_Addr_Space_B:** DMA CH 22 PARAM 4: Line Stride for Device B side of the connection.

5.2.398 DMA_CH23_Stride_Addr_Space_B (isp_dma_DMA_CH23_Stride_Addr_Space_B)—Offset 4145Ch

DMA CH 23 PARAM 4: Line Stride for Device B side of the connection.

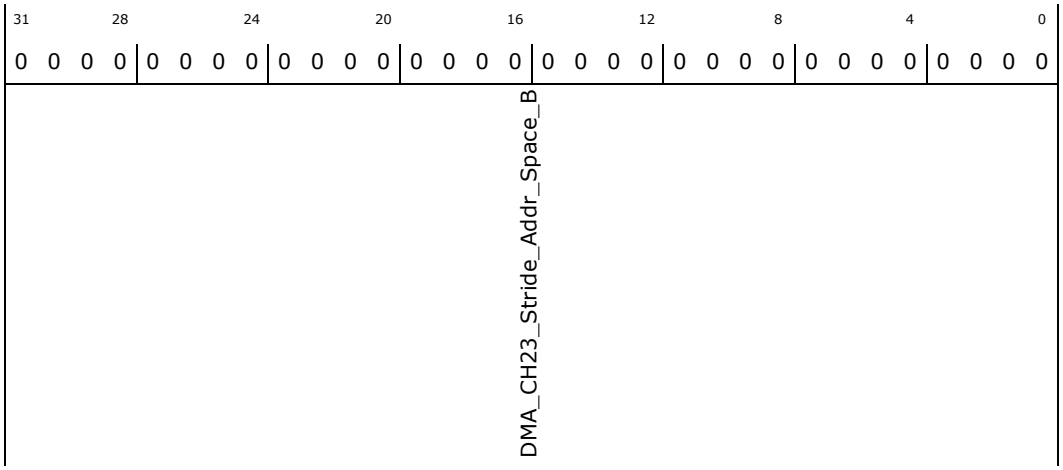
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4145Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH23_Stride_Addr_Space_B:** DMA CH 23 PARAM 4: Line Stride for Device B side of the connection.

5.2.399 DMA_CH24_Stride_Addr_Space_B (isp_dma_DMA_CH24_Stride_Addr_Space_B)—Offset 41460h

DMA CH 24 PARAM 4: Line Stride for Device B side of the connection.

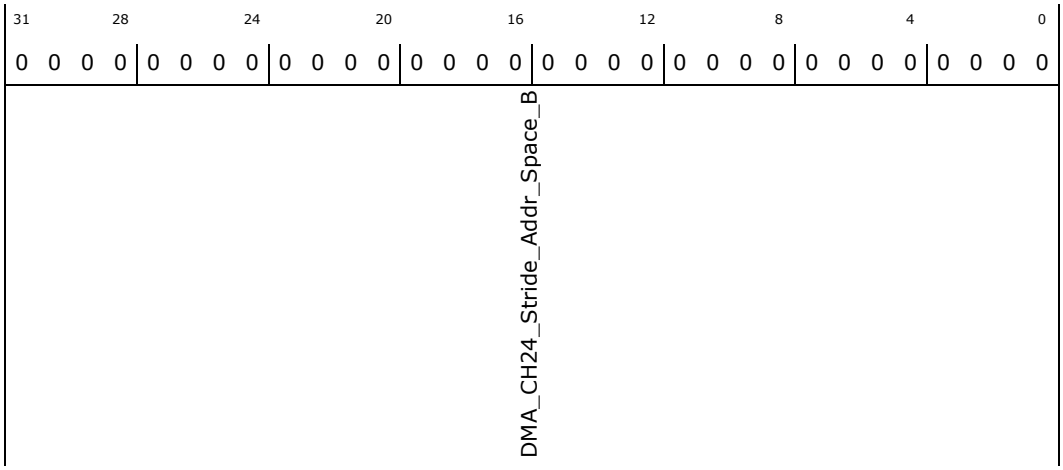
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41460h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH24_Stride_Addr_Space_B:** DMA CH 24 PARAM 4: Line Stride for Device B side of the connection.

5.2.400 DMA_CH25_Stride_Addr_Space_B (isp_dma_DMA_CH25_Stride_Addr_Space_B)—Offset 41464h

DMA CH 25 PARAM 4: Line Stride for Device B side of the connection.

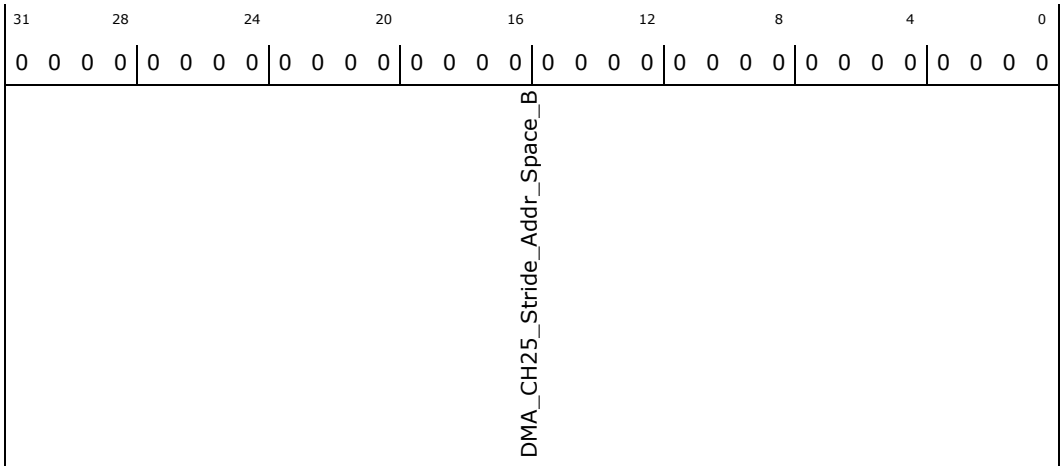
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41464h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH25_Stride_Addr_Space_B:** DMA CH 25 PARAM 4: Line Stride for Device B side of the connection.

5.2.401 DMA_CH26_Stride_Addr_Space_B (isp_dma_DMA_CH26_Stride_Addr_Space_B)—Offset 41468h

DMA CH 26 PARAM 4: Line Stride for Device B side of the connection.

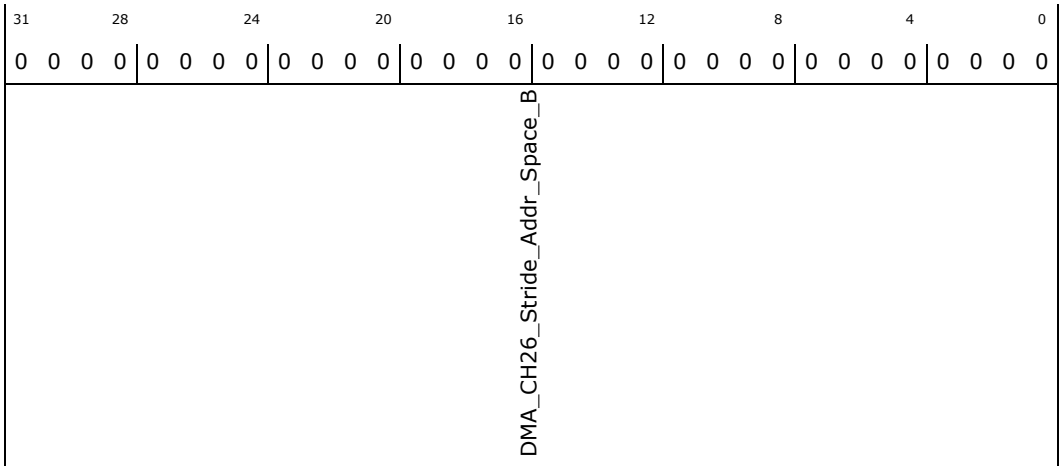
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41468h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH26_Stride_Addr_Space_B:** DMA CH 26 PARAM 4: Line Stride for Device B side of the connection.

5.2.402 DMA_CH27_Stride_Addr_Space_B (isp_dma_DMA_CH27_Stride_Addr_Space_B)—Offset 4146Ch

DMA CH 27 PARAM 4: Line Stride for Device B side of the connection.

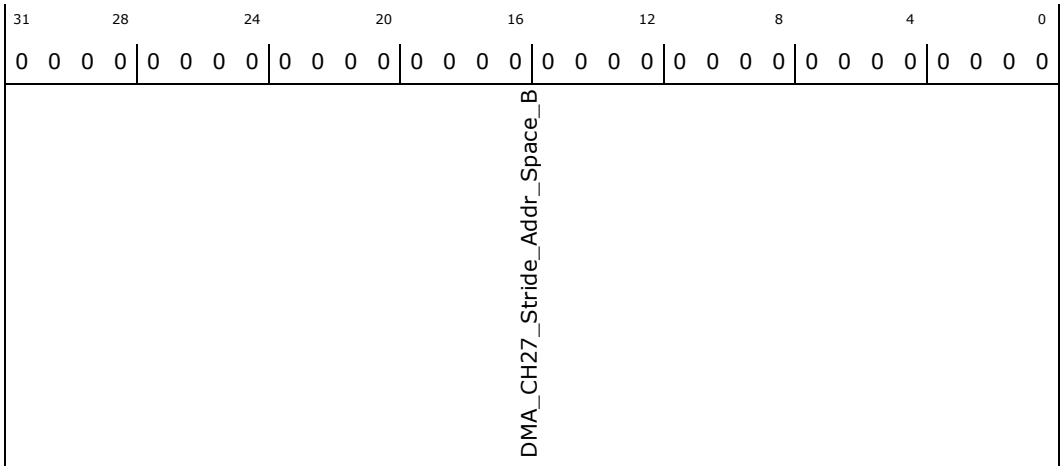
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4146Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH27_Stride_Addr_Space_B:** DMA CH 27 PARAM 4: Line Stride for Device B side of the connection.

5.2.403 DMA_CH28_Stride_Addr_Space_B (isp_dma_DMA_CH28_Stride_Addr_Space_B)—Offset 41470h

DMA CH 28 PARAM 4: Line Stride for Device B side of the connection.

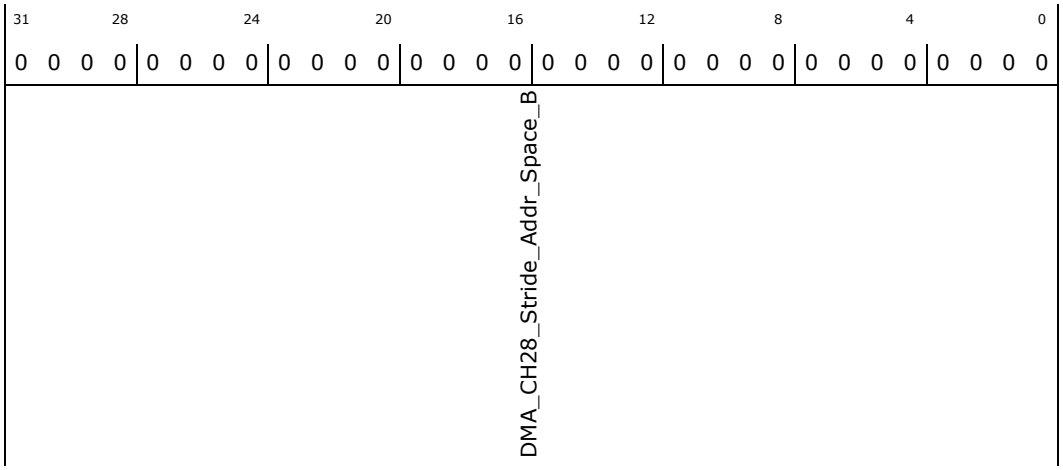
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41470h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH28_Stride_Addr_Space_B:** DMA CH 28 PARAM 4: Line Stride for Device B side of the connection.

5.2.404 DMA_CH29_Stride_Addr_Space_B (isp_dma_DMA_CH29_Stride_Addr_Space_B)—Offset 41474h

DMA CH 29 PARAM 4: Line Stride for Device B side of the connection.

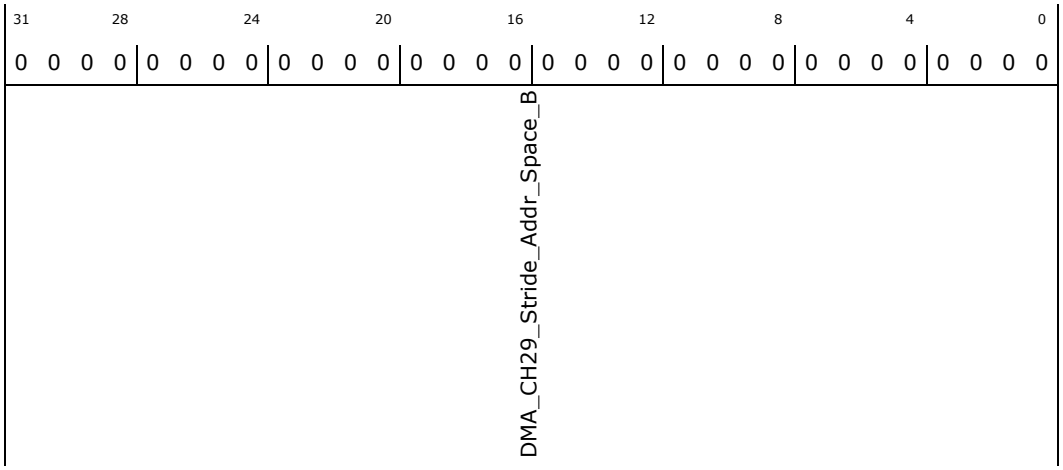
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41474h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH29_Stride_Addr_Space_B:** DMA CH 29 PARAM 4: Line Stride for Device B side of the connection.

5.2.405 DMA_CH30_Stride_Addr_Space_B (isp_dma_DMA_CH30_Stride_Addr_Space_B)—Offset 41478h

DMA CH 30 PARAM 4: Line Stride for Device B side of the connection.

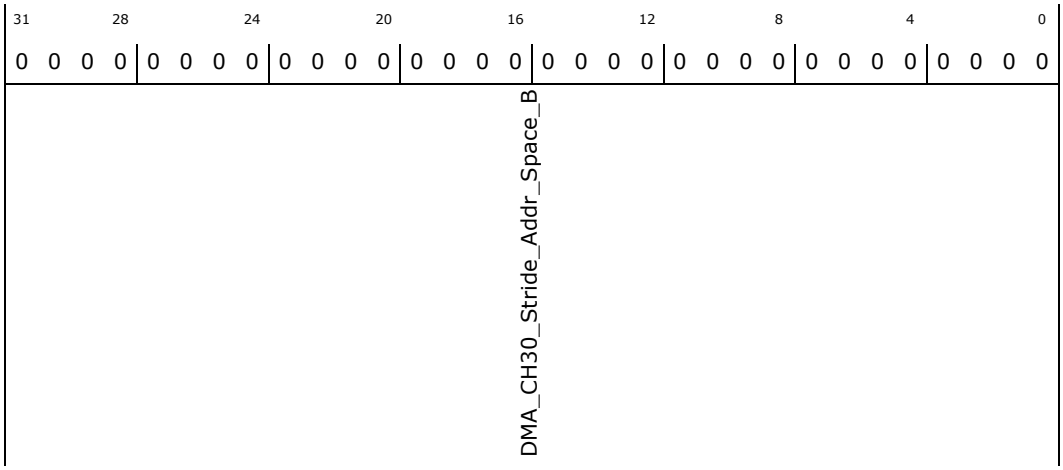
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41478h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH30_Stride_Addr_Space_B:** DMA CH 30 PARAM 4: Line Stride for Device B side of the connection.

5.2.406 DMA_CH31_Stride_Addr_Space_B (isp_dma_DMA_CH31_Stride_Addr_Space_B)—Offset 4147Ch

DMA CH 30 PARAM 4: Line Stride for Device B side of the connection.

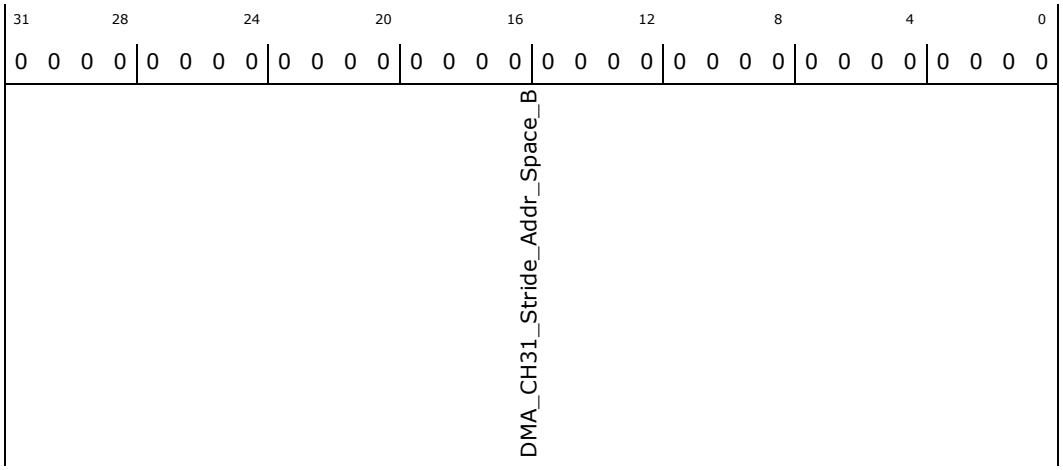
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4147Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH31_Stride_Addr_Space_B:** DMA CH 30 PARAM 4: Line Stride for Device B side of the connection.

5.2.407 DMA_CH0_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH0_Left_Crop_and_Elem_Addr_Space_B)—Offset 41500h

DMA CH 0 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

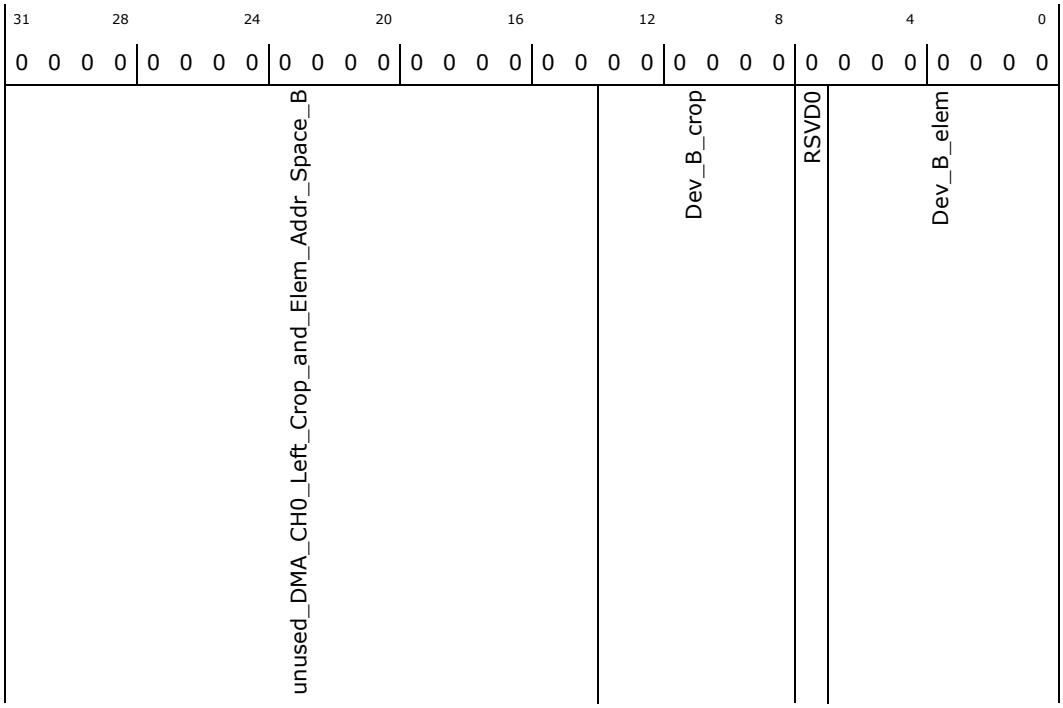
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41500h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH0_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.408 DMA_CH1_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH1_Left_Crop_and_Elem_Addr_Space_B)—Offset 41504h

DMA CH 1 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

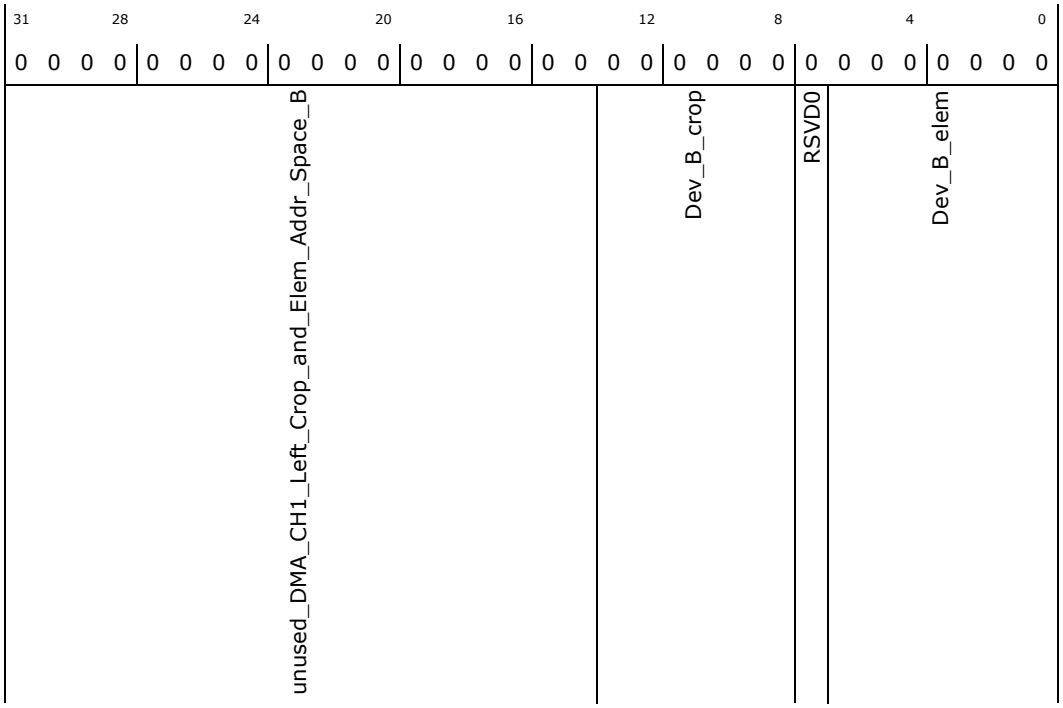
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41504h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH1_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.409 DMA_CH2_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH2_Left_Crop_and_Elem_Addr_Space_B)—Offset 41508h

DMA CH 2 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

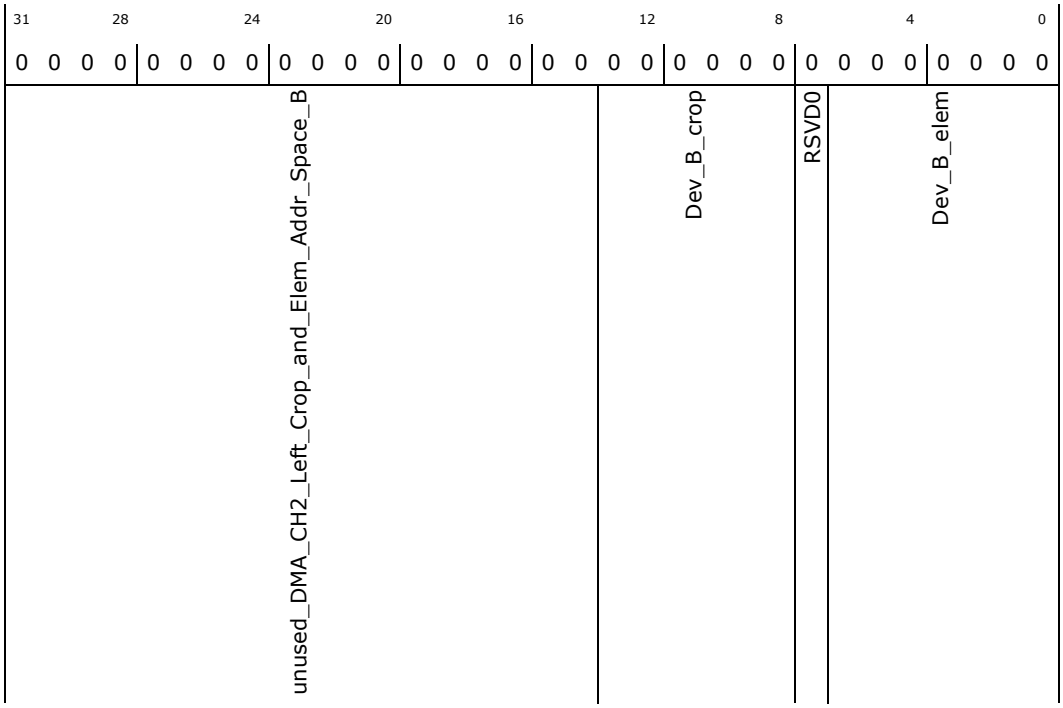
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41508h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH2_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.410 DMA_CH3_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH3_Left_Crop_and_Elem_Addr_Space_B)—Offset 4150Ch

DMA CH 3 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

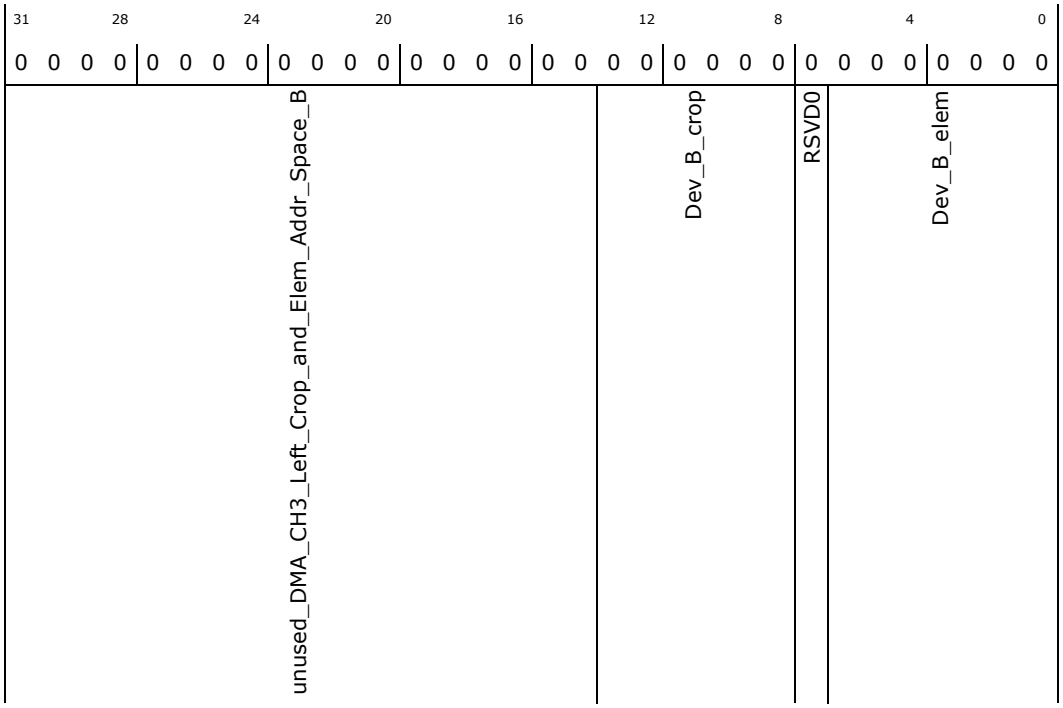
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4150Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH3_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.411 DMA_CH4_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH4_Left_Crop_and_Elem_Addr_Space_B)—Offset 41510h

DMA CH 4 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

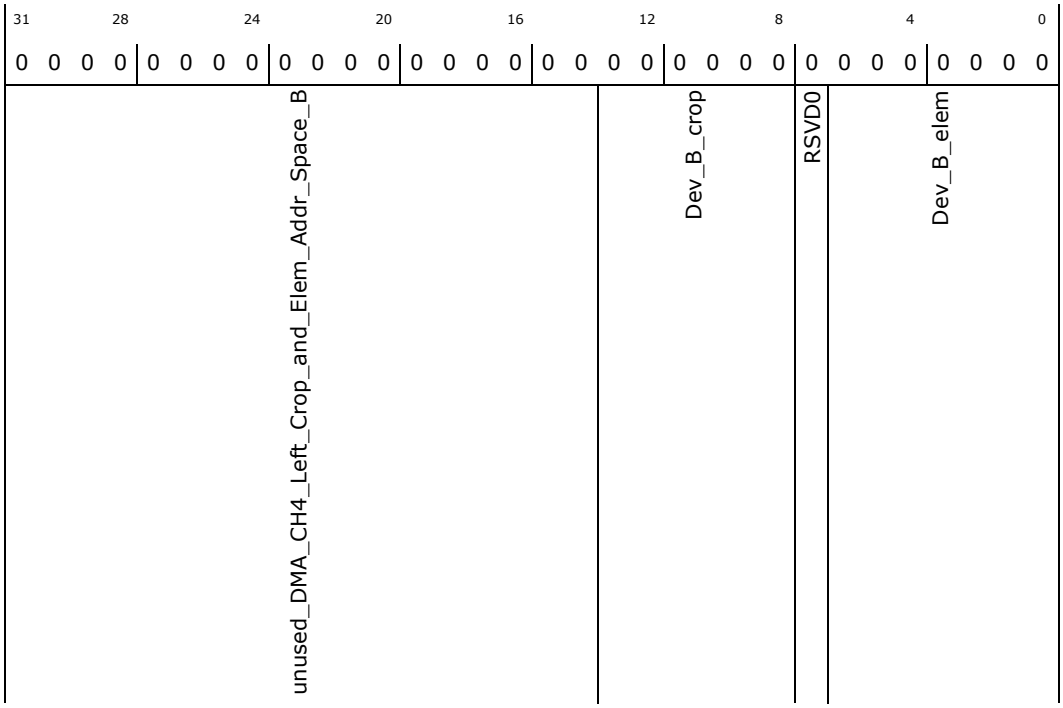
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41510h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH4_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.412 DMA_CH5_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH5_Left_Crop_and_Elem_Addr_Space_B)—Offset 41514h

DMA CH 5 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

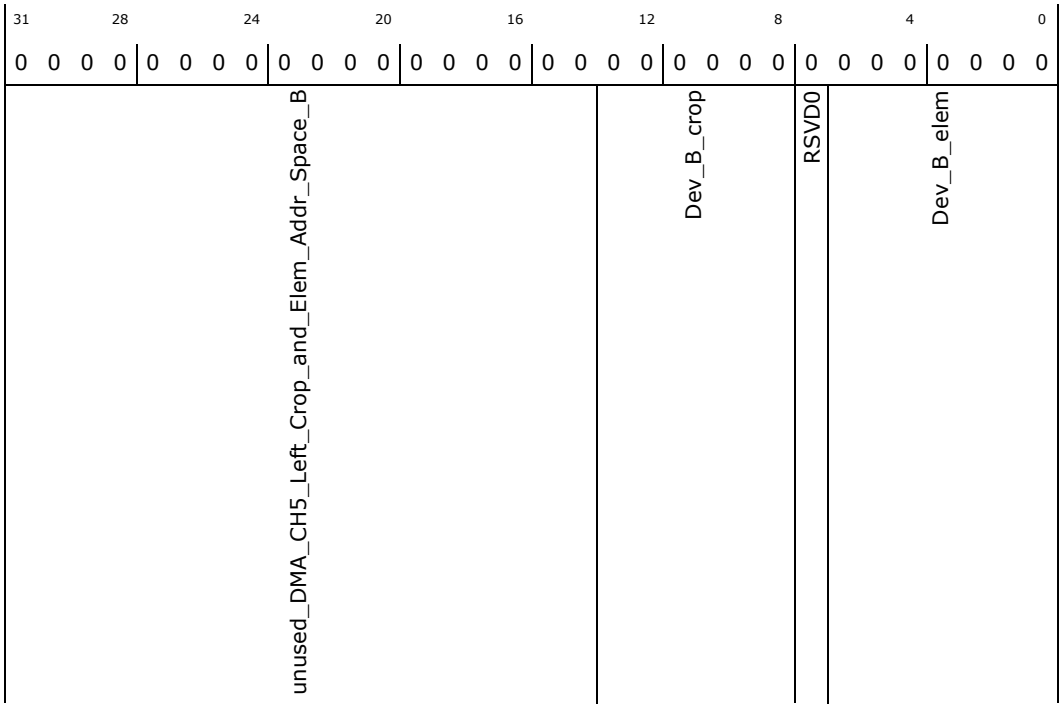
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41514h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH5_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.413 DMA_CH6_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH6_Left_Crop_and_Elem_Addr_Space_B)—Offset 41518h

DMA CH 6 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

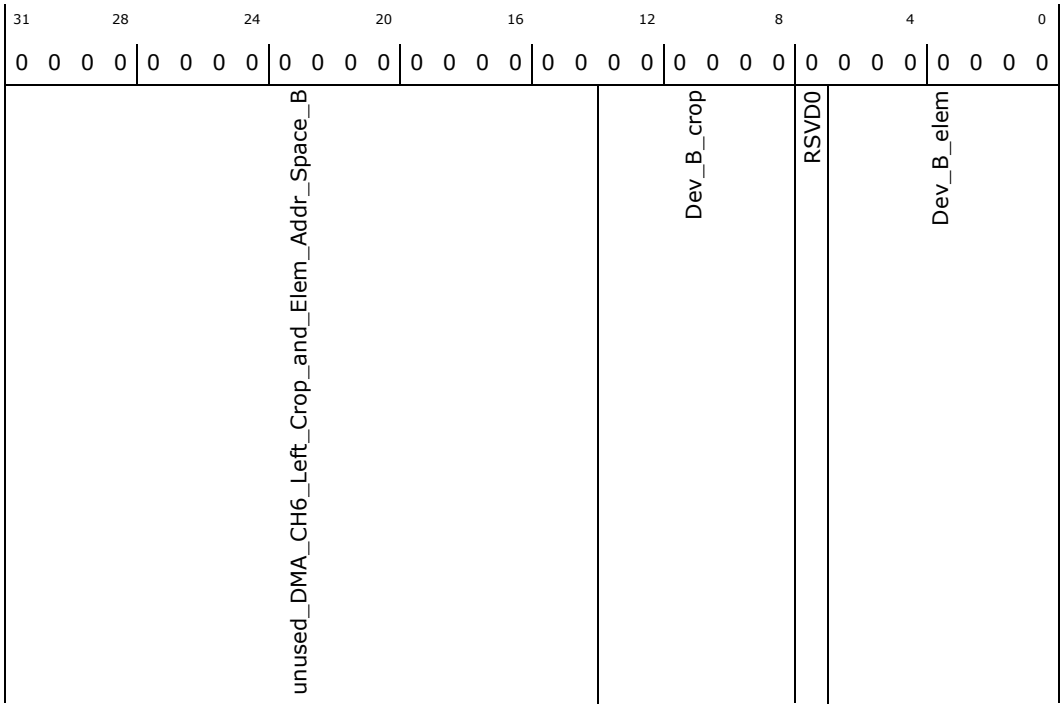
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41518h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH6_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.414 DMA_CH7_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH7_Left_Crop_and_Elem_Addr_Space_B)—Offset 4151Ch

DMA CH 7 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

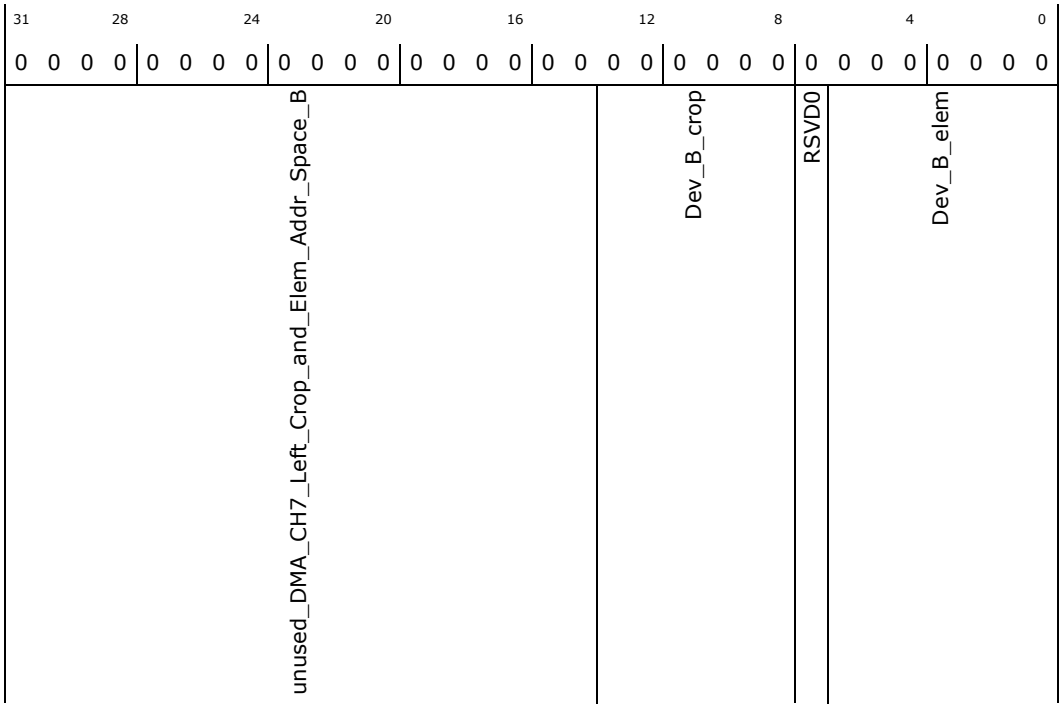
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4151Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH7_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.415 DMA_CH8_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH8_Left_Crop_and_Elem_Addr_Space_B)—Offset 41520h

DMA CH 8 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

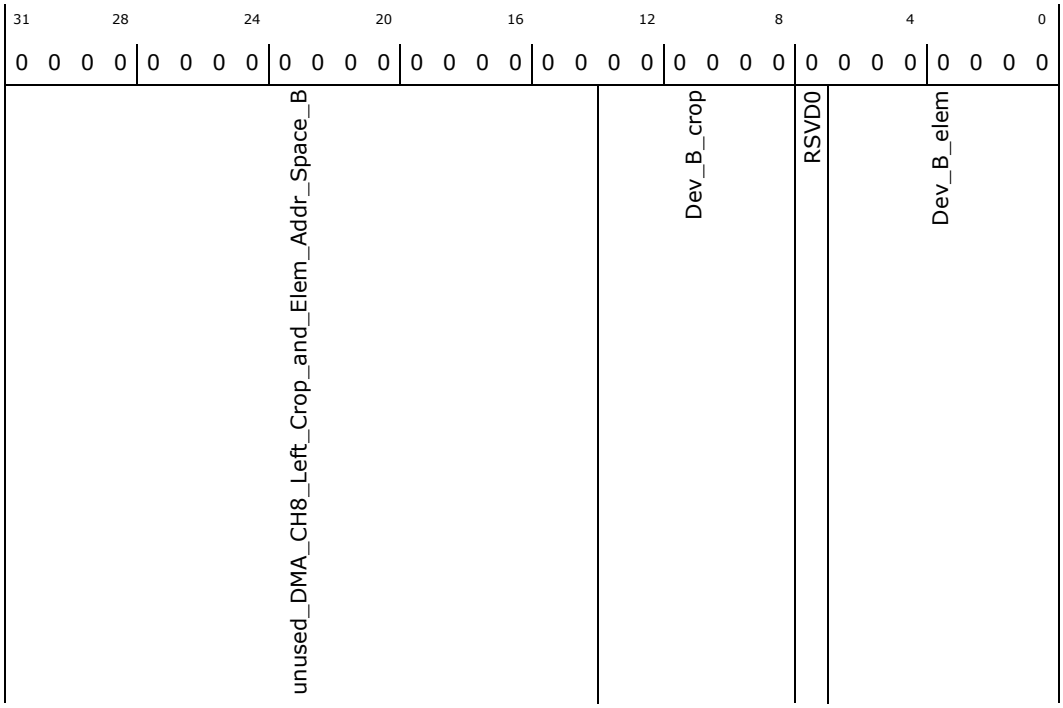
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41520h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH8_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.416 DMA_CH9_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH9_Left_Crop_and_Elem_Addr_Space_B)—Offset 41524h

DMA CH 9 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

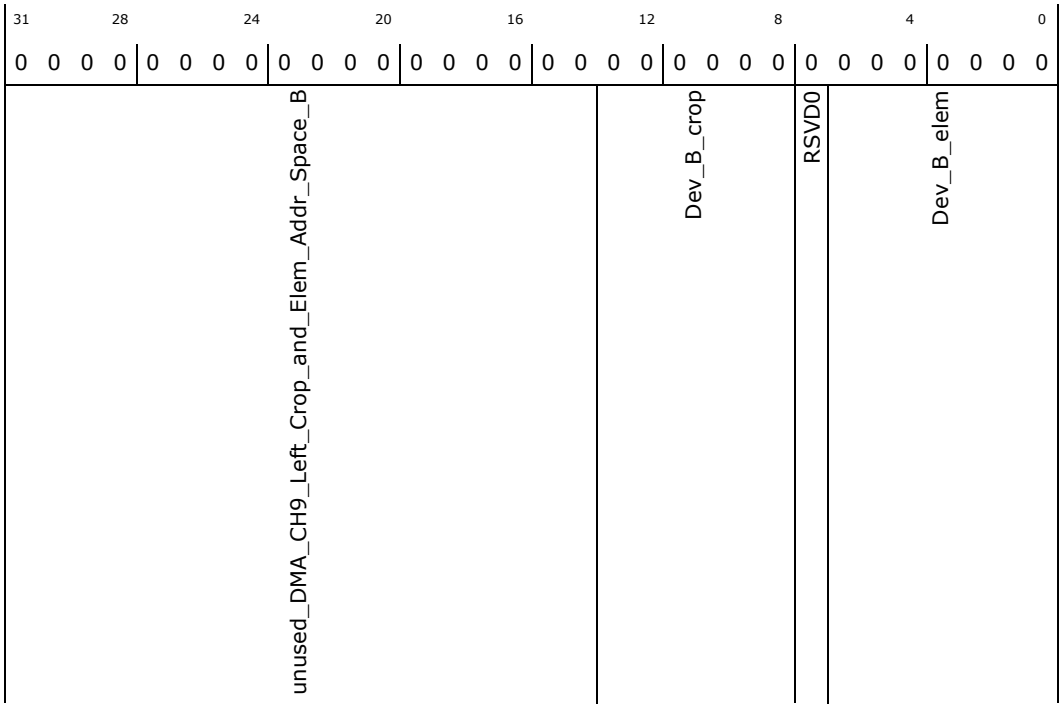
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41524h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH9_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.417 DMA_CH10_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH10_Left_Crop_and_Elem_Addr_Space_B)—Offset 41528h

DMA CH 10 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

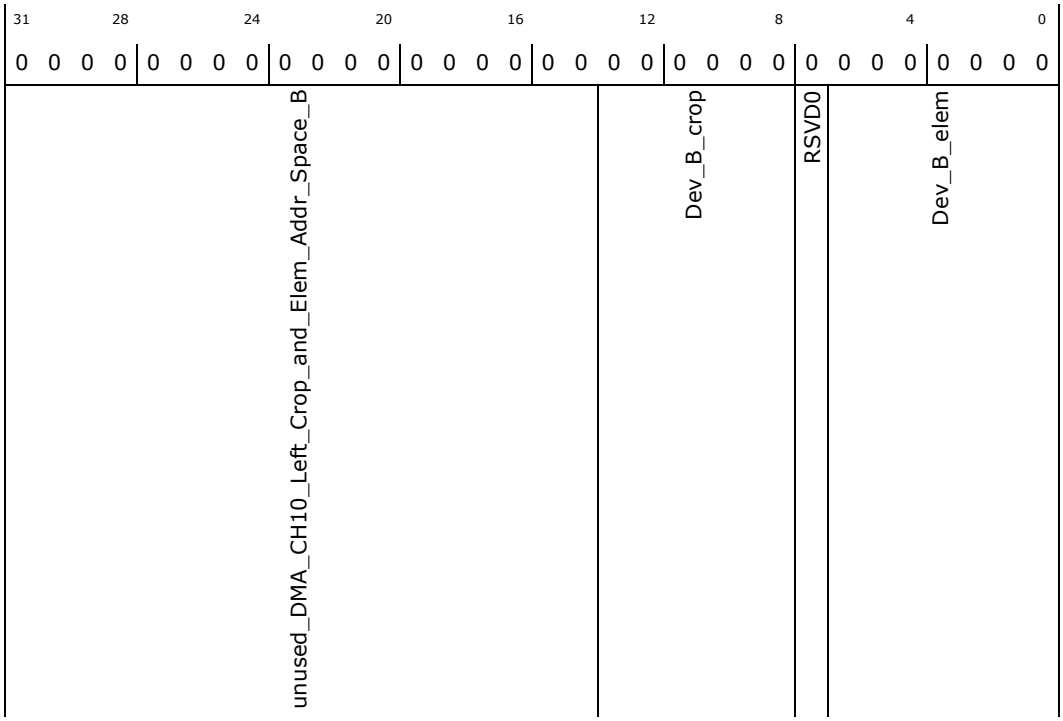
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41528h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH10_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.418 DMA_CH11_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH11_Left_Crop_and_Elem_Addr_Space_B)—Offset 4152Ch

DMA CH 11 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

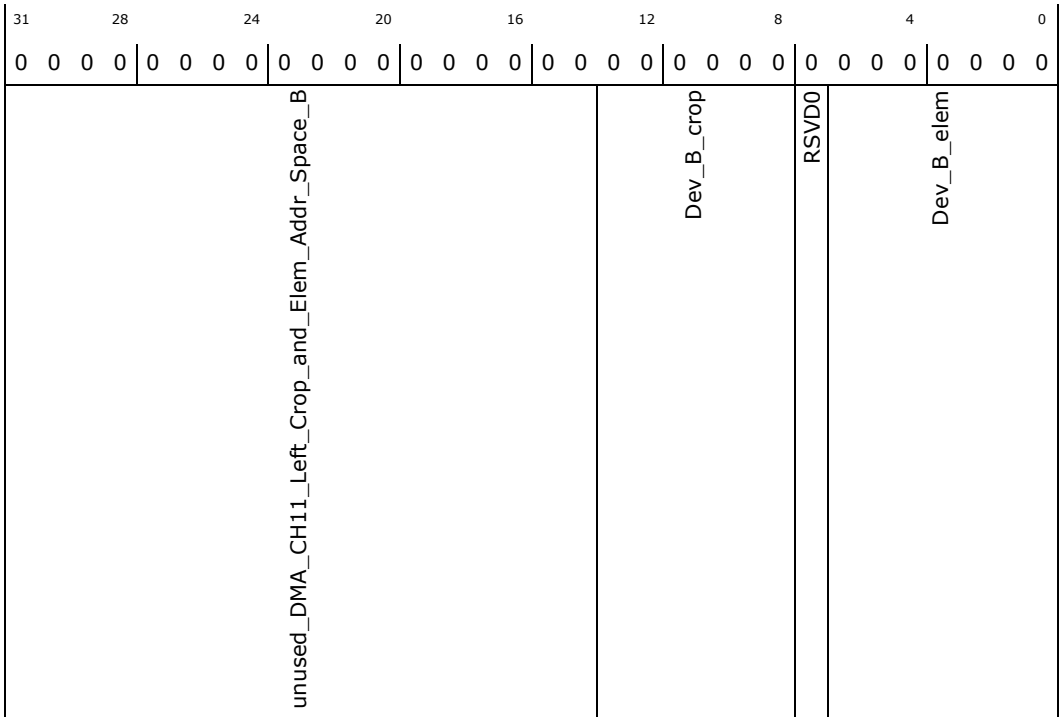
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4152Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH11_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.419 DMA_CH12_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH12_Left_Crop_and_Elem_Addr_Space_B)—Offset 41530h

DMA CH 12 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

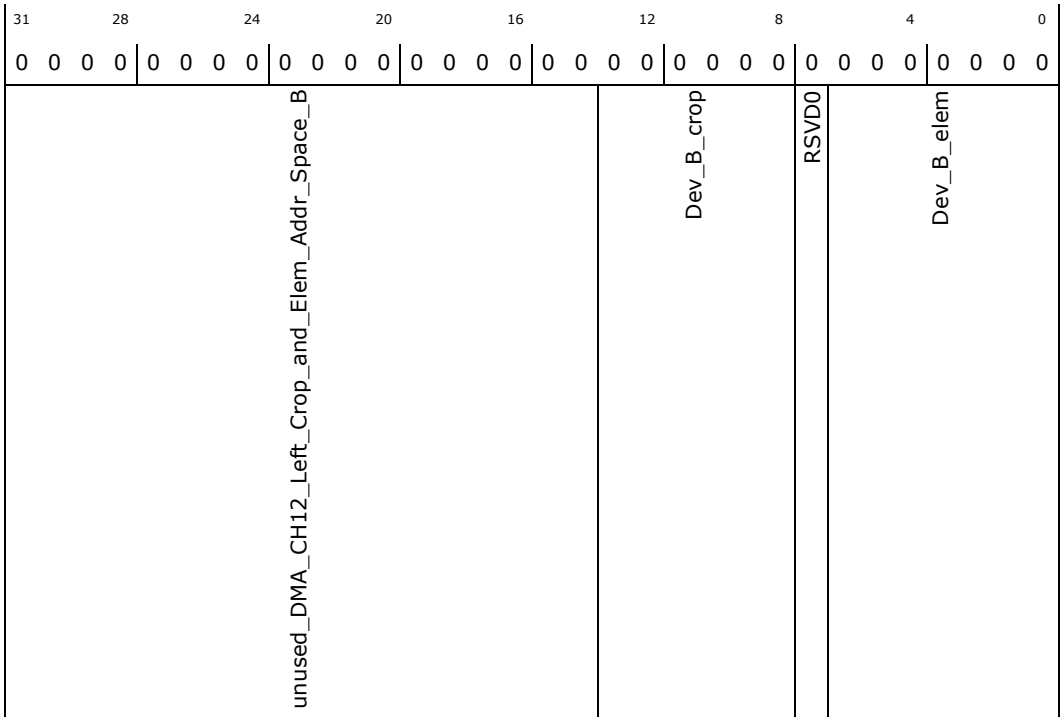
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41530h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH12_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.420 DMA_CH13_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH13_Left_Crop_and_Elem_Addr_Space_B)—Offset 41534h

DMA CH 13 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

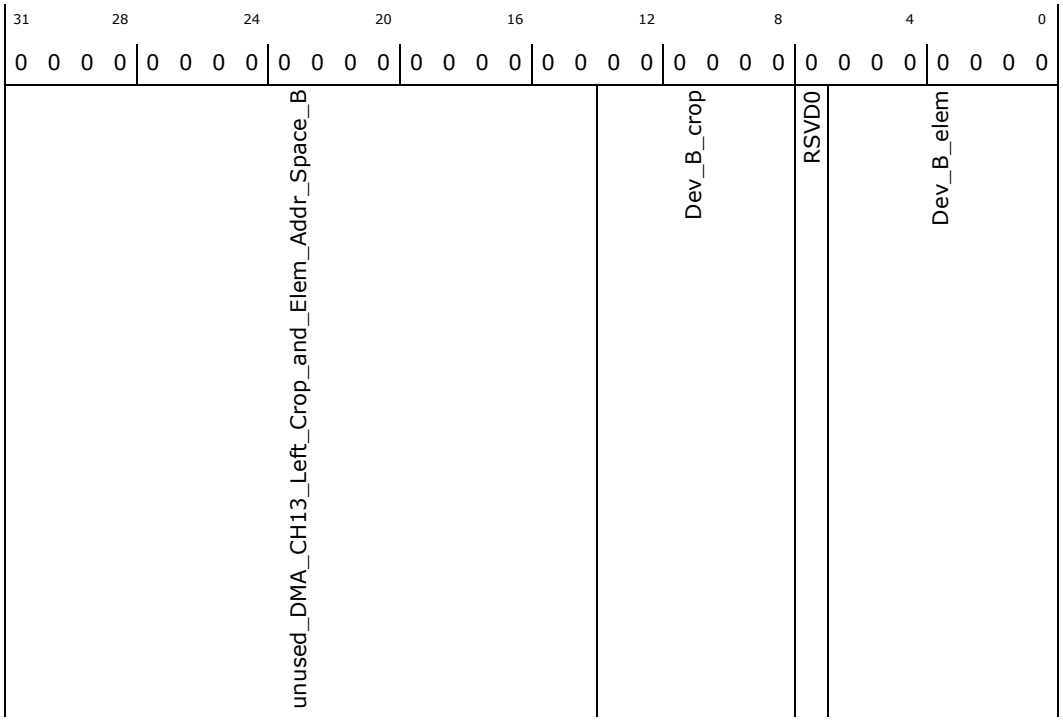
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41534h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH13_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.421 DMA_CH14_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH14_Left_Crop_and_Elem_Addr_Space_B)—Offset 41538h

DMA CH 14 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

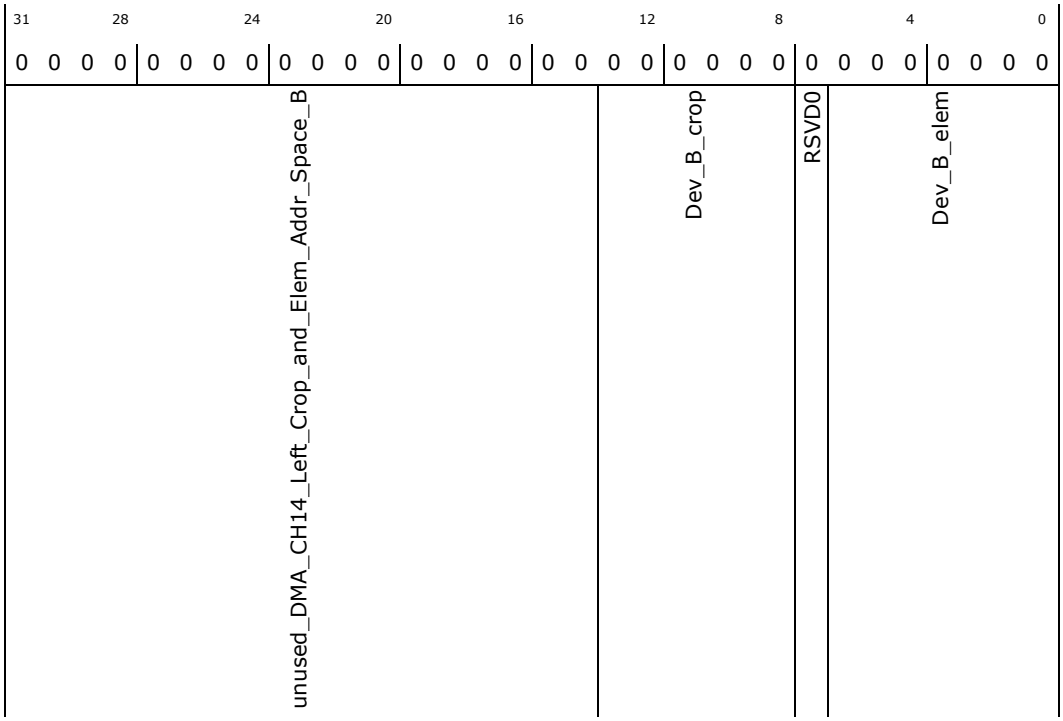
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41538h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH14_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.422 DMA_CH15_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH15_Left_Crop_and_Elem_Addr_Space_B)—Offset 4153Ch

DMA CH 15 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

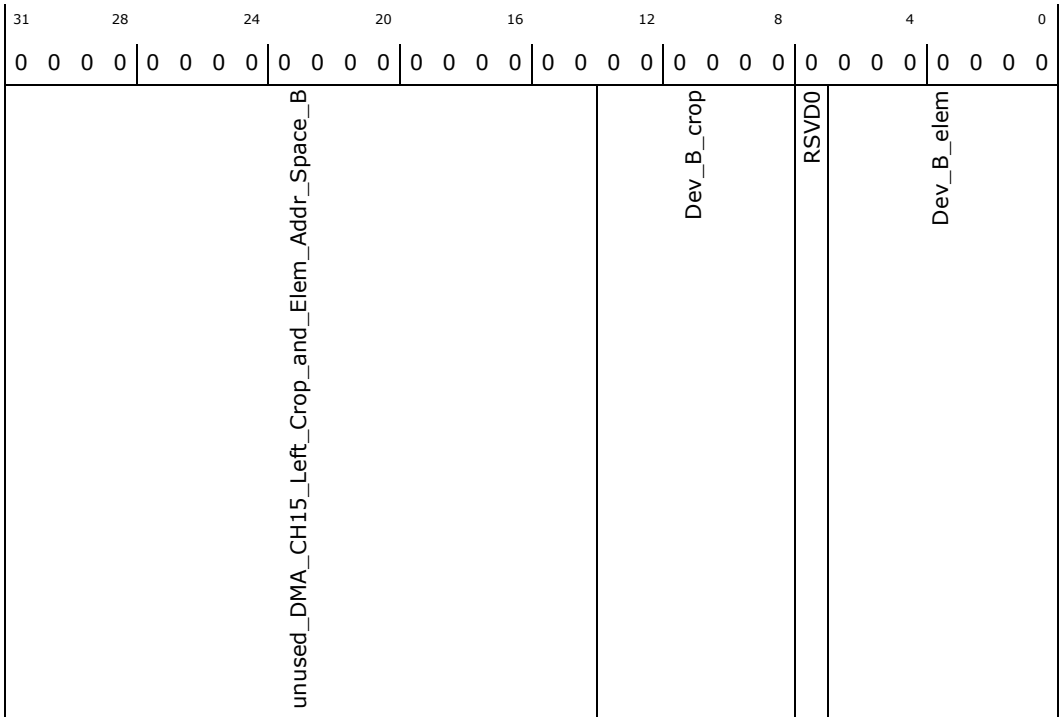
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4153Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH15_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.423 DMA_CH16_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH16_Left_Crop_and_Elem_Addr_Space_B)—Offset 41540h

DMA CH 16 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

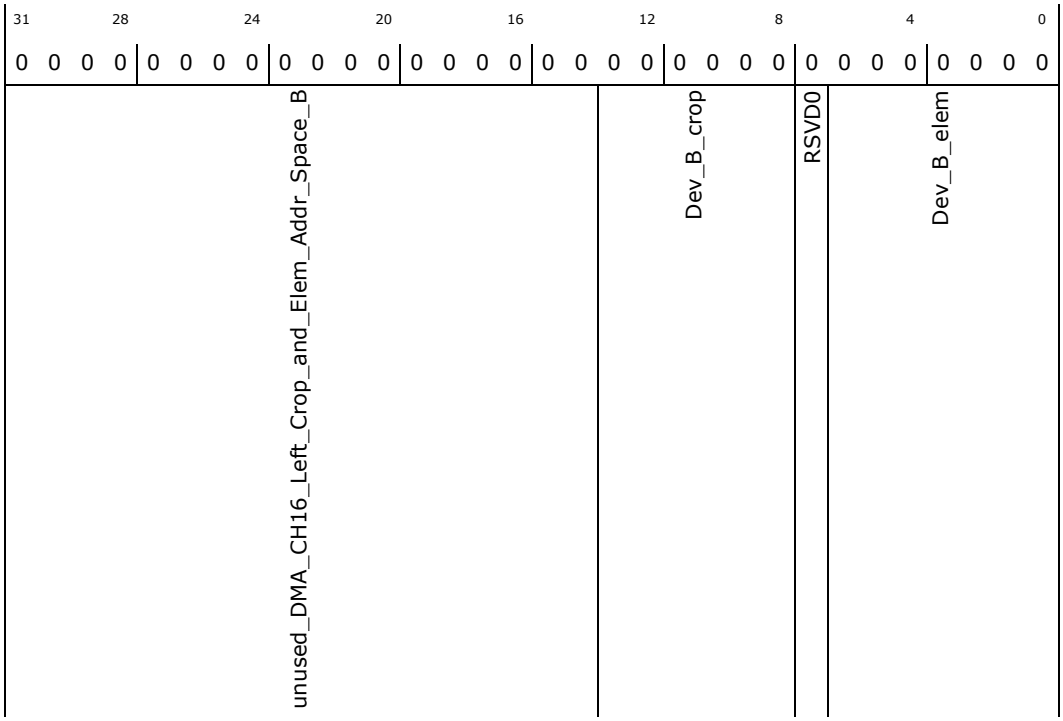
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41540h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH16_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.424 DMA_CH17_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH17_Left_Crop_and_Elem_Addr_Space_B)—Offset 41544h

DMA CH 17 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

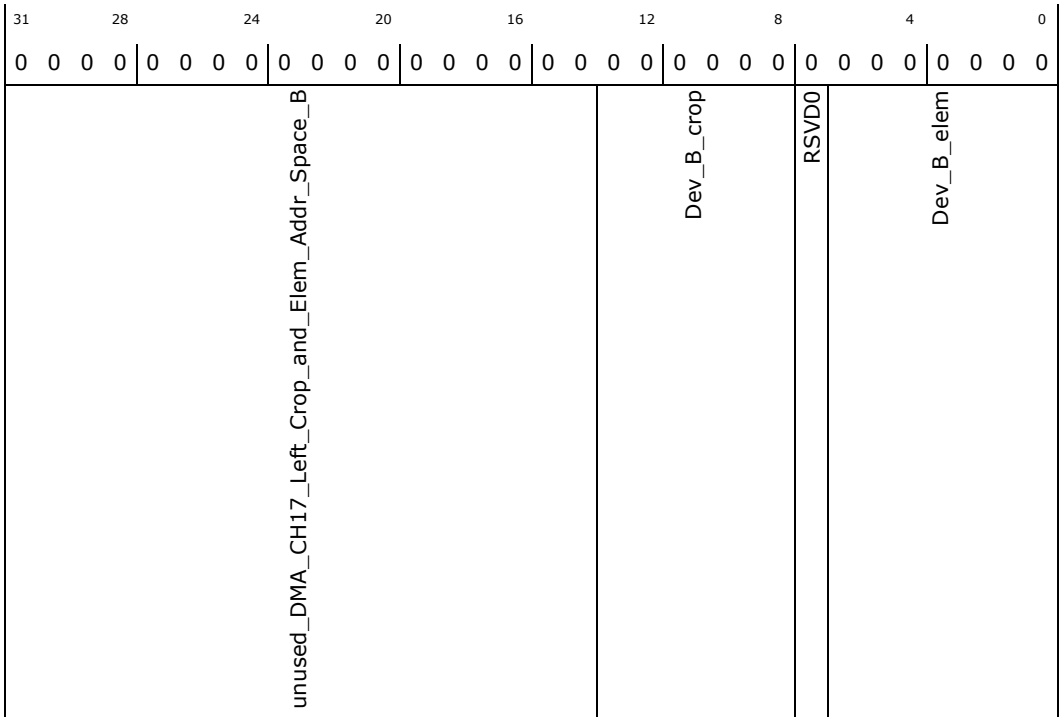
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41544h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH17_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.425 DMA_CH18_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH18_Left_Crop_and_Elem_Addr_Space_B)—Offset 41548h

DMA CH 18 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

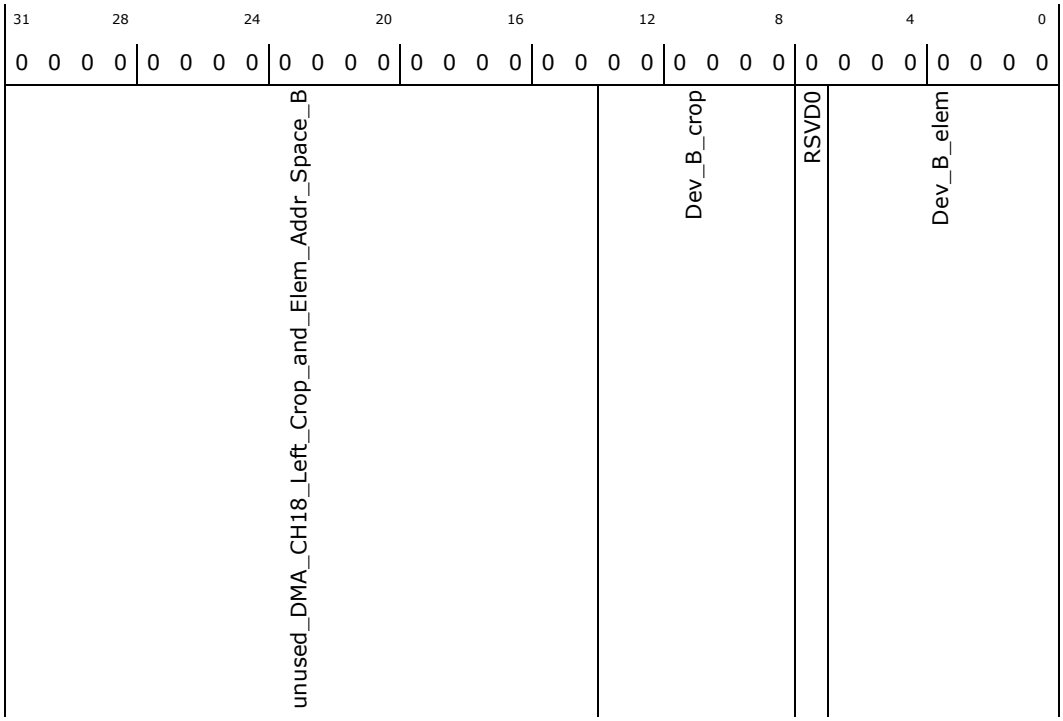
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41548h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH18_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.426 DMA_CH19_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH19_Left_Crop_and_Elem_Addr_Space_B)—Offset 4154Ch

DMA CH 19 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

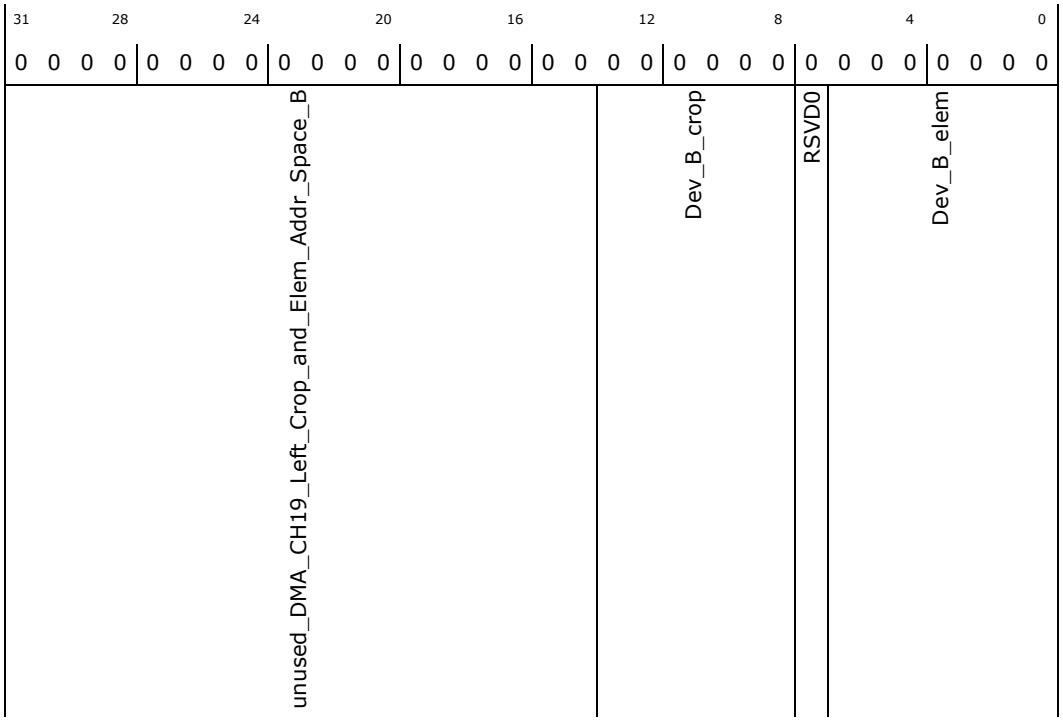
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4154Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH19_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.427 DMA_CH20_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH20_Left_Crop_and_Elem_Addr_Space_B)—Offset 41550h

DMA CH 20 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

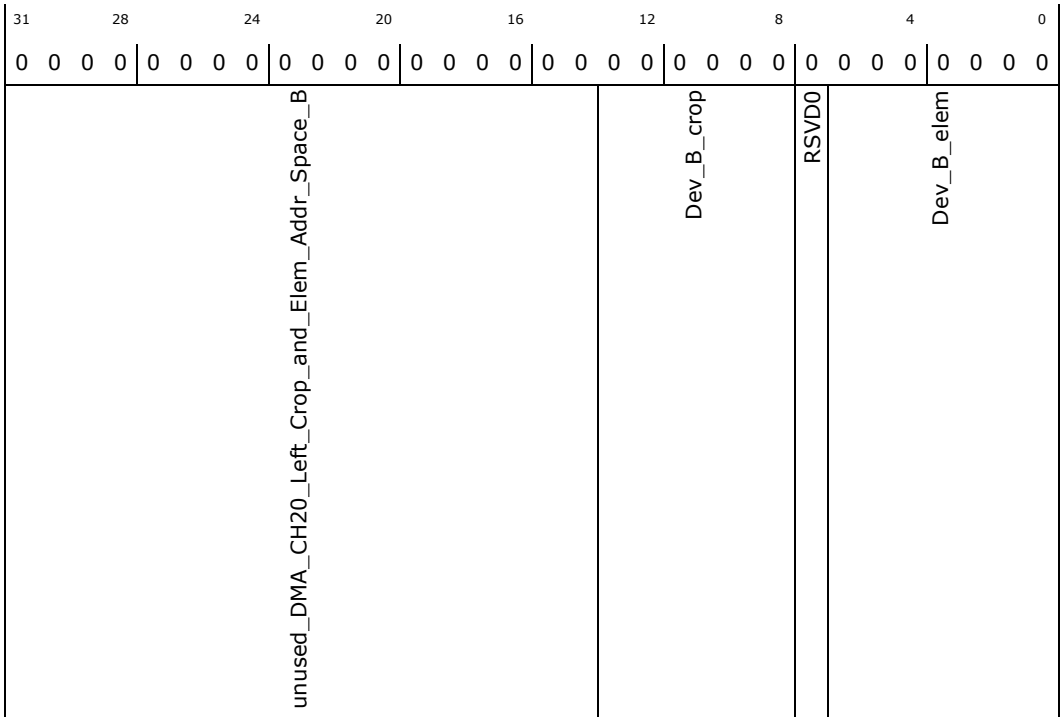
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41550h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH20_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.428 DMA_CH21_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH21_Left_Crop_and_Elem_Addr_Space_B)—Offset 41554h

DMA CH 21 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

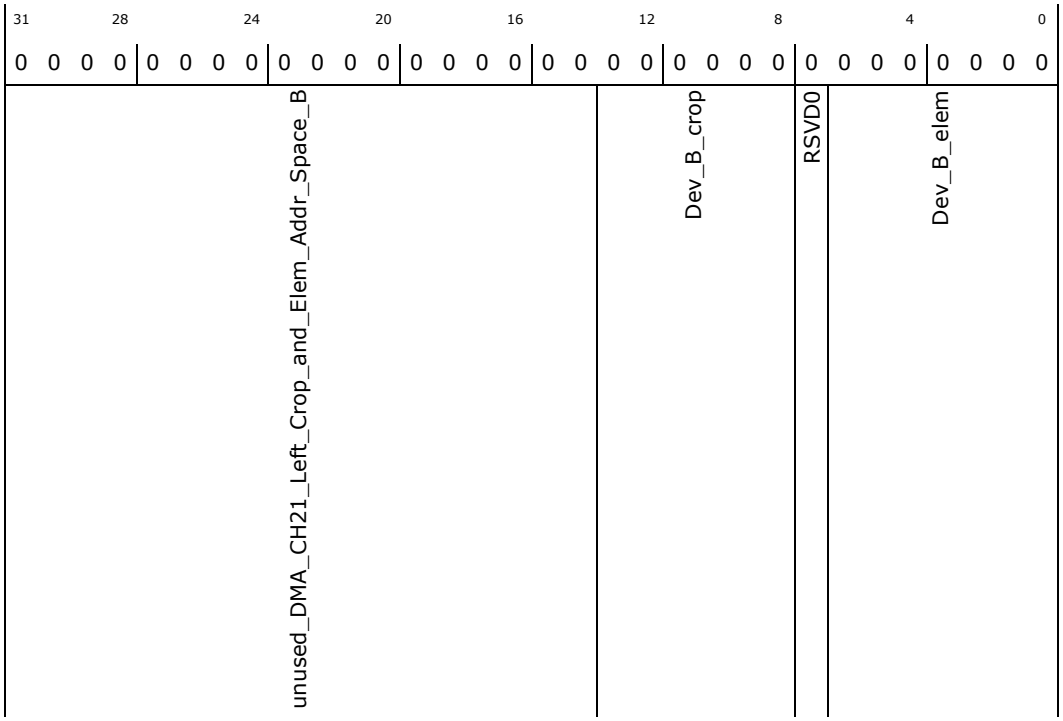
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41554h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH21_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.429 DMA_CH22_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH22_Left_Crop_and_Elem_Addr_Space_B)—Offset 41558h

DMA CH 22 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

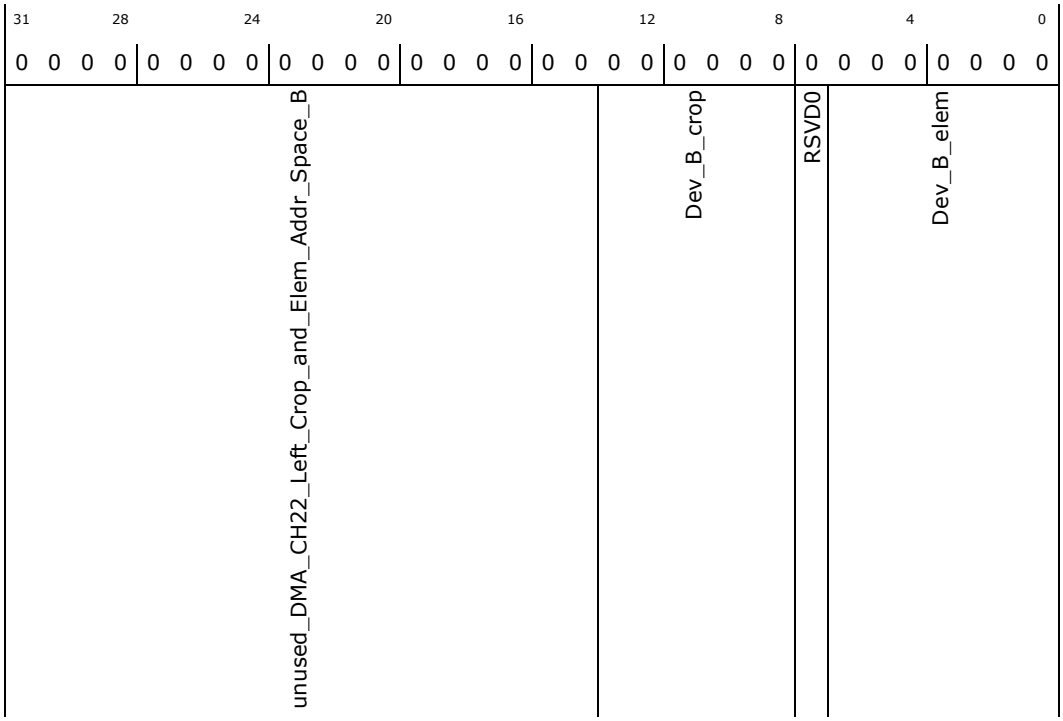
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41558h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH22_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.430 DMA_CH23_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH23_Left_Crop_and_Elem_Addr_Space_B)—Offset 4155Ch

DMA CH 23 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

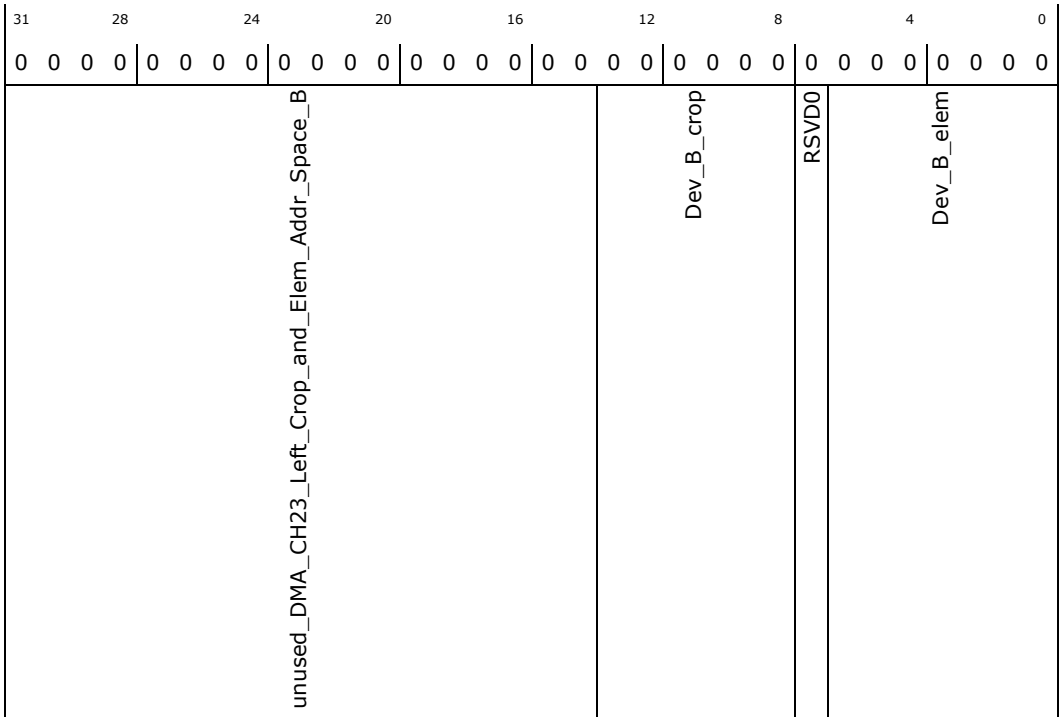
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4155Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH23_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.431 DMA_CH24_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH24_Left_Crop_and_Elem_Addr_Space_B)—Offset 41560h

DMA CH 24 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

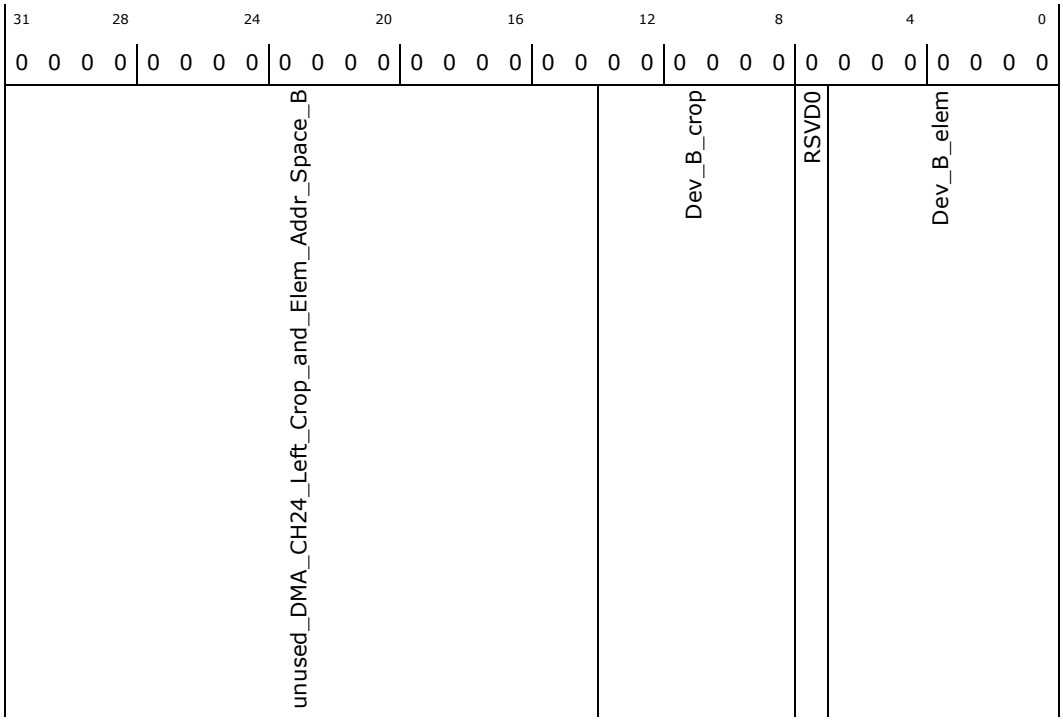
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41560h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH24_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.432 DMA_CH25_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH25_Left_Crop_and_Elem_Addr_Space_B)—Offset 41564h

DMA CH 25 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

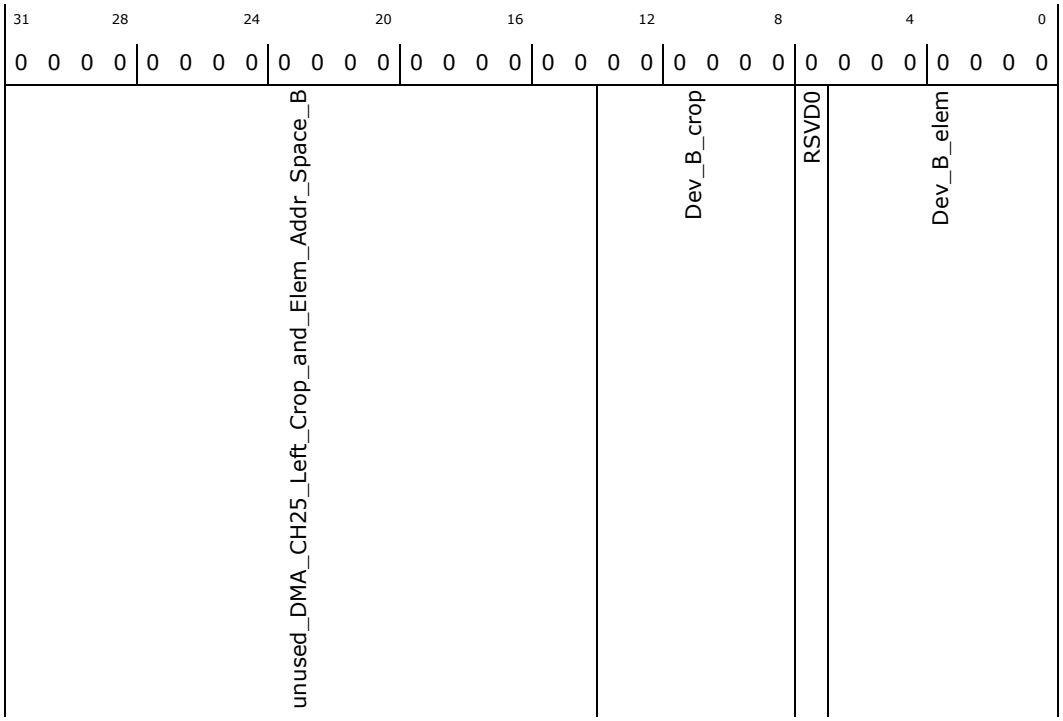
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41564h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH25_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.433 DMA_CH26_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH26_Left_Crop_and_Elem_Addr_Space_B)—Offset 41568h

DMA CH 26 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

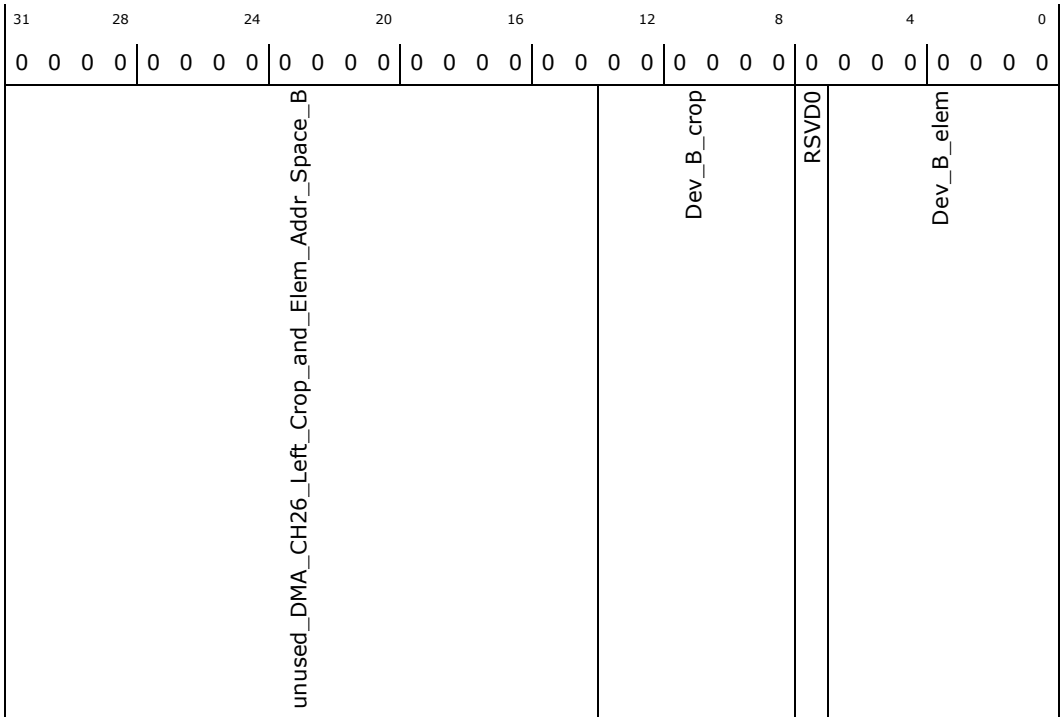
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41568h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH26_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.434 DMA_CH27_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH27_Left_Crop_and_Elem_Addr_Space_B)—Offset 4156Ch

DMA CH 27 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

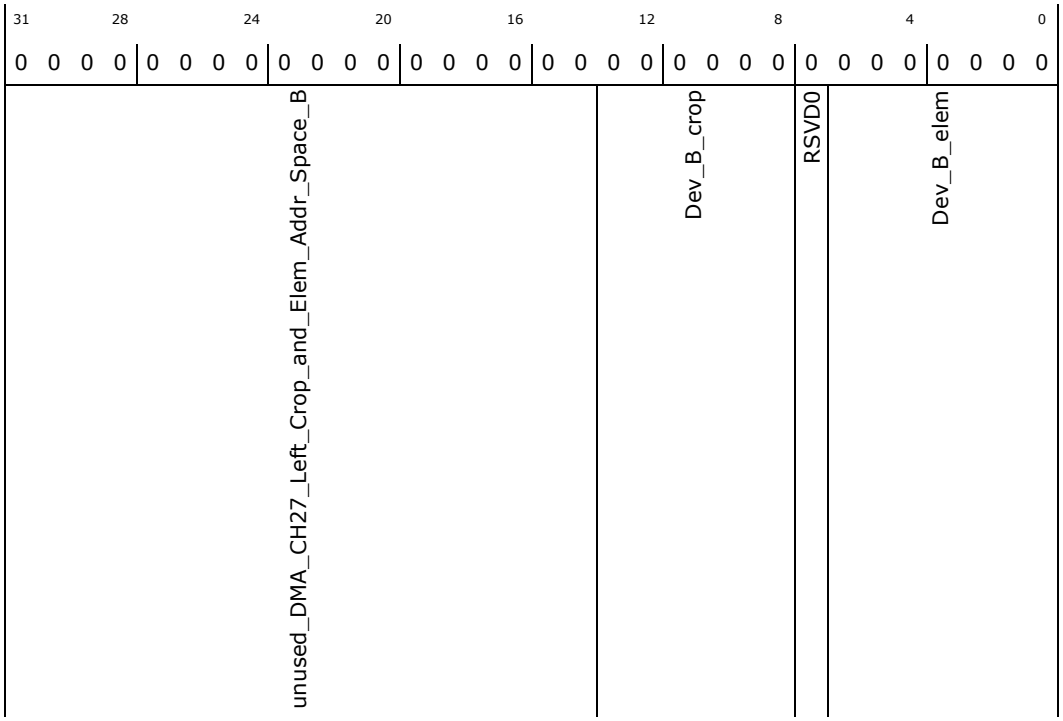
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4156Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH27_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.435 DMA_CH28_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH28_Left_Crop_and_Elem_Addr_Space_B)—Offset 41570h

DMA CH 28 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

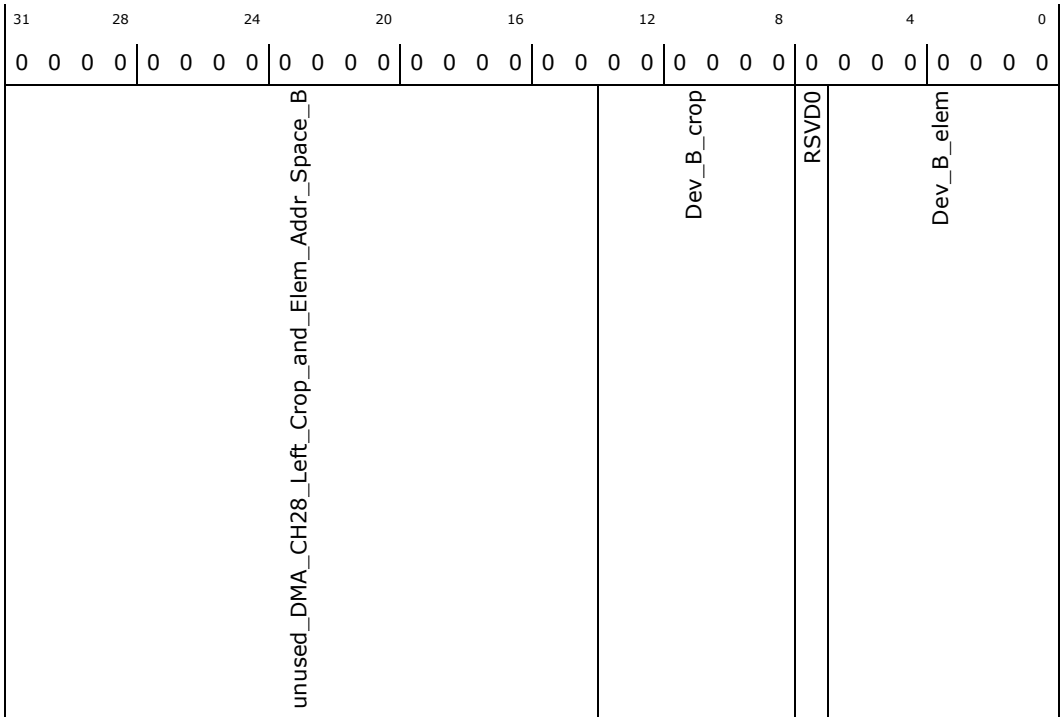
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41570h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH28_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.436 DMA_CH29_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH29_Left_Crop_and_Elem_Addr_Space_B)—Offset 41574h

DMA CH 29 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

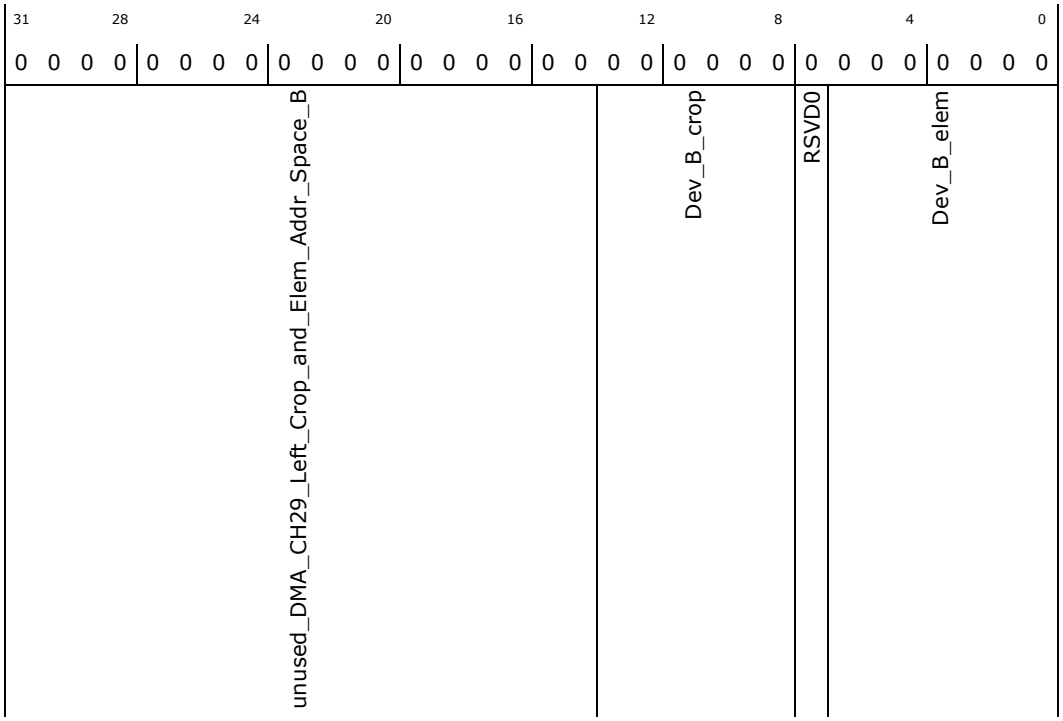
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41574h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH29_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.437 DMA_CH30_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH30_Left_Crop_and_Elem_Addr_Space_B)—Offset 41578h

DMA CH 30 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

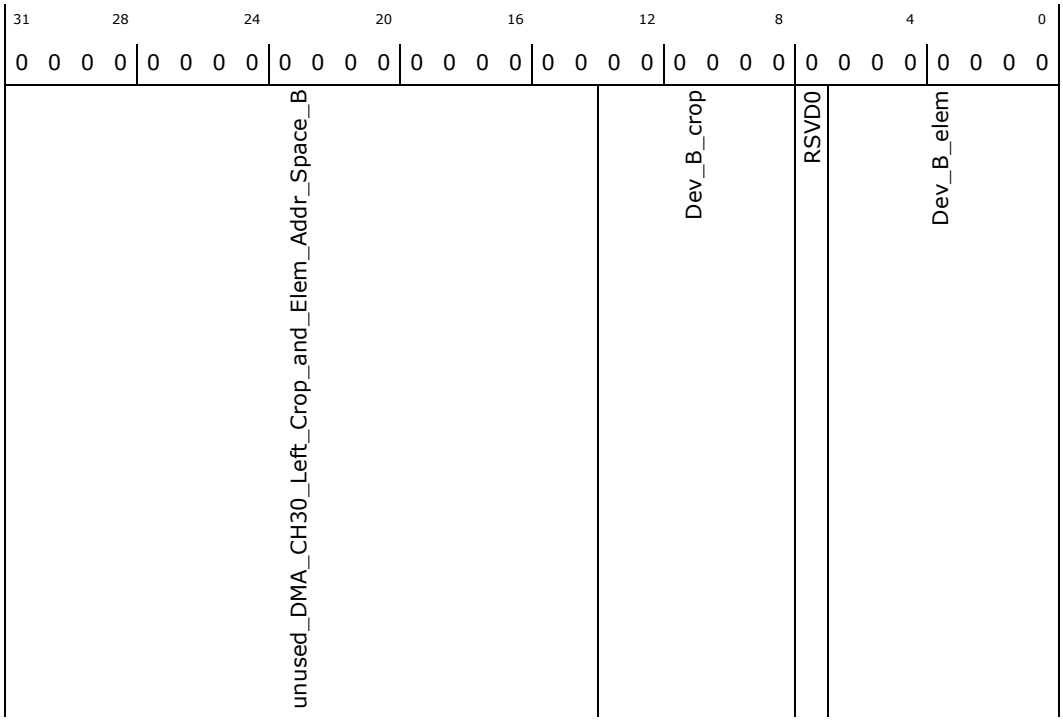
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41578h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH30_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.438 DMA_CH31_Left_Crop_and_Elem_Addr_Space_B (isp_dma_DMA_CH31_Left_Crop_and_Elem_Addr_Space_B)—Offset 4157Ch

DMA CH 31 PARAM 5: Setting value of cropped pixels for each line and number of elements in a word for Device B side of the connection.

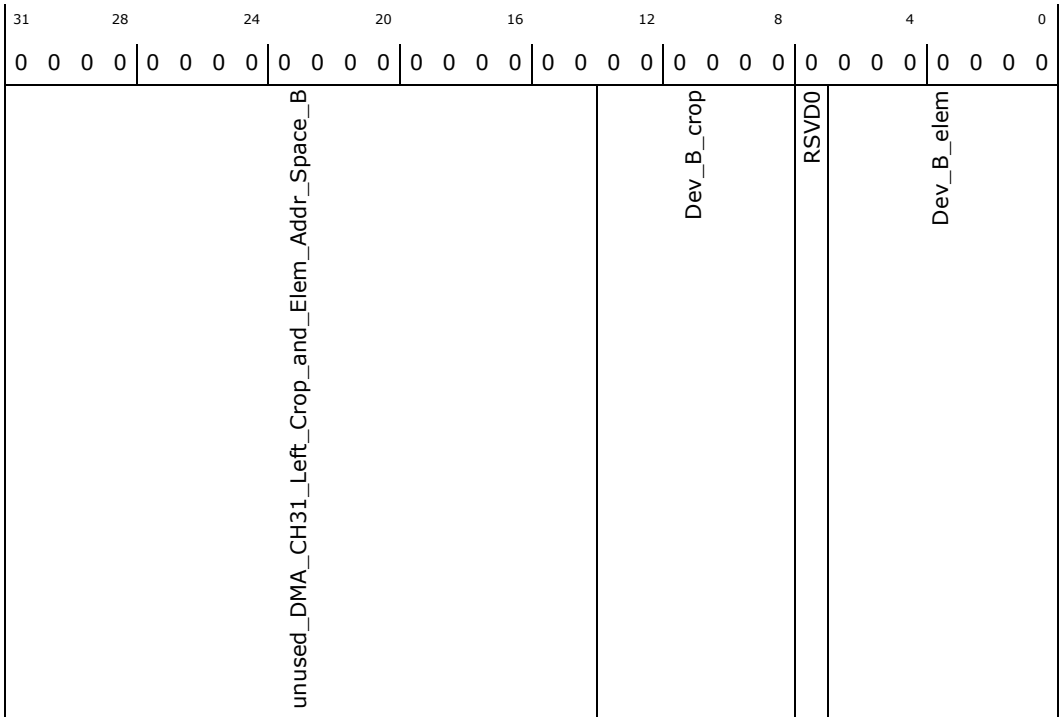
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4157Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH31_Left_Crop_and_Elem_Addr_Space_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping
7	0x0 RO	**RSVD0:** Reserved
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.2.439 DMA_CH0_Block_Width_Addr_Space_B (isp_dma_DMA_CH0_Block_Width_Addr_Space_B)—Offset 41600h

DMA CH 0 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

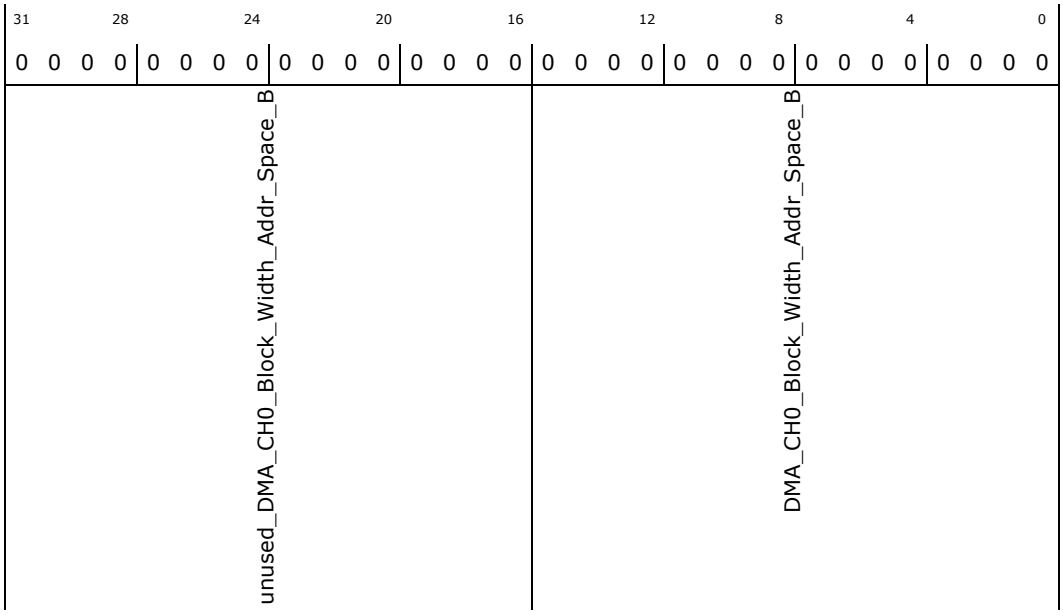
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41600h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH0_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH0_Block_Width_Addr_Space_B:** DMA CH 0 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.440 DMA_CH1_Block_Width_Addr_Space_B (isp_dma_DMA_CH1_Block_Width_Addr_Space_B)—Offset 41604h

DMA CH 1 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

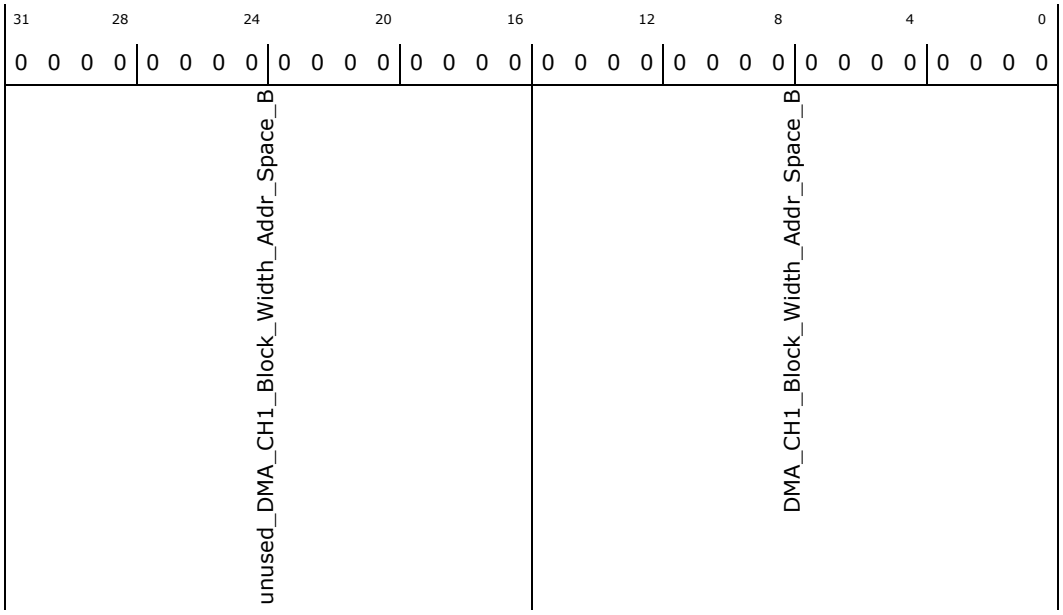
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41604h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH1_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH1_Block_Width_Addr_Space_B:** DMA CH 1 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.441 DMA_CH2_Block_Width_Addr_Space_B (isp_dma_DMA_CH2_Block_Width_Addr_Space_B)—Offset 41608h

DMA CH 2 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

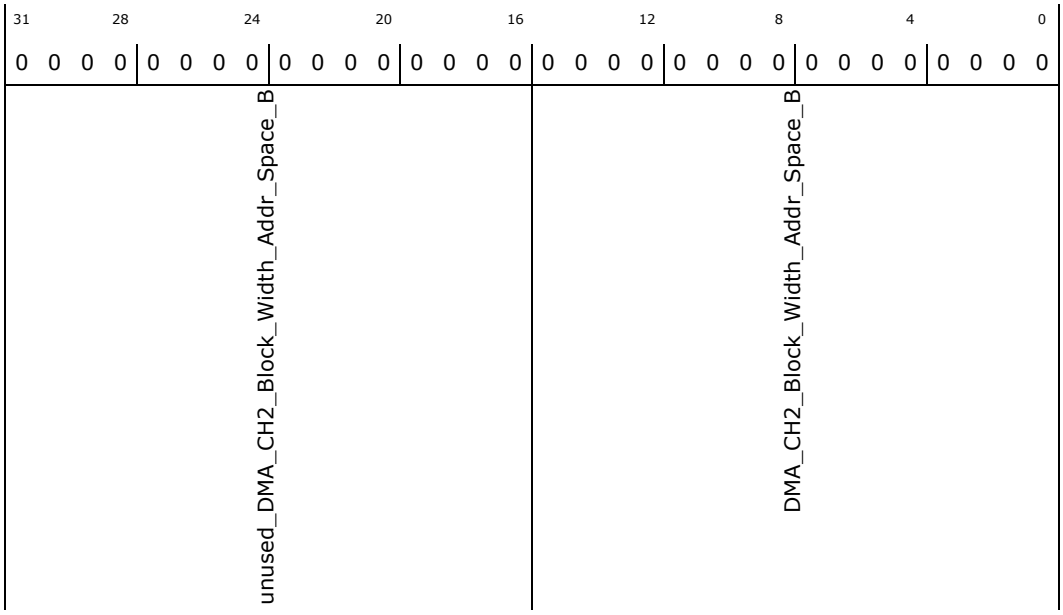
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41608h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH2_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH2_Block_Width_Addr_Space_B:** DMA CH 2 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.442 DMA_CH3_Block_Width_Addr_Space_B (isp_dma_DMA_CH3_Block_Width_Addr_Space_B)—Offset 4160Ch

DMA CH 3 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

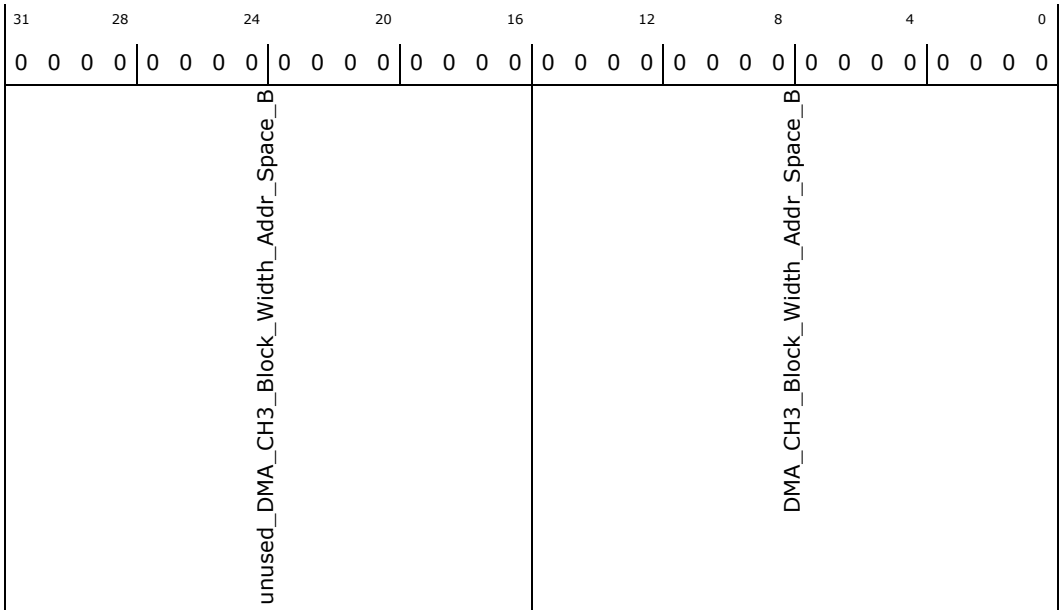
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4160Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH3_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH3_Block_Width_Addr_Space_B:** DMA CH 3 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.443 DMA_CH4_Block_Width_Addr_Space_B (isp_dma_DMA_CH4_Block_Width_Addr_Space_B)—Offset 41610h

DMA CH 4 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

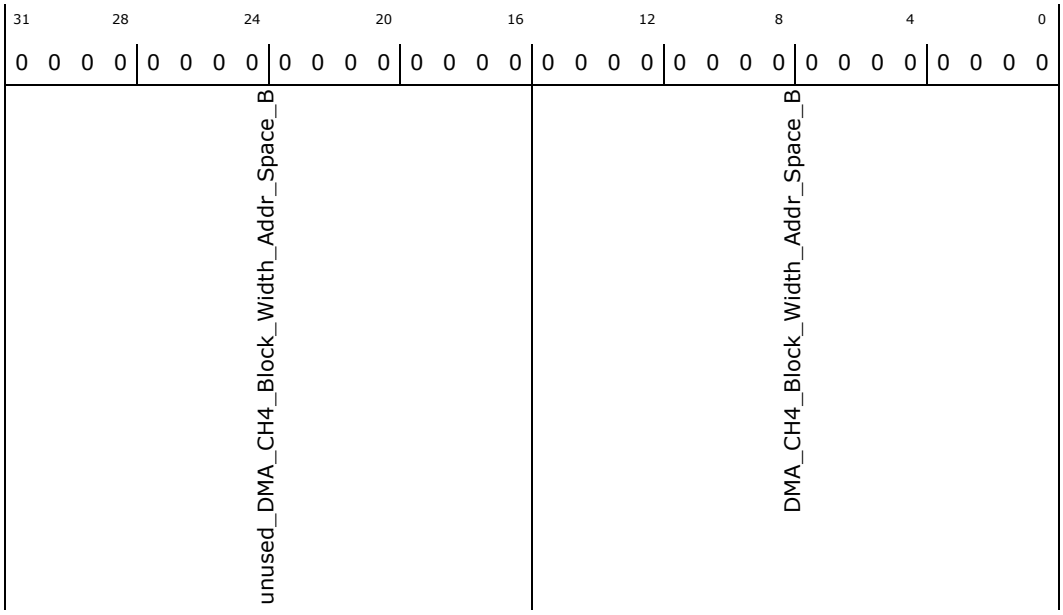
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41610h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH4_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH4_Block_Width_Addr_Space_B:** DMA CH 4 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.444 DMA_CH5_Block_Width_Addr_Space_B (isp_dma_DMA_CH5_Block_Width_Addr_Space_B)—Offset 41614h

DMA CH 5 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

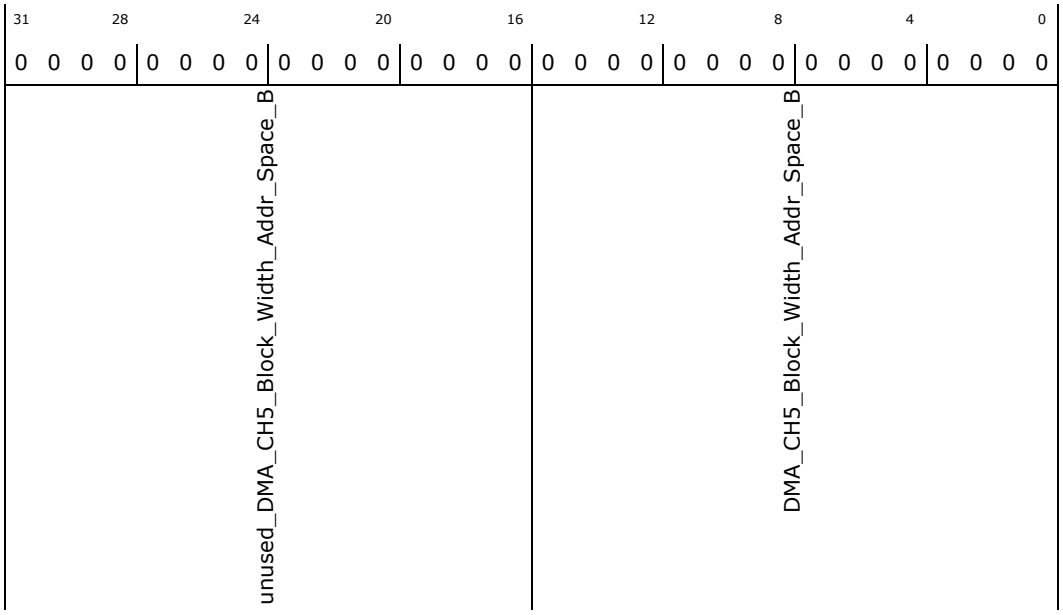
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41614h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH5_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH5_Block_Width_Addr_Space_B:** DMA CH 5 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.445 DMA_CH6_Block_Width_Addr_Space_B (isp_dma_DMA_CH6_Block_Width_Addr_Space_B)—Offset 41618h

DMA CH 6 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

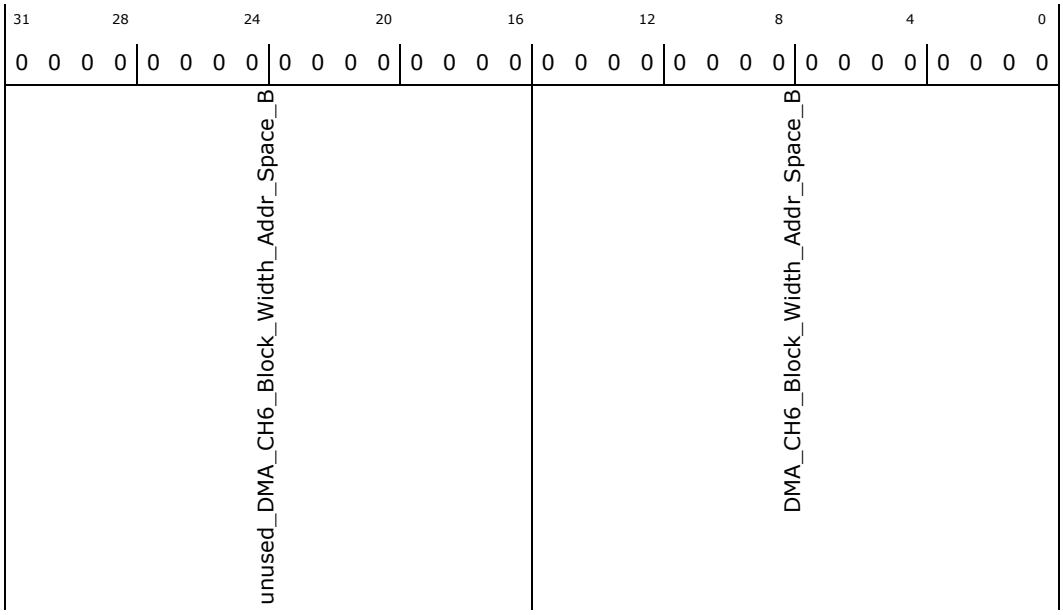
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41618h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH6_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH6_Block_Width_Addr_Space_B:** DMA CH 6 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.446 DMA_CH7_Block_Width_Addr_Space_B (isp_dma_DMA_CH7_Block_Width_Addr_Space_B)—Offset 4161Ch

DMA CH 7 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

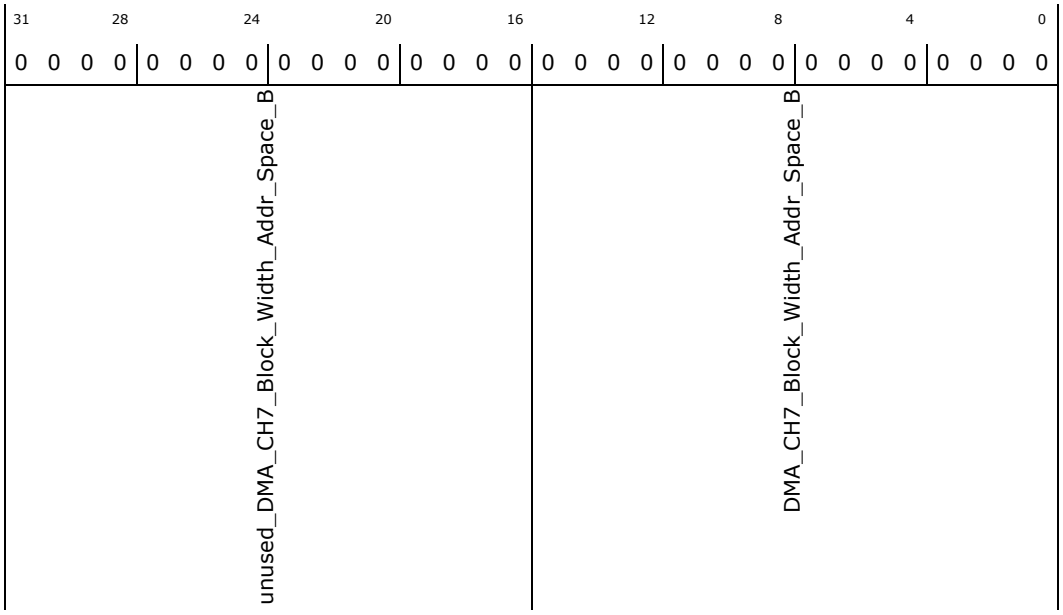
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4161Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH7_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH7_Block_Width_Addr_Space_B:** DMA CH 7 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.447 DMA_CH8_Block_Width_Addr_Space_B (isp_dma_DMA_CH8_Block_Width_Addr_Space_B)—Offset 41620h

DMA CH 8 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

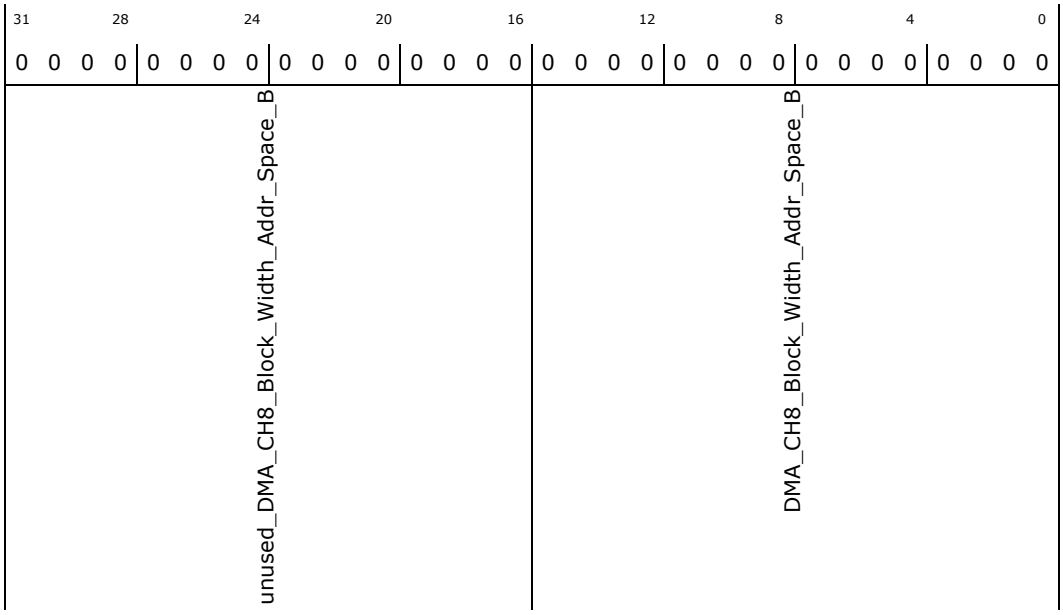
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41620h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH8_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH8_Block_Width_Addr_Space_B:** DMA CH 8 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.448 DMA_CH9_Block_Width_Addr_Space_B (isp_dma_DMA_CH9_Block_Width_Addr_Space_B)—Offset 41624h

DMA CH 9 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

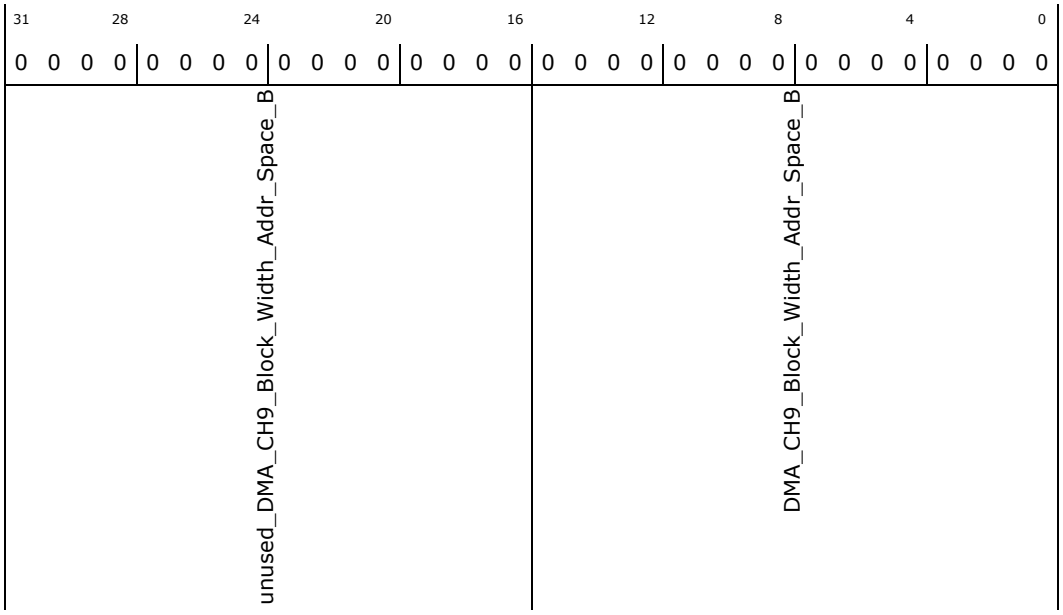
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41624h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH9_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH9_Block_Width_Addr_Space_B:** DMA CH 9 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.449 DMA_CH10_Block_Width_Addr_Space_B (isp_dma_DMA_CH10_Block_Width_Addr_Space_B)—Offset 41628h

DMA CH 10 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

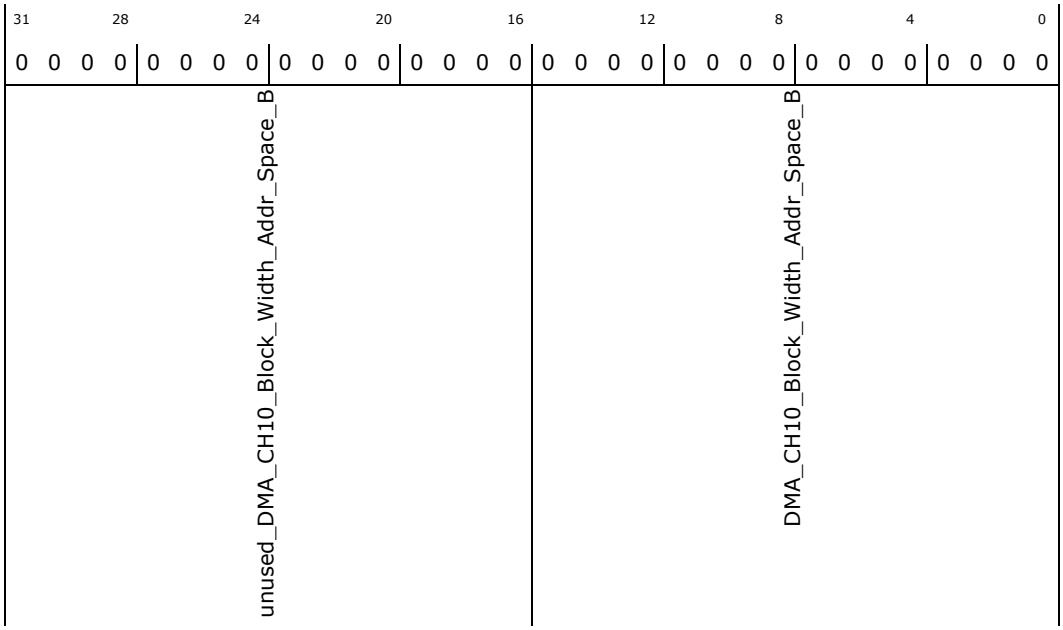
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41628h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH10_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH10_Block_Width_Addr_Space_B:** DMA CH 10 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.450 DMA_CH11_Block_Width_Addr_Space_B (isp_dma_DMA_CH11_Block_Width_Addr_Space_B)—Offset 4162Ch

DMA CH 11 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

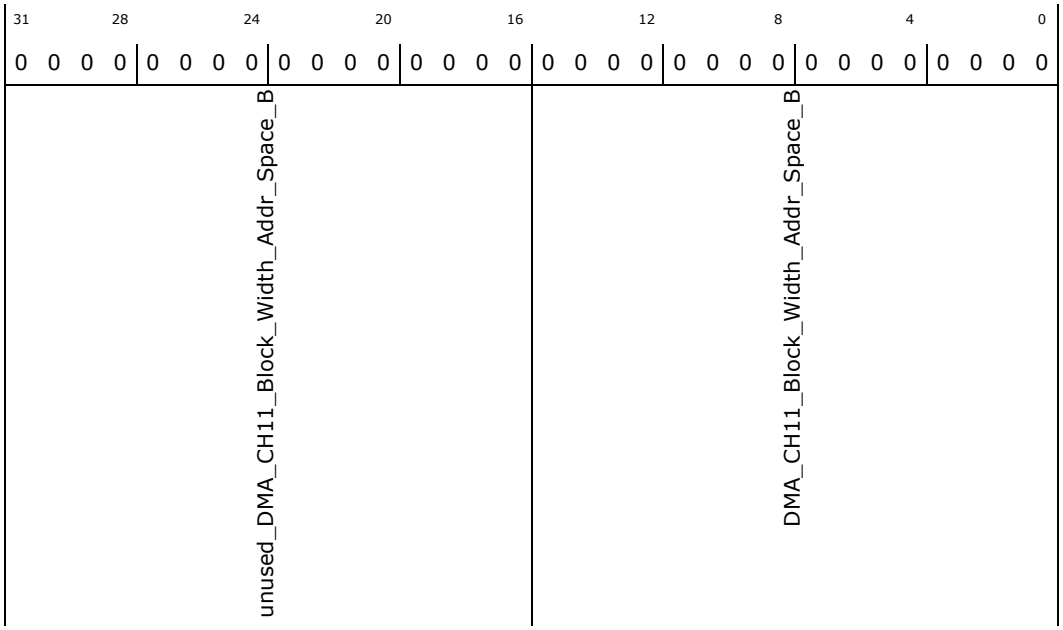
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4162Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH11_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH11_Block_Width_Addr_Space_B:** DMA CH 11 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.451 DMA_CH12_Block_Width_Addr_Space_B (isp_dma_DMA_CH12_Block_Width_Addr_Space_B)—Offset 41630h

DMA CH 12 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

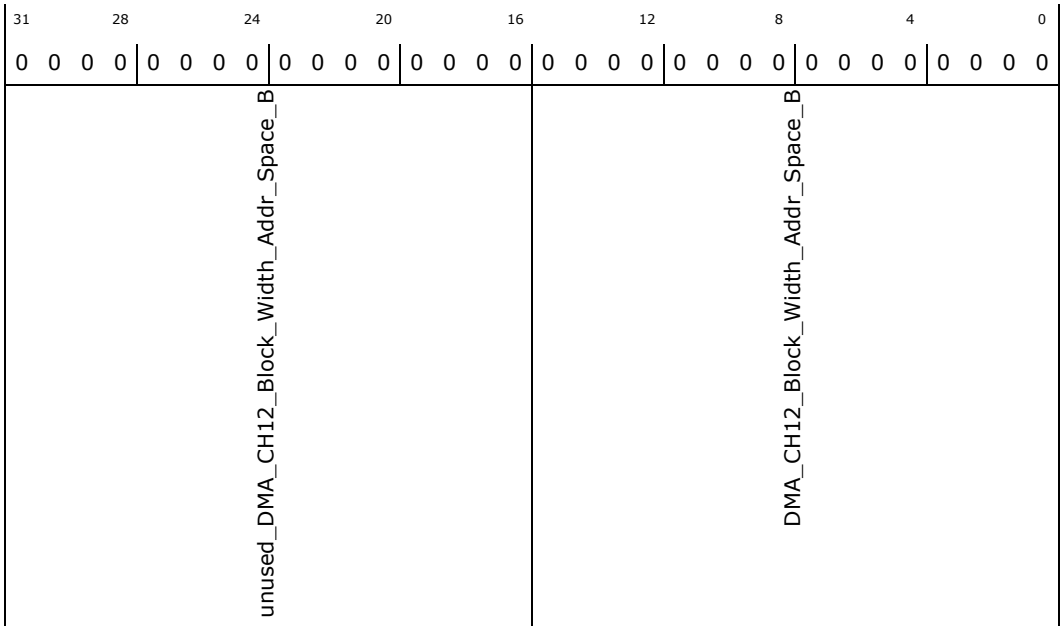
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41630h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH12_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH12_Block_Width_Addr_Space_B:** DMA CH 12 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.452 DMA_CH13_Block_Width_Addr_Space_B (isp_dma_DMA_CH13_Block_Width_Addr_Space_B)—Offset 41634h

DMA CH 13 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

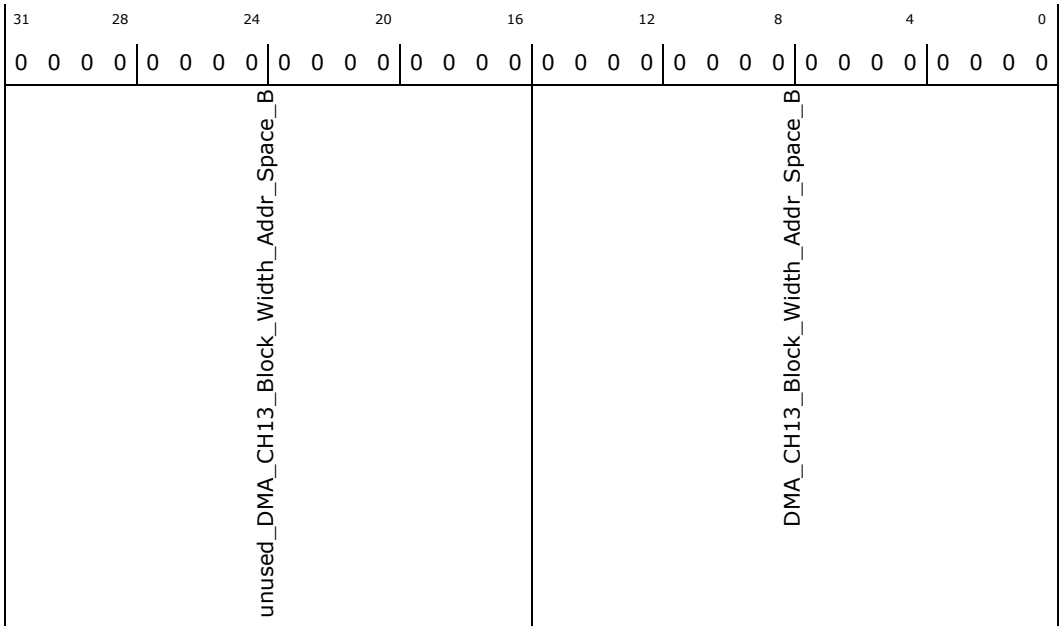
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41634h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH13_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH13_Block_Width_Addr_Space_B:** DMA CH 13 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.453 DMA_CH14_Block_Width_Addr_Space_B (isp_dma_DMA_CH14_Block_Width_Addr_Space_B)—Offset 41638h

DMA CH 14 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

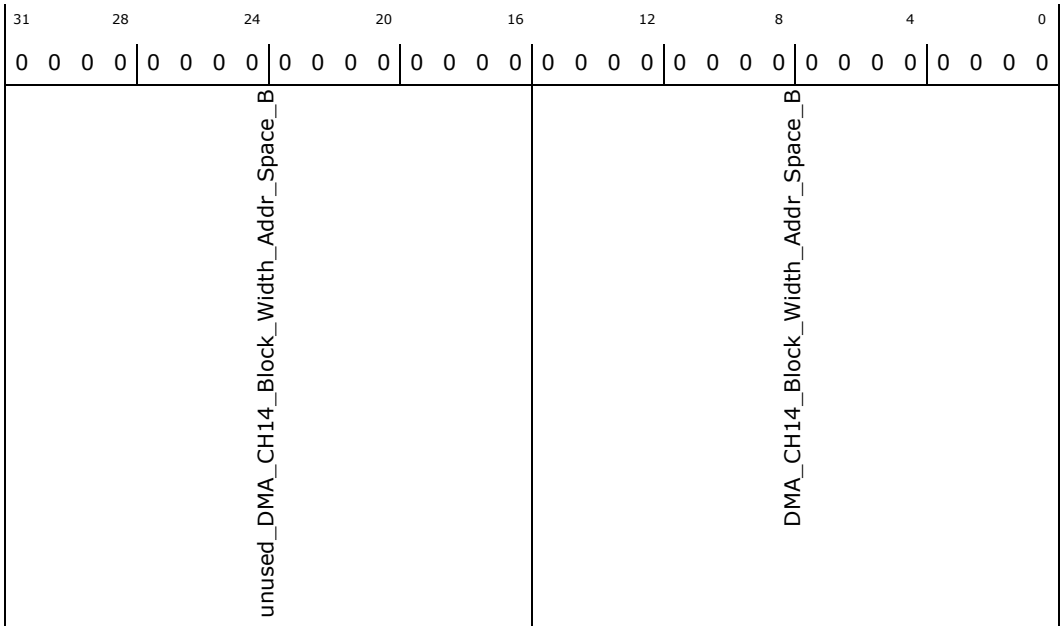
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41638h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH14_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH14_Block_Width_Addr_Space_B:** DMA CH 14 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.454 DMA_CH15_Block_Width_Addr_Space_B (isp_dma_DMA_CH15_Block_Width_Addr_Space_B)—Offset 4163Ch

DMA CH 15 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

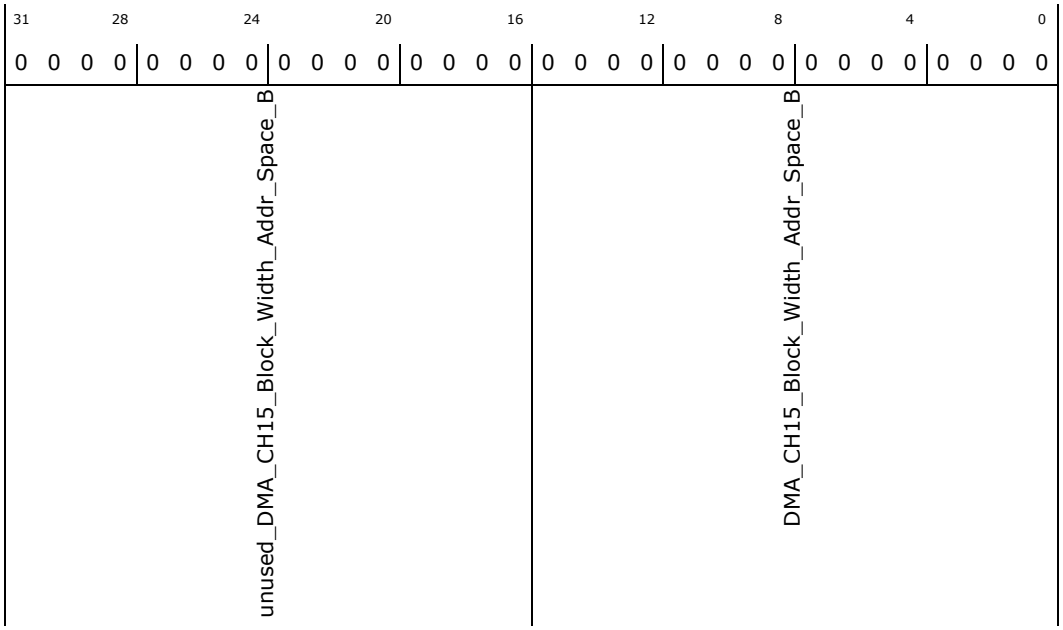
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4163Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH15_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH15_Block_Width_Addr_Space_B:** DMA CH 15 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.455 DMA_CH16_Block_Width_Addr_Space_B (isp_dma_DMA_CH16_Block_Width_Addr_Space_B)—Offset 41640h

DMA CH 16 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

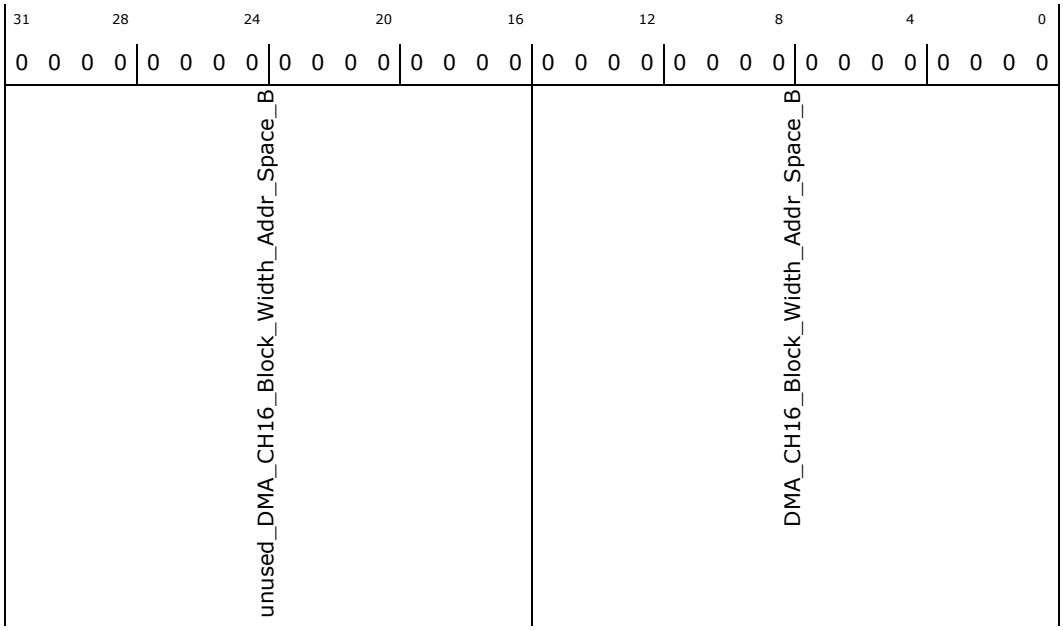
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41640h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH16_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH16_Block_Width_Addr_Space_B:** DMA CH 16 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.456 DMA_CH17_Block_Width_Addr_Space_B (isp_dma_DMA_CH17_Block_Width_Addr_Space_B)—Offset 41644h

DMA CH 17 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

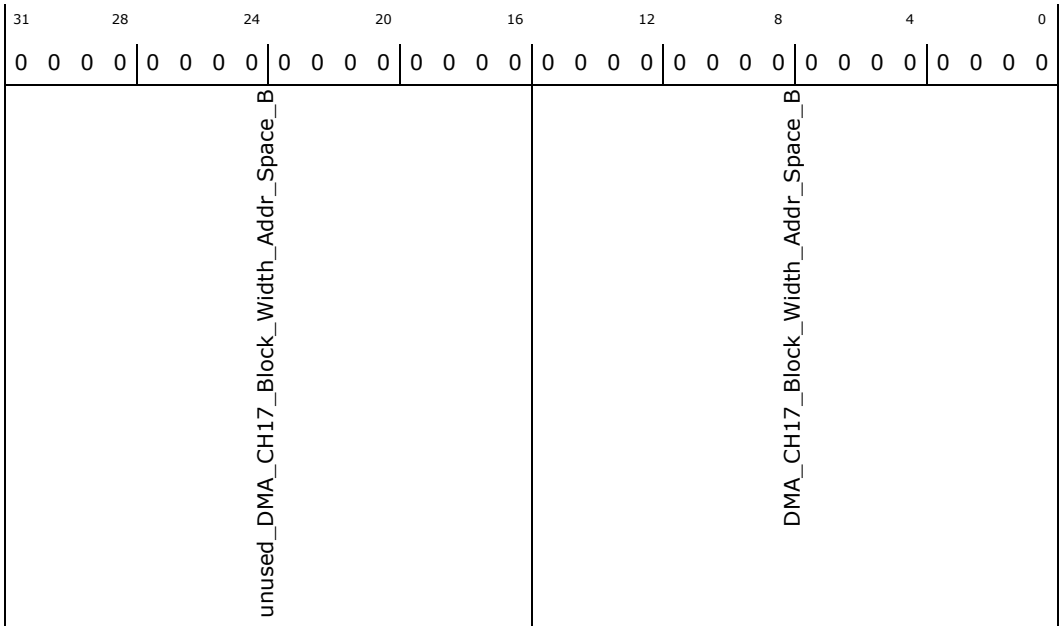
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41644h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH17_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH17_Block_Width_Addr_Space_B:** DMA CH 17 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.457 DMA_CH18_Block_Width_Addr_Space_B (isp_dma_DMA_CH18_Block_Width_Addr_Space_B)—Offset 41648h

DMA CH 18 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

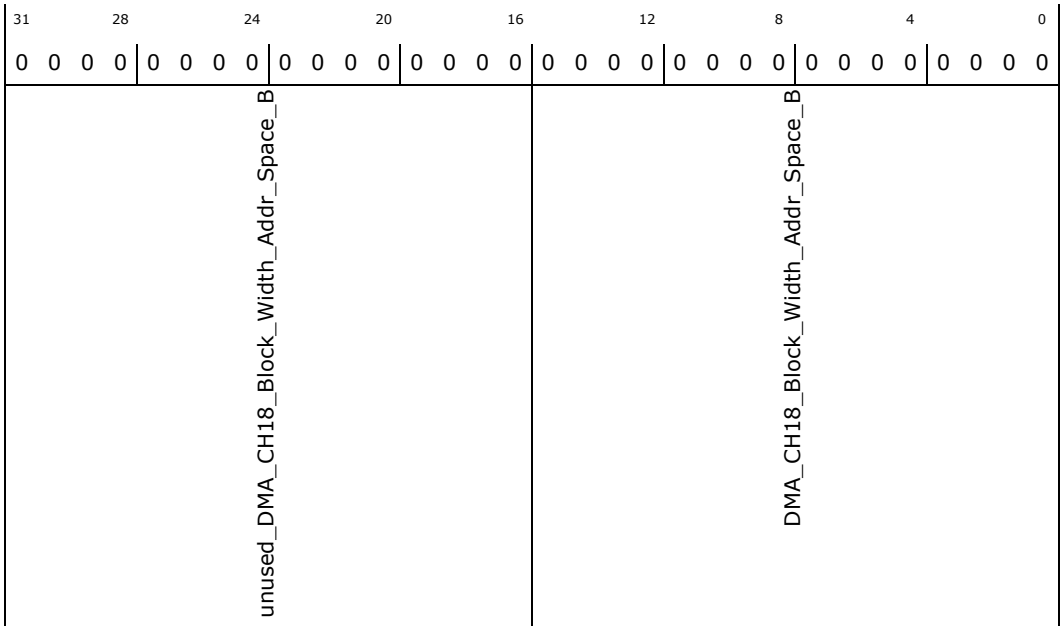
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41648h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH18_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH18_Block_Width_Addr_Space_B:** DMA CH 18 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.458 DMA_CH19_Block_Width_Addr_Space_B (isp_dma_DMA_CH19_Block_Width_Addr_Space_B)—Offset 4164Ch

DMA CH 19 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

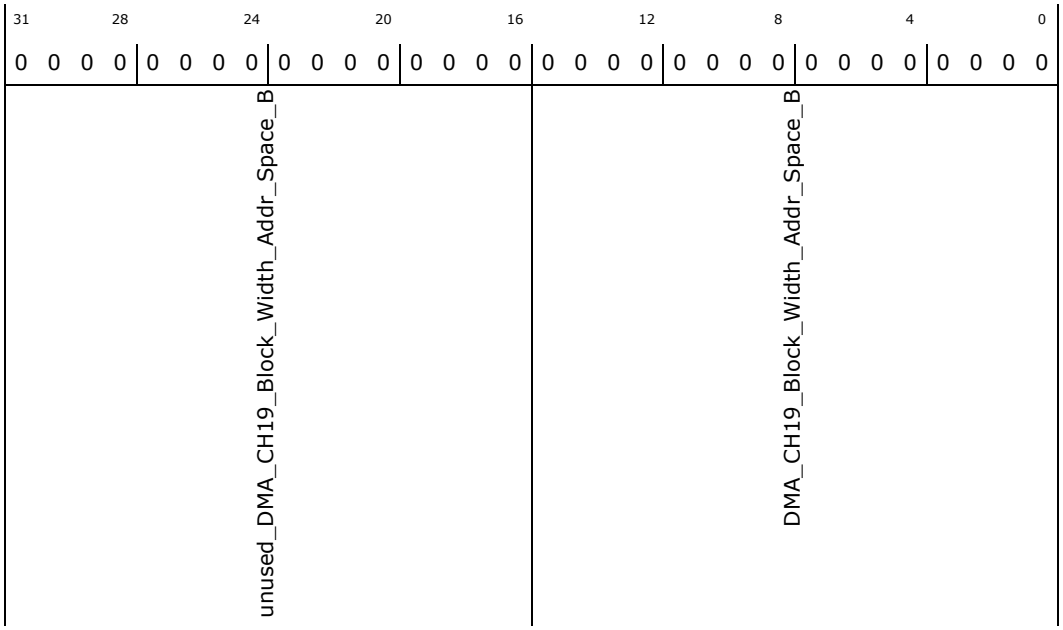
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4164Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH19_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH19_Block_Width_Addr_Space_B:** DMA CH 19 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.459 DMA_CH20_Block_Width_Addr_Space_B (isp_dma_DMA_CH20_Block_Width_Addr_Space_B)—Offset 41650h

DMA CH 20 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

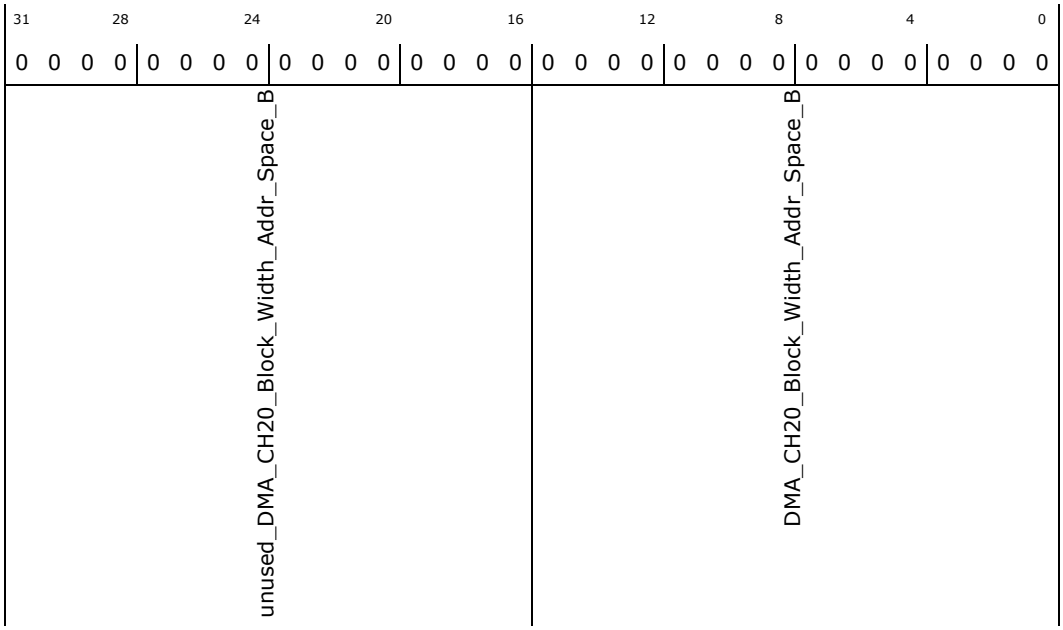
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41650h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH20_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH20_Block_Width_Addr_Space_B:** DMA CH 20 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.460 DMA_CH21_Block_Width_Addr_Space_B (isp_dma_DMA_CH21_Block_Width_Addr_Space_B)—Offset 41654h

DMA CH 21 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

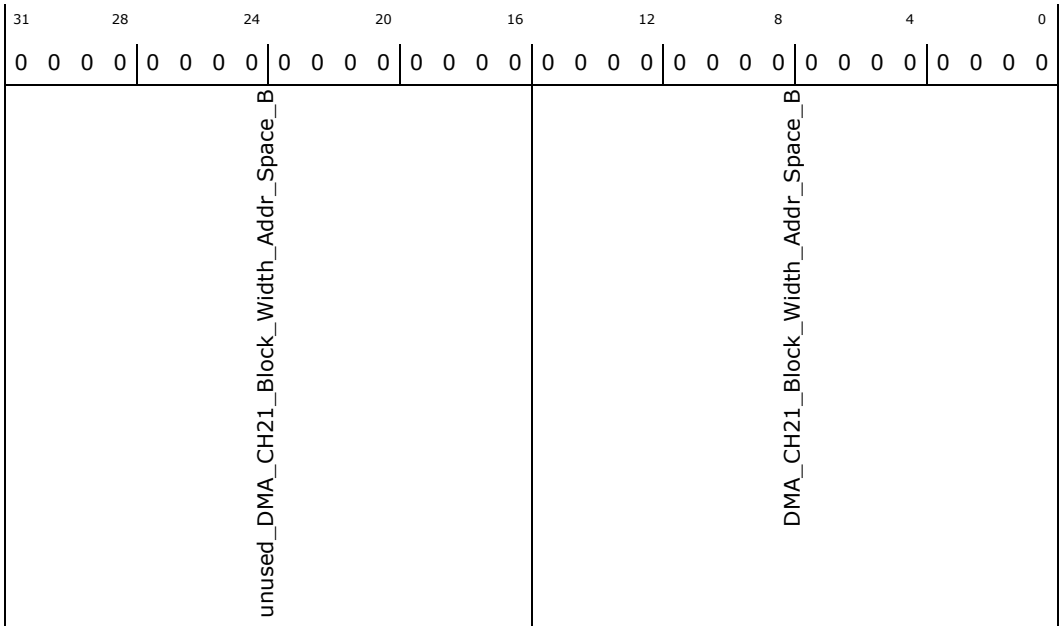
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41654h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH21_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH21_Block_Width_Addr_Space_B:** DMA CH 21 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.461 DMA_CH22_Block_Width_Addr_Space_B (isp_dma_DMA_CH22_Block_Width_Addr_Space_B)—Offset 41658h

DMA CH 22 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

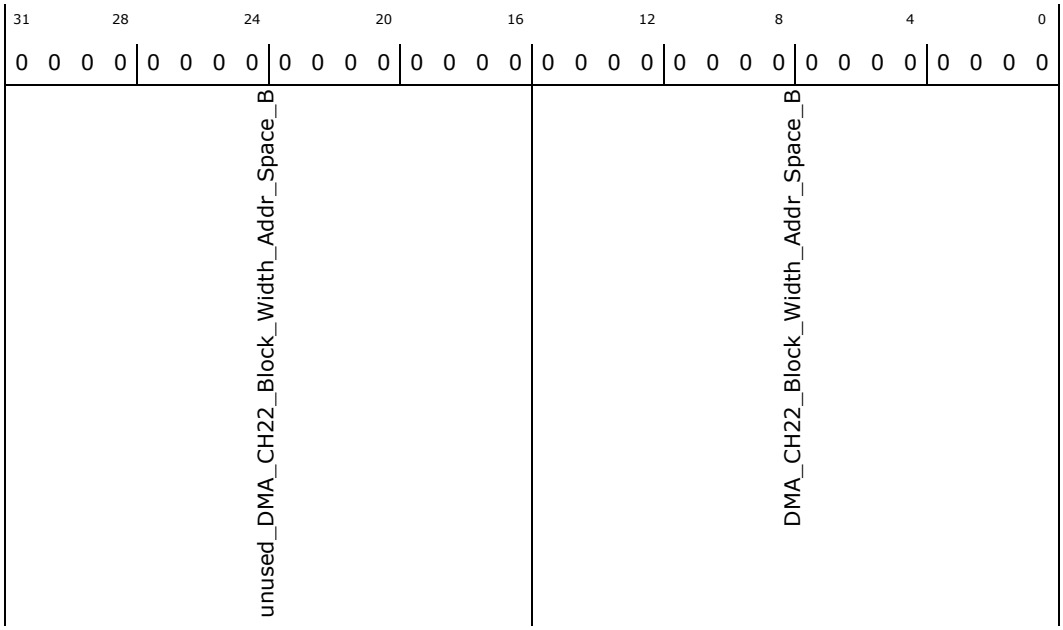
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41658h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH22_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH22_Block_Width_Addr_Space_B:** DMA CH 22 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.462 DMA_CH23_Block_Width_Addr_Space_B (isp_dma_DMA_CH23_Block_Width_Addr_Space_B)—Offset 4165Ch

DMA CH 23 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

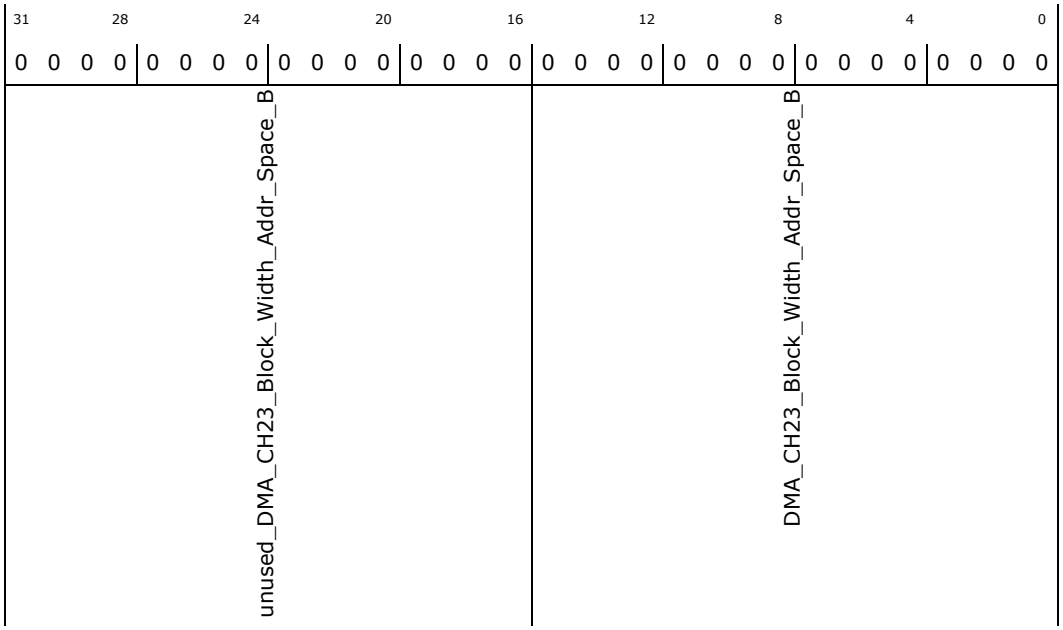
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4165Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH23_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH23_Block_Width_Addr_Space_B:** DMA CH 23 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.463 DMA_CH24_Block_Width_Addr_Space_B (isp_dma_DMA_CH24_Block_Width_Addr_Space_B)—Offset 41660h

DMA CH 24 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

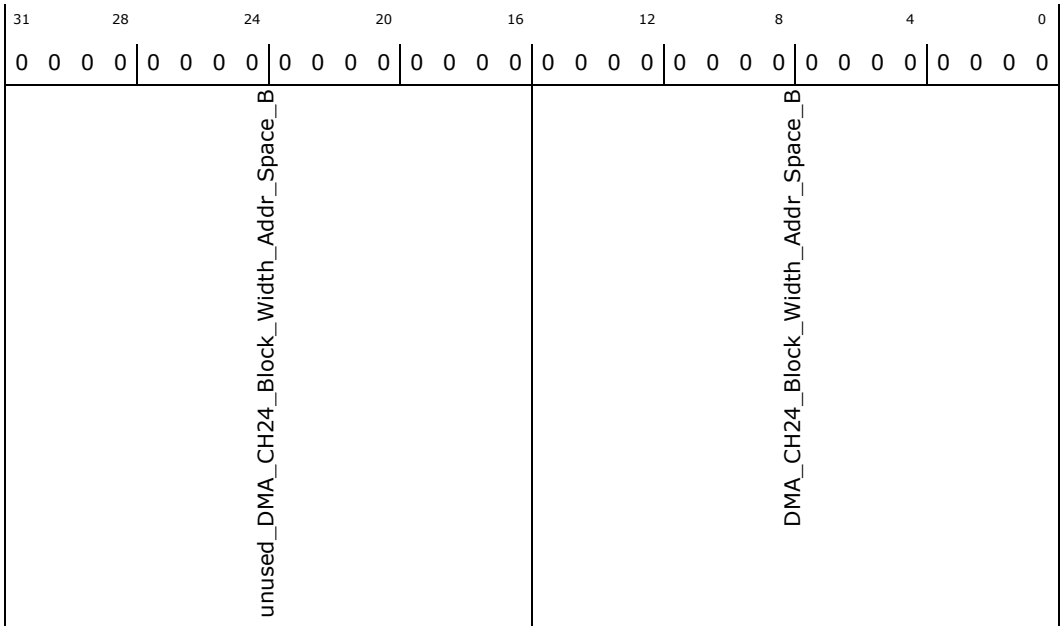
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41660h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH24_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH24_Block_Width_Addr_Space_B:** DMA CH 24 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.464 DMA_CH25_Block_Width_Addr_Space_B (isp_dma_DMA_CH25_Block_Width_Addr_Space_B)—Offset 41664h

DMA CH 25 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

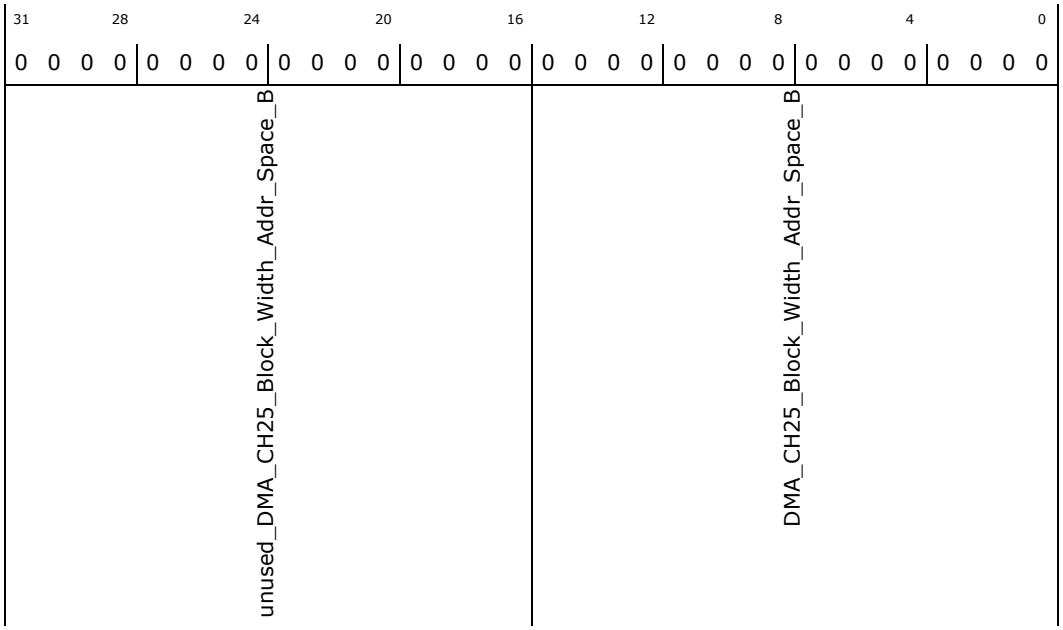
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41664h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH25_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH25_Block_Width_Addr_Space_B:** DMA CH 25 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.465 DMA_CH26_Block_Width_Addr_Space_B (isp_dma_DMA_CH26_Block_Width_Addr_Space_B)—Offset 41668h

DMA CH 26 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

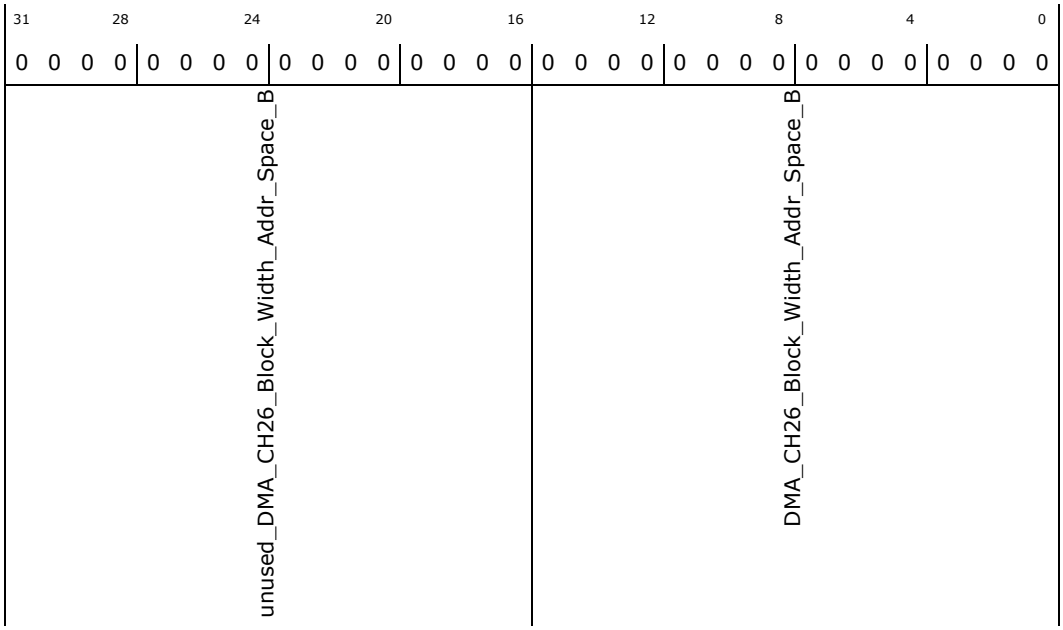
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41668h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH26_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH26_Block_Width_Addr_Space_B:** DMA CH 26 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.466 DMA_CH27_Block_Width_Addr_Space_B (isp_dma_DMA_CH27_Block_Width_Addr_Space_B)—Offset 4166Ch

DMA CH 27 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

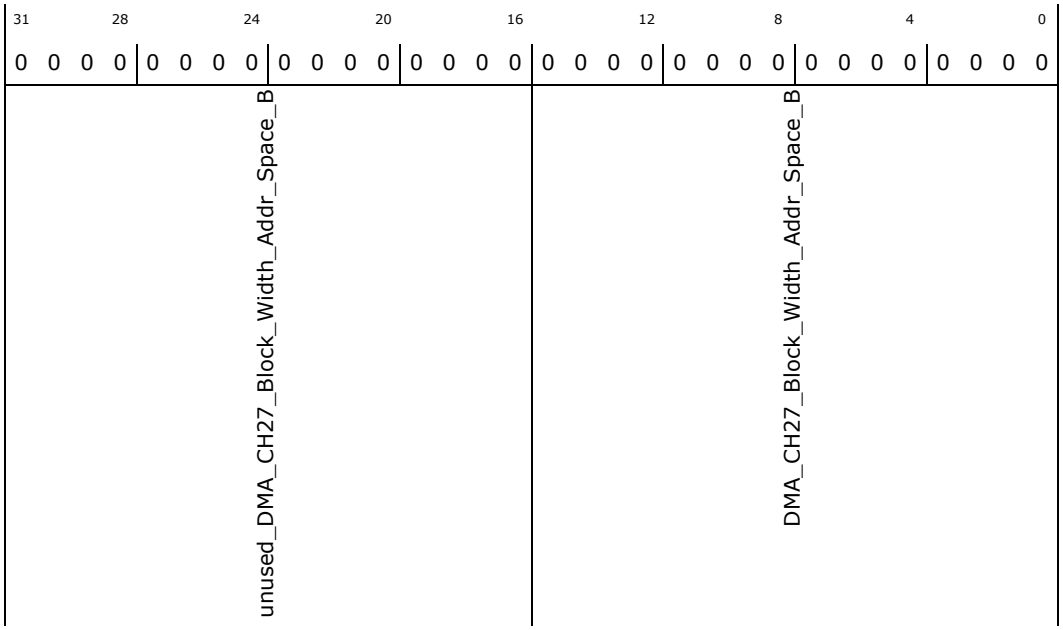
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4166Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH27_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH27_Block_Width_Addr_Space_B:** DMA CH 27 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.467 DMA_CH28_Block_Width_Addr_Space_B (isp_dma_DMA_CH28_Block_Width_Addr_Space_B)—Offset 41670h

DMA CH 28 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

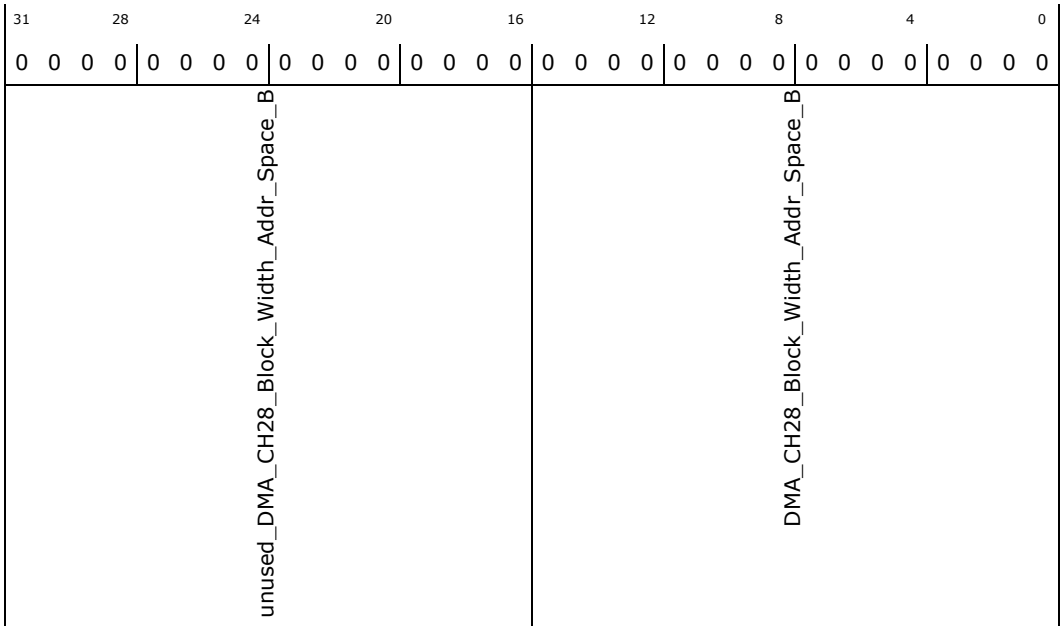
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41670h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH28_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH28_Block_Width_Addr_Space_B:** DMA CH 28 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.468 DMA_CH29_Block_Width_Addr_Space_B (isp_dma_DMA_CH29_Block_Width_Addr_Space_B)—Offset 41674h

DMA CH 29 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

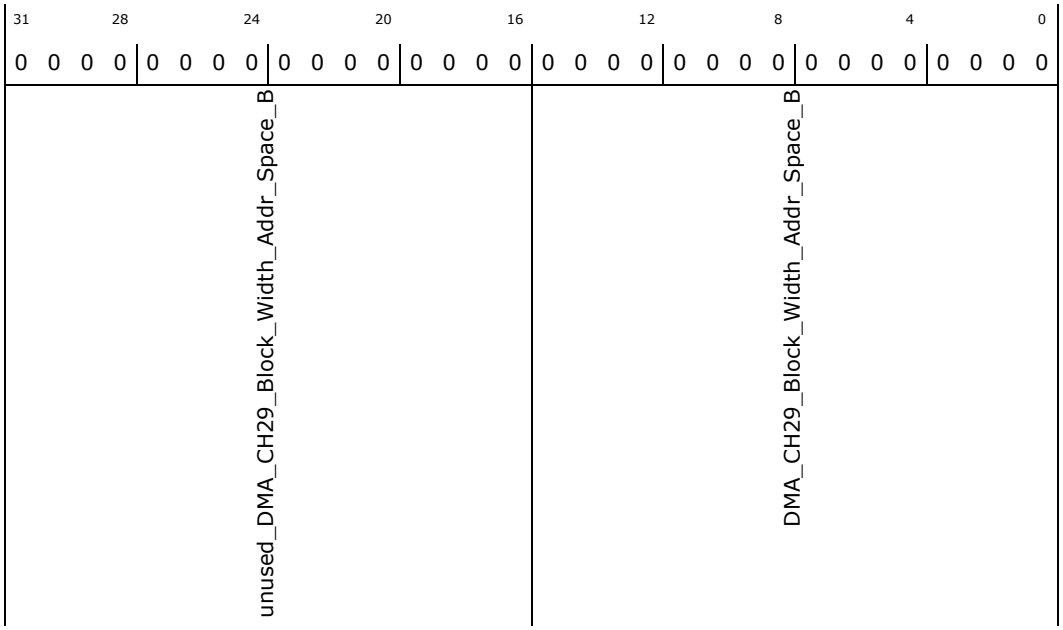
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41674h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH29_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH29_Block_Width_Addr_Space_B:** DMA CH 29 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.469 DMA_CH30_Block_Width_Addr_Space_B (isp_dma_DMA_CH30_Block_Width_Addr_Space_B)—Offset 41678h

DMA CH 30 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

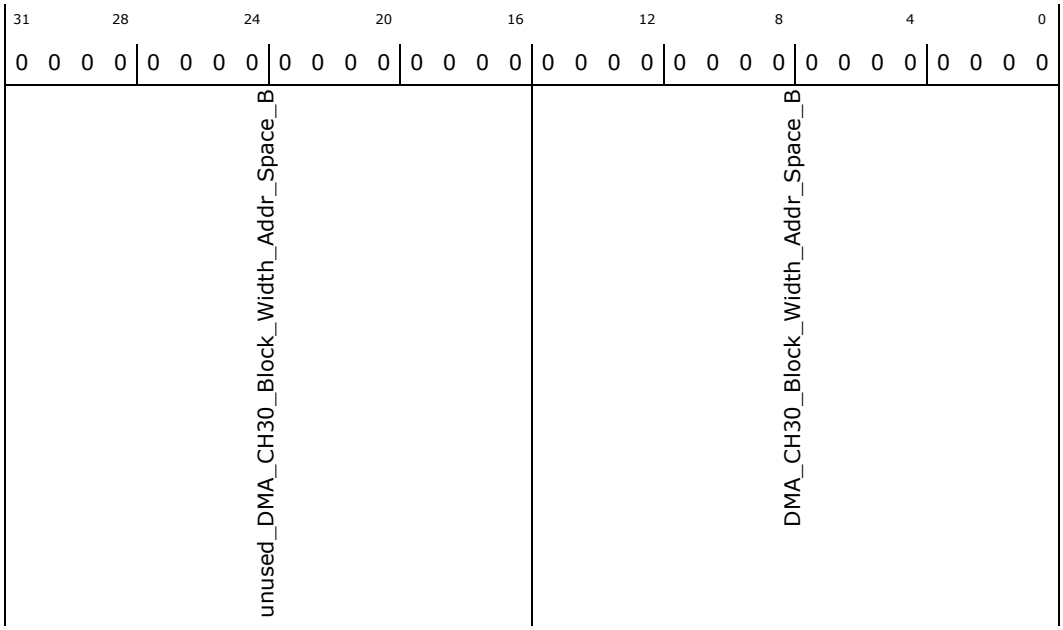
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41678h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH30_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH30_Block_Width_Addr_Space_B:** DMA CH 30 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.470 DMA_CH31_Block_Width_Addr_Space_B (isp_dma_DMA_CH31_Block_Width_Addr_Space_B)—Offset 4167Ch

DMA CH 31 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

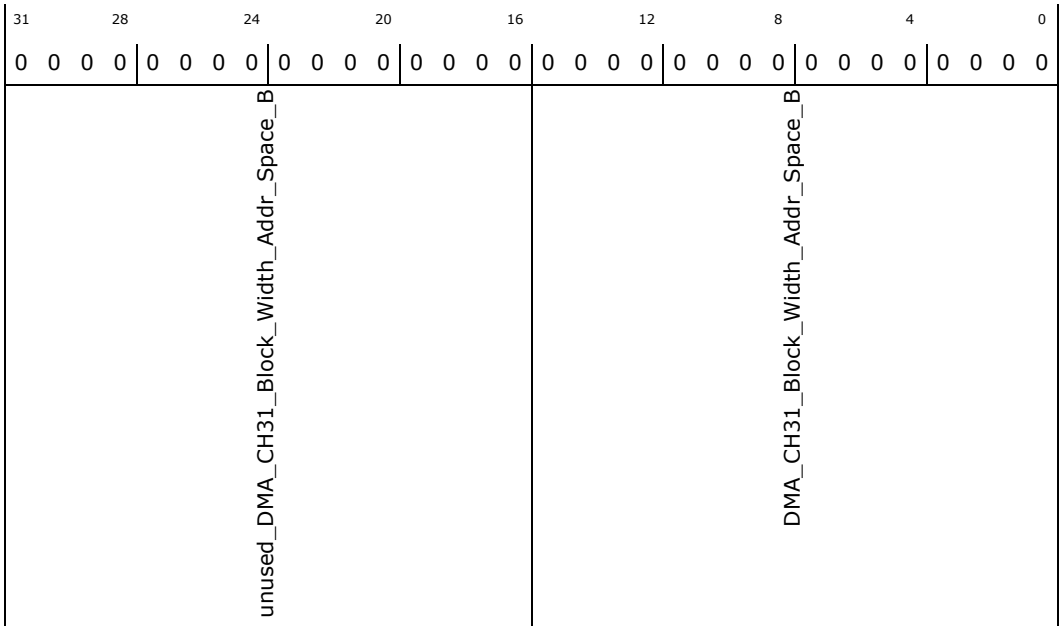
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4167Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH31_Block_Width_Addr_Space_B):** Unused
15:0	0x0 RO	**DMA_CH31_Block_Width_Addr_Space_B:** DMA CH 31 PARAM 6: Block Width (Xb) for Device B side of the connection in terms of Device B words.

5.2.471 DMA_CH0_Block_Height (isp_dma_DMA_CH0_Block_Height)—Offset 41700h

DMA CH 0 PARAM 7: block height (Yb), in terms of lines

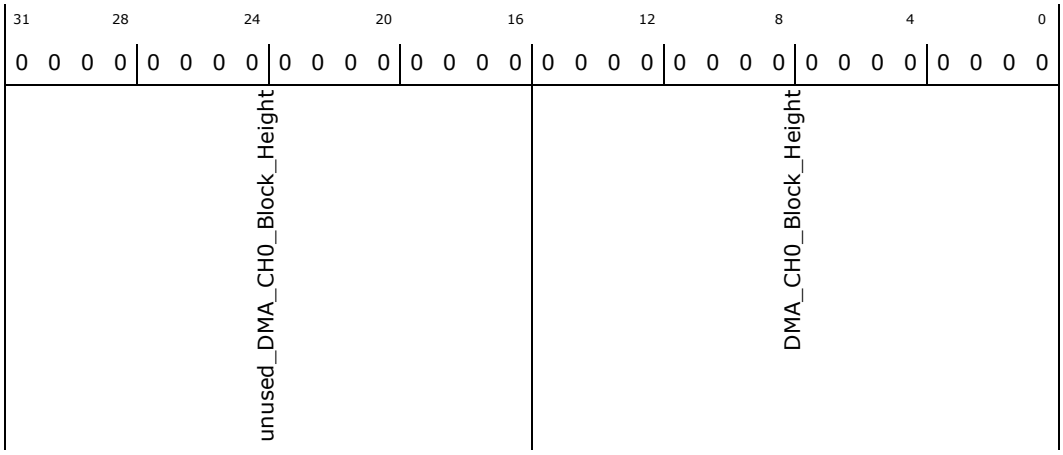
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41700h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH0_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH0_Block_Height:** DMA CH 0 PARAM 7: block height (Yb), in terms of lines

5.2.472 DMA_CH1_Block_Height (isp_dma_DMA_CH1_Block_Height)—Offset 41704h

DMA CH 1 PARAM 7: block height (Yb), in terms of lines

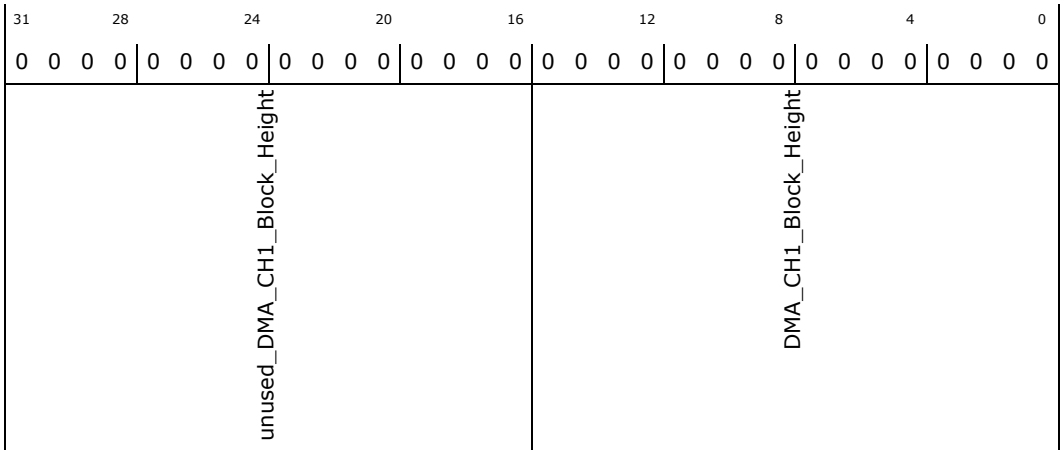
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41704h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH1_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH1_Block_Height:** DMA CH 1 PARAM 7: block height (Yb), in terms of lines

5.2.473 DMA_CH2_Block_Height (isp_dma_DMA_CH2_Block_Height)—Offset 41708h

DMA CH 2 PARAM 7: block height (Yb), in terms of lines

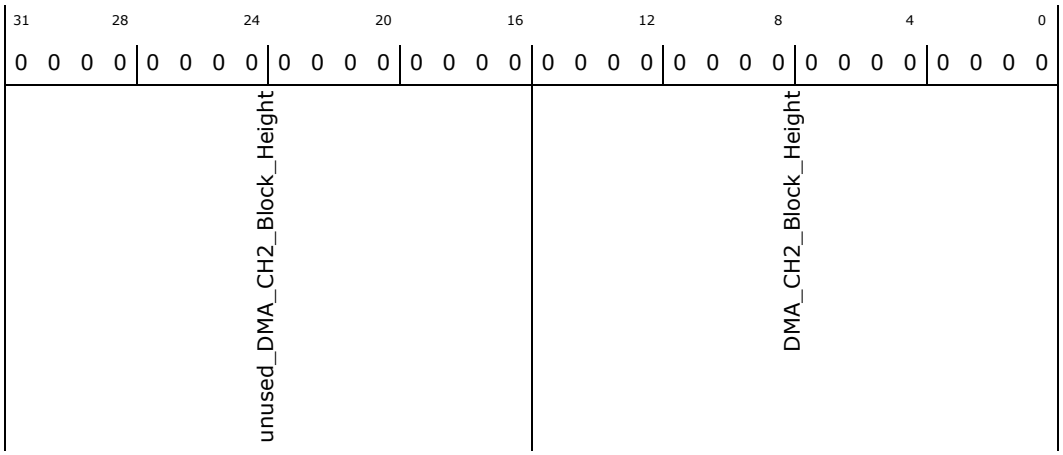
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41708h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH2_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH2_Block_Height:** DMA CH 2 PARAM 7: block height (Yb), in terms of lines

5.2.474 DMA_CH3_Block_Height (isp_dma_DMA_CH3_Block_Height)—Offset 4170Ch

DMA CH 3 PARAM 7: block height (Yb), in terms of lines

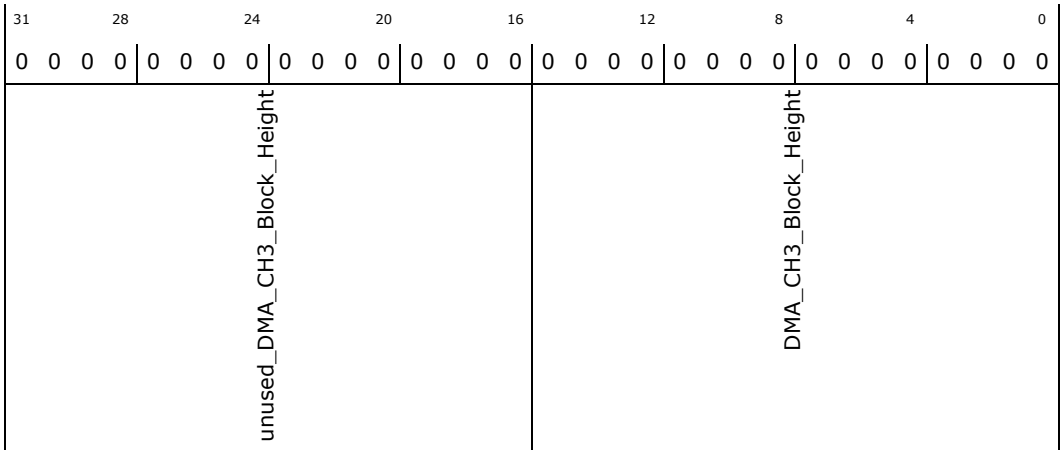
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4170Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH3_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH3_Block_Height:** DMA CH 3 PARAM 7: block height (Yb), in terms of lines

5.2.475 DMA_CH4_Block_Height (isp_dma_DMA_CH4_Block_Height)—Offset 41710h

DMA CH 4 PARAM 7: block height (Yb), in terms of lines

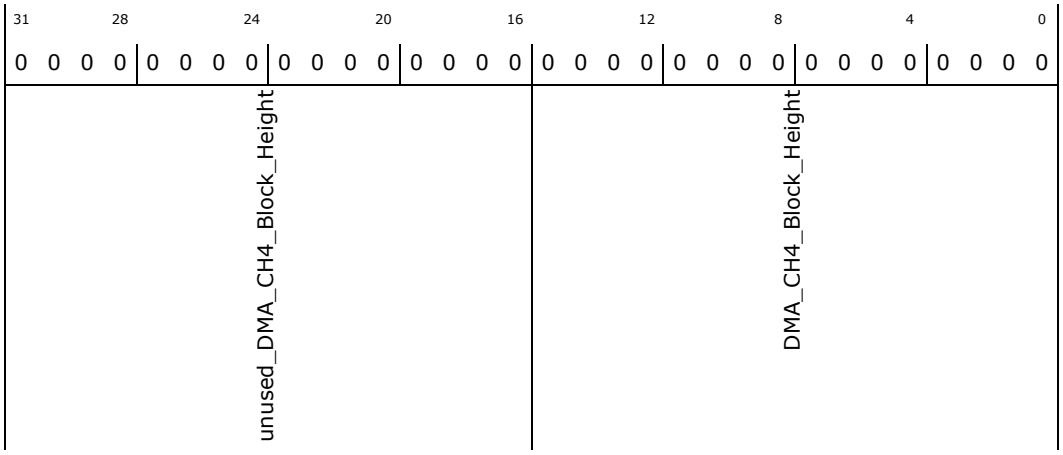
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41710h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH4_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH4_Block_Height:** DMA CH 4 PARAM 7: block height (Yb), in terms of lines

5.2.476 DMA_CH5_Block_Height (isp_dma_DMA_CH5_Block_Height)—Offset 41714h

DMA CH 5 PARAM 7: block height (Yb), in terms of lines

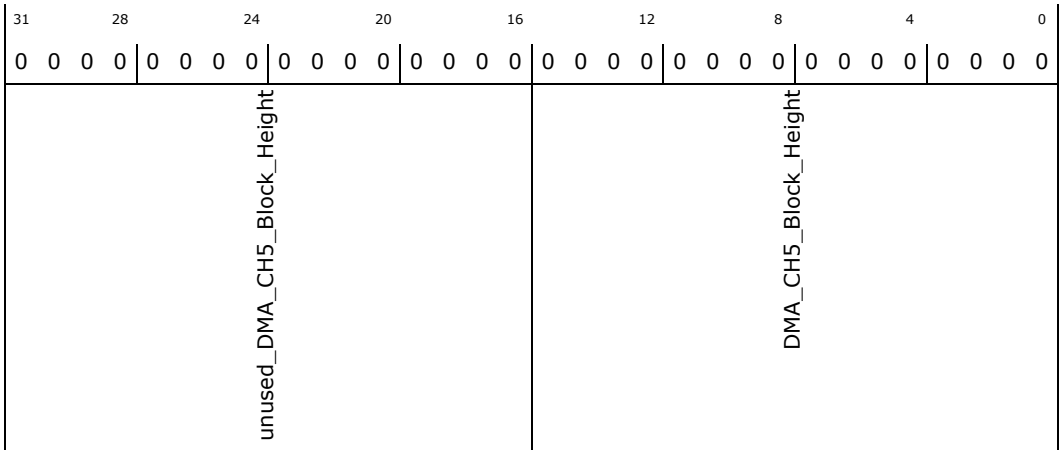
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41714h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH5_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH5_Block_Height:** DMA CH 5 PARAM 7: block height (Yb), in terms of lines

5.2.477 DMA_CH6_Block_Height (isp_dma_DMA_CH6_Block_Height)—Offset 41718h

DMA CH 6 PARAM 7: block height (Yb), in terms of lines

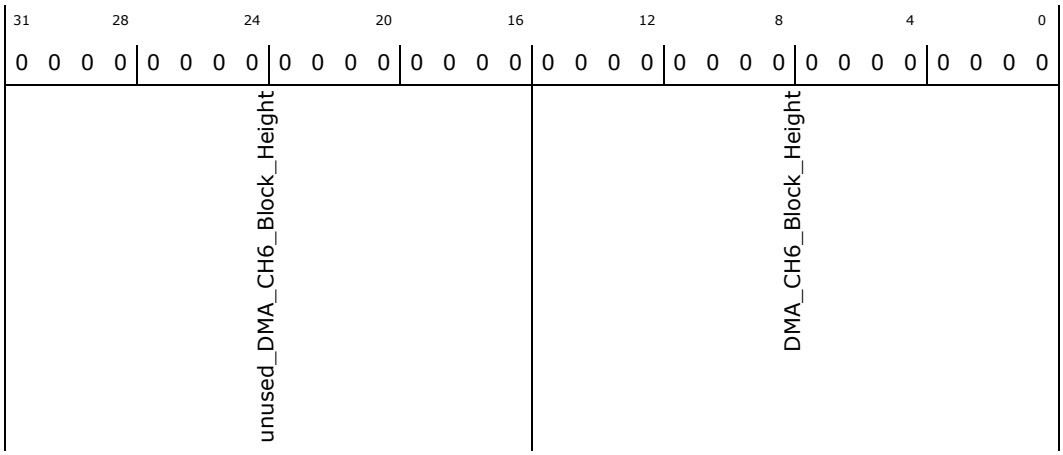
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41718h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH6_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH6_Block_Height:** DMA CH 6 PARAM 7: block height (Yb), in terms of lines

5.2.478 DMA_CH7_Block_Height (isp_dma_DMA_CH7_Block_Height)—Offset 4171Ch

DMA CH 7 PARAM 7: block height (Yb), in terms of lines

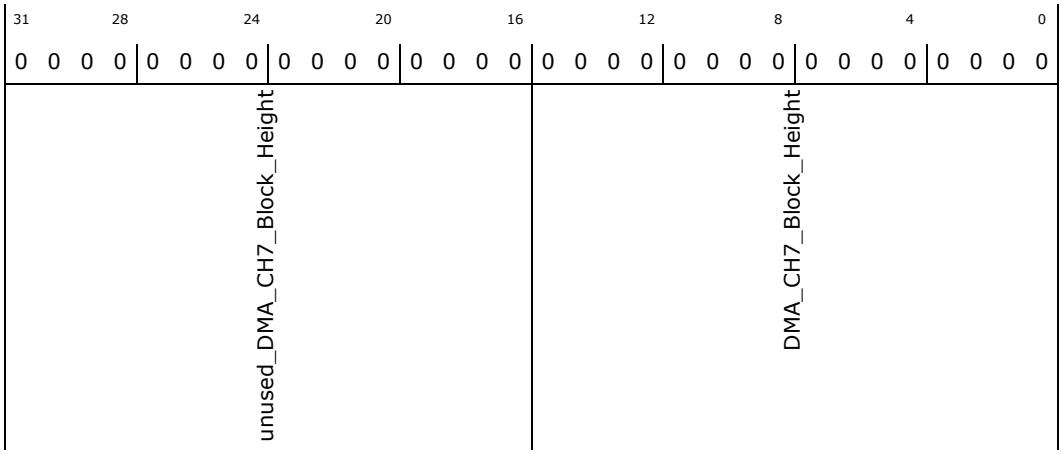
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4171Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH7_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH7_Block_Height:** DMA CH 7 PARAM 7: block height (Yb), in terms of lines

5.2.479 DMA_CH8_Block_Height (isp_dma_DMA_CH8_Block_Height)—Offset 41720h

DMA CH 8 PARAM 7: block height (Yb), in terms of lines

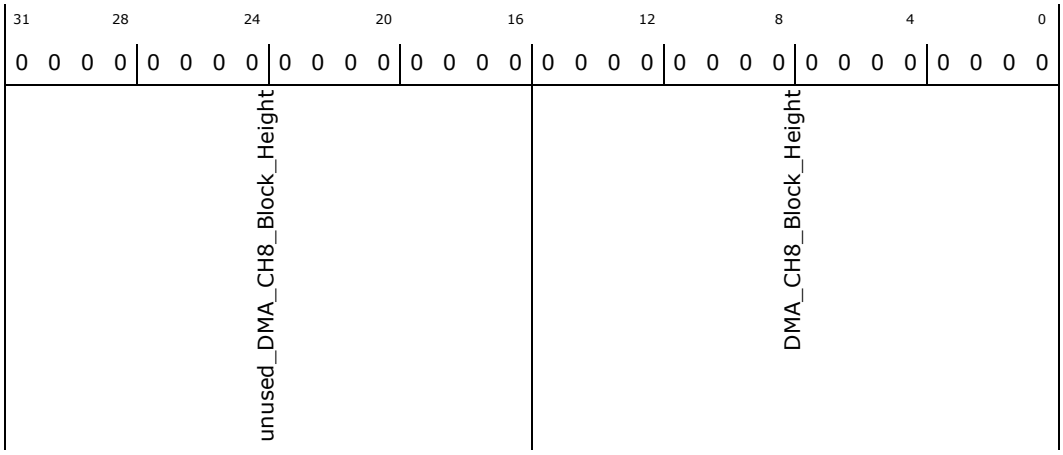
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41720h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH8_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH8_Block_Height:** DMA CH 8 PARAM 7: block height (Yb), in terms of lines

5.2.480 DMA_CH9_Block_Height (isp_dma_DMA_CH9_Block_Height)—Offset 41724h

DMA CH 9 PARAM 7: block height (Yb), in terms of lines

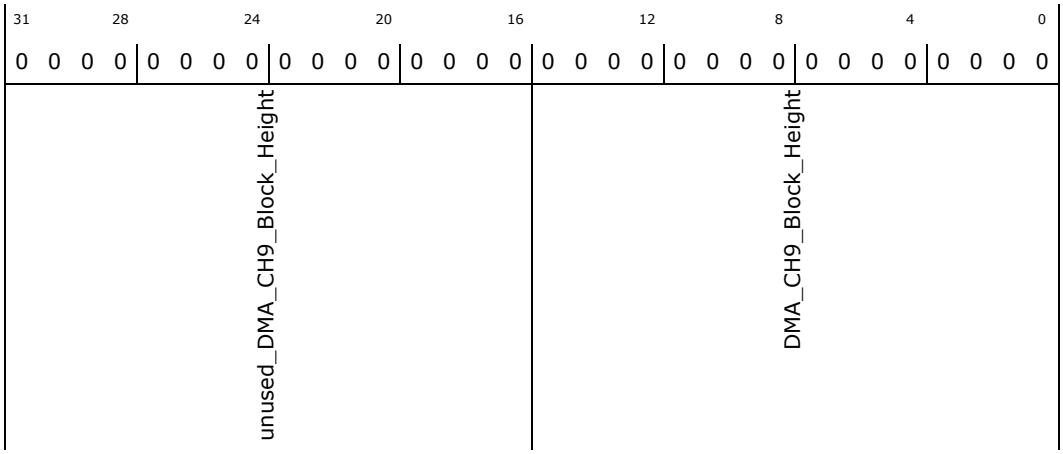
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41724h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH9_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH9_Block_Height:** DMA CH 9 PARAM 7: block height (Yb), in terms of lines

5.2.481 DMA_CH10_Block_Height (isp_dma_DMA_CH10_Block_Height)—Offset 41728h

DMA CH 10 PARAM 7: block height (Yb), in terms of lines

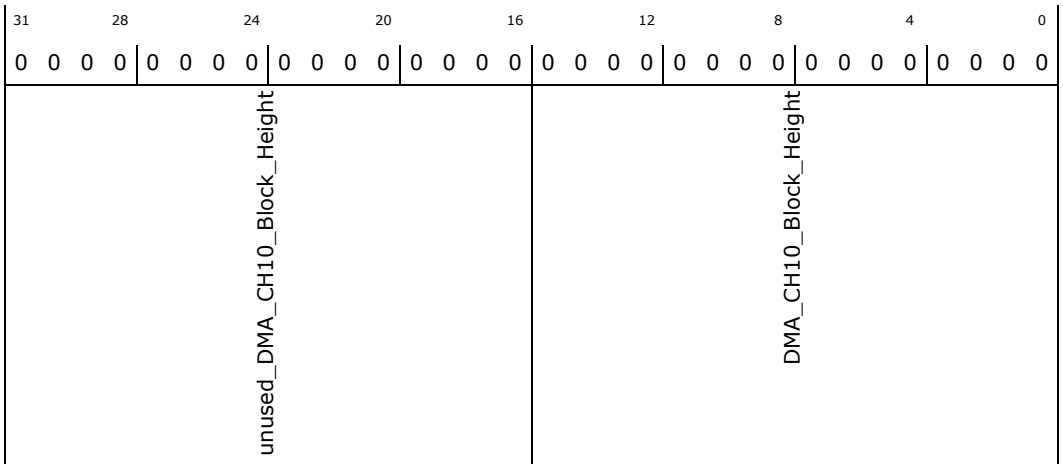
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41728h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH10_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH10_Block_Height:** DMA CH 10 PARAM 7: block height (Yb), in terms of lines

5.2.482 DMA_CH11_Block_Height (isp_dma_DMA_CH11_Block_Height)—Offset 4172Ch

DMA CH 11 PARAM 7: block height (Yb), in terms of lines

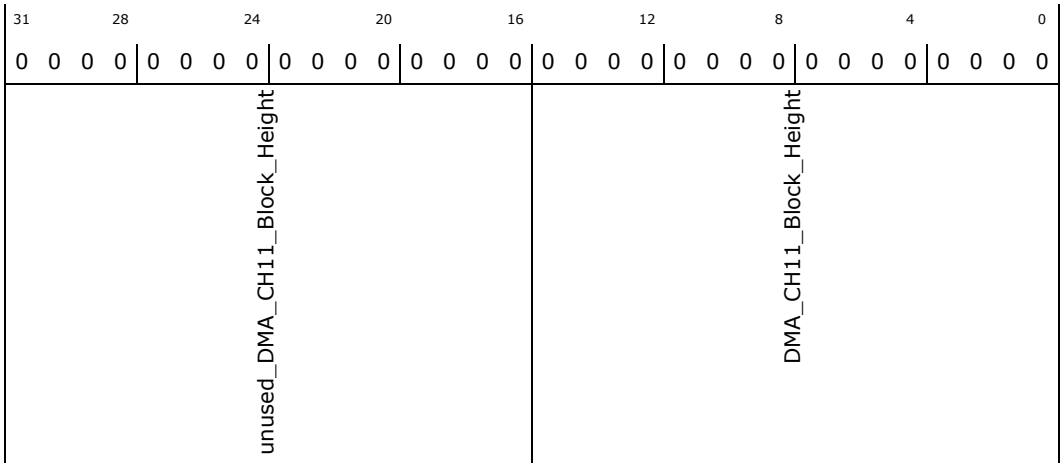
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4172Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH11_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH11_Block_Height:** DMA CH 11 PARAM 7: block height (Yb), in terms of lines

5.2.483 DMA_CH12_Block_Height (isp_dma_DMA_CH12_Block_Height)—Offset 41730h

DMA CH 12 PARAM 7: block height (Yb), in terms of lines

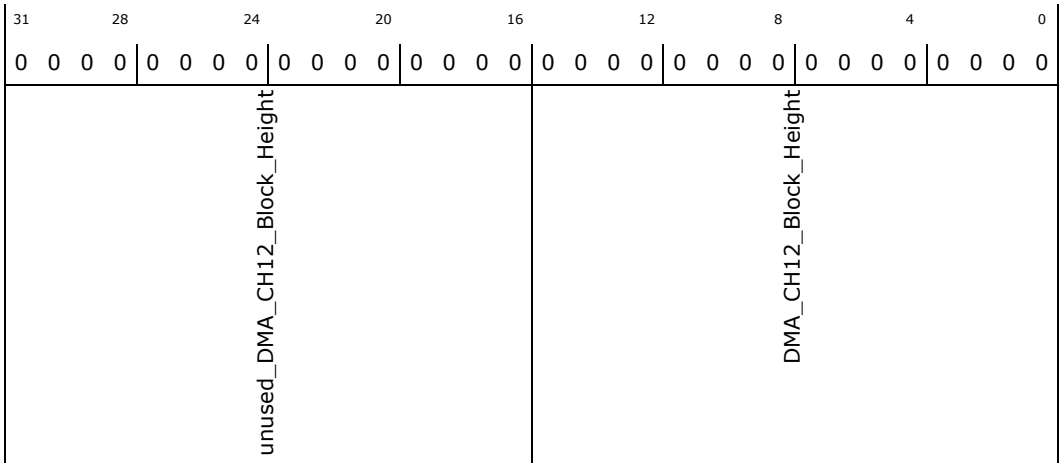
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41730h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH12_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH12_Block_Height:** DMA CH 12 PARAM 7: block height (Yb), in terms of lines

5.2.484 DMA_CH13_Block_Height (isp_dma_DMA_CH13_Block_Height)—Offset 41734h

DMA CH 13 PARAM 7: block height (Yb), in terms of lines

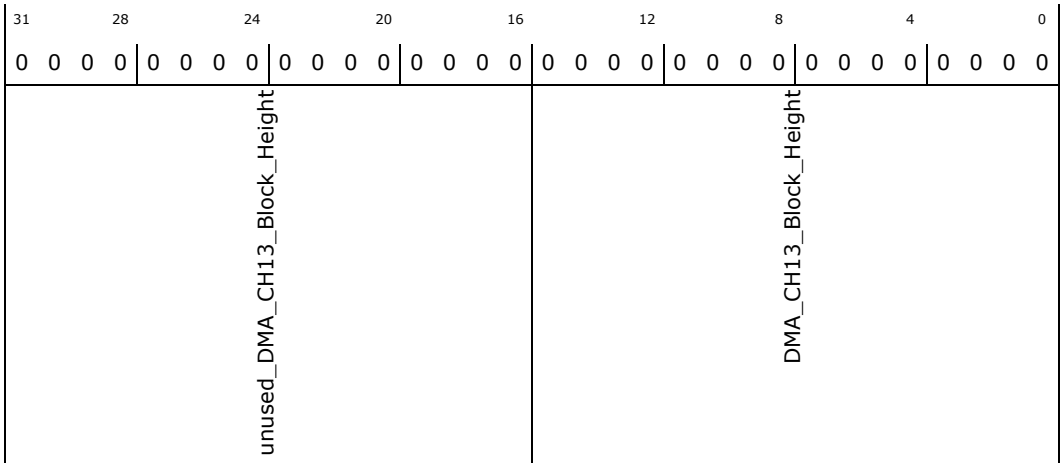
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41734h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH13_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH13_Block_Height:** DMA CH 13 PARAM 7: block height (Yb), in terms of lines

5.2.485 DMA_CH14_Block_Height (isp_dma_DMA_CH14_Block_Height)—Offset 41738h

DMA CH 14 PARAM 7: block height (Yb), in terms of lines

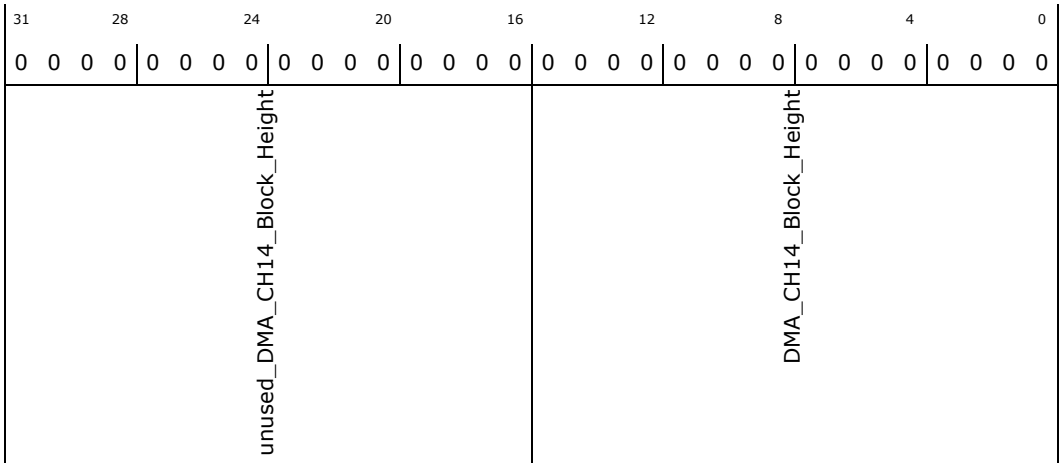
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41738h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH14_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH14_Block_Height:** DMA CH 14 PARAM 7: block height (Yb), in terms of lines

5.2.486 DMA_CH15_Block_Height (isp_dma_DMA_CH15_Block_Height)—Offset 4173Ch

DMA CH 15 PARAM 7: block height (Yb), in terms of lines

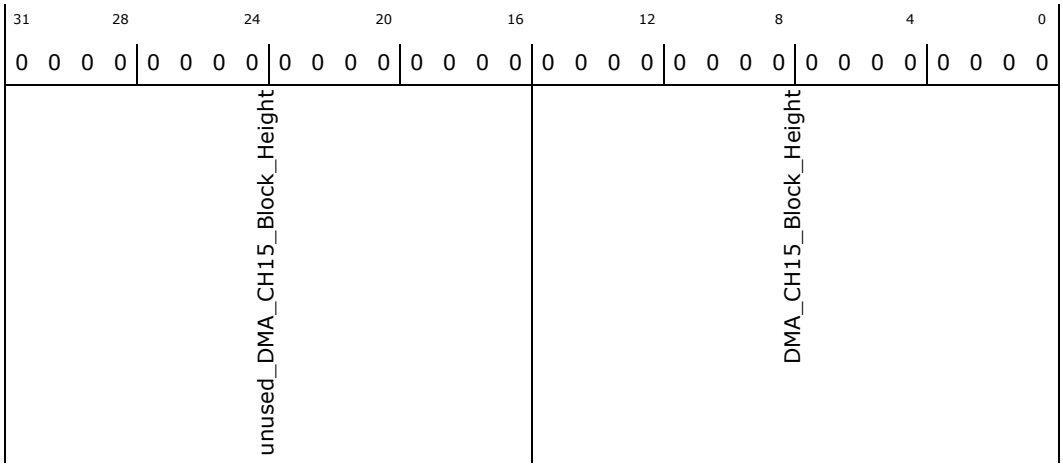
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4173Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH15_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH15_Block_Height:** DMA CH 15 PARAM 7: block height (Yb), in terms of lines

5.2.487 DMA_CH16_Block_Height (isp_dma_DMA_CH16_Block_Height)—Offset 41740h

DMA CH 16 PARAM 7: block height (Yb), in terms of lines

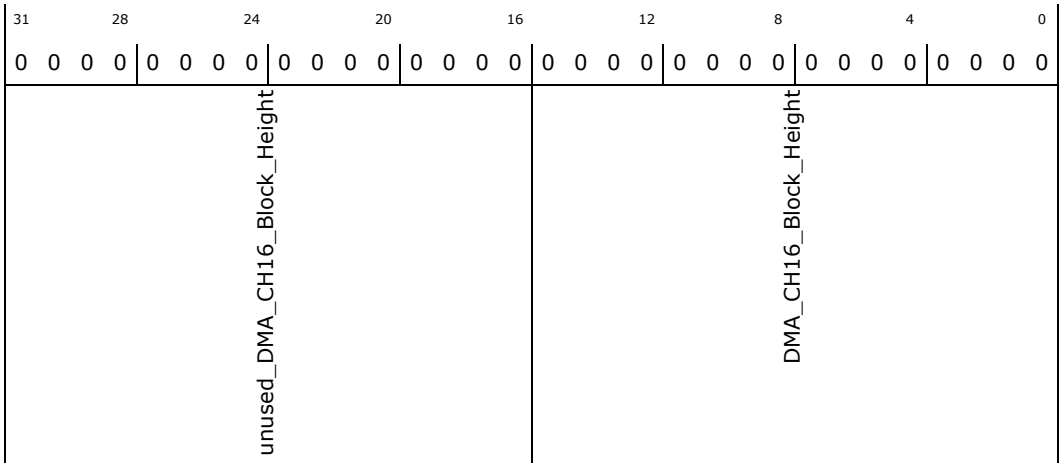
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41740h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH16_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH16_Block_Height:** DMA CH 16 PARAM 7: block height (Yb), in terms of lines

5.2.488 DMA_CH17_Block_Height (isp_dma_DMA_CH17_Block_Height)—Offset 41744h

DMA CH 17 PARAM 7: block height (Yb), in terms of lines

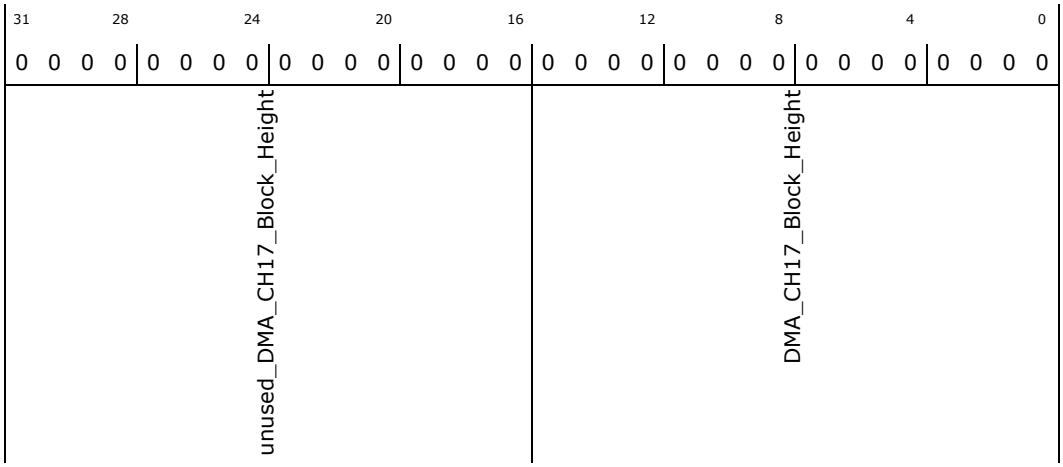
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41744h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH17_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH17_Block_Height:** DMA CH 17 PARAM 7: block height (Yb), in terms of lines

5.2.489 DMA_CH18_Block_Height (isp_dma_DMA_CH18_Block_Height)—Offset 41748h

DMA CH 18 PARAM 7: block height (Yb), in terms of lines

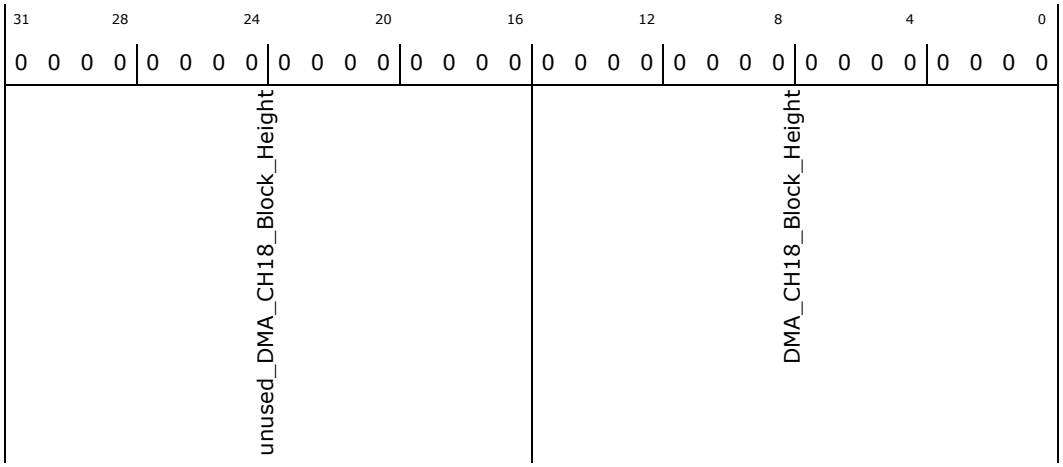
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41748h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH18_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH18_Block_Height:** DMA CH 18 PARAM 7: block height (Yb), in terms of lines

5.2.490 DMA_CH19_Block_Height (isp_dma_DMA_CH19_Block_Height)—Offset 4174Ch

DMA CH 19 PARAM 7: block height (Yb), in terms of lines

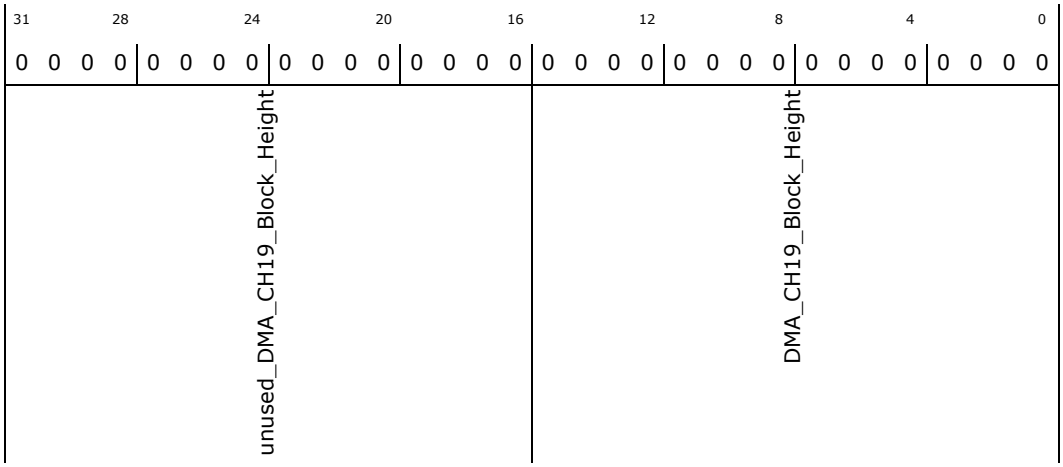
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4174Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH19_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH19_Block_Height:** DMA CH 19 PARAM 7: block height (Yb), in terms of lines

5.2.491 DMA_CH20_Block_Height (isp_dma_DMA_CH20_Block_Height)—Offset 41750h

DMA CH 20 PARAM 7: block height (Yb), in terms of lines

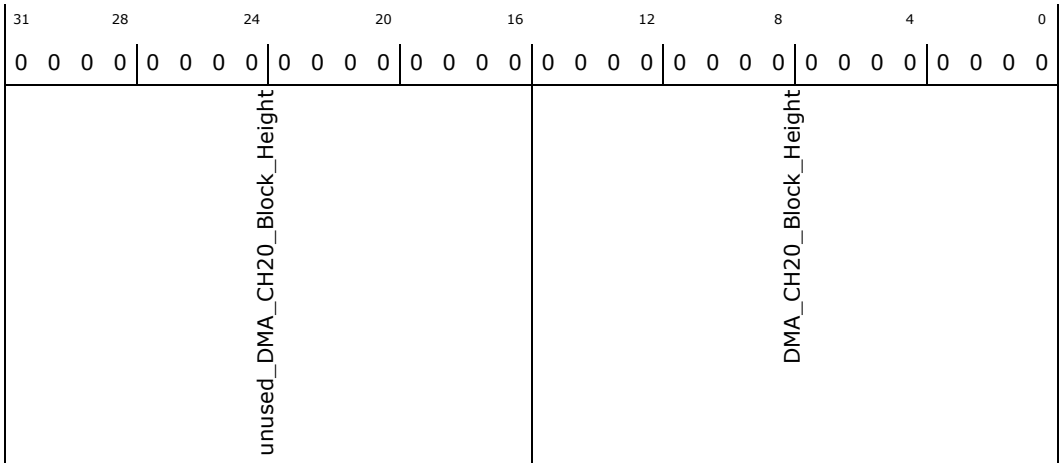
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41750h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH20_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH20_Block_Height:** DMA CH 20 PARAM 7: block height (Yb), in terms of lines

5.2.492 DMA_CH21_Block_Height (isp_dma_DMA_CH21_Block_Height)—Offset 41754h

DMA CH 21 PARAM 7: block height (Yb), in terms of lines

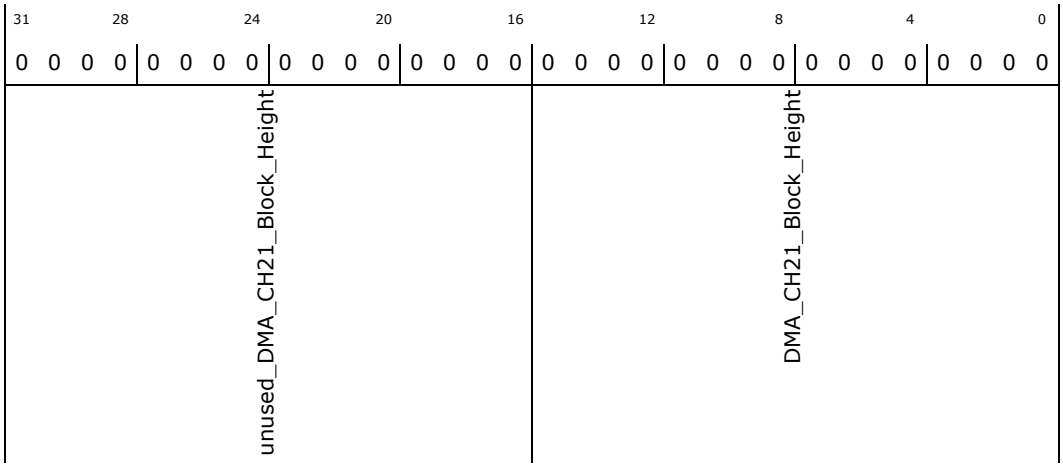
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41754h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH21_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH21_Block_Height:** DMA CH 21 PARAM 7: block height (Yb), in terms of lines

5.2.493 DMA_CH22_Block_Height (isp_dma_DMA_CH22_Block_Height)—Offset 41758h

DMA CH 22 PARAM 7: block height (Yb), in terms of lines

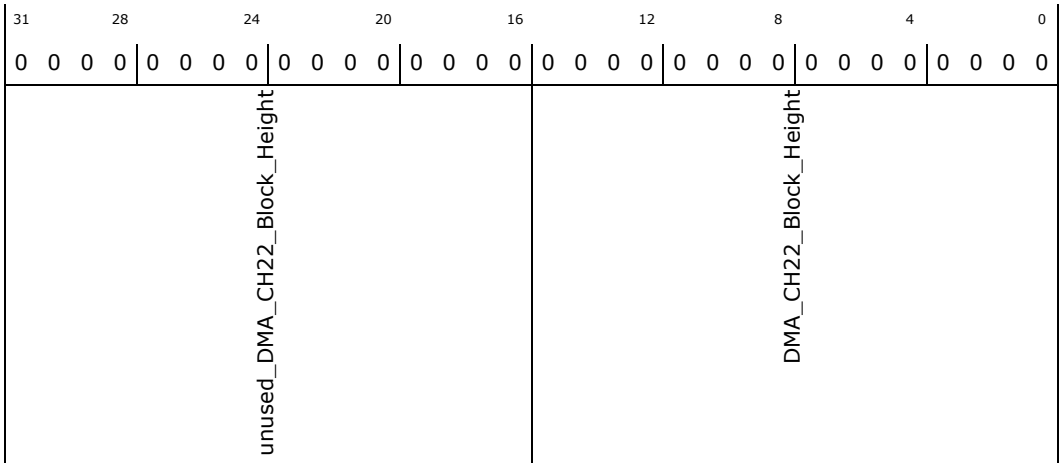
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41758h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH22_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH22_Block_Height:** DMA CH 22 PARAM 7: block height (Yb), in terms of lines

5.2.494 DMA_CH23_Block_Height (isp_dma_DMA_CH23_Block_Height)—Offset 4175Ch

DMA CH 23 PARAM 7: block height (Yb), in terms of lines

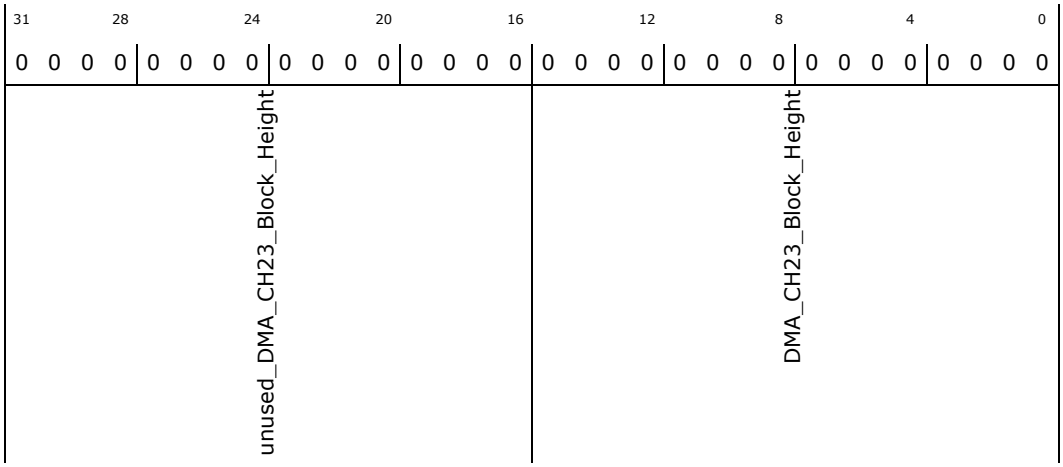
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4175Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH23_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH23_Block_Height:** DMA CH 23 PARAM 7: block height (Yb), in terms of lines

5.2.495 DMA_CH24_Block_Height (isp_dma_DMA_CH24_Block_Height)—Offset 41760h

DMA CH 24 PARAM 7: block height (Yb), in terms of lines

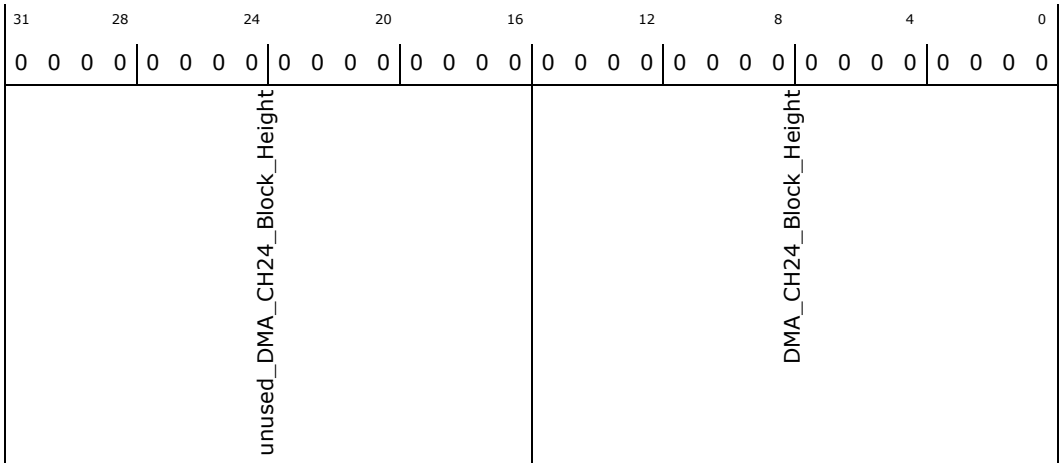
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41760h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH24_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH24_Block_Height:** DMA CH 24 PARAM 7: block height (Yb), in terms of lines

5.2.496 DMA_CH25_Block_Height (isp_dma_DMA_CH25_Block_Height)—Offset 41764h

DMA CH 25 PARAM 7: block height (Yb), in terms of lines

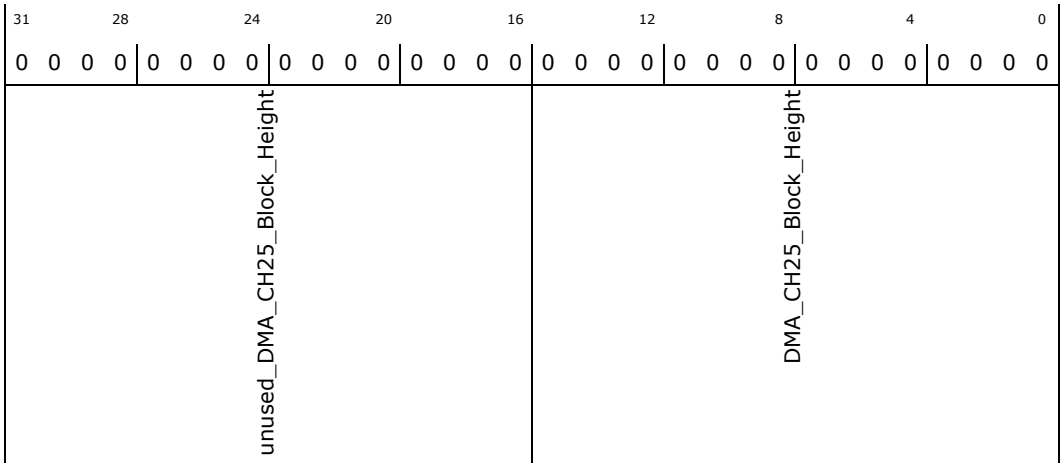
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41764h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH25_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH25_Block_Height:** DMA CH 25 PARAM 7: block height (Yb), in terms of lines

5.2.497 DMA_CH26_Block_Height (isp_dma_DMA_CH26_Block_Height)—Offset 41768h

DMA CH 26 PARAM 7: block height (Yb), in terms of lines

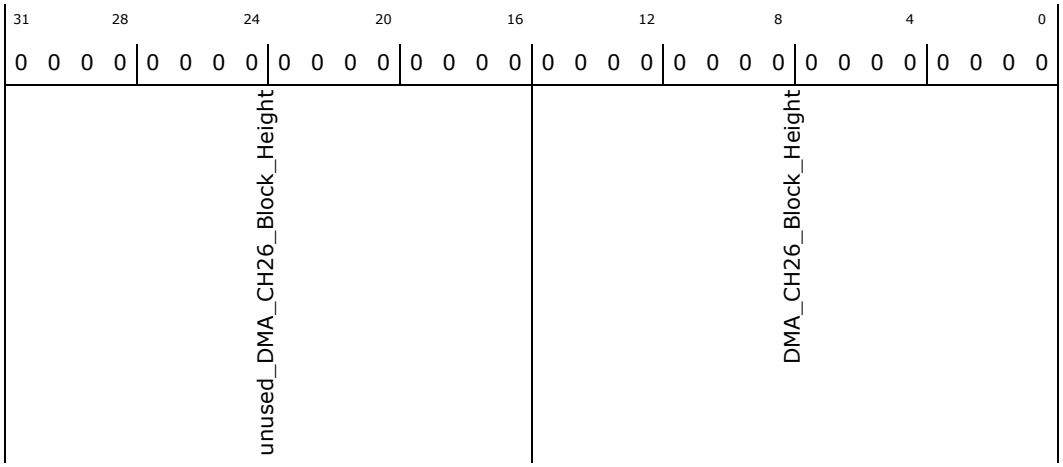
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41768h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH26_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH26_Block_Height:** DMA CH 26 PARAM 7: block height (Yb), in terms of lines

5.2.498 DMA_CH27_Block_Height (isp_dma_DMA_CH27_Block_Height)—Offset 4176Ch

DMA CH 27 PARAM 7: block height (Yb), in terms of lines

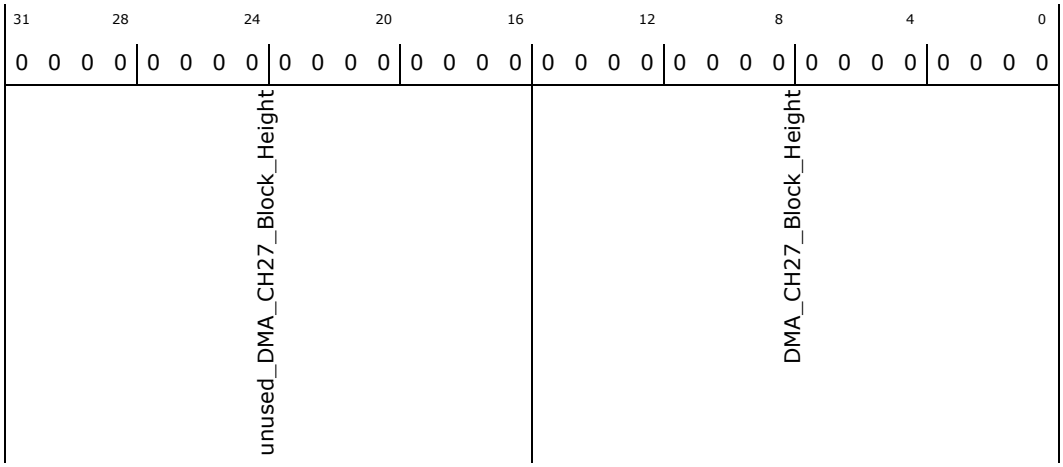
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4176Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH27_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH27_Block_Height:** DMA CH 27 PARAM 7: block height (Yb), in terms of lines

5.2.499 DMA_CH28_Block_Height (isp_dma_DMA_CH28_Block_Height)—Offset 41770h

DMA CH 28 PARAM 7: block height (Yb), in terms of lines

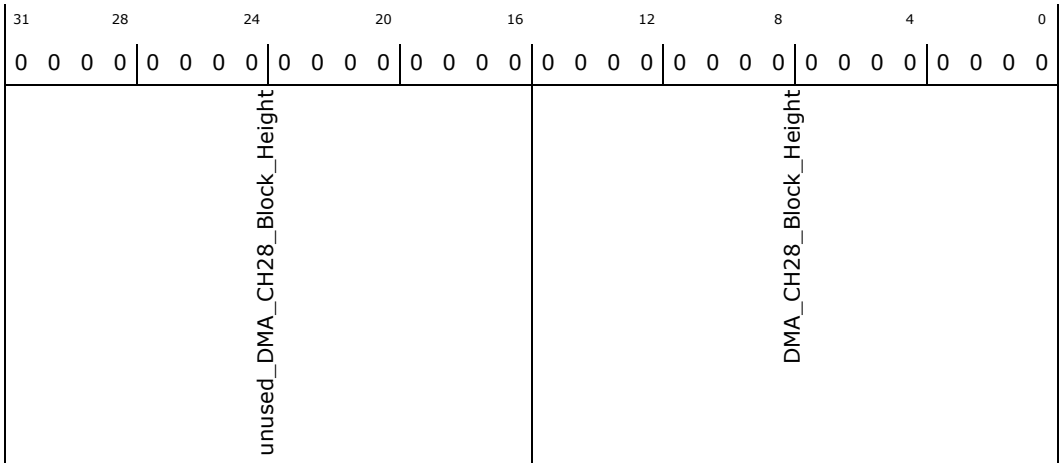
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41770h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH28_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH28_Block_Height:** DMA CH 28 PARAM 7: block height (Yb), in terms of lines

5.2.500 DMA_CH29_Block_Height (isp_dma_DMA_CH29_Block_Height)—Offset 41774h

DMA CH 29 PARAM 7: block height (Yb), in terms of lines

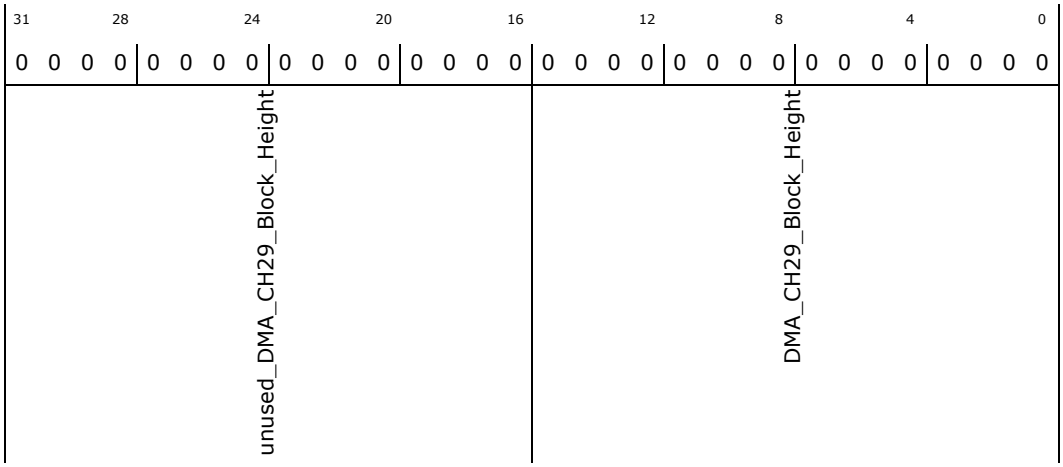
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41774h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH29_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH29_Block_Height:** DMA CH 29 PARAM 7: block height (Yb), in terms of lines

5.2.501 DMA_CH30_Block_Height (isp_dma_DMA_CH30_Block_Height)—Offset 41778h

DMA CH 30 PARAM 7: block height (Yb), in terms of lines

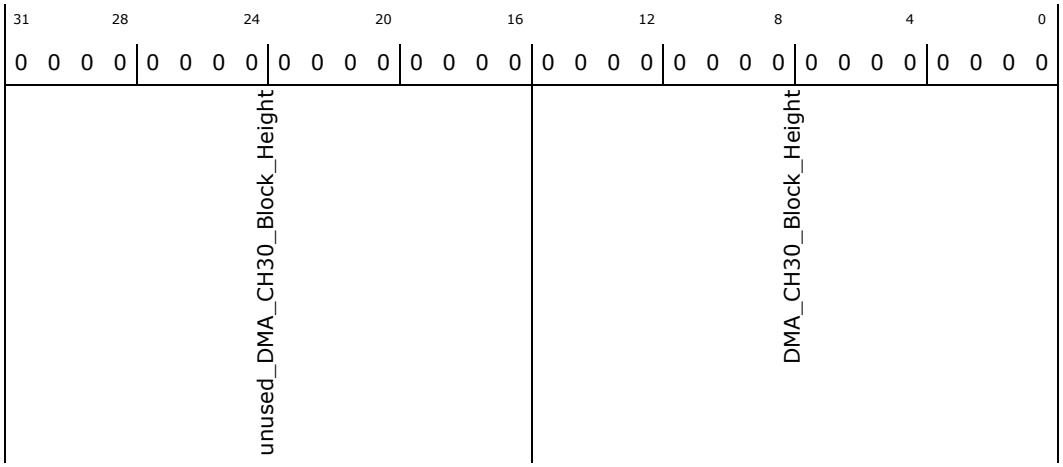
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41778h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH30_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH30_Block_Height:** DMA CH 30 PARAM 7: block height (Yb), in terms of lines

5.2.502 DMA_CH31_Block_Height (isp_dma_DMA_CH31_Block_Height)—Offset 4177Ch

DMA CH 31 PARAM 7: block height (Yb), in terms of lines

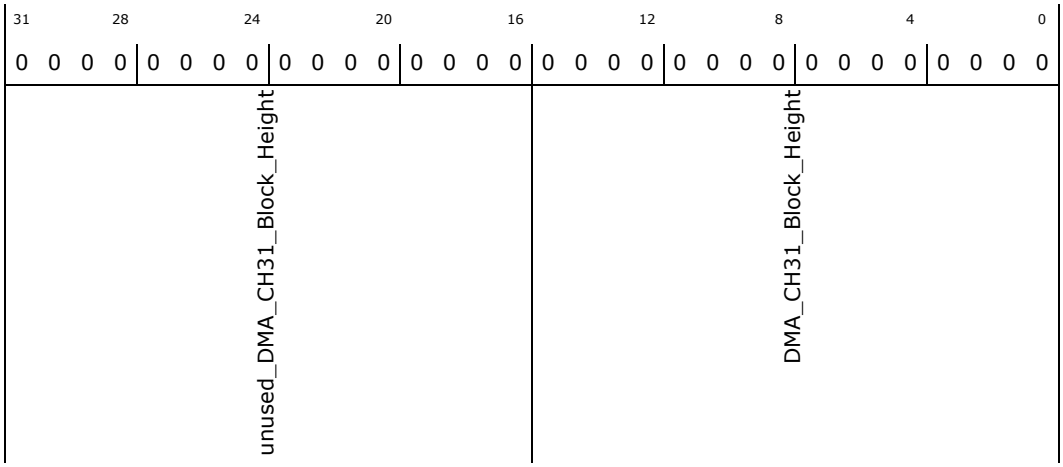
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4177Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH31_Block_Height):** Unused
15:0	0x0 RO	**DMA_CH31_Block_Height:** DMA CH 31 PARAM 7: block height (Yb), in terms of lines

5.2.503 DMA_CH0_cnt_pending_commands (isp_dma_DMA_CH0_cnt_pending_commands)—Offset 41800h

DMA CH 0 PARAM 8: Number of pending commands which will use channel 0

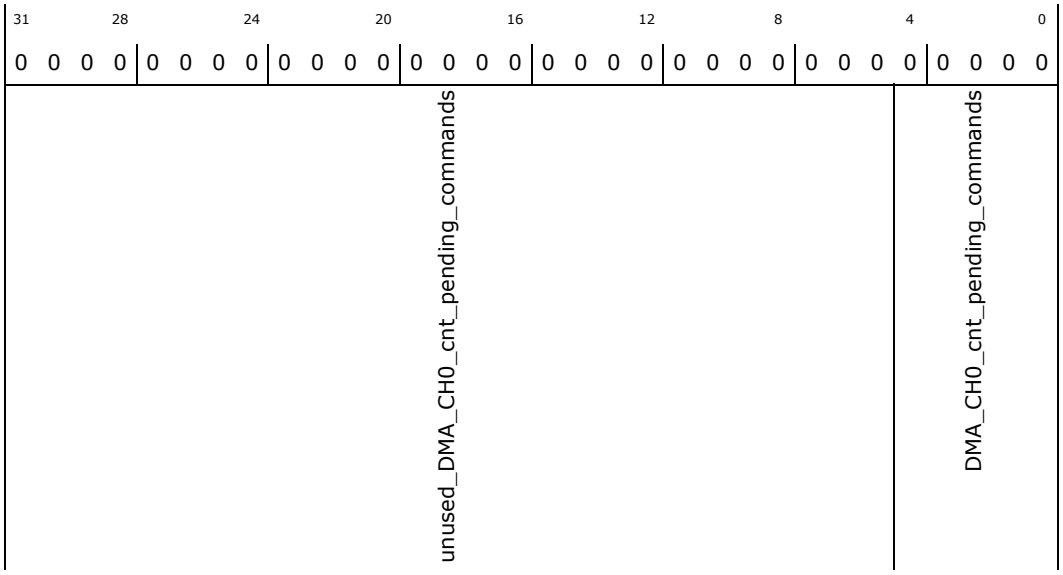
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41800h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH0_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH0_cnt_pending_commands:** DMA CH 0 PARAM 8: Number of pending commands which will use channel 0

5.2.504 DMA_CH1_cnt_pending_commands (isp_dma_DMA_CH1_cnt_pending_commands)—Offset 41804h

DMA CH 1 PARAM 8: Number of pending commands which will use channel 1

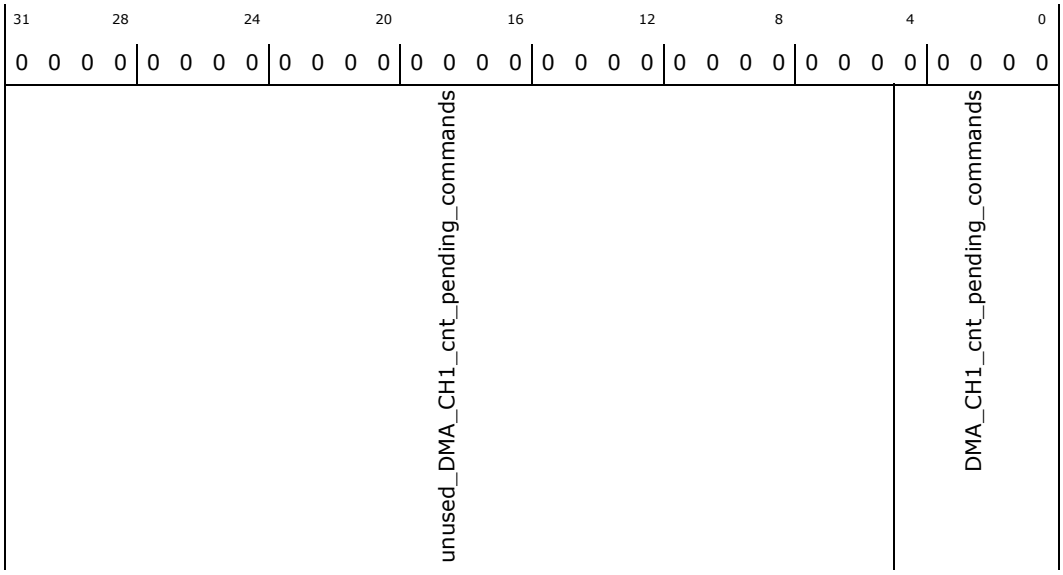
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41804h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH1_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH1_cnt_pending_commands:** DMA CH 1 PARAM 8: Number of pending commands which will use channel 1

5.2.505 DMA_CH2_cnt_pending_commands (isp_dma_DMA_CH2_cnt_pending_commands)—Offset 41808h

DMA CH 2 PARAM 8: Number of pending commands which will use channel 2

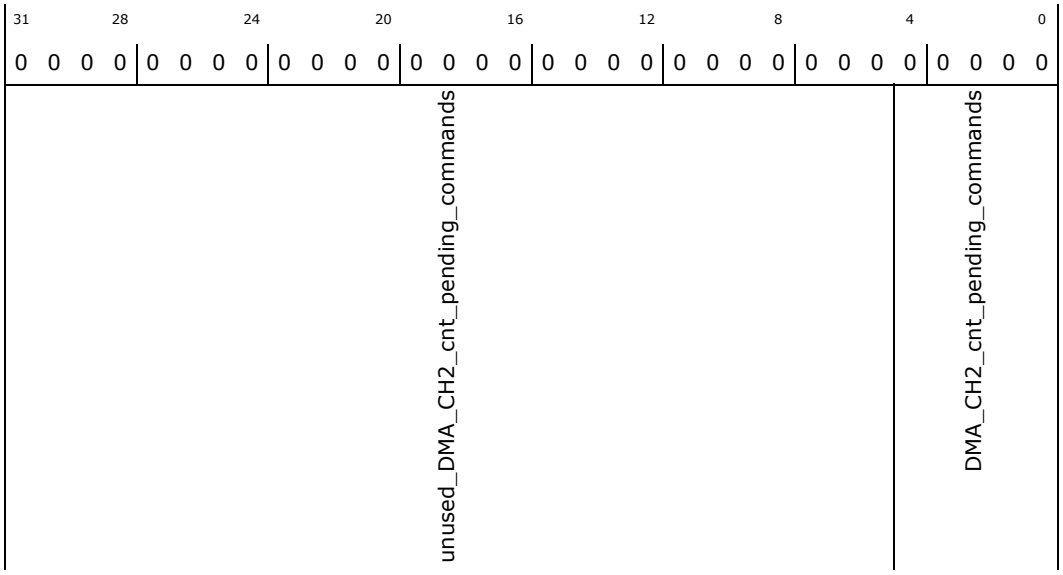
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41808h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH2_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH2_cnt_pending_commands:** DMA CH 2 PARAM 8: Number of pending commands which will use channel 2

5.2.506 DMA_CH3_cnt_pending_commands (isp_dma_DMA_CH3_cnt_pending_commands)—Offset 4180Ch

DMA CH 0 PARAM 8: Number of pending commands which will use channel 3

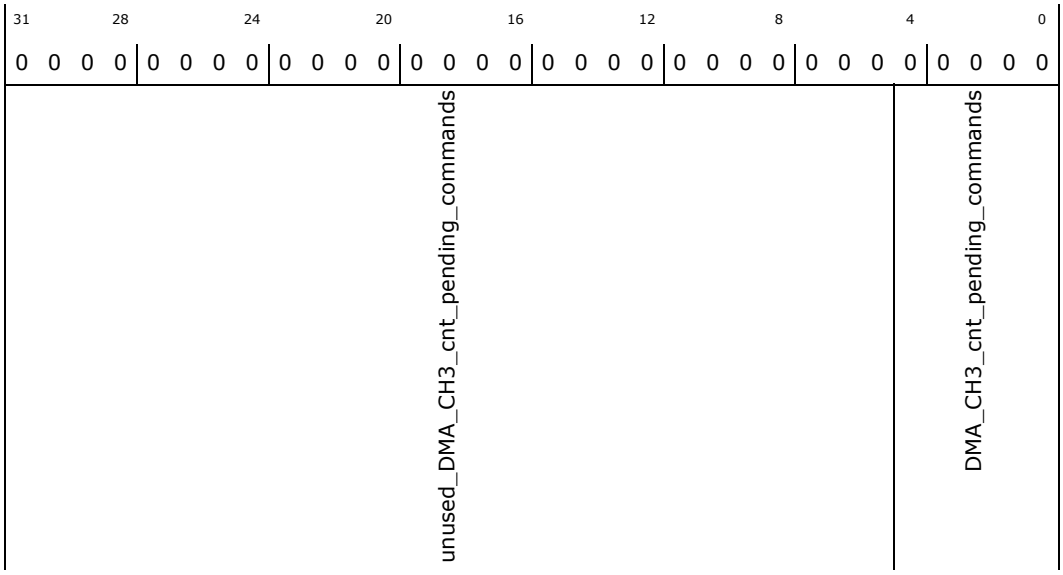
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4180Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH3_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH3_cnt_pending_commands:** DMA CH 0 PARAM 8: Number of pending commands which will use channel 3

5.2.507 DMA_CH4_cnt_pending_commands (isp_dma_DMA_CH4_cnt_pending_commands)—Offset 41810h

DMA CH 4 PARAM 8: Number of pending commands which will use channel 4

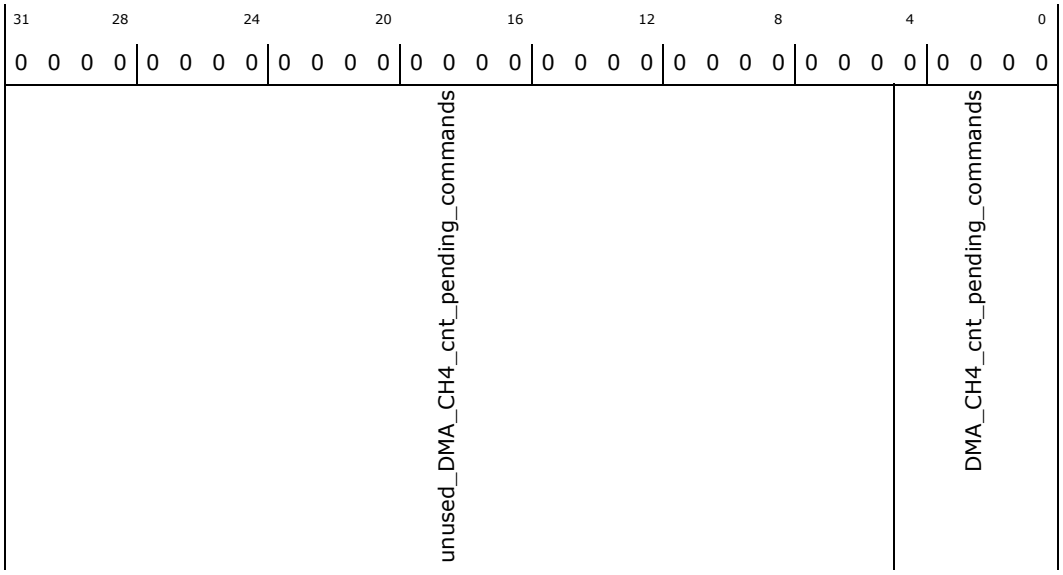
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41810h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH4_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH4_cnt_pending_commands:** DMA CH 4 PARAM 8: Number of pending commands which will use channel 4

5.2.508 DMA_CH5_cnt_pending_commands (isp_dma_DMA_CH5_cnt_pending_commands)—Offset 41814h

DMA CH 5 PARAM 8: Number of pending commands which will use channel 5

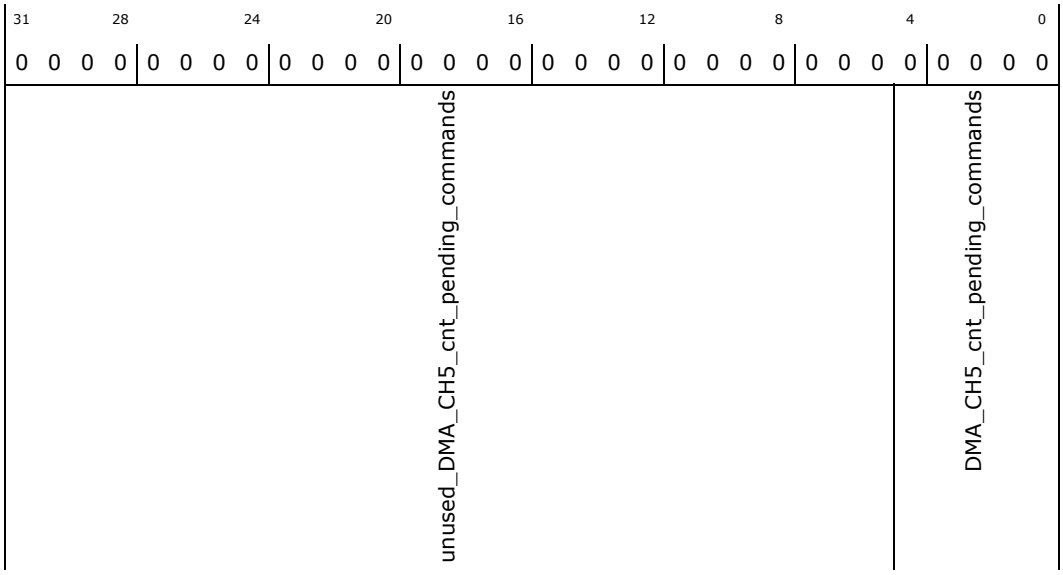
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41814h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH5_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH5_cnt_pending_commands:** DMA CH 5 PARAM 8: Number of pending commands which will use channel 5

5.2.509 DMA_CH6_cnt_pending_commands (isp_dma_DMA_CH6_cnt_pending_commands)—Offset 41818h

DMA CH 6 PARAM 8: Number of pending commands which will use channel 6

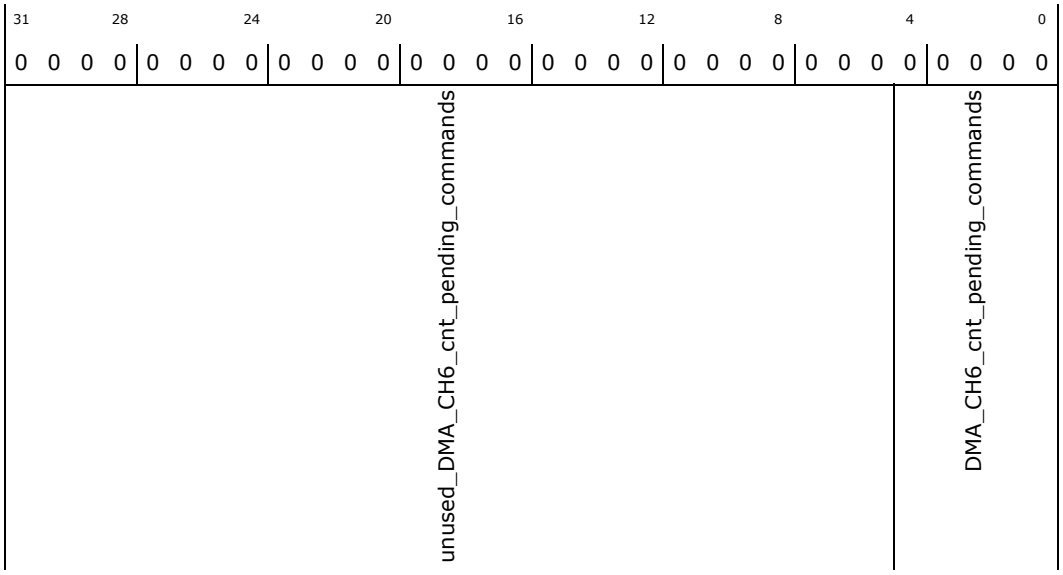
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41818h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH6_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH6_cnt_pending_commands:** DMA CH 6 PARAM 8: Number of pending commands which will use channel 6

5.2.510 DMA_CH7_cnt_pending_commands (isp_dma_DMA_CH7_cnt_pending_commands)—Offset 4181Ch

DMA CH 7 PARAM 8: Number of pending commands which will use channel 7

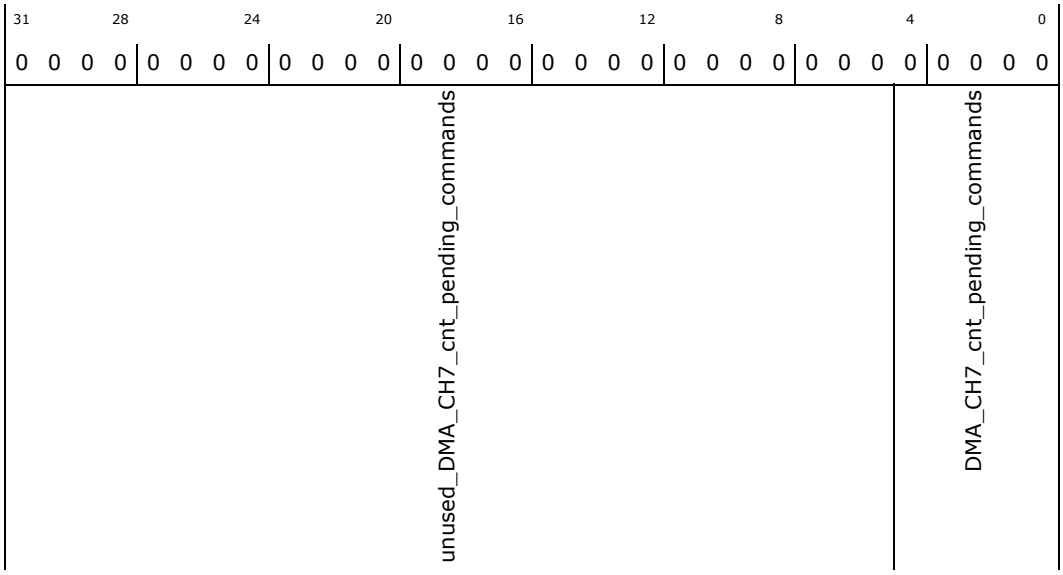
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4181Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH7_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH7_cnt_pending_commands:** DMA CH 7 PARAM 8: Number of pending commands which will use channel 7

5.2.511 DMA_CH8_cnt_pending_commands (isp_dma_DMA_CH8_cnt_pending_commands)—Offset 41820h

DMA CH 8 PARAM 8: Number of pending commands which will use channel 6

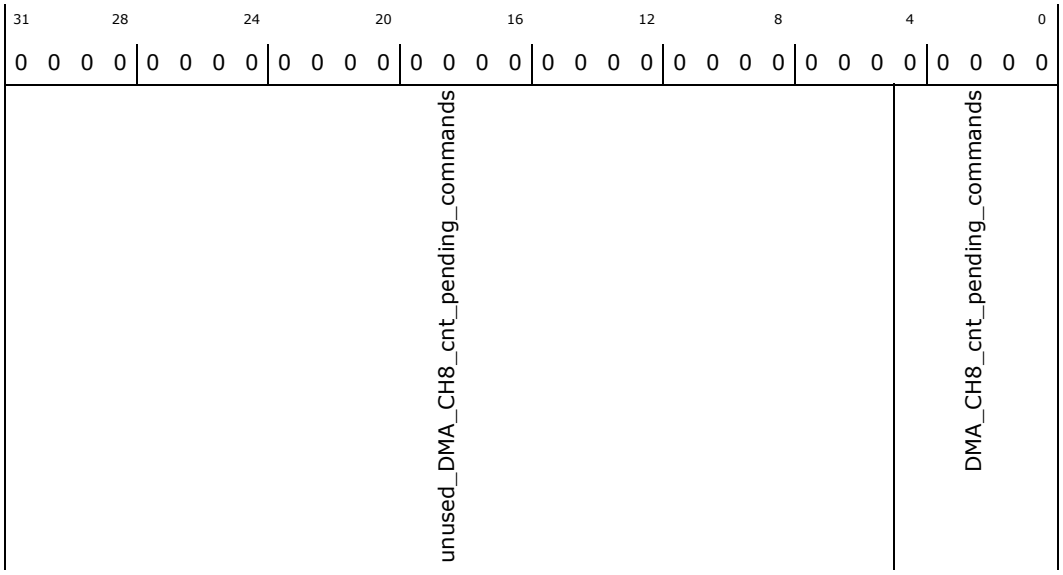
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41820h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH8_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH8_cnt_pending_commands:** DMA CH 8 PARAM 8: Number of pending commands which will use channel 6

5.2.512 DMA_CH9_cnt_pending_commands (isp_dma_DMA_CH9_cnt_pending_commands)—Offset 41824h

DMA CH 9 PARAM 8: Number of pending commands which will use channel 7

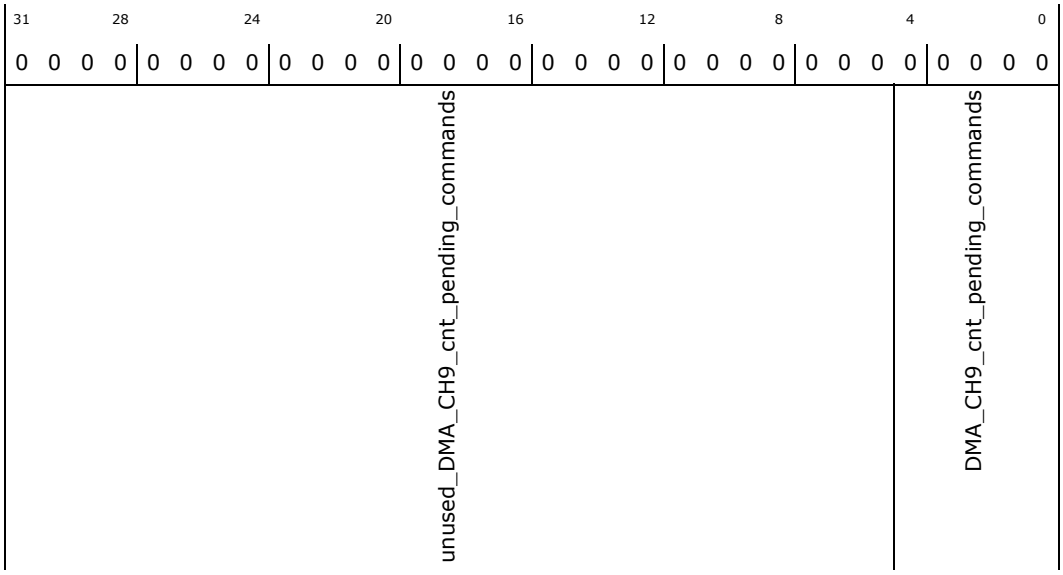
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41824h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH9_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH9_cnt_pending_commands:** DMA CH 9 PARAM 8: Number of pending commands which will use channel 7

5.2.513 DMA_CH10_cnt_pending_commands (isp_dma_DMA_CH10_cnt_pending_commands)—Offset 41828h

DMA CH 10 PARAM 8: Number of pending commands which will use channel 0

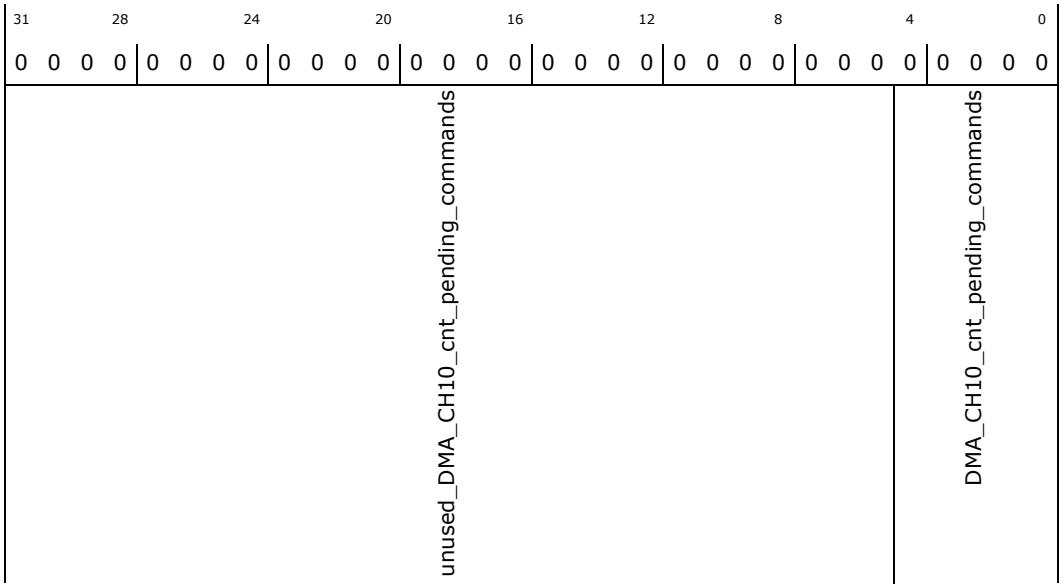
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41828h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH10_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH10_cnt_pending_commands:** DMA CH 10 PARAM 8: Number of pending commands which will use channel 0

5.2.514 DMA_CH11_cnt_pending_commands (isp_dma_DMA_CH11_cnt_pending_commands)—Offset 4182Ch

DMA CH 11 PARAM 8: Number of pending commands which will use channel 1

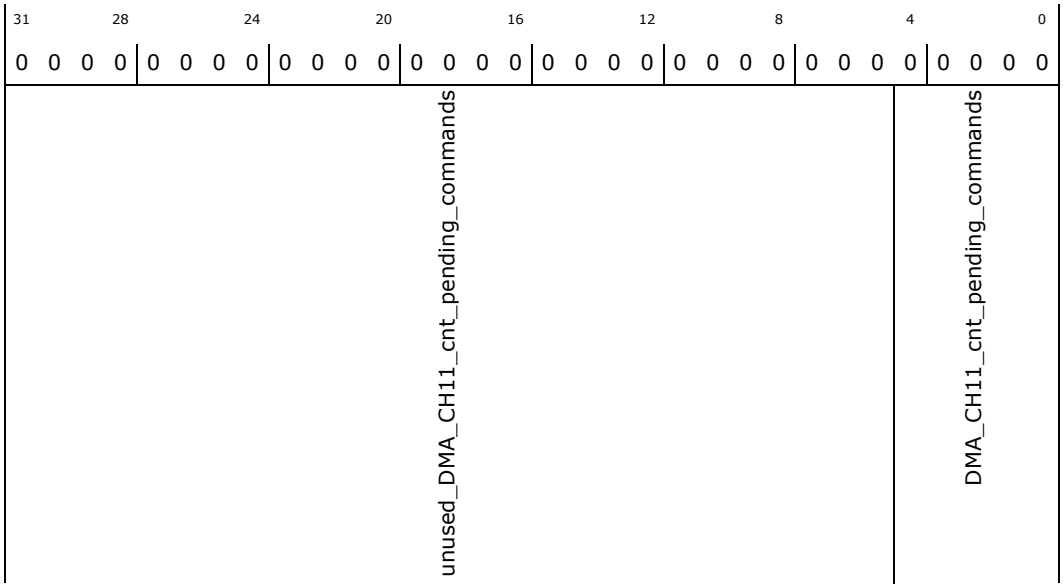
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4182Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH11_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH11_cnt_pending_commands:** DMA CH 11 PARAM 8: Number of pending commands which will use channel 1

5.2.515 DMA_CH12_cnt_pending_commands (isp_dma_DMA_CH12_cnt_pending_commands)—Offset 41830h

DMA CH 12 PARAM 8: Number of pending commands which will use channel 2

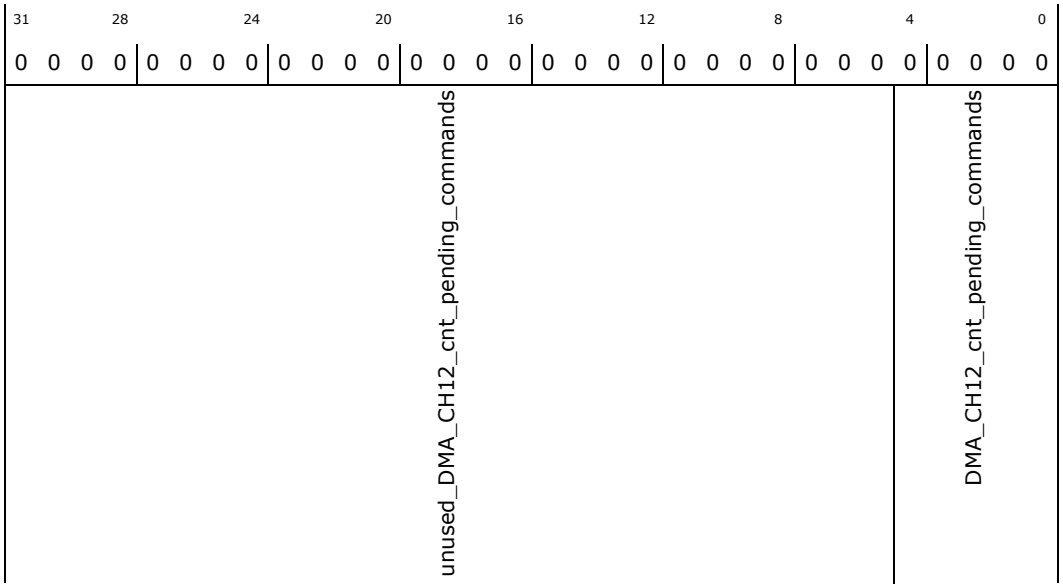
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41830h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH12_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH12_cnt_pending_commands:** DMA CH 12 PARAM 8: Number of pending commands which will use channel 2

5.2.516 DMA_CH13_cnt_pending_commands (isp_dma_DMA_CH13_cnt_pending_commands)—Offset 41834h

DMA CH 10 PARAM 8: Number of pending commands which will use channel 3

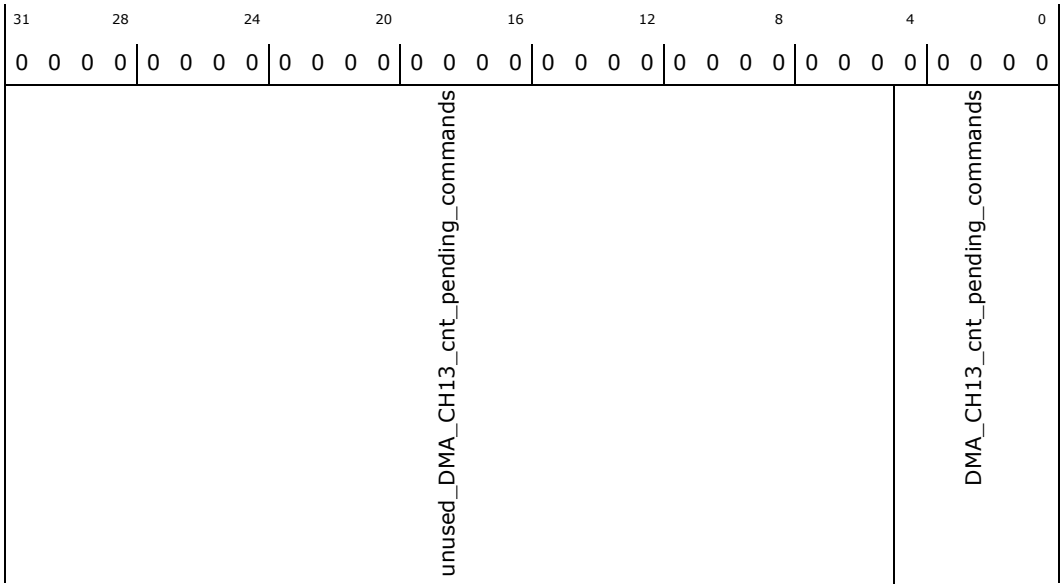
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41834h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH13_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH13_cnt_pending_commands:** DMA CH 10 PARAM 8: Number of pending commands which will use channel 3

5.2.517 DMA_CH14_cnt_pending_commands (isp_dma_DMA_CH14_cnt_pending_commands)—Offset 41838h

DMA CH 14 PARAM 8: Number of pending commands which will use channel 4

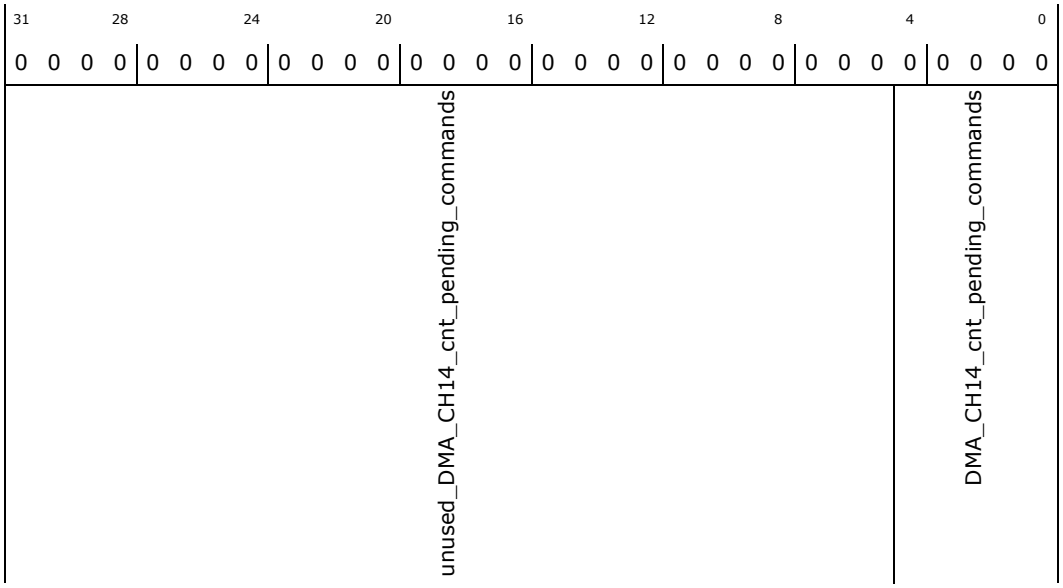
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41838h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH14_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH14_cnt_pending_commands:** DMA CH 14 PARAM 8: Number of pending commands which will use channel 4

5.2.518 DMA_CH15_cnt_pending_commands (isp_dma_DMA_CH15_cnt_pending_commands)—Offset 4183Ch

DMA CH 15 PARAM 8: Number of pending commands which will use channel 5

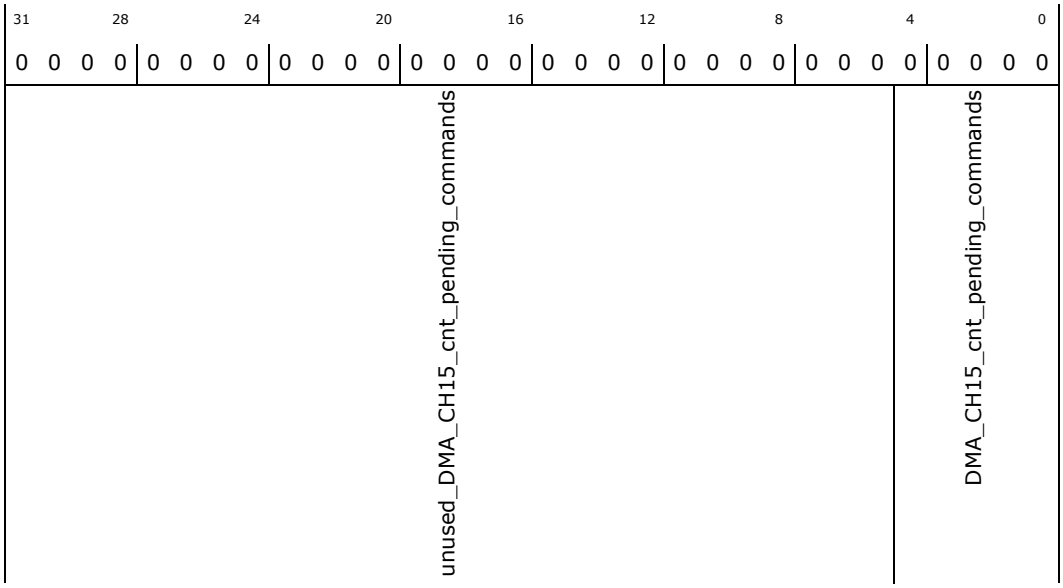
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4183Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH15_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH15_cnt_pending_commands:** DMA CH 15 PARAM 8: Number of pending commands which will use channel 5

5.2.519 DMA_CH16_cnt_pending_commands (isp_dma_DMA_CH16_cnt_pending_commands)—Offset 41840h

DMA CH 16 PARAM 8: Number of pending commands which will use channel 6

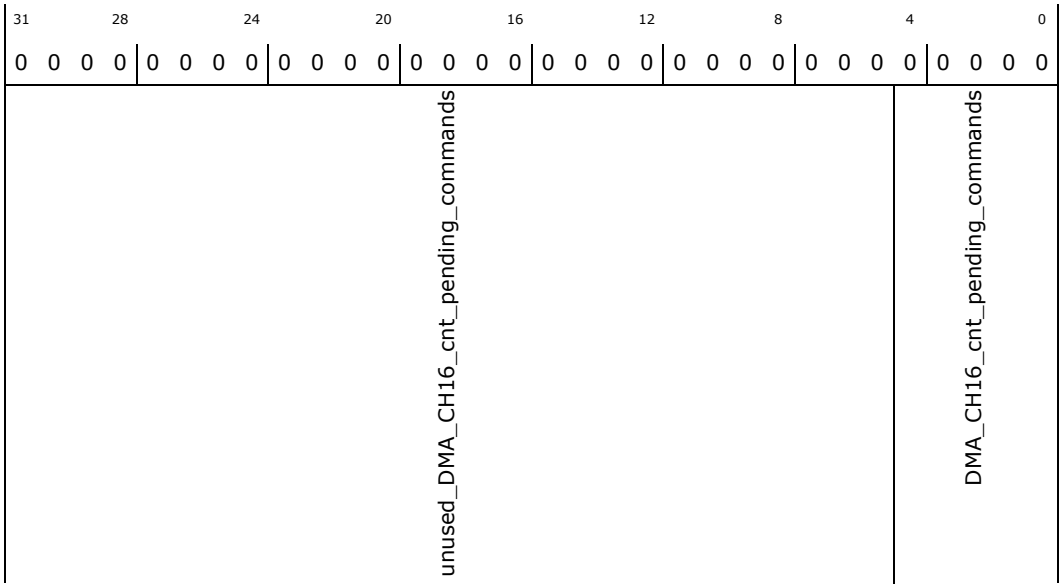
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41840h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH16_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH16_cnt_pending_commands:** DMA CH 16 PARAM 8: Number of pending commands which will use channel 6

5.2.520 DMA_CH17_cnt_pending_commands (isp_dma_DMA_CH17_cnt_pending_commands)—Offset 41844h

DMA CH 17 PARAM 8: Number of pending commands which will use channel 7

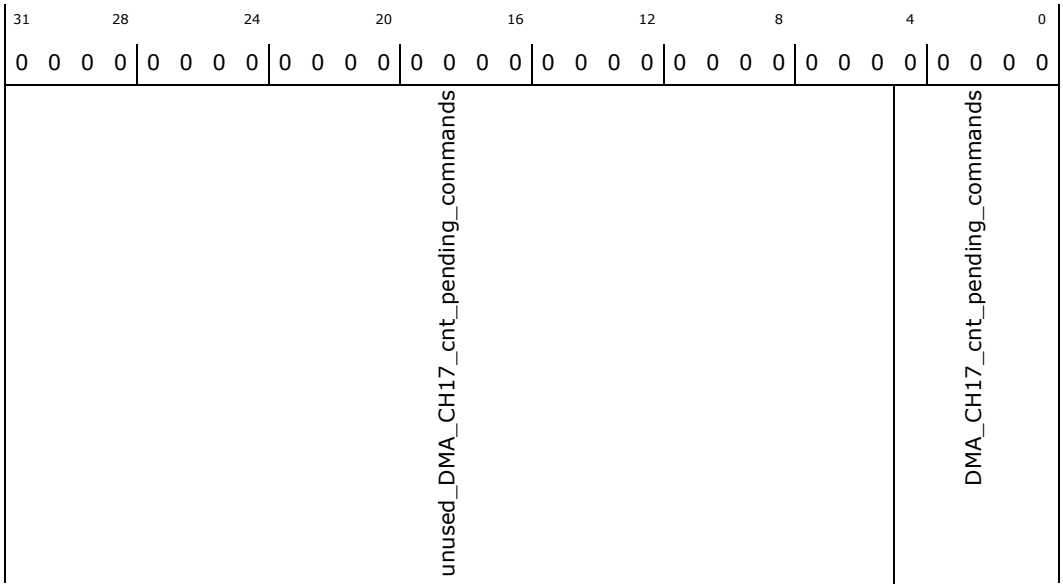
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41844h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH17_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH17_cnt_pending_commands:** DMA CH 17 PARAM 8: Number of pending commands which will use channel 7

5.2.521 DMA_CH18_cnt_pending_commands (isp_dma_DMA_CH18_cnt_pending_commands)—Offset 41848h

DMA CH 18 PARAM 8: Number of pending commands which will use channel 6

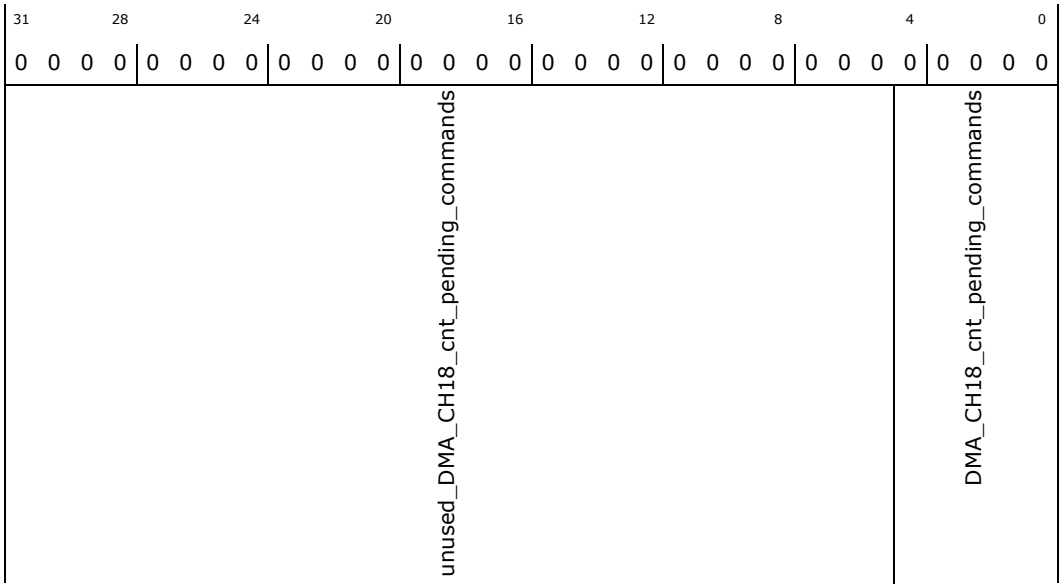
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41848h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH18_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH18_cnt_pending_commands:** DMA CH 18 PARAM 8: Number of pending commands which will use channel 6

5.2.522 DMA_CH19_cnt_pending_commands (isp_dma_DMA_CH19_cnt_pending_commands)—Offset 4184Ch

DMA CH 19 PARAM 8: Number of pending commands which will use channel 7

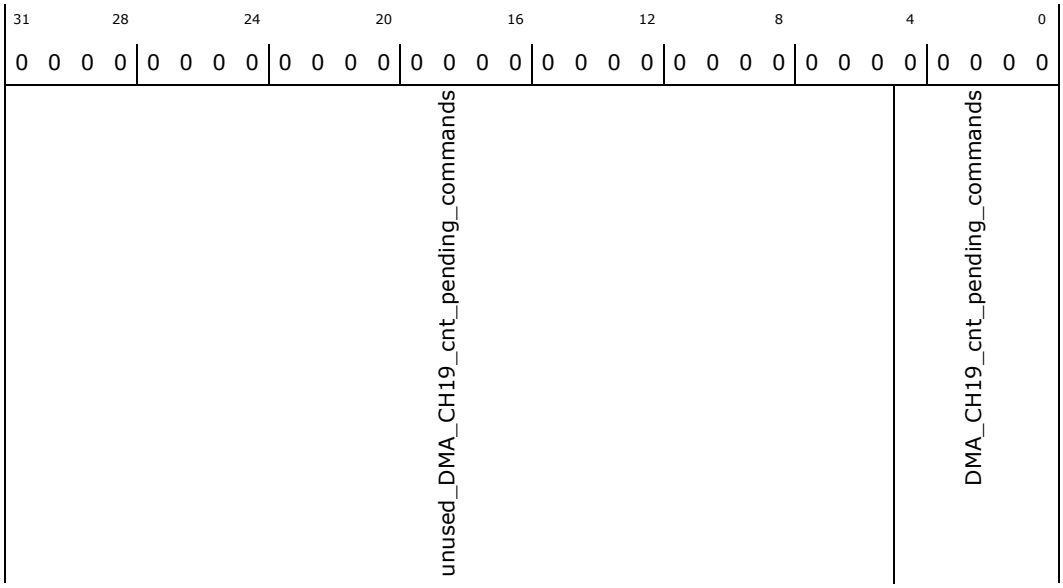
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4184Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH19_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH19_cnt_pending_commands:** DMA CH 19 PARAM 8: Number of pending commands which will use channel 7

5.2.523 DMA_CH20_cnt_pending_commands (isp_dma_DMA_CH20_cnt_pending_commands)—Offset 41850h

DMA CH 20 PARAM 8: Number of pending commands which will use channel 0

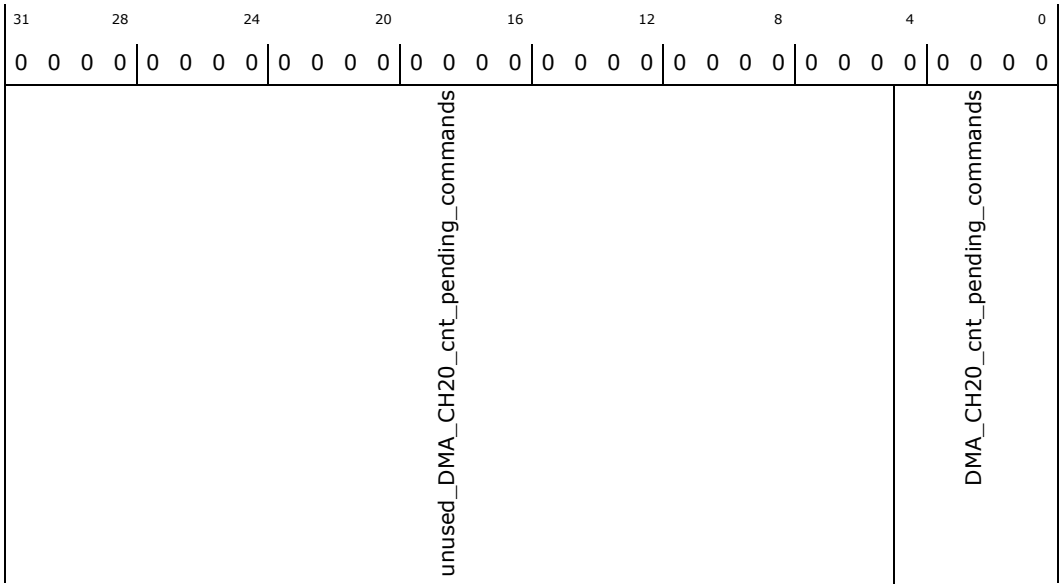
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41850h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH20_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH20_cnt_pending_commands:** DMA CH 20 PARAM 8: Number of pending commands which will use channel 0

5.2.524 DMA_CH21_cnt_pending_commands (isp_dma_DMA_CH21_cnt_pending_commands)—Offset 41854h

DMA CH 21 PARAM 8: Number of pending commands which will use channel 1

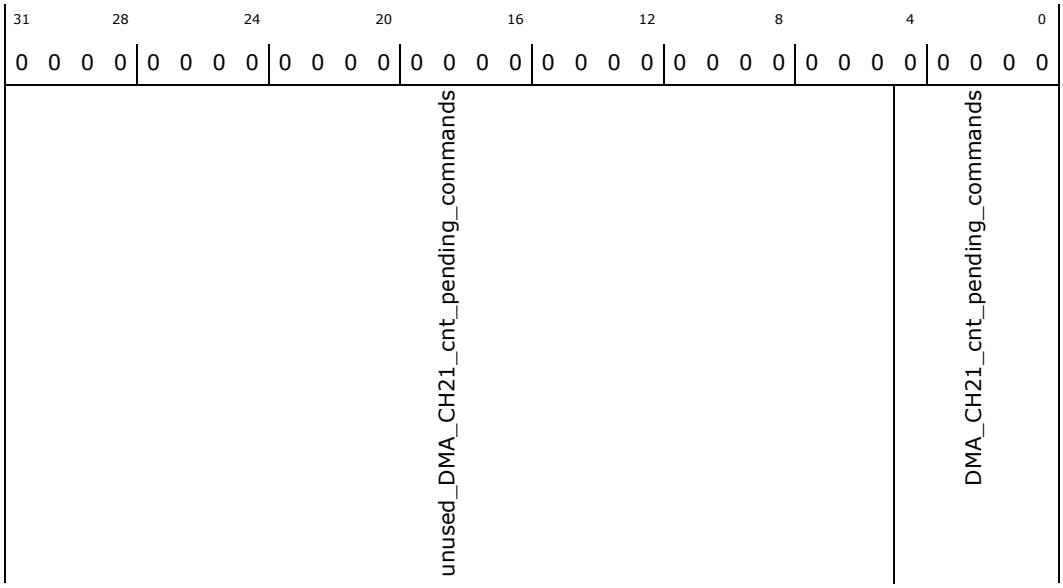
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41854h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH21_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH21_cnt_pending_commands:** DMA CH 21 PARAM 8: Number of pending commands which will use channel 1

5.2.525 DMA_CH22_cnt_pending_commands (isp_dma_DMA_CH22_cnt_pending_commands)—Offset 41858h

DMA CH 22 PARAM 8: Number of pending commands which will use channel 2

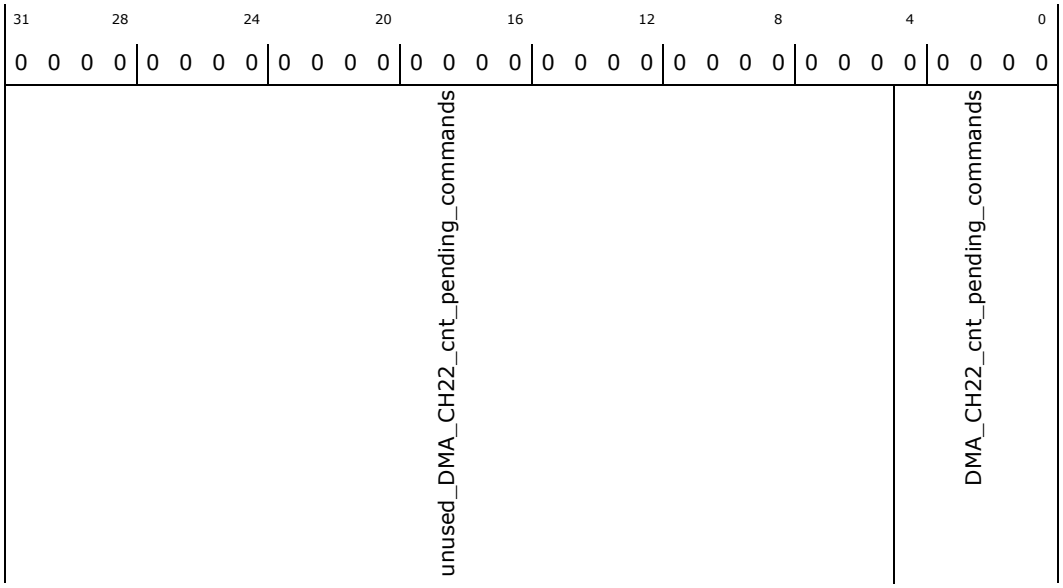
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41858h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH22_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH22_cnt_pending_commands:** DMA CH 22 PARAM 8: Number of pending commands which will use channel 2

5.2.526 DMA_CH23_cnt_pending_commands (isp_dma_DMA_CH23_cnt_pending_commands)—Offset 4185Ch

DMA CH 20 PARAM 8: Number of pending commands which will use channel 3

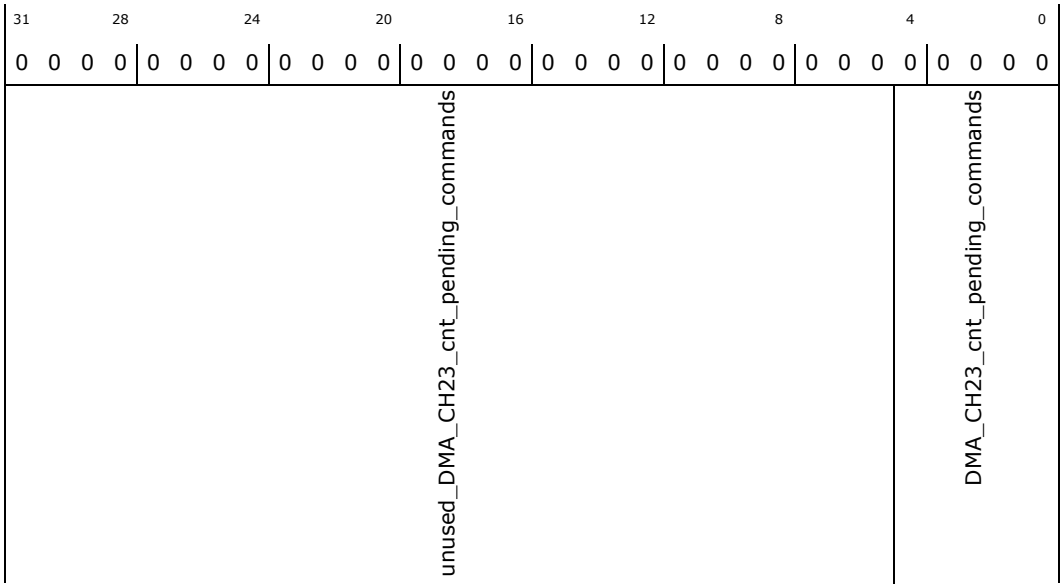
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4185Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH23_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH23_cnt_pending_commands:** DMA CH 20 PARAM 8: Number of pending commands which will use channel 3

5.2.527 DMA_CH24_cnt_pending_commands (isp_dma_DMA_CH24_cnt_pending_commands)—Offset 41860h

DMA CH 24 PARAM 8: Number of pending commands which will use channel 4

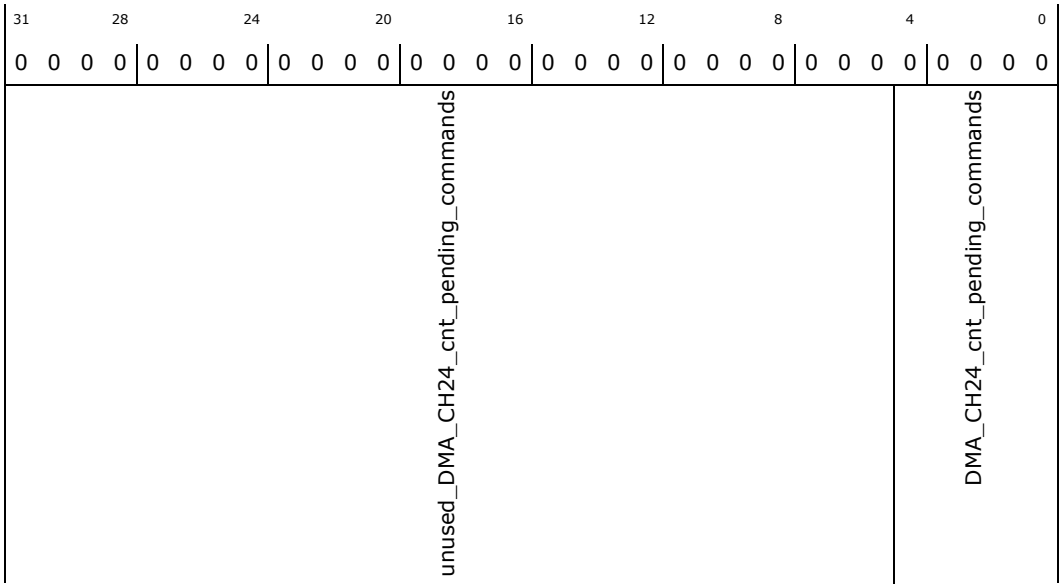
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41860h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH24_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH24_cnt_pending_commands:** DMA CH 24 PARAM 8: Number of pending commands which will use channel 4

5.2.528 DMA_CH25_cnt_pending_commands (isp_dma_DMA_CH25_cnt_pending_commands)—Offset 41864h

DMA CH 25 PARAM 8: Number of pending commands which will use channel 5

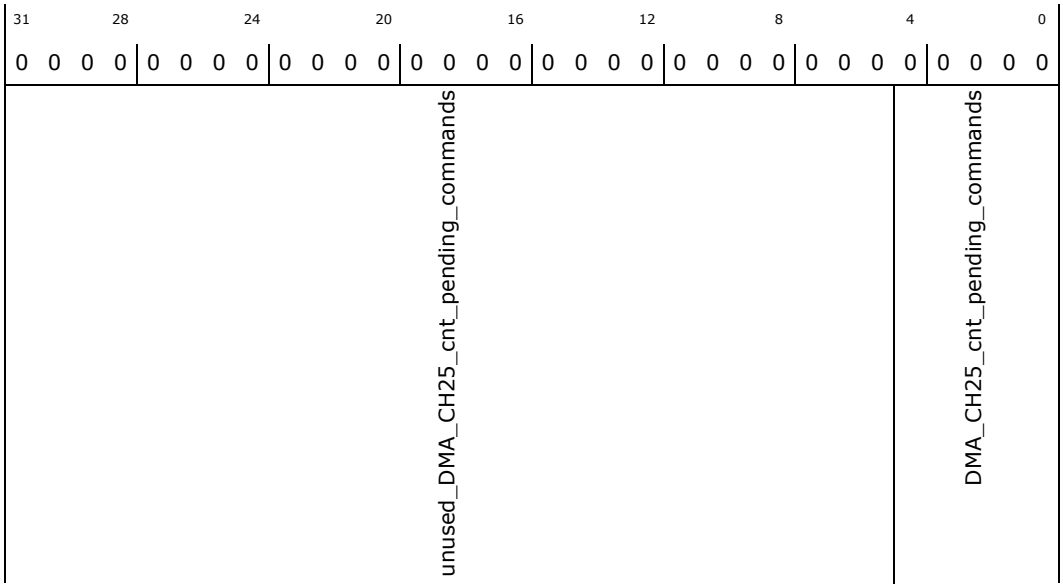
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41864h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH25_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH25_cnt_pending_commands:** DMA CH 25 PARAM 8: Number of pending commands which will use channel 5

5.2.529 DMA_CH26_cnt_pending_commands (isp_dma_DMA_CH26_cnt_pending_commands)—Offset 41868h

DMA CH 26 PARAM 8: Number of pending commands which will use channel 6

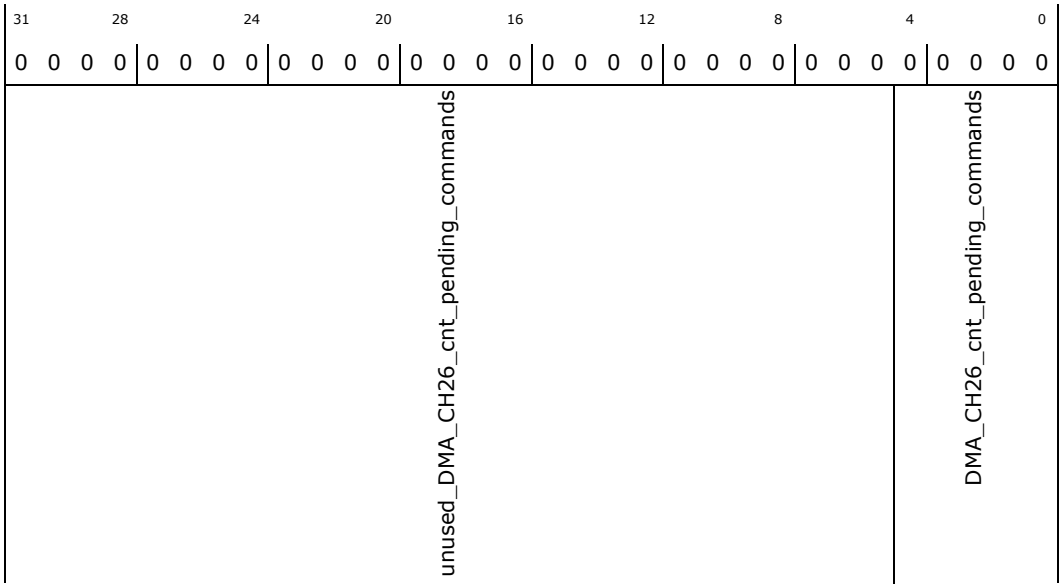
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41868h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH26_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH26_cnt_pending_commands:** DMA CH 26 PARAM 8: Number of pending commands which will use channel 6

5.2.530 DMA_CH27_cnt_pending_commands (isp_dma_DMA_CH27_cnt_pending_commands)—Offset 4186Ch

DMA CH 27 PARAM 8: Number of pending commands which will use channel 7

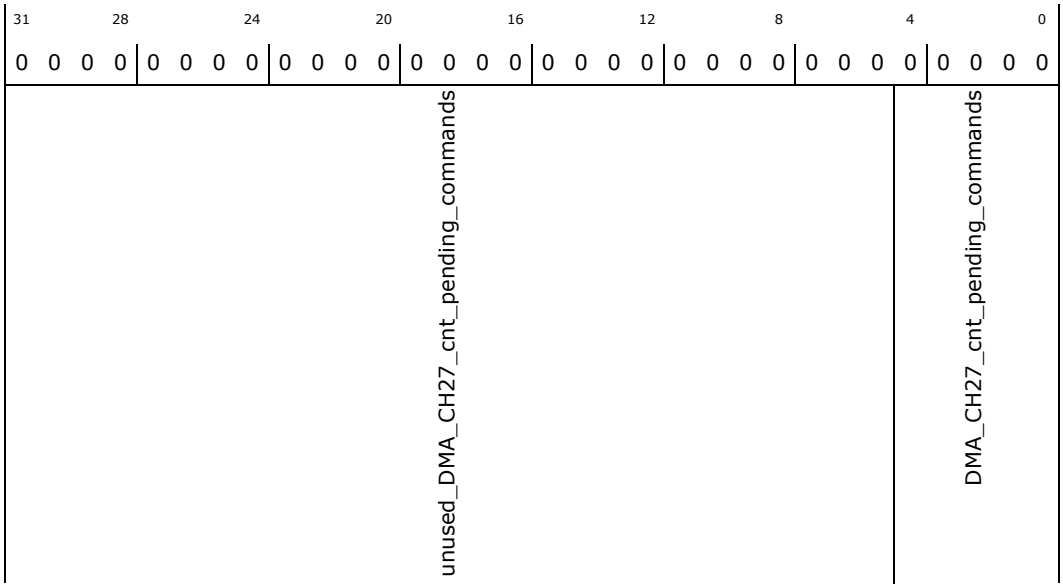
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4186Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH27_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH27_cnt_pending_commands:** DMA CH 27 PARAM 8: Number of pending commands which will use channel 7

5.2.531 DMA_CH28_cnt_pending_commands (isp_dma_DMA_CH28_cnt_pending_commands)—Offset 41870h

DMA CH 28 PARAM 8: Number of pending commands which will use channel 6

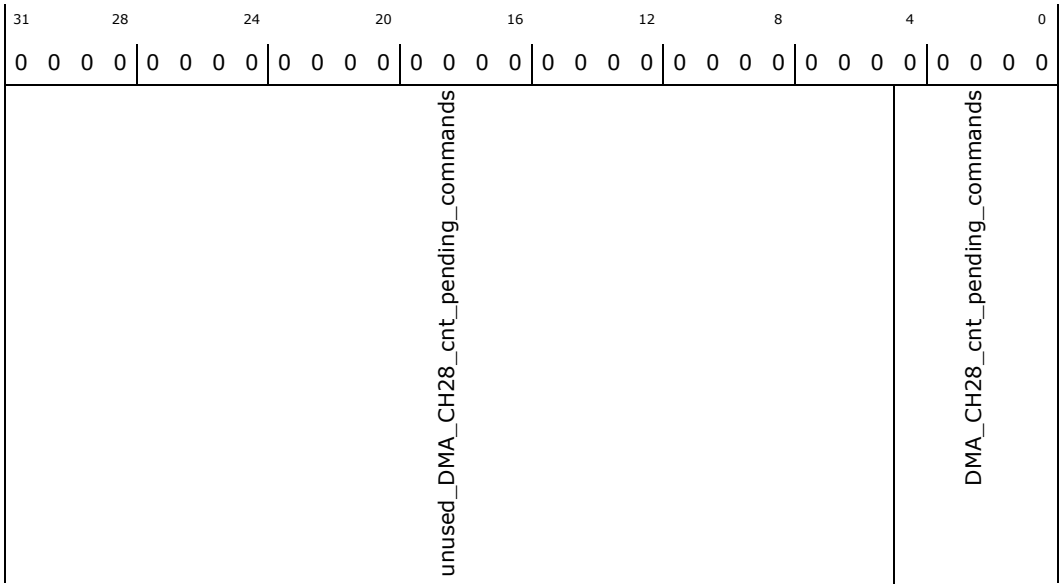
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41870h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH28_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH28_cnt_pending_commands:** DMA CH 28 PARAM 8: Number of pending commands which will use channel 6

5.2.532 DMA_CH29_cnt_pending_commands (isp_dma_DMA_CH29_cnt_pending_commands)—Offset 41874h

DMA CH 29 PARAM 8: Number of pending commands which will use channel 7

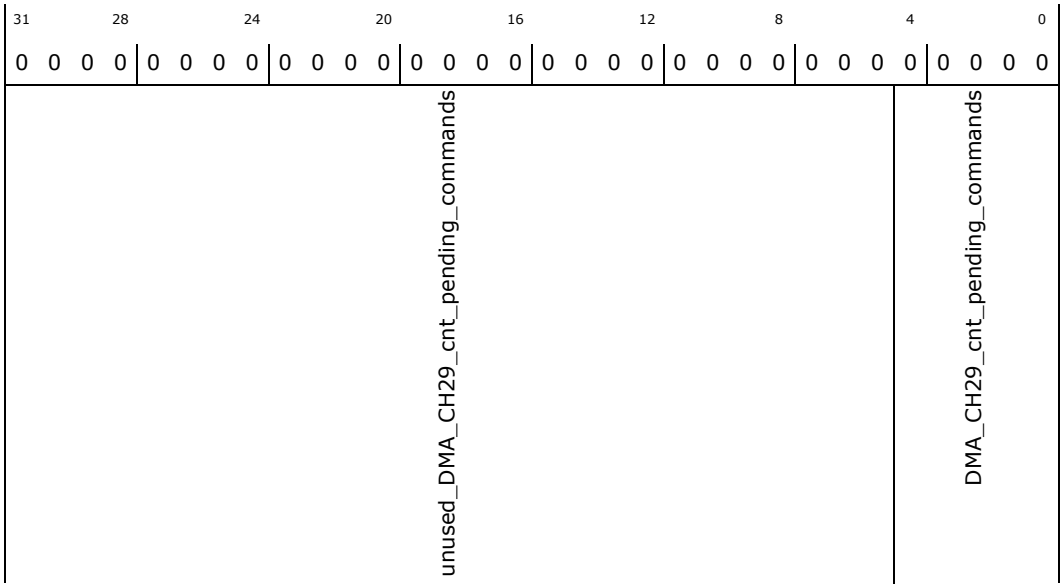
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41874h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH29_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH29_cnt_pending_commands:** DMA CH 29 PARAM 8: Number of pending commands which will use channel 7

5.2.533 DMA_CH30_cnt_pending_commands (isp_dma_DMA_CH30_cnt_pending_commands)—Offset 41878h

DMA CH 30 PARAM 8: Number of pending commands which will use channel 6

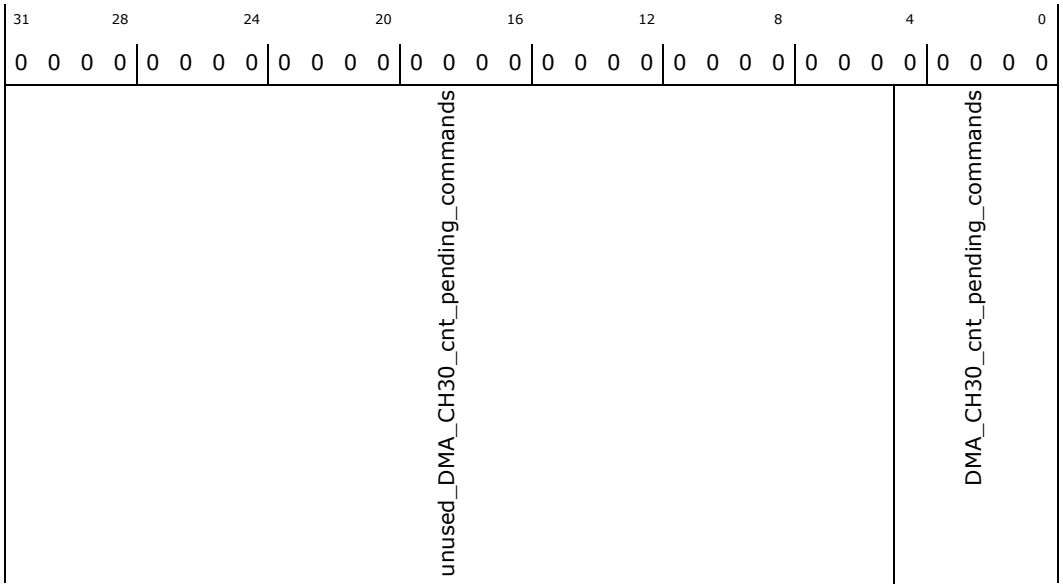
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 41878h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH30_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH30_cnt_pending_commands:** DMA CH 30 PARAM 8: Number of pending commands which will use channel 6

5.2.534 DMA_CH31_cnt_pending_commands (isp_dma_DMA_CH31_cnt_pending_commands)—Offset 4187Ch

DMA CH 30 PARAM 8: Number of pending commands which will use channel 7

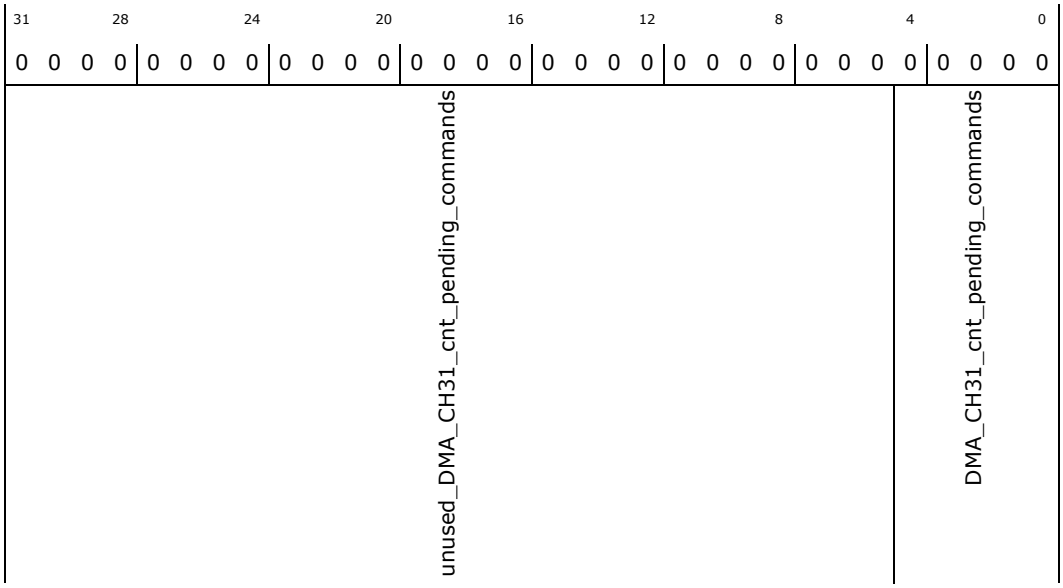
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4187Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_DMA_CH31_cnt_pending_commands):** Unused
4:0	0x0 RO	**DMA_CH31_cnt_pending_commands:** DMA CH 30 PARAM 8: Number of pending commands which will use channel 7

5.2.535 DMA_command_token (isp_dma_DMA_command_token)—Offset 42000h

Pending or last executed command token

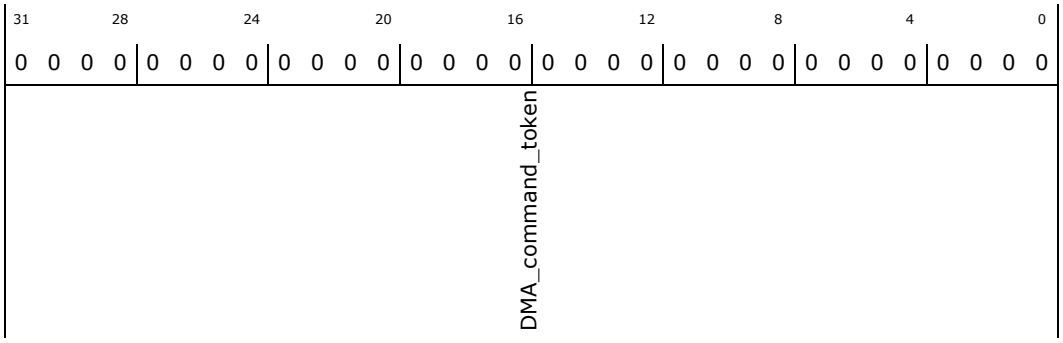
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_command_token:** Pending or last executed command token

5.2.536 DMA_command_src_addr (isp_dma_DMA_command_src_addr)—Offset 42004h

Source address of the pending or last executed command token

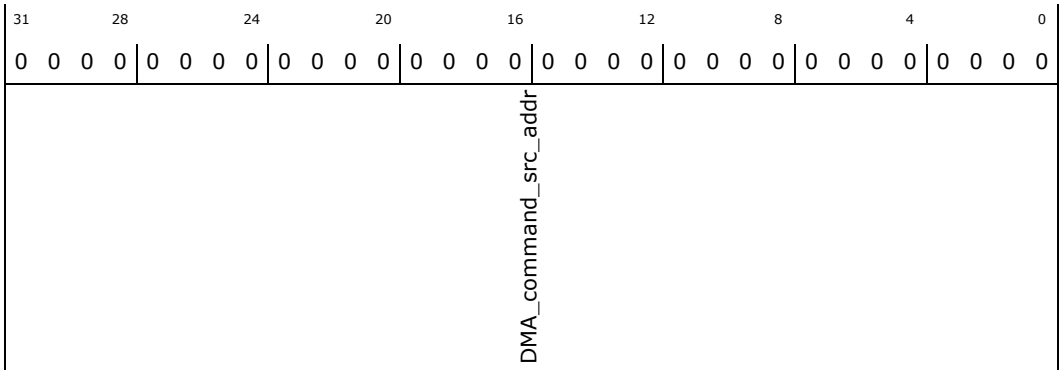
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_command_src_addr:** Source address of the pending or last executed command token

5.2.537 DMA_command_dst_addr (isp_dma_DMA_command_dst_addr)—Offset 42008h

Destination address of the pending or last executed command token

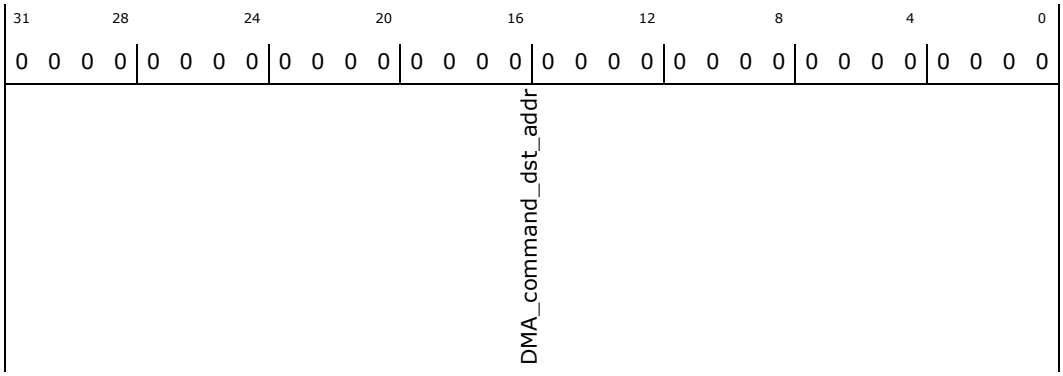
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_command_dst_addr:** Destination address of the pending or last executed command token

5.2.538 DMA_command_ctrl_idx (isp_dma_DMA_command_ctrl_idx)—Offset 4200Ch

Controller index of the pending or last executed command token

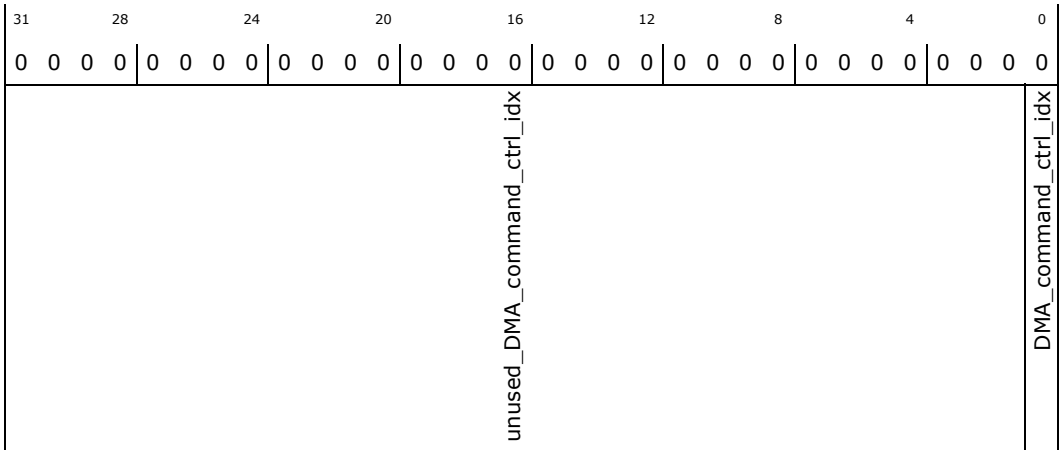
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4200Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_DMA_command_ctrl_idx):** Unused
0	0x0 RO	**DMA_command_ctrl_idx:** Controller index of the pending or last executed command token

5.2.539 DMA_FSM_Ctrl_status (isp_dma_DMA_FSM_Ctrl_status)—Offset 42010h

DMA FSM Control state and flags

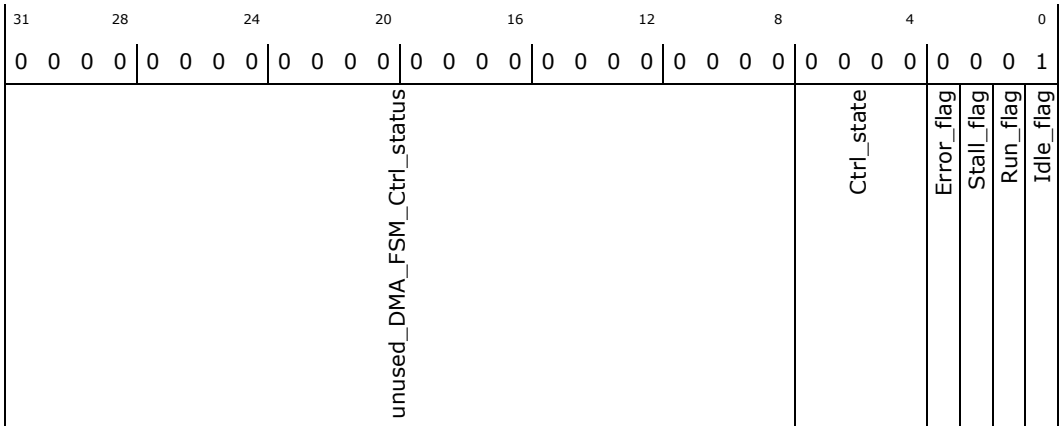
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (unused_DMA_FSM_Ctrl_status):** Unused
7:4	0x0 RO	**Ctrl_state:** FSM control state: 0)Idle -- 1)req_rcv -- 2)rcv -- 3)rcv_req -- 4)INIT
3	0x0 RO	**Error_flag:** Error flag
2	0x0 RO	**Stall_flag:** Stall flag
1	0x0 RO	**Run_flag:** Run flag
0	0x1 RO	**Idle_flag:** Idle flag

5.2.540 DMA_FSM_Pack_status (isp_dma_DMA_FSM_Pack_status)—Offset 42014h

DMA FSM Pack state

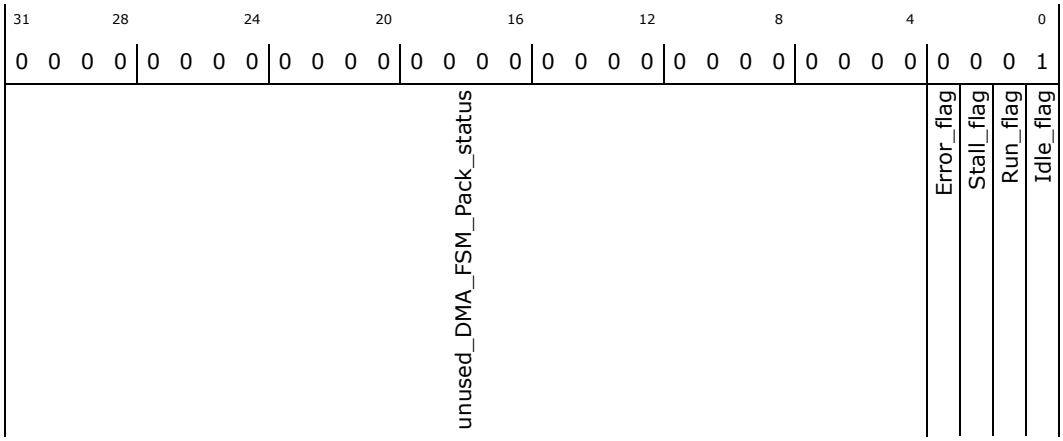
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_DMA_FSM_Pack_status):** Unused

Bit Range	Default and Access	Field Name (ID): Description
3	0x0 RO	**Error_flag:** Error flag
2	0x0 RO	**Stall_flag:** Stall flag
1	0x0 RO	**Run_flag:** Run flag
0	0x1 RO	**Idle_flag:** Idle flag

5.2.541 DMA_FSM_request_status (isp_dma_DMA_FSM_request_status)—Offset 42018h

DMA FSM Request state: 0)Idle -- 1)req -- 2)Next line

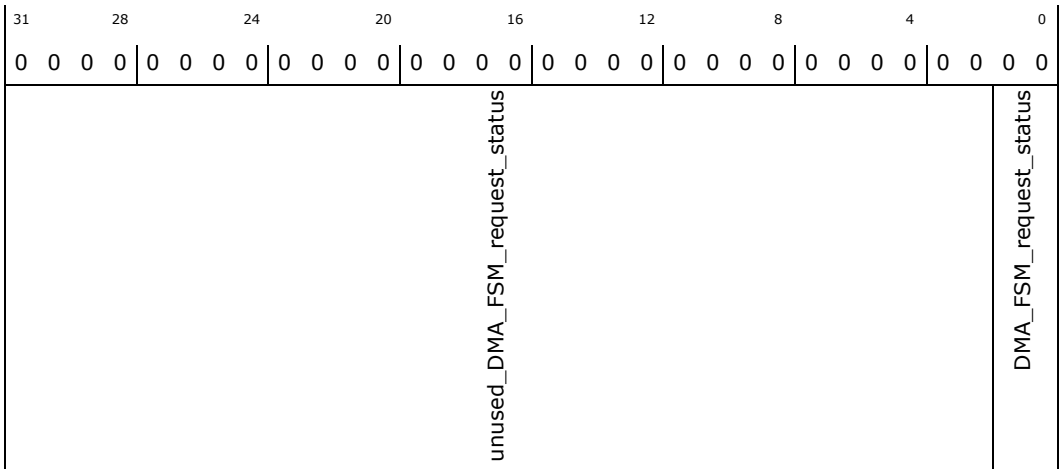
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_DMA_FSM_request_status):** Unused
1:0	0x0 RO	**DMA_FSM_request_status:** DMA FSM Request state: 0)Idle -- 1)req -- 2)Next line

5.2.542 DMA_FSM_write_status (isp_dma_DMA_FSM_write_status)—Offset 4201Ch

DMA FSM Write state: 0)Idle -- 1)req -- 2)Next line

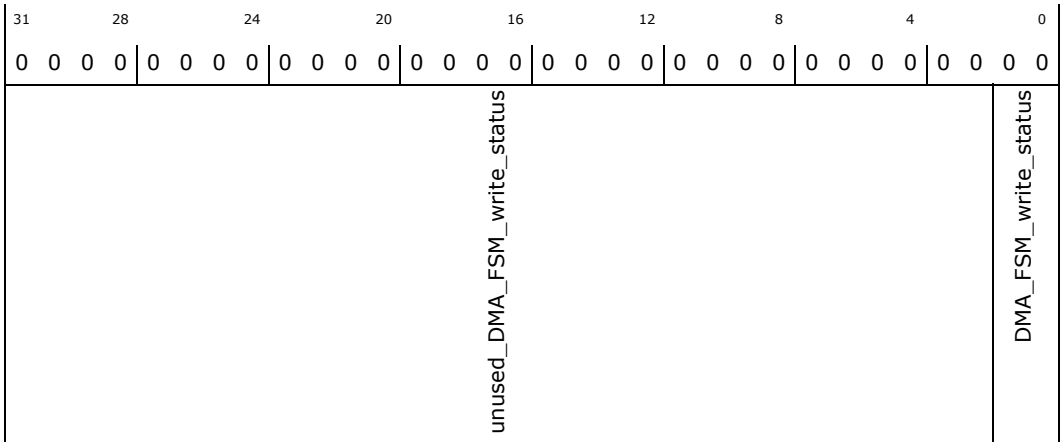
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4201Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_DMA_FSM_write_status):** Unused
1:0	0x0 RO	**DMA_FSM_write_status:** DMA FSM Write state: 0)Idle -- 1)req -- 2)Next line

5.2.543 DMA_FSM_Ctrl_dev_interf_idx (isp_dma_DMA_FSM_Ctrl_dev_interf_idx)—Offset 42110h

DMA FSM Control request device idx

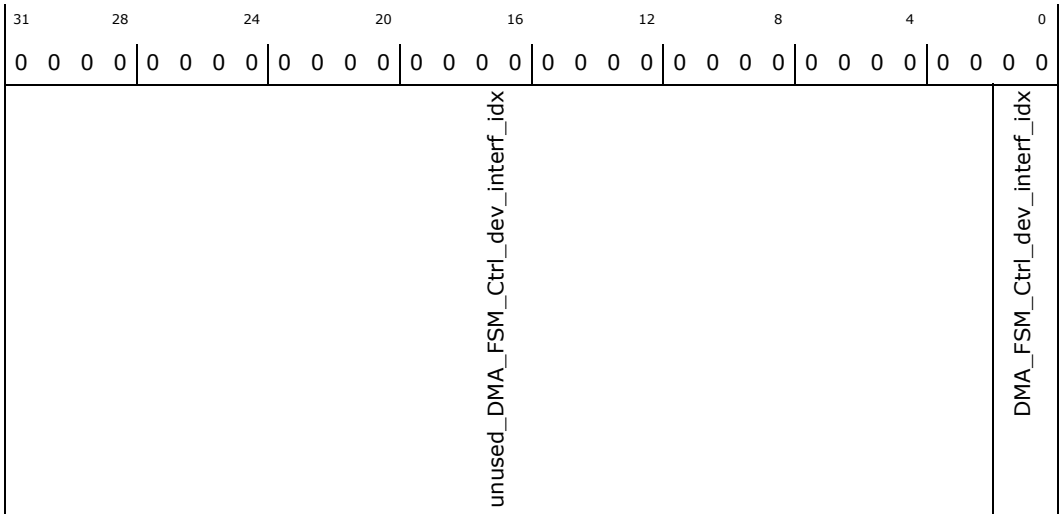
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42110h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_dev_interf_idx):** Unused
1:0	0x0 RO	**DMA_FSM_Ctrl_dev_interf_idx:** DMA FSM Control request device idx

5.2.544 DMA_FSM_Pack_cnt_Block_Height (isp_dma_DMA_FSM_Pack_cnt_Block_Height)—Offset 42114h

DMA FSM pack counter processed block Lines (Yb)

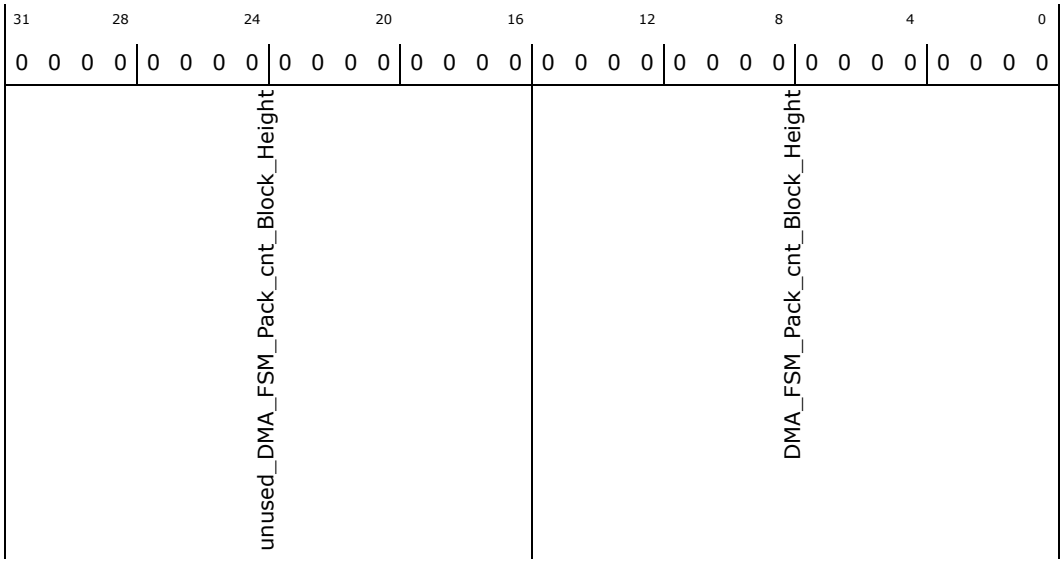
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42114h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Pack_cnt_Block_Height):** Unused
15:0	0x0 RO	**DMA_FSM_Pack_cnt_Block_Height:** DMA FSM pack counter processed block Lines (Yb)

5.2.545 DMA_FSM_Request_cnt_Block_Height (isp_dma_DMA_FSM_Request_cnt_Block_Height)—Offset 42118h

DMA FSM request counter processed block lines (Yb)

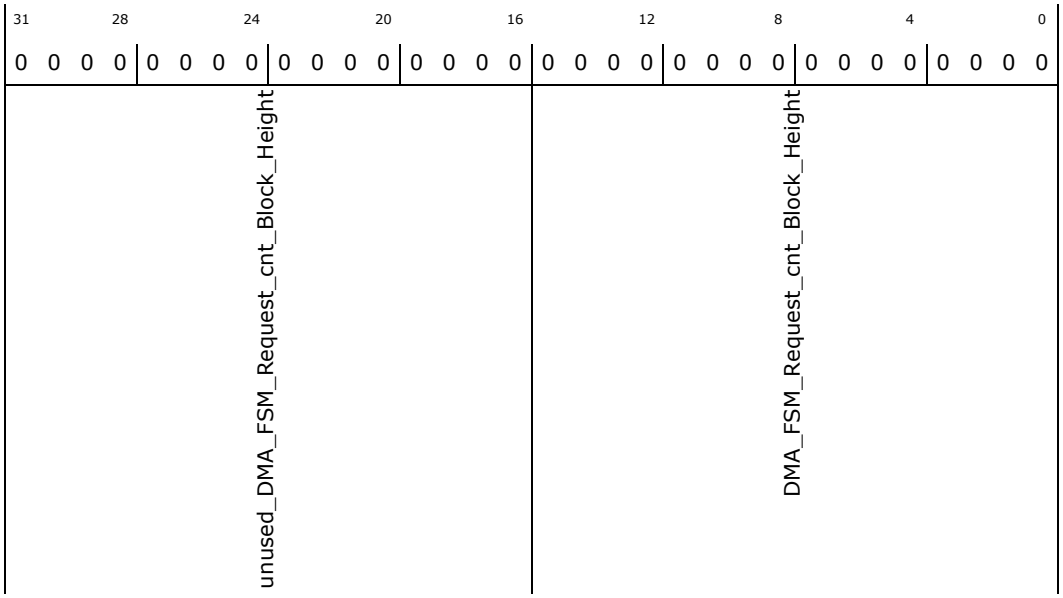
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42118h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Request_cnt_Block_Height):** Unused
15:0	0x0 RO	**DMA_FSM_Request_cnt_Block_Height:** DMA FSM request counter processed block lines (Yb)

5.2.546 DMA_FSM_Write_cnt_Block_Height (isp_dma_DMA_FSM_Write_cnt_Block_Height)—Offset 4211Ch

DMA FSM Write counter processed block lines (Yb)

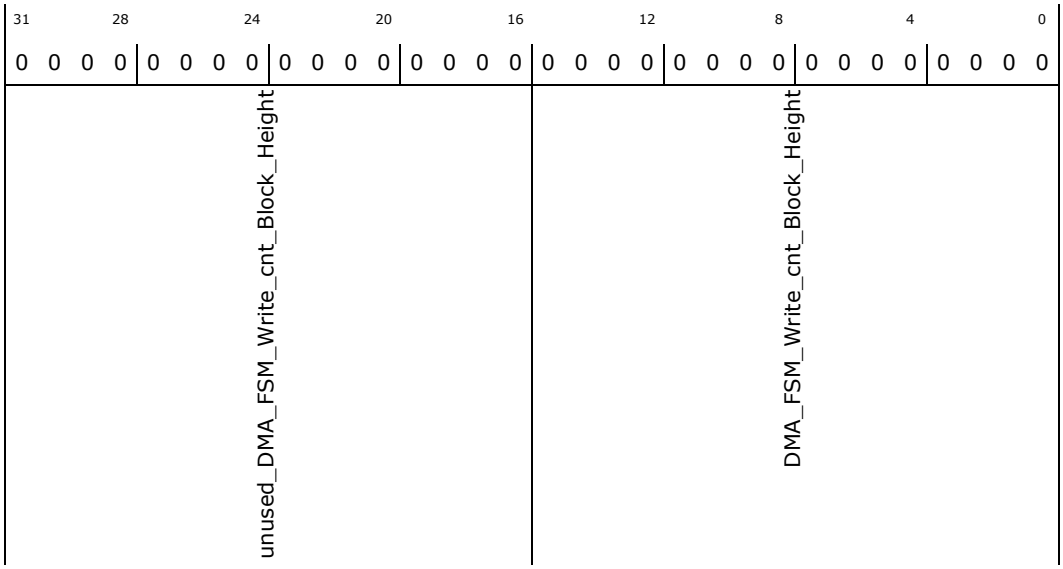
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4211Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Write_cnt_Block_Height):** Unused
15:0	0x0 RO	**DMA_FSM_Write_cnt_Block_Height:** DMA FSM Write counter processed block lines (Yb)

5.2.547 DMA_FSM_Ctrl_req_addr (isp_dma_DMA_FSM_Ctrl_req_addr)—Offset 42210h

DMA FSM Control request address

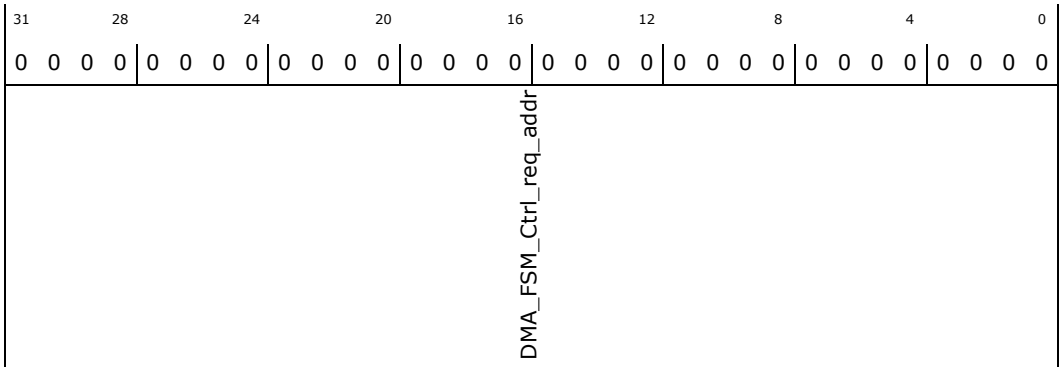
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42210h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_FSM_Ctrl_req_addr:** DMA FSM Control request address

5.2.548 DMA_FSM_Pack_req_cnt_Block_Width (isp_dma_DMA_FSM_Pack_req_cnt_Block_Width)—Offset 42214h

DMA FSM pack request counter block width (Xb)

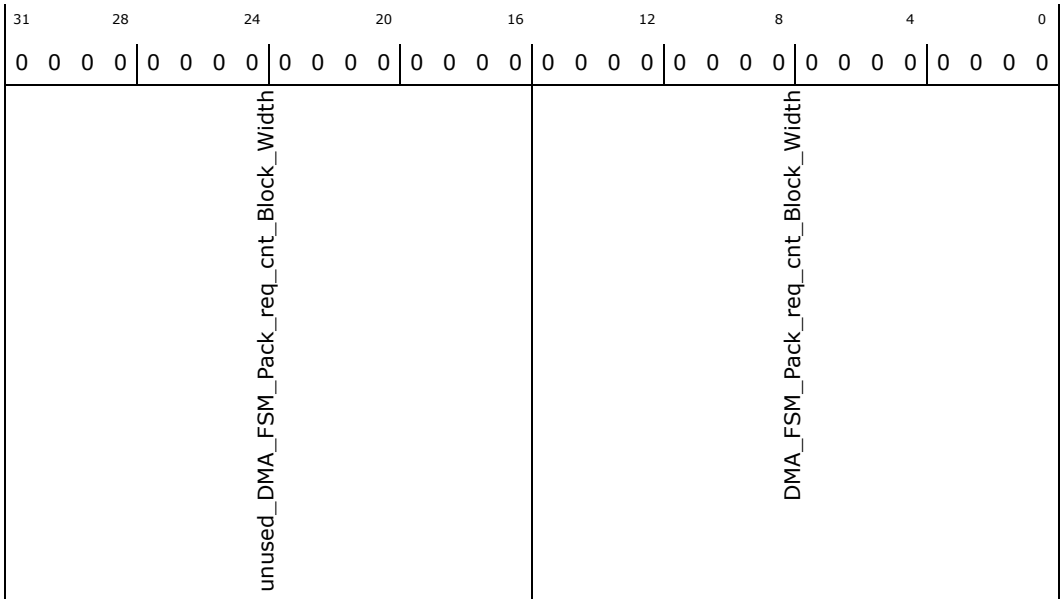
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42214h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Pack_req_cnt_Block_Width):** Unused
15:0	0x0 RO	**DMA_FSM_Pack_req_cnt_Block_Width:** DMA FSM pack request counter block width (Xb)

5.2.549 DMA_FSM_Request_cnt_Block_Width (isp_dma_DMA_FSM_Request_cnt_Block_Width)—Offset 42218h

DMA FSM Request counter block width (Xb)

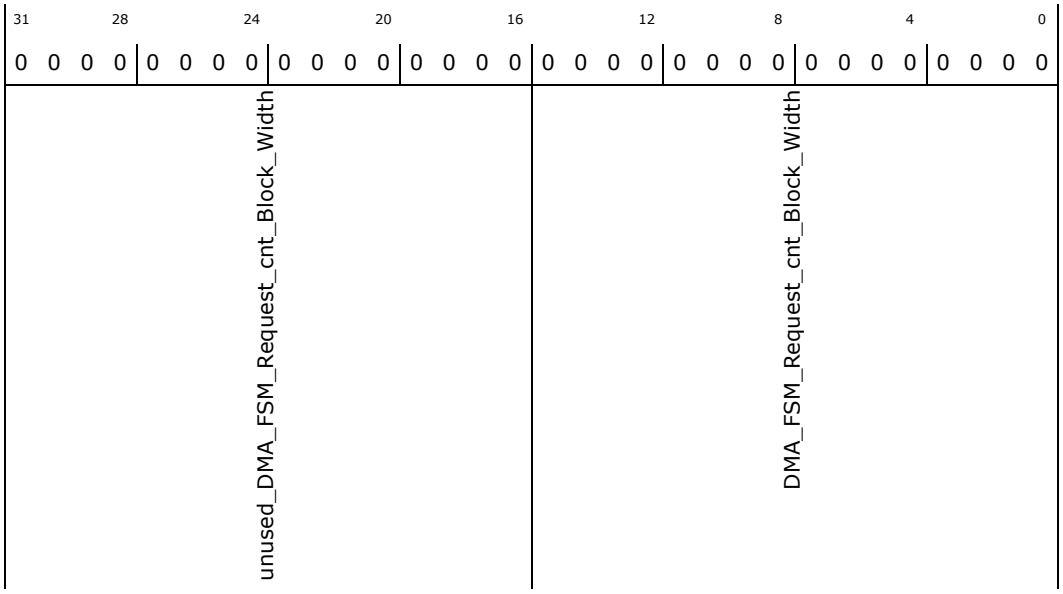
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42218h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Request_cnt_Block_Width):** Unused
15:0	0x0 RO	**DMA_FSM_Request_cnt_Block_Width:** DMA FSM Request counter block width (Xb)

5.2.550 DMA_FSM_Write_cnt_Xb (isp_dma_DMA_FSM_Write_cnt_Xb)—Offset 4221Ch

DMA FSM Write counter width (Xb)

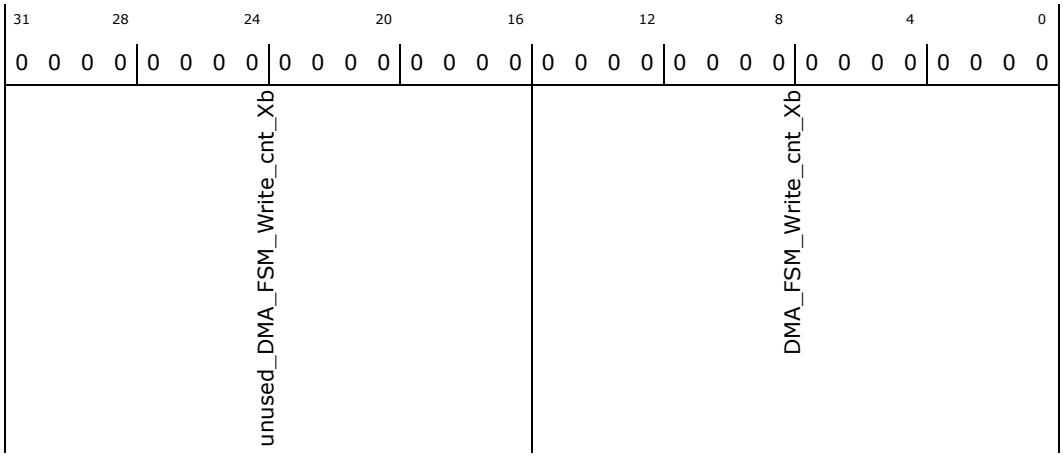
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4221Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Write_cnt_Xb):** Unused
15:0	0x0 RO	**DMA_FSM_Write_cnt_Xb:** DMA FSM Write counter width (Xb)

5.2.551 DMA_FSM_Ctrl_req_stride (isp_dma_DMA_FSM_Ctrl_req_stride)—Offset 42310h

DMA FSM Control request stride

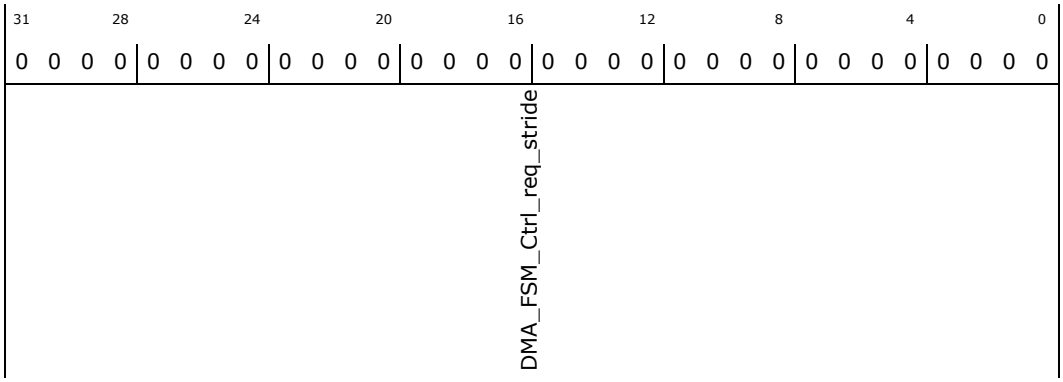
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42310h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_FSM_Ctrl_req_stride:** DMA FSM Control request stride

5.2.552 DMA_FSM_Pack_wr_cnt_Block_Width (isp_dma_DMA_FSM_Pack_wr_cnt_Block_Width)—Offset 42314h

DMA FSM pack write counter block width (Xb)

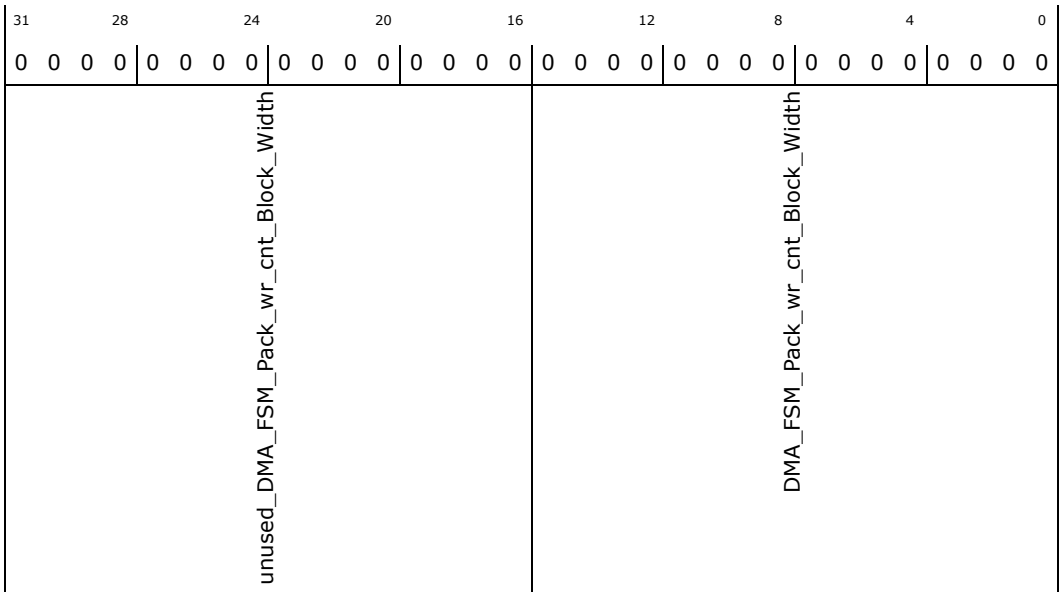
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42314h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Pack_wr_cnt_Block_Width):** Unused
15:0	0x0 RO	**DMA_FSM_Pack_wr_cnt_Block_Width:** DMA FSM pack write counter block width (Xb)

5.2.553 DMA_FSM_Req_remaining_Block_Width (isp_dma_DMA_FSM_Req_remaining_Block_Width)—Offset 42318h

DMA FSM Request counter remaining block width

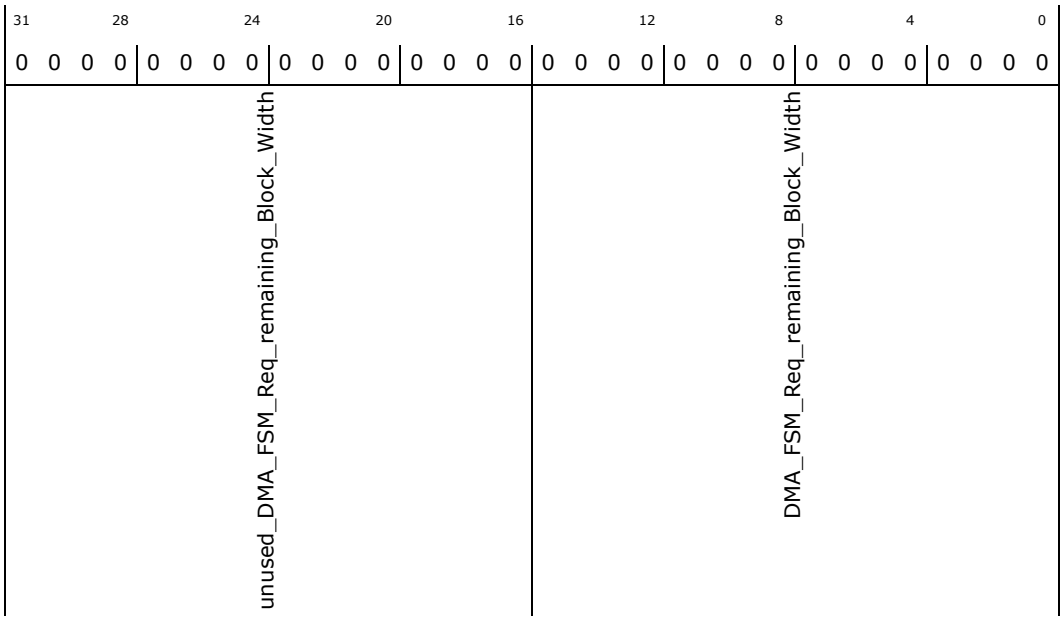
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42318h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Req_remaining_Block_Width):** Unused
15:0	0x0 RO	**DMA_FSM_Req_remaining_Block_Width:** DMA FSM Request counter remaining block width

5.2.554 DMA_FSM_Wr_remaining_Block_Width (isp_dma_DMA_FSM_Wr_remaining_Block_Width)—Offset 4231Ch

DMA FSM Write counter remaining block width

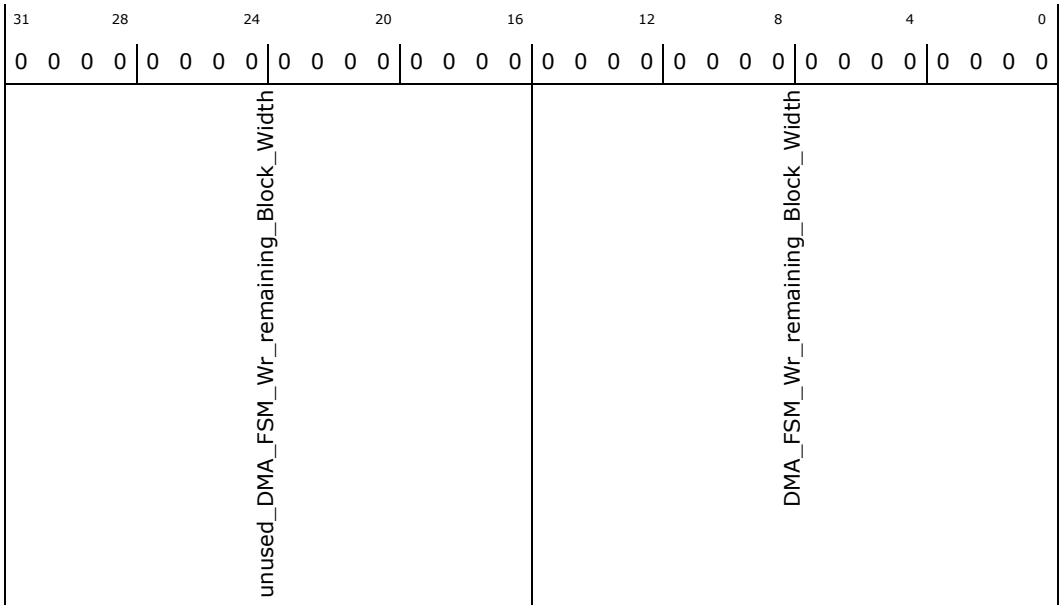
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4231Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Wr_remaining_Block_Width):** Unused
15:0	0x0 RO	**DMA_FSM_Wr_remaining_Block_Width:** DMA FSM Write counter remaining block width

5.2.555 DMA_FSM_Ctrl_req_Block_Width (isp_dma_DMA_FSM_Ctrl_req_Block_Width)—Offset 42410h

DMA FSM Control request block width (Xb)

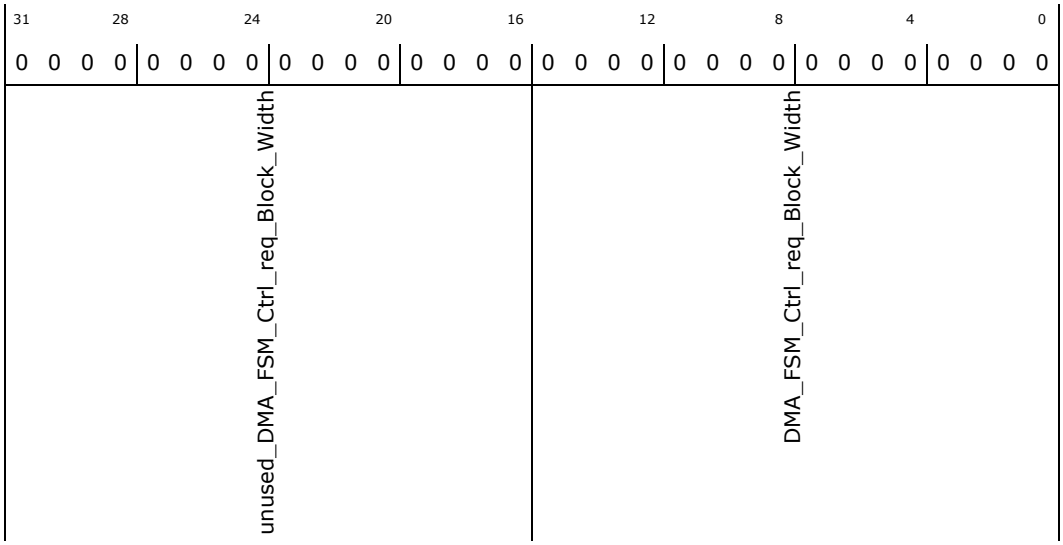
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42410h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_req_Block_Width):** Unused
15:0	0x0 RO	**DMA_FSM_Ctrl_req_Block_Width:** DMA FSM Control request block width (Xb)

5.2.556 DMA_FSM_Req_burst_cnt (isp_dma_DMA_FSM_Req_burst_cnt)—Offset 42418h

DMA FSM Request word burst counter

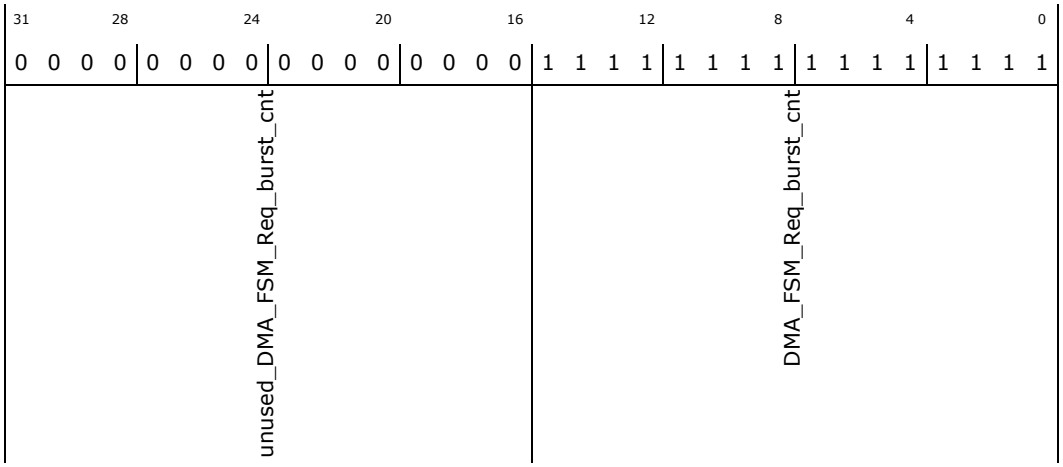
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42418h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000FFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Req_burst_cnt):** Unused
15:0	0xffff RO	**DMA_FSM_Req_burst_cnt:** DMA FSM Request word burst counter

5.2.557 DMA_FSM_Wr_burst_cnt (isp_dma_DMA_FSM_Wr_burst_cnt)—Offset 4241Ch

DMA FSM Write word burst counter

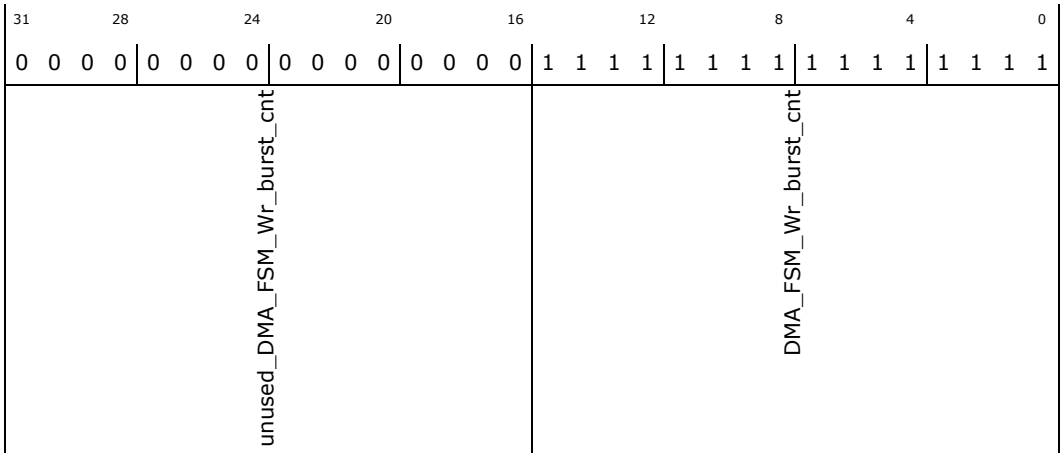
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 4241Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000FFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Wr_burst_cnt):** Unused
15:0	0xffff RO	**DMA_FSM_Wr_burst_cnt:** DMA FSM Write word burst counter

5.2.558 DMA_FSM_Ctrl_req_Block_Height (isp_dma_DMA_FSM_Ctrl_req_Block_Height)—Offset 42510h

DMA FSM Control request height (Yb)

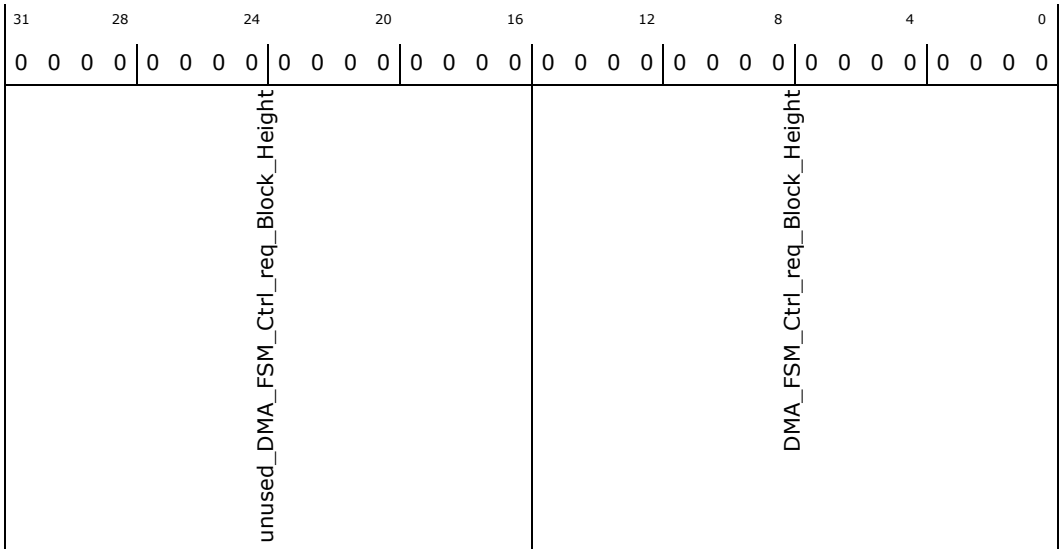
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42510h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_req_Block_Height):** Unused
15:0	0x0 RO	**DMA_FSM_Ctrl_req_Block_Height:** DMA FSM Control request height (Yb)

5.2.559 DMA_FSM_Ctrl_Pack_req_dev_interf_idx (isp_dma_DMA_FSM_Ctrl_Pack_req_dev_interf_idx)—Offset 42610h

DMA FSM Control pack request device idx

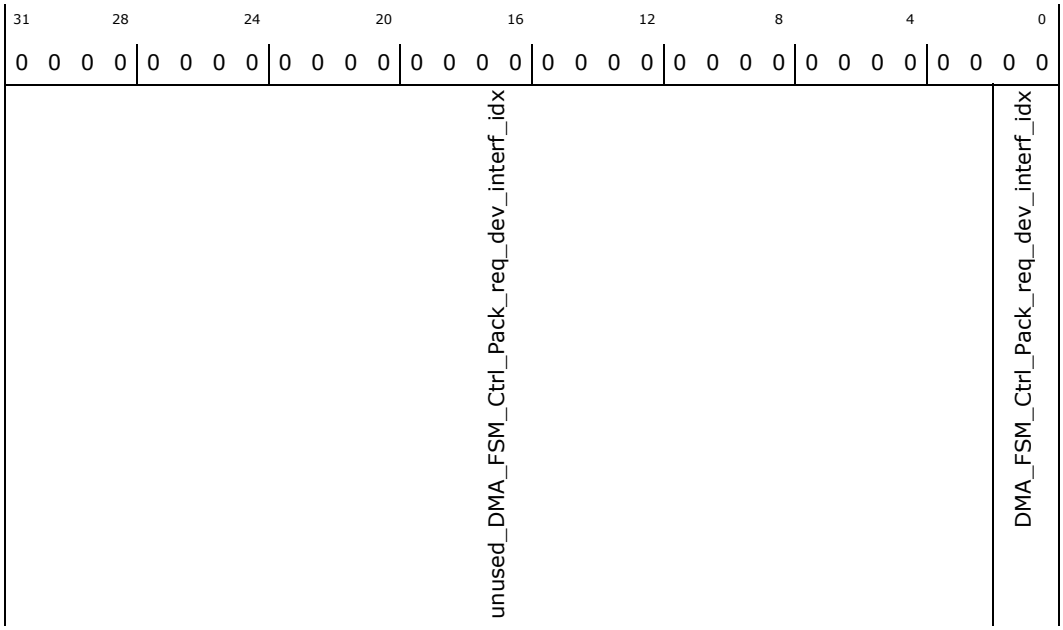
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42610h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_Pack_req_dev_interf_idx):** Unused
1:0	0x0 RO	**DMA_FSM_Ctrl_Pack_req_dev_interf_idx:** DMA FSM Control pack request device idx

5.2.560 DMA_FSM_Ctrl_Pack_wr_dev_interf_idx (isp_dma_DMA_FSM_Ctrl_Pack_wr_dev_interf_idx)—Offset 42710h

DMA FSM Control pack write device idx

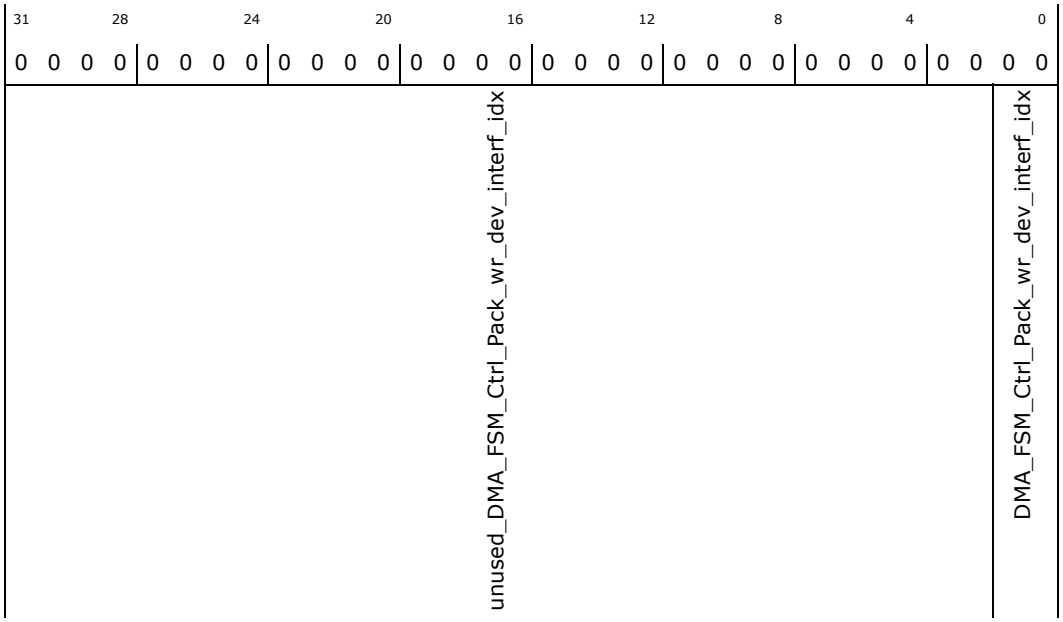
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42710h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_Pack_wr_dev_interf_idx):** Unused
1:0	0x0 RO	**DMA_FSM_Ctrl_Pack_wr_dev_interf_idx:** DMA FSM Control pack write device idx

5.2.561 DMA_FSM_Ctrl_Wr_addr (isp_dma_DMA_FSM_Ctrl_Wr_addr)—Offset 42810h

DMA FSM Control write address

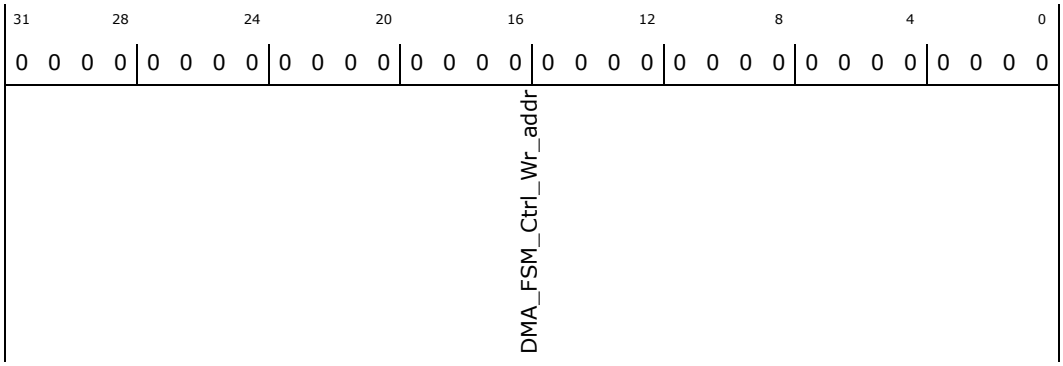
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42810h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_FSM_Ctrl_Wr_addr:** DMA FSM Control write address

5.2.562 DMA_FSM_Ctrl_Wr_stride (isp_dma_DMA_FSM_Ctrl_Wr_stride)—Offset 42910h

DMA FSM Control write stride

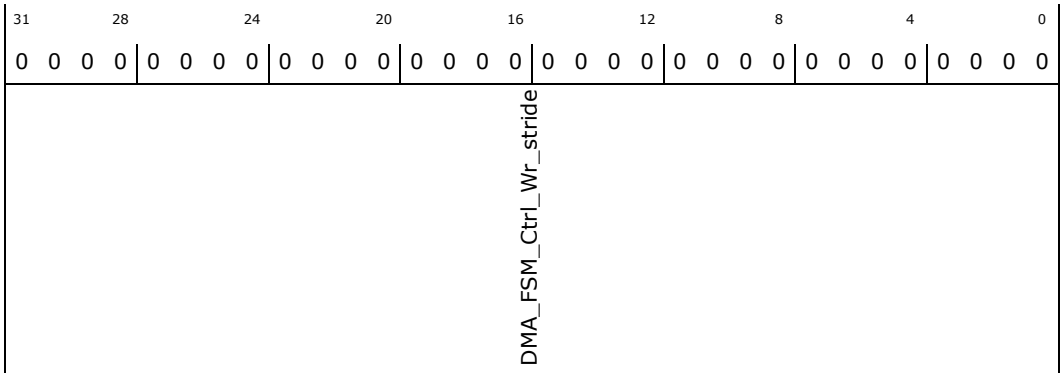
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42910h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_FSM_Ctrl_Wr_stride:** DMA FSM Control write stride

5.2.563 DMA_FSM_Ctrl_pack_req_Block_Width (isp_dma_DMA_FSM_Ctrl_pack_req_Block_Width)—Offset 42A10h

DMA FSM Control FSM Pack request block width (Xb)

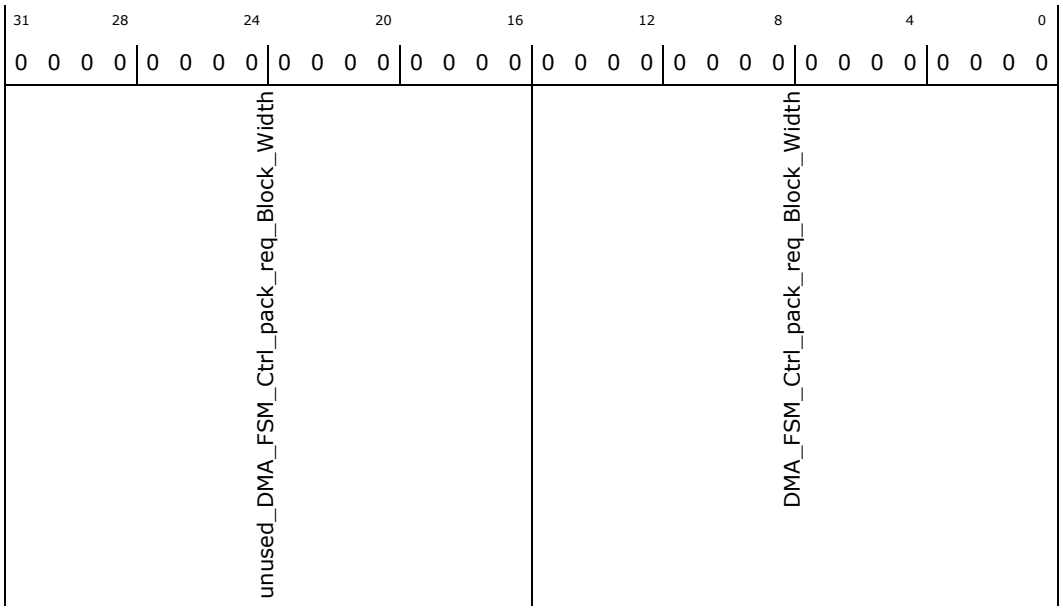
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42A10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_pack_req_Block_Width):** Unused
15:0	0x0 RO	**DMA_FSM_Ctrl_pack_req_Block_Width:** DMA FSM Control FSM Pack request block width (Xb)

5.2.564 DMA_FSM_Ctrl_pack_Block_Height (isp_dma_DMA_FSM_Ctrl_pack_Block_Height)—Offset 42B10h

DMA FSM Control FSM Pack block height (Yb), in terms of lines

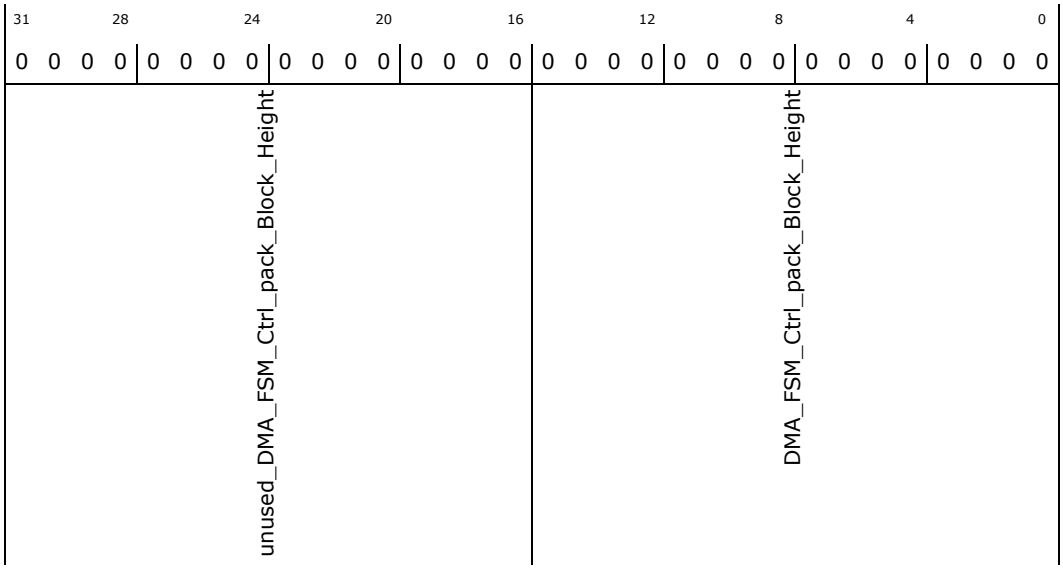
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42B10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_pack_Block_Height):** Unused
15:0	0x0 RO	**DMA_FSM_Ctrl_pack_Block_Height:** DMA FSM Control FSM Pack block height (Yb), in terms of lines

5.2.565 DMA_FSM_Ctrl_pack_wr_Block_Width (isp_dma_DMA_FSM_Ctrl_pack_wr_Block_Width)—Offset 42C10h

DMA FSM Control FSM Pack write block width (Xb)

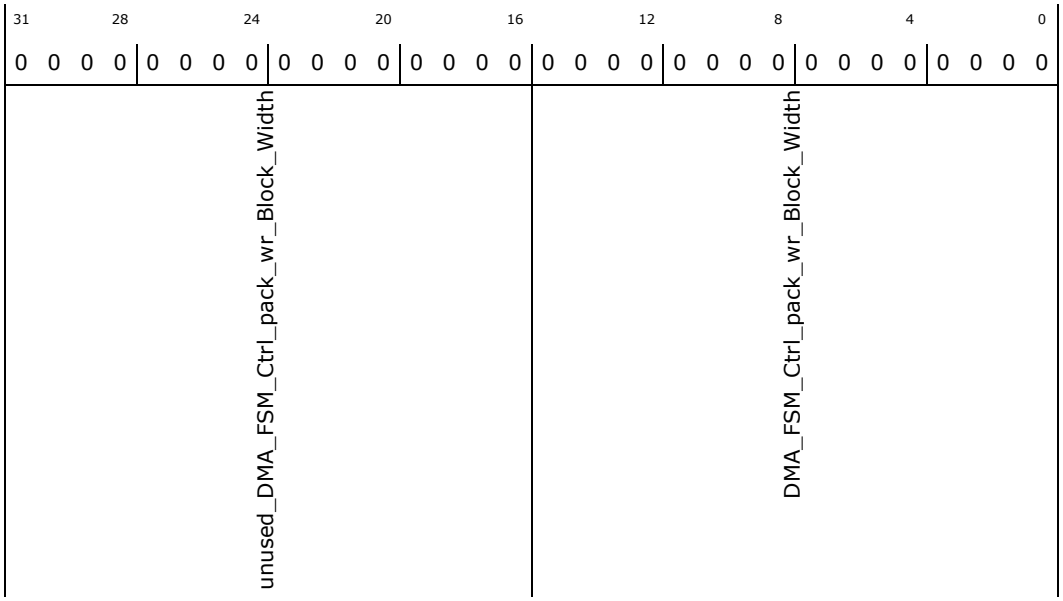
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42C10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_pack_wr_Block_Width):** Unused
15:0	0x0 RO	**DMA_FSM_Ctrl_pack_wr_Block_Width:** DMA FSM Control FSM Pack write block width (Xb)

5.2.566 DMA_FSM_Ctrl_pack_req_elem (isp_dma_DMA_FSM_Ctrl_pack_req_elem)—Offset 42D10h

DMA FSM Control pack request element per word

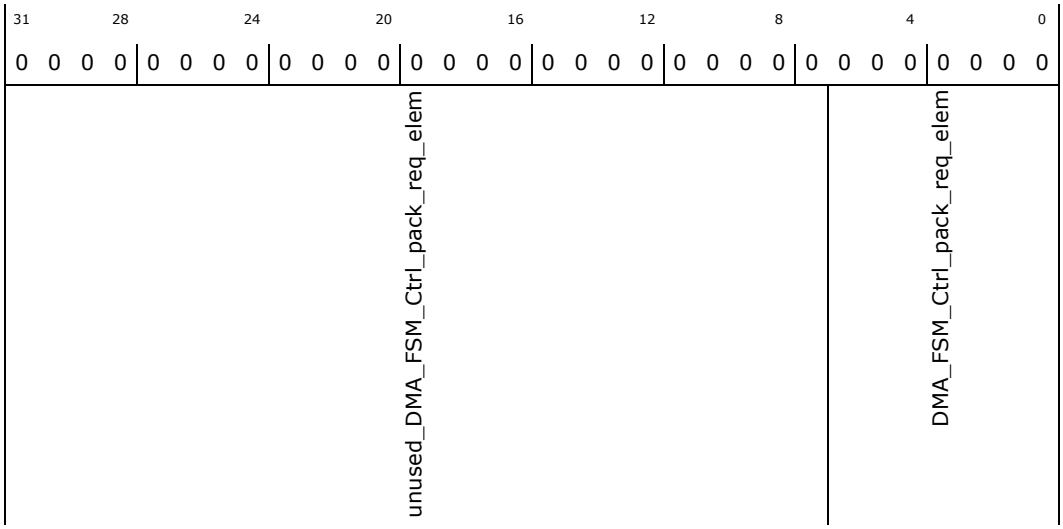
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42D10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:7	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_pack_req_elem):** Unused
6:0	0x0 RO	**DMA_FSM_Ctrl_pack_req_elem:** DMA FSM Control pack request element per word

5.2.567 DMA_FSM_Ctrl_pack_wr_elem (isp_dma_DMA_FSM_Ctrl_pack_wr_elem)—Offset 42E10h

DMA FSM Control pack write element per word

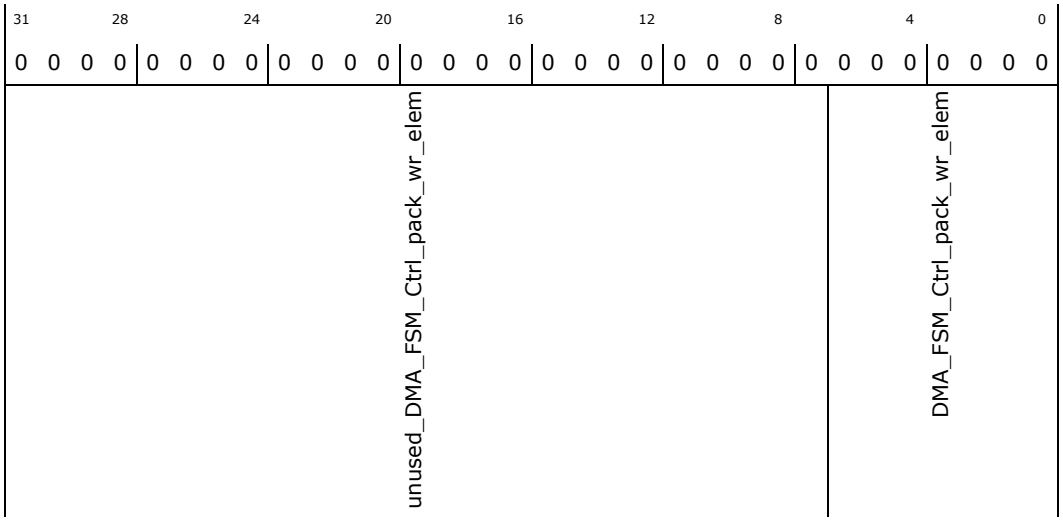
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42E10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:7	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_pack_wr_elem):** Unused
6:0	0x0 RO	**DMA_FSM_Ctrl_pack_wr_elem:** DMA FSM Control pack write element per word

5.2.568 DMA_FSM_Ctrl_pack_sgnzext_ctrl_idx (isp_dma_DMA_FSM_Ctrl_pack_sgnzext_ctrl_idx)—Offset 42F10h

DMA FSM Control pack element sign zero extension and controller index

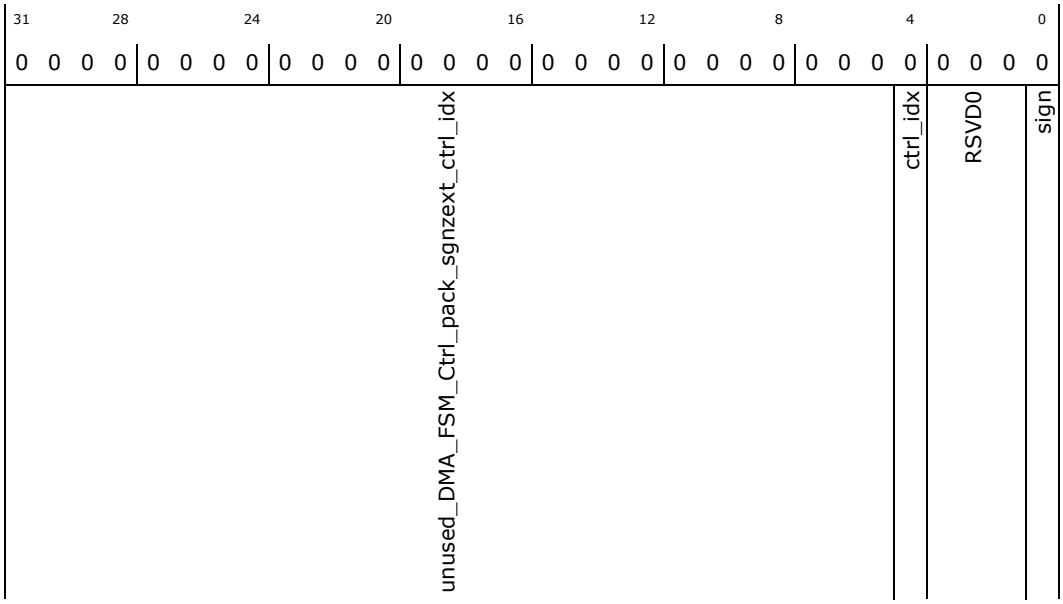
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 42F10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_FSM_Ctrl_pack_sgnzext_ctrl_idx):** Unused
4	0x0 RO	**ctrl_idx:** Controller index
3:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RO	**sign:** element sign(1)/zero(0) extension

5.2.569 Dev_Interf_0_status_req_side (isp_dma_Dev_Interf_0_status_req_side)—Offset 43000h

DMA Device interface 0 internal side status

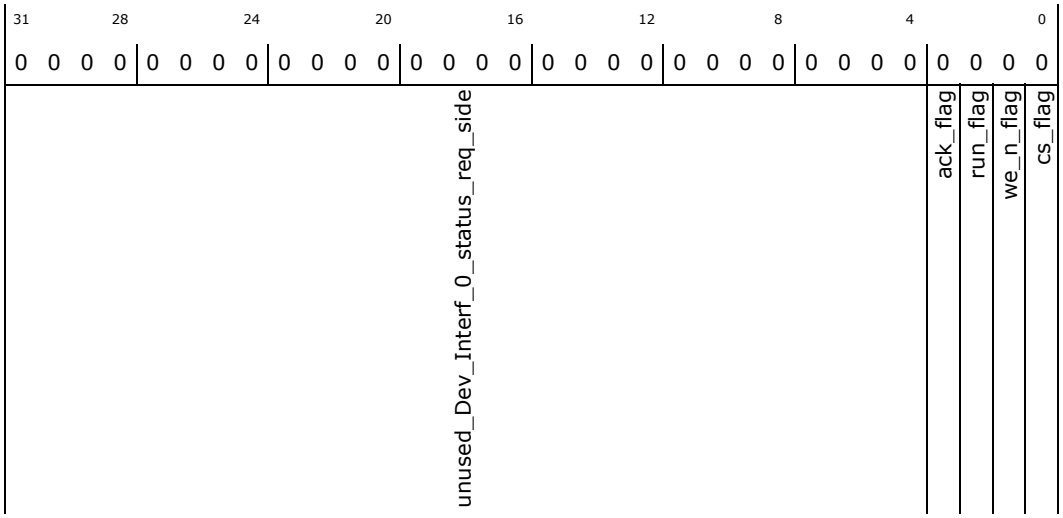
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 43000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_Dev_Interf_0_status_req_side):** Unused
3	0x0 RO	**ack_flag:** Ack flag
2	0x0 RO	**run_flag:** Run flag
1	0x0 RO	**we_n_flag:** We_n flag
0	0x0 RO	**cs_flag:** CS flag

5.2.570 Dev_Interf_1_status_req_side (isp_dma_Dev_Interf_1_status_req_side)—Offset 43004h

DMA Device interface 1 internal side status

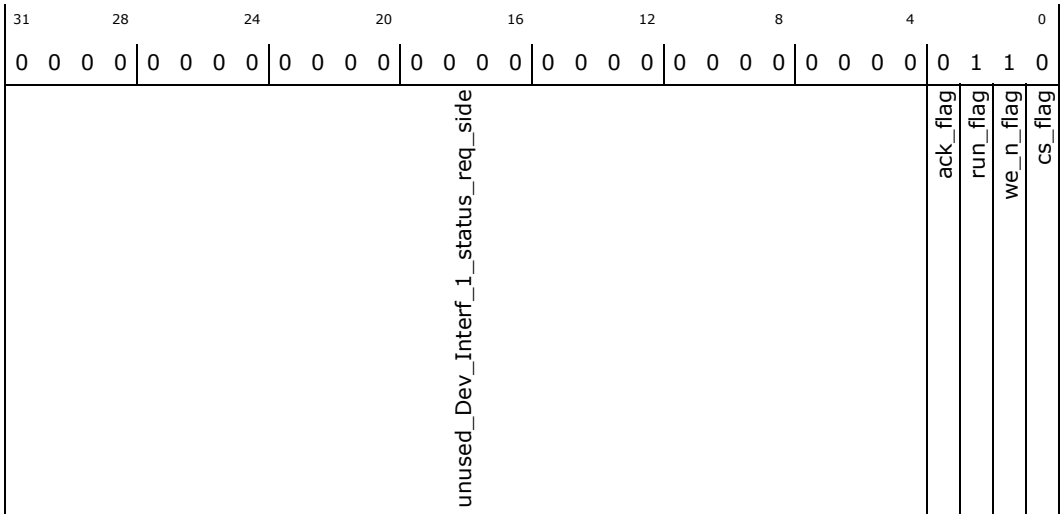
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 43004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000006h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_Dev_Interf_1_status_req_side):** Unused
3	0x0 RO	**ack_flag:** Ack flag
2	0x1 RO	**run_flag:** Run flag
1	0x1 RO	**we_n_flag:** We_n flag
0	0x0 RO	**cs_flag:** CS flag

5.2.571 Dev_Interf_2_status_req_side (isp_dma_Dev_Interf_2_status_req_side)—Offset 43008h

DMA Device interface 2 internal side status

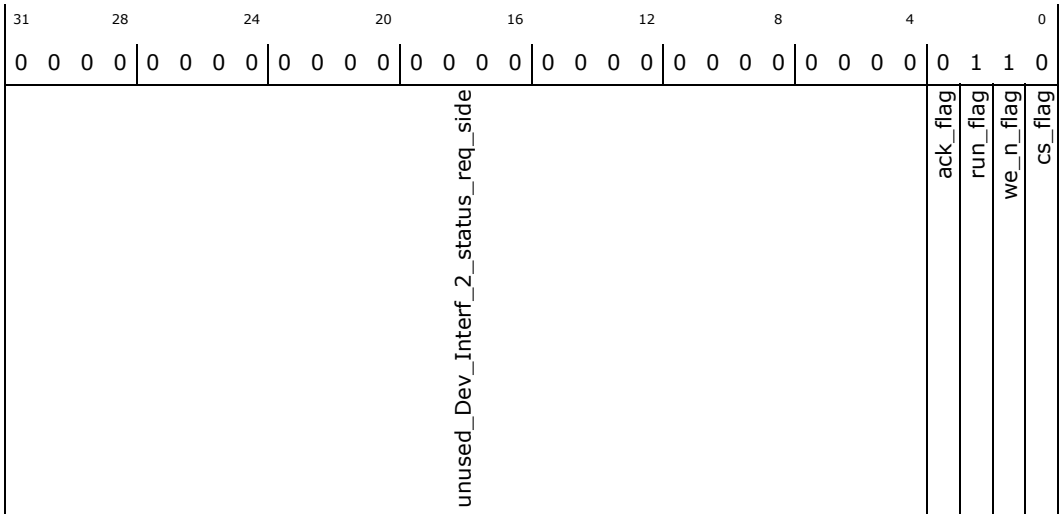
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 43008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000006h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_Dev_Interf_2_status_req_side):** Unused
3	0x0 RO	**ack_flag:** Ack flag
2	0x1 RO	**run_flag:** Run flag
1	0x1 RO	**we_n_flag:** We_n flag
0	0x0 RO	**cs_flag:** CS flag

5.2.572 Dev_Interf_0_status_send_side (isp_dma_Dev_Interf_0_status_send_side)—Offset 43100h

DMA Device interface 0 output side status

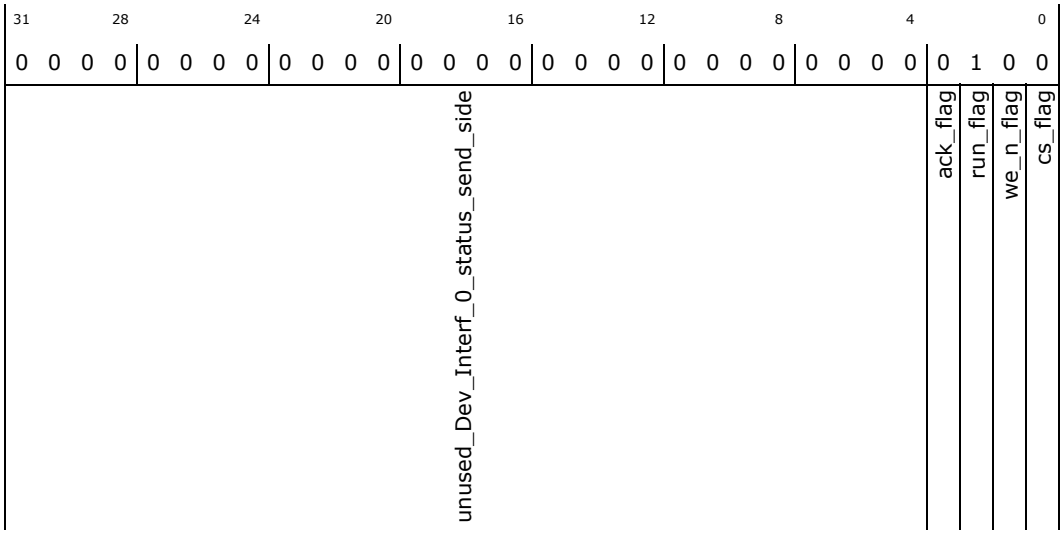
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 43100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_Dev_Interf_0_status_send_side):** Unused
3	0x0 RO	**ack_flag:** Ack flag
2	0x1 RO	**run_flag:** Run flag
1	0x0 RO	**we_n_flag:** We_n flag
0	0x0 RO	**cs_flag:** CS flag

5.2.573 Dev_Interf_1_status_send_side (isp_dma_Dev_Interf_1_status_send_side)—Offset 43104h

DMA Device interface 1 output side status

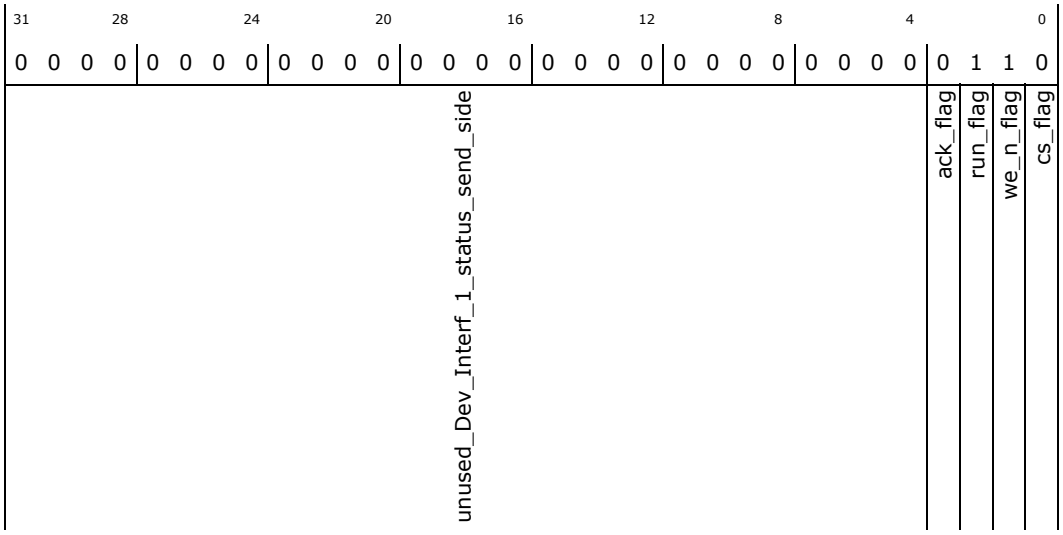
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 43104h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000006h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_Dev_Interf_1_status_send_side):** Unused
3	0x0 RO	**ack_flag:** Ack flag
2	0x1 RO	**run_flag:** Run flag
1	0x1 RO	**we_n_flag:** We_n flag
0	0x0 RO	**cs_flag:** CS flag

5.2.574 Dev_Interf_2_status_send_side (isp_dma_Dev_Interf_2_status_send_side)—Offset 43108h

DMA Device interface 2 output side status

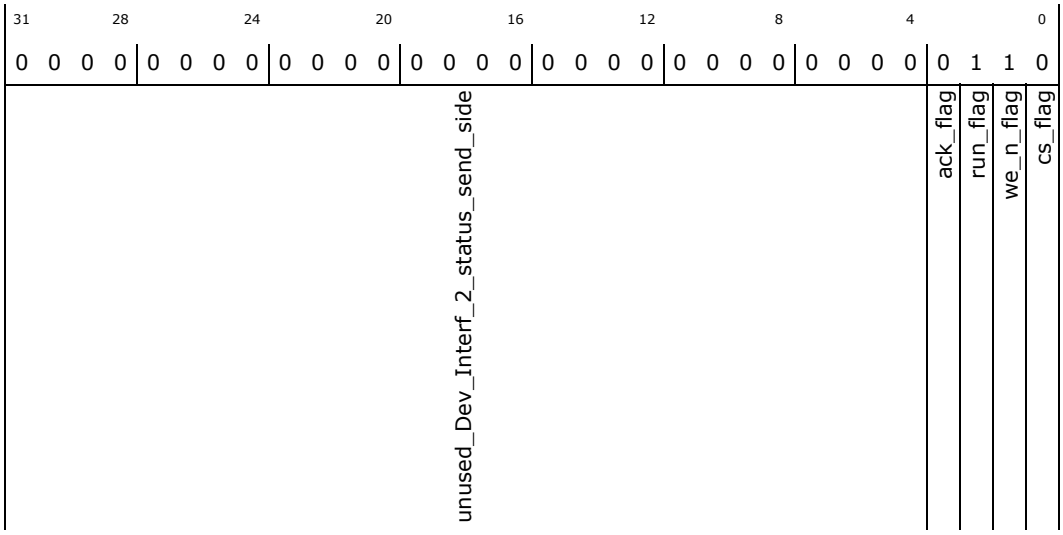
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 43108h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000006h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_Dev_Interf_2_status_send_side):** Unused
3	0x0 RO	**ack_flag:** Ack flag
2	0x1 RO	**run_flag:** Run flag
1	0x1 RO	**we_n_flag:** We_n flag
0	0x0 RO	**cs_flag:** CS flag

5.2.575 Dev_Interf_0_Fifo_status (isp_dma_Dev_Interf_0_Fifo_status)—Offset 43200h

Device Interface 0 FIFO status

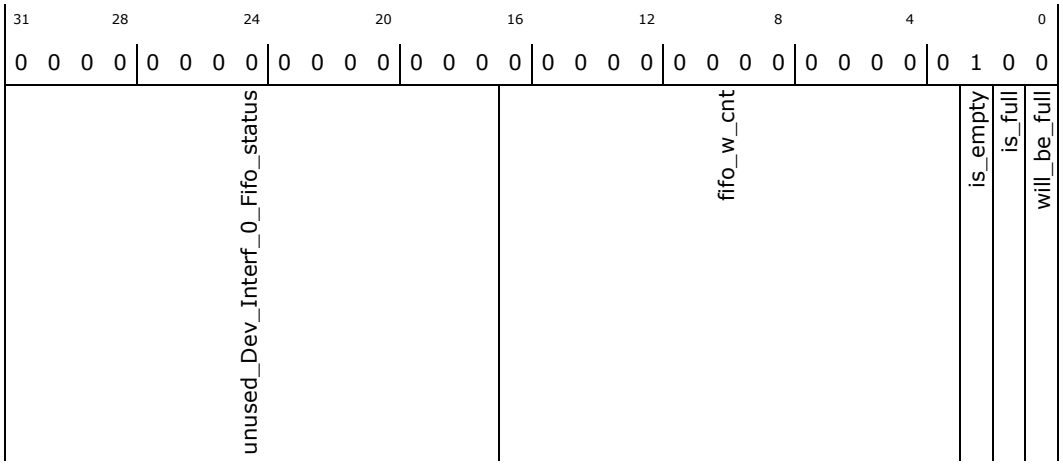
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 43200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h



Bit Range	Default and Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (unused_Dev_Interf_0_Fifo_status):** Unused
16:3	0x0 RO	**fifo_w_cnt:** Fifo word counter
2	0x1 RO	**is_empty:** FIFO is empty
1	0x0 RO	**is_full:** FIFO is full
0	0x0 RO	**will_be_full:** FIFO will be full

5.2.576 Dev_Interf_1_Fifo_status (isp_dma_Dev_Interf_1_Fifo_status)—Offset 43204h

Device Interface 1 FIFO status

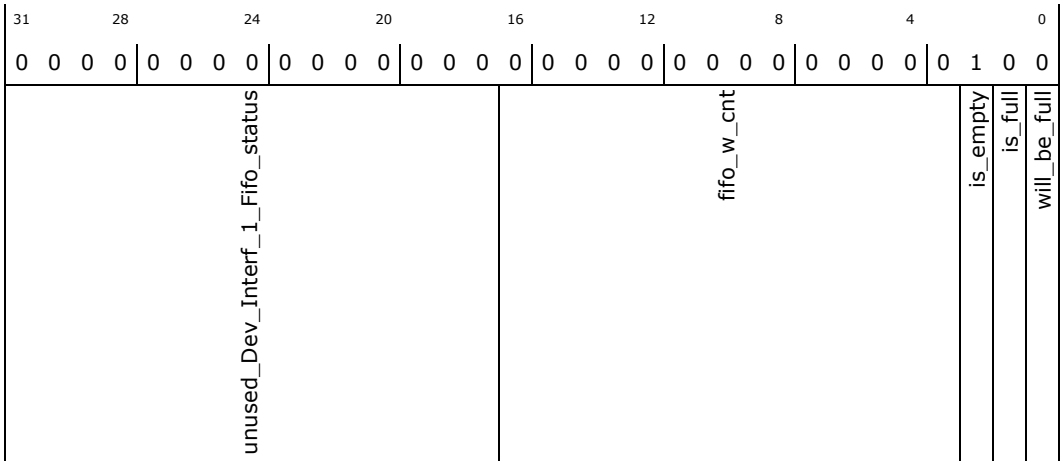
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 43204h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h



Bit Range	Default and Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (unused_Dev_Interf_1_Fifo_status):** Unused
16:3	0x0 RO	**fifo_w_cnt:** FIFO word counter
2	0x1 RO	**is_empty:** FIFO is empty
1	0x0 RO	**is_full:** FIFO is full
0	0x0 RO	**will_be_full:** FIFO will be full

5.2.577 Dev_Interf_2_Fifo_status (isp_dma_Dev_Interf_2_Fifo_status)—Offset 43208h

Device Interface 2 FIFO status

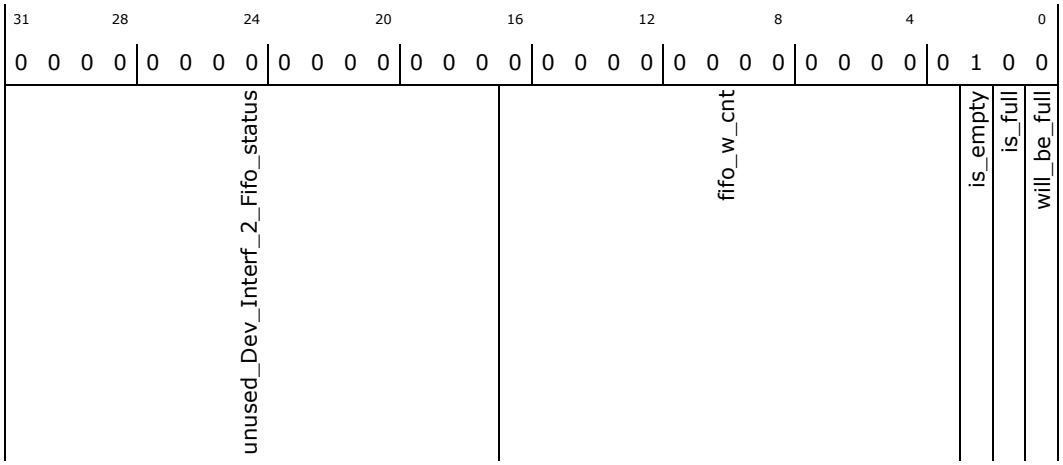
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 43208h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h



Bit Range	Default and Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (unused_Dev_Interf_2_Fifo_status):** Unused
16:3	0x0 RO	**fifo_w_cnt:** FIFO word counter
2	0x1 RO	**is_empty:** FIFO is empty
1	0x0 RO	**is_full:** FIFO is full
0	0x0 RO	**will_be_full:** FIFO will be full

5.2.578 Dev_Interf_0_Req_complete_bust (isp_dma_Dev_Interf_0_Req_complete_bust)—Offset 43300h

DMA Device interface 0 Request only complete burst

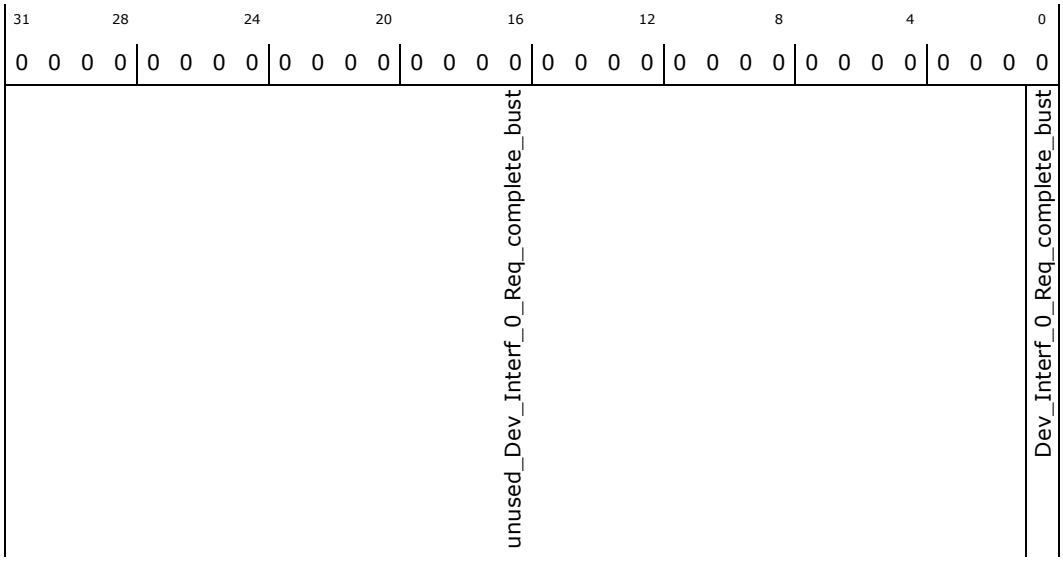
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 43300h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_Dev_Interf_0_Req_complete_bust):** Unused
0	0x0 RW	**Dev_Interf_0_Req_complete_bust:** DMA Device interface 0 Request only complete burst

5.2.579 Dev_Interf_1_Req_complete_bust (isp_dma_Dev_Interf_1_Req_complete_bust)—Offset 43304h

DMA Device interface 1 Request only complete burst

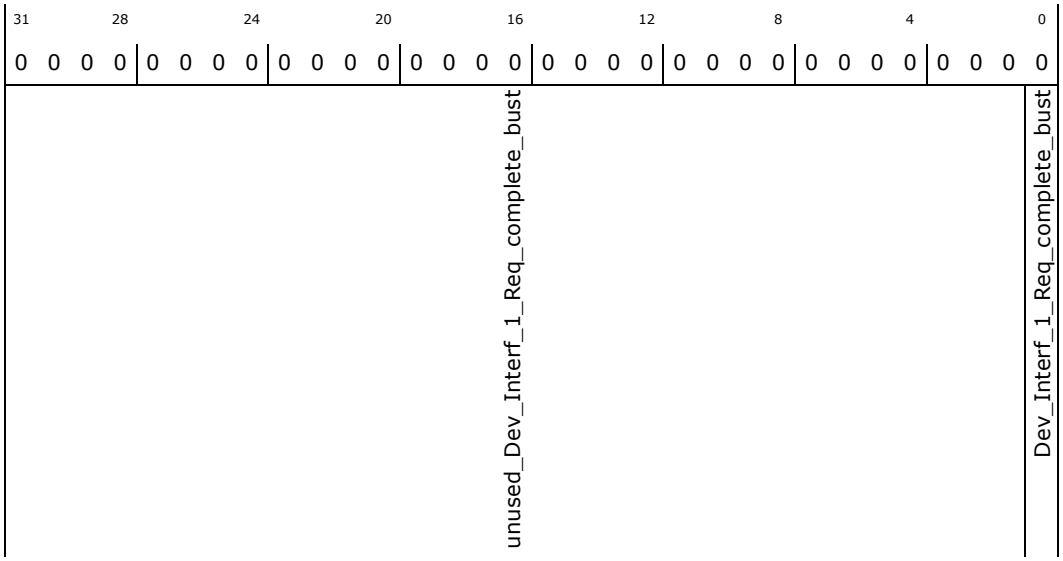
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 43304h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_Dev_Interf_1_Req_complete_bust):** Unused
0	0x0 RW	**Dev_Interf_1_Req_complete_bust:** DMA Device interface 1 Request only complete burst

5.2.580 Dev_Interf_2_Req_complete_bust (isp_dma_Dev_Interf_2_Req_complete_bust)—Offset 43308h

DMA Device interface 2 Request only complete burst

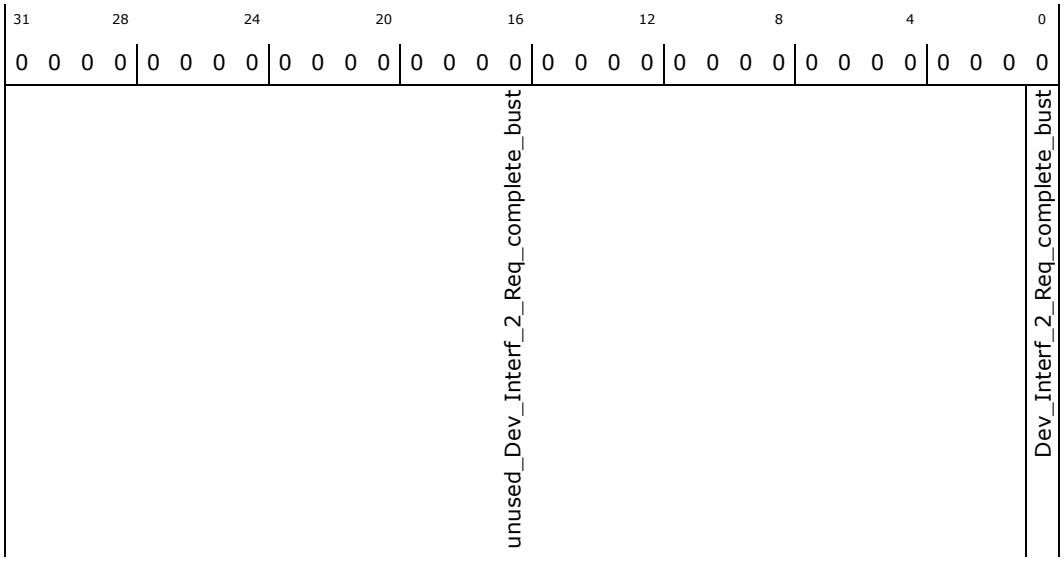
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 43308h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_Dev_Interf_2_Req_complete_bust):** Unused
0	0x0 RW	**Dev_Interf_2_Req_complete_bust:** DMA Device interface 2 Request only complete burst

5.2.581 Dev_Interf_2_Max_Burst_Size (isp_dma_Dev_Interf_2_Max_Burst_Size)—Offset 43408h

DMA Device interface 2 maximum burst size

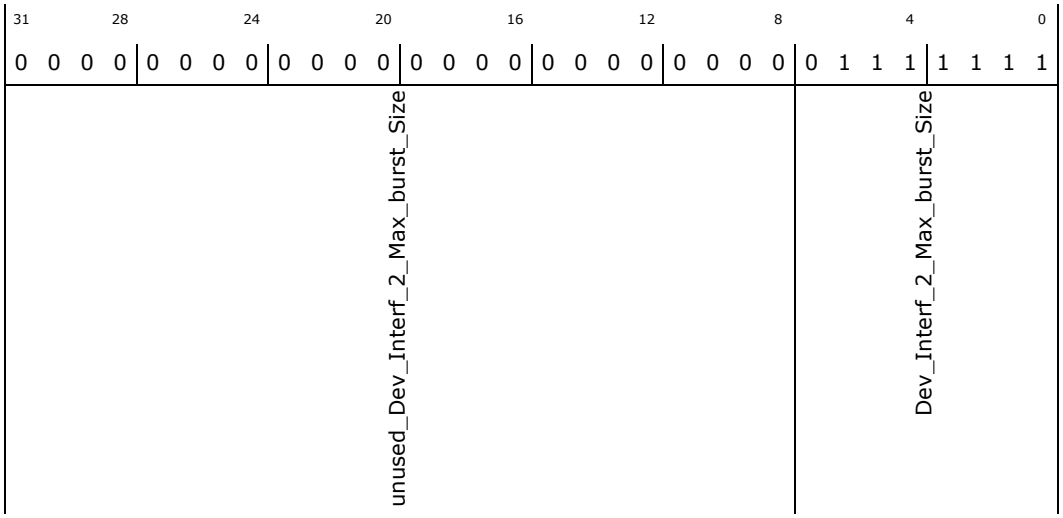
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 43408h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000007Fh



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved (unused_Dev_Interf_2_Max_Burst_Size):** Unused
7:0	0x7f RW	**Dev_Interf_2_Max_Burst_Size:** DMA Device interface 2 maximum burst size

5.2.582 reg0 (gdc1_reg0)—Offset 50000h

Status register: Current opx, opy, top-level FSM state

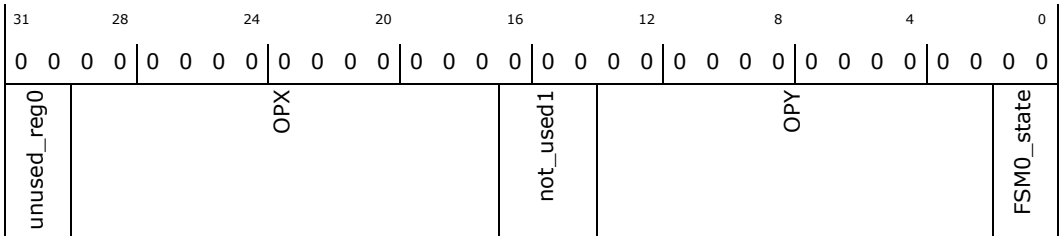
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved (unused_reg0):** Unused

Bit Range	Default and Access	Field Name (ID): Description
29:17	0x0 RO	**OPX:** OPX value
16:14	0x0 RO	**not_used1:** N/A
13:2	0x0 RO	**OPY:** OPY value
1:0	0x0 RO	**FSM0_state:** FSM0 state: 00=Idle; 01=Busy-receiving data needed to kick the device; 10=Busy-wait state; 11=Busy-run state

5.2.583 woi_x (gdc1_woi_x)—Offset 50004h

Configured X dimension of the internal window-of-interest (local memory)

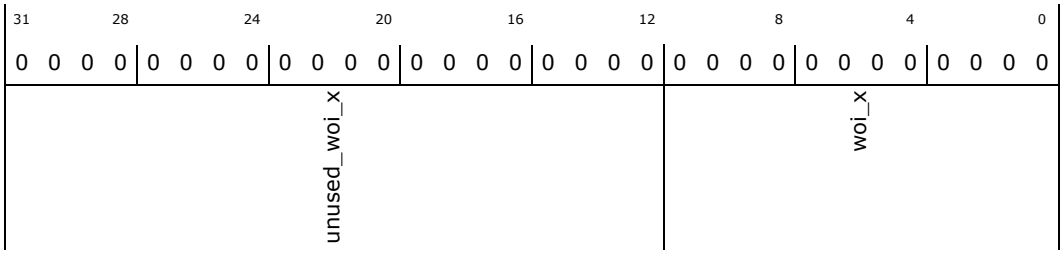
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_woi_x):** Unused
11:0	0x0 RO	**woi_x:** Configured X dimension of the internal window-of-interest (local memory)

5.2.584 woi_y (gdc1_woi_y)—Offset 50008h

Configured Y dimension of the internal window-of-interest (local memory)

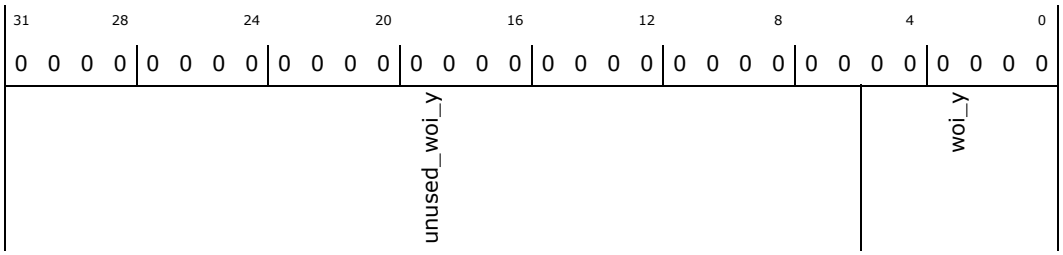
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_woi_y):** Unused
5:0	0x0 RO	**woi_y:** Configured Y dimension of the internal window-of-interest (local memory)

5.2.585 bpp (gdc1_bpp)—Offset 5000Ch

Bits per input/output pixel, allowed: 8, 10, 12, 14

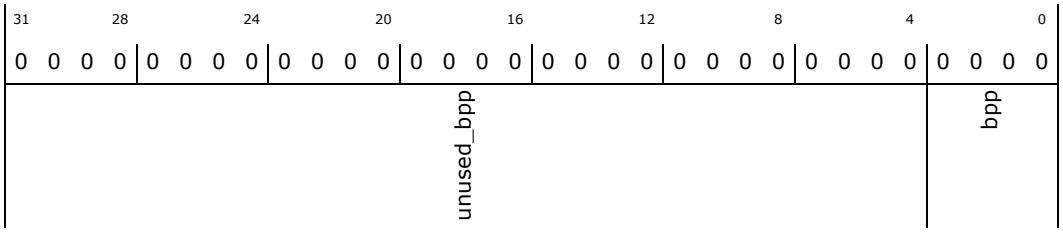
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 5000Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RW	**Reserved (unused_bpp):** Unused
3:0	0x0 RW	**bpp:** Bits per input/output pixel, allowed: 8, 10, 12, 14

5.2.586 fryipxfrx_start (gdc1_fryipxfrx_start)—Offset 50010h

Fractional component of the starting X and Y position for scaling given in fixed point notation

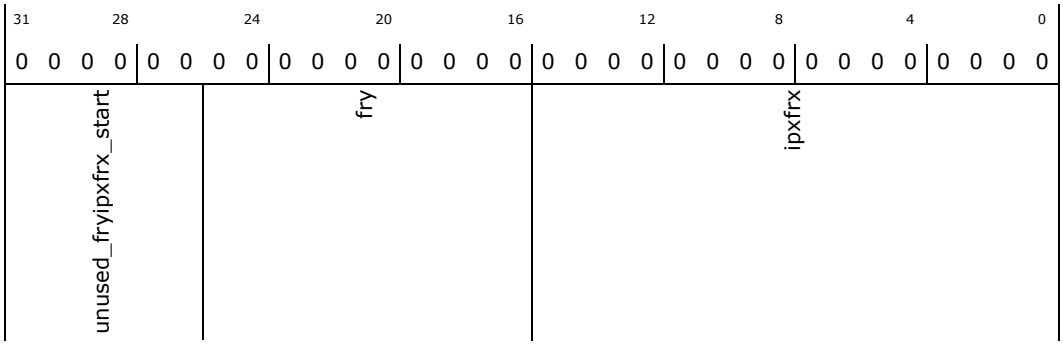
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:26	0x0 RO	**Reserved (unused_fryipxfrx_start):** Unused
25:16	0x0 RW	**fry:** Fractional component of the Y start
15:0	0x0 RW	**ipxfrx:** Integer (6) and Fractional (10) component of the X start

5.2.587 oxdim (gdc1_oxdim)—Offset 50014h

Output X dimension of the produced block of pixels

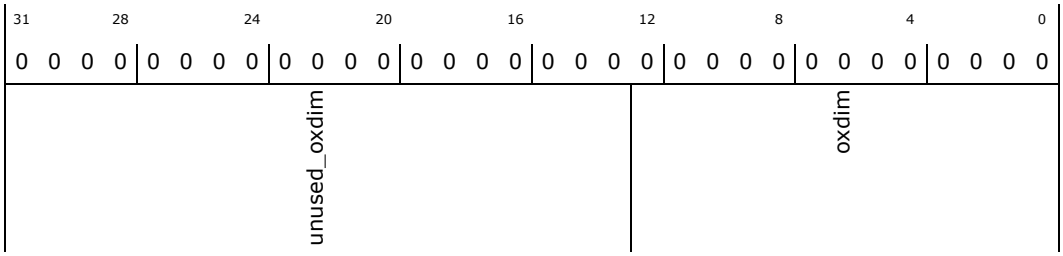
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:13	0x0 RW	**Reserved (unused_oxdim):** Unused
12:0	0x0 RW	**oxdim:** Output X dimension of the produced block of pixels

5.2.588 oydim (gdc1_oydim)—Offset 50018h

Output Y dimension of the produced block of pixels

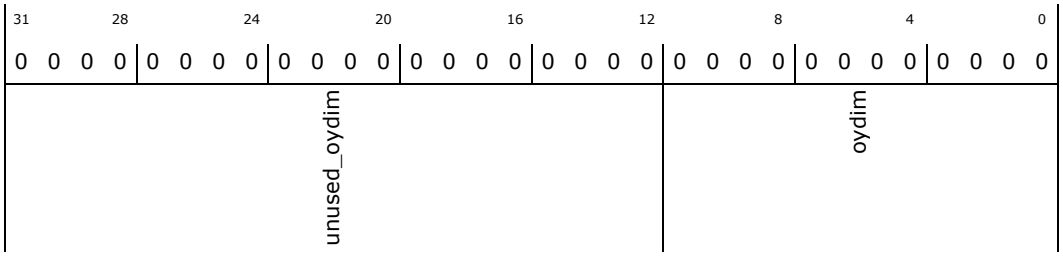
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_oydim):** Unused
11:0	0x0 RW	**oydim:** Output Y dimension of the produced block of pixels

5.2.589 src_addr (gdc1_src_addr)—Offset 5001Ch

Source (input) pixel base address [byte-based]

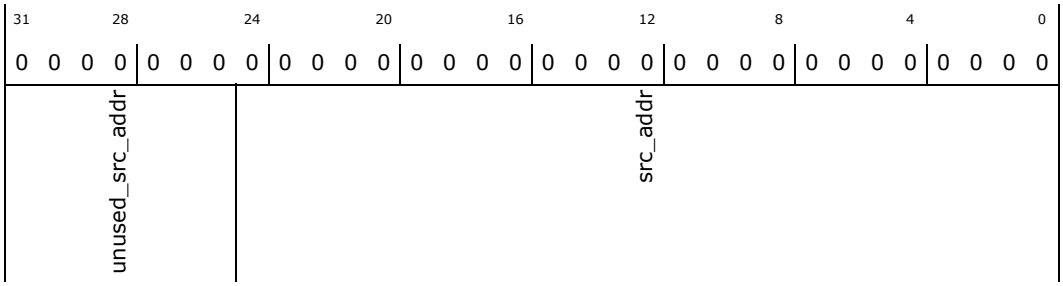
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 5001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:25	0x0 RW	**Reserved (unused_src_addr):** Unused
24:0	0x0 RW	**src_addr:** Source (input) pixel base address [byte-based]

5.2.590 src_end (gdc1_src_end)—Offset 50020h

End address. When reached wrap around. [byte-based]

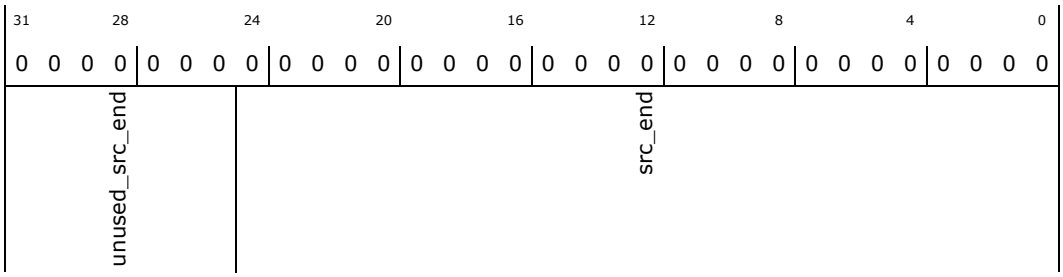
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:25	0x0 RW	**Reserved (unused_src_end):** Unused
24:0	0x0 RW	**src_end:** End address. When reached wrap around. [byte-based]

5.2.591 src_wrap (gdc1_src_wrap)—Offset 50024h

Wrap addr. Wrap here when src_end reached [byte-based]

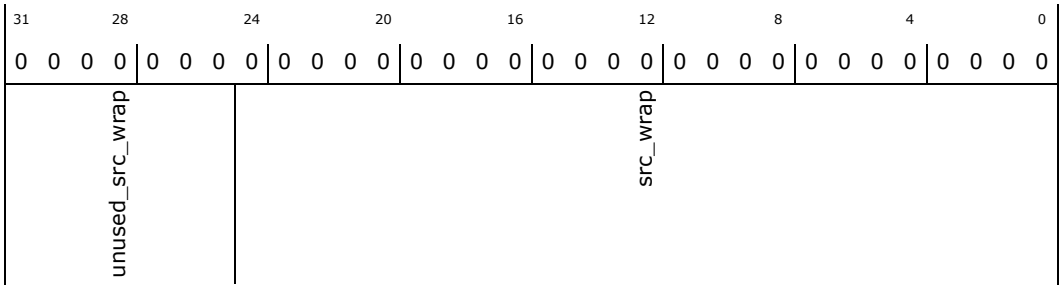
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:25	0x0 RW	**Reserved (unused_src_wrap):** Unused
24:0	0x0 RW	**src_wrap:** Wrap addr. Wrap here when src_end reached [byte-based]

5.2.592 src_stride (gdc1_src_stride)—Offset 50028h

Source (input) pixel stride [byte-based]

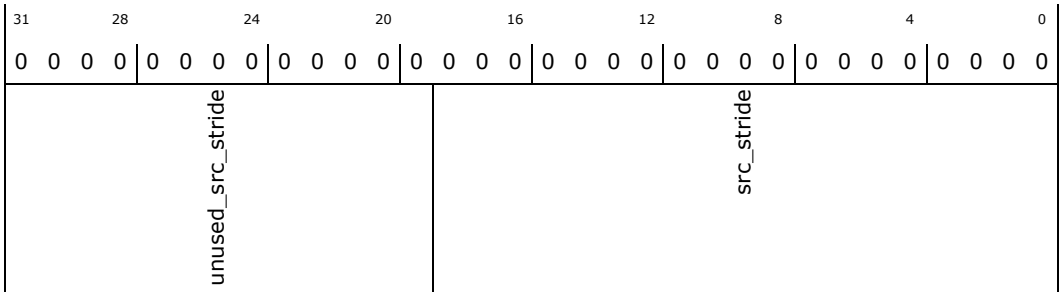
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:19	0x0 RW	**Reserved (unused_src_stride):** Unused
18:0	0x0 RW	**src_stride:** Source (input) pixel stride [byte-based]

5.2.593 dst_addr (gdc1_dst_addr)—Offset 5002Ch

Destination (output) pixel base address [byte-based]

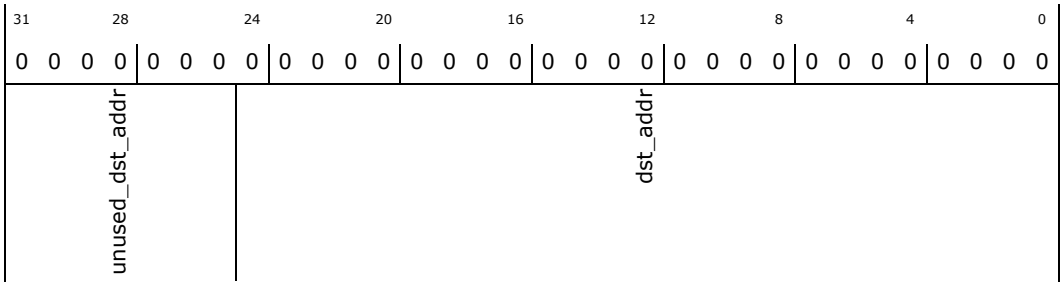
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 5002Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:25	0x0 RW	**Reserved (unused_dst_addr):** Unused
24:0	0x0 RW	**dst_addr:** Destination (output) pixel base address [byte-based]

5.2.594 dst_stride (gdc1_dst_stride)—Offset 50030h

Destination (output) pixel stride [byte-based]

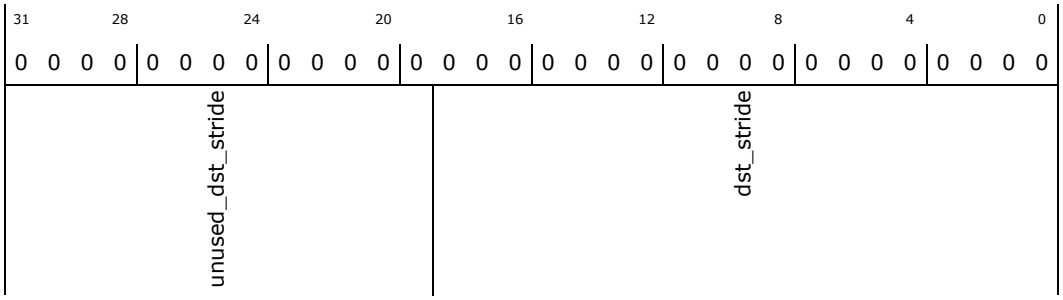
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:19	0x0 RW	**Reserved (unused_dst_stride):** Unused
18:0	0x0 RW	**dst_stride:** Destination (output) pixel stride [byte-based]

5.2.595 dx (gdc1_dx)—Offset 50034h

Scaling only: Horizontal scaling factor

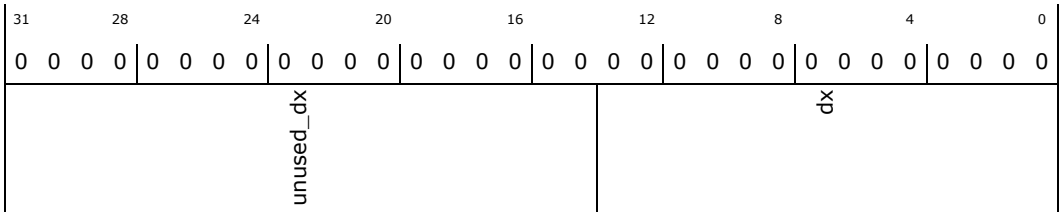
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RW	**Reserved (unused_dx):** Unused
13:0	0x0 RW	**dx:** Scaling only: Horizontal scaling factor

5.2.596 dy (gdc1_dy)—Offset 50038h

Scaling only: Vertical scaling factor

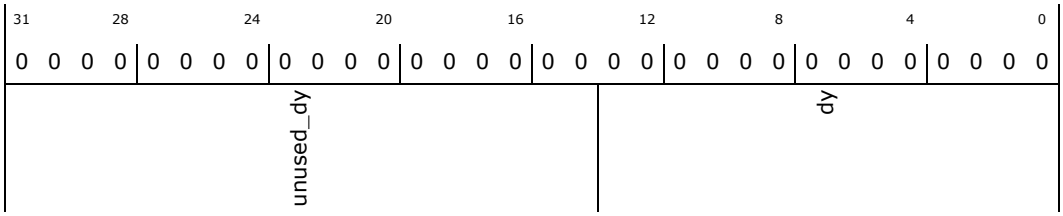
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RW	**Reserved (unused_dy):** Unused
13:0	0x0 RW	**dy:** Scaling only: Vertical scaling factor

5.2.597 P0_primX_ixdim (gdc1_P0_primX_ixdim)—Offset 5003Ch

P0(X) Tetragon mode: top-left coordinate (X), Scaling mode: dimension of the input region (X), fixed point notation, 13.10

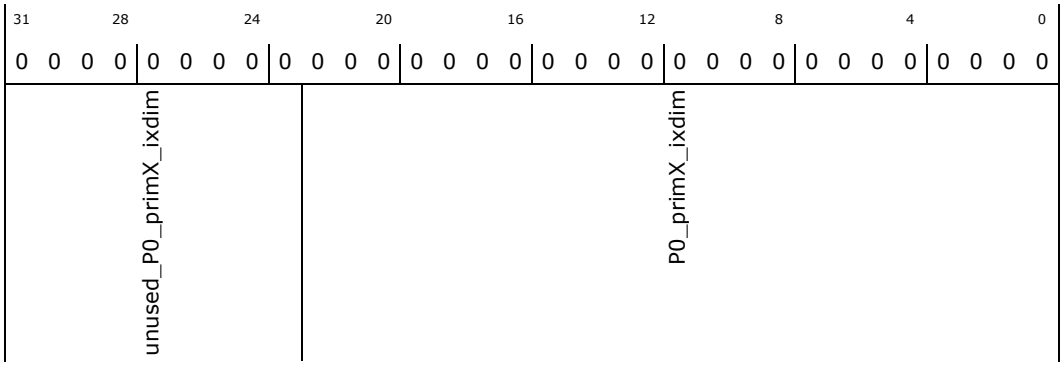
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 5003Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:23	0x0 RW	**Reserved (unused_P0_primX_ixdim):** Unused
22:0	0x0 RW	**P0_primX_ixdim:** P0(X) Tetragon mode: top-left coordinate (X), Scaling mode: dimension of the input region (X), fixed point notation, 13.10

5.2.598 P0_primY_iydim (gdc1_P0_primY_iydim)—Offset 50040h

P0(Y) Tetragon mode: top-left coordinate (Y), Scaling mode: dimension of the input region (Y), fixed point notation, 12.10

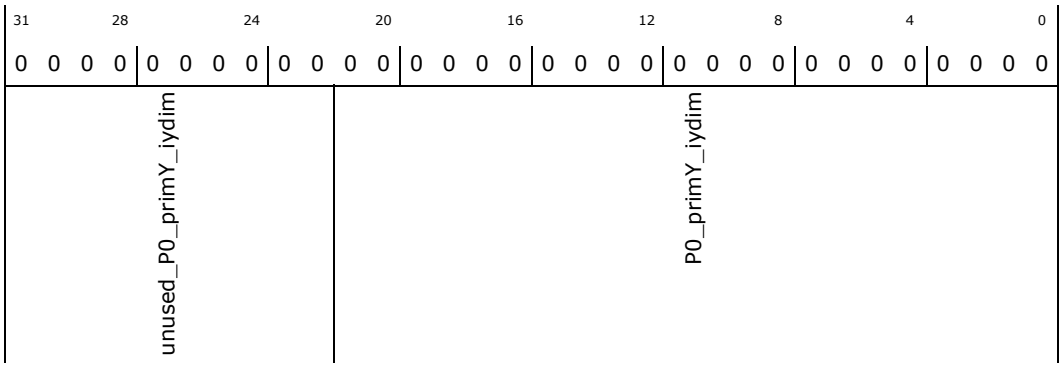
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50040h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:22	0x0 RW	**Reserved (unused_P0_primY_iydim):** Unused
21:0	0x0 RW	**P0_primY_iydim:** P0(Y) Tetragon mode: top-left coordinate (Y), Scaling mode: dimension of the input region (Y), fixed point notation, 12.10

5.2.599 P1_primX (gdc1_P1_primX)—Offset 50044h

P1(X) Tetragon mode only: top-right coordinate (X), fixed point notation, 13.10

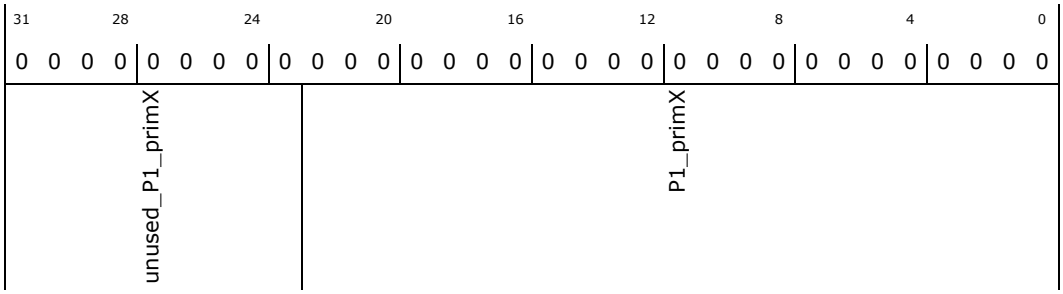
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50044h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:23	0x0 RW	**Reserved (unused_P1_primX):** Unused
22:0	0x0 RW	**P1_primX:** P1(X) Tetragon mode only: top-right coordinate (X), fixed point notation, 13.10

5.2.600 P1_primY (gdc1_P1_primY)—Offset 50048h

P1(Y) Tetragon mode only: top-right coordinate (Y), fixed point notation, 12.10

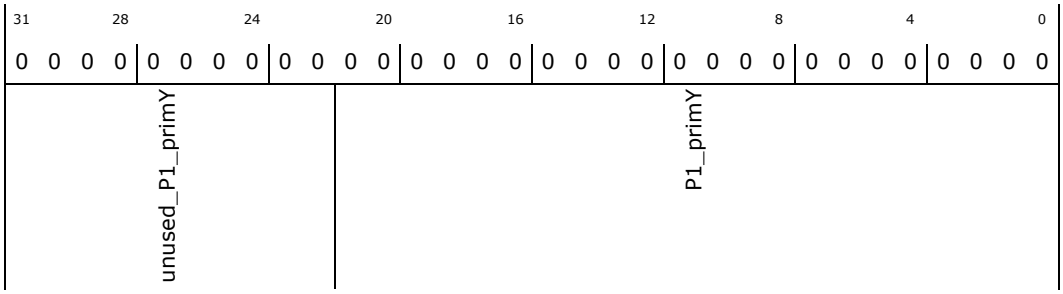
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50048h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:22	0x0 RW	**Reserved (unused_P1_primY):** Unused

Bit Range	Default and Access	Field Name (ID): Description
21:0	0x0 RW	**P1_primY:** P1(Y) Tetragon mode only: top-right coordinate (Y), fixed point notation, 12.10

5.2.601 P2_primX (gdc1_P2_primX)—Offset 5004Ch

P2(X) Tetragon mode only: bottom-left coordinate (X), fixed point notation, 13.10

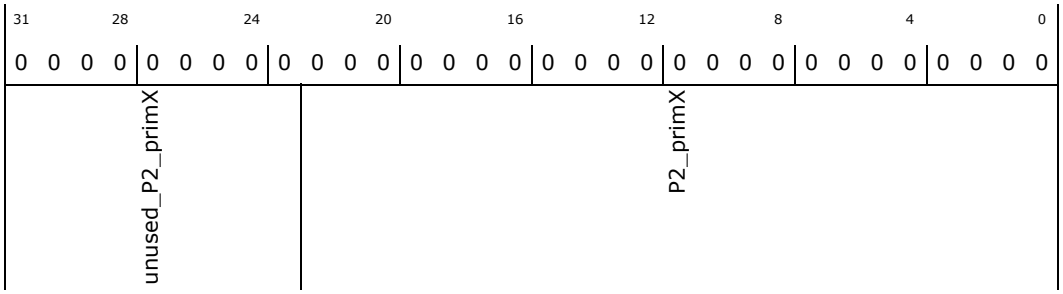
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 5004Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:23	0x0 RW	**Reserved (unused_P2_primX):** Unused
22:0	0x0 RW	**P2_primX:** P2(X) Tetragon mode only: bottom-left coordinate (X), fixed point notation, 13.10

5.2.602 P2_primY (gdc1_P2_primY)—Offset 50050h

P2(Y) Tetragon mode only: bottom-left coordinate (Y), fixed point notation, 12.10

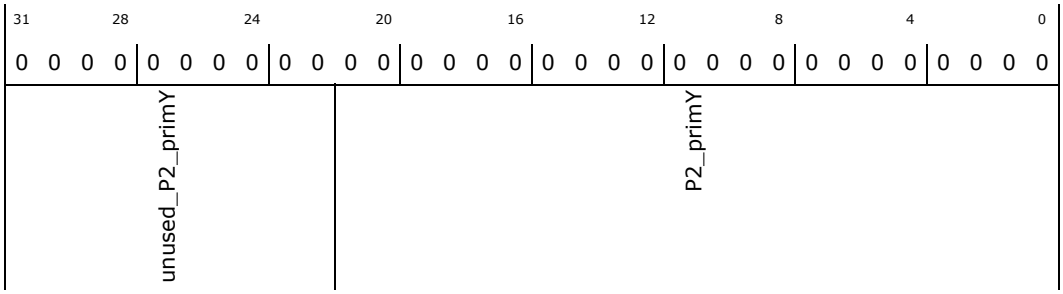
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50050h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:22	0x0 RW	**Reserved (unused_P2_primY):** Unused
21:0	0x0 RW	**P2_primY:** P2(Y) Tetragon mode only: bottom-left coordinate (Y), fixed point notation, 12.10

5.2.603 P3_primX (gdc1_P3_primX)—Offset 50054h

P3(X) Tetragon mode only: bottom-right coordinate (X), fixed point notation, 13.10

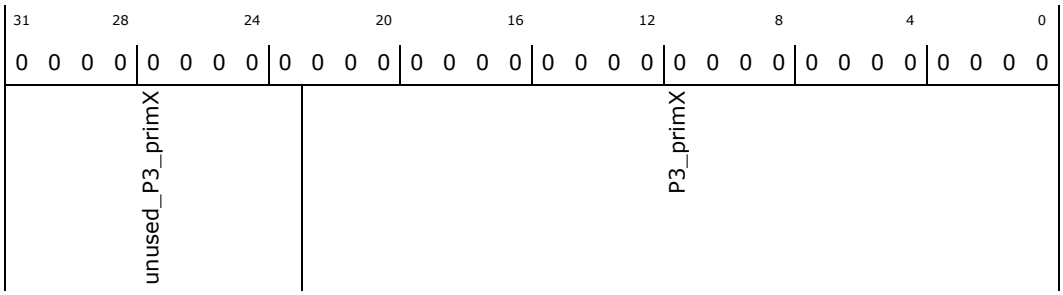
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50054h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:23	0x0 RW	**Reserved (unused_P3_primX):** Unused
22:0	0x0 RW	**P3_primX:** P3(X) Tetragon mode only: bottom-right coordinate (X), fixed point notation, 13.10

5.2.604 P3_primY (gdc1_P3_primY)—Offset 50058h

P3(Y) Tetragon mode only: bottom-right coordinate (Y), fixed point notation, 12.10

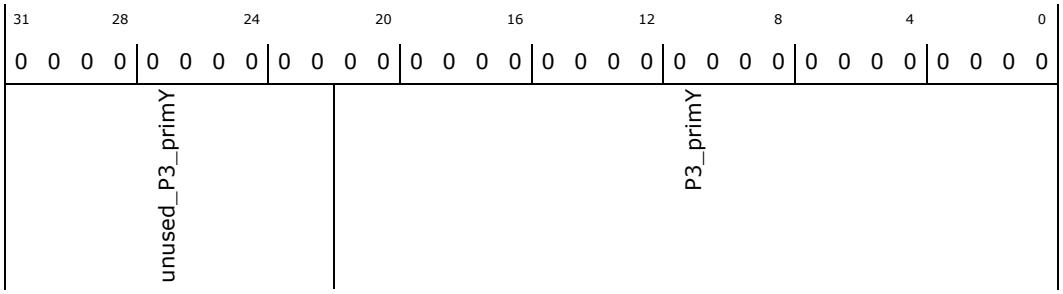
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50058h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:22	0x0 RW	**Reserved (unused_P3_primY):** Unused
21:0	0x0 RW	**P3_primY:** P3(Y) Tetragon mode only: bottom-right coordinate (Y), fixed point notation, 12.10

5.2.605 perf_mode (gdc1_perf_mode)—Offset 5005Ch

Number and location of pixels produced per clock cycle: 00=1x1 pixels; 01=2x1 pixels; 10=1x2 pixels; 11=2x2 pixels

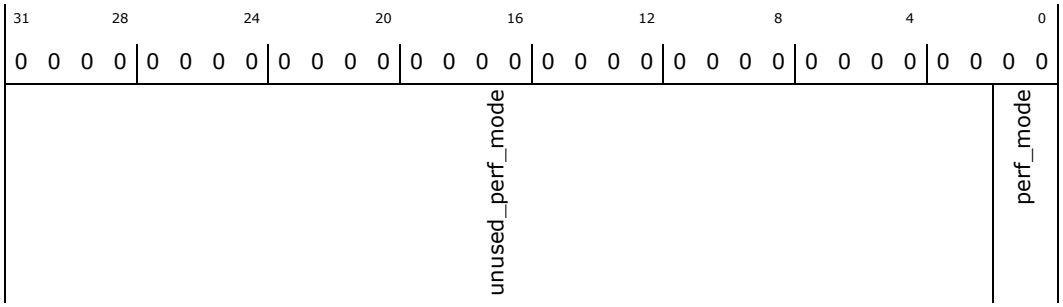
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 5005Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_perf_mode):** Unused
1:0	0x0 RW	**perf_mode:** Number and location of pixels produced per clock cycle: 00=1x1 pixels; 01=2x1 pixels; 10=1x2 pixels; 11=2x2 pixels

5.2.606 interp_type (gdc1_interp_type)—Offset 50060h

Type of interpolation: 00=NND; 01=BLI; 10=BCI; 11=

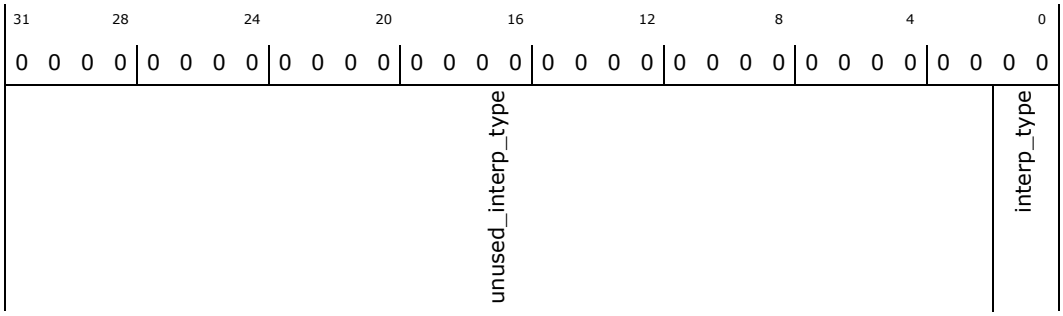
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50060h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_interp_type):** Unused
1:0	0x0 RW	**interp_type:** Type of interpolation: 00=NND; 01=BLI; 10=BCI; 11=

5.2.607 scan_mode (gdc1_scan_mode)—Offset 50064h

Scanning mode: 0 = STB (Slide To Bottom); 1 = STR (Slide To Right)

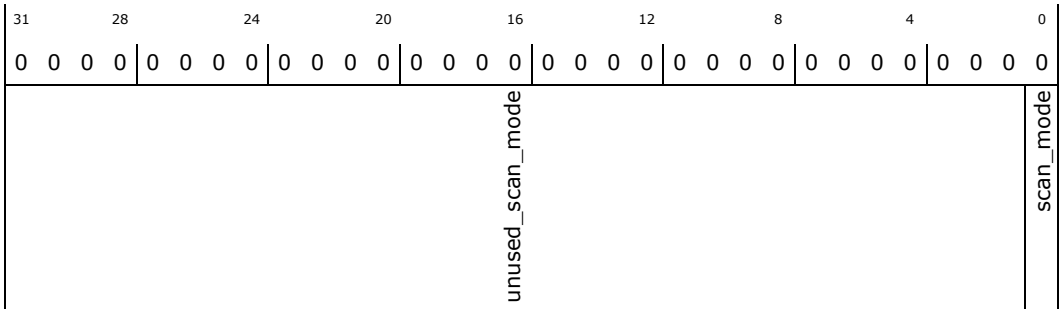
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50064h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_scan_mode):** Unused
0	0x0 RW	**scan_mode:** Scanning mode: 0 = STB (Slide To Bottom); 1 = STR (Slide To Right)

5.2.608 proc_mode (gdc1_proc_mode)—Offset 50068h

Processing mode: 0 = Rectangular-based scaling; 1 = Tetragon-based scaling

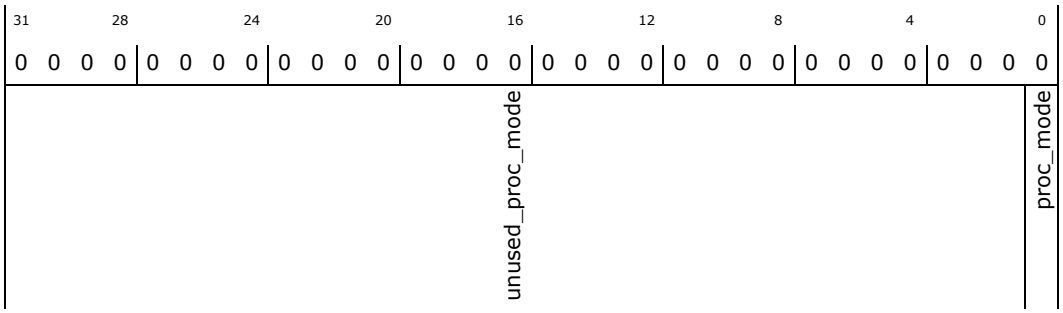
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 50068h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_proc_mode):** Unused
0	0x0 RW	**proc_mode:** Processing mode: 0 = Rectangular-based scaling; 1 = Tetragon-based scaling

5.2.609 reg0 (gdc2_reg0)—Offset 60000h

Status register: Current opx, opy, top-level FSM state

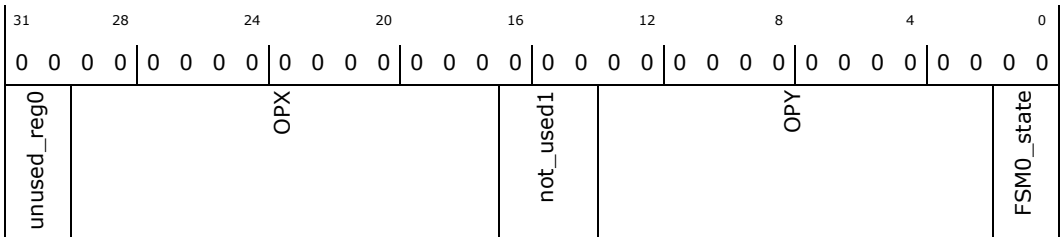
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved (unused_reg0):** Unused
29:17	0x0 RO	**OPX:** OPX value
16:14	0x0 RO	**not_used1:** N/A
13:2	0x0 RO	**OPY:** OPY value
1:0	0x0 RO	**FSM0_state:** FSM0 state: 00=Idle; 01=Busy-receiving data needed to kick the device; 10=Busy-wait state; 11=Busy-run state

5.2.610 woi_x (gdc2_woi_x)—Offset 60004h

Configured X dimension of the internal window-of-interest (local memory)

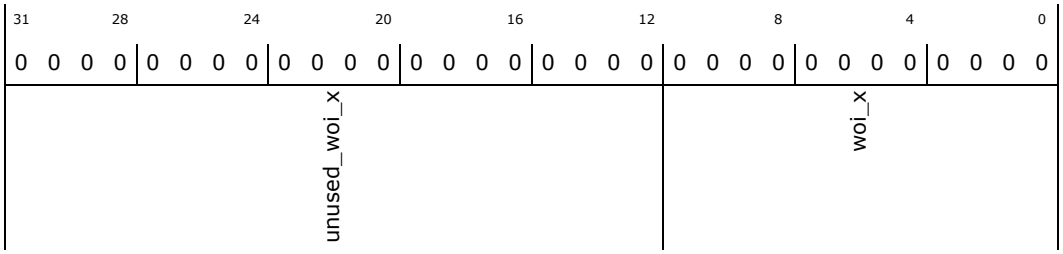
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_woi_x):** Unused
11:0	0x0 RO	**woi_x:** Configured X dimension of the internal window-of-interest (local memory)

5.2.611 woi_y (gdc2_woi_y)—Offset 60008h

Configured Y dimension of the internal window-of-interest (local memory)

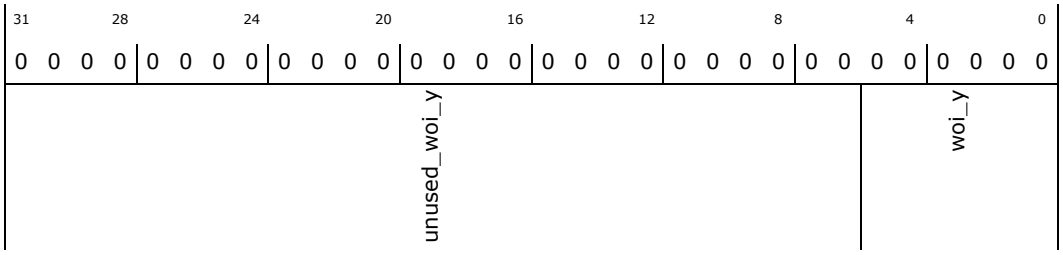
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**Reserved (unused_woi_y):** Unused
5:0	0x0 RO	**woi_y:** Configured Y dimension of the internal window-of-interest (local memory)

5.2.612 bpp (gdc2_bpp)—Offset 6000Ch

Bits per input/output pixel, allowed: 8, 10, 12, 14

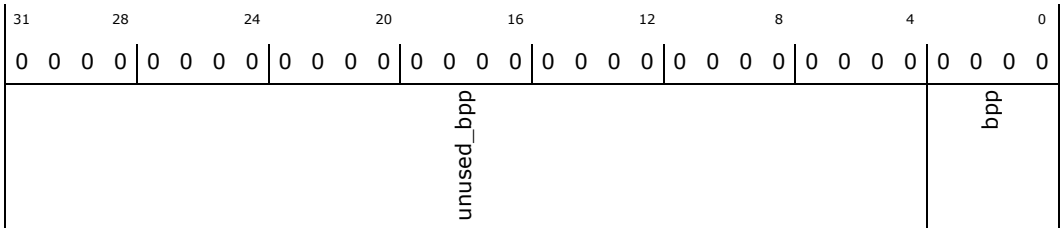
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 6000Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RW	**Reserved (unused_bpp):** Unused
3:0	0x0 RW	**bpp:** Bits per input/output pixel, allowed: 8, 10, 12, 14

5.2.613 fryipxfrx_start (gdc2_fryipxfrx_start)—Offset 60010h

Fractional component of the starting X and Y position for scaling given in fixed point notation

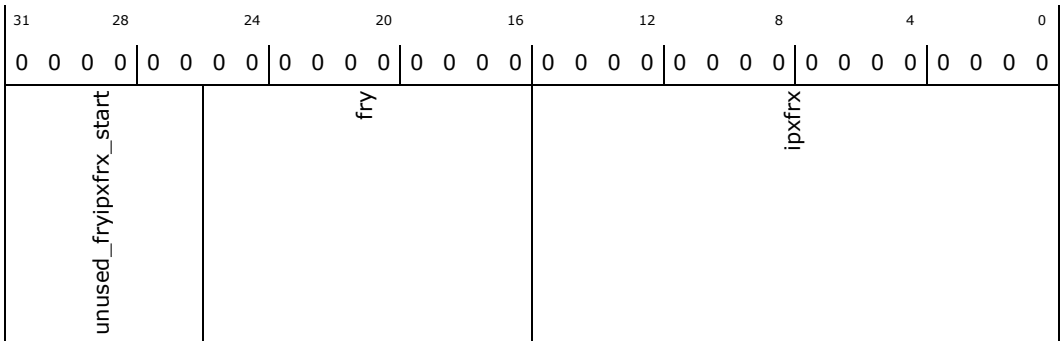
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:26	0x0 RO	**Reserved (unused_fryipxfrx_start):** Unused
25:16	0x0 RW	**fry:** Fractional component of the Y start
15:0	0x0 RW	**ipxfrx:** Integer (6) and Fractional (10) component of the X start

5.2.614 oxdim (gdc2_oxdim)—Offset 60014h

Output X dimension of the produced block of pixels

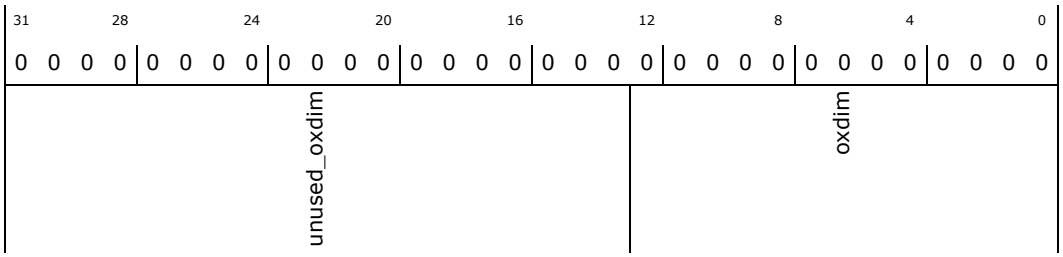
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:13	0x0 RW	**Reserved (unused_oxdim):** Unused
12:0	0x0 RW	**oxdim:** Output X dimension of the produced block of pixels

5.2.615 oydim (gdc2_oydim)—Offset 60018h

Output Y dimension of the produced block of pixels

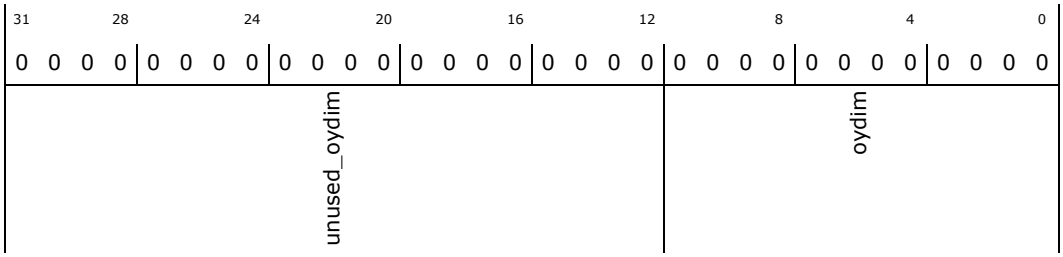
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_oydim):** Unused
11:0	0x0 RW	**oydim:** Output Y dimension of the produced block of pixels

5.2.616 src_addr (gdc2_src_addr)—Offset 6001Ch

Source (input) pixel base address [byte-based]

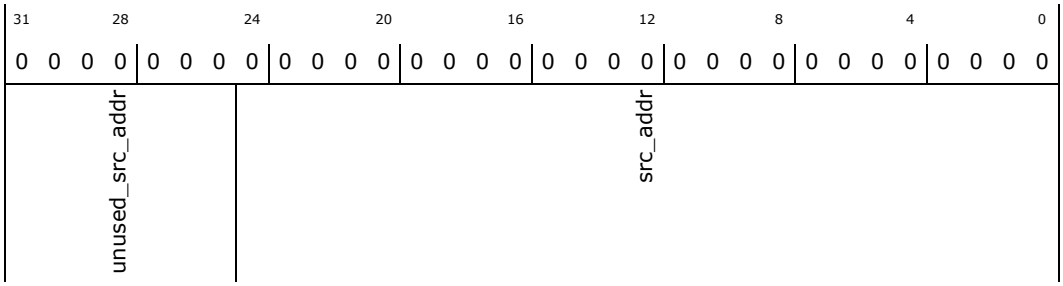
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 6001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:25	0x0 RW	**Reserved (unused_src_addr):** Unused
24:0	0x0 RW	**src_addr:** Source (input) pixel base address [byte-based]

5.2.617 src_end (gdc2_src_end)—Offset 60020h

End address. When reached wrap around. [byte-based]

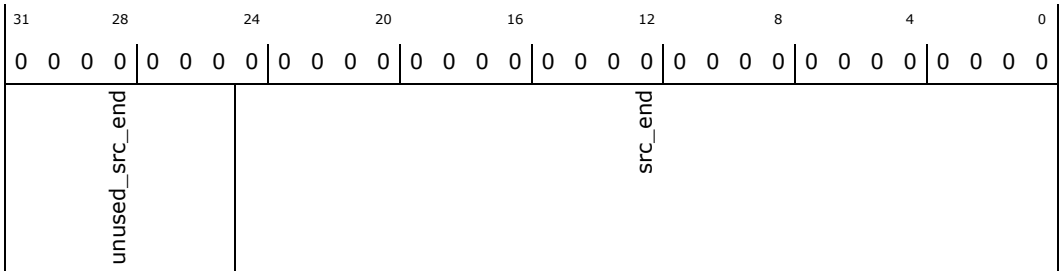
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:25	0x0 RW	**Reserved (unused_src_end):** Unused
24:0	0x0 RW	**src_end:** End address. When reached wrap around. [byte-based]

5.2.618 src_wrap (gdc2_src_wrap)—Offset 60024h

Wrap addr. Wrap here when src_end reached [byte-based]

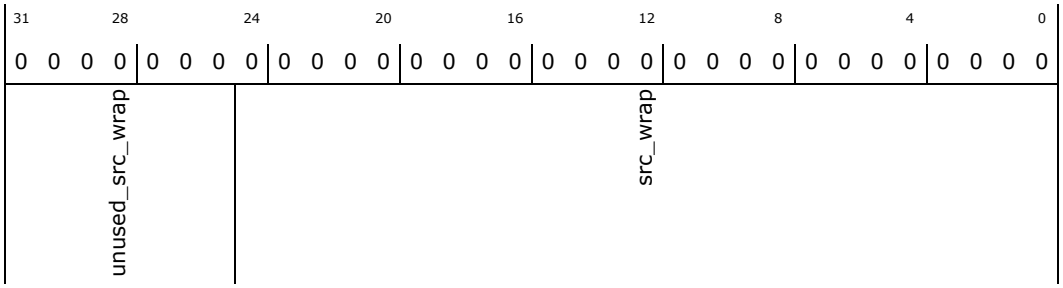
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:25	0x0 RW	**Reserved (unused_src_wrap):** Unused

Bit Range	Default and Access	Field Name (ID): Description
24:0	0x0 RW	**src_wrap:** Wrap addr. Wrap here when src_end reached [byte-based]

5.2.619 src_stride (gdc2_src_stride)—Offset 60028h

Source (input) pixel stride [byte-based]

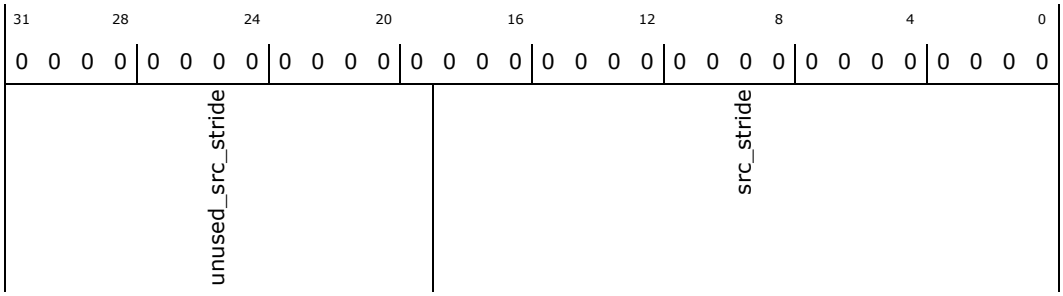
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:19	0x0 RW	**Reserved (unused_src_stride):** Unused
18:0	0x0 RW	**src_stride:** Source (input) pixel stride [byte-based]

5.2.620 dst_addr (gdc2_dst_addr)—Offset 6002Ch

Destination (output) pixel base address [byte-based]

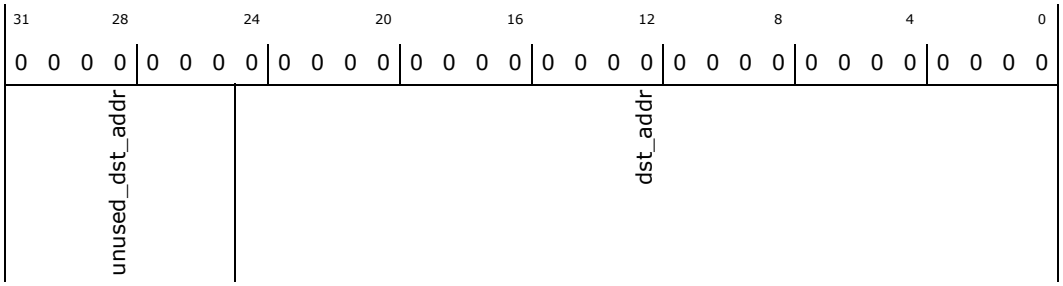
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 6002Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:25	0x0 RW	**Reserved (unused_dst_addr):** Unused
24:0	0x0 RW	**dst_addr:** Destination (output) pixel base address [byte-based]

5.2.621 dst_stride (gdc2_dst_stride)—Offset 60030h

Destination (output) pixel stride [byte-based]

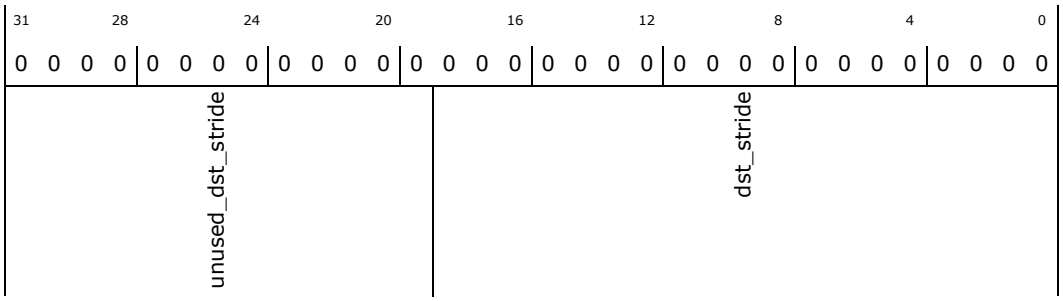
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:19	0x0 RW	**Reserved (unused_dst_stride):** Unused
18:0	0x0 RW	**dst_stride:** Destination (output) pixel stride [byte-based]

5.2.622 dx (gdc2_dx)—Offset 60034h

Scaling only: Horizontal scaling factor

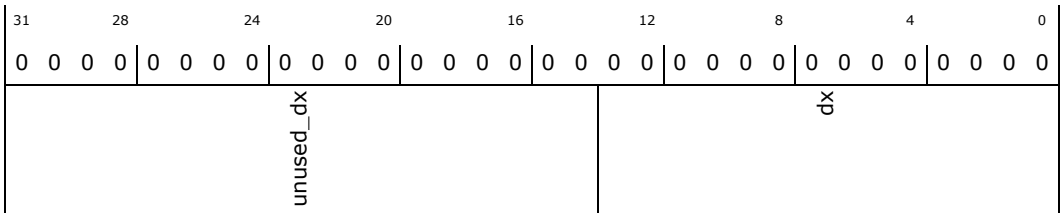
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RW	**Reserved (unused_dx):** Unused
13:0	0x0 RW	**dx:** Scaling only: Horizontal scaling factor

5.2.623 dy (gdc2_dy)—Offset 60038h

Scaling only: Vertical scaling factor

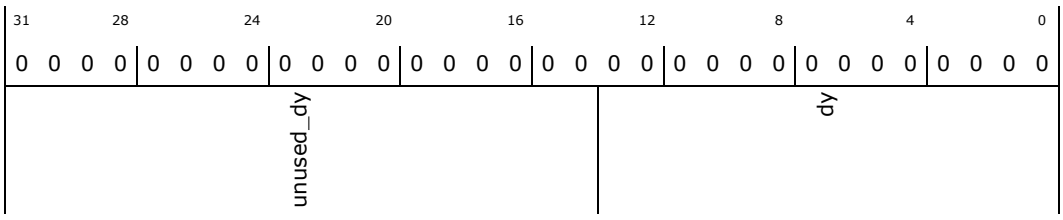
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RW	**Reserved (unused_dy):** Unused

Bit Range	Default and Access	Field Name (ID): Description
13:0	0x0 RW	**dy:** Scaling only: Vertical scaling factor

5.2.624 P0_primX_ixdim (gdc2_P0_primX_ixdim)—Offset 6003Ch

P0(X) Tetragon mode: top-left coordinate (X), Scaling mode: dimension of the input region (X), fixed point notation, 13.10

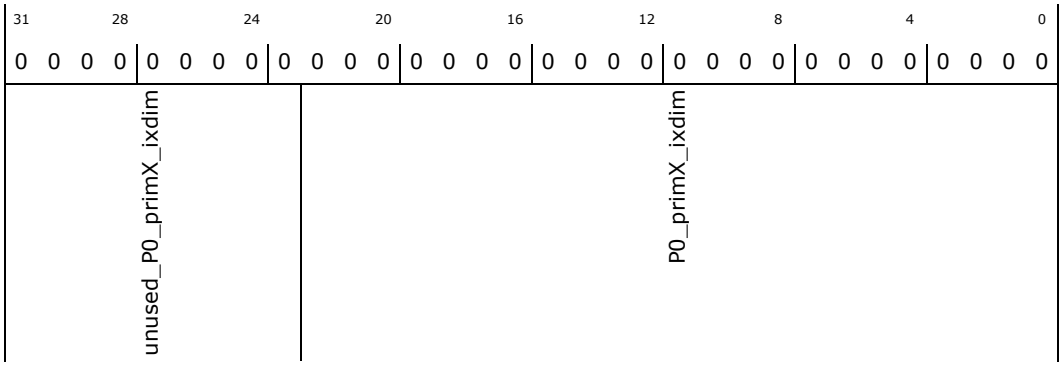
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 6003Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:23	0x0 RW	**Reserved (unused_P0_primX_ixdim):** Unused
22:0	0x0 RW	**P0_primX_ixdim:** P0(X) Tetragon mode: top-left coordinate (X), Scaling mode: dimension of the input region (X), fixed point notation, 13.10

5.2.625 P0_primY_iydim (gdc2_P0_primY_iydim)—Offset 60040h

P0(Y) Tetragon mode: top-left coordinate (Y), Scaling mode: dimension of the input region (Y), fixed point notation, 12.10

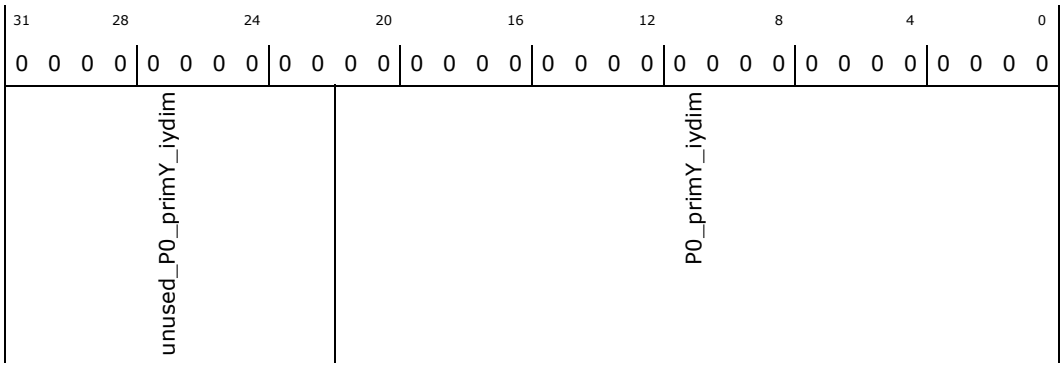
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60040h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:22	0x0 RW	**Reserved (unused_P0_primY_iydim):** Unused
21:0	0x0 RW	**P0_primY_iydim:** P0(Y) Tetragon mode: top-left coordinate (Y), Scaling mode: dimension of the input region (Y), fixed point notation, 12.10

5.2.626 P1_primX (gdc2_P1_primX)—Offset 60044h

P1(X) Tetragon mode only: top-right coordinate (X), fixed point notation, 13.10

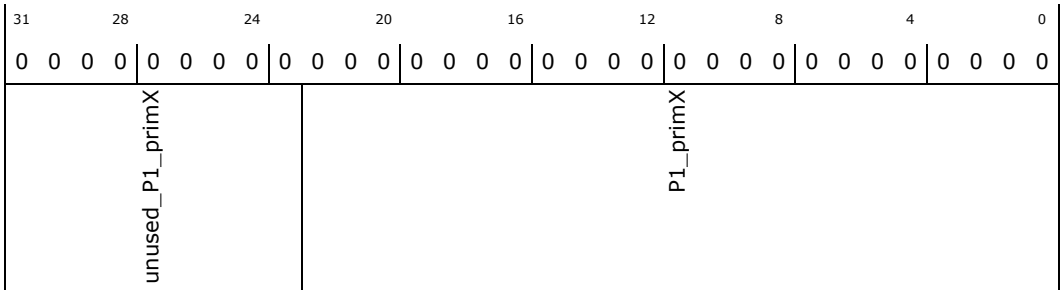
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60044h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:23	0x0 RW	**Reserved (unused_P1_primX):** Unused
22:0	0x0 RW	**P1_primX:** P1(X) Tetragon mode only: top-right coordinate (X), fixed point notation, 13.10

5.2.627 P1_primY (gdc2_P1_primY)—Offset 60048h

P1(Y) Tetragon mode only: top-right coordinate (Y), fixed point notation, 12.10

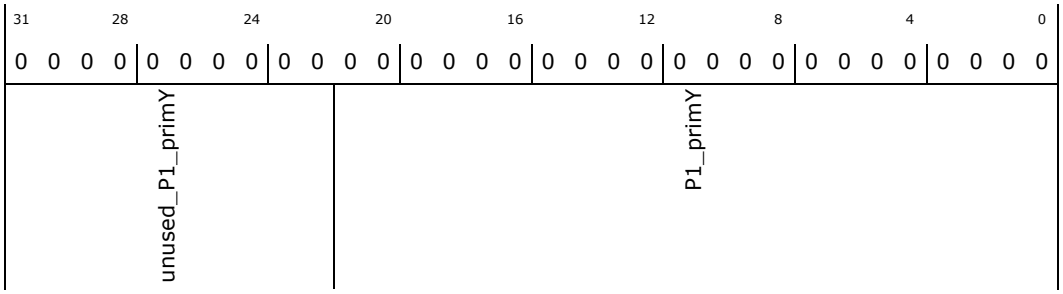
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60048h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:22	0x0 RW	**Reserved (unused_P1_primY):** Unused
21:0	0x0 RW	**P1_primY:** P1(Y) Tetragon mode only: top-right coordinate (Y), fixed point notation, 12.10

5.2.628 P2_primX (gdc2_P2_primX)—Offset 6004Ch

P2(X) Tetragon mode only: bottom-left coordinate (X), fixed point notation, 13.10

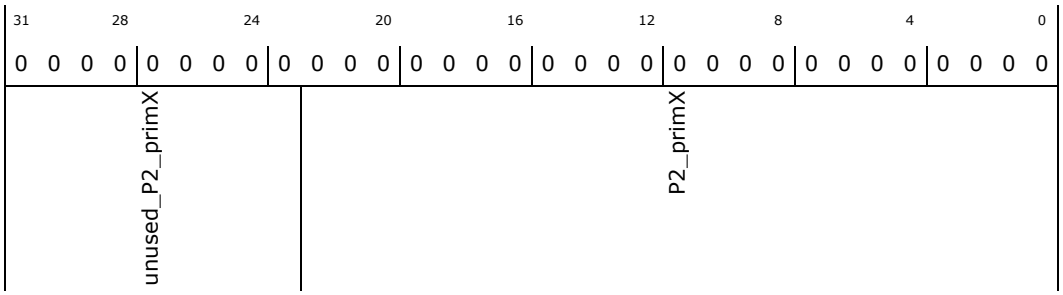
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 6004Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:23	0x0 RW	**Reserved (unused_P2_primX):** Unused
22:0	0x0 RW	**P2_primX:** P2(X) Tetragon mode only: bottom-left coordinate (X), fixed point notation, 13.10

5.2.629 P2_primY (gdc2_P2_primY)—Offset 60050h

P2(Y) Tetragon mode only: bottom-left coordinate (Y), fixed point notation, 12.10

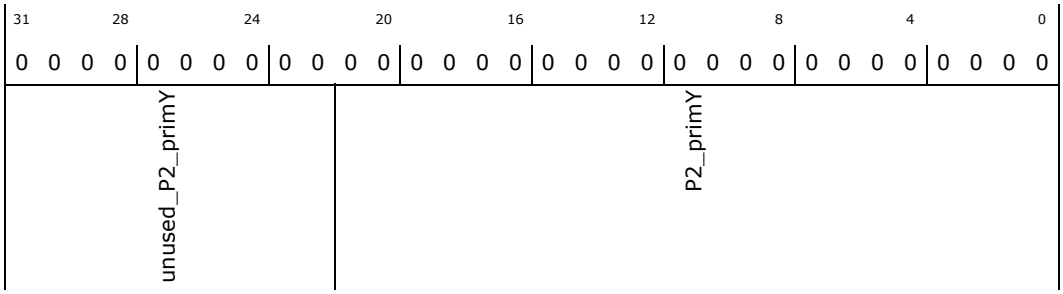
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60050h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:22	0x0 RW	**Reserved (unused_P2_primY):** Unused
21:0	0x0 RW	**P2_primY:** P2(Y) Tetragon mode only: bottom-left coordinate (Y), fixed point notation, 12.10

5.2.630 P3_primX (gdc2_P3_primX)—Offset 60054h

P3(X) Tetragon mode only: bottom-right coordinate (X), fixed point notation, 13.10

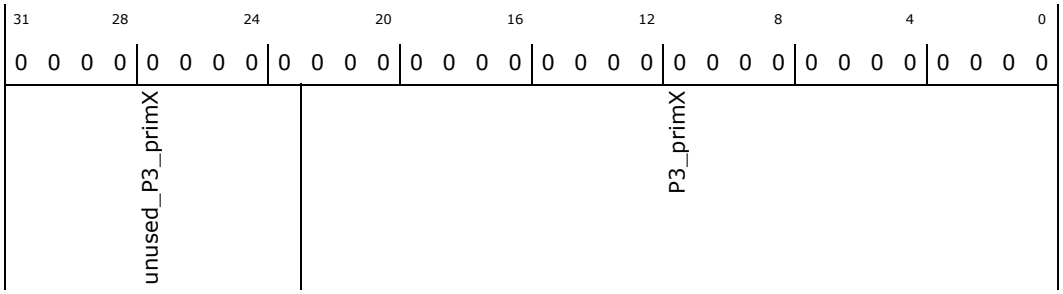
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60054h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:23	0x0 RW	**Reserved (unused_P3_primX):** Unused
22:0	0x0 RW	**P3_primX:** P3(X) Tetragon mode only: bottom-right coordinate (X), fixed point notation, 13.10

5.2.631 P3_primY (gdc2_P3_primY)—Offset 60058h

P3(Y) Tetragon mode only: bottom-right coordinate (Y), fixed point notation, 12.10

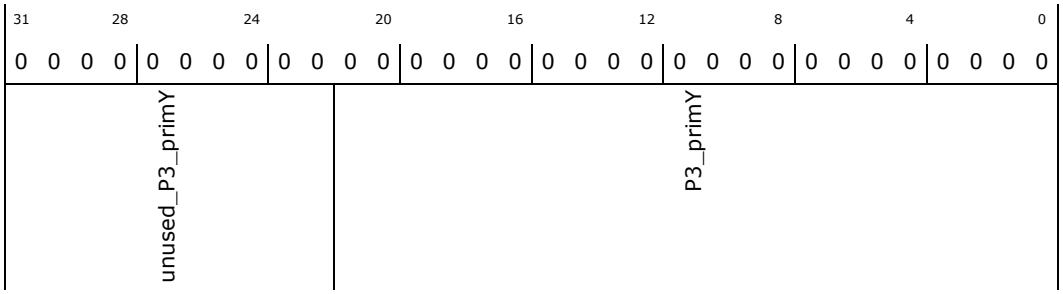
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60058h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:22	0x0 RW	**Reserved (unused_P3_primY):** Unused
21:0	0x0 RW	**P3_primY:** P3(Y) Tetragon mode only: bottom-right coordinate (Y), fixed point notation, 12.10

5.2.632 perf_mode (gdc2_perf_mode)—Offset 6005Ch

Number and location of pixels produced per clock cycle: 00=1x1 pixels; 01=2x1 pixels; 10=1x2 pixels; 11=2x2 pixels

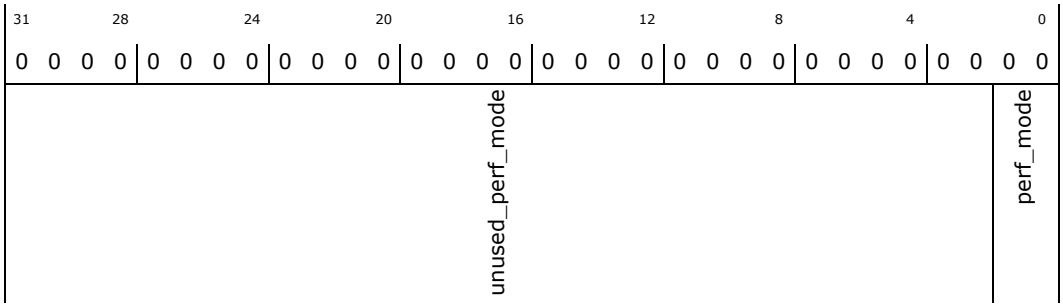
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 6005Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_perf_mode):** Unused
1:0	0x0 RW	**perf_mode:** Number and location of pixels produced per clock cycle: 00=1x1 pixels; 01=2x1 pixels; 10=1x2 pixels; 11=2x2 pixels

5.2.633 interp_type (gdc2_interp_type)—Offset 60060h

Type of interpolation: 00=NND; 01=BLI; 10=BCI; 11=LUT

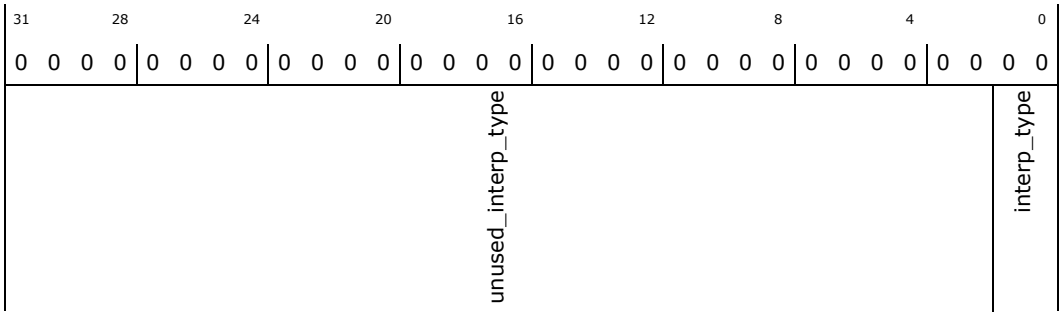
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60060h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_interp_type):** Unused
1:0	0x0 RW	**interp_type:** Type of interpolation: 00=NND; 01=BLI; 10=BCI; 11=LUT

5.2.634 scan_mode (gdc2_scan_mode)—Offset 60064h

Scanning mode: 0 = STB (Slide To Bottom); 1 = STR (Slide To Right)

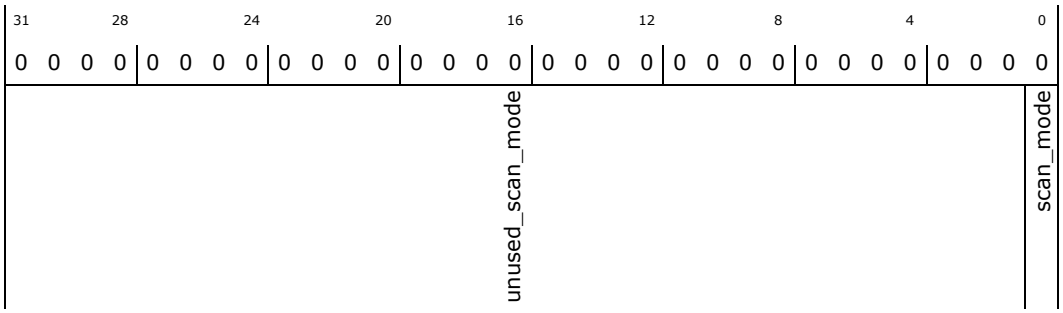
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60064h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_scan_mode):** Unused
0	0x0 RW	**scan_mode:** Scanning mode: 0 = STB (Slide To Bottom); 1 = STR (Slide To Right)

5.2.635 proc_mode (gdc2_proc_mode)—Offset 60068h

Processing mode: 0 = Rectangular-based scaling; 1 = Tetragon-based scaling

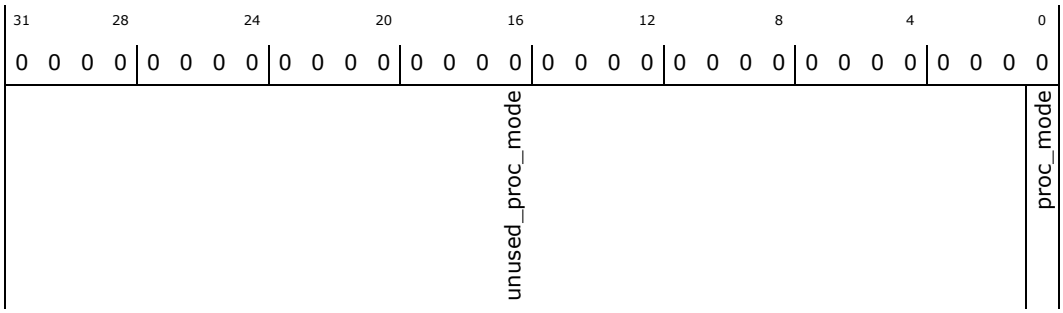
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 60068h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_proc_mode):** Unused
0	0x0 RW	**proc_mode:** Processing mode: 0 = Rectangular-based scaling; 1 = Tetragon-based scaling

5.2.636 MMU_invalidate_cache (data_out_sys_c_mmu_MMU_invalidate_cache)—Offset 70000h

MMU invalidate cache. When '1', the MMUs TLB is invalidated.

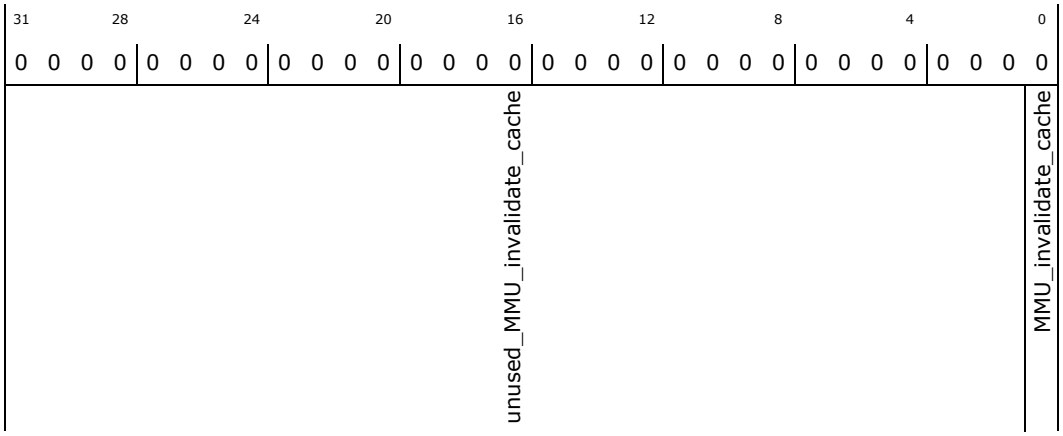
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 70000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_MMU_invalidate_cache):** Unused
0	0x0 WO	**MMU_invalidate_cache:** MMU invalidate cache. When '1', the MMUs TLB is invalidated.

5.2.637 MMU_page_table_base (data_out_sys_c_mmu_MMU_page_table_base)—Offset 70004h

Defines the physical page number of the page tables

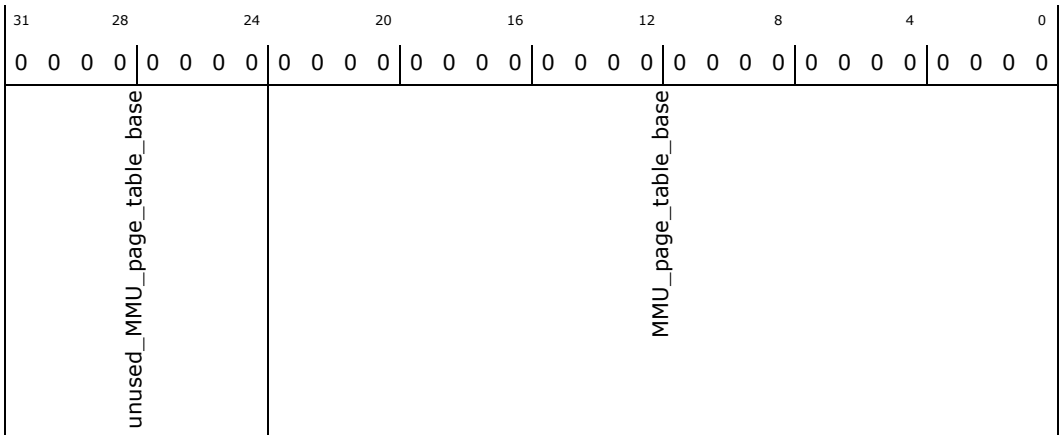
Access Method

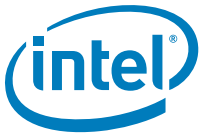
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 70004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h





Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved (unused_MMU_page_table_base):** Unused
23:0	0x0 RW	**MMU_page_table_base:** Defines the physical page number of the page tables

5.3 Image Signal Processor Memory Mapped I/O Registers

Table 28. Summary of Memory Mapped I/O Registers—ISPMMADR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
80100–80103h	4	"csi1_dev_ready (is_2400_inp_sys_csi_receiver_csi1_dev_ready)—Offset 80100h" on page 1620	00000000h
80104–80107h	4	"csi1_int_status (is_2400_inp_sys_csi_receiver_csi1_int_status)—Offset 80104h" on page 1621	00000000h
80108–8010Bh	4	"csi1_int_enable (is_2400_inp_sys_csi_receiver_csi1_int_enable)—Offset 80108h" on page 1622	00000000h
8010C–8010Fh	4	"csi1_func_prg (is_2400_inp_sys_csi_receiver_csi1_func_prg)—Offset 8010Ch" on page 1623	0007FFFFh
80110–80113h	4	"csi1_init_cnt (is_2400_inp_sys_csi_receiver_csi1_init_cnt)—Offset 80110h" on page 1624	00000000h
8011C–8011Fh	4	"csi_backend_fs_ls (is_2400_inp_sys_csi_receiver_csi_backend_fs_ls)—Offset 8011Ch" on page 1625	00000002h
80120–80123h	4	"csi_backend_ls_dvalid (is_2400_inp_sys_csi_receiver_csi_backend_ls_dvalid)—Offset 80120h" on page 1625	00000002h
80124–80127h	4	"csi_backend_dvalid_le (is_2400_inp_sys_csi_receiver_csi_backend_dvalid_le)—Offset 80124h" on page 1626	00000002h
80128–8012Bh	4	"csi_backend_le_fe (is_2400_inp_sys_csi_receiver_csi_backend_le_fe)—Offset 80128h" on page 1627	00000002h
8012C–8012Fh	4	"csi_backend_fe_fs (is_2400_inp_sys_csi_receiver_csi_backend_fe_fs)—Offset 8012Ch" on page 1628	00000002h

Table 28. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
80130–80133h	4	"csi_backend_le_ls (is_2400_inp_sys_csi_receiver_csi_backend_le_ls)—Offset 80130h" on page 1628	00000004h
80134–80137h	4	"csi_backend_two_pixel_en (is_2400_inp_sys_csi_receiver_csi_backend_two_pixel_en)—Offset 80134h" on page 1629	00000000h
80138–8013Bh	4	"csi1_raw16_18_data_id (is_2400_inp_sys_csi_receiver_csi1_raw16_18_data_id)—Offset 80138h" on page 1630	00000000h
8013C–8013Fh	4	"csi1_sync_cnt (is_2400_inp_sys_csi_receiver_csi1_sync_cnt)—Offset 8013Ch" on page 1631	FFFFFFFFh
80140–80143h	4	"csi1_rx_cnt (is_2400_inp_sys_csi_receiver_csi1_rx_cnt)—Offset 80140h" on page 1632	FFFFFFFFh
80144–80147h	4	"csi_backend_rst (is_2400_inp_sys_csi_receiver_csi_backend_rst)—Offset 80144h" on page 1633	00000000h
80148–8014Bh	4	"csi_backend_comp_pred_reg0_vc0 (is_2400_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc0)—Offset 80148h" on page 1634	00000000h
8014C–8014Fh	4	"csi_backend_comp_reg1_vc0 (is_2400_inp_sys_csi_receiver_csi_backend_comp_reg1_vc0)—Offset 8014Ch" on page 1635	00000000h
80150–80153h	4	"csi_backend_comp_pred_reg0_vc1 (is_2400_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc1)—Offset 80150h" on page 1636	00000000h
80154–80157h	4	"csi_backend_comp_reg1_vc1 (is_2400_inp_sys_csi_receiver_csi_backend_comp_reg1_vc1)—Offset 80154h" on page 1638	00000000h
80158–8015Bh	4	"csi_backend_comp_pred_reg0_vc2 (is_2400_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc2)—Offset 80158h" on page 1639	00000000h
8015C–8015Fh	4	"csi_backend_comp_reg1_vc2 (is_2400_inp_sys_csi_receiver_csi_backend_comp_reg1_vc2)—Offset 8015Ch" on page 1640	00000000h
80160–80163h	4	"csi_backend_comp_pred_reg0_vc3 (is_2400_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc3)—Offset 80160h" on page 1641	00000000h
80164–80167h	4	"csi_backend_comp_reg1_vc3 (is_2400_inp_sys_csi_receiver_csi_backend_comp_reg1_vc3)—Offset 80164h" on page 1643	00000000h
80168–8016Bh	4	"csi_backend_raw18_reg (is_2400_inp_sys_csi_receiver_csi_backend_raw18_reg)—Offset 80168h" on page 1644	00000000h

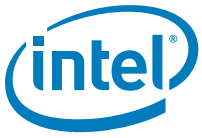


Table 28. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8016C–8016Fh	4	"csi_backend_force_raw8_reg (is_2400_inp_sys_csi_receiver_csi_backend_force_raw8_reg)—Offset 8016Ch" on page 1645	00000000h
80170–80173h	4	"csi_backend_raw16_reg (is_2400_inp_sys_csi_receiver_csi_backend_raw16_reg)—Offset 80170h" on page 1645	00000000h
80200–80203h	4	"csi2_dev_ready (is_2400_inp_sys_csi_receiver_csi2_dev_ready)—Offset 80200h" on page 1646	00000000h
80204–80207h	4	"csi2_int_status (is_2400_inp_sys_csi_receiver_csi2_int_status)—Offset 80204h" on page 1647	00000000h
80208–8020Bh	4	"csi2_int_enable (is_2400_inp_sys_csi_receiver_csi2_int_enable)—Offset 80208h" on page 1649	00000000h
8020C–8020Fh	4	"csi2_func_prg (is_2400_inp_sys_csi_receiver_csi2_func_prg)—Offset 8020Ch" on page 1650	0007FFFFh
80210–80213h	4	"csi2_init_cnt (is_2400_inp_sys_csi_receiver_csi2_init_cnt)—Offset 80210h" on page 1651	00000000h
80238–8023Bh	4	"csi2_raw16_18_data_id (is_2400_inp_sys_csi_receiver_csi2_raw16_18_data_id)—Offset 80238h" on page 1652	00000000h
8023C–8023Fh	4	"csi2_sync_cnt (is_2400_inp_sys_csi_receiver_csi2_sync_cnt)—Offset 8023Ch" on page 1653	000000FFh
80240–80243h	4	"csi2_rx_cnt (is_2400_inp_sys_csi_receiver_csi2_rx_cnt)—Offset 80240h" on page 1653	000000FFh
80300–80303h	4	"csi3_dev_ready (is_2400_inp_sys_csi_receiver_csi3_dev_ready)—Offset 80300h" on page 1654	00000000h
80304–80307h	4	"csi3_int_status (is_2400_inp_sys_csi_receiver_csi3_int_status)—Offset 80304h" on page 1655	00000000h
80308–8030Bh	4	"csi3_int_enable (is_2400_inp_sys_csi_receiver_csi3_int_enable)—Offset 80308h" on page 1656	00000000h
8030C–8030Fh	4	"csi3_func_prg (is_2400_inp_sys_csi_receiver_csi3_func_prg)—Offset 8030Ch" on page 1658	0007FFFFh
80310–80313h	4	"csi3_init_cnt (is_2400_inp_sys_csi_receiver_csi3_init_cnt)—Offset 80310h" on page 1659	00000000h

Table 28. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
80338–8033Bh	4	"csi3_raw16_18_data_id (is_2400_inp_sys_csi_receiver_csi3_raw16_18_data_id)—Offset 80338h" on page 1659	00000000h
8033C–8033Fh	4	"csi3_sync_cnt (is_2400_inp_sys_csi_receiver_csi3_sync_cnt)—Offset 8033Ch" on page 1660	0000FFFFh
80340–80343h	4	"csi3_rx_cnt (is_2400_inp_sys_csi_receiver_csi3_rx_cnt)—Offset 80340h" on page 1661	00000000h
80800–80803h	4	"csi_be_gen_sh_acc_ovl (is_2400_inp_sys_csi_receiver_csi_be_gen_sh_acc_ovl)—Offset 80800h" on page 1662	00000000h
80804–80807h	4	"csi_sh_be_srst (is_2400_inp_sys_csi_receiver_csi_sh_be_srst)—Offset 80804h" on page 1663	00000000h
80808–8080Bh	4	"csi_sh_be_two_ppc (is_2400_inp_sys_csi_receiver_csi_sh_be_two_ppc)—Offset 80808h" on page 1664	00000000h
8080C–8080Fh	4	"csi_sh_be_comp_reg_vc0 (is_2400_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc0)—Offset 8080Ch" on page 1664	00000000h
80810–80813h	4	"csi_sh_be_comp_reg_vc1 (is_2400_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc1)—Offset 80810h" on page 1666	00000000h
80814–80817h	4	"csi_sh_be_comp_reg_vc2 (is_2400_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc2)—Offset 80814h" on page 1667	00000000h
80818–8081Bh	4	"csi_sh_be_comp_reg_vc3 (is_2400_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc3)—Offset 80818h" on page 1669	00000000h
8081C–8081Fh	4	"csi_sh_be_sel_be (is_2400_inp_sys_csi_receiver_csi_sh_be_sel_be)—Offset 8081Ch" on page 1670	00000000h
80820–80823h	4	"csi_sh_be_raw16_reg (is_2400_inp_sys_csi_receiver_csi_sh_be_raw16_reg)—Offset 80820h" on page 1671	00000000h
80824–80827h	4	"csi_sh_be_raw18_reg (is_2400_inp_sys_csi_receiver_csi_sh_be_raw18_reg)—Offset 80824h" on page 1672	00000000h
80828–8082Bh	4	"csi_sh_be_force_raw8_reg (is_2400_inp_sys_csi_receiver_csi_sh_be_force_raw8_reg)—Offset 80828h" on page 1673	00000000h
8082C–8082Fh	4	"csi_sh_be_irq_stat_reg (is_2400_inp_sys_csi_receiver_csi_sh_be_irq_stat_reg)—Offset 8082Ch" on page 1673	00000000h

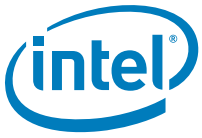


Table 28. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
80830–80833h	4	"csi_sh_be_irq_stat_clear_reg (is_2400_inp_sys_csi_receiver_csi_sh_be_irq_stat_clear_reg)—Offset 80830h" on page 1674	00000000h
80834–80837h	4	"csi_sh_be_custom_enable_reg (is_2400_inp_sys_csi_receiver_csi_sh_be_custom_enable_reg)—Offset 80834h" on page 1675	00000000h
81000–81003h	4	"reg_CaptStartMode (is_2400_inp_sys_capt_unit_a_reg_CaptStartMode)—Offset 81000h" on page 1676	00000000h
81004–81007h	4	"reg_Capt_Start_Addr (is_2400_inp_sys_capt_unit_a_reg_Capt_Start_Addr)—Offset 81004h" on page 1677	00000000h
81008–8100Bh	4	"reg_Capt_Mem_Region_Size (is_2400_inp_sys_capt_unit_a_reg_Capt_Mem_Region_Size)—Offset 81008h" on page 1678	00000080h
8100C–8100Fh	4	"reg_Capt_Num_Mem_Regions (is_2400_inp_sys_capt_unit_a_reg_Capt_Num_Mem_Regions)—Offset 8100Ch" on page 1679	00000003h
81010–81013h	4	"reg_Capt_Init (is_2400_inp_sys_capt_unit_a_reg_Capt_Init)—Offset 81010h" on page 1679	00000000h
81014–81017h	4	"reg_Capt_Start_Addr (is_2400_inp_sys_capt_unit_a_reg_Capt_Start_Addr)—Offset 81004h" on page 1677	00000000h
81018–8101Bh	4	"reg_Capt_Stop (is_2400_inp_sys_capt_unit_a_reg_Capt_Stop)—Offset 81018h" on page 1681	00000000h
8101C–8101Fh	4	"reg_Capt_Packet_Length (is_2400_inp_sys_capt_unit_a_reg_Capt_Packet_Length)—Offset 8101Ch" on page 1682	00000000h
81020–81023h	4	"reg_Capt_Received_Length (is_2400_inp_sys_capt_unit_a_reg_Capt_Received_Length)—Offset 81020h" on page 1682	00000000h
81024–81027h	4	"reg_Capt_Received_Short_Packets (is_2400_inp_sys_capt_unit_a_reg_Capt_Received_Short_Packets)—Offset 81024h" on page 1683	00000000h
81028–8102Bh	4	"reg_Capt_Received_Long_Packets (is_2400_inp_sys_capt_unit_a_reg_Capt_Received_Long_Packets)—Offset 81028h" on page 1684	00000000h
8102C–8102Fh	4	"reg_Capt_Last_Command (is_2400_inp_sys_capt_unit_a_reg_Capt_Last_Command)—Offset 8102Ch" on page 1685	0000000Fh
81030–81033h	4	"reg_Capt_Next_Command (is_2400_inp_sys_capt_unit_a_reg_Capt_Next_Command)—Offset 81030h" on page 1685	0000000Fh

Table 28. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
81034–81037h	4	"reg_Capt_Last_Acknowledge (is_2400_inp_sys_capt_unit_a_reg_Capt_Last_Acknowledge)—Offset 81034h" on page 1686	0000000Fh
81038–8103Bh	4	"reg_Capt_Next_Acknowledge (is_2400_inp_sys_capt_unit_a_reg_Capt_Next_Acknowledge)—Offset 81038h" on page 1687	0000000Fh
8103C–8103Fh	4	"reg_Capt_FSM_State_Info (is_2400_inp_sys_capt_unit_a_reg_Capt_FSM_State_Info)—Offset 8103Ch" on page 1687	00000000h
82000–82003h	4	"reg_CaptStartMode (is_2400_inp_sys_capt_unit_b_reg_CaptStartMode)—Offset 82000h" on page 1688	00000000h
82004–82007h	4	"reg_Capt_Start_Addr (is_2400_inp_sys_capt_unit_b_reg_Capt_Start_Addr)—Offset 82004h" on page 1689	00000000h
82008–8200Bh	4	"reg_Capt_Mem_Region_Size (is_2400_inp_sys_capt_unit_b_reg_Capt_Mem_Region_Size)—Offset 82008h" on page 1690	00000080h
8200C–8200Fh	4	"reg_Capt_Num_Mem_Regions (is_2400_inp_sys_capt_unit_b_reg_Capt_Num_Mem_Regions)—Offset 8200Ch" on page 1691	00000003h
82010–82013h	4	"reg_Capt_Init (is_2400_inp_sys_capt_unit_b_reg_Capt_Init)—Offset 82010h" on page 1692	00000000h
82014–82017h	4	"reg_Capt_Start_Addr (is_2400_inp_sys_capt_unit_b_reg_Capt_Start_Addr)—Offset 82004h" on page 1689	00000000h
82018–8201Bh	4	"reg_Capt_Stop (is_2400_inp_sys_capt_unit_b_reg_Capt_Stop)—Offset 82018h" on page 1694	00000000h
8201C–8201Fh	4	"reg_Capt_Packet_Length (is_2400_inp_sys_capt_unit_b_reg_Capt_Packet_Length)—Offset 8201Ch" on page 1694	00000000h
82020–82023h	4	"reg_Capt_Received_Length (is_2400_inp_sys_capt_unit_b_reg_Capt_Received_Length)—Offset 82020h" on page 1695	00000000h
82024–82027h	4	"reg_Capt_Received_Short_Packets (is_2400_inp_sys_capt_unit_b_reg_Capt_Received_Short_Packets)—Offset 82024h" on page 1696	00000000h
82028–8202Bh	4	"reg_Capt_Received_Long_Packets (is_2400_inp_sys_capt_unit_b_reg_Capt_Received_Long_Packets)—Offset 82028h" on page 1696	00000000h
8202C–8202Fh	4	"reg_Capt_Last_Command (is_2400_inp_sys_capt_unit_b_reg_Capt_Last_Command)—Offset 8202Ch" on page 1697	0000000Fh

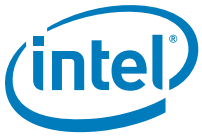


Table 28. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
82030–82033h	4	"reg_Capt_Next_Command (is_2400_inp_sys_capt_unit_b_reg_Capt_Next_Command)—Offset 82030h" on page 1698	0000000Fh
82034–82037h	4	"reg_Capt_Last_Acknowledge (is_2400_inp_sys_capt_unit_b_reg_Capt_Last_Acknowledge)—Offset 82034h" on page 1699	0000000Fh
82038–8203Bh	4	"reg_Capt_Next_Acknowledge (is_2400_inp_sys_capt_unit_b_reg_Capt_Next_Acknowledge)—Offset 82038h" on page 1699	0000000Fh
8203C–8203Fh	4	"reg_Capt_FSM_State_Info (is_2400_inp_sys_capt_unit_b_reg_Capt_FSM_State_Info)—Offset 8203Ch" on page 1700	00000000h
83000–83003h	4	"reg_CaptStartMode (is_2400_inp_sys_capt_unit_c_reg_CaptStartMode)—Offset 83000h" on page 1701	00000000h
83004–83007h	4	"reg_Capt_Start_Addr (is_2400_inp_sys_capt_unit_c_reg_Capt_Start_Addr)—Offset 83004h" on page 1702	00000000h
83008–8300Bh	4	"reg_Capt_Mem_Region_Size (is_2400_inp_sys_capt_unit_c_reg_Capt_Mem_Region_Size)—Offset 83008h" on page 1703	00000080h
8300C–8300Fh	4	"reg_Capt_Num_Mem_Regions (is_2400_inp_sys_capt_unit_c_reg_Capt_Num_Mem_Regions)—Offset 8300Ch" on page 1704	00000003h
83010–83013h	4	"reg_Capt_Init (is_2400_inp_sys_capt_unit_c_reg_Capt_Init)—Offset 83010h" on page 1704	00000000h
83014–83017h	4	"reg_Capt_Start_Addr (is_2400_inp_sys_capt_unit_c_reg_Capt_Start_Addr)—Offset 83004h" on page 1702	00000000h
83018–8301Bh	4	"reg_Capt_Stop (is_2400_inp_sys_capt_unit_c_reg_Capt_Stop)—Offset 83018h" on page 1706	00000000h
8301C–8301Fh	4	"reg_Capt_Packet_Length (is_2400_inp_sys_capt_unit_c_reg_Capt_Packet_Length)—Offset 8301Ch" on page 1707	00000000h
83020–83023h	4	"reg_Capt_Received_Length (is_2400_inp_sys_capt_unit_c_reg_Capt_Received_Length)—Offset 83020h" on page 1707	00000000h
83024–83027h	4	"reg_Capt_Received_Short_Packets (is_2400_inp_sys_capt_unit_c_reg_Capt_Received_Short_Packets)—Offset 83024h" on page 1708	00000000h
83028–8302Bh	4	"reg_Capt_Received_Long_Packets (is_2400_inp_sys_capt_unit_c_reg_Capt_Received_Long_Packets)—Offset 83028h" on page 1709	00000000h

Table 28. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8302C–8302Fh	4	"reg_Capt_Last_Command (is_2400_inp_sys_capt_unit_c_reg_Capt_Last_Command)—Offset 8302Ch" on page 1710	0000000Fh
83030–83033h	4	"reg_Capt_Next_Command (is_2400_inp_sys_capt_unit_c_reg_Capt_Next_Command)—Offset 83030h" on page 1710	0000000Fh
83034–83037h	4	"reg_Capt_Last_Acknowledge (is_2400_inp_sys_capt_unit_c_reg_Capt_Last_Acknowledge)—Offset 83034h" on page 1711	0000000Fh
83038–8303Bh	4	"reg_Capt_Next_Acknowledge (is_2400_inp_sys_capt_unit_c_reg_Capt_Next_Acknowledge)—Offset 83038h" on page 1712	0000000Fh
8303C–8303Fh	4	"reg_Capt_FSM_State_Info (is_2400_inp_sys_capt_unit_c_reg_Capt_FSM_State_Info)—Offset 8303Ch" on page 1712	00000000h
84000–84003h	4	"reg_Acq_Start_Addr (is_2400_inp_sys_acq_unit_reg_Acq_Start_Addr)—Offset 84000h" on page 1713	00000000h
84004–84007h	4	"reg_Acq_Mem_Region_Size (is_2400_inp_sys_acq_unit_reg_Acq_Mem_Region_Size)—Offset 84004h" on page 1714	00000080h
84008–8400Bh	4	"reg_Acq_Num_Mem_Regions (is_2400_inp_sys_acq_unit_reg_Acq_Num_Mem_Regions)—Offset 84008h" on page 1715	00000003h
8400C–8400Fh	4	"reg_Acq_Init (is_2400_inp_sys_acq_unit_reg_Acq_Init)—Offset 8400Ch" on page 1716	00000000h
84010–84013h	4	"reg_Acq_Received_Short_Packets (is_2400_inp_sys_acq_unit_reg_Acq_Received_Short_Packets)—Offset 84010h" on page 1717	00000000h
84014–84017h	4	"reg_Acq_Received_Long_Packets (is_2400_inp_sys_acq_unit_reg_Acq_Received_Long_Packets)—Offset 84014h" on page 1718	00000000h
84018–8401Bh	4	"reg_Acq_Last_Command (is_2400_inp_sys_acq_unit_reg_Acq_Last_Command)—Offset 84018h" on page 1718	0000000Fh
8401C–8401Fh	4	"reg_Acq_Next_Command (is_2400_inp_sys_acq_unit_reg_Acq_Next_Command)—Offset 8401Ch" on page 1719	0000000Fh
84020–84023h	4	"reg_Acq_Last_Acknowledge (is_2400_inp_sys_acq_unit_reg_Acq_Last_Acknowledge)—Offset 84020h" on page 1720	0000000Fh
84024–84027h	4	"reg_Acq_Next_Acknowledge (is_2400_inp_sys_acq_unit_reg_Acq_Next_Acknowledge)—Offset 84024h" on page 1720	0000000Fh

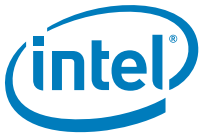


Table 28. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
84028–8402Bh	4	"reg_Acq_FSM_State_Info (is_2400_inp_sys_acq_unit_reg_Acq_FSM_State_Info)—Offset 84028h" on page 1721	00000000h
8402C–8402Fh	4	"reg_Acq_Int_Cntr_Info (is_2400_inp_sys_acq_unit_reg_Acq_Int_Cntr_Info)—Offset 8402Ch" on page 1722	00000000h
85000–85003h	4	"DMA_FSM_Command (is_2400_inp_sys_dma_DMA_FSM_Command)—Offset 85000h" on page 1723	00000000h
86000–86003h	4	"DMA_CH0_Packing_setup (is_2400_inp_sys_dma_DMA_CH0_Packing_setup)—Offset 86000h" on page 1724	00000000h
86100–86103h	4	"DMA_CH0_dev_stride_A (is_2400_inp_sys_dma_DMA_CH0_dev_stride_A)—Offset 86100h" on page 1725	00000000h
86200–86203h	4	"DMA_CH0_dev_Pack_left_crop_and_elem_A (is_2400_inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A)—Offset 86200h" on page 1725	00000000h
86300–86303h	4	"DMA_CH0_Device_Xb_A (is_2400_inp_sys_dma_DMA_CH0_Device_Xb_A)—Offset 86300h" on page 1726	00000000h
86400–86403h	4	"DMA_CH0_dev_stride_B (is_2400_inp_sys_dma_DMA_CH0_dev_stride_B)—Offset 86400h" on page 1727	00000000h
86500–86503h	4	"DMA_CH0_dev_Pack_left_crop_and_elem_B (is_2400_inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B)—Offset 86500h" on page 1728	00000000h
86600–86603h	4	"DMA_CH0_Device_Xb_B (is_2400_inp_sys_dma_DMA_CH0_Device_Xb_B)—Offset 86600h" on page 1729	00000000h
86700–86703h	4	"DMA_CH0_Yb (is_2400_inp_sys_dma_DMA_CH0_Yb)—Offset 86700h" on page 1729	00000000h
86800–86803h	4	"DMA_CH0_pending_command (is_2400_inp_sys_dma_DMA_CH0_pending_command)—Offset 86800h" on page 1730	00000000h
87000–87003h	4	"DMA_command_token (is_2400_inp_sys_dma_DMA_command_token)—Offset 87000h" on page 1731	00000000h
87004–87007h	4	"DMA_command_src_addr (is_2400_inp_sys_dma_DMA_command_src_addr)—Offset 87004h" on page 1732	00000000h
87008–8700Bh	4	"DMA_command_dst_addr (is_2400_inp_sys_dma_DMA_command_dst_addr)—Offset 87008h" on page 1732	00000000h

Table 28. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8700C–8700Fh	4	"DMA_command_ctrl_id (is_2400_inp_sys_dma_DMA_command_ctrl_id)—Offset 8700Ch" on page 1733	00000000h
87010–87013h	4	"DMA_FSM_Ctrl_status (is_2400_inp_sys_dma_DMA_FSM_Ctrl_status)—Offset 87010h" on page 1734	00000001h
87014–87017h	4	"DMA_FSM_Pack_status (is_2400_inp_sys_dma_DMA_FSM_Pack_status)—Offset 87014h" on page 1735	00000000h
87018–8701Bh	4	"DMA_FSM_request_status (is_2400_inp_sys_dma_DMA_FSM_request_status)—Offset 87018h" on page 1736	00000000h
8701C–8701Fh	4	"DMA_FSM_write_status (is_2400_inp_sys_dma_DMA_FSM_write_status)—Offset 8701Ch" on page 1736	00000000h
87110–87113h	4	"DMA_FSM_Ctrl_dev_idx (is_2400_inp_sys_dma_DMA_FSM_Ctrl_dev_idx)—Offset 87110h" on page 1737	00000000h
87114–87117h	4	"DMA_FSM_Pack_cnt_Yb (is_2400_inp_sys_dma_DMA_FSM_Pack_cnt_Yb)—Offset 87114h" on page 1738	00000000h
87118–8711Bh	4	"DMA_FSM_Request_cnt_Yb (is_2400_inp_sys_dma_DMA_FSM_Request_cnt_Yb)—Offset 87118h" on page 1739	00000000h
8711C–8711Fh	4	"DMA_FSM_Write_cnt_Y (is_2400_inp_sys_dma_DMA_FSM_Write_cnt_Y)—Offset 8711Ch" on page 1740	00000000h
87210–87213h	4	"DMA_FSM_Ctrl_req_addr (is_2400_inp_sys_dma_DMA_FSM_Ctrl_req_addr)—Offset 87210h" on page 1741	00000000h
87214–87217h	4	"DMA_FSM_Pack_req_cnt_Xb (is_2400_inp_sys_dma_DMA_FSM_Pack_req_cnt_Xb)—Offset 87214h" on page 1742	00000000h
87218–8721Bh	4	"DMA_FSM_Request_cnt_Xb (is_2400_inp_sys_dma_DMA_FSM_Request_cnt_Xb)—Offset 87218h" on page 1742	00000000h
8721C–8721Fh	4	"DMA_FSM_Write_cnt_Xb (is_2400_inp_sys_dma_DMA_FSM_Write_cnt_Xb)—Offset 8721Ch" on page 1743	00000000h
87310–87313h	4	"DMA_FSM_Ctrl_req_stride (is_2400_inp_sys_dma_DMA_FSM_Ctrl_req_stride)—Offset 87310h" on page 1744	00000000h
87314–87317h	4	"DMA_FSM_Pack_wr_cnt_Xb (is_2400_inp_sys_dma_DMA_FSM_Pack_wr_cnt_Xb)—Offset 87314h" on page 1745	00000000h

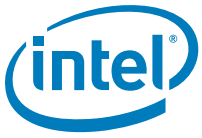


Table 28. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
87318–8731Bh	4	"DMA_FSM_Req_remining_Xb (is_2400_inp_sys_dma_DMA_FSM_Req_remining_Xb)—Offset 87318h" on page 1745	00000000h
8731C–8731Fh	4	"DMA_FSM_Wr_remining_Xb (is_2400_inp_sys_dma_DMA_FSM_Wr_remining_Xb)—Offset 8731Ch" on page 1746	00000000h
87410–87413h	4	"DMA_FSM_Ctrl_req_Xb (is_2400_inp_sys_dma_DMA_FSM_Ctrl_req_Xb)—Offset 87410h" on page 1747	00000000h
87418–8741Bh	4	"DMA_FSM_Req_burst_cnt (is_2400_inp_sys_dma_DMA_FSM_Req_burst_cnt)—Offset 87418h" on page 1748	0000FFFFh
8741C–8741Fh	4	"DMA_FSM_Wr_burst_cnt (is_2400_inp_sys_dma_DMA_FSM_Wr_burst_cnt)—Offset 8741Ch" on page 1749	0000FFFFh
87510–87513h	4	"DMA_FSM_Ctrl_req_Yb (is_2400_inp_sys_dma_DMA_FSM_Ctrl_req_Yb)—Offset 87510h" on page 1750	00000000h
87610–87613h	4	"DMA_FSM_Ctrl_Pack_req_dev_idx (is_2400_inp_sys_dma_DMA_FSM_Ctrl_Pack_req_dev_idx)—Offset 87610h" on page 1751	00000000h
87710–87713h	4	"DMA_FSM_Ctrl_Pack_wr_dev_idx (is_2400_inp_sys_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx)—Offset 87710h" on page 1752	00000000h
87810–87813h	4	"DMA_FSM_Ctrl_Wr_addr (is_2400_inp_sys_dma_DMA_FSM_Ctrl_Wr_addr)—Offset 87810h" on page 1753	00000000h
87910–87913h	4	"DMA_FSM_Ctrl_Wr_stride (is_2400_inp_sys_dma_DMA_FSM_Ctrl_Wr_stride)—Offset 87910h" on page 1754	00000000h
87A10–87A13h	4	"DMA_FSM_Ctrl_pack_req_Xb (is_2400_inp_sys_dma_DMA_FSM_Ctrl_pack_req_Xb)—Offset 87A10h" on page 1755	00000000h
87B10–87B13h	4	"DMA_FSM_Ctrl_pack_Yb (is_2400_inp_sys_dma_DMA_FSM_Ctrl_pack_Yb)—Offset 87B10h" on page 1755	00000000h
87C10–87C13h	4	"DMA_FSM_Ctrl_pack_wr_Xb (is_2400_inp_sys_dma_DMA_FSM_Ctrl_pack_wr_Xb)—Offset 87C10h" on page 1756	00000000h
87D10–87D13h	4	"DMA_FSM_Ctrl_pack_req_elem (is_2400_inp_sys_dma_DMA_FSM_Ctrl_pack_req_elem)—Offset 87D10h" on page 1757	00000000h
87E10–87E13h	4	"DMA_FSM_Ctrl_pack_wr_elem (is_2400_inp_sys_dma_DMA_FSM_Ctrl_pack_wr_elem)—Offset 87E10h" on page 1758	00000000h

Table 28. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
87F10–87F13h	4	"DMA_FSM_Ctrl_pack_sz_ext_ctrl_id (is_2400_inp_sys_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id)—Offset 87F10h" on page 1759	00000000h
88000–88003h	4	"Dev_Interf_0_req_side (is_2400_inp_sys_dma_Dev_Interf_0_req_side)—Offset 88000h" on page 1760	00000000h
88004–88007h	4	"Dev_Interf_1_req_side (is_2400_inp_sys_dma_Dev_Interf_1_req_side)—Offset 88004h" on page 1761	00000006h
88100–88103h	4	"Dev_Interf_0_snd_side (is_2400_inp_sys_dma_Dev_Interf_0_snd_side)—Offset 88100h" on page 1762	00000004h
88104–88107h	4	"Dev_Interf_1_snd_side (is_2400_inp_sys_dma_Dev_Interf_1_snd_side)—Offset 88104h" on page 1763	00000006h
88200–88203h	4	"Dev_Interf_0_Fifo_status (is_2400_inp_sys_dma_Dev_Interf_0_Fifo_status)—Offset 88200h" on page 1764	00000004h
88204–88207h	4	"Dev_Interf_1_Fifo_status (is_2400_inp_sys_dma_Dev_Interf_1_Fifo_status)—Offset 88204h" on page 1765	00000004h
88300–88303h	4	"Dev_Interf_0_Req_complete_bust (is_2400_inp_sys_dma_Dev_Interf_0_Req_complete_bust)—Offset 88300h" on page 1766	00000000h
88304–88307h	4	"Dev_Interf_1_Req_complete_bust (is_2400_inp_sys_dma_Dev_Interf_1_Req_complete_bust)—Offset 88304h" on page 1767	00000000h
88400–88403h	4	"Dev_Interf_1_Max_Burst_Size (is_2400_inp_sys_dma_Dev_Interf_1_Max_Burst_Size)—Offset 88400h" on page 1768	0000007Fh
89000–89003h	4	"inpsys_captA_start_addr (is_2400_inp_sys_inp_ctrl_inpsys_captA_start_addr)—Offset 89000h" on page 1769	00000000h
89004–89007h	4	"inpsys_captB_start_addr (is_2400_inp_sys_inp_ctrl_inpsys_captB_start_addr)—Offset 89004h" on page 1770	00000000h
89008–8900Bh	4	"inpsys_captC_start_addr (is_2400_inp_sys_inp_ctrl_inpsys_captC_start_addr)—Offset 89008h" on page 1771	00000000h
8900C–8900Fh	4	"inpsys_captA_mem_region_size (is_2400_inp_sys_inp_ctrl_inpsys_captA_mem_region_size)—Offset 8900Ch" on page 1772	00000080h
89010–89013h	4	"inpsys_captB_mem_region_size (is_2400_inp_sys_inp_ctrl_inpsys_captB_mem_region_size)—Offset 89010h" on page 1773	00000080h

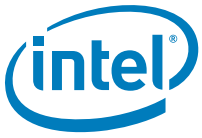


Table 28. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
89014–89017h	4	"inpsys_captC_mem_region_size (is_2400_inp_sys_inp_ctrl_inpsys_captC_mem_region_size)—Offset 89014h" on page 1774	00000080h
89018–8901Bh	4	"inpsys_captA_num_mem_regions (is_2400_inp_sys_inp_ctrl_inpsys_captA_num_mem_regions)—Offset 89018h" on page 1775	00000003h
8901C–8901Fh	4	"inpsys_captB_num_mem_regions (is_2400_inp_sys_inp_ctrl_inpsys_captB_num_mem_regions)—Offset 8901Ch" on page 1776	00000003h
89020–89023h	4	"inpsys_captC_num_mem_regions (is_2400_inp_sys_inp_ctrl_inpsys_captC_num_mem_regions)—Offset 89020h" on page 1777	00000003h
89024–89027h	4	"inpsys_acq_start_addr (is_2400_inp_sys_inp_ctrl_inpsys_acq_start_addr)—Offset 89024h" on page 1778	00000000h
89028–8902Bh	4	"inpsys_acq_mem_region_size (is_2400_inp_sys_inp_ctrl_inpsys_acq_mem_region_size)—Offset 89028h" on page 1779	00000080h
8902C–8902Fh	4	"inpsys_acq_num_mem_regions (is_2400_inp_sys_inp_ctrl_inpsys_acq_num_mem_regions)—Offset 8902Ch" on page 1780	00000003h
89030–89033h	4	"inpsys_ctrl_init (is_2400_inp_sys_inp_ctrl_inpsys_ctrl_init)—Offset 89030h" on page 1781	00000000h
89034–89037h	4	"inpsys_last_cmd (is_2400_inp_sys_inp_ctrl_inpsys_last_cmd)—Offset 89034h" on page 1782	0000000Fh
89038–8903Bh	4	"inpsys_next_cmd (is_2400_inp_sys_inp_ctrl_inpsys_next_cmd)—Offset 89038h" on page 1783	0000000Fh
8903C–8903Fh	4	"inpsys_last_ack (is_2400_inp_sys_inp_ctrl_inpsys_last_ack)—Offset 8903Ch" on page 1783	0000000Fh
89040–89043h	4	"inpsys_next_ack (is_2400_inp_sys_inp_ctrl_inpsys_next_ack)—Offset 89040h" on page 1784	0000000Fh
89044–89047h	4	"inpsys_top_fsm_state (is_2400_inp_sys_inp_ctrl_inpsys_top_fsm_state)—Offset 89044h" on page 1784	00000000h
89048–8904Bh	4	"inpsys_captA_fsm_state (is_2400_inp_sys_inp_ctrl_inpsys_captA_fsm_state)—Offset 89048h" on page 1785	00000000h
8904C–8904Fh	4	"inpsys_captB_fsm_state (is_2400_inp_sys_inp_ctrl_inpsys_captB_fsm_state)—Offset 8904Ch" on page 1786	00000000h

Table 28. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
89050–89053h	4	"inpsys_captC_fsm_state (is_2400_inp_sys_inp_ctrl_inpsys_captC_fsm_state)—Offset 89050h" on page 1787	00000000h
89054–89057h	4	"inpsys_acq_fsm_state (is_2400_inp_sys_inp_ctrl_inpsys_acq_fsm_state)—Offset 89054h" on page 1788	00000000h
89058–8905Bh	4	"inpsys_capt_reserve_one_mem_region (is_2400_inp_sys_inp_ctrl_inpsys_capt_reserve_one_mem_region)—Offset 89058h" on page 1788	00000000h
8A000–8A003h	4	"str_multicastA_sel (is_2400_inp_sys_gpreg_str_multicastA_sel)—Offset 8A000h" on page 1789	00000000h
8A004–8A007h	4	"str_multicastB_sel (is_2400_inp_sys_gpreg_str_multicastB_sel)—Offset 8A004h" on page 1790	00000000h
8A008–8A00Bh	4	"str_multicastC_sel (is_2400_inp_sys_gpreg_str_multicastC_sel)—Offset 8A008h" on page 1791	00000000h
8A00C–8A00Fh	4	"str_mux_sel (is_2400_inp_sys_gpreg_str_mux_sel)—Offset 8A00Ch" on page 1791	00000000h
8A010–8A013h	4	"str_mon_status (is_2400_inp_sys_gpreg_str_mon_status)—Offset 8A010h" on page 1792	00000000h
8A014–8A017h	4	"str_mon_irq_cond (is_2400_inp_sys_gpreg_str_mon_irq_cond)—Offset 8A014h" on page 1793	00000000h
8A018–8A01Bh	4	"str_mon_irq_en (is_2400_inp_sys_gpreg_str_mon_irq_en)—Offset 8A018h" on page 1794	00000000h
8A01C–8A01Fh	4	"isys_srst (is_2400_inp_sys_gpreg_isys_srst)—Offset 8A01Ch" on page 1796	00000000h
8A020–8A023h	4	"isys_slv_reg_srst (is_2400_inp_sys_gpreg_isys_slv_reg_srst)—Offset 8A020h" on page 1797	00000000h
8A024–8A027h	4	"str_deint_portA_cnt (is_2400_inp_sys_gpreg_str_deint_portA_cnt)—Offset 8A024h" on page 1798	00000000h
8A028–8A02Bh	4	"str_deint_portB_cnt (is_2400_inp_sys_gpreg_str_deint_portB_cnt)—Offset 8A028h" on page 1799	00000000h
8B000–8B003h	4	"CSI_generic_short_packet (is_2400_inp_sys_fifo_adapter_CSI_generic_short_packet)—Offset 8B000h" on page 1800	00000000h
8B008–8B00Bh	4	"CSI_generic_short_packet_available (is_2400_inp_sys_fifo_adapter_CSI_generic_short_packet_available)—Offset 8B008h" on page 1801	00000001h

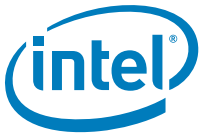


Table 28. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8C000–8C003h	4	"irq_edge (is_2400_inp_sys_irq_ctrl_irq_edge)—Offset 8C000h" on page 1802	00000000h
8C004–8C007h	4	"irq_mask (is_2400_inp_sys_irq_ctrl_irq_mask)—Offset 8C004h" on page 1803	00000000h
8C008–8C00Bh	4	"irq_status (is_2400_inp_sys_irq_ctrl_irq_status)—Offset 8C008h" on page 1805	00000000h
8C00C–8C00Fh	4	"irq_clear (is_2400_inp_sys_irq_ctrl_irq_clear)—Offset 8C00Ch" on page 1806	00000000h
8C010–8C013h	4	"irq_en (is_2400_inp_sys_irq_ctrl_irq_en)—Offset 8C010h" on page 1807	00000000h
8C014–8C017h	4	"irq_level_not_pulse (is_2400_inp_sys_irq_ctrl_irq_level_not_pulse)—Offset 8C014h" on page 1809	00000000h
90000–90003h	4	"reg_gp_syncgen_enable (is_2400_isel_gpr_reg_gp_syncgen_enable)—Offset 90000h" on page 1810	00000000h
90004–90007h	4	"reg_gp_syncgen_free_running (is_2400_isel_gpr_reg_gp_syncgen_free_running)—Offset 90004h" on page 1811	00000000h
90008–9000Bh	4	"reg_gp_syncgen_pause (is_2400_isel_gpr_reg_gp_syncgen_pause)—Offset 90008h" on page 1812	00000000h
9000C–9000Fh	4	"reg_gp_nr_frames (is_2400_isel_gpr_reg_gp_nr_frames)—Offset 9000Ch" on page 1812	00000000h
90010–90013h	4	"reg_gp_syngen_nr_pix (is_2400_isel_gpr_reg_gp_syngen_nr_pix)—Offset 90010h" on page 1813	00000000h
90014–90017h	4	"reg_gp_syngen_nr_lines (is_2400_isel_gpr_reg_gp_syngen_nr_lines)—Offset 90014h" on page 1814	00000000h
90018–9001Bh	4	"reg_gp_syngen_hblank_cycles (is_2400_isel_gpr_reg_gp_syngen_hblank_cycles)—Offset 90018h" on page 1815	00000000h
9001C–9001Fh	4	"reg_gp_syngen_vblank_cycles (is_2400_isel_gpr_reg_gp_syngen_vblank_cycles)—Offset 9001Ch" on page 1815	00000000h
90020–90023h	4	"reg_gp_isel_sof (is_2400_isel_gpr_reg_gp_isel_sof)—Offset 90020h" on page 1816	00000000h
90024–90027h	4	"reg_gp_isel_eof (is_2400_isel_gpr_reg_gp_isel_eof)—Offset 90024h" on page 1817	00000000h
90028–9002Bh	4	"reg_gp_isel_sol (is_2400_isel_gpr_reg_gp_isel_sol)—Offset 90028h" on page 1818	00000000h
9002C–9002Fh	4	"reg_gp_isel_eol (is_2400_isel_gpr_reg_gp_isel_eol)—Offset 9002Ch" on page 1819	00000000h

Table 28. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
90030–90033h	4	"reg_gp_isel_lfsr_enable (is_2400_isel_gpr_reg_gp_isel_lfsr_enable)—Offset 90030h" on page 1819	00000000h
90034–90037h	4	"reg_gp_isel_lfsr_enable_b (is_2400_isel_gpr_reg_gp_isel_lfsr_enable_b)—Offset 90034h" on page 1820	00000000h
90038–9003Bh	4	"reg_gp_isel_lfsr_reset_value (is_2400_isel_gpr_reg_gp_isel_lfsr_reset_value)—Offset 90038h" on page 1821	00000000h
9003C–9003Fh	4	"reg_gp_isel_tpg_enable (is_2400_isel_gpr_reg_gp_isel_tpg_enable)—Offset 9003Ch" on page 1822	00000000h
90040–90043h	4	"reg_gp_isel_tpg_enable_b (is_2400_isel_gpr_reg_gp_isel_tpg_enable_b)—Offset 90040h" on page 1823	00000000h
90044–90047h	4	"reg_gp_isel_hor_cnt_mask (is_2400_isel_gpr_reg_gp_isel_hor_cnt_mask)—Offset 90044h" on page 1824	00000000h
90048–9004Bh	4	"reg_gp_isel_ver_cnt_mask (is_2400_isel_gpr_reg_gp_isel_ver_cnt_mask)—Offset 90048h" on page 1825	00000000h
9004C–9004Fh	4	"reg_gp_isel_xy_cnt_mask (is_2400_isel_gpr_reg_gp_isel_xy_cnt_mask)—Offset 9004Ch" on page 1826	00000000h
90050–90053h	4	"reg_gp_isel_hor_cnt_delta (is_2400_isel_gpr_reg_gp_isel_hor_cnt_delta)—Offset 90050h" on page 1827	00000000h
90054–90057h	4	"reg_gp_isel_ver_cnt_delta (is_2400_isel_gpr_reg_gp_isel_ver_cnt_delta)—Offset 90054h" on page 1828	00000000h
90058–9005Bh	4	"reg_gp_isel_tpg_mode (is_2400_isel_gpr_reg_gp_isel_tpg_mode)—Offset 90058h" on page 1829	00000000h
9005C–9005Fh	4	"reg_gp_isel_tpg_red1 (is_2400_isel_gpr_reg_gp_isel_tpg_red1)—Offset 9005Ch" on page 1830	00000000h
90060–90063h	4	"reg_gp_isel_tpg_green1 (is_2400_isel_gpr_reg_gp_isel_tpg_green1)—Offset 90060h" on page 1831	00000000h
90064–90067h	4	"reg_gp_isel_tpg_blue1 (is_2400_isel_gpr_reg_gp_isel_tpg_blue1)—Offset 90064h" on page 1832	00000000h
90068–9006Bh	4	"reg_gp_isel_tpg_red2 (is_2400_isel_gpr_reg_gp_isel_tpg_red2)—Offset 90068h" on page 1832	00000000h

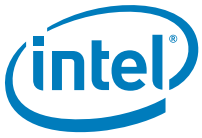


Table 28. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
9006C–9006Fh	4	"reg_gp_isel_tpg_green2 (is_2400_isel_gpr_reg_gp_isel_tpg_green2)—Offset 9006Ch" on page 1833	00000000h
90070–90073h	4	"reg_gp_isel_tpg_blue2 (is_2400_isel_gpr_reg_gp_isel_tpg_blue2)—Offset 90070h" on page 1834	00000000h
90074–90077h	4	"reg_gp_isel_ch_id (is_2400_isel_gpr_reg_gp_isel_ch_id)—Offset 90074h" on page 1834	00000000h
90078–9007Bh	4	"reg_gp_isel_fmt_type (is_2400_isel_gpr_reg_gp_isel_fmt_type)—Offset 90078h" on page 1835	00000000h
9007C–9007Fh	4	"reg_gp_isel_data_sel (is_2400_isel_gpr_reg_gp_isel_data_sel)—Offset 9007Ch" on page 1836	00000000h
90080–90083h	4	"reg_gp_isel_sband_sel (is_2400_isel_gpr_reg_gp_isel_sband_sel)—Offset 90080h" on page 1837	00000000h
90084–90087h	4	"reg_gp_isel_sync_sel (is_2400_isel_gpr_reg_gp_isel_sync_sel)—Offset 90084h" on page 1837	00000000h
90088–9008Bh	4	"reg_gp_syncgen_hor_cnt (is_2400_isel_gpr_reg_gp_syncgen_hor_cnt)—Offset 90088h" on page 1838	00000000h
9008C–9008Fh	4	"reg_gp_syncgen_ver_cnt (is_2400_isel_gpr_reg_gp_syncgen_ver_cnt)—Offset 9008Ch" on page 1839	00000000h
90090–90093h	4	"reg_gp_syncgen_frame_cnt (is_2400_isel_gpr_reg_gp_syncgen_frame_cnt)—Offset 90090h" on page 1840	00000000h
90094–90097h	4	"reg_gp_soft_reset (is_2400_isel_gpr_reg_gp_soft_reset)—Offset 90094h" on page 1841	00000000h
90104–90107h	4	"send_to_GP_FIFO (is_2400_isel_fa_send_to_GP_FIFO)—Offset 90104h" on page 1842	00000000h
9010C–9010Fh	4	"check_send_to_GP_FIFO (is_2400_isel_fa_check_send_to_GP_FIFO)—Offset 9010Ch" on page 1843	00000001h
90200–90203h	4	"reg_irq_edge (is_2400_isel_irq_ctrl_reg_irq_edge)—Offset 90200h" on page 1843	00000000h
90204–90207h	4	"reg_irq_mask (is_2400_isel_irq_ctrl_reg_irq_mask)—Offset 90204h" on page 1844	00000000h
90208–9020Bh	4	"reg_irq_status (is_2400_isel_irq_ctrl_reg_irq_status)—Offset 90208h" on page 1845	00000000h
9020C–9020Fh	4	"reg_irq_clear (is_2400_isel_irq_ctrl_reg_irq_clear)—Offset 9020Ch" on page 1846	00000000h

Table 28. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
90210–90213h	4	"reg_irq_enable (is_2400_isel_irq_ctrl_reg_irq_enable)—Offset 90210h" on page 1846	00000000h
90214–90217h	4	"reg_irq_level_not_pulse (is_2400_isel_irq_ctrl_reg_irq_level_not_pulse)—Offset 90214h" on page 1847	00000000h
A0000–A0003h	4	"MMU_invalidate_cache (icache_out_sys_c_mmu_MMU_invalidate_cache)—Offset A0000h" on page 1848	00000000h
A0004–A0007h	4	"MMU_page_table_base (icache_out_sys_c_mmu_MMU_page_table_base)—Offset A0004h" on page 1849	00000000h
B0000–B0007h	8	"mem_scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_first_type (scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_first)—Offset B0000h" on page 1849	0000000000000000h
B7FF8–B7FFFh	8	"mem_scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_last_type (scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_last)—Offset B7FF8h" on page 1851	0000000000000000h

5.3.1 csi1_dev_ready (is_2400_inp_sys_csi_receiver_csi1_dev_ready)—Offset 80100h

Set after programming operational registers to enable receiver

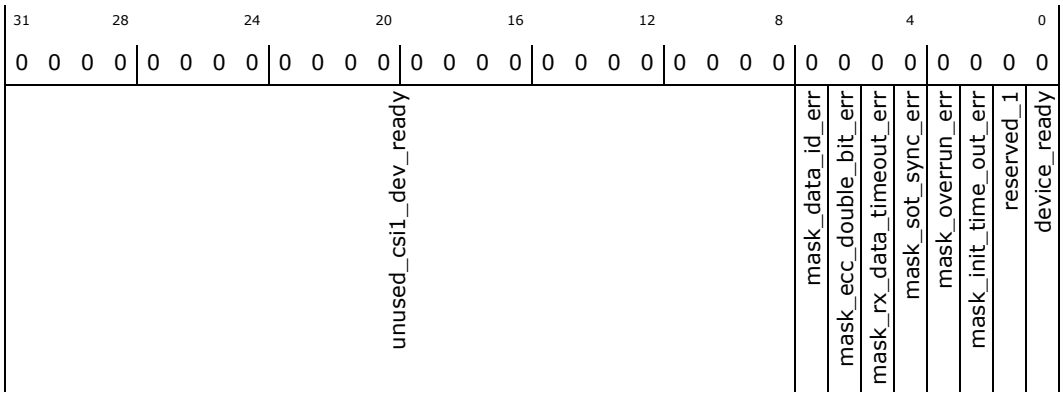
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (unused_csi1_dev_ready):** Unused
7	0x0 RW	**mask_data_id_err:** Set to mask error recovery when data ID error is detected
6	0x0 RW	**mask_ecc_double_bit_err:** Set to mask error recovery when ECC double bit error is detected
5	0x0 RW	**mask_rx_data_timeout_err:** Set to mask error recovery when receive data time out error is detected
4	0x0 RW	**mask_sot_sync_err:** Set to mask error recovery when start of transmission sync error is detected
3	0x0 RW	**mask_overrun_err:** set to mask overrun: NOT used now, can be discarded
2	0x0 RW	**mask_init_time_out_err:** Set to mask error recovery when initialization time out error is detected
1	0x0 RO	**reserved_1:** Reserved
0	0x0 RW	**device_ready:** Set to indicate that device is ready for reception

5.3.2 csi1_int_status (is_2400_inp_sys_csi_receiver_csi1_int_status)—Offset 80104h

Interrupt Status

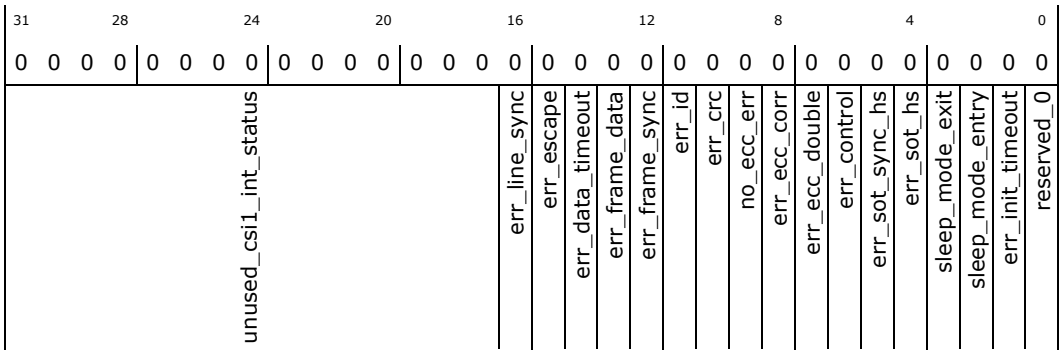
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80104h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (unused_csi1_int_status):** Unused
16	0x0 RW/1C	**err_line_sync:** Set if line number for line start and line end packets do not match
15	0x0 RW/1C	**err_escape:** Set if an unrecognized escape entry command is received
14	0x0 RW/1C	**err_data_timeout:** Set if time taken to receive a packet exceeds programmed timeout value
13	0x0 RW/1C	**err_frame_data:** Set if data packets within a frame has errors
12	0x0 RW/1C	**err_frame_sync:** Set if frame start is not paired with frame end for same virtual channel
11	0x0 RW/1C	**err_id:** Set if packet header has a unrecognized data id
10	0x0 RW/1C	**err_crc:** Set if computed CRC differs from received value
9	0x0 RW/1C	**no_ecc_err:** Set if no ECC error detected in packet
8	0x0 RW/1C	**err_ecc_corr:** Set if ECC error detected and corrected for one bit

Bit Range	Default and Access	Field Name (ID): Description
7	0x0 RW/1C	**err_ecc_double:** Set if ECC error detected for two or more bits
6	0x0 RW/1C	**err_control:** Set if DPHY flags a control error
5	0x0 RW/1C	**err_sot_sync_hs:** Set if DPHY flags start of transmission synchronisation error
4	0x0 RW/1C	**err_sot_hs:** Set if DPHY flags start of transmission error
3	0x0 RW/1C	**sleep_mode_exit:** Set if DPHY exits ultra low power state
2	0x0 RW/1C	**sleep_mode_entry:** Set if DPHY enters ultra low power state
1	0x0 RW/1C	**err_init_timeout:** Set if Initialization timeout error occurs on DPHY data lanes
0	0x0 RO	**reserved_0:** Always set to 0

5.3.3 csi1_int_enable (is_2400_inp_sys_csi_receiver_csi1_int_enable)—Offset 80108h

Interrupt Enable

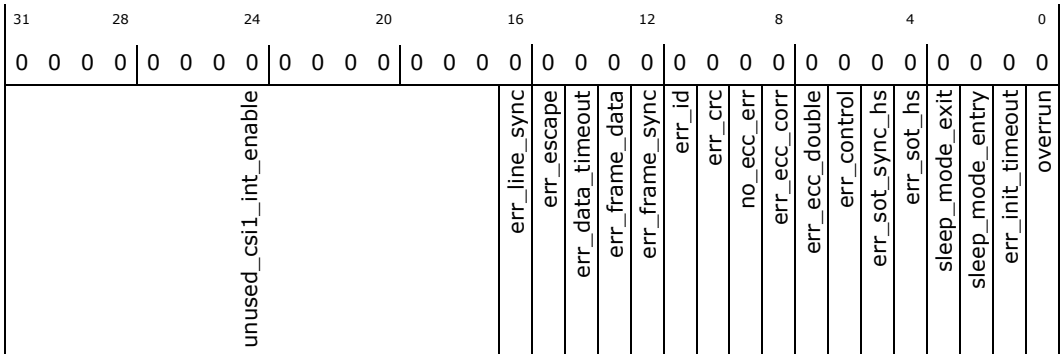
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80108h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (unused_csi1_int_enable):** Unused
16	0x0 RW	**err_line_sync:** Enable line sync error interrupt
15	0x0 RW	**err_escape:** Enable escape entry error interrupt
14	0x0 RW	**err_data_timeout:** Enable timeout error interrupt
13	0x0 RW	**err_frame_data:** Enable frame data error interrupt
12	0x0 RW	**err_frame_sync:** Enable frame sync error interrupt
11	0x0 RW	**err_id:** Enable data id error interrupt
10	0x0 RW	**err_crc:** Enable CRC error interrupt
9	0x0 RW	**no_ecc_err:** Enable no ECC error interrupt
8	0x0 RW	**err_ecc_corr:** Enable ECC error detected and corrected for one bit interrupt
7	0x0 RW	**err_ecc_double:** Enable ECC error detected for two or more bits interrupt
6	0x0 RW	**err_control:** Enable control error interrupt
5	0x0 RW	**err_sot_sync_hs:** Enable start of transmission synchronisation error interrupt
4	0x0 RW	**err_sot_hs:** Enable start of transmission error interrupt
3	0x0 RW	**sleep_mode_exit:** Enable sleep mode exit interrupt
2	0x0 RW	**sleep_mode_entry:** Enable sleep mode entry interrupt
1	0x0 RW	**err_init_timeout:** Enable Initialization timeout error interrupt
0	0x0 RW	**overrun:** Not used

5.3.4 csi1_func_prg (is_2400_inp_sys_csi_receiver_csi1_func_prg)—Offset 8010Ch

Functional Programming CSI1

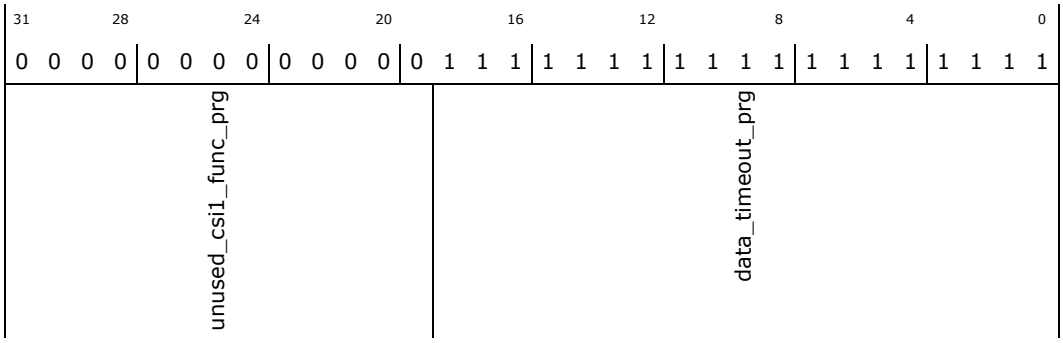
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8010Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0007FFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:19	0x0 RO	**Reserved (unused_csi1_func_prg):** Unused
18:0	0x7ffff RW	**data_timeout_prg:** Data timeout value to be checked for long packets

5.3.5 csi1_init_cnt (is_2400_inp_sys_csi_receiver_csi1_init_cnt)—Offset 80110h

Duration after power up when DPHY lanes will not be observed

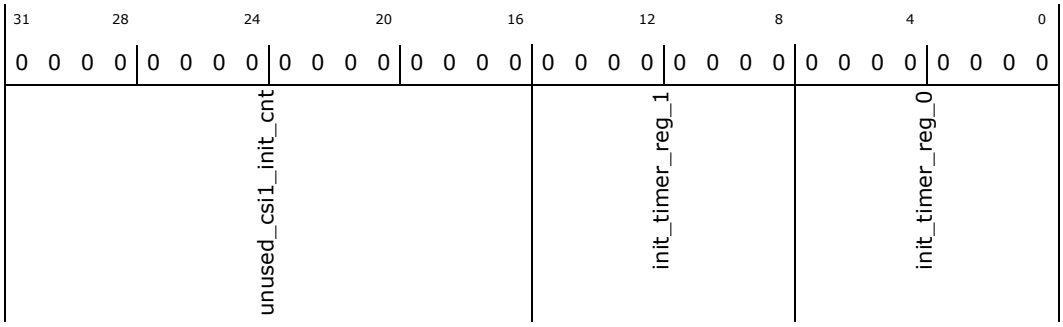
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80110h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (unused_csi1_init_cnt):** Unused
15:8	0x0 RW	**init_timer_reg_1:** Byte 1 for power up timer
7:0	0x0 RW	**init_timer_reg_0:** Byte 0 for power up timer

5.3.6 csi_backend_fs_ls (is_2400_inp_sys_csi_receiver_csi_backend_fs_ls)—Offset 8011Ch

Minimum interval between frame start and line start syncs

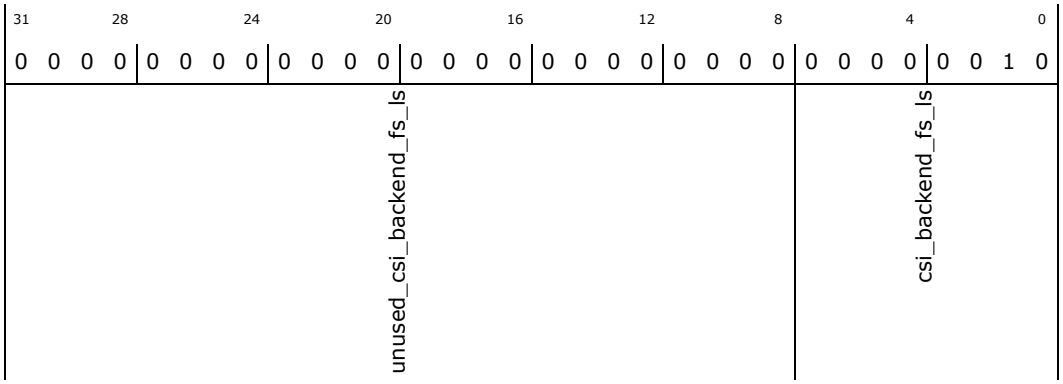
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8011Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000002h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved (unused_csi_backend_fs_ls):** Unused
7:0	0x2 RW	**csi_backend_fs_ls:** Minimum interval between frame start and line start syncs

5.3.7 csi_backend_ls_dvalid (is_2400_inp_sys_csi_receiver_csi_backend_ls_dvalid)—Offset 80120h

Minimum interval between line start sync and valid data

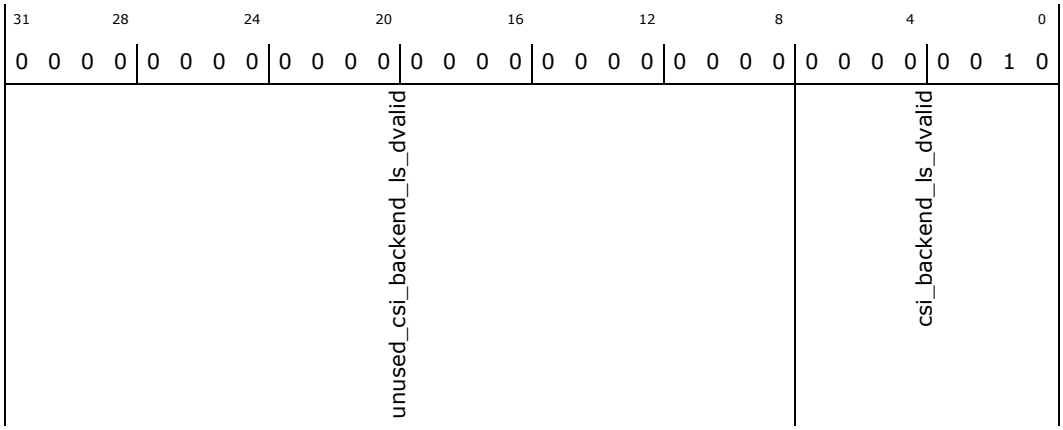
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80120h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000002h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved (unused_csi_backend_ls_dvalid):** Unused
7:0	0x2 RW	**csi_backend_ls_dvalid:** Minimum interval between line start sync and valid data

5.3.8 csi_backend_dvalid_le (is_2400_inp_sys_csi_receiver_csi_backend_dvalid_le)—Offset 80124h

Minimum interval between valid data and line end sync

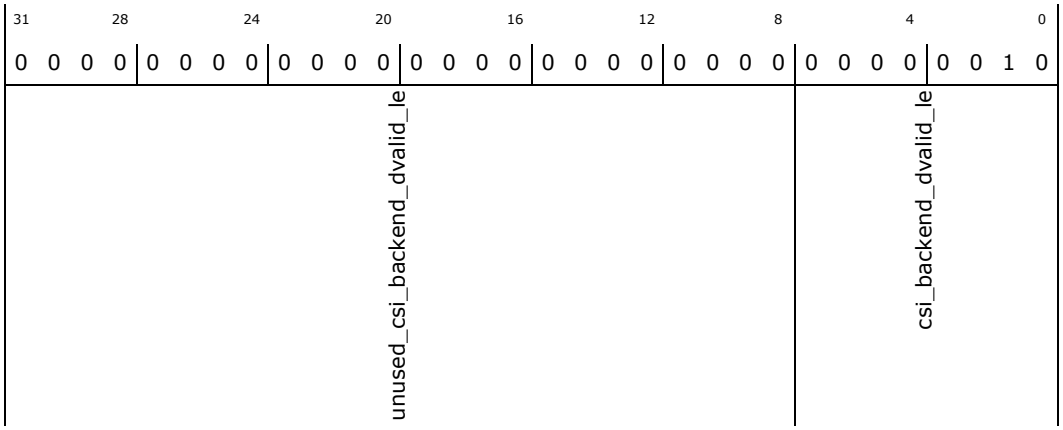
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80124h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000002h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved (unused_csi_backend_dvalid_le):** Unused
7:0	0x2 RW	**csi_backend_dvalid_le:** Minimum interval between valid data and line end sync

5.3.9 csi_backend_le_fe (is_2400_inp_sys_csi_receiver_csi_backend_le_fe)—Offset 80128h

Minimum interval between line end and frame end syncs

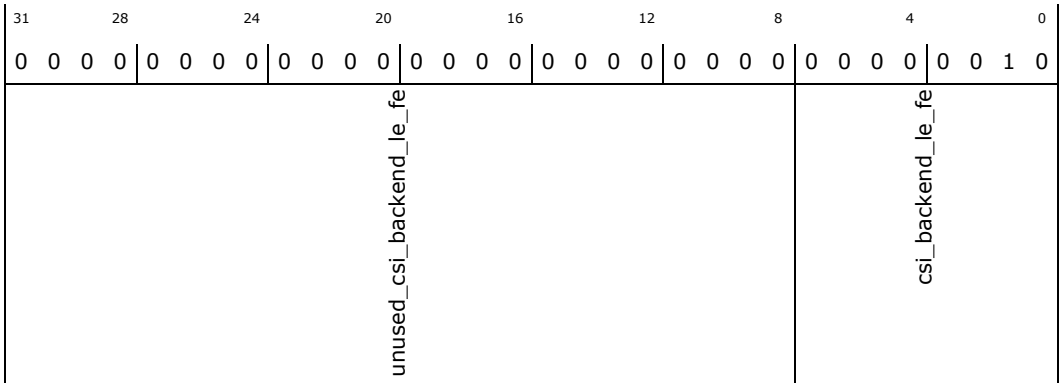
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80128h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000002h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved (unused_csi_backend_le_fe):** Unused
7:0	0x2 RW	**csi_backend_le_fe:** Minimum interval between line end and frame end syncs

5.3.10 csi_backend_fe_fs (is_2400_inp_sys_csi_receiver_csi_backend_fe_fs)—Offset 8012Ch

Minimum interval between frame end and frame start syncs

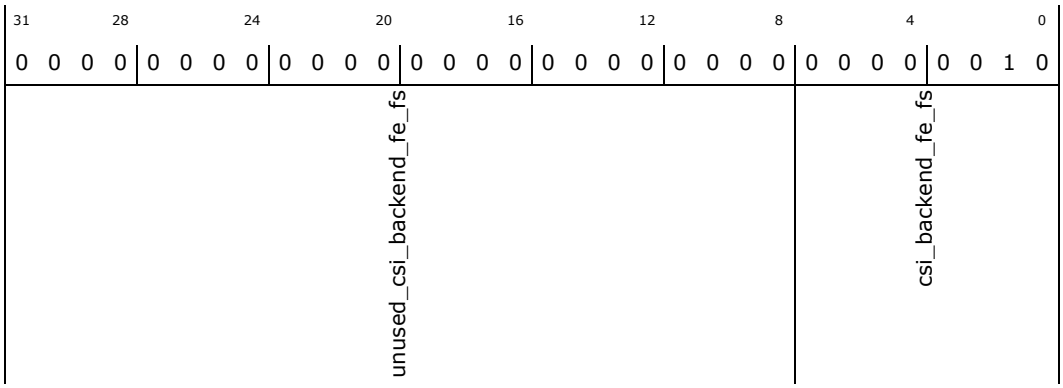
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8012Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000002h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved (unused_csi_backend_fe_fs):** Unused
7:0	0x2 RW	**csi_backend_fe_fs:** Minimum interval between frame end and frame start syncs

5.3.11 csi_backend_le_ls (is_2400_inp_sys_csi_receiver_csi_backend_le_ls)—Offset 80130h

Minimum interval between line end and line start syncs

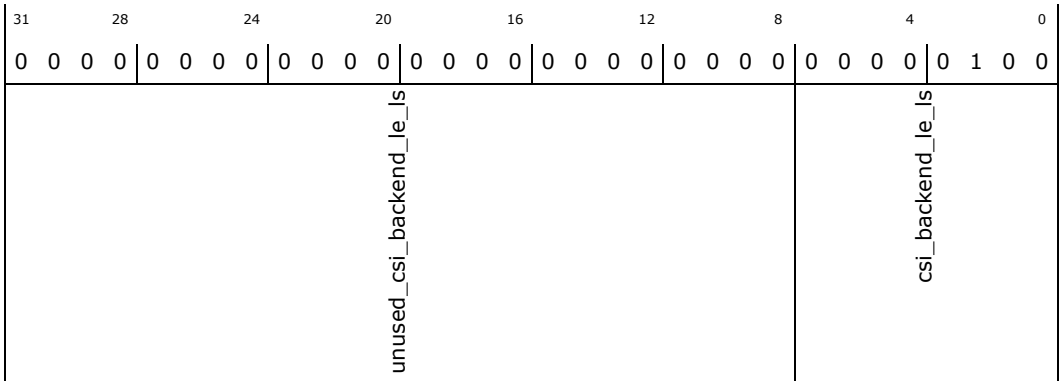
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80130h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved (unused_csi_backend_le_ls):** Unused
7:0	0x4 RW	**csi_backend_le_ls:** Minimum interval between line end and line start syncs

5.3.12 csi_backend_two_pixel_en (is_2400_inp_sys_csi_receiver_csi_backend_two_pixel_en)—Offset 80134h

Enable two pixels per clock mode

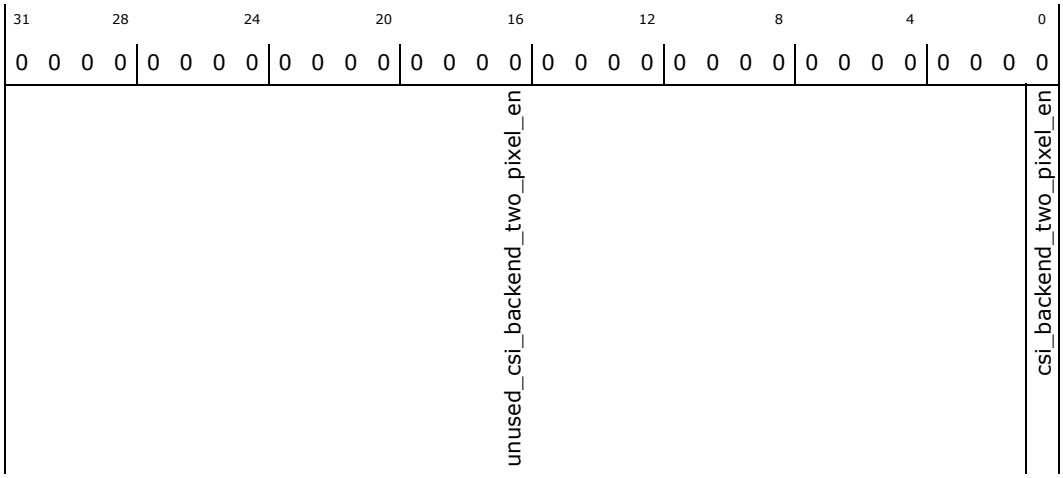
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80134h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_csi_backend_two_pixel_en):** Unused
0	0x0 RW	**csi_backend_two_pixel_en:** Enable two pixels per clock mode

5.3.13 csi1_raw16_18_data_id (is_2400_inp_sys_csi_receiver_csi1_raw16_18_data_id) —Offset 80138h

RAW 16 and RAW 18 data ID register

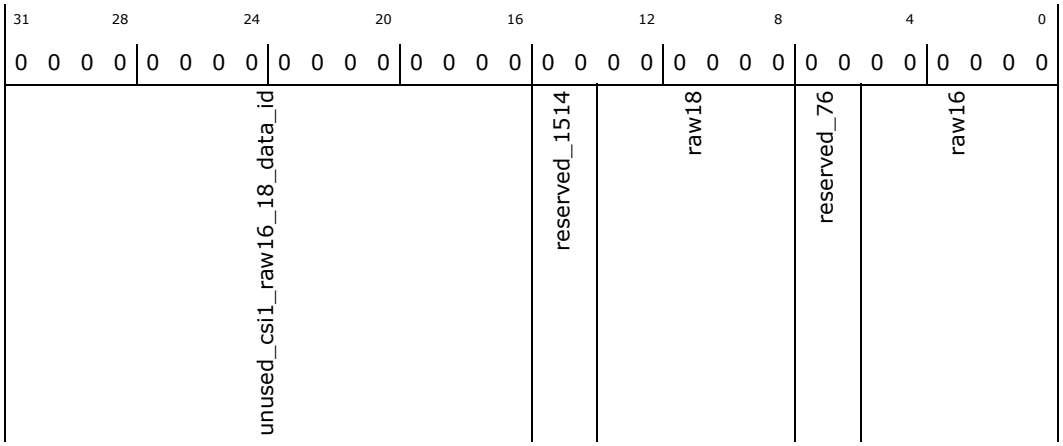
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80138h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (unused_csi1_raw16_18_data_id):** Unused
15:14	0x0 RO	**reserved_1514:** Reserved
13:8	0x0 RW	**raw18:** 6 bit format id value for RAW 18. If CSI receiver backend receives a packet with this format id, it will unpack it as RAW 18 data
7:6	0x0 RO	**reserved_76:** Reserved
5:0	0x0 RW	**raw16:** 6 bit format id value for RAW 16. If CSI receiver backend receives a packet with this format id, it will unpack it as RAW 16 data

5.3.14 csi1_sync_cnt (is_2400_inp_sys_csi_receiver_csi1_sync_cnt)—Offset 8013Ch

Synchronisation count value in terms of MIPI high speed byte clock

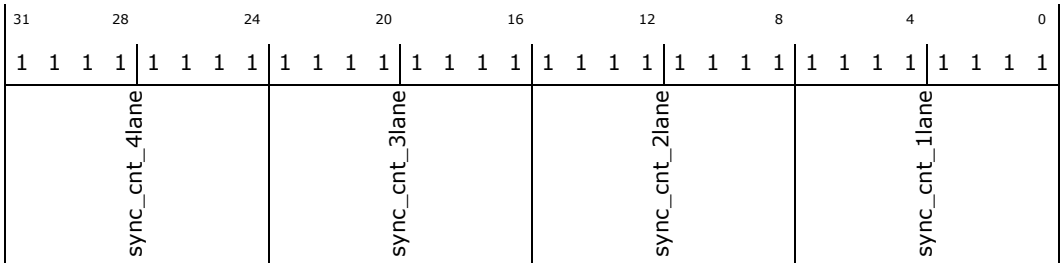
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8013Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:24	0xff RW	**sync_cnt_4lane:** Synchronisation count value for lane 4. Number of MIPI high speed clock cycles from high speed enable to SOT pattern detection. If this period has elapsed without an SOT pattern detection, an SOT sync error will be triggered
23:16	0xff RW	**sync_cnt_3lane:** Synchronisation count value for lane 3. Number of MIPI high speed clock cycles from high speed enable to SOT pattern detection. If this period has elapsed without an SOT pattern detection, an SOT sync error will be triggered
15:8	0xff RW	**sync_cnt_2lane:** Synchronisation count value for lane 2. Number of MIPI high speed clock cycles from high speed enable to SOT pattern detection. If this period has elapsed without an SOT pattern detection, an SOT sync error will be triggered
7:0	0xff RW	**sync_cnt_1lane:** Synchronisation count value for lane 1. Number of MIPI high speed clock cycles from high speed enable to SOT pattern detection. If this period has elapsed without an SOT pattern detection, an SOT sync error will be triggered

5.3.15 csi1_rx_cnt (is_2400_inp_sys_csi_receiver_csi1_rx_cnt)—Offset 80140h

Receive count value in terms of MIPI high speed byte clock

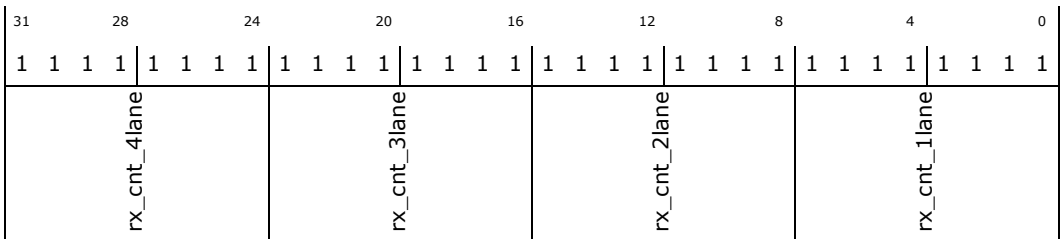
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80140h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:24	0xff RW	**rx_cnt_4lane:** Receive count value for lane 4. Controls the number of MIPI high speed clock cycles between LP-00 state detection and enabling of high speed receiver
23:16	0xff RW	**rx_cnt_3lane:** Receive count value for lane 3. Controls the number of MIPI high speed clock cycles between LP-00 state detection and enabling of high speed receiver
15:8	0xff RW	**rx_cnt_2lane:** Receive count value for lane 2. Controls the number of MIPI high speed clock cycles between LP-00 state detection and enabling of high speed receiver
7:0	0xff RW	**rx_cnt_1lane:** Receive count value for lane 1. Controls the number of MIPI high speed clock cycles between LP-00 state detection and enabling of high speed receiver

5.3.16 csi_backend_rst (is_2400_inp_sys_csi_receiver_csi_backend_rst)—Offset 80144h

Reset CSI Rx backend block

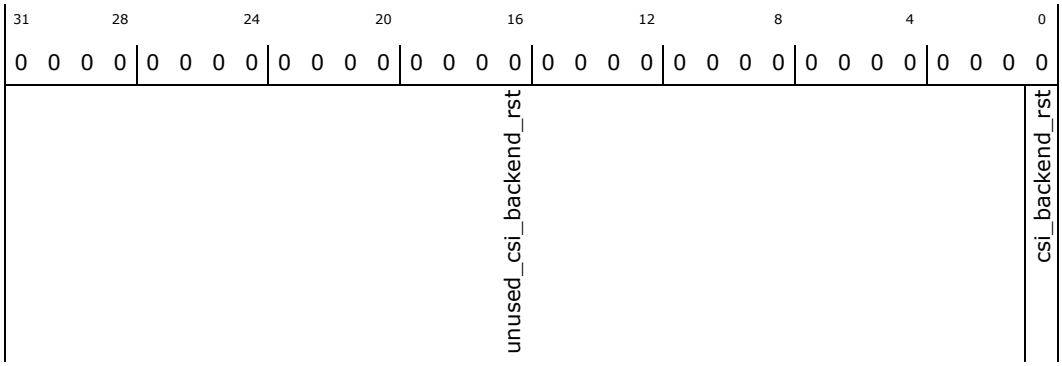
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80144h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_csi_backend_rst):** Unused
0	0x0 RW	**csi_backend_rst:** Reset CSI Rx backend block

5.3.17 csi_backend_comp_pred_reg0_vc0 (is_2400_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc0)—Offset 80148h

Compression and Prediction scheme register 0 for virtual channel 0

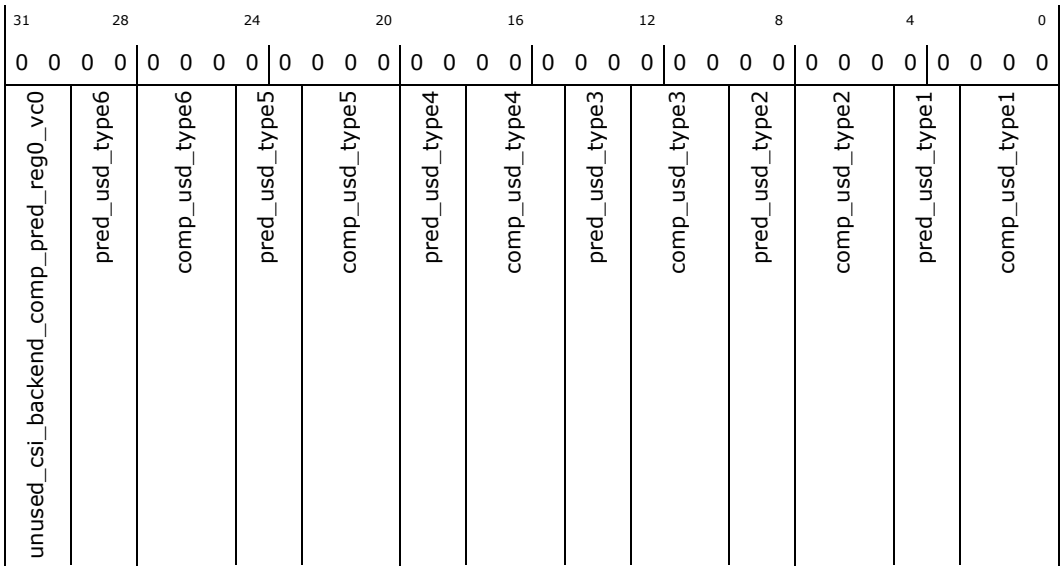
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80148h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved (unused_csi_backend_comp_pred_reg0_vc0):** Unused
29:28	0x0 RW	**pred_usd_type6:** prediction algorithm for user defined type 6 data: 1 -) pred1, 2 -) pred2
27:25	0x0 RW	**comp_usd_type6:** compression format for user defined type 6 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
24:23	0x0 RW	**pred_usd_type5:** prediction algorithm for user defined type 5 data: 1 -) pred1, 2 -) pred2
22:20	0x0 RW	**comp_usd_type5:** compression format for user defined type 5 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
19:18	0x0 RW	**pred_usd_type4:** prediction algorithm for user defined type 4 data: 1 -) pred1, 2 -) pred2

Bit Range	Default and Access	Field Name (ID): Description
17:15	0x0 RW	**comp_usd_type4:** compression format for user defined type 4 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
14:13	0x0 RW	**pred_usd_type3:** prediction algorithm for user defined type 3 data: 1 -) pred1, 2 -) pred2
12:10	0x0 RW	**comp_usd_type3:** compression format for user defined type 3 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
9:8	0x0 RW	**pred_usd_type2:** prediction algorithm for user defined type 2 data: 1 -) pred1, 2 -) pred2
7:5	0x0 RW	**comp_usd_type2:** compression format for user defined type 2 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
4:3	0x0 RW	**pred_usd_type1:** prediction algorithm for user defined type 1 data: 1 -) pred1, 2 -) pred2
2:0	0x0 RW	**comp_usd_type1:** compression format for user defined type 1 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.

5.3.18 csi_backend_comp_reg1_vc0 (is_2400_inp_sys_csi_receiver_csi_backend_comp_reg1_vc0)—Offset 8014Ch

Compression scheme register 1 for virtual channel 0

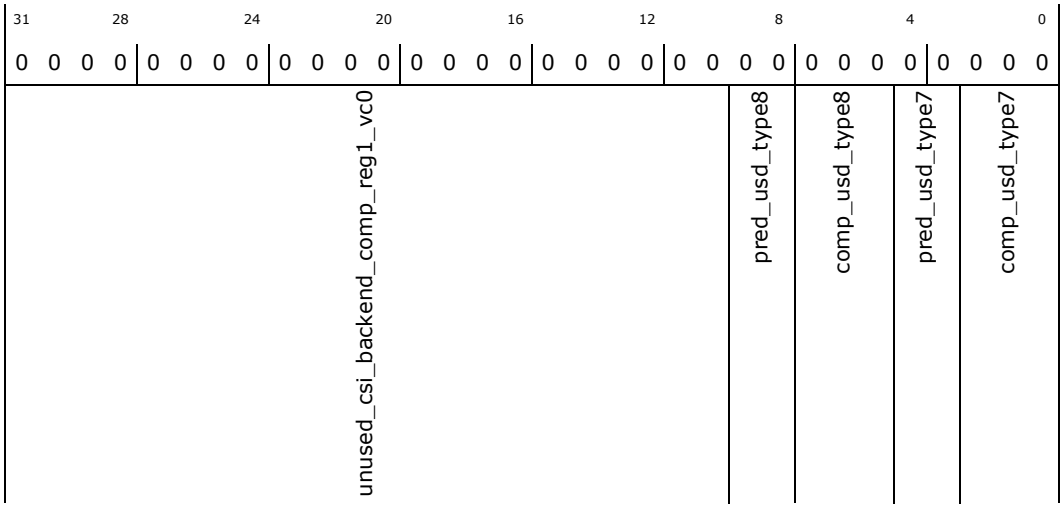
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8014Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:10	0x0 RO	**Reserved (unused_csi_backend_comp_reg1_vc0):** Unused
9:8	0x0 RW	**pred_usd_type8:** prediction algorithm for user defined type 8 data: 1 -) pred1, 2 -) pred2
7:5	0x0 RW	**comp_usd_type8:** compression format for user defined type 8 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
4:3	0x0 RW	**pred_usd_type7:** prediction algorithm for user defined type 7 data: 1 -) pred1, 2 -) pred2
2:0	0x0 RW	**comp_usd_type7:** compression format for user defined type 7 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.

5.3.19 csi_backend_comp_pred_reg0_vc1 (is_2400_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc1)—Offset 80150h

Compression and Prediction scheme register 0 for virtual channel 1

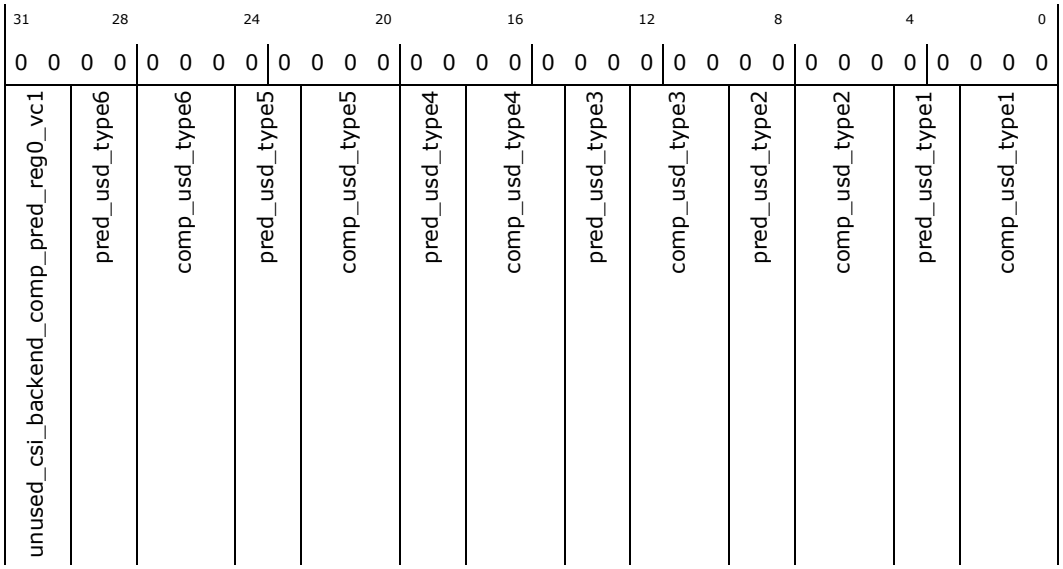
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80150h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved (unused_csi_backend_comp_pred_reg0_vc1):** Unused
29:28	0x0 RW	**pred_usd_type6:** prediction algorithm for user defined type 6 data: 1 -) pred1, 2 -) pred2
27:25	0x0 RW	**comp_usd_type6:** compression format for user defined type 6 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
24:23	0x0 RW	**pred_usd_type5:** prediction algorithm for user defined type 5 data: 1 -) pred1, 2 -) pred2
22:20	0x0 RW	**comp_usd_type5:** compression format for user defined type 5 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
19:18	0x0 RW	**pred_usd_type4:** prediction algorithm for user defined type 4 data: 1 -) pred1, 2 -) pred2
17:15	0x0 RW	**comp_usd_type4:** compression format for user defined type 4 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
14:13	0x0 RW	**pred_usd_type3:** prediction algorithm for user defined type 3 data: 1 -) pred1, 2 -) pred2
12:10	0x0 RW	**comp_usd_type3:** compression format for user defined type 3 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
9:8	0x0 RW	**pred_usd_type2:** prediction algorithm for user defined type 2 data: 1 -) pred1, 2 -) pred2
7:5	0x0 RW	**comp_usd_type2:** compression format for user defined type 2 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.

Bit Range	Default and Access	Field Name (ID): Description
4:3	0x0 RW	**pred_usd_type1:** prediction algorithm for user defined type 1 data: 1 -) pred1, 2 -) pred2
2:0	0x0 RW	**comp_usd_type1:** compression format for user defined type 1 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.

5.3.20 csi_backend_comp_reg1_vc1 (is_2400_inp_sys_csi_receiver_csi_backend_comp_reg1_vc1)—Offset 80154h

Compression scheme register 1 for virtual channel 1

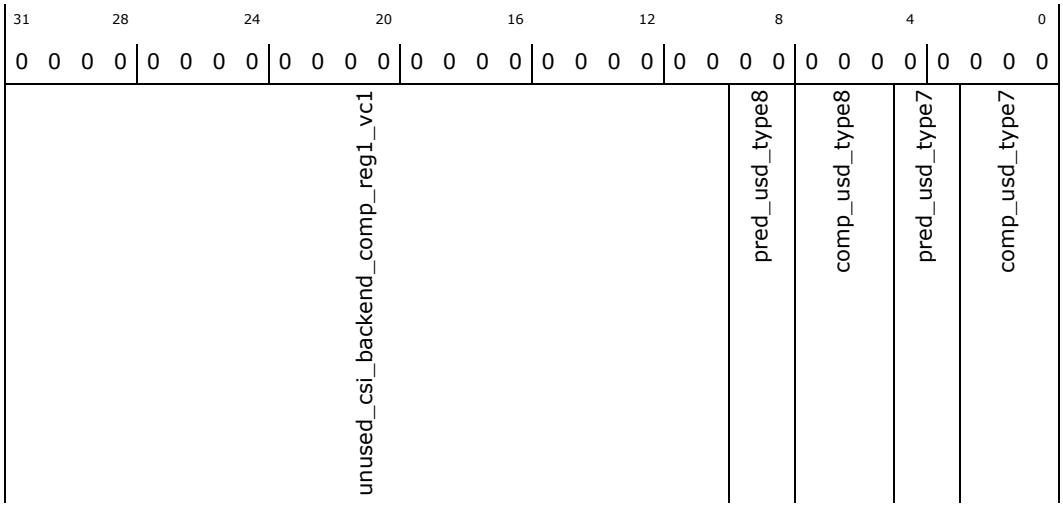
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80154h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:10	0x0 RO	**Reserved (unused_csi_backend_comp_reg1_vc1):** Unused
9:8	0x0 RW	**pred_usd_type8:** prediction algorithm for user defined type 8 data: 1 -) pred1, 2 -) pred2
7:5	0x0 RW	**comp_usd_type8:** compression format for user defined type 8 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.

Bit Range	Default and Access	Field Name (ID): Description
4:3	0x0 RW	**pred_usd_type7:** prediction algorithm for user defined type 7 data: 1 -) pred1, 2 -) pred2
2:0	0x0 RW	**comp_usd_type7:** compression format for user defined type 7 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.

5.3.21 csi_backend_comp_pred_reg0_vc2 (is_2400_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc2)—Offset 80158h

Compression and Prediction scheme register 0 for virtual channel 2

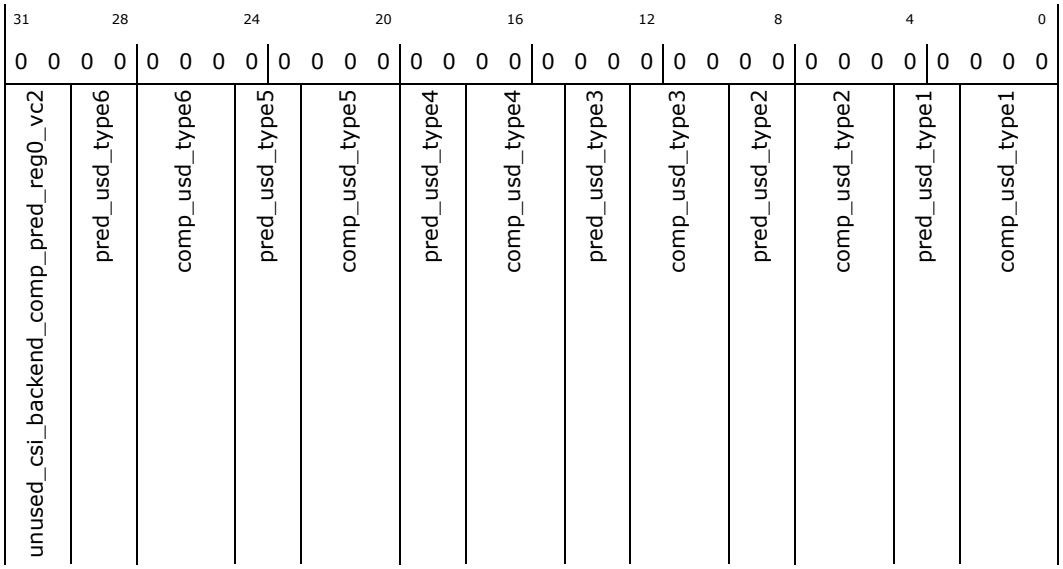
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

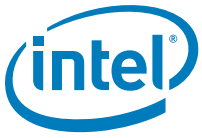
Offset: [ISPMMADR] + 80158h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved (unused_csi_backend_comp_pred_reg0_vc2):** Unused
29:28	0x0 RW	**pred_usd_type6:** prediction algorithm for user defined type 6 data: 1 -) pred1, 2 -) pred2



Bit Range	Default and Access	Field Name (ID): Description
27:25	0x0 RW	**comp_usd_type6:** compression format for user defined type 6 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
24:23	0x0 RW	**pred_usd_type5:** prediction algorithm for user defined type 5 data: 1 -) pred1, 2 -) pred2
22:20	0x0 RW	**comp_usd_type5:** compression format for user defined type 5 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
19:18	0x0 RW	**pred_usd_type4:** prediction algorithm for user defined type 4 data: 1 -) pred1, 2 -) pred2
17:15	0x0 RW	**comp_usd_type4:** compression format for user defined type 4 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
14:13	0x0 RW	**pred_usd_type3:** prediction algorithm for user defined type 3 data: 1 -) pred1, 2 -) pred2
12:10	0x0 RW	**comp_usd_type3:** compression format for user defined type 3 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
9:8	0x0 RW	**pred_usd_type2:** prediction algorithm for user defined type 2 data: 1 -) pred1, 2 -) pred2
7:5	0x0 RW	**comp_usd_type2:** compression format for user defined type 2 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
4:3	0x0 RW	**pred_usd_type1:** prediction algorithm for user defined type 1 data: 1 -) pred1, 2 -) pred2
2:0	0x0 RW	**comp_usd_type1:** compression format for user defined type 1 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.

5.3.22 csi_backend_comp_reg1_vc2 (is_2400_inp_sys_csi_receiver_csi_backend_comp_reg1_vc2)—Offset 8015Ch

Compression scheme register 1 for virtual channel 2

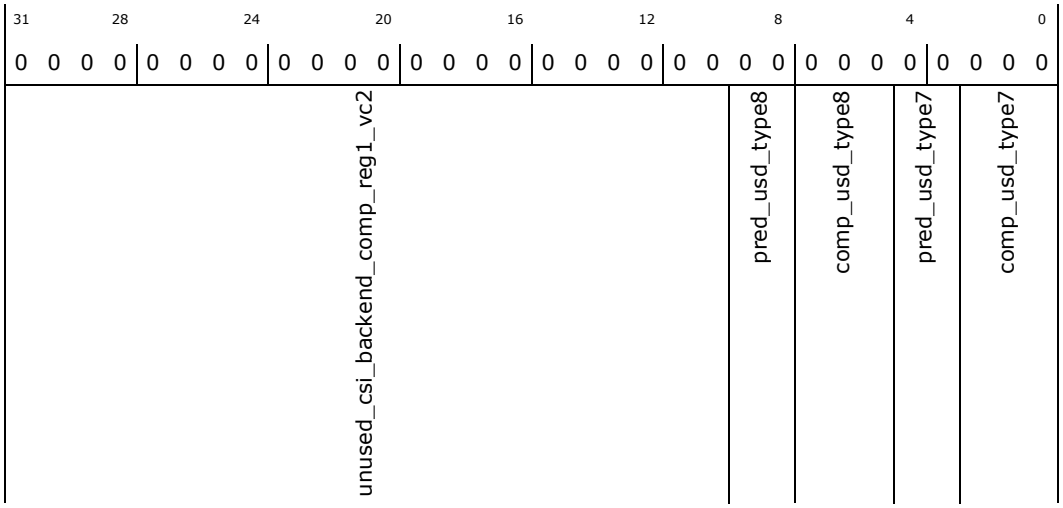
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8015Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:10	0x0 RO	**Reserved (unused_csi_backend_comp_reg1_vc2):** Unused
9:8	0x0 RW	**pred_usd_type8:** prediction algorithm for user defined type 8 data: 1 -) pred1, 2 -) pred2
7:5	0x0 RW	**comp_usd_type8:** compression format for user defined type 8 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
4:3	0x0 RW	**pred_usd_type7:** prediction algorithm for user defined type 7 data: 1 -) pred1, 2 -) pred2
2:0	0x0 RW	**comp_usd_type7:** compression format for user defined type 7 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.

5.3.23 csi_backend_comp_pred_reg0_vc3 (is_2400_inp_sys_csi_receiver_csi_backend_comp_pred_reg0_vc3)—Offset 80160h

Compression and Prediction scheme register 0 for virtual channel 3

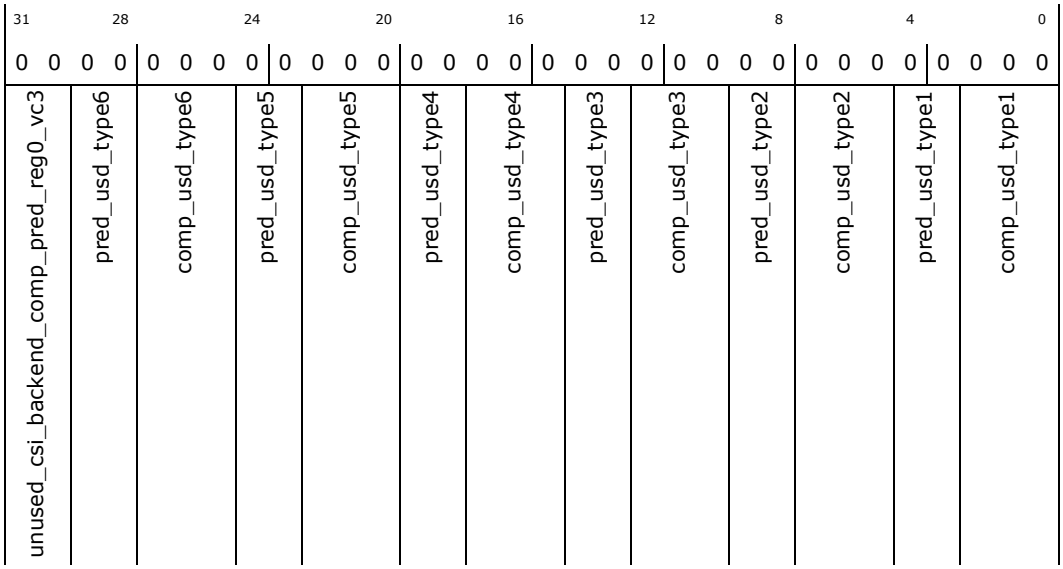
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80160h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved (unused_csi_backend_comp_pred_reg0_vc3):** Unused
29:28	0x0 RW	**pred_usd_type6:** prediction algorithm for user defined type 6 data: 1 -) pred1, 2 -) pred2
27:25	0x0 RW	**comp_usd_type6:** compression format for user defined type 6 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
24:23	0x0 RW	**pred_usd_type5:** prediction algorithm for user defined type 5 data: 1 -) pred1, 2 -) pred2
22:20	0x0 RW	**comp_usd_type5:** compression format for user defined type 5 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
19:18	0x0 RW	**pred_usd_type4:** prediction algorithm for user defined type 4 data: 1 -) pred1, 2 -) pred2
17:15	0x0 RW	**comp_usd_type4:** compression format for user defined type 4 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
14:13	0x0 RW	**pred_usd_type3:** prediction algorithm for user defined type 3 data: 1 -) pred1, 2 -) pred2
12:10	0x0 RW	**comp_usd_type3:** compression format for user defined type 3 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
9:8	0x0 RW	**pred_usd_type2:** prediction algorithm for user defined type 2 data: 1 -) pred1, 2 -) pred2
7:5	0x0 RW	**comp_usd_type2:** compression format for user defined type 2 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.

Bit Range	Default and Access	Field Name (ID): Description
4:3	0x0 RW	**pred_usd_type1:** prediction algorithm for user defined type 1 data: 1 -) pred1, 2 -) pred2
2:0	0x0 RW	**comp_usd_type1:** compression format for user defined type 1 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.

5.3.24 csi_backend_comp_reg1_vc3 (is_2400_inp_sys_csi_receiver_csi_backend_comp_reg1_vc3)—Offset 80164h

Compression scheme register 1 for virtual channel 3

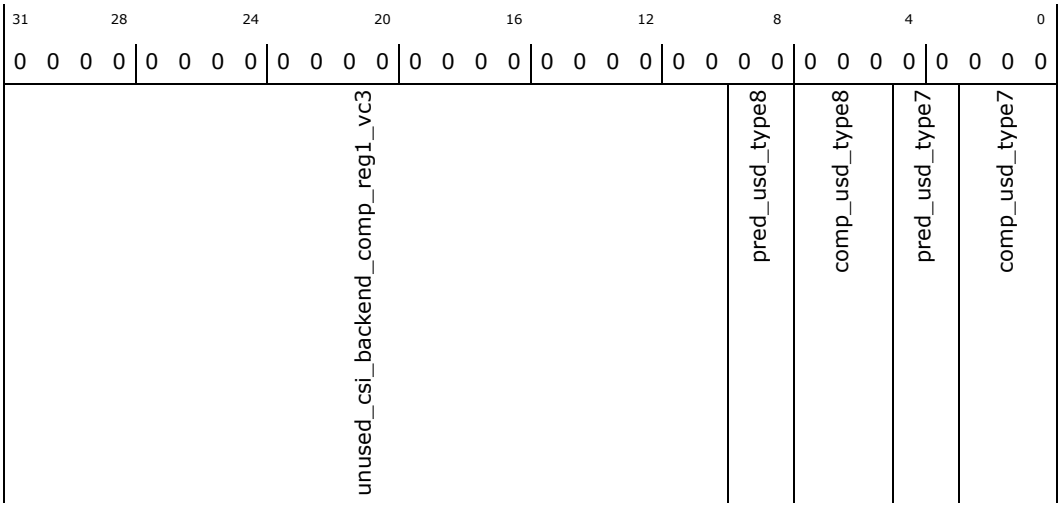
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80164h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:10	0x0 RO	**Reserved (unused_csi_backend_comp_reg1_vc3):** Unused
9:8	0x0 RW	**pred_usd_type8:** prediction algorithm for user defined type 8 data: 1 -) pred1, 2 -) pred2
7:5	0x0 RW	**comp_usd_type8:** compression format for user defined type 8 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.

Bit Range	Default and Access	Field Name (ID): Description
4:3	0x0 RW	**pred_usd_type7:** prediction algorithm for user defined type 7 data: 1 -) pred1, 2 -) pred2
2:0	0x0 RW	**comp_usd_type7:** compression format for user defined type 7 data: 000:Not Defined, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.

5.3.25 csi_backend_raw18_reg (is_2400_inp_sys_csi_receiver_csi_backend_raw18_reg) —Offset 80168h

Configuration register for RAW 18 data type decode

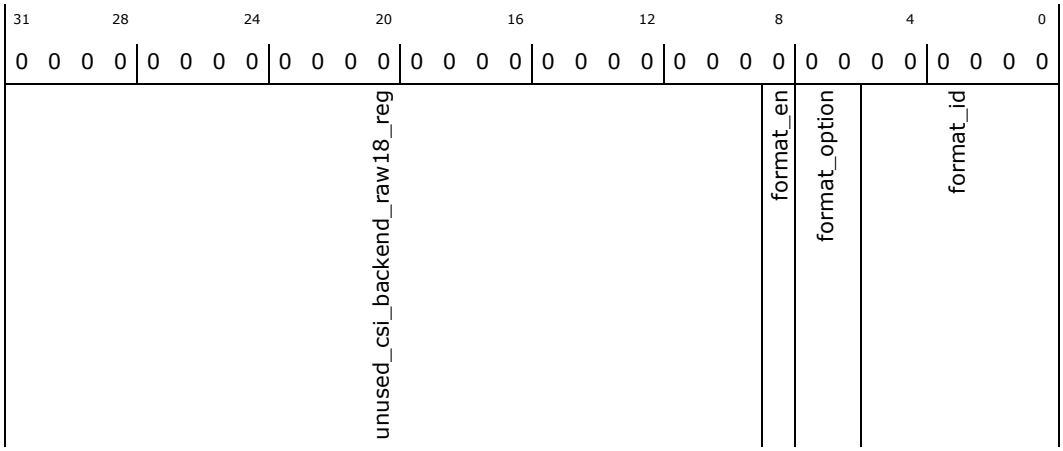
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80168h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:9	0x0 RO	**Reserved (unused_csi_backend_raw18_reg):** Unused
8	0x0 RW	**format_en:** enable RAW 18 type decode
7:6	0x0 RW	**format_option:** format option for RAW 18 data type: 3 options possible (1,2,3)
5:0	0x0 RW	**format_id:** data id for RAW 18

5.3.26 csi_backend_force_raw8_reg (is_2400_inp_sys_csi_receiver_csi_backend_force_raw8_reg)—Offset 8016Ch

Force RAW8(byte) decoding for LONG data packets

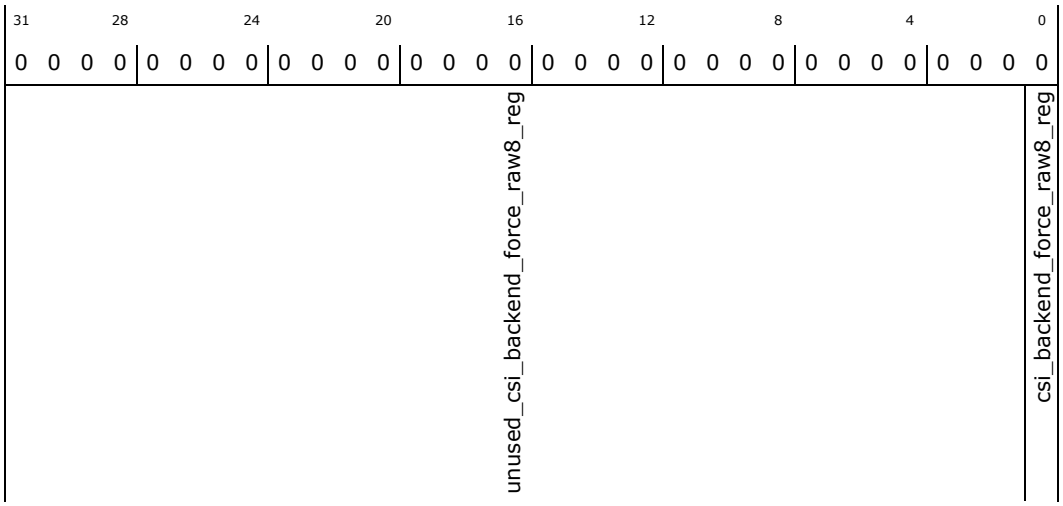
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8016Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_csi_backend_force_raw8_reg):** Unused
0	0x0 RW	**csi_backend_force_raw8_reg:** Force RAW8(byte) decoding for LONG data packets

5.3.27 csi_backend_raw16_reg (is_2400_inp_sys_csi_receiver_csi_backend_raw16_reg)—Offset 80170h

Configuration register for RAW 16 data type decode

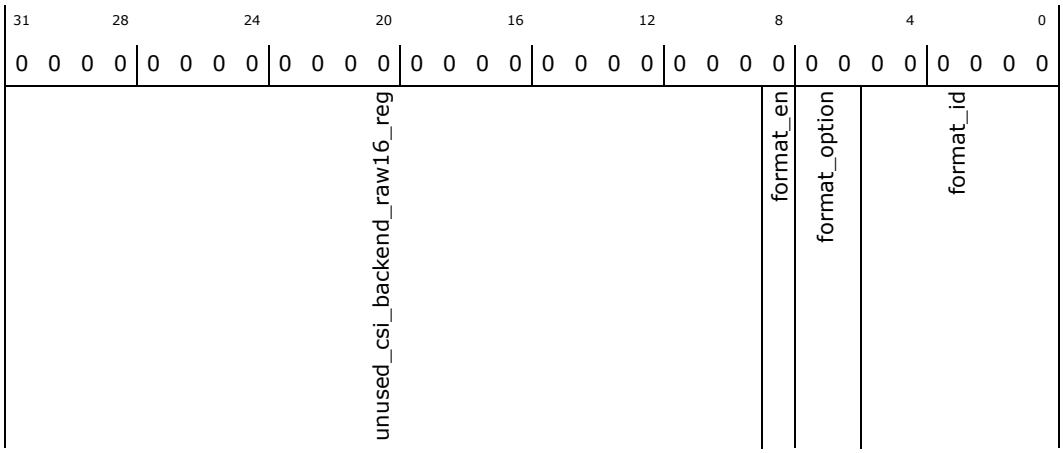
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80170h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:9	0x0 RO	**Reserved (unused_csi_backend_raw16_reg):** Unused
8	0x0 RW	**format_en:** enable RAW 16 type decode
7:6	0x0 RW	**format_option:** format option for RAW 16 data type: ONLY 1 option possible (1)
5:0	0x0 RW	**format_id:** data id for RAW 16

5.3.28 csi2_dev_ready (is_2400_inp_sys_csi_receiver_csi2_dev_ready)—Offset 80200h

Set after programming operational registers to enable receiver

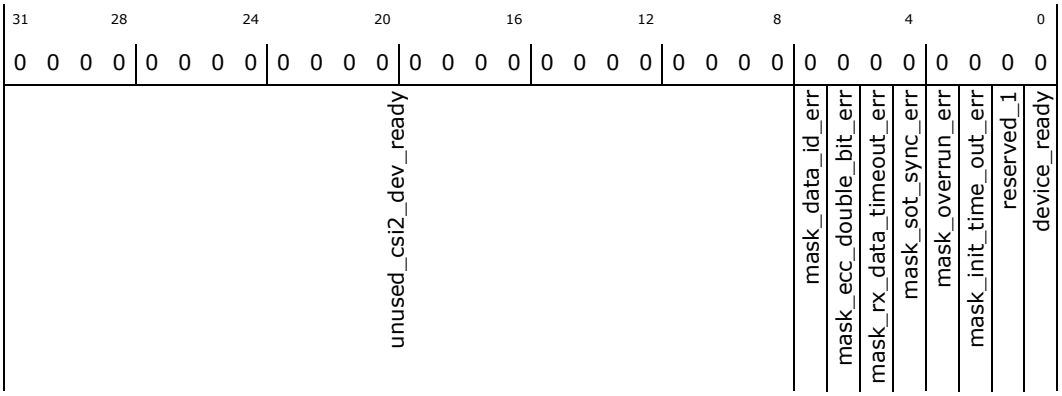
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (unused_csi2_dev_ready):** Unused
7	0x0 RW	**mask_data_id_err:** Set to mask error recovery when data ID error is detected
6	0x0 RW	**mask_ecc_double_bit_err:** Set to mask error recovery when ECC double bit error is detected
5	0x0 RW	**mask_rx_data_timeout_err:** Set to mask error recovery when receive data time out error is detected
4	0x0 RW	**mask_sot_sync_err:** Set to mask error recovery when start of transmission sync error is detected
3	0x0 RW	**mask_overrun_err:** set to mask overrun: NOT used now, can be discarded
2	0x0 RW	**mask_init_time_out_err:** Set to mask error recovery when initialization time out error is detected
1	0x0 RO	**reserved_1:** Reserved
0	0x0 RW	**device_ready:** Set to indicate that device is ready for reception

5.3.29 csi2_int_status (is_2400_inp_sys_csi_receiver_csi2_int_status)—Offset 80204h

Interrupt Status

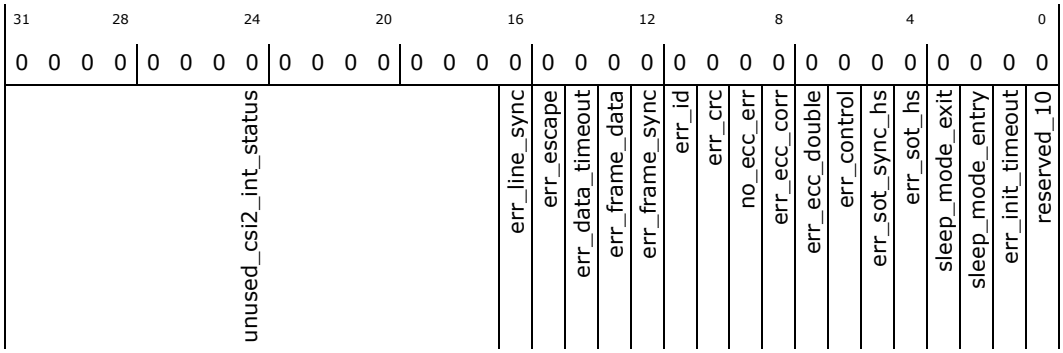
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80204h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (unused_csi2_int_status):** Unused
16	0x0 RW/1C	**err_line_sync:** Set if line number for line start and line end packets do not match
15	0x0 RW/1C	**err_escape:** Set if an unrecognized escape entry command is received
14	0x0 RW/1C	**err_data_timeout:** Set if time taken to receive a packet exceeds programmed timeout value
13	0x0 RW/1C	**err_frame_data:** Set if data packets within a frame has errors
12	0x0 RW/1C	**err_frame_sync:** Set if frame start is not paired with frame end for same virtual channel
11	0x0 RW/1C	**err_id:** Set if packet header has a recognized data id
10	0x0 RW/1C	**err_crc:** Set if computed CRC differs from received value
9	0x0 RW/1C	**no_ecc_err:** Set if no ECC error detected in packet
8	0x0 RW/1C	**err_ecc_corr:** Set if ECC error detected and corrected for one bit
7	0x0 RW/1C	**err_ecc_double:** Set if ECC error detected for two or more bits
6	0x0 RW/1C	**err_control:** Set if DPHY flags a control error
5	0x0 RW/1C	**err_sot_sync_hs:** Set if DPHY flags start of transmission synchronisation error
4	0x0 RW/1C	**err_sot_hs:** Set if DPHY flags start of transmission error
3	0x0 RW/1C	**sleep_mode_exit:** Set if DPHY exits ultra low power state
2	0x0 RW/1C	**sleep_mode_entry:** Set if DPHY enters ultra low power state

Bit Range	Default and Access	Field Name (ID): Description
1	0x0 RW/1C	**err_init_timeout:** Set if Initialization timeout error occurs on DPHY data lanes
0	0x0 RO	**reserved_10:** Always set to 0

5.3.30 csi2_int_enable (is_2400_inp_sys_csi_receiver_csi2_int_enable)—Offset 80208h

Interrupt Enable

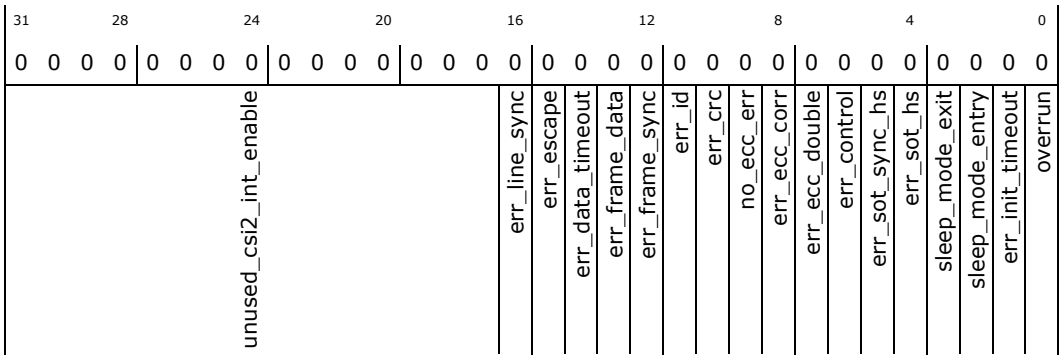
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80208h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (unused_csi2_int_enable):** Unused
16	0x0 RW	**err_line_sync:** Enable line sync error interrupt
15	0x0 RW	**err_escape:** Enable escape entry error interrupt
14	0x0 RW	**err_data_timeout:** Enable timeout error interrupt
13	0x0 RW	**err_frame_data:** Enable frame data error interrupt
12	0x0 RW	**err_frame_sync:** Enable frame sync error interrupt

Bit Range	Default and Access	Field Name (ID): Description
11	0x0 RW	**err_id:** Enable data id error interrupt
10	0x0 RW	**err_crc:** Enable CRC error interrupt
9	0x0 RW	**no_ecc_err:** Enable no ECC error interrupt
8	0x0 RW	**err_ecc_corr:** Enable ECC error detected and corrected for one bit interrupt
7	0x0 RW	**err_ecc_double:** Enable ECC error detected for two or more bits interrupt
6	0x0 RW	**err_control:** Enable control error interrupt
5	0x0 RW	**err_sot_sync_hs:** Enable start of transmission synchronisation error interrupt
4	0x0 RW	**err_sot_hs:** Enable start of transmission error interrupt
3	0x0 RW	**sleep_mode_exit:** Enable sleep mode exit interrupt
2	0x0 RW	**sleep_mode_entry:** Enable sleep mode entry interrupt
1	0x0 RW	**err_init_timeout:** Enable Initialization timeout error interrupt
0	0x0 RW	**overrun:** Not used

5.3.31 csi2_func_prg (is_2400_inp_sys_csi_receiver_csi2_func_prg)—Offset 8020Ch

Functional Programming CSI2

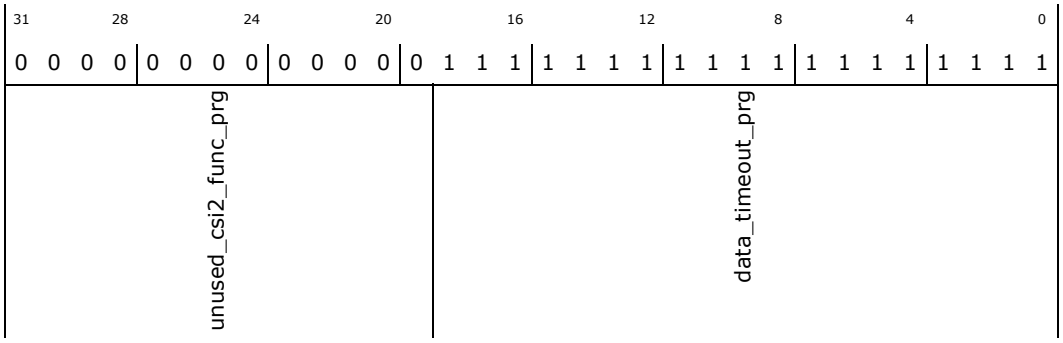
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8020Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0007FFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:19	0x0 RO	**Reserved (unused_csi2_func_prg):** Unused
18:0	0x7ffff RW	**data_timeout_prg:** Data timeout value to be checked for long packets

5.3.32 csi2_init_cnt (is_2400_inp_sys_csi_receiver_csi2_init_cnt)—Offset 80210h

Duration after power up when DPHY lanes will not be observed

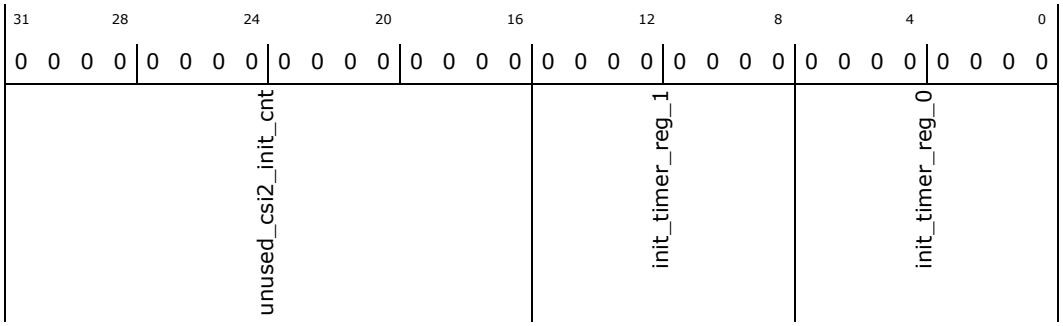
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80210h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (unused_csi2_init_cnt):** Unused

Bit Range	Default and Access	Field Name (ID): Description
15:8	0x0 RW	**init_timer_reg_1:** Byte 1 for power up timer
7:0	0x0 RW	**init_timer_reg_0:** Byte 0 for power up timer

5.3.33 csi2_raw16_18_data_id (is_2400_inp_sys_csi_receiver_csi2_raw16_18_data_id) —Offset 80238h

RAW 16 and RAW 18 data ID register

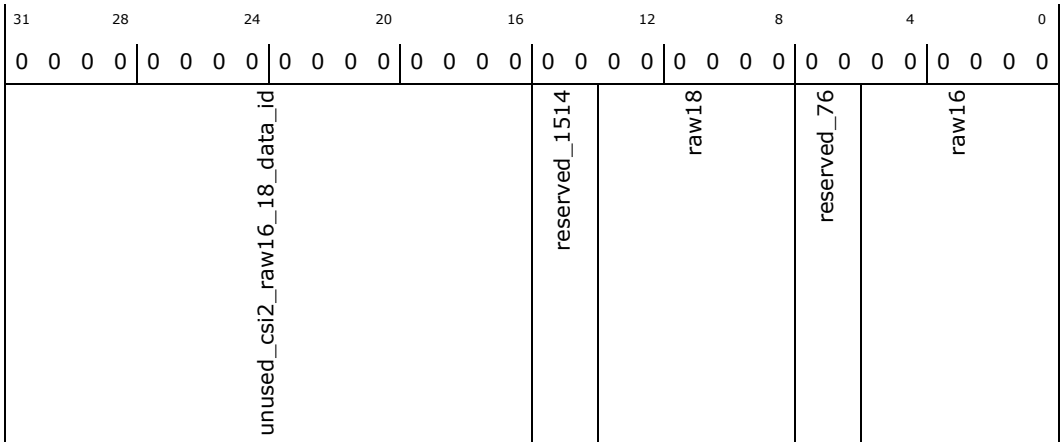
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80238h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (unused_csi2_raw16_18_data_id):** Unused
15:14	0x0 RO	**reserved_1514:** Reserved
13:8	0x0 RW	**raw18:** 6 bit format id value for RAW 18. If CSI receiver backend receives a packet with this format id, it will unpack it as RAW 18 data
7:6	0x0 RO	**reserved_76:** Reserved
5:0	0x0 RW	**raw16:** 6 bit format id value for RAW 16. If CSI receiver backend receives a packet with this format id, it will unpack it as RAW 16 data

5.3.34 csi2_sync_cnt (is_2400_inp_sys_csi_receiver_csi2_sync_cnt)—Offset 8023Ch

Synchronisation count value in terms of MIPI high speed byte clock

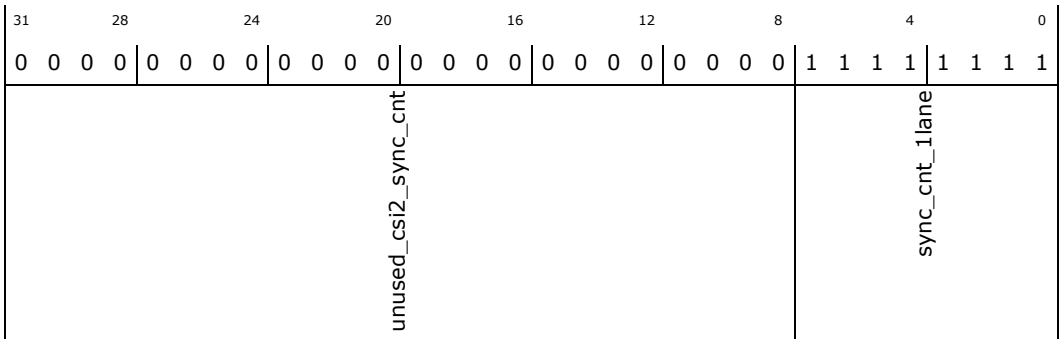
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8023Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 000000FFh



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (unused_csi2_sync_cnt):** Unused
7:0	0xff RW	**sync_cnt_1lane:** Synchronisation count value for 1 lane

5.3.35 csi2_rx_cnt (is_2400_inp_sys_csi_receiver_csi2_rx_cnt)—Offset 80240h

Receive count value in terms of MIPI high speed byte clock

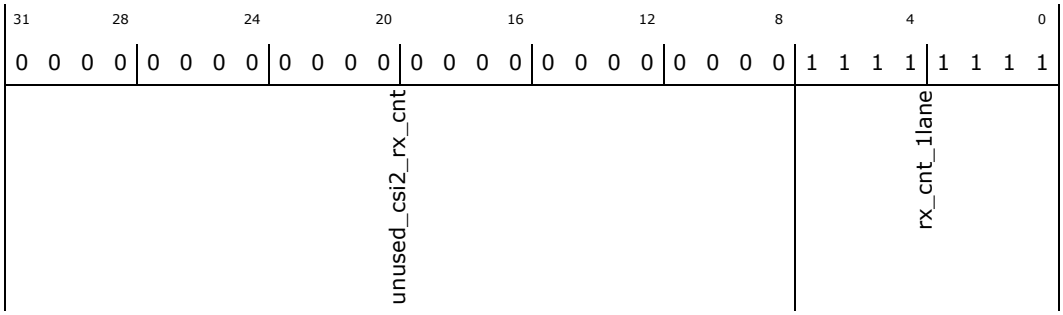
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80240h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 000000FFh



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (unused_csi2_rx_cnt):** Unused
7:0	0xff RW	**rx_cnt_1lane:** Receive count value for lane 1. Controls the number of MIPI high speed clock cycles between LP-00 state detection and enabling of high speed receiver

5.3.36 csi3_dev_ready (is_2400_inp_sys_csi_receiver_csi3_dev_ready)—Offset 80300h

Set after programming operational registers to enable receiver

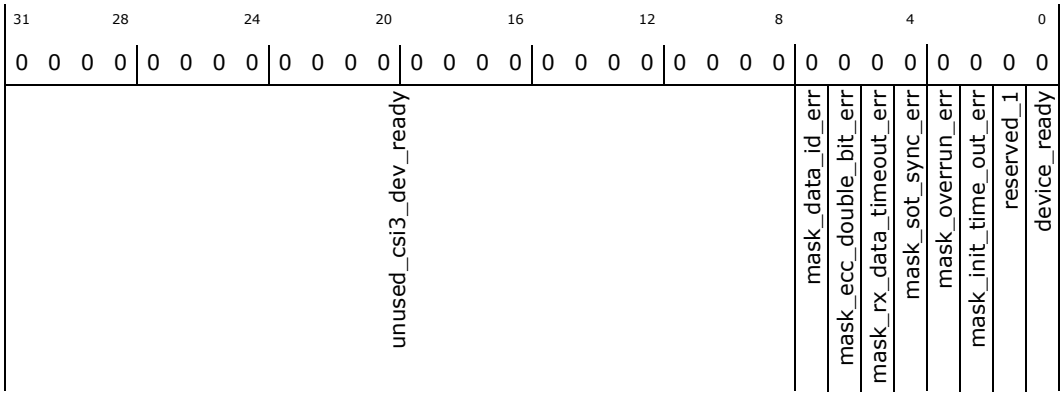
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80300h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (unused_csi3_dev_ready):** Unused
7	0x0 RW	**mask_data_id_err:** Set to mask error recovery when data ID error is detected
6	0x0 RW	**mask_ecc_double_bit_err:** Set to mask error recovery when ECC double bit error is detected
5	0x0 RW	**mask_rx_data_timeout_err:** Set to mask error recovery when receive data time out error is detected
4	0x0 RW	**mask_sot_sync_err:** Set to mask error recovery when start of transmission sync error is detected
3	0x0 RW	**mask_overrun_err:** set to mask overrun: NOT used now, can be discarded
2	0x0 RW	**mask_init_time_out_err:** Set to mask error recovery when initialization time out error is detected
1	0x0 RO	**reserved_1:** Reserved
0	0x0 RW	**device_ready:** Set to indicate that device is ready for reception

5.3.37 csi3_int_status (is_2400_inp_sys_csi_receiver_csi3_int_status)—Offset 80304h

Interrupt Status

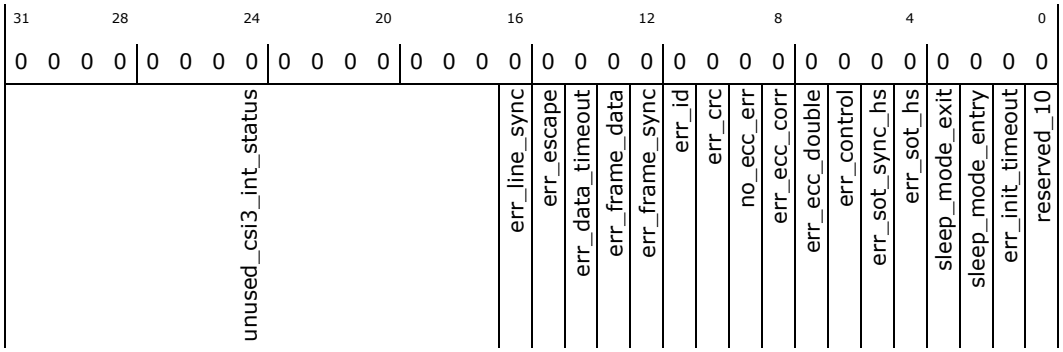
Access Method

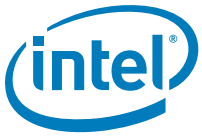
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80304h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h





Bit Range	Default and Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (unused_csi3_int_status):** Unused
16	0x0 RW/1C	**err_line_sync:** Set if line number for line start and line end packets do not match
15	0x0 RW/1C	**err_escape:** Set if an recognized escape entry command is received
14	0x0 RW/1C	**err_data_timeout:** Set if time taken to receive a packet exceeds programmed timeout value
13	0x0 RW/1C	**err_frame_data:** Set if data packets within a frame has errors
12	0x0 RW/1C	**err_frame_sync:** Set if frame start is not paired with frame end for same virtual channel
11	0x0 RW/1C	**err_id:** Set if packet header has a recognized data id
10	0x0 RW/1C	**err_crc:** Set if computed CRC differs from received value
9	0x0 RW/1C	**no_ecc_err:** Set if no ECC error detected in packet
8	0x0 RW/1C	**err_ecc_corr:** Set if ECC error detected and corrected for one bit
7	0x0 RW/1C	**err_ecc_double:** Set if ECC error detected for two or more bits
6	0x0 RW/1C	**err_control:** Set if DPHY flags a control error
5	0x0 RW/1C	**err_sot_sync_hs:** Set if DPHY flags start of transmission synchronisation error
4	0x0 RW/1C	**err_sot_hs:** Set if DPHY flags start of transmission error
3	0x0 RW/1C	**sleep_mode_exit:** Set if DPHY exits ultra low power state
2	0x0 RW/1C	**sleep_mode_entry:** Set if DPHY enters ultra low power state
1	0x0 RW/1C	**err_init_timeout:** Set if Initialization timeout error occurs on DPHY data lanes
0	0x0 RO	**reserved_10:** Always set to 0

5.3.38 csi3_int_enable (is_2400_inp_sys_csi_receiver_csi3_int_enable)—Offset 80308h

Interrupt Enable

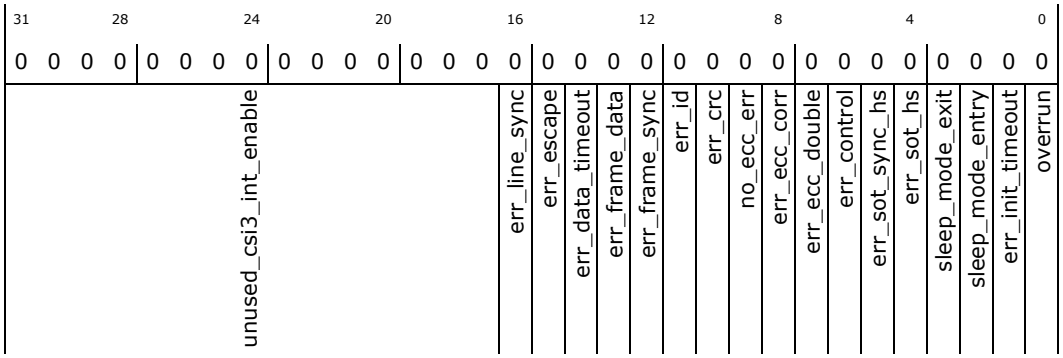
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80308h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (unused_csi3_int_enable):** Unused
16	0x0 RW	**err_line_sync:** Enable line sync error interrupt
15	0x0 RW	**err_escape:** Enable escape entry error interrupt
14	0x0 RW	**err_data_timeout:** Enable timeout error interrupt
13	0x0 RW	**err_frame_data:** Enable frame data error interrupt
12	0x0 RW	**err_frame_sync:** Enable frame sync error interrupt
11	0x0 RW	**err_id:** Enable data id error interrupt
10	0x0 RW	**err_crc:** Enable CRC error interrupt
9	0x0 RW	**no_ecc_err:** Enable no ECC error interrupt
8	0x0 RW	**err_ecc_corr:** Enable ECC error detected and corrected for one bit interrupt
7	0x0 RW	**err_ecc_double:** Enable ECC error detected for two or more bits interrupt
6	0x0 RW	**err_control:** Enable control error interrupt
5	0x0 RW	**err_sot_sync_hs:** Enable start of transmission synchronisation error interrupt
4	0x0 RW	**err_sot_hs:** Enable start of transmission error interrupt

Bit Range	Default and Access	Field Name (ID): Description
3	0x0 RW	**sleep_mode_exit:** Enable sleep mode exit interrupt
2	0x0 RW	**sleep_mode_entry:** Enable sleep mode entry interrupt
1	0x0 RW	**err_init_timeout:** Enable Initialization timeout error interrupt
0	0x0 RW	**overrun:** Not used

5.3.39 csi3_func_prg (is_2400_inp_sys_csi_receiver_csi3_func_prg)—Offset 8030Ch

Functional Programming CSI3

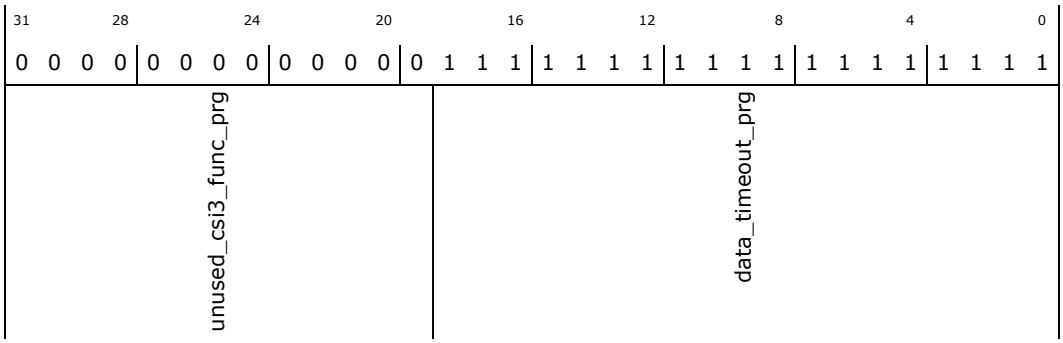
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8030Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0007FFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:19	0x0 RO	**Reserved (unused_csi3_func_prg):** Unused
18:0	0x7ffff RW	**data_timeout_prg:** Data timeout value to be checked for long packets

5.3.40 csi3_init_cnt (is_2400_inp_sys_csi_receiver_csi3_init_cnt)—Offset 80310h

Duration after power up when DPHY lanes will not be observed

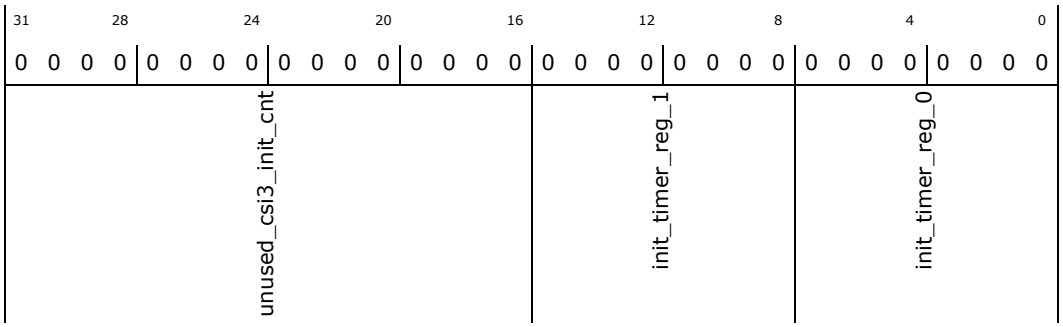
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80310h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (unused_csi3_init_cnt):** Unused
15:8	0x0 RW	**init_timer_reg_1:** Byte 1 for power up timer
7:0	0x0 RW	**init_timer_reg_0:** Byte 0 for power up timer

5.3.41 csi3_raw16_18_data_id (is_2400_inp_sys_csi_receiver_csi3_raw16_18_data_id)—Offset 80338h

RAW 16 and RAW 18 data ID register

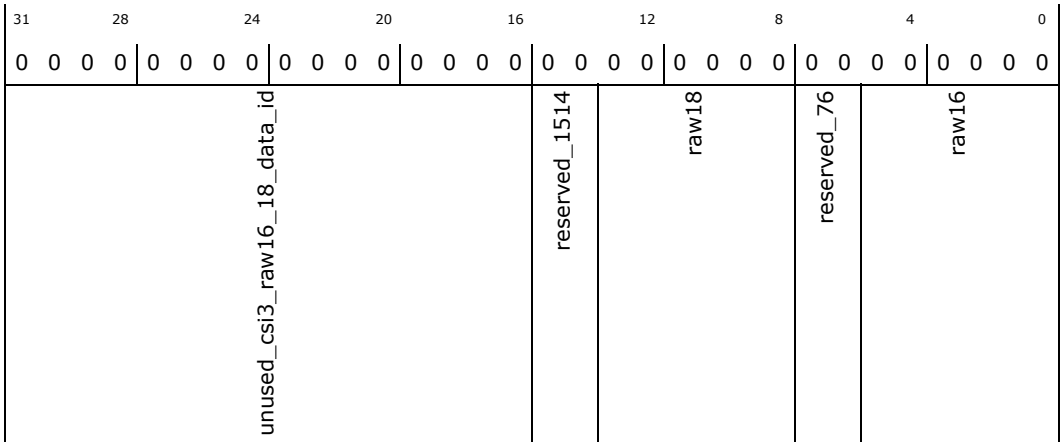
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80338h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (unused_csi3_raw16_18_data_id):** Unused
15:14	0x0 RO	**reserved_1514:** Reserved
13:8	0x0 RW	**raw18:** 6 bit format id value for RAW 18. If CSI receiver backend receives a packet with this format id, it will unpack it as RAW 18 data
7:6	0x0 RO	**reserved_76:** Reserved
5:0	0x0 RW	**raw16:** 6 bit format id value for RAW 16. If CSI receiver backend receives a packet with this format id, it will unpack it as RAW 16 data

5.3.42 csi3_sync_cnt (is_2400_inp_sys_csi_receiver_csi3_sync_cnt)—Offset 8033Ch

Synchronisation count value in terms of MIPI high speed byte clock

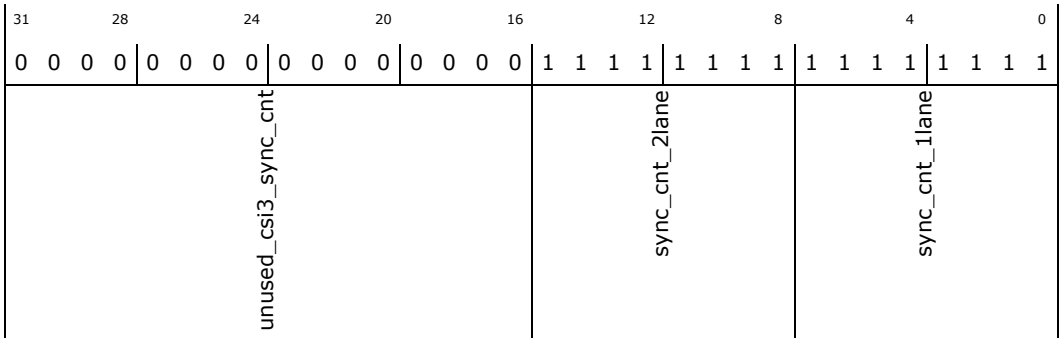
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8033Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000FFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (unused_csi3_sync_cnt):** Unused
15:8	0xff RW	**sync_cnt_2lane:** Synchronisation count value for 2 lane
7:0	0xff RW	**sync_cnt_1lane:** Synchronisation count value for 1 lane

5.3.43 csi3_rx_cnt (is_2400_inp_sys_csi_receiver_csi3_rx_cnt)—Offset 80340h

Receive count value in terms of MIPI high speed byte clock

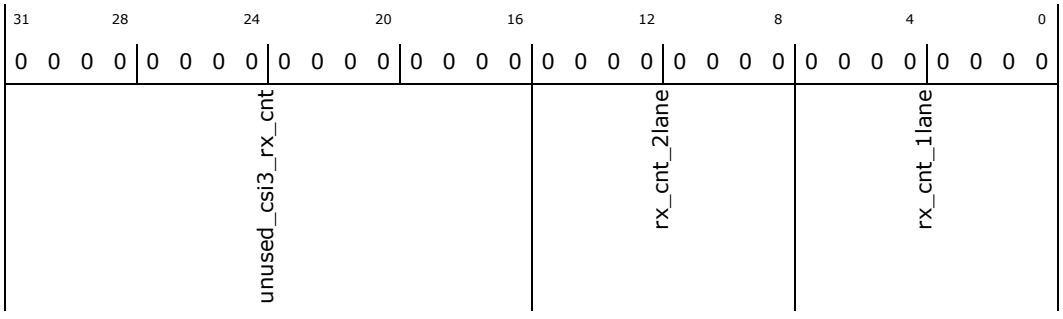
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80340h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (unused_csi3_rx_cnt):** Unused
15:8	0x0 RW	**rx_cnt_2lane:** Receive count value for lane 2. Controls the number of MIPI high speed clock cycles between LP-00 state detection and enabling of high speed receiver
7:0	0x0 RW	**rx_cnt_1lane:** Receive count value for lane 1. Controls the number of MIPI high speed clock cycles between LP-00 state detection and enabling of high speed receiver

5.3.44 csi_be_gen_sh_acc_ovl (is_2400_inp_sys_csi_receiver_csi_be_gen_sh_acc_ovl) —Offset 80800h

Allows for overruling the accept signal generated by the generic short packet FIFO, going to the CSI receiver backend.

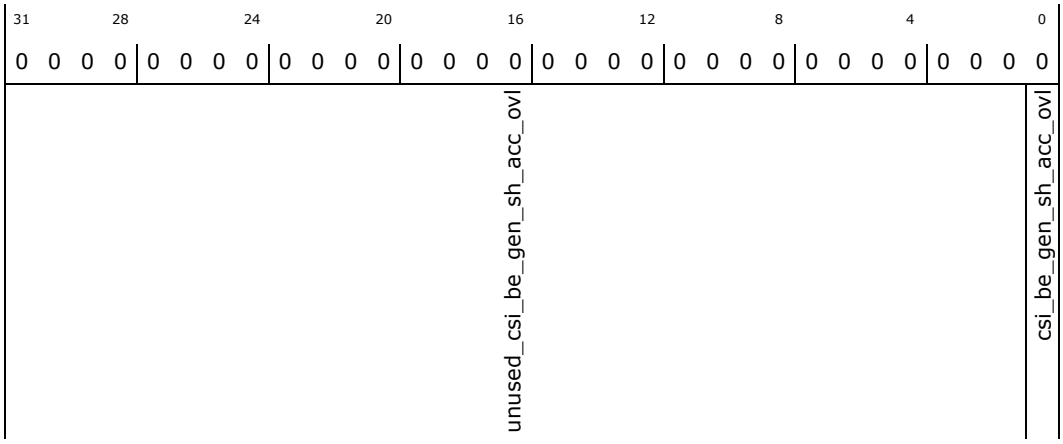
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80800h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_csi_be_gen_sh_acc_ovl):** Unused
0	0x0 RW	**csi_be_gen_sh_acc_ovl:** Allows for overruling the accept signal generated by the generic short packet FIFO, going to the CSI receiver backend.

5.3.45 csi_sh_be_srst (is_2400_inp_sys_csi_receiver_csi_sh_be_srst)—Offset 80804h

soft reset modules of the SH CSI receiver Back End

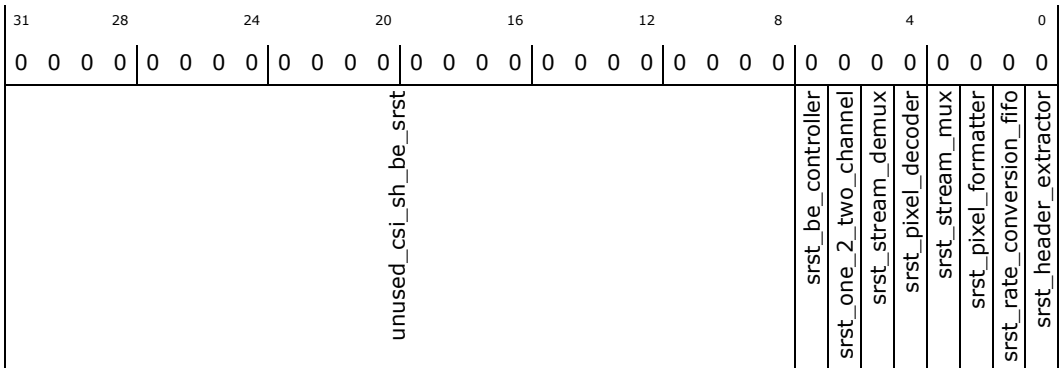
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80804h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (unused_csi_sh_be_srst):** Unused
7	0x0 RW	**srst_be_controller:** Soft resets the backend controller module
6	0x0 RW	**srst_one_2_two_channel:** Soft resets the one 2 two channel module
5	0x0 RW	**srst_stream_demux:** Soft resets the stream demux module
4	0x0 RW	**srst_pixel_decoder:** Soft resets the pixel decoder module
3	0x0 RW	**srst_stream_mux:** Soft resets the stream mux module
2	0x0 RW	**srst_pixel_formatter:** Soft resets the pixel formatter module
1	0x0 RW	**srst_rate_conversion_fifo:** Soft resets the rate conversion FIFO module
0	0x0 RW	**srst_header_extractor:** Soft resets the header extractor module

5.3.46 csi_sh_be_two_ppc (is_2400_inp_sys_csi_receiver_csi_sh_be_two_ppc)—Offset 80808h

Sets the output rate of the backend and the precision

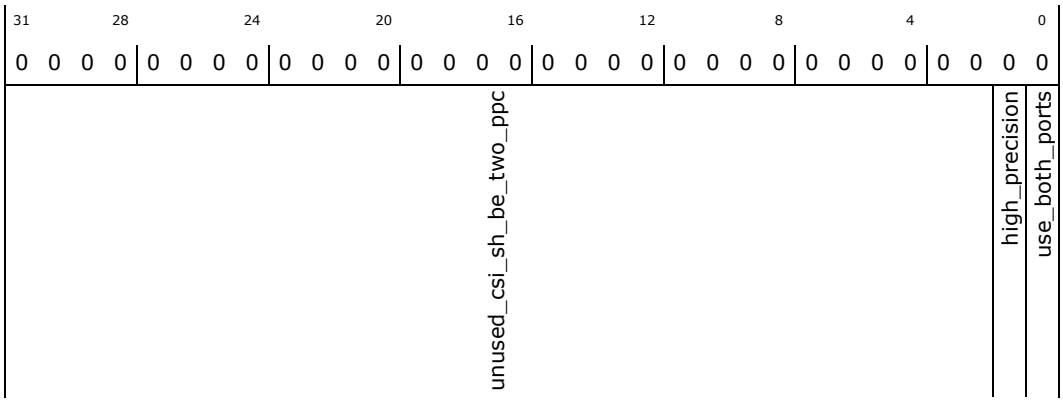
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80808h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved (unused_csi_sh_be_two_ppc):** Unused
1	0x0 RW	**high_precision:** When '1', (and use_both_ports='1' as well) both ports A and B are used to output one high precision pixel, when '0', high_precision pixels are saturated to fit on one port.
0	0x0 RW	**use_both_ports:** When '1', both ports A and B are active. When '0' only port A is active

5.3.47 csi_sh_be_comp_reg_vc0 (is_2400_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc0)—Offset 8080Ch

Compression scheme register for virtual channel 0

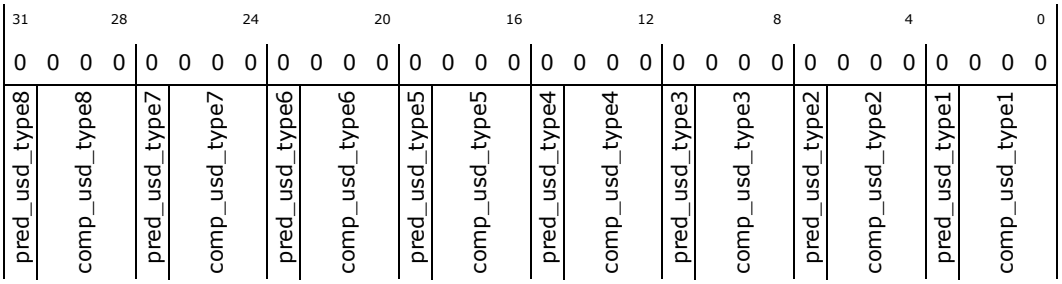
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8080Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**pred_usd_type8:** prediction algorithm for vc=0, user defined type 8 data: 0 -) pred1, 1 -) pred2
30:28	0x0 RW	**comp_usd_type8:** compression format for vc=0, user defined type 8 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
27	0x0 RW	**pred_usd_type7:** prediction algorithm for vc=0, user defined type 7 data: 0 -) pred1, 1 -) pred2
26:24	0x0 RW	**comp_usd_type7:** compression format for vc=0, user defined type 7 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
23	0x0 RW	**pred_usd_type6:** prediction algorithm for vc=0, user defined type 6 data: 0 -) pred1, 1 -) pred2
22:20	0x0 RW	**comp_usd_type6:** compression format for vc=0, user defined type 6 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
19	0x0 RW	**pred_usd_type5:** prediction algorithm for vc=0, user defined type 5 data: 0 -) pred1, 1 -) pred2
18:16	0x0 RW	**comp_usd_type5:** compression format for vc=0, user defined type 5 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
15	0x0 RW	**pred_usd_type4:** prediction algorithm for vc=0, user defined type 4 data: 0 -) pred1, 1 -) pred2
14:12	0x0 RW	**comp_usd_type4:** compression format for vc=0, user defined type 4 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
11	0x0 RW	**pred_usd_type3:** prediction algorithm for vc=0, user defined type 3 data: 0 -) pred1, 1 -) pred2
10:8	0x0 RW	**comp_usd_type3:** compression format for vc=0, user defined type 3 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
7	0x0 RW	**pred_usd_type2:** prediction algorithm for vc=0, user defined type 2 data: 0 -) pred1, 1 -) pred2
6:4	0x0 RW	**comp_usd_type2:** compression format for vc=0, user defined type 2 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.

Bit Range	Default and Access	Field Name (ID): Description
3	0x0 RW	**pred_usd_type1:** prediction algorithm for vc=0, user defined type 1 data: 0 -) pred1, 1 -) pred2
2:0	0x0 RW	**comp_usd_type1:** compression format for vc=0, user defined type 1 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.

5.3.48 csi_sh_be_comp_reg_vc1 (is_2400_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc1)—Offset 80810h

Compression scheme register for virtual channel 1

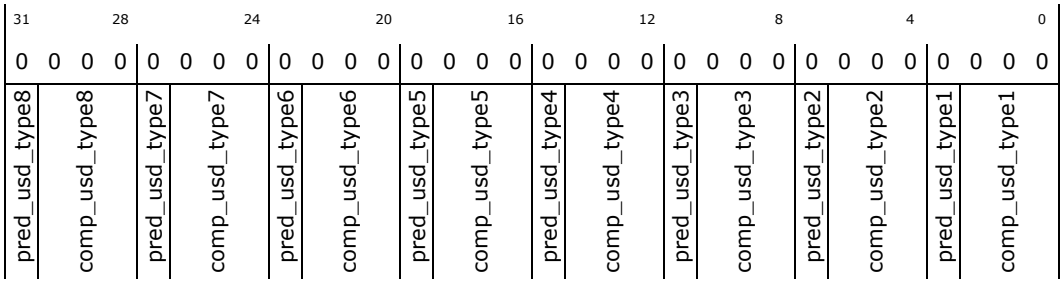
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80810h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**pred_usd_type8:** prediction algorithm for vc=1, user defined type 8 data: 0 -) pred1, 1 -) pred2
30:28	0x0 RW	**comp_usd_type8:** compression format for vc=1, user defined type 8 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
27	0x0 RW	**pred_usd_type7:** prediction algorithm for vc=1, user defined type 7 data: 0 -) pred1, 1 -) pred2
26:24	0x0 RW	**comp_usd_type7:** compression format for vc=1, user defined type 7 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
23	0x0 RW	**pred_usd_type6:** prediction algorithm for vc=1, user defined type 6 data: 0 -) pred1, 1 -) pred2

Bit Range	Default and Access	Field Name (ID): Description
22:20	0x0 RW	**comp_usd_type6:** compression format for vc=1, user defined type 6 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
19	0x0 RW	**pred_usd_type5:** prediction algorithm for vc=1, user defined type 5 data: 0 -) pred1, 1 -) pred2
18:16	0x0 RW	**comp_usd_type5:** compression format for vc=1, user defined type 5 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
15	0x0 RW	**pred_usd_type4:** prediction algorithm for vc=1, user defined type 4 data: 0 -) pred1, 1 -) pred2
14:12	0x0 RW	**comp_usd_type4:** compression format for vc=1, user defined type 4 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
11	0x0 RW	**pred_usd_type3:** prediction algorithm for vc=1, user defined type 3 data: 0 -) pred1, 1 -) pred2
10:8	0x0 RW	**comp_usd_type3:** compression format for vc=1, user defined type 3 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
7	0x0 RW	**pred_usd_type2:** prediction algorithm for vc=1, user defined type 2 data: 0 -) pred1, 1 -) pred2
6:4	0x0 RW	**comp_usd_type2:** compression format for vc=1, user defined type 2 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
3	0x0 RW	**pred_usd_type1:** prediction algorithm for vc=1, user defined type 1 data: 0 -) pred1, 1 -) pred2
2:0	0x0 RW	**comp_usd_type1:** compression format for vc=1, user defined type 1 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.

5.3.49 csi_sh_be_comp_reg_vc2 (is_2400_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc2)—Offset 80814h

Compression scheme register for virtual channel 0

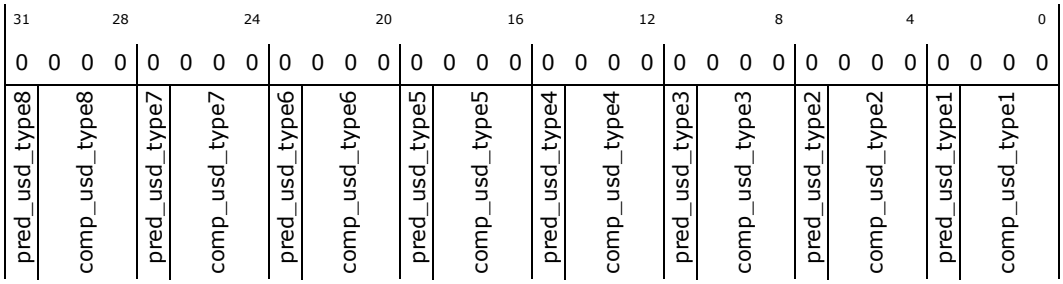
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80814h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**pred_usd_type8:** prediction algorithm for vc=2, user defined type 8 data: 0 -) pred1, 1 -) pred2
30:28	0x0 RW	**comp_usd_type8:** compression format for vc=2, user defined type 8 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
27	0x0 RW	**pred_usd_type7:** prediction algorithm for vc=2, user defined type 7 data: 0 -) pred1, 1 -) pred2
26:24	0x0 RW	**comp_usd_type7:** compression format for vc=2, user defined type 7 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
23	0x0 RW	**pred_usd_type6:** prediction algorithm for vc=2, user defined type 6 data: 0 -) pred1, 1 -) pred2
22:20	0x0 RW	**comp_usd_type6:** compression format for vc=2, user defined type 6 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
19	0x0 RW	**pred_usd_type5:** prediction algorithm for vc=2, user defined type 5 data: 0 -) pred1, 1 -) pred2
18:16	0x0 RW	**comp_usd_type5:** compression format for vc=2, user defined type 5 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
15	0x0 RW	**pred_usd_type4:** prediction algorithm for vc=2, user defined type 4 data: 0 -) pred1, 1 -) pred2
14:12	0x0 RW	**comp_usd_type4:** compression format for vc=2, user defined type 4 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
11	0x0 RW	**pred_usd_type3:** prediction algorithm for vc=2, user defined type 3 data: 0 -) pred1, 1 -) pred2
10:8	0x0 RW	**comp_usd_type3:** compression format for vc=2, user defined type 3 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
7	0x0 RW	**pred_usd_type2:** prediction algorithm for vc=2, user defined type 2 data: 0 -) pred1, 1 -) pred2
6:4	0x0 RW	**comp_usd_type2:** compression format for vc=2, user defined type 2 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.

Bit Range	Default and Access	Field Name (ID): Description
3	0x0 RW	**pred_usd_type1:** prediction algorithm for vc=2, user defined type 1 data: 0 -) pred1, 1 -) pred2
2:0	0x0 RW	**comp_usd_type1:** compression format for vc=2, user defined type 1 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.

5.3.50 csi_sh_be_comp_reg_vc3 (is_2400_inp_sys_csi_receiver_csi_sh_be_comp_reg_vc3)—Offset 80818h

Compression scheme register for virtual channel 0

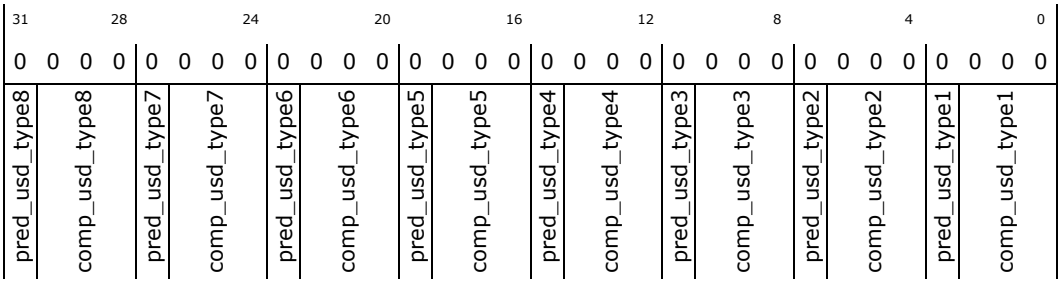
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

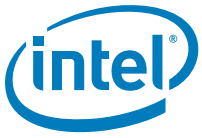
Offset: [ISPMMADR] + 80818h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**pred_usd_type8:** prediction algorithm for vc=3, user defined type 8 data: 0 -) pred1, 1 -) pred2
30:28	0x0 RW	**comp_usd_type8:** compression format for vc=3, user defined type 8 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
27	0x0 RW	**pred_usd_type7:** prediction algorithm for vc=3, user defined type 7 data: 0 -) pred1, 1 -) pred2
26:24	0x0 RW	**comp_usd_type7:** compression format for vc=3, user defined type 7 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
23	0x0 RW	**pred_usd_type6:** prediction algorithm for vc=3, user defined type 6 data: 0 -) pred1, 1 -) pred2



Bit Range	Default and Access	Field Name (ID): Description
22:20	0x0 RW	**comp_usd_type6:** compression format for vc=3, user defined type 6 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
19	0x0 RW	**pred_usd_type5:** prediction algorithm for vc=3, user defined type 5 data: 0 -) pred1, 1 -) pred2
18:16	0x0 RW	**comp_usd_type5:** compression format for vc=3, user defined type 5 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
15	0x0 RW	**pred_usd_type4:** prediction algorithm for vc=3, user defined type 4 data: 0 -) pred1, 1 -) pred2
14:12	0x0 RW	**comp_usd_type4:** compression format for vc=3, user defined type 4 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
11	0x0 RW	**pred_usd_type3:** prediction algorithm for vc=3, user defined type 3 data: 0 -) pred1, 1 -) pred2
10:8	0x0 RW	**comp_usd_type3:** compression format for vc=3, user defined type 3 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
7	0x0 RW	**pred_usd_type2:** prediction algorithm for vc=3, user defined type 2 data: 0 -) pred1, 1 -) pred2
6:4	0x0 RW	**comp_usd_type2:** compression format for vc=3, user defined type 2 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.
3	0x0 RW	**pred_usd_type1:** prediction algorithm for vc=3, user defined type 1 data: 0 -) pred1, 1 -) pred2
2:0	0x0 RW	**comp_usd_type1:** compression format for vc=3, user defined type 1 data: 000:No compression, 001:10-6-10, 010:10-7-10, 011:10-8-10, 100:12-6-12, 101:12-7-12, 110:12-8-12.

5.3.51 csi_sh_be_sel_be (is_2400_inp_sys_csi_receiver_csi_sh_be_sel_be)—Offset 8081Ch

Selects which CSI Receiver Backend to use 0-Arasan Backend, 1-Silicon Hive Backend

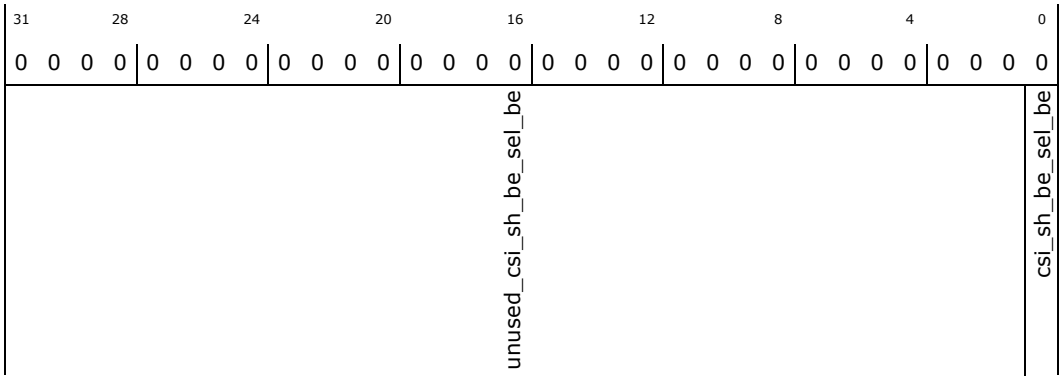
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8081Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_csi_sh_be_sel_be):** Unused
0	0x0 RW	**csi_sh_be_sel_be:** Selects which CSI Receiver Backend to use 0-Arasan Backend, 1-Silicon Hive Backend

5.3.52 csi_sh_be_raw16_reg (is_2400_inp_sys_csi_receiver_csi_sh_be_raw16_reg)—Offset 80820h

Configuration register for RAW 16 data type decode

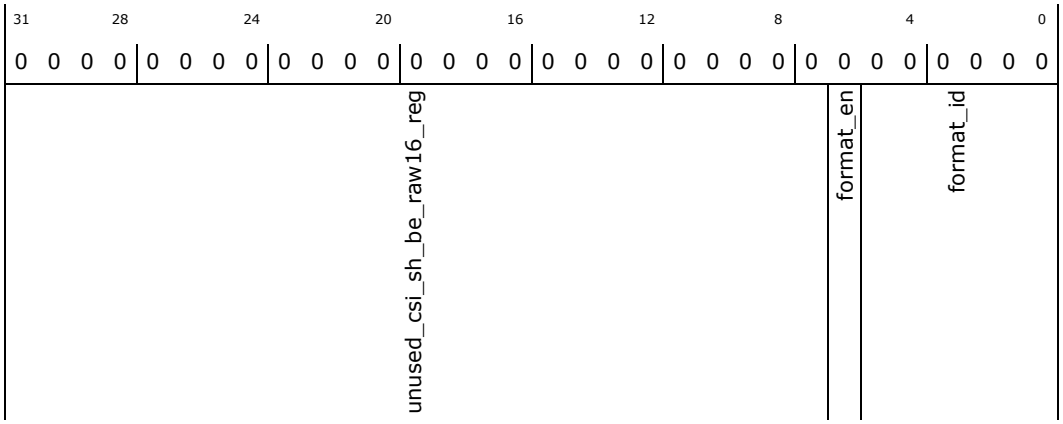
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80820h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:7	0x0 RO	**Reserved (unused_csi_sh_be_raw16_reg):** Unused
6	0x0 RW	**format_en:** enable RAW 16 type decode
5:0	0x0 RW	**format_id:** data id for RAW 16

5.3.53 csi_sh_be_raw18_reg (is_2400_inp_sys_csi_receiver_csi_sh_be_raw18_reg)—Offset 80824h

Configuration register for RAW 18 data type decode

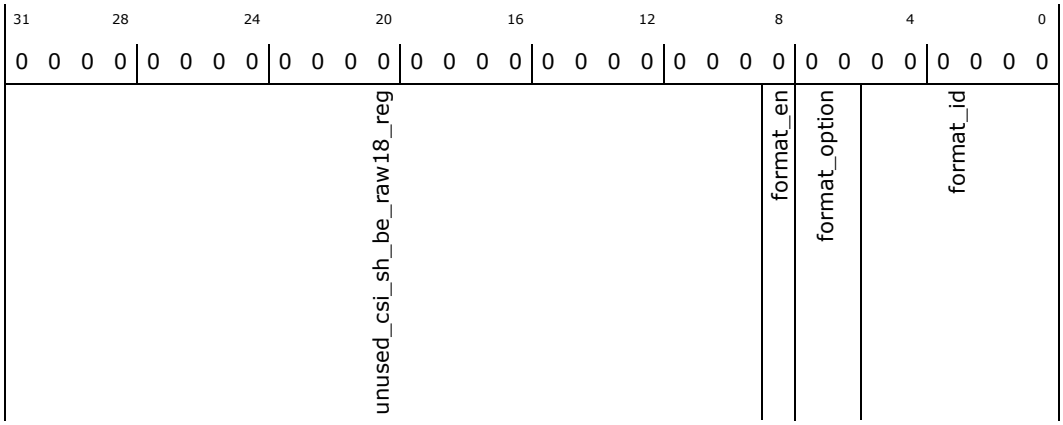
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80824h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:9	0x0 RO	**Reserved (unused_csi_sh_be_raw18_reg):** Unused
8	0x0 RW	**format_en:** enable RAW 16 type decode
7:6	0x0 RW	**format_option:** format option for RAW 18 data type: 3 options possible (1,2,3)
5:0	0x0 RW	**format_id:** data id for RAW 16

5.3.54 csi_sh_be_force_raw8_reg (is_2400_inp_sys_csi_receiver_csi_sh_be_force_raw8_reg)—Offset 80828h

Force RAW8(byte) decoding for LONG data packets

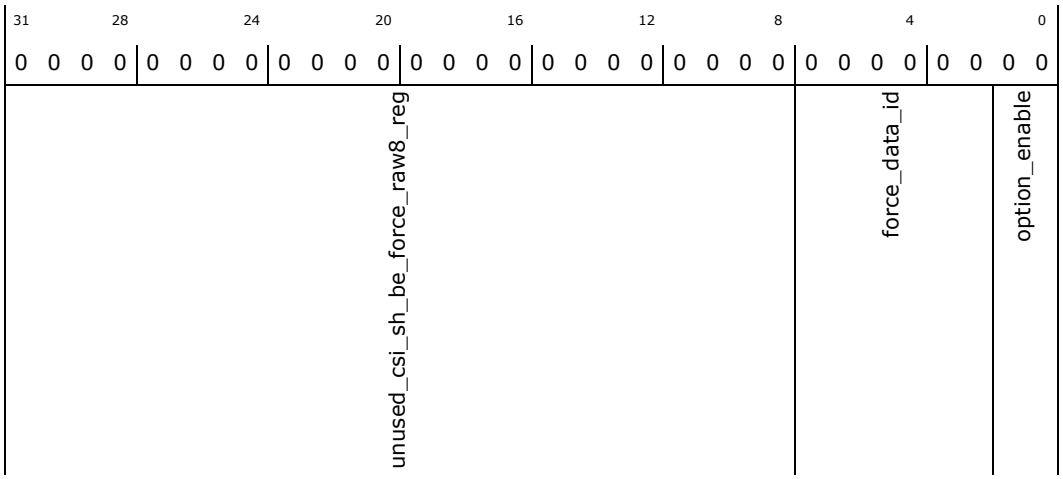
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80828h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (unused_csi_sh_be_force_raw8_reg):** Unused
7:2	0x0 RW	**force_data_id:** Data_id that should be forced to RAW8
1:0	0x0 RW	**option_enable:** 00-Do not force anything in RAW8 mode. 01-force all data types in RAW8 mode, 11-force only packets with data_id force_data_id to RAW8 mode

5.3.55 csi_sh_be_irq_stat_reg (is_2400_inp_sys_csi_receiver_csi_sh_be_irq_stat_reg)—Offset 8082Ch

IRQ status register

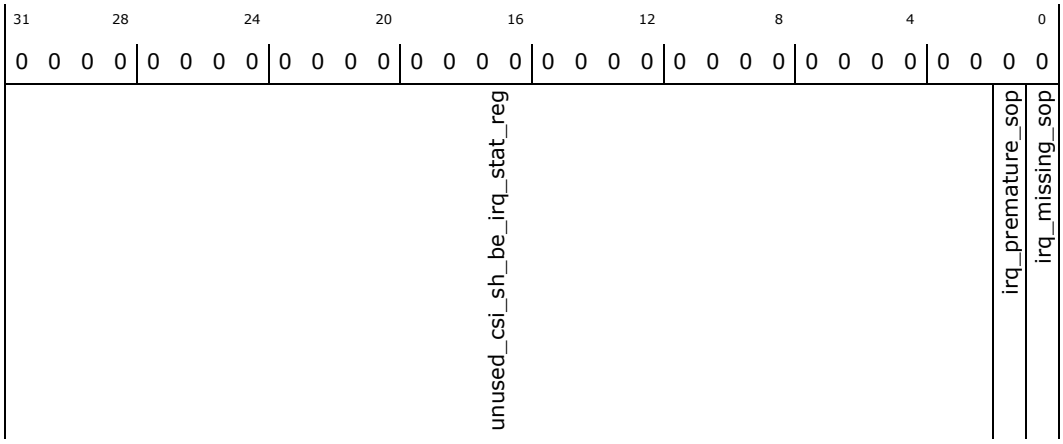
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8082Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved (unused_csi_sh_be_irq_stat_reg):** Unused
1	0x0 RO	**irq_premature_sop:** If '1', sh_be has detected a premature sop
0	0x0 RO	**irq_missing_sop:** If '1', sh_be has detected a missing sop

5.3.56 csi_sh_be_irq_stat_clear_reg (is_2400_inp_sys_csi_receiver_csi_sh_be_irq_stat_clear_reg)—Offset 80830h

IRQ Status Clear Register

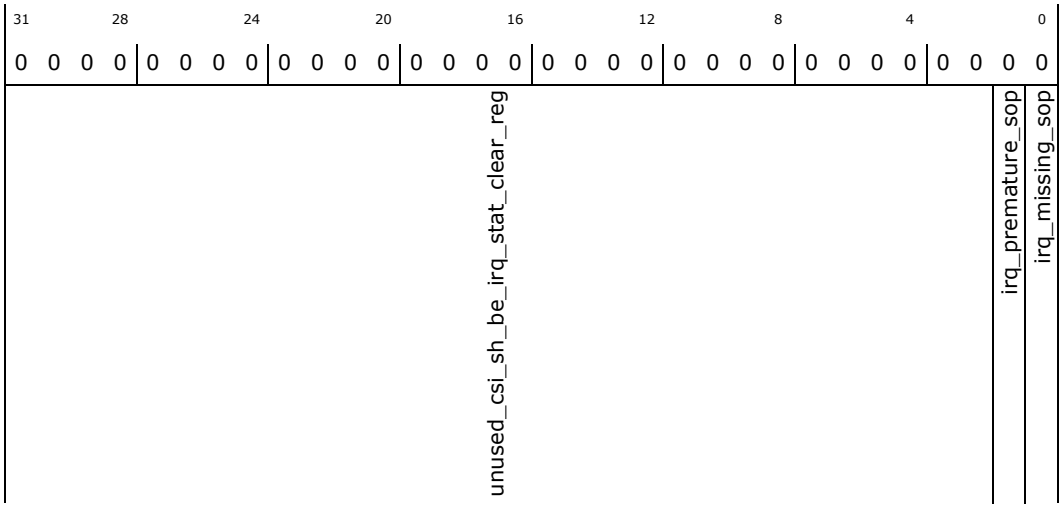
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80830h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved (unused_csi_sh_be_irq_stat_clear_reg):** Unused
1	0x0 WO	**irq_premature_sop:** A '1' written into this field, clears the premature_sop field to '0'
0	0x0 WO	**irq_missing_sop:** A '1' written into this field, clears the irq_missing_sop field to '0'

5.3.57 csi_sh_be_custom_enable_reg (is_2400_inp_sys_csi_receiver_csi_sh_be_custom_enable_reg)—Offset 80834h

Enable custom mode decoding for LONG data packets

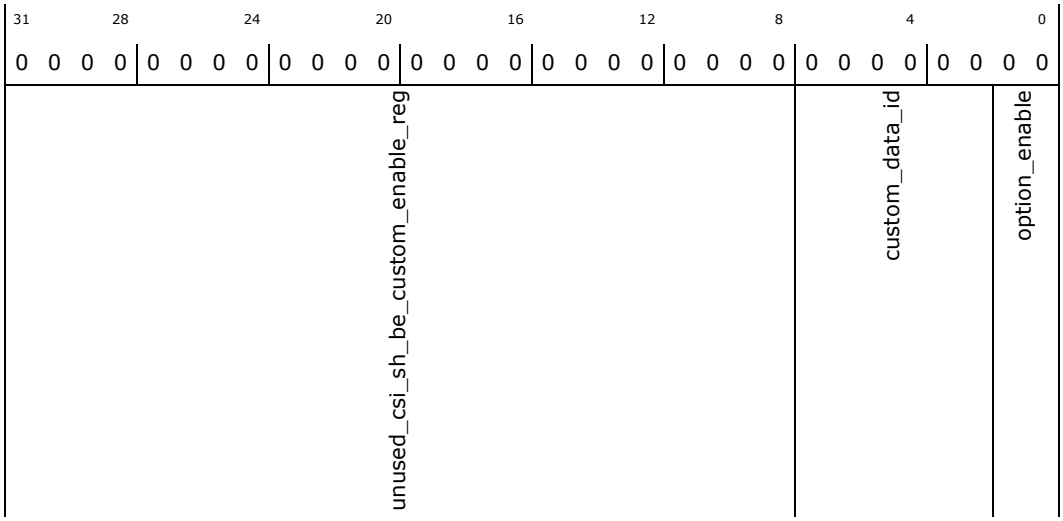
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 80834h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (unused_csi_sh_be_custom_enable_reg):** Unused
7:2	0x0 RW	**custom_data_id:** Data_id that should be processed in custom mode
1:0	0x0 RW	**option_enable:** 00-Custom mode switched off. 01-all data types in custom mode, 11-only packets with data id custom_data_id are processed in custom mode

5.3.58 reg_CaptStartMode (is_2400_inp_sys_capt_unit_a_reg_CaptStartMode)—Offset 81000h

Synchronize on any packet header or on a frame start

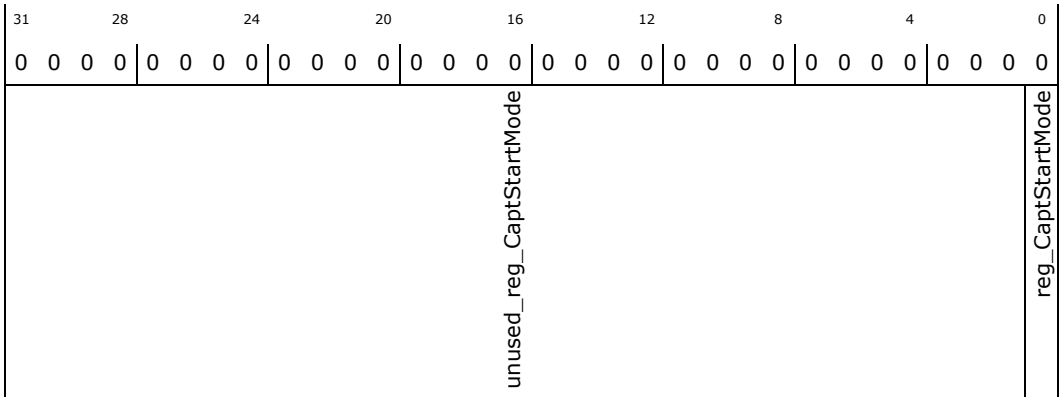
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 81000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_CaptStartMode):** Unused
0	0x0 RW	**reg_CaptStartMode:** Synchronize on any packet header or on a frame start

5.3.59 reg_Capt_Start_Addr (is_2400_inp_sys_capt_unit_a_reg_Capt_Start_Addr)—Offset 81004h

Start Address of first memory region

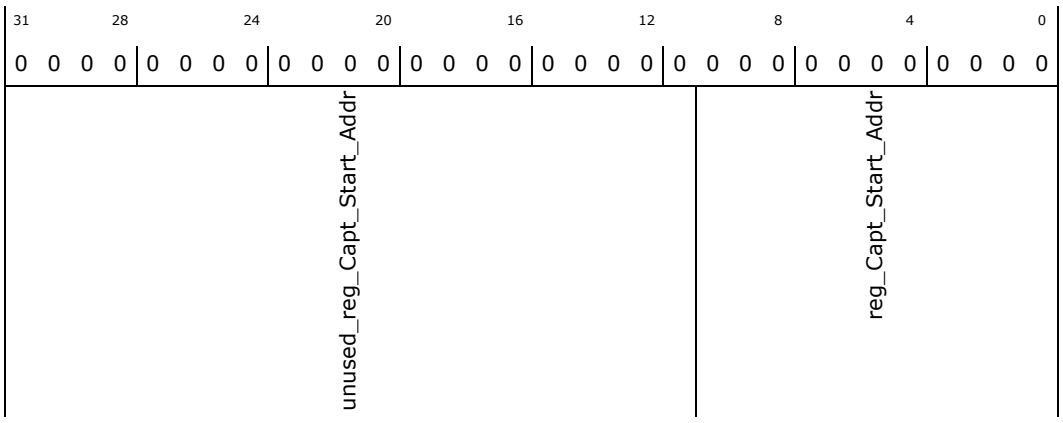
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 81004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:11	0x0 RW	**Reserved (unused_reg_Capt_Start_Addr):** Unused
10:0	0x0 RW	**reg_Capt_Start_Addr:** Start Address of first memory region

5.3.60 reg_Capt_Mem_Region_Size (is_2400_inp_sys_capt_unit_a_reg_Capt_Mem_Region_Size)—Offset 81008h

Memory region size

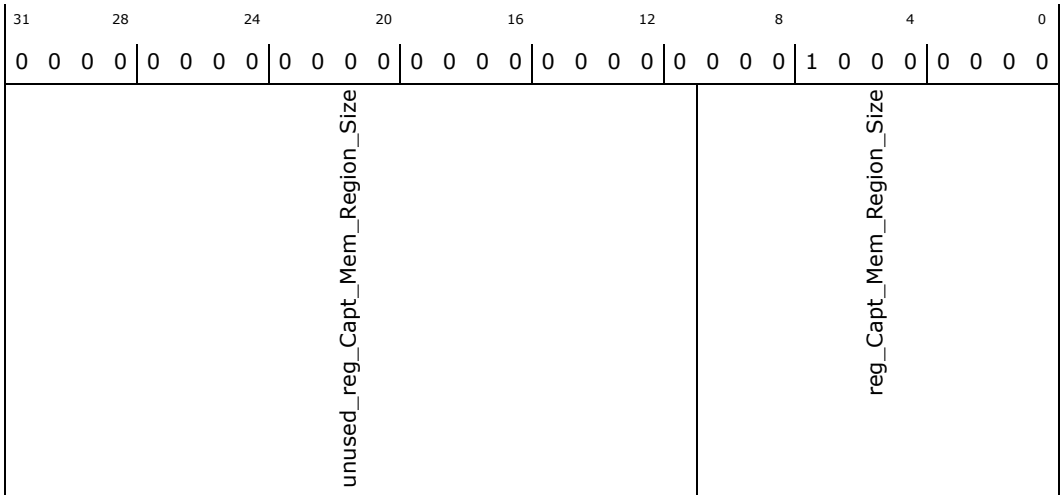
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 81008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h



Bit Range	Default and Access	Field Name (ID): Description
31:11	0x0 RW	**Reserved (unused_reg_Capt_Mem_Region_Size):** Unused
10:0	0x80 RW	**reg_Capt_Mem_Region_Size:** Memory region size

5.3.61 reg_Capt_Num_Mem_Regions (is_2400_inp_sys_capt_unit_a_reg_Capt_Num_Mem_Regions)—Offset 8100Ch

Number of memory regions

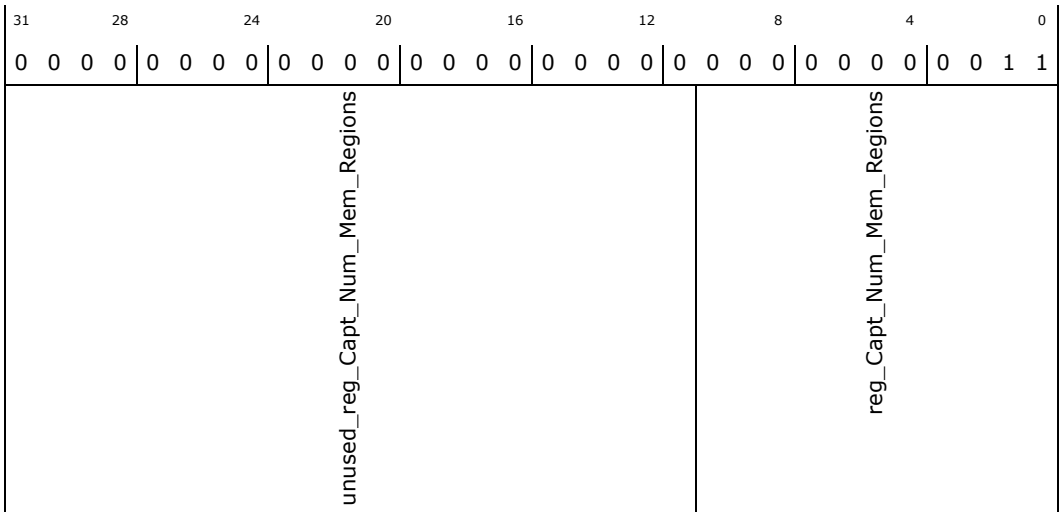
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8100Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h



Bit Range	Default and Access	Field Name (ID): Description
31:11	0x0 RW	**Reserved (unused_reg_Capt_Num_Mem_Regions):** Unused
10:0	0x3 RW	**reg_Capt_Num_Mem_Regions:** Number of memory regions

5.3.62 reg_Capt_Init (is_2400_inp_sys_capt_unit_a_reg_Capt_Init)—Offset 81010h

Initialize Capture Unit

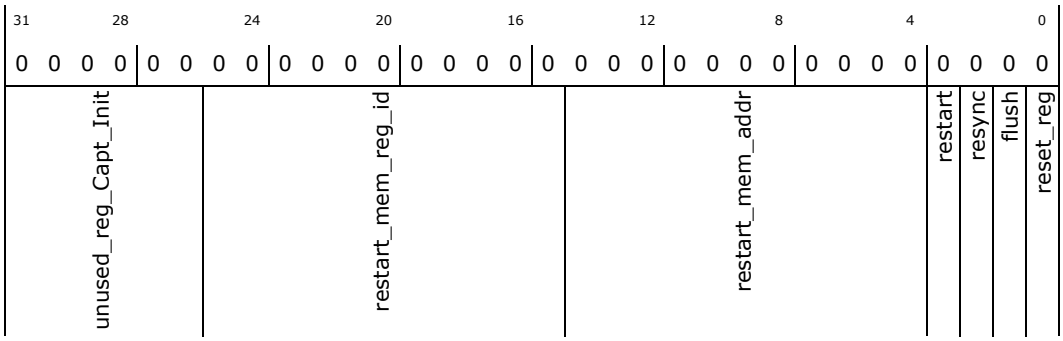
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 81010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:26	0x0 RO	**Reserved (unused_reg_Capt_Init):** Unused
25:15	0x0 WO	**restart_mem_reg_id:** Restart Memory Region ID
14:4	0x0 WO	**restart_mem_addr:** Restart Memory Address
3	0x0 WO	**restart:** Restart Capture Unit
2	0x0 WO	**resync:** Re-synchronize Capture Unit
1	0x0 WO	**flush:** Flush Internal Buffers
0	0x0 WO	**reset_reg:** Reset Status Registers

5.3.63 reg_Capt_Start (is_2400_inp_sys_capt_unit_a_reg_Capt_Start)—Offset 81014h

Start Capturing

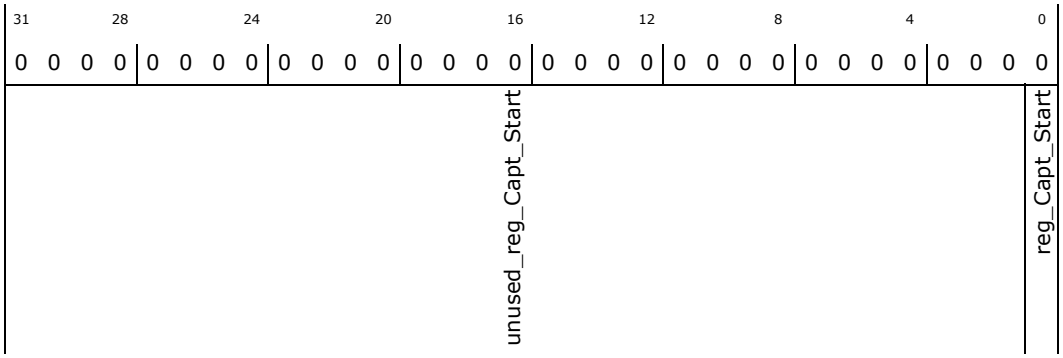
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 81014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_Capt_Start):** Unused
0	0x0 WO	**reg_Capt_Start:** Start Capturing

5.3.64 reg_Capt_Stop (is_2400_inp_sys_capt_unit_a_reg_Capt_Stop)—Offset 81018h

Stop Capturing

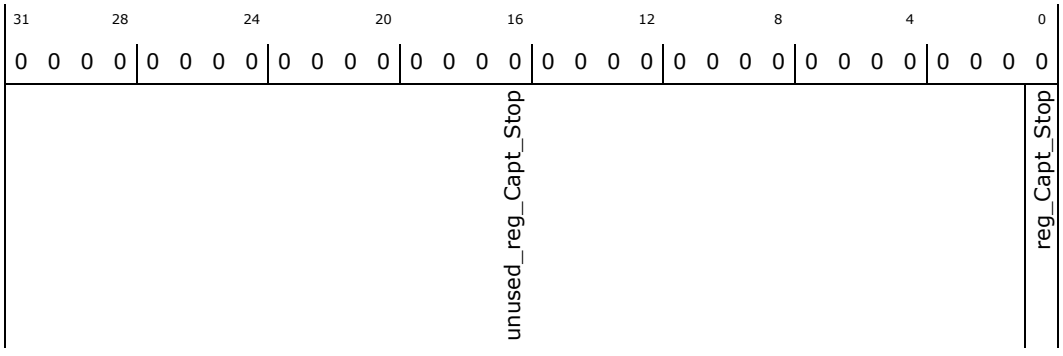
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 81018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_Capt_Stop):** Unused
0	0x0 WO	**reg_Capt_Stop:** Stop Capturing

5.3.65 reg_Capt_Packet_Length (is_2400_inp_sys_capt_unit_a_reg_Capt_Packet_Length)—Offset 8101Ch

Packet length of multi_word packet (MWP) as decoded from packet header

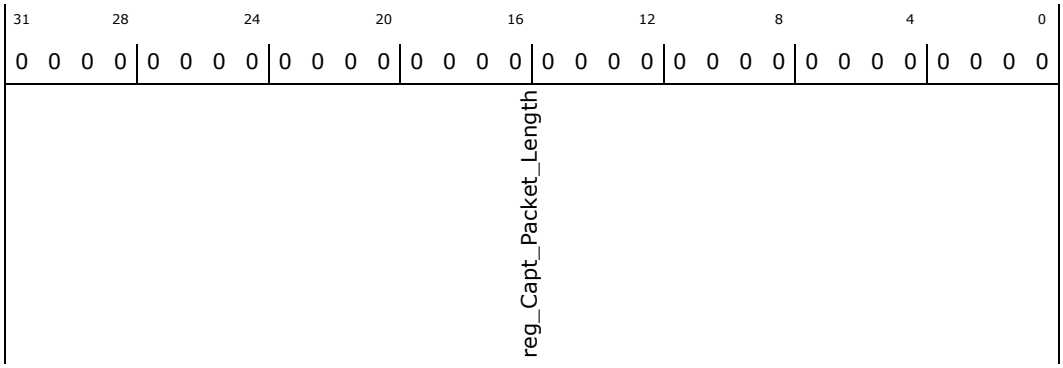
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8101Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**reg_Capt_Packet_Length:** Packet length of multi_word packet (MWP) as decoded from packet header

5.3.66 reg_Capt_Received_Length (is_2400_inp_sys_capt_unit_a_reg_Capt_Received_Length)—Offset 81020h

(Incremental) received packet length of current multi-word packet (MWP)

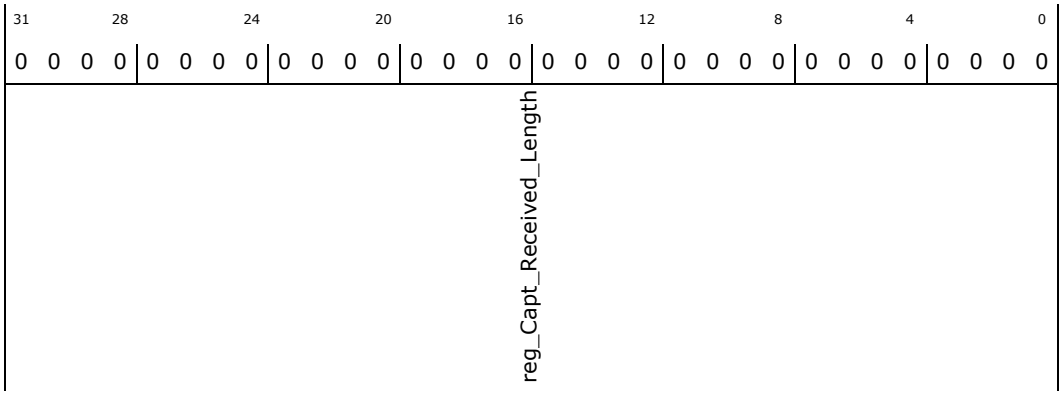
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 81020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**reg_Capt_Received_Length:** (Incremental) received packet length of current multi-word packet (MWP)

5.3.67 reg_Capt_Received_Short_Packets (is_2400_inp_sys_capt_unit_a_reg_Capt_Received_Short_Packets)—Offset 81024h

Number of received short packets

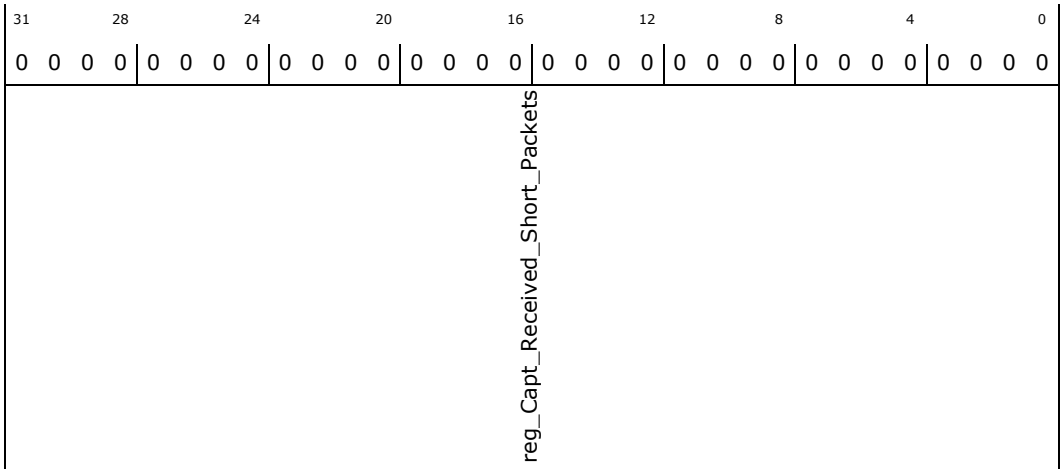
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 81024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**reg_Capt_Received_Short_Packets:** Number of received short packets

5.3.68 reg_Capt_Received_Long_Packets (is_2400_inp_sys_capt_unit_a_reg_Capt_Received_Long_Packets)—Offset 81028h

Number of received long packets

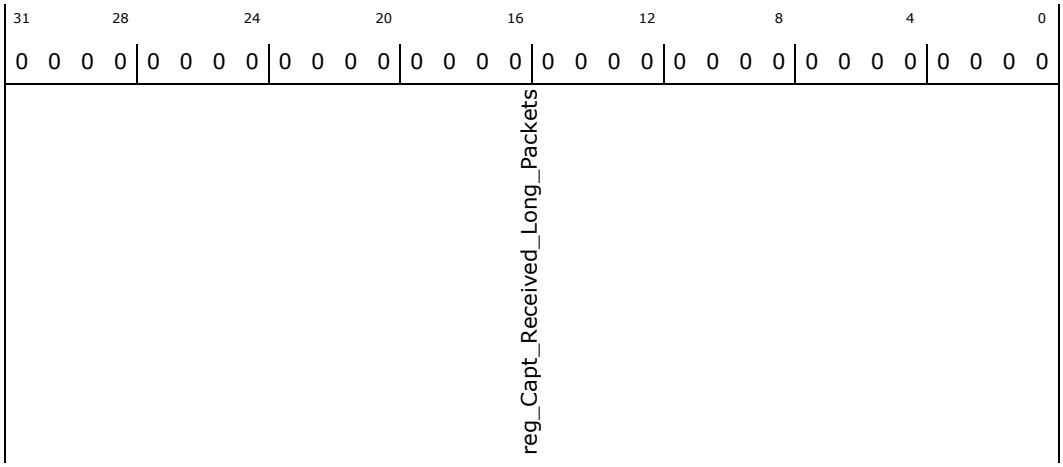
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 81028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**reg_Capt_Received_Long_Packets:** Number of received long packets

5.3.69 reg_Capt_Last_Command (is_2400_inp_sys_capt_unit_a_reg_Capt_Last_Command)—Offset 8102Ch

Last command token accepted

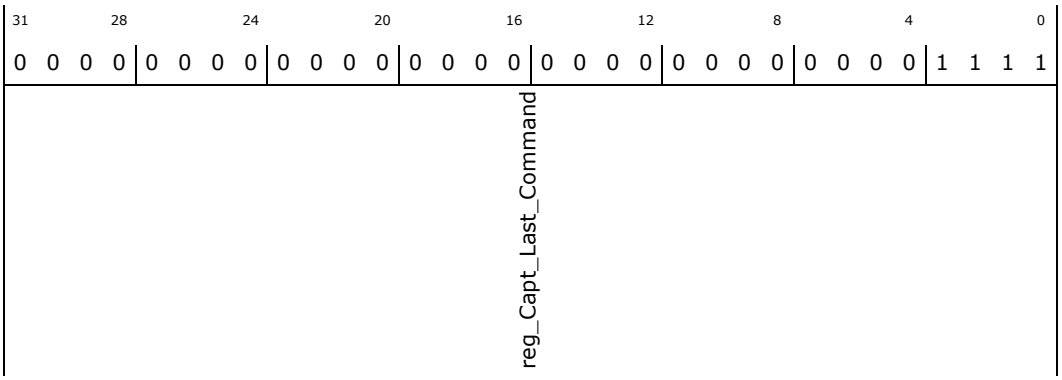
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8102Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**reg_Capt_Last_Command:** Last command token accepted

5.3.70 reg_Capt_Next_Command (is_2400_inp_sys_capt_unit_a_reg_Capt_Next_Command)—Offset 81030h

Next command token to be accepted

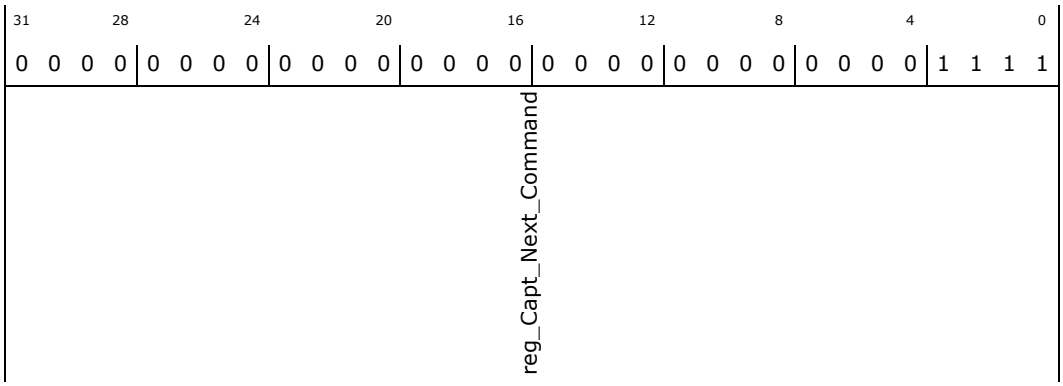
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 81030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**reg_Capt_Next_Command:** Next command token to be accepted

5.3.71 reg_Capt_Last_Acknowledge (is_2400_inp_sys_capt_unit_a_reg_Capt_Last_Acknowledge)—Offset 81034h

Last acknowledge token send

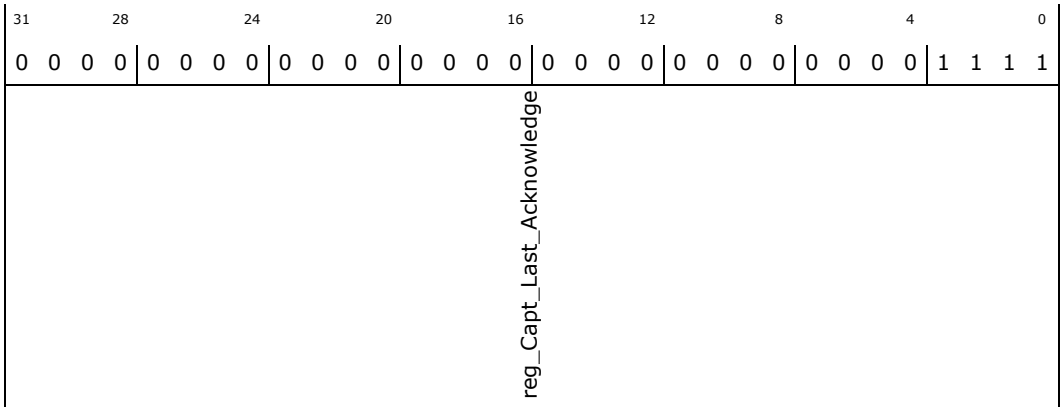
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 81034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**reg_Capt_Last_Acknowledge:** Last acknowledge token send

5.3.72 reg_Capt_Next_Acknowledge (is_2400_inp_sys_capt_unit_a_reg_Capt_Next_Acknowledge)—Offset 81038h

Next acknowledge token to be send

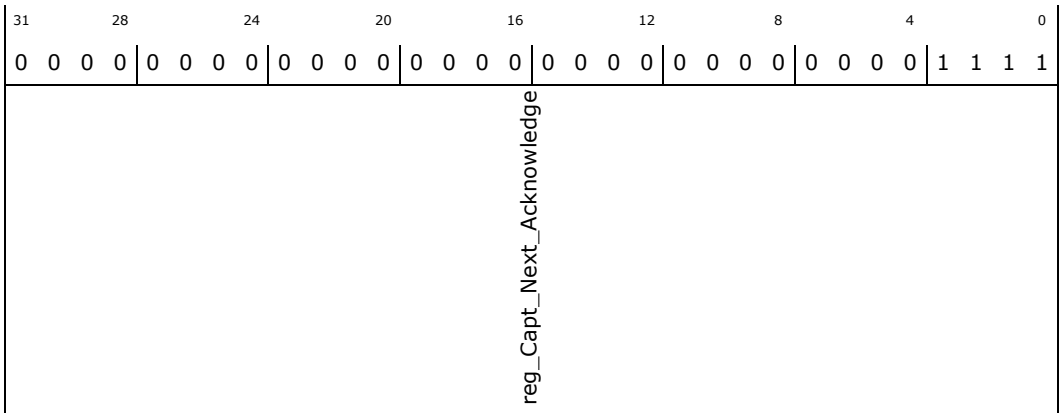
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 81038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**reg_Capt_Next_Acknowledge:** Next acknowledge token to be send

5.3.73 reg_Capt_FSM_State_Info (is_2400_inp_sys_capt_unit_a_reg_Capt_FSM_State_Info)—Offset 8103Ch

Capture Unit State Machine Information

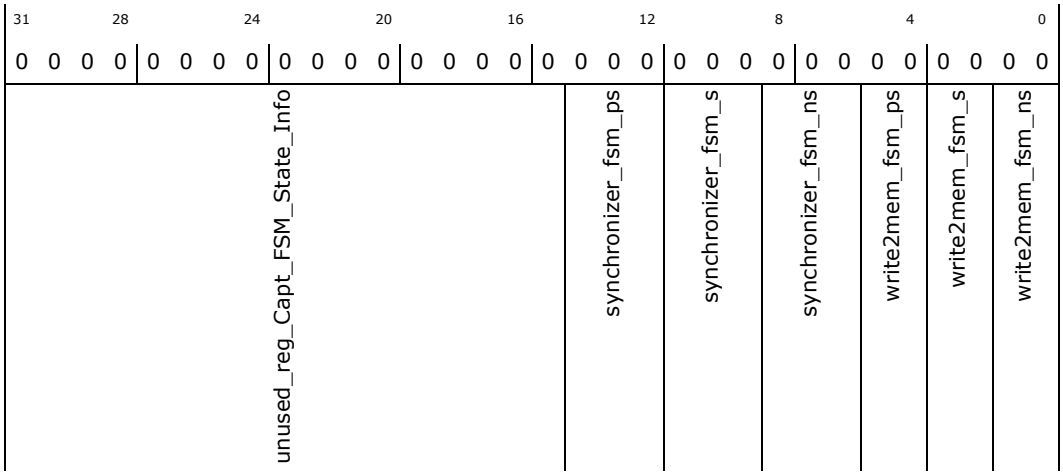
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8103Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:15	0x0 RO	**Reserved (unused_reg_Capt_FSM_State_Info):** Unused
14:12	0x0 RO	**synchronizer_fsm_ps:** Previous state of Synchronizer State Machine: 00=free run, 01=no sync, 10=sync sp, 11=sync lp, 100=sync wait
11:9	0x0 RO	**synchronizer_fsm_s:** Current state of Synchronizer State Machine: 00=free run, 01=no sync, 10=sync sp, 11=sync lp, 100=sync wait
8:6	0x0 RO	**synchronizer_fsm_ns:** Next state of Synchronizer State Machine: 00=free run, 01=no sync, 10=sync sp, 11=sync lp, 100=sync wait
5:4	0x0 RO	**write2mem_fsm_ps:** Previous state of Write2Mem State Machine: 00=idle, 01=buffer,11=write
3:2	0x0 RO	**write2mem_fsm_s:** Current state of Write2Mem State Machine: 00=idle, 01=buffer,11=write
1:0	0x0 RO	**write2mem_fsm_ns:** Next state of Write2Mem State Machine: 00=idle, 01=buffer,11=write

5.3.74 reg_CaptStartMode (is_2400_inp_sys_capt_unit_b_reg_CaptStartMode)—Offset 82000h

Synchronize on any packet header or on a frame start

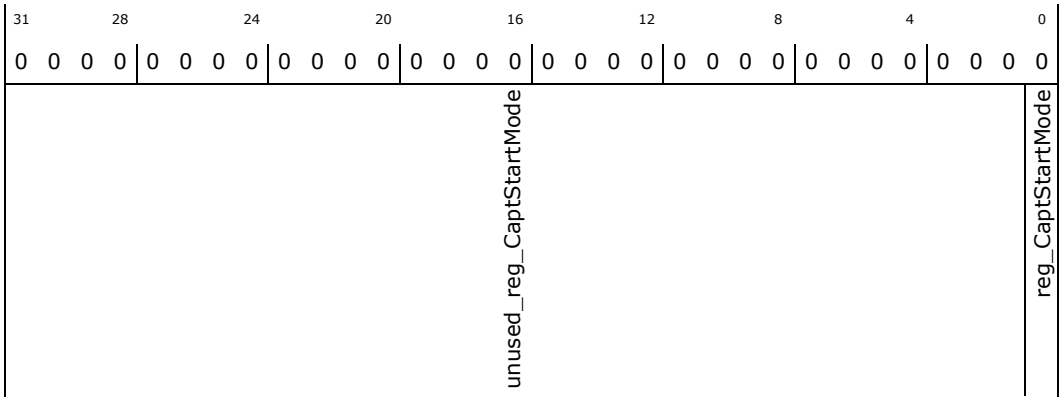
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 82000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_CaptStartMode):** Unused
0	0x0 RW	**reg_CaptStartMode:** Synchronize on any packet header or on a frame start

5.3.75 reg_Capt_Start_Addr (is_2400_inp_sys_capt_unit_b_reg_Capt_Start_Addr)—Offset 82004h

Start Address of first memory region

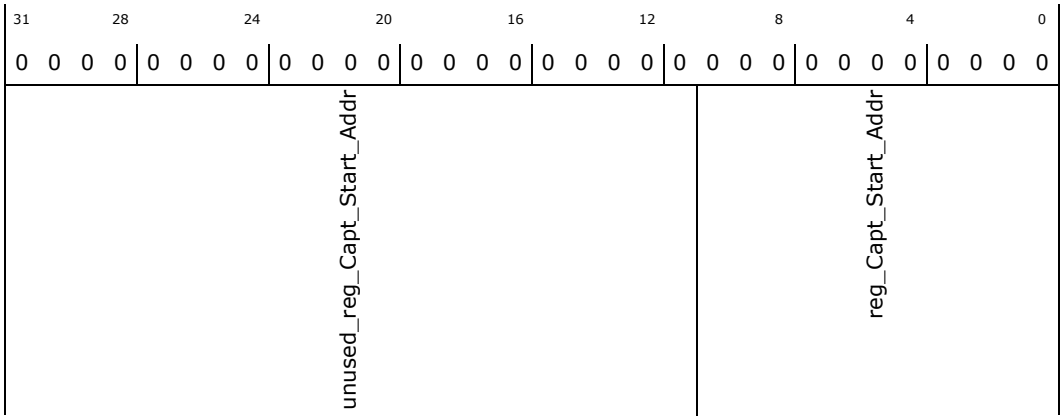
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 82004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:11	0x0 RW	**Reserved (unused_reg_Capt_Start_Addr):** Unused
10:0	0x0 RW	**reg_Capt_Start_Addr:** Start Address of first memory region

5.3.76 reg_Capt_Mem_Region_Size (is_2400_inp_sys_capt_unit_b_reg_Capt_Mem_Region_Size)—Offset 82008h

Memory region size

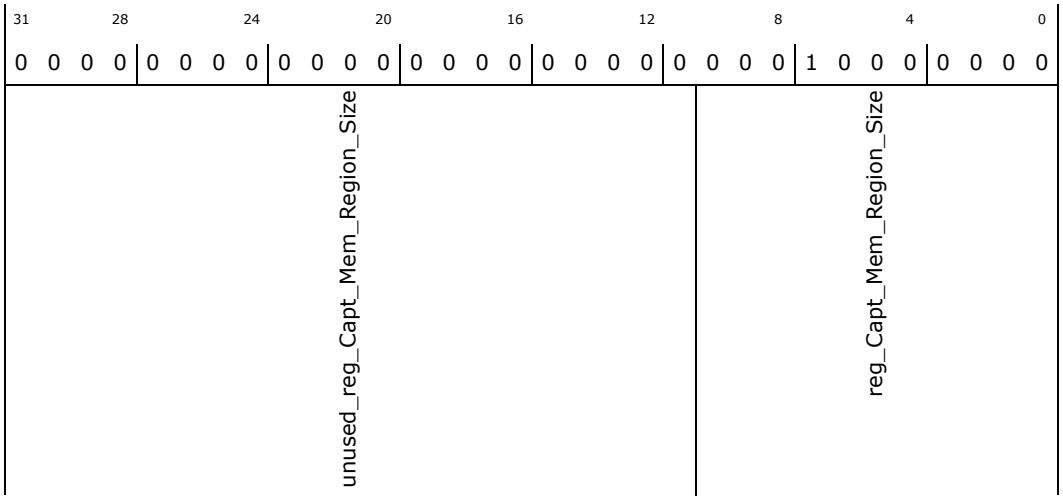
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 82008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h



Bit Range	Default and Access	Field Name (ID): Description
31:11	0x0 RW	**Reserved (unused_reg_Capt_Mem_Region_Size):** Unused
10:0	0x80 RW	**reg_Capt_Mem_Region_Size:** Memory region size

5.3.77 reg_Capt_Num_Mem_Regions (is_2400_inp_sys_capt_unit_b_reg_Capt_Num_Mem_Regions)—Offset 8200Ch

Number of memory regions

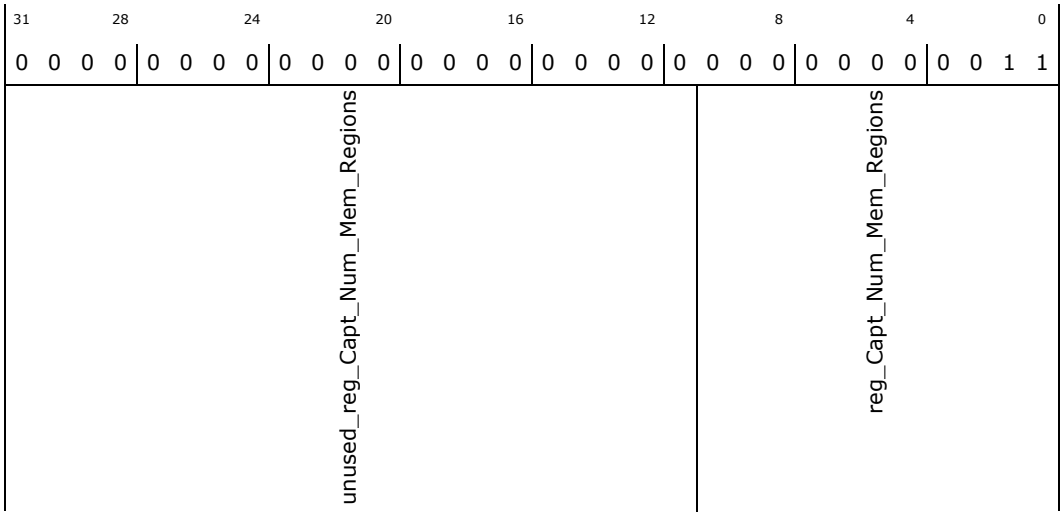
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8200Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h



Bit Range	Default and Access	Field Name (ID): Description
31:11	0x0 RW	**Reserved (unused_reg_Capt_Num_Mem_Regions):** Unused
10:0	0x3 RW	**reg_Capt_Num_Mem_Regions:** Number of memory regions

5.3.78 reg_Capt_Init (is_2400_inp_sys_capt_unit_b_reg_Capt_Init)—Offset 82010h

Initialize Capture Unit

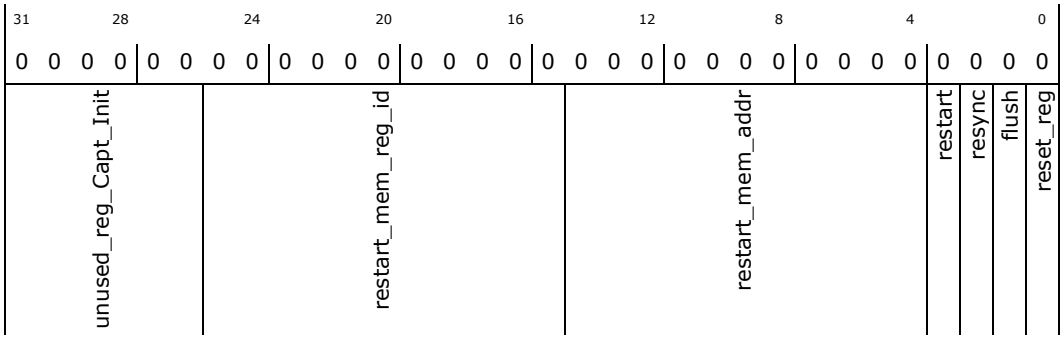
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 82010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:26	0x0 RO	**Reserved (unused_reg_Capt_Init):** Unused
25:15	0x0 WO	**restart_mem_reg_id:** Restart Memory Region ID
14:4	0x0 WO	**restart_mem_addr:** Restart Memory Address
3	0x0 WO	**restart:** Restart Capture Unit
2	0x0 WO	**resync:** Re-synchronize Capture Unit
1	0x0 WO	**flush:** Flush Internal Buffers
0	0x0 WO	**reset_reg:** Reset Status Registers

5.3.79 reg_Capt_Start (is_2400_inp_sys_capt_unit_b_reg_Capt_Start)—Offset 82014h

Start Capturing

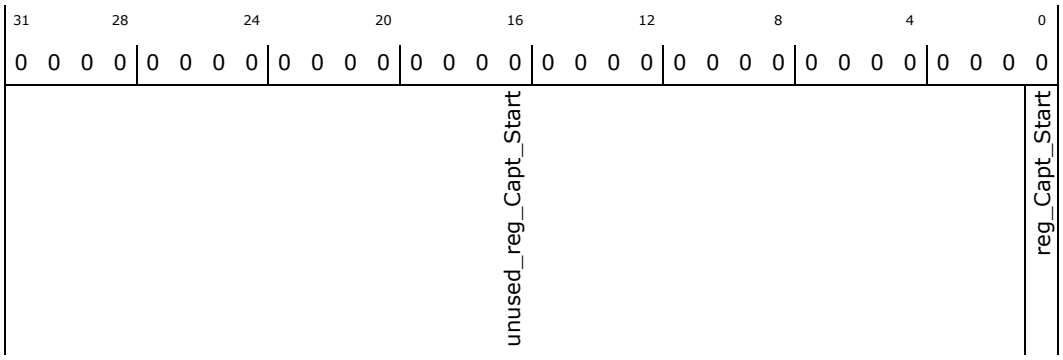
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 82014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_Capt_Start):** Unused

Bit Range	Default and Access	Field Name (ID): Description
0	0x0 WO	**reg_Capt_Start:** Start Capturing

5.3.80 reg_Capt_Stop (is_2400_inp_sys_capt_unit_b_reg_Capt_Stop)—Offset 82018h

Stop Capturing

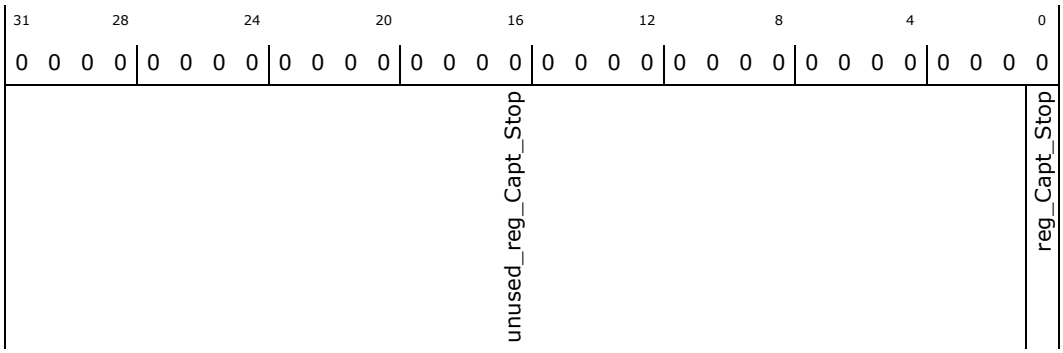
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 82018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_Capt_Stop):** Unused
0	0x0 WO	**reg_Capt_Stop:** Stop Capturing

5.3.81 reg_Capt_Packet_Length (is_2400_inp_sys_capt_unit_b_reg_Capt_Packet_Length)—Offset 8201Ch

Packet length of multi_word packet (MWP) as decoded from packet header

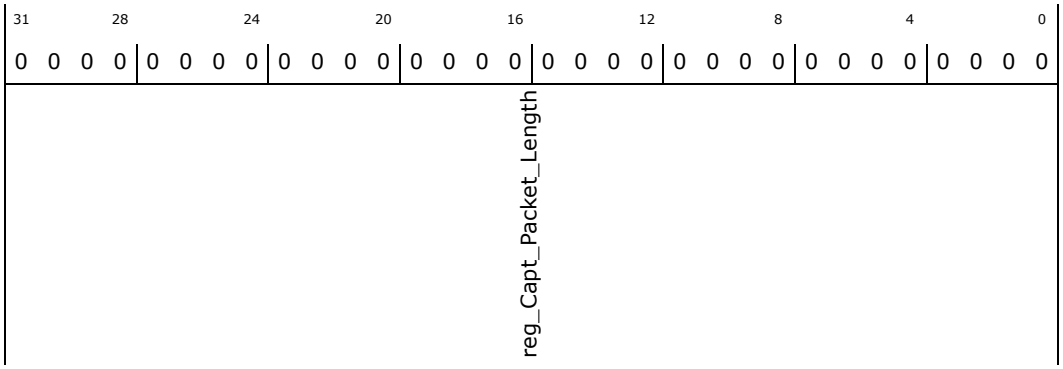
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8201Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**reg_Capt_Packet_Length:** Packet length of multi_word packet (MWP) as decoded from packet header

5.3.82 reg_Capt_Received_Length (is_2400_inp_sys_capt_unit_b_reg_Capt_Received_Length)—Offset 82020h

(Incremental) received packet length of current multi-word packet (MWP)

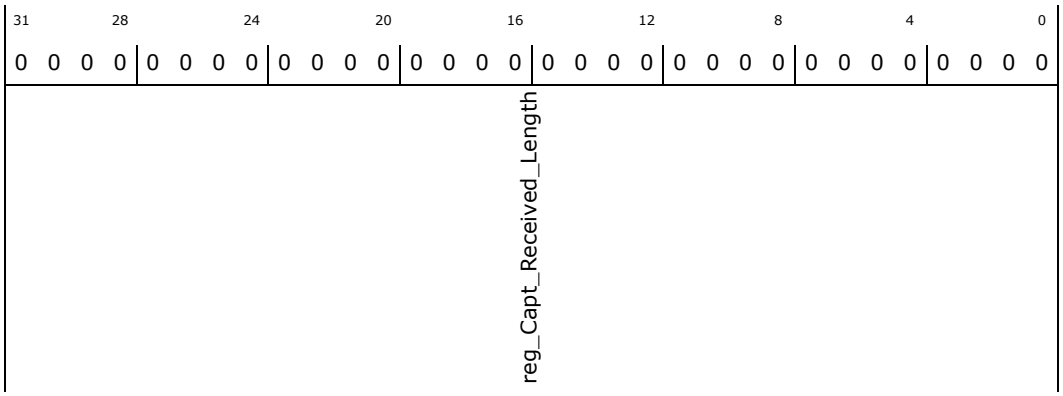
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 82020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**reg_Capt_Received_Length:** (Incremental) received packet length of current multi-word packet (MWP)

5.3.83 reg_Capt_Received_Short_Packets (is_2400_inp_sys_capt_unit_b_reg_Capt_Received_Short_Packets)—Offset 82024h

Number of received short packets

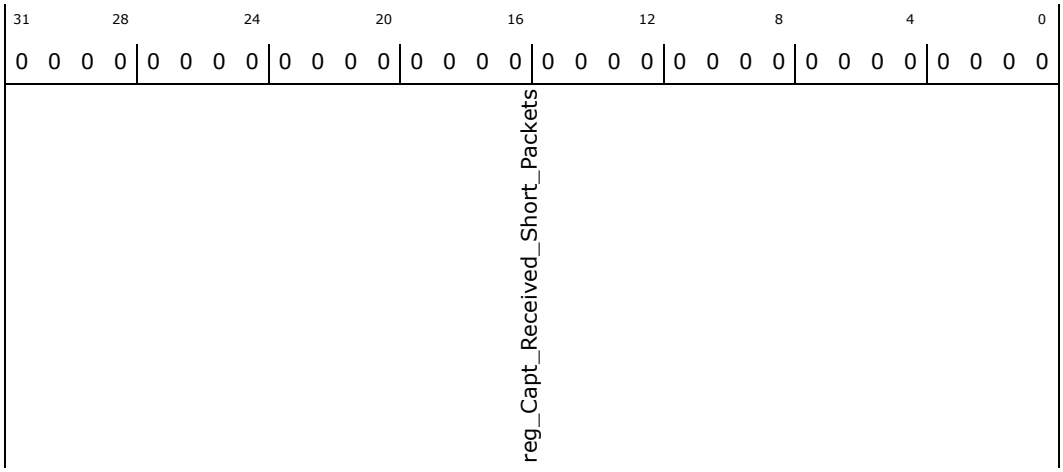
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 82024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**reg_Capt_Received_Short_Packets:** Number of received short packets

5.3.84 reg_Capt_Received_Long_Packets (is_2400_inp_sys_capt_unit_b_reg_Capt_Received_Long_Packets)—Offset 82028h

Number of received long packets

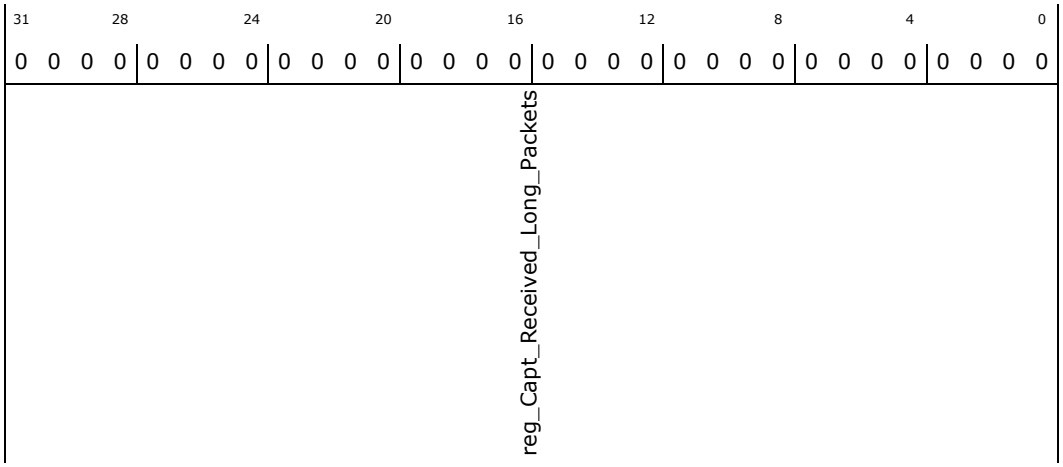
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 82028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**reg_Capt_Received_Long_Packets:** Number of received long packets

5.3.85 reg_Capt_Last_Command (is_2400_inp_sys_capt_unit_b_reg_Capt_Last_Command)—Offset 8202Ch

Last command token accepted

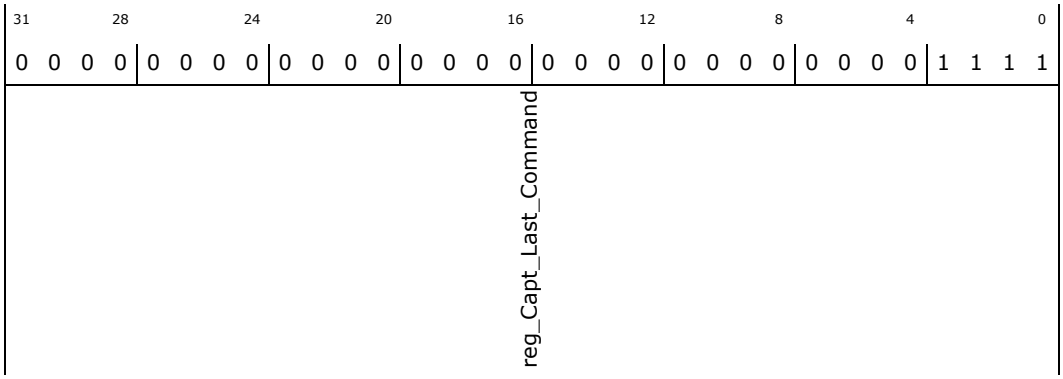
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8202Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**reg_Capt_Last_Command:** Last command token accepted

5.3.86 reg_Capt_Next_Command (is_2400_inp_sys_capt_unit_b_reg_Capt_Next_Command)—Offset 82030h

Next command token to be accepted

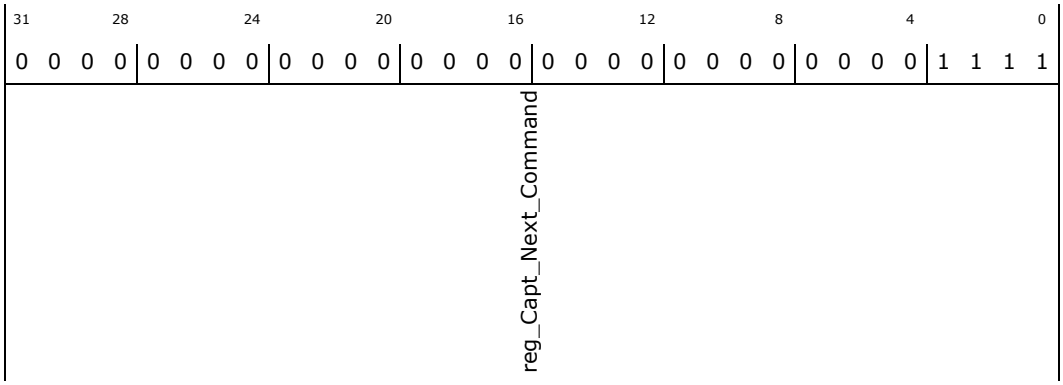
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 82030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**reg_Capt_Next_Command:** Next command token to be accepted

5.3.87 reg_Capt_Last_Acknowledge (is_2400_inp_sys_capt_unit_b_reg_Capt_Last_Acknowledge)—Offset 82034h

Last acknowledge token send

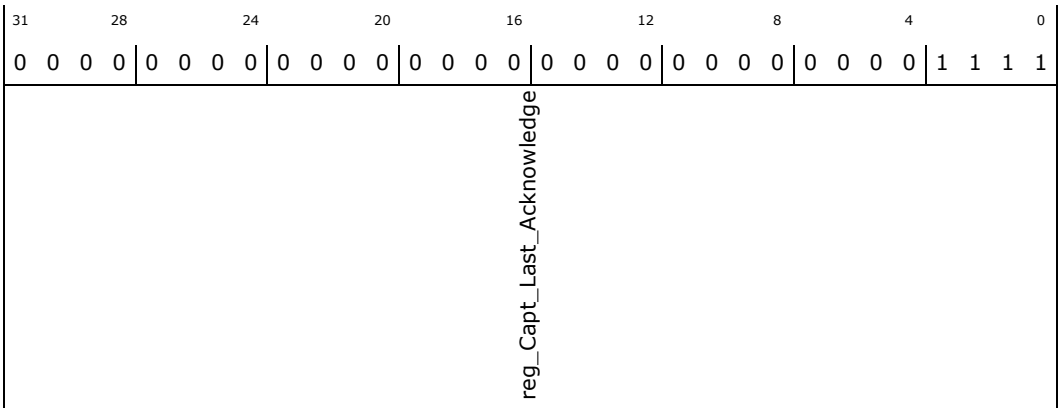
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 82034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**reg_Capt_Last_Acknowledge:** Last acknowledge token send

5.3.88 reg_Capt_Next_Acknowledge (is_2400_inp_sys_capt_unit_b_reg_Capt_Next_Acknowledge)—Offset 82038h

Next acknowledge token to be send

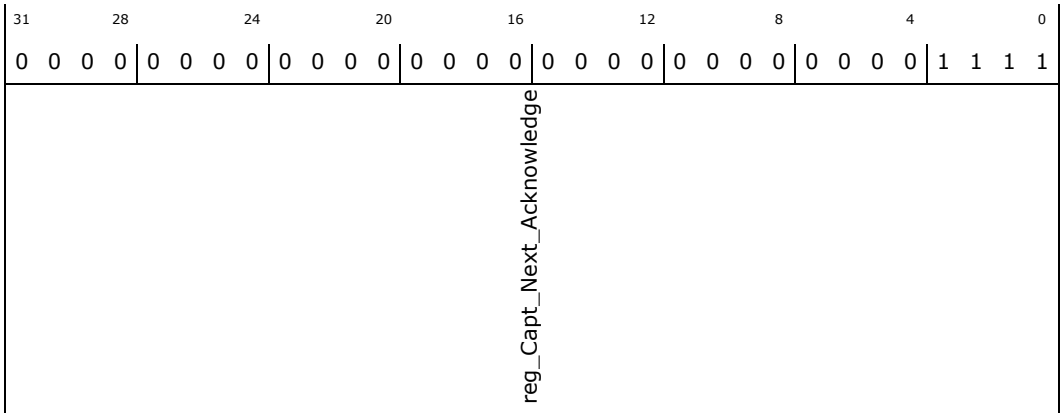
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 82038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**reg_Capt_Next_Acknowledge:** Next acknowledge token to be send

5.3.89 reg_Capt_FSM_State_Info (is_2400_inp_sys_capt_unit_b_reg_Capt_FSM_State_Info)—Offset 8203Ch

Capture Unit State Machine Information

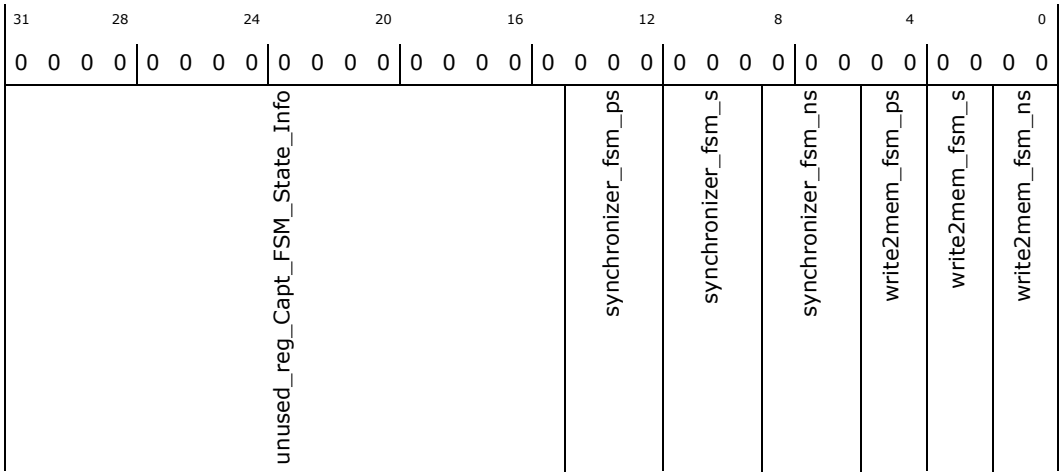
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8203Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:15	0x0 RO	**Reserved (unused_reg_Capt_FSM_State_Info):** Unused
14:12	0x0 RO	**synchronizer_fsm_ps:** Previous state of Synchronizer State Machine: 00=free run, 01=no sync, 10=sync sp, 11=sync lp, 100=sync wait
11:9	0x0 RO	**synchronizer_fsm_s:** Current state of Synchronizer State Machine: 00=free run, 01=no sync, 10=sync sp, 11=sync lp, 100=sync wait
8:6	0x0 RO	**synchronizer_fsm_ns:** Next state of Synchronizer State Machine: 00=free run, 01=no sync, 10=sync sp, 11=sync lp, 100=sync wait
5:4	0x0 RO	**write2mem_fsm_ps:** Previous state of Write2Mem State Machine: 00=idle, 01=buffer,11=write
3:2	0x0 RO	**write2mem_fsm_s:** Current state of Write2Mem State Machine: 00=idle, 01=buffer,11=write
1:0	0x0 RO	**write2mem_fsm_ns:** Next state of Write2Mem State Machine: 00=idle, 01=buffer,11=write

5.3.90 reg_CaptStartMode (is_2400_inp_sys_capt_unit_c_reg_CaptStartMode)—Offset 83000h

Synchronize on any packet header or on a frame start

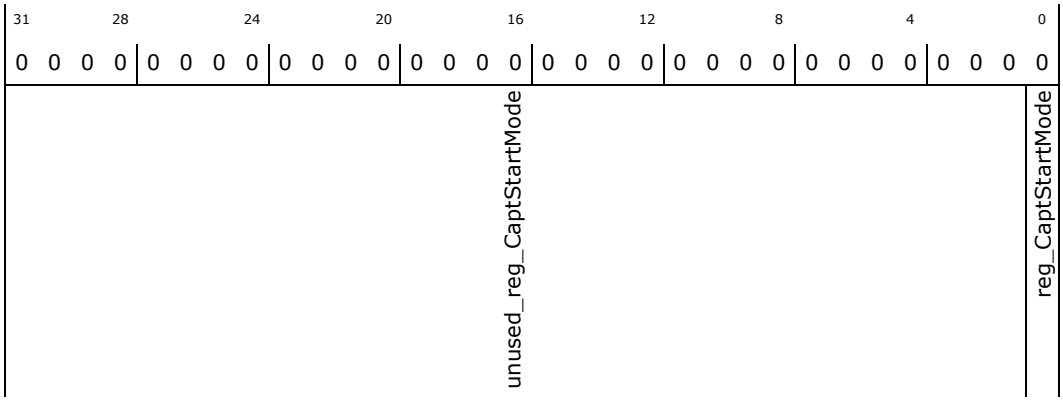
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 83000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_CaptStartMode):** Unused
0	0x0 RW	**reg_CaptStartMode:** Synchronize on any packet header or on a frame start

5.3.91 reg_Capt_Start_Addr (is_2400_inp_sys_capt_unit_c_reg_Capt_Start_Addr)—Offset 83004h

Start Address of first memory region

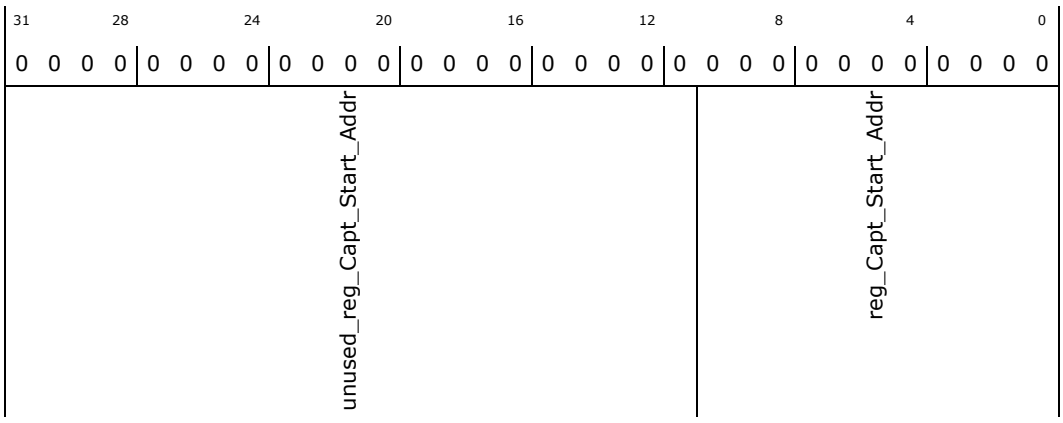
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 83004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:11	0x0 RW	**Reserved (unused_reg_Capt_Start_Addr):** Unused
10:0	0x0 RW	**reg_Capt_Start_Addr:** Start Address of first memory region

5.3.92 reg_Capt_Mem_Region_Size (is_2400_inp_sys_capt_unit_c_reg_Capt_Mem_Region_Size)—Offset 83008h

Memory region size

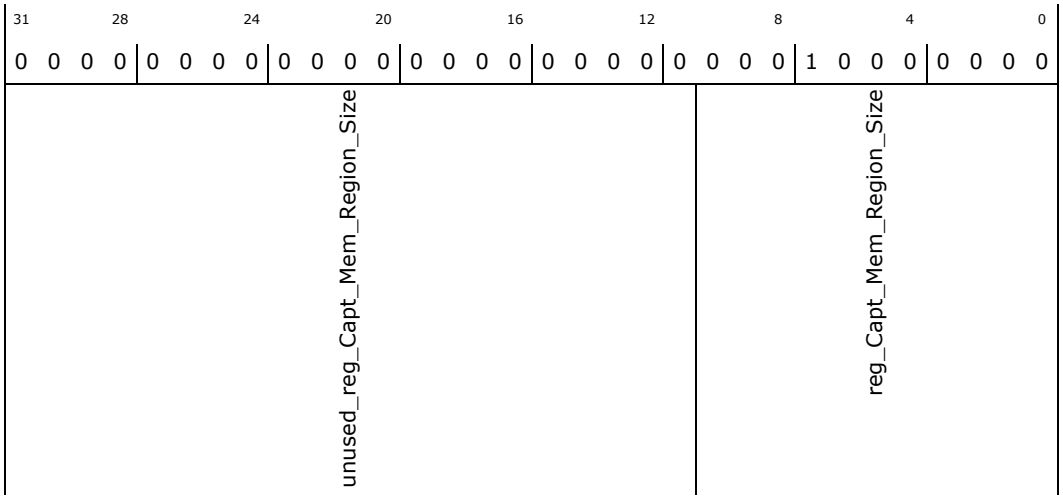
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 83008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h



Bit Range	Default and Access	Field Name (ID): Description
31:11	0x0 RW	**Reserved (unused_reg_Capt_Mem_Region_Size):** Unused
10:0	0x80 RW	**reg_Capt_Mem_Region_Size:** Memory region size

5.3.93 reg_Capt_Num_Mem_Regions (is_2400_inp_sys_capt_unit_c_reg_Capt_Num_Mem_Regions)—Offset 8300Ch

Number of memory regions

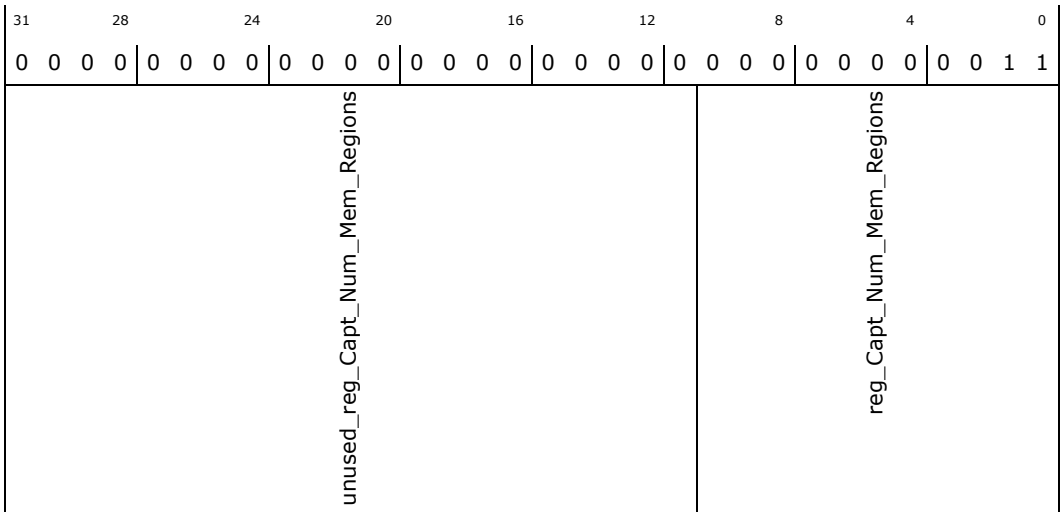
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8300Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h



Bit Range	Default and Access	Field Name (ID): Description
31:11	0x0 RW	**Reserved (unused_reg_Capt_Num_Mem_Regions):** Unused
10:0	0x3 RW	**reg_Capt_Num_Mem_Regions:** Number of memory regions

5.3.94 reg_Capt_Init (is_2400_inp_sys_capt_unit_c_reg_Capt_Init)—Offset 83010h

Initialize Capture Unit

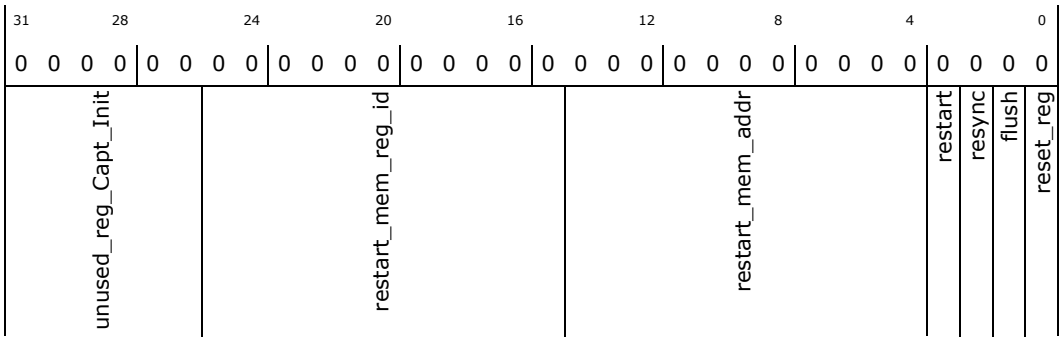
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 83010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:26	0x0 RO	**Reserved (unused_reg_Capt_Init):** Unused
25:15	0x0 WO	**restart_mem_reg_id:** Restart Memory Region ID
14:4	0x0 WO	**restart_mem_addr:** Restart Memory Address
3	0x0 WO	**restart:** Restart Capture Unit
2	0x0 WO	**resync:** Re-synchronize Capture Unit
1	0x0 WO	**flush:** Flush Internal Buffers
0	0x0 WO	**reset_reg:** Reset Status Registers

5.3.95 reg_Capt_Start (is_2400_inp_sys_capt_unit_c_reg_Capt_Start)—Offset 83014h

Start Capturing

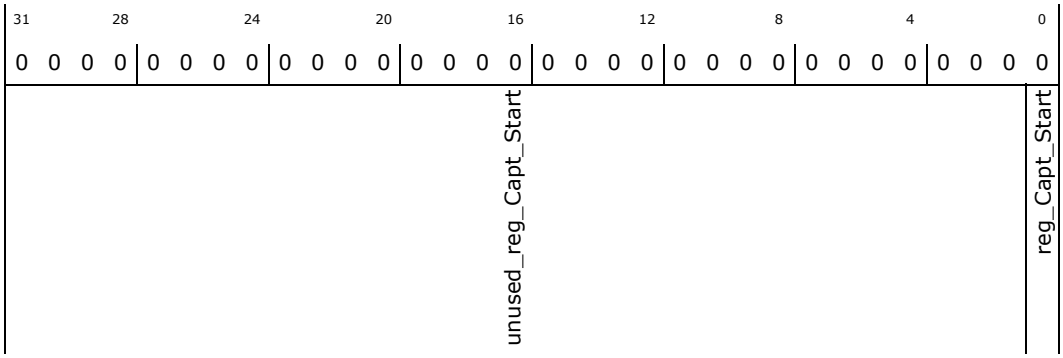
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 83014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_Capt_Start):** Unused
0	0x0 WO	**reg_Capt_Start:** Start Capturing

5.3.96 reg_Capt_Stop (is_2400_inp_sys_capt_unit_c_reg_Capt_Stop)—Offset 83018h

Stop Capturing

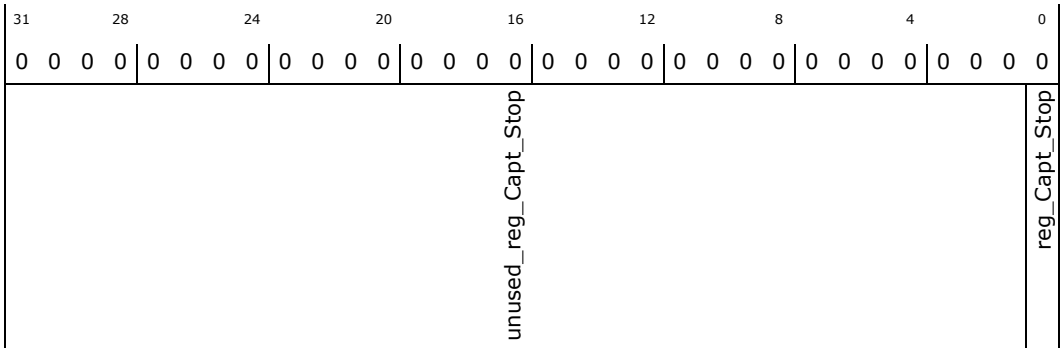
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 83018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_Capt_Stop):** Unused
0	0x0 WO	**reg_Capt_Stop:** Stop Capturing

5.3.97 reg_Capt_Packet_Length (is_2400_inp_sys_capt_unit_c_reg_Capt_Packet_Length)—Offset 8301Ch

Packet length of multi_word packet (MWP) as decoded from packet header

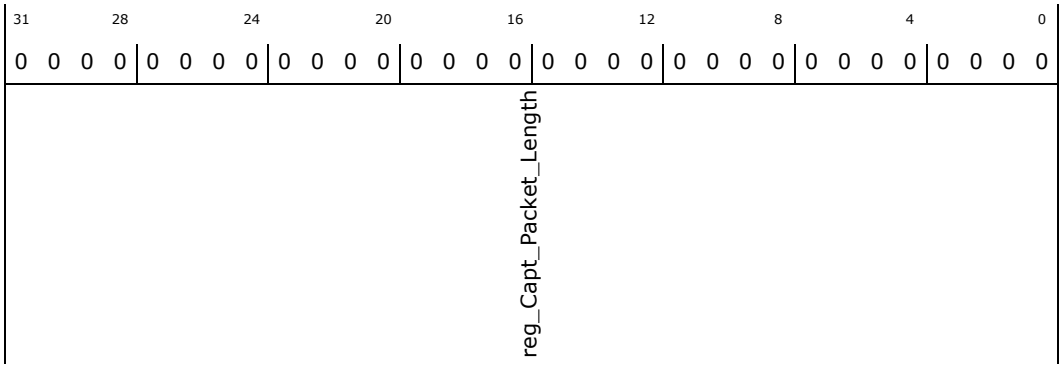
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8301Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**reg_Capt_Packet_Length:** Packet length of multi_word packet (MWP) as decoded from packet header

5.3.98 reg_Capt_Received_Length (is_2400_inp_sys_capt_unit_c_reg_Capt_Received_Length)—Offset 83020h

(Incremental) received packet length of current multi-word packet (MWP)

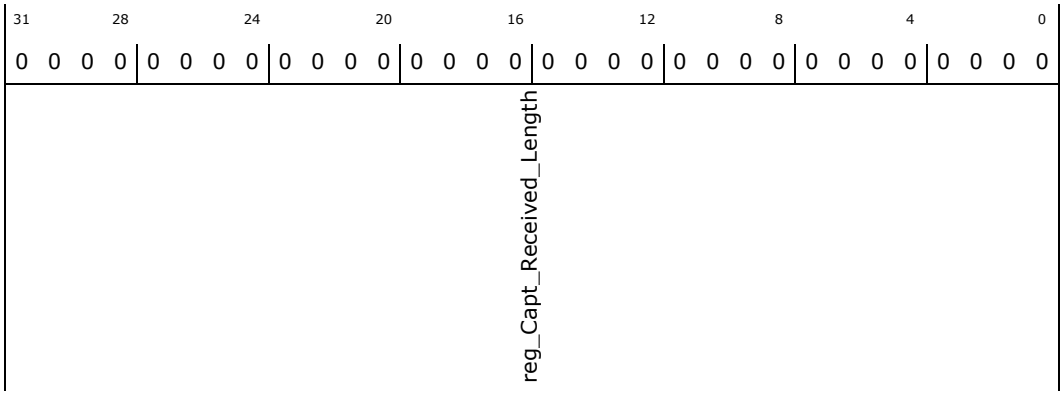
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 83020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**reg_Capt_Received_Length:** (Incremental) received packet length of current multi-word packet (MWP)

5.3.99 reg_Capt_Received_Short_Packets (is_2400_inp_sys_capt_unit_c_reg_Capt_Received_Short_Packets)—Offset 83024h

Number of received short packets

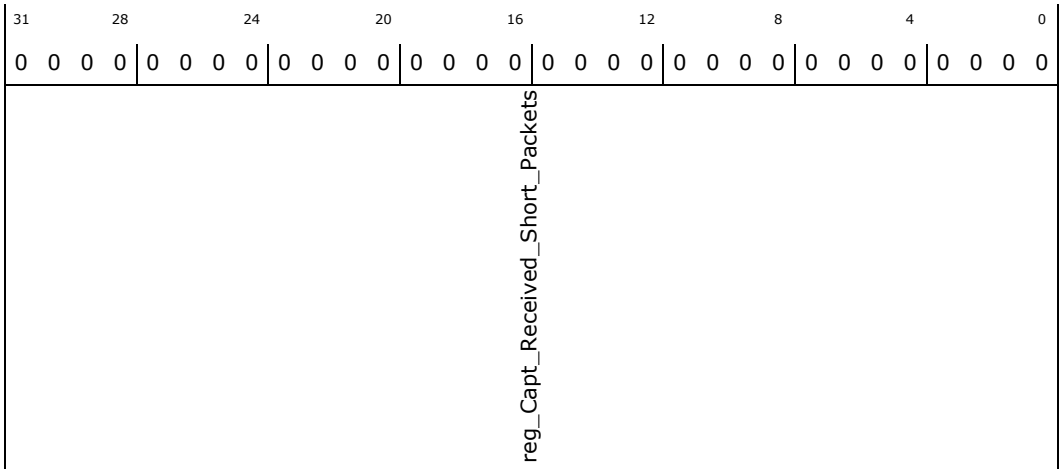
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 83024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**reg_Capt_Received_Short_Packets:** Number of received short packets

5.3.100 reg_Capt_Received_Long_Packets (is_2400_inp_sys_capt_unit_c_reg_Capt_Received_Long_Packets)—Offset 83028h

Number of received long packets

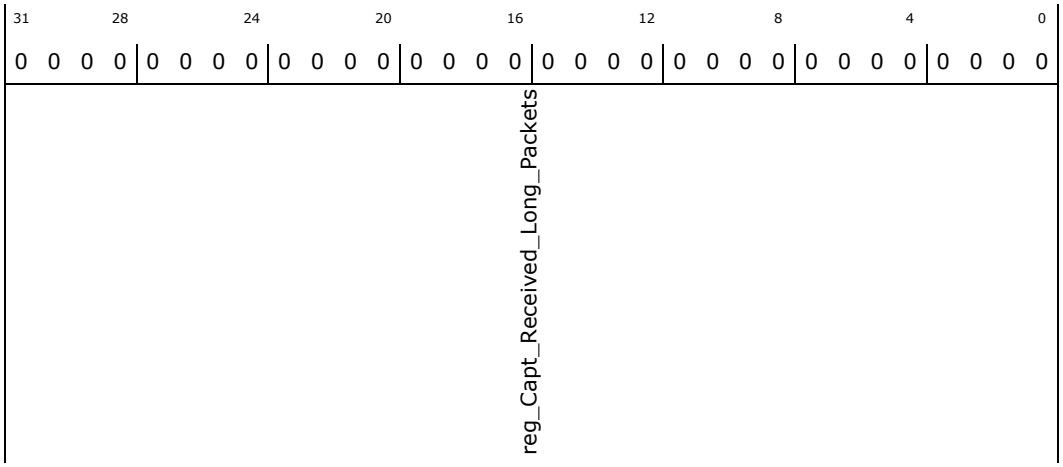
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 83028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**reg_Capt_Received_Long_Packets:** Number of received long packets

5.3.101 reg_Capt_Last_Command (is_2400_inp_sys_capt_unit_c_reg_Capt_Last_Command)—Offset 8302Ch

Last command token accepted

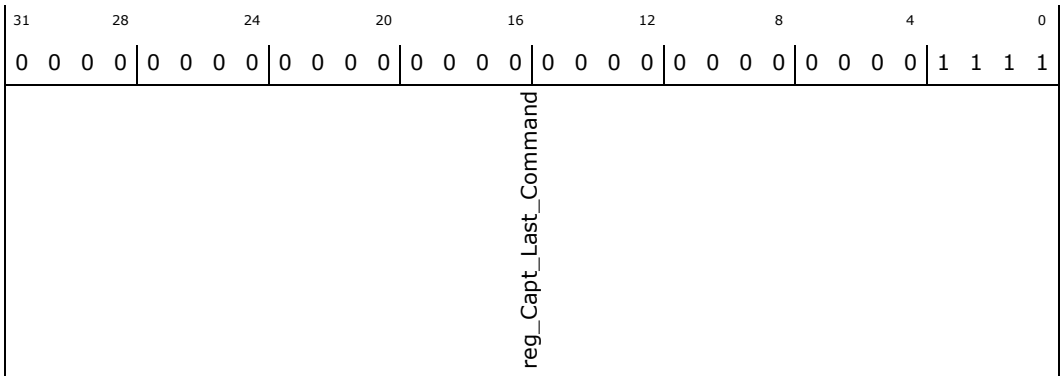
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8302Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**reg_Capt_Last_Command:** Last command token accepted

5.3.102 reg_Capt_Next_Command (is_2400_inp_sys_capt_unit_c_reg_Capt_Next_Command)—Offset 83030h

Next command token to be accepted

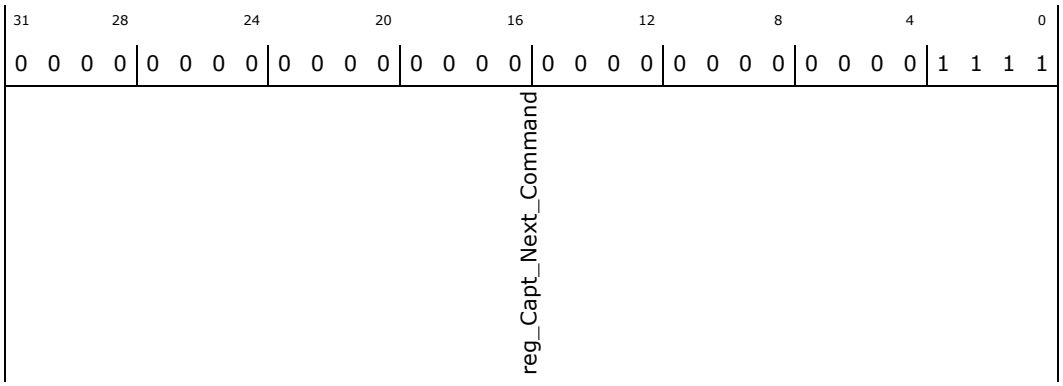
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 83030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**reg_Capt_Next_Command:** Next command token to be accepted

5.3.103 reg_Capt_Last_Acknowledge (is_2400_inp_sys_capt_unit_c_reg_Capt_Last_Acknowledge)—Offset 83034h

Last acknowledge token send

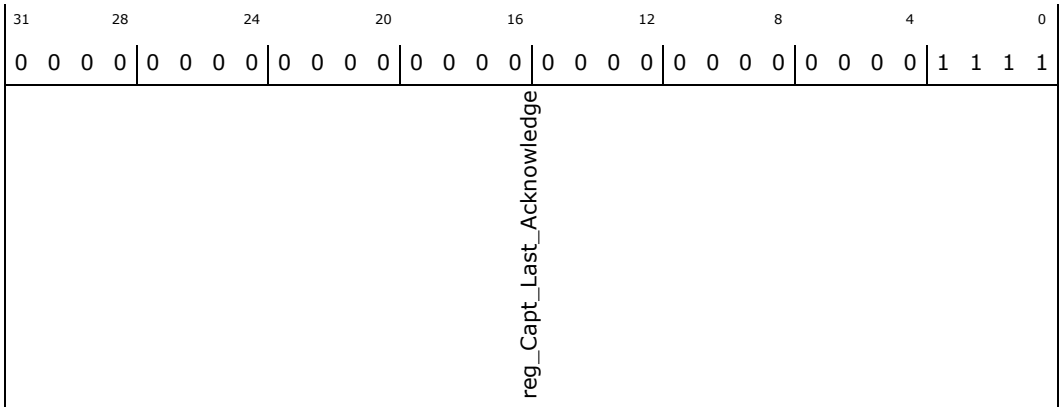
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 83034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**reg_Capt_Last_Acknowledge:** Last acknowledge token send

5.3.104 reg_Capt_Next_Acknowledge (is_2400_inp_sys_capt_unit_c_reg_Capt_Next_Acknowledge)—Offset 83038h

Next acknowledge token to be send

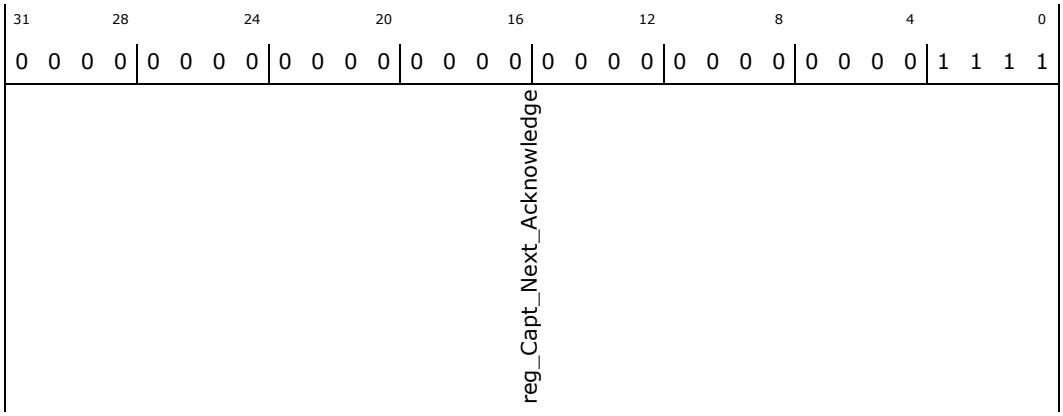
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 83038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**reg_Capt_Next_Acknowledge:** Next acknowledge token to be send

5.3.105 reg_Capt_FSM_State_Info (is_2400_inp_sys_capt_unit_c_reg_Capt_FSM_State_Info)—Offset 8303Ch

Capture Unit State Machine Information

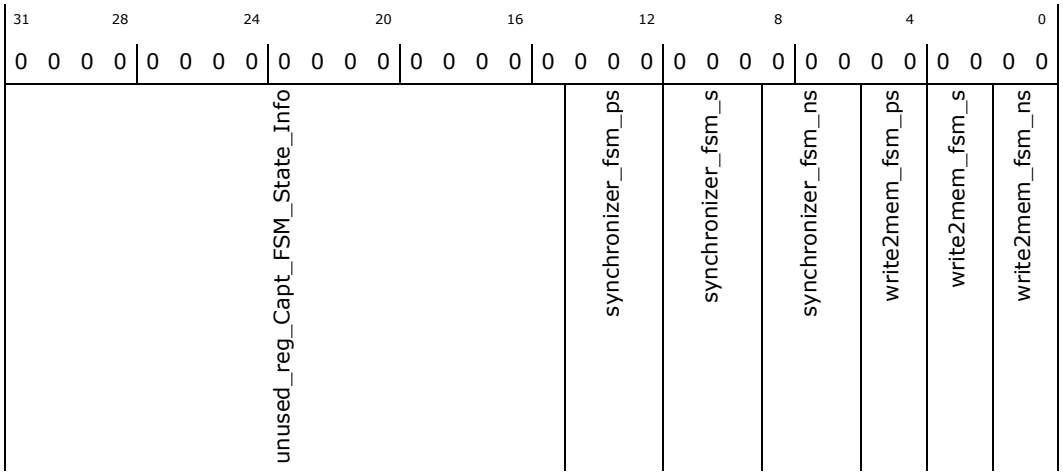
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8303Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:15	0x0 RO	**Reserved (unused_reg_Capt_FSM_State_Info):** Unused
14:12	0x0 RO	**synchronizer_fsm_ps:** Previous state of Synchronizer State Machine: 00=free run, 01=no sync, 10=sync sp, 11=sync lp, 100=sync wait
11:9	0x0 RO	**synchronizer_fsm_s:** Current state of Synchronizer State Machine: 00=free run, 01=no sync, 10=sync sp, 11=sync lp, 100=sync wait
8:6	0x0 RO	**synchronizer_fsm_ns:** Next state of Synchronizer State Machine: 00=free run, 01=no sync, 10=sync sp, 11=sync lp, 100=sync wait
5:4	0x0 RO	**write2mem_fsm_ps:** Previous state of Write2Mem State Machine: 00=idle, 01=buffer,11=write
3:2	0x0 RO	**write2mem_fsm_s:** Current state of Write2Mem State Machine: 00=idle, 01=buffer,11=write
1:0	0x0 RO	**write2mem_fsm_ns:** Next state of Write2Mem State Machine: 00=idle, 01=buffer,11=write

5.3.106 reg_Acq_Start_Addr (is_2400_inp_sys_acq_unit_reg_Acq_Start_Addr)—Offset 84000h

Start Address of first memory region

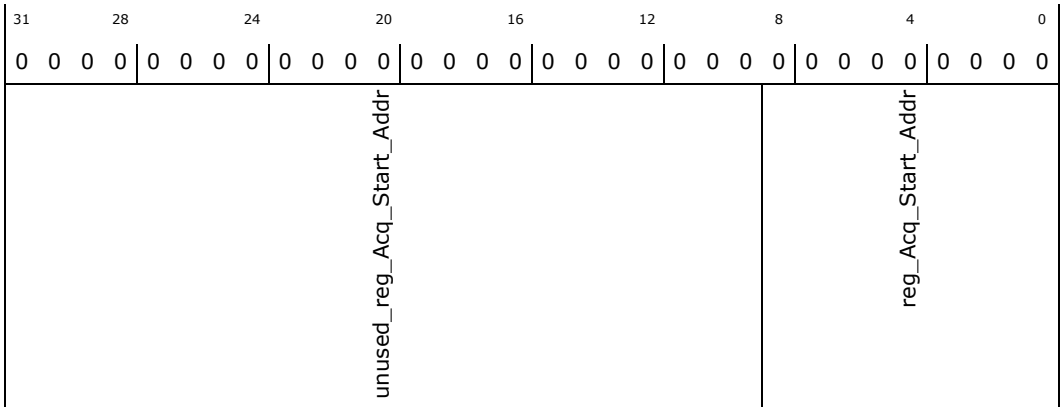
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 84000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved (unused_reg_Acq_Start_Addr):** Unused
8:0	0x0 RW	**reg_Acq_Start_Addr:** Start Address of first memory region

5.3.107 reg_Acq_Mem_Region_Size (is_2400_inp_sys_acq_unit_reg_Acq_Mem_Region_Size) —Offset 84004h

Memory region size

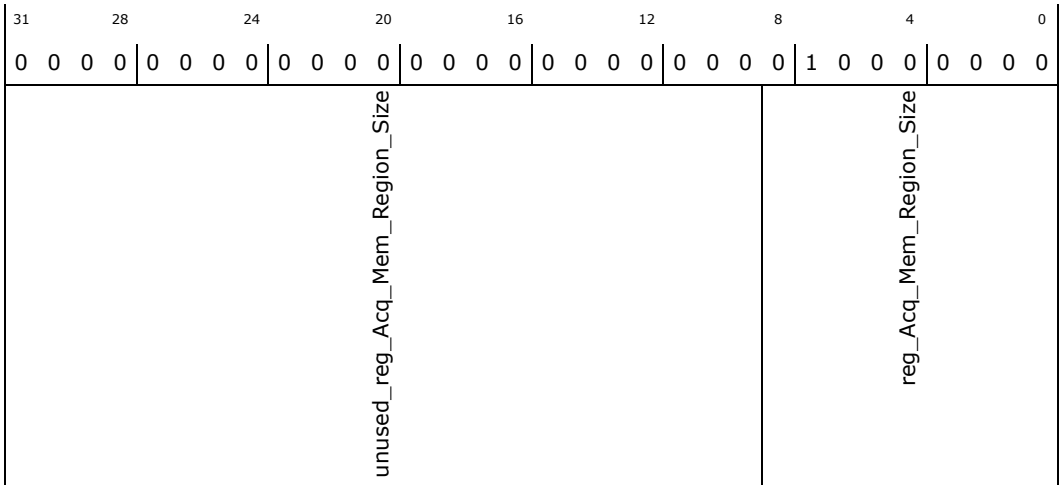
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 84004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h



Bit Range	Default and Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved (unused_reg_Acq_Mem_Region_Size):** Unused
8:0	0x80 RW	**reg_Acq_Mem_Region_Size:** Memory region size

5.3.108 reg_Acq_Num_Mem_Regions (is_2400_inp_sys_acq_unit_reg_Acq_Num_Mem_Regions)—Offset 84008h

Number of memory regions

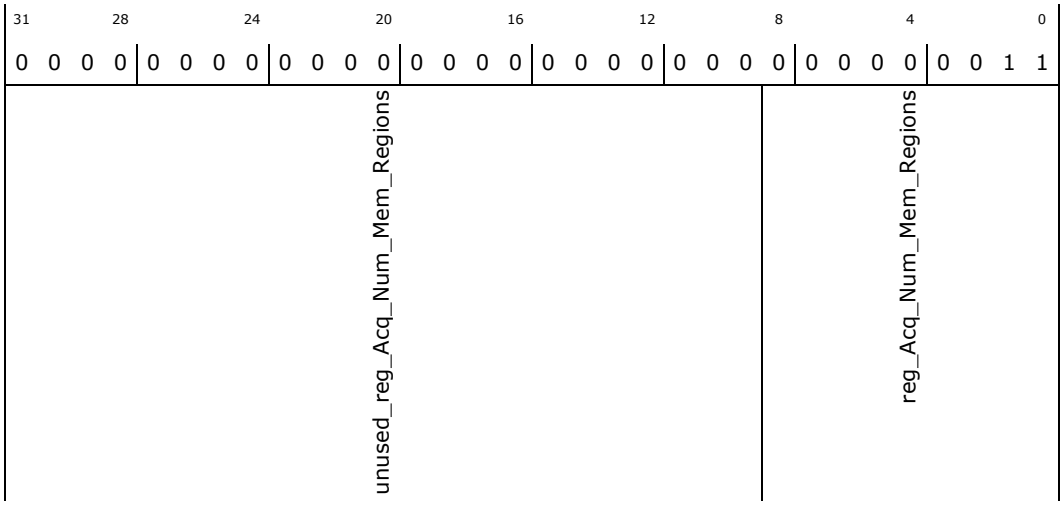
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 84008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h



Bit Range	Default and Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved (unused_reg_Acq_Num_Mem_Regions):** Unused
8:0	0x3 RW	**reg_Acq_Num_Mem_Regions:** Number of memory regions

5.3.109 reg_Acq_Init (is_2400_inp_sys_acq_unit_reg_Acq_Init)—Offset 8400Ch

Initialize Acquisition Unit

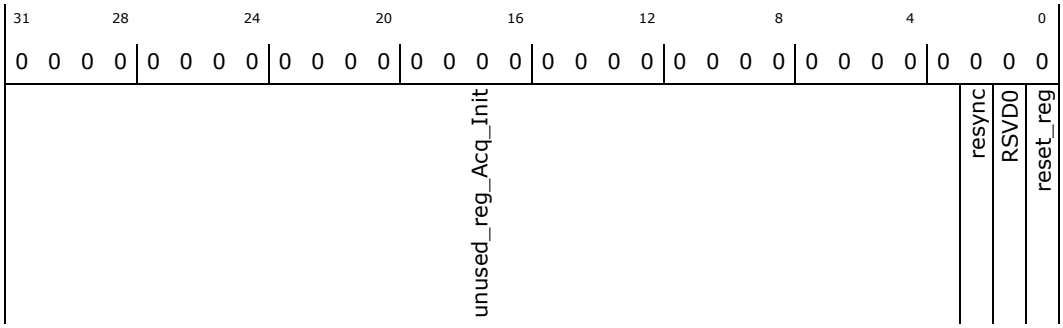
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8400Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:3	0x0 RO	**Reserved (unused_reg_Acq_Init):** Unused
2	0x0 WO	**resync:** Re-synchronize the Acquisition Unit
1	0x0 RO	**RSVD0:** Reserved
0	0x0 WO	**reset_reg:** Reset Status Registers

5.3.110 reg_Acq_Received_Short_Packets (is_2400_inp_sys_acq_unit_reg_Acq_Received_Short_Packets)—Offset 84010h

Number of received short packets

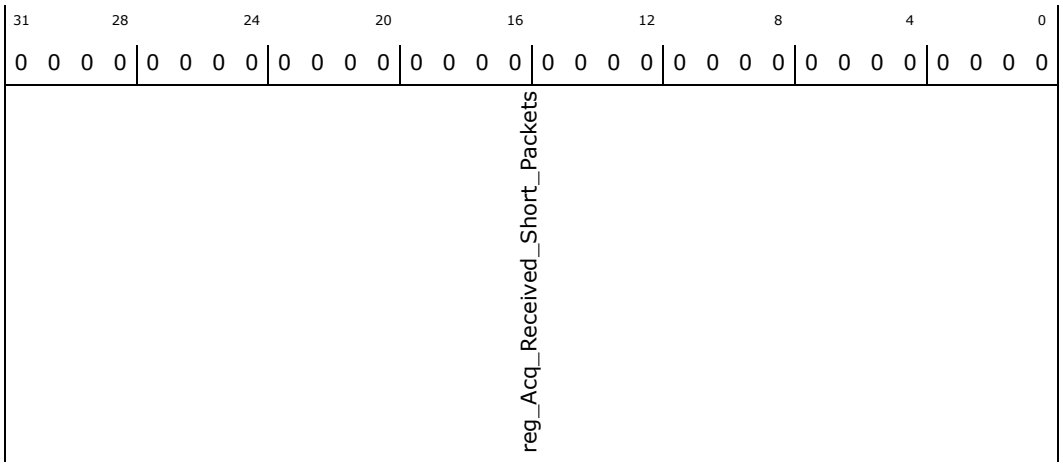
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 84010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**reg_Acq_Received_Short_Packets:** Number of received short packets

5.3.111 reg_Acq_Received_Long_Packets (is_2400_inp_sys_acq_unit_reg_Acq_Received_Long_Packets)—Offset 84014h

Number of received long packets

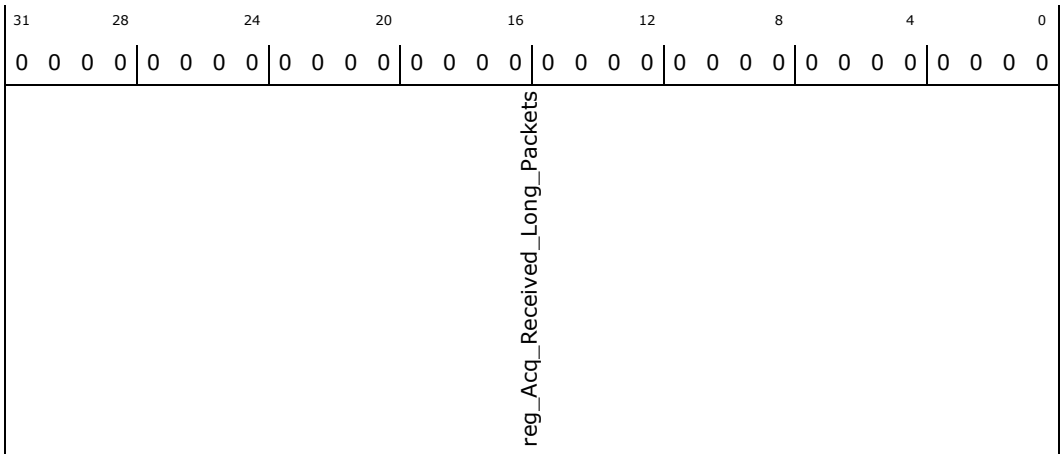
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 84014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**reg_Acq_Received_Long_Packets:** Number of received long packets

5.3.112 reg_Acq_Last_Command (is_2400_inp_sys_acq_unit_reg_Acq_Last_Command)—Offset 84018h

Last command token accepted

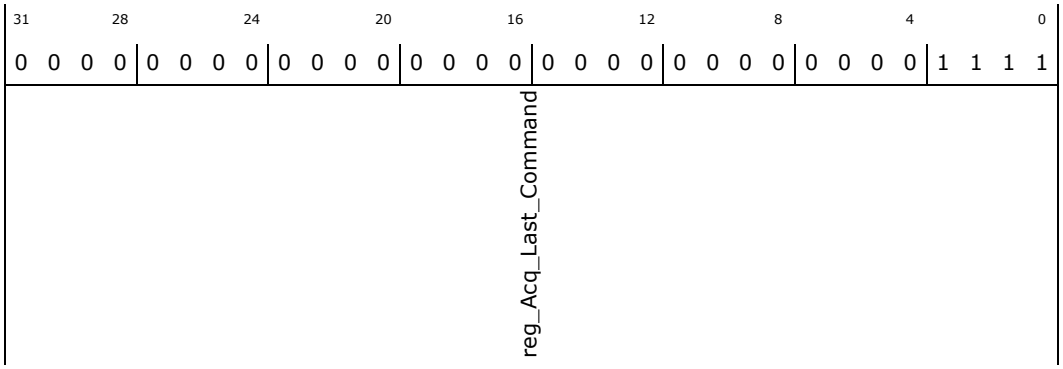
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 84018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**reg_Acq_Last_Command:** Last command token accepted

5.3.113 reg_Acq_Next_Command (is_2400_inp_sys_acq_unit_reg_Acq_Next_Command)—Offset 8401Ch

Next command token to be accepted

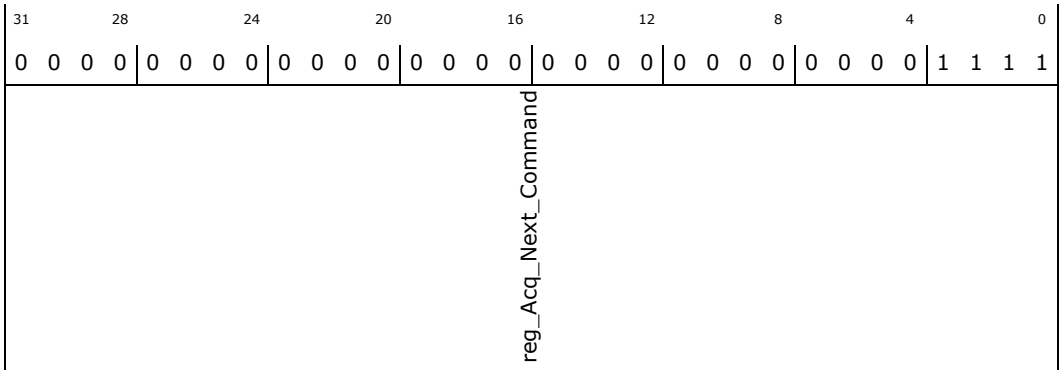
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8401Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**reg_Acq_Next_Command:** Next command token to be accepted

5.3.114 reg_Acq_Last_Acknowledge (is_2400_inp_sys_acq_unit_reg_Acq_Last_Acknowledge)—Offset 84020h

Last acknowledge token send

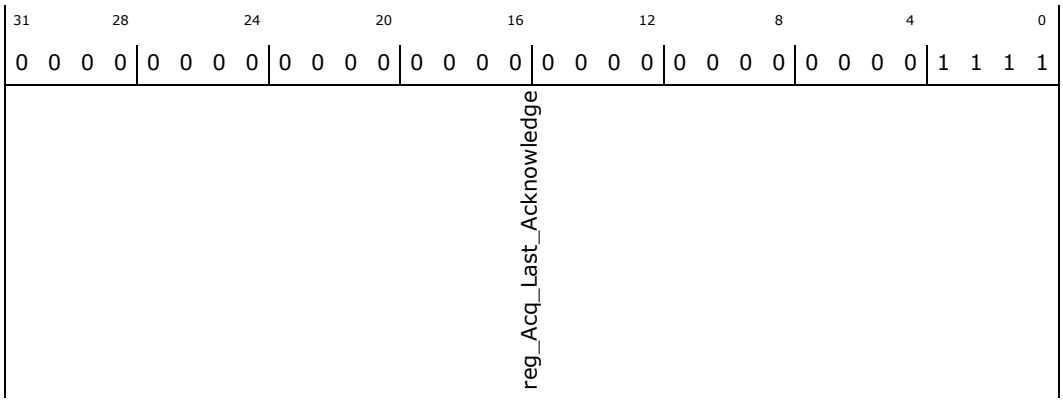
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 84020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**reg_Acq_Last_Acknowledge:** Last acknowledge token send

5.3.115 reg_Acq_Next_Acknowledge (is_2400_inp_sys_acq_unit_reg_Acq_Next_Acknowledge)—Offset 84024h

Next acknowledge token to be send

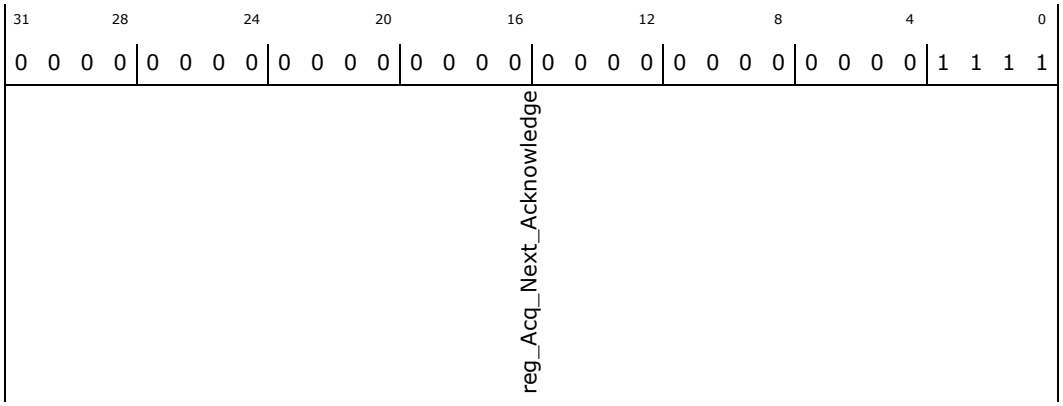
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 84024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**reg_Acq_Next_Acknowledge:** Next acknowledge token to be send

5.3.116 reg_Acq_FSM_State_Info (is_2400_inp_sys_acq_unit_reg_Acq_FSM_State_Info)—Offset 84028h

Acquisition unit State Machine information

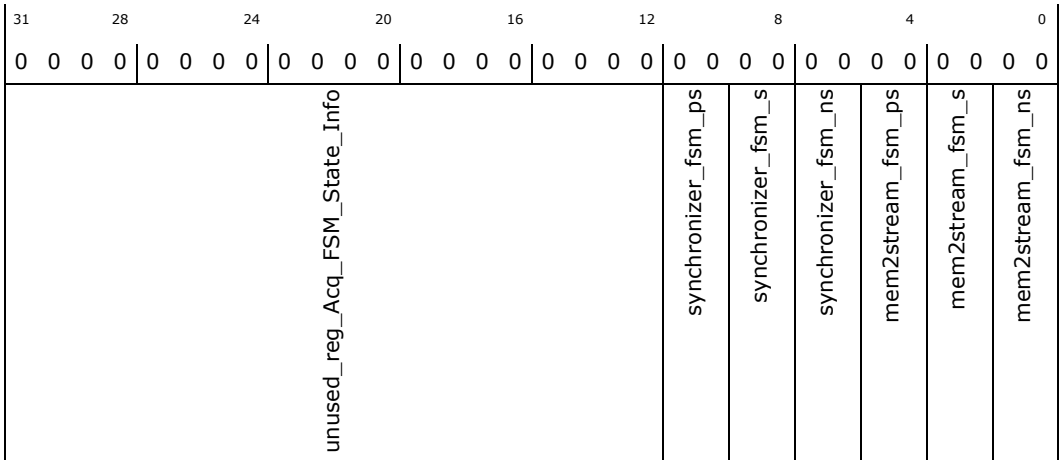
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 84028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved (unused_reg_Acq_FSM_State_Info):** Unused
11:10	0x0 RO	**synchronizer_fsm_ps:** Previous state of Synchronizer State Machine
9:8	0x0 RO	**synchronizer_fsm_s:** Current state of Synchronizer State Machine
7:6	0x0 RO	**synchronizer_fsm_ns:** Next state of Synchronizer State Machine
5:4	0x0 RO	**mem2stream_fsm_ps:** Previous state of Mem2Stream State Machine
3:2	0x0 RO	**mem2stream_fsm_s:** Current state of Mem2Stream State Machine
1:0	0x0 RO	**mem2stream_fsm_ns:** Next state of Mem2Stream State Machine

5.3.117 reg_Acq_Int_Cntr_Info (is_2400_inp_sys_acq_unit_reg_Acq_Int_Cntr_Info)—Offset 8402Ch

Acq_Int_Cntr_Info

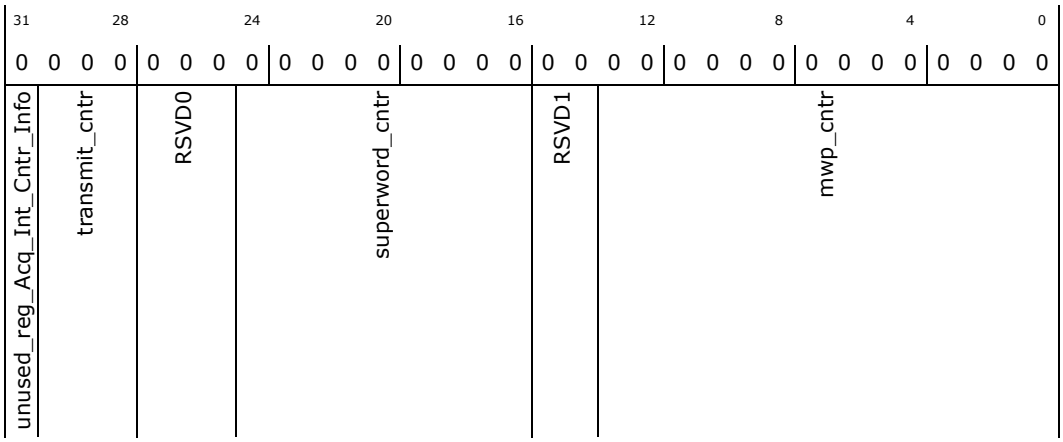
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8402Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RO	**Reserved (unused_reg_Acq_Int_Cntr_Info):** Unused
30:28	0x0 RO	**transmit_cntr:** Counter used for determining which word (part of a super word) to be send
27:25	0x0 RO	**RSVD0:** Reserved
24:16	0x0 RO	**superword_cntr:** Counts number of super words read from wide bus (input buffer)
15:14	0x0 RO	**RSVD1:** Reserved
13:0	0x0 RO	**mwp_cntr:** Counts words in multi word packet

5.3.118 DMA_FSM_Command (is_2400_inp_sys_dma_DMA_FSM_Command)—Offset 85000h

FSM Command: Last command and State

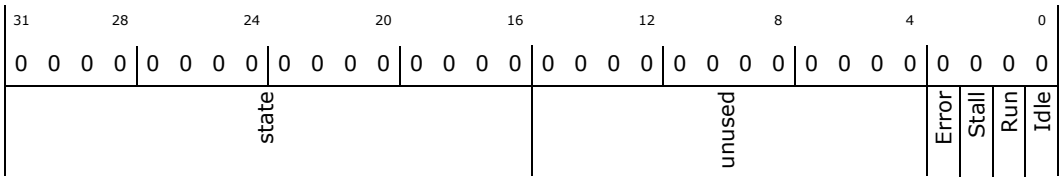
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 85000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RO	**state:** Lower 16 bits of the last command received and processed
15:4	0x0 RO	**unused:** unused
3	0x0 RO	**Error:** Error flag
2	0x0 RO	**Stall:** Stall flag
1	0x0 RO	**Run:** Run flag

Bit Range	Default and Access	Field Name (ID): Description
0	0x0 RO	**Idle:** Idle flag

5.3.119 DMA_CH0_Packing_setup (is_2400_inp_sys_dma_DMA_CH0_Packing_setup)—Offset 86000h

DMA CH 0 PARAM 0: Packing setup

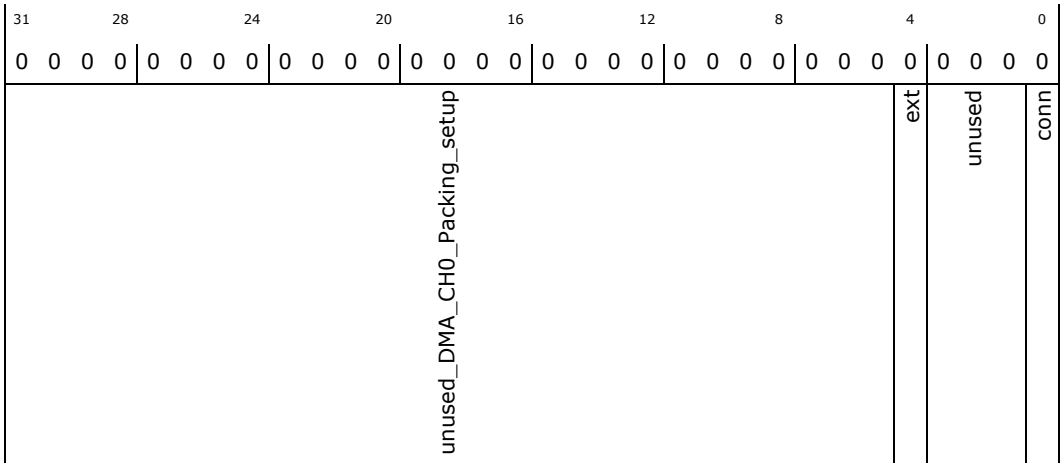
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 86000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RO	**Reserved (unused_DMA_CH0_Packing_setup):** Unused
4	0x0 RO	**ext:** Zero(0)/Sign(1) extension
3:1	0x0 RO	**unused:** unused
0	0x0 RO	**conn:** Connection ID

5.3.120 DMA_CH0_dev_stride_A (is_2400_inp_sys_dma_DMA_CH0_dev_stride_A)—Offset 86100h

DMA CH 0 PARAM 1: Device A stride

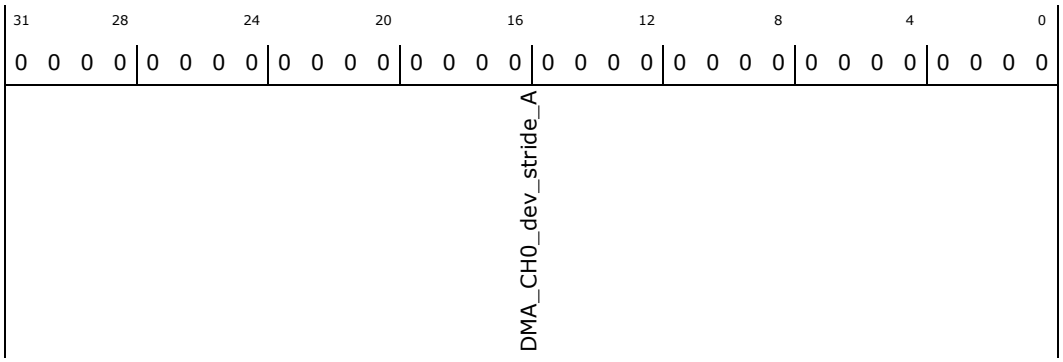
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 86100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH0_dev_stride_A:** DMA CH 0 PARAM 1: Device A stride

5.3.121 DMA_CH0_dev_Pack_left_crop_and_elem_A (is_2400_inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_A)—Offset 86200h

DMA CH 0 PARAM 2: Device A Packing LSE cropping/Elements

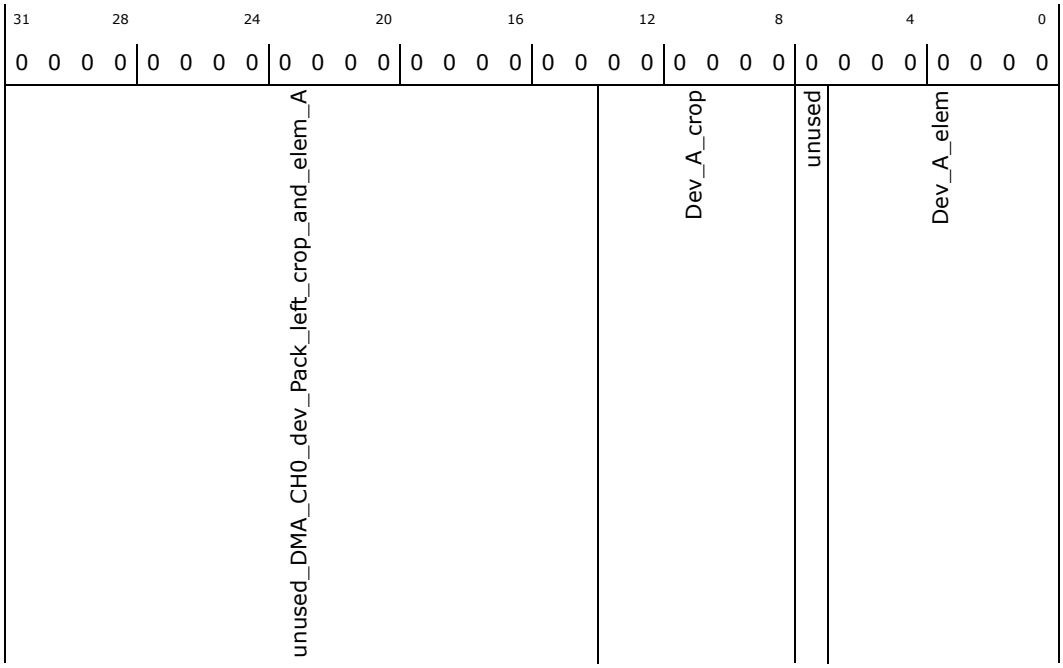
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 86200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH0_dev_Pack_left_crop_and_elem_A):** Unused
13:8	0x0 RO	**Dev_A_crop:** Device A left element cropping
7	0x0 RO	**unused:** unused
6:0	0x0 RO	**Dev_A_elem:** Device A element per word

5.3.122 DMA_CH0_Device_Xb_A (is_2400_inp_sys_dma_DMA_CH0_Device_Xb_A)—Offset 86300h

DMA CH 0 PARAM 3: Device A block width (Xb)

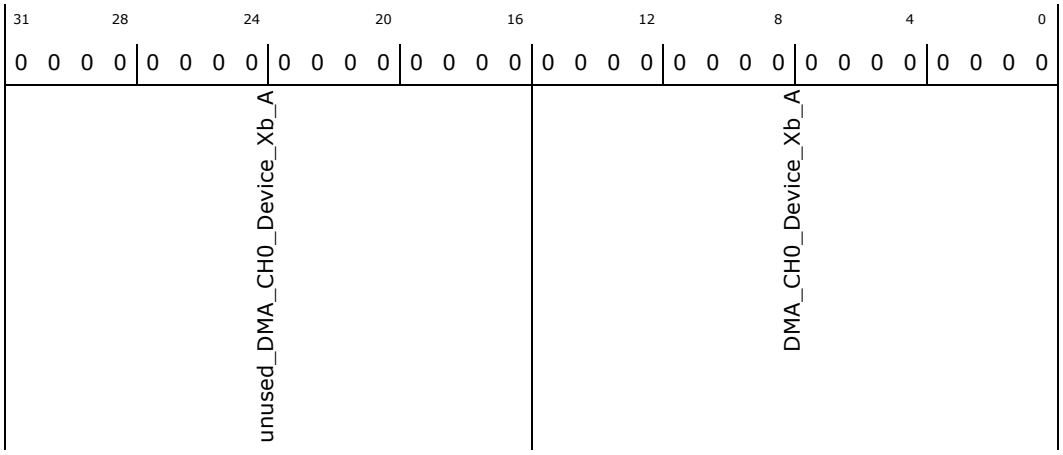
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 86300h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH0_Device_Xb_A):** Unused
15:0	0x0 RO	**DMA_CH0_Device_Xb_A:** DMA CH 0 PARAM 3: Device A block width (Xb)

5.3.123 DMA_CH0_dev_stride_B (is_2400_inp_sys_dma_DMA_CH0_dev_stride_B)—Offset 86400h

DMA CH 0 PARAM 4: Device B stride

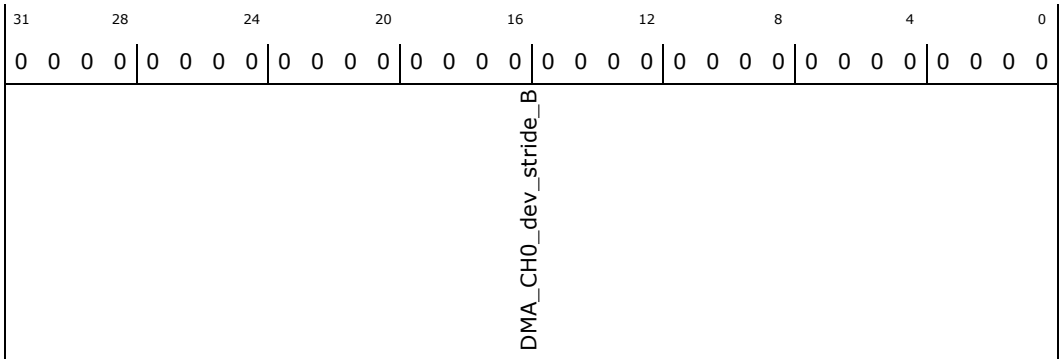
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 86400h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_CH0_dev_stride_B:** DMA CH 0 PARAM 4: Device B stride

5.3.124 DMA_CH0_dev_Pack_left_crop_and_elem_B (is_2400_inp_sys_dma_DMA_CH0_dev_Pack_left_crop_and_elem_B)—Offset 86500h

DMA CH 0 PARAM 5: Device B Packing LSE cropping/Elements

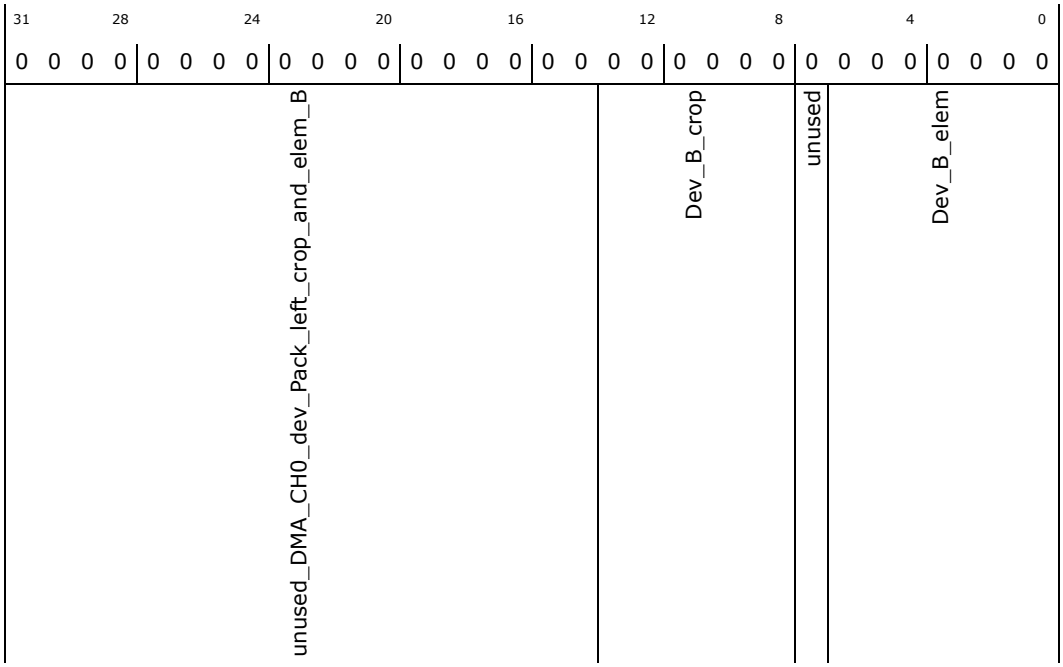
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 86500h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (unused_DMA_CH0_dev_Pack_left_crop_and_elem_B):** Unused
13:8	0x0 RO	**Dev_B_crop:** Device B left element cropping

Bit Range	Default and Access	Field Name (ID): Description
7	0x0 RO	**unused:** unused
6:0	0x0 RO	**Dev_B_elem:** Device B element per word

5.3.125 DMA_CH0_Device_Xb_B (is_2400_inp_sys_dma_DMA_CH0_Device_Xb_B)—Offset 86600h

DMA CH 0 PARAM 6: Device B block width (Xb)

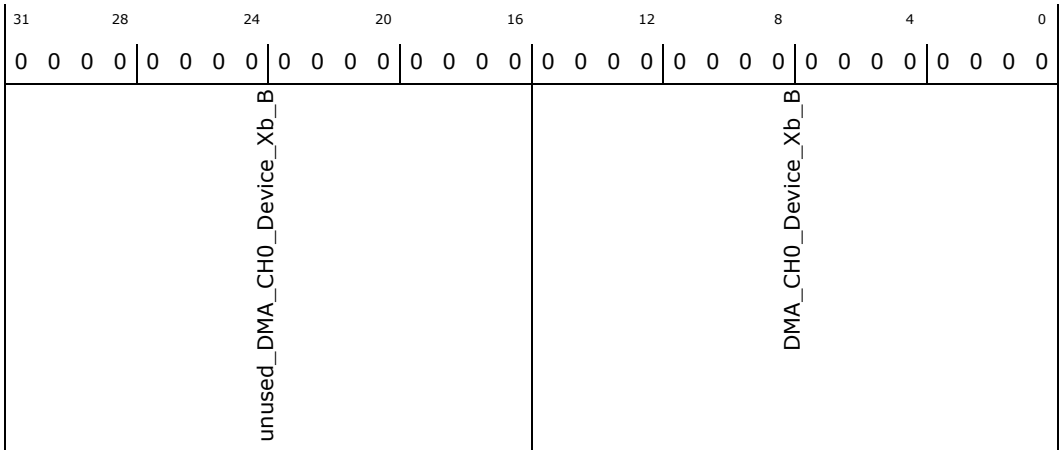
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 86600h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH0_Device_Xb_B):** Unused
15:0	0x0 RO	**DMA_CH0_Device_Xb_B:** DMA CH 0 PARAM 6: Device B block width (Xb)

5.3.126 DMA_CH0_Yb (is_2400_inp_sys_dma_DMA_CH0_Yb)—Offset 86700h

DMA CH 0 PARAM 7: block Height (Yb)

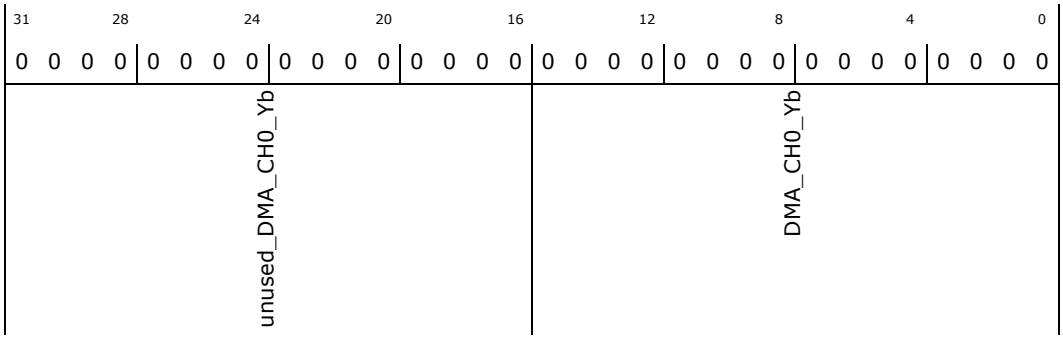
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 86700h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_CH0_Yb):** Unused
15:0	0x0 RO	**DMA_CH0_Yb:** DMA CH 0 PARAM 7: block Height (Yb)

5.3.127 DMA_CH0_pending_command (is_2400_inp_sys_dma_DMA_CH0_pending_command)—Offset 86800h

DMA CH 0 PARAM 8: Pending commands which will use channel 0

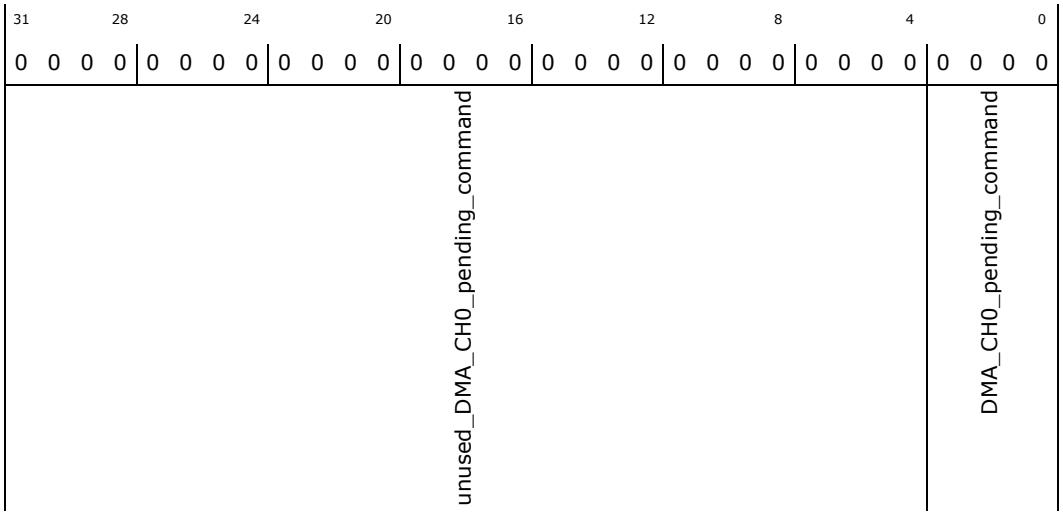
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 86800h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RW	**Reserved (unused_DMA_CH0_pending_command):** Unused
3:0	0x0 RO	**DMA_CH0_pending_command:** DMA CH 0 PARAM 8: Pending commands which will use channel 0

5.3.128 DMA_command_token (is_2400_inp_sys_dma_DMA_command_token)—Offset 87000h

Pending or last executed command token

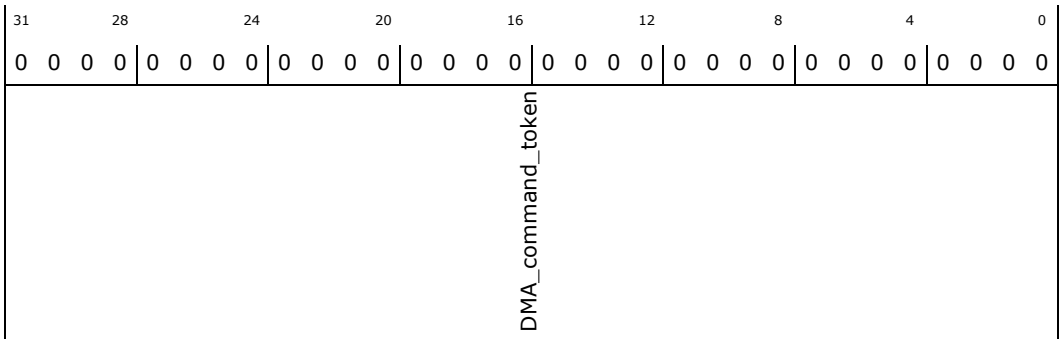
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_command_token:** Pending or last executed command token

5.3.129 DMA_command_src_addr (is_2400_inp_sys_dma_DMA_command_src_addr)—Offset 87004h

Source address of the pending or last executed command token

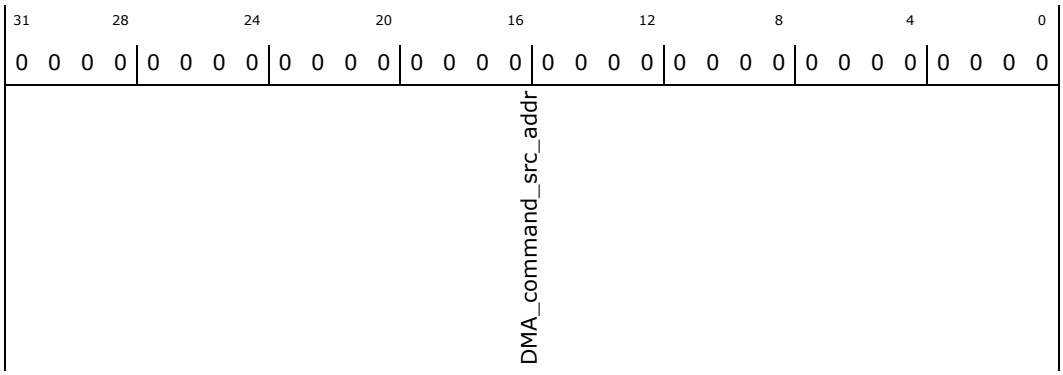
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_command_src_addr:** Source address of the pending or last executed command token

5.3.130 DMA_command_dst_addr (is_2400_inp_sys_dma_DMA_command_dst_addr)—Offset 87008h

Destination address of the pending or last executed command token

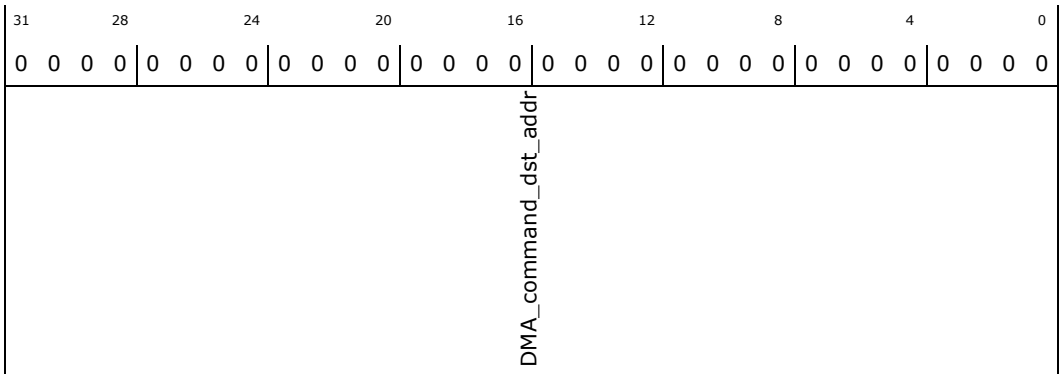
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_command_dst_addr:** Destination address of the pending or last executed command token

5.3.131 DMA_command_ctrl_id (is_2400_inp_sys_dma_DMA_command_ctrl_id)—Offset 8700Ch

Controller id of the pending or last executed command token

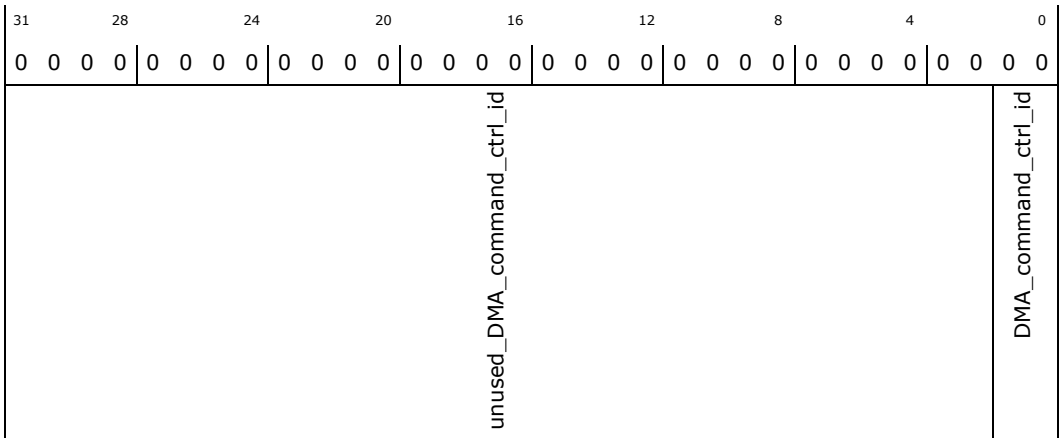
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8700Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_DMA_command_ctrl_id):** Unused
1:0	0x0 RO	**DMA_command_ctrl_id:** Controller id of the pending or last executed command token

5.3.132 DMA_FSM_Ctrl_status (is_2400_inp_sys_dma_DMA_FSM_Ctrl_status)—Offset 87010h

DMA FSM Control state and flags

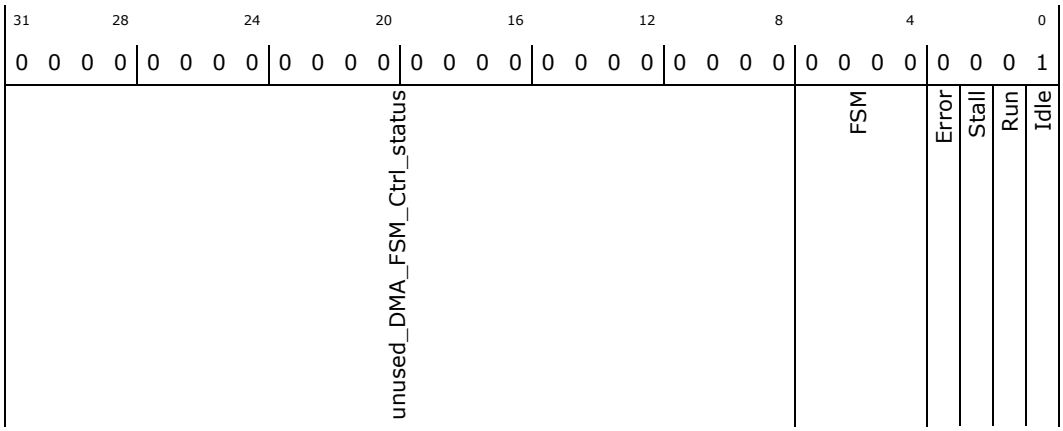
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (unused_DMA_FSM_Ctrl_status):** Unused
7:4	0x0 RO	**FSM:** FSM control state: 0)Idle -- 1)req_rcv -- 2)rcv -- 3)rcv_req -- 4)INIT
3	0x0 RO	**Error:** Error flag
2	0x0 RO	**Stall:** Stall flag
1	0x0 RO	**Run:** Run flag

Bit Range	Default and Access	Field Name (ID): Description
0	0x1 RO	**Idle:** Idle flag

5.3.133 DMA_FSM_Pack_status (is_2400_inp_sys_dma_DMA_FSM_Pack_status)—Offset 87014h

DMA FSM Pack state

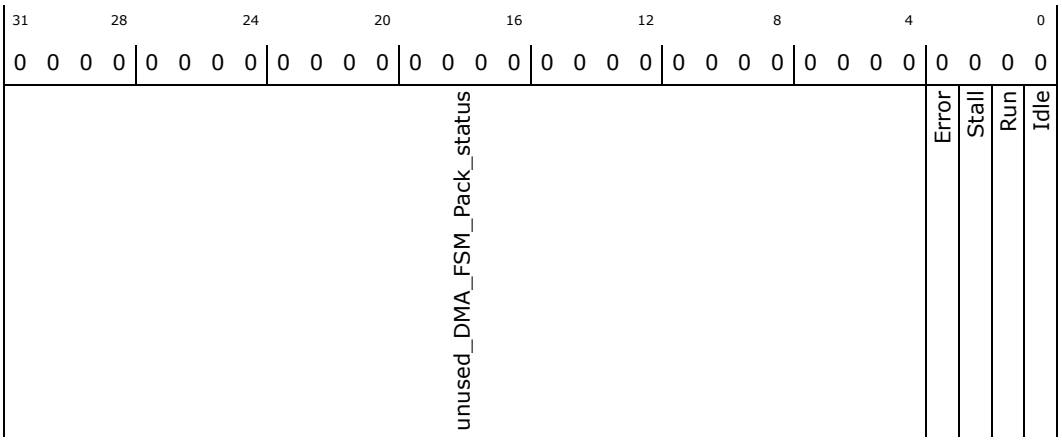
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_DMA_FSM_Pack_status):** Unused
3	0x0 RO	**Error:** Error flag
2	0x0 RO	**Stall:** Stall flag
1	0x0 RO	**Run:** Run flag
0	0x0 RO	**Idle:** Idle flag

5.3.134 DMA_FSM_request_status (is_2400_inp_sys_dma_DMA_FSM_request_status)—Offset 87018h

DMA FSM Request state: 0)Idle -- 1)req -- 2)Next line

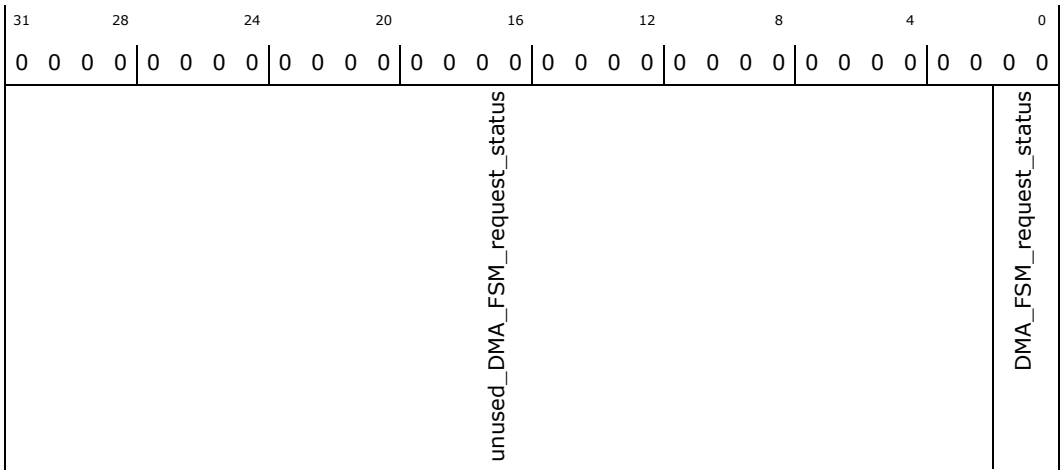
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_DMA_FSM_request_status):** Unused
1:0	0x0 RO	**DMA_FSM_request_status:** DMA FSM Request state: 0)Idle -- 1)req -- 2)Next line

5.3.135 DMA_FSM_write_status (is_2400_inp_sys_dma_DMA_FSM_write_status)—Offset 8701Ch

DMA FSM Write state: 0)Idle -- 1)req -- 2)Next line

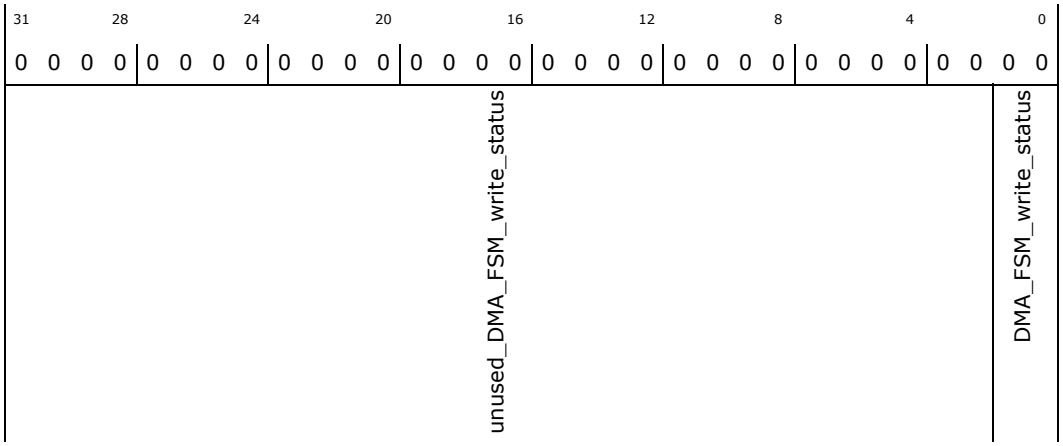
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8701Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_DMA_FSM_write_status):** Unused
1:0	0x0 RO	**DMA_FSM_write_status:** DMA FSM Write state: 0)Idle -- 1)req -- 2)Next line

5.3.136 DMA_FSM_Ctrl_dev_idx (is_2400_inp_sys_dma_DMA_FSM_Ctrl_dev_idx)—Offset 87110h

DMA FSM Control request device idx

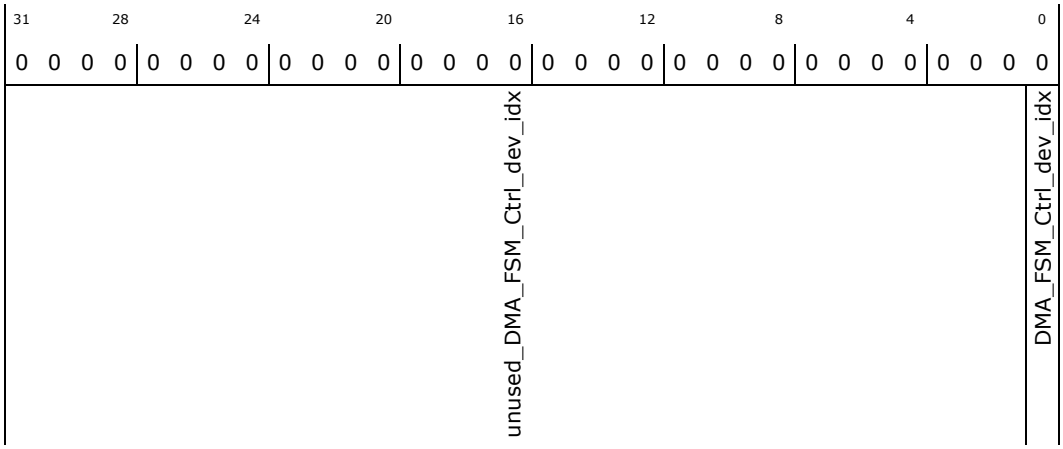
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87110h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_dev_idx):** Unused
0	0x0 RO	**DMA_FSM_Ctrl_dev_idx:** DMA FSM Control request device idx

5.3.137 DMA_FSM_Pack_cnt_Yb (is_2400_inp_sys_dma_DMA_FSM_Pack_cnt_Yb)—Offset 87114h

DMA FSM Pack Counter Height (Yb)

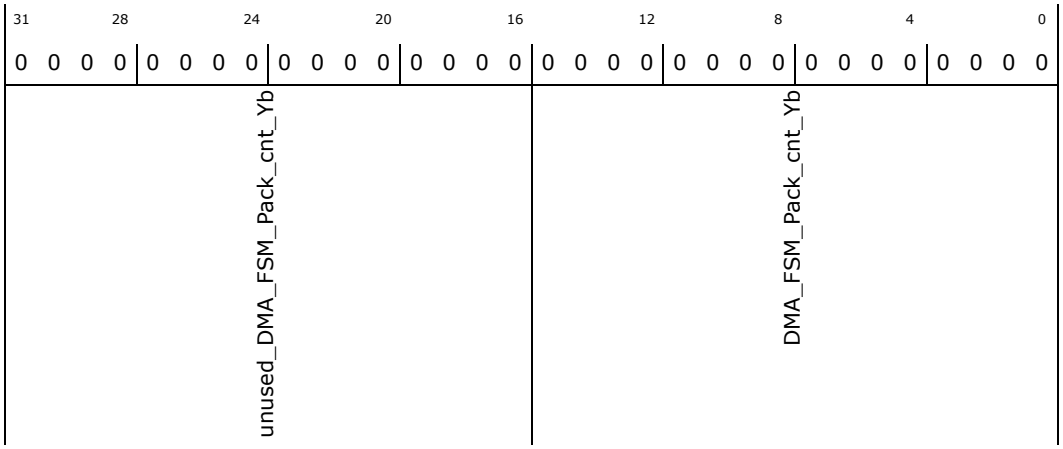
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87114h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Pack_cnt_Yb):** Unused
15:0	0x0 RO	**DMA_FSM_Pack_cnt_Yb:** DMA FSM pack counter height (Yb)

5.3.138 DMA_FSM_Request_cnt_Yb (is_2400_inp_sys_dma_DMA_FSM_Request_cnt_Yb)—Offset 87118h

DMA FSM request counter height (Yb)

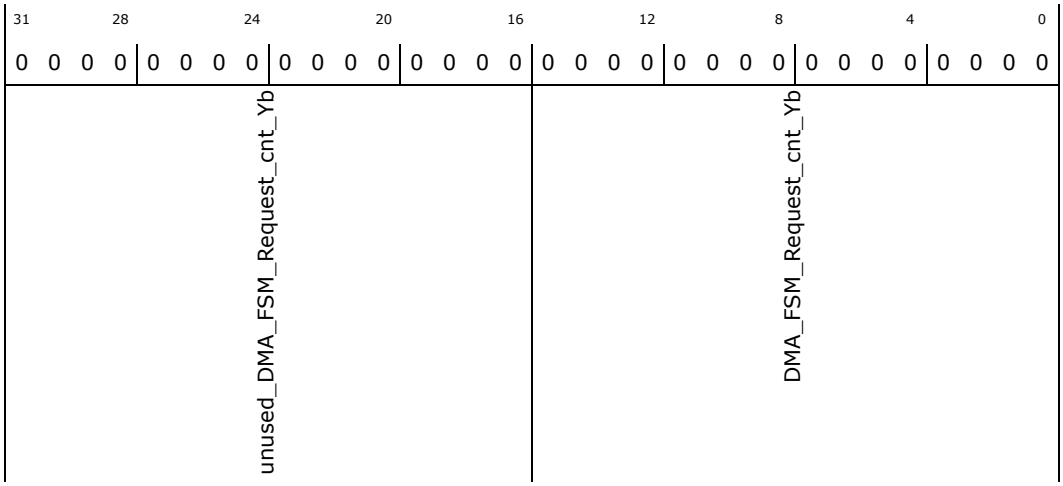
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87118h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Request_cnt_Yb):** Unused
15:0	0x0 RO	**DMA_FSM_Request_cnt_Yb:** DMA FSM request counter height (Yb)

5.3.139 DMA_FSM_Write_cnt_Y (is_2400_inp_sys_dma_DMA_FSM_Write_cnt_Y)—Offset 8711Ch

DMA FSM Write counter height (Yb)

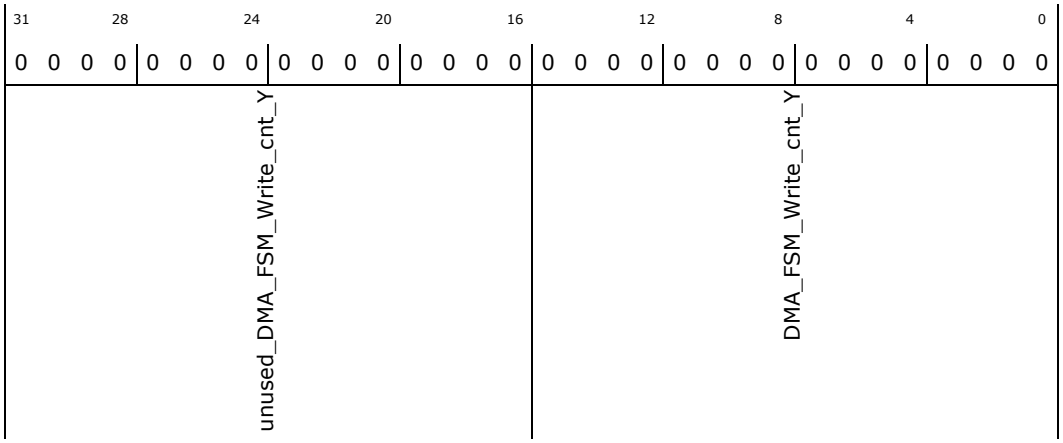
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8711Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Write_cnt_Y):** Unused
15:0	0x0 RO	**DMA_FSM_Write_cnt_Y:** DMA FSM Write counter height (Yb)

5.3.140 DMA_FSM_Ctrl_req_addr (is_2400_inp_sys_dma_DMA_FSM_Ctrl_req_addr)—Offset 87210h

DMA FSM Control request address

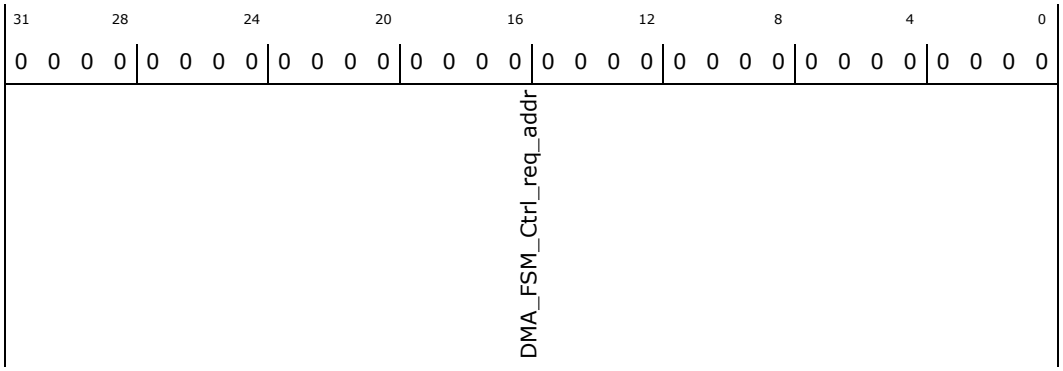
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87210h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_FSM_Ctrl_req_addr:** DMA FSM Control request address

5.3.141 DMA_FSM_Pack_req_cnt_Xb (is_2400_inp_sys_dma_DMA_FSM_Pack_req_cnt_Xb)—Offset 87214h

DMA FSM pack request counter width (Xb)

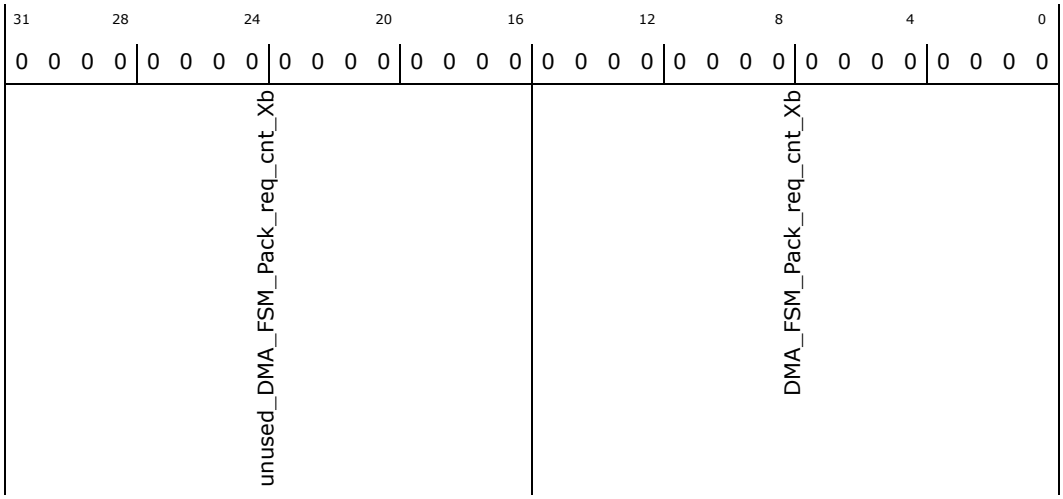
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87214h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Pack_req_cnt_Xb):** Unused
15:0	0x0 RO	**DMA_FSM_Pack_req_cnt_Xb:** DMA FSM pack request counter width (Xb)

5.3.142 DMA_FSM_Request_cnt_Xb (is_2400_inp_sys_dma_DMA_FSM_Request_cnt_Xb)—Offset 87218h

DMA FSM Request counter width (Xb)

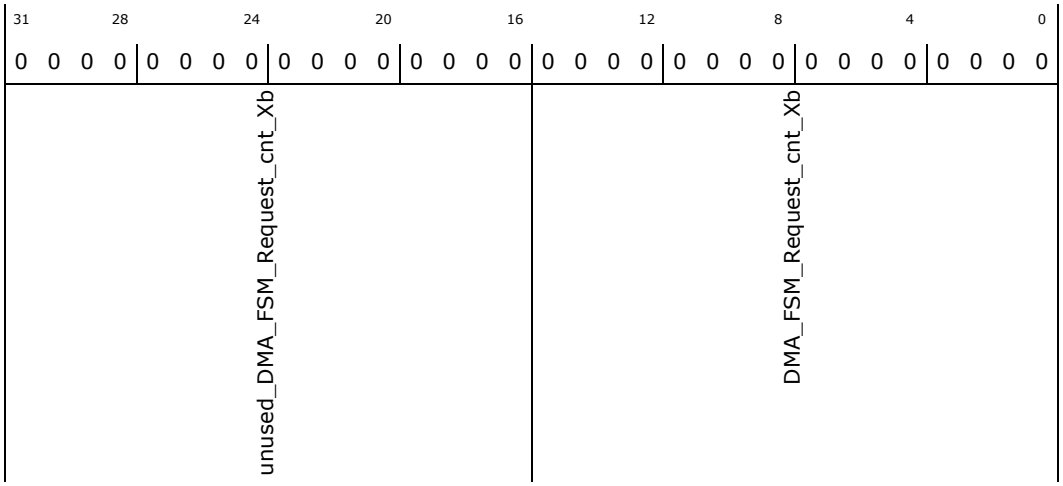
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87218h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Request_cnt_Xb):** Unused
15:0	0x0 RO	**DMA_FSM_Request_cnt_Xb:** DMA FSM Request counter width (Xb)

5.3.143 DMA_FSM_Write_cnt_Xb (is_2400_inp_sys_dma_DMA_FSM_Write_cnt_Xb)—Offset 8721Ch

DMA FSM Write counter width (Xb)

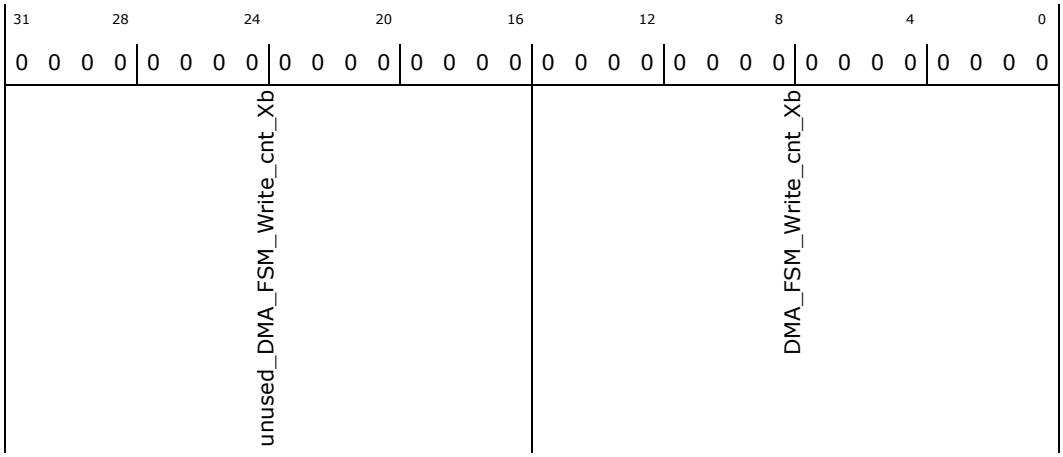
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8721Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Write_cnt_Xb):** Unused
15:0	0x0 RO	**DMA_FSM_Write_cnt_Xb:** DMA FSM Write counter width (Xb)

5.3.144 DMA_FSM_Ctrl_req_stride (is_2400_inp_sys_dma_DMA_FSM_Ctrl_req_stride)—Offset 87310h

DMA FSM Control request stride

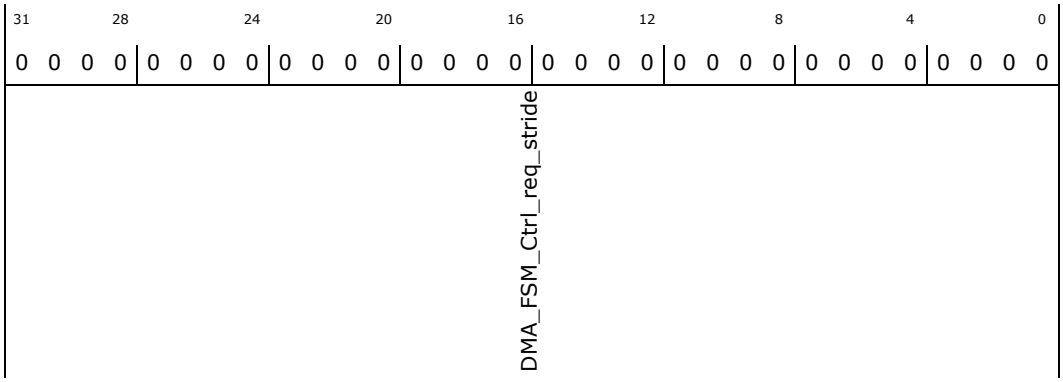
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87310h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_FSM_Ctrl_req_stride:** DMA FSM Control request stride

5.3.145 DMA_FSM_Pack_wr_cnt_Xb (is_2400_inp_sys_dma_DMA_FSM_Pack_wr_cnt_Xb)—Offset 87314h

DMA FSM pack write counter width (Xb)

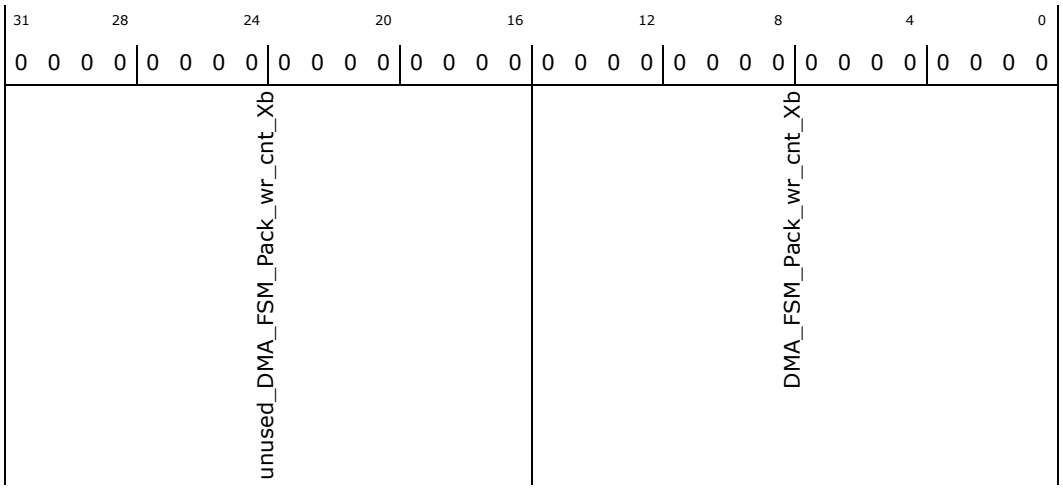
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87314h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Pack_wr_cnt_Xb):** Unused
15:0	0x0 RO	**DMA_FSM_Pack_wr_cnt_Xb:** DMA FSM pack write counter width (Xb)

5.3.146 DMA_FSM_Req_remining_Xb (is_2400_inp_sys_dma_DMA_FSM_Req_remining_Xb)—Offset 87318h

DMA FSM Request counter remaining word width

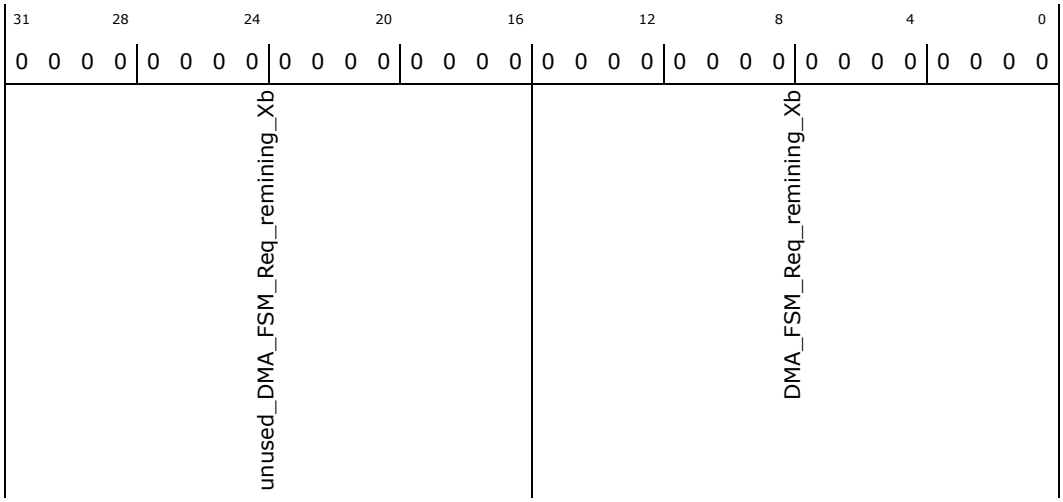
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87318h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Req_remining_Xb):** Unused
15:0	0x0 RO	**DMA_FSM_Req_remining_Xb:** DMA FSM Request counter remaining word width

5.3.147 DMA_FSM_Wr_remining_Xb (is_2400_inp_sys_dma_DMA_FSM_Wr_remining_Xb)—Offset 8731Ch

DMA FSM Write counter remaining word width

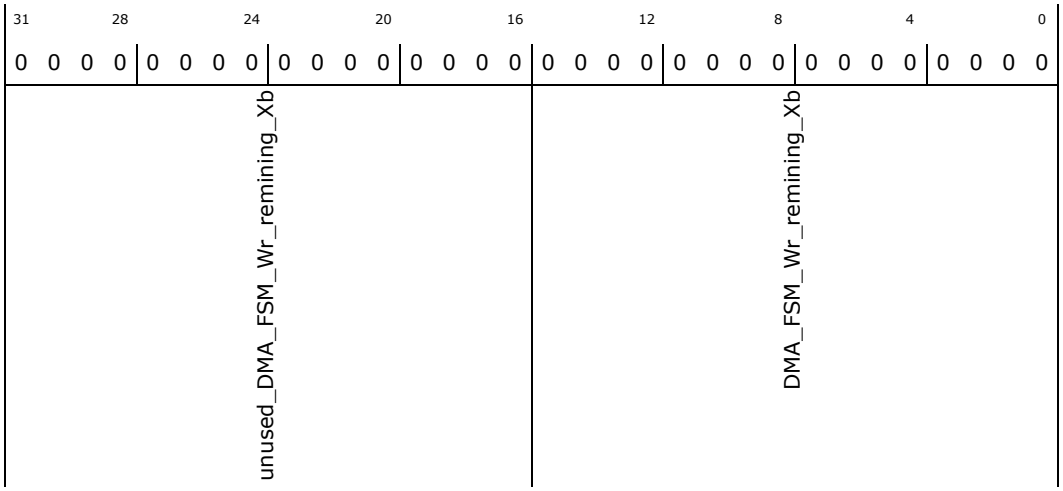
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8731Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Wr_remining_Xb):** Unused
15:0	0x0 RO	**DMA_FSM_Wr_remining_Xb:** DMA FSM Write counter remaining word width

5.3.148 DMA_FSM_Ctrl_req_Xb (is_2400_inp_sys_dma_DMA_FSM_Ctrl_req_Xb)—Offset 87410h

DMA FSM Control request width (Xb)

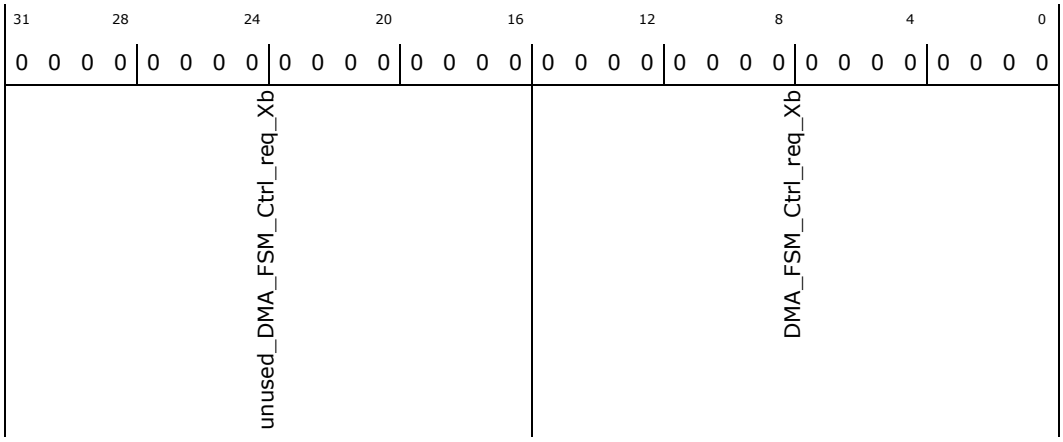
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87410h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_req_Xb):** Unused
15:0	0x0 RO	**DMA_FSM_Ctrl_req_Xb:** DMA FSM Control request width (Xb)

5.3.149 DMA_FSM_Req_burst_cnt (is_2400_inp_sys_dma_DMA_FSM_Req_burst_cnt)—Offset 87418h

DMA FSM Request word burst counter

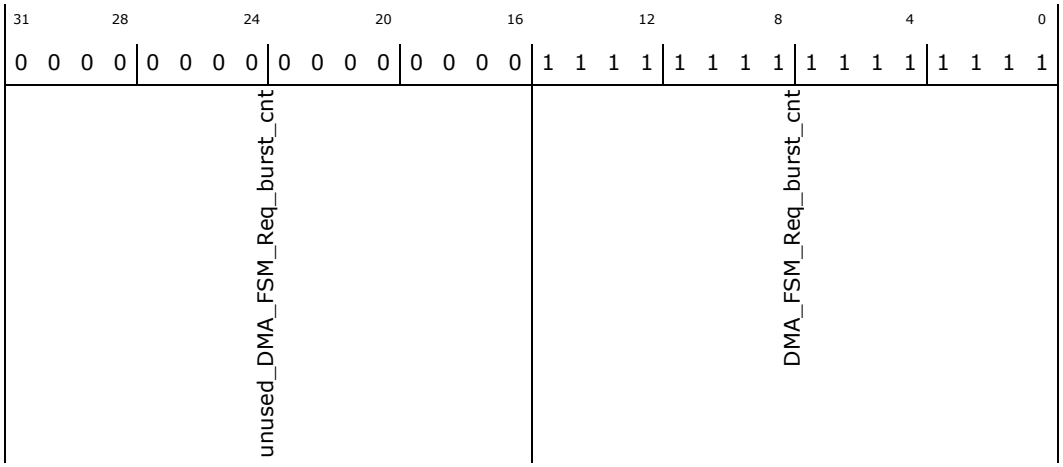
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87418h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000FFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Req_burst_cnt):** Unused
15:0	0xffff RO	**DMA_FSM_Req_burst_cnt:** DMA FSM Request word burst counter

5.3.150 DMA_FSM_Wr_burst_cnt (is_2400_inp_sys_dma_DMA_FSM_Wr_burst_cnt)—Offset 8741Ch

DMA FSM Write word burst counter

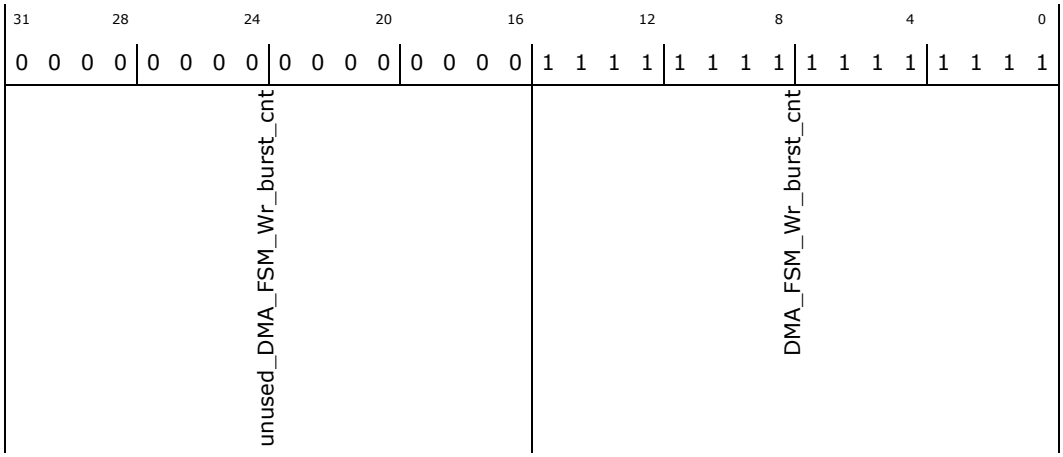
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8741Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000FFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Wr_burst_cnt):** Unused
15:0	0xffff RO	**DMA_FSM_Wr_burst_cnt:** DMA FSM Write word burst counter

5.3.151 DMA_FSM_Ctrl_req_Yb (is_2400_inp_sys_dma_DMA_FSM_Ctrl_req_Yb)—Offset 87510h

DMA FSM Control Request Height (Yb)

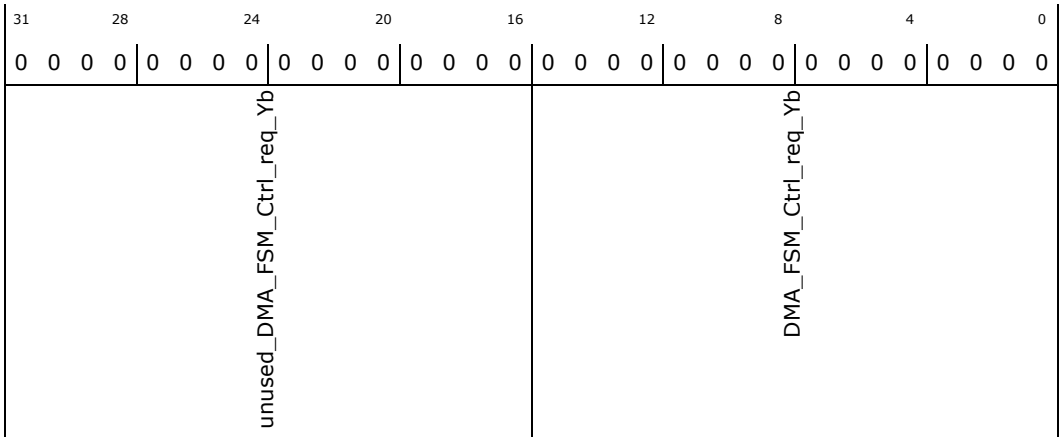
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87510h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_req_Yb):** Unused
15:0	0x0 RO	**DMA_FSM_Ctrl_req_Yb:** DMA FSM Control request height (Yb)

5.3.152 DMA_FSM_Ctrl_Pack_req_dev_idx (is_2400_inp_sys_dma_DMA_FSM_Ctrl_Pack_req_dev_idx)—Offset 87610h

DMA FSM Control pack request device idx

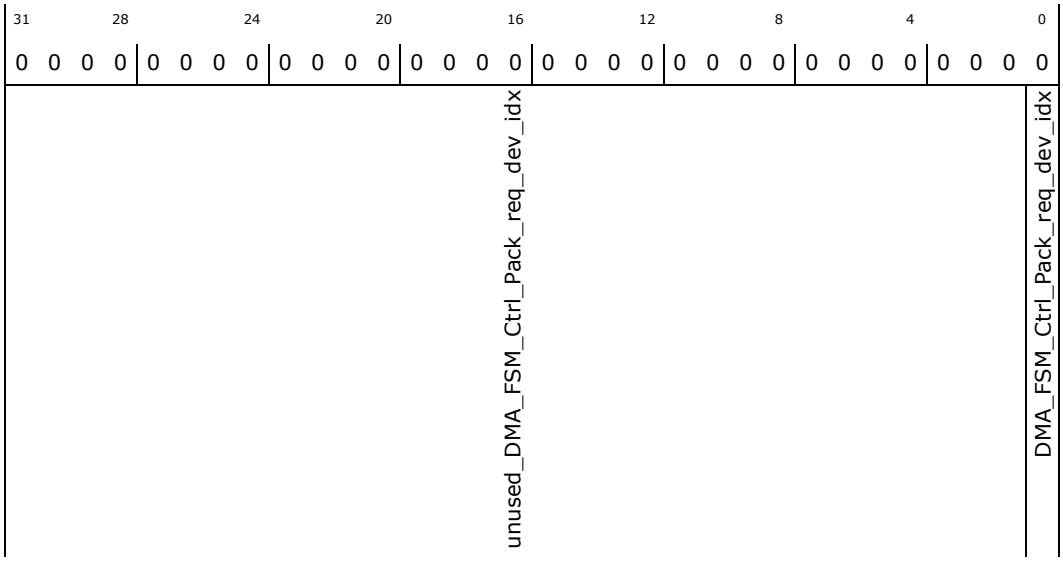
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87610h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_Pack_req_dev_idx):** Unused
0	0x0 RO	**DMA_FSM_Ctrl_Pack_req_dev_idx:** DMA FSM Control pack request device idx

5.3.153 DMA_FSM_Ctrl_Pack_wr_dev_idx (is_2400_inp_sys_dma_DMA_FSM_Ctrl_Pack_wr_dev_idx)—Offset 87710h

DMA FSM Control pack write device idx

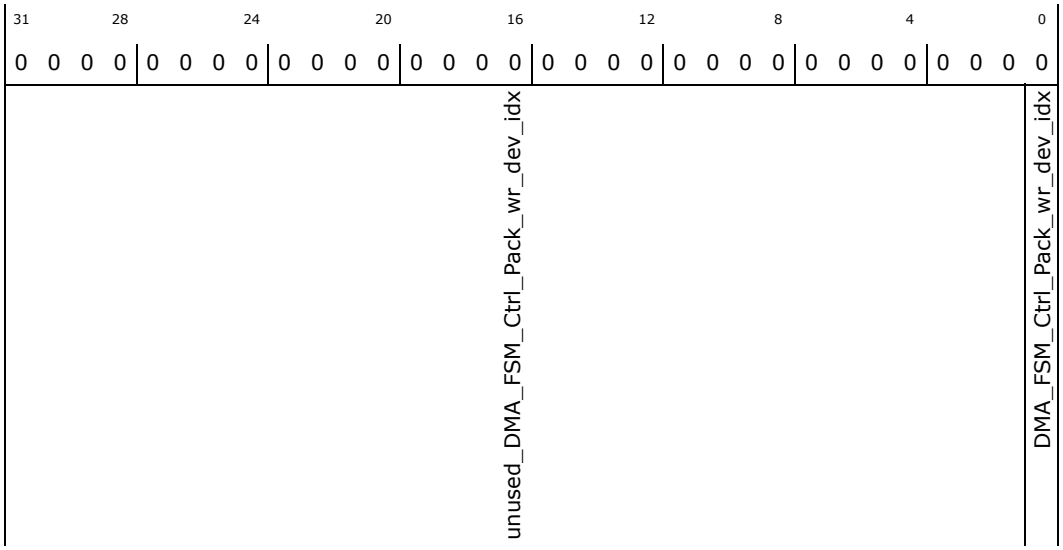
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87710h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_Pack_wr_dev_idx):** Unused
0	0x0 RO	**DMA_FSM_Ctrl_Pack_wr_dev_idx:** DMA FSM Control pack write device idx

5.3.154 DMA_FSM_Ctrl_Wr_addr (is_2400_inp_sys_dma_DMA_FSM_Ctrl_Wr_addr)—Offset 87810h

DMA FSM Control write address

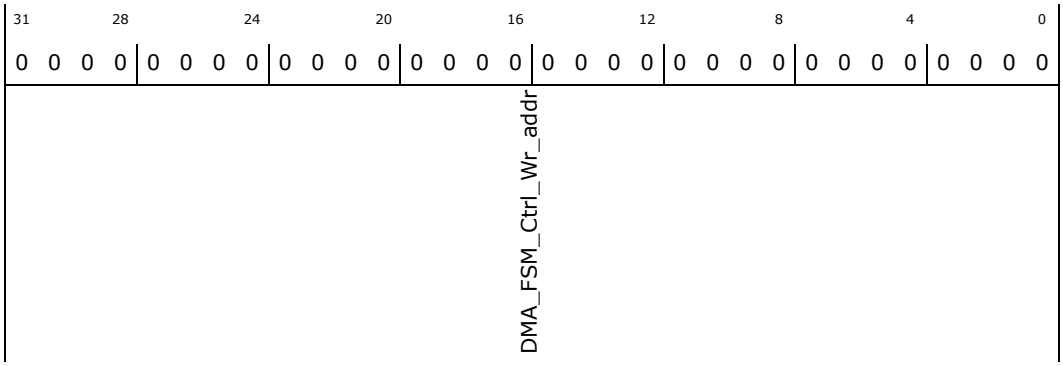
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87810h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_FSM_Ctrl_Wr_addr:** DMA FSM Control write address

5.3.155 DMA_FSM_Ctrl_Wr_stride (is_2400_inp_sys_dma_DMA_FSM_Ctrl_Wr_stride)—Offset 87910h

DMA FSM Control write stride

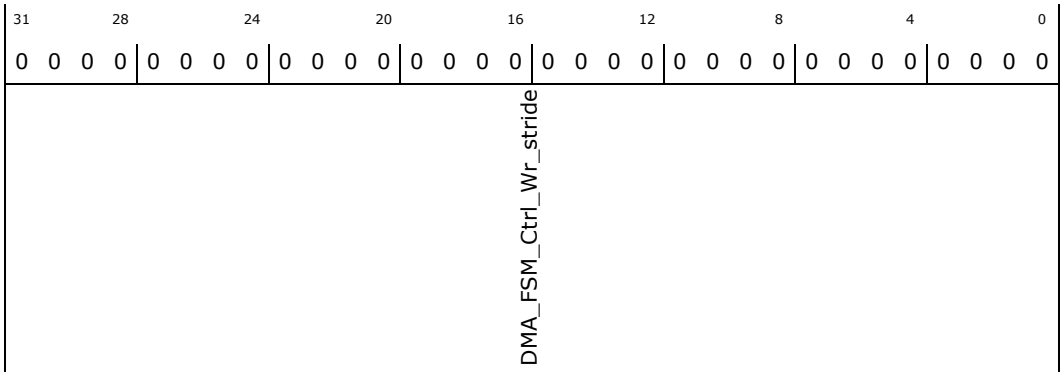
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87910h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**DMA_FSM_Ctrl_Wr_stride:** DMA FSM Control write stride

5.3.156 DMA_FSM_Ctrl_pack_req_Xb (is_2400_inp_sys_dma_DMA_FSM_Ctrl_pack_req_Xb)—Offset 87A10h

DMA FSM Control FSM Pack request width (Xb)

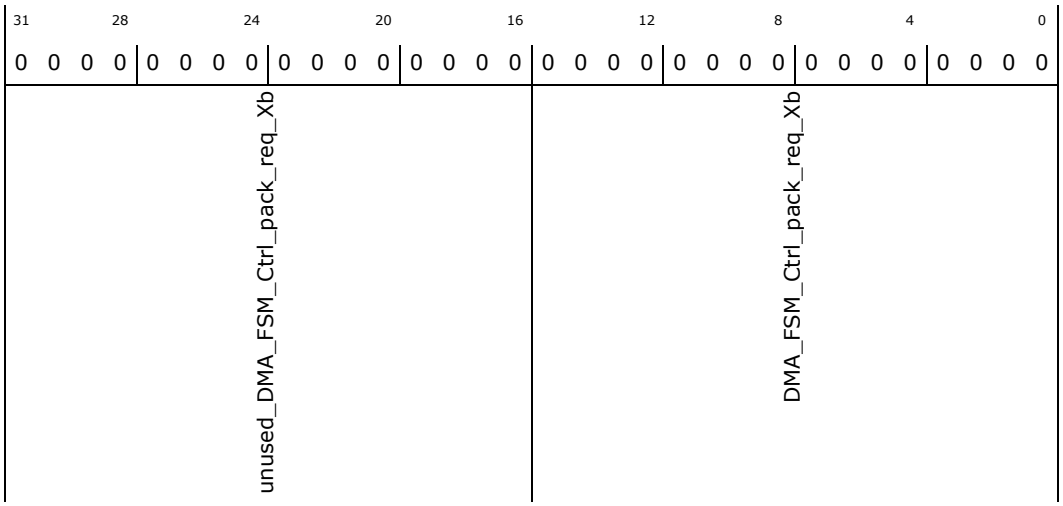
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87A10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_pack_req_Xb):** Unused
15:0	0x0 RO	**DMA_FSM_Ctrl_pack_req_Xb:** DMA FSM Control FSM Pack request width (Xb)

5.3.157 DMA_FSM_Ctrl_pack_Yb (is_2400_inp_sys_dma_DMA_FSM_Ctrl_pack_Yb)—Offset 87B10h

DMA FSM Control FSM Pack height (Yb)

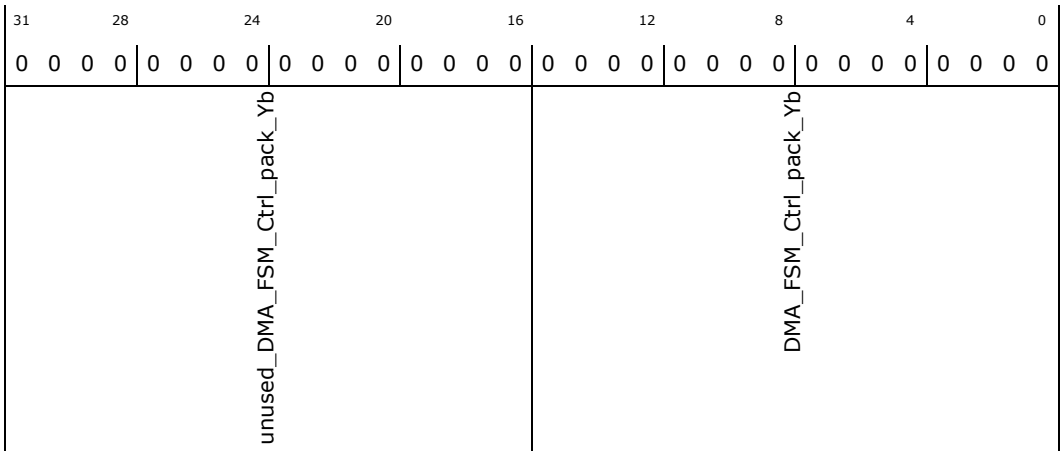
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87B10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_pack_Yb):** Unused
15:0	0x0 RO	**DMA_FSM_Ctrl_pack_Yb:** DMA FSM Control FSM Pack height (Yb)

5.3.158 DMA_FSM_Ctrl_pack_wr_Xb (is_2400_inp_sys_dma_DMA_FSM_Ctrl_pack_wr_Xb)—Offset 87C10h

DMA FSM Control FSM Pack write width (Xb)

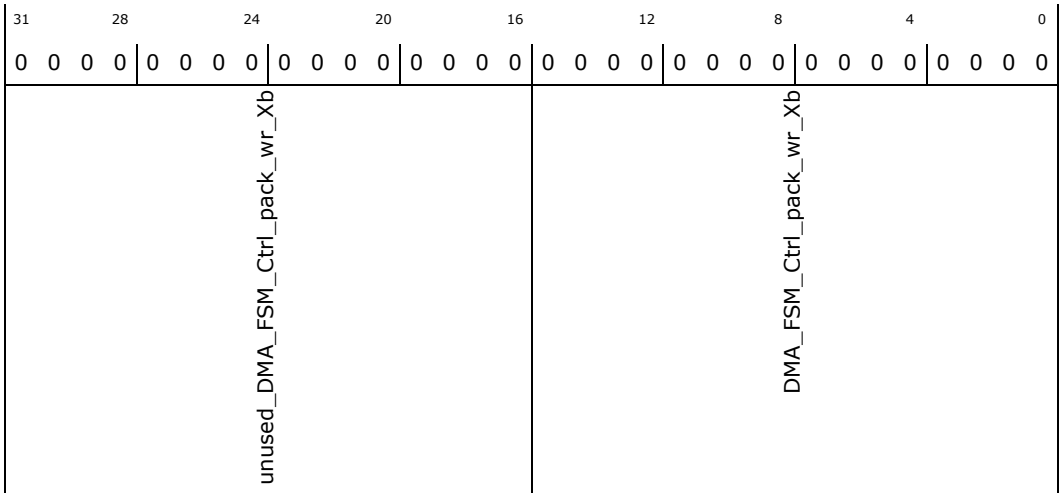
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87C10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_pack_wr_Xb):** Unused
15:0	0x0 RO	**DMA_FSM_Ctrl_pack_wr_Xb:** DMA FSM Control FSM Pack write width (Xb)

5.3.159 DMA_FSM_Ctrl_pack_req_elem (is_2400_inp_sys_dma_DMA_FSM_Ctrl_pack_req_elem) —Offset 87D10h

DMA FSM Control pack request element per word

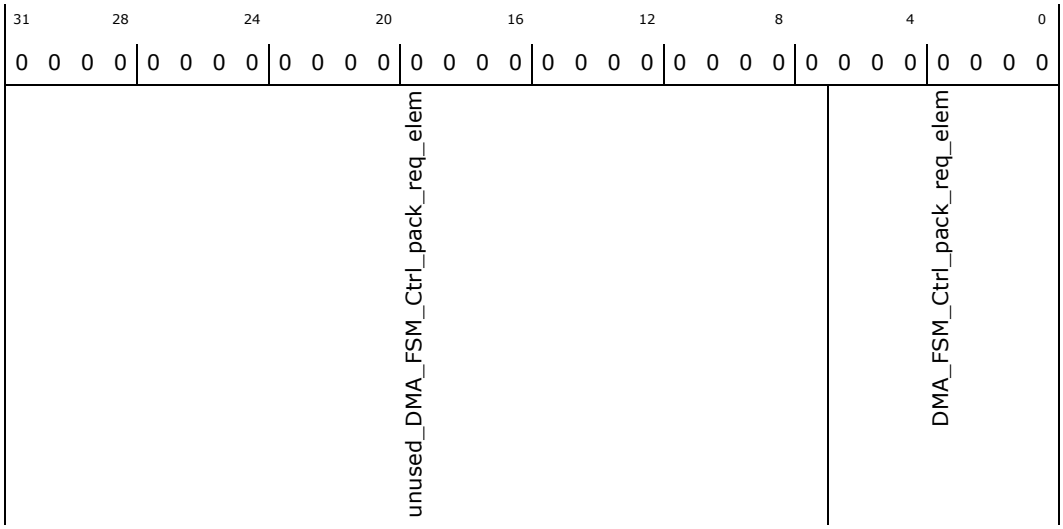
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87D10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:7	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_pack_req_elem):** Unused
6:0	0x0 RO	**DMA_FSM_Ctrl_pack_req_elem:** DMA FSM Control pack request element per word

5.3.160 DMA_FSM_Ctrl_pack_wr_elem (is_2400_inp_sys_dma_DMA_FSM_Ctrl_pack_wr_elem)—Offset 87E10h

DMA FSM Control pack write element per word

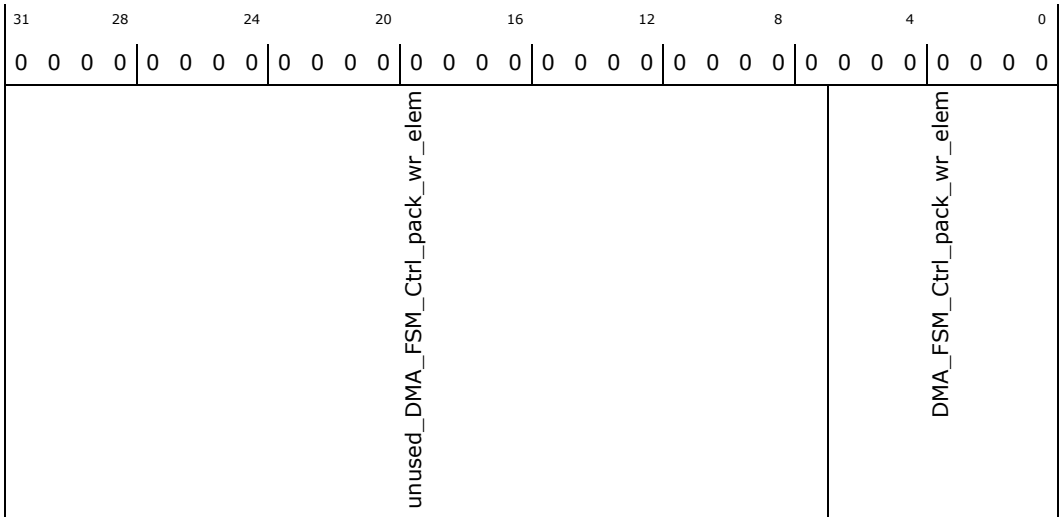
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87E10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:7	0x0 RW	**Reserved (unused_DMA_FSM_Ctrl_pack_wr_elem):** Unused
6:0	0x0 RO	**DMA_FSM_Ctrl_pack_wr_elem:** DMA FSM Control pack write element per word

5.3.161 DMA_FSM_Ctrl_pack_sz_ext_ctrl_id (is_2400_inp_sys_dma_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id)—Offset 87F10h

DMA FSM Control pack element sign zero extension and controller ID

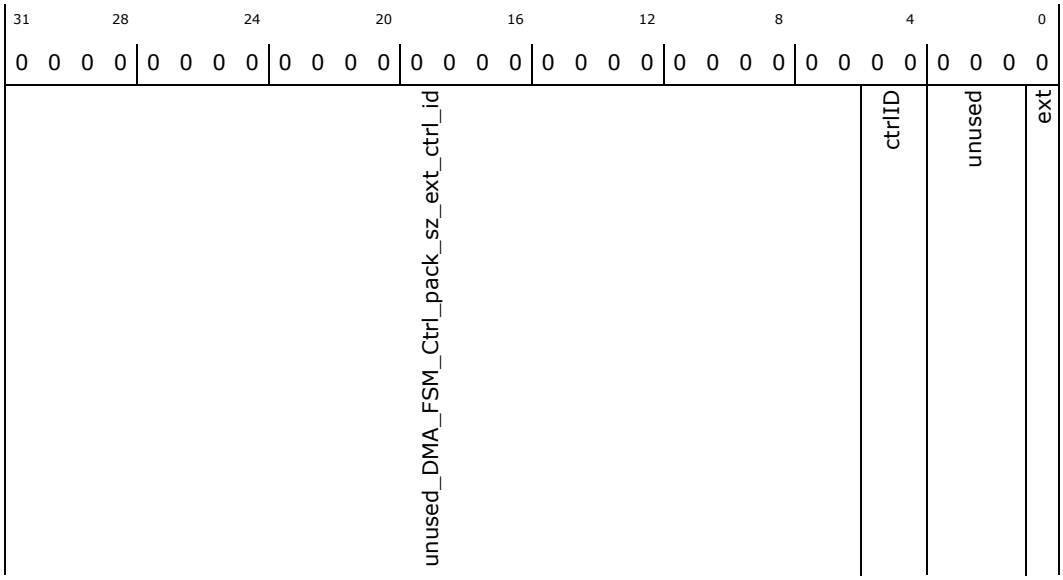
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 87F10h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RO	**Reserved (unused_DMA_FSM_Ctrl_pack_sz_ext_ctrl_id):** Unused
5:4	0x0 RO	**ctrlID:** Controller ID
3:1	0x0 RO	**unused:** unused
0	0x0 RO	**ext:** element sign(1)/zero(0) extension

5.3.162 Dev_Interf_0_req_side (is_2400_inp_sys_dma_Dev_Interf_0_req_side)—Offset 88000h

DMA Device interface 0 internal side status

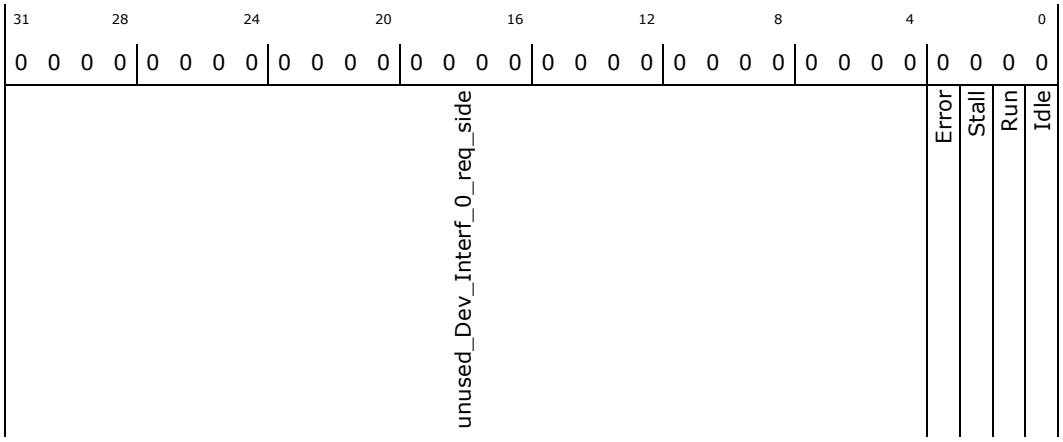
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 88000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_Dev_Interf_0_req_side):** Unused
3	0x0 RO	**Error:** Ack flag
2	0x0 RO	**Stall:** Run flag
1	0x0 RO	**Run:** We_n flag
0	0x0 RO	**Idle:** CS flag

5.3.163 Dev_Interf_1_req_side (is_2400_inp_sys_dma_Dev_Interf_1_req_side)—Offset 88004h

DMA Device interface 1 internal side status

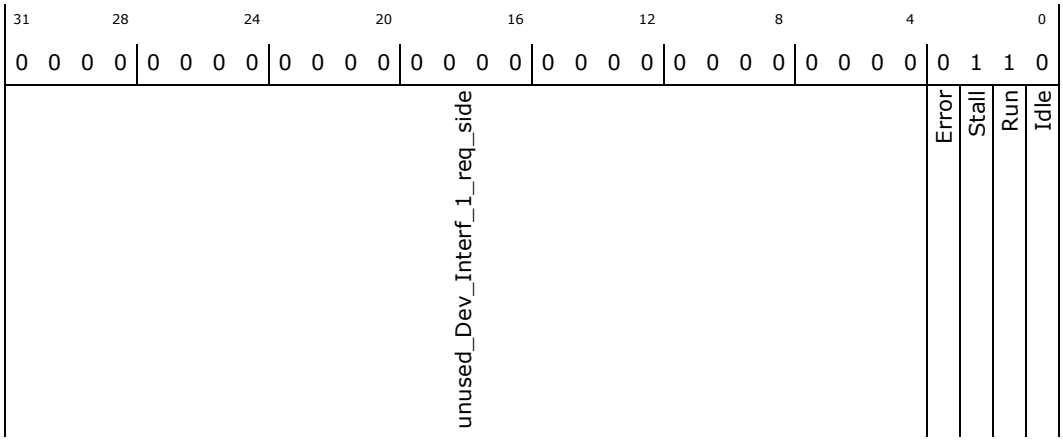
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 88004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000006h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_Dev_Interf_1_req_side):** Unused
3	0x0 RO	**Error:** Ack flag
2	0x1 RO	**Stall:** Run flag
1	0x1 RO	**Run:** We_n flag
0	0x0 RO	**Idle:** CS flag

5.3.164 Dev_Interf_0_snd_side (is_2400_inp_sys_dma_Dev_Interf_0_snd_side)—Offset 88100h

DMA Device interface 0 output side status

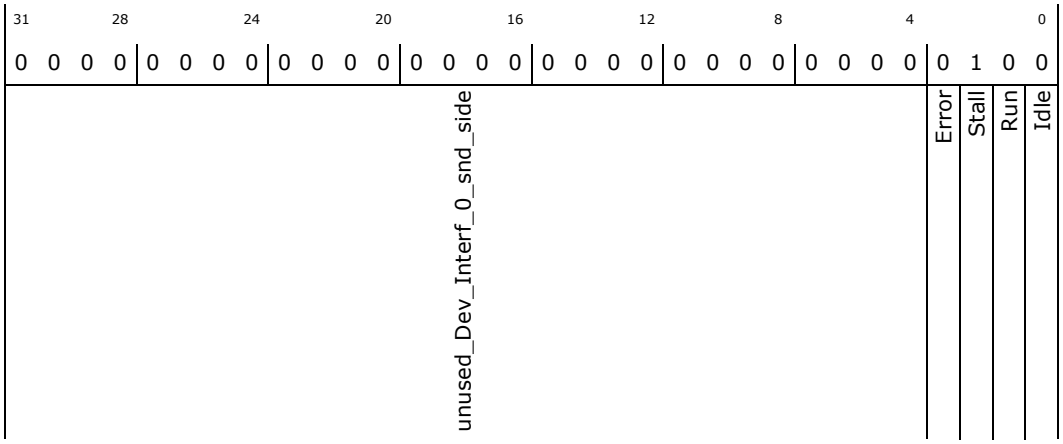
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 88100h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_Dev_Interf_0_snd_side):** Unused
3	0x0 RO	**Error:** Ack flag
2	0x1 RO	**Stall:** Run flag
1	0x0 RO	**Run:** We_n flag
0	0x0 RO	**Idle:** CS flag

5.3.165 Dev_Interf_1_snd_side (is_2400_inp_sys_dma_Dev_Interf_1_snd_side)—Offset 88104h

DMA Device interface 1 output side status

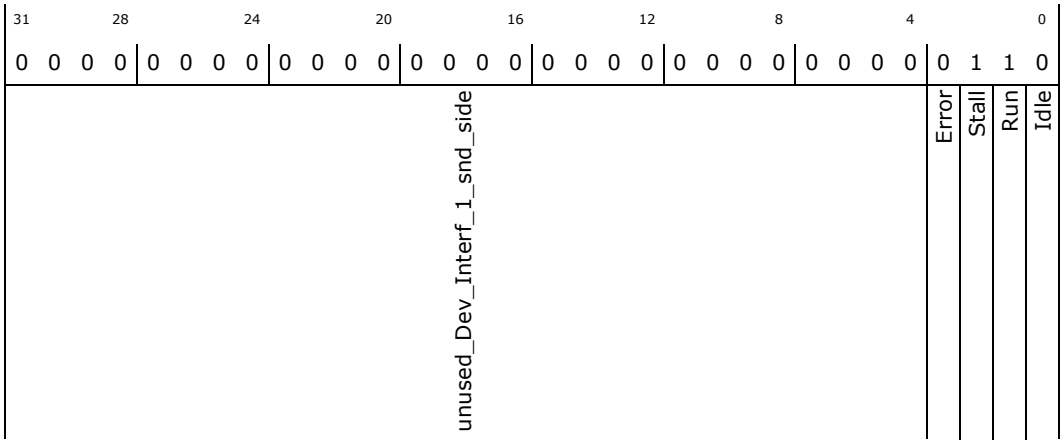
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 88104h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000006h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_Dev_Interf_1_snd_side):** Unused
3	0x0 RO	**Error:** Ack flag
2	0x1 RO	**Stall:** Run flag
1	0x1 RO	**Run:** We_n flag
0	0x0 RO	**Idle:** CS flag

5.3.166 Dev_Interf_0_Fifo_status (is_2400_inp_sys_dma_Dev_Interf_0_Fifo_status)—Offset 88200h

Device Interface 0 FIFO Status

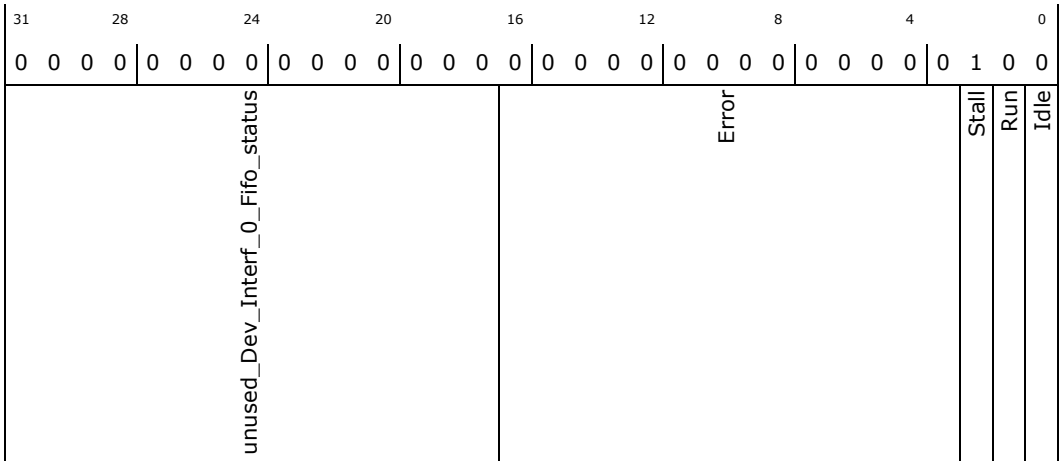
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 88200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h



Bit Range	Default and Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (unused_Dev_Interf_0_Fifo_status):** Unused
16:3	0x0 RO	**Error:** FIFO word counter
2	0x1 RO	**Stall:** FIFO is empty
1	0x0 RO	**Run:** FIFO is full
0	0x0 RO	**Idle:** FIFO will be full

5.3.167 Dev_Interf_1_Fifo_status (is_2400_inp_sys_dma_Dev_Interf_1_Fifo_status)—Offset 88204h

Device Interface 1 FIFO Status

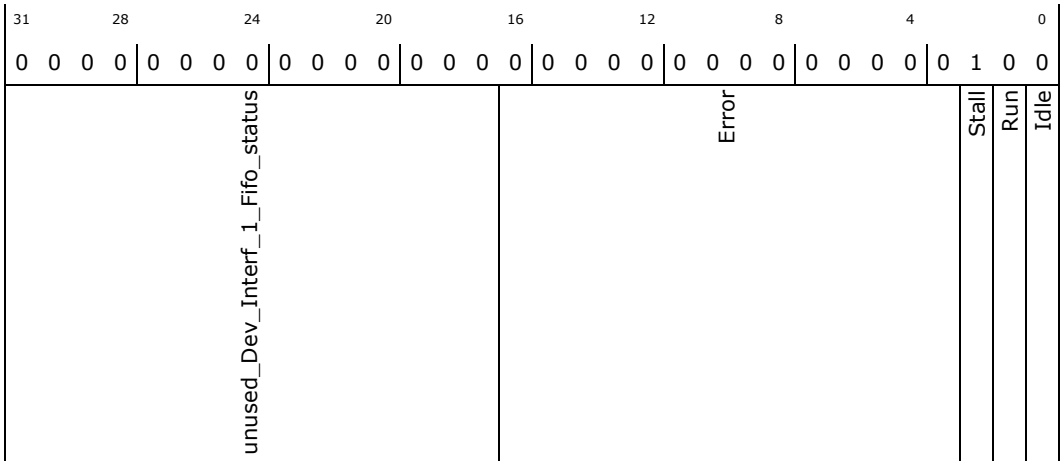
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 88204h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000004h



Bit Range	Default and Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (unused_Dev_Interf_1_Fifo_status):** Unused
16:3	0x0 RO	**Error:** FIFO word counter
2	0x1 RO	**Stall:** FIFO is empty
1	0x0 RO	**Run:** FIFO is full
0	0x0 RO	**Idle:** FIFO will be full

5.3.168 Dev_Interf_0_Req_complete_bust (is_2400_inp_sys_dma_Dev_Interf_0_Req_complete_bust)—Offset 88300h

DMA Device interface 0 Request only complete burst

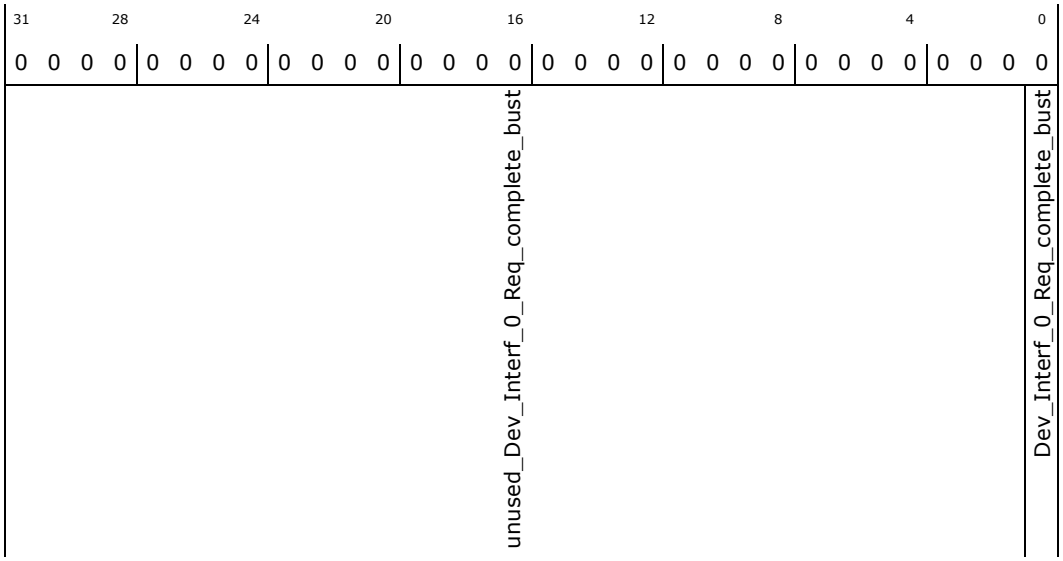
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 88300h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_Dev_Interf_0_Req_complete_bust):** Unused
0	0x0 RW	**Dev_Interf_0_Req_complete_bust:** DMA Device interface 0 Request only complete burst

5.3.169 Dev_Interf_1_Req_complete_bust (is_2400_inp_sys_dma_Dev_Interf_1_Req_complete_bust)—Offset 88304h

DMA Device interface 1 Request only complete burst

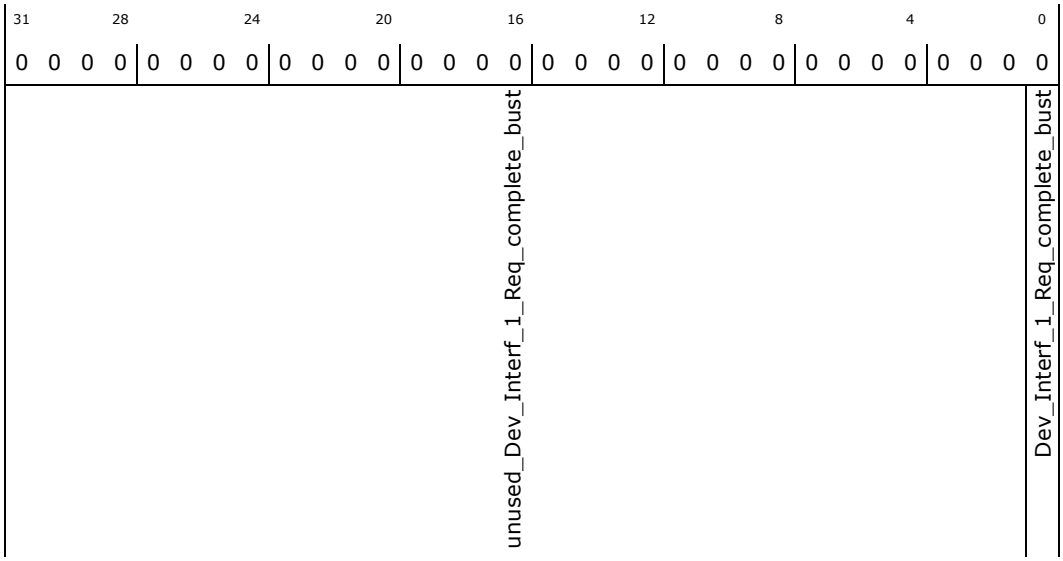
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 88304h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_Dev_Interf_1_Req_complete_bust):** Unused
0	0x0 RW	**Dev_Interf_1_Req_complete_bust:** DMA Device interface 1 Request only complete burst

5.3.170 Dev_Interf_1_Max_Burst_Size (is_2400_inp_sys_dma_Dev_Interf_1_Max_Burst_Size)—Offset 88400h

DMA Device interface 1 maximum burst size

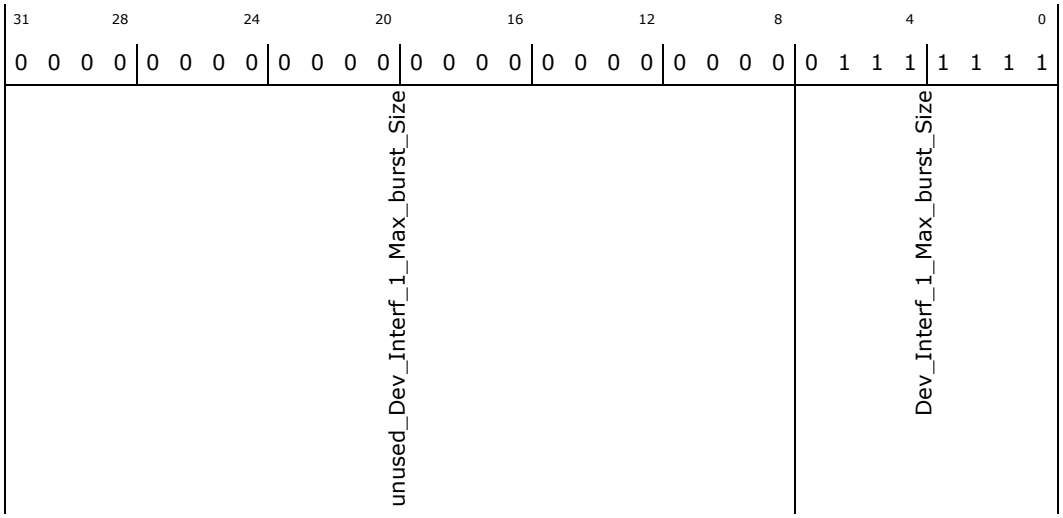
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 88400h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000007Fh



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved (unused_Dev_Interf_1_Max_burst_Size):** Unused
7:0	0x7f RW	**Dev_Interf_1_Max_Burst_Size:** DMA Device interface 1 maximum burst size

5.3.171 inpsys_captA_start_addr (is_2400_inp_sys_inp_ctrl_inpsys_captA_start_addr)—Offset 89000h

Input System Controller Capt A mem region start address

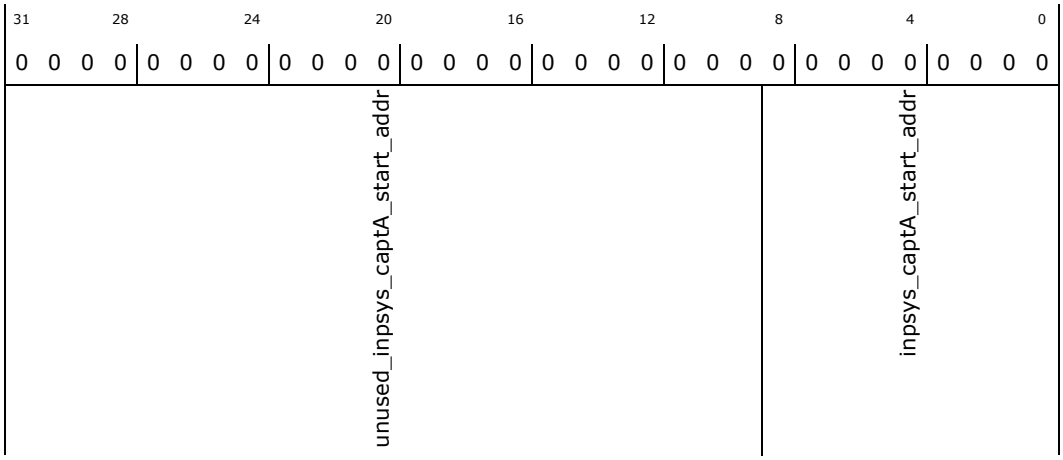
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 89000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved (unused_inpsys_captA_start_addr):** Unused
8:0	0x0 RW	**inpsys_captA_start_addr:** Input System Controller Capt A mem region start address

5.3.172 inpsys_captB_start_addr (is_2400_inp_sys_inp_ctrl_inpsys_captB_start_addr)—Offset 89004h

Input System Controller Capt B mem region start address

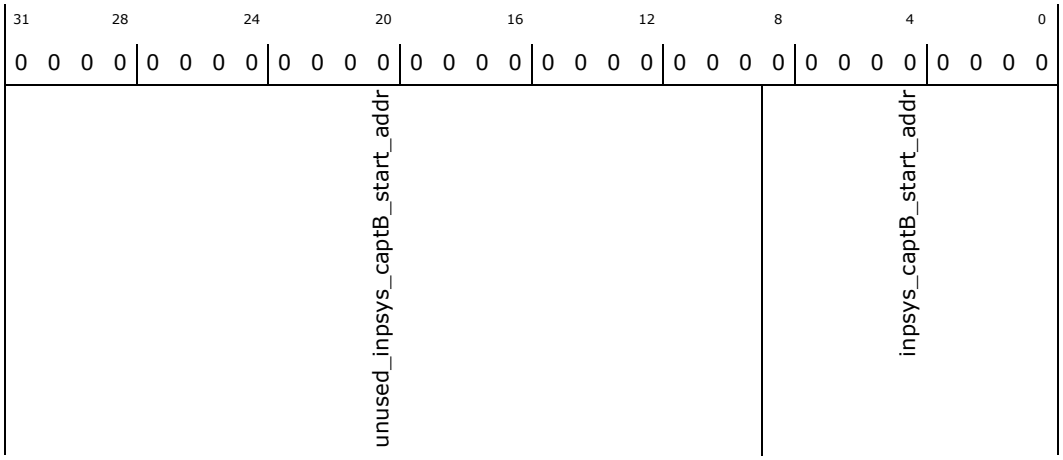
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 89004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved (unused_inpsys_captB_start_addr):** Unused
8:0	0x0 RW	**inpsys_captB_start_addr:** Input System Controller Capt B mem region start address

5.3.173 inpsys_captC_start_addr (is_2400_inp_sys_inp_ctrl_inpsys_captC_start_addr)—Offset 89008h

Input System Controller Capt C mem region start address

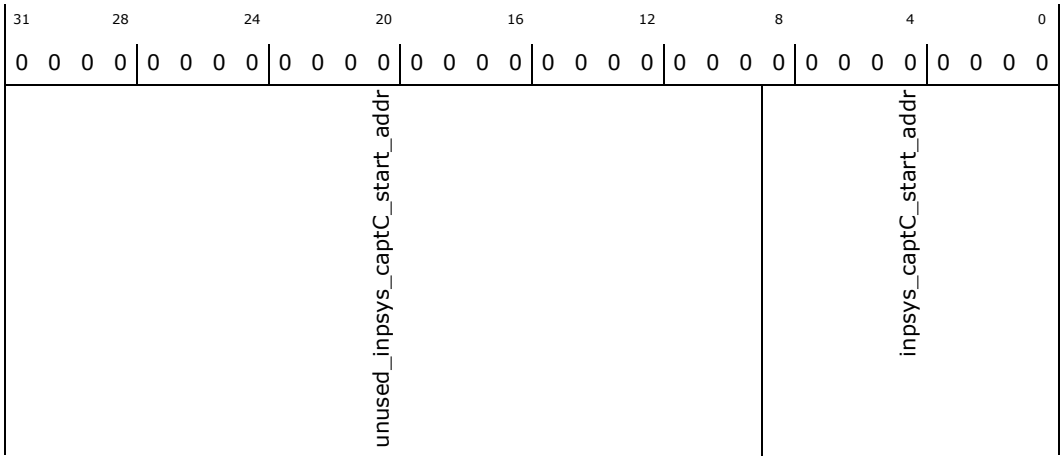
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 89008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved (unused_inpsys_captC_start_addr):** Unused
8:0	0x0 RW	**inpsys_captC_start_addr:** Input System Controller Capt C mem region start address

5.3.174 inpsys_captA_mem_region_size (is_2400_inp_sys_inp_ctrl_inpsys_captA_mem_region_size)—Offset 8900Ch

Input System Controller Capt A mem region size

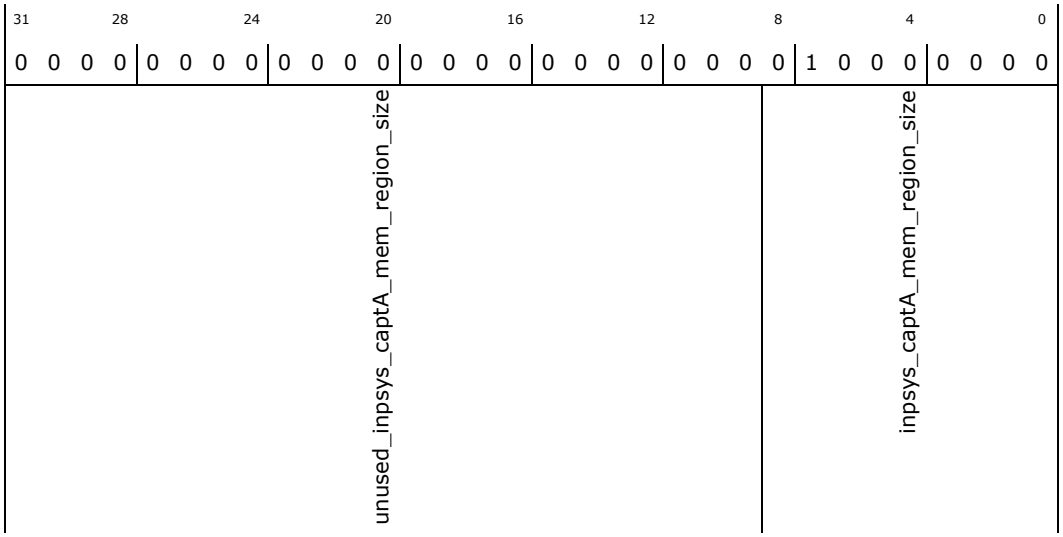
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8900Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h



Bit Range	Default and Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved (unused_inpsys_captA_mem_region_size):** Unused
8:0	0x80 RW	**inpsys_captA_mem_region_size:** Input System Controller Capt A mem region size

5.3.175 inpsys_captB_mem_region_size (is_2400_inp_sys_inp_ctrl_inpsys_captB_mem_region_size)—Offset 89010h

Input System Controller Capt B mem region size

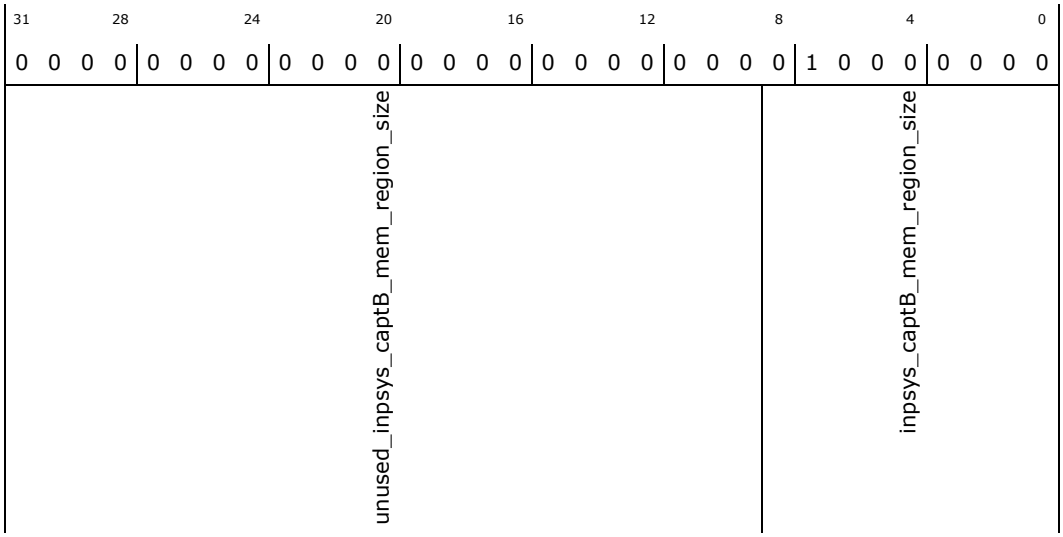
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 89010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h



Bit Range	Default and Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved (unused_inpsys_captB_mem_region_size):** Unused
8:0	0x80 RW	**inpsys_captB_mem_region_size:** Input System Controller Capt B mem region size

5.3.176 inpsys_captC_mem_region_size (is_2400_inp_sys_inp_ctrl_inpsys_captC_mem_region_size)—Offset 89014h

Input System Controller Capt C mem region size

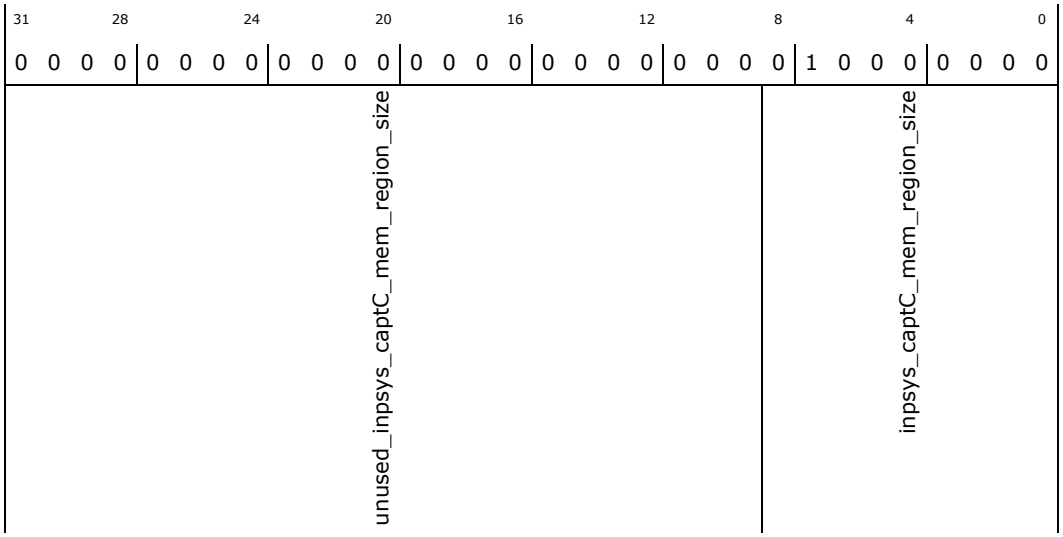
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 89014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h



Bit Range	Default and Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved (unused_inpsys_captC_mem_region_size):** Unused
8:0	0x80 RW	**inpsys_captC_mem_region_size:** Input System Controller Capt C mem region size

5.3.177 inpsys_captA_num_mem_regions (is_2400_inp_sys_inp_ctrl_inpsys_captA_num_mem_regions)—Offset 89018h

Input System Controller Capt A number of mem regions

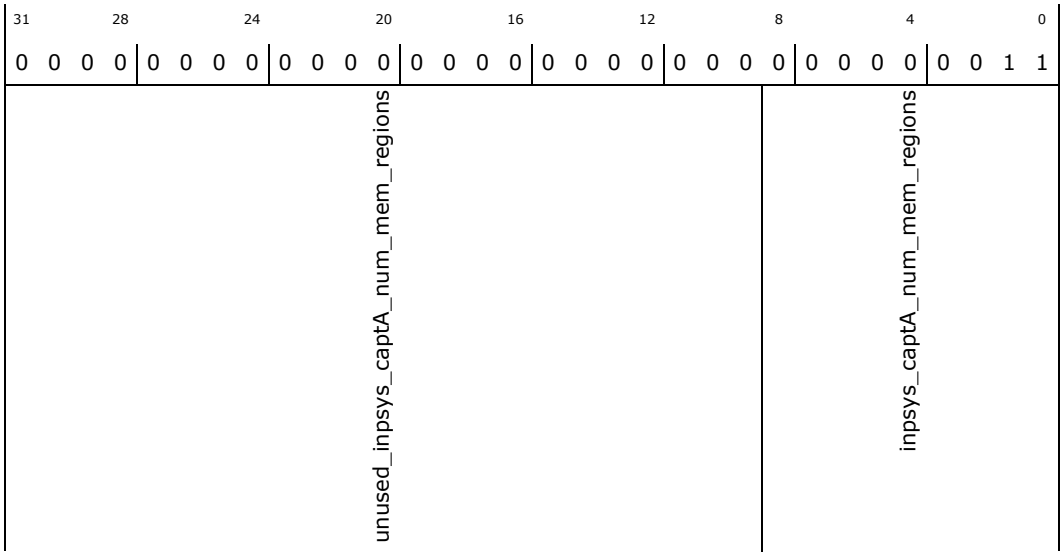
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 89018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h



Bit Range	Default and Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved (unused_inpsys_captA_num_mem_regions):** Unused
8:0	0x3 RW	**inpsys_captA_num_mem_regions:** Input System Controller Capt A number of mem regions

5.3.178 inpsys_captB_num_mem_regions (is_2400_inp_sys_inp_ctrl_inpsys_captB_num_mem_regions)—Offset 8901Ch

Input System Controller Capt B number of mem regions

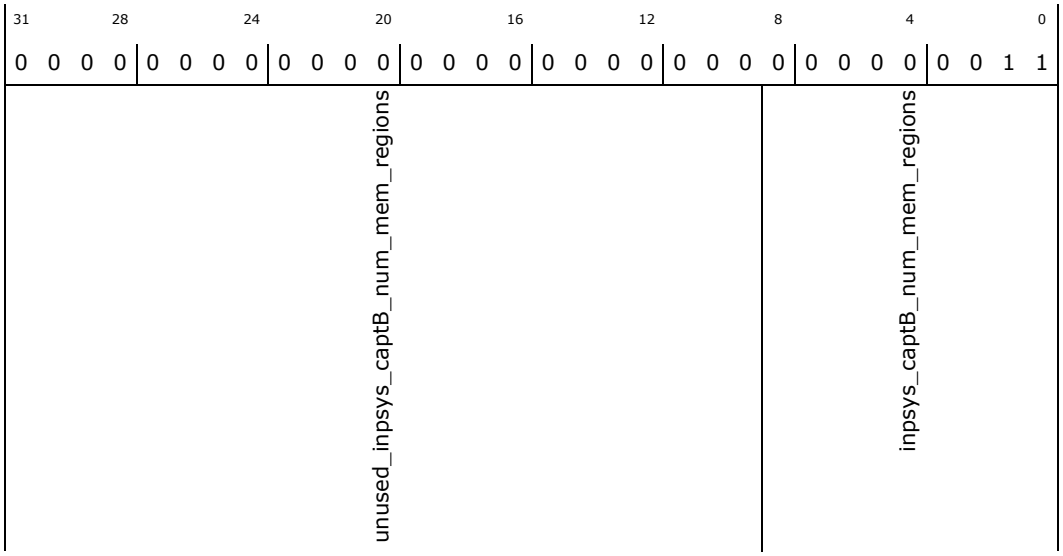
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8901Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h



Bit Range	Default and Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved (unused_inpsys_captB_num_mem_regions):** Unused
8:0	0x3 RW	**inpsys_captB_num_mem_regions:** Input System Controller Capt B number of mem regions

5.3.179 inpsys_captC_num_mem_regions (is_2400_inp_sys_inp_ctrl_inpsys_captC_num_mem_regions)—Offset 89020h

Input System Controller Capt C number of mem regions

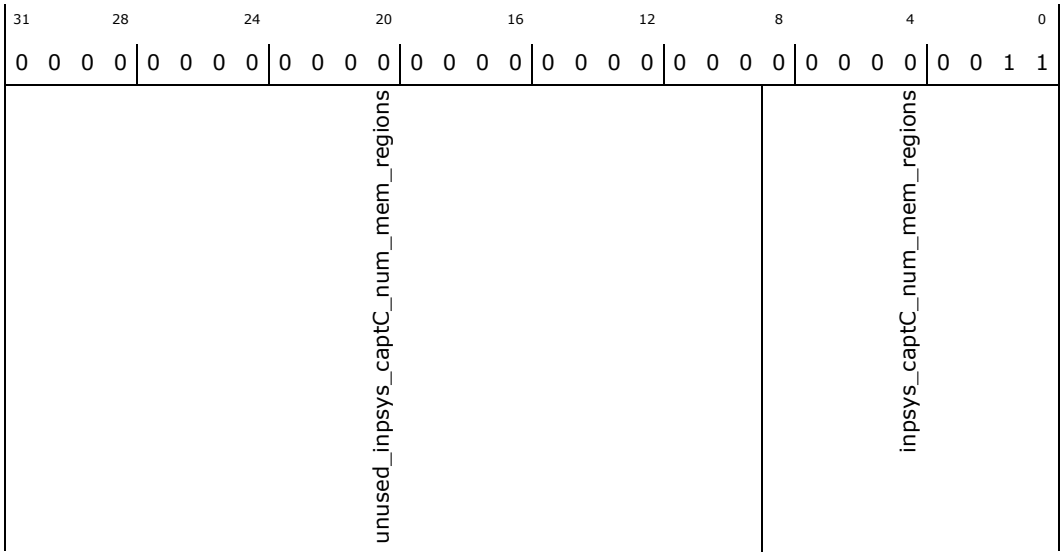
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 89020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h



Bit Range	Default and Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved (unused_inpsys_captC_num_mem_regions):** Unused
8:0	0x3 RW	**inpsys_captC_num_mem_regions:** Input System Controller Capt C number of mem regions

5.3.180 inpsys_acq_start_addr (is_2400_inp_sys_inp_ctrl_inpsys_acq_start_addr)—Offset 89024h

Input System Controller Acquisition mem region start address

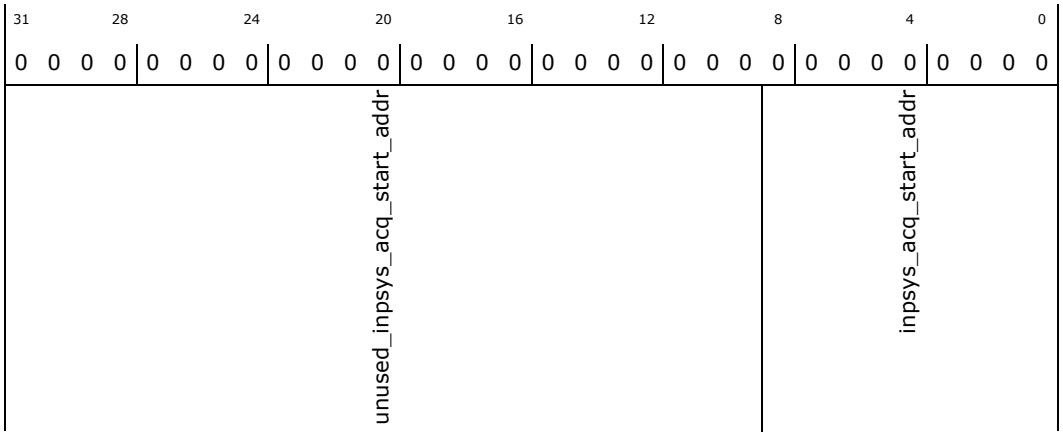
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 89024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved (unused_inpsys_acq_start_addr):** Unused
8:0	0x0 RW	**inpsys_acq_start_addr:** Input System Controller Acquisition mem region start address

5.3.181 inpsys_acq_mem_region_size (is_2400_inp_sys_inp_ctrl_inpsys_acq_mem_region_size)—Offset 89028h

Input System Controller Acquisition mem region size

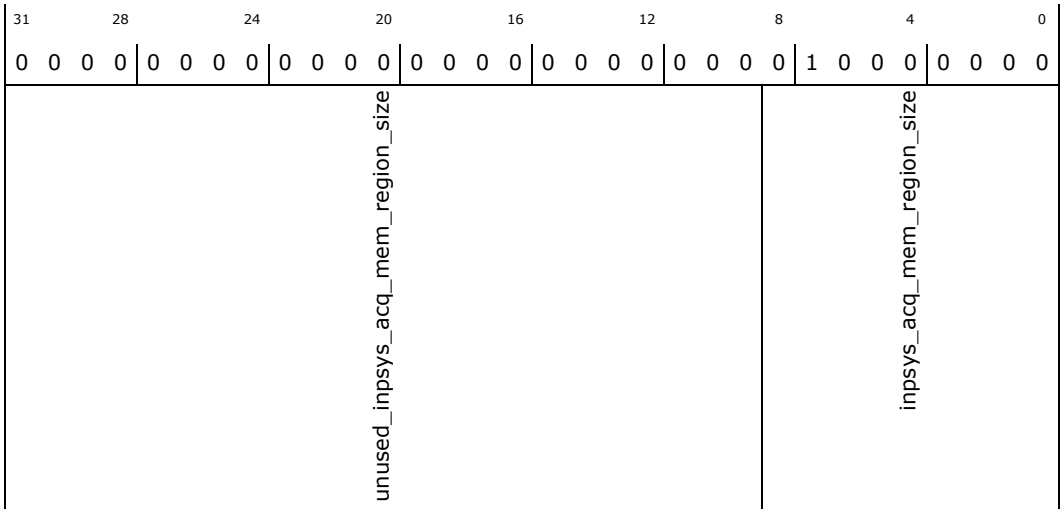
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 89028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000080h



Bit Range	Default and Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved (unused_inpsys_acq_mem_region_size):** Unused
8:0	0x80 RW	**inpsys_acq_mem_region_size:** Input System Controller Acquisition mem region size

5.3.182 inpsys_acq_num_mem_regions (is_2400_inp_sys_inp_ctrl_inpsys_acq_num_mem_regions)—Offset 8902Ch

Input System Controller Acquisition number of mem regions

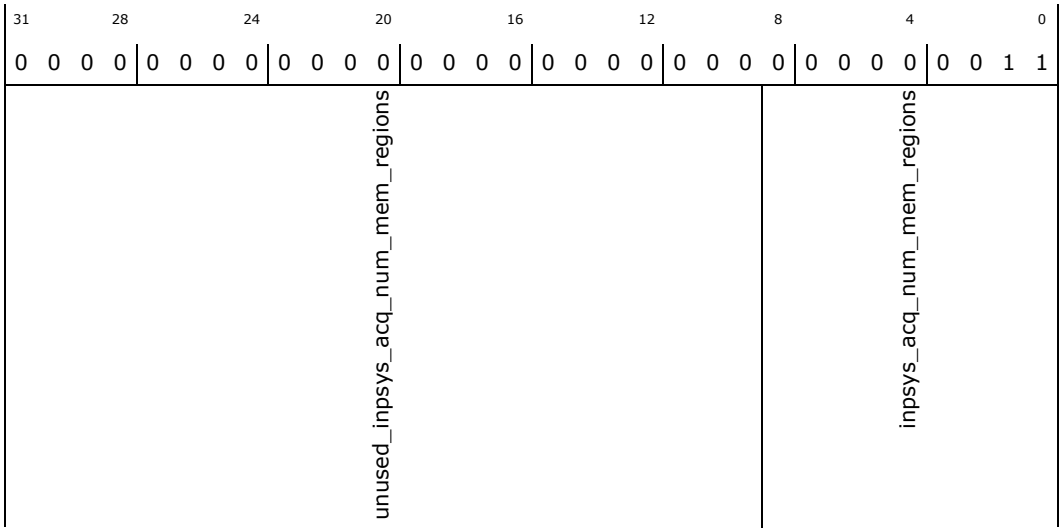
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8902Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000003h



Bit Range	Default and Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved (unused_inpsys_acq_num_mem_regions):** Unused
8:0	0x3 RW	**inpsys_acq_num_mem_regions:** Input System Controller Acquisition number of mem regions

5.3.183 inpsys_ctrl_init (is_2400_inp_sys_inp_ctrl_inpsys_ctrl_init)—Offset 89030h

Input System Controller initialization register

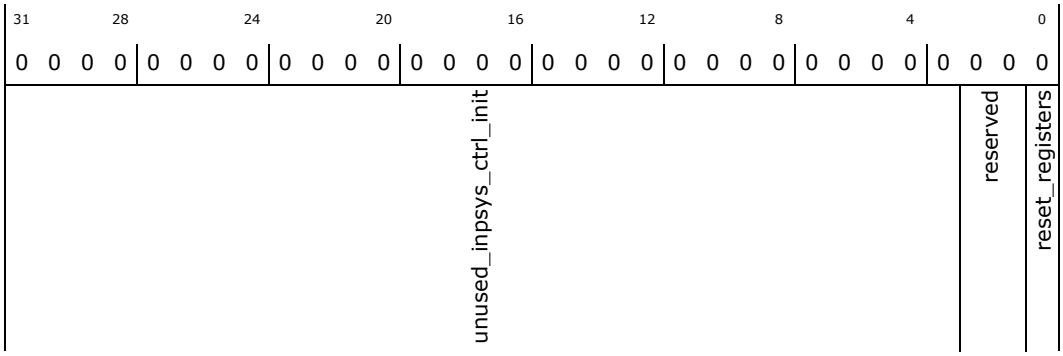
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 89030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:3	0x0 RO	**Reserved (unused_inpsys_ctrl_init):** Unused
2:1	0x0 RW	**reserved:** reserved bits, no action for now
0	0x0 RW	**reset_registers:** Reset all registers in Input System Controller

5.3.184 inpsys_last_cmd (is_2400_inp_sys_inp_ctrl_inpsys_last_cmd)—Offset 89034h

Input System Controller last command register

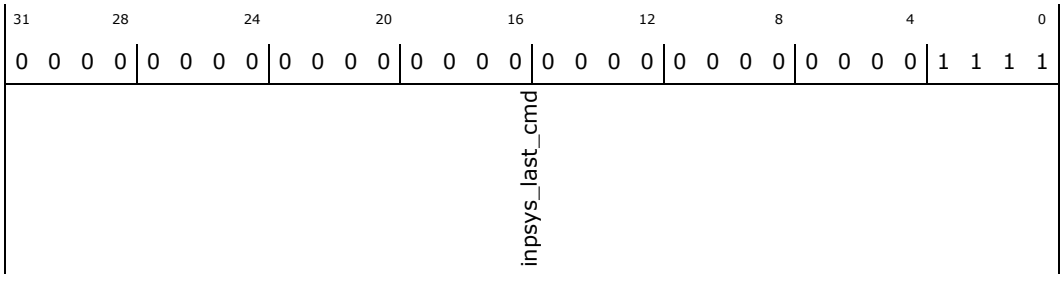
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 89034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**inpsys_last_cmd:** Input System Controller last command register

5.3.185 inpsys_next_cmd (is_2400_inp_sys_inp_ctrl_inpsys_next_cmd)—Offset 89038h

Input System Controller next command register

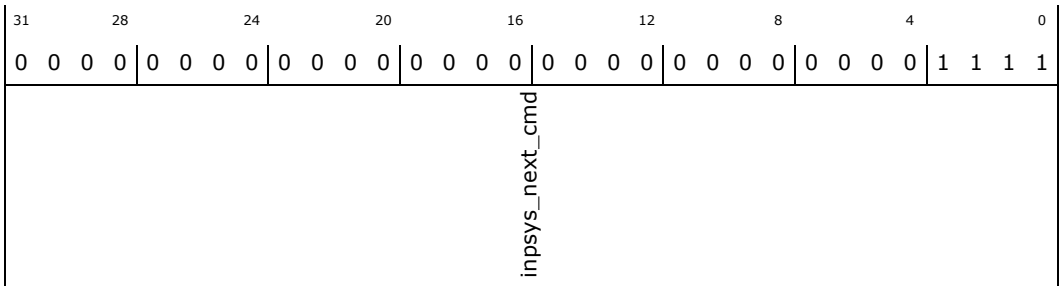
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 89038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**inpsys_next_cmd:** Input System Controller next command register

5.3.186 inpsys_last_ack (is_2400_inp_sys_inp_ctrl_inpsys_last_ack)—Offset 8903Ch

Input System Controller last acknowledge register

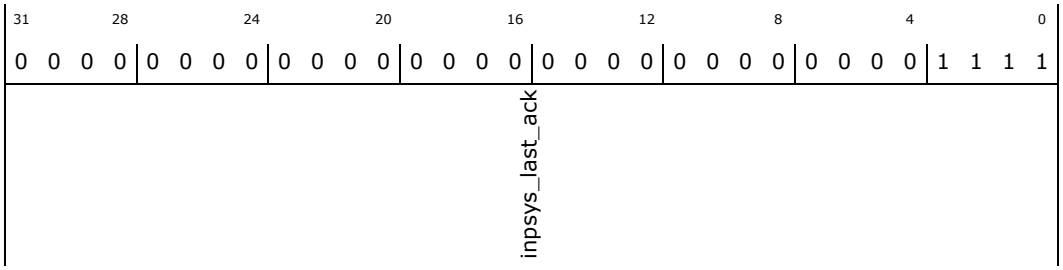
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8903Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**inpsys_last_ack:** Input System Controller last acknowledge register

5.3.187 inpsys_next_ack (is_2400_inp_sys_inp_ctrl_inpsys_next_ack)—Offset 89040h

Input System Controller next acknowledge register

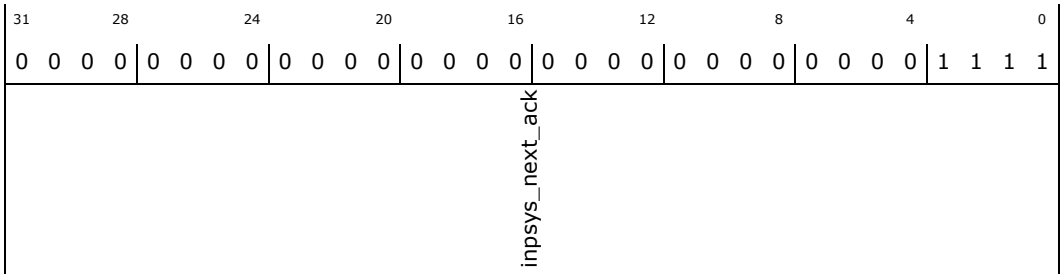
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 89040h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000Fh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xf RO	**inpsys_next_ack:** Input System Controller next acknowledge register

5.3.188 inpsys_top_fsm_state (is_2400_inp_sys_inp_ctrl_inpsys_top_fsm_state)—Offset 89044h

Input System Controller top-ctrl FSM current and next state information Register (both Cmd/Ack FSM)

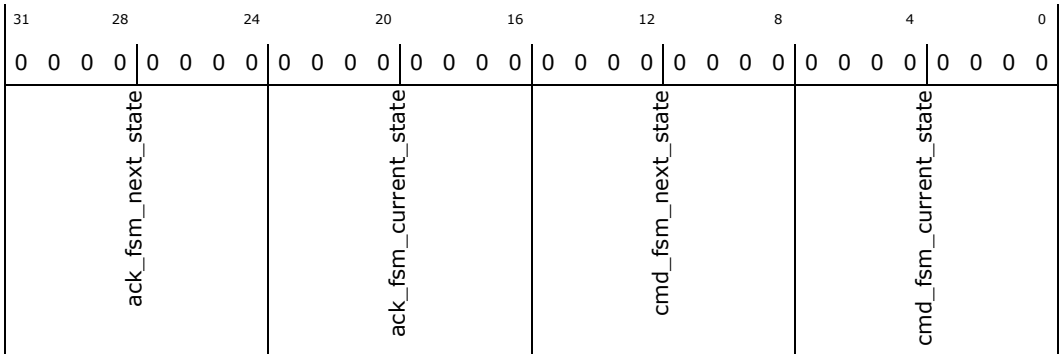
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 89044h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RW	**ack_fsm_next_state:** Next state of top-ctrl Acknowledge FSM
23:16	0x0 RW	**ack_fsm_current_state:** Current state of top-ctrl Acknowledge FSM
15:8	0x0 RW	**cmd_fsm_next_state:** Next state of top-ctrl Command FSM
7:0	0x0 RW	**cmd_fsm_current_state:** Current state of top-ctrl Command FSM

5.3.189 inpsys_captA_fsm_state (is_2400_inp_sys_inp_ctrl_inpsys_captA_fsm_state)—Offset 89048h

Input System Controller CaptureA sub-ctrl current and next state information Register (FSM and DMA cmd state)

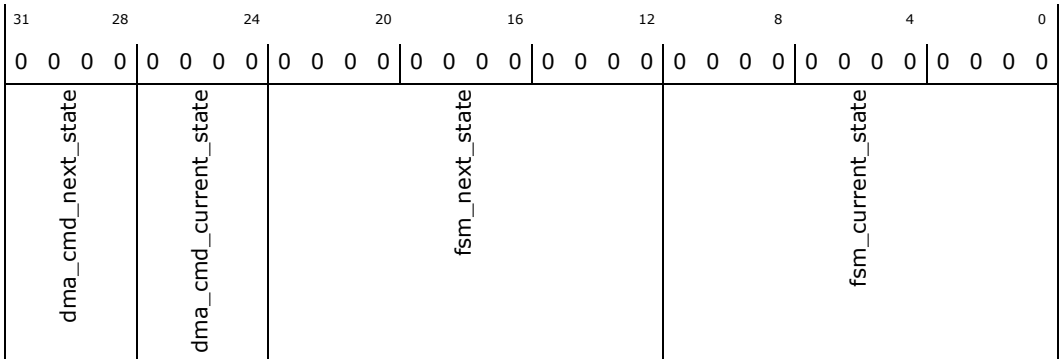
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 89048h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**dma_cmd_next_state:** Next state of DMA cmd
27:24	0x0 RW	**dma_cmd_current_state:** Current state of DMA cmd
23:12	0x0 RW	**fsm_next_state:** Next state of sub-ctrl FSM
11:0	0x0 RW	**fsm_current_state:** Current state of sub-ctrl FSM

5.3.190 inpsys_captB_fsm_state (is_2400_inp_sys_inp_ctrl_inpsys_captB_fsm_state)—Offset 8904Ch

Input System Controller CaptureB sub-ctrl current and next state information Register (FSM and DMA cmd state)

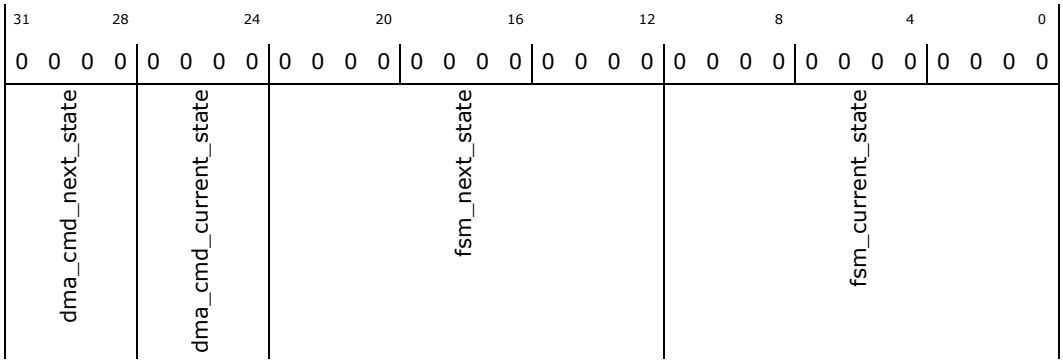
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8904Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**dma_cmd_next_state:** Next state of DMA cmd
27:24	0x0 RW	**dma_cmd_current_state:** Current state of DMA cmd
23:12	0x0 RW	**fsm_next_state:** Next state of sub-ctrl FSM

Bit Range	Default and Access	Field Name (ID): Description
11:0	0x0 RW	**fsm_current_state:** Current state of sub-ctrl FSM

5.3.191 inpsys_captC_fsm_state (is_2400_inp_sys_inp_ctrl_inpsys_captC_fsm_state)—Offset 89050h

Input System Controller CaptureC sub-ctrl current and next state information Register (FSM and DMA cmd state)

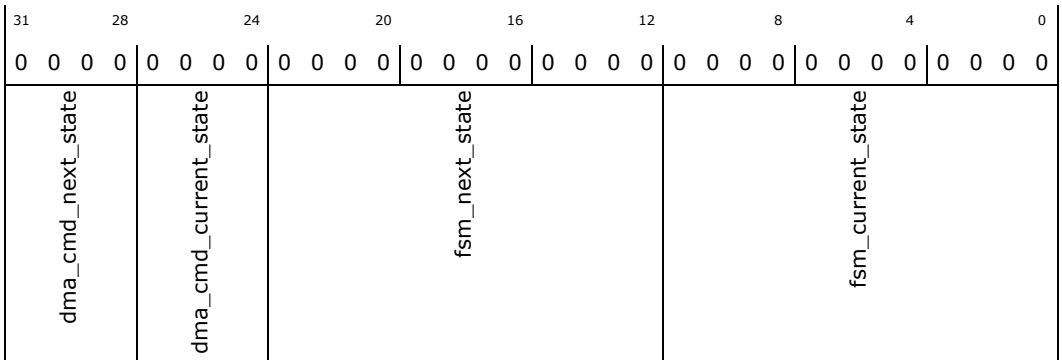
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 89050h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**dma_cmd_next_state:** Next state of DMA cmd
27:24	0x0 RW	**dma_cmd_current_state:** Current state of DMA cmd
23:12	0x0 RW	**fsm_next_state:** Next state of sub-ctrl FSM
11:0	0x0 RW	**fsm_current_state:** Current state of sub-ctrl FSM

5.3.192 inpsys_acq_fsm_state (is_2400_inp_sys_inp_ctrl_inpsys_acq_fsm_state)—Offset 89054h

Input System Controller acquisition sub-ctrl current and next state information Register (FSM and DMA cmd state)

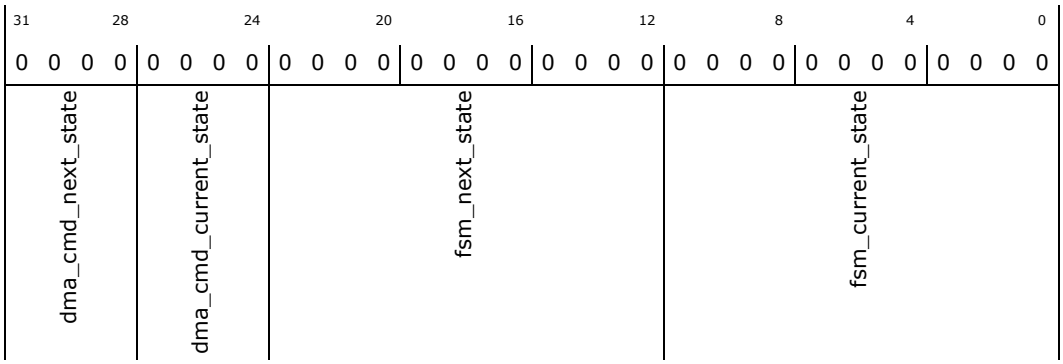
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 89054h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**dma_cmd_next_state:** Next state of DMA cmd
27:24	0x0 RW	**dma_cmd_current_state:** Current state of DMA cmd
23:12	0x0 RW	**fsm_next_state:** Next state of sub-ctrl FSM
11:0	0x0 RW	**fsm_current_state:** Current state of sub-ctrl FSM

5.3.193 inpsys_capt_reserve_one_mem_region (is_2400_inp_sys_inp_ctrl_inpsys_capt_reserve_one_mem_region)—Offset 89058h

Reserve 1 or 0 mem region of capture units in input buffer to avoid overflow of captured data. 0: zero mem region reserved, 1: one mem region reserved

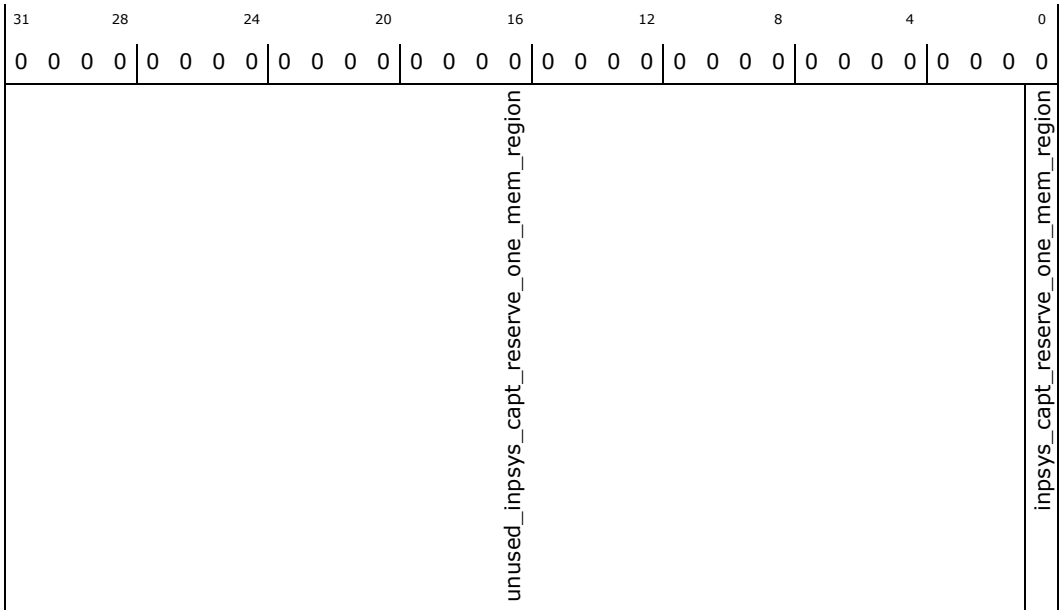
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 89058h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_inpsys_capt_reserve_one_mem_region):** Unused
0	0x0 RW	**inpsys_capt_reserve_one_mem_region:** Reserve 1 or 0 mem region of capture units in input buffer to avoid overflow of captured data. 0: zero mem region reserved, 1: one mem region reserved

5.3.194 str_multicastA_sel (is_2400_inp_sys_gpreg_str_multicastA_sel)—Offset 8A000h

StreamMulticastA_select

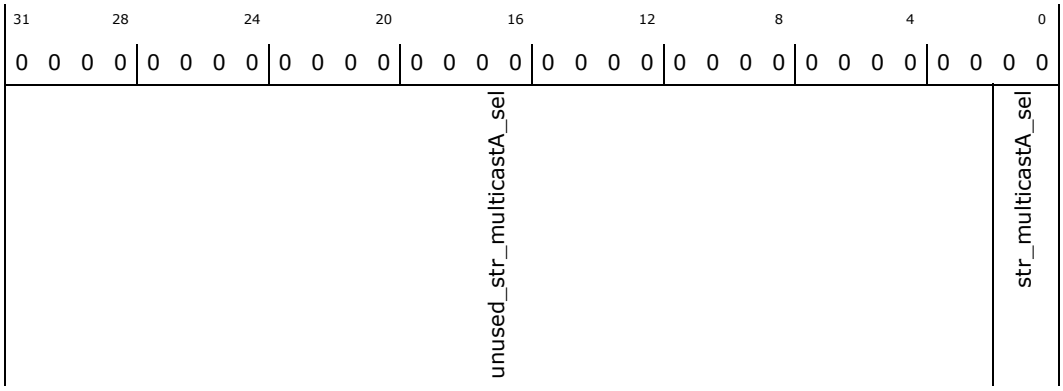
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8A000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_str_multicastA_sel):** Unused
1:0	0x0 RW	**str_multicastA_sel:** StreamMulticastA_select

5.3.195 str_multicastB_sel (is_2400_inp_sys_gpreg_str_multicastB_sel)—Offset 8A004h

StreamMulticastB_select

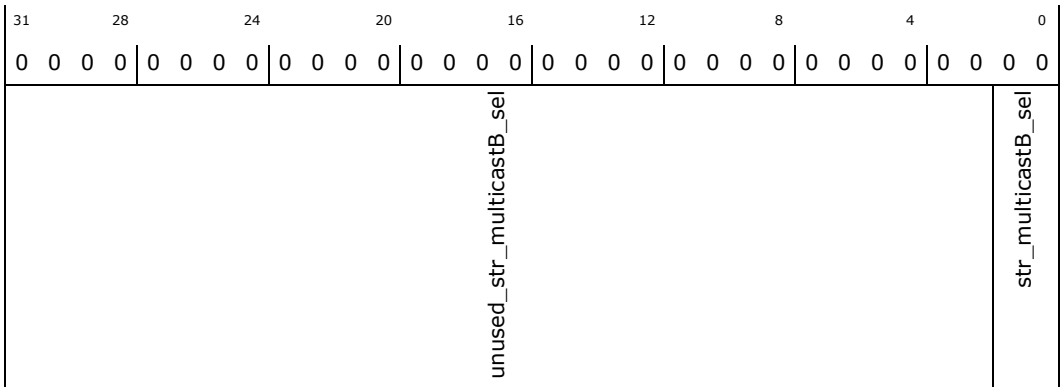
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8A004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_str_multicastB_sel):** Unused
1:0	0x0 RW	**str_multicastB_sel:** StreamMulticastB_select

5.3.196 str_multicastC_sel (is_2400_inp_sys_gpreg_str_multicastC_sel)—Offset 8A008h

StreamMulticastC_select

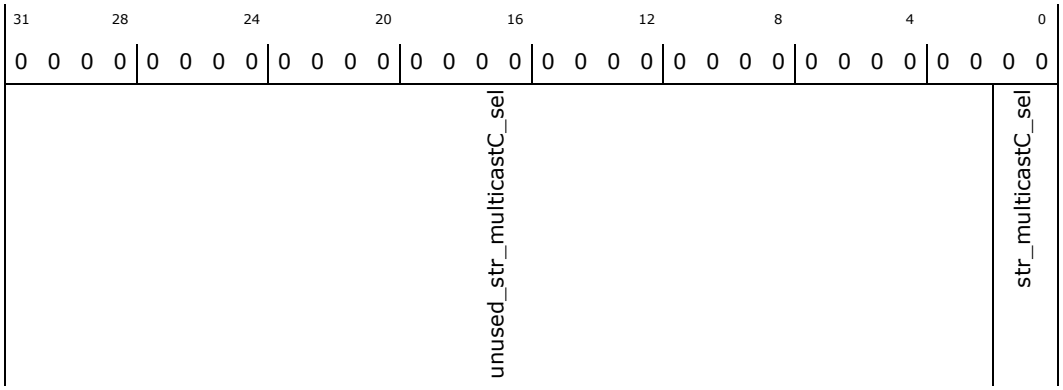
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8A008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_str_multicastC_sel):** Unused
1:0	0x0 RW	**str_multicastC_sel:** StreamMulticastC_select

5.3.197 str_mux_sel (is_2400_inp_sys_gpreg_str_mux_sel)—Offset 8A00Ch

StreamMux_select

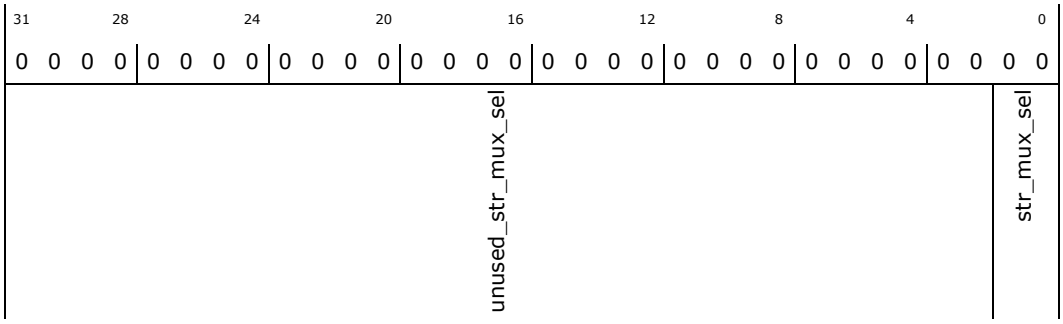
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8A00Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_str_mux_sel):** Unused
1:0	0x0 RW	**str_mux_sel:** StreamMux_select

5.3.198 str_mon_status (is_2400_inp_sys_gpreg_str_mon_status)—Offset 8A010h

Streaming Monitor Status, [accept, valid] of streaming port

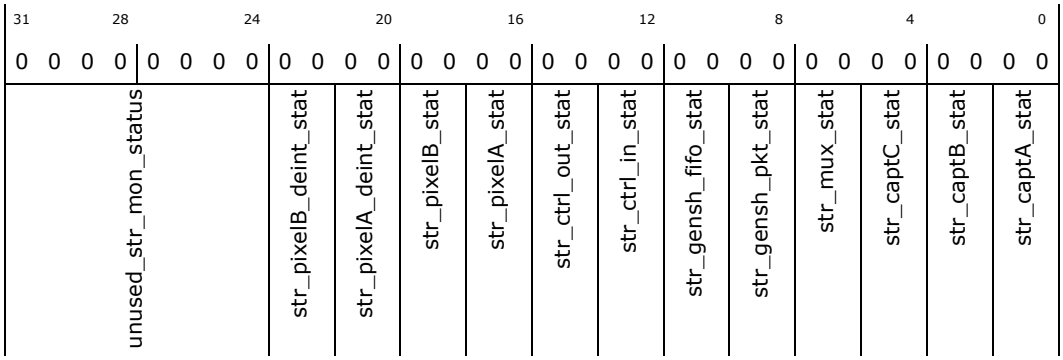
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8A010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (unused_str_mon_status):** Unused
23:22	0x0 RW	**str_pixelB_deint_stat:** Pixel B streaming output from Stream Deinterleaver
21:20	0x0 RW	**str_pixelA_deint_stat:** Pixel A streaming output from Stream Deinterleaver
19:18	0x0 RW	**str_pixelB_stat:** Pixel B streaming output from CSI receiver
17:16	0x0 RW	**str_pixelA_stat:** Pixel A streaming output from CSI receiver
15:14	0x0 RW	**str_ctrl_out_stat:** Control streaming output
13:12	0x0 RW	**str_ctrl_in_stat:** Control streaming input
11:10	0x0 RW	**str_gensh_fifo_stat:** Generic short FIFO streaming output
9:8	0x0 RW	**str_gensh_pkt_stat:** Generic short packet streaming output from CSI receiver
7:6	0x0 RW	**str_mux_stat:** Stream Mux streaming output
5:4	0x0 RW	**str_captC_stat:** Capture port C streaming output from CSI receiver
3:2	0x0 RW	**str_captB_stat:** Capture port B streaming output from CSI receiver
1:0	0x0 RW	**str_captA_stat:** Capture port A streaming output from CSI receiver

5.3.199 str_mon_irq_cond (is_2400_inp_sys_gpreg_str_mon_irq_cond)—Offset 8A014h

Streaming Monitor IRQ condition, [accept, valid] for streaming port

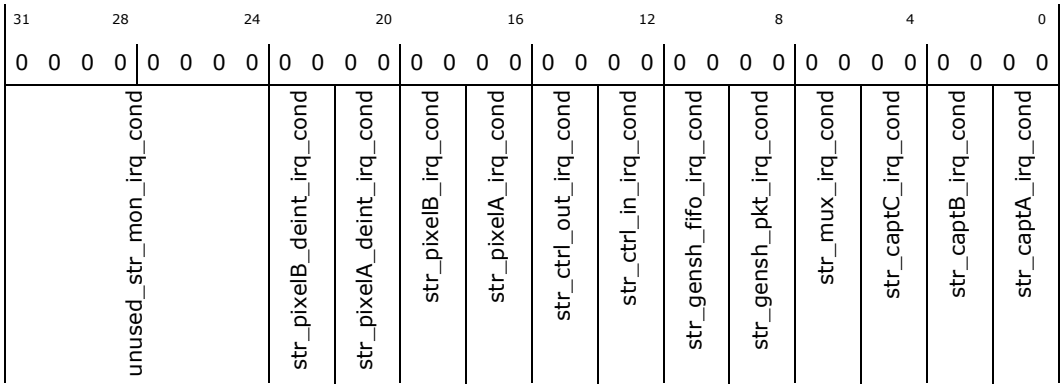
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8A014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (unused_str_mon_irq_cond):** Unused
23:22	0x0 RW	**str_pixelB_deint_irq_cond:** Pixel B streaming output from Stream Deinterleaver
21:20	0x0 RW	**str_pixelA_deint_irq_cond:** Pixel A streaming output from Stream Deinterleaver
19:18	0x0 RW	**str_pixelB_irq_cond:** Pixel B streaming output from CSI receiver
17:16	0x0 RW	**str_pixelA_irq_cond:** Pixel A streaming output from CSI receiver
15:14	0x0 RW	**str_ctrl_out_irq_cond:** Control streaming output
13:12	0x0 RW	**str_ctrl_in_irq_cond:** Control streaming input
11:10	0x0 RW	**str_gensh_fifo_irq_cond:** Generic short FIFO streaming output
9:8	0x0 RW	**str_gensh_pkt_irq_cond:** Generic short packet streaming output from CSI receiver
7:6	0x0 RW	**str_mux_irq_cond:** Stream Mux streaming output
5:4	0x0 RW	**str_captC_irq_cond:** Capture port C streaming output from CSI receiver
3:2	0x0 RW	**str_captB_irq_cond:** Capture port B streaming output from CSI receiver
1:0	0x0 RW	**str_captA_irq_cond:** Capture port A streaming output from CSI receiver

5.3.200 str_mon_irq_en (is_2400_inp_sys_gpreg_str_mon_irq_en)—Offset 8A018h

Streaming Monitor IRQ Enable

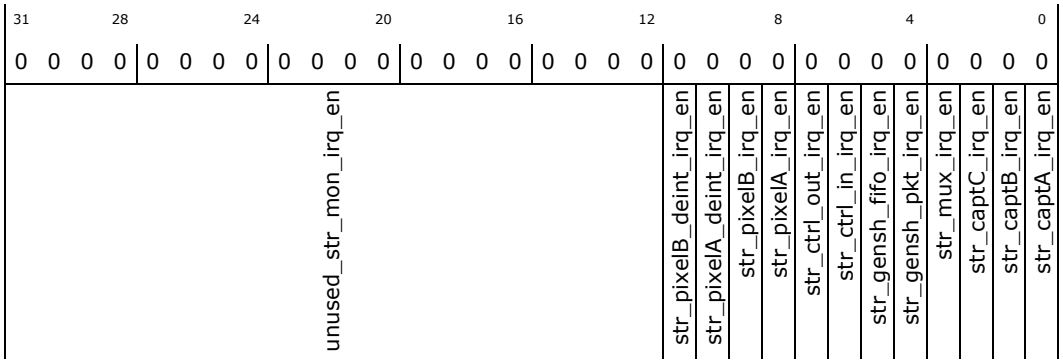
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8A018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved (unused_str_mon_irq_en):** Unused
11	0x0 RW	**str_pixelB_deint_irq_en:** Pixel B streaming output from Stream Deinterleaver
10	0x0 RW	**str_pixelA_deint_irq_en:** Pixel A streaming output from Stream Deinterleaver
9	0x0 RW	**str_pixelB_irq_en:** Pixel B streaming output from CSI receiver
8	0x0 RW	**str_pixelA_irq_en:** Pixel A streaming output from CSI receiver
7	0x0 RW	**str_ctrl_out_irq_en:** Control streaming output
6	0x0 RW	**str_ctrl_in_irq_en:** Control streaming input
5	0x0 RW	**str_gensh_fifo_irq_en:** Generic short FIFO streaming output
4	0x0 RW	**str_gensh_pkt_irq_en:** Generic short packet streaming output from CSI receiver
3	0x0 RW	**str_mux_irq_en:** Stream Mux streaming output
2	0x0 RW	**str_captC_irq_en:** Capture port C streaming output from CSI receiver
1	0x0 RW	**str_captB_irq_en:** Capture port B streaming output from CSI receiver
0	0x0 RW	**str_captA_irq_en:** Capture port A streaming output from CSI receiver

5.3.201 isys_srst (is_2400_inp_sys_gpreg_isys_srst)—Offset 8A01Ch

Soft resets the modules of the input system. Writing a 1 to a field brings a module in reset, writing a 0 brings that module out of reset

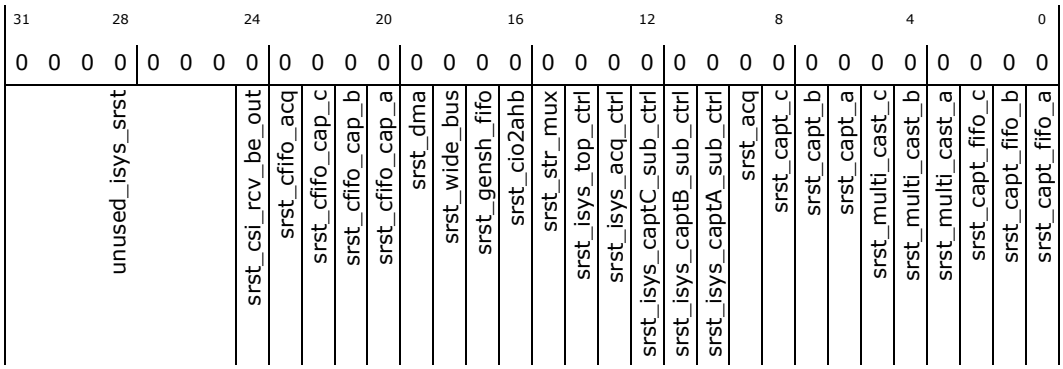
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8A01Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:25	0x0 RO	**Reserved (unused_isys_srst):** Unused
24	0x0 RW	**srst_csi_rcv_be_out:** Soft resets the output of the CSI receiver backend
23	0x0 RW	**srst_cfifo_acq:** Soft resets the control and acknowledge FIFOs for the acquisition unit
22	0x0 RW	**srst_cfifo_cap_c:** Soft resets the control and acknowledge FIFOs for capture unit C
21	0x0 RW	**srst_cfifo_cap_b:** Soft resets the control and acknowledge FIFOs for capture unit B
20	0x0 RW	**srst_cfifo_cap_a:** Soft resets the control and acknowledge FIFOs for capture unit A
19	0x0 RW	**srst_dma:** Soft resets the DMA
18	0x0 RW	**srst_wide_bus:** Soft resets the wide bus including the CIO converter
17	0x0 RW	**srst_gensh_fifo:** Soft resets the generic short FIFO
16	0x0 RW	**srst_cio2ahb:** Soft resets the CIO2AHB adapter

Bit Range	Default and Access	Field Name (ID): Description
15	0x0 RW	**srst_str_mux:** Soft resets the streaming mux
14	0x0 RW	**srst_isys_top_ctrl:** Soft resets the input system Top controller
13	0x0 RW	**srst_isys_acq_ctrl:** Soft resets the input system Acquisition sub-controller (controls data-path from selected captA/captB/captC/dma_acq to acq)
12	0x0 RW	**srst_isys_captC_sub_ctrl:** Soft resets the input system CaptureC sub-controller (controls data-path from captC to dma_captC)
11	0x0 RW	**srst_isys_captB_sub_ctrl:** Soft resets the input system CaptureB sub-controller (controls data-path from captB to dma_captB)
10	0x0 RW	**srst_isys_captA_sub_ctrl:** Soft resets the input system CaptureA sub-controller (controls data-path from captA to dma_captA)
9	0x0 RW	**srst_acq:** Soft resets the equation unit
8	0x0 RW	**srst_capt_c:** Soft resets the capture unit C
7	0x0 RW	**srst_capt_b:** Soft resets the capture unit B
6	0x0 RW	**srst_capt_a:** Soft resets the capture unit A
5	0x0 RW	**srst_multi_cast_c:** Soft resets multi cast C
4	0x0 RW	**srst_multi_cast_b:** Soft resets multi cast B
3	0x0 RW	**srst_multi_cast_a:** Soft resets multi cast A
2	0x0 RW	**srst_capt_fifo_c:** Soft resets the FIFO before multi cast C
1	0x0 RW	**srst_capt_fifo_b:** Soft resets the FIFO before multi cast B
0	0x0 RW	**srst_capt_fifo_a:** Soft resets the FIFO before multi cast A

5.3.202 isys_slv_reg_srst (is_2400_inp_sys_gpreg_isys_slv_reg_srst)—Offset 8A020h

Soft resets the slave accessible registers of certain input system modules. Writing a 1 to a field brings the registers for a module to their default value, writing a 0 allows them to be overwritten

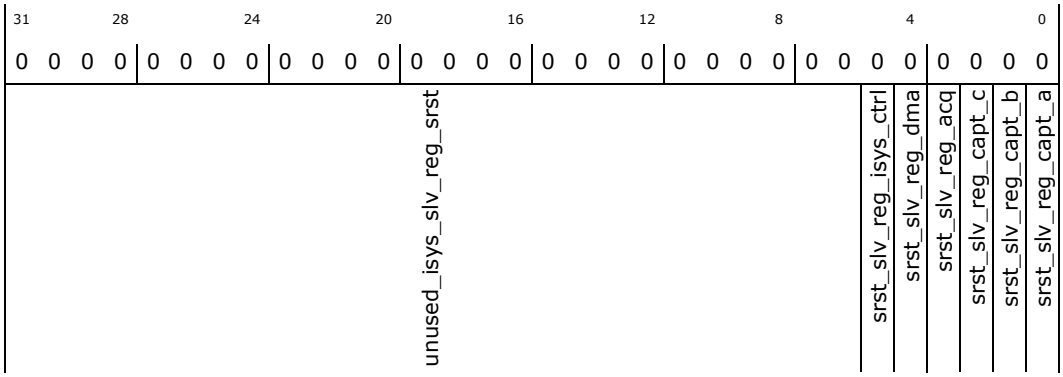
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8A020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RO	**Reserved (unused_isys_slv_reg_srst):** Unused
5	0x0 RW	**srst_slv_reg_isys_ctrl:** Soft resets the slave accessible registers of the input system controller
4	0x0 RW	**srst_slv_reg_dma:** Soft resets the slave accessible registers of the DMA
3	0x0 RW	**srst_slv_reg_acq:** Soft resets the slave accessible registers of the acquisition unit
2	0x0 RW	**srst_slv_reg_capt_c:** Soft resets the slave accessible registers of capture unit C
1	0x0 RW	**srst_slv_reg_capt_b:** Soft resets the slave accessible registers of capture unit B
0	0x0 RW	**srst_slv_reg_capt_a:** Soft resets the slave accessible registers of capture unit A

5.3.203 str_deint_portA_cnt (is_2400_inp_sys_gpreg_str_deint_portA_cnt)—Offset 8A024h

stream data count for portA of stream de-interleave block

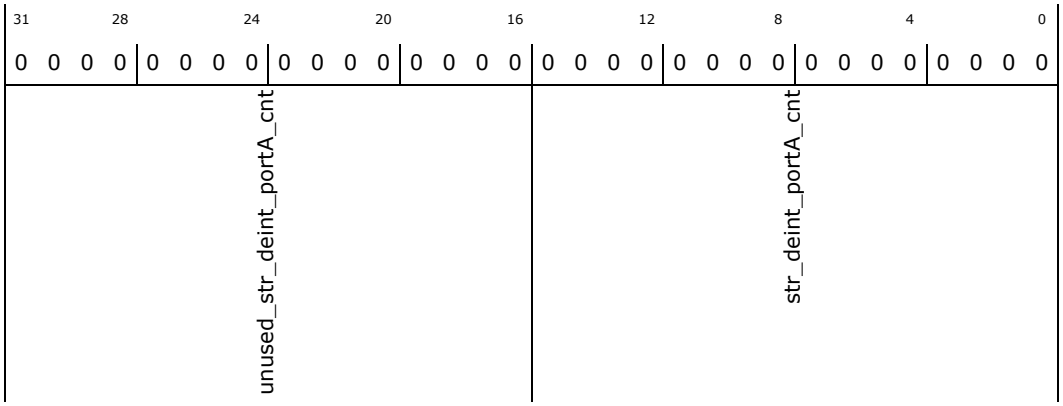
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8A024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_str_deint_portA_cnt):** Unused
15:0	0x0 RW	**str_deint_portA_cnt:** stream data count for portA of stream de-interleave block

5.3.204 str_deint_portB_cnt (is_2400_inp_sys_gpreg_str_deint_portB_cnt)—Offset 8A028h

stream data count for PortB of stream de-interleave block

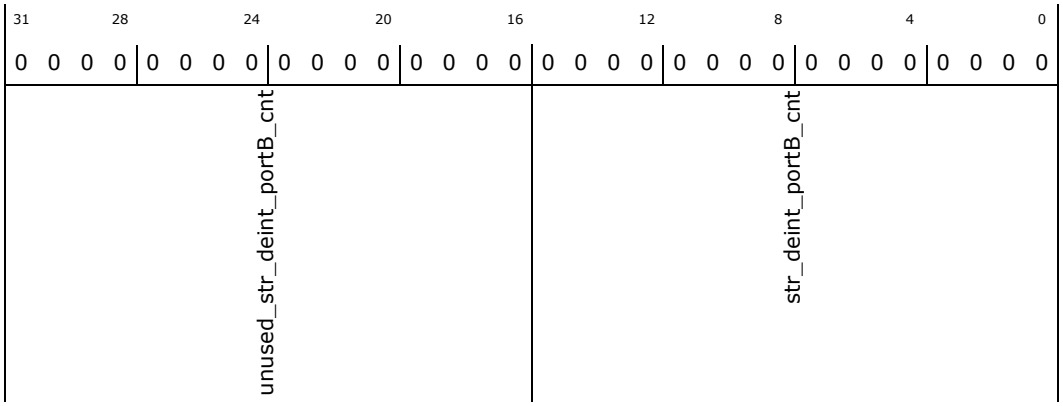
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8A028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (unused_str_deint_portB_cnt):** Unused
15:0	0x0 RW	**str_deint_portB_cnt:** stream data count for PortB of stream de-interleave block

5.3.205 CSI_generic_short_packet (is_2400_inp_sys_fifo_adapter_CSI_generic_short_packet)—Offset 8B000h

Received data from generic short packet streaming port

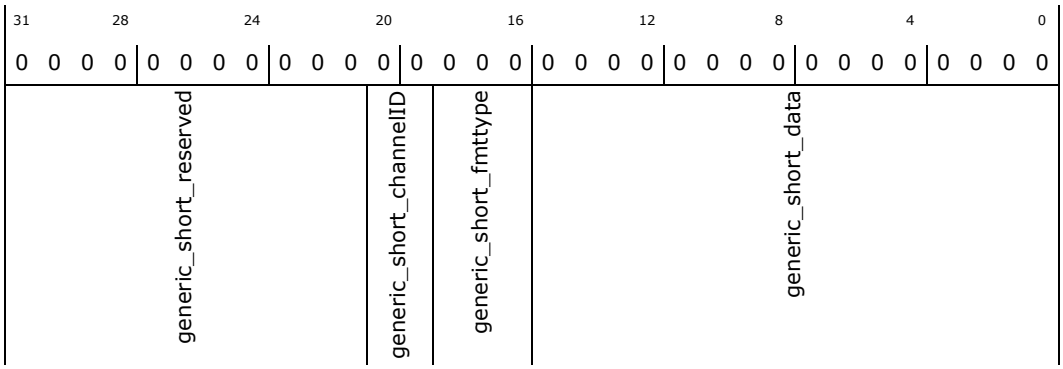
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8B000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:21	0x0 RO	**generic_short_reserved:** Reserved, tied to 0
20:19	0x0 RO	**generic_short_channelID:** Generic Short Channel ID from CSI receiver
18:16	0x0 RO	**generic_short_fmttype:** Generic Short Format Type from CSI receiver
15:0	0x0 RO	**generic_short_data:** Generic Short Data from CSI receiver

5.3.206 CSI_generic_short_packet_available (is_2400_inp_sys_fifo_adapter_CSI_generic_short_packet_available)—Offset 8B008h

Returns 1 if there is a generic short packet available. Returns 0 is there is no generic short packet available.

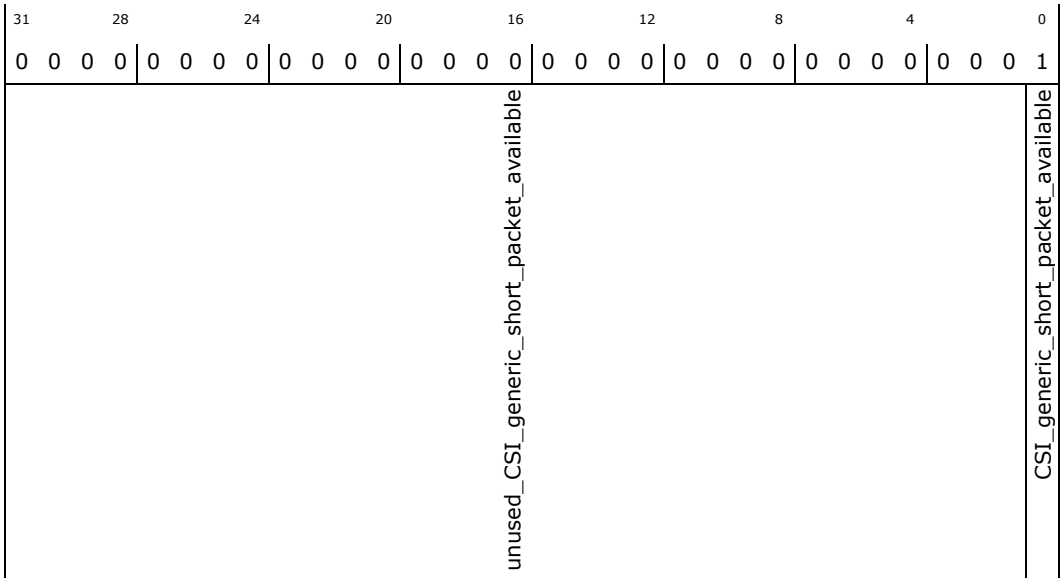
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8B008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_CSI_generic_short_packet_available):** Unused
0	0x1 RO	**CSI_generic_short_packet_available:** Returns 1 if there is a generic short packet available. Returns 0 is there is no generic short packet available.

5.3.207 irq_edge (is_2400_inp_sys_irq_ctrl_irq_edge)—Offset 8C000h

IRQ active edge select per interrupt input. Rising edge: 1, Falling edge: 0

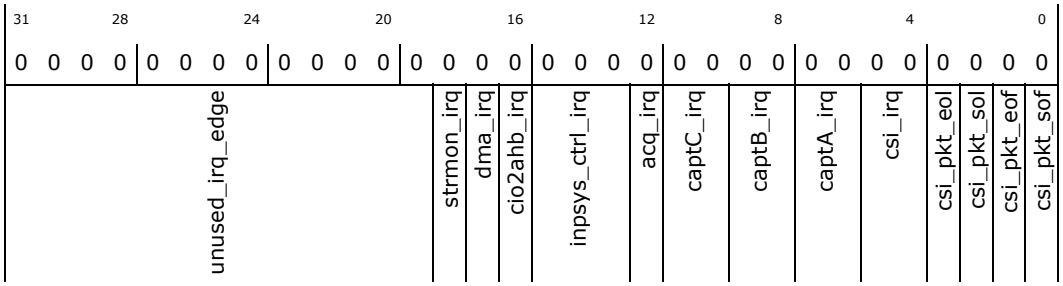
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8C000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:19	0x0 RO	**Reserved (unused_irq_edge):** Unused
18	0x0 RW	**strmon_irq:** Streaming monitor interrupt request
17	0x0 RO	**dma_irq:** DMA interrupt request
16	0x0 RW	**cio2ahb_irq:** CIO to AHB converter (for CSI receiver AHB slave) interrupt request
15:13	0x0 RW	**inpsys_ctrl_irq:** Input system controller interrupt request
12	0x0 RW	**acq_irq:** Acquisition unit interrupt request
11:10	0x0 RW	**captC_irq:** Capture unit C interrupt request
9:8	0x0 RW	**captB_irq:** Capture unit B interrupt request
7:6	0x0 RW	**captA_irq:** Capture unit A interrupt request
5:4	0x0 RW	**csi_irq:** CSI receiver interrupt request
3	0x0 RW	**csi_pkt_eol:** End of Line of Frame packet from CSI receiver
2	0x0 RW	**csi_pkt_sol:** Start of Line packet from CSI receiver
1	0x0 RW	**csi_pkt_eof:** End of Frame packet from CSI receiver
0	0x0 RW	**csi_pkt_sof:** Start of Frame packet from CSI receiver

5.3.208 irq_mask (is_2400_inp_sys_irq_ctrl_irq_mask)—Offset 8C004h

IRQ Mask Per Interrupt

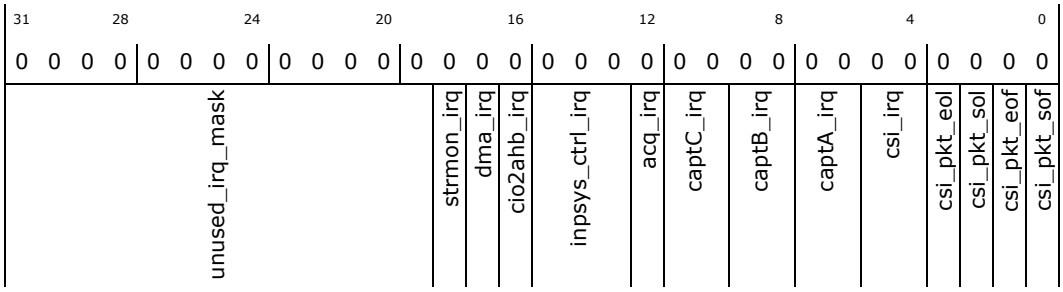
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8C004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:19	0x0 RO	**Reserved (unused_irq_mask):** Unused
18	0x0 RW	**strmon_irq:** Streaming monitor interrupt request
17	0x0 RO	**dma_irq:** DMA interrupt request
16	0x0 RW	**cio2ahb_irq:** CIO to AHB converter (for CSI receiver AHB slave) interrupt request
15:13	0x0 RW	**inpsys_ctrl_irq:** Input system controller interrupt request
12	0x0 RW	**acq_irq:** Acquisition unit interrupt request
11:10	0x0 RW	**captC_irq:** Capture unit C interrupt request
9:8	0x0 RW	**captB_irq:** Capture unit B interrupt request
7:6	0x0 RW	**captA_irq:** Capture unit A interrupt request
5:4	0x0 RW	**csi_irq:** CSI receiver interrupt request
3	0x0 RW	**csi_pkt_eol:** End of Line of Frame packet from CSI receiver
2	0x0 RW	**csi_pkt_sol:** Start of Line packet from CSI receiver
1	0x0 RW	**csi_pkt_eof:** End of Frame packet from CSI receiver
0	0x0 RW	**csi_pkt_sof:** Start of Frame packet from CSI receiver

5.3.209 irq_status (is_2400_inp_sys_irq_ctrl_irq_status)—Offset 8C008h

IRQ Status for each Unmasked Interrupt

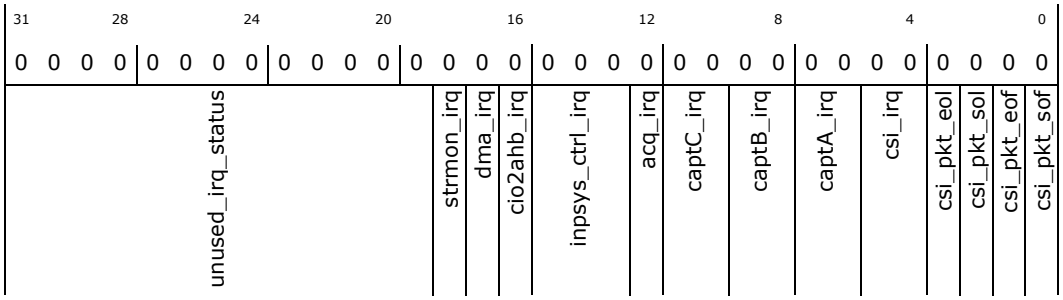
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8C008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:19	0x0 RO	**Reserved (unused_irq_status):** Unused
18	0x0 RO	**strmon_irq:** Streaming monitor interrupt request
17	0x0 RO	**dma_irq:** DMA interrupt request
16	0x0 RO	**cio2ahb_irq:** CIO to AHB converter (for CSI receiver AHB slave) interrupt request
15:13	0x0 RO	**inpsys_ctrl_irq:** Input system controller interrupt request
12	0x0 RO	**acq_irq:** Acquisition unit interrupt request
11:10	0x0 RO	**captC_irq:** Capture unit C interrupt request
9:8	0x0 RO	**captB_irq:** Capture unit B interrupt request
7:6	0x0 RO	**captA_irq:** Capture unit A interrupt request
5:4	0x0 RO	**csi_irq:** CSI receiver interrupt request
3	0x0 RO	**csi_pkt_eol:** End of Line of Frame packet from CSI receiver
2	0x0 RO	**csi_pkt_sol:** Start of Line packet from CSI receiver

Bit Range	Default and Access	Field Name (ID): Description
1	0x0 RO	**csi_pkt_eof:** End of Frame packet from CSI receiver
0	0x0 RO	**csi_pkt_sof:** Start of Frame packet from CSI receiver

5.3.210 irq_clear (is_2400_inp_sys_irq_ctrl_irq_clear)—Offset 8C00Ch

IRQ clear for interrupt set in irq_status

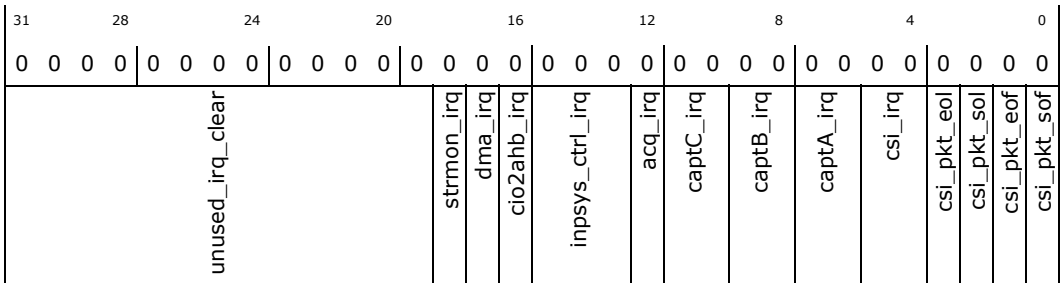
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8C00Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:19	0x0 RO	**Reserved (unused_irq_clear):** Unused
18	0x0 WO	**strmon_irq:** Streaming monitor interrupt request
17	0x0 RO	**dma_irq:** DMA interrupt request
16	0x0 WO	**cio2ahb_irq:** CIO to AHB converter (for CSI receiver AHB slave) interrupt request
15:13	0x0 WO	**inpsys_ctrl_irq:** Input system controller interrupt request
12	0x0 WO	**acq_irq:** Acquisition unit interrupt request
11:10	0x0 WO	**captC_irq:** Capture unit C interrupt request
9:8	0x0 WO	**captB_irq:** Capture unit B interrupt request

Bit Range	Default and Access	Field Name (ID): Description
7:6	0x0 WO	**captA_irq:** Capture unit A interrupt request
5:4	0x0 WO	**csi_irq:** CSI receiver interrupt request
3	0x0 WO	**csi_pkt_eol:** End of Line of Frame packet from CSI receiver
2	0x0 WO	**csi_pkt_sol:** Start of Line packet from CSI receiver
1	0x0 WO	**csi_pkt_eof:** End of Frame packet from CSI receiver
0	0x0 WO	**csi_pkt_sof:** Start of Frame packet from CSI receiver

5.3.211 irq_en (is_2400_inp_sys_irq_ctrl_irq_en)—Offset 8C010h

IRQ Enable per interrupt bit

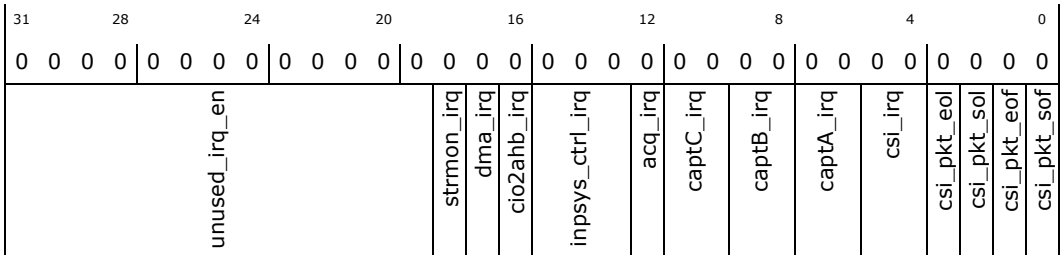
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8C010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:19	0x0 RO	**Reserved (unused_irq_en):** Unused
18	0x0 RW	**strmon_irq:** Streaming monitor interrupt request
17	0x0 RO	**dma_irq:** DMA interrupt request
16	0x0 RW	**cio2ahb_irq:** CIO to AHB converter (for CSI receiver AHB slave) interrupt request
15:13	0x0 RW	**inpsys_ctrl_irq:** Input system controller interrupt request
12	0x0 RW	**acq_irq:** Acquisition unit interrupt request
11:10	0x0 RW	**captC_irq:** Capture unit C interrupt request
9:8	0x0 RW	**captB_irq:** Capture unit B interrupt request
7:6	0x0 RW	**captA_irq:** Capture unit A interrupt request
5:4	0x0 RW	**csi_irq:** CSI receiver interrupt request
3	0x0 RW	**csi_pkt_eol:** End of Line of Frame packet from CSI receiver
2	0x0 RW	**csi_pkt_sol:** Start of Line packet from CSI receiver
1	0x0 RW	**csi_pkt_eof:** End of Frame packet from CSI receiver
0	0x0 RW	**csi_pkt_sof:** Start of Frame packet from CSI receiver

5.3.212 irq_level_not_pulse (is_2400_inp_sys_irq_ctrl_irq_level_not_pulse)—Offset 8C014h

IRQ setting per interrupt bit for level or pulse IRQ generation at output pin. Level: 1, Pulse: 0

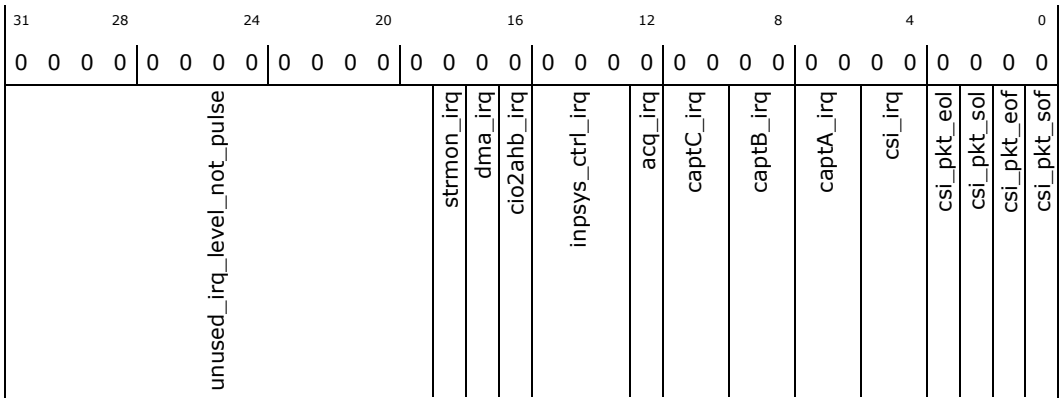
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 8C014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:19	0x0 RO	**Reserved (unused_irq_level_not_pulse):** Unused
18	0x0 RW	**strmon_irq:** Streaming monitor interrupt request
17	0x0 RO	**dma_irq:** DMA interrupt request
16	0x0 RW	**cio2ahb_irq:** CIO to AHB converter (for CSI receiver AHB slave) interrupt request
15:13	0x0 RW	**inpsys_ctrl_irq:** Input system controller interrupt request
12	0x0 RW	**acq_irq:** Acquisition unit interrupt request
11:10	0x0 RW	**captC_irq:** Capture unit C interrupt request
9:8	0x0 RW	**captB_irq:** Capture unit B interrupt request
7:6	0x0 RW	**captA_irq:** Capture unit A interrupt request

Bit Range	Default and Access	Field Name (ID): Description
5:4	0x0 RW	**csi_irq:** CSI receiver interrupt request
3	0x0 RW	**csi_pkt_eol:** End of Line of Frame packet from CSI receiver
2	0x0 RW	**csi_pkt_sol:** Start of Line packet from CSI receiver
1	0x0 RW	**csi_pkt_eof:** End of Frame packet from CSI receiver
0	0x0 RW	**csi_pkt_sof:** Start of Frame packet from CSI receiver

5.3.213 reg_gp_syncgen_enable (is_2400_isel_gpr_reg_gp_syncgen_enable)—Offset 90000h

Enables (value=1) or disables (value=0) the Sync Generator.

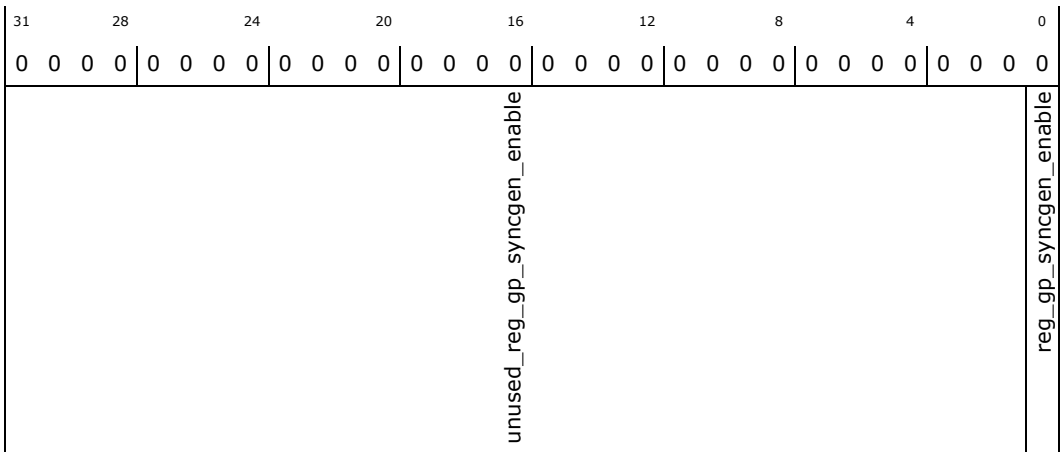
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_gp_syncgen_enable):** Unused

Bit Range	Default and Access	Field Name (ID): Description
0	0x0 RW	**reg_gp_syncgen_enable:** Enables (value=1) or disables (value=0) the Sync Generator.

5.3.214 reg_gp_syncgen_free_running (is_2400_isel_gpr_reg_gp_syncgen_free_running)—Offset 90004h

Sets the sync generator in free running mode (value=1) or let it stall in sync with either the PRBS or TPG (value=0)

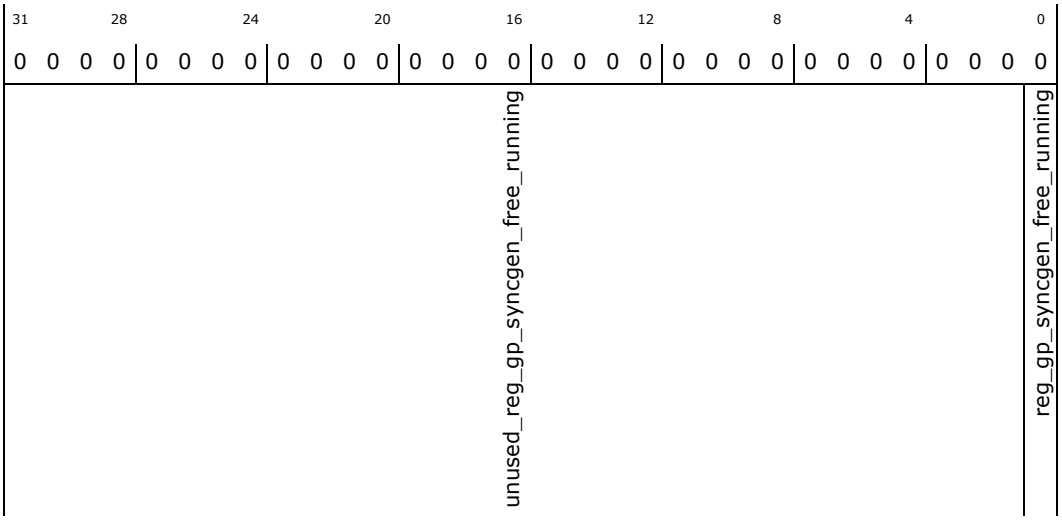
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_gp_syncgen_free_running):** Unused
0	0x0 RW	**reg_gp_syncgen_free_running:** Sets the sync generator in free running mode (value=1) or let it stall in sync with either the PRBS or TPG (value=0)

5.3.215 reg_gp_syncgen_pause (is_2400_isel_gpr_reg_gp_syncgen_pause)—Offset 90008h

Sets the sync generator in pause mode (value=1) or not (value=0)

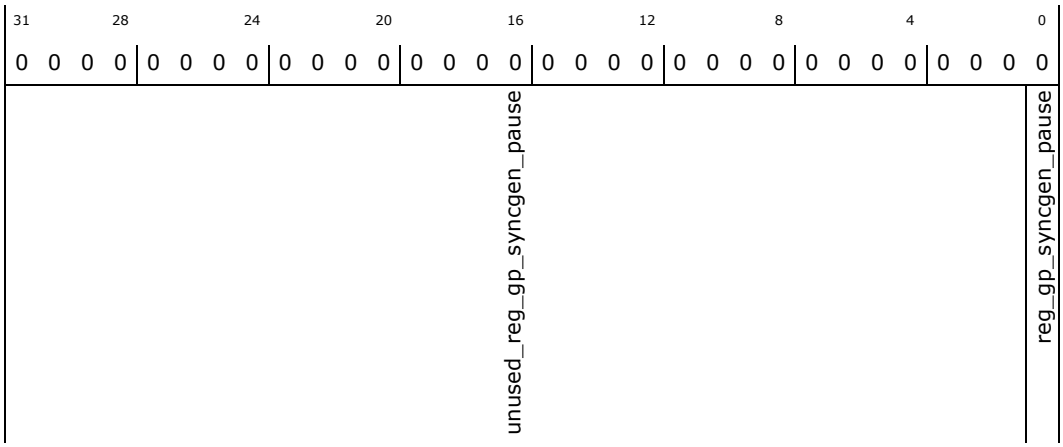
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_gp_syncgen_pause):** Unused
0	0x0 RW	**reg_gp_syncgen_pause:** Sets the sync generator in pause mode (value=1) or not (value=0)

5.3.216 reg_gp_nr_frames (is_2400_isel_gpr_reg_gp_nr_frames)—Offset 9000Ch

Sets the sync generator parameter Number of Frames

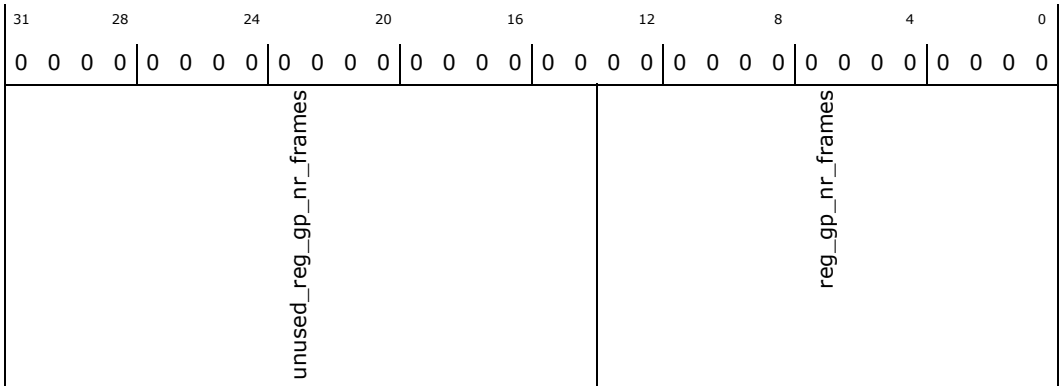
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 9000Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RW	**Reserved (unused_reg_gp_nr_frames):** Unused
13:0	0x0 RW	**reg_gp_nr_frames:** Sets the sync generator parameter Number of Frames

5.3.217 reg_gp_syngen_nr_pix (is_2400_isel_gpr_reg_gp_syngen_nr_pix)—Offset 90010h

Sets the number of active pixels per line in the Sync Generator

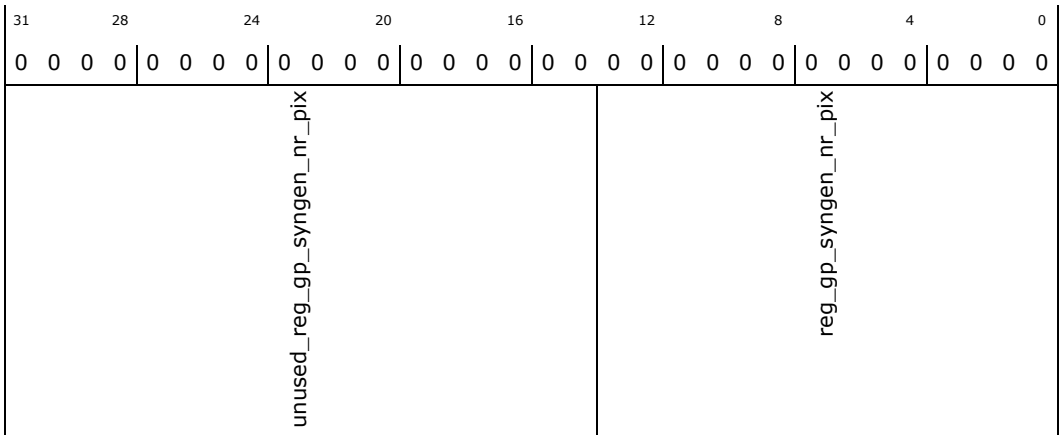
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RW	**Reserved (unused_reg_gp_syngen_nr_pix):** Unused
13:0	0x0 RW	**reg_gp_syngen_nr_pix:** Sets the number of active pixels per line in the Sync Generator

5.3.218 reg_gp_syngen_nr_lines (is_2400_isel_gpr_reg_gp_syngen_nr_lines)—Offset 90014h

Sets the number of lines per frame in the Sync generator

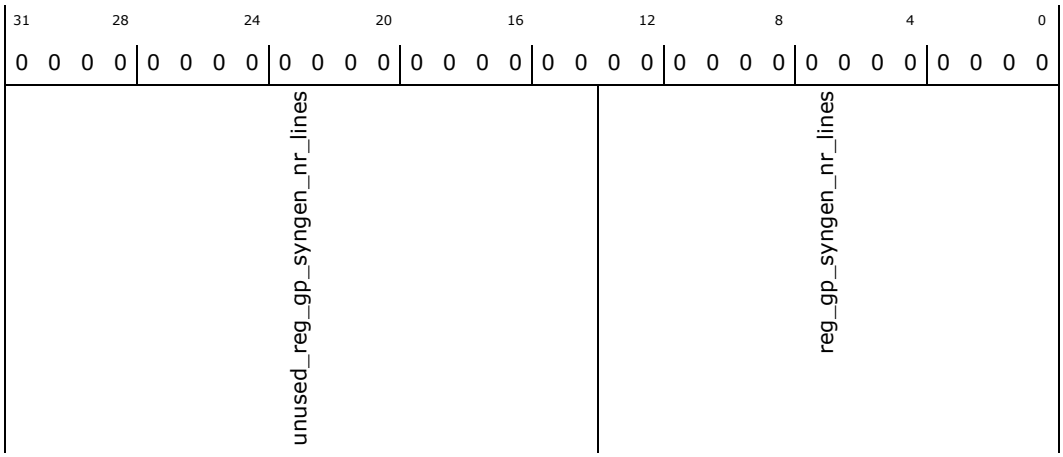
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RW	**Reserved (unused_reg_gp_syngen_nr_lines):** Unused
13:0	0x0 RW	**reg_gp_syngen_nr_lines:** Sets the number of lines per frame in the Sync generator

5.3.219 reg_gp_syngen_hblank_cycles (is_2400_isel_gpr_reg_gp_syngen_hblank_cycles)—Offset 90018h

Sets the number of cycles between the end-of-line and start-of-line pulses.

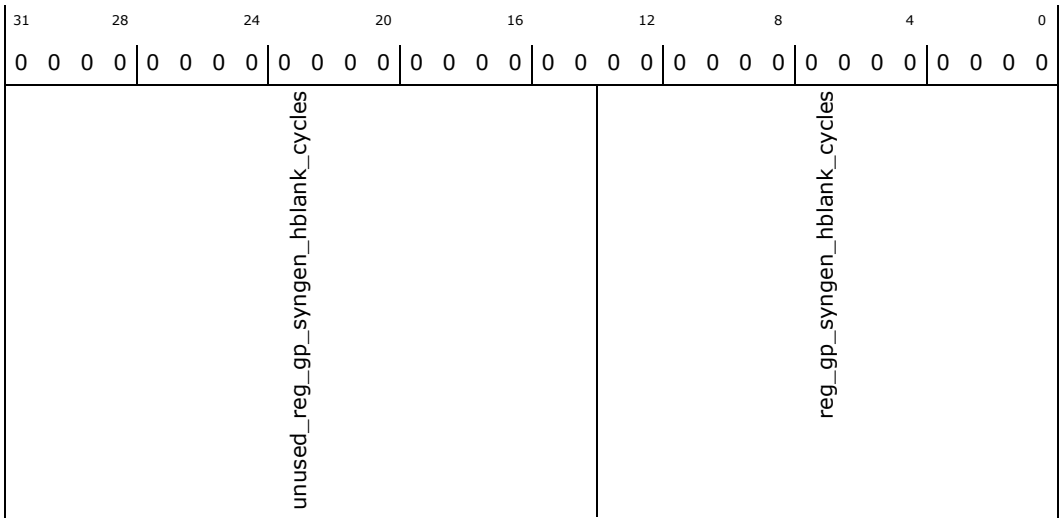
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RW	**Reserved (unused_reg_gp_syngen_hblank_cycles):** Unused
13:0	0x0 RW	**reg_gp_syngen_hblank_cycles:** Sets the number of cycles between the end-of-line and start-of-line pulses.

5.3.220 reg_gp_syngen_vblank_cycles (is_2400_isel_gpr_reg_gp_syngen_vblank_cycles)—Offset 9001Ch

Sets the number of cycles between the end-of-frame and start-of-frame pulses.

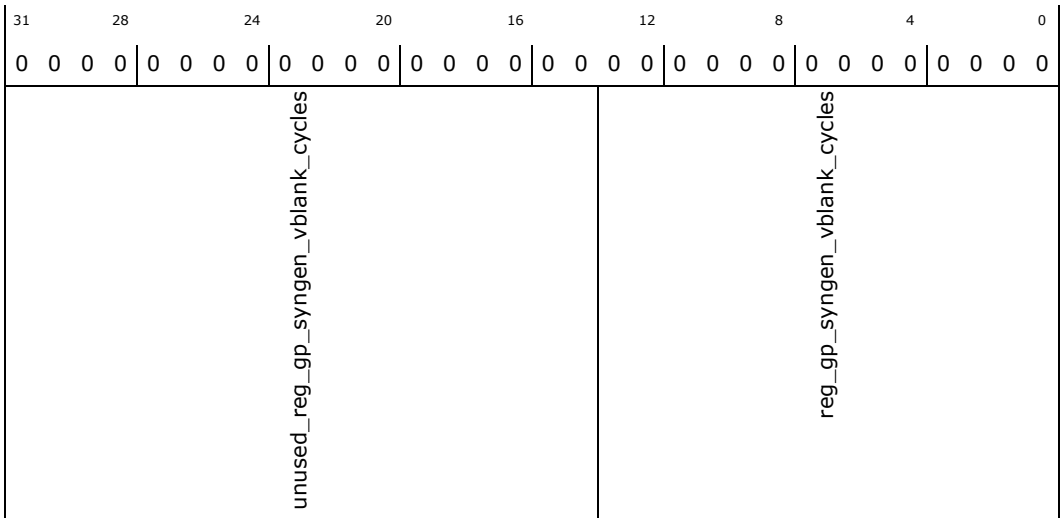
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 9001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RW	**Reserved (unused_reg_gp_syngen_vblank_cycles):** Unused
13:0	0x0 RW	**reg_gp_syngen_vblank_cycles:** Sets the number of cycles between the end-of-frame and start-of-frame pulses.

5.3.221 reg_gp_isel_sof (is_2400_isel_gpr_reg_gp_isel_sof)—Offset 90020h

Sets the input selector gp_sof input.

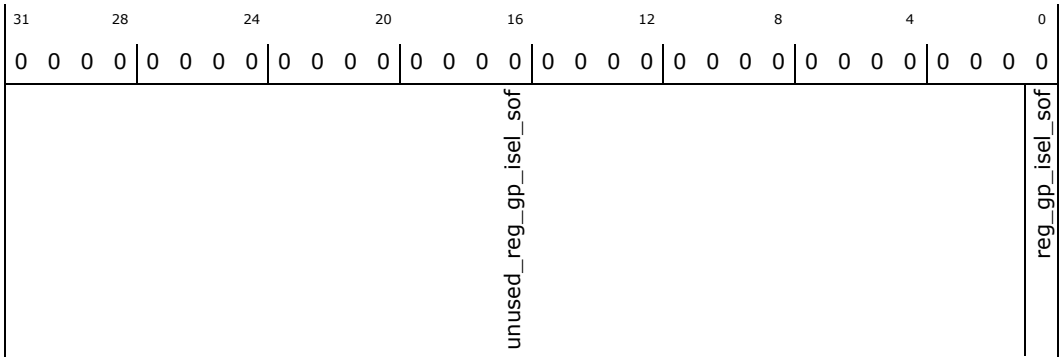
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90020h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_gp_isel_sof):** Unused
0	0x0 RW	**reg_gp_isel_sof:** Sets the input selector gp_sof input.

5.3.222 reg_gp_isel_eof (is_2400_isel_gpr_reg_gp_isel_eof)—Offset 90024h

Sets the input selector gp_eof input.

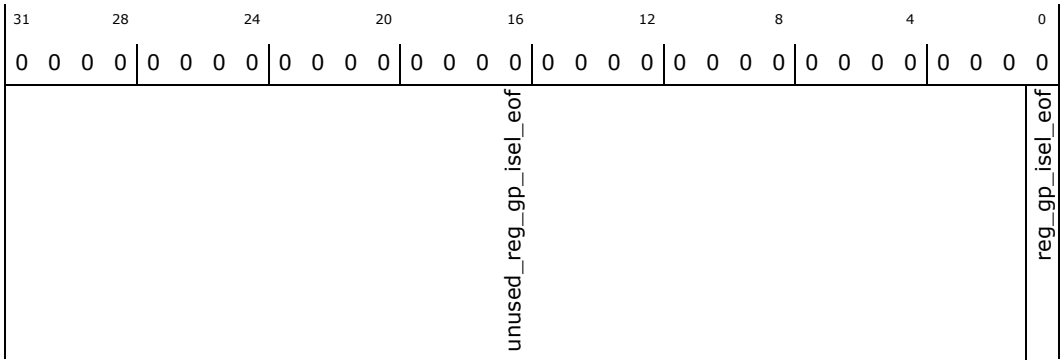
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90024h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_gp_isel_eof):** Unused
0	0x0 RW	**reg_gp_isel_eof:** Sets the input selector gp_eof input.

5.3.223 reg_gp_isel_sol (is_2400_isel_gpr_reg_gp_isel_sol)—Offset 90028h

Sets the input selector gp_sol input.

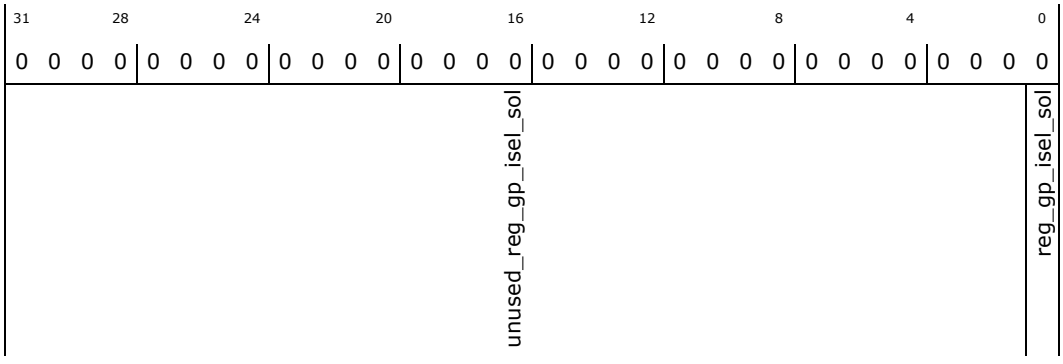
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90028h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_gp_isel_sol):** Unused

Bit Range	Default and Access	Field Name (ID): Description
0	0x0 RW	**reg_gp_isel_sol:** Sets the input selector gp_sol input.

5.3.224 reg_gp_isel_eol (is_2400_isel_gpr_reg_gp_isel_eol)—Offset 9002Ch

Sets the input selector gp_eol input.

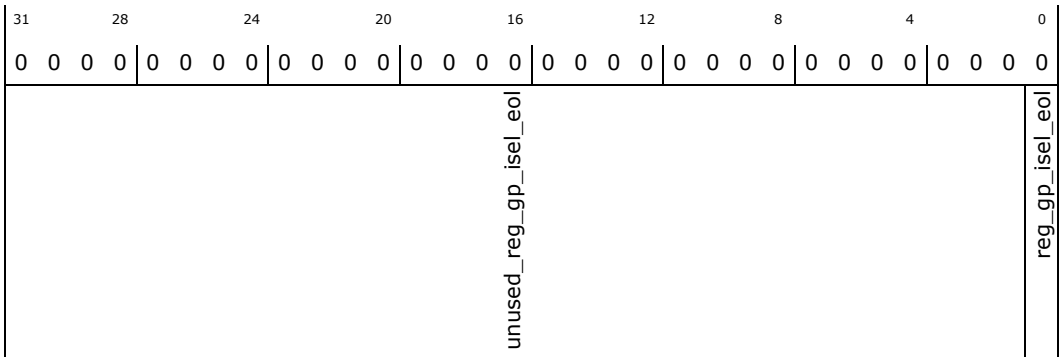
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 9002Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_gp_isel_eol):** Unused
0	0x0 RW	**reg_gp_isel_eol:** Sets the input selector gp_eol input.

5.3.225 reg_gp_isel_lfsr_enable (is_2400_isel_gpr_reg_gp_isel_lfsr_enable)—Offset 90030h

Enables the PRBS

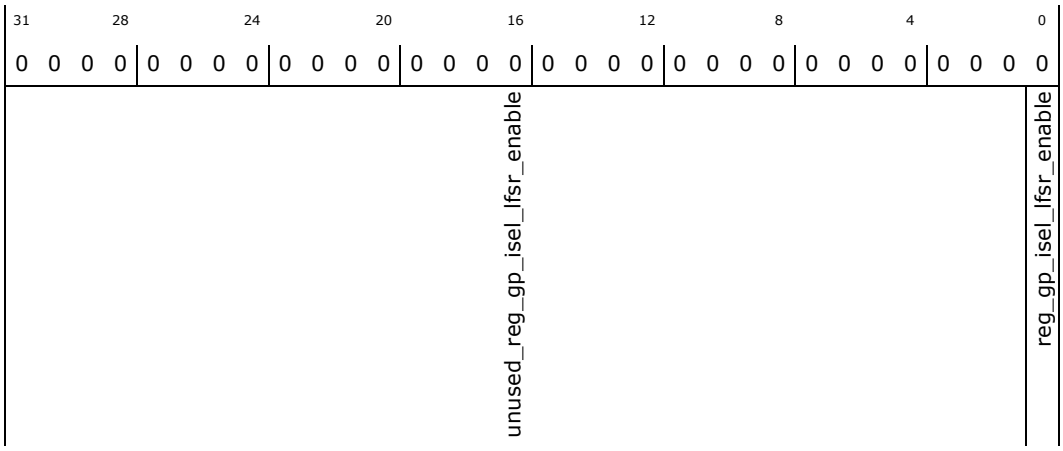
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90030h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_gp_isel_lfsr_enable):** Unused
0	0x0 RW	**reg_gp_isel_lfsr_enable:** Enables the PRBS

5.3.226 reg_gp_isel_lfsr_enable_b (is_2400_isel_gpr_reg_gp_isel_lfsr_enable_b)—Offset 90034h

Enables the PRBS for port b

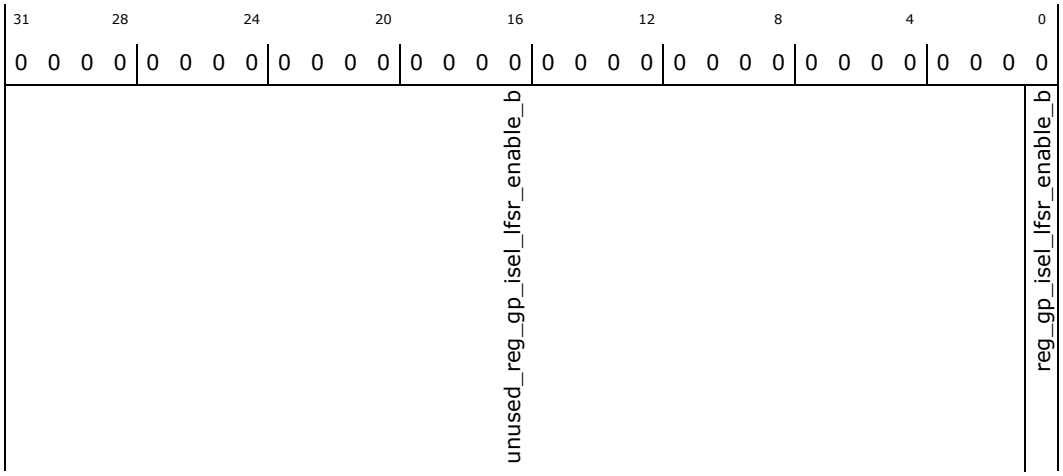
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90034h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_gp_isel_lfsr_enable_b):** Unused
0	0x0 RW	**reg_gp_isel_lfsr_enable_b:** Enables the PRBS for port b

5.3.227 reg_gp_isel_lfsr_reset_value (is_2400_isel_gpr_reg_gp_isel_lfsr_reset_value)—Offset 90038h

Set the reset value of the LFSR in the PRBS of the Input selector

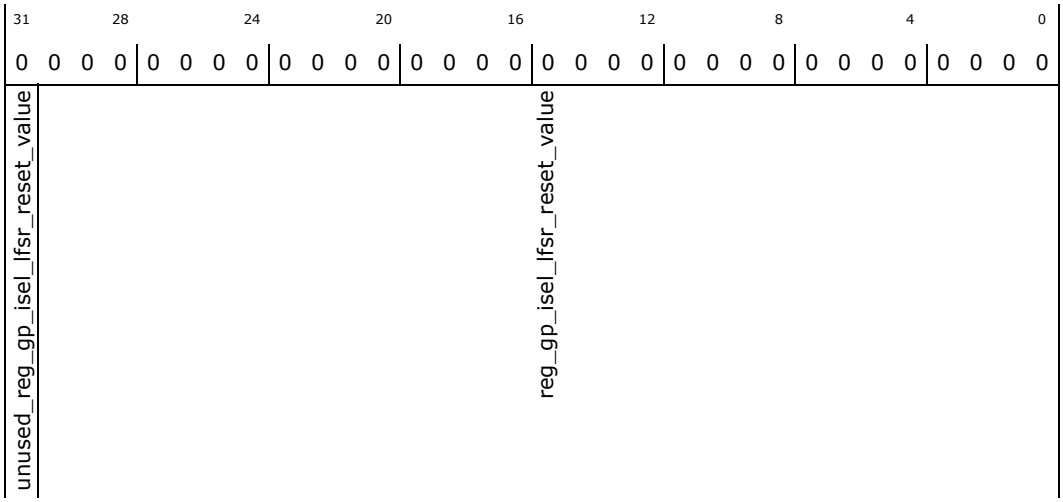
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90038h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**Reserved (unused_reg_gp_isel_lfsr_reset_value):** Unused
30:0	0x0 RW	**reg_gp_isel_lfsr_reset_value:** Set the reset value of the LFSR in the PRBS of the Input selector

5.3.228 reg_gp_isel_tpg_enable (is_2400_isel_gpr_reg_gp_isel_tpg_enable)—Offset 9003Ch

Enables the test pattern generator

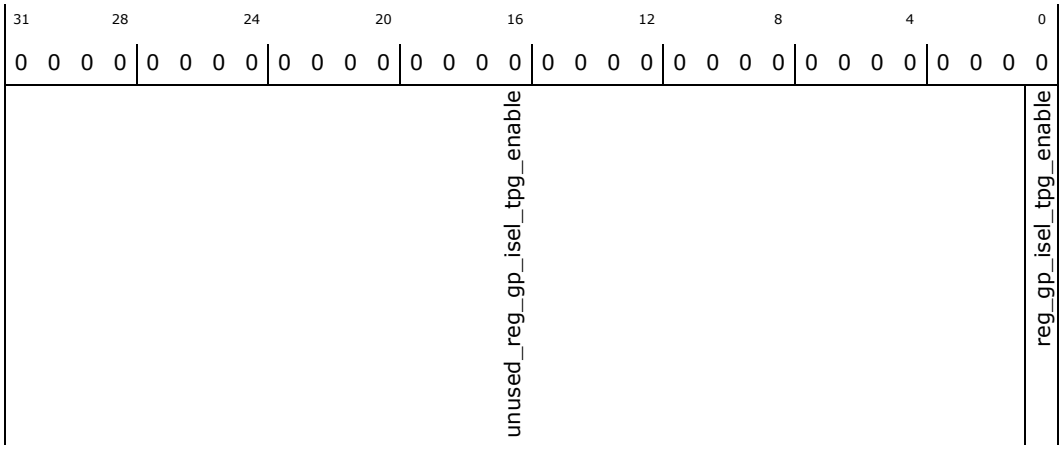
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 9003Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_gp_isel_tpg_enable):** Unused
0	0x0 RW	**reg_gp_isel_tpg_enable:** Enables the test pattern generator

5.3.229 reg_gp_isel_tpg_enable_b (is_2400_isel_gpr_reg_gp_isel_tpg_enable_b)—Offset 90040h

Enables the test pattern generator for port b

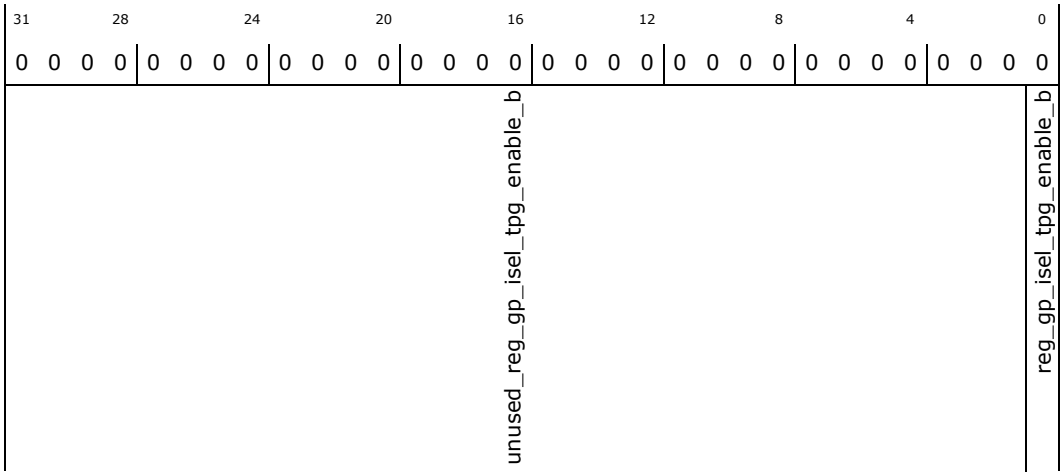
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90040h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_reg_gp_isel_tpg_enable_b):** Unused
0	0x0 RW	**reg_gp_isel_tpg_enable_b:** Enables the test pattern generator for port b

5.3.230 reg_gp_isel_hor_cnt_mask (is_2400_isel_gpr_reg_gp_isel_hor_cnt_mask)—Offset 90044h

Sets the Horizontal Counter Mask in the Input Selector

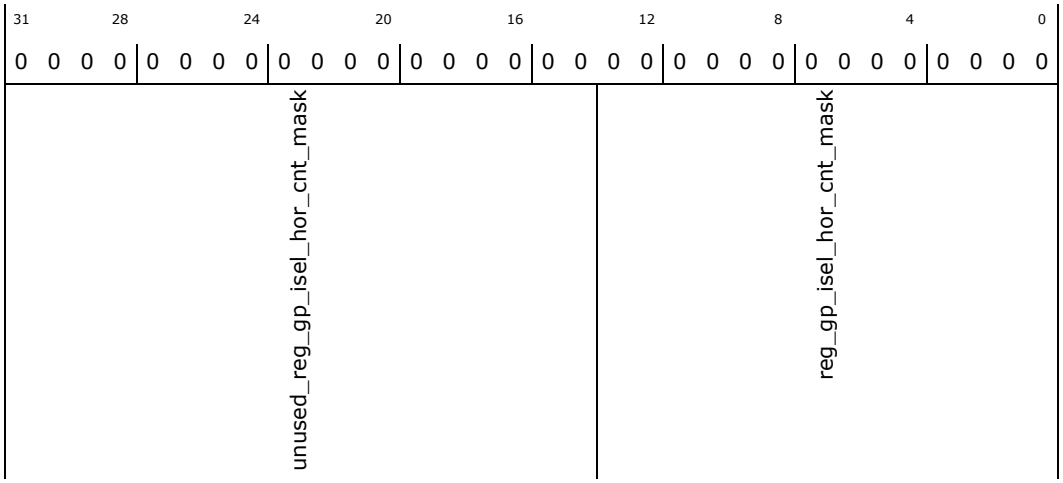
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90044h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RW	**Reserved (unused_reg_gp_isel_hor_cnt_mask):** Unused
13:0	0x0 RW	**reg_gp_isel_hor_cnt_mask:** Sets the horizontal counter mask in the Input selector

5.3.231 reg_gp_isel_ver_cnt_mask (is_2400_isel_gpr_reg_gp_isel_ver_cnt_mask)—Offset 90048h

Sets the vertical counter mask in the Input selector

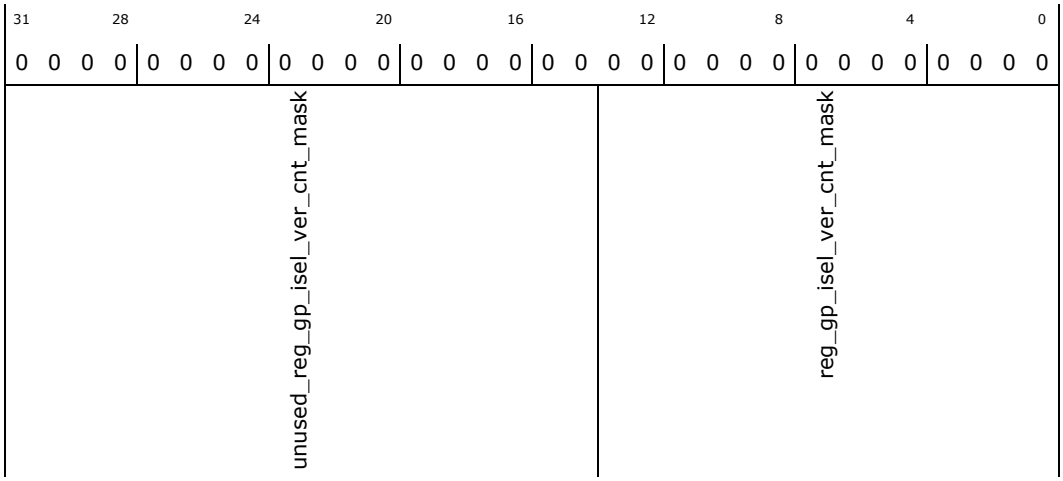
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90048h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RW	**Reserved (unused_reg_gp_isel_ver_cnt_mask):** Unused
13:0	0x0 RW	**reg_gp_isel_ver_cnt_mask:** Sets the vertical counter mask in the Input selector

5.3.232 reg_gp_isel_xy_cnt_mask (is_2400_isel_gpr_reg_gp_isel_xy_cnt_mask)—Offset 9004Ch

Sets the XY Counter Mask in the Input Selector

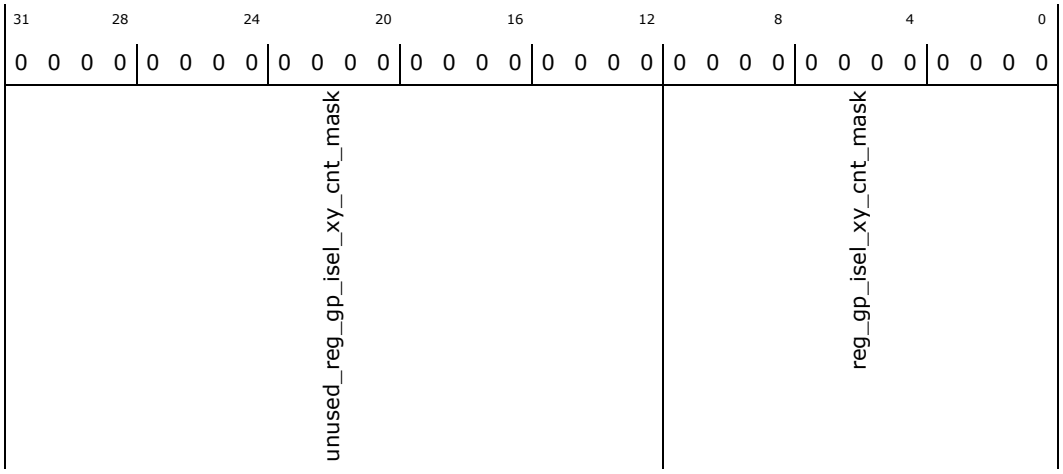
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 9004Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_reg_gp_isel_xy_cnt_mask):** Unused
11:0	0x0 RW	**reg_gp_isel_xy_cnt_mask:** Sets the xy counter mask in the Input selector

5.3.233 reg_gp_isel_hor_cnt_delta (is_2400_isel_gpr_reg_gp_isel_hor_cnt_delta)—Offset 90050h

sets the horizontal counter delta in the Input selector

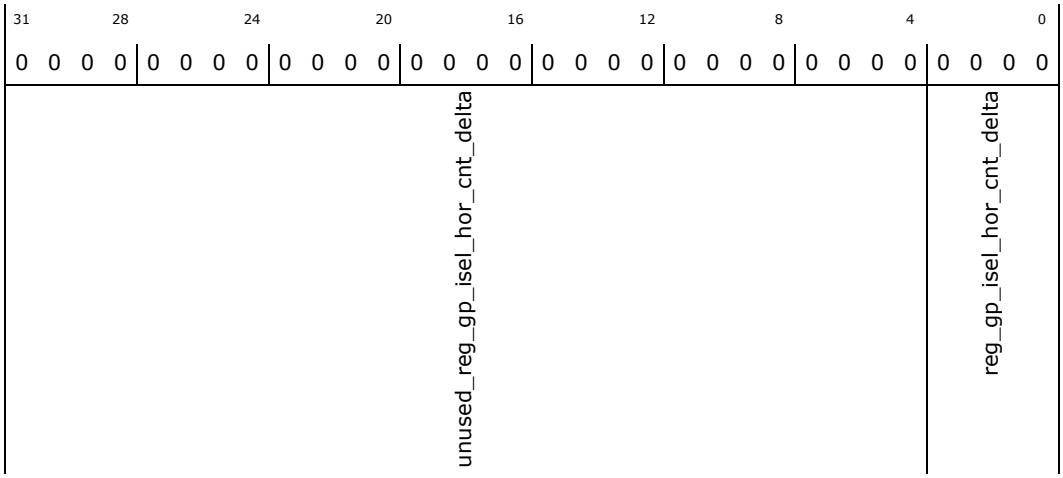
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90050h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RW	**Reserved (unused_reg_gp_isel_hor_cnt_delta):** Unused
3:0	0x0 RW	**reg_gp_isel_hor_cnt_delta:** sets the horizontal counter delta in the Input selector

5.3.234 reg_gp_isel_ver_cnt_delta (is_2400_isel_gpr_reg_gp_isel_ver_cnt_delta)—Offset 90054h

Sets the vertical counter delta in the Input selector

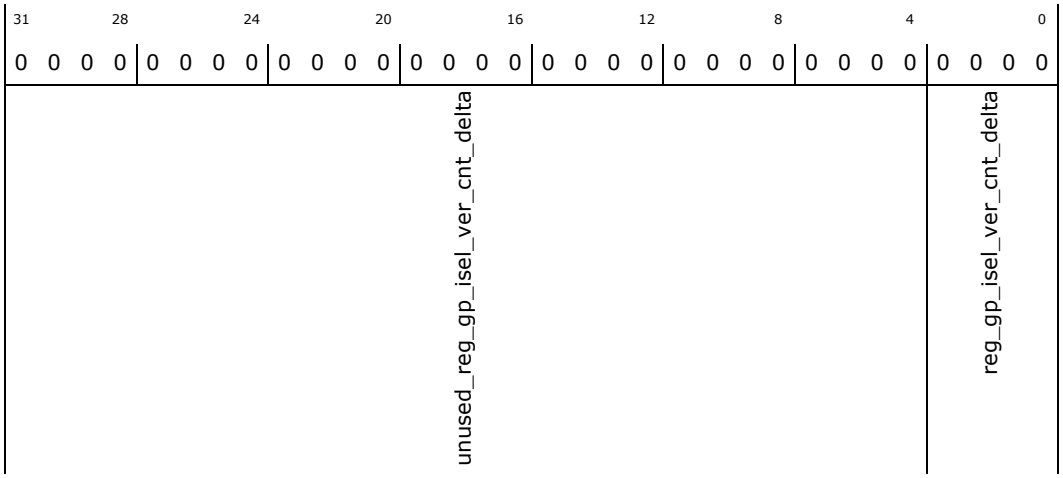
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90054h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RW	**Reserved (unused_reg_gp_isel_ver_cnt_delta):** Unused
3:0	0x0 RW	**reg_gp_isel_ver_cnt_delta:** Sets the vertical counter delta in the Input selector

5.3.235 reg_gp_isel_tpg_mode (is_2400_isel_gpr_reg_gp_isel_tpg_mode)—Offset 90058h

Sets the mode of the test pattern generator. 'b00-ramp mode, 'b01-checkerboard, 'b10-frame based color

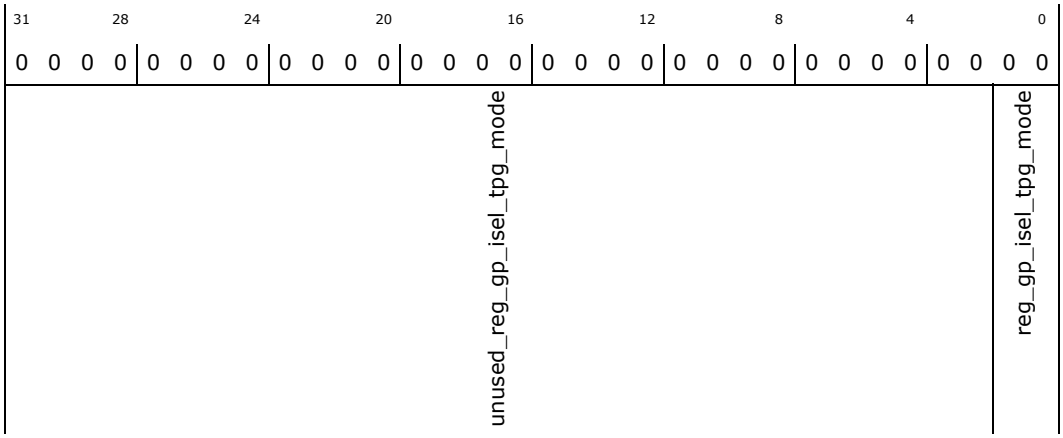
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90058h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_reg_gp_isel_tpg_mode):** Unused
1:0	0x0 RW	**reg_gp_isel_tpg_mode:** Sets the mode of the test pattern generator. 'b00-ramp mode, 'b01-checkerboard, 'b10-frame based color

5.3.236 reg_gp_isel_tpg_red1 (is_2400_isel_gpr_reg_gp_isel_tpg_red1)—Offset 9005Ch

Defines the red1 color for test pattern generator

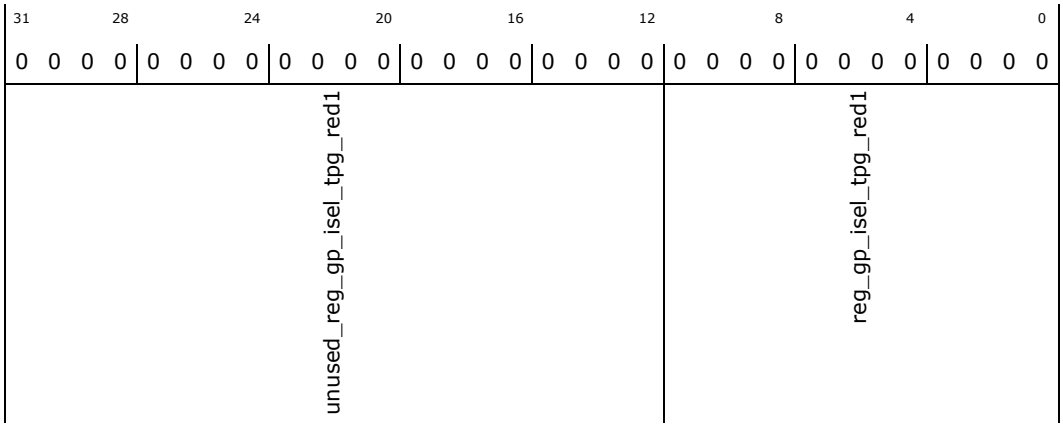
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 9005Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_reg_gp_isel_tpg_red1):** Unused
11:0	0x0 RW	**reg_gp_isel_tpg_red1:** Defines the red1 color for test pattern generator

5.3.237 reg_gp_isel_tpg_green1 (is_2400_isel_gpr_reg_gp_isel_tpg_green1)—Offset 90060h

Defines the green1 color for test pattern generator

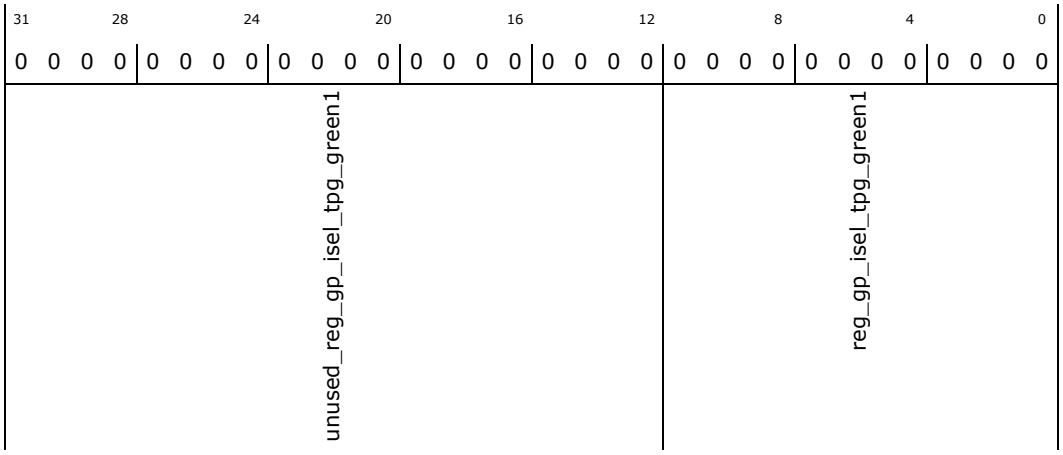
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90060h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_reg_gp_isel_tpg_green1):** Unused
11:0	0x0 RW	**reg_gp_isel_tpg_green1:** Defines the green1 color for test pattern generator

5.3.238 reg_gp_isel_tpg_blue1 (is_2400_isel_gpr_reg_gp_isel_tpg_blue1)—Offset 90064h

Defines the blue1 color for test pattern generator

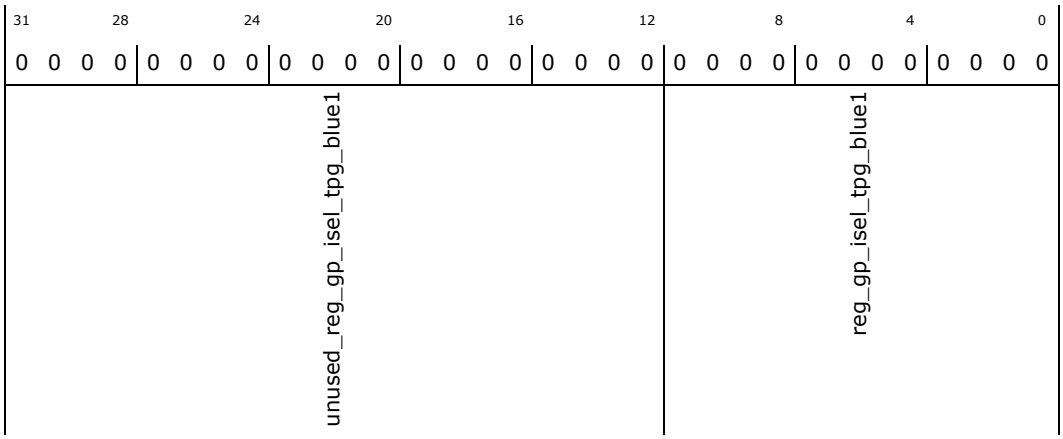
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90064h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_reg_gp_isel_tpg_blue1):** Unused
11:0	0x0 RW	**reg_gp_isel_tpg_blue1:** Defines the blue1 color for test pattern generator

5.3.239 reg_gp_isel_tpg_red2 (is_2400_isel_gpr_reg_gp_isel_tpg_red2)—Offset 90068h

Defines the red2 color for test pattern generator

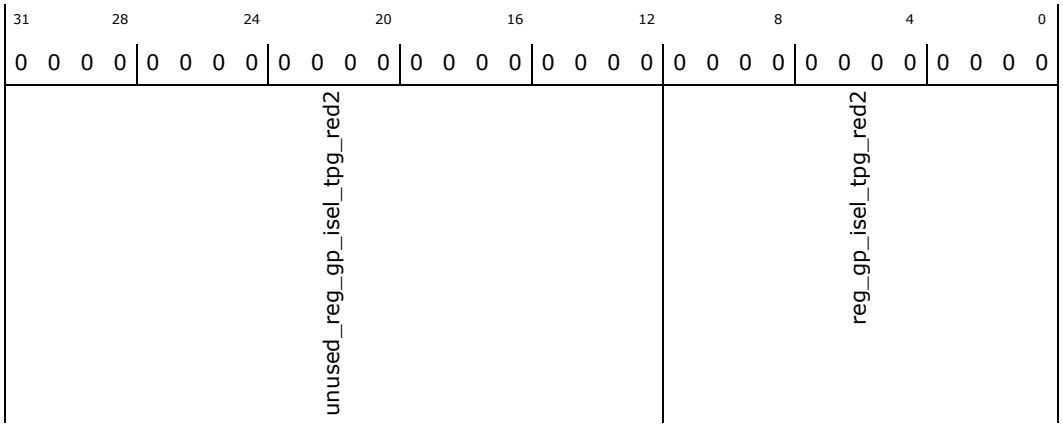
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90068h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_reg_gp_isel_tpg_red2):** Unused
11:0	0x0 RW	**reg_gp_isel_tpg_red2:** Defines the red2 color for test pattern generator

5.3.240 reg_gp_isel_tpg_green2 (is_2400_isel_gpr_reg_gp_isel_tpg_green2)—Offset 9006Ch

Defines the green2 color for test pattern generator

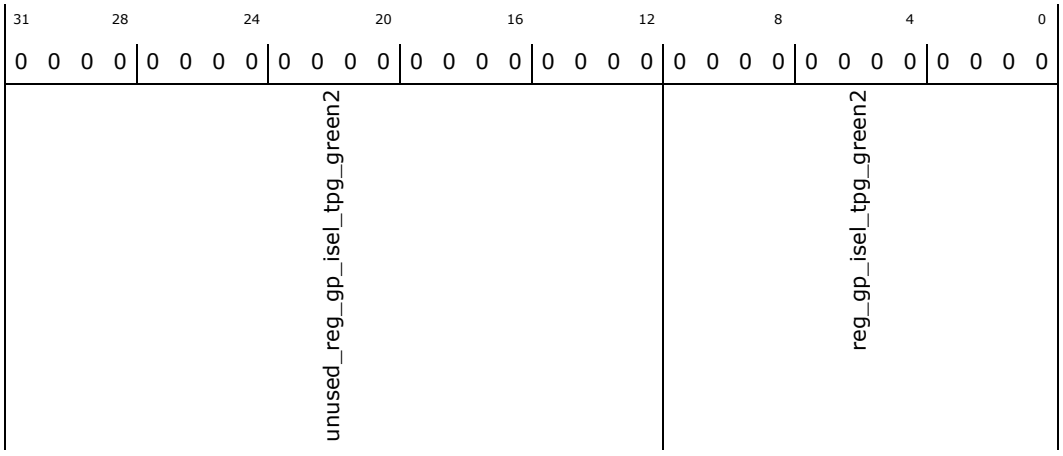
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 9006Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_reg_gp_isel_tpg_green2):** Unused
11:0	0x0 RW	**reg_gp_isel_tpg_green2:** Defines the green2 color for test pattern generator

5.3.241 reg_gp_isel_tpg_blue2 (is_2400_isel_gpr_reg_gp_isel_tpg_blue2)—Offset 90070h

Defines the blue2 color for test pattern generator

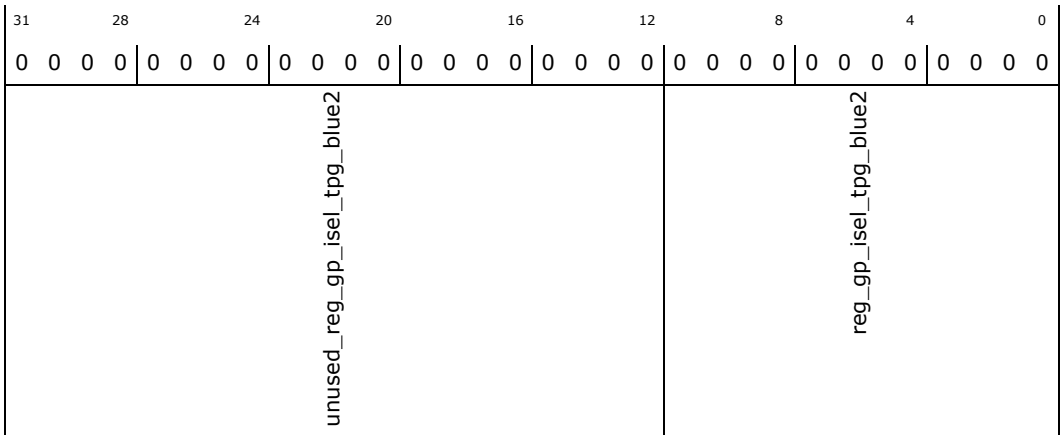
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90070h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved (unused_reg_gp_isel_tpg_blue2):** Unused
11:0	0x0 RW	**reg_gp_isel_tpg_blue2:** Defines the blue2 color for test pattern generator

5.3.242 reg_gp_isel_ch_id (is_2400_isel_gpr_reg_gp_isel_ch_id)—Offset 90074h

Sets the channel id input for the Input selector

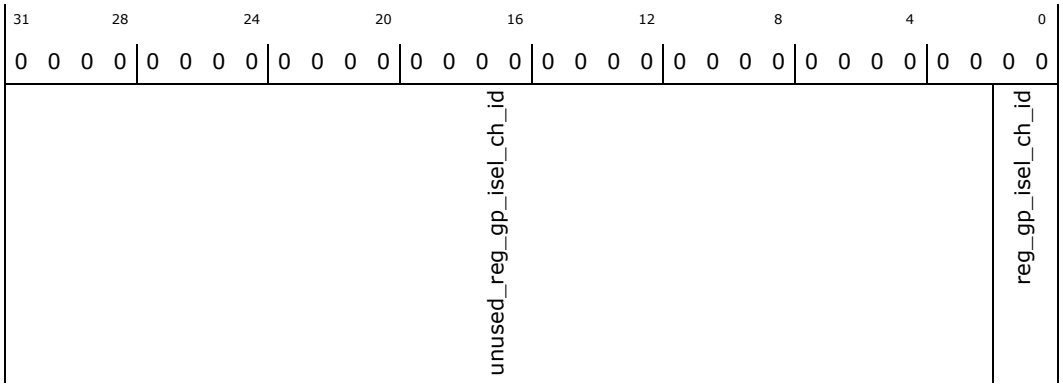
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90074h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_reg_gp_isel_ch_id):** Unused
1:0	0x0 RW	**reg_gp_isel_ch_id:** Sets the channel id input for the Input selector

5.3.243 reg_gp_isel_fmt_type (is_2400_isel_gpr_reg_gp_isel_fmt_type)—Offset 90078h

Sets the format type input for the Input selector

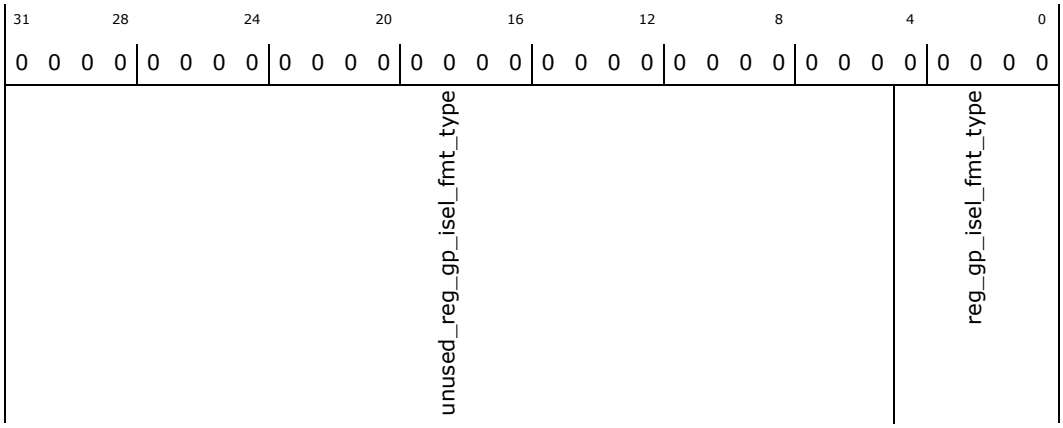
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90078h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:5	0x0 RW	**Reserved (unused_reg_gp_isel_fmt_type):** Unused
4:0	0x0 RW	**reg_gp_isel_fmt_type:** Sets the format type input for the Input selector

5.3.244 reg_gp_isel_data_sel (is_2400_isel_gpr_reg_gp_isel_data_sel)—Offset 9007Ch

Select value for the data multiplexer in the Input selector

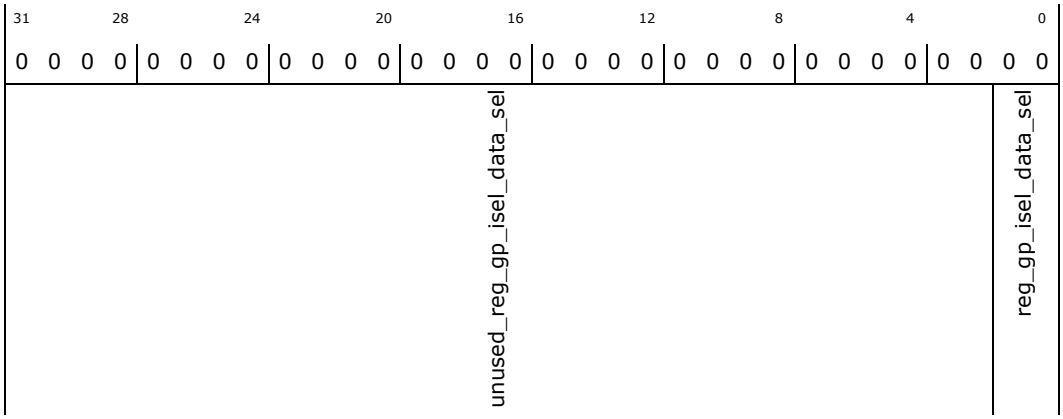
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 9007Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_reg_gp_isel_data_sel):** Unused
1:0	0x0 RW	**reg_gp_isel_data_sel:** Select value for the data multiplexer in the Input selector

5.3.245 reg_gp_isel_sband_sel (is_2400_isel_gpr_reg_gp_isel_sband_sel)—Offset 90080h

Select value for the side band multiplexer in the Input selector

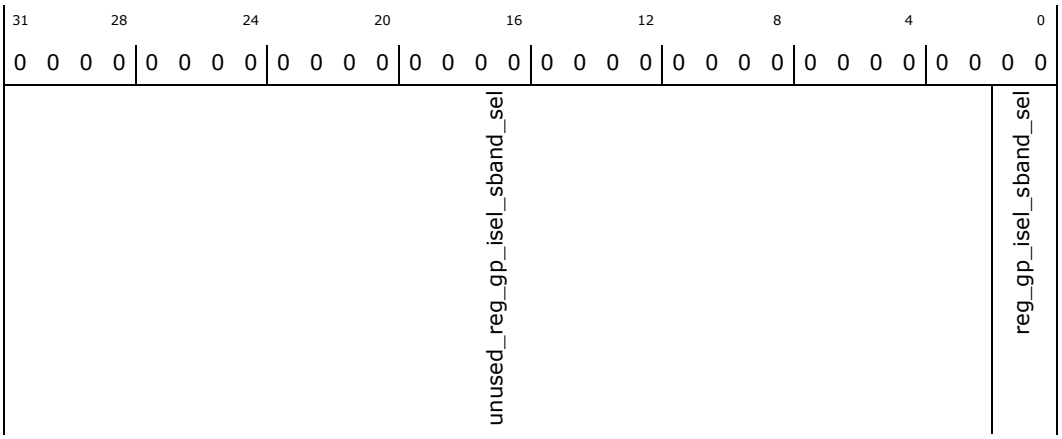
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90080h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_reg_gp_isel_sband_sel):** Unused
1:0	0x0 RW	**reg_gp_isel_sband_sel:** Select value for the side band multiplexer in the Input selector

5.3.246 reg_gp_isel_sync_sel (is_2400_isel_gpr_reg_gp_isel_sync_sel)—Offset 90084h

Select value for the sync multiplexer in the Input selector

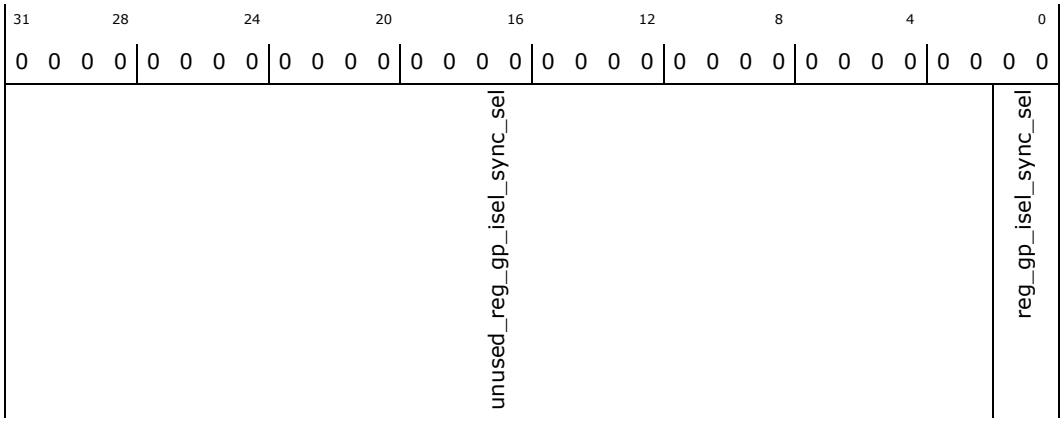
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90084h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (unused_reg_gp_isel_sync_sel):** Unused
1:0	0x0 RW	**reg_gp_isel_sync_sel:** Select value for the sync multiplexer in the Input selector

5.3.247 reg_gp_syncgen_hor_cnt (is_2400_isel_gpr_reg_gp_syncgen_hor_cnt)—Offset 90088h

Returns the value of the horizontal counter in the sync generator

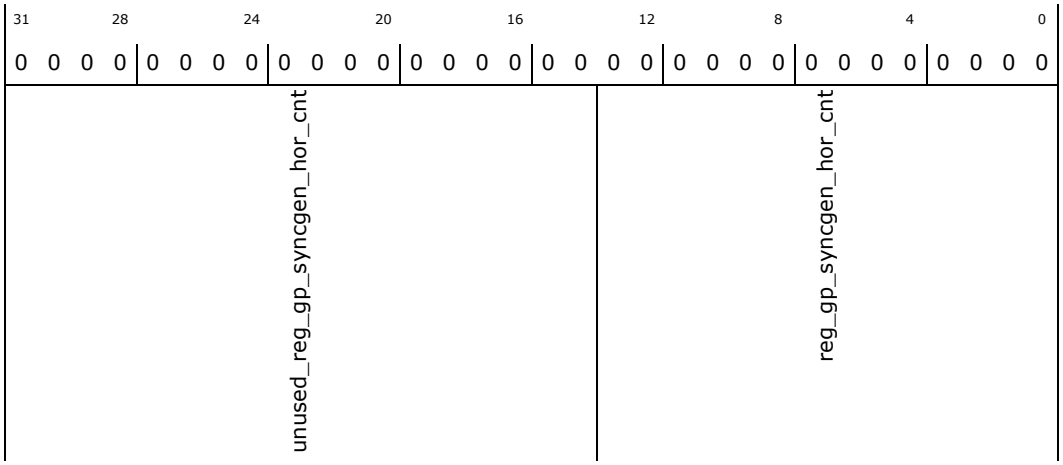
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90088h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RW	**Reserved (unused_reg_gp_syncgen_hor_cnt):** Unused
13:0	0x0 RO	**reg_gp_syncgen_hor_cnt:** Returns the value of the horizontal counter in the sync generator

5.3.248 reg_gp_syncgen_ver_cnt (is_2400_isel_gpr_reg_gp_syncgen_ver_cnt)—Offset 9008Ch

Returns the value of the vertical counter in the sync generator

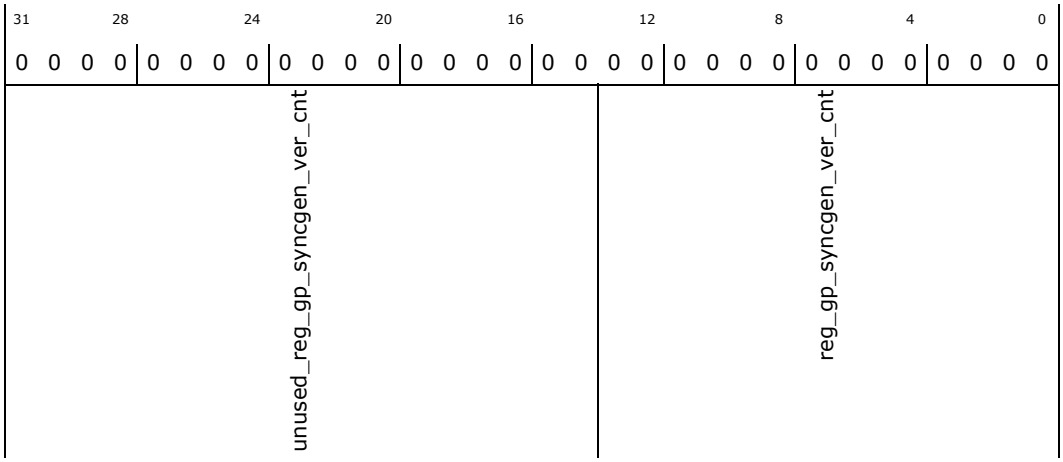
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 9008Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RW	**Reserved (unused_reg_gp_syncgen_ver_cnt):** Unused
13:0	0x0 RO	**reg_gp_syncgen_ver_cnt:** Returns the value of the vertical counter in the sync generator

5.3.249 reg_gp_syncgen_frame_cnt (is_2400_isel_gpr_reg_gp_syncgen_frame_cnt)—Offset 90090h

Returns the value of the frame counter in the sync generator

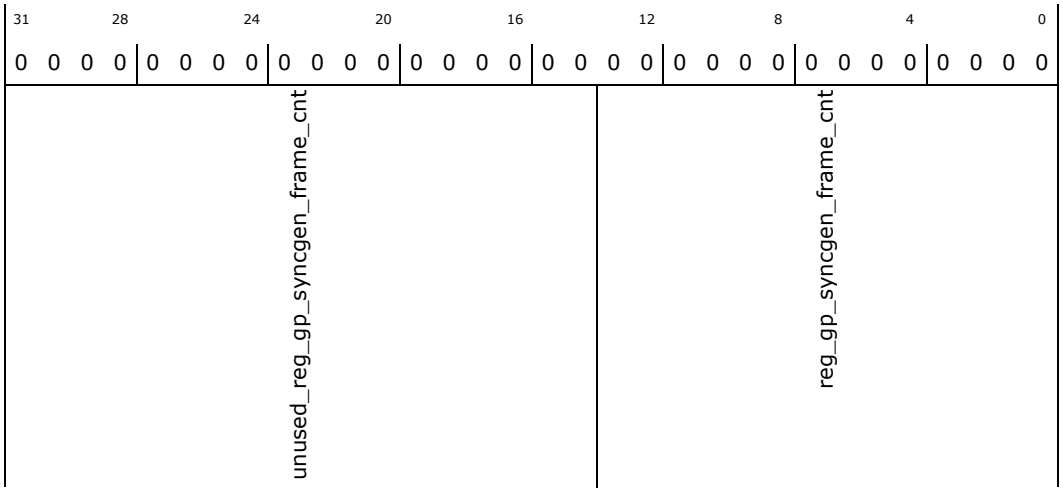
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90090h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RW	**Reserved (unused_reg_gp_syncgen_frame_cnt):** Unused
13:0	0x0 RO	**reg_gp_syncgen_frame_cnt:** Returns the value of the frame counter in the sync generator

5.3.250 reg_gp_soft_reset (is_2400_isel_gpr_reg_gp_soft_reset)—Offset 90094h

Soft resets the modules in the input selector cluster

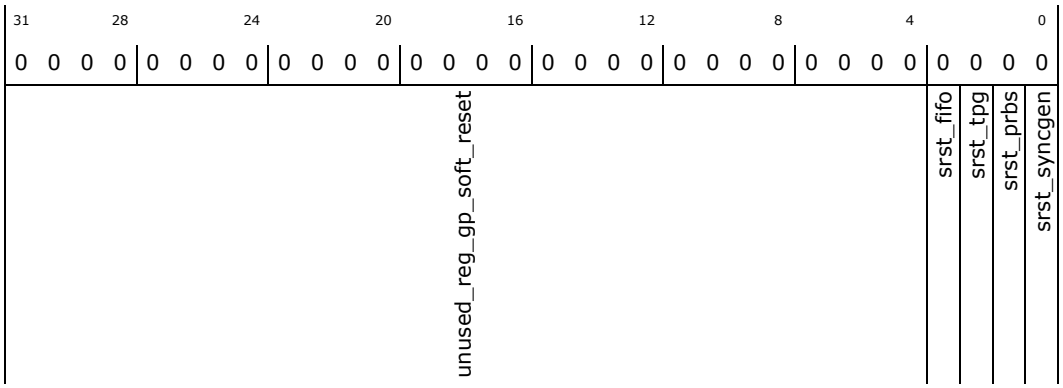
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90094h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_reg_gp_soft_reset):** Unused
3	0x0 RW	**srst_fifo:** If 1, the FIFO is held in reset mode. If 0, the FIFO is not in reset state.
2	0x0 RW	**srst_tpg:** If 1, the TPG is held in reset mode. If 0, the TPG is not in reset state.
1	0x0 RW	**srst_prbs:** If 1, the PRBS is held in reset mode. If 0, the PRBS is not in reset state.
0	0x0 RW	**srst_syncgen:** If 1, the sync generator is held in reset mode. If 0, the sync generator is not in reset state.

5.3.251 send_to_GP_FIFO (is_2400_isel_fa_send_to_GP_FIFO)—Offset 90104h

Send data to input selector GP FIFO

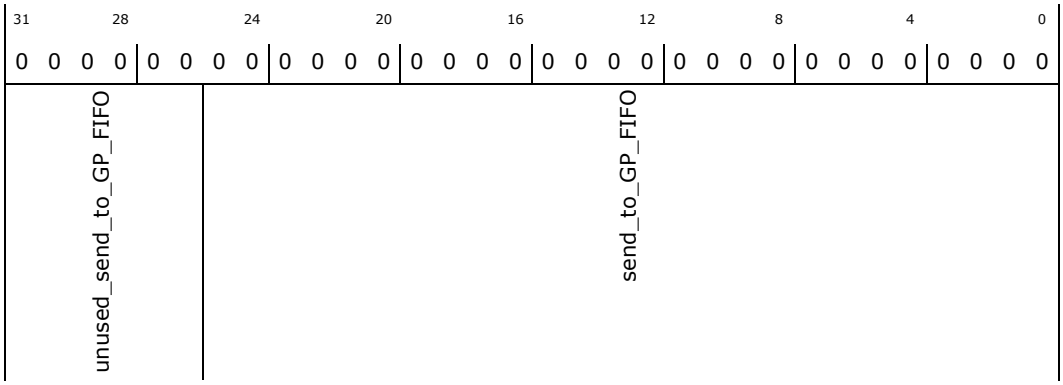
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90104h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:26	0x0 RW	**Reserved (unused_send_to_GP_FIFO):** Unused
25:0	0x0 WO	**send_to_GP_FIFO:** Send data to input selector GP FIFO

5.3.252 check_send_to_GP_FIFO (is_2400_isel_fa_check_send_to_GP_FIFO)—Offset 9010Ch

Check for availability of GP FIFO. Returns 1 if a word can be send to the input selector, without it being stalled

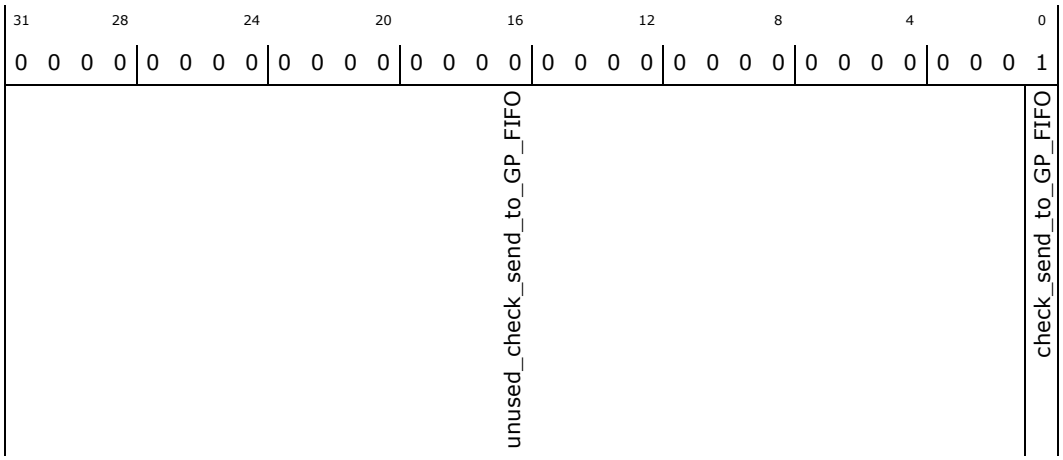
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 9010Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_check_send_to_GP_FIFO):** Unused
0	0x1 WO	**check_send_to_GP_FIFO:** Check for availability of GP FIFO. Returns 1 if a word can be send to the input selector, without it being stalled

5.3.253 reg_irq_edge (is_2400_isel_irq_ctrl_reg_irq_edge)—Offset 90200h

indicates for each bit whether an interrupt request should be generated on a falling edge (value='0') or a rising edge (value='1').

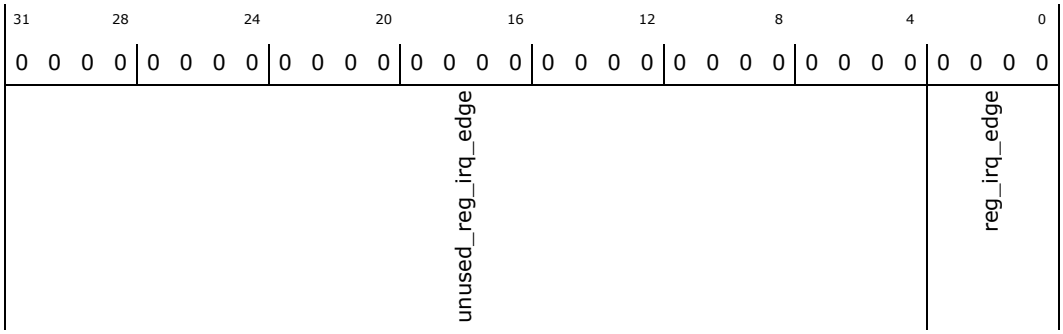
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90200h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RW	**Reserved (unused_reg_irq_edge):** Unused
3:0	0x0 RW	**reg_irq_edge:** indicates for each bit whether an interrupt request should be generated on a falling edge (value='0') or a rising edge (value='1').

5.3.254 reg_irq_mask (is_2400_isel_irq_ctrl_reg_irq_mask)—Offset 90204h

indicates for each bit of irq_di whether it can generate an interrupt request (value='1') or not (value='0'). Setting will affect reg_irq_value as well as IRQ output pin

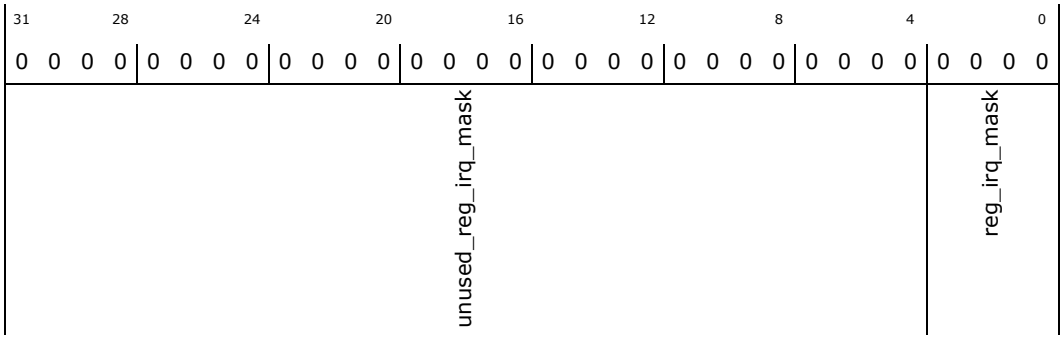
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90204h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RW	**Reserved (unused_reg_irq_mask):** Unused

Bit Range	Default and Access	Field Name (ID): Description
3:0	0x0 RW	**reg_irq_mask:** indicates for each bit of irq_di whether it can generate an interrupt request (value='1') or not (value='0'). Setting will affect reg_irq_value as well as IRQ output pin

5.3.255 reg_irq_status (is_2400_isel_irq_ctrl_reg_irq_status)—Offset 90208h

Indicates for each bit whether a non-masked interrupt has been generated (value='1'). Can be cleared by writing a '1' into the corresponding bit of the req_irq_clear register.

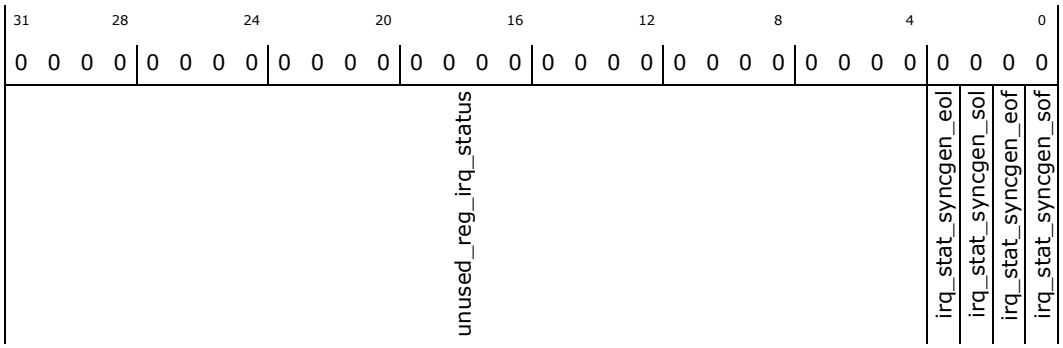
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90208h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved (unused_reg_irq_status):** Unused
3	0x0 RO	**irq_stat_syncgen_eol:** Represents the IRQ status of the EoL (End of Line) bit generated by the sync generator
2	0x0 RO	**irq_stat_syncgen_sol:** Represents the IRQ status of the SoL (Start of Line) bit generated by the sync generator
1	0x0 RO	**irq_stat_syncgen_eof:** Represents the IRQ status of the eof (end of frame) bit generated by the sync generator
0	0x0 RO	**irq_stat_syncgen_sof:** Represents the IRQ status of the sof (start of frame) bit generated by the sync generator

5.3.256 reg_irq_clear (is_2400_isel_irq_ctrl_reg_irq_clear)—Offset 9020Ch

Clears (set to '0') bits in reg_irq_status. When writing a '1' into a bit of this register, the corresponding bit in the req_irq_status is cleared. When writing a '0' into a bit of this register, the corresponding bit in the req_irq_status is not affected.

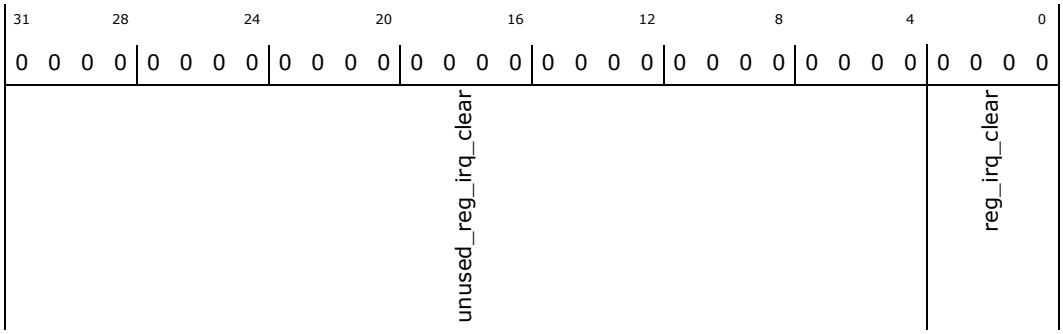
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 9020Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RW	**Reserved (unused_reg_irq_clear):** Unused
3:0	0x0 WO	**reg_irq_clear:** Clears (set to '0') bits in reg_irq_status. When writing a '1' into a bit of this register, the corresponding bit in the req_irq_status is cleared. When writing a '0' into a bit of this register, the corresponding bit in the req_irq_status is not affected.

5.3.257 reg_irq_enable (is_2400_isel_irq_ctrl_reg_irq_enable)—Offset 90210h

Indicates for each bit whether an interrupt cause as monitored by the req_irq_status register also affects the IRQ pin (value='1') or not (value='0')

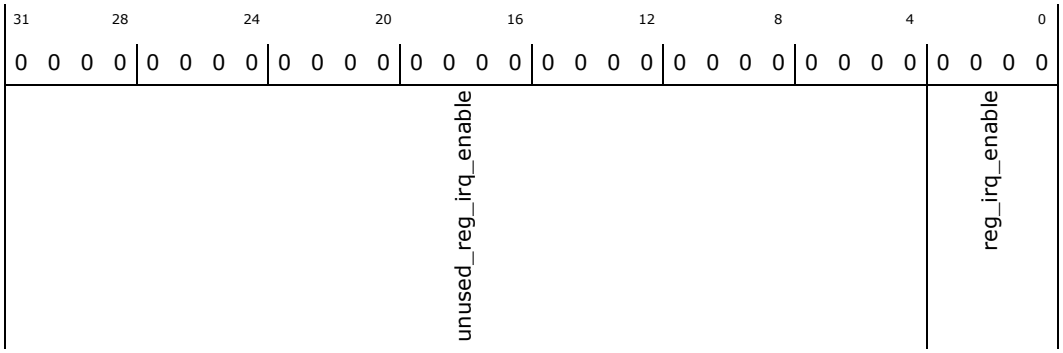
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90210h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RW	**Reserved (unused_reg_irq_enable):** Unused
3:0	0x0 RW	**reg_irq_enable:** Indicates for each bit whether an interrupt cause as monitored by the req_irq_status register also affects the IRQ pin (value='1') or not (value='0')

5.3.258 reg_irq_level_not_pulse (is_2400_isel_irq_ctrl_reg_irq_level_not_pulse)—Offset 90214h

Indicates for each bit whether an interrupt cause is translated into a pulse (value='0') or into a constant level '1' (value='1') on the IRQ pin

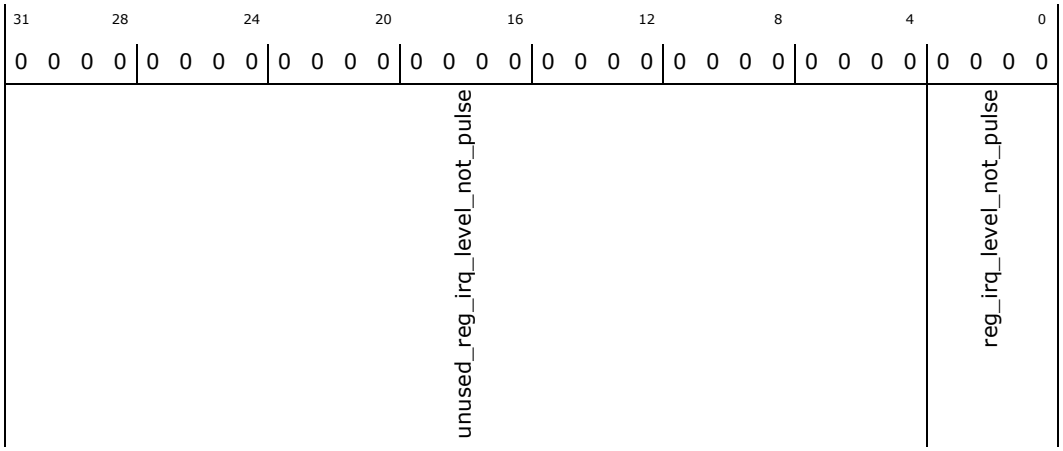
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 90214h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RW	**Reserved (unused_reg_irq_level_not_pulse):** Unused
3:0	0x0 RW	**reg_irq_level_not_pulse:** Indicates for each bit whether an interrupt cause is translated into a pulse (value='0') or into a constant level '1' (value='1') on the IRQ pin

5.3.259 MMU_invalidate_cache (icache_out_sys_c_mmu_MMU_invalidate_cache)—Offset A0000h

MMU invalidate cache. When '1', the MMUs TLB is invalidated.

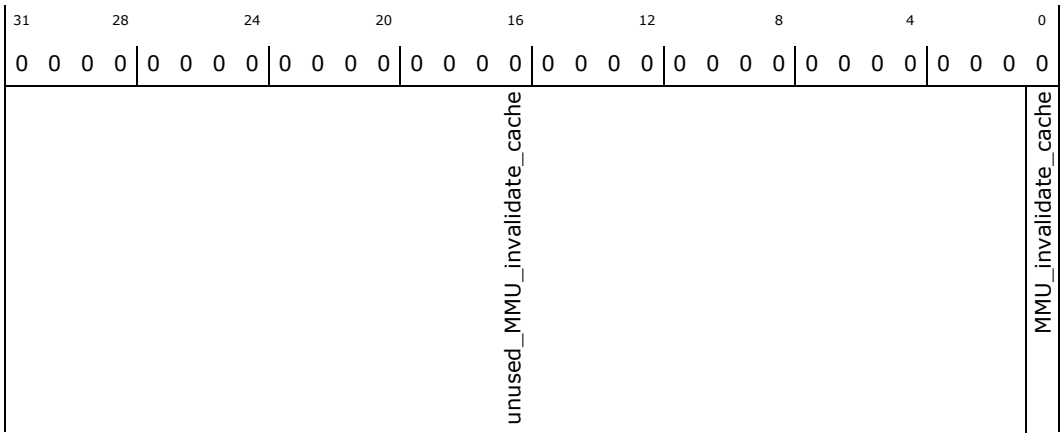
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + A0000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_MMU_invalidate_cache):** Unused
0	0x0 WO	**MMU_invalidate_cache:** MMU invalidate cache. When '1', the MMUs TLB is invalidated.

5.3.260 MMU_page_table_base (icache_out_sys_c_mmu_MMU_page_table_base)—Offset A0004h

Defines the physical page number of the page tables

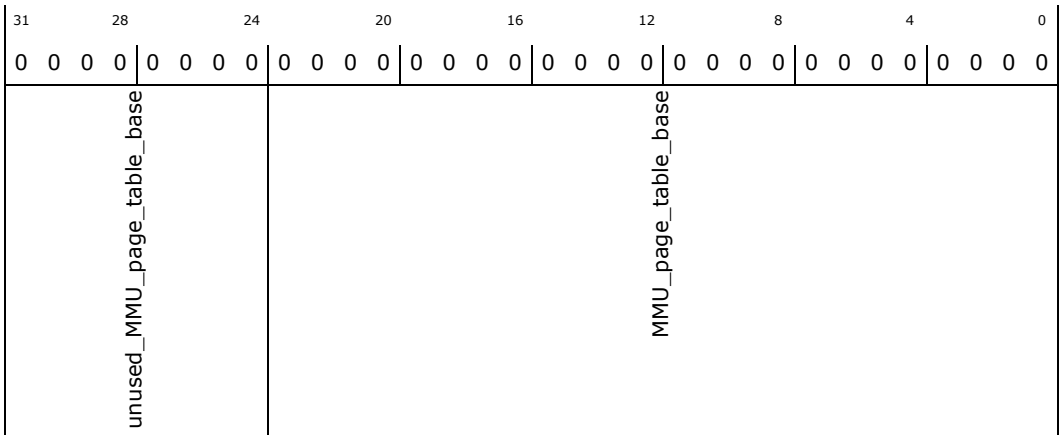
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + A0004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved (unused_MMU_page_table_base):** Unused
23:0	0x0 RW	**MMU_page_table_base:** Defines the physical page number of the page tables

5.3.261 mem_scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_first_type (scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_first)—Offset B0000h

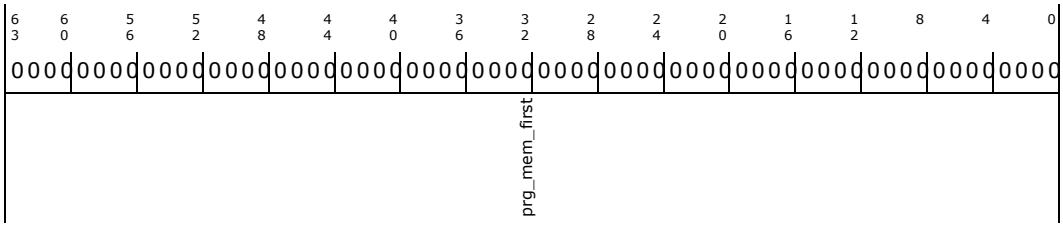
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [ISPMMADR] + B0000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default and Access	Field Name (ID): Description
63:0	0x0 RW	**prg_mem_first:** Read Latency of 1 cycles. Write latency of 0 cycles

5.3.262 mem_scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_last_type (scp_config_ilm_conf_ilm_prg_mem_sl_ip_pmem_prg_mem_last)—Offset B7FF8h

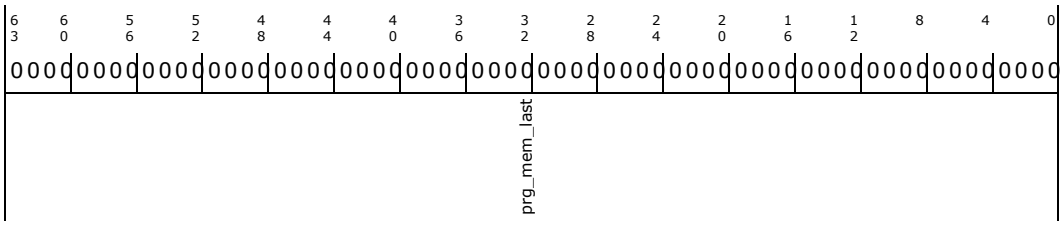
Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [ISPMMADR] + B7FF8h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000000000000000h



Bit Range	Default and Access	Field Name (ID): Description
63:0	0x0 RW	**prg_mem_last:** Read Latency of 1 cycles. Write latency of 0 cycles

5.4 Image Signal Processor Memory Mapped I/O Registers

Table 29. Summary of Memory Mapped I/O Registers—ISPMMADR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1C0000–1C0001h	2	"mem_isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_first_type (isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_first)—Offset 1C0000h" on page 1853	0000h
1C0FFE–1C0FFFh	2	"mem_isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_last_type (isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_last)—Offset 1C0FFEh" on page 1853	0000h
1D0000–1D0001h	2	"mem_isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_first_type (isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_first)—Offset 1D0000h" on page 1854	0000h
1D0FFE–1D0FFFh	2	"mem_isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_last_type (isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_last)—Offset 1D0FFEh" on page 1854	0000h
1E0000–1E0001h	2	"mem_isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_first_type (isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_first)—Offset 1E0000h" on page 1855	0000h

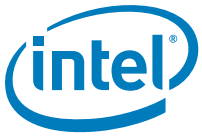


Table 29. Summary of Memory Mapped I/O Registers—ISPMMADR (Continued)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1E0FFE–1E0FFFh	2	"mem_isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_last_type (isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_last)—Offset 1E0FFEh" on page 1855	0000h
1F0000–1F0003h	4	"mem_isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_first_type (isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_first)—Offset 1F0000h" on page 1856	00000000h
1F0FFC–1F0FFFh	4	"mem_isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_last_type (isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_last)—Offset 1F0FFCh" on page 1857	00000000h
200000–200003h	4	"mem_isp_base_dmem_data_mem_sl_ipdmem_data_mem_first_type (isp_base_dmem_data_mem_sl_ipdmem_data_mem_first)—Offset 200000h" on page 1857	00000000h
203FFC–203FFFh	4	"mem_isp_base_dmem_data_mem_sl_ipdmem_data_mem_last_type (isp_base_dmem_data_mem_sl_ipdmem_data_mem_last)—Offset 203FFCh" on page 1858	00000000h
300000–300003h	4	"mem_scp_dmem_mem_sl_ip_dmem_mem_first_type (scp_dmem_mem_sl_ip_dmem_mem_first)—Offset 300000h" on page 1859	00000000h
307FFC–307FFFh	4	"mem_scp_dmem_mem_sl_ip_dmem_mem_last_type (scp_dmem_mem_sl_ip_dmem_mem_last)—Offset 307FFCh" on page 1859	00000000h
380000–380003h	4	"receive_from_SP (fa_sp_isp_receive_from_SP)—Offset 380000h" on page 1860	00000000h
380004–380007h	4	"receive_from_ISP (fa_sp_isp_receive_from_ISP)—Offset 380004h" on page 1860	00000000h
380008–38000Bh	4	"send_to_SP (fa_sp_isp_send_to_SP)—Offset 380008h" on page 1861	00000000h
38000C–38000Fh	4	"send_to_ISP (fa_sp_isp_send_to_ISP)—Offset 38000Ch" on page 1861	00000000h
380010–380013h	4	"check_receive_from_SP (fa_sp_isp_check_receive_from_SP)—Offset 380010h" on page 1862	00000001h
380014–380017h	4	"check_receive_from_ISP (fa_sp_isp_check_receive_from_ISP)—Offset 380014h" on page 1863	00000001h
380018–38001Bh	4	"check_send_to_SP (fa_sp_isp_check_send_to_SP)—Offset 380018h" on page 1864	00000000h
38001C–38001Fh	4	"check_send_to_ISP (fa_sp_isp_check_send_to_ISP)—Offset 38001Ch" on page 1864	00000000h

5.4.1 mem_isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_first_type (isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_first)—Offset 1C0000h

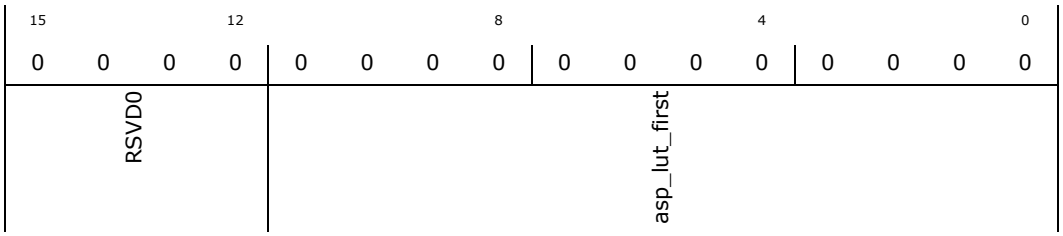
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ISPMMADR] + 1C0000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000h



Bit Range	Default and Access	Field Name (ID): Description
15:12	0x0 RO	**RSVD0:** Reserved
11:0	0x0 RW	**asp_lut_first:** Read Latency of 67 cycles. Write latency of 0 cycles

5.4.2 mem_isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_last_type (isp_simd_vamem1_asp_lut_sl_ipvamem_asp_lut_last)—Offset 1C0FFEh

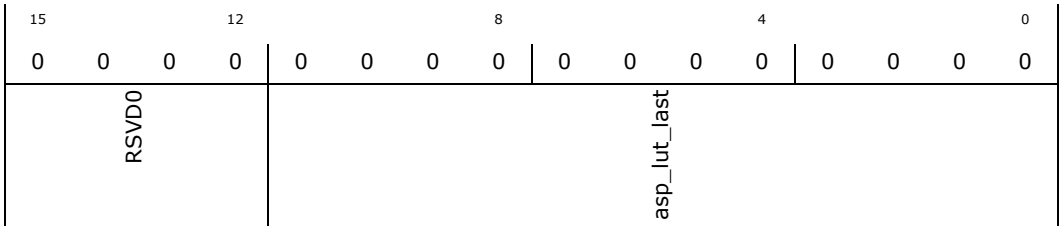
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ISPMMADR] + 1C0FFEh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000h



Bit Range	Default and Access	Field Name (ID): Description
15:12	0x0 RO	**RSVD0:** Reserved
11:0	0x0 RW	**asp_lut_last:** Read Latency of 67 cycles. Write latency of 0 cycles

5.4.3 mem_isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_first_type (isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_first)—Offset 1D0000h

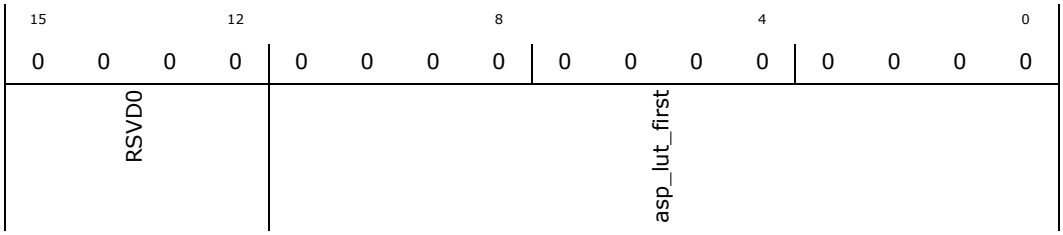
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ISPMMADR] + 1D0000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000h



Bit Range	Default and Access	Field Name (ID): Description
15:12	0x0 RO	**RSVD0:** Reserved
11:0	0x0 RW	**asp_lut_first:** Read Latency of 67 cycles. Write latency of 0 cycles

5.4.4 mem_isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_last_type (isp_simd_vamem2_asp_lut_sl_ipvamem_asp_lut_last)—Offset 1D0FFEh

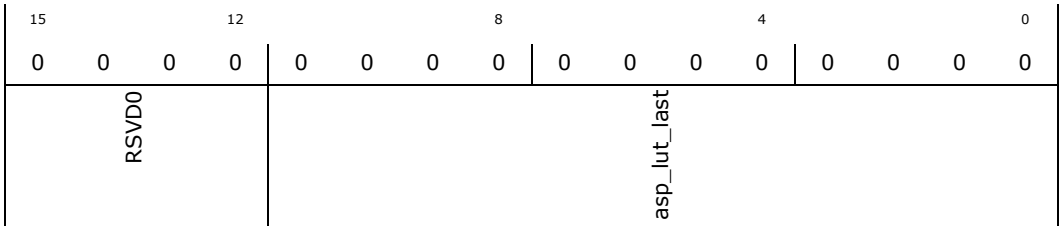
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ISPMMADR] + 1D0FFEh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000h



Bit Range	Default and Access	Field Name (ID): Description
15:12	0x0 RO	**RSVD0:** Reserved
11:0	0x0 RW	**asp_lut_last:** Read Latency of 67 cycles. Write latency of 0 cycles

5.4.5 mem_isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_first_type (isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_first) —Offset 1E0000h

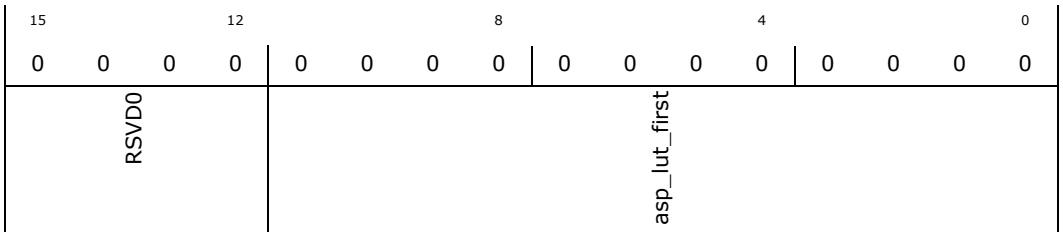
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ISPMMADR] + 1E0000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000h



Bit Range	Default and Access	Field Name (ID): Description
15:12	0x0 RO	**RSVD0:** Reserved
11:0	0x0 RW	**asp_lut_first:** Read Latency of 67 cycles. Write latency of 0 cycles

5.4.6 mem_isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_last_type

(isp_simd_vamem3_asp_lut_sl_ipvamem_asp_lut_last)—Offset 1E0FFEh

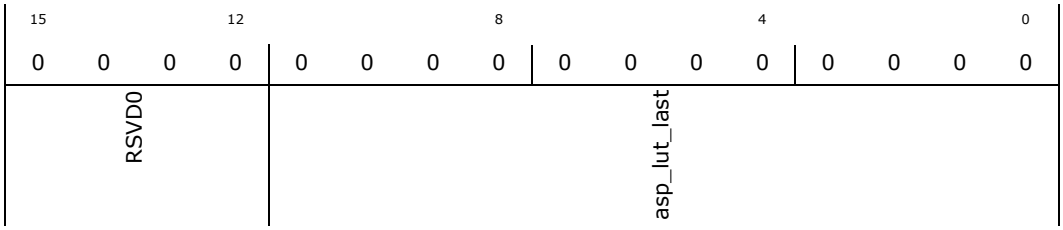
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ISPMMADR] + 1E0FFEh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 0000h



Bit Range	Default and Access	Field Name (ID): Description
15:12	0x0 RO	**RSVD0:** Reserved
11:0	0x0 RW	**asp_lut_last:** Read Latency of 67 cycles. Write latency of 0 cycles

5.4.7 mem_isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_first_type (isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_first)—Offset 1F0000h

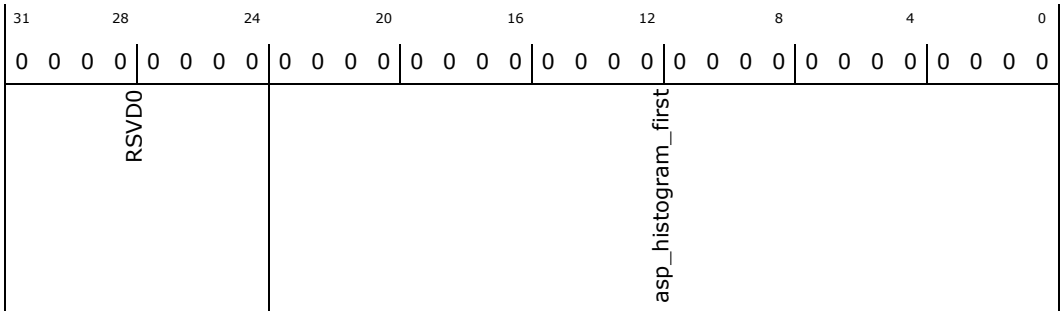
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 1F0000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD0:** Reserved
23:0	0x0 RW	**asp_histogram_first:** Read Latency of 66 cycles. Write latency of 0 cycles

5.4.8 mem_isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_last_type (isp_simd_histogram_asp_histogram_sl_iphist_asp_histogram_last)—Offset 1F0FFCh

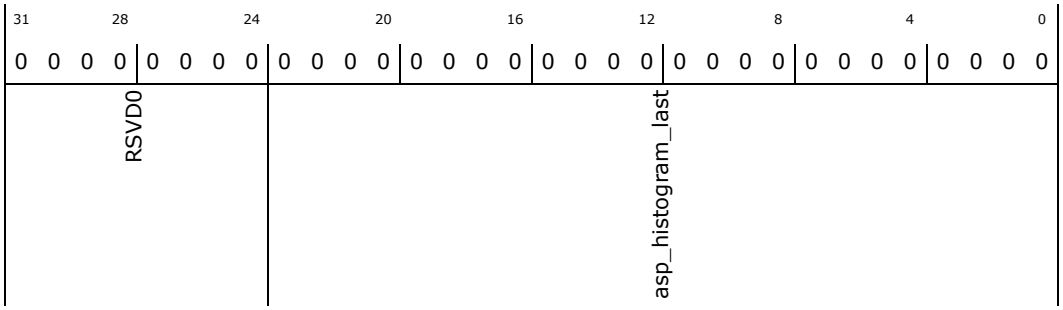
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 1F0FFCh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD0:** Reserved
23:0	0x0 RW	**asp_histogram_last:** Read Latency of 66 cycles. Write latency of 0 cycles

5.4.9 mem_isp_base_dmem_data_mem_sl_ipdmem_data_mem_first_type (isp_base_dmem_data_mem_sl_ipdmem_data_mem_first)—Offset 200000h

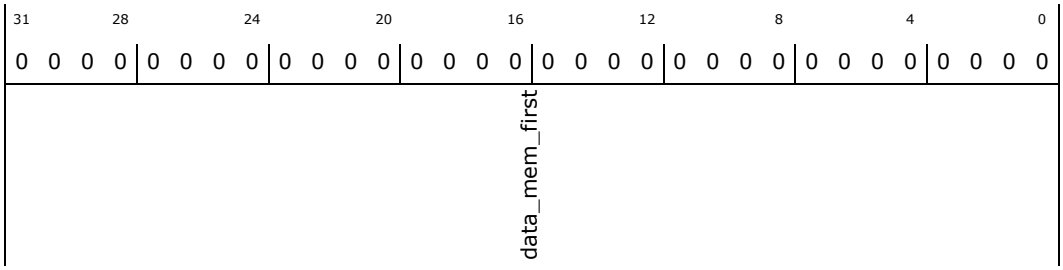
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 200000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**data_mem_first:** Read Latency of 2 cycles. Write latency of 0 cycles

5.4.10 mem_isp_base_dmem_data_mem_sl_ipdmem_data_mem_last_type (isp_base_dmem_data_mem_sl_ipdmem_data_mem_last)—Offset 203FFCh

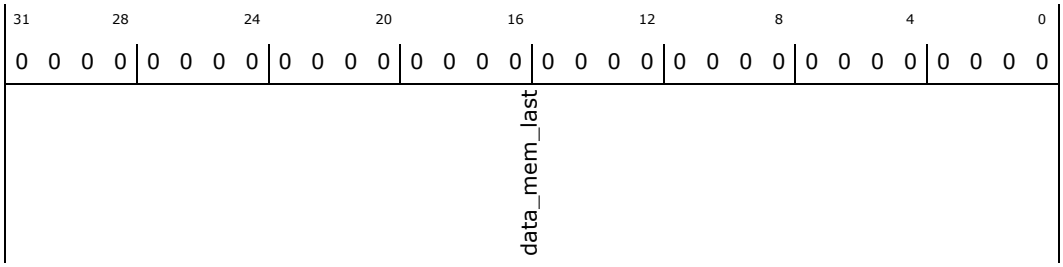
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 203FFCh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**data_mem_last:** Read Latency of 2 cycles. Write latency of 0 cycles

5.4.11 mem_scp_dmem_mem_sl_ip_dmem_mem_first_type (scp_dmem_mem_sl_ip_dmem_mem_first)—Offset 300000h

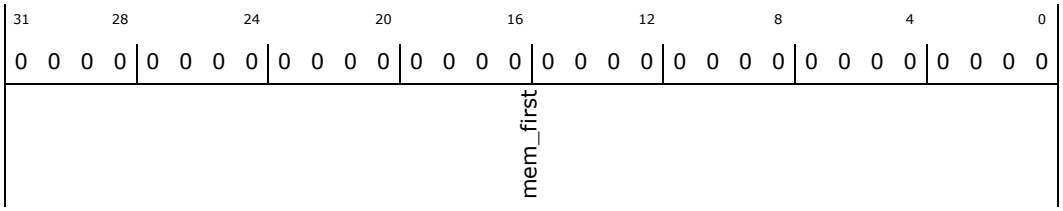
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 300000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**mem_first:** Read Latency of 2 cycles. Write latency of 0 cycles

5.4.12 mem_scp_dmem_mem_sl_ip_dmem_mem_last_type (scp_dmem_mem_sl_ip_dmem_mem_last)—Offset 307FFCh

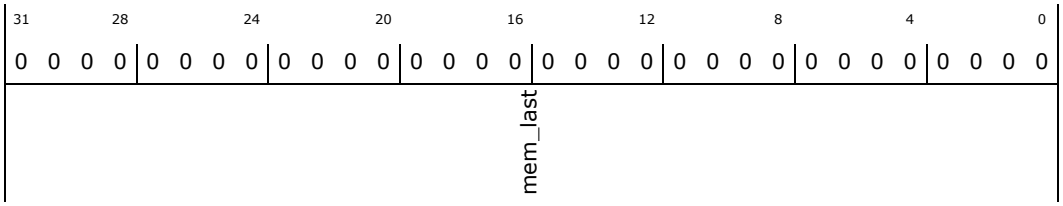
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 307FFCh

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**mem_last:** Read Latency of 2 cycles. Write latency of 0 cycles

5.4.13 receive_from_SP (fa_sp_isp_receive_from_SP)—Offset 380000h

Receive data from the FIFO between SP streaming output port and the host. Mind that a read to this register will stall if the FIFO is empty!

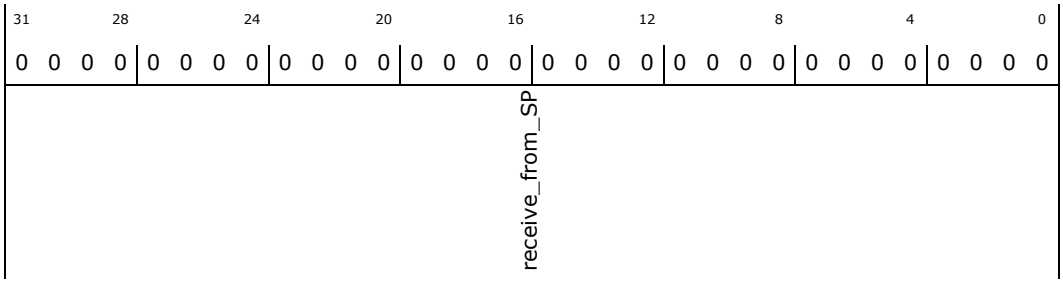
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 380000h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**receive_from_SP:** Receive data from the FIFO between SP streaming output port and the host. Mind that a read to this register will stall if the FIFO is empty!

5.4.14 receive_from_ISP (fa_sp_isp_receive_from_ISP)—Offset 380004h

Receive data from the FIFO between ISP streaming output port and the host. Mind that a read to this register will stall if the FIFO is empty!

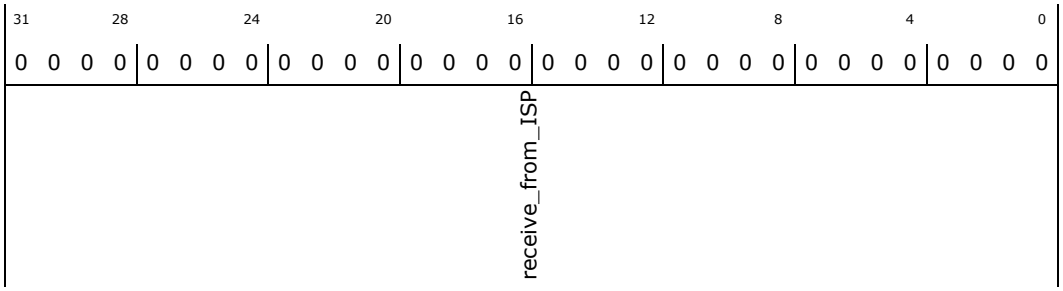
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 380004h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RO	**receive_from_ISP:** Receive data from the FIFO between ISP streaming output port and the host. Mind that a read to this register will stall if the FIFO is empty!

5.4.15 send_to_SP (fa_sp_isp_send_to_SP)—Offset 380008h

Send data to the FIFO between the host and the SP streaming input port. Mind that a write to this register will stall if the FIFO is full!

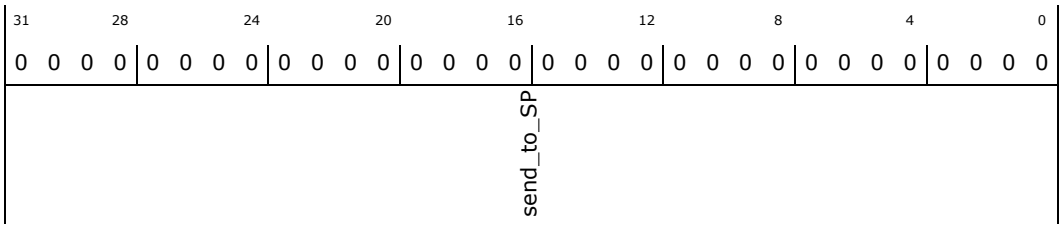
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 380008h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 WO	**send_to_SP:** Send data to the FIFO between the host and the SP streaming input port. Mind that a write to this register will stall if the FIFO is full!

5.4.16 send_to_ISP (fa_sp_isp_send_to_ISP)—Offset 38000Ch

Send data to the FIFO between the host and the ISP streaming input port. Mind that a write to this register will stall if the FIFO is full!

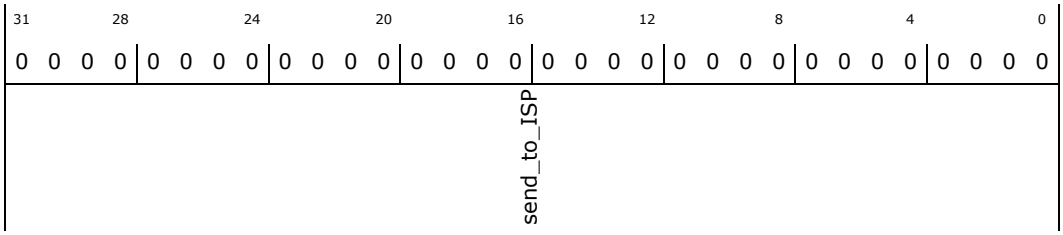
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 38000Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 WO	**send_to_ISP:** Send data to the FIFO between the host and the ISP streaming input port. Mind that a write to this register will stall if the FIFO is full!

5.4.17 check_receive_from_SP (fa_sp_isp_check_receive_from_SP)—Offset 380010h

Check the status of the FIFO between SP and host. Returns 1 if this FIFO is empty. Returns 0 if a token is available from the SP.

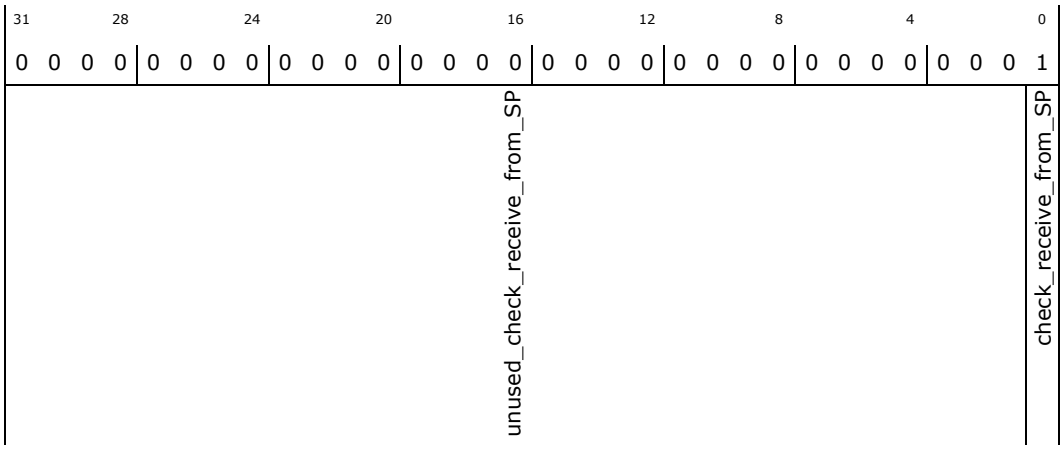
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 380010h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_check_receive_from_SP):** Unused
0	0x1 RO	**check_receive_from_SP:** Check the status of the FIFO between SP and host. Returns 1 if this FIFO is empty. Returns 0 if a token is available from the SP.

5.4.18 check_receive_from_ISP (fa_sp_isp_check_receive_from_ISP)—Offset 380014h

Check the status of the FIFO between ISP and host. Returns 1 if this FIFO is empty. Returns 0 if a token is available from the ISP.

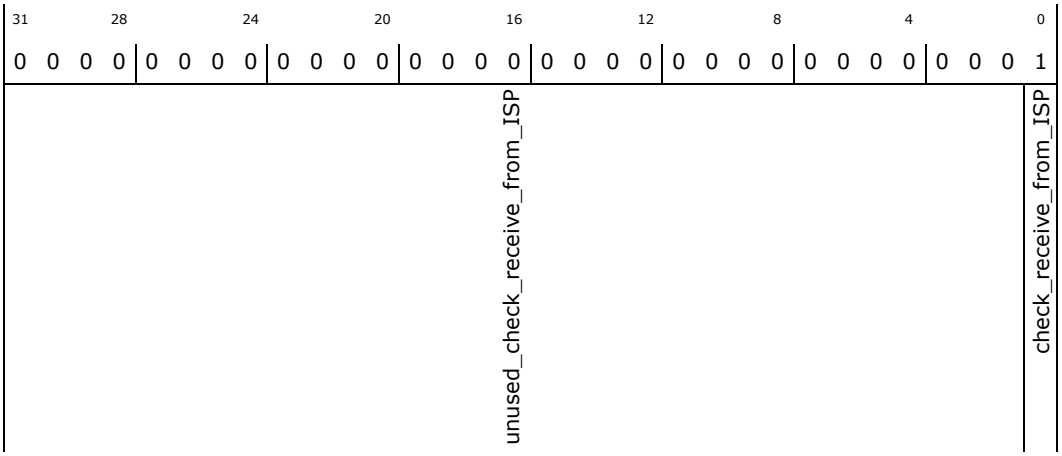
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 380014h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000001h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_check_receive_from_ISP):** Unused
0	0x1 RO	**check_receive_from_ISP:** Check the status of the FIFO between ISP and host. Returns 1 if this FIFO is empty. Returns 0 if a token is available from the ISP.

5.4.19 check_send_to_SP (fa_sp_isp_check_send_to_SP)—Offset 380018h

Check the status of the FIFO between host and SP streaming input port. Returns 1 if this FIFO is full. Returns 0 when this FIFO is not full.

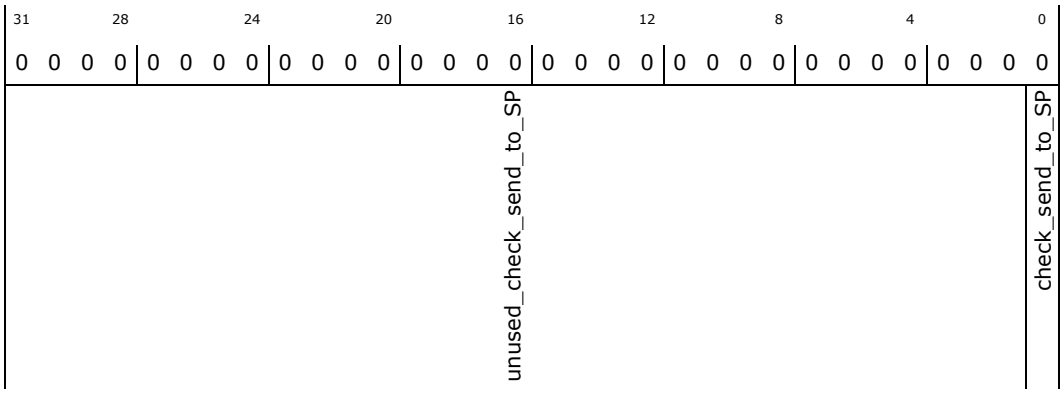
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 380018h

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_check_send_to_SP):** Unused
0	0x0 RO	**check_send_to_SP:** Check the status of the FIFO between host and SP streaming input port. Returns 1 if this FIFO is full. Returns 0 when this FIFO is not full

5.4.20 check_send_to_ISP (fa_sp_isp_check_send_to_ISP)—Offset 38001Ch

Check the status of the FIFO between host and ISP streaming input port. Returns 1 if this FIFO is full. Returns 0 when this FIFO is not full

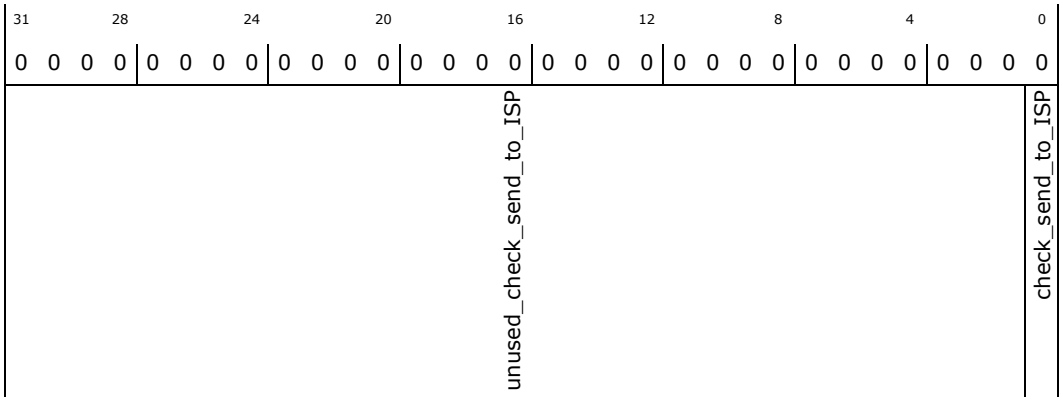
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ISPMMADR] + 38001Ch

ISPMMADR Type: PCI Configuration Register (Size: 32 bits)
ISPMMADR Reference: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved (unused_check_send_to_ISP):** Unused
0	0x0 RO	**check_send_to_ISP:** Check the status of the FIFO between host and ISP streaming input port. Returns 1 if this FIFO is full. Returns 0 when this FIFO is not full

5.5 Imaging Unit Doorbell PCI Configuration Registers

Table 30. Summary of Imaging Unit Doorbell PCI Configuration Registers—0/3/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
A0–A3h	4	"Sideband Packet (SB_PCKT)—Offset A0h" on page 1867	00000000h
A4–A7h	4	"Sideband Data (SB_DATA)—Offset A4h" on page 1867	00000000h
A8–ABh	4	"Sideband Address (SB_ADDR)—Offset A8h" on page 1868	00000000h
AC–AFh	4	"Sideband Status (SB_STATUS)—Offset ACh" on page 1868	00000000h

5.5.1 Sideband Packet (SB_PCKT)—Offset A0h

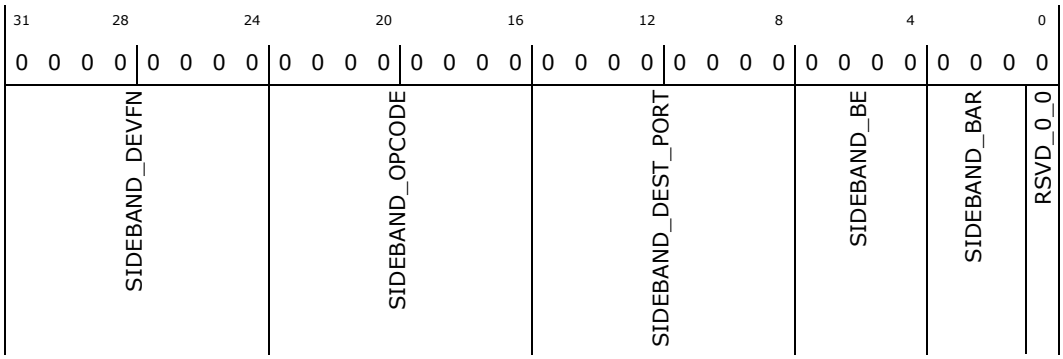
Sideband Packet: When the Sideband Packet Register is written the IUNIT creates a transaction towards the destination agent on the IOSF sideband channel. Register is only writeable when SB_STATUS[0] is cleared.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**SIDEBAND_DEVFN:** The device and function number to be used by the triggered transaction.
23:16	0x0 RW	**SIDEBAND_OPCODE:** The opcode to be used by the triggered transaction.
15:8	0x0 RW	**SIDEBAND_DEST_PORT:** The destination port to be used by the triggered transaction.
7:4	0x0 RW	**SIDEBAND_BE:** The byte enables to be used by the triggered transaction.
3:1	0x0 RW	**SIDEBAND_BAR:** The BAR value.
0	0x0 RO	**RSVD_0_0:** Reserved

5.5.2 Sideband Data (SB_DATA)—Offset A4h

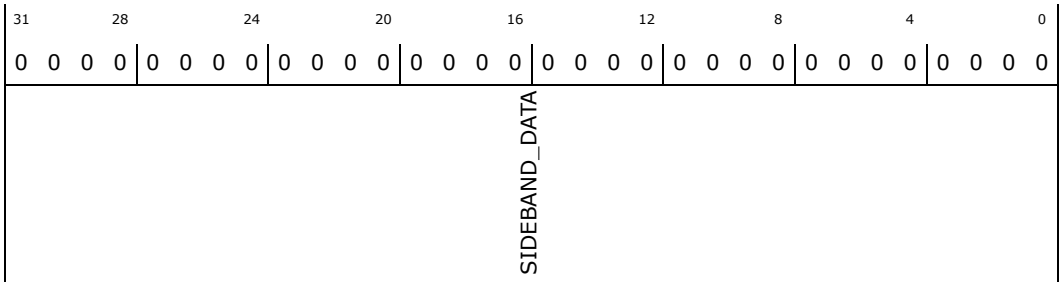
Sideband Data: The Sideband Data Register is used by the sideband register access mechanism (triggered by Sideband Packet Register) for holding write data for write transactions or read data for read transactions.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SIDEBAND_DATA:** When the operation triggered by writing to SB_PCKT register is a read transaction, the completion read data is stored in this register and is valid when SB_STATUS[0] register is cleared. When the operation triggered by writing to SB_PCKT register is a write transaction, the write data used for the transaction is taken from this register. Only writeable by software if SB_STATUS[0] is cleared.

5.5.3 Sideband Address (SB_ADDR)—Offset A8h

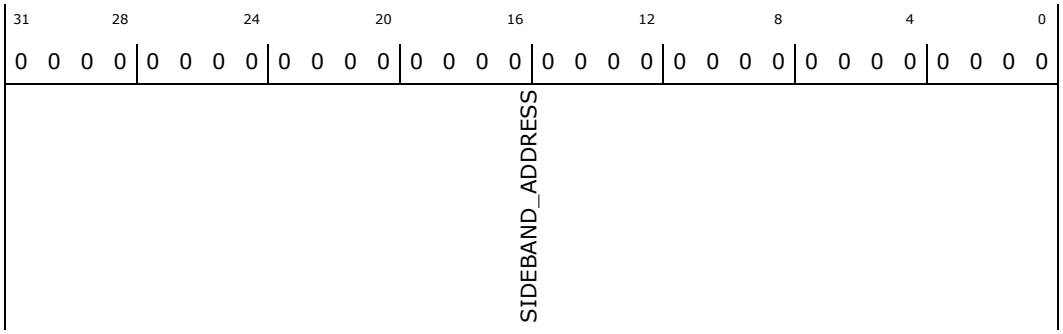
Sideband Address: The Sideband Address Register is used by the sideband register access mechanism (triggered by Sideband Packet Register) for holding the address.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SIDEBAND_ADDRESS:** The address to be used by the triggered transaction. Only writeable if SB_STATUS[0] is cleared.

5.5.4 Sideband Status (SB_STATUS)—Offset ACh

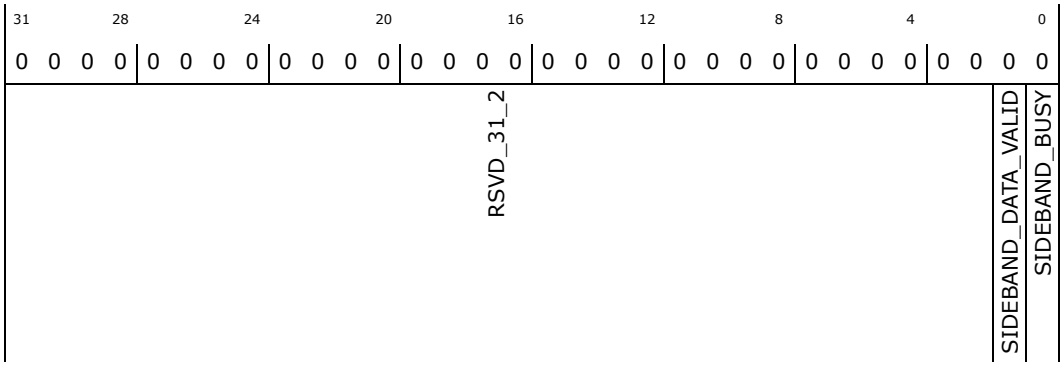
Sideband Status: When a sideband doorbell transaction is initiated.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**RSVD_31_2:** Reserved
1	0x0 RO	**SIDEBAND_DATA_VALID:** For non-posted messages, the completion status (1'b1 for successful, 1'b0 for unsuccessful) is written to this bit by hardware. For Cmp/CmpD commands this bit is cleared by hardware. For posted commands this bit is set.by hardware. This bit is valid when the SB_STATUS[0] register is cleared.
0	0x0 RO	**SIDEBAND_BUSY:** A status bit to be polled by SW before next SB access. SB_DATA, SB_ADDR and SB_PCKT registers cannot be written by software when this bit is set. In case of read transaction, data bits at SB_DATA register and data valid bit at SB_STATUS[1] register will be valid only when this bit is cleared.

5.6 Imaging Unit PCI Configuration Registers

Table 31. Summary of Imaging Unit PCI Configuration Registers—0/3/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"PCI Device and Vendor ID Register (ID)—Offset 0h" on page 1872	22B88086h
4–7h	4	"PCI Command and Status Register (PCICMDSTS)—Offset 4h" on page 1872	00100000h
8–Bh	4	"Revision Identification and Class Codes (RIDCC)—Offset 8h" on page 1873	04800000h
C–Fh	4	"Header Type (HDR)—Offset Ch" on page 1874	00000000h
10–13h	4	"Memory Mapped Address Range (ISPMMADR)—Offset 10h" on page 1874	00000000h
2C–2Fh	4	"Subsystem Identifiers (SSID)—Offset 2Ch" on page 1875	00000000h
34–37h	4	"Capabilities Pointer (CAPPOINT)—Offset 34h" on page 1875	00000080h
3C–3Fh	4	"Interrupt (INTR)—Offset 3Ch" on page 1876	00000000h
80–83h	4	"Power Management Capabilities (PMCAP)—Offset 80h" on page 1876	00229001h
84–87h	4	"Power Management Control/Status. (PMCS)—Offset 84h" on page 1877	00000000h
90–93h	4	"Message Signaled Interrupts Capability ID and Control Register (MSI_CAPID)—Offset 90h" on page 1878	00000005h
94–97h	4	"MSI Message Address (MSI_ADDRESS)—Offset 94h" on page 1879	00000000h
98–9Bh	4	"MSI Message Data (MSI_DATA)—Offset 98h" on page 1879	00000000h
9C–9Fh	4	"INTERRUPT_CONTROL—Offset 9Ch" on page 1880	00000100h
B0–B3h	4	"Performance 0 (PERF0)—Offset B0h" on page 1881	00000000h
B4–B7h	4	"Performance 1 (PERF1)—Offset B4h" on page 1881	00000000h
B8–BBh	4	"Performance 2 (PERF2)—Offset B8h" on page 1882	00000000h
BC–BFh	4	"Performance 3 (PERF3)—Offset BCh" on page 1883	00000000h
C0–C3h	4	"OCP Master Write Data (MISR0)—Offset C0h" on page 1883	FFFFFFFFh
C4–C7h	4	"OCP Master Read Data (MISR1)—Offset C4h" on page 1884	FFFFFFFFh
C8–CBh	4	"OCP Master Address and Control (MISR2)—Offset C8h" on page 1884	FFFFFFFFh
CC–CFh	4	"Scalar Processor output (MISR3)—Offset CCh" on page 1885	FFFFFFFFh
D0–D3h	4	"Manufacturing ID (MANUFACTURING_ID)—Offset D0h" on page 1885	00000000h
D4–D7h	4	"IUNIT Access control violation register (IUNIT_ACCESS_CTRL_VIOL)—Offset D4h" on page 1886	00000000h
D8–DBh	4	"IUNIT Deadline Status Register (IUNIT_DEADLINE_STATUS)—Offset D8h" on page 1887	00000000h
DC–DFh	4	"High-speed termination control MIPI CSI DPHY (IUNIT_AFE_HS_CONTROL)—Offset DCh" on page 1887	64000A00h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
E0–E3h	4	"AFE RCOMP control (IUNIT_AFE_RCOMP_CONTROL)—Offset E0h" on page 1889	00000000h
E8–EBh	4	"Control register for MIPI-CSI (IUNIT_CSI_CONTROL)—Offset E8h" on page 1890	000007F8h
EC–EFh	4	"IUNIT Deadline Control Register (IUNIT_DEADLINE_CONTROL)—Offset ECh" on page 1891	040A0100h
F0–F3h	4	"IUNIT RCOMP Status Register (IUNIT_RCOMP_STATUS)—Offset F0h" on page 1892	0C0C0C0Ch
F4–F7h	4	"MIPI CSI RCOMP control register (IUNIT_RCOMP_CONTROL)—Offset F4h" on page 1894	00200001h
F8–FBh	4	"IUNIT Status Register (IUNIT_STATUS)—Offset F8h" on page 1895	0000EB01h
FC–FFh	4	"IUNIT Control Register (IUNIT_CONTROL)—Offset FCh" on page 1896	00000103h

5.6.1 PCI Device and Vendor ID Register (ID)—Offset 0h

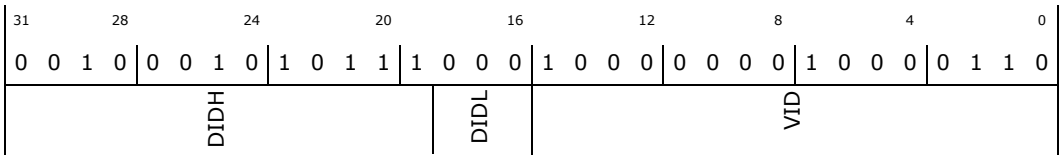
PCI Device and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 0h

Default: 22B88086h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0x457 RO	**DIDH:** DEVICE_IDENTIFICATION_NUMBER_HIGH: Upper bits of ISP Device ID. Connected to straps at IUNIT top level. (SoC IUNIT Device IDs range from 16'h22B8 through 16'h22BF
18:16	0x0 RO	**DIDL:** DEVICE_IDENTIFICATION_NUMBER_LOW: Lower bits of ISP Device ID. Connected to fuse FB_isp_device_id.
15:0	0x8086 RO	**VID:** VENDOR_IDENTIFICATION_NUMBER: PCI standard identification for Intel.

5.6.2 PCI Command and Status Register (PCICMDSTS)—Offset 4h

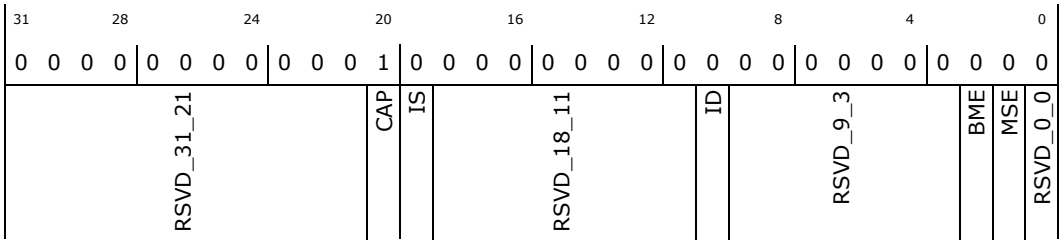
PCI Command and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RO	**RSVD_31_21:** Reserved
20	0x1 RO	**CAP:** CAPABILITY_LIST: Indicates that the CAPPOINT register at 34h provides an offset into PCI Configuration Space containing a pointer to the location of the first item in the list.

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RO	**IS:** INTERRUPT_STATUS: Reflects the state of the interrupt in the camera device. Is set to 1 if IER and IIR are both set. Otherwise is set to 0.
18:11	0x0 RO	**RSVD_18_11:** Reserved
10	0x0 RW	**ID:** INTERRUPT_DISABLE: When 1, blocks the sending of ASSERT_INTA and DEASSERT_INTA messages to the Intel Legacy Block (ILB). The interrupt status is not blocked from being reflected in PCICMDSTS.IS. When 0, permits the sending of ASSERT_INTA and DEASSERT_INTA messages to the ILB.
9:3	0x0 RO	**RSVD_9_3:** Reserved
2	0x0 RW	**BME:** BUS_MASTER_ENABLE: Enables ISP to function as a PCI compliant master. When 0, blocks the sending of MSI interrupts. When 1, permits the sending of MSI interrupts.
1	0x0 RW	**MSE:** MEMORY_SPACE_ENABLE: When set, accesses to this device's memory space is enabled. When 1, the ISP will compare the incoming address on the IOSF bus with ISPMMADR(31:22). If there is a match and if the IOSF command is either a MEMRD or MEMWR, the ISP will select the command and present it on the AHB bus. When 0, the ISP will not claim MEMRD or MEMWR IOSF commands.
0	0x0 RO	**RSVD_0_0:** Reserved

5.6.3 Revision Identification and Class Codes (RIDCC)—Offset 8h

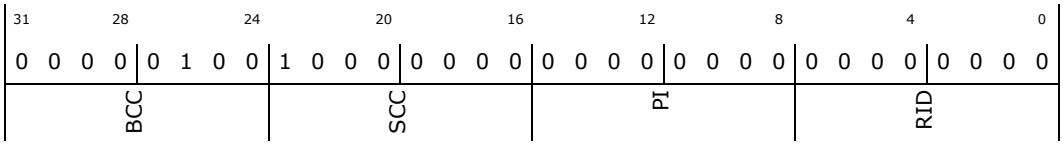
Revision Identification and Class Codes

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 8h

Default: 04800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x4 RO	**BCC:** BASE_CLASS_CODE: Indicates a multimedia device.
23:16	0x80 RO	**SCC:** SUB_CLASS_CODE: Indicates other multimedia device.
15:8	0x0 RO	**PI:** PROGRAMMING_INTERFACE: Default programming interface.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**RID:** REVISION_ID: The value in this field reflects the value of strapRID(7:0) (which is an input pin of ISP) and can be changed with each stepping of the silicon.

5.6.4 Header Type (HDR)—Offset Ch

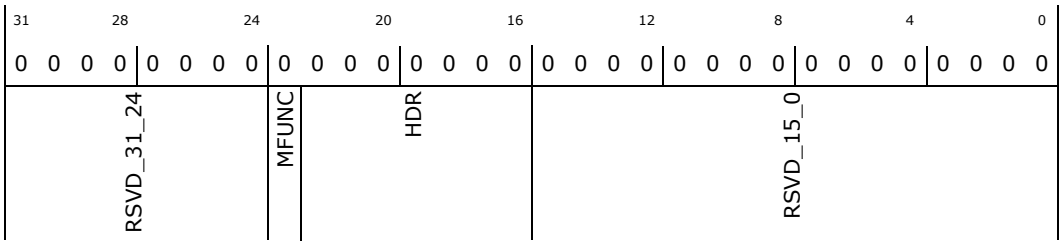
Header Type

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD_31_24:** Reserved
23	0x0 RO	**MFUNC:** MULTI_FUNCTION_STATUS: IUNIT is a single function.
22:16	0x0 RO	**HDR:** HEADER_CODE: Indicates a type 0 header format.
15:0	0x0 RO	**RSVD_15_0:** Reserved

5.6.5 Memory Mapped Address Range (ISPMMADR)—Offset 10h

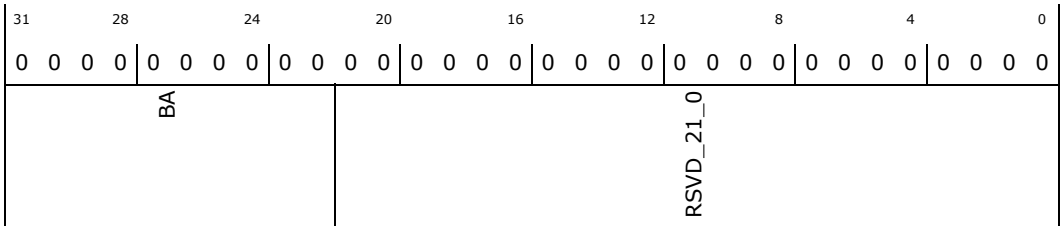
Memory Mapped Address Range. This is the base address for all memory mapped registers.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RW	**BA:** BASE_ADDRESS: Set by the OS, these bits correspond to address signals (31:22). The ISP will compare the IOSF address (31:22) with ISPMMADR(31:22). If there is a match, and PCICMDSTS(1) = MSE = 1 and the IOSF command is either a MEMRD or MEMWR, the ISP will select the command and present it on the AHB bus to the vendor IP.
21:0	0x0 RO	**RSVD_21_0:** Reserved

5.6.6 Subsystem Identifiers (SSID)—Offset 2Ch

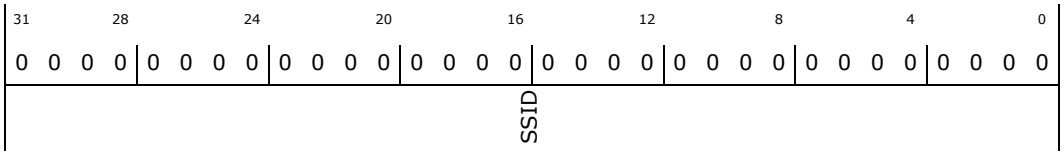
Subsystem Identifiers

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**SSID:** SUBSYSTEM_IDENTIFIERS: The value in this field is a copy of the SSID register programmed by the graphics device driver or BIOS in the Device 0/2/0 PCI header. To change the subsystem ID, write to Device 0/2/0 SSID instead of to this SSID.

5.6.7 Capabilities Pointer (CAPPOINT)—Offset 34h

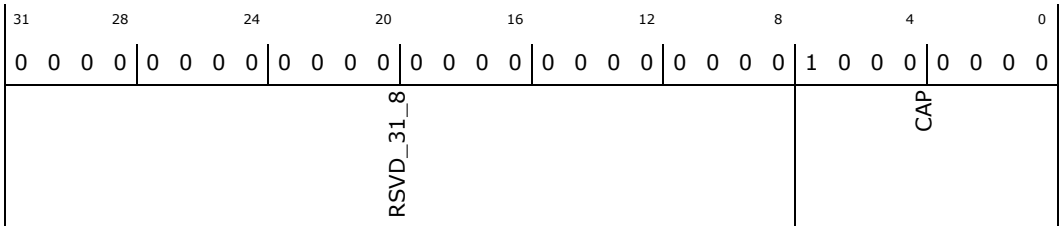
Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 34h

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD_31_8:** Reserved
7:0	0x80 RO	**CAP:** CAPABILITIES_POINTER: The first item in the capabilities list is at address 80h.

5.6.8 Interrupt (INTR)—Offset 3Ch

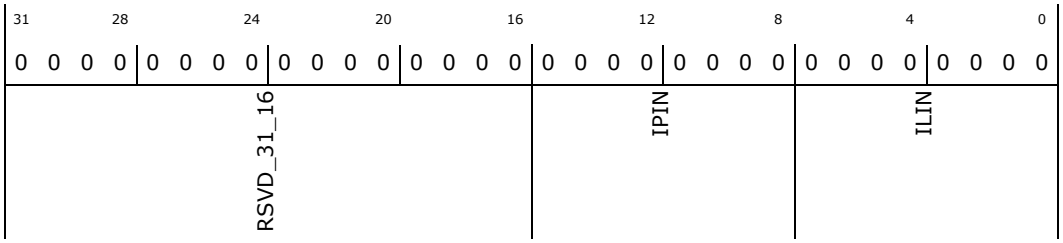
Interrupt. This register is programmed by SBIOS.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 3Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD_31_16:** Reserved
15:8	0x0 RO	**IPIN:** INTERRUPT_PIN: PCI Device 0/3/0 (IUNIT) is a single function device. If INTx is used, the PCI spec requires that it use INTA#. If INTx is used (FB_intx_supported fuse is 1), then this field is hard coded to 01h. If INTx is not used (FB_intx_supported fuse is 0), this field is hard coded to 00h.
7:0	0x0 RW	**ILIN:** INTERRUPT_LINE: BIOS written value to communicate interrupt line routing information to the ISP device driver.

5.6.9 Power Management Capabilities (PMCAP)—Offset 80h

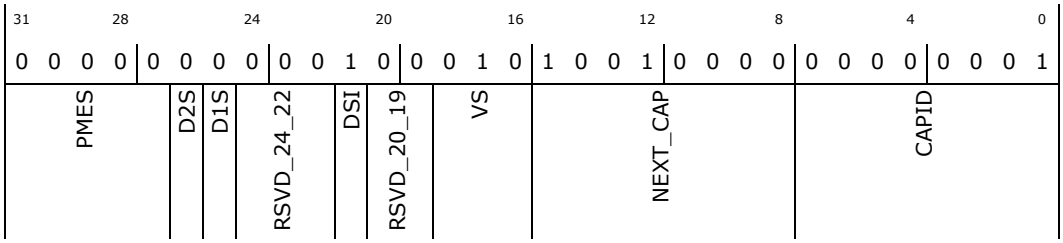
Power Management Capabilities

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 80h

Default: 00229001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMES:** PME_SUPPORT: The camera controller does not generate PME#.
26	0x0 RO	**D2S:** D2_SUPPORT: The D2 power management state is not supported.
25	0x0 RO	**D1S:** D1_SUPPORT: The D1 power management state is not supported.
24:22	0x0 RO	**RSVD_24_22:** Reserved
21	0x1 RO	**DSI:** DEVICE_SPECIFIC_INITIALIZATION: Hardwired to 1 to indicate that special initialization of the camera controller is required before generic class device driver is to use it.
20:19	0x0 RO	**RSVD_20_19:** Reserved
18:16	0x2 RO	**VS:** VERSION: Indicates compliance with revision 1.1 of the PCI Power Management Specification.
15:8	0x90 RO	**NEXT_CAP:** POINTER_TO_NEXT_CAPABILITY: Indicates the next item in the capabilities list.
7:0	0x1 RO	**CAPID:** CAPABILITIES: SIG defines this ID is 01h for power management.

5.6.10 Power Management Control/Status. (PMCS)—Offset 84h

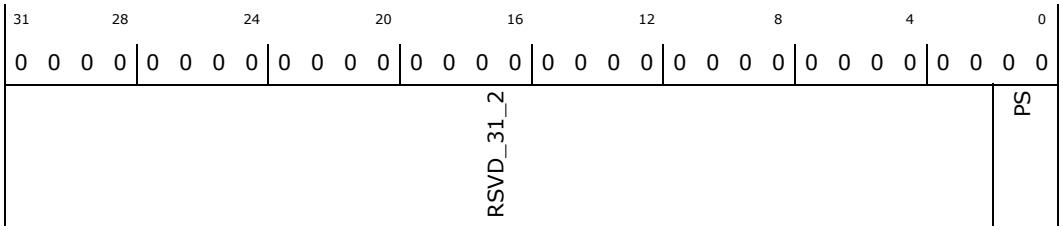
Power Management Control/Status.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 84h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**RSVD_31_2:** Reserved
1:0	0x0 RW	**PS:** POWER_STATE: Power management is implemented by writing to control registers in the PUNIT. This field may be programmed by the software driver, but no action is taken based on writing to this field.

5.6.11 Message Signaled Interrupts Capability ID and Control Register (MSI_CAPID)—Offset 90h

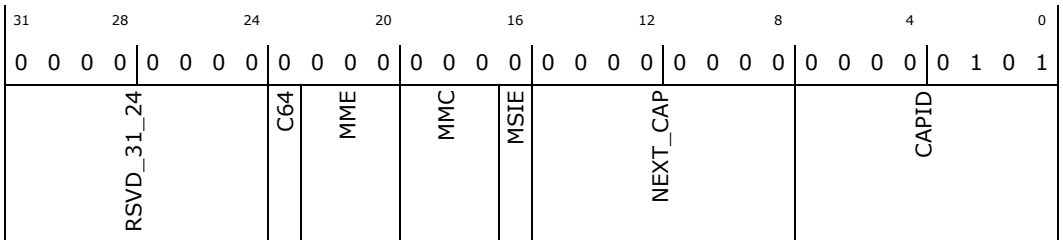
Message Signaled Interrupts Capability ID and Control Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 90h

Default: 00000005h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD_31_24:** Reserved
23	0x0 RO	**C64:** 64_BIT_ADDRESS_CAPABLE: 32-bit capable only.
22:20	0x0 RW	**MME:** MULTIPLE_MESSAGE_ENABLE: This field is RW for software compatibility, but only a single message is ever generated.
19:17	0x0 RO	**MMC:** MULTIPLE_MESSAGE_CAPABLE: This device is only single message capable.
16	0x0 RW	**MSIE:** MSI_ENABLE: If set, MSI is enabled. PCICMDSTS.BME must be set for an MSI to be generated.When 0, blocks the sending of a MSI interrupt. The interrupt status is not blocked from being reflected in the PCICMDSTS.IS bit. When 1, permits sending of a MSI interrupt.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**NEXT_CAP:** POINTER_TO_NEXT_CAPABILITY: Indicates this is the last item in the list.
7:0	0x5 RO	**CAPID:** CAPABILITY_ID: Indicates an MSI capability.

5.6.12 MSI Message Address (MSI_ADDRESS)—Offset 94h

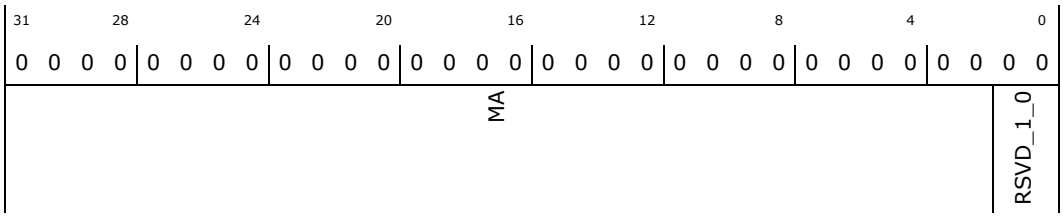
MSI Message Address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 94h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**MA:** MSI_ADDRESS: System specified message address, always DW aligned. When the ISP issues an MSI interrupt as a MEMWR on the IOSF, the memory address used is 12xFEE, MSI_ADDRESS[19:0].
1:0	0x0 RO	**RSVD_1_0:** Reserved

5.6.13 MSI Message Data (MSI_DATA)—Offset 98h

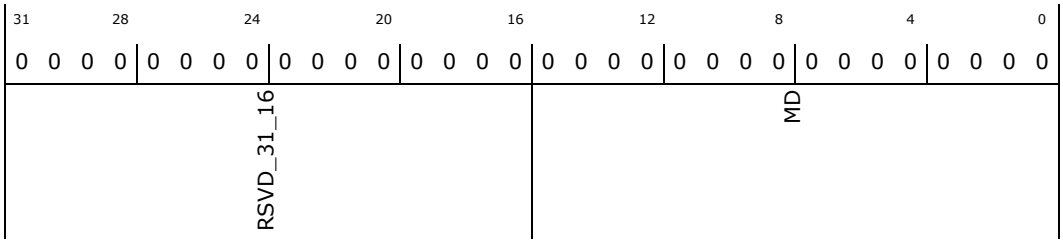
MSI Message Data

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 98h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD_31_16:** Reserved
15:0	0x0 RW	**MD:** MSI_DATA: This 16-bit field is programmed by system software and is driven onto the lower word of data during the data phase of the MSI write transaction. When the ISP issues an MSI interrupt as a MEMWR on the IOSF, the write data corresponds to the value of this field.

5.6.14 INTERRUPT_CONTROL—Offset 9Ch

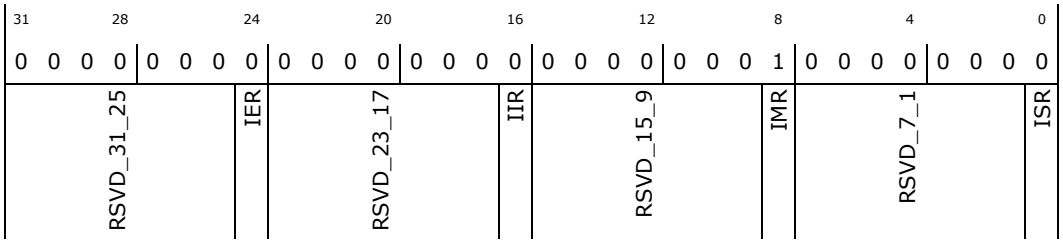
INTERRUPT_CONTROL

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + 9Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD_31_25:** Reserved
24	0x0 RW	**IER:** IER: This is an enable bit that allows the sending of an interrupt to the CPU using either MSI or INTR mechanisms. The interrupt is sent immediately to the CPU. The firmware running on the ISP guarantees ordering by reading the last data write from memory before raising the interrupt. 1 = If MSI_ENABLE is set, then an MSI is sent to the CPU when the IIR bit is set, or if the IIR bit remains set after software writes to this register. If INTERRUPT_DISABLE is not set, then an ASSERT_INTA message is sent to the Intel Legacy Block (ILB) when the IIR bit is set by hardware, or if the IIR bit remains set after software writes to this register. If software clears the IIR bit, and INTERRUPT_DISABLE is not set then a DEASSERT_INTA message is sent to the ILB. 0 = Do not generate an MSI even if the MSI_ENABLE bit is set. Do not send ASSERT_INTA or DEASSERT_INTA messages to the ILB even if the INTERRUPT_DISABLE bit is not set.
23:17	0x0 RO	**RSVD_23_17:** Reserved
16	0x0 RW/1C	**IIR:** IIR: This is the persistent value of the interrupt bit. It is set by hardware, and cleared by software. Software must write a 1 to clear this bit. Writing a 0 is a NOP. If both software and hardware attempt to write to this field in the same clock cycle, hardware wins. 1 = An interrupt was received from the vendor IP when the IMR bit was not set, and software has not yet cleared it. 0 = There is no pending interrupt.

Bit Range	Default & Access	Field Name (ID): Description
15:9	0x0 RO	**RSVD_15_9:** Reserved
8	0x1 RW	**IMR:** IMR: Interrupt Mask bit. 1 = IIR bit will not be set when the ISR bit is set. 0 = IIR bit will be set when the ISR bit is set.
7:1	0x0 RO	**RSVD_7_1:** Reserved
0	0x0 RO	**ISR:** ISR: Reflects the state of the interrupt line from the vendor IP, after it is synchronized to the czclk domain.

5.6.15 Performance 0 (PERF0)—Offset B0h

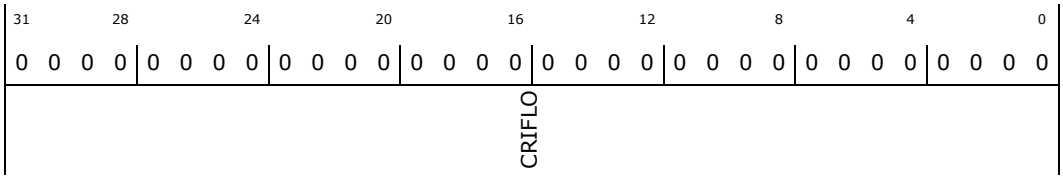
Performance

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/SE	**CRIFLO:** IUNIT has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 31:0 of the cumulative_reads_in_flight counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will enable all four counters.

5.6.16 Performance 1 (PERF1)—Offset B4h

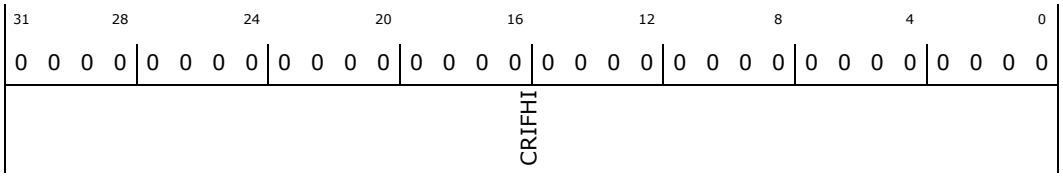
Performance

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + B4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/SE	**CRIFHI:** IUNIT has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 63:32 of the cumulative_reads_in_flight counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will disable all four counters.

5.6.17 Performance 2 (PERF2)—Offset B8h

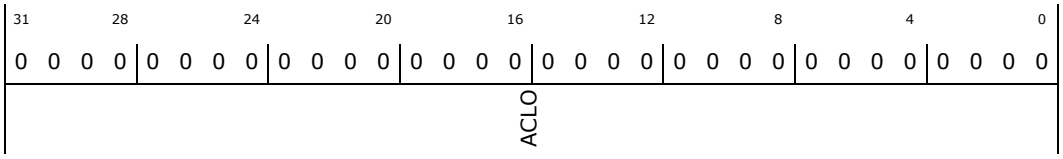
Performance

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/SE	**ACLO:** IUNIT has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 31:0 of the active_cycles counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will clear all four counters. The counters should only be cleared after they are disabled.

5.6.18 Performance 3 (PERF3)—Offset BCh

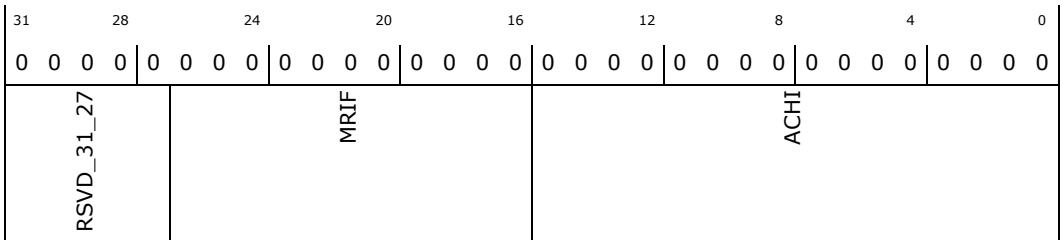
Performance

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + BCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RSVD_31_27:** Reserved
26:16	0x0 RW/SE	**MRIF:** IUNIT has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 11:0 of the max_reads_in_flight counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will clear the max_reads_in_flight counters only. The counters should only be cleared after they are disabled.
15:0	0x0 RW/SE	**ACHI:** IUNIT has four performance counters. When counting is enabled, the 11-bit reads_in_flight counter keeps track of the number of outstanding reads that have been requested, but not yet returned back at the OCP master interface. The 11-bit max_reads_in_flight counter keeps track of the maximum number of reads in flight in any given clock cycle. Each clock cycle, if there are any reads in flight, the reads_in_fight counter is added to a 64-bit cumulative_reads_in_flight counter, and the 48-bit active_cycles counter is incremented by 1. Reading this register returns bits 47:32 of the active_cycles counter. This counter should be read only after counting is disabled. Reading while the counters are enabled will return undefined values. All four counters are disabled at reset. Writing (any value) to this register, will clear the max_reads_in_flight counters only. The counters should only be cleared after they are disabled.

5.6.19 OCP Master Write Data (MISR0)—Offset C0h

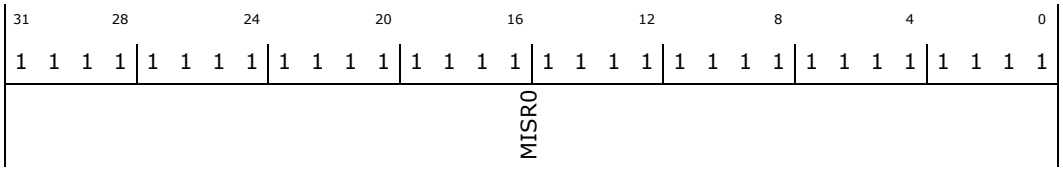
OCP Master Write Data

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + C0h

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW/C	**MISR0:** MISR0: Write to this register address clears this MISR. This is a 8:1 compression MISR capturing the 256-bit write data on the OCP interface between ISP_CSS and Iunit wrapper.

5.6.20 OCP Master Read Data (MISR1)—Offset C4h

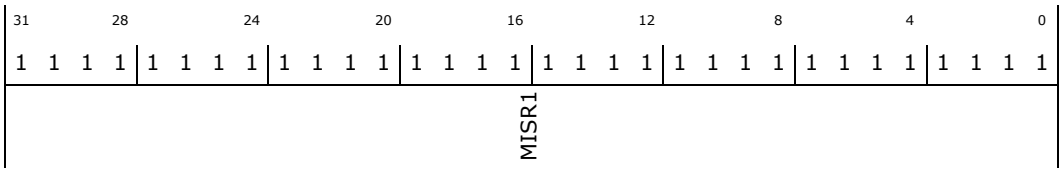
OCP Master Read Data

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + C4h

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW/C	**MISR1:** MISR1: Write to this register address clears this MISR. This is a 8:1 compression MISR capturing the 256-bit read return data on the OCP interface between ISP_CSS and Iunit wrapper.

5.6.21 OCP Master Address and Control (MISR2)—Offset C8h

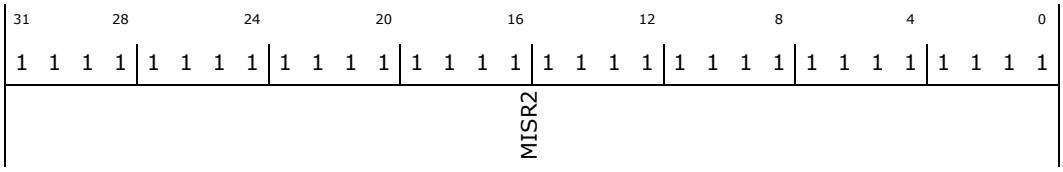
OCP Master Address and Control

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + C8h

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW/C	**MISR2:** MISR2: Write to this register address clears this MISR. This is a 4:1 compression MISR capturing the control signals on the OCP Master port in the Iunit.

5.6.22 Scalar Processor output (MISR3)—Offset CCh

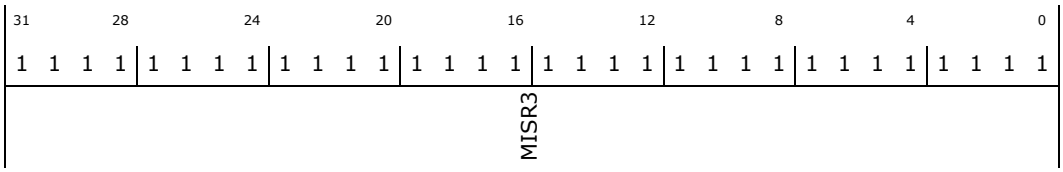
Scalar Processor output

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + CCh

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW/C	**MISR3:** MISR3: Write to this register address clears this MISR. This is a 4:1 compression MISR capturing the output signals of the Scalar Processor.

5.6.23 Manufacturing ID (MANUFACTURING_ID)—Offset D0h

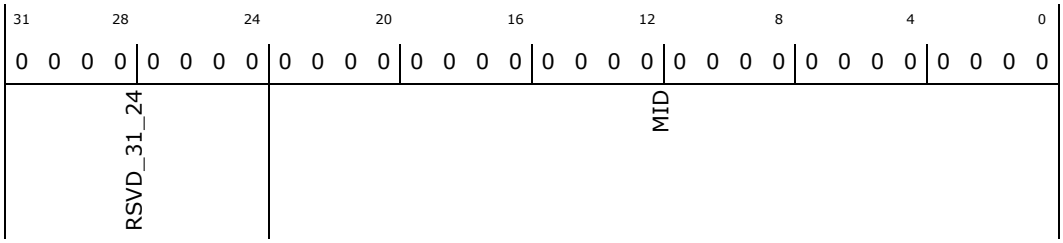
Manufacturing ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD_31_24:** Reserved
23:0	0x0 RO	**MID:** MANUFACTURING_ID: Hardwired to strapMANID(23:0).

5.6.24 IUNIT Access control violation register (IUNIT_ACCESS_CTRL_VIOL)—Offset D4h

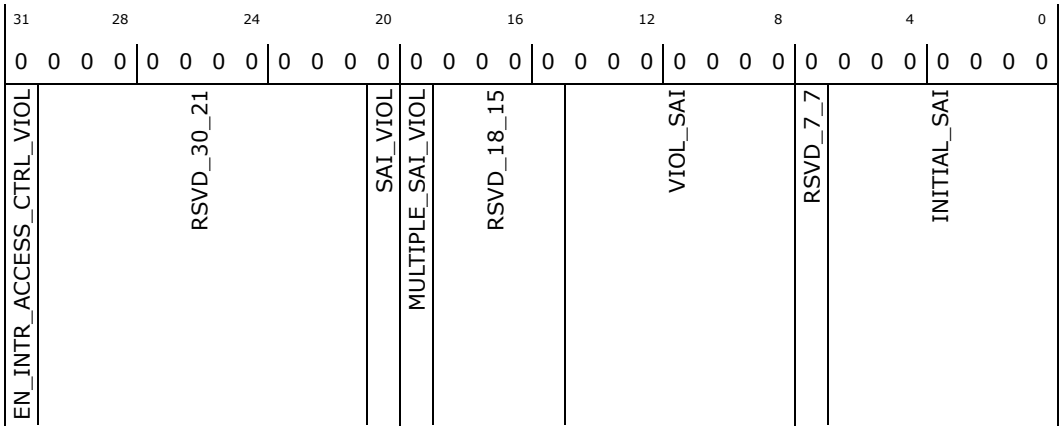
IUNIT Access control violation register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + D4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**EN_INTR_ACCESS_CTRL_VIOL:** Enable Interrupt on access control violation: When set, the IUNIT will latch violation information into this register and send an interrupt request (opcode 0XEE) and (port 0x04) to the PUNIT.
30:21	0x0 RO	**RSVD_30_21:** Reserved
20	0x0 RW	**SAI_VIOL:** SAI_VIOL: If set, the IUNIT has detected an SAI violation and has captured the status in this register. This bit must be cleared by software in order for IUNIT to capture the next violation.
19	0x0 RW	**MULTIPLE_SAI_VIOL:** If set, more than one SAI violation has been detected in the IUNIT. Status for the 1st violation has been captured in this register. It is recommend that software clear this bit whenever it clears bit[20] of this register.
18:15	0x0 RO	**RSVD_18_15:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
14:8	0x0 RW	**VIOL_SAI:** VIOL_SAI: SAI bits that triggered the violation: This 7-bit value indicates the SAI of the subsequent transaction which caused the violation.
7	0x0 RO	**RSVD_7_7:** Reserved
6:0	0x0 RW	**INITIAL_SAI:** INITIAL_SAI: This 7-bit value indicates the SAI of the initial transaction for SAI mismatch error codes.

5.6.25 IUNIT Deadline Status Register (IUNIT_DEADLINE_STATUS)—Offset D8h

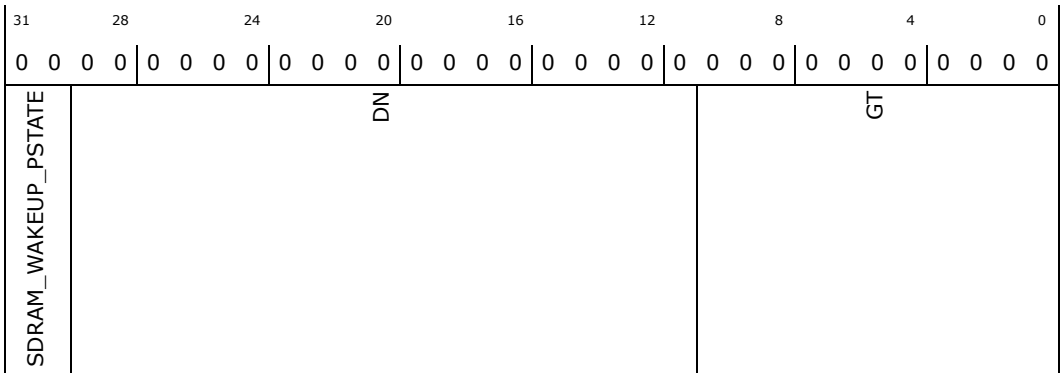
IUNIT Deadline Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + D8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**SDRAM_WAKEUP_PSTATE:** SDRAM_WAKEUP_PSTATE: State of the SDRAM_WAKEUP state machine. 00b = State machine is idle; 01b = sdram_wakeup seen, waiting for all memory transactions in flight to complete; 10b = All memory transactions are completed, waiting for acknowledgement from czclk domain before returning to idle state;
29:11	0x0 RO	**DN:** DN: Computed deadline value to be send with the next request on IB PFI bus. This is the internal deadline value. The actual deadline that is sent on the IB PFI bus is the maximum of GT+MDD or DN.
10:0	0x0 RO	**GT:** GT: Current value of Global Timer

5.6.26 High-speed termination control MIPI CSI DPHY (IUNIT_AFE_HS_CONTROL)—Offset DCh

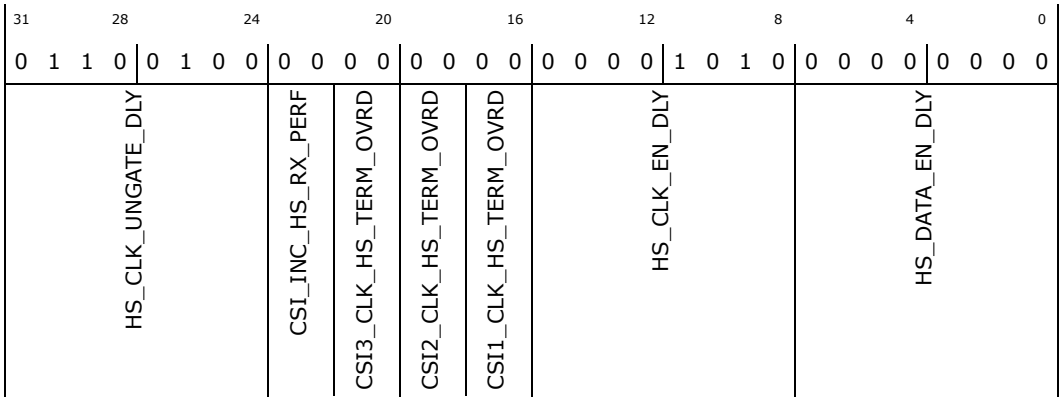
High-speed termination control MIPI CSI DPHY

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + DCh

Default: 64000A00h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x64 RW	**HS_CLK_UNGATE_DLY:** HS_CLK_UNGATE_DLY: Delay between the assertion of HS enable and the ungating of the HS clocks going to the DPHY logic for all clock lanes. HS clocks are gated by default and are ungated after Tclk-settle time. The range of this field is 0 nsec to 510 nsec in increments of 2 nsec, with reset value 0x64 indicating 200 nsec. Note that we use czclk to increment the counter, hence the actual delay can be as much as 10 nsec larger than the programmed value.
23:22	0x0 RW	**CSI_INC_HS_RX_PERF:** INC_HS_RX_PERF: Config bits to increase the High-speed Receiver performance; 00 = POR (default), 01 = +10% bias current (Stage 1 adder), 10 = TBD, 11 = TBD
21:20	0x0 RW	**CSI3_CLK_HS_TERM_OVRD:** CSI3_CLK_HS_TERM_OVRD: Override for HS termination enable for CSI3 clock lane. 00b = Use the termination enable output from the DPHY IP and gate XOR clocks in high speed mode; 01b = Keep HS termination (and HS enable) always on; 10b = Generate HS termination by sampling the CP/CN lines using coreclk and gate XOR clocks in high speed mode; 11b = Use the termination enable output from the DPHY IP;
19:18	0x0 RW	**CSI2_CLK_HS_TERM_OVRD:** CSI2_CLK_HS_TERM_OVRD: Override for HS termination enable for CSI2 clock lane. 00b = Use the termination enable output from the DPHY IP and gate XOR clocks in high speed mode; 01b = Keep HS termination (and HS enable) always on; 10b = Generate HS termination by sampling the CP/CN lines using coreclk and gate XOR clocks in high speed mode; 11b = Use the termination enable output from the DPHY IP;
17:16	0x0 RW	**CSI1_CLK_HS_TERM_OVRD:** CSI1_CLK_HS_TERM_OVRD: Override for HS termination enable for CSI1 clock lane. 00b = Use the termination enable output from the DPHY IP and gate XOR clocks in high speed mode; 01b = Keep HS termination (and HS enable) always on; 10b = Generate HS termination by sampling the CP/CN lines using coreclk and gate XOR clocks in high speed mode; 11b = Use the termination enable output from the DPHY IP;

Bit Range	Default & Access	Field Name (ID): Description
15:8	0xa RW	**HS_CLK_EN_DLY:** HS_CLK_EN_DLY: Delay between the assertion of HS termination enable and the assertion of HS enable for all clock lanes. The range of this field is 0 nsec to 510 nsec in increments of 2 nsec, with reset value 0x0A indicating 20 nsec. Note that we use czclk to increment the counter, hence the actual delay can be as much as 10 nsec larger than the programmed value.
7:0	0x0 RW	**HS_DATA_EN_DLY:** HS_DATA_EN_DLY: Delay between the assertion of HS termination enable and the assertion of HS enable for all data lanes. The range of this field is 0 nsec to 510 nsec in increments of 2 nsec, with reset value 0x0 indicating 0 nsec. Note that we use czclk to increment the counter, hence the actual delay can be as much as 10 nsec larger than the programmed value.

5.6.27 AFE RCOMP control (IUNIT_AFE_RCOMP_CONTROL)—Offset E0h

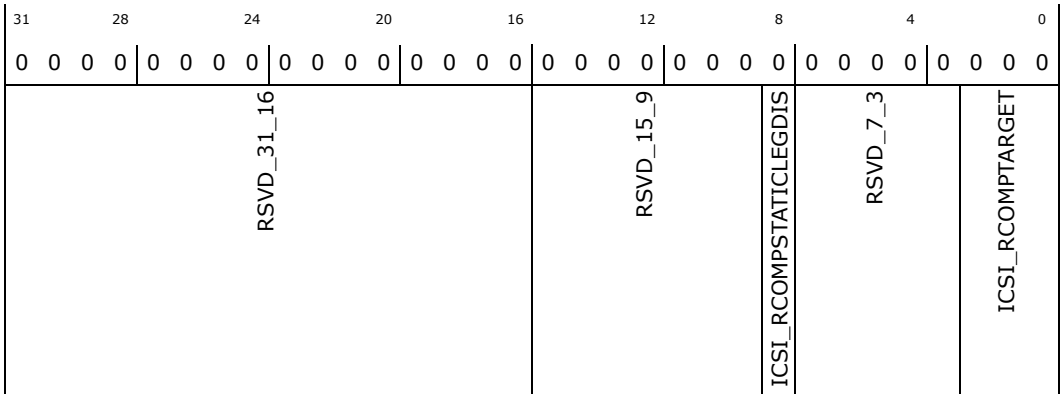
AFE RCOMP control

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + E0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD_31_16:** Reserved
15:9	0x0 RW	**RSVD_15_9:** Reserved
8	0x0 RW	**ICSI_RCOMPSTATICLEGDIS:** ICSI_RCOMPSTATICLEGDIS: Disable RCOMP static leg in AFE
7:3	0x0 RW	**RSVD_7_3:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
2:0	0x0 RW	**ICSI_RCOMPTARGET:** ICSI_RCOMPTARGET: RCOMP target level range is 90ohm or 100ohm differential impedance. 000b = 50ohms; 001b = 45ohms; other values = reserved

5.6.28 Control register for MIPI-CSI (IUNIT_CSI_CONTROL)—Offset E8h

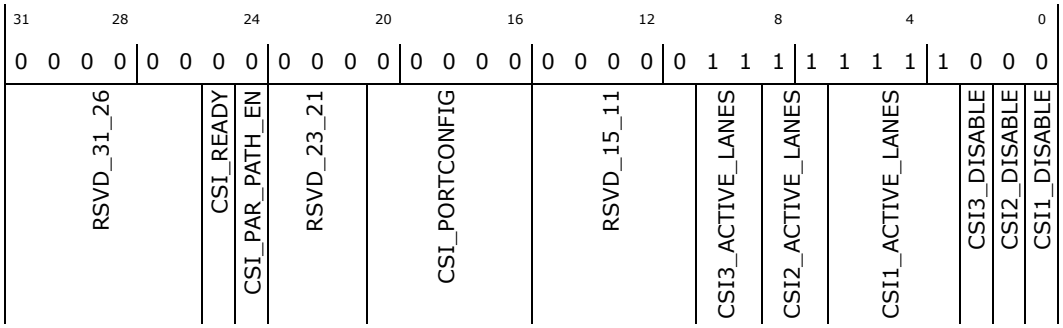
Control register for MIPI-CSI

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + E8h

Default: 000007F8h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RW	**RSVD_31_26:** Reserved
25	0x0 RW	**CSI_READY:** CSI_READY: The CSI interfaces are disabled out-of-reset to allow driver time to configure the CSI receiver before incoming packets are seen. When the input system is ready to receive CSI packets, driver must write this bit to enable the CSI interfaces at the next LP11 state. If CSI_READY_DISABLE fuse is set, the CSI interfaces are enabled out-of-reset and this field is ignored.
24	0x0 RW	**CSI_PAR_PATH_EN:** PAR_PATH_EN: Selection between Arasan DPHY and VIED DPHY; 0b = Arasan DPHY supporting up to 1.0 Gbps (default), 1b = VIED DPHY supporting up to 1.5 Gbps
23:21	0x0 RW	**RSVD_23_21:** Reserved
20:16	0x0 RW	**CSI_PORTCONFIG:** CSI_PORTCONFIG: Used to enable the CSI data lanes to CSI ports if FB_csi_portconfig_override fuse is set. This field is ignored if FB_csi_portconfig_override fuse is clear.
15:11	0x0 RW	**RSVD_15_11:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
10:9	0x3 RW	**CSI3_ACTIVE_LANES:** Used to determine which of the lanes that are enabled by the FB_csi_portconfig fuses or the CSI_PORTCONFIG field, are currently being used on the MIPI CSI3 interface. 1=active, 0=inactive.
8:7	0x3 RW	**CSI2_ACTIVE_LANES:** Used to determine which of the lanes that are enabled by the FB_csi_portconfig fuses or the CSI_PORTCONFIG field, are currently being used on the MIPI CSI2 interface. 1=active, 0=inactive.
6:3	0xf RW	**CSI1_ACTIVE_LANES:** Used to determine which of the lanes that are enabled by the FB_csi_portconfig fuses or the CSI_PORTCONFIG field, are currently being used on the MIPI CSI1 interface. 1=active, 0=inactive.
2	0x0 RW	**CSI3_DISABLE:** 1 = Disable MIPI CSI3 interface. 0 = Enable MIPI CSI3 interface if FB_csi_portdisable[2] fuse is cleared
1	0x0 RW	**CSI2_DISABLE:** 1 = Disable MIPI CSI2 interface. 0 = Enable MIPI CSI2 interface if FB_csi_portdisable[1] fuse is cleared
0	0x0 RW	**CSI1_DISABLE:** 1 = Disable MIPI CSI1 interface. 0 = Enable MIPI CSI1 interface if FB_csi_portdisable[0] fuse is cleared

5.6.29 IUNIT Deadline Control Register (IUNIT_DEADLINE_CONTROL)—Offset ECh

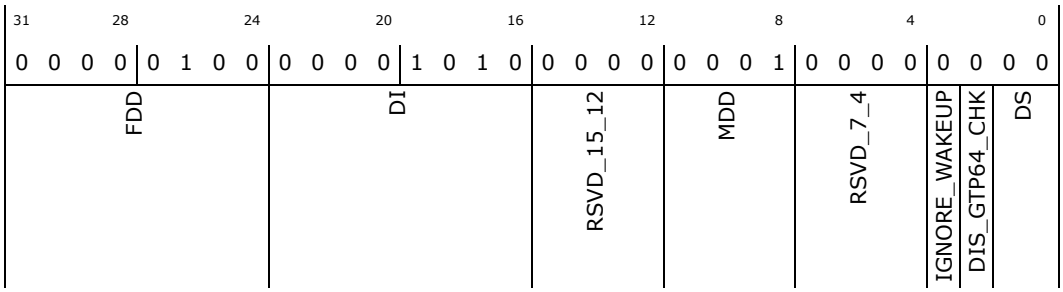
IUNIT Deadline Control Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + ECh

Default: 040A0100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x4 RW	**FDD:** FIRST_DEADLINE_DELAY: Delay between the rising edge of WAKEUP signal and the fake deadline that will be specified for the first request of that line. Unit in 250 nsec. Reset value of 8'h04 indicates FDD = 1 usec.
23:16	0xa RW	**DI:** DEADLINE_INCREMENT: Difference in deadline times between adjacent requests. If the current request is for 32B, the next deadline will be DI more than the current deadline. If the current request is for 64B, the next deadline will be 2*DI more than the current deadline. Unit in 1/1024 usec. Reset value of 8'h0A indicates DI = 9.765625 nsec.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0x0 RW	**RSVD_15_12:** Reserved
11:8	0x1 RW	**MDD:** MINIMUM_DEADLINE_DELAY: Minimum separation between current Global Timer value and the deadline specified with any request on the PFI interface. Unit is 250 nsec. Reset value of 4'h1 indicates MDD = 250 nsec.
7:4	0x0 RW	**RSVD_7_4:** Reserved
3	0x0 RW	**IGNORE_WAKEUP:** If clear, then after each rising edge of sdram_wakeup, the OCP master interface is stalled until all reads in flight and all FIFOs are empty and then the next deadline is set to GT + FDD. If set, the sdram_wakeup signal from ISP_CSS is ignored.
2	0x0 RW	**DIS_GTP64_CHK:** If clear, then the PFI interface is stalled whenever the next deadline value exceeds GT + 64 usec. This check is a safety measure to make sure that deadline does not drift too far into the future. If set, this check is not performed.
1:0	0x0 RW	**DS:** DEADLINE_SCHEME: 11b = Reserved; 10b = Reserved; 01b = When WAKEUP is asserted, FDD is added to the current global timer to compute DN. With each request, the deadline sent to System Agent is either DN, or the sum of the global timer and MDD, whichever is larger. After each request is sent, DN is computed by adding DI for each 32Byte request sent to either DN or the sum of the global timer and MDD, whichever is larger. Each clock cycle, DN is checked to make sure it is greater than the current global timer, else it is set to the global timer.; 00b = When WAKEUP is asserted, FDD is added to the current global timer to compute DN. With each request, the deadline sent to System Agent is either DN, or the sum of the global timer and MDD, whichever is larger. After each request is sent, DN is computed by adding DI for each 32Byte request sent to DN. Each cycle, DN is checked to make sure that it is either greater than the current global timer, or is less than the global timer by no more than 64 usec, else it is set to the global timer minus 64 usec.

5.6.30 IUNIT RCOMP Status Register (IUNIT_RCOMP_STATUS)—Offset F0h

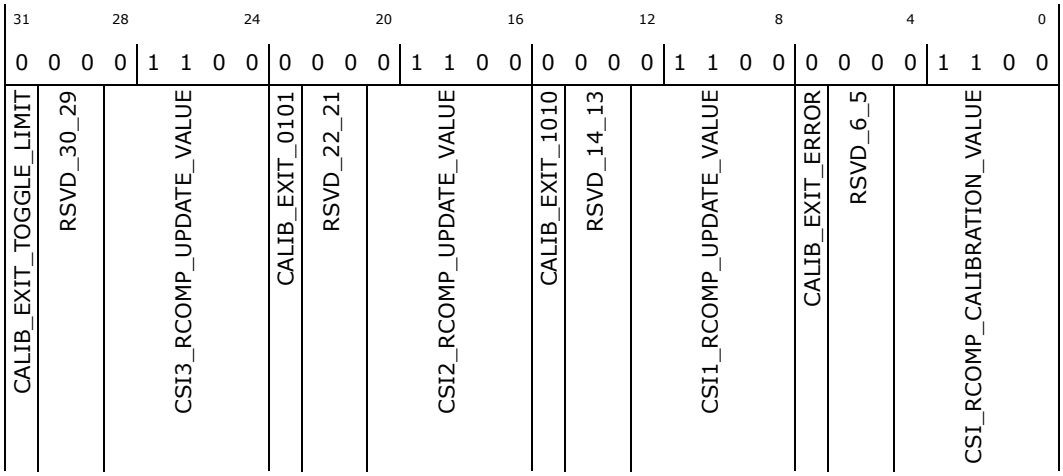
IUNIT RCOMP Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + F0h

Default: 0C0C0C0Ch



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**CALIB_EXIT_TOGGLE_LIMIT:** CALIB_EXIT_TOGGLE_LIMIT: If set, indicates that the last calibration cycle exited because the number of toggles matched the value specified by the CSI_HS_ROGGLE_LIMIT_CREG_ENC field of the IUNIT_RCOMP_CONTROL register.
30:29	0x0 RO	**RSVD_30_29:** Reserved
28:24	0xc RO	**CSI3_RCOMP_UPDATE_VALUE:** MIPI CSI3 RCOMP value: Current RCOMP value on MIPI CSI3 port
23	0x0 RO	**CALIB_EXIT_0101:** CALIB_EXIT_0101: If set, indicates that the last calibration cycle exited because the last four states of rcompcountup were 0101
22:21	0x0 RO	**RSVD_22_21:** Reserved
20:16	0xc RO	**CSI2_RCOMP_UPDATE_VALUE:** MIPI CSI2 RCOMP value: Current RCOMP value on MIPI CSI2 port
15	0x0 RO	**CALIB_EXIT_1010:** CALIB_EXIT_1010: If set, indicates that the last calibration cycle exited because the last four states of rcompcountup were 1010
14:13	0x0 RO	**RSVD_14_13:** Reserved
12:8	0xc RO	**CSI1_RCOMP_UPDATE_VALUE:** MIPI CSI1 RCOMP value: Current RCOMP value on MIPI CSI1 port
7	0x0 RO	**CALIB_EXIT_ERROR:** CALIB_EXIT_ERROR: If set, indicates that the last calibration cycle exited due to an error condition.
6:5	0x0 RO	**RSVD_6_5:** Reserved
4:0	0xc RO	**CSI_RCOMP_CALIBRATION_VALUE:** MIPI CSI RCOMP value from last calibration cycle

5.6.31 MIPI CSI RCOMP control register (IUNIT_RCOMP_CONTROL)—Offset F4h

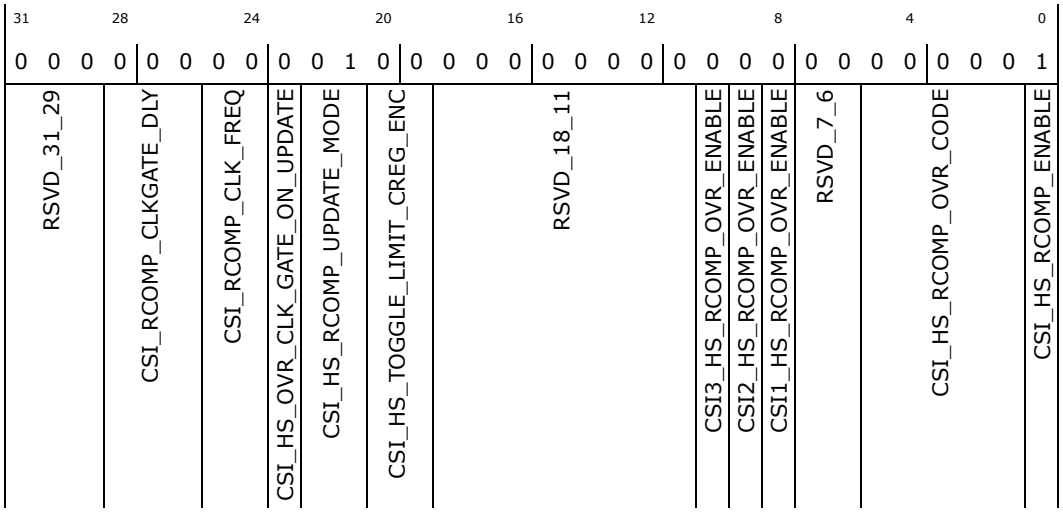
MIPI CSI RCOMP control register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + F4h

Default: 00200001h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**RSVD_31_29:** Reserved
28:26	0x0 RW	**CSI_RCOMP_CLKGATE_DLY:** CSI_RCOMP_CLKGATE_DLY: Number of CSI byte clocks to wait for after the data lanes go into LP11 state and before gating the HS or byte clock when RCOMP update is happening.
25:24	0x0 RW	**CSI_RCOMP_CLK_FREQ:** CSI_RCOMP_CLK_FREQ: Bandgap/RCOMP clock frequency. 0h=)20MHz; 1h=)15MHz; 2h=)10MHz; 3h=)reserved. At the start of each RCOMP calibration cycle, the state machine waits for 8 clock cycle before starting to sample the count up/down signal.
23	0x0 RW	**CSI_HS_OVR_CLK_GATE_ON_UPDATE:** CSI_HS_OVR_CLK_GATE_ON_UPDATE: If cleared, the high speed clock going to the digital logic is gated when RCOMP update is happening. The clock is gated for a minimum of 100 nsec. If this bit is set, then the high speed clock is not gated during the update cycle.
22:21	0x1 RW	**CSI_HS_RCOMP_UPDATE_MODE:** CSI_HS_RCOMP_UPDATE_MODE: 00b = RCOMP is updated if the clock lane is in LP11 state. 01b = RCOMP is updated if all the data lanes are in LP11 state. 10b = RCOMP is updated immediately after calibration is completed, or the CSI[1-3]_HS_RCOMP_OVR_ENABLE bits are written to 1 by software. 11b = Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20:19	0x0 RW	**CSI_HS_TOGGLE_LIMIT_CREG_ENC:** CSI_HS_TOGGLE_LIMIT_CREG_ENC: HS state machine toggle limit. Number of times RCOMP state machine will toggle before exiting. 2'b00: 6 toggles; 2'b01: 4 toggles; 2'b10: 8 toggles; 2'b11: 10 toggles;
18:11	0x0 RW	**RSVD_18_11:** Reserved
10	0x0 RW	**CSI3_HS_RCOMP_OVR_ENABLE:** CSI3_HS_RCOMP_OVR_ENABLE: If set, then the CSI_HS_RCOMP_OVRD field is used as the RCOMP value during the update cycle for CSI port 3. If clear, then the output of the RCOMP calibration engine (stored in CSI_RCOMP_CALIBRATION_VALUE field of IUNIT_RCOMP_STATUS register) is used as the RCOMP value during the update cycle for CSI port 3.
9	0x0 RW	**CSI2_HS_RCOMP_OVR_ENABLE:** CSI2_HS_RCOMP_OVR_ENABLE: If set, then the CSI_HS_RCOMP_OVRD field is used as the RCOMP value during the update cycle for CSI port 2. If clear, then the output of the RCOMP calibration engine (stored in CSI_RCOMP_CALIBRATION_VALUE field of IUNIT_RCOMP_STATUS register) is used as the RCOMP value during the update cycle for CSI port 2.
8	0x0 RW	**CSI1_HS_RCOMP_OVR_ENABLE:** CSI1_HS_RCOMP_OVR_ENABLE: If set, then the CSI_HS_RCOMP_OVRD field is used as the RCOMP value during the update cycle for CSI port 1. If clear, then the output of the RCOMP calibration engine (stored in CSI_RCOMP_CALIBRATION_VALUE field of IUNIT_RCOMP_STATUS register) is used as the RCOMP value during the update cycle for CSI port 1.
7:6	0x0 RW	**RSVD_7_6:** Reserved
5:1	0x0 RW	**CSI_HS_RCOMP_OVR_CODE:** CSI_HS_RCOMP_OVR_CODE: Software defined value to use as the RCOMP value for CSI[1-3] ports if the CSI[1-3]_HS_RCOMP_OVR_ENABLE fields are set.
0	0x1 RW	**CSI_HS_RCOMP_ENABLE:** CSI_HS_RCOMP_ENABLE: Enable CSI HS RCOMP. (Note: This bit does not affect the initial RCOMP at the de-assertion of reset which is controlled by the fuse FB_disable_initial_RCOMP.)

5.6.32 IUNIT Status Register (IUNIT_STATUS)—Offset F8h

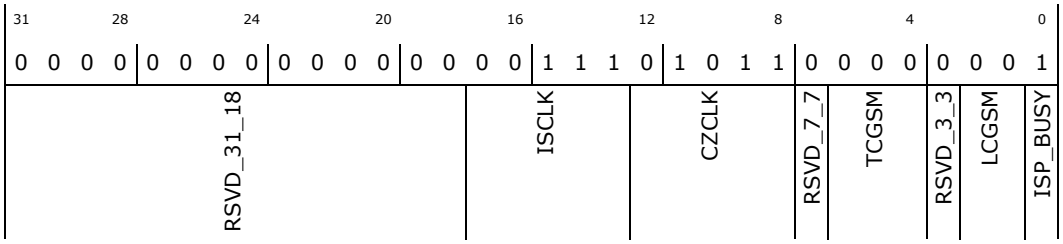
IUNIT Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + F8h

Default: 0000EB01h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0x0 RO	**RSVD_31_18:** Reserved
17:13	0x7 RO	**ISCLK:** Reflects the value of cck_isp_isclk_ratio_zcznfwh input pin.
12:8	0xb RO	**CZCLK:** Reflects the value of cck_xxx_czclk_ratio_zcznfwh input pin.
7	0x0 RO	**RSVD_7_7:** Reserved
6:4	0x0 RO	**TCGSM:** ISP trunk clock gating state machine. 0h = RUN_TRUNK_CLK; 1h = STOP_TRUNK_CLK; 2h = WAIT_FOR_RESUME; 3h = START_TRUNK_CLK; 4h = WAIT_FOR_LOCAL_CLK_TO_START. The reset value will be RUN_TRUNK_CLK. If the FB_override_initial_clock_gating fuse is not set, then shortly after reset, the value of this register will automatically change to STOP_TRUNK_CLK.
3	0x0 RO	**RSVD_3_3:** Reserved
2:1	0x0 RO	**LCGSM:** ISP local clock gating state machine. 0h = RUN_LOCAL_CLK; 1h = WAIT_FOR_FIFO_EMPTY; 2h = STOP_LOCAL_CLK. The reset value will be RUN_LOCAL_CLK. If the FB_override_initial_clock_gating fuse is not set, then shortly after reset, the value of this register will automatically change to STOP_LOCAL_CLK.
0	0x1 RO	**ISP_BUSY:** ISP_BUSY: 1 = ISP is busy; 0 = ISP is idle.

5.6.33 IUNIT Control Register (IUNIT_CONTROL)—Offset FCh

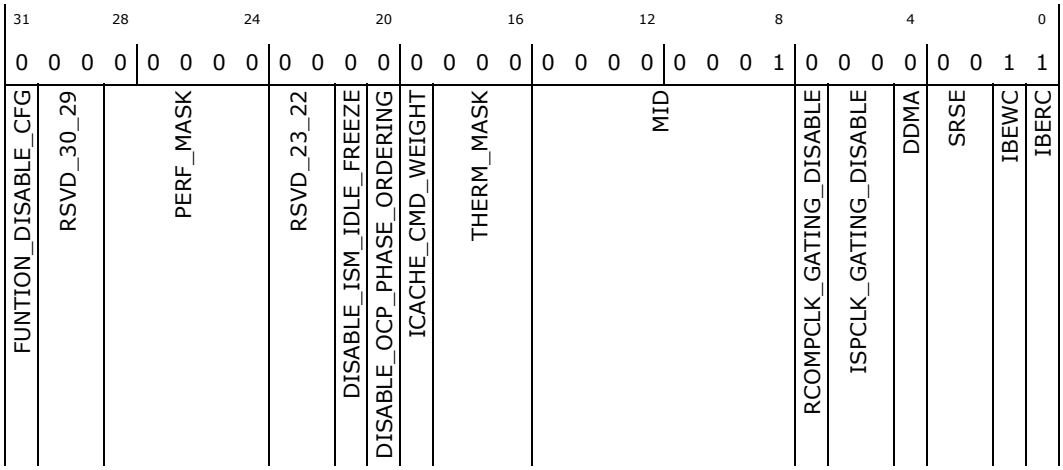
IUNIT Control Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:3, F:0] + FCh

Default: 00000103h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**FUNTION_DISABLE_CFG:** FUNCTION_DISABLE_INT: When set, both legacy and MSI interrupts are disabled.
30:29	0x0 RW	**RSVD_30_29:** Reserved
28:24	0x0 RW	**PERF_MASK:** PERF_MASK: This field determines the amount of performance throttling applied to ispclk. The value of this field determines how many beat periods of ispclk are killed, where a beat period is defined as 16 ispclk cycles. A 16 cycle period was chosen to make the throttling independent of the actual clock ratio between ispclk and coreclk. Note that clock gating should be enabled when thermal throttling is enabled.
23:22	0x0 RW	**RSVD_23_22:** Reserved
21	0x0 RW	**DISABLE_ISM_IDLE_FREEZE:** DISABLE_ISM_IDLE_FREEZE: When IUNIT receive a RESET_WARN message from PUNIT, it will freeze the IOSF primary Idle State Machine (among other things), before sending an OK_TO_RESET message to PUNIT. If the DISABLE_ISM_IDLE_FREEZE bit is set, IUNIT will not freeze the ISM in the IDLE state as part of this reset sequence.
20	0x0 RW	**DISABLE_OCP_PHASE_ORDERING:** DISABLE_OCP_PHASE_ORDERING: By default, IUNIT will follow the OCP phase ordering protocol and wait until a write command is accepted before accepting the write data corresponding to that command. If the DISABLE_OCP_PHASE_ORDERING bit is set, the IUNIT wrapper will accept the write data independent of the write command.
19	0x0 RW	**ICACHE_CMD_WEIGHT:** ICACHE_CMD_WEIGHT: 0b = Requests from the OCP master port sending Icache miss traffic will win arbitration over requests from the OCP master port that sends pixel data traffic. 1b = Requests from the two OCP master interfaces will be accepted in a round robin fashion.

Bit Range	Default & Access	Field Name (ID): Description
18:16	0x0 RW	**THERM_MASK:** THERM_MASK: This field determines the amount of thermal throttling applied to ispclk. The value of this field determines how many beat periods of ispclk are killed, where a beat period is defined as 16 ispclk cycles. A 16 cycle period was chosen to make the throttling independent of the actual clock ratio between ispclk and coreclk. 000 = No throttling; 001 = 12.5% throttling; 010 = 25% throttling; 011 = 37.5% throttling; 100 = 50% throttling; 101 = 62.5% throttling; 110 = 75% throttling; 111 = 87.5% throttling;
15:8	0x1 RW	**MID:** MIN_IDLE_DELAY: Minimum wait time after the rising edge of idle, before the clock gating state machine will start the sequence to gate ispclk. Range is 0 to 130 usec. Unit is 0.512 usec. Reset value of 8'h1 indicates MID = 0.512 usec.
7	0x0 RW	**RCOMPCLK_GATING_DISABLE:** 1 = Disable clock gating for rcompclk. 0 = Enable clock gating for rcompclk. Note: All clock gating is disabled by hardware while reset is asserted, regardless of the state of this field.
6:5	0x0 RW	**ISPCLK_GATING_DISABLE:** ISPCLK_GATING_DISABLE: 11 = Disable local clock gating and trunk clock gating for ispclk.; 10 = Enable local clock gating for ispclk, but disable trunk clock gating.; 01 = Reserved; 00 = Enable local clock gating and trunk clock gating for ispclk. Note: All clock gating is disabled by hardware while reset is asserted, regardless of the state of this field.
4	0x0 RW	**DDMA:** 1 = Disable DMA. Stop sending any requests on the IB PFI port. 0 = Enable DMA. IB PFI port operates normally.
3:2	0x0 RW	**SRSE:** SOFT_RESET_SEQUENCE_ENABLE: If SRSE=2b00: When an IUNIT_RESET_WARN message is received from PUNIT, IUNIT will a) stop accepting requests on the IOSF primary interface, b) stop accepting new requests from the OCP master interface, c) wait until read data from all earlier read requests received from the OCP master interface have been returned by SSA, d) wait until SSA reads data for all earlier PFI write requests, and e) wait for all DPHY lanes to enter stop state (LP11), and then f) send an IUNIT_OK_TO_RESET posted message to PUNIT. If SRSE=2b01: When an IUNIT_RESET_WARN message is received from PUNIT, IUNIT will a) stop accepting requests on the IOSF primary interface, b) stop accepting new requests from the OCP master interface, c) wait until read data from all earlier read requests received from the OCP master interface have been returned by SSA, d) wait until SSA reads data for all earlier PFI write requests, and then e) send an IUNIT_OK_TO_RESET posted message to PUNIT. If SRSE=2b10: When an IUNIT_RESET_WARN message is received from PUNIT, IUNIT will wait for all DPHY lanes to enter stop state (LP11), and then send an IUNIT_OK_TO_RESET posted message to PUNIT. If SRSE=2b11: When an IUNIT_RESET_WARN message is received from PUNIT, IUNIT will immediately send an IUINT_OK_TO_RESET posted message to PUNIT.
1	0x1 RW	**IBEWC:** IB_ENABLE_WRITE_COMBINING: When set, enables the combining of adjacent 32-byte write requests to the same cache line. When cleared, each 32-byte write request is sent as a separate request on the IB interface.
0	0x1 RW	**IBERC:** IB_ENABLE_READ_COMBINING: When set, enables the combining of adjacent 32-byte read requests to the same cache line. When cleared, each 32-byte read request is sent as a separate request on the IB interface.

§

6 SoC Storage

6.1 SDIO PCI Configuration Registers

Table 32. Summary of SDIO PCI Configuration Registers—0/16/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 1901	22948086h
4–7h	4	"Status and Command Register (STATUSCOMMAND)—Offset 4h" on page 1901	00100000h
8–Bh	4	"Revision ID and Class Code Register (REVCLASSCODE)—Offset 8h" on page 1902	00000000h
C–Fh	4	"Cache Line Latency Header and BIST Register (CLLATHEADERBIST)—Offset Ch" on page 1903	00000000h
10–13h	4	"Base Address Register low (BAR)—Offset 10h" on page 1904	00000000h
14–17h	4	"Base Address Register high (BAR_HIGH)—Offset 14h" on page 1904	00000000h
18–1Bh	4	"Base Address Register1 low (BAR1)—Offset 18h" on page 1905	00000000h
1C–1Fh	4	"Base Address Register1 high (BAR1_HIGH)—Offset 1Ch" on page 1906	00000000h
2C–2Fh	4	"Subsystem Vendor and Subsystem ID Register (SUBSYSTEMID)—Offset 2Ch" on page 1906	00000000h
30–33h	4	"EXPANSION ROM base address Register (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 1907	00000000h
34–37h	4	"Capabilities Pointer Register (CAPABILITYPTR)—Offset 34h" on page 1907	00000080h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 1908	00000100h
80–83h	4	"PowerManagement Capability ID Register (POWERCAPID)—Offset 80h" on page 1909	48030001h
84–87h	4	"Power Management Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 1909	00000008h
A0–A3h	4	"General Purpose Read Write Register1 (GEN_REGRW1)—Offset A0h" on page 1910	00000000h
A4–A7h	4	"General Purpose Read Write Register2 (GEN_REGRW2)—Offset A4h" on page 1911	00000000h
A8–ABh	4	"General Purpose Read Write Register3 (GEN_REGRW3)—Offset A8h" on page 1911	00000000h
AC–AFh	4	"General Purpose Read Write Register4 (GEN_REGRW4)—Offset ACh" on page 1912	00000000h
C0–C3h	4	"General Purpose Input Register (GEN_INPUT_REG)—Offset C0h" on page 1912	00000000h
F8–FBh	4	"Manufacturers ID Register (MANID)—Offset F8h" on page 1913	00000000h

6.1.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

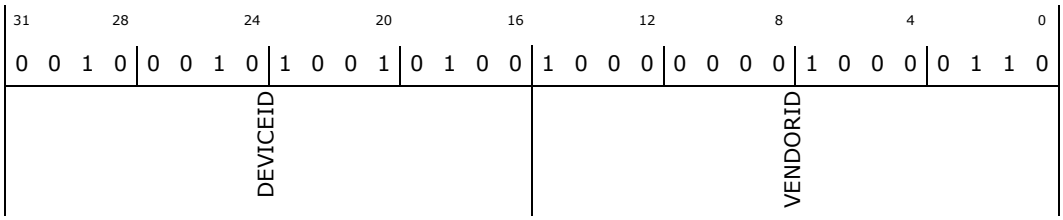
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + 0h

Default: 22948086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x2294 RO	**DEVICEID:** Device ID identifies the particular PCI device. The Default value is taken from a strap at the top level. SetIDValue message updates 15:7 of this strap. Value shown below is after SetIDValue from CHV_RevIdDevId_HAS: SDIO1(smmc) : 16'h2294 SDIO2(sdio) : 16'h2295 SDIO3(sdcard) : 16'h2296
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by the PCI SIG, which identifies the manufacturer of the device. This is tied to a strap the top level.

6.1.2 Status and Command Register (STATUSCOMMAND)—Offset 4h

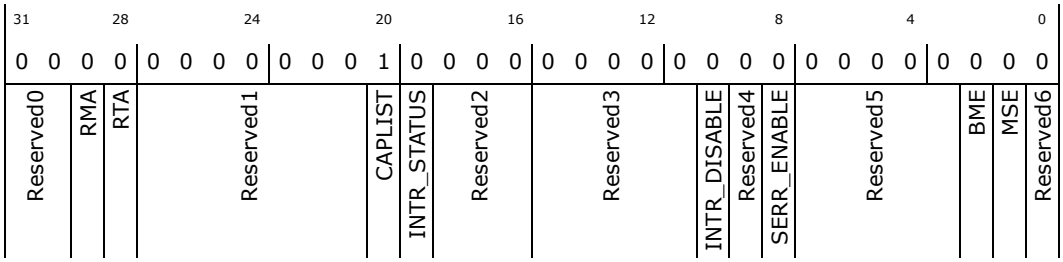
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved0:** Reserved, [30]: Signaled System Error, Not implemented
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, the Bridge sets this bit.
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, the Bridge sets this bit.
27:21	0x0 RO	**Reserved1:** Reserved, [27]: Signaled Target Abort: Not implemented
20	0x1 RO	**CAPLIST:** Capabilities List: Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at the configuration offset 34h.
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, is the device/function interrupt message sent. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, which is the Bridge does not send Interrupt Assert message through the IOSF Sideband Channel. Reset value of this bit is 0. This bit has no connection with the interrupt status bit.
9	0x0 RO	**Reserved4:** Reserved
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: Not implemented
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0,the Bridge does not generate any new upstream transaction on IOSF as a master.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge response to downstream memory accesses. When set, accesses to memory space of the device is enabled.
0	0x0 RO	**Reserved6:** Reserved

6.1.3 Revision ID and Class Code Register (REVCLASSCODE)—Offset 8h

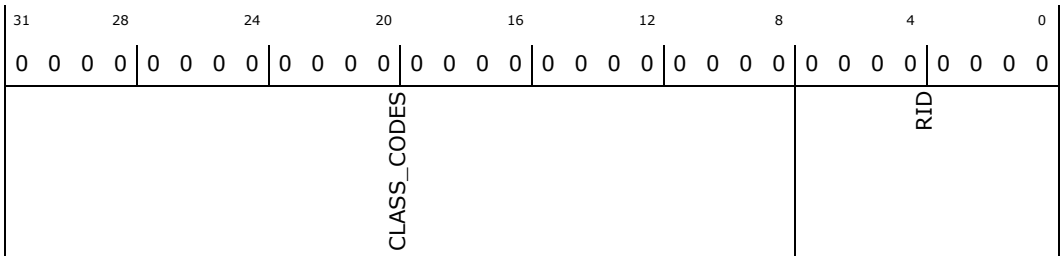
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** The Class Code register is read-only and is used to identify the generic function of the device, and in some cases, a specific register-level programming interface. The register is broken into 3 Byte-size fields. 1. The upper Byte (at offset 0Bh) is a base class code that broadly classifies the type of function the device performs. 2. The middle Byte (at offset 0Ah) is a sub-class code that identifies more specifically the function of the device. 3. The lower Byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular PCI device. The default value comes from a strap. A SetIDValue message updates this value.

6.1.4 Cache Line Latency Header and BIST Register (CLLATHEADERBIST)—Offset Ch

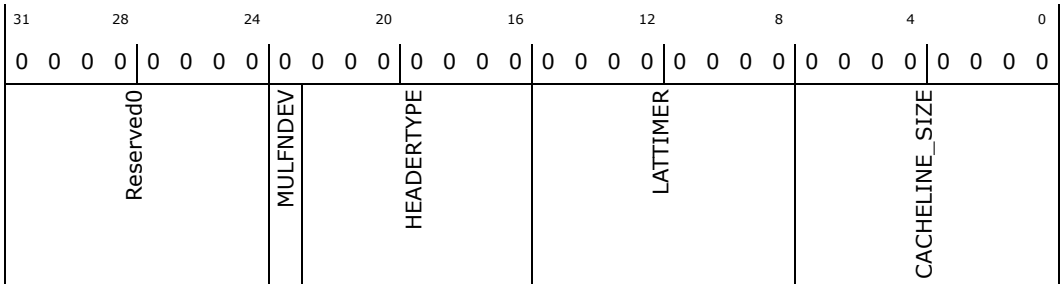
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x0 RO	**MULFNDEV:** Multi-Function Device: This bit is 0 to indicate Single Function Device

Bit Range	Default & Access	Field Name (ID): Description
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header
15:8	0x0 RO	**LATTIMER:** Latency Timer
7:0	0x0 RW	**CACHELINE_SIZE:** Cacheline Size: This register is implemented as R/W with default as 0. Similar to other Intel IPs.

6.1.5 Base Address Register low (BAR)—Offset 10h

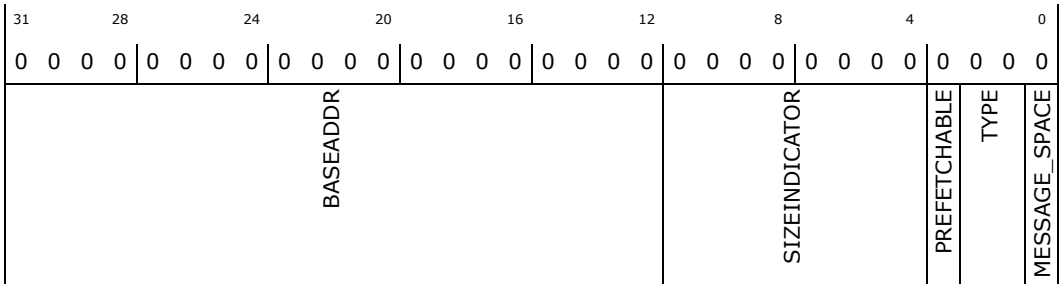
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the OCP fabric memory space. bit [31] is always read write as Bridge expects the size of the device to be limited to 2G Taken from Strap values as ones.
11:4	0x0 RO	**SIZEINDICATOR:** Always is 0, as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0x0 RO	**TYPE:** Type: If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

6.1.6 Base Address Register high (BAR_HIGH)—Offset 14h

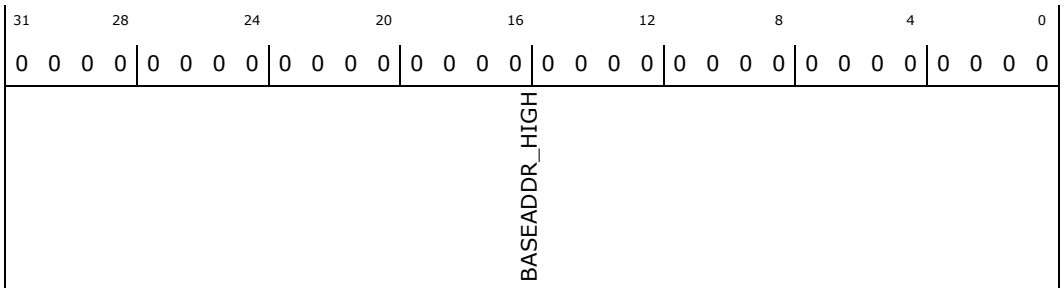
BAR -Base Address Register High

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**BASEADDR_HIGH:** High 32 bits for BAR, RO as SCC is set to 32 bits only

6.1.7 Base Address Register1 low (BAR1)—Offset 18h

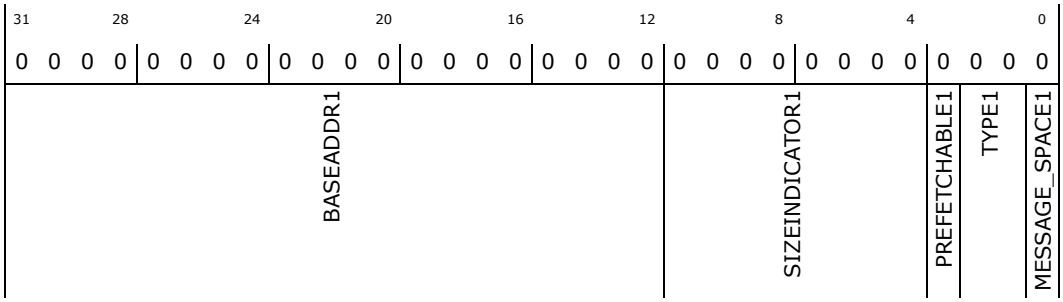
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + 18h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: This field is present if BAR1 is enabled through private configuration space.
11:4	0x0 RO	**SIZEINDICATOR1:** Always is 0 as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0x0 RO	**TYPE1:** Type: If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0 Indicates this BAR is present in the memory space.

6.1.8 Base Address Register1 high (BAR1_HIGH)—Offset 1Ch

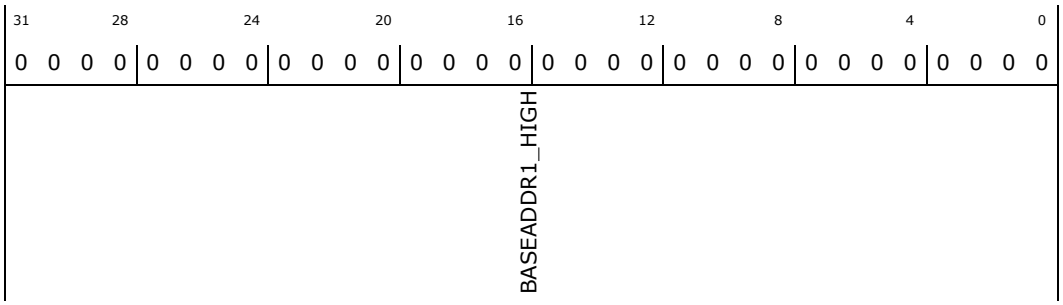
BAR1 -Base Address Register1 High

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + 1Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**BASEADDR1_HIGH:** High 32 bits for BAR1, RO as SCC is set to 32 bits only

6.1.9 Subsystem Vendor and Subsystem ID Register (SUBSYSTEMID)—Offset 2Ch

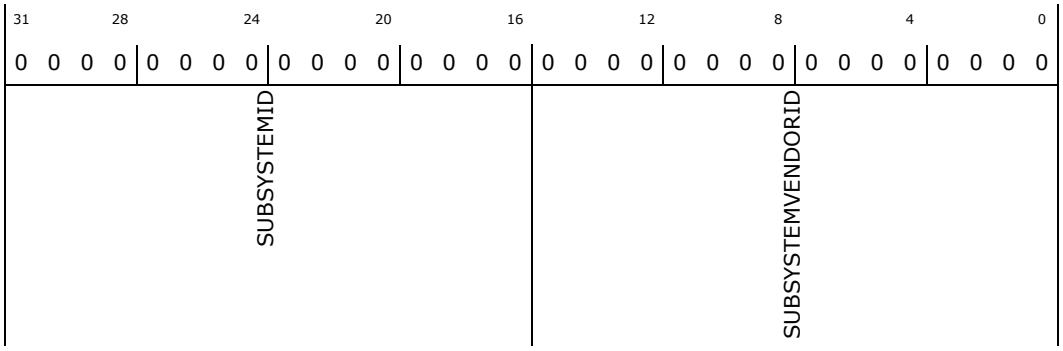
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

6.1.10 EXPANSION ROM base address Register (EXPANSION_ROM_BASEADDR)—Offset 30h

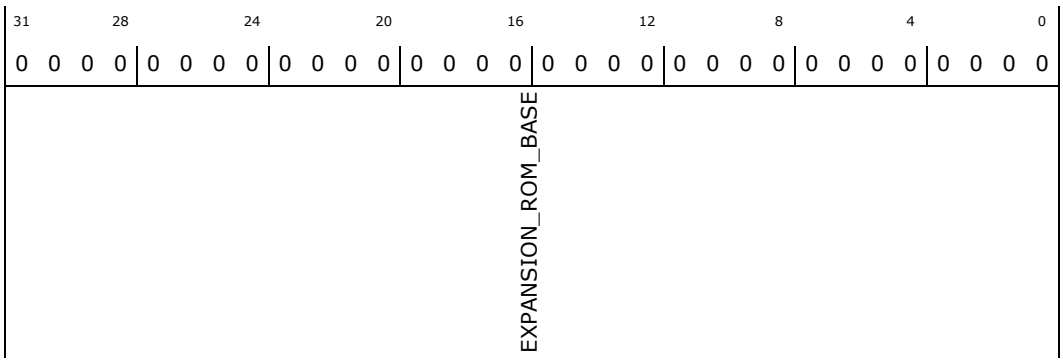
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** [31:11]-) Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM [10:1] -) Reserved [0] -) Expansion ROM Enable: Bridge does not have support for Expansion ROMs.

6.1.11 Capabilities Pointer Register (CAPABILITYPTR)—Offset 34h

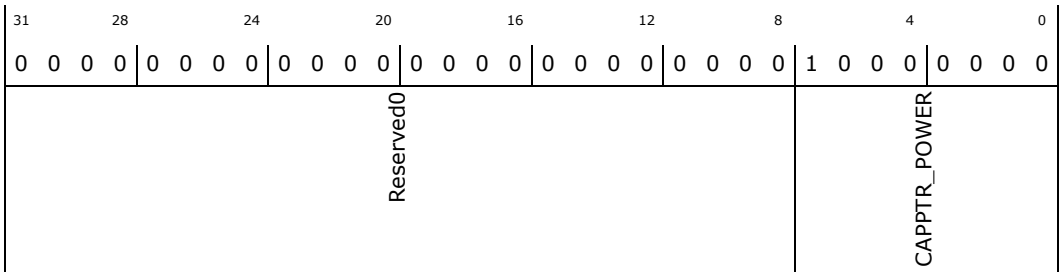
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + 34h

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x80 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability points to the PM Capability (0x80) structure.

6.1.12 Interrupt Register (INTERRUPTREG)—Offset 3Ch

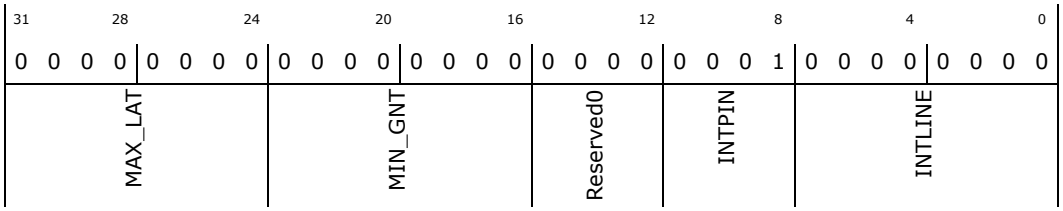
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space. For a single function device, this ideally is INTA.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

6.1.13 PowerManagement Capability ID Register (POWERCAPID)—Offset 80h

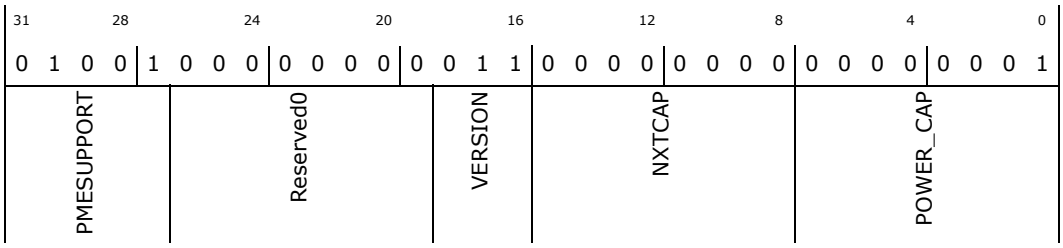
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + 80h

Default: 48030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x9 RO	**PMESUPPORT:** PME_Support: This 5-bit field indicates the power states in which the function can assert the PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal at the same time in that power state. bit(11) X XXX1b: PME# can be asserted from D0 bit(12) X XX1Xb: PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb: PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb:PME# can be asserted from D3hot bit(15) 1 XXXXb:PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the private configuration space PME_Support XORed with the PME_Support strap.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

6.1.14 Power Management Control and Status Register (PMECTRLSTATUS)—Offset 84h

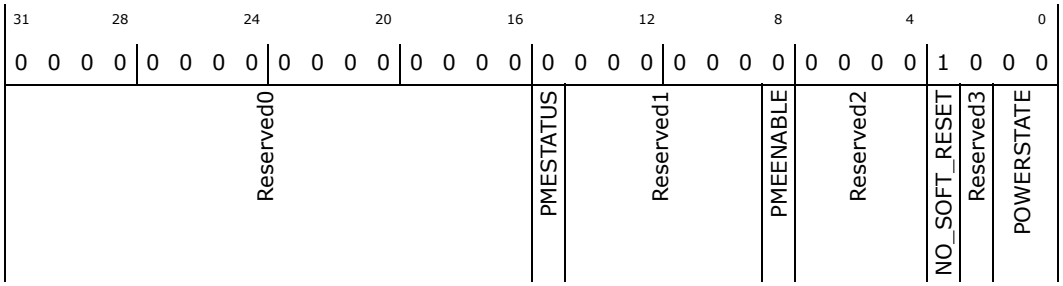
PMECTRLSTATUS: Power Management Control and Status

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 Software clears the bit by writing a 1 to it. 1 This bit is set when the PME# signal is asserted independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: 1 Enables the function to assert PME#. 0 PME# message on Sideband is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state and to set a new power state. The values are: 00 D0 state 11 D3HOT state Others Reserved Note: If the software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally. The data is discarded and no state change occurs. Note: When in the D3HOT states, interrupts are blocked. Note: D3Hot cannot be used for downstream decode on fabric ports.

6.1.15 General Purpose Read Write Register1 (GEN_REGRW1)—Offset A0h

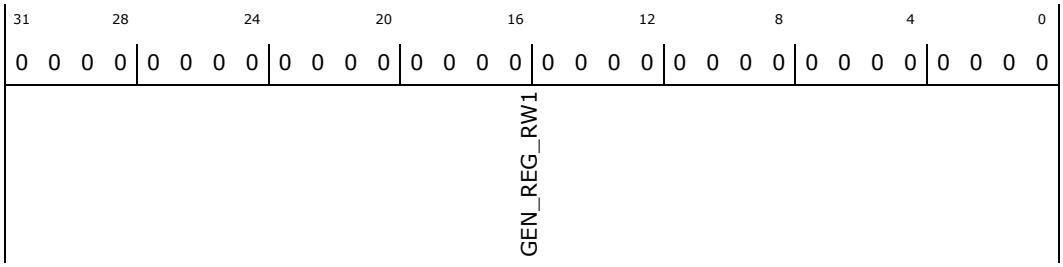
General Purpose Read Write Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW1:** General Purpose PCIRegister: This register value is brought out as oob_gen_pci_reg1 out of band signal

6.1.16 General Purpose Read Write Register2 (GEN_REGRW2)—Offset A4h

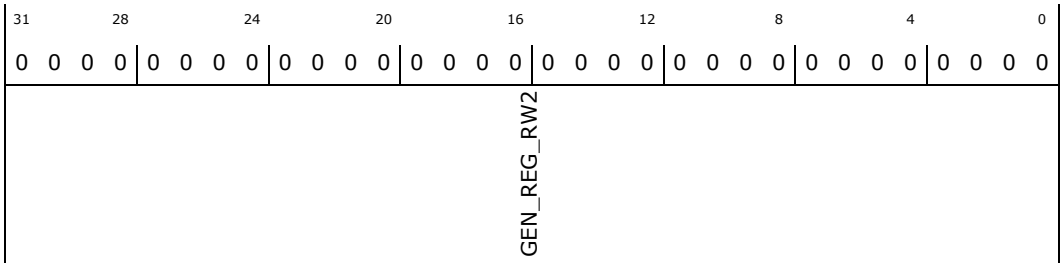
General Purpose Read Write Register2

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW2:** General Purpose PCI Register: This register value is brought out as oob_gen_pci_reg2 Out of Band signal

6.1.17 General Purpose Read Write Register3 (GEN_REGRW3)—Offset A8h

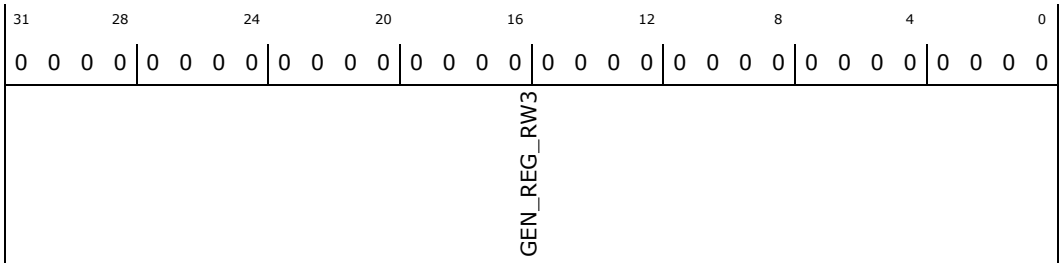
General Purpose Read Write Register3

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW3:** General Purpose PCI Register: This register value is brought out as oob_gen_pci_reg3 Out of Band signal

6.1.18 General Purpose Read Write Register4 (GEN_REGRW4)—Offset ACh

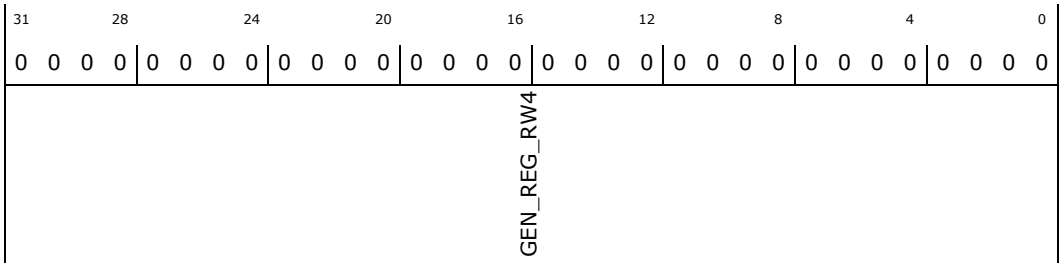
General Purpose Read Write Register4

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW4:** General Purpose PCI Register: This register value is brought out as oob_gen_pci_reg4 Out of Band signal

6.1.19 General Purpose Input Register (GEN_INPUT_REG)—Offset C0h

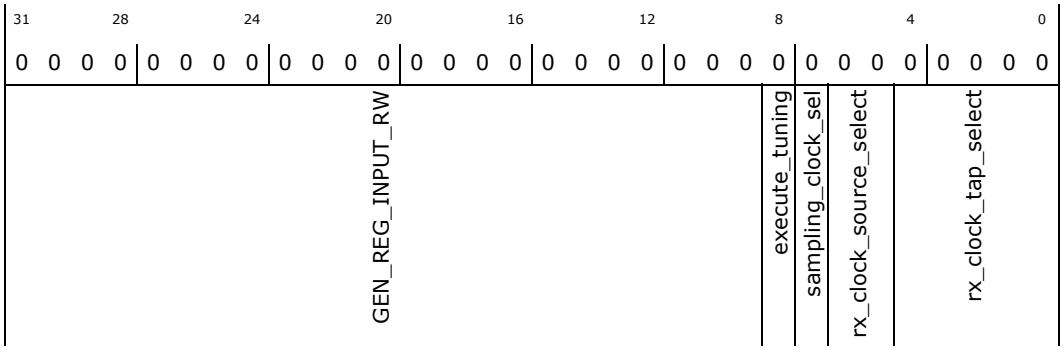
General Purpose Input Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**GEN_REG_INPUT_RW:** Reserved.
8	0x0 RO	**execute_tuning:** Execute Tuning. This is intended for debug use only.
7	0x0 RO	**sampling_clock_sel:** Sampling Clock Select. This is intended for debug use only.
6:5	0x0 RO	**rx_clock_source_select:** Rx Clock Source Select: 00: loopback clock 01: SDR50 10: DDR50 11: tuned clock This is intended only for debug use.
4:0	0x0 RO	**rx_clock_tap_select:** Rx Clock Tap Select: This indicates which tap select the host controller's tuning algorithm settled on. This is intended only for debug use.

6.1.20 Manufacturers ID Register (MANID)—Offset F8h

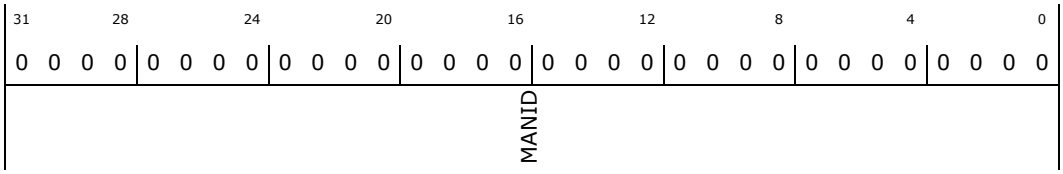
Manufacturers ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:16, F:0] + F8h

Default: 00000000h

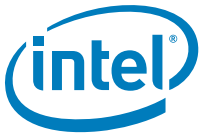


Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: Default value comes from straps. This value can be updated from SetIDValue Message

6.2 SDIO Memory Mapped I/O Registers

Table 33. Summary of SDIO Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"SDMA System Address Register (SYS_ADR)—Offset 0h" on page 1916	00000000h
4–5h	2	"Block Size Register (BLK_SIZE)—Offset 4h" on page 1916	0000h
6–7h	2	"Block Count Register (BLK_COUNT)—Offset 6h" on page 1917	0000h
8–Bh	4	"Argument Register (ARGUMENT)—Offset 8h" on page 1918	00000000h
C–Dh	2	"Transfer Mode Register (TX_MODE)—Offset Ch" on page 1918	0000h
E–Fh	2	"Command Register (CMD)—Offset Eh" on page 1919	0000h
10–13h	4	"Response Register0 (RESPONSE0)—Offset 10h" on page 1920	00000000h
14–17h	4	"Response Register2 (RESPONSE2)—Offset 14h" on page 1921	00000000h
18–1Bh	4	"Response Register4 (RESPONSE4)—Offset 18h" on page 1921	00000000h
1C–1Fh	4	"Response Register6 (RESPONSE6)—Offset 1Ch" on page 1922	00000000h
20–23h	4	"Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h" on page 1923	00000000h
24–27h	4	"Present State Register (PRE_STATE)—Offset 24h" on page 1923	1FFF0000h
28–28h	1	"Host Control Register (HOST_CTL)—Offset 28h" on page 1924	00h
29–29h	1	"Power Control Register (PWR_CTL)—Offset 29h" on page 1925	01h
2A–2Ah	1	"Block Gap Control Register (BLK_GAP_CTL)—Offset 2Ah" on page 1926	80h
2B–2Bh	1	"Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh" on page 1927	00h
2C–2Dh	2	"Clock Control Register (CLK_CTL)—Offset 2Ch" on page 1928	0000h
2E–2Eh	1	"Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh" on page 1928	00h
2F–2Fh	1	"Software Reset Register (SW_RST)—Offset 2Fh" on page 1929	00h
30–31h	2	"Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h" on page 1930	0000h
32–33h	2	"Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h" on page 1931	0000h
34–35h	2	"Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h" on page 1932	0000h
36–37h	2	"Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h" on page 1933	0000h
38–39h	2	"Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h" on page 1935	0000h
3A–3Bh	2	"Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah" on page 1936	0000h
3C–3Fh	4	"Auto CMD12 Error Status Register and Host control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch" on page 1937	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40–43h	4	"Capabilities Register (CAPABILITIES)—Offset 40h" on page 1939	446CC8B2h
44–47h	4	"Capabilities Register 2 (CAPABILITIES_2)—Offset 44h" on page 1939	00000007h
48–4Bh	4	"Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h" on page 1940	00000000h
50–51h	2	"Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h" on page 1941	0000h
52–53h	2	"Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h" on page 1942	0000h
54–54h	1	"ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h" on page 1943	00h
58–5Bh	4	"ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h" on page 1943	00000000h
5C–5Fh	4	"ADMA System Address Register (ADMA_SYS_ADDR_HIGH)—Offset 5Ch" on page 1944	00000000h
60–63h	4	"Preset Values registers (PRESET_VALUE_0)—Offset 60h" on page 1944	00040004h
64–67h	4	"Preset Values 1 registers (PRESET_VALUE_1)—Offset 64h" on page 1945	00040002h
68–6Bh	4	"Preset Values 2 registers (PRESET_VALUE_2)—Offset 68h" on page 1945	00010002h
6C–6Fh	4	"Preset Values 3 registers (PRESET_VALUE_3)—Offset 6Ch" on page 1946	00020000h
70–73h	4	"BOOT_TIMEOUT_CTRL (BOOT_TIMEOUT_CTRL)—Offset 70h" on page 1946	00000000h
74–74h	1	"DEBUG_SEL (DEBUG_SEL)—Offset 74h" on page 1947	00h
E0–E3h	4	"Shared Bus Control Register (SHARED_BUS)—Offset E0h" on page 1947	00000000h
F0–F0h	1	"SPI_INT_SUP (SPI_INT_SUP)—Offset F0h" on page 1948	00h
FC–FDh	2	"Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh" on page 1948	0000h
FE–FFh	2	"Host Controller Version Register (HOST_CTRL_VER)—Offset FEh" on page 1949	1002h

6.2.1 SDMA System Address Register (SYS_ADR)—Offset 0h

This register contains the physical system memory address used for DMA transfers

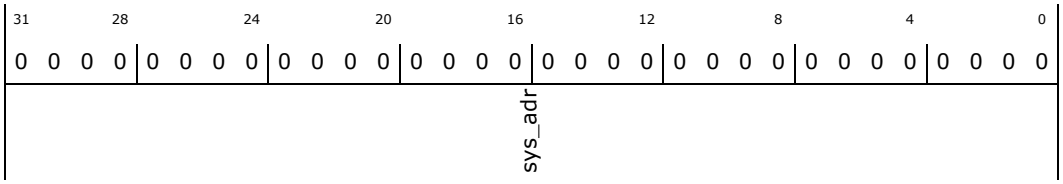
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SYS_ADR (sys_adr):** SDMA System Address This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value. The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at the every boundary specified by the Host SDMA Buffer Boundary in the Block Size register. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register (003h) is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by the Resume command or by setting Continue Request in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register. ADMA does not use this register.

6.2.2 Block Size Register (BLK_SIZE)—Offset 4h

This register is used to configure the number of bytes in a data block.

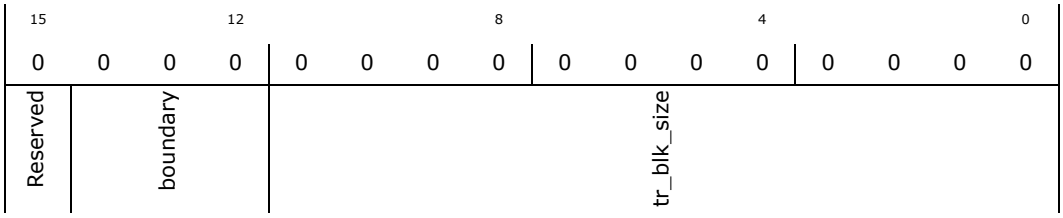
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**Reserved:** Reserved
14:12	0x0 RW	**BOUNDARY (boundary):** Host SDMA Buffer Boundary The large contiguous memory space may not be available in the virtual memory system. To perform long SDMA transfer, SDMA System Address register shall be updated at every system memory boundary during SDMA transfer. These bits specify the size of contiguous buffer in the system memory. The SDMA transfer shall wait at the every boundary specified by these fields and the Host Controller generates the DMA Interrupt to request the Host Driver to update the SDMA System Address register. At the end of transfer, the Host Controller may issue or may not issue DMA Interrupt. In particular, DMA Interrupt shall not be issued after Transfer Complete Interrupt is issued. In case of this register is set to 0 (buffer size = 4K bytes), lower 12-bit of byte address points data in the contiguous buffer and the upper 20-bit points the location of the buffer in the system memory. The SDMA transfer stops when the Host Controller detects carry out of the address from bit 11 to 12. These bits shall be supported when the SDMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. ADMA does not use this register. 000b - 4K bytes (Detects A11 carry out) 001b - 8K bytes (Detects A12 carry out) 010b - 16K Bytes (Detects A13 carry out) 011b - 32K Bytes (Detects A14 carry out) 100b - 64K bytes (Detects A15 carry out) 101b - 128K Bytes (Detects A16 carry out) 110b - 256K Bytes (Detects A17 carry out) 111b - 512K Bytes (Detects A18 carry out)
11:0	0x0 RW	**TR_BLK_SIZE (tr_blk_size):** Transfer Block Size This register specifies the block size of data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. Values ranging from 1 up to the maximum buffer size can be set. In case of memory, it shall be set up to 512 bytes (Refer to Implementation Note in Section 1.7.2). It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value, and write operations shall be ignored. 0800h 2048 Bytes ... ... 0200h 512 Bytes 01FFh 511 Bytes ... ... 0004h 4 Bytes 0003h 3 Bytes 0002h 2 Bytes 0001h 1 Byte 0000h No data transfer

6.2.3 Block Count Register (BLK_COUNT)—Offset 6h

This register is used to configure the number of data blocks

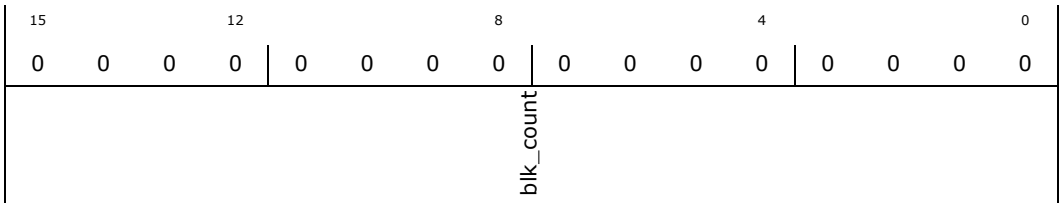
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 6h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW	**BLK_COUNT (blk_count):** Blocks Count For Current Transfer This register is enabled when Block Count Enable in the Transfer Mode register is set to 1 and is valid only for multiple block transfers

6.2.4 Argument Register (ARGUMENT)—Offset 8h

This register contains the SD Command Argument.

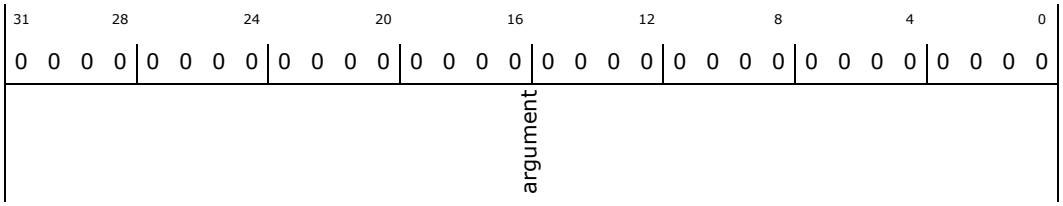
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**ARGUMENT (argument):** Command Argument The SD Command Argument is specified as bit39-8 of Command-Format in the Physical Layer Specification.

6.2.5 Transfer Mode Register (TX_MODE)—Offset Ch

Transfer Mode Register

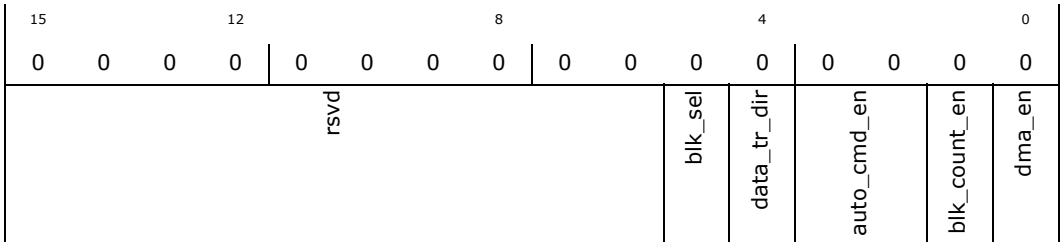
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:6	0x0 RO	**RSVD (rsvd):** Reserved
5	0x0 RW	**BLK_SEL (blk_sel):** Multi / Single Block Select This bit is set when issuing multiple-block transfer commands using DAT line. For any other commands, this bit shall be set to 0. If this bit is 0, it is not necessary to set the Block Count register. (Refer to Table 2-8) 1 Multiple Block 0 Single Block
4	0x0 RW	**Data_TR_Dir (data_tr_dir):** Data Transfer Direction Select This bit defines the direction of DAT line data transfers. The bit is set to 1 by the Host Driver to transfer data from the SD card to the SD Host Controller and it is set to 0 for all other commands. 1 Read (Card to Host) 0 Write (Host to Card)
3:2	0x0 RW	**AUTO_CMD_EN (auto_cmd_en):** This field determines use of auto command functions 00b - Auto Command Disabled 01b - Auto CMD12 Enable 10b - Auto CMD23 Enable 11b - Reserved
1	0x0 RW	**BLK_COUNT_EN (blk_count_en):** Block Count Enable This bit is used to enable the Block Count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. (Refer to Table 2-8) If ADMA2 data transfer is more than 65535 blocks, this bit shall be set to 0. In this case, data transfer length is designated by Descriptor Table. 1 Enable 0 Disable
0	0x0 RW	**DMA_EN (dma_en):** DMA Enable This bit enables DMA functionality as described in section 1.4. DMA can be enabled only if it is supported as indicated in the Capabilities register. One of the DMA modes can be selected by DMA Select in the Host Control register. If DMA is not supported, this bit is meaningless and shall always read 0. If this bit is set to 1, a DMA operation shall begin when the Host Driver writes to the upper byte of Command register (00Fh). 1 DMA Data transfer 0 No data transfer or Non DMA data transfer

6.2.6 Command Register (CMD)—Offset Eh

Command Register

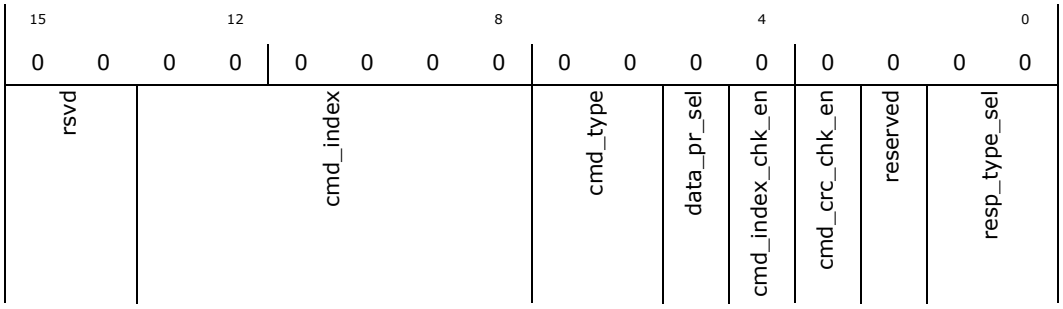
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RO	**RSVD (rsvd):** Reserved
13:8	0x0 RW	**CMD_INDEX (cmd_index):** Command Index These bits shall be set to the command number (CMD0-63, ACMD0-63) that is specified in bits 45-40 of the Command-Format in the Physical Layer Specification and SDIO Card Specification.
7:6	0x0 RW	**CMD_TYPE (cmd_type):** Command Type
5	0x0 RW	**DATA_PR_SEL (data_pr_sel):** Data Present Select This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. It is set to 0 for the following: (1) Commands using only CMD line (ex. CMD52). (2) Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b ex. CMD38) (3) Resume command 1 Data Present 0 No Data Present
4	0x0 RW	**CMD_INDEX_CHK_EN (cmd_index_chk_en):** Command Index Check Enable If this bit is set to 1, the Host Controller shall check the Index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked. 1 Enable 0 Disable
3	0x0 RW	**CMD_CRC_CHK_EN (cmd_crc_chk_en):** Command CRC Check Enable If this bit is set to 1, the Host Controller shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. The position of CRC field is determined according to the length of the response. (Refer to definition in D01-00 and Table 2-10 below.) 1 Enable 0 Disable
2	0x0 RO	**Reserved (reserved):** Reserved
1:0	0x0 RW	**RESP_TYPE_SEL (resp_type_sel):** Response Type Select 00 No Response 01 Response Length 136 10 Response Length 48 11 Response Length 48 check Busy after response

6.2.7 Response Register0 (RESPONSE0)—Offset 10h

This register is used to store responses from SD cards

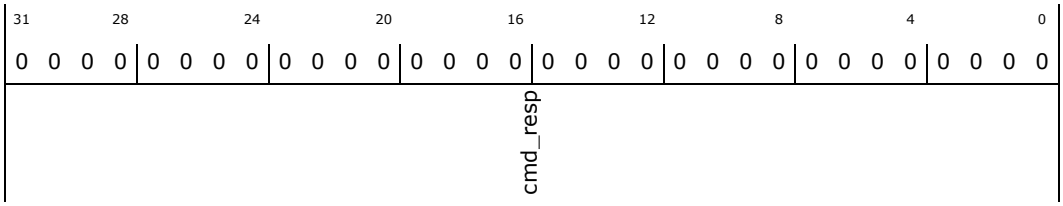
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**CMD_RESP0 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

6.2.8 Response Register2 (RESPONSE2)—Offset 14h

This register is used to store responses from SD cards

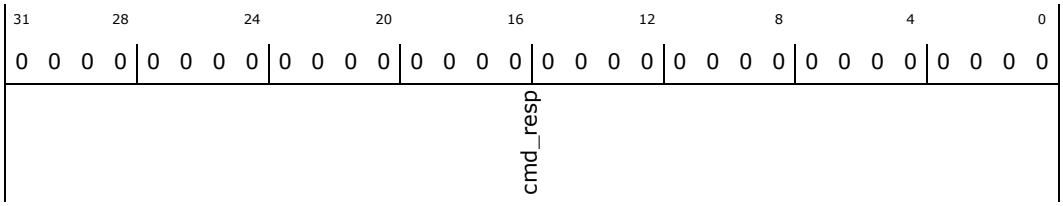
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**CMD_RESP2 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

6.2.9 Response Register4 (RESPONSE4)—Offset 18h

This register is used to store responses from SD cards

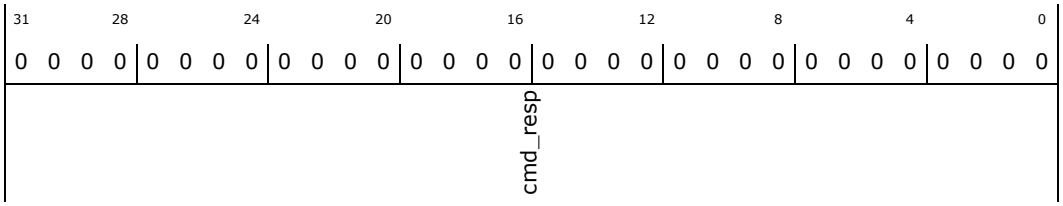
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**CMD_RESP4 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

6.2.10 Response Register6 (RESPONSE6)—Offset 1Ch

This register is used to store responses from SD cards

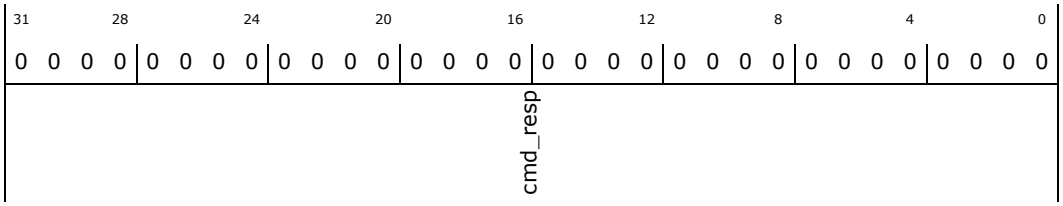
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**CMD_RESP6 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

6.2.11 Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h

32-bit data port register to access internal buffer

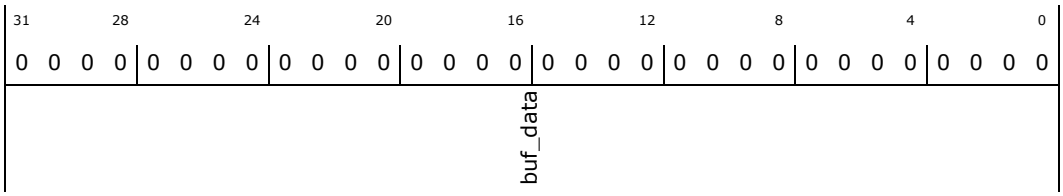
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**BUF_DATA (buf_data):** Buffer Data The Host Controller buffer can be accessed through this 32-bit Data Port register. RW depends on read or write transfer, it doesn't mean what's written can be read back

6.2.12 Present State Register (PRE_STATE)—Offset 24h

The Host Driver can get status of the Host Controller from this 32-bit read only register

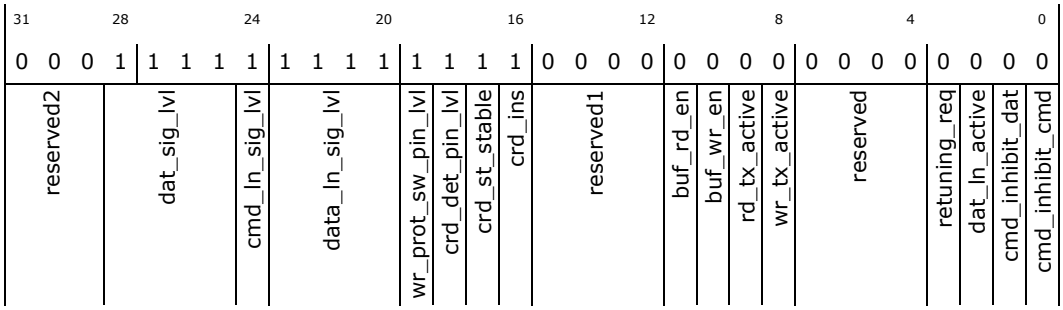
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 1FFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**Reserved2 (reserved2):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
28:25	0xf RO	**DAT_SIG_LVL (dat_sig_lvl):** This status is used to check DAT line level to recover from errors, and for debugging. D28 - DAT[7] D27 - DAT[6] D26 - DAT[5] D25 - DAT[4]
24	0x1 RO	**CMD_LN_SIG_LVL (cmd_ln_sig_lvl):** CMD Line Signal Level This status is used to check the CMD line level to recover from errors, and for debugging.
23:20	0xf RO	**DATA_LN_SIG_LVL (data_ln_sig_lvl):** DAT[3:0] Line Signal Level This status is used to check the DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. D23 DAT[3] D22 DAT[2] D21 DAT[1] D20 DAT[0]
19	0x1 RO	**WR_PROT_SW_PIN_LVL (wr_prot_sw_pin_lvl):** Write Protect Switch Pin Level
18	0x1 RO	**CRD_DET_PIN_LVL (crd_det_pin_lvl):** Card Detect Pin Level
17	0x1 RO	**CRD_ST_STABLE (crd_st_stable):** Card State Stable
16	0x1 RO	**CRD_INS (crd_ins):** Card Inserted
15:12	0x0 RO	**Reserved1 (reserved1):** Reserved
11	0x0 RO	**BUF_RD_EN (buf_rd_en):** Buffer Read Enable
10	0x0 RO	**BUF_WR_EN (buf_wr_en):** Buffer Write Enable
9	0x0 RO	**RD_TX_ACTIVE (rd_tx_active):** Read Transfer Active
8	0x0 RO	**WR_TX_ACTIVE (wr_tx_active):** Write Transfer Active
7:4	0x0 RO	**Reserved (reserved):** Reserved
3	0x0 RO	**RETUNING_REQ (retuning_req):** Re-Tuning Request
2	0x0 RO	**DAT_LN_ACTIVE (dat_ln_active):** DAT Line Active
1	0x0 RO	**CMD_INHIBIT_DAT (cmd_inhibit_dat):** Command Inhibit (DAT)
0	0x0 RO	**CMD_INHIBIT_CMD (cmd_inhibit_cmd):** Command Inhibit (CMD)

6.2.13 Host Control Register (HOST_CTL)—Offset 28h

Host Control Register

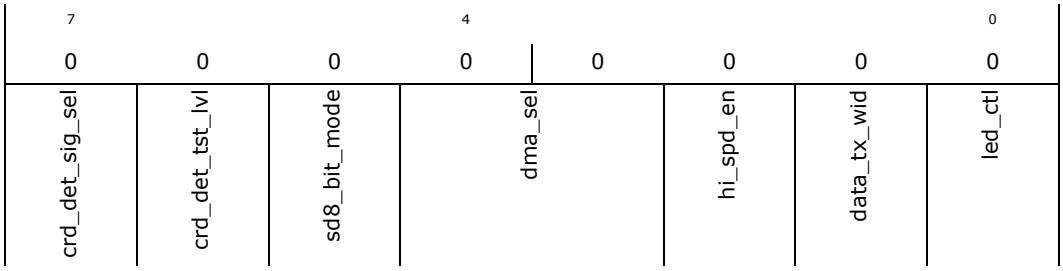
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW	**CRD_DET_SIG_SEL (crd_det_sig_sel):** Card Detect Signal Selection
6	0x0 RW	**CRD_DET_TST_LVL (crd_det_tst_lvl):** Card Detect Test Level
5	0x0 RW	**SD8_BIT_MODE (sd8_bit_mode):** This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card.
4:3	0x0 RW	**DMA_SEL (dma_sel):** DMA Select
2	0x0 RW	**HI_SPD_EN (hi_spd_en):** High Speed Enable
1	0x0 RW	**DATA_TX_WID (data_tx_wid):** Data Transfer Width
0	0x0 RW	**LED_CTL (led_ctl):** LED Control

6.2.14 Power Control Register (PWR_CTL)—Offset 29h

Power Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 29h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 01h

7			4				0
0	0	0	0	0	0	0	1
rsvd			hw_rst	sd_bus_volt_sel			sd_bus_pwr

Bit Range	Default & Access	Field Name (ID): Description
7:5	0x0 RO	**RSVD (rsvd):** Reserved
4	0x0 RW	**HW_rst (hw_rst):** HW reset
3:1	0x0 RW	**SD_BUS_VOLT_SEL (sd_bus_volt_sel):** SD Bus Voltage Select
0	0x1 RW	**SD_BUS_PWR (sd_bus_pwr):** SD Bus Power

6.2.15 Block Gap Control Register (BLK_GAP_CTL)—Offset 2Ah

Block Gap Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 2Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
boot_ack_chk	alt_boot_en	boot_en	spi_mode	int_blk_gap	rd_wait_ctl	cont_req	stp_blk_gap_req

Bit Range	Default & Access	Field Name (ID): Description
7	0x1 RW	**BOOT_ACK_CHK (boot_ack_chk):** To check for the boot acknowledge in boot operation; 0 = Will not wait for boot ack from eMMC card; 1 = Wake for boot ack from eMMC card
6	0x0 RW	**ALT_BOOT_EN (alt_boot_en):** To start boot code access in alternative mode; 0 = To stop alternate boot mode access; 1 = To start alternate boot mode access

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**BOOT_EN (boot_en):** To start boot code access; 0 = To stop boot code access; 1 = To start boot code access
4	0x0 RW	**SPI_MODE (spi_mode):** SPI mode enable bit; 0 = SD mode; 1 = SPI mode
3	0x0 RW	**INT_BLK_GAP (int_blk_gap):** Interrupt At Block Gap
2	0x0 RW	**RD_WAIT_CTL (rd_wait_ctl):** Read Wait Control
1	0x0 RW	**CONT_REQ (cont_req):** Continue Request
0	0x0 RW	**STP_BLK_GAP_REQ (stp_blk_gap_req):** Stop At Block Gap Request

6.2.16 Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh

This register is used for wakeup event control.

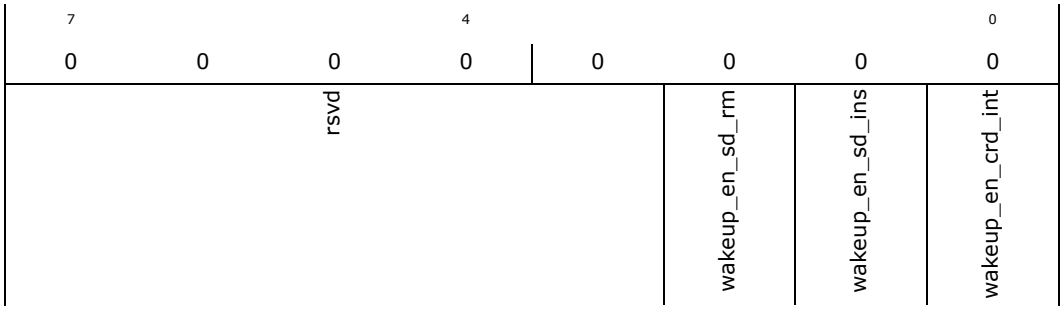
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 2Bh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0x0 RO	**RSVD (rsvd):** Reserved
2	0x0 RW	**WAKEUP_EN_SD_RM (wakeup_en_sd_rm):** Wakeup Event Enable On SD Card Removal
1	0x0 RW	**WAKEUP_EN_SD_INS (wakeup_en_sd_ins):** Wakeup Event Enable On SD Card Insertion
0	0x0 RW	**WAKEUP_EN_CRD_INT (wakeup_en_crd_int):** Wakeup Event Enable On Card Interrupt

6.2.17 Clock Control Register (CLK_CTL)—Offset 2Ch

This register is used configure the frequency of the SDIO controller, and enable the clock.

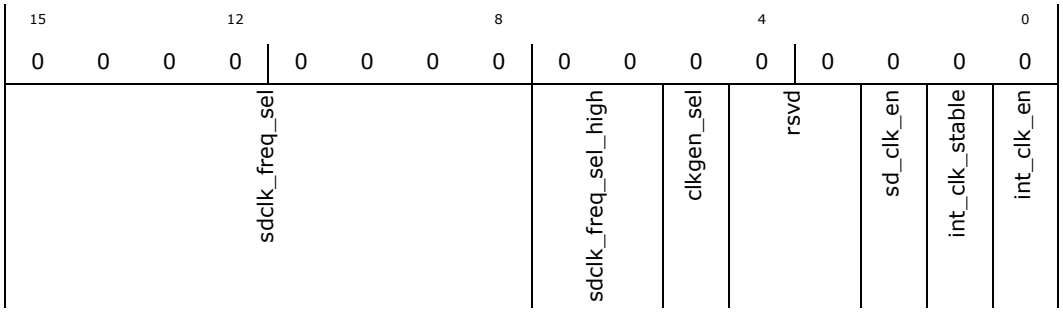
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RW	**SDCLK_FREQ_SEL (sdclk_freq_sel):** SDCLK Frequency Select
7:6	0x0 RW	**SDCLK_FREQ_SEL_HIGH (sdclk_freq_sel_high):** Bit 07-06 is assigned to bit 09-08 of clock divider in SDCLK Frequency Select
5	0x0 RW	**CLKGEN_SEL (clkgen_sel):** This bit is used to select the clock generator mode in SDCLK Frequency Select. 1: Programmable Clock Mode, 0: Divided Clock Mode
4:3	0x0 RO	**RSVD (rsvd):** Reserved
2	0x0 RW	**SD_CLK_EN (sd_clk_en):** SD Clock Enable
1	0x0 RO	**INT_CLK_STABLE (int_clk_stable):** Internal Clock Stable
0	0x0 RW	**INT_CLK_EN (int_clk_en):** Internal Clock Enable

6.2.18 Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh

Timeout Control Register

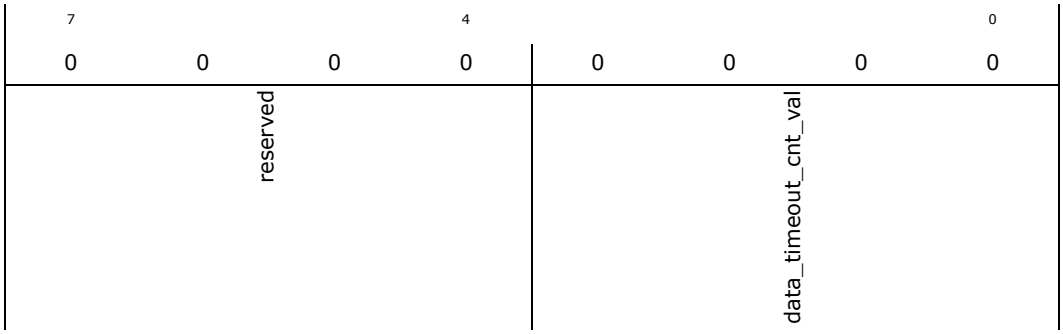
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 2Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RO	**Reserved (reserved):** Reserved
3:0	0x0 RW	**DATA_TIMEOUT_CNT_VAL (data_timeout_cnt_val):** Data Timeout Counter Value

6.2.19 Software Reset Register (SW_RST)—Offset 2Fh

Software Reset Register

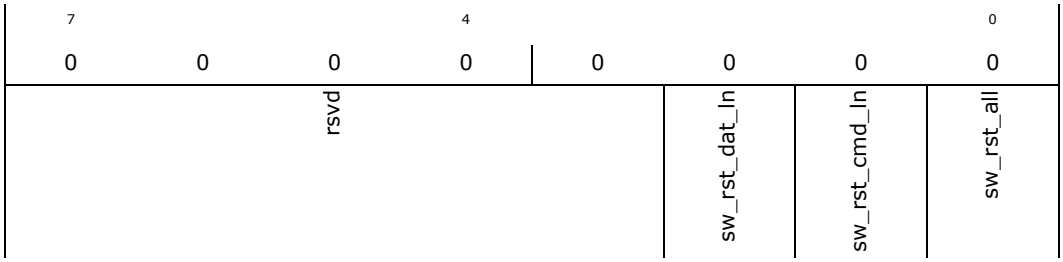
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 2Fh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0x0 RO	**RSVD (rsvd):** Reserved
2	0x0 RW	**SW_RST_DAT_LN (sw_rst_dat_ln):** Software Reset For DAT Line
1	0x0 RW	**SW_RST_CMD_LN (sw_rst_cmd_ln):** Software Reset For CMD Line
0	0x0 RW	**SW_RST_ALL (sw_rst_all):** Software Reset For All

6.2.20 Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h

Normal Interrupt Status Register

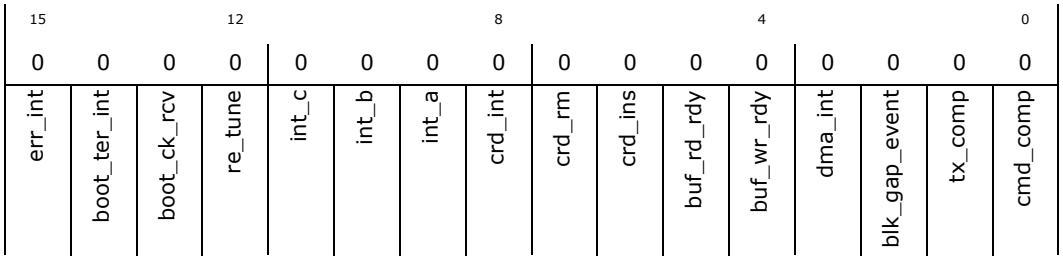
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**ERR_INT (err_int):** Error Interrupt
14	0x0 RW/1C	**BOOT_TER_INT (boot_ter_int):** boot ter int
13	0x0 RW/1C	**BOOT_ACK_RCV (boot_ck_rcv):** boot ack rcv
12	0x0 RO	**RE_TUNE (re_tune):** re tunning event
11	0x0 RO	**INT_C (int_c):** int c
10	0x0 RO	**INT_B (int_b):** int b
9	0x0 RO	**INT_A (int_a):** int a
8	0x0 RO	**CRD_INT (crd_int):** Card Interrupt
7	0x0 RW/1C	**CRD_RM (crd_rm):** Card Removal
6	0x0 RW/1C	**CRD_INS (crd_ins):** Card Insertion
5	0x0 RW/1C	**BUF_RD_RDY (buf_rd_rdy):** Buffer Read Ready
4	0x0 RW/1C	**BUF_WR_RDY (buf_wr_rdy):** Buffer Write Ready
3	0x0 RW/1C	**DMA_INT (dma_int):** DMA Interrupt

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW/1C	**BLK_GAP_EVENT (blk_gap_event):** Block Gap Event
1	0x0 RW/1C	**TX_COMP (tx_comp):** Transfer Complete
0	0x0 RW/1C	**CMD_COMP (cmd_comp):** Command Complete

6.2.21 Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h

Error Interrupt Status Register

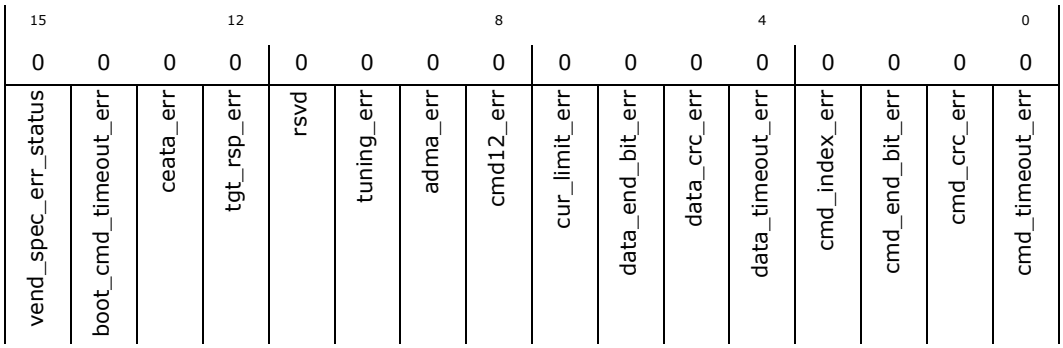
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 32h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**VEND_SPEC_ERR_STATUS (vend_spec_err_status):** Vendor Specific Error Status
14	0x0 RO	**BOOT_CMD_TIMEOUT_ERR (boot_cmd_timeout_err):** Occur if the boot are access command is issued to the agent which has no permission to access the boot area.
13	0x0 RO	**CEATA_ERR (ceata_err):** Occurs when ATA command termination has occurred due to an error condition the device has encountered.
12	0x0 RW/1C	**TGT_RSP_ERR (tgt_rsp_err):** Occurs when detecting ERROR in m_hresp(dma transaction)
11	0x0 RO	**RSVD (rsvd):** Reserved
10	0x0 RO	**TUNING_ERR (tuning_err):** Tuning Error

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RW/1C	**ADMA_ERR (adma_err):** ADMA Error
8	0x0 RW/1C	**CMD12_ERR (cmd12_err):** Auto CMD12 Error
7	0x0 RW/1C	**CUR_LIMIT_ERR (cur_limit_err):** Current Limit Error
6	0x0 RW/1C	**DATA_END_BIT_ERR (data_end_bit_err):** Data End Bit Error
5	0x0 RW/1C	**DATA_CRC_ERR (data_crc_err):** Data CRC Error
4	0x0 RW/1C	**DATA_TIMEOUT_ERR (data_timeout_err):** Data Timeout Error
3	0x0 RW/1C	**CMD_INDEX_ERR (cmd_index_err):** Command Index Error
2	0x0 RW/1C	**CMD_END_BIT_ERR (cmd_end_bit_err):** Command End Bit Error
1	0x0 RW/1C	**CMD_CRC_ERR (cmd_crc_err):** Command CRC Error
0	0x0 RW/1C	**CMD_TIMEOUT_ERR (cmd_timeout_err):** Command Timeout Error

6.2.22 Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h

Normal Interrupt Status Enable

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
fixed_0	boot_term_int_en	boot_ack_rcv_en	re_tune_en	int_c_en	int_b_en	int_a_en	crd_int_stat_en	crd_rm_stat_en	crd_ins_stat_en	buf_rd_rdy_stat_en	buf_wr_rdy_stat_en	dma_int_stat_en	blk_gap_event_stat_en	tx_comp_stat_en	cmd_comp_stat_en

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**FIXED_0 (fixed_0):** Fixed to 0
14	0x0 RW	**BOOT_TERM_INT_EN (boot_term_int_en):** 0 - Masked
13	0x0 RW	**BOOT_ACK_RCV_EN (boot_ack_rcv_en):** 0 -Masked
12	0x0 RW	**RE_TUNE_EN (re_tune_en):** re tunning event enable
11	0x0 RW	**INT_C_EN (int_c_en):** int c enable
10	0x0 RW	**INT_B_EN (int_b_en):** int b enable
9	0x0 RW	**INT_A_EN (int_a_en):** int a enable
8	0x0 RW	**CRD_INT_STAT_EN (crd_int_stat_en):** Card Interrupt Status Enable
7	0x0 RW	**CRD_RM_STAT_EN (crd_rm_stat_en):** Card Removal Status Enable
6	0x0 RW	**CRD_INS_STAT_EN (crd_ins_stat_en):** Card Insertion Status Enable
5	0x0 RW	**BUF_RD_RDY_STAT_EN (buf_rd_rdy_stat_en):** Buffer Read Ready Status Enable
4	0x0 RW	**BUF_WR_RDY_STAT_EN (buf_wr_rdy_stat_en):** Buffer Write Ready Status Enable
3	0x0 RW	**DMA_INT_STAT_EN (dma_int_stat_en):** DMA Interrupt Status Enable
2	0x0 RW	**BLK_GAP_EVENT_STAT_EN (blk_gap_event_stat_en):** Block Gap Event Status Enable
1	0x0 RW	**TX_COMP_STAT_EN (tx_comp_stat_en):** Transfer Complete Status Enable
0	0x0 RW	**CMD_COMP_STAT_EN (cmd_comp_stat_en):** Command Complete Status Enable

6.2.23 Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h

Error Interrupt Status Enable Register

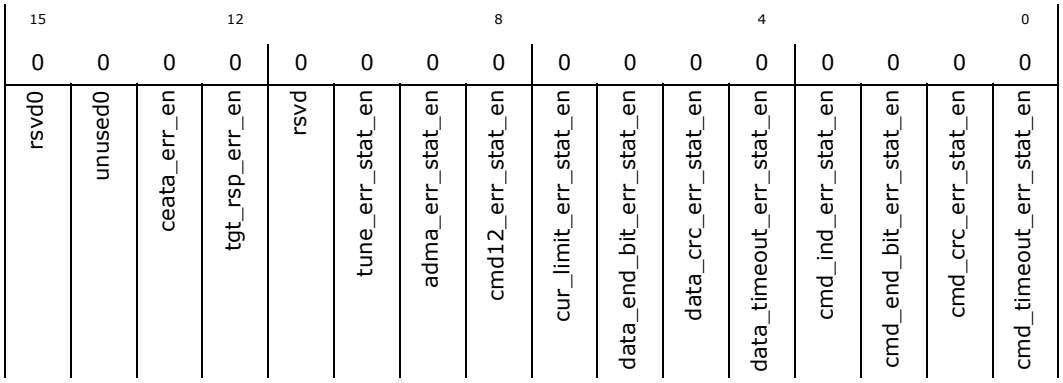
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 36h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**RSVD0 (rsvd0):** Reserved
14	0x0 RW	**UNUSED0 (unused0):** Unused
13	0x0 RW	**CEATA_ERR_EN (ceata_err_en):** 0 - masked
12	0x0 RW	**TGT_RSP_ERR_EN (tgt_rsp_err_en):** 0 - masked
11	0x0 RO	**RSVD (rsvd):** Reserved
10	0x0 RW	**TUNE_ERR_STATE_EN (tune_err_stat_en):** 0 - masked
9	0x0 RW	**ADMA_ERR_STAT_EN (adma_err_stat_en):** ADMA Error Status Enable
8	0x0 RW	**CMD12_ERR_STAT_EN (cmd12_err_stat_en):** Auto CMD12 Error Status Enable
7	0x0 RW	**CUR_LIMIT_ERR_STAT_EN (cur_limit_err_stat_en):** Current Limit Error Status Enable
6	0x0 RW	**DATA_END_BIT_ERR_STAT_EN (data_end_bit_err_stat_en):** Data End Bit Error Status Enable
5	0x0 RW	**DATA_CRC_ERR_STAT_EN (data_crc_err_stat_en):** Data CRC Error Status Enable
4	0x0 RW	**DATA_TIMEOUT_ERR_STAT_EN (data_timeout_err_stat_en):** Data Timeout Error Status Enable
3	0x0 RW	**CMD_IND_ERR_STAT_EN (cmd_ind_err_stat_en):** Command Index Error Status Enable
2	0x0 RW	**CMD_END_BIT_ERR_STAT_EN (cmd_end_bit_err_stat_en):** Command End Bit Error Status Enable
1	0x0 RW	**CMD_CRC_ERR_STAT_EN (cmd_crc_err_stat_en):** Command CRC Error Status Enable
0	0x0 RW	**CMD_TIMEOUT_ERR_STAT_EN (cmd_timeout_err_stat_en):** Command Timeout Error Status Enable

6.2.24 Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h

Normal Interrupt Signal Enable Register

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
fixed_0	boot_term_int_sig_en	boot_ack_rcv_sig_en	re_tune_sig_en	int_c_sig_en	int_b_sig_en	int_a_sig_en	crd_int_sig_en	crd_rm_sig_en	crd_ins_sig_en	buf_rd_rdy_sig_en	buf_wr_rdy_sig_en	dma_int_sig_en	blk_gap_event_sig_en	tx_comp_sig_en	cmd_comp_sig_en

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**FIXED_0 (fixed_0):** Fixed to 0
14	0x0 RW	**BOOT_TERM_INT_SIG_EN (boot_term_int_sig_en):** 0 - masked
13	0x0 RW	**BOOT_ACK_RCV_SIG_EN (boot_ack_rcv_sig_en):** 0 - masked
12	0x0 RW	**RE_TUNE_SIG_EN (re_tune_sig_en):** re tunning event Signal Enable
11	0x0 RW	**INT_C_SIG_EN (int_c_sig_en):** int c Signal Enable
10	0x0 RW	**INT_B_SIG_EN (int_b_sig_en):** int b Signal Enable
9	0x0 RW	**INT_A_SIG_EN (int_a_sig_en):** int a Signal Enable
8	0x0 RW	**CRD_INT_SIG_EN (crd_int_sig_en):** Card Interrupt Signal Enable
7	0x0 RW	**CRD_RM_SIG_EN (crd_rm_sig_en):** Card Removal Signal Enable
6	0x0 RW	**CRD_INS_SIG_EN (crd_ins_sig_en):** Card Insertion Signal Enable
5	0x0 RW	**BUF_RD_RDY_SIG_EN (buf_rd_rdy_sig_en):** Buffer Read Ready Signal Enable
4	0x0 RW	**BUF_WR_RDY_SIG_EN (buf_wr_rdy_sig_en):** Buffer Write Ready Signal Enable

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**DMA_INT_SIG_EN (dma_int_sig_en):** DMA Interrupt Signal Enable
2	0x0 RW	**BLK_GAP_EVENT_SIG_EN (blk_gap_event_sig_en):** Block Gap Event Signal Enable
1	0x0 RW	**TX_COMP_SIG_EN (tx_comp_sig_en):** Transfer Complete Signal Enable
0	0x0 RW	**CMD_COMP_SIG_EN (cmd_comp_sig_en):** Command Complete Signal Enable

6.2.25 Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah

Error Interrupt Signal Enable Register

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 3Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0	unused0	ceata_err_sig_en	tgt_err_rsp_sig_en	rsvd	tune_err_sig	adma_err_sig_en	cmd12_err_sig_en	cur_limit_err_sig_en	data_end_bit_err_sig_en	data_crc_err_sig_en	data_timeout_err_stat_en	cmd_ind_err_stat_en	cmd_end_bit_err_stat_en	cmd_crc_err_stat_en	cmd_timeout_err_stat_en

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**RSVD0 (rsvd0):** Reserved
14	0x0 RW	**UNUSED0 (unused0):** Unused
13	0x0 RW	**CEATA_ERR_SIG_EN (ceata_err_sig_en):** 0 - masked
12	0x0 RW	**TGT_ERR_RSP_SIG_EN (tgt_err_rsp_sig_en):** 0 - masked
11	0x0 RO	**RSVD (rsvd):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RW	**TUNE_ERR_SIG (tune_err_sig):** 0 - masked
9	0x0 RW	**ADMA_ERR_SIG_EN (adma_err_sig_en):** ADMA Error Signal Enable
8	0x0 RW	**CMD12_ERR_SIG_EN (cmd12_err_sig_en):** Auto CMD12 Error Signal Enable
7	0x0 RW	**CUR_LIMIT_ERR_SIG_EN (cur_limit_err_sig_en):** Current Limit Error Signal Enable
6	0x0 RW	**DATA_END_BIT_ERR_SIG_EN (data_end_bit_err_sig_en):** Data End Bit Error Signal Enable
5	0x0 RW	**DATA_CRC_ERR_SIG_EN (data_crc_err_sig_en):** Data CRC Error Signal Enable
4	0x0 RW	**DATA_TIMEOUT_ERR_STAT_EN (data_timeout_err_stat_en):** Data Timeout Error Signal Enable
3	0x0 RW	**CMD_IND_ERR_STAT_EN (cmd_ind_err_stat_en):** Command Index Error Signal Enable
2	0x0 RW	**CMD_END_BIT_ERR_STAT_EN (cmd_end_bit_err_stat_en):** Command End Bit Error Signal Enable
1	0x0 RW	**CMD_CRC_ERR_STAT_EN (cmd_crc_err_stat_en):** Command CRC Error Signal Enable
0	0x0 RW	**CMD_TIMEOUT_ERR_STAT_EN (cmd_timeout_err_stat_en):** Command Timeout Error Signal Enable

6.2.26 Auto CMD12 Error Status Register and Host control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch

Auto CMD12 Error Status Register and Host control 2 Register

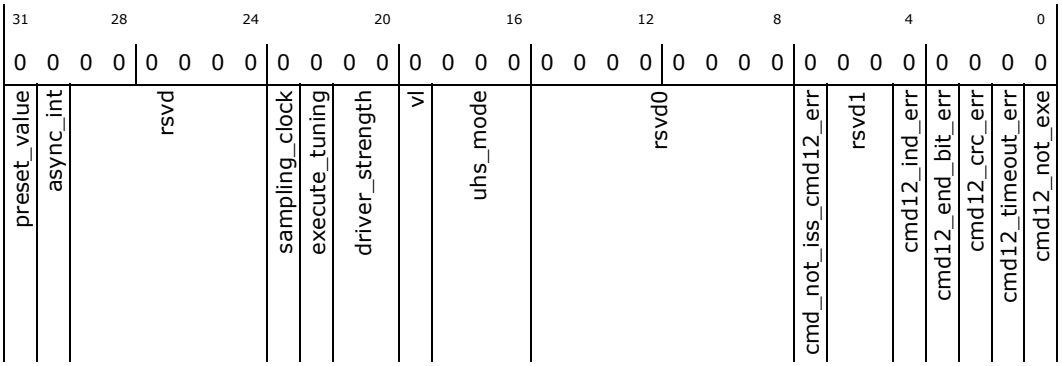
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**PRESET_VALUE (preset_value):** Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set to automatic This bit enables the functions defined in the Preset Value registers. 1 Automatic Selection by Preset Value are Enabled 0 SDCLK and Driver Strength are controlled by Host Driver If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver. If this bit is set to 1, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Controller as specified in the Preset Value registers.
30	0x0 RW	**ASYNC_INT (async_int):** This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode (and zero is set to Interrupt Pin Select in the Shared Bus Control register). If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card. 1 Enabled 0 Disabled
29:24	0x0 RO	**RSVD (rsvd):** Reserved
23	0x0 RW	**SAMPLING_CLOCK (sampling_clock):** This bit is set by tuning procedure when Execute Tuning is cleared
22	0x0 RW/AC	**EXECUTE_TUNING (execute_tuning):** This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by writing 0 for more detail about tuning procedure. 1 Execute Tuning 0 Not Tuned or Tuning Completed
21:20	0x0 RW	**DRIVER_STRENGTH (driver_strength):** Host Controller output driver in 1.8V signaling is selected by this bit
19	0x0 RW	**VL (vl):** This bit controls voltage regulator for I/O cell, 1 - 1.8V Signaling, 0 - 3.3V Signaling. This bit has to be set based on actual I/O signal voltage even though only a single voltage is supported in a platform
18:16	0x0 RW	**UHS_MODE (uhs_mode):** This field is used to select one of UHS-I modes

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**RSVD0 (rsvd0):** Reserved
7	0x0 RO	**CMD_NOT_ISS_CMD12_ERR (cmd_not_iss_cmd12_err):** Command Not Issued By Auto CMD12 Error
6:5	0x0 RO	**RSVD1 (rsvd1):** Reserved
4	0x0 RO	**CMD12_IND_ERR (cmd12_ind_err):** Auto CMD12 Index Error
3	0x0 RO	**CMD12_END_BIT_ERR (cmd12_end_bit_err):** Auto CMD12 End Bit Error
2	0x0 RO	**CMD12_CRC_ERR (cmd12_crc_err):** Auto CMD12 CRC Error
1	0x0 RO	**CMD12_TIMEOUT_ERR (cmd12_timeout_err):** Auto CMD12 Timeout Error
0	0x0 RO	**CMD12_NOT_EXE (cmd12_not_exe):** Auto CMD12 Not Executed

6.2.27 Capabilities Register (CAPABILITIES)—Offset 40h

Capabilities Register

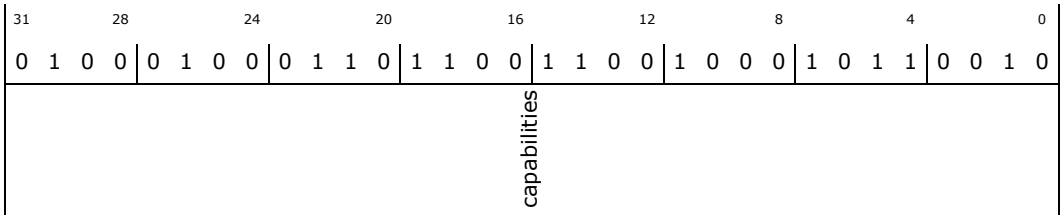
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 446CC8B2h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x446cc8b2 RO	**capabilities:** capabilities

6.2.28 Capabilities Register 2 (CAPABILITIES_2)—Offset 44h

Capabilities Register 2

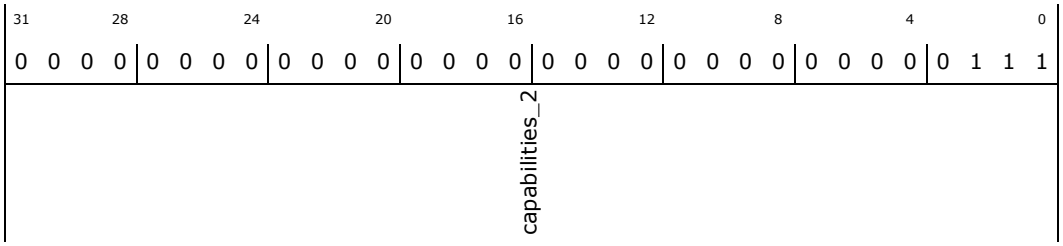
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000007h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x7 RO	**capabilities_2:** capabilities 2

6.2.29 Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h

These registers indicate maximum current capability for each voltage

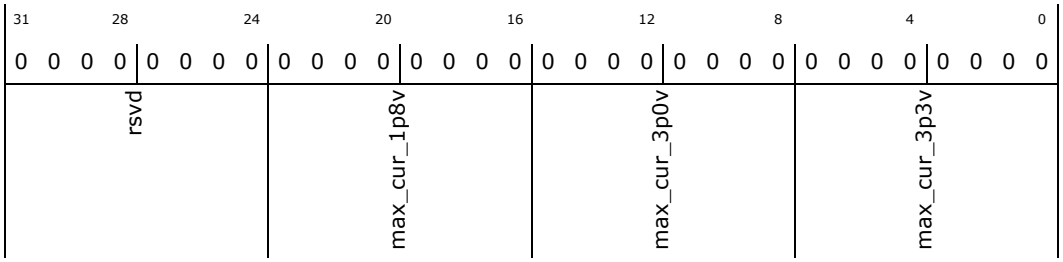
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD (rsvd):** Reserved
23:16	0x0 RO	**MAX_CUR_1p8V (max_cur_1p8v):** Maximum Current for 1.8V
15:8	0x0 RO	**MAX_CUR_3p0V (max_cur_3p0v):** Maximum Current for 3.0V

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**MAX_CUR_3p3V (max_cur_3p3v):** Maximum Current for 3.3V

6.2.30 Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h

Force Event Register for Auto CMD12 Error Status

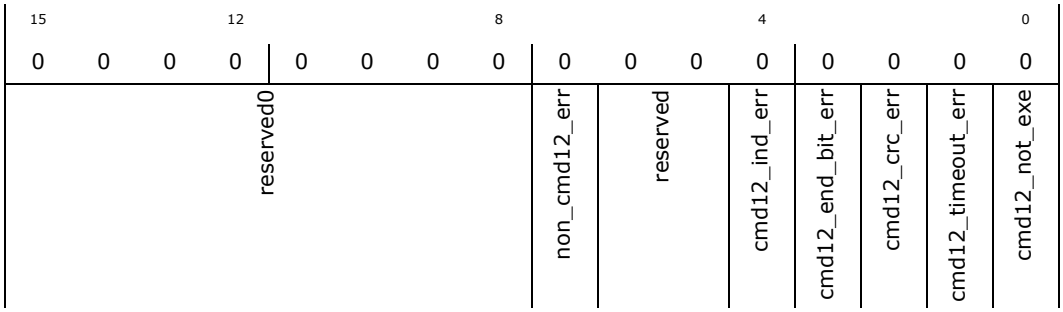
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Reserved0 (reserved0):** Reserved
7	0x0 WO	**NON_CMD12_ERR (non_cmd12_err):** Force Event for Command Not Issued By Auto CMD12 Error :
6:5	0x0 RO	**Reserved (reserved):** Reserved
4	0x0 WO	**CMD12_IND_ERR (cmd12_ind_err):** Force Event for Auto CMD12 Index Error
3	0x0 WO	**CMD12_END_BIT_ERR (cmd12_end_bit_err):** Force Event for Auto CMD12 End Bit Error
2	0x0 WO	**CMD12_CRC_ERR (cmd12_crc_err):** Force Event for Auto CMD12 CRC Error
1	0x0 WO	**CMD12_TIMEOUT_ERR (cmd12_timeout_err):** Force Event for Auto CMD12 Timeout Error
0	0x0 WO	**CMD12_NOT_EXE (cmd12_not_exe):** Force Event for Auto CMD12 Not Executed

6.2.31 Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h

Force Event Register for Error Interrupt Status

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 52h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0		ceata_err	tgt_rsp_err	rsvd		adma_err	cmd12_err	cur_limit_err	data_end_bit_err	data_crc_err	data_timeout_err	cmd_ind_err	cmd_end_bit_err	cmd_crc_err	cmd_timeout_err

Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RO	**RSVD0 (rsvd0):** Reserved
13	0x0 RO	**CEATA_ERR (ceata_err):** Force Event for CEATA error, legacy feature not implemented
12	0x0 RO	**TGT_RSP_ERR (tgt_rsp_err):** Force Event for Target Response Error, legacy feature not implemented
11:10	0x0 RO	**RSVD (rsvd):** Reserved
9	0x0 WO	**ADMA_ERR (adma_err):** Force Event for ADMA Error
8	0x0 WO	**CMD12_ERR (cmd12_err):** Force Event for Auto CMD12 Error
7	0x0 WO	**CUR_LIMIT_ERR (cur_limit_err):** Force Event for Current Limit Error
6	0x0 WO	**DATA_END_BIT_ERR (data_end_bit_err):** Force Event for Data End Bit Error
5	0x0 WO	**DATA_CRC_ERR (data_crc_err):** Event for Data CRC Error
4	0x0 WO	**DATA_TIMEOUT_ERR (data_timeout_err):** Event for Data Timeout Error
3	0x0 WO	**CMD_IND_ERR (cmd_ind_err):** Force Event for Command Index Error
2	0x0 WO	**CMD_END_BIT_ERR (cmd_end_bit_err):** Force Event for Command End Bit Error

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 WO	**CMD_CRC_ERR (cmd_crc_err):** Force Event for Command CRC Error
0	0x0 WO	**CMD_TIMEOUT_ERR (cmd_timeout_err):** Force Event for Command Timeout Error

6.2.32 ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h

ADMA Error Status Register

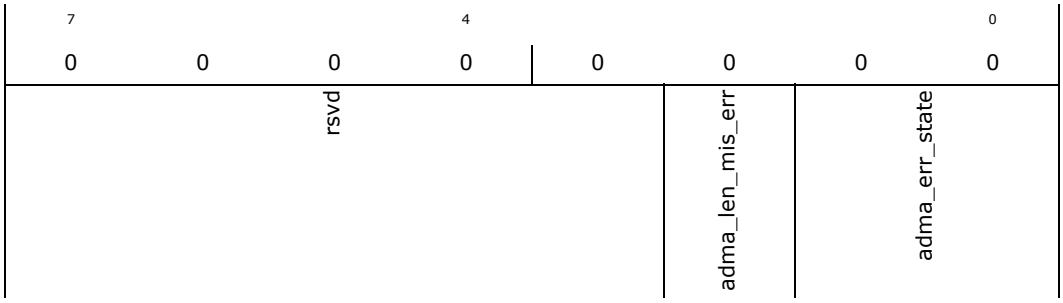
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0x0 RO	**RSVD (rsvd):** Reserved
2	0x0 RO	**ADMA_LEN_MIS_ERR (adma_len_mis_err):** ADMA Length Mismatch Error
1:0	0x0 RO	**ADMA_ERR_STATE (adma_err_state):** ADMA Error State

6.2.33 ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h

This register contains the physical Descriptor address used for ADMA data transfer.

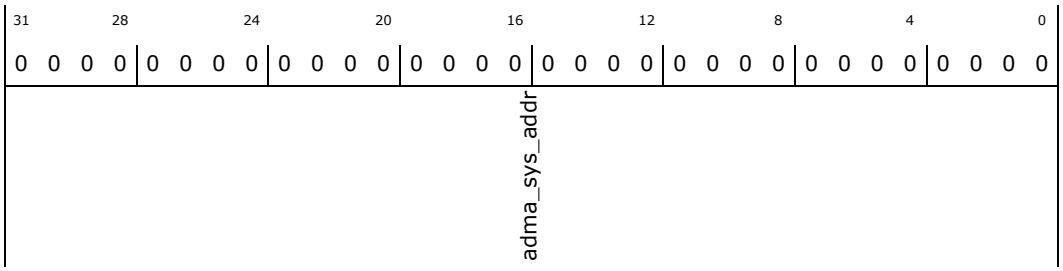
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**ADMA_SYS_ADDR (adma_sys_addr):** ADMA System Address

6.2.34 ADMA System Address Register (ADMA_SYS_ADDR_HIGH)—Offset 5Ch

This register contains the physical Descriptor address used for ADMA data transfer.

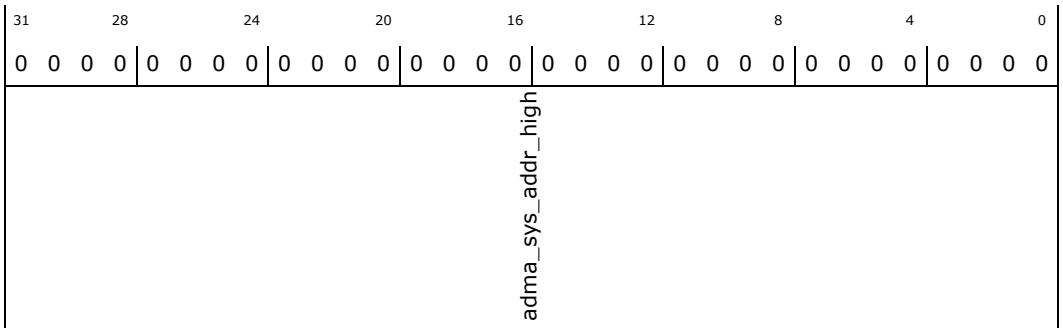
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**ADMA_SYS_ADDR_HIGH (adma_sys_addr_high):** High 32 bits of ADMA System Address for 64bit system

6.2.35 Preset Values registers (PRESET_VALUE_0)—Offset 60h

Preset Values init and default speed

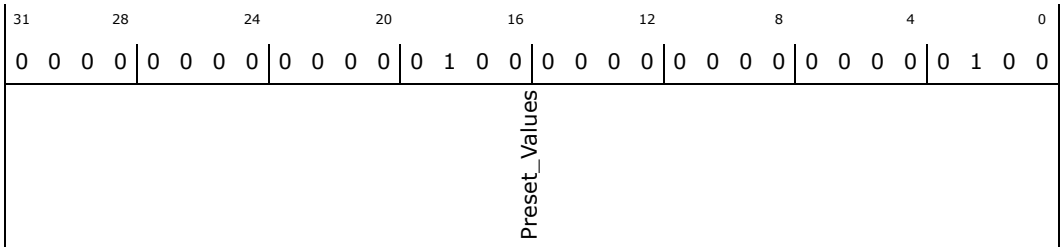
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00040004h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x40004 RO	**PresetValues (Preset_Values):** Reserved.

6.2.36 Preset Values 1 registers (PRESET_VALUE_1)—Offset 64h

Preset Values high and sdr12

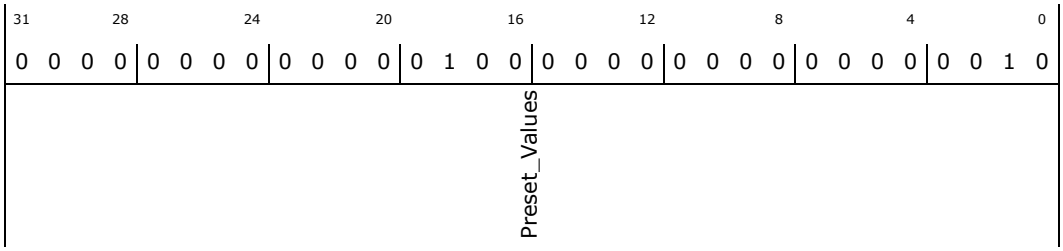
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00040002h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x40002 RO	**PresetValues (Preset_Values):** Reserved.

6.2.37 Preset Values 2 registers (PRESET_VALUE_2)—Offset 68h

Preset Values sdr25 and sdr50

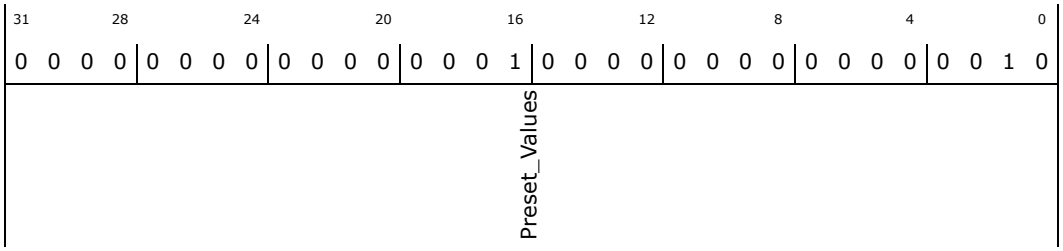
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00010002h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x10002 RO	**PresetValues (Preset_Values):** Reserved.

6.2.38 Preset Values 3 registers (PRESET_VALUE_3)—Offset 6Ch

Preset Values sdr104 and ddr50

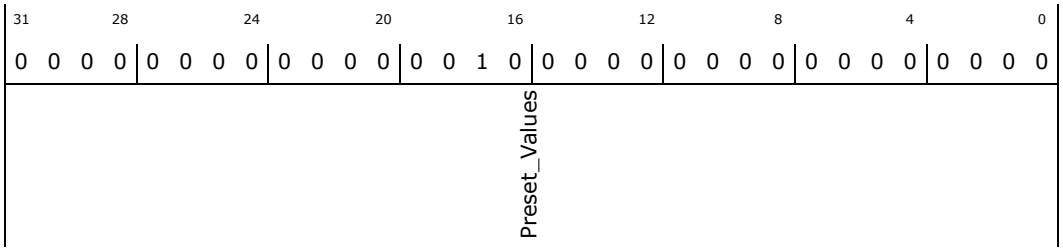
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00020000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x20000 RO	**PresetValues (Preset_Values):** Reserved.

6.2.39 BOOT_TIMEOUT_CTRL (BOOT_TIMEOUT_CTRL)—Offset 70h

BOOT_TIMEOUT_CTRL

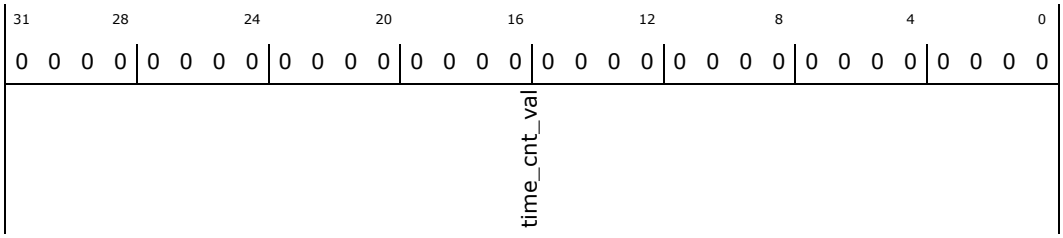
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**TIME_CNT_VAL (time_cnt_val):** Boot Data Timeout Counter Value

6.2.40 DEBUG_SEL (DEBUG_SEL)—Offset 74h

Debug Selection Register

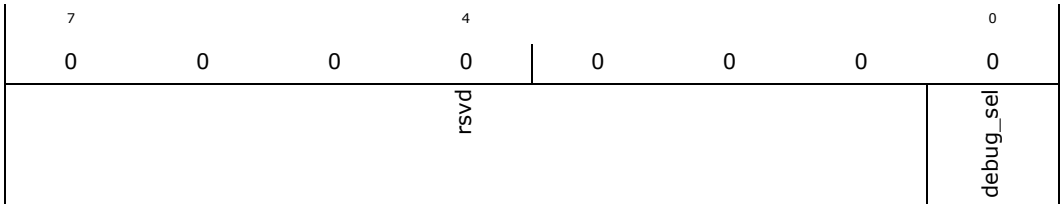
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:1	0x0 RO	**RSVD (rsvd):** Reserved
0	0x0 RO	**DEBUG_SEL (debug_sel):** 1 - cmd register, interrupt status, transmitter module, ahb_iface module and clk sdcard signals are probed out..

6.2.41 Shared Bus Control Register (SHARED_BUS)—Offset E0h

Shared Bus Control Register

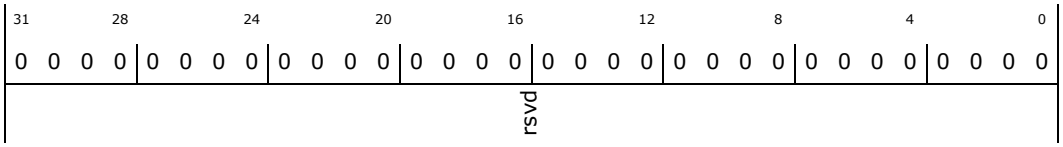
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD (rsvd):** Reserved

6.2.42 SPI_INT_SUP (SPI_INT_SUP)—Offset F0h

SPI_INT_SUP

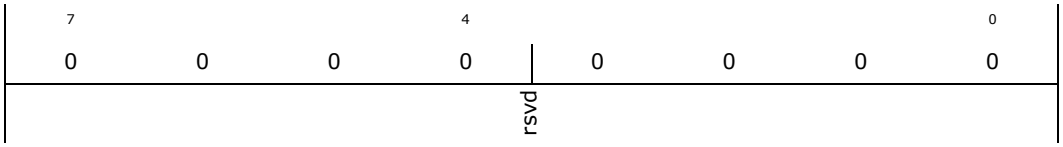
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**RSVD (rsvd):** Reserved

6.2.43 Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh

Slot Interrupt Status Register

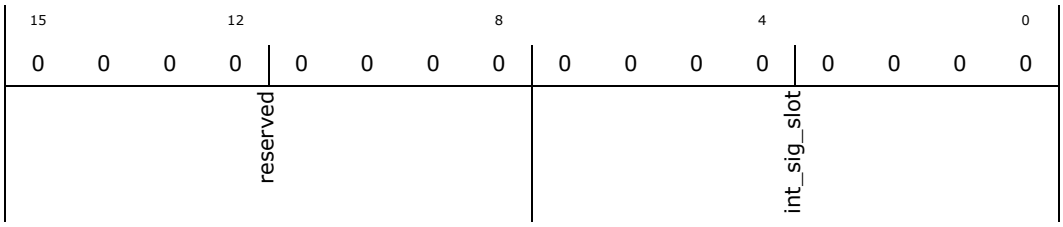
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Reserved (reserved):** Reserved
7:0	0x0 RO	**INT_SIG_SLOT (int_sig_slot):** Interrupt Signal For Each Slot

6.2.44 Host Controller Version Register (HOST_CTRL_VER)—Offset FEh

Host Controller Version Register

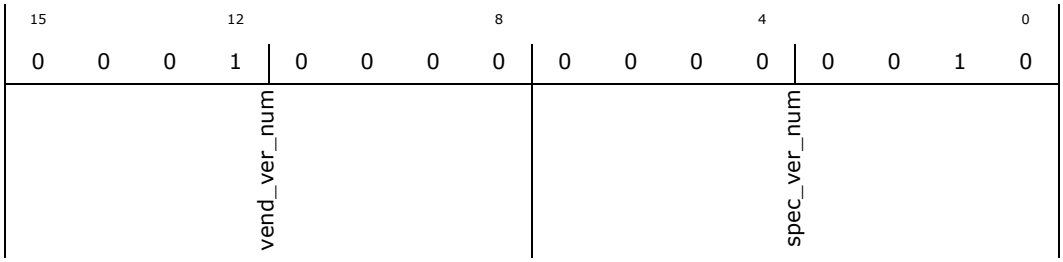
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + FEh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:16, F:0] + 10h

Default: 1002h

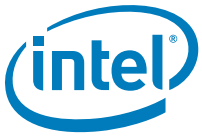


Bit Range	Default & Access	Field Name (ID): Description
15:8	0x10 RO	**VEND_VER_NUM (vend_ver_num):** Vendor Version Number
7:0	0x2 RO	**SPEC_VER_NUM (spec_ver_num):** Version Number

6.3 SDIO 1 PCI Configuration Registers

Table 34. Summary of SDIO 1 PCI Configuration Registers—0/17/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 1951	22948086h
4–7h	4	"Status and Command Register (STATUSCOMMAND)—Offset 4h" on page 1951	00100000h
8–Bh	4	"Revision ID and Class Code Register (REVCLASSCODE)—Offset 8h" on page 1952	00000000h
C–Fh	4	"Cache Line Latency Header and BIST Register (CLLATHEADERBIST)—Offset Ch" on page 1953	00000000h
10–13h	4	"Base Address Register low (BAR)—Offset 10h" on page 1954	00000000h
14–17h	4	"Base Address Register high (BAR_HIGH)—Offset 14h" on page 1954	00000000h
18–1Bh	4	"Base Address Register1 low (BAR1)—Offset 18h" on page 1955	00000000h
1C–1Fh	4	"Base Address Register1 high (BAR1_HIGH)—Offset 1Ch" on page 1956	00000000h
2C–2Fh	4	"Subsystem Vendor and Subsystem ID Register (SUBSYSTEMID)—Offset 2Ch" on page 1956	00000000h
30–33h	4	"EXPANSION ROM base address Register (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 1957	00000000h
34–37h	4	"Capabilities Pointer Register (CAPABILITYPTR)—Offset 34h" on page 1957	00000080h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 1958	00000100h
80–83h	4	"PowerManagement Capability ID Register (POWERCAPID)—Offset 80h" on page 1959	48030001h
84–87h	4	"Power Management Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 1959	00000008h
A0–A3h	4	"General Purpose Read Write Register1 (GEN_REGRW1)—Offset A0h" on page 1960	00000000h
A4–A7h	4	"General Purpose Read Write Register2 (GEN_REGRW2)—Offset A4h" on page 1961	00000000h
A8–ABh	4	"General Purpose Read Write Register3 (GEN_REGRW3)—Offset A8h" on page 1961	00000000h
AC–AFh	4	"General Purpose Read Write Register4 (GEN_REGRW4)—Offset ACh" on page 1962	00000000h
C0–C3h	4	"General Purpose Input Register (GEN_INPUT_REG)—Offset C0h" on page 1962	00000000h
F8–FBh	4	"Manufacturers ID Register (MANID)—Offset F8h" on page 1963	00000000h



6.3.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

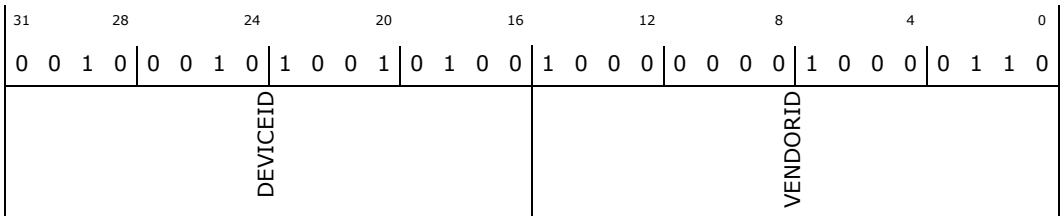
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 0h

Default: 22948086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x2294 RO	**DEVICEID:** Device ID identifies the particular PCI device. The Default value is taken from a strap at the top level. SetIDValue message updates 15:7 of this strap. Value shown below is after SetIDValue from CHV_RevIdDevId_HAS: SDIO1(smmc) : 16'h2294 SDIO2(sdio) : 16'h2295 SDIO3(sdcard) : 16'h2296
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by the PCI SIG, which identifies the manufacturer of the device. This is tied to a strap the top level.

6.3.2 Status and Command Register (STATUSCOMMAND)—Offset 4h

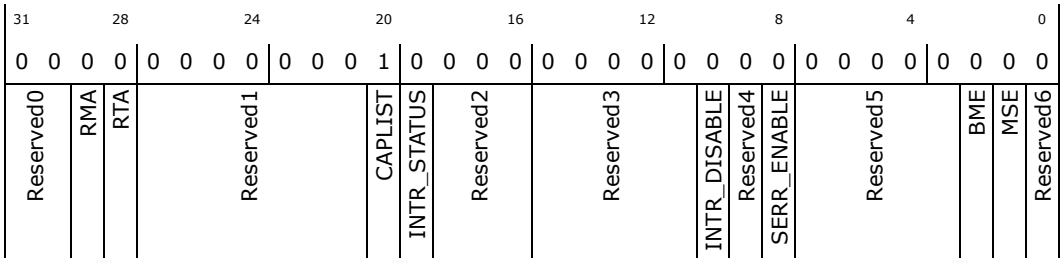
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved0:** Reserved, [30]: Signaled System Error, Not implemented
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, the Bridge sets this bit.
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, the Bridge sets this bit.
27:21	0x0 RO	**Reserved1:** Reserved, [27]: Signaled Target Abort: Not implemented
20	0x1 RO	**CAPLIST:** Capabilities List: Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at the configuration offset 34h.
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, is the device/function interrupt message sent. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, which is the Bridge does not send Interrupt Assert message through the IOSF Sideband Channel. Reset value of this bit is 0. This bit has no connection with the interrupt status bit.
9	0x0 RO	**Reserved4:** Reserved
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: Not implemented
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0,the Bridge does not generate any new upstream transaction on IOSF as a master.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge response to downstream memory accesses. When set, accesses to memory space of the device is enabled.
0	0x0 RO	**Reserved6:** Reserved

6.3.3 Revision ID and Class Code Register (REVCLASSCODE)—Offset 8h

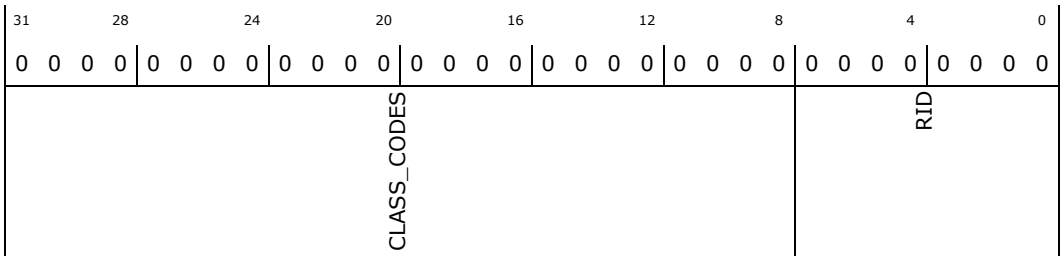
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** The Class Code register is read-only and is used to identify the generic function of the device, and in some cases, a specific register-level programming interface. The register is broken into 3 Byte-size fields. 1. The upper Byte (at offset 0Bh) is a base class code that broadly classifies the type of function the device performs. 2. The middle Byte (at offset 0Ah) is a sub-class code that identifies more specifically the function of the device. 3. The lower Byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular PCI device. The default value comes from a strap. A SetIDValue message updates this value.

6.3.4 Cache Line Latency Header and BIST Register (CLLATHEADERBIST)—Offset Ch

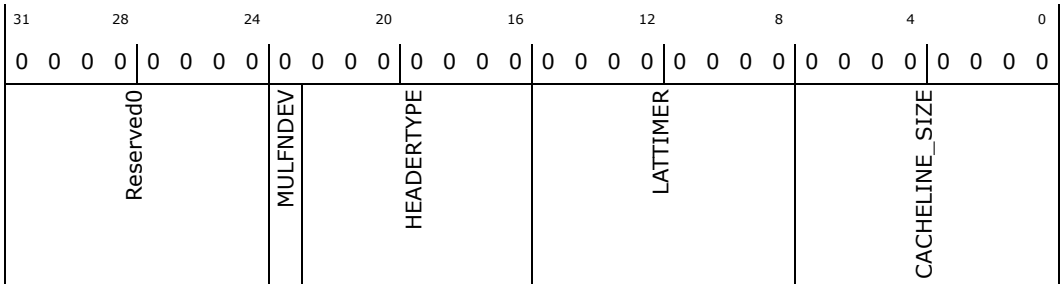
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x0 RO	**MULFNDEV:** Multi-Function Device: This bit is 0 to indicate Single Function Device

Bit Range	Default & Access	Field Name (ID): Description
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header
15:8	0x0 RO	**LATTIMER:** Latency Timer
7:0	0x0 RW	**CACHELINE_SIZE:** Cacheline Size: This register is implemented as R/W with default as 0. Similar to other Intel IPs.

6.3.5 Base Address Register low (BAR)—Offset 10h

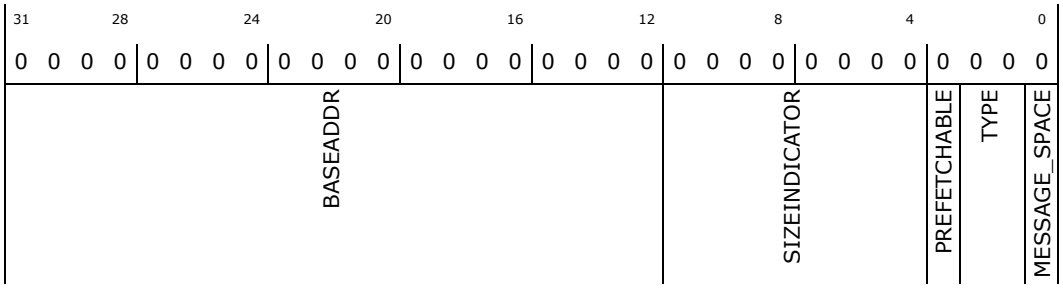
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the OCP fabric memory space. bit [31] is always read write as Bridge expects the size of the device to be limited to 2G Taken from Strap values as ones.
11:4	0x0 RO	**SIZEINDICATOR:** Always is 0, as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0x0 RO	**TYPE:** Type: If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

6.3.6 Base Address Register high (BAR_HIGH)—Offset 14h

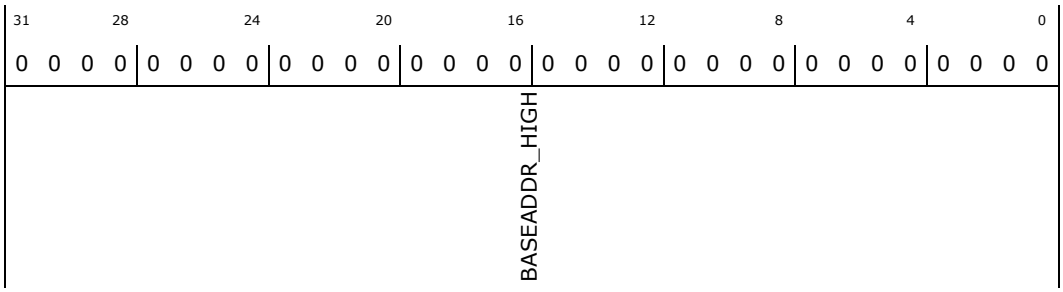
BAR -Base Address Register High

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**BASEADDR_HIGH:** High 32 bits for BAR, RO as SCC is set to 32 bits only

6.3.7 Base Address Register1 low (BAR1)—Offset 18h

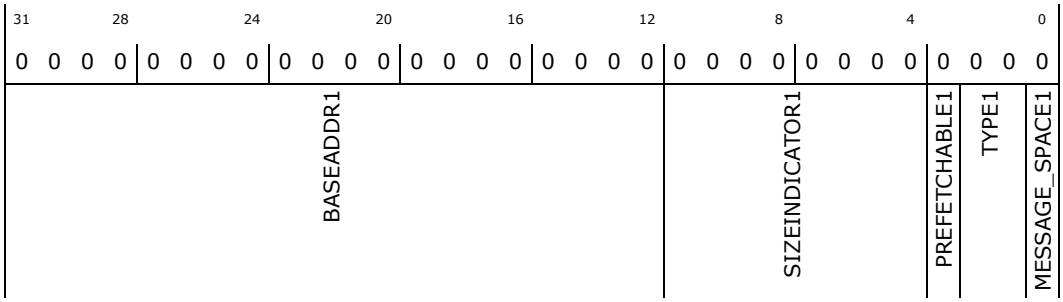
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 18h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: This field is present if BAR1 is enabled through private configuration space.
11:4	0x0 RO	**SIZEINDICATOR1:** Always is 0 as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0x0 RO	**TYPE1:** Type: If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0 Indicates this BAR is present in the memory space.

6.3.8 Base Address Register1 high (BAR1_HIGH)—Offset 1Ch

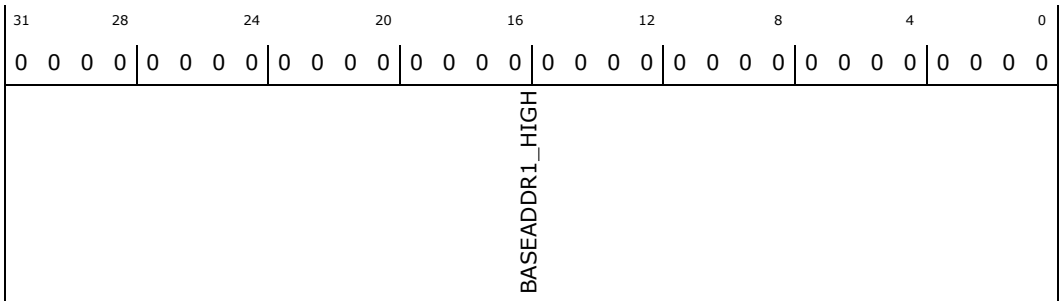
BAR1 -Base Address Register1 High

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 1Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**BASEADDR1_HIGH:** High 32 bits for BAR1, RO as SCC is set to 32 bits only

6.3.9 Subsystem Vendor and Subsystem ID Register (SUBSYSTEMID)—Offset 2Ch

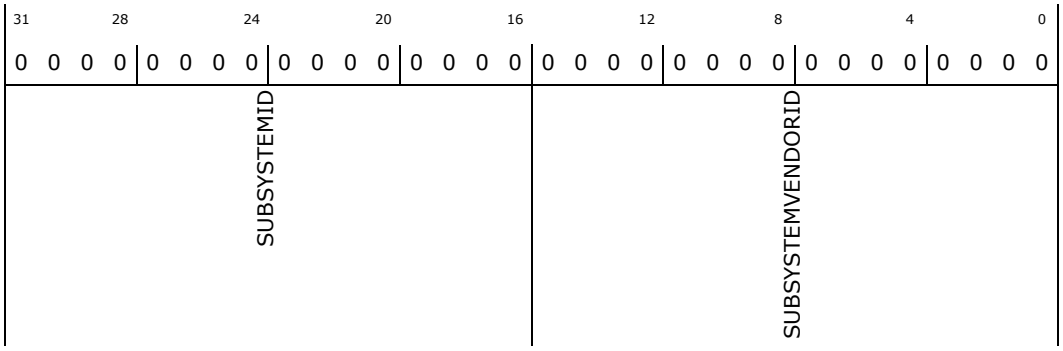
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

6.3.10 EXPANSION ROM base address Register (EXPANSION_ROM_BASEADDR)—Offset 30h

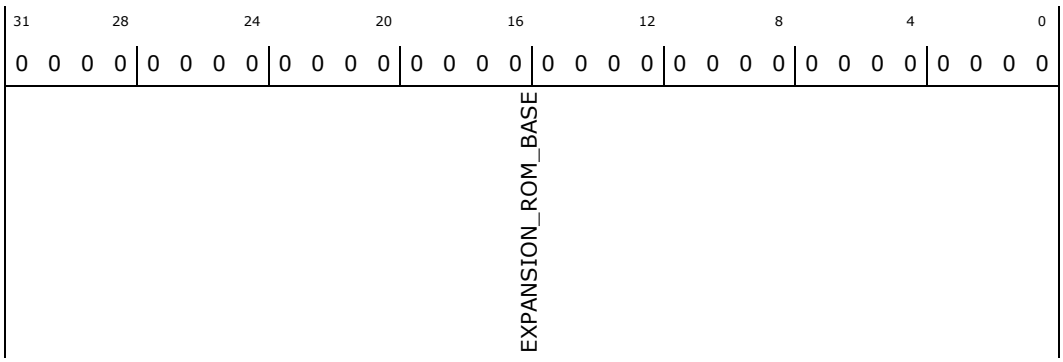
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** [31:11]-) Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM [10:1] -) Reserved [0] -) Expansion ROM Enable: Bridge does not have support for Expansion ROMs.

6.3.11 Capabilities Pointer Register (CAPABILITYPTR)—Offset 34h

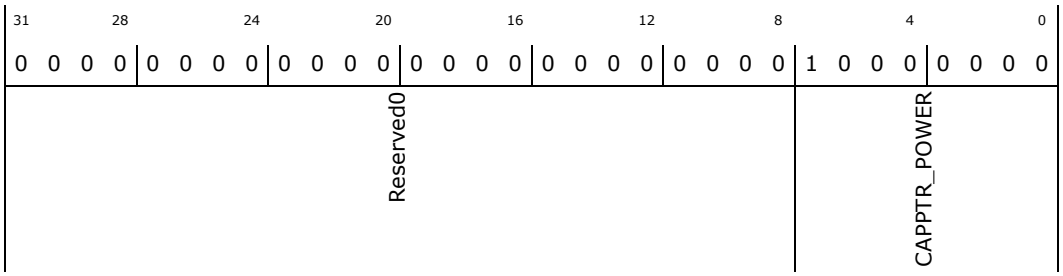
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 34h

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x80 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability points to the PM Capability (0x80) structure.

6.3.12 Interrupt Register (INTERRUPTREG)—Offset 3Ch

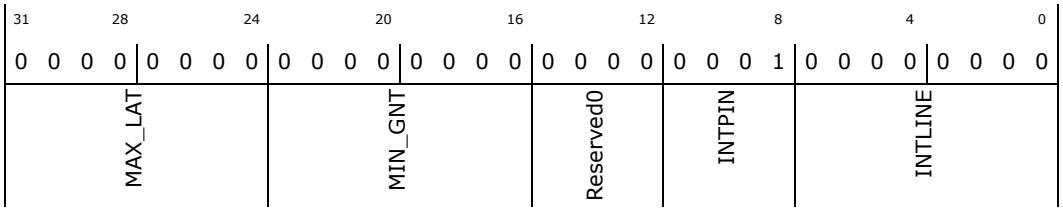
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space. For a single function device, this ideally is INTA.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

6.3.13 PowerManagement Capability ID Register (POWERCAPID)—Offset 80h

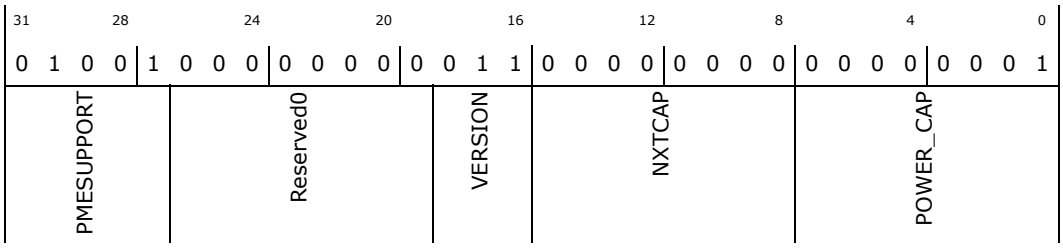
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 80h

Default: 48030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x9 RO	**PMESUPPORT:** PME_Support: This 5-bit field indicates the power states in which the function can assert the PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal at the same time in that power state. bit(11) X XXX1b: PME# can be asserted from D0 bit(12) X XX1Xb: PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb: PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb:PME# can be asserted from D3hot bit(15) 1 XXXXb:PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the private configuration space PME_Support XORed with the PME_Support strap.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

6.3.14 Power Management Control and Status Register (PMECTRLSTATUS)—Offset 84h

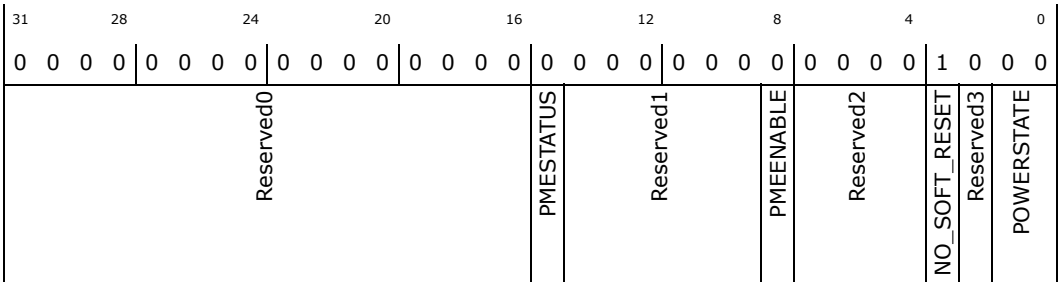
PMECTRLSTATUS: Power Management Control and Status

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 Software clears the bit by writing a 1 to it. 1 This bit is set when the PME# signal is asserted independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: 1 Enables the function to assert PME#. 0 PME# message on Sideband is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state and to set a new power state. The values are: 00 D0 state 11 D3HOT state Others Reserved Note: If the software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally. The data is discarded and no state change occurs. Note: When in the D3HOT states, interrupts are blocked. Note: D3Hot cannot be used for downstream decode on fabric ports.

6.3.15 General Purpose Read Write Register1 (GEN_REGRW1)—Offset A0h

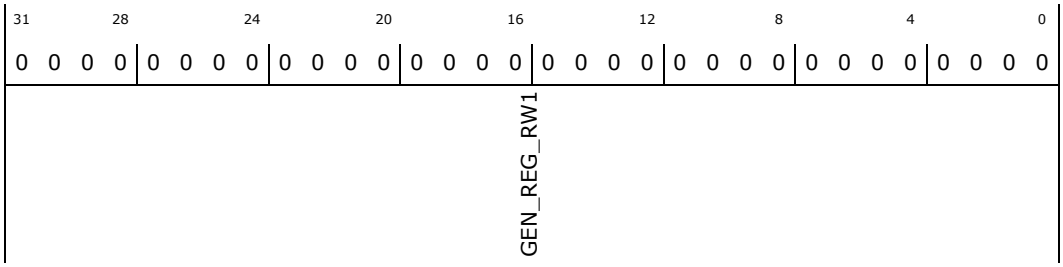
General Purpose Read Write Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW1:** General Purpose PCIRegister: This register value is brought out as oob_gen_pci_reg1 out of band signal

6.3.16 General Purpose Read Write Register2 (GEN_REGRW2)—Offset A4h

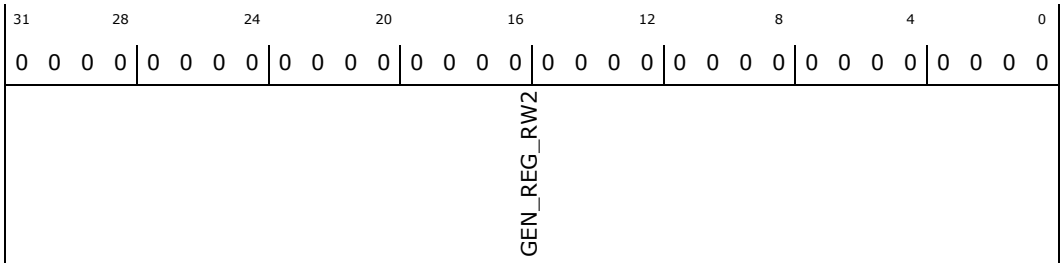
General Purpose Read Write Register2

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW2:** General Purpose PCI Register: This register value is brought out as oob_gen_pci_reg2 Out of Band signal

6.3.17 General Purpose Read Write Register3 (GEN_REGRW3)—Offset A8h

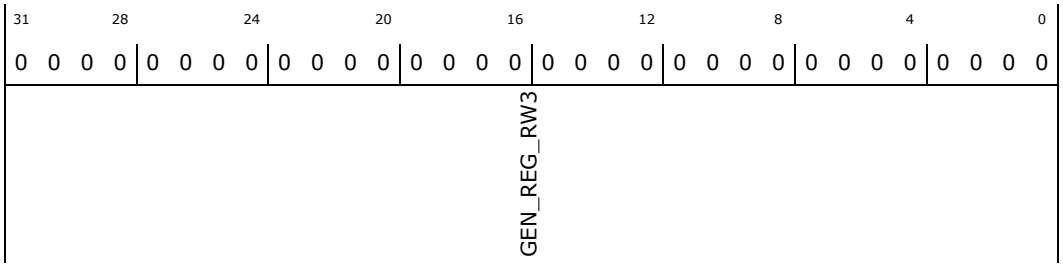
General Purpose Read Write Register3

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW3:** General Purpose PCI Register: This register value is brought out as oob_gen_pci_reg3 Out of Band signal

6.3.18 General Purpose Read Write Register4 (GEN_REGRW4)—Offset ACh

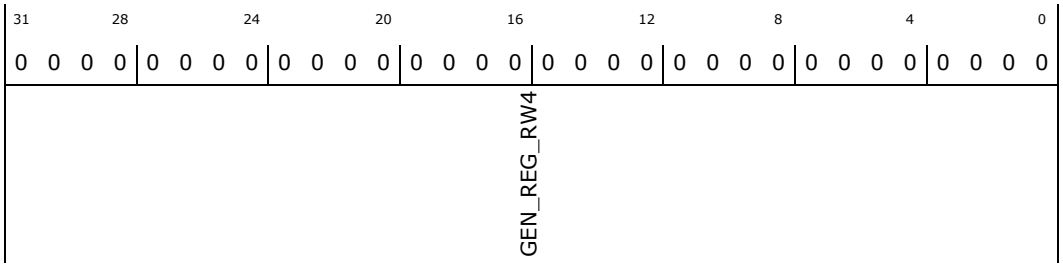
General Purpose Read Write Register4

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW4:** General Purpose PCI Register: This register value is brought out as oob_gen_pci_reg4 Out of Band signal

6.3.19 General Purpose Input Register (GEN_INPUT_REG)—Offset C0h

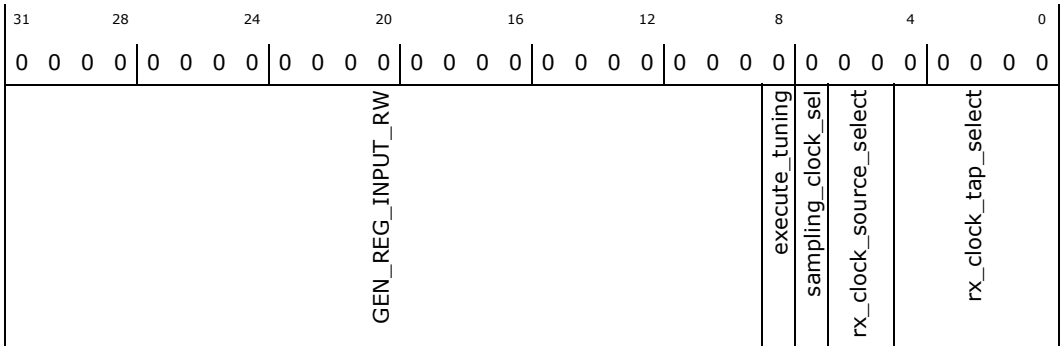
General Purpose Input Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**GEN_REG_INPUT_RW:** Reserved.
8	0x0 RO	**execute_tuning:** Execute Tuning. This is intended for debug use only.
7	0x0 RO	**sampling_clock_sel:** Sampling Clock Select. This is intended for debug use only.
6:5	0x0 RO	**rx_clock_source_select:** Rx Clock Source Select: 00: loopback clock 01: SDR50 10: DDR50 11: tuned clock This is intended only for debug use.
4:0	0x0 RO	**rx_clock_tap_select:** Rx Clock Tap Select: This indicates which tap select the host controller's tuning algorithm settled on. This is intended only for debug use.

6.3.20 Manufacturers ID Register (MANID)—Offset F8h

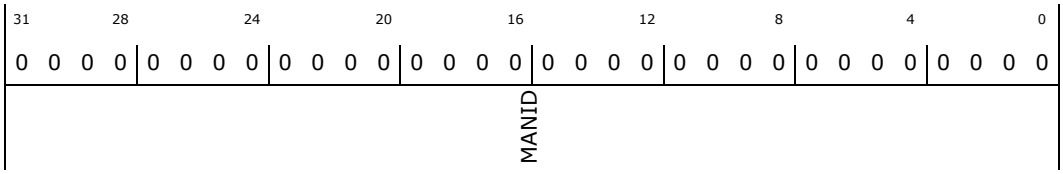
Manufacturers ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:17, F:0] + F8h

Default: 00000000h

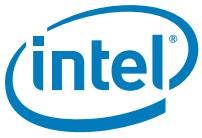


Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: Default value comes from straps. This value can be updated from SetIDValue Message

6.4 SDIO 1 Memory Mapped I/O Registers

Table 35. Summary of SDIO 1 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"SDMA System Address Register (SYS_ADR)—Offset 0h" on page 1966	00000000h
4–5h	2	"Block Size Register (BLK_SIZE)—Offset 4h" on page 1966	0000h
6–7h	2	"Block Count Register (BLK_COUNT)—Offset 6h" on page 1967	0000h
8–Bh	4	"Argument Register (ARGUMENT)—Offset 8h" on page 1968	00000000h
C–Dh	2	"Transfer Mode Register (TX_MODE)—Offset Ch" on page 1968	0000h
E–Fh	2	"Command Register (CMD)—Offset Eh" on page 1969	0000h
10–13h	4	"Response Register0 (RESPONSE0)—Offset 10h" on page 1970	00000000h
14–17h	4	"Response Register2 (RESPONSE2)—Offset 14h" on page 1971	00000000h
18–1Bh	4	"Response Register4 (RESPONSE4)—Offset 18h" on page 1971	00000000h
1C–1Fh	4	"Response Register6 (RESPONSE6)—Offset 1Ch" on page 1972	00000000h
20–23h	4	"Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h" on page 1973	00000000h
24–27h	4	"Present State Register (PRE_STATE)—Offset 24h" on page 1973	1FFF0000h
28–28h	1	"Host Control Register (HOST_CTL)—Offset 28h" on page 1974	00h
29–29h	1	"Power Control Register (PWR_CTL)—Offset 29h" on page 1975	01h
2A–2Ah	1	"Block Gap Control Register (BLK_GAP_CTL)—Offset 2Ah" on page 1976	80h
2B–2Bh	1	"Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh" on page 1977	00h
2C–2Dh	2	"Clock Control Register (CLK_CTL)—Offset 2Ch" on page 1978	0000h
2E–2Eh	1	"Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh" on page 1978	00h
2F–2Fh	1	"Software Reset Register (SW_RST)—Offset 2Fh" on page 1979	00h
30–31h	2	"Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h" on page 1980	0000h
32–33h	2	"Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h" on page 1981	0000h
34–35h	2	"Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h" on page 1982	0000h
36–37h	2	"Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h" on page 1983	0000h
38–39h	2	"Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h" on page 1985	0000h
3A–3Bh	2	"Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah" on page 1986	0000h
3C–3Fh	4	"Auto CMD12 Error Status Register and Host control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch" on page 1987	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40–43h	4	"Capabilities Register (CAPABILITIES)—Offset 40h" on page 1989	446CC8B2h
44–47h	4	"Capabilities Register 2 (CAPABILITIES_2)—Offset 44h" on page 1989	00000007h
48–4Bh	4	"Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h" on page 1990	00000000h
50–51h	2	"Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h" on page 1991	0000h
52–53h	2	"Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h" on page 1992	0000h
54–54h	1	"ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h" on page 1993	00h
58–5Bh	4	"ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h" on page 1993	00000000h
5C–5Fh	4	"ADMA System Address Register (ADMA_SYS_ADDR_HIGH)—Offset 5Ch" on page 1994	00000000h
60–63h	4	"Preset Values registers (PRESET_VALUE_0)—Offset 60h" on page 1994	00040004h
64–67h	4	"Preset Values 1 registers (PRESET_VALUE_1)—Offset 64h" on page 1995	00040002h
68–6Bh	4	"Preset Values 2 registers (PRESET_VALUE_2)—Offset 68h" on page 1995	00010002h
6C–6Fh	4	"Preset Values 3 registers (PRESET_VALUE_3)—Offset 6Ch" on page 1996	00020000h
70–73h	4	"BOOT_TIMEOUT_CTRL (BOOT_TIMEOUT_CTRL)—Offset 70h" on page 1996	00000000h
74–74h	1	"DEBUG_SEL (DEBUG_SEL)—Offset 74h" on page 1997	00h
E0–E3h	4	"Shared Bus Control Register (SHARED_BUS)—Offset E0h" on page 1997	00000000h
F0–F0h	1	"SPI_INT_SUP (SPI_INT_SUP)—Offset F0h" on page 1998	00h
FC–FDh	2	"Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh" on page 1998	0000h
FE–FFh	2	"Host Controller Version Register (HOST_CTRL_VER)—Offset FEh" on page 1999	1002h

6.4.1 SDMA System Address Register (SYS_ADR)—Offset 0h

This register contains the physical system memory address used for DMA transfers

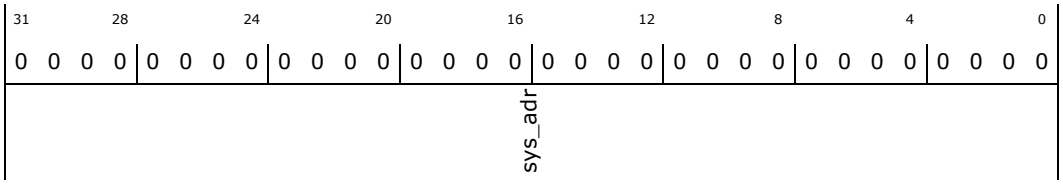
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SYS_ADR (sys_adr):** SDMA System Address This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value. The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at the every boundary specified by the Host SDMA Buffer Boundary in the Block Size register. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register (003h) is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by the Resume command or by setting Continue Request in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register. ADMA does not use this register.

6.4.2 Block Size Register (BLK_SIZE)—Offset 4h

This register is used to configure the number of bytes in a data block.

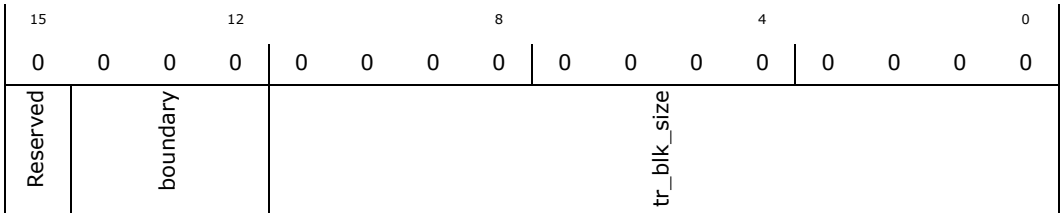
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**Reserved:** Reserved
14:12	0x0 RW	**BOUNDARY (boundary):** Host SDMA Buffer Boundary The large contiguous memory space may not be available in the virtual memory system. To perform long SDMA transfer, SDMA System Address register shall be updated at every system memory boundary during SDMA transfer. These bits specify the size of contiguous buffer in the system memory. The SDMA transfer shall wait at the every boundary specified by these fields and the Host Controller generates the DMA Interrupt to request the Host Driver to update the SDMA System Address register. At the end of transfer, the Host Controller may issue or may not issue DMA Interrupt. In particular, DMA Interrupt shall not be issued after Transfer Complete Interrupt is issued. In case of this register is set to 0 (buffer size = 4K bytes), lower 12-bit of byte address points data in the contiguous buffer and the upper 20-bit points the location of the buffer in the system memory. The SDMA transfer stops when the Host Controller detects carry out of the address from bit 11 to 12. These bits shall be supported when the SDMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. ADMA does not use this register. 000b - 4K bytes (Detects A11 carry out) 001b - 8K bytes (Detects A12 carry out) 010b - 16K Bytes (Detects A13 carry out) 011b - 32K Bytes (Detects A14 carry out) 100b - 64K bytes (Detects A15 carry out) 101b - 128K Bytes (Detects A16 carry out) 110b - 256K Bytes (Detects A17 carry out) 111b - 512K Bytes (Detects A18 carry out)
11:0	0x0 RW	**TR_BLK_SIZE (tr_blk_size):** Transfer Block Size This register specifies the block size of data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. Values ranging from 1 up to the maximum buffer size can be set. In case of memory, it shall be set up to 512 bytes (Refer to Implementation Note in Section 1.7.2). It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value, and write operations shall be ignored. 0800h 2048 Bytes ... ... 0200h 512 Bytes 01FFh 511 Bytes ... ... 0004h 4 Bytes 0003h 3 Bytes 0002h 2 Bytes 0001h 1 Byte 0000h No data transfer

6.4.3 Block Count Register (BLK_COUNT)—Offset 6h

This register is used to configure the number of data blocks

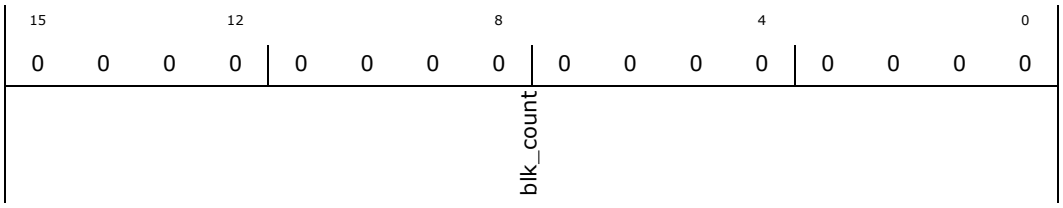
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 6h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW	**BLK_COUNT (blk_count):** Blocks Count For Current Transfer This register is enabled when Block Count Enable in the Transfer Mode register is set to 1 and is valid only for multiple block transfers

6.4.4 Argument Register (ARGUMENT)—Offset 8h

This register contains the SD Command Argument.

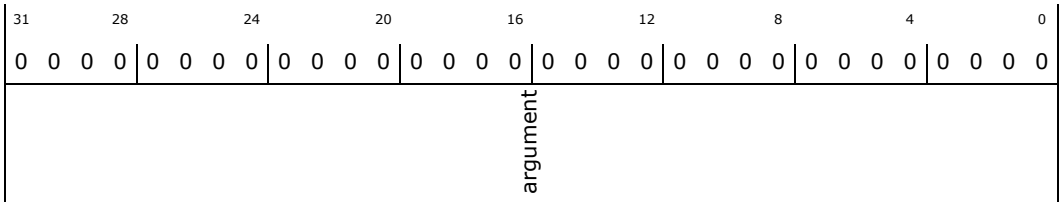
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**ARGUMENT (argument):** Command Argument The SD Command Argument is specified as bit39-8 of Command-Format in the Physical Layer Specification.

6.4.5 Transfer Mode Register (TX_MODE)—Offset Ch

Transfer Mode Register

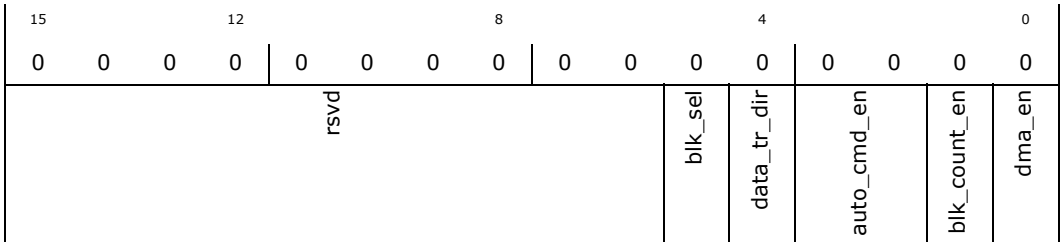
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:6	0x0 RO	**RSVD (rsvd):** Reserved
5	0x0 RW	**BLK_SEL (blk_sel):** Multi / Single Block Select This bit is set when issuing multiple-block transfer commands using DAT line. For any other commands, this bit shall be set to 0. If this bit is 0, it is not necessary to set the Block Count register. (Refer to Table 2-8) 1 Multiple Block 0 Single Block
4	0x0 RW	**Data_TR_Dir (data_tr_dir):** Data Transfer Direction Select This bit defines the direction of DAT line data transfers. The bit is set to 1 by the Host Driver to transfer data from the SD card to the SD Host Controller and it is set to 0 for all other commands. 1 Read (Card to Host) 0 Write (Host to Card)
3:2	0x0 RW	**AUTO_CMD_EN (auto_cmd_en):** This field determines use of auto command functions 00b - Auto Command Disabled 01b - Auto CMD12 Enable 10b - Auto CMD23 Enable 11b - Reserved
1	0x0 RW	**BLK_COUNT_EN (blk_count_en):** Block Count Enable This bit is used to enable the Block Count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. (Refer to Table 2-8) If ADMA2 data transfer is more than 65535 blocks, this bit shall be set to 0. In this case, data transfer length is designated by Descriptor Table. 1 Enable 0 Disable
0	0x0 RW	**DMA_EN (dma_en):** DMA Enable This bit enables DMA functionality as described in section 1.4. DMA can be enabled only if it is supported as indicated in the Capabilities register. One of the DMA modes can be selected by DMA Select in the Host Control register. If DMA is not supported, this bit is meaningless and shall always read 0. If this bit is set to 1, a DMA operation shall begin when the Host Driver writes to the upper byte of Command register (00Fh). 1 DMA Data transfer 0 No data transfer or Non DMA data transfer

6.4.6 Command Register (CMD)—Offset Eh

Command Register

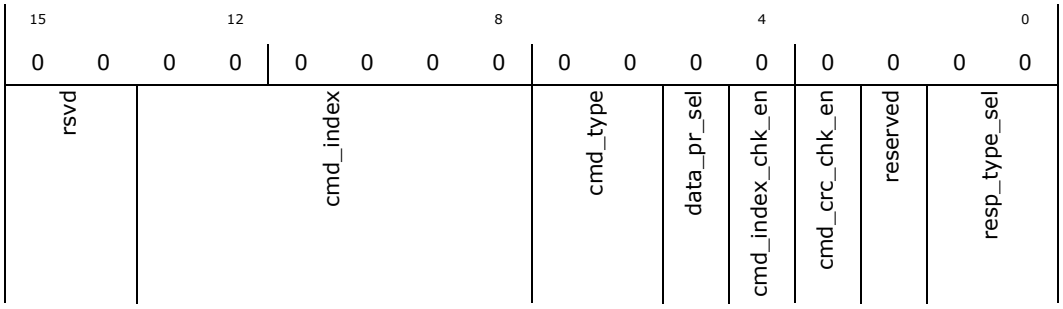
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RO	**RSVD (rsvd):** Reserved
13:8	0x0 RW	**CMD_INDEX (cmd_index):** Command Index These bits shall be set to the command number (CMD0-63, ACMD0-63) that is specified in bits 45-40 of the Command-Format in the Physical Layer Specification and SDIO Card Specification.
7:6	0x0 RW	**CMD_TYPE (cmd_type):** Command Type
5	0x0 RW	**DATA_PR_SEL (data_pr_sel):** Data Present Select This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. It is set to 0 for the following: (1) Commands using only CMD line (ex. CMD52). (2) Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b ex. CMD38) (3) Resume command 1 Data Present 0 No Data Present
4	0x0 RW	**CMD_INDEX_CHK_EN (cmd_index_chk_en):** Command Index Check Enable If this bit is set to 1, the Host Controller shall check the Index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked. 1 Enable 0 Disable
3	0x0 RW	**CMD_CRC_CHK_EN (cmd_crc_chk_en):** Command CRC Check Enable If this bit is set to 1, the Host Controller shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. The position of CRC field is determined according to the length of the response. (Refer to definition in D01-00 and Table 2-10 below.) 1 Enable 0 Disable
2	0x0 RO	**Reserved (reserved):** Reserved
1:0	0x0 RW	**RESP_TYPE_SEL (resp_type_sel):** Response Type Select 00 No Response 01 Response Length 136 10 Response Length 48 11 Response Length 48 check Busy after response

6.4.7 Response Register0 (RESPONSE0)—Offset 10h

This register is used to store responses from SD cards

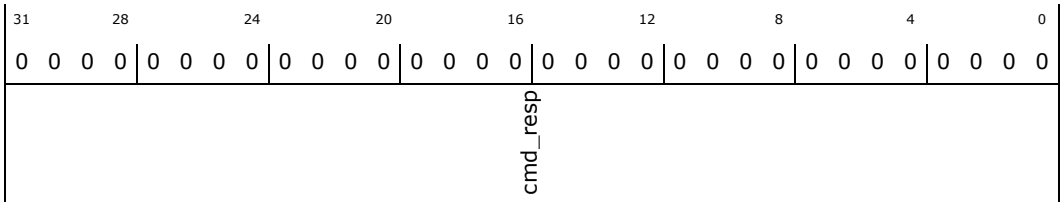
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**CMD_RESP0 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

6.4.8 Response Register2 (RESPONSE2)—Offset 14h

This register is used to store responses from SD cards

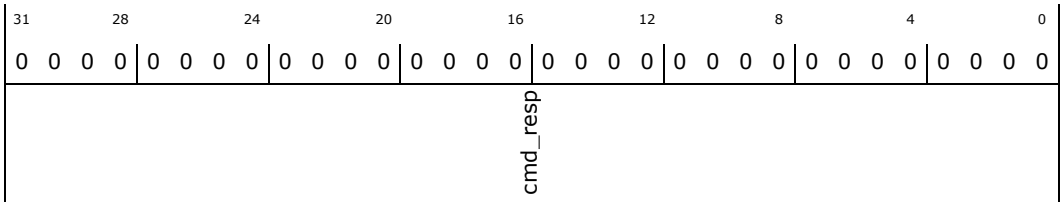
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**CMD_RESP2 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

6.4.9 Response Register4 (RESPONSE4)—Offset 18h

This register is used to store responses from SD cards

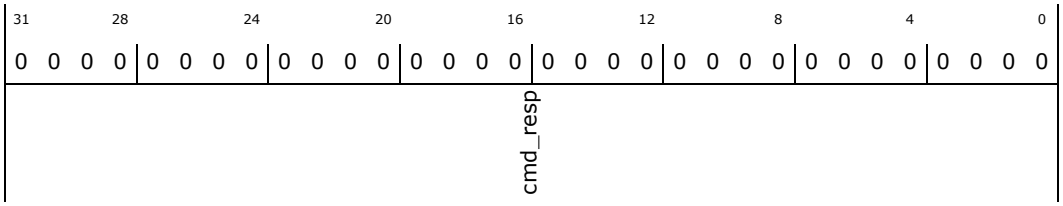
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**CMD_RESP4 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

6.4.10 Response Register6 (RESPONSE6)—Offset 1Ch

This register is used to store responses from SD cards

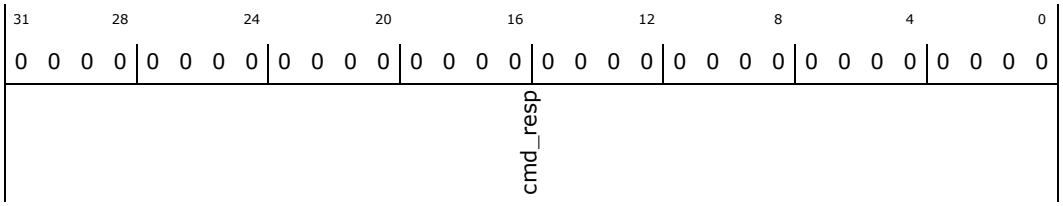
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**CMD_RESP6 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

6.4.11 Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h

32-bit data port register to access internal buffer

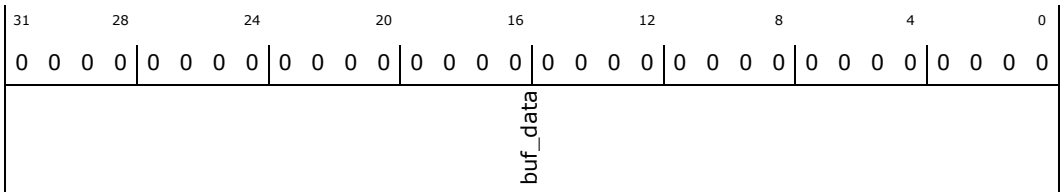
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**BUF_DATA (buf_data):** Buffer Data The Host Controller buffer can be accessed through this 32-bit Data Port register. RW depends on read or write transfer, it doesn't mean what's written can be read back

6.4.12 Present State Register (PRE_STATE)—Offset 24h

The Host Driver can get status of the Host Controller from this 32-bit read only register

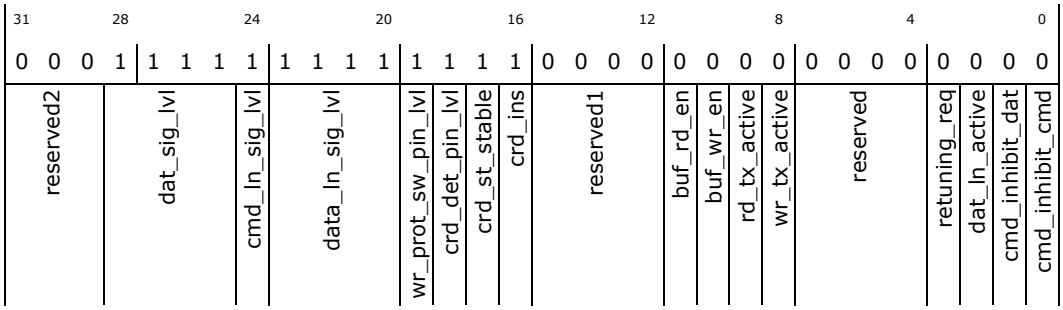
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 1FFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**Reserved2 (reserved2):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
28:25	0xf RO	**DAT_SIG_LVL (dat_sig_lvl):** This status is used to check DAT line level to recover from errors, and for debugging. D28 - DAT[7] D27 - DAT[6] D26 - DAT[5] D25 - DAT[4]
24	0x1 RO	**CMD_LN_SIG_LVL (cmd_ln_sig_lvl):** CMD Line Signal Level This status is used to check the CMD line level to recover from errors, and for debugging.
23:20	0xf RO	**DATA_LN_SIG_LVL (data_ln_sig_lvl):** DAT[3:0] Line Signal Level This status is used to check the DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. D23 DAT[3] D22 DAT[2] D21 DAT[1] D20 DAT[0]
19	0x1 RO	**WR_PROT_SW_PIN_LVL (wr_prot_sw_pin_lvl):** Write Protect Switch Pin Level
18	0x1 RO	**CRD_DET_PIN_LVL (crd_det_pin_lvl):** Card Detect Pin Level
17	0x1 RO	**CRD_ST_STABLE (crd_st_stable):** Card State Stable
16	0x1 RO	**CRD_INS (crd_ins):** Card Inserted
15:12	0x0 RO	**Reserved1 (reserved1):** Reserved
11	0x0 RO	**BUF_RD_EN (buf_rd_en):** Buffer Read Enable
10	0x0 RO	**BUF_WR_EN (buf_wr_en):** Buffer Write Enable
9	0x0 RO	**RD_TX_ACTIVE (rd_tx_active):** Read Transfer Active
8	0x0 RO	**WR_TX_ACTIVE (wr_tx_active):** Write Transfer Active
7:4	0x0 RO	**Reserved (reserved):** Reserved
3	0x0 RO	**RETUNING_REQ (retuning_req):** Re-Tuning Request
2	0x0 RO	**DAT_LN_ACTIVE (dat_ln_active):** DAT Line Active
1	0x0 RO	**CMD_INHIBIT_DAT (cmd_inhibit_dat):** Command Inhibit (DAT)
0	0x0 RO	**CMD_INHIBIT_CMD (cmd_inhibit_cmd):** Command Inhibit (CMD)

6.4.13 Host Control Register (HOST_CTL)—Offset 28h

Host Control Register

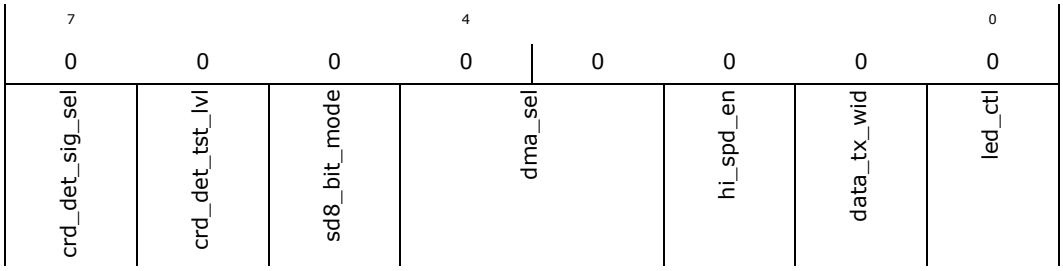
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW	**CRD_DET_SIG_SEL (crd_det_sig_sel):** Card Detect Signal Selection
6	0x0 RW	**CRD_DET_TST_LVL (crd_det_tst_lvl):** Card Detect Test Level
5	0x0 RW	**SD8_BIT_MODE (sd8_bit_mode):** This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card.
4:3	0x0 RW	**DMA_SEL (dma_sel):** DMA Select
2	0x0 RW	**HI_SPD_EN (hi_spd_en):** High Speed Enable
1	0x0 RW	**DATA_TX_WID (data_tx_wid):** Data Transfer Width
0	0x0 RW	**LED_CTL (led_ctl):** LED Control

6.4.14 Power Control Register (PWR_CTL)—Offset 29h

Power Control Register

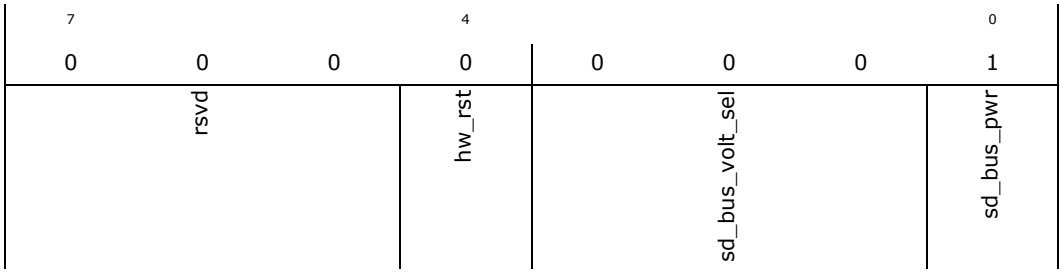
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 29h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 01h



Bit Range	Default & Access	Field Name (ID): Description
7:5	0x0 RO	**RSVD (rsvd):** Reserved
4	0x0 RW	**HW_rst (hw_rst):** HW reset
3:1	0x0 RW	**SD_BUS_VOLT_SEL (sd_bus_volt_sel):** SD Bus Voltage Select
0	0x1 RW	**SD_BUS_PWR (sd_bus_pwr):** SD Bus Power

6.4.15 Block Gap Control Register (BLK_GAP_CTL)—Offset 2Ah

Block Gap Control Register

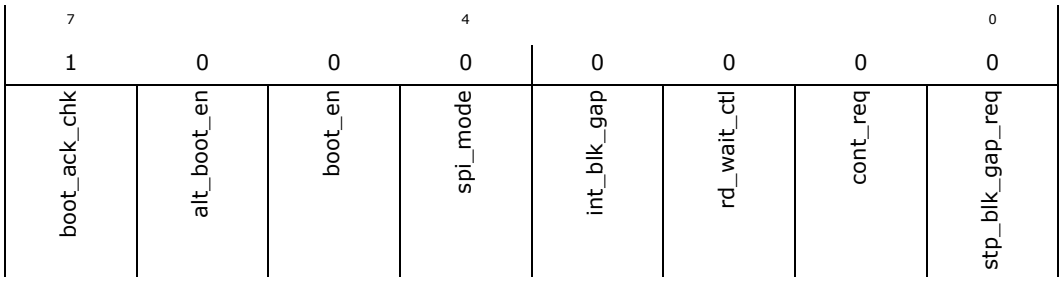
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 2Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7	0x1 RW	**BOOT_ACK_CHK (boot_ack_chk):** To check for the boot acknowledge in boot operation; 0 = Will not wait for boot ack from eMMC card; 1 = Wake for boot ack from eMMC card
6	0x0 RW	**ALT_BOOT_EN (alt_boot_en):** To start boot code access in alternative mode; 0 = To stop alternate boot mode access; 1 = To start alternate boot mode access

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**BOOT_EN (boot_en):** To start boot code access; 0 = To stop boot code access; 1 = To start boot code access
4	0x0 RW	**SPI_MODE (spi_mode):** SPI mode enable bit; 0 = SD mode; 1 = SPI mode
3	0x0 RW	**INT_BLK_GAP (int_blk_gap):** Interrupt At Block Gap
2	0x0 RW	**RD_WAIT_CTL (rd_wait_ctl):** Read Wait Control
1	0x0 RW	**CONT_REQ (cont_req):** Continue Request
0	0x0 RW	**STP_BLK_GAP_REQ (stp_blk_gap_req):** Stop At Block Gap Request

6.4.16 Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh

This register is used for wakeup event control.

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

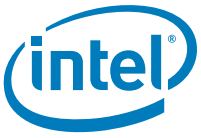
Offset: [BAR] + 2Bh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd					wakeup_en_sd_rm	wakeup_en_sd_ins	wakeup_en_crd_int

Bit Range	Default & Access	Field Name (ID): Description
7:3	0x0 RO	**RSVD (rsvd):** Reserved
2	0x0 RW	**WAKEUP_EN_SD_RM (wakeup_en_sd_rm):** Wakeup Event Enable On SD Card Removal
1	0x0 RW	**WAKEUP_EN_SD_INS (wakeup_en_sd_ins):** Wakeup Event Enable On SD Card Insertion
0	0x0 RW	**WAKEUP_EN_CRD_INT (wakeup_en_crd_int):** Wakeup Event Enable On Card Interrupt



6.4.17 Clock Control Register (CLK_CTL)—Offset 2Ch

This register is used configure the frequency of the SDIO controller, and enable the clock.

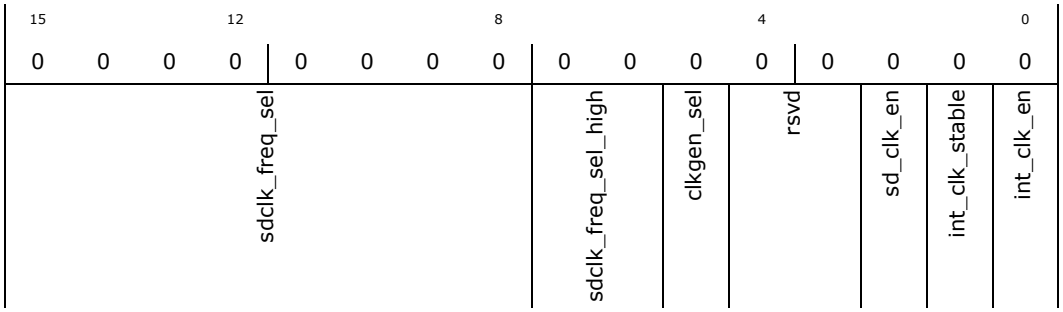
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RW	**SDCLK_FREQ_SEL (sdclk_freq_sel):** SDCLK Frequency Select
7:6	0x0 RW	**SDCLK_FREQ_SEL_HIGH (sdclk_freq_sel_high):** Bit 07-06 is assigned to bit 09-08 of clock divider in SDCLK Frequency Select
5	0x0 RW	**CLKGEN_SEL (clkgen_sel):** This bit is used to select the clock generator mode in SDCLK Frequency Select. 1: Programmable Clock Mode, 0: Divided Clock Mode
4:3	0x0 RO	**RSVD (rsvd):** Reserved
2	0x0 RW	**SD_CLK_EN (sd_clk_en):** SD Clock Enable
1	0x0 RO	**INT_CLK_STABLE (int_clk_stable):** Internal Clock Stable
0	0x0 RW	**INT_CLK_EN (int_clk_en):** Internal Clock Enable

6.4.18 Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh

Timeout Control Register

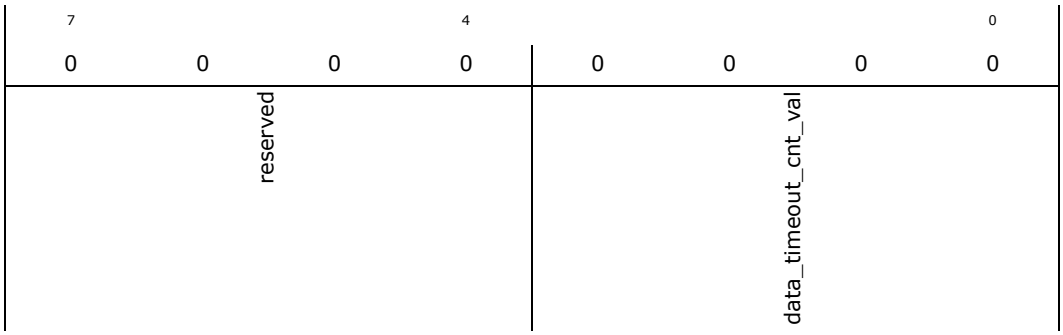
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 2Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RO	**Reserved (reserved):** Reserved
3:0	0x0 RW	**DATA_TIMEOUT_CNT_VAL (data_timeout_cnt_val):** Data Timeout Counter Value

6.4.19 Software Reset Register (SW_RST)—Offset 2Fh

Software Reset Register

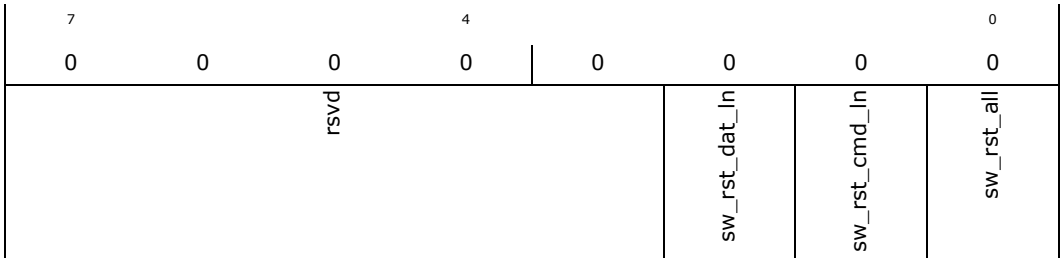
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 2Fh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0x0 RO	**RSVD (rsvd):** Reserved
2	0x0 RW	**SW_RST_DAT_LN (sw_rst_dat_ln):** Software Reset For DAT Line
1	0x0 RW	**SW_RST_CMD_LN (sw_rst_cmd_ln):** Software Reset For CMD Line
0	0x0 RW	**SW_RST_ALL (sw_rst_all):** Software Reset For All

6.4.20 Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h

Normal Interrupt Status Register

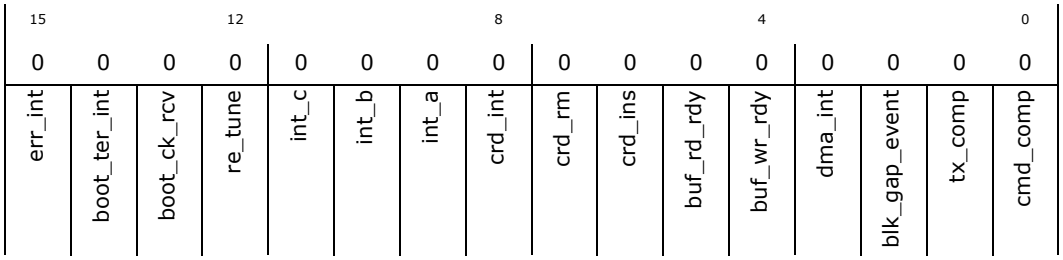
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**ERR_INT (err_int):** Error Interrupt
14	0x0 RW/1C	**BOOT_TER_INT (boot_ter_int):** boot ter int
13	0x0 RW/1C	**BOOT_ACK_RCV (boot_ck_rcv):** boot ack rcv
12	0x0 RO	**RE_TUNE (re_tune):** re tunning event
11	0x0 RO	**INT_C (int_c):** int c
10	0x0 RO	**INT_B (int_b):** int b
9	0x0 RO	**INT_A (int_a):** int a
8	0x0 RO	**CRD_INT (crd_int):** Card Interrupt
7	0x0 RW/1C	**CRD_RM (crd_rm):** Card Removal
6	0x0 RW/1C	**CRD_INS (crd_ins):** Card Insertion
5	0x0 RW/1C	**BUF_RD_RDY (buf_rd_rdy):** Buffer Read Ready
4	0x0 RW/1C	**BUF_WR_RDY (buf_wr_rdy):** Buffer Write Ready
3	0x0 RW/1C	**DMA_INT (dma_int):** DMA Interrupt

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW/1C	**BLK_GAP_EVENT (blk_gap_event):** Block Gap Event
1	0x0 RW/1C	**TX_COMP (tx_comp):** Transfer Complete
0	0x0 RW/1C	**CMD_COMP (cmd_comp):** Command Complete

6.4.21 Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h

Error Interrupt Status Register

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 32h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
vend_spec_err_status	boot_cmd_timeout_err	ceata_err	tgt_rsp_err	rsvd	tuning_err	adma_err	cmd12_err	cur_limit_err	data_end_bit_err	data_crc_err	data_timeout_err	cmd_index_err	cmd_end_bit_err	cmd_crc_err	cmd_timeout_err

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**VEND_SPEC_ERR_STATUS (vend_spec_err_status):** Vendor Specific Error Status
14	0x0 RO	**BOOT_CMD_TIMEOUT_ERR (boot_cmd_timeout_err):** Occur if the boot are access command is issued to the agent which has no permission to access the boot area.
13	0x0 RO	**CEATA_ERR (ceata_err):** Occurs when ATA command termination has occured due to an error condition the device has encountered.
12	0x0 RW/1C	**TGT_RSP_ERR (tgt_rsp_err):** Occurs when detecting ERROR in m_hresp(dma transaction)
11	0x0 RO	**RSVD (rsvd):** Reserved
10	0x0 RO	**TUNING_ERR (tuning_err):** Tuning Error

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RW/1C	**ADMA_ERR (adma_err):** ADMA Error
8	0x0 RW/1C	**CMD12_ERR (cmd12_err):** Auto CMD12 Error
7	0x0 RW/1C	**CUR_LIMIT_ERR (cur_limit_err):** Current Limit Error
6	0x0 RW/1C	**DATA_END_BIT_ERR (data_end_bit_err):** Data End Bit Error
5	0x0 RW/1C	**DATA_CRC_ERR (data_crc_err):** Data CRC Error
4	0x0 RW/1C	**DATA_TIMEOUT_ERR (data_timeout_err):** Data Timeout Error
3	0x0 RW/1C	**CMD_INDEX_ERR (cmd_index_err):** Command Index Error
2	0x0 RW/1C	**CMD_END_BIT_ERR (cmd_end_bit_err):** Command End Bit Error
1	0x0 RW/1C	**CMD_CRC_ERR (cmd_crc_err):** Command CRC Error
0	0x0 RW/1C	**CMD_TIMEOUT_ERR (cmd_timeout_err):** Command Timeout Error

6.4.22 Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h

Normal Interrupt Status Enable

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
fixed_0	boot_term_int_en	boot_ack_rcv_en	re_tune_en	int_c_en	int_b_en	int_a_en	crd_int_stat_en	crd_rm_stat_en	crd_ins_stat_en	buf_rd_rdy_stat_en	buf_wr_rdy_stat_en	dma_int_stat_en	blk_gap_event_stat_en	tx_comp_stat_en	cmd_comp_stat_en

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**FIXED_0 (fixed_0):** Fixed to 0
14	0x0 RW	**BOOT_TERM_INT_EN (boot_term_int_en):** 0 - Masked
13	0x0 RW	**BOOT_ACK_RCV_EN (boot_ack_rcv_en):** 0 -Masked
12	0x0 RW	**RE_TUNE_EN (re_tune_en):** re tunning event enable
11	0x0 RW	**INT_C_EN (int_c_en):** int c enable
10	0x0 RW	**INT_B_EN (int_b_en):** int b enable
9	0x0 RW	**INT_A_EN (int_a_en):** int a enable
8	0x0 RW	**CRD_INT_STAT_EN (crd_int_stat_en):** Card Interrupt Status Enable
7	0x0 RW	**CRD_RM_STAT_EN (crd_rm_stat_en):** Card Removal Status Enable
6	0x0 RW	**CRD_INS_STAT_EN (crd_ins_stat_en):** Card Insertion Status Enable
5	0x0 RW	**BUF_RD_RDY_STAT_EN (buf_rd_rdy_stat_en):** Buffer Read Ready Status Enable
4	0x0 RW	**BUF_WR_RDY_STAT_EN (buf_wr_rdy_stat_en):** Buffer Write Ready Status Enable
3	0x0 RW	**DMA_INT_STAT_EN (dma_int_stat_en):** DMA Interrupt Status Enable
2	0x0 RW	**BLK_GAP_EVENT_STAT_EN (blk_gap_event_stat_en):** Block Gap Event Status Enable
1	0x0 RW	**TX_COMP_STAT_EN (tx_comp_stat_en):** Transfer Complete Status Enable
0	0x0 RW	**CMD_COMP_STAT_EN (cmd_comp_stat_en):** Command Complete Status Enable

6.4.23 Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h

Error Interrupt Status Enable Register

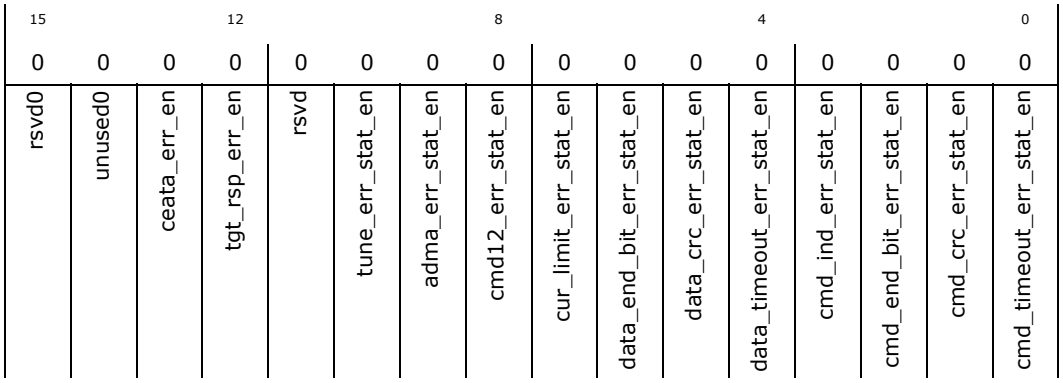
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 36h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**RSVD0 (rsvd0):** Reserved
14	0x0 RW	**UNUSED0 (unused0):** Unused
13	0x0 RW	**CEATA_ERR_EN (ceata_err_en):** 0 - masked
12	0x0 RW	**TGT_RSP_ERR_EN (tgt_rsp_err_en):** 0 - masked
11	0x0 RO	**RSVD (rsvd):** Reserved
10	0x0 RW	**TUNE_ERR_STATE_EN (tune_err_stat_en):** 0 - masked
9	0x0 RW	**ADMA_ERR_STAT_EN (adma_err_stat_en):** ADMA Error Status Enable
8	0x0 RW	**CMD12_ERR_STAT_EN (cmd12_err_stat_en):** Auto CMD12 Error Status Enable
7	0x0 RW	**CUR_LIMIT_ERR_STAT_EN (cur_limit_err_stat_en):** Current Limit Error Status Enable
6	0x0 RW	**DATA_END_BIT_ERR_STAT_EN (data_end_bit_err_stat_en):** Data End Bit Error Status Enable
5	0x0 RW	**DATA_CRC_ERR_STAT_EN (data_crc_err_stat_en):** Data CRC Error Status Enable
4	0x0 RW	**DATA_TIMEOUT_ERR_STAT_EN (data_timeout_err_stat_en):** Data Timeout Error Status Enable
3	0x0 RW	**CMD_IND_ERR_STAT_EN (cmd_ind_err_stat_en):** Command Index Error Status Enable
2	0x0 RW	**CMD_END_BIT_ERR_STAT_EN (cmd_end_bit_err_stat_en):** Command End Bit Error Status Enable
1	0x0 RW	**CMD_CRC_ERR_STAT_EN (cmd_crc_err_stat_en):** Command CRC Error Status Enable
0	0x0 RW	**CMD_TIMEOUT_ERR_STAT_EN (cmd_timeout_err_stat_en):** Command Timeout Error Status Enable

6.4.24 Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h

Normal Interrupt Signal Enable Register

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
fixed_0	boot_term_int_sig_en	boot_ack_rcv_sig_en	re_tune_sig_en	int_c_sig_en	int_b_sig_en	int_a_sig_en	crd_int_sig_en	crd_rm_sig_en	crd_ins_sig_en	buf_rd_rdy_sig_en	buf_wr_rdy_sig_en	dma_int_sig_en	blk_gap_event_sig_en	tx_comp_sig_en	cmd_comp_sig_en

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**FIXED_0 (fixed_0):** Fixed to 0
14	0x0 RW	**BOOT_TERM_INT_SIG_EN (boot_term_int_sig_en):** 0 - masked
13	0x0 RW	**BOOT_ACK_RCV_SIG_EN (boot_ack_rcv_sig_en):** 0 - masked
12	0x0 RW	**RE_TUNE_SIG_EN (re_tune_sig_en):** re tunning event Signal Enable
11	0x0 RW	**INT_C_SIG_EN (int_c_sig_en):** int c Signal Enable
10	0x0 RW	**INT_B_SIG_EN (int_b_sig_en):** int b Signal Enable
9	0x0 RW	**INT_A_SIG_EN (int_a_sig_en):** int a Signal Enable
8	0x0 RW	**CRD_INT_SIG_EN (crd_int_sig_en):** Card Interrupt Signal Enable
7	0x0 RW	**CRD_RM_SIG_EN (crd_rm_sig_en):** Card Removal Signal Enable
6	0x0 RW	**CRD_INS_SIG_EN (crd_ins_sig_en):** Card Insertion Signal Enable
5	0x0 RW	**BUF_RD_RDY_SIG_EN (buf_rd_rdy_sig_en):** Buffer Read Ready Signal Enable
4	0x0 RW	**BUF_WR_RDY_SIG_EN (buf_wr_rdy_sig_en):** Buffer Write Ready Signal Enable

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**DMA_INT_SIG_EN (dma_int_sig_en):** DMA Interrupt Signal Enable
2	0x0 RW	**BLK_GAP_EVENT_SIG_EN (blk_gap_event_sig_en):** Block Gap Event Signal Enable
1	0x0 RW	**TX_COMP_SIG_EN (tx_comp_sig_en):** Transfer Complete Signal Enable
0	0x0 RW	**CMD_COMP_SIG_EN (cmd_comp_sig_en):** Command Complete Signal Enable

6.4.25 Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah

Error Interrupt Signal Enable Register

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 3Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0	unused0	ceata_err_sig_en	tgt_err_rsp_sig_en	rsvd	tune_err_sig	adma_err_sig_en	cmd12_err_sig_en	cur_limit_err_sig_en	data_end_bit_err_sig_en	data_crc_err_sig_en	data_timeout_err_stat_en	cmd_ind_err_stat_en	cmd_end_bit_err_stat_en	cmd_crc_err_stat_en	cmd_timeout_err_stat_en

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**RSVD0 (rsvd0):** Reserved
14	0x0 RW	**UNUSED0 (unused0):** Unused
13	0x0 RW	**CEATA_ERR_SIG_EN (ceata_err_sig_en):** 0 - masked
12	0x0 RW	**TGT_ERR_RSP_SIG_EN (tgt_err_rsp_sig_en):** 0 - masked
11	0x0 RO	**RSVD (rsvd):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RW	**TUNE_ERR_SIG (tune_err_sig):** 0 - masked
9	0x0 RW	**ADMA_ERR_SIG_EN (adma_err_sig_en):** ADMA Error Signal Enable
8	0x0 RW	**CMD12_ERR_SIG_EN (cmd12_err_sig_en):** Auto CMD12 Error Signal Enable
7	0x0 RW	**CUR_LIMIT_ERR_SIG_EN (cur_limit_err_sig_en):** Current Limit Error Signal Enable
6	0x0 RW	**DATA_END_BIT_ERR_SIG_EN (data_end_bit_err_sig_en):** Data End Bit Error Signal Enable
5	0x0 RW	**DATA_CRC_ERR_SIG_EN (data_crc_err_sig_en):** Data CRC Error Signal Enable
4	0x0 RW	**DATA_TIMEOUT_ERR_STAT_EN (data_timeout_err_stat_en):** Data Timeout Error Signal Enable
3	0x0 RW	**CMD_IND_ERR_STAT_EN (cmd_ind_err_stat_en):** Command Index Error Signal Enable
2	0x0 RW	**CMD_END_BIT_ERR_STAT_EN (cmd_end_bit_err_stat_en):** Command End Bit Error Signal Enable
1	0x0 RW	**CMD_CRC_ERR_STAT_EN (cmd_crc_err_stat_en):** Command CRC Error Signal Enable
0	0x0 RW	**CMD_TIMEOUT_ERR_STAT_EN (cmd_timeout_err_stat_en):** Command Timeout Error Signal Enable

6.4.26 Auto CMD12 Error Status Register and Host control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch

Auto CMD12 Error Status Register and Host control 2 Register

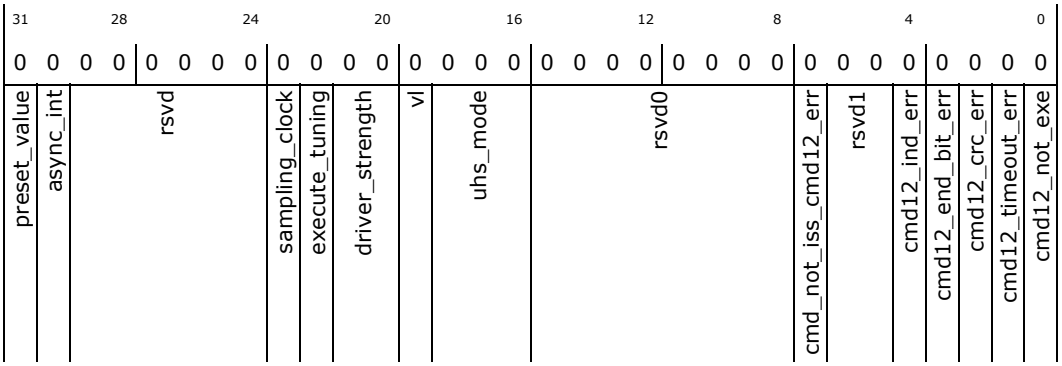
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**PRESET_VALUE (preset_value):** Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set to automatic This bit enables the functions defined in the Preset Value registers. 1 Automatic Selection by Preset Value are Enabled 0 SDCLK and Driver Strength are controlled by Host Driver If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver. If this bit is set to 1, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Controller as specified in the Preset Value registers.
30	0x0 RW	**ASYNC_INT (async_int):** This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode (and zero is set to Interrupt Pin Select in the Shared Bus Control register). If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card. 1 Enabled 0 Disabled
29:24	0x0 RO	**RSVD (rsvd):** Reserved
23	0x0 RW	**SAMPLING_CLOCK (sampling_clock):** This bit is set by tuning procedure when Execute Tuning is cleared
22	0x0 RW/AC	**EXECUTE_TUNING (execute_tuning):** This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by writing 0 for more detail about tuning procedure. 1 Execute Tuning 0 Not Tuned or Tuning Completed
21:20	0x0 RW	**DRIVER_STRENGTH (driver_strength):** Host Controller output driver in 1.8V signaling is selected by this bit
19	0x0 RW	**VL (vl):** This bit controls voltage regulator for I/O cell, 1 - 1.8V Signaling, 0 - 3.3V Signaling. This bit has to be set based on actual I/O signal voltage even though only a single voltage is supported in a platform
18:16	0x0 RW	**UHS_MODE (uhs_mode):** This field is used to select one of UHS-I modes

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**RSVD0 (rsvd0):** Reserved
7	0x0 RO	**CMD_NOT_ISS_CMD12_ERR (cmd_not_iss_cmd12_err):** Command Not Issued By Auto CMD12 Error
6:5	0x0 RO	**RSVD1 (rsvd1):** Reserved
4	0x0 RO	**CMD12_IND_ERR (cmd12_ind_err):** Auto CMD12 Index Error
3	0x0 RO	**CMD12_END_BIT_ERR (cmd12_end_bit_err):** Auto CMD12 End Bit Error
2	0x0 RO	**CMD12_CRC_ERR (cmd12_crc_err):** Auto CMD12 CRC Error
1	0x0 RO	**CMD12_TIMEOUT_ERR (cmd12_timeout_err):** Auto CMD12 Timeout Error
0	0x0 RO	**CMD12_NOT_EXE (cmd12_not_exe):** Auto CMD12 Not Executed

6.4.27 Capabilities Register (CAPABILITIES)—Offset 40h

Capabilities Register

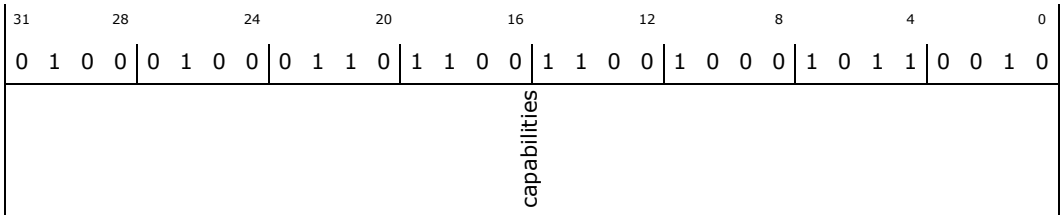
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 446CC8B2h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x446cc8b2 RO	**capabilities:** capabilities

6.4.28 Capabilities Register 2 (CAPABILITIES_2)—Offset 44h

Capabilities Register 2

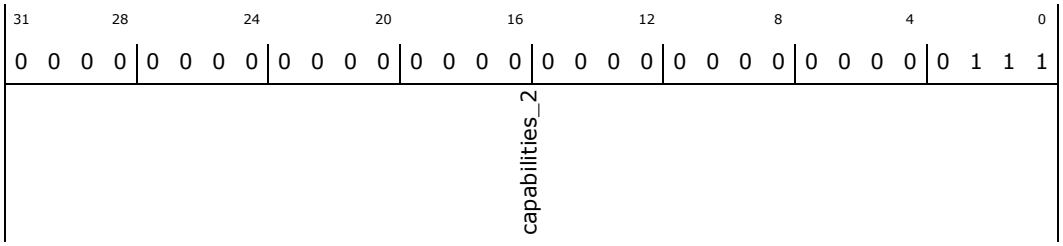
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000007h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x7 RO	**capabilities_2:** capabilities 2

6.4.29 Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h

These registers indicate maximum current capability for each voltage

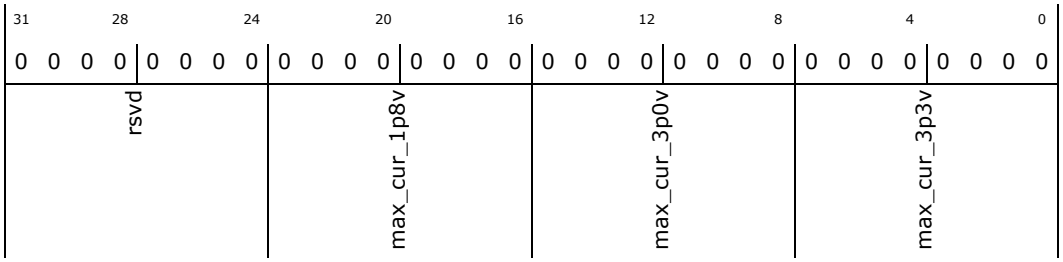
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD (rsvd):** Reserved
23:16	0x0 RO	**MAX_CUR_1p8V (max_cur_1p8v):** Maximum Current for 1.8V
15:8	0x0 RO	**MAX_CUR_3p0V (max_cur_3p0v):** Maximum Current for 3.0V

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**MAX_CUR_3p3V (max_cur_3p3v):** Maximum Current for 3.3V

6.4.30 Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h

Force Event Register for Auto CMD12 Error Status

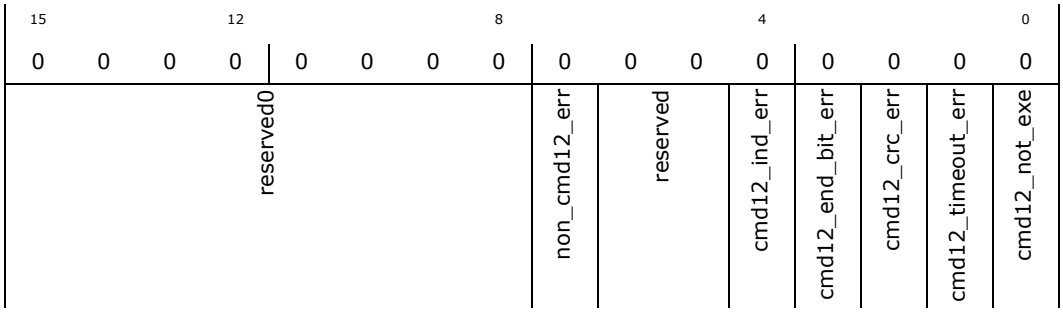
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Reserved0 (reserved0):** Reserved
7	0x0 WO	**NON_CMD12_ERR (non_cmd12_err):** Force Event for Command Not Issued By Auto CMD12 Error :
6:5	0x0 RO	**Reserved (reserved):** Reserved
4	0x0 WO	**CMD12_IND_ERR (cmd12_ind_err):** Force Event for Auto CMD12 Index Error
3	0x0 WO	**CMD12_END_BIT_ERR (cmd12_end_bit_err):** Force Event for Auto CMD12 End Bit Error
2	0x0 WO	**CMD12_CRC_ERR (cmd12_crc_err):** Force Event for Auto CMD12 CRC Error
1	0x0 WO	**CMD12_TIMEOUT_ERR (cmd12_timeout_err):** Force Event for Auto CMD12 Timeout Error
0	0x0 WO	**CMD12_NOT_EXE (cmd12_not_exe):** Force Event for Auto CMD12 Not Executed

6.4.31 Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h

Force Event Register for Error Interrupt Status

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 52h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0		ceata_err	tgt_rsp_err	rsvd		adma_err	cmd12_err	cur_limit_err	data_end_bit_err	data_crc_err	data_timeout_err	cmd_ind_err	cmd_end_bit_err	cmd_crc_err	cmd_timeout_err

Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RO	**RSVD0 (rsvd0):** Reserved
13	0x0 RO	**CEATA_ERR (ceata_err):** Force Event for CEATA error, legacy feature not implemented
12	0x0 RO	**TGT_RSP_ERR (tgt_rsp_err):** Force Event for Target Response Error, legacy feature not implemented
11:10	0x0 RO	**RSVD (rsvd):** Reserved
9	0x0 WO	**ADMA_ERR (adma_err):** Force Event for ADMA Error
8	0x0 WO	**CMD12_ERR (cmd12_err):** Force Event for Auto CMD12 Error
7	0x0 WO	**CUR_LIMIT_ERR (cur_limit_err):** Force Event for Current Limit Error
6	0x0 WO	**DATA_END_BIT_ERR (data_end_bit_err):** Force Event for Data End Bit Error
5	0x0 WO	**DATA_CRC_ERR (data_crc_err):** Event for Data CRC Error
4	0x0 WO	**DATA_TIMEOUT_ERR (data_timeout_err):** Event for Data Timeout Error
3	0x0 WO	**CMD_IND_ERR (cmd_ind_err):** Force Event for Command Index Error
2	0x0 WO	**CMD_END_BIT_ERR (cmd_end_bit_err):** Force Event for Command End Bit Error

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 WO	**CMD_CRC_ERR (cmd_crc_err):** Force Event for Command CRC Error
0	0x0 WO	**CMD_TIMEOUT_ERR (cmd_timeout_err):** Force Event for Command Timeout Error

6.4.32 ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h

ADMA Error Status Register

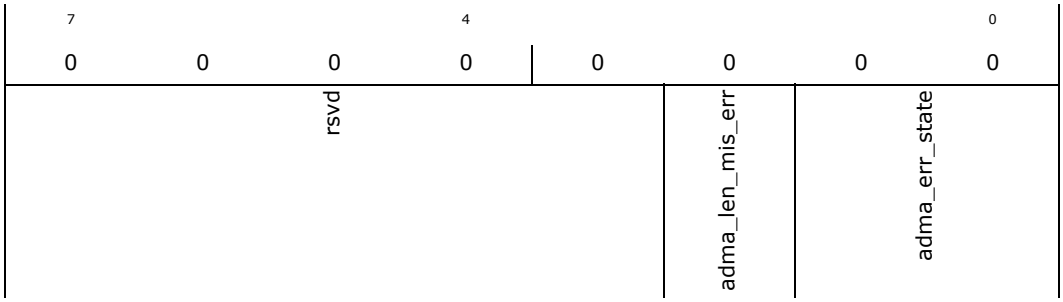
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0x0 RO	**RSVD (rsvd):** Reserved
2	0x0 RO	**ADMA_LEN_MIS_ERR (adma_len_mis_err):** ADMA Length Mismatch Error
1:0	0x0 RO	**ADMA_ERR_STATE (adma_err_state):** ADMA Error State

6.4.33 ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h

This register contains the physical Descriptor address used for ADMA data transfer.

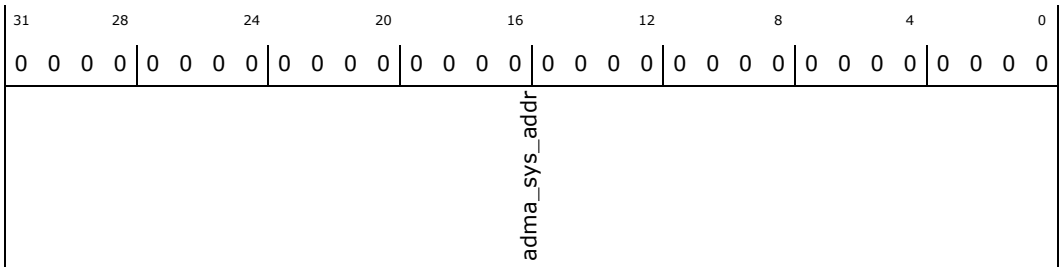
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**ADMA_SYS_ADDR (adma_sys_addr):** ADMA System Address

6.4.34 ADMA System Address Register (ADMA_SYS_ADDR_HIGH)—Offset 5Ch

This register contains the physical Descriptor address used for ADMA data transfer.

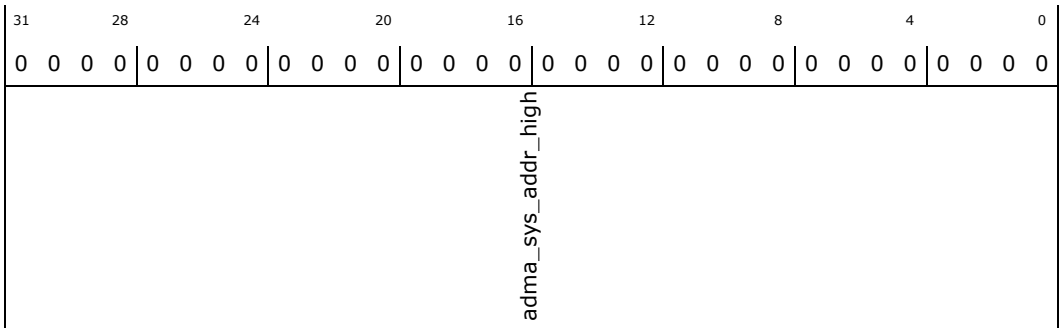
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**ADMA_SYS_ADDR_HIGH (adma_sys_addr_high):** High 32 bits of ADMA System Address for 64bit system

6.4.35 Preset Values registers (PRESET_VALUE_0)—Offset 60h

Preset Values init and default speed

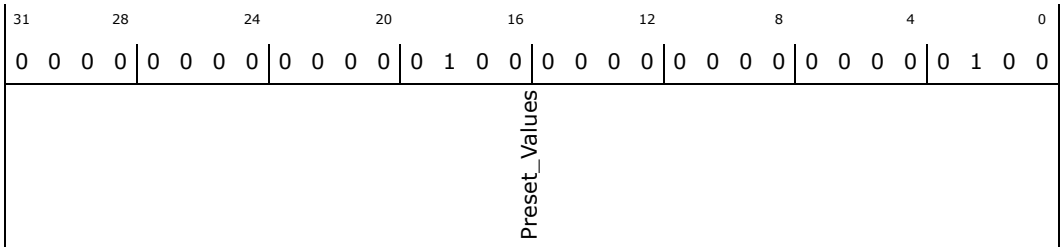
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00040004h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x40004 RO	**PresetValues (Preset_Values):** Reserved.

6.4.36 Preset Values 1 registers (PRESET_VALUE_1)—Offset 64h

Preset Values high and sdr12

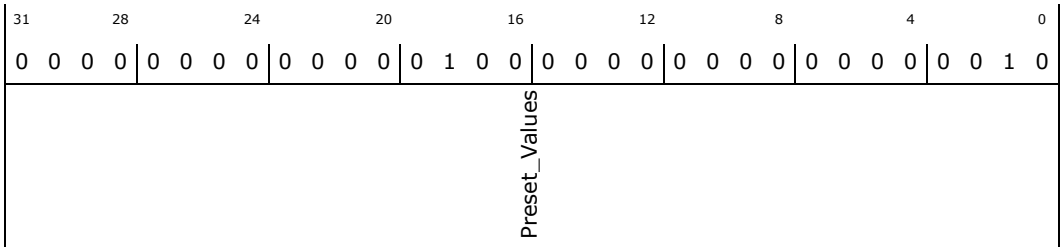
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00040002h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x40002 RO	**PresetValues (Preset_Values):** Reserved.

6.4.37 Preset Values 2 registers (PRESET_VALUE_2)—Offset 68h

Preset Values sdr25 and sdr50

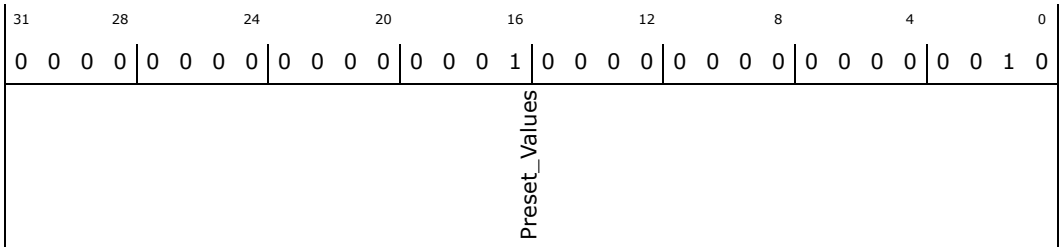
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00010002h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x10002 RO	**PresetValues (Preset_Values):** Reserved.

6.4.38 Preset Values 3 registers (PRESET_VALUE_3)—Offset 6Ch

Preset Values sdr104 and ddr50

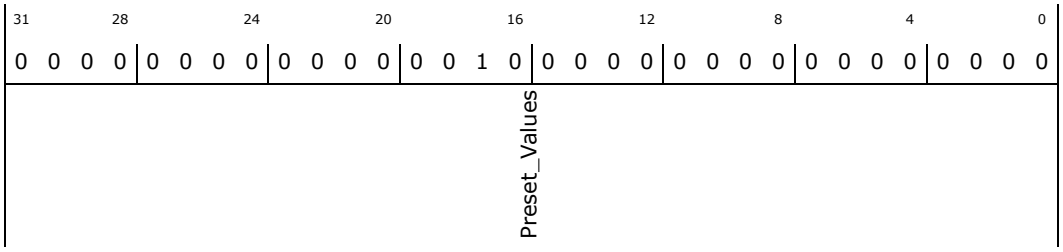
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00020000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x20000 RO	**PresetValues (Preset_Values):** Reserved.

6.4.39 BOOT_TIMEOUT_CTRL (BOOT_TIMEOUT_CTRL)—Offset 70h

BOOT_TIMEOUT_CTRL

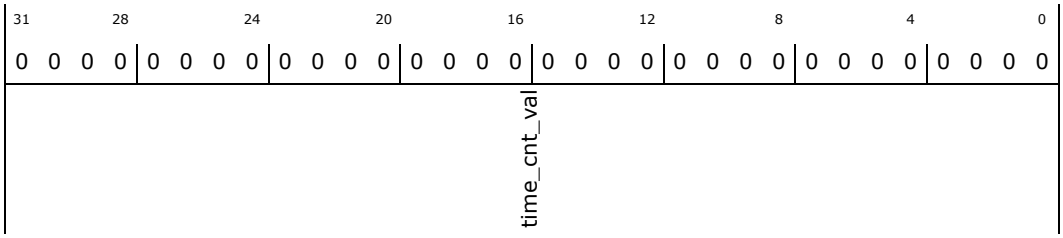
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**TIME_CNT_VAL (time_cnt_val):** Boot Data Timeout Counter Value

6.4.40 DEBUG_SEL (DEBUG_SEL)—Offset 74h

Debug Selection Register

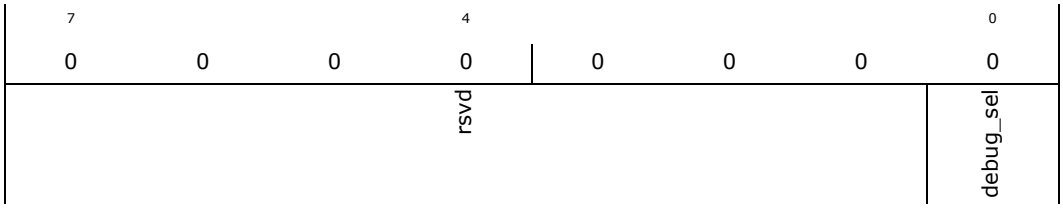
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:1	0x0 RO	**RSVD (rsvd):** Reserved
0	0x0 RO	**DEBUG_SEL (debug_sel):** 1 - cmd register, interrupt status, transmitter module, ahb_iface module and clk sdcard signals are probed out..

6.4.41 Shared Bus Control Register (SHARED_BUS)—Offset E0h

Shared Bus Control Register

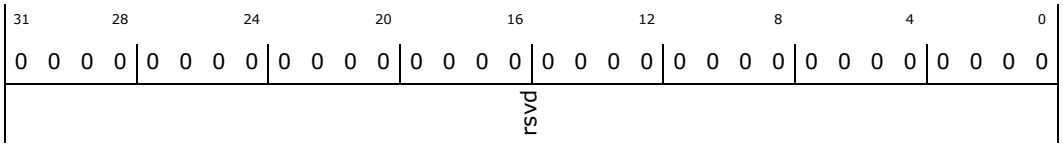
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD (rsvd):** Reserved

6.4.42 SPI_INT_SUP (SPI_INT_SUP)—Offset F0h

SPI_INT_SUP

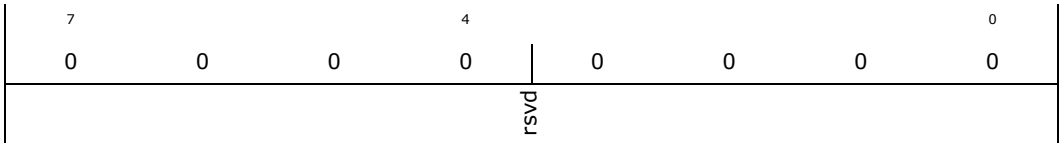
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**RSVD (rsvd):** Reserved

6.4.43 Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh

Slot Interrupt Status Register

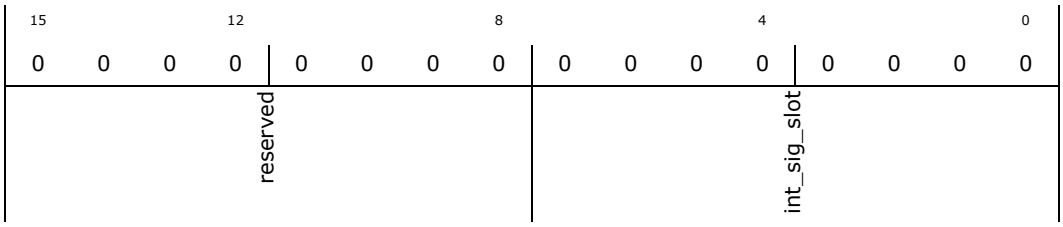
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Reserved (reserved):** Reserved
7:0	0x0 RO	**INT_SIG_SLOT (int_sig_slot):** Interrupt Signal For Each Slot

6.4.44 Host Controller Version Register (HOST_CTRL_VER)—Offset FEh

Host Controller Version Register

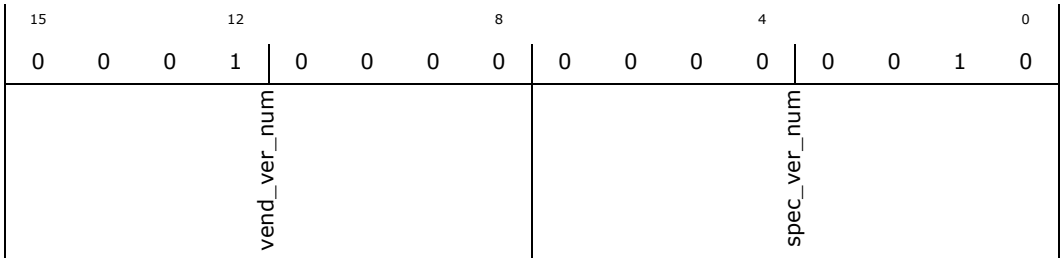
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + FEh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:17, F:0] + 10h

Default: 1002h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0x10 RO	**VEND_VER_NUM (vend_ver_num):** Vendor Version Number
7:0	0x2 RO	**SPEC_VER_NUM (spec_ver_num):** Version Number

6.5 SDIO 2 PCI Configuration Registers

Table 36. Summary of SDIO 2 PCI Configuration Registers—0/18/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 2001	22948086h
4–7h	4	"Status and Command Register (STATUSCOMMAND)—Offset 4h" on page 2001	00100000h
8–Bh	4	"Revision ID and Class Code Register (REVCLASSCODE)—Offset 8h" on page 2002	00000000h
C–Fh	4	"Cache Line Latency Header and BIST Register (CLLATHEADERBIST)—Offset Ch" on page 2003	00000000h
10–13h	4	"Base Address Register low (BAR)—Offset 10h" on page 2004	00000000h
14–17h	4	"Base Address Register high (BAR_HIGH)—Offset 14h" on page 2004	00000000h
18–1Bh	4	"Base Address Register1 low (BAR1)—Offset 18h" on page 2005	00000000h
1C–1Fh	4	"Base Address Register1 high (BAR1_HIGH)—Offset 1Ch" on page 2006	00000000h
2C–2Fh	4	"Subsystem Vendor and Subsystem ID Register (SUBSYSTEMID)—Offset 2Ch" on page 2006	00000000h
30–33h	4	"EXPANSION ROM base address Register (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 2007	00000000h
34–37h	4	"Capabilities Pointer Register (CAPABILITYPTR)—Offset 34h" on page 2007	00000080h
3C–3Fh	4	"Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 2008	00000100h
80–83h	4	"PowerManagement Capability ID Register (POWERCAPID)—Offset 80h" on page 2009	48030001h
84–87h	4	"Power Management Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 2009	00000008h
A0–A3h	4	"General Purpose Read Write Register1 (GEN_REGRW1)—Offset A0h" on page 2010	00000000h
A4–A7h	4	"General Purpose Read Write Register2 (GEN_REGRW2)—Offset A4h" on page 2011	00000000h
A8–ABh	4	"General Purpose Read Write Register3 (GEN_REGRW3)—Offset A8h" on page 2011	00000000h
AC–AFh	4	"General Purpose Read Write Register4 (GEN_REGRW4)—Offset ACh" on page 2012	00000000h
C0–C3h	4	"General Purpose Input Register (GEN_INPUT_REG)—Offset C0h" on page 2012	00000000h
F8–FBh	4	"Manufacturers ID Register (MANID)—Offset F8h" on page 2013	00000000h

6.5.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

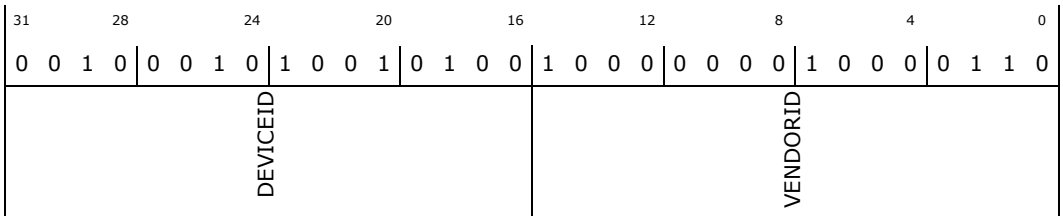
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 0h

Default: 22948086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x2294 RO	**DEVICEID:** Device ID identifies the particular PCI device. The Default value is taken from a strap at the top level. SetIDValue message updates 15:7 of this strap. Value shown below is after SetIDValue from CHV_RevIdDevId_HAS: SDIO1(smmc) : 16'h2294 SDIO2(sdio) : 16'h2295 SDIO3(sdcard) : 16'h2296
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by the PCI SIG, which identifies the manufacturer of the device. This is tied to a strap the top level.

6.5.2 Status and Command Register (STATUSCOMMAND)—Offset 4h

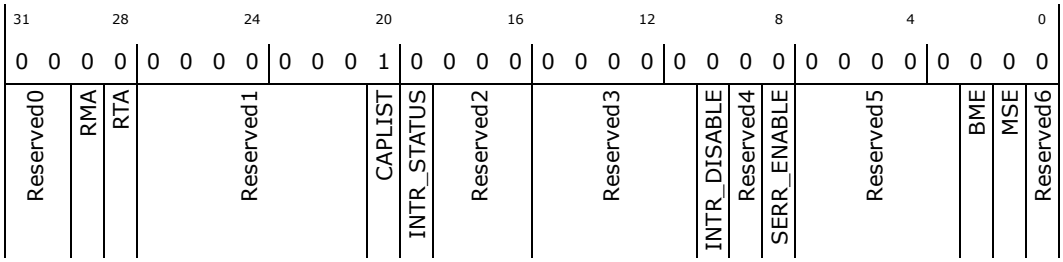
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved0:** Reserved, [30]: Signaled System Error, Not implemented
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, the Bridge sets this bit.
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, the Bridge sets this bit.
27:21	0x0 RO	**Reserved1:** Reserved, [27]: Signaled Target Abort: Not implemented
20	0x1 RO	**CAPLIST:** Capabilities List: Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at the configuration offset 34h.
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, is the device/function interrupt message sent. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, which is the Bridge does not send Interrupt Assert message through the IOSF Sideband Channel. Reset value of this bit is 0. This bit has no connection with the interrupt status bit.
9	0x0 RO	**Reserved4:** Reserved
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: Not implemented
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0,the Bridge does not generate any new upstream transaction on IOSF as a master.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge response to downstream memory accesses. When set, accesses to memory space of the device is enabled.
0	0x0 RO	**Reserved6:** Reserved

6.5.3 Revision ID and Class Code Register (REVCLASSCODE)—Offset 8h

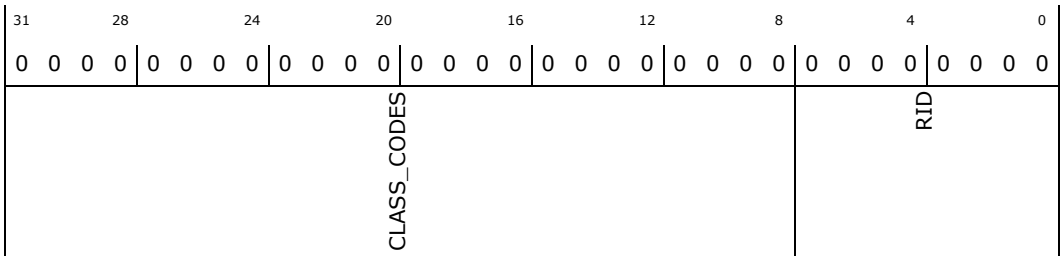
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** The Class Code register is read-only and is used to identify the generic function of the device, and in some cases, a specific register-level programming interface. The register is broken into 3 Byte-size fields. 1. The upper Byte (at offset 0Bh) is a base class code that broadly classifies the type of function the device performs. 2. The middle Byte (at offset 0Ah) is a sub-class code that identifies more specifically the function of the device. 3. The lower Byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular PCI device. The default value comes from a strap. A SetIDValue message updates this value.

6.5.4 Cache Line Latency Header and BIST Register (CLLATHEADERBIST)—Offset Ch

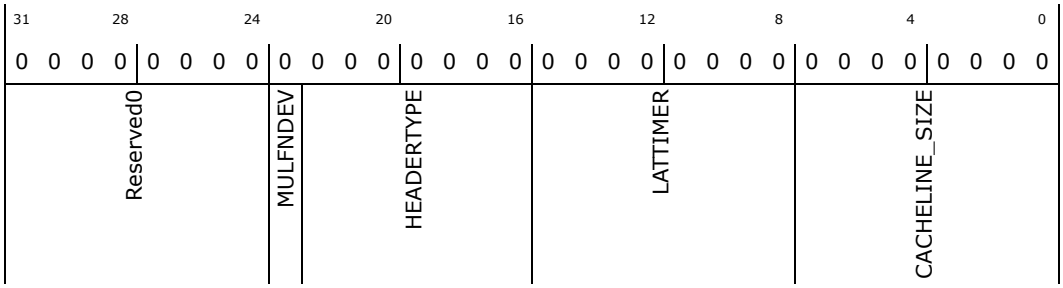
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x0 RO	**MULFNDEV:** Multi-Function Device: This bit is 0 to indicate Single Function Device

Bit Range	Default & Access	Field Name (ID): Description
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header
15:8	0x0 RO	**LATTIMER:** Latency Timer
7:0	0x0 RW	**CACHELINE_SIZE:** Cacheline Size: This register is implemented as R/W with default as 0. Similar to other Intel IPs.

6.5.5 Base Address Register low (BAR)—Offset 10h

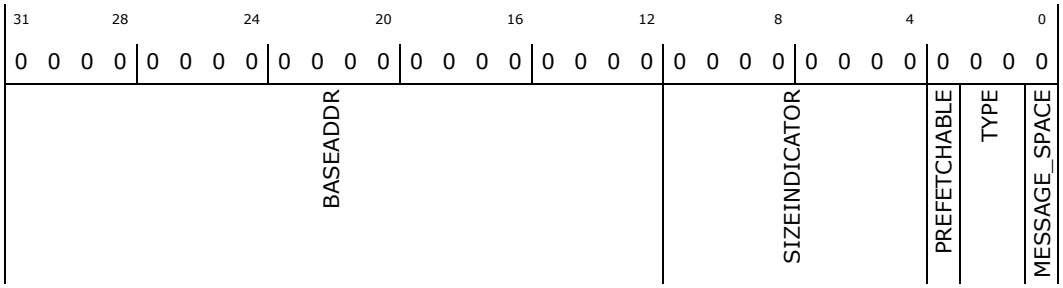
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the OCP fabric memory space. bit [31] is always read write as Bridge expects the size of the device to be limited to 2G Taken from Strap values as ones.
11:4	0x0 RO	**SIZEINDICATOR:** Always is 0, as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0x0 RO	**TYPE:** Type: If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

6.5.6 Base Address Register high (BAR_HIGH)—Offset 14h

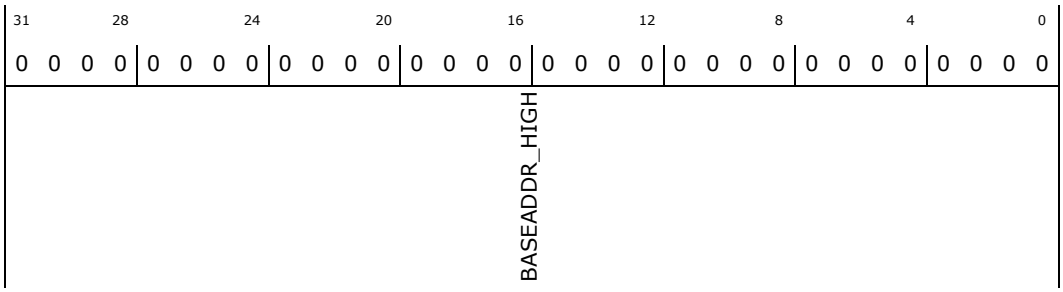
BAR -Base Address Register High

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**BASEADDR_HIGH:** High 32 bits for BAR, RO as SCC is set to 32 bits only

6.5.7 Base Address Register1 low (BAR1)—Offset 18h

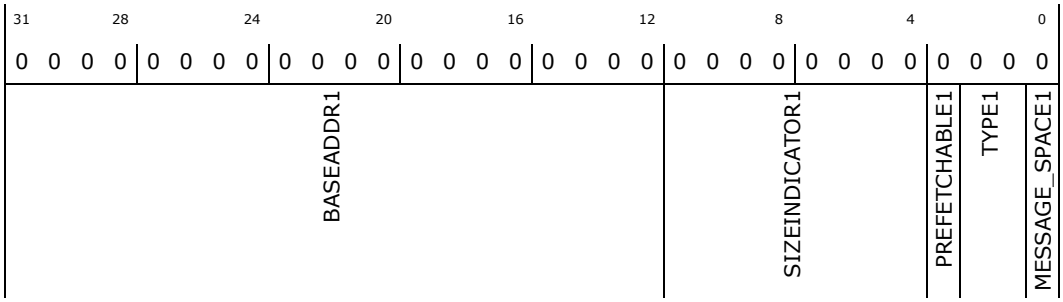
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 18h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: This field is present if BAR1 is enabled through private configuration space.
11:4	0x0 RO	**SIZEINDICATOR1:** Always is 0 as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0x0 RO	**TYPE1:** Type: If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0 Indicates this BAR is present in the memory space.

6.5.8 Base Address Register1 high (BAR1_HIGH)—Offset 1Ch

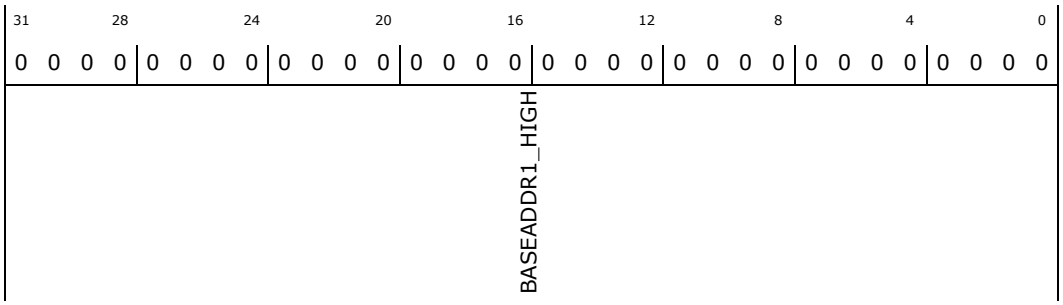
BAR1 -Base Address Register1 High

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 1Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**BASEADDR1_HIGH:** High 32 bits for BAR1, RO as SCC is set to 32 bits only

6.5.9 Subsystem Vendor and Subsystem ID Register (SUBSYSTEMID)—Offset 2Ch

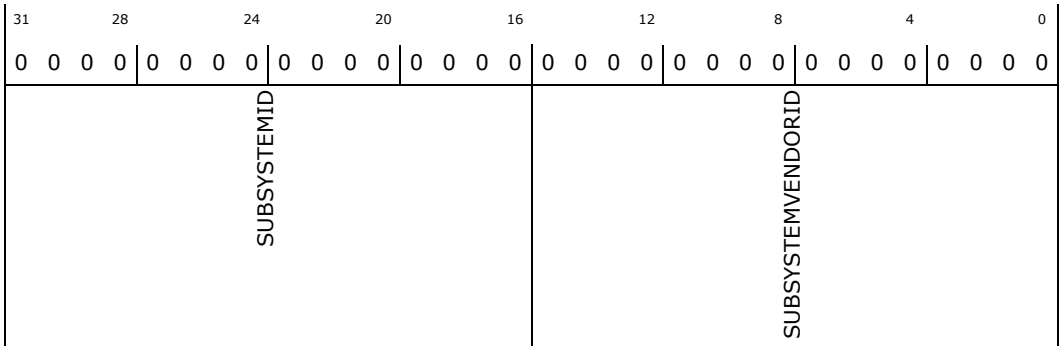
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

6.5.10 EXPANSION ROM base address Register (EXPANSION_ROM_BASEADDR)—Offset 30h

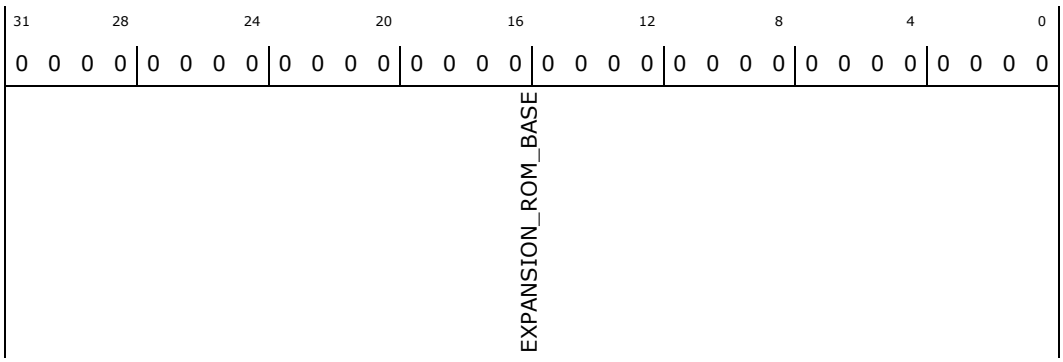
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** [31:11]-) Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM [10:1] -) Reserved [0] -) Expansion ROM Enable: Bridge does not have support for Expansion ROMs.

6.5.11 Capabilities Pointer Register (CAPABILITYPTR)—Offset 34h

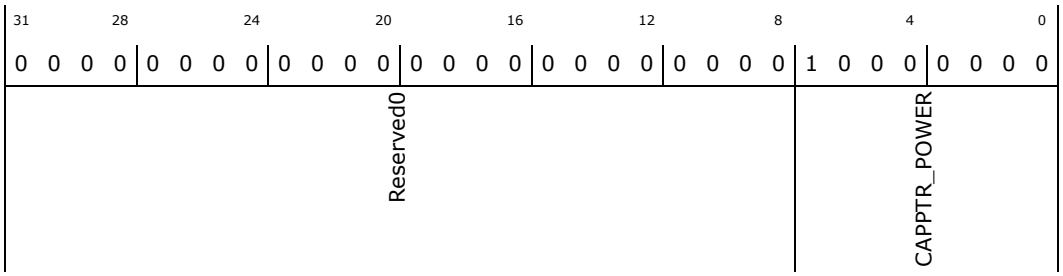
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 34h

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x80 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability points to the PM Capability (0x80) structure.

6.5.12 Interrupt Register (INTERRUPTREG)—Offset 3Ch

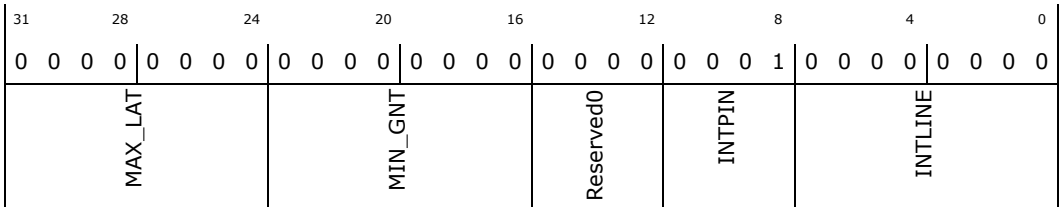
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space. For a single function device, this ideally is INTA.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

6.5.13 PowerManagement Capability ID Register (POWERCAPID)—Offset 80h

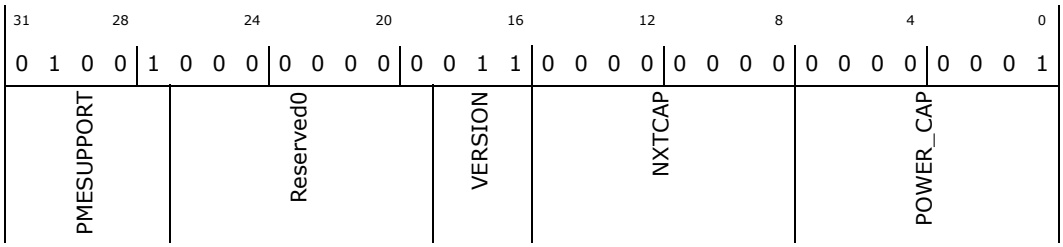
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 80h

Default: 48030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x9 RO	**PMESUPPORT:** PME_Support: This 5-bit field indicates the power states in which the function can assert the PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal at the same time in that power state. bit(11) X XXX1b: PME# can be asserted from D0 bit(12) X XX1Xb: PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb: PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb:PME# can be asserted from D3hot bit(15) 1 XXXXb:PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the private configuration space PME_Support XORed with the PME_Support strap.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

6.5.14 Power Management Control and Status Register (PMECTRLSTATUS)—Offset 84h

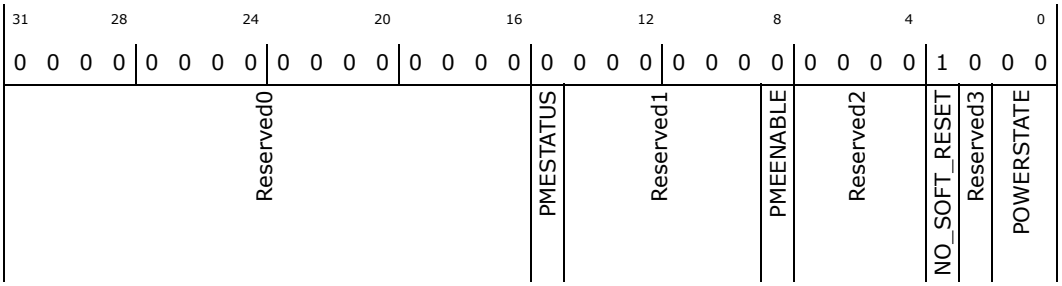
PMECTRLSTATUS: Power Management Control and Status

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 Software clears the bit by writing a 1 to it. 1 This bit is set when the PME# signal is asserted independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: 1 Enables the function to assert PME#. 0 PME# message on Sideband is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state and to set a new power state. The values are: 00 D0 state 11 D3HOT state Others Reserved Note: If the software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally. The data is discarded and no state change occurs. Note: When in the D3HOT states, interrupts are blocked. Note: D3Hot cannot be used for downstream decode on fabric ports.

6.5.15 General Purpose Read Write Register1 (GEN_REGRW1)—Offset A0h

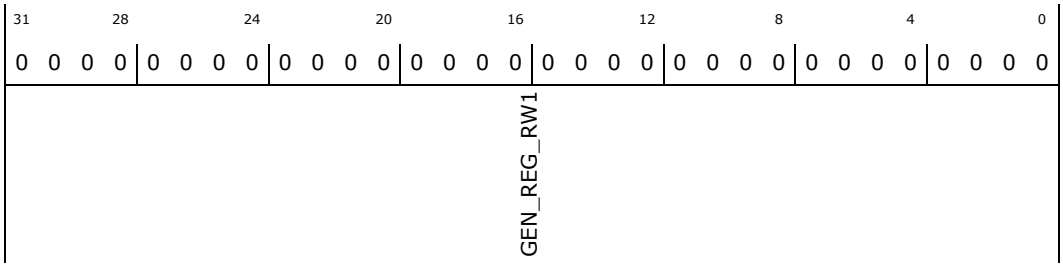
General Purpose Read Write Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW1:** General Purpose PCIRegister: This register value is brought out as oob_gen_pci_reg1 out of band signal

6.5.16 General Purpose Read Write Register2 (GEN_REGRW2)—Offset A4h

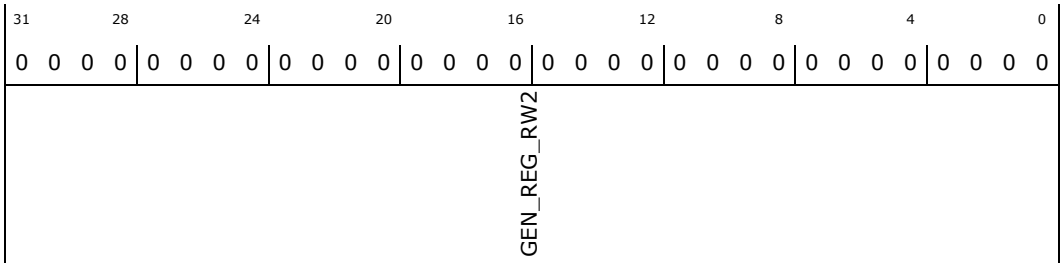
General Purpose Read Write Register2

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW2:** General Purpose PCI Register: This register value is brought out as oob_gen_pci_reg2 Out of Band signal

6.5.17 General Purpose Read Write Register3 (GEN_REGRW3)—Offset A8h

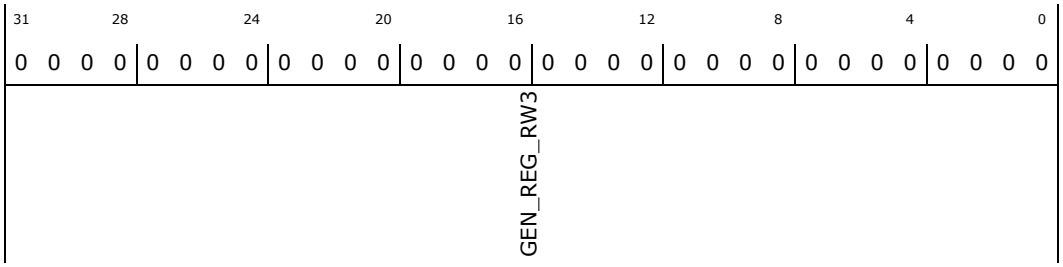
General Purpose Read Write Register3

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW3:** General Purpose PCI Register: This register value is brought out as oob_gen_pci_reg3 Out of Band signal

6.5.18 General Purpose Read Write Register4 (GEN_REGRW4)—Offset ACh

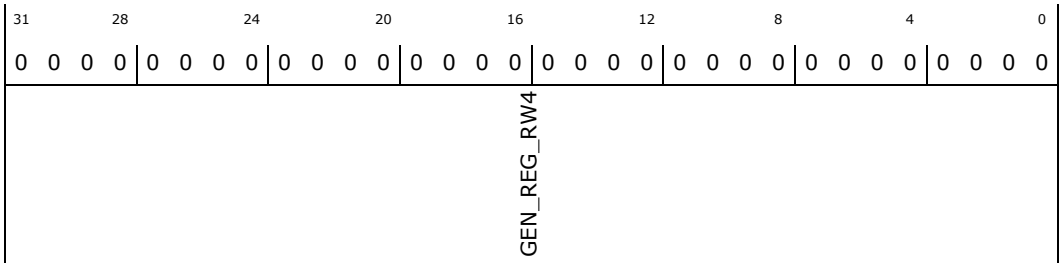
General Purpose Read Write Register4

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW4:** General Purpose PCI Register: This register value is brought out as oob_gen_pci_reg4 Out of Band signal

6.5.19 General Purpose Input Register (GEN_INPUT_REG)—Offset C0h

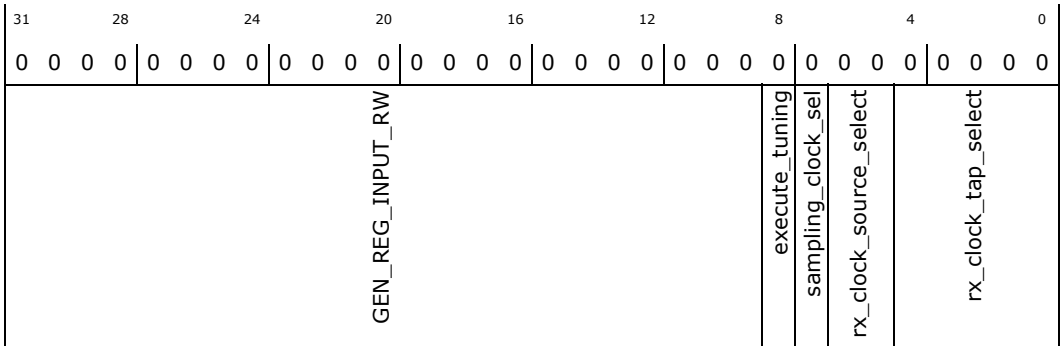
General Purpose Input Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**GEN_REG_INPUT_RW:** Reserved.
8	0x0 RO	**execute_tuning:** Execute Tuning. This is intended for debug use only.
7	0x0 RO	**sampling_clock_sel:** Sampling Clock Select. This is intended for debug use only.
6:5	0x0 RO	**rx_clock_source_select:** Rx Clock Source Select: 00: loopback clock 01: SDR50 10: DDR50 11: tuned clock This is intended only for debug use.
4:0	0x0 RO	**rx_clock_tap_select:** Rx Clock Tap Select: This indicates which tap select the host controller's tuning algorithm settled on. This is intended only for debug use.

6.5.20 Manufacturers ID Register (MANID)—Offset F8h

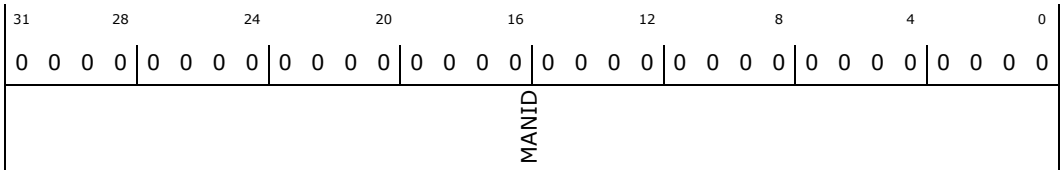
Manufacturers ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:18, F:0] + F8h

Default: 00000000h

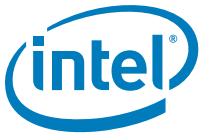


Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: Default value comes from straps. This value can be updated from SetIDValue Message

6.6 SDIO 2 Memory Mapped I/O Registers

Table 37. Summary of SDIO 2 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"SDMA System Address Register (SYS_ADR)—Offset 0h" on page 2016	00000000h
4–5h	2	"Block Size Register (BLK_SIZE)—Offset 4h" on page 2016	0000h
6–7h	2	"Block Count Register (BLK_COUNT)—Offset 6h" on page 2017	0000h
8–Bh	4	"Argument Register (ARGUMENT)—Offset 8h" on page 2018	00000000h
C–Dh	2	"Transfer Mode Register (TX_MODE)—Offset Ch" on page 2018	0000h
E–Fh	2	"Command Register (CMD)—Offset Eh" on page 2019	0000h
10–13h	4	"Response Register0 (RESPONSE0)—Offset 10h" on page 2020	00000000h
14–17h	4	"Response Register2 (RESPONSE2)—Offset 14h" on page 2021	00000000h
18–1Bh	4	"Response Register4 (RESPONSE4)—Offset 18h" on page 2021	00000000h
1C–1Fh	4	"Response Register6 (RESPONSE6)—Offset 1Ch" on page 2022	00000000h
20–23h	4	"Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h" on page 2023	00000000h
24–27h	4	"Present State Register (PRE_STATE)—Offset 24h" on page 2023	1FFF0000h
28–28h	1	"Host Control Register (HOST_CTL)—Offset 28h" on page 2024	00h
29–29h	1	"Power Control Register (PWR_CTL)—Offset 29h" on page 2025	01h
2A–2Ah	1	"Block Gap Control Register (BLK_GAP_CTL)—Offset 2Ah" on page 2026	80h
2B–2Bh	1	"Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh" on page 2027	00h
2C–2Dh	2	"Clock Control Register (CLK_CTL)—Offset 2Ch" on page 2028	0000h
2E–2Eh	1	"Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh" on page 2028	00h
2F–2Fh	1	"Software Reset Register (SW_RST)—Offset 2Fh" on page 2029	00h
30–31h	2	"Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h" on page 2030	0000h
32–33h	2	"Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h" on page 2031	0000h
34–35h	2	"Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h" on page 2032	0000h
36–37h	2	"Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h" on page 2033	0000h
38–39h	2	"Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h" on page 2035	0000h
3A–3Bh	2	"Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah" on page 2036	0000h
3C–3Fh	4	"Auto CMD12 Error Status Register and Host control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch" on page 2037	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40–43h	4	"Capabilities Register (CAPABILITIES)—Offset 40h" on page 2039	446CC8B2h
44–47h	4	"Capabilities Register 2 (CAPABILITIES_2)—Offset 44h" on page 2039	00000007h
48–4Bh	4	"Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h" on page 2040	00000000h
50–51h	2	"Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h" on page 2041	0000h
52–53h	2	"Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h" on page 2042	0000h
54–54h	1	"ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h" on page 2043	00h
58–5Bh	4	"ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h" on page 2043	00000000h
5C–5Fh	4	"ADMA System Address Register (ADMA_SYS_ADDR_HIGH)—Offset 5Ch" on page 2044	00000000h
60–63h	4	"Preset Values registers (PRESET_VALUE_0)—Offset 60h" on page 2044	00040004h
64–67h	4	"Preset Values 1 registers (PRESET_VALUE_1)—Offset 64h" on page 2045	00040002h
68–6Bh	4	"Preset Values 2 registers (PRESET_VALUE_2)—Offset 68h" on page 2045	00010002h
6C–6Fh	4	"Preset Values 3 registers (PRESET_VALUE_3)—Offset 6Ch" on page 2046	00020000h
70–73h	4	"BOOT_TIMEOUT_CTRL (BOOT_TIMEOUT_CTRL)—Offset 70h" on page 2046	00000000h
74–74h	1	"DEBUG_SEL (DEBUG_SEL)—Offset 74h" on page 2047	00h
E0–E3h	4	"Shared Bus Control Register (SHARED_BUS)—Offset E0h" on page 2047	00000000h
F0–F0h	1	"SPI_INT_SUP (SPI_INT_SUP)—Offset F0h" on page 2048	00h
FC–FDh	2	"Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh" on page 2048	0000h
FE–FFh	2	"Host Controller Version Register (HOST_CTRL_VER)—Offset FEh" on page 2049	1002h

6.6.1 SDMA System Address Register (SYS_ADR)—Offset 0h

This register contains the physical system memory address used for DMA transfers

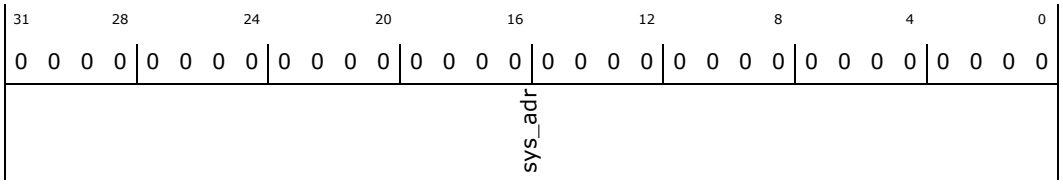
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SYS_ADR (sys_adr):** SDMA System Address This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value. The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at the every boundary specified by the Host SDMA Buffer Boundary in the Block Size register. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register (003h) is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by the Resume command or by setting Continue Request in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register. ADMA does not use this register.

6.6.2 Block Size Register (BLK_SIZE)—Offset 4h

This register is used to configure the number of bytes in a data block.

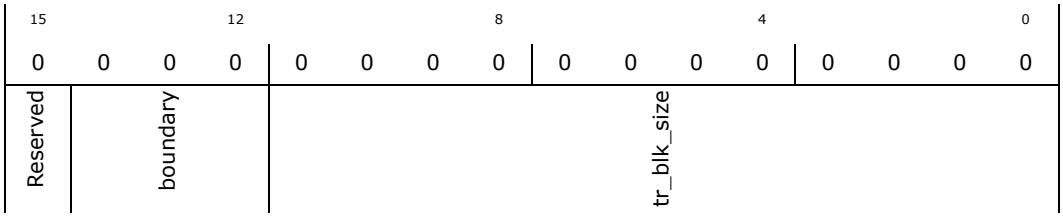
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**Reserved:** Reserved
14:12	0x0 RW	**BOUNDARY (boundary):** Host SDMA Buffer Boundary The large contiguous memory space may not be available in the virtual memory system. To perform long SDMA transfer, SDMA System Address register shall be updated at every system memory boundary during SDMA transfer. These bits specify the size of contiguous buffer in the system memory. The SDMA transfer shall wait at the every boundary specified by these fields and the Host Controller generates the DMA Interrupt to request the Host Driver to update the SDMA System Address register. At the end of transfer, the Host Controller may issue or may not issue DMA Interrupt. In particular, DMA Interrupt shall not be issued after Transfer Complete Interrupt is issued. In case of this register is set to 0 (buffer size = 4K bytes), lower 12-bit of byte address points data in the contiguous buffer and the upper 20-bit points the location of the buffer in the system memory. The SDMA transfer stops when the Host Controller detects carry out of the address from bit 11 to 12. These bits shall be supported when the SDMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. ADMA does not use this register. 000b - 4K bytes (Detects A11 carry out) 001b - 8K bytes (Detects A12 carry out) 010b - 16K Bytes (Detects A13 carry out) 011b - 32K Bytes (Detects A14 carry out) 100b - 64K bytes (Detects A15 carry out) 101b - 128K Bytes (Detects A16 carry out) 110b - 256K Bytes (Detects A17 carry out) 111b - 512K Bytes (Detects A18 carry out)
11:0	0x0 RW	**TR_BLK_SIZE (tr_blk_size):** Transfer Block Size This register specifies the block size of data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. Values ranging from 1 up to the maximum buffer size can be set. In case of memory, it shall be set up to 512 bytes (Refer to Implementation Note in Section 1.7.2). It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value, and write operations shall be ignored. 0800h 2048 Bytes ... ... 0200h 512 Bytes 01FFh 511 Bytes ... ... 0004h 4 Bytes 0003h 3 Bytes 0002h 2 Bytes 0001h 1 Byte 0000h No data transfer

6.6.3 Block Count Register (BLK_COUNT)—Offset 6h

This register is used to configure the number of data blocks

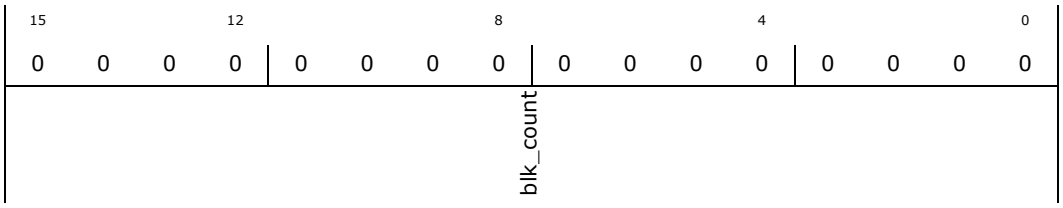
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 6h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW	**BLK_COUNT (blk_count):** Blocks Count For Current Transfer This register is enabled when Block Count Enable in the Transfer Mode register is set to 1 and is valid only for multiple block transfers

6.6.4 Argument Register (ARGUMENT)—Offset 8h

This register contains the SD Command Argument.

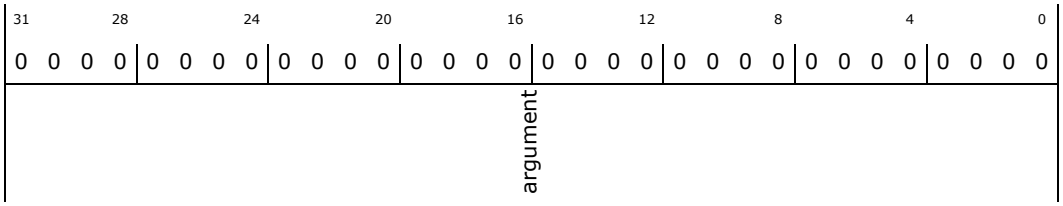
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**ARGUMENT (argument):** Command Argument The SD Command Argument is specified as bit39-8 of Command-Format in the Physical Layer Specification.

6.6.5 Transfer Mode Register (TX_MODE)—Offset Ch

Transfer Mode Register

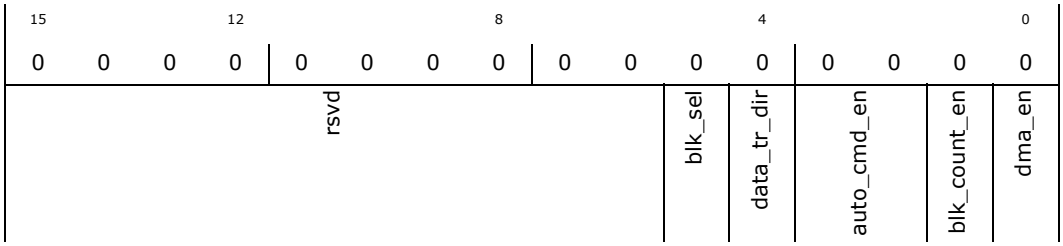
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:6	0x0 RO	**RSVD (rsvd):** Reserved
5	0x0 RW	**BLK_SEL (blk_sel):** Multi / Single Block Select This bit is set when issuing multiple-block transfer commands using DAT line. For any other commands, this bit shall be set to 0. If this bit is 0, it is not necessary to set the Block Count register. (Refer to Table 2-8) 1 Multiple Block 0 Single Block
4	0x0 RW	**Data_TR_Dir (data_tr_dir):** Data Transfer Direction Select This bit defines the direction of DAT line data transfers. The bit is set to 1 by the Host Driver to transfer data from the SD card to the SD Host Controller and it is set to 0 for all other commands. 1 Read (Card to Host) 0 Write (Host to Card)
3:2	0x0 RW	**AUTO_CMD_EN (auto_cmd_en):** This field determines use of auto command functions 00b - Auto Command Disabled 01b - Auto CMD12 Enable 10b - Auto CMD23 Enable 11b - Reserved
1	0x0 RW	**BLK_COUNT_EN (blk_count_en):** Block Count Enable This bit is used to enable the Block Count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. (Refer to Table 2-8) If ADMA2 data transfer is more than 65535 blocks, this bit shall be set to 0. In this case, data transfer length is designated by Descriptor Table. 1 Enable 0 Disable
0	0x0 RW	**DMA_EN (dma_en):** DMA Enable This bit enables DMA functionality as described in section 1.4. DMA can be enabled only if it is supported as indicated in the Capabilities register. One of the DMA modes can be selected by DMA Select in the Host Control register. If DMA is not supported, this bit is meaningless and shall always read 0. If this bit is set to 1, a DMA operation shall begin when the Host Driver writes to the upper byte of Command register (00Fh). 1 DMA Data transfer 0 No data transfer or Non DMA data transfer

6.6.6 Command Register (CMD)—Offset Eh

Command Register

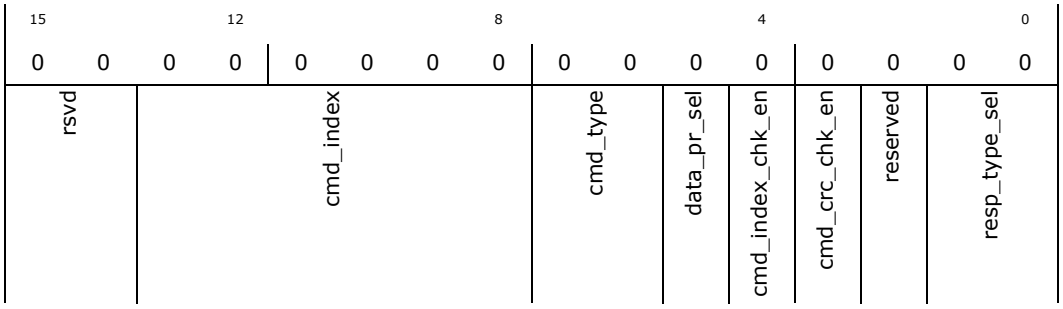
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RO	**RSVD (rsvd):** Reserved
13:8	0x0 RW	**CMD_INDEX (cmd_index):** Command Index These bits shall be set to the command number (CMD0-63, ACMD0-63) that is specified in bits 45-40 of the Command-Format in the Physical Layer Specification and SDIO Card Specification.
7:6	0x0 RW	**CMD_TYPE (cmd_type):** Command Type
5	0x0 RW	**DATA_PR_SEL (data_pr_sel):** Data Present Select This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. It is set to 0 for the following: (1) Commands using only CMD line (ex. CMD52). (2) Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b ex. CMD38) (3) Resume command 1 Data Present 0 No Data Present
4	0x0 RW	**CMD_INDEX_CHK_EN (cmd_index_chk_en):** Command Index Check Enable If this bit is set to 1, the Host Controller shall check the Index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked. 1 Enable 0 Disable
3	0x0 RW	**CMD_CRC_CHK_EN (cmd_crc_chk_en):** Command CRC Check Enable If this bit is set to 1, the Host Controller shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. The position of CRC field is determined according to the length of the response. (Refer to definition in D01-00 and Table 2-10 below.) 1 Enable 0 Disable
2	0x0 RO	**Reserved (reserved):** Reserved
1:0	0x0 RW	**RESP_TYPE_SEL (resp_type_sel):** Response Type Select 00 No Response 01 Response Length 136 10 Response Length 48 11 Response Length 48 check Busy after response

6.6.7 Response Register0 (RESPONSE0)—Offset 10h

This register is used to store responses from SD cards

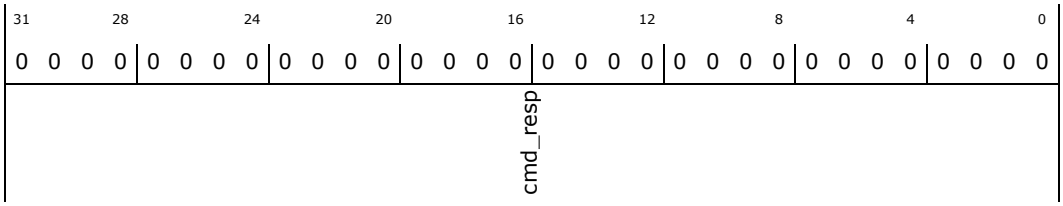
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**CMD_RESP0 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

6.6.8 Response Register2 (RESPONSE2)—Offset 14h

This register is used to store responses from SD cards

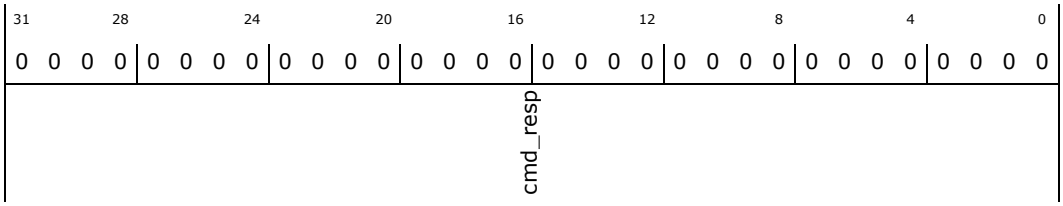
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**CMD_RESP2 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

6.6.9 Response Register4 (RESPONSE4)—Offset 18h

This register is used to store responses from SD cards

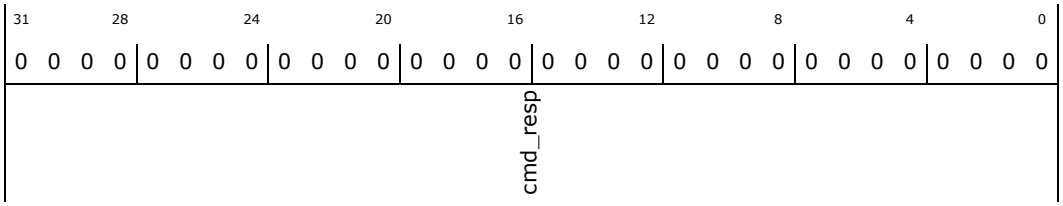
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**CMD_RESP4 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

6.6.10 Response Register6 (RESPONSE6)—Offset 1Ch

This register is used to store responses from SD cards

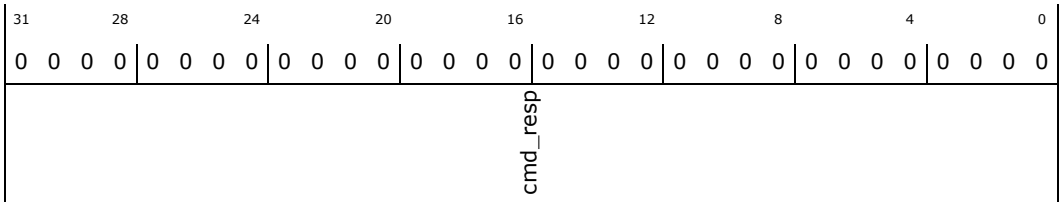
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**CMD_RESP6 (cmd_resp):** Command Response The Table 2-12 describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register

6.6.11 Buffer Data Port Register (BUF_DATA_PORT)—Offset 20h

32-bit data port register to access internal buffer

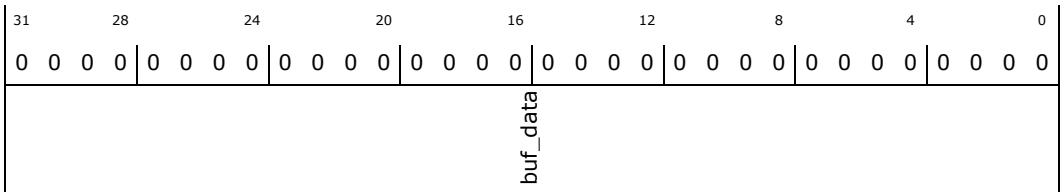
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**BUF_DATA (buf_data):** Buffer Data The Host Controller buffer can be accessed through this 32-bit Data Port register. RW depends on read or write transfer, it doesn't mean what's written can be read back

6.6.12 Present State Register (PRE_STATE)—Offset 24h

The Host Driver can get status of the Host Controller from this 32-bit read only register

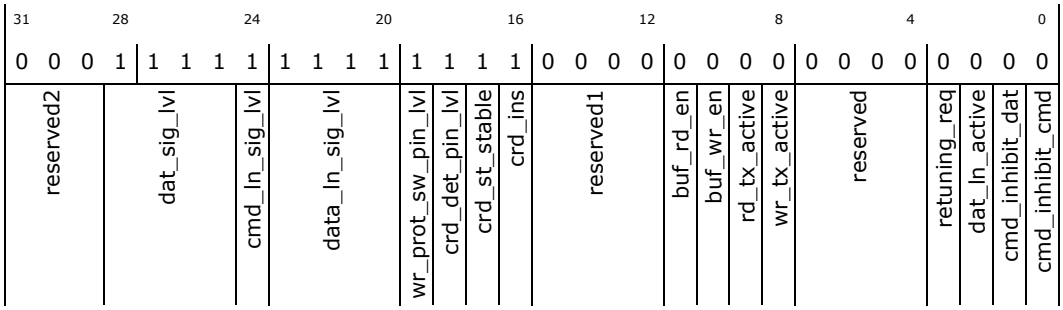
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 1FFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**Reserved2 (reserved2):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
28:25	0xf RO	**DAT_SIG_LVL (dat_sig_lvl):** This status is used to check DAT line level to recover from errors, and for debugging. D28 - DAT[7] D27 - DAT[6] D26 - DAT[5] D25 - DAT[4]
24	0x1 RO	**CMD_LN_SIG_LVL (cmd_ln_sig_lvl):** CMD Line Signal Level This status is used to check the CMD line level to recover from errors, and for debugging.
23:20	0xf RO	**DATA_LN_SIG_LVL (data_ln_sig_lvl):** DAT[3:0] Line Signal Level This status is used to check the DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. D23 DAT[3] D22 DAT[2] D21 DAT[1] D20 DAT[0]
19	0x1 RO	**WR_PROT_SW_PIN_LVL (wr_prot_sw_pin_lvl):** Write Protect Switch Pin Level
18	0x1 RO	**CRD_DET_PIN_LVL (crd_det_pin_lvl):** Card Detect Pin Level
17	0x1 RO	**CRD_ST_STABLE (crd_st_stable):** Card State Stable
16	0x1 RO	**CRD_INS (crd_ins):** Card Inserted
15:12	0x0 RO	**Reserved1 (reserved1):** Reserved
11	0x0 RO	**BUF_RD_EN (buf_rd_en):** Buffer Read Enable
10	0x0 RO	**BUF_WR_EN (buf_wr_en):** Buffer Write Enable
9	0x0 RO	**RD_TX_ACTIVE (rd_tx_active):** Read Transfer Active
8	0x0 RO	**WR_TX_ACTIVE (wr_tx_active):** Write Transfer Active
7:4	0x0 RO	**Reserved (reserved):** Reserved
3	0x0 RO	**RETUNING_REQ (retuning_req):** Re-Tuning Request
2	0x0 RO	**DAT_LN_ACTIVE (dat_ln_active):** DAT Line Active
1	0x0 RO	**CMD_INHIBIT_DAT (cmd_inhibit_dat):** Command Inhibit (DAT)
0	0x0 RO	**CMD_INHIBIT_CMD (cmd_inhibit_cmd):** Command Inhibit (CMD)

6.6.13 Host Control Register (HOST_CTL)—Offset 28h

Host Control Register

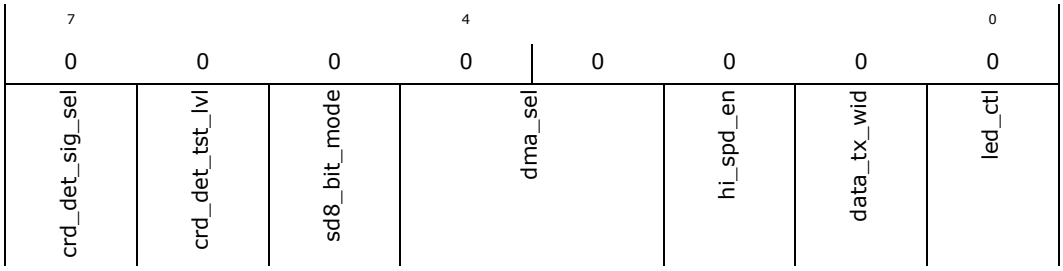
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW	**CRD_DET_SIG_SEL (crd_det_sig_sel):** Card Detect Signal Selection
6	0x0 RW	**CRD_DET_TST_LVL (crd_det_tst_lvl):** Card Detect Test Level
5	0x0 RW	**SD8_BIT_MODE (sd8_bit_mode):** This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card.
4:3	0x0 RW	**DMA_SEL (dma_sel):** DMA Select
2	0x0 RW	**HI_SPD_EN (hi_spd_en):** High Speed Enable
1	0x0 RW	**DATA_TX_WID (data_tx_wid):** Data Transfer Width
0	0x0 RW	**LED_CTL (led_ctl):** LED Control

6.6.14 Power Control Register (PWR_CTL)—Offset 29h

Power Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 29h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 01h

7			4				0
0	0	0	0	0	0	0	1
rsvd			hw_rst	sd_bus_volt_sel			sd_bus_pwr

Bit Range	Default & Access	Field Name (ID): Description
7:5	0x0 RO	**RSVD (rsvd):** Reserved
4	0x0 RW	**HW_rst (hw_rst):** HW reset
3:1	0x0 RW	**SD_BUS_VOLT_SEL (sd_bus_volt_sel):** SD Bus Voltage Select
0	0x1 RW	**SD_BUS_PWR (sd_bus_pwr):** SD Bus Power

6.6.15 Block Gap Control Register (BLK_GAP_CTL)—Offset 2Ah

Block Gap Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 2Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
boot_ack_chk	alt_boot_en	boot_en	spi_mode	int_blk_gap	rd_wait_ctl	cont_req	stp_blk_gap_req

Bit Range	Default & Access	Field Name (ID): Description
7	0x1 RW	**BOOT_ACK_CHK (boot_ack_chk):** To check for the boot acknowledge in boot operation; 0 = Will not wait for boot ack from eMMC card; 1 = Wake for boot ack from eMMC card
6	0x0 RW	**ALT_BOOT_EN (alt_boot_en):** To start boot code access in alternative mode; 0 = To stop alternate boot mode access; 1 = To start alternate boot mode access

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**BOOT_EN (boot_en):** To start boot code access; 0 = To stop boot code access; 1 = To start boot code access
4	0x0 RW	**SPI_MODE (spi_mode):** SPI mode enable bit; 0 = SD mode; 1 = SPI mode
3	0x0 RW	**INT_BLK_GAP (int_blk_gap):** Interrupt At Block Gap
2	0x0 RW	**RD_WAIT_CTL (rd_wait_ctl):** Read Wait Control
1	0x0 RW	**CONT_REQ (cont_req):** Continue Request
0	0x0 RW	**STP_BLK_GAP_REQ (stp_blk_gap_req):** Stop At Block Gap Request

6.6.16 Wakeup Control Register (WAKEUP_CTL)—Offset 2Bh

This register is used for wakeup event control.

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 2Bh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
rsvd					wakeup_en_sd_rm	wakeup_en_sd_ins	wakeup_en_crd_int

Bit Range	Default & Access	Field Name (ID): Description
7:3	0x0 RO	**RSVD (rsvd):** Reserved
2	0x0 RW	**WAKEUP_EN_SD_RM (wakeup_en_sd_rm):** Wakeup Event Enable On SD Card Removal
1	0x0 RW	**WAKEUP_EN_SD_INS (wakeup_en_sd_ins):** Wakeup Event Enable On SD Card Insertion
0	0x0 RW	**WAKEUP_EN_CRD_INT (wakeup_en_crd_int):** Wakeup Event Enable On Card Interrupt

6.6.17 Clock Control Register (CLK_CTL)—Offset 2Ch

This register is used configure the frequency of the SDIO controller, and enable the clock.

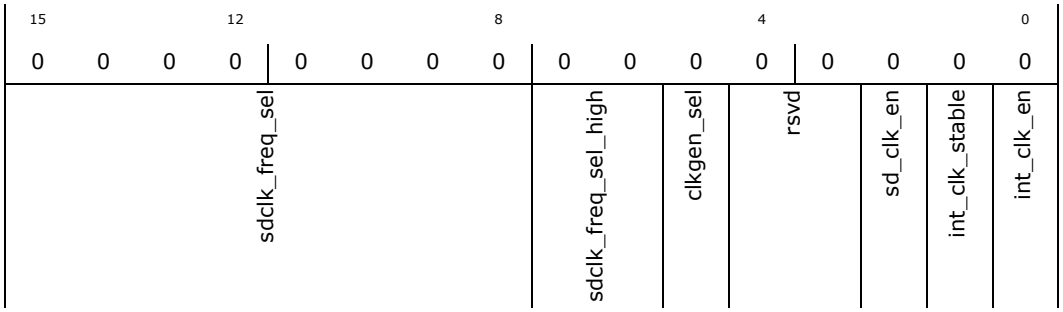
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RW	**SDCLK_FREQ_SEL (sdclk_freq_sel):** SDCLK Frequency Select
7:6	0x0 RW	**SDCLK_FREQ_SEL_HIGH (sdclk_freq_sel_high):** Bit 07-06 is assigned to bit 09-08 of clock divider in SDCLK Frequency Select
5	0x0 RW	**CLKGEN_SEL (clkgen_sel):** This bit is used to select the clock generator mode in SDCLK Frequency Select. 1: Programmable Clock Mode, 0: Divided Clock Mode
4:3	0x0 RO	**RSVD (rsvd):** Reserved
2	0x0 RW	**SD_CLK_EN (sd_clk_en):** SD Clock Enable
1	0x0 RO	**INT_CLK_STABLE (int_clk_stable):** Internal Clock Stable
0	0x0 RW	**INT_CLK_EN (int_clk_en):** Internal Clock Enable

6.6.18 Timeout Control Register (TIMEOUT_CTL)—Offset 2Eh

Timeout Control Register

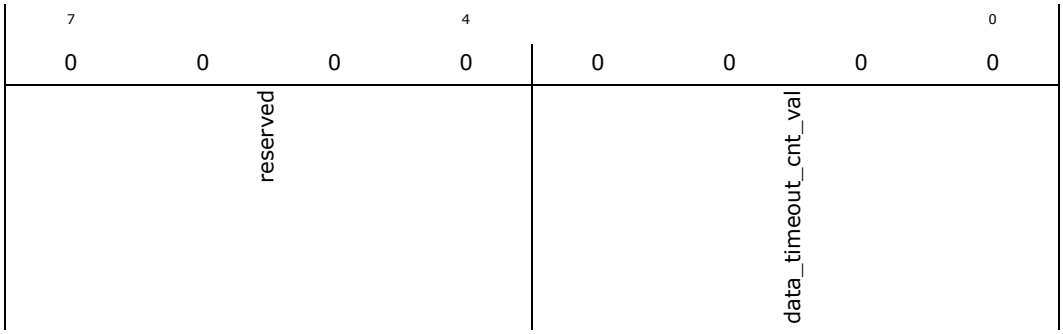
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 2Eh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RO	**Reserved (reserved):** Reserved
3:0	0x0 RW	**DATA_TIMEOUT_CNT_VAL (data_timeout_cnt_val):** Data Timeout Counter Value

6.6.19 Software Reset Register (SW_RST)—Offset 2Fh

Software Reset Register

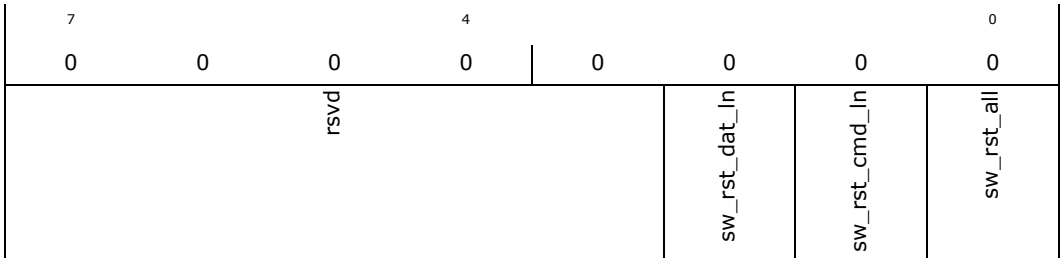
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 2Fh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0x0 RO	**RSVD (rsvd):** Reserved
2	0x0 RW	**SW_RST_DAT_LN (sw_rst_dat_ln):** Software Reset For DAT Line
1	0x0 RW	**SW_RST_CMD_LN (sw_rst_cmd_ln):** Software Reset For CMD Line
0	0x0 RW	**SW_RST_ALL (sw_rst_all):** Software Reset For All

6.6.20 Normal Interrupt Status Register (NML_INT_STATUS)—Offset 30h

Normal Interrupt Status Register

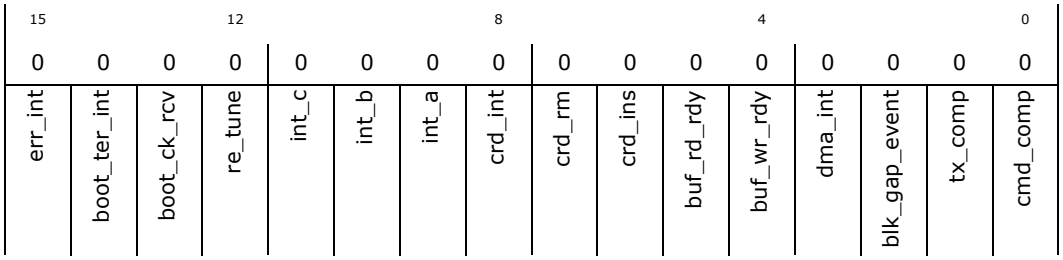
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**ERR_INT (err_int):** Error Interrupt
14	0x0 RW/1C	**BOOT_TER_INT (boot_ter_int):** boot ter int
13	0x0 RW/1C	**BOOT_ACK_RCV (boot_ck_rcv):** boot ack rcv
12	0x0 RO	**RE_TUNE (re_tune):** re tuning event
11	0x0 RO	**INT_C (int_c):** int c
10	0x0 RO	**INT_B (int_b):** int b
9	0x0 RO	**INT_A (int_a):** int a
8	0x0 RO	**CRD_INT (crd_int):** Card Interrupt
7	0x0 RW/1C	**CRD_RM (crd_rm):** Card Removal
6	0x0 RW/1C	**CRD_INS (crd_ins):** Card Insertion
5	0x0 RW/1C	**BUF_RD_RDY (buf_rd_rdy):** Buffer Read Ready
4	0x0 RW/1C	**BUF_WR_RDY (buf_wr_rdy):** Buffer Write Ready
3	0x0 RW/1C	**DMA_INT (dma_int):** DMA Interrupt

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW/1C	**BLK_GAP_EVENT (blk_gap_event):** Block Gap Event
1	0x0 RW/1C	**TX_COMP (tx_comp):** Transfer Complete
0	0x0 RW/1C	**CMD_COMP (cmd_comp):** Command Complete

6.6.21 Error Interrupt Status Register (ERR_INT_STATUS)—Offset 32h

Error Interrupt Status Register

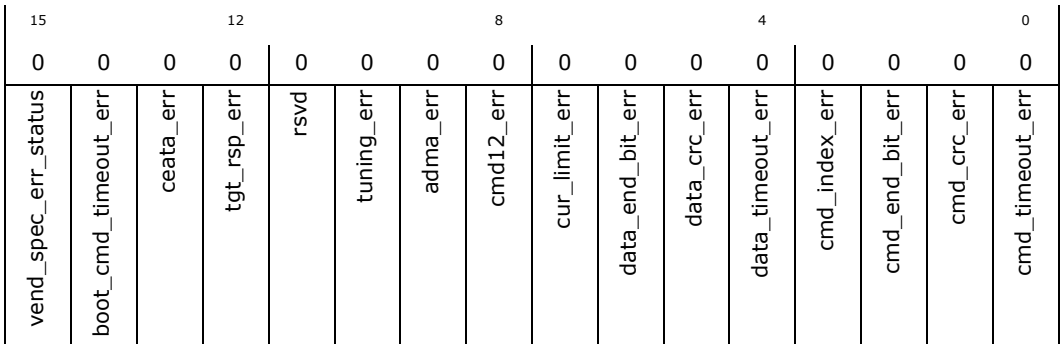
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 32h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**VEND_SPEC_ERR_STATUS (vend_spec_err_status):** Vendor Specific Error Status
14	0x0 RO	**BOOT_CMD_TIMEOUT_ERR (boot_cmd_timeout_err):** Occur if the boot are access command is issued to the agent which has no permission to access the boot area.
13	0x0 RO	**CEATA_ERR (ceata_err):** Occurs when ATA command termination has occurred due to an error condition the device has encountered.
12	0x0 RW/1C	**TGT_RSP_ERR (tgt_rsp_err):** Occurs when detecting ERROR in m_hresp(dma transaction)
11	0x0 RO	**RSVD (rsvd):** Reserved
10	0x0 RO	**TUNING_ERR (tuning_err):** Tuning Error

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RW/1C	**ADMA_ERR (adma_err):** ADMA Error
8	0x0 RW/1C	**CMD12_ERR (cmd12_err):** Auto CMD12 Error
7	0x0 RW/1C	**CUR_LIMIT_ERR (cur_limit_err):** Current Limit Error
6	0x0 RW/1C	**DATA_END_BIT_ERR (data_end_bit_err):** Data End Bit Error
5	0x0 RW/1C	**DATA_CRC_ERR (data_crc_err):** Data CRC Error
4	0x0 RW/1C	**DATA_TIMEOUT_ERR (data_timeout_err):** Data Timeout Error
3	0x0 RW/1C	**CMD_INDEX_ERR (cmd_index_err):** Command Index Error
2	0x0 RW/1C	**CMD_END_BIT_ERR (cmd_end_bit_err):** Command End Bit Error
1	0x0 RW/1C	**CMD_CRC_ERR (cmd_crc_err):** Command CRC Error
0	0x0 RW/1C	**CMD_TIMEOUT_ERR (cmd_timeout_err):** Command Timeout Error

6.6.22 Normal Interrupt Status Enable (NRM_INT_STATUS_EN)—Offset 34h

Normal Interrupt Status Enable

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
fixed_0	boot_term_int_en	boot_ack_rcv_en	re_tune_en	int_c_en	int_b_en	int_a_en	crd_int_stat_en	crd_rm_stat_en	crd_ins_stat_en	buf_rd_rdy_stat_en	buf_wr_rdy_stat_en	dma_int_stat_en	blk_gap_event_stat_en	tx_comp_stat_en	cmd_comp_stat_en

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**FIXED_0 (fixed_0):** Fixed to 0
14	0x0 RW	**BOOT_TERM_INT_EN (boot_term_int_en):** 0 - Masked
13	0x0 RW	**BOOT_ACK_RCV_EN (boot_ack_rcv_en):** 0 -Masked
12	0x0 RW	**RE_TUNE_EN (re_tune_en):** re tuning event enable
11	0x0 RW	**INT_C_EN (int_c_en):** int c enable
10	0x0 RW	**INT_B_EN (int_b_en):** int b enable
9	0x0 RW	**INT_A_EN (int_a_en):** int a enable
8	0x0 RW	**CRD_INT_STAT_EN (crd_int_stat_en):** Card Interrupt Status Enable
7	0x0 RW	**CRD_RM_STAT_EN (crd_rm_stat_en):** Card Removal Status Enable
6	0x0 RW	**CRD_INS_STAT_EN (crd_ins_stat_en):** Card Insertion Status Enable
5	0x0 RW	**BUF_RD_RDY_STAT_EN (buf_rd_rdy_stat_en):** Buffer Read Ready Status Enable
4	0x0 RW	**BUF_WR_RDY_STAT_EN (buf_wr_rdy_stat_en):** Buffer Write Ready Status Enable
3	0x0 RW	**DMA_INT_STAT_EN (dma_int_stat_en):** DMA Interrupt Status Enable
2	0x0 RW	**BLK_GAP_EVENT_STAT_EN (blk_gap_event_stat_en):** Block Gap Event Status Enable
1	0x0 RW	**TX_COMP_STAT_EN (tx_comp_stat_en):** Transfer Complete Status Enable
0	0x0 RW	**CMD_COMP_STAT_EN (cmd_comp_stat_en):** Command Complete Status Enable

6.6.23 Error Interrupt Status Enable Register (ERR_INT_STAT_EN)—Offset 36h

Error Interrupt Status Enable Register

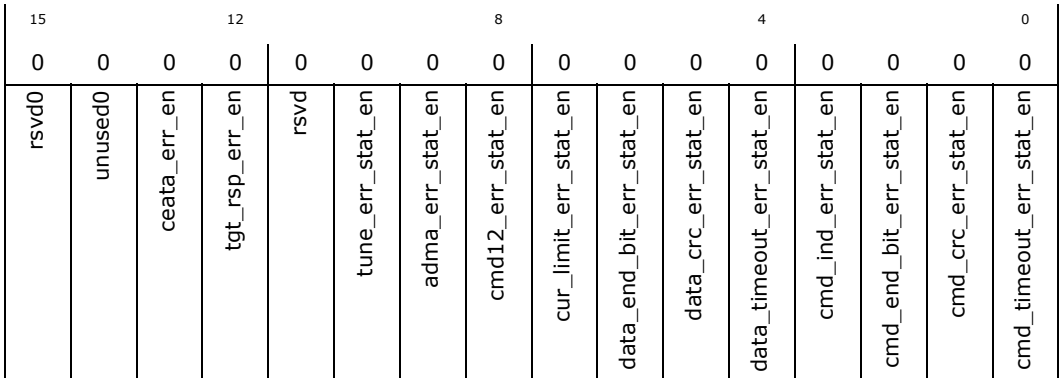
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 36h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**RSVD0 (rsvd0):** Reserved
14	0x0 RW	**UNUSED0 (unused0):** Unused
13	0x0 RW	**CEATA_ERR_EN (ceata_err_en):** 0 - masked
12	0x0 RW	**TGT_RSP_ERR_EN (tgt_rsp_err_en):** 0 - masked
11	0x0 RO	**RSVD (rsvd):** Reserved
10	0x0 RW	**TUNE_ERR_STATE_EN (tune_err_stat_en):** 0 - masked
9	0x0 RW	**ADMA_ERR_STAT_EN (adma_err_stat_en):** ADMA Error Status Enable
8	0x0 RW	**CMD12_ERR_STAT_EN (cmd12_err_stat_en):** Auto CMD12 Error Status Enable
7	0x0 RW	**CUR_LIMIT_ERR_STAT_EN (cur_limit_err_stat_en):** Current Limit Error Status Enable
6	0x0 RW	**DATA_END_BIT_ERR_STAT_EN (data_end_bit_err_stat_en):** Data End Bit Error Status Enable
5	0x0 RW	**DATA_CRC_ERR_STAT_EN (data_crc_err_stat_en):** Data CRC Error Status Enable
4	0x0 RW	**DATA_TIMEOUT_ERR_STAT_EN (data_timeout_err_stat_en):** Data Timeout Error Status Enable
3	0x0 RW	**CMD_IND_ERR_STAT_EN (cmd_ind_err_stat_en):** Command Index Error Status Enable
2	0x0 RW	**CMD_END_BIT_ERR_STAT_EN (cmd_end_bit_err_stat_en):** Command End Bit Error Status Enable
1	0x0 RW	**CMD_CRC_ERR_STAT_EN (cmd_crc_err_stat_en):** Command CRC Error Status Enable
0	0x0 RW	**CMD_TIMEOUT_ERR_STAT_EN (cmd_timeout_err_stat_en):** Command Timeout Error Status Enable

6.6.24 Normal Interrupt Signal Enable Register (NRM_INT_SIG_EN)—Offset 38h

Normal Interrupt Signal Enable Register

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
fixed_0	boot_term_int_sig_en	boot_ack_rcv_sig_en	re_tune_sig_en	int_c_sig_en	int_b_sig_en	int_a_sig_en	crd_int_sig_en	crd_rm_sig_en	crd_ins_sig_en	buf_rd_rdy_sig_en	buf_wr_rdy_sig_en	dma_int_sig_en	blk_gap_event_sig_en	tx_comp_sig_en	cmd_comp_sig_en

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**FIXED_0 (fixed_0):** Fixed to 0
14	0x0 RW	**BOOT_TERM_INT_SIG_EN (boot_term_int_sig_en):** 0 - masked
13	0x0 RW	**BOOT_ACK_RCV_SIG_EN (boot_ack_rcv_sig_en):** 0 - masked
12	0x0 RW	**RE_TUNE_SIG_EN (re_tune_sig_en):** re tuning event Signal Enable
11	0x0 RW	**INT_C_SIG_EN (int_c_sig_en):** int c Signal Enable
10	0x0 RW	**INT_B_SIG_EN (int_b_sig_en):** int b Signal Enable
9	0x0 RW	**INT_A_SIG_EN (int_a_sig_en):** int a Signal Enable
8	0x0 RW	**CRD_INT_SIG_EN (crd_int_sig_en):** Card Interrupt Signal Enable
7	0x0 RW	**CRD_RM_SIG_EN (crd_rm_sig_en):** Card Removal Signal Enable
6	0x0 RW	**CRD_INS_SIG_EN (crd_ins_sig_en):** Card Insertion Signal Enable
5	0x0 RW	**BUF_RD_RDY_SIG_EN (buf_rd_rdy_sig_en):** Buffer Read Ready Signal Enable
4	0x0 RW	**BUF_WR_RDY_SIG_EN (buf_wr_rdy_sig_en):** Buffer Write Ready Signal Enable

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**DMA_INT_SIG_EN (dma_int_sig_en):** DMA Interrupt Signal Enable
2	0x0 RW	**BLK_GAP_EVENT_SIG_EN (blk_gap_event_sig_en):** Block Gap Event Signal Enable
1	0x0 RW	**TX_COMP_SIG_EN (tx_comp_sig_en):** Transfer Complete Signal Enable
0	0x0 RW	**CMD_COMP_SIG_EN (cmd_comp_sig_en):** Command Complete Signal Enable

6.6.25 Error Interrupt Signal Enable Register (ERR_INT_SIG_EN)—Offset 3Ah

Error Interrupt Signal Enable Register

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 3Ah

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0	unused0	ceata_err_sig_en	tgt_err_rsp_sig_en	rsvd	tune_err_sig	adma_err_sig_en	cmd12_err_sig_en	cur_limit_err_sig_en	data_end_bit_err_sig_en	data_crc_err_sig_en	data_timeout_err_stat_en	cmd_ind_err_stat_en	cmd_end_bit_err_stat_en	cmd_crc_err_stat_en	cmd_timeout_err_stat_en

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**RSVD0 (rsvd0):** Reserved
14	0x0 RW	**UNUSED0 (unused0):** Unused
13	0x0 RW	**CEATA_ERR_SIG_EN (ceata_err_sig_en):** 0 - masked
12	0x0 RW	**TGT_ERR_RSP_SIG_EN (tgt_err_rsp_sig_en):** 0 - masked
11	0x0 RO	**RSVD (rsvd):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RW	**TUNE_ERR_SIG (tune_err_sig):** 0 - masked
9	0x0 RW	**ADMA_ERR_SIG_EN (adma_err_sig_en):** ADMA Error Signal Enable
8	0x0 RW	**CMD12_ERR_SIG_EN (cmd12_err_sig_en):** Auto CMD12 Error Signal Enable
7	0x0 RW	**CUR_LIMIT_ERR_SIG_EN (cur_limit_err_sig_en):** Current Limit Error Signal Enable
6	0x0 RW	**DATA_END_BIT_ERR_SIG_EN (data_end_bit_err_sig_en):** Data End Bit Error Signal Enable
5	0x0 RW	**DATA_CRC_ERR_SIG_EN (data_crc_err_sig_en):** Data CRC Error Signal Enable
4	0x0 RW	**DATA_TIMEOUT_ERR_STAT_EN (data_timeout_err_stat_en):** Data Timeout Error Signal Enable
3	0x0 RW	**CMD_IND_ERR_STAT_EN (cmd_ind_err_stat_en):** Command Index Error Signal Enable
2	0x0 RW	**CMD_END_BIT_ERR_STAT_EN (cmd_end_bit_err_stat_en):** Command End Bit Error Signal Enable
1	0x0 RW	**CMD_CRC_ERR_STAT_EN (cmd_crc_err_stat_en):** Command CRC Error Signal Enable
0	0x0 RW	**CMD_TIMEOUT_ERR_STAT_EN (cmd_timeout_err_stat_en):** Command Timeout Error Signal Enable

6.6.26 Auto CMD12 Error Status Register and Host control 2 Register (CMD12_ERR_STAT_HOST_CTRL_2)—Offset 3Ch

Auto CMD12 Error Status Register and Host control 2 Register

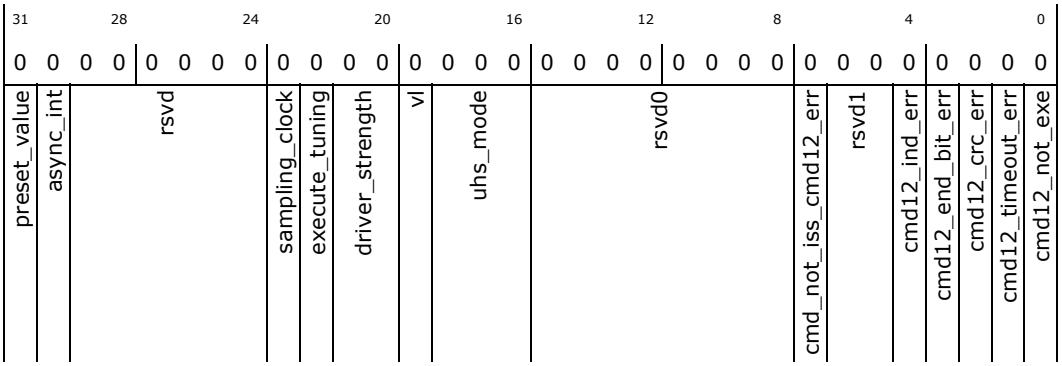
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**PRESET_VALUE (preset_value):** Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set to automatic This bit enables the functions defined in the Preset Value registers. 1 Automatic Selection by Preset Value are Enabled 0 SDCLK and Driver Strength are controlled by Host Driver If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver. If this bit is set to 1, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Controller as specified in the Preset Value registers.
30	0x0 RW	**ASYNC_INT (async_int):** This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode (and zero is set to Interrupt Pin Select in the Shared Bus Control register). If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card. 1 Enabled 0 Disabled
29:24	0x0 RO	**RSVD (rsvd):** Reserved
23	0x0 RW	**SAMPLING_CLOCK (sampling_clock):** This bit is set by tuning procedure when Execute Tuning is cleared
22	0x0 RW/AC	**EXECUTE_TUNING (execute_tuning):** This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by writing 0 for more detail about tuning procedure. 1 Execute Tuning 0 Not Tuned or Tuning Completed
21:20	0x0 RW	**DRIVER_STRENGTH (driver_strength):** Host Controller output driver in 1.8V signaling is selected by this bit
19	0x0 RW	**VL (vl):** This bit controls voltage regulator for I/O cell, 1 - 1.8V Signaling, 0 - 3.3V Signaling. This bit has to be set based on actual I/O signal voltage even though only a single voltage is supported in a platform
18:16	0x0 RW	**UHS_MODE (uhs_mode):** This field is used to select one of UHS-I modes

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**RSVD0 (rsvd0):** Reserved
7	0x0 RO	**CMD_NOT_ISS_CMD12_ERR (cmd_not_iss_cmd12_err):** Command Not Issued By Auto CMD12 Error
6:5	0x0 RO	**RSVD1 (rsvd1):** Reserved
4	0x0 RO	**CMD12_IND_ERR (cmd12_ind_err):** Auto CMD12 Index Error
3	0x0 RO	**CMD12_END_BIT_ERR (cmd12_end_bit_err):** Auto CMD12 End Bit Error
2	0x0 RO	**CMD12_CRC_ERR (cmd12_crc_err):** Auto CMD12 CRC Error
1	0x0 RO	**CMD12_TIMEOUT_ERR (cmd12_timeout_err):** Auto CMD12 Timeout Error
0	0x0 RO	**CMD12_NOT_EXE (cmd12_not_exe):** Auto CMD12 Not Executed

6.6.27 Capabilities Register (CAPABILITIES)—Offset 40h

Capabilities Register

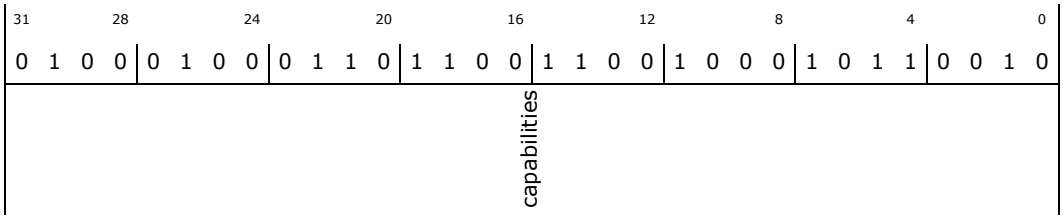
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 446CC8B2h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x446cc8b2 RO	**capabilities:** capabilities

6.6.28 Capabilities Register 2 (CAPABILITIES_2)—Offset 44h

Capabilities Register 2

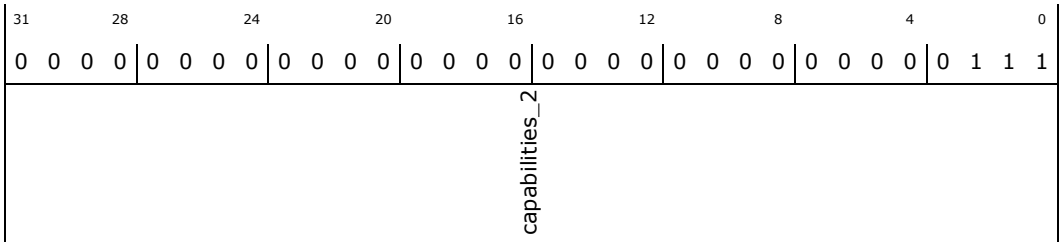
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000007h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x7 RO	**capabilities_2:** capabilities 2

6.6.29 Maximum Current Capabilities Register (MAX_CUR_CAP)—Offset 48h

These registers indicate maximum current capability for each voltage

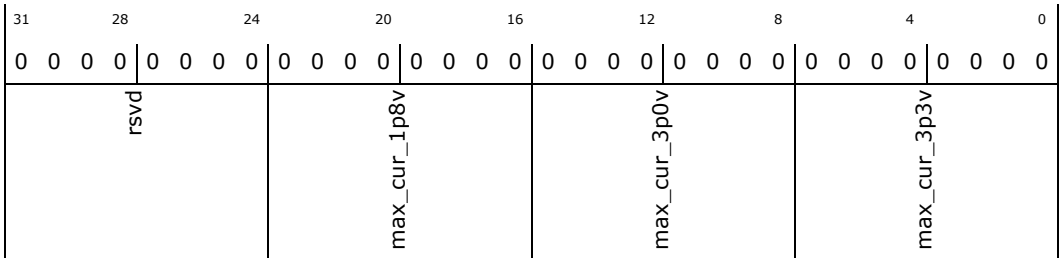
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD (rsvd):** Reserved
23:16	0x0 RO	**MAX_CUR_1p8V (max_cur_1p8v):** Maximum Current for 1.8V
15:8	0x0 RO	**MAX_CUR_3p0V (max_cur_3p0v):** Maximum Current for 3.0V

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**MAX_CUR_3p3V (max_cur_3p3v):** Maximum Current for 3.3V

6.6.30 Force Event Register for Auto CMD12 Error Status (FORCE_EVENT_CMD12_ERR_STAT)—Offset 50h

Force Event Register for Auto CMD12 Error Status

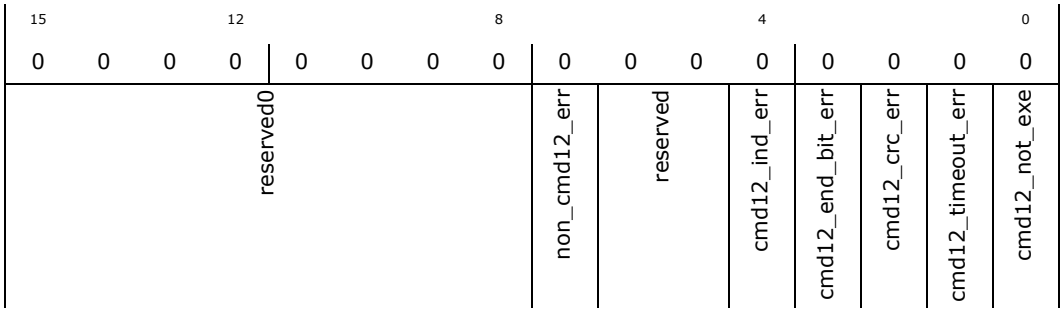
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Reserved0 (reserved0):** Reserved
7	0x0 WO	**NON_CMD12_ERR (non_cmd12_err):** Force Event for Command Not Issued By Auto CMD12 Error :
6:5	0x0 RO	**Reserved (reserved):** Reserved
4	0x0 WO	**CMD12_IND_ERR (cmd12_ind_err):** Force Event for Auto CMD12 Index Error
3	0x0 WO	**CMD12_END_BIT_ERR (cmd12_end_bit_err):** Force Event for Auto CMD12 End Bit Error
2	0x0 WO	**CMD12_CRC_ERR (cmd12_crc_err):** Force Event for Auto CMD12 CRC Error
1	0x0 WO	**CMD12_TIMEOUT_ERR (cmd12_timeout_err):** Force Event for Auto CMD12 Timeout Error
0	0x0 WO	**CMD12_NOT_EXE (cmd12_not_exe):** Force Event for Auto CMD12 Not Executed

6.6.31 Force Event Register for Error Interrupt Status (FORCE_EVENT_ERR_INT_STAT)—Offset 52h

Force Event Register for Error Interrupt Status

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + 52h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rsvd0		ceata_err	tgt_rsp_err	rsvd		adma_err	cmd12_err	cur_limit_err	data_end_bit_err	data_crc_err	data_timeout_err	cmd_ind_err	cmd_end_bit_err	cmd_crc_err	cmd_timeout_err

Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RO	**RSVD0 (rsvd0):** Reserved
13	0x0 RO	**CEATA_ERR (ceata_err):** Force Event for CEATA error, legacy feature not implemented
12	0x0 RO	**TGT_RSP_ERR (tgt_rsp_err):** Force Event for Target Response Error, legacy feature not implemented
11:10	0x0 RO	**RSVD (rsvd):** Reserved
9	0x0 WO	**ADMA_ERR (adma_err):** Force Event for ADMA Error
8	0x0 WO	**CMD12_ERR (cmd12_err):** Force Event for Auto CMD12 Error
7	0x0 WO	**CUR_LIMIT_ERR (cur_limit_err):** Force Event for Current Limit Error
6	0x0 WO	**DATA_END_BIT_ERR (data_end_bit_err):** Force Event for Data End Bit Error
5	0x0 WO	**DATA_CRC_ERR (data_crc_err):** Event for Data CRC Error
4	0x0 WO	**DATA_TIMEOUT_ERR (data_timeout_err):** Event for Data Timeout Error
3	0x0 WO	**CMD_IND_ERR (cmd_ind_err):** Force Event for Command Index Error
2	0x0 WO	**CMD_END_BIT_ERR (cmd_end_bit_err):** Force Event for Command End Bit Error

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 WO	**CMD_CRC_ERR (cmd_crc_err):** Force Event for Command CRC Error
0	0x0 WO	**CMD_TIMEOUT_ERR (cmd_timeout_err):** Force Event for Command Timeout Error

6.6.32 ADMA Error Status Register (ADMA_ERR_STAT)—Offset 54h

ADMA Error Status Register

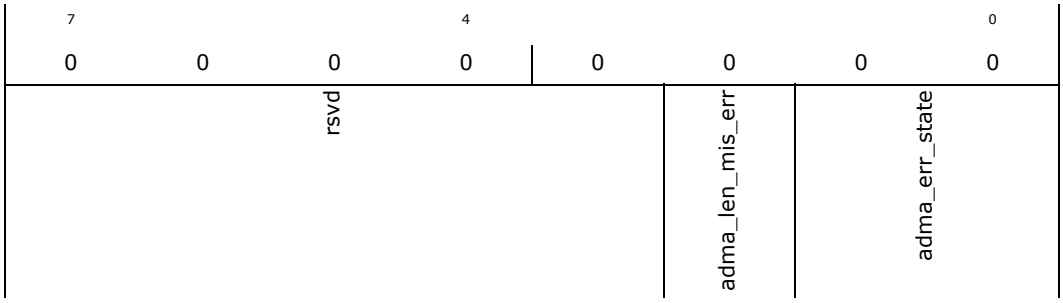
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0x0 RO	**RSVD (rsvd):** Reserved
2	0x0 RO	**ADMA_LEN_MIS_ERR (adma_len_mis_err):** ADMA Length Mismatch Error
1:0	0x0 RO	**ADMA_ERR_STATE (adma_err_state):** ADMA Error State

6.6.33 ADMA System Address Register (ADMA_SYS_ADDR)—Offset 58h

This register contains the physical Descriptor address used for ADMA data transfer.

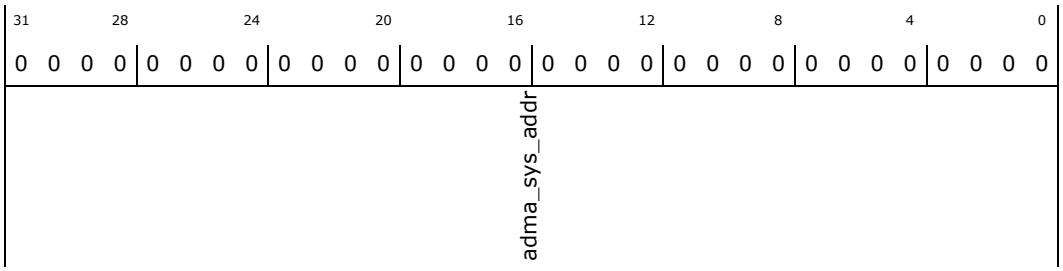
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**ADMA_SYS_ADDR (adma_sys_addr):** ADMA System Address

6.6.34 ADMA System Address Register (ADMA_SYS_ADDR_HIGH)—Offset 5Ch

This register contains the physical Descriptor address used for ADMA data transfer.

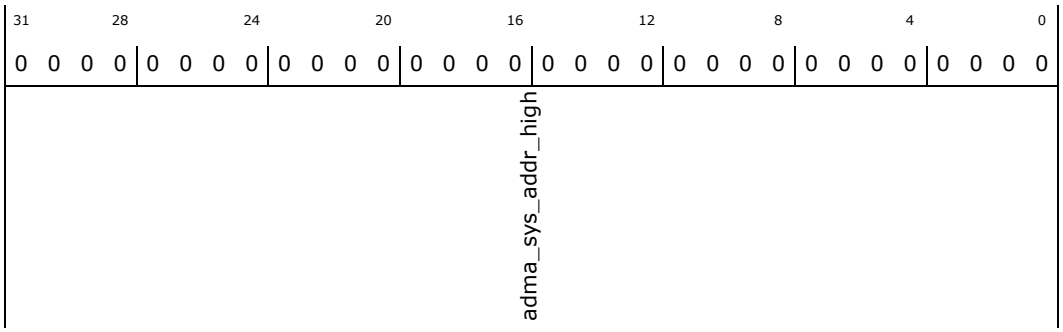
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**ADMA_SYS_ADDR_HIGH (adma_sys_addr_high):** High 32 bits of ADMA System Address for 64bit system

6.6.35 Preset Values registers (PRESET_VALUE_0)—Offset 60h

Preset Values init and default speed

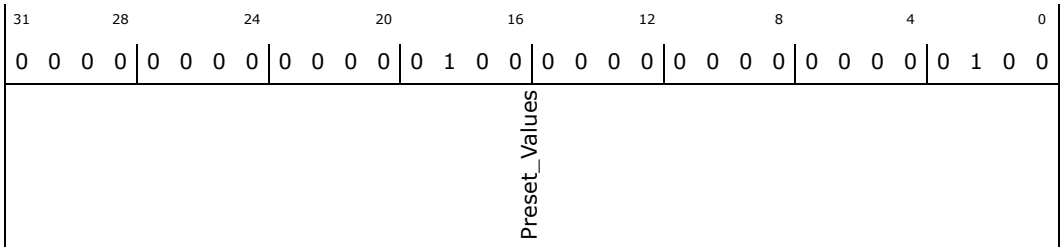
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00040004h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x40004 RO	**PresetValues (Preset_Values):** Reserved.

6.6.36 Preset Values 1 registers (PRESET_VALUE_1)—Offset 64h

Preset Values high and sdr12

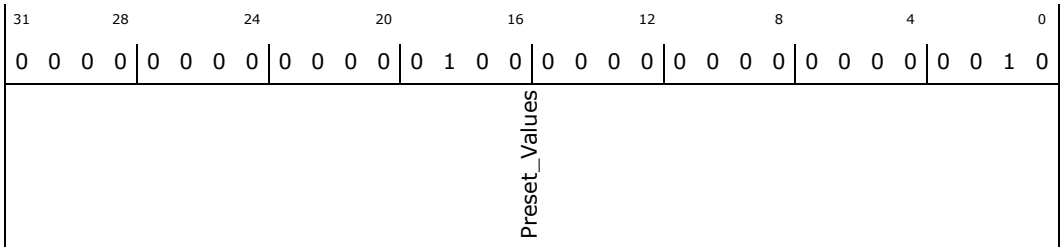
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00040002h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x40002 RO	**PresetValues (Preset_Values):** Reserved.

6.6.37 Preset Values 2 registers (PRESET_VALUE_2)—Offset 68h

Preset Values sdr25 and sdr50

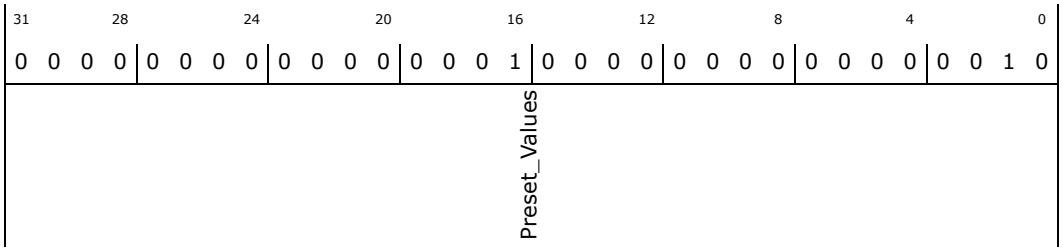
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00010002h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x10002 RO	**PresetValues (Preset_Values):** Reserved.

6.6.38 Preset Values 3 registers (PRESET_VALUE_3)—Offset 6Ch

Preset Values sdr104 and ddr50

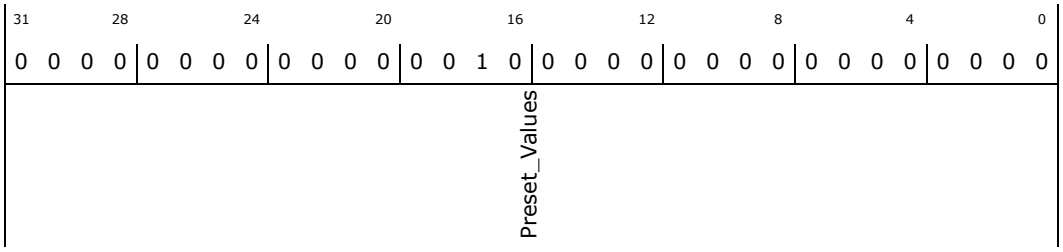
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00020000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x20000 RO	**PresetValues (Preset_Values):** Reserved.

6.6.39 BOOT_TIMEOUT_CTRL (BOOT_TIMEOUT_CTRL)—Offset 70h

BOOT_TIMEOUT_CTRL

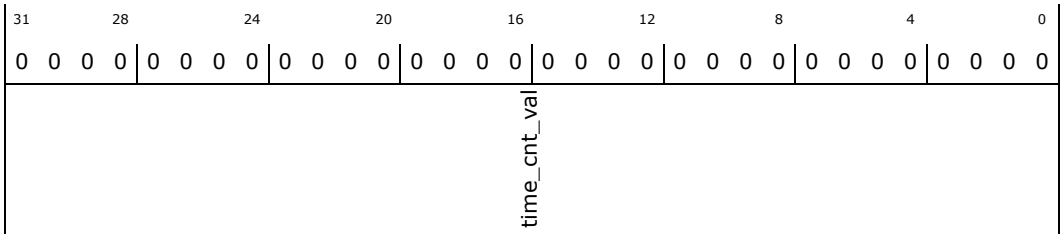
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**TIME_CNT_VAL (time_cnt_val):** Boot Data Timeout Counter Value

6.6.40 DEBUG_SEL (DEBUG_SEL)—Offset 74h

Debug Selection Register

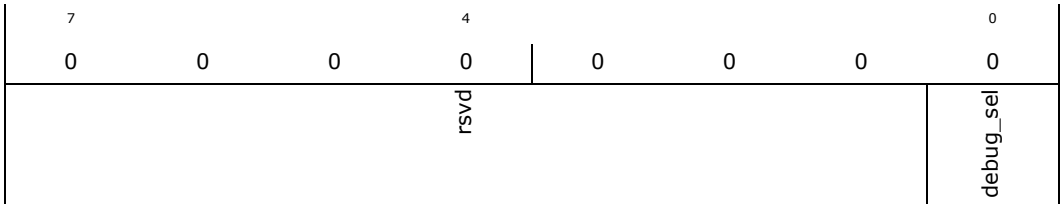
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:1	0x0 RO	**RSVD (rsvd):** Reserved
0	0x0 RO	**DEBUG_SEL (debug_sel):** 1 - cmd register, interrupt status, transmitter module, ahb_iface module and clk sdcard signals are probed out..

6.6.41 Shared Bus Control Register (SHARED_BUS)—Offset E0h

Shared Bus Control Register

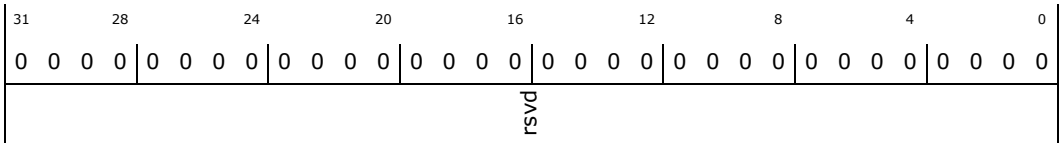
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD (rsvd):** Reserved

6.6.42 SPI_INT_SUP (SPI_INT_SUP)—Offset F0h

SPI_INT_SUP

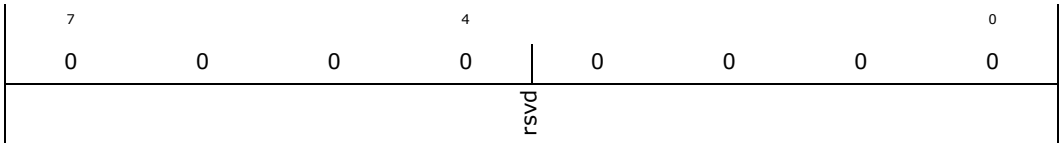
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [BAR] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**RSVD (rsvd):** Reserved

6.6.43 Slot Interrupt Status Register (SLOT_INT_STAT)—Offset FCh

Slot Interrupt Status Register

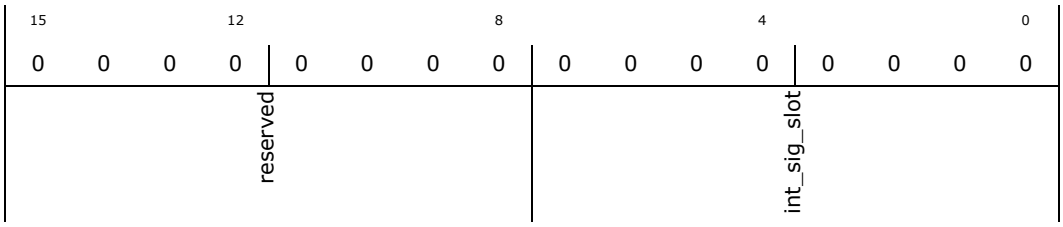
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Reserved (reserved):** Reserved
7:0	0x0 RO	**INT_SIG_SLOT (int_sig_slot):** Interrupt Signal For Each Slot

6.6.44 Host Controller Version Register (HOST_CTRL_VER)—Offset FEh

Host Controller Version Register

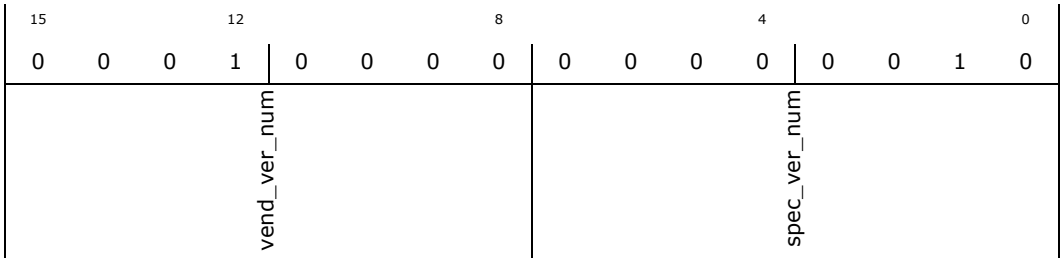
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [BAR] + FEh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:18, F:0] + 10h

Default: 1002h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0x10 RO	**VEND_VER_NUM (vend_ver_num):** Vendor Version Number
7:0	0x2 RO	**SPEC_VER_NUM (spec_ver_num):** Version Number

7 USB Controller Interfaces

7.1 USB xHCI PCI Configuration Registers

7.1.1 Summary of PCI Configuration Registers—0/20/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–1h	2	"Vendor ID (VID)—Offset 0h" on page 2052	8086h
2–3h	2	"Device ID (DID)—Offset 2h" on page 2052	8C31h
4–5h	2	"Access MethodDefault: 8C31h" on page 2052	0000h
6–7h	2	"Access MethodDefault: 0000h" on page 2052	0290h
8–8h	1	"Access MethodDefault: 0290h" on page 2053	00h
9–9h	1	"Programming Interface (PI)—Offset 9h" on page 2055	30h
A–Ah	1	"Access MethodDefault: 30h" on page 2055	03h
B–Ch	2	"Access MethodDefault: 03h" on page 2056	0Ch
D–Dh	1	"Access MethodDefault: 0Ch" on page 2056	00h
E–Fh	2	"Access MethodDefault: 00h" on page 2056	00h
10–17h	8	"Memory Base Address (MBAR)—Offset 10h" on page 2057	0000000000000004h
2C–2Dh	2	"Access MethodDefault: 0000000000000004h" on page 2057	0000h
2E–2Fh	2	"Access MethodDefault: 0000h" on page 2058	0000h
34–34h	1	"Access MethodDefault: 0000h" on page 2058	70h
3C–3Ch	1	"Access MethodDefault: 70h" on page 2059	00h
3D–3Fh	3	"Access MethodDefault: 00h" on page 2059	00h
58–5Bh	4	"Access MethodDefault: 00h" on page 2060	00000000h
60–60h	1	"Access MethodDefault: 00000000h" on page 2060	30h
61–61h	1	"Access MethodDefault: 30h" on page 2061	60h
62–62h	1	"Access MethodDefault: 60h" on page 2061	00h
70–70h	1	"Access MethodDefault: 00h" on page 2062	01h
71–71h	1	"Access MethodDefault: 01h" on page 2063	80h
72–73h	2	"Access MethodDefault: 80h" on page 2063	C1C2h
74–75h	2	"Access MethodDefault: C1C2h" on page 2064	0008h
80–80h	1	"Access MethodDefault: 0008h" on page 2065	05h
81–81h	1	"Access MethodDefault: 05h" on page 2066	00h
82–83h	2	"Access MethodDefault: 00h" on page 2066	0086h
84–87h	4	"Access MethodDefault: 0086h" on page 2067	00000000h

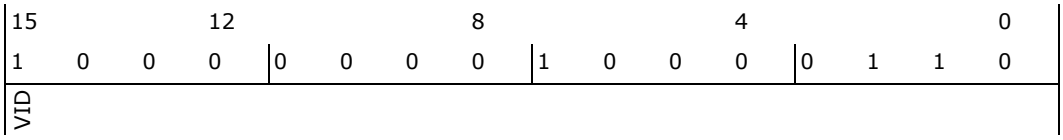
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
88–8Bh	4	"Access MethodDefault: 00000000h" on page 2068	00000000h
8C–8Dh	2	"Access MethodDefault: 00000000h" on page 2068	0000h
94–97h	4	"Fuse and Strap (FUS)—Offset 94h" on page 2069	00000000h
A4–A7h	4	"Access MethodDefault: 00000000h" on page 2069	00002000h
B0–B3h	4	"Access MethodDefault: 00002000h" on page 2070	00000000h
B4–B7h	4	"Access MethodDefault: 00000000h" on page 2071	00000000h
D0–D3h	4	"Access MethodDefault: 00000000h" on page 2072	00000000h
D4–D7h	4	"Access MethodDefault: 00000000h" on page 2073	00000000h

7.1.2 Vendor ID (VID)—Offset 0h

Access MethodDefault: 8086h

Type: PCI Configuration Register
(Size: 16 bits)

Offset: [B:0, D:20, F:0] + 0h



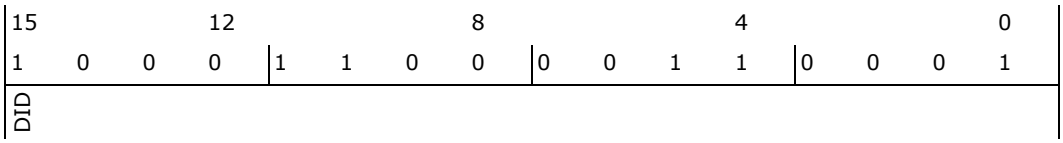
Bit Range	Default & Access	Field Name (ID): Description
15:0	0x8086 RO	**Vendor ID (VID):** Reserved. **Power Well:** Core

Device ID (DID)—Offset 2h

Access MethodDefault: 8C31h

Type: PCI Configuration Register
(Size: 16 bits)

Offset: [B:0, D:20, F:0] + 2h



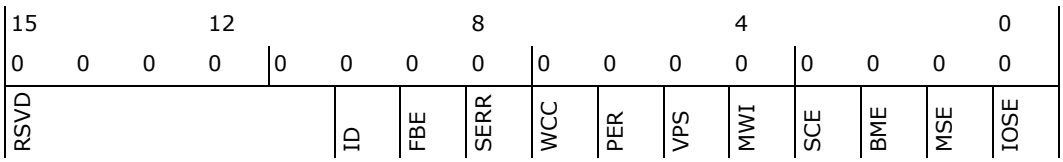
Bit Range	Default & Access	Field Name (ID): Description
15:0	0x8c31 RO/V	**Device ID (DID):** **Power Well:** Core

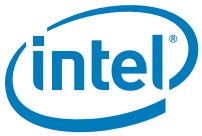
7.1.3 Command (CMD)—Offset 4h

Access MethodDefault: 0000h

Type: PCI Configuration Register
(Size: 16 bits)

Offset: [B:0, D:20, F:0] + 4h





Bit Range	Default & Access	Field Name (ID): Description
15:11	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
10	0x0 RW	**Interrupt Disable (ID):** When cleared to 0, the function is capable of generating interrupts. When 1, the function can not generate its interrupt to the interrupt controller. Note that the corresponding Interrupt Status bit is not affected by the interrupt enable. **Power Well:** Core
9	0x0 RO	**Fast Back to Back Enable (FBE):** Reserved. **Power Well:** Core
8	0x0 RW	**SERR# Enable (SERR):** When set to 1, the XHC is capable of generating (internally) SERR#. Refer section on error handling. **Power Well:** Core
7	0x0 RO	**Wait Cycle Control (WCC):** Reserved. **Power Well:** Core
6	0x0 RW	**Parity Error Response (PER):** When set to 1, the XHCI Host Controller will check for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase as recommended by the XHCI specification. Note that this applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#. **Power Well:** Core
4	0x0 RO	**Memory Write Invalidate (MWI):** Reserved. **Power Well:** Core
3	0x0 RO	**Special Cycle Enable (SCE):** Reserved. **Power Well:** Core
2	0x0 RW	**Bus Master Enable (BME):** When set, it allows XHC to act as a bus master. When cleared, it disable XHC from initiating transactions on the system bus. **Power Well:** Core
1	0x0 RW	**Memory Space Enable (MSE):** This bit controls access to the XHC Memory Space registers. If this bit is set, accesses to the XHC registers are enabled. The Base Address register for the XHC should be programmed before this bit is set. **Power Well:** Core
0	0x0 RO	**I/O Space Enable (IOSE):** Reserved as 0. Read-Only. **Power Well:** Core

7.1.4 Device Status (STS)—Offset 6h

Access MethodDefault: 0290h

Type: PCI Configuration Register
(Size: 16 bits)

Offset: [B:0, D:20, F:0] + 6h

15				12				8				4				0
0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	
DPE	SSE	RMA	RTA	STA	DEVT		MDPED	FBBC	UDF	MC	CL	IS	RSVD			

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW/1C	**Detected Parity Error (DPE):** This bit is set by the Intel PCH whenever a parity error is seen on the internal interface to the XHC host controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
14	0x0 RW/1C	**Signaled System Error (SSE):** This bit is set by the Intel PCH whenever it signals SERR# (internally). The SERR_EN bit (bit 8 in the Command Register) must be 1 for this bit to be set. Refer error handling section for complete list of conditions handled. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
13	0x0 RW/1C	**Received Master-Abort Status (RMA):** This bit is set when XHC, as a master, receives a master-abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
12	0x0 RW/1C	**Received Target Abort Status (RTA):** This bit is set when XHC, as a master, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
11	0x0 RW/1C	**Signaled Target-Abort Status (STA):** This bit is used to indicate when the XHC function responds to a cycle with a target abort. **Power Well:** Core
10:9	0x1 RO	**DEVSEL# Timing Status (DEVT):** This 2-bit field defines the timing for DEVSEL# assertion. Read-Only. **Power Well:** Core
8	0x0 RW/1C	**Master Data Parity Error Detected (MDPED):** This bit is set by the Intel PCH whenever a data parity error is detected on a XHC read completion packet on the internal interface to the XHC host controller and bit 6 of the Command register is set to 1. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
7	0x1 RO	**Fast Back-to-Back Capable (FBBC):** Reserved as 1 Read-Only. **Power Well:** Core
6	0x0 RO	**User Definable Features (UDF):** Reserved as 0. Read-Only. **Power Well:** Core
5	0x0 RO	**66 MHz Capable (MC):** Reserved as 0. Read-Only. **Power Well:** Core
4	0x1 RO	**Capabilities List (CL):** Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RO/V	**Interrupt Status (IS):** This read-only bit reflects the state of this function's interrupt at the input of the enable/disable logic. This bit is a 1 when the interrupt is asserted. This bit will be 0 when the interrupt is deasserted. The value reported in this bit is independent of the value in the Interrupt Enable bit. **Power Well:** Core
2:0	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

7.1.5 Revision ID (RID)—Offset 8h

Access MethodDefault: 00h

Type: PCI Configuration Register
(Size: 8 bits)

Offset: [B:0, D:20, F:0] + 8h

7			4				0
0	0	0	0	0	0	0	0
RID							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO/V	**Revision ID (RID):** Refer Chap 6 for value. **Power Well:** Core

7.1.6 Programming Interface (PI)—Offset 9h

Access MethodDefault: 30h

Type: PCI Configuration Register
(Size: 8 bits)

Offset: [B:0, D:20, F:0] + 9h

7			4				0
0	0	1	1	0	0	0	0
PI							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x30 RO	**Programming Interface (PI):** A value of 30h indicates that this USB Host Controller conforms to the XHCI specification. **Power Well:** Core

7.1.7 Sub Class Code (SCC)—Offset Ah

Access MethodDefault: 03h

Type: PCI Configuration Register
(Size: 8 bits)

Offset: [B:0, D:20, F:0] + Ah

7			4				0
0	0	0	0	0	0	1	1
SCC							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x3 RO	**Sub Class Code (SCC):** A value of 03h indicates that this is a Universal Serial Bus Host Controller. **Power Well:** Core

7.1.8 Base Class Code (BCC)—Offset Bh

Access MethodDefault: 0Ch

Type: PCI Configuration Register
(Size: 8 bits)

Offset: [B:0, D:20, F:0] + Bh

7			4				0
0	0	0	0	1	1	0	0
BCC							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0xc RO	**Base Class Code (BCC):** A value of 0Ch indicates that this is a Serial Bus controller. **Power Well:** Core

Master Latency Timer (MLT)—Offset Dh

Access MethodDefault: 00h

Type: PCI Configuration Register
(Size: 8 bits)

Offset: [B:0, D:20, F:0] + Dh

7			4				0
0	0	0	0	0	0	0	0
MLT							

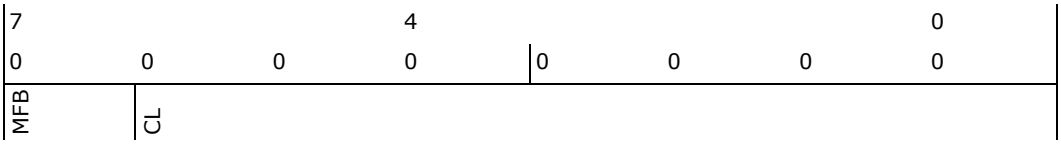
Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**Master Latency Timer (MLT):** Because the XHC controller is internally implemented with arbitration on an internal interface, it does not need a master latency timer. The bits will be fixed at 0. **Power Well:** Core

7.1.9 Header Type (HT)—Offset Eh

Access MethodDefault: 00h

Type: PCI Configuration Register
(Size: 8 bits)

Offset: [B:0, D:20, F:0] + Eh



Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**Multi-Function Bit (MFB):** Read only indicating single function device. **Power Well:** Core
6:0	0x0 RO	**Configuration layout (CL):** Hardwired to 0 to indicate a standard PCI configuration layout. **Power Well:** Core

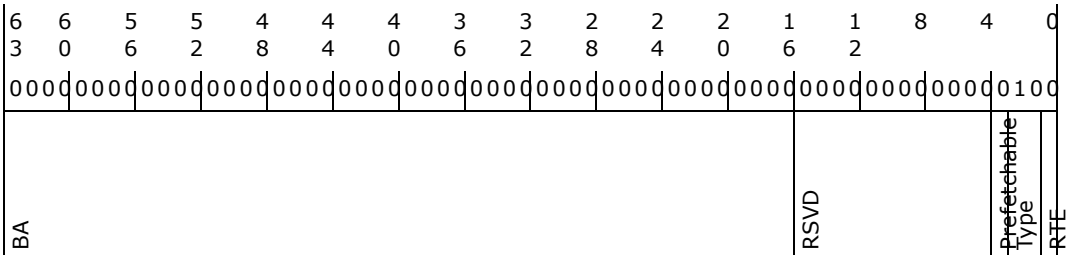
7.1.10 Memory Base Address (MBAR)—Offset 10h

Value in this register will be different after the enumeration process.

Access MethodDefault: 0000000000000004h

Type: PCI Configuration Register
(Size: 64 bits)

Offset: [B:0, D:20, F:0] + 10h



Bit Range	Default & Access	Field Name (ID): Description
63:16	0x0 RW	**Base Address (BA):** Bits (63:16) correspond to memory address signals (63:16), respectively. This gives 64 KB of relocatable memory space aligned to 64 KB boundaries. **Power Well:** Core
15:4	0x0 RO	**Reserved (RSVD):** Reserved. Read-Only 0, this indicates that this function is requesting an 64KB block of memory. **Power Well:** Core
3	0x0 RO	**Prefetchable:** This bit is hardwired to 0 indicating that this range should not be prefetched. **Power Well:** Core
2:1	0x2 RO	**Type:** If this field is hardwired to 00 it indicates that this range can be mapped anywhere within 32-bit address space. If this field is hardwired to 10 it indicates that this range can be mapped anywhere within 64-bit address space. **Power Well:** Core
0	0x0 RO	**Resource Type Indicator (RTE):** This bit is hardwired to 0 indicating that the base address field in this register maps to memory space **Power Well:** Core

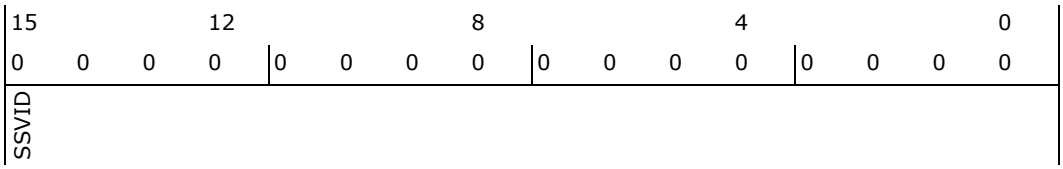
7.1.11 USB Subsystem Vendor ID (SSVID)—Offset 2Ch

This register is modified and maintained by BIOS

Access MethodDefault: 0000h

Type: PCI Configuration Register
(Size: 16 bits)

Offset: [B:0, D:20, F:0] + 2Ch



Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW/L	**USB Subsystem Vendor ID (SSVID):** This register, in combination with the USB Subsystem ID register, enables the operating system to distinguish each subsystem from the others. **Power Well:** Core

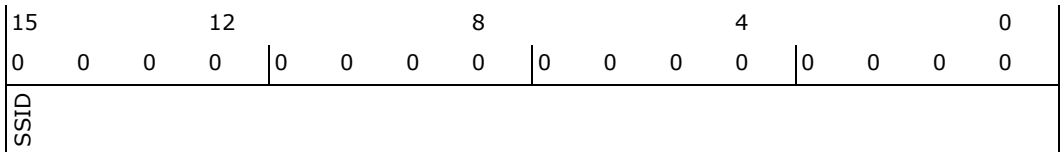
7.1.12 USB Subsystem ID (SSID)—Offset 2Eh

This register is modified and maintained by BIOS

Access MethodDefault: 0000h

Type: PCI Configuration Register
(Size: 16 bits)

Offset: [B:0, D:20, F:0] + 2Eh



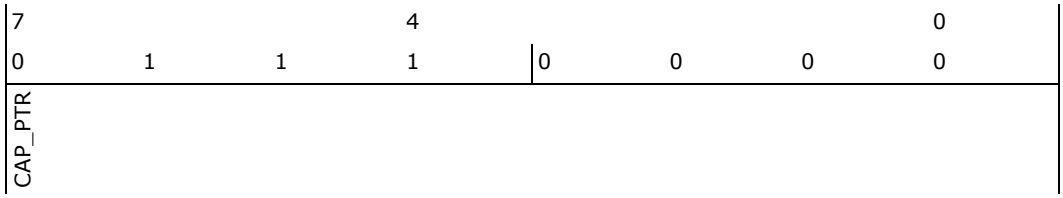
Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW/L	**USB Subsystem ID (SSID):** BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s). **Power Well:** Core

7.1.13 Capabilities Pointer (CAP_PTR)—Offset 34h

Access MethodDefault: 70h

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:20, F:0] + 34h



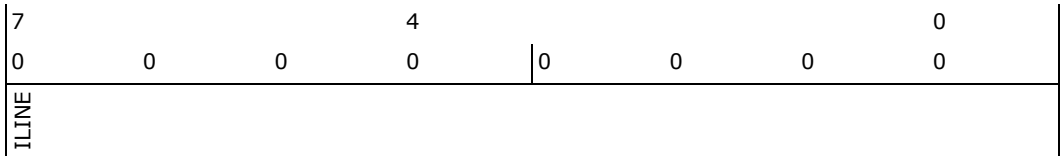
Bit Range	Default & Access	Field Name (ID): Description
7:0	0x70 RO	**Capabilities Pointer (CAP_PTR):** This register points to the starting offset of the capabilities ranges. **Power Well:** Core

7.1.14 Interrupt Line (ILINE)—Offset 3Ch

Access MethodDefault: 00h

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:20, F:0] + 3Ch



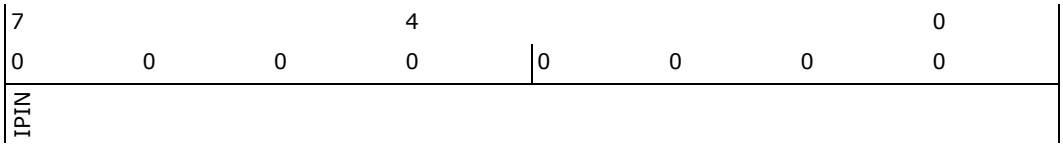
Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**Interrupt Line (ILINE):** This data is not used by the Intel PCH. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to. **Power Well:** Core

7.1.15 Interrupt Pin (IPIN)—Offset 3Dh

Access MethodDefault: 00h

Type: PCI Configuration Register
(Size: 8 bits)

Offset: [B:0, D:20, F:0] + 3Dh



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**Interrupt pin (IPIN):** Bits 7:0 reflect the Interrupt Pin assigned to the host controller by the platform (and are hardwired). **Power Well:** Core

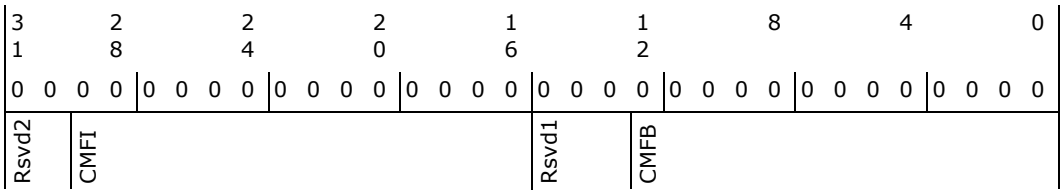
This 32 bit register is used for audio stream synchronization across different devices. Global signal sample_now captures a value in AUDSYNC register.

7.1.16 Audio Time Synchronization (AUDSYNC)—Offset 58h

Access MethodDefault: 00000000h

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:20, F:0] + 58h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
29:16	0x0 RO/V	**Captured Frame List Current Index/Frame Number (CMFI):** The value in this register is updated in response to sample_now signal. Bits (29:16) reflect state of bits (13:0) of FRINDEX **Power Well:** Core
15:13	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12:0	0x0 RO/V	**Captured Micro-frame BLIF (CMFB):** The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done in FLA. **Power Well:** Core

7.1.17 Serial Bus Release Number (SBRN)—Offset 60h

Access MethodDefault: 30h

Type: PCI Configuration Register
(Size: 8 bits)

Offset: [B:0, D:20, F:0] + 60h

7			4				0
0	0	1	1	0	0	0	0
SBRN							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x30 RO	**Serial Bus Release Number (SBRN):** A value of 30h indicates that this controller follows USB release 3.0. **Power Well:** SUS

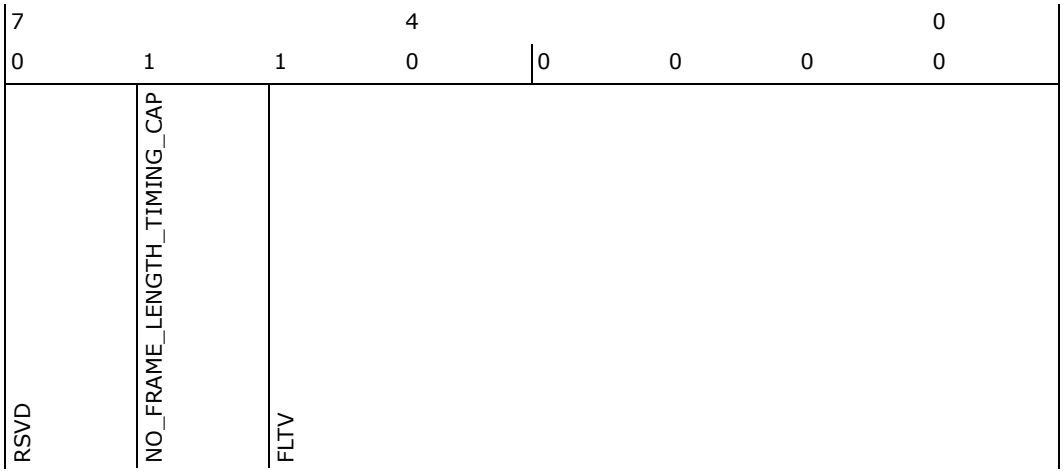
7.1.18 Frame Length Adjustment (FLADJ)—Offset 61h

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register should only be modified when the HChalted bit in the USBSTS register is a one. Changing value of this register while the host controller is operating yields undefined results.

Access MethodDefault: 60h

Type: PCI Configuration Register
(Size: 8 bits)

Offset: [B:0, D:20, F:0] + 61h



Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**Reserved (RSVD):** . **Power Well:** SUS
6	0x1 RO	**No Frame Length Timing Capability (NO_FRAME_LENGTH_TIMING_CAP):** This flag is set to 1 to indicate that the host controller does not support a programmable Frame Length Timing Value field. **Power Well:** Core
5:0	0x20 RO	**Frame Length Timing Value (FLTV):** SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (number of High Speed bit times) FLADJ Value (decimal) (decimal) 59488 0 (00h) 59504 1 (01h) 59520 2 (02h) ... 59984 31 (1Fh) 60000 32 (20h) ... 60480 62 (3Eh) 60496 63 (3Fh) Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (# High Speed bit times) FLADJ Value **Power Well:** SUS

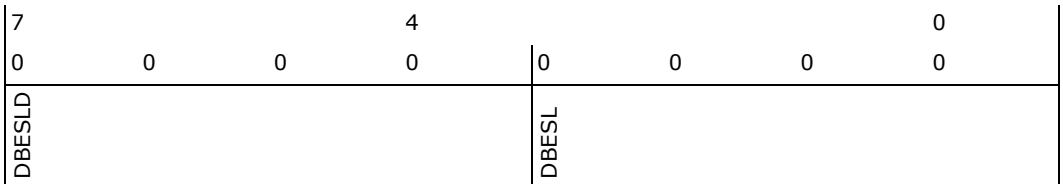
7.1.19 Best Effort Service Latency (BESL)—Offset 62h

Best Effort Service Latency.

Access MethodDefault: 00h

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:20, F:0] + 62h



Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW/L	**Default Best Effort Service Latency Deep (DBESLD):** Default Best Effort Service Latency (DBESLD) If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESLD field. This is programmed by BIOS based on platform parameters. **Power Well:** Core
3:0	0x0 RW/L	**Default Best Effort Service Latency (DBESL):** If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESL field. This is programmed by BIOS based on platform parameters. **Power Well:** Core

7.1.20 PCI Power Management Capability ID (PM_CID)—Offset 70h

Access MethodDefault: 01h

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:20, F:0] + 70h

7			4				0
0	0	0	0	0	0	0	1
PM_CID							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x1 RO	**PCI Power Management Capability ID (PM_CID):** A value of 01h indicates that this is a PCI Power Management capabilities field. **Power Well:** Core

7.1.21 Next Item Pointer #1 (PM_NEXT)—Offset 71h

This register is modified and maintained by BIOS

Access MethodDefault: 80h

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:20, F:0] + 71h

7			4				0
1	0	0	0	0	0	0	0
PM_NEXT							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x80 RW/L	**Next Item Pointer #1 (PM_NEXT):** This register defaults to 80h, which indicates that the next capability registers begin at configuration offset 80h. This register is writable when the Access Control bit is set to '0'. This allows BIOS to effectively hide the next capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Values of: 80h implies next capability is MSI 00h implies that MSI capability is hidden. Note: This value is never expected to be programmed. **Power Well:** Core

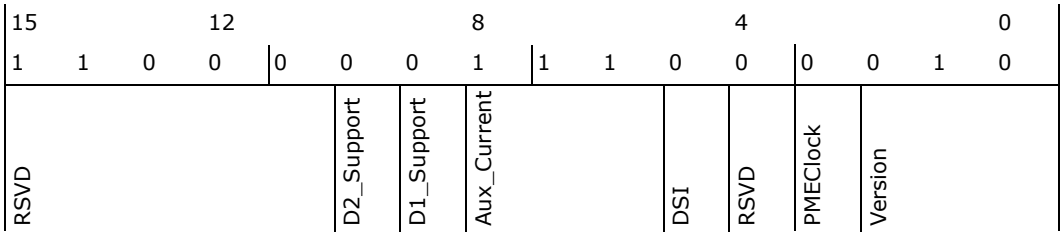
7.1.22 Power Management Capabilities (PM_CAP)—Offset 72h

Normally, this register is read-only to report capabilities to the power management software. In order to report different power management capabilities depending on the system in which the Intel PCH is used, the write access to this register is controlled by the Access Control bit (ACCTRL). The value written to this register does not affect the hardware other than changing the value returned during a read. This register is modified and maintained by BIOS

Access MethodDefault: C1C2h

Type: PCI Configuration Register (Size: 16 bits)

Offset: [B:0, D:20, F:0] + 72h



Bit Range	Default & Access	Field Name (ID): Description
15:11	0x18 RO	**Reserved (RSVD):** Reserved.
10	0x0 RW/L	**D2_Support:** The D2 state is not supported. **Power Well:** Core
9	0x0 RW/L	**D1_Support:** The D1 state is not supported. **Power Well:** Core
8:6	0x7 RW/L	**Aux_Current:** The Intel PCH XHC reports 375mA maximum Suspend well current required when in the D3cold state. This value can be written by BIOS when a more accurate value is known. **Power Well:** Core
5	0x0 RW/L	**DSI:** The Intel PCH reports 0, indicating that no device-specific initialization is required. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
3	0x0 RW/L	**PME Clock (PMEClock):** The Intel PCH reports 0, indicating that no PCI clock is required to generate PME#. **Power Well:** Core
2:0	0x2 RW/L	**Version:** The Intel PCH reports 010, indicating that it complies with Revision 1.1 of the PCI Power Management Specification. **Power Well:** Core

7.1.23 Power Management Control/Status (PM_CS)—Offset 74h

Access MethodDefault: 0008h

Type: PCI Configuration Register
(Size: 16 bits)

Offset: [B:0, D:20, F:0] + 74h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
PME_Status	Data_Scale		Data_Select				PME_En	RSVD				NSR	RSVD2	PowerState	

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW/1C	**PME_Status:** This bit is set when the Intel PCH XHC would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). Writing a 0 has no effect. This bit must be explicitly cleared by the operating system each time the operating system is loaded. **Power Well:** SUS
14:13	0x0 RO	**Data_Scale:** The Intel PCH hardwires these bits to 00 because it does not support the associated Data register. **Power Well:** Core
12:9	0x0 RO	**Data_Select:** The Intel PCH hardwires these bits to 0000 because it does not support the associated Data register. **Power Well:** Core
8	0x0 RW	**PME_En:** A 1 enables the Intel PCH XHC to generate an internal PME signal when PME_Status is 1. This bit must be explicitly cleared by the operating system each time it is initially loaded. **Power Well:** SUS
7:4	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3	0x1 RO	**No Soft Reset (NSR):**), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. Transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. **Power Well:** Core
2	0x0 RO	**Reserved (RSVD2):** Reserved. **Power Well:** Core
1:0	0x0 RW	**PowerState:** This 2-bit field is used both to determine the current power state of XHC function and to set a new power state. The definition of the field values are: 00b - D0 state 11b - D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3hot state, the Intel PCH must not accept accesses to the XHC memory range, but the configuration space must still be accessible. **Power Well:** Core

7.1.24 Message Signaled Interrupt CID (MSI_CID)—Offset 80h

Access MethodDefault: 05h

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:20, F:0] + 80h

7			4				0
0	0	0	0	0	1	0	1
CID							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x5 RO	**Capability ID (CID):** Indicates that this is an MSI capability **Power Well:** Core

7.1.25 Next item pointer (MSI_NEXT)—Offset 81h

Access MethodDefault: 00h

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:20, F:0] + 81h

7			4				0
0	0	0	0	0	0	0	0
NEXT							

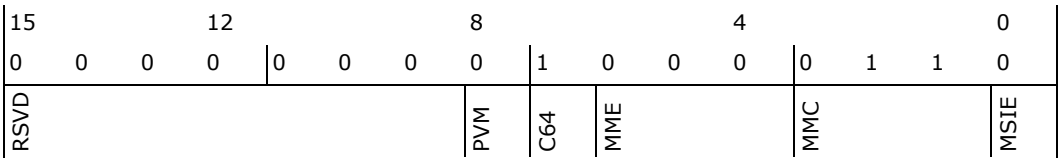
Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**Next Pointer (NEXT):** Indicates that this is the last item on the capability list **Power Well:** Core

7.1.26 Message Signaled Interrupt Message Control (MSI_MCTL)—Offset 82h

Access MethodDefault: 0086h

Type: PCI Configuration Register
(Size: 16 bits)

Offset: [B:0, D:20, F:0] + 82h



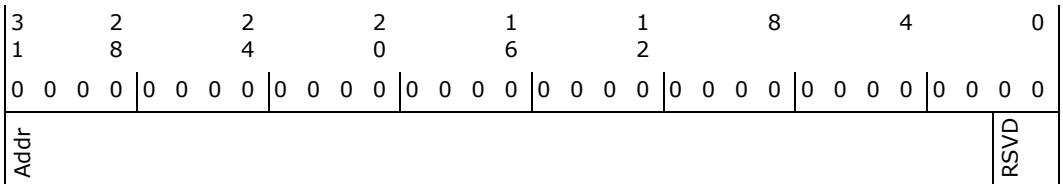
Bit Range	Default & Access	Field Name (ID): Description
15:9	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
8	0x0 RO	**Per-Vector Masking Capable (PVM):** Specifies whether controller supports MSI per vector masking. Not supported **Power Well:** Core
7	0x1 RO	**64 Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages. This device is 64-bit capable. **Power Well:** Core
6:4	0x0 RW	**Multiple Message Enable (MME):** Indicates the number of messages the controller should assert. This device supports multiple message MSI. **Power Well:** Core
3:1	0x3 RO	**Multiple Message Capable (MMC):** Indicates the number of messages the controller wishes to assert. This field must be set by HW to reflect the number of Interrupters supported. Encoding number of Vectors requested (number of Interrupters) 000 1 001 2 010 4 011 8 100 16 101 32 110-111 Reserved **Power Well:** Core
0	0x0 RW	**MSI Enable (MSIE):** If set to 1, MSI is enabled and the traditional interrupt pins are not used to generate interrupts. If cleared to 0, MSI operation is disabled and the traditional interrupt pins are used. **Power Well:** Core

7.1.27 Message Signaled Interrupt Message Address (MSI_MAD)—Offset 84h

Access MethodDefault: 00000000h

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:20, F:0] + 84h



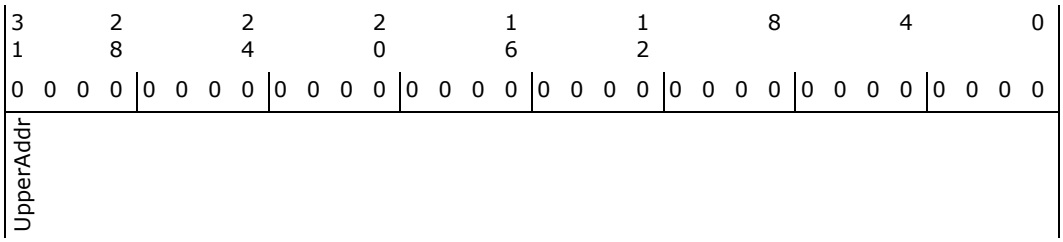
Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Addr:** Lower DW of system specified message address, always DWORD aligned **Power Well:** Core
1:0	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

7.1.28 Message Signaled Interrupt Upper Address (MSI_MUAD)—Offset 88h

Access MethodDefault: 00000000h

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:20, F:0] + 88h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Upper Addr (UpperAddr):** Upper DW of system specified message address. **Power Well:** Core

7.1.29 Message Signaled Interrupt Message Data (MSI_MD)—Offset 8Ch

Access MethodDefault: 0000h

Type: PCI Configuration Register
(Size: 16 bits)

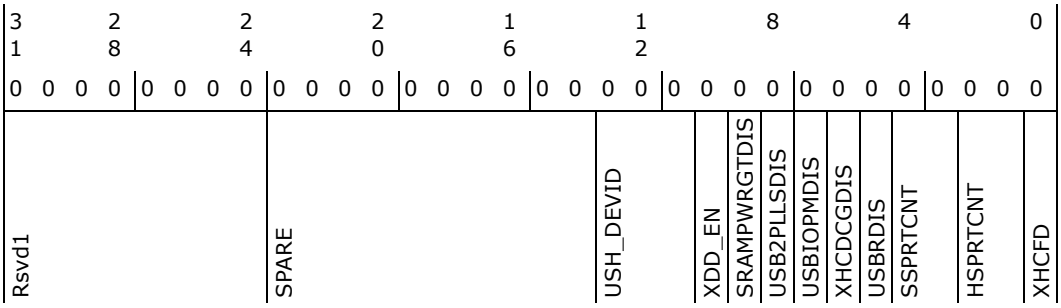
Offset: [B:0, D:20, F:0] + 8Ch

7.1.30 Fuse and Strap (FUS)—Offset 94h

Access MethodDefault: 00000000h

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:20, F:0] + 94h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
23:14	0x0 RO/V	**Spare Fuses (SPARE)** **Power Well:** SUS
13:11	0x0 RO/V	**USH DevID (USH_DEVID):** LSB bits of USH PCIe Device ID The 3 LSB bits enable defining up to 8 separate USH SKUs if required **Power Well:** SUS
10	0x0 RO/V	**Debug Device Enable (XDD_EN):** 0 : Debug Device is Enabled 1: Debug Device is Disabled **Power Well:** SUS
9	0x0 RO/V	**SRAM Power Gating Disable (SRAMPWRGTDIS):** 0: SRAM Power Gating Enabled 1: SRAM Power Gating Disabled **Power Well:** SUS
8	0x0 RO/V	**USB2 PLL Shutdown Disable (USB2PLLSDIS):** 0: USB2 PLL shutdown enabled 1: USB2 PLL shutdown disabled **Power Well:** SUS
7	0x0 RO/V	**USB I/O Power Management Disable (USBIOPMDIS):** 0: USB2 HW LPM and USB3 HW Ux under XHC enabled 1: USB2 HW LPM and USB3 HW Ux under XHC disabled **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
6	0x0 RO/V	**XHC Dynamic Clock Gating Disable (XHCDCGDIS):** 0: USB3 (XHC) dynamic clock gating enabled 1: USB3 (XHC) dynamic clock gating disabled **Power Well:** SUS
5	0x0 RO/V	**USBr Disable (USBRDIS):** 0: USBr enabled 1: USBr disabled **Power Well:** SUS
4:3	0x0 RO/V	**SS Port Count (SSPRTCNT):** This field specifies number of SS ports present. Supported combinations are: 00: 6 SS ports 01: 4 SS ports 10: 2 SS ports 11: 0 SS ports **Power Well:** SUS
2:1	0x0 RO/V	**HS Port Count (HSPRTCNT):** This field specifies number HS ports present. Supported combinations are: 00: 14 HS ports 01: 12 HS ports 10: 10 HS ports 11: N/A (reserved) **Power Well:** SUS
0	0x0 RO/V	**XHCI Function Disable (XHCFD):** When asserted, it indicates the XHCI is fused to function disabled. **Power Well:** SUS

7.1.31 High Speed Configuration 2 (HSCFG2)—Offset A4h

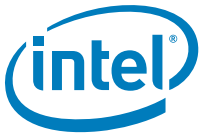
Access MethodDefault: 00002000h

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:20, F:0] + A4h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Rsvd1																PORT1_HOST_MODE_OVERRIDE	eUSB2SEL	HSAAIM	HSOAAPEPM	HSIAAPEPM	HSIIPAPC	HSIIPANEPT							HSIIPASIT			

Bit Range	Default & Access	Field Name (ID): Description
31:19	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
18	0x0 RW	**PORT1_HOST_MODE_OVERRIDE:** When set, this bit causes the Host_Device mux on port 1 to be forced into the Host mode. **Power Well:** Core
17:16	0x0 RW	**eUSB2SEL:** The two bits are associate with USB2 ports 1 - bit 16 and 2 - bit 2 0: Port is mapped to USB2 1: Port is mapped to eUSB2 **Power Well:** Core
15	0x0 RW	**HS ASYNC Active IN Mask (HSAAIM):** Determines if the Async Active will mask/ ignore IN EP s. 0 HS ASYNC Active will include IN EP s. 1 HS ASYNC Active will mask/ ignore IN EP s. **Power Well:** Core
14	0x0 RW	**HS OUT ASYNC Active Polling EP Mask (HSOAAPEPM):** Determines if the Async Active for OUT HS/FS/LS masks/ignores EP s that are polling/PINGing (HS) due to NAK. 0 HS OUT ASYNC Active will include EP s that are polling. 1 HS OUT ASYNC Active will mask/ignore EP s that are polling. **Power Well:** Core
13	0x1 RW	**HS IN ASYNC Active Polling EP Mask (HSIAAPEPM):** Determines if the Async Active for IN HS/FS/LS masks/ignores EP s that are polling due to NAK. 0 HS IN ASYNC Active will include EP s that are polling. 1 HS IN ASYNC Active will mask/ignore EP s that are polling. **Power Well:** Core
12:11	0x0 RW	**HS INTR IN Periodic Active Policy Control (HSIIPAPC):** Controls how the HS INTR IN periodic active is used to generate the global periodic active. This will determine how the smallest service interval among active EP s and number of active EP s are used. 0 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold OR Numb of EP Threshold values meet the requirement. 1 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold AND Numb of EP Threshold values meet the requirement. 2 Always allow HS INTR EP s to be used in the generation of the global Periodic Active indication. 3 Never allow HS INTR EP s to be used in the generation of the global Periodic Active indication **Power Well:** Core
10:4	0x0 RW	**HS INTR IN Periodic Active Num of EP Threshold (HSIIPANEPT):** Defines the threshold used to determine if Periodic Acive may include HS/FS/LS INTR IN EP active indication. If there are more than NumEPThreshold active HS/FS/LS INTR EP s then they may be included as part of the periodic active generation. **Power Well:** Core
3:0	0x0 RW	**HS INTR IN Periodic Active Service Interval Threshold (HSIIPASIT):** Defines the Service Interval threshold used to determine if Periodic Acive will include HS/FS/LS INTR IN EP active indication. If there are any active HS/FS/LS INTR EP s with a service interval less than or equal to this threshold then they may be included as part of the periodic active generation. **Power Well:** Core

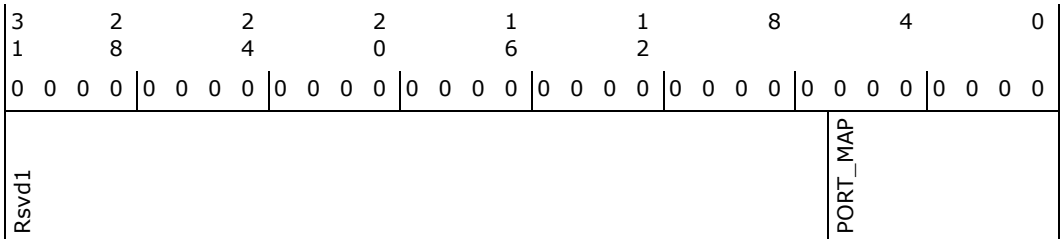
7.1.32 xHCI USB2 Overcurrent Pin Mapping 1 (U2OCM1)—Offset B0h

Reserved

Access MethodDefault: 00000000h

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:20, F:0] + B0h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**Rsvd (Rsvd1):** Reserved **Power Well:** Core
6:0	0x0 RW/L	**Port mapping (PORT_MAP):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std **Power Well:** Core

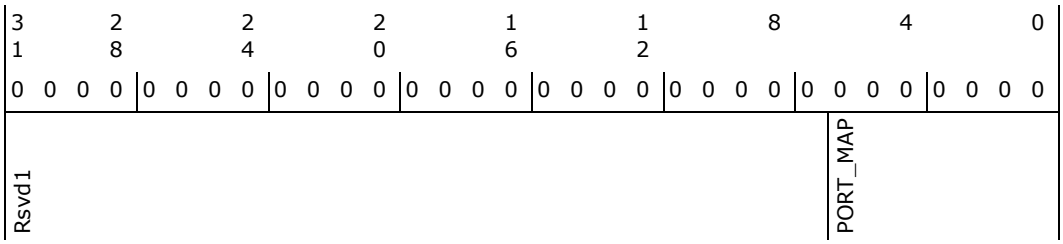
7.1.33 XHCI USB2 Overcurrent Pin Mapping 2 (U2OCM2)—Offset B4h

Reserved

Access MethodDefault: 00000000h

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:20, F:0] + B4h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**Rsvd (Rsvd1):** Reserved **Power Well:** Core
6:0	0x0 RW/L	**Port mapping (PORT_MAP):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std **Power Well:** Core

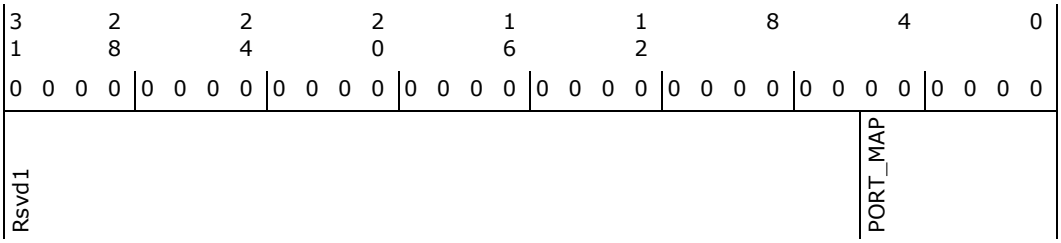
7.1.34 XHCI USB3 Overcurrent Pin Mapping 1 (U3OCM1)—Offset D0h

Reserved

Access MethodDefault: 00000000h

Type: PCI Configuration Register
(Size: 32 bits)

Offset: [B:0, D:20, F:0] + D0h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**Rsvd (Rsvd1):** Reserved **Power Well:** Core
5:0	0x0 RW/L	**Port mapping (PORT_MAP):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std **Power Well:** Core

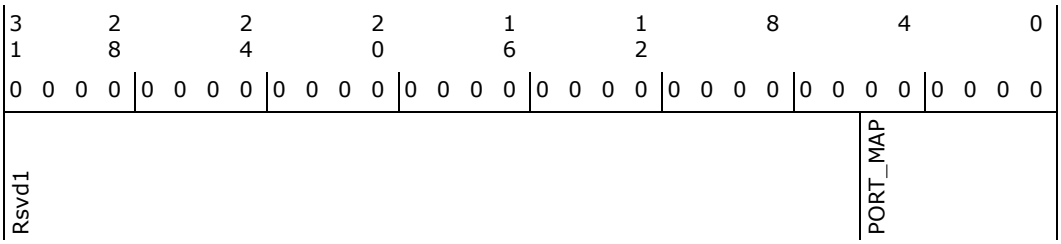
7.1.35 XHCI USB3 Overcurrent Pin Mapping 2 (U3OCM2)—Offset D4h

Reserved

Access MethodDefault: 00000000h

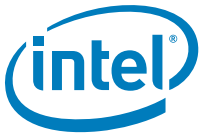
Type: PCI Configuration Register
(Size: 32 bits)

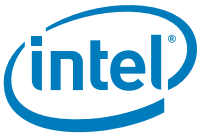
Offset: [B:0, D:20, F:0] + D4h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**Rsvd (Rsvd1):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5:0	0x0 RW/L	**Port mapping (PORT_MAP):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std **Power Well:** Core

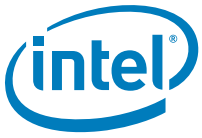




7.2 USB xHCI Memory Mapped I/O Registers Address Map

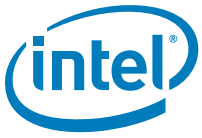
Table 38. Summary of Memory Mapped I/O Registers—MBAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–1h	2	"Capability Registers Length (CAPLENGTH)—Offset 0h" on page 2086	80h
2–3h	2	"Host Controller Interface Version Number (HCIVERSION)—Offset 2h" on page 2086	0100h
4–7h	4	"Structural Parameters 1 (HCSPARAMS1)—Offset 4h" on page 2087	0D000820h
8–Bh	4	"Structural Parameters 2 (HCSPARAMS2)—Offset 8h" on page 2087	94000054h
C–Fh	4	"Structural Parameters 3 (HCSPARAMS3)—Offset Ch" on page 2088	00040001h
10–13h	4	"Capability Parameters (HCCPARAMS)—Offset 10h" on page 2089	200077C1h
14–17h	4	"Doorbell Offset (DBOFF)—Offset 14h" on page 2090	00003000h
18–1Bh	4	"Runtime Register Space Offset (RTSOFF)—Offset 18h" on page 2091	00002000h
80–83h	4	"USB Command (USBCMD)—Offset 80h" on page 2091	00000000h
84–87h	4	"USB Status (USBSTS)—Offset 84h" on page 2092	00000001h
88–8Bh	4	"Page Size (PAGESIZE)—Offset 88h" on page 2094	00000001h
94–97h	4	"Device Notification Control (DNCTRL)—Offset 94h" on page 2094	00000000h
98–9Bh	4	"Command Ring Low (CRCR_LO)—Offset 98h" on page 2095	00000000h
9C–9Fh	4	"Command Ring High (CRCR_HI)—Offset 9Ch" on page 2095	00000000h
B0–B3h	4	"Device Context Base Address Array Pointer Low (DCBAAP_LO)—Offset B0h" on page 2096	00000000h
B4–B7h	4	"Device Context Base Address Array Pointer High (DCBAAP_HI)—Offset B4h" on page 2096	00000000h
B8–BBh	4	"Configure (CONFIG)—Offset B8h" on page 2097	00000000h
480–483h	4	"Port Status and Control USB2 (PORTSC1)—Offset 480h" on page 2097	000002A0h
484–487h	4	"Port Power Management Status and Control USB2 (PORTPMSC1)—Offset 484h" on page 2099	00000000h
48C–48Fh	4	"Port X Hardware LPM Control Register (PORTHLPMC1)—Offset 48Ch" on page 2100	00000000h
490–493h	4	"Port Status and Control USB2 (PORTSC2)—Offset 490h" on page 2101	000002A0h
494–497h	4	"Port Power Management Status and Control USB2 (PORTPMSC2)—Offset 494h" on page 2103	00000000h
49C–49Fh	4	"Port X Hardware LPM Control Register (PORTHLPMC2)—Offset 49Ch" on page 2104	00000000h



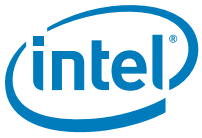
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4A0–4A3h	4	"Port Status and Control USB2 (PORTSC3)—Offset 4A0h" on page 2105	000002A0h
4A4–4A7h	4	"Port Power Management Status and Control USB2 (PORTPMSC3)—Offset 4A4h" on page 2107	00000000h
4AC–4AFh	4	"Port X Hardware LPM Control Register (PORTHLPMC3)—Offset 4ACh" on page 2108	00000000h
4B0–4B3h	4	"Port Status and Control USB2 (PORTSC4)—Offset 4B0h" on page 2109	000002A0h
4B4–4B7h	4	"Port Power Management Status and Control USB2 (PORTPMSC4)—Offset 4B4h" on page 2111	00000000h
4BC–4BFh	4	"Port X Hardware LPM Control Register (PORTHLPMC4)—Offset 4BCh" on page 2112	00000000h
4C0–4C3h	4	"Port Status and Control USB2 (PORTSC5)—Offset 4C0h" on page 2113	000002A0h
4C4–4C7h	4	"Port Power Management Status and Control USB2 (PORTPMSC5)—Offset 4C4h" on page 2115	00000000h
4CC–4CFh	4	"Port X Hardware LPM Control Register (PORTHLPMC5)—Offset 4CCh" on page 2116	00000000h
4D0–4D3h	4	"Port Status and Control USB2 (PORTSC6)—Offset 4D0h" on page 2117	000002A0h
4D4–4D7h	4	"Port Power Management Status and Control USB2 (PORTPMSC6)—Offset 4D4h" on page 2119	00000000h
4DC–4DFh	4	"Port X Hardware LPM Control Register (PORTHLPMC6)—Offset 4DCh" on page 2120	00000000h
4E0–4E3h	4	"Port Status and Control USB2 (PORTSC7)—Offset 4E0h" on page 2121	000002A0h
4E4–4E7h	4	"Port Power Management Status and Control USB2 (PORTPMSC7)—Offset 4E4h" on page 2123	00000000h
4EC–4EFh	4	"Port X Hardware LPM Control Register (PORTHLPMC7)—Offset 4ECh" on page 2124	00000000h
4F0–4F3h	4	"Port Status and Control USB3 (PORTSC8)—Offset 4F0h" on page 2125	000002A0h
4F4–4F7h	4	"Port Power Management Status and Control USB3 (PORTPMSC8)—Offset 4F4h" on page 2127	00000000h
4F8–4FBh	4	"USB3 Port Link Info (PORTLI8)—Offset 4F8h" on page 2128	00000000h
500–503h	4	"Port Status and Control USB3 (PORTSC9)—Offset 500h" on page 2128	000002A0h
504–507h	4	"Port Power Management Status and Control USB3 (PORTPMSC9)—Offset 504h" on page 2130	00000000h
508–50Bh	4	"USB3 Port Link Info (PORTLI9)—Offset 508h" on page 2131	00000000h
510–513h	4	"Port Status and Control USB3 (PORTSC10)—Offset 510h" on page 2131	000002A0h
514–517h	4	"Port Power Management Status and Control USB3 (PORTPMSC10)—Offset 514h" on page 2133	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
518–51Bh	4	"USB3 Port Link Info (PORTLI10)—Offset 518h" on page 2134	00000000h
520–523h	4	"Port Status and Control USB3 (PORTSC11)—Offset 520h" on page 2134	000002A0h
524–527h	4	"Port Power Management Status and Control USB3 (PORTPMSC11)—Offset 524h" on page 2137	00000000h
528–52Bh	4	"USB3 Port Link Info (PORTLI11)—Offset 528h" on page 2137	00000000h
530–533h	4	"Port Status and Control USB3 (PORTSC12)—Offset 530h" on page 2138	000002A0h
534–537h	4	"Port Power Management Status and Control USB3 (PORTPMSC12)—Offset 534h" on page 2140	00000000h
538–53Bh	4	"USB3 Port Link Info (PORTLI12)—Offset 538h" on page 2140	00000000h
540–543h	4	"Port Status and Control USB3 (PORTSC13)—Offset 540h" on page 2141	000002A0h
544–547h	4	"Port Power Management Status and Control USB3 (PORTPMSC13)—Offset 544h" on page 2143	00000000h
548–54Bh	4	"USB3 Port Link Info (PORTLI13)—Offset 548h" on page 2144	00000000h
2000–2003h	4	"Microframe Index (RTMFINDEX)—Offset 2000h" on page 2144	00000000h
2020–2023h	4	"Interrupter 1 Management (IMAN0)—Offset 2020h" on page 2144	00000000h
2024–2027h	4	"Interrupter 1 Moderation (IMOD0)—Offset 2024h" on page 2145	00000FA0h
2028–202Bh	4	"Event Ring Segment Table Size 1 (ERSTSZ0)—Offset 2028h" on page 2146	00000000h
2030–2033h	4	"Event Ring Segment Table Base Address Low 1 (ERSTBA_LO0)—Offset 2030h" on page 2146	00000000h
2034–2037h	4	"Event Ring Segment Table Base Address High 1 (ERSTBA_HI0)—Offset 2034h" on page 2147	00000000h
2038–203Bh	4	"Event Ring Dequeue Pointer Low 1 (ERDP_LO0)—Offset 2038h" on page 2147	00000000h
203C–203Fh	4	"Event Ring Dequeue Pointer High 1 (ERDP_HI0)—Offset 203Ch" on page 2148	00000000h
2040–2043h	4	"Interrupter 2 Management (IMAN1)—Offset 2040h" on page 2148	00000000h
2044–2047h	4	"Interrupter 2 Moderation (IMOD1)—Offset 2044h" on page 2149	00000FA0h
2048–204Bh	4	"Event Ring Segment Table Size 2 (ERSTSZ1)—Offset 2048h" on page 2149	00000000h
2050–2053h	4	"Event Ring Segment Table Base Address Low 2 (ERSTBA_LO1)—Offset 2050h" on page 2150	00000000h

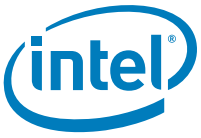


Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2054–2057h	4	"Event Ring Segment Table Base Address High 2 (ERSTBA_HI1)—Offset 2054h" on page 2150	00000000h
2058–205Bh	4	"Event Ring Dequeue Pointer Low 2 (ERDP_LO1)—Offset 2058h" on page 2151	00000000h
205C–205Fh	4	"Event Ring Dequeue Pointer High 2 (ERDP_HI1)—Offset 205Ch" on page 2151	00000000h
2060–2063h	4	"Interrupter 3 Management (IMAN2)—Offset 2060h" on page 2152	00000000h
2064–2067h	4	"Interrupter 3 Moderation (IMOD2)—Offset 2064h" on page 2152	00000FA0h
2068–206Bh	4	"Event Ring Segment Table Size 3 (ERSTSZ2)—Offset 2068h" on page 2153	00000000h
2070–2073h	4	"Event Ring Segment Table Base Address Low 3 (ERSTBA_LO2)—Offset 2070h" on page 2153	00000000h
2074–2077h	4	"Event Ring Segment Table Base Address High 3 (ERSTBA_HI2)—Offset 2074h" on page 2154	00000000h
2078–207Bh	4	"Event Ring Dequeue Pointer Low 3 (ERDP_LO2)—Offset 2078h" on page 2154	00000000h
207C–207Fh	4	"Event Ring Dequeue Pointer High 3 (ERDP_HI2)—Offset 207Ch" on page 2155	00000000h
2080–2083h	4	"Interrupter 4 Management (IMAN3)—Offset 2080h" on page 2155	00000000h
2084–2087h	4	"Interrupter 4 Moderation (IMOD3)—Offset 2084h" on page 2156	00000FA0h
2088–208Bh	4	"Event Ring Segment Table Size 4 (ERSTSZ3)—Offset 2088h" on page 2157	00000000h
2090–2093h	4	"Event Ring Segment Table Base Address Low 4 (ERSTBA_LO3)—Offset 2090h" on page 2157	00000000h
2094–2097h	4	"Event Ring Segment Table Base Address High 4 (ERSTBA_HI3)—Offset 2094h" on page 2158	00000000h
2098–209Bh	4	"Event Ring Dequeue Pointer Low 4 (ERDP_LO3)—Offset 2098h" on page 2158	00000000h
209C–209Fh	4	"Event Ring Dequeue Pointer High 4 (ERDP_HI3)—Offset 209Ch" on page 2159	00000000h
20A0–20A3h	4	"Interrupter 5 Management (IMAN4)—Offset 20A0h" on page 2159	00000000h
20A4–20A7h	4	"Interrupter 5 Moderation (IMOD4)—Offset 20A4h" on page 2160	00000FA0h
20A8–20ABh	4	"Event Ring Segment Table Size 5 (ERSTSZ4)—Offset 20A8h" on page 2160	00000000h
20B0–20B3h	4	"Event Ring Segment Table Base Address Low 5 (ERSTBA_LO4)—Offset 20B0h" on page 2161	00000000h
20B4–20B7h	4	"Event Ring Segment Table Base Address High 5 (ERSTBA_HI4)—Offset 20B4h" on page 2161	00000000h

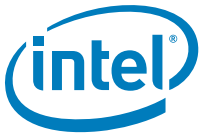
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
20B8–20BBh	4	"Event Ring Dequeue Pointer Low 5 (ERDP_LO4)—Offset 20B8h" on page 2162	00000000h
20BC–20BFh	4	"Event Ring Dequeue Pointer High 5 (ERDP_HI4)—Offset 20BCh" on page 2162	00000000h
20C0–20C3h	4	"Interrupter 6 Management (IMAN5)—Offset 20C0h" on page 2163	00000000h
20C4–20C7h	4	"Interrupter 6 Moderation (IMOD5)—Offset 20C4h" on page 2163	00000FA0h
20C8–20CBh	4	"Event Ring Segment Table Size 6 (ERSTSZ5)—Offset 20C8h" on page 2164	00000000h
20D0–20D3h	4	"Event Ring Segment Table Base Address Low 6 (ERSTBA_LO5)—Offset 20D0h" on page 2164	00000000h
20D4–20D7h	4	"Event Ring Segment Table Base Address High 6 (ERSTBA_HI5)—Offset 20D4h" on page 2165	00000000h
20D8–20DBh	4	"Event Ring Dequeue Pointer Low 6 (ERDP_LO5)—Offset 20D8h" on page 2165	00000000h
20DC–20DFh	4	"Event Ring Dequeue Pointer High 6 (ERDP_HI5)—Offset 20DCh" on page 2166	00000000h
20E0–20E3h	4	"Interrupter 7 Management (IMAN6)—Offset 20E0h" on page 2166	00000000h
20E4–20E7h	4	"Interrupter 7 Moderation (IMOD6)—Offset 20E4h" on page 2167	00000FA0h
20E8–20EBh	4	"Event Ring Segment Table Size 7 (ERSTSZ6)—Offset 20E8h" on page 2168	00000000h
20F0–20F3h	4	"Event Ring Segment Table Base Address Low 7 (ERSTBA_LO6)—Offset 20F0h" on page 2168	00000000h
20F4–20F7h	4	"Event Ring Segment Table Base Address High 7 (ERSTBA_HI6)—Offset 20F4h" on page 2169	00000000h
20F8–20FBh	4	"Event Ring Dequeue Pointer Low 7 (ERDP_LO6)—Offset 20F8h" on page 2169	00000000h
20FC–20FFh	4	"Event Ring Dequeue Pointer High 7 (ERDP_HI6)—Offset 20FCh" on page 2170	00000000h
2100–2103h	4	"Interrupter 8 Management (IMAN7)—Offset 2100h" on page 2170	00000000h
2104–2107h	4	"Interrupter 8 Moderation (IMOD7)—Offset 2104h" on page 2171	00000FA0h
2108–210Bh	4	"Event Ring Segment Table Size 8 (ERSTSZ7)—Offset 2108h" on page 2171	00000000h
2110–2113h	4	"Event Ring Segment Table Base Address Low 8 (ERSTBA_LO7)—Offset 2110h" on page 2172	00000000h
2114–2117h	4	"Event Ring Segment Table Base Address High 8 (ERSTBA_HI7)—Offset 2114h" on page 2172	00000000h
2118–211Bh	4	"Event Ring Dequeue Pointer Low 8 (ERDP_LO7)—Offset 2118h" on page 2173	00000000h



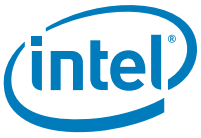
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
211C–211Fh	4	"Event Ring Dequeue Pointer High 8 (ERDP_HI7)—Offset 211Ch" on page 2173	00000000h
3000–3003h	4	"Door Bell 1 (DB0)—Offset 3000h" on page 2174	00000000h
3004–3007h	4	"Door Bell 2 (DB1)—Offset 3004h" on page 2174	00000000h
3008–300Bh	4	"Door Bell 3 (DB2)—Offset 3008h" on page 2175	00000000h
300C–300Fh	4	"Door Bell 4 (DB3)—Offset 300Ch" on page 2176	00000000h
3010–3013h	4	"Door Bell 5 (DB4)—Offset 3010h" on page 2176	00000000h
3014–3017h	4	"Door Bell 6 (DB5)—Offset 3014h" on page 2177	00000000h
3018–301Bh	4	"Door Bell 7 (DB6)—Offset 3018h" on page 2178	00000000h
301C–301Fh	4	"Door Bell 8 (DB7)—Offset 301Ch" on page 2178	00000000h
3020–3023h	4	"Door Bell 9 (DB8)—Offset 3020h" on page 2179	00000000h
3024–3027h	4	"Door Bell 10 (DB9)—Offset 3024h" on page 2179	00000000h
3028–302Bh	4	"Door Bell 11 (DB10)—Offset 3028h" on page 2180	00000000h
302C–302Fh	4	"Door Bell 12 (DB11)—Offset 302Ch" on page 2181	00000000h
3030–3033h	4	"Door Bell 13 (DB12)—Offset 3030h" on page 2181	00000000h
3034–3037h	4	"Door Bell 14 (DB13)—Offset 3034h" on page 2182	00000000h
3038–303Bh	4	"Door Bell 15 (DB14)—Offset 3038h" on page 2182	00000000h
303C–303Fh	4	"Door Bell 16 (DB15)—Offset 303Ch" on page 2183	00000000h
3040–3043h	4	"Door Bell 17 (DB16)—Offset 3040h" on page 2184	00000000h
3044–3047h	4	"Door Bell 18 (DB17)—Offset 3044h" on page 2184	00000000h
3048–304Bh	4	"Door Bell 19 (DB18)—Offset 3048h" on page 2185	00000000h
304C–304Fh	4	"Door Bell 20 (DB19)—Offset 304Ch" on page 2185	00000000h
3050–3053h	4	"Door Bell 21 (DB20)—Offset 3050h" on page 2186	00000000h
3054–3057h	4	"Door Bell 22 (DB21)—Offset 3054h" on page 2187	00000000h
3058–305Bh	4	"Door Bell 23 (DB22)—Offset 3058h" on page 2187	00000000h
305C–305Fh	4	"Door Bell 24 (DB23)—Offset 305Ch" on page 2188	00000000h
3060–3063h	4	"Door Bell 25 (DB24)—Offset 3060h" on page 2188	00000000h
3064–3067h	4	"Door Bell 26 (DB25)—Offset 3064h" on page 2189	00000000h
3068–306Bh	4	"Door Bell 27 (DB26)—Offset 3068h" on page 2190	00000000h
306C–306Fh	4	"Door Bell 28 (DB27)—Offset 306Ch" on page 2190	00000000h
3070–3073h	4	"Door Bell 29 (DB28)—Offset 3070h" on page 2191	00000000h
3074–3077h	4	"Door Bell 30 (DB29)—Offset 3074h" on page 2191	00000000h
3078–307Bh	4	"Door Bell 31 (DB30)—Offset 3078h" on page 2192	00000000h
307C–307Fh	4	"Door Bell 32 (DB31)—Offset 307Ch" on page 2193	00000000h
3080–3083h	4	"Door Bell 32 (DB32)—Offset 3080h" on page 2193	00000000h
8000–8003h	4	"XECP_SUPP_USB2_0—Offset 8000h" on page 2194	02000802h
8004–8007h	4	"XECP_SUPP_USB2_1—Offset 8004h" on page 2194	20425355h



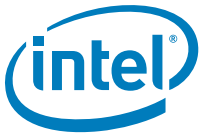
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8008–800Bh	4	"XECP_SUPP_USB2_2—Offset 8008h" on page 2195	30190701h
8010–8013h	4	"XECP_SUPP_USB2_3 (Full Speed) (XECP_SUPP_USB2_3)—Offset 8010h" on page 2196	000C0021h
8014–8017h	4	"XECP_SUPP_USB2_4 (Low Speed) (XECP_SUPP_USB2_4)—Offset 8014h" on page 2197	05DC0012h
8018–801Bh	4	"XECP_SUPP_USB2_5 (High Speed) (XECP_SUPP_USB2_5)—Offset 8018h" on page 2198	01E00023h
8020–8023h	4	"XECP_SUPP_USB3_0—Offset 8020h" on page 2199	03001402h
8024–8027h	4	"XECP_SUPP_USB3_1—Offset 8024h" on page 2199	20425355h
8028–802Bh	4	"XECP_SUPP_USB3_2—Offset 8028h" on page 2200	30000608h
8030–8033h	4	"XECP_SUPP_USB3_3—Offset 8030h" on page 2200	04E00121h
8034–8037h	4	"XECP_SUPP_USB3_4—Offset 8034h" on page 2201	09C00122h
8038–803Bh	4	"XECP_SUPP_USB3_5—Offset 8038h" on page 2202	13800123h
803C–803Fh	4	"XECP_SUPP_USB3_6—Offset 803Ch" on page 2203	00050134h
8040–8043h	4	"XECP_SUPP_USB3_7—Offset 8040h" on page 2203	05B10125h
8044–8047h	4	"XECP_SUPP_USB3_8—Offset 8044h" on page 2204	0B630126h
8048–804Bh	4	"XECP_SUPP_USB3_9—Offset 8048h" on page 2205	16C60127h
8070–8073h	4	"Host Controller Capability (HOST_CTRL_CAP_REG)—Offset 8070h" on page 2206	004DFFC0h
8078–807Bh	4	"Override EP Flow Control (HOST_CLR_MASK_REG)—Offset 8078h" on page 2207	00000000h
807C–807Fh	4	"Clear Active IN EP ID Control (HOST_CLR_IN_EP_VALID_REG)—Offset 807Ch" on page 2208	00000000h
8080–8083h	4	"Clear Poll Mask Control (HOST_CLR_PMASK_REG)—Offset 8080h" on page 2208	00000000h
8094–8097h	4	"Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h" on page 2209	00008100h
80A0–80A3h	4	"Global Port Control (HOST_CTRL_PORT_CTRL)—Offset 80A0h" on page 2210	0000380Fh
80A4–80A7h	4	"Power Management Control (PMCTRL_REG)—Offset 80A4h" on page 2211	0001FF90h
80A8–80ABh	4	"PGCB Control (PGCBCTRL_REG)—Offset 80A8h" on page 2214	00315555h
80AC–80AFh	4	"D0I3 Control (DOI3CTRL_REG)—Offset 80ACh" on page 2217	00000008h
80B0–80B3h	4	"HOST_CTRL_MISC_REG—Offset 80B0h" on page 2218	0001037Fh
80B4–80B7h	4	"HOST_CTRL_MISC_REG2—Offset 80B4h" on page 2220	00000000h
80B8–80BBh	4	"SSPE_REG—Offset 80B8h" on page 2221	00000000h
80BC–80BFh	4	"reg_SSPITPE_type (SSPITPE)—Offset 80BCh" on page 2222	0000003Fh



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
80C0–80C3h	4	"AUX Reset Control (AUX_CTRL_REG)—Offset 80C0h" on page 2222	015FC0F0h
80C4–80C7h	4	"Super Speed Bandwidth Overload (HOST_BW_OV_SS_REG)—Offset 80C4h" on page 2226	004A4008h
80C8–80CBh	4	"High Speed TT Bandwidth Overload (HOST_BW_OV_HS_REG)—Offset 80C8h" on page 2227	0001A01Fh
80CC–80CFh	4	"Bandwidth Overload Full Low Speed (HOST_BW_OV_FS_LS_REG)—Offset 80CCh" on page 2227	00014080h
80D0–80D3h	4	"System Bandwidth Overload (HOST_BW_OV_SYS_REG)—Offset 80D0h" on page 2228	00032010h
80D4–80D7h	4	"Scheduler Async Delay (HOST_CTRL_SCH_ASYNC_DELAY_REG)—Offset 80D4h" on page 2229	00000000h
80D8–80DBh	4	"DEVICE MODE CONTROL REG 0 (DUAL_ROLE_CFG_REG0)—Offset 80D8h" on page 2230	00000800h
80DC–80DFh	4	"DEVICE MODE CONTROL REG 1 (DUAL_ROLE_CFG_REG1)—Offset 80DCh" on page 2233	10000000h
80E0–80E3h	4	"AUX Power Management Control (AUX_CTRL_REG1)—Offset 80E0h" on page 2234	808DBCA0h
80E4–80E7h	4	"Battery Charge (BATTERY_CHARGE_REG)—Offset 80E4h" on page 2237	00000000h
80E8–80EBh	4	"Port Watermark (HOST_CTRL_WATERMARK_REG)—Offset 80E8h" on page 2238	00800080h
80EC–80EFh	4	"SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)—Offset 80ECh" on page 2239	18010000h
80F0–80F3h	4	"USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)—Offset 80F0h" on page 2241	310803A0h
80F4–80F7h	4	"USB2 Port Link Control 2 (USB2_LINK_MGR_CTRL_REG2)—Offset 80F4h" on page 2244	80C40620h
80F8–80FBh	4	"USB2 Port Link Control 3 (USB2_LINK_MGR_CTRL_REG3)—Offset 80F8h" on page 2244	F865EB6Bh
80FC–80FFh	4	"USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)—Offset 80FCh" on page 2245	00008003h
8100–8103h	4	"Bandwidth Calc Control (HOST_CTRL_BW_CTRL_REG)—Offset 8100h" on page 2246	00008008h
8108–810Bh	4	"Host Interface Control (HOST_IF_CTRL_REG)—Offset 8108h" on page 2247	00000001h
810C–810Fh	4	"Bandwidth Overload Burst (HOST_BW_OV_BURST_REG)—Offset 810Ch" on page 2247	00008020h
8128–812Fh	8	"USB Max Bandwidth Control 4 (HOST_CTRL_BW_MAX_REG)—Offset 8128h" on page 2248	0F42528505647F42h
8130–8133h	4	"USB2 Linestate Debug (LINESTATE_DEBUG_REG)—Offset 8130h" on page 2249	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8134–813Bh	8	"USB2 Protocol Gap Timer (USB2_PROTOCOL_GAP_TIMER_REG)—Offset 8134h" on page 2250	000C3C640C05140Ch
813C–813Fh	4	"USB2 Protocol Bus Timeout Timer (USB2_PROTOCOL_BTO_TIMER_REG)—Offset 813Ch" on page 2251	8D4258B8h
8140–8143h	4	"Power Scheduler Control-0 (PWR_SCHED_CTRL0)—Offset 8140h" on page 2252	0A019132h
8144–8147h	4	"Power Scheduler Control-2 (PWR_SCHED_CTRL2)—Offset 8144h" on page 2253	0000033Fh
8154–8157h	4	"AUX Power Management Control (AUX_CTRL_REG2)—Offset 8154h" on page 2254	81390206h
8164–8167h	4	"USB2 PHY Power Management Control (USB2_PHY_PMC)—Offset 8164h" on page 2258	000000FCh
8168–816Bh	4	"USB2 Phy Power Management Control 2 (USB2_PHY_PMC2)—Offset 8168h" on page 2259	000282EEh
816C–816Fh	4	"xHCI Aux Clock Control Register (XHCI_AUX_CCR)—Offset 816Ch" on page 2260	00000400h
8170–8173h	4	"USB LPM Parameters (USB_LPM_PARAM)—Offset 8170h" on page 2263	00090032h
8174–8177h	4	"xHC Latency Tolerance Parameters - LTV Control (XLTP_LTV1)—Offset 8174h" on page 2264	0040047Dh
8178–817Bh	4	"xHC Latency Tolerance Parameters LTV Control 2 (XLTP_LTV2)—Offset 8178h" on page 2265	000017FFh
817C–817Fh	4	"xHC Latency Tolerance Parameters - High Idle Time Control (XLTP_HITC)—Offset 817Ch" on page 2266	00000000h
8180–8183h	4	"xHC Latency Tolerance Parameters - Medium Idle Time Control (XLTP_MITC)—Offset 8180h" on page 2267	00000000h
8184–8187h	4	"xHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)—Offset 8184h" on page 2268	00000000h
8188–818Bh	4	"HOST_CTRL_BW_MAX3_REG—Offset 8188h" on page 2268	00F42F42h
8198–819Bh	4	"PDDIS_REG—Offset 8198h" on page 2269	00000000h
819C–819Fh	4	"THRM_HOST_CTRL_REG—Offset 819Ch" on page 2270	00000000h
81A0–81A3h	4	"LFPS_PM_CTRL_REG—Offset 81A0h" on page 2272	00000000h
81A4–81A7h	4	"U2PDM—Offset 81A4h" on page 2272	00000000h
81A8–81ABh	4	"U2PCM—Offset 81A8h" on page 2273	00000000h
81AC–81AFh	4	"U3PDM—Offset 81ACh" on page 2273	00000000h
81B0–81B3h	4	"U3PCM—Offset 81B0h" on page 2274	00000000h
81B8–81BBh	4	"LFPSONCOUNT_REG—Offset 81B8h" on page 2274	000020C8h
81BC–81BFh	4	"reg_D0i2_CTRL_REG_type (D0i2_CTRL_REG)—Offset 81BCh" on page 2275	084204B0h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
81C0–81C3h	4	"reg_D0i2_SCH_ALARM_CTRL_REG_type (D0i2_SCH_ALARM_CTRL_REG)—Offset 81C0h" on page 2277	00000000h
81C4–81C7h	4	"reg_USB2PMCTRL_REG_type (USB2PMCTRL_REG)—Offset 81C4h" on page 2278	00000000h
8410–8413h	4	"FUS1_REG—Offset 8410h" on page 2280	00000000h
8430–8433h	4	"DFT_REG1—Offset 8430h" on page 2282	00000000h
8434–8437h	4	"DFT_REG2—Offset 8434h" on page 2283	00000000h

7.2.1 Capability Registers Length (CAPLENGTH)—Offset 0h

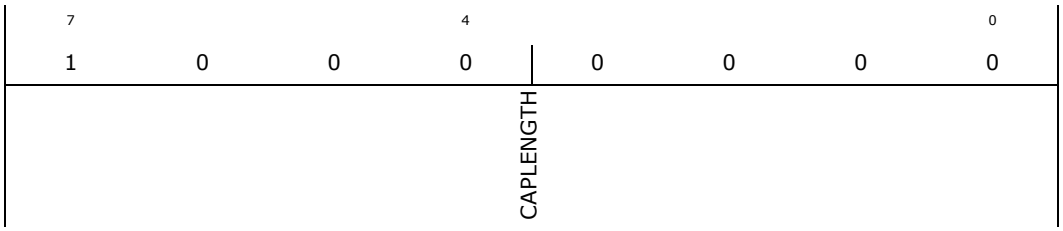
This register is modified and maintained by BIOS

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [MBAR] + 0h

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x80 RW/L	**Capability Registers Length (CAPLENGTH):** Reserved. **Power Well:** Core

7.2.2 Host Controller Interface Version Number (HCIVERSION)—Offset 2h

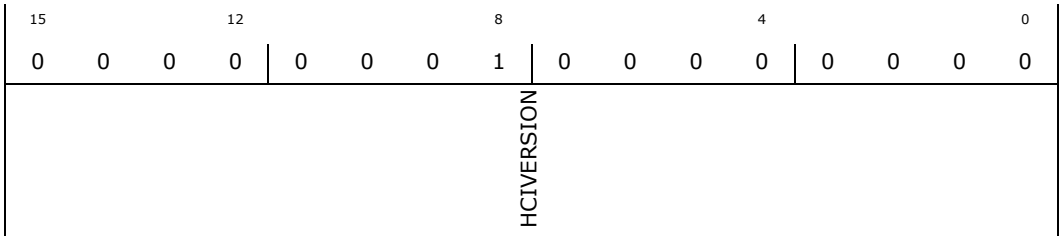
This register is modified and maintained by BIOS

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [MBAR] + 2h

Default: 0100h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0x100 RO	**Host Controller Interface Version Number (HCIVERSION):** Reserved. **Power Well:** Core

7.2.3 Structural Parameters 1 (HCSPARAMS1)—Offset 4h

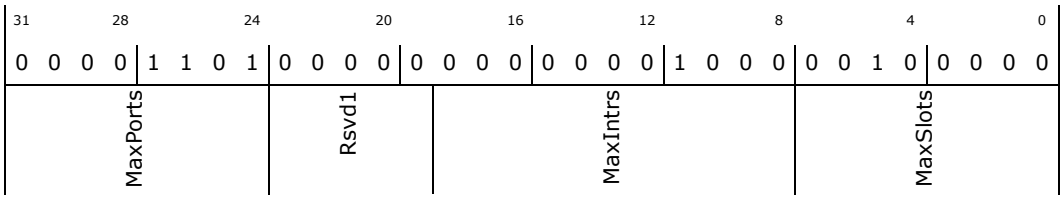
This register is modified and maintained by BIOS

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4h

Default: 0D000820h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0xd RO	**Number of Ports (MaxPorts):** Reserved. **Power Well:** Core
23:19	0x0 RW/L	**Rsvd1:** Reserved. **Power Well:** Core
18:8	0x8 RW/L	**Number of Interrupters (MaxIntrs):** Reserved. **Power Well:** Core
7:0	0x20 RW/L	**Number of Device Slots (MaxSlots):** Reserved. **Power Well:** Core

7.2.4 Structural Parameters 2 (HCSPARAMS2)—Offset 8h

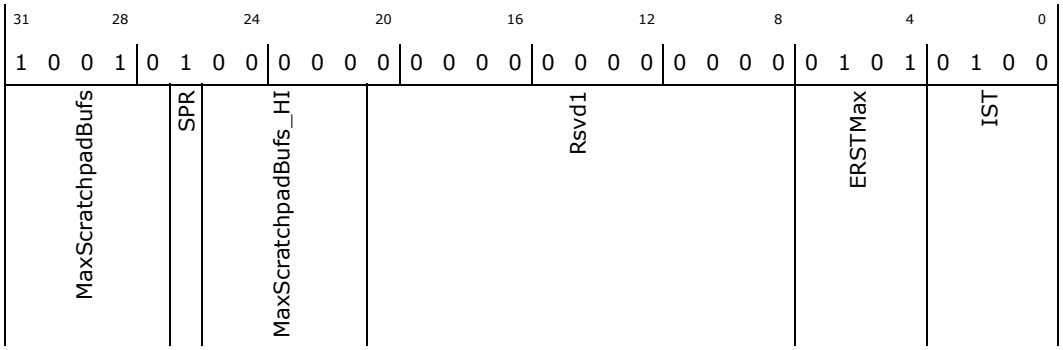
This register is modified and maintained by BIOS

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8h

Default: 94000054h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x12 RW/L	**Max Scratchpad Buffers LO (MaxScratchpadBufs):** Reserved. **Power Well:** Core
26	0x1 RW/L	**Scratchpad Restore (SPR):** Reserved. **Power Well:** Core
25:21	0x0 RW/L	**Max Scratchpad Buffers HI (MaxScratchpadBufs_HI):** Reserved. **Power Well:** Core
20:8	0x0 RW/L	**Rsvd1:** Reserved. **Power Well:** Core
7:4	0x5 RW/L	**Event Ring Segment Table Max (ERSTMax):** Reserved. **Power Well:** Core
3:0	0x4 RW/L	**Isochronous Scheduling Threshold (IST):** Reserved. **Power Well:** Core

7.2.5 Structural Parameters 3 (HCSPARAMS3)—Offset Ch

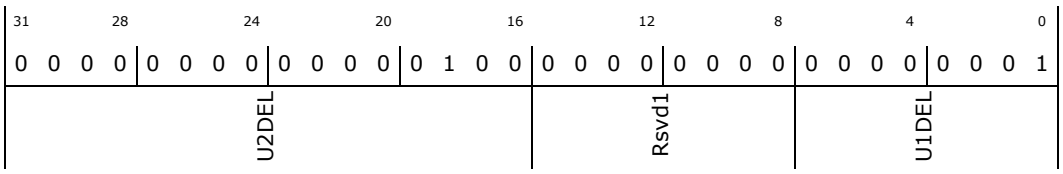
This register is modified and maintained by BIOS

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + Ch

Default: 00040001h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x4 RW/L	**U2 Device Exit Latency (U2DEL):** Reserved. **Power Well:** Core
15:8	0x0 RW/L	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x1 RW/L	**U1 Device Exit Latency (U1DEL):** Reserved. **Power Well:** Core

7.2.6 Capability Parameters (HCCPARAMS)—Offset 10h

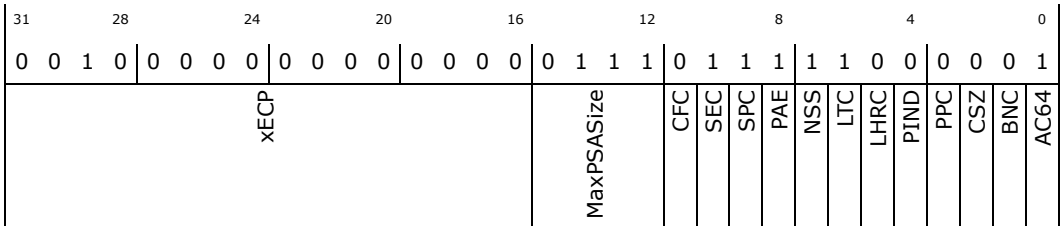
This register is modified and maintained by BIOS

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 10h

Default: 200077C1h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x2000 RW/L	**xHCI Extended Capabilities Pointer (xECP):** Reserved. **Power Well:** Core
15:12	0x7 RW/L	**Maximum Primary Stream Array Size (MaxPSASize):** Reserved. **Power Well:** Core
11	0x0 RW/L	**Contiguous Frame ID Capability (CFC):** Reserved. **Power Well:** Core
10	0x1 RW/L	**Stopped EDLTA Capabilty (SEC):** Reserved. **Power Well:** Core
9	0x1 RW/L	**Stopped - Short Packet Capability (SPC):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
8	0x1 RW/L	**Parst All Event Data (PAE):** Reserved. **Power Well:** Core
7	0x1 RW/L	**No Secondary SID Support (NSS):** Reserved. **Power Well:** Core
6	0x1 RW/L	**Latency Tolerance Messaging Capability (LTC):** Reserved. **Power Well:** Core
5	0x0 RW/L	**Light HC Reset Capability (LHRC):** Reserved. **Power Well:** Core
4	0x0 RW/L	**Port Indicators (PIND):** Reserved. **Power Well:** Core
3	0x0 RW/L	**Port Power Control (PPC):** Reserved. **Power Well:** Core
2	0x0 RW/L	**Context Size (CSZ):** Reserved. **Power Well:** Core
1	0x0 RW/L	**BW Negotiation Capability (BNC):** Reserved. **Power Well:** Core
0	0x1 RW/L	**64-bit Addressing Capability (AC64):** Reserved. **Power Well:** Core

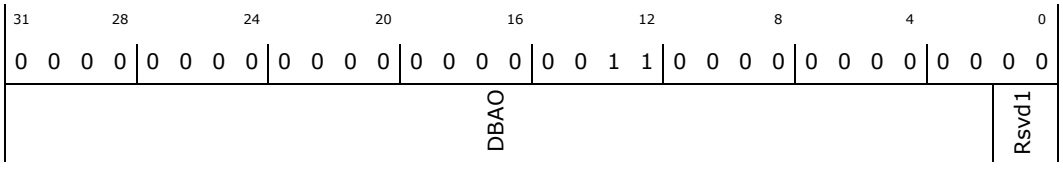
7.2.7 Doorbell Offset (DBOFF)—Offset 14h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 14h

Default: 00003000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0xc00 RO	**Doorbell Array Offset (DBAO):** Reserved. **Power Well:** Core
1:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

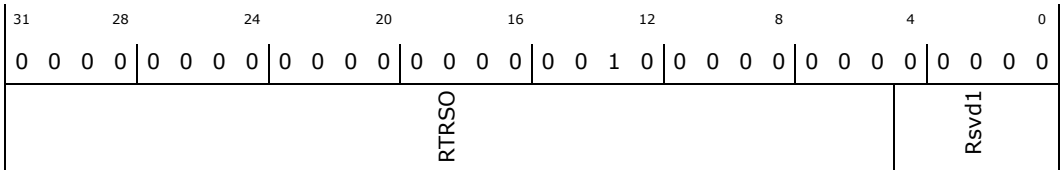
7.2.8 Runtime Register Space Offset (RTSOFF)—Offset 18h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 18h

Default: 00002000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x100 RO	**Runtime Register Space Offset (RTRSO):** Reserved. **Power Well:** Core
4:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

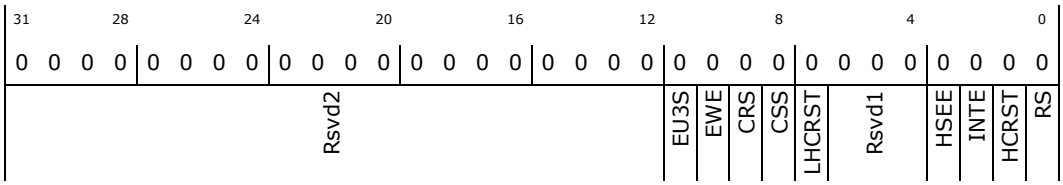
7.2.9 USB Command (USBCMD)—Offset 80h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
11	0x0 RW	**Enable U3 MFINDEX Stop (EU3S):** Reserved. **Power Well:** Core
10	0x0 RW	**Enable Wrap Event (EWE):** Reserved. **Power Well:** Core
9	0x0 RW	**Controller Restore State (CRS):** Reserved. **Power Well:** Core
8	0x0 RW	**Controller Save State (CSS):** Reserved. **Power Well:** Core
7	0x0 RW	**Light Host Controller Reset (LHCRST):** Reserved. **Power Well:** Core
6:4	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
3	0x0 RW	**Host System Error Enable (HSEE):** Reserved. **Power Well:** Core
2	0x0 RW	**Interrupter Enable (INTE):** Reserved. **Power Well:** Core
1	0x0 RW	**Host Controller Reset (HCRST):** Reserved. **Power Well:** Core
0	0x0 RW	**Run/Stop (RS):** Reserved. **Power Well:** Core

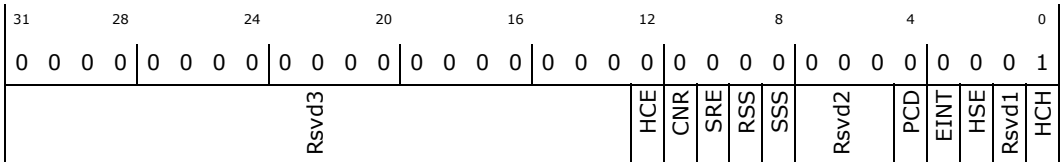
7.2.10 USB Status (USBSTS)—Offset 84h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 84h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**Rsvd3:** Reserved. **Power Well:** Core
12	0x0 RO	**Host Controller Error (HCE):** This bit is not preset in HC, this is deviation from XHCI 1.0 spec. **Power Well:** Core
11	0x0 RO	**Controller Not Ready (CNR):** This is deviation from XHCI 1.0 spec. **Power Well:** Core
10	0x0 RW/C	**Save/Restore Error (SRE):** Reserved. **Power Well:** Core
9	0x0 RO	**Restore State Status (RSS):** Reserved. **Power Well:** Core
8	0x0 RO	**Save State Status (SSS):** Reserved. **Power Well:** Core
7:5	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
4	0x0 RW/C	**Port Change Detect (PCD):** Reserved. **Power Well:** Core
3	0x0 RW/C	**Event Interrupt (EINT):** Reserved. **Power Well:** Core
2	0x0 RW/C	**Host System Error (HSE):** Reserved. **Power Well:** Core
1	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
0	0x1 RO	**HCHalted (HCH):** Reserved. **Power Well:** Core

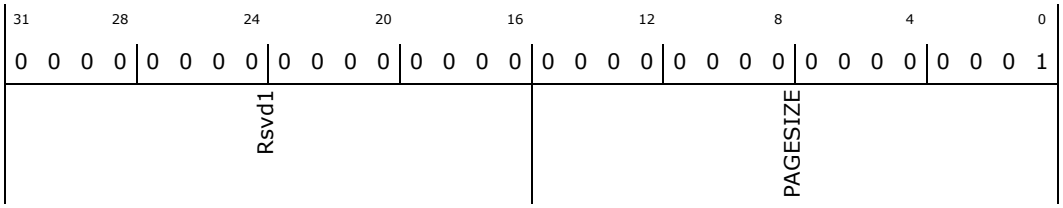
7.2.11 Page Size (PAGESIZE)—Offset 88h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 88h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x1 RO	**Page Size (PAGESIZE):** Reserved. **Power Well:** Core

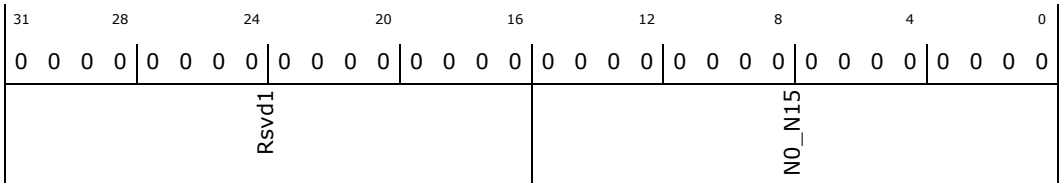
7.2.12 Device Notification Control (DNCTRL)—Offset 94h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 94h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RW	**Notification Enable (N0_N15):** Reserved. **Power Well:** Core

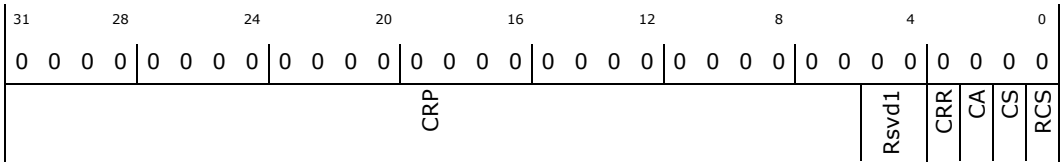
7.2.13 Command Ring Low (CRCR_LO)—Offset 98h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 98h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Command Ring Pointer (CRP):** Reserved. **Power Well:** Core
5:4	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
3	0x0 RO	**Command Ring Running (CRR):** Reserved. **Power Well:** Core
2	0x0 RW/1S	**Command Abort (CA):** Reserved. **Power Well:** Core
1	0x0 RW/1S	**Command Stop (CS):** Reserved. **Power Well:** Core
0	0x0 RW	**Ring Cycle State (RCS):** Reserved. **Power Well:** Core

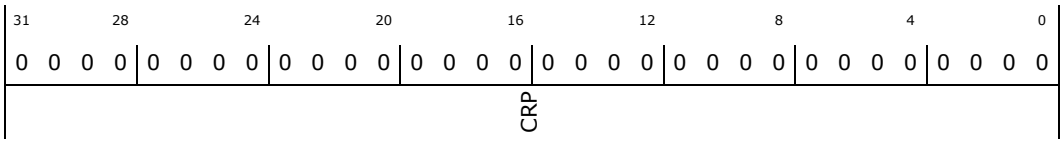
7.2.14 Command Ring High (CRCR_HI)—Offset 9Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 9Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Command Ring Pointer (CRP):** Reserved. **Power Well:** Core

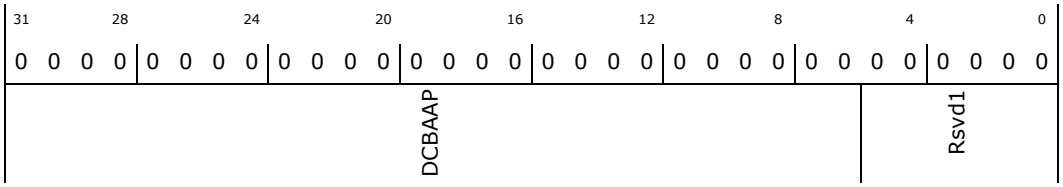
7.2.15 Device Context Base Address Array Pointer Low (DCBAAP_LO)—Offset B0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Device Context Base Address Array Pointer (DCBAAP):** Reserved. **Power Well:** Core
5:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

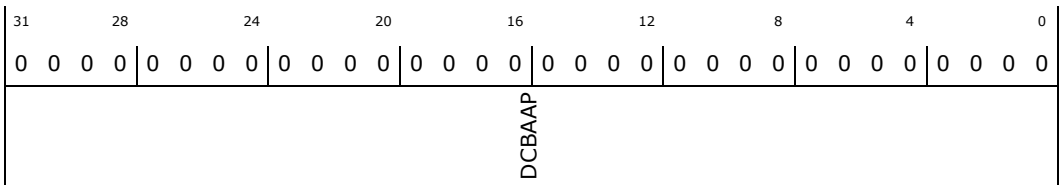
7.2.16 Device Context Base Address Array Pointer High (DCBAAP_HI)—Offset B4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + B4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Device Context Base Address Array Pointer (DCBAAP):** Reserved. **Power Well:** Core

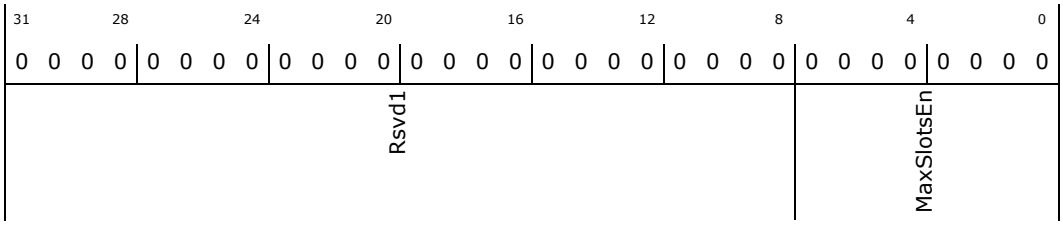
7.2.17 Configure (CONFIG)—Offset B8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**Max Device Slots Enabled (MaxSlotsEn):** Reserved. **Power Well:** Core

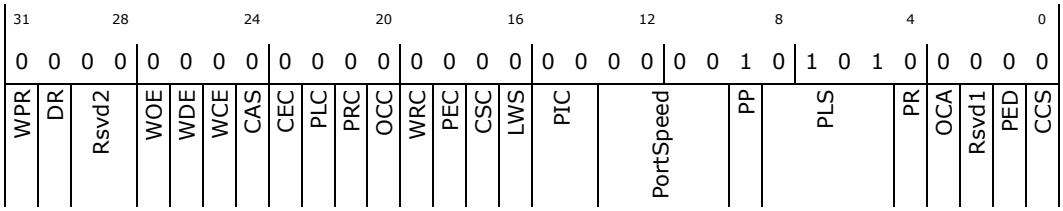
7.2.18 Port Status and Control USB2 (PORTSC1)—Offset 480h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 480h

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

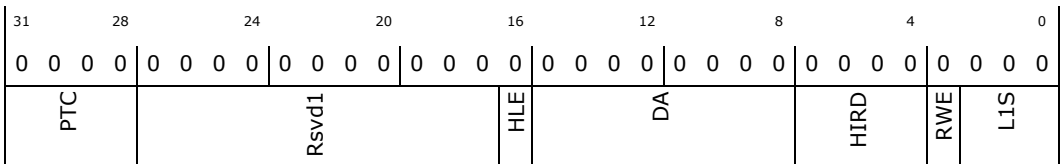
7.2.19 Port Power Management Status and Control USB2 (PORTPMSC1)—Offset 484h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 484h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS
27:17	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0x0 RW	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	0x0 RW	**Device Address (DA):** Note: This register is sticky. **Power Well:** SUS
7:4	0x0 RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0x0 RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0x0 RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

7.2.20 Port X Hardware LPM Control Register (PORTHLPMC1)—Offset 48Ch

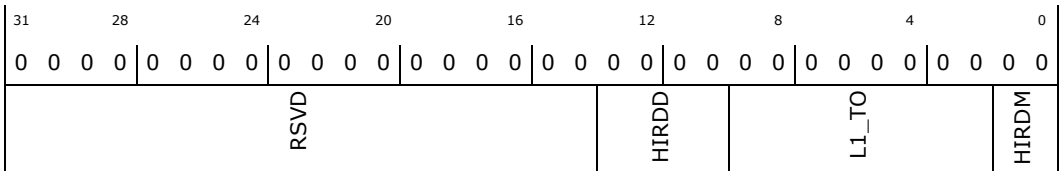
There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters necessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 48Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
13:10	0x0 RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS
9:2	0x0 RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0x0 RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky. **Power Well:** SUS

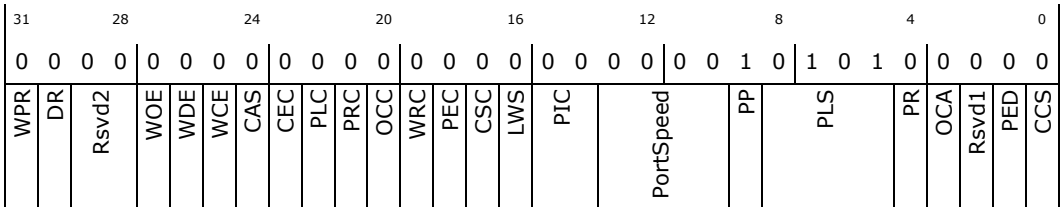
7.2.21 Port Status and Control USB2 (PORTSC2)—Offset 490h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 490h

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

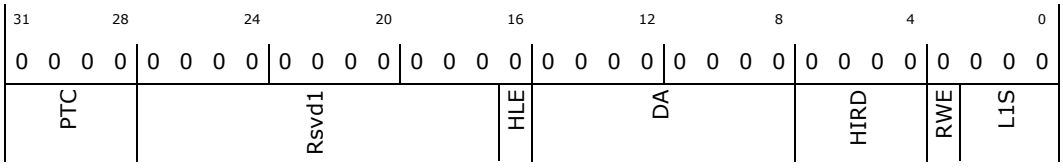
7.2.22 Port Power Management Status and Control USB2 (PORTPMSC2)—Offset 494h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 494h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
27:17	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0x0 RW	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	0x0 RW	**Device Address (DA):** Note: This register is sticky. **Power Well:** SUS
7:4	0x0 RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0x0 RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0x0 RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

7.2.23 Port X Hardware LPM Control Register (PORTHLPMC2)—Offset 49Ch

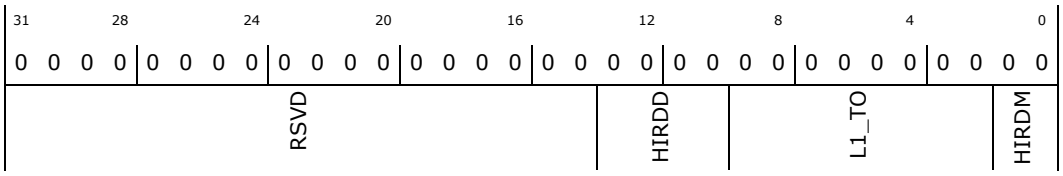
There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 49Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
13:10	0x0 RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS
9:2	0x0 RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0x0 RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky. **Power Well:** SUS

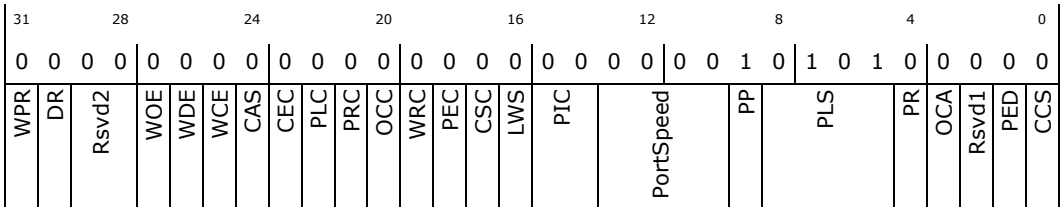
7.2.24 Port Status and Control USB2 (PORTSC3)—Offset 4A0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4A0h

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

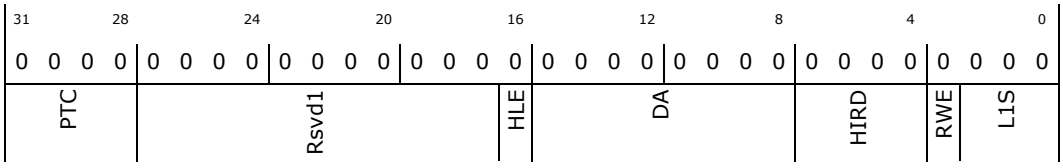
7.2.25 Port Power Management Status and Control USB2 (PORTPMSC3)—Offset 4A4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
27:17	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0x0 RW	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	0x0 RW	**Device Address (DA):** Note: This register is sticky. **Power Well:** SUS
7:4	0x0 RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0x0 RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0x0 RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

7.2.26 Port X Hardware LPM Control Register (PORTHLPMC3)—Offset 4ACh

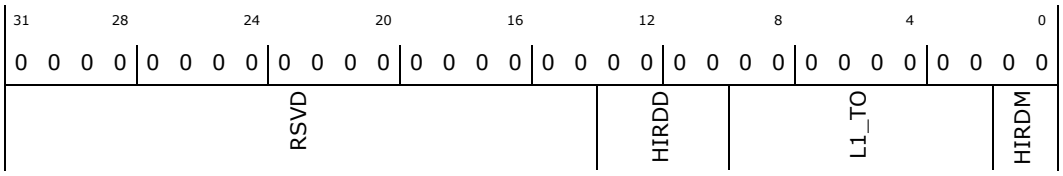
There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
13:10	0x0 RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS
9:2	0x0 RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0x0 RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky. **Power Well:** SUS

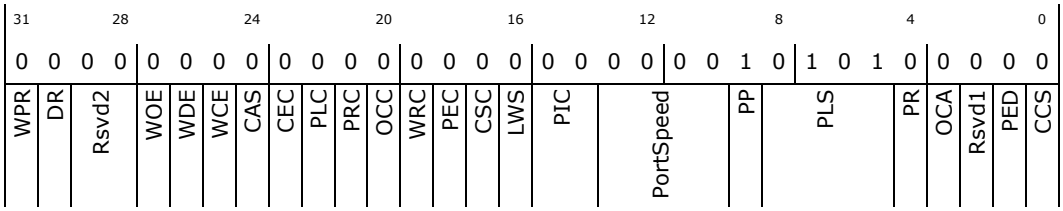
7.2.27 Port Status and Control USB2 (PORTSC4)—Offset 4B0h

Access Method

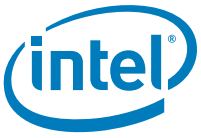
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4B0h

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

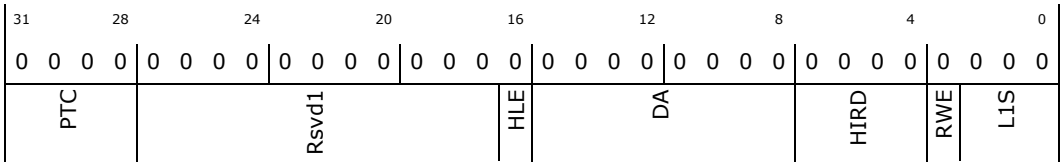
7.2.28 Port Power Management Status and Control USB2 (PORTPMSC4)—Offset 4B4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4B4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
27:17	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0x0 RW	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	0x0 RW	**Device Address (DA):** Note: This register is sticky. **Power Well:** SUS
7:4	0x0 RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0x0 RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0x0 RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

7.2.29 Port X Hardware LPM Control Register (PORTHLPMC4)—Offset 4BCh

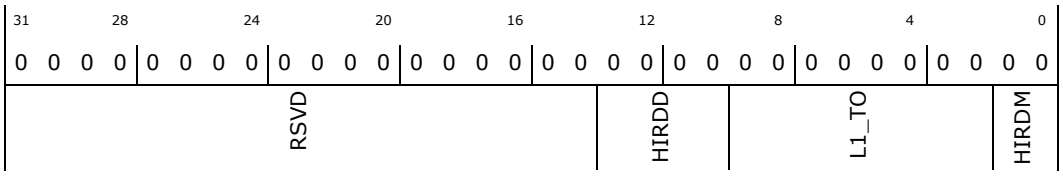
There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4BCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
13:10	0x0 RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS
9:2	0x0 RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0x0 RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky. **Power Well:** SUS

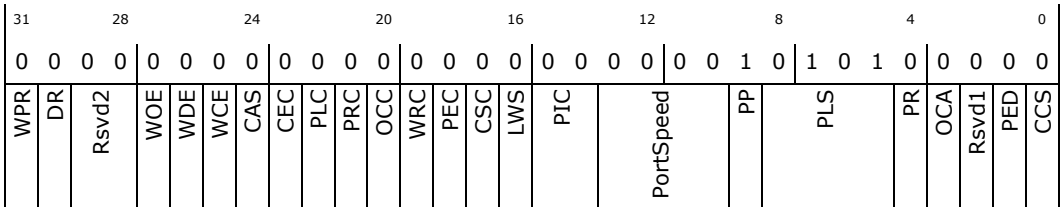
7.2.30 Port Status and Control USB2 (PORTSC5)—Offset 4C0h

Access Method

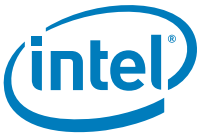
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4C0h

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

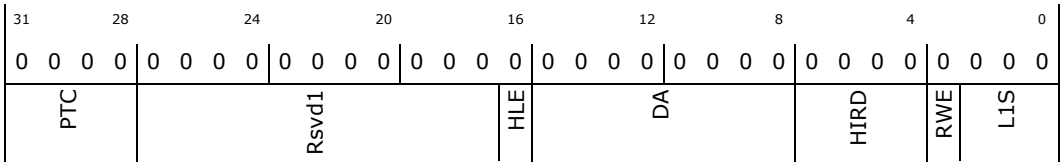
7.2.31 Port Power Management Status and Control USB2 (PORTPMSC5)—Offset 4C4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4C4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
27:17	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0x0 RW	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	0x0 RW	**Device Address (DA):** Note: This register is sticky. **Power Well:** SUS
7:4	0x0 RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0x0 RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0x0 RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

7.2.32 Port X Hardware LPM Control Register (PORTHLPMC5)—Offset 4CCh

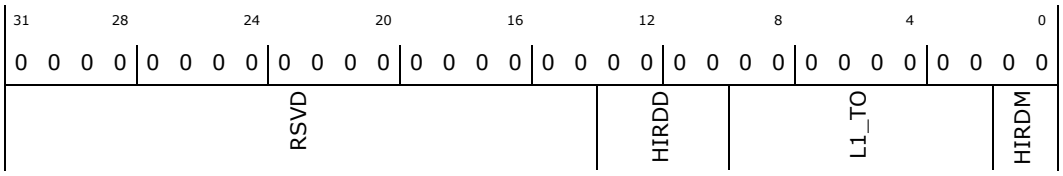
There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4CCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
13:10	0x0 RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS
9:2	0x0 RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0x0 RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky. **Power Well:** SUS

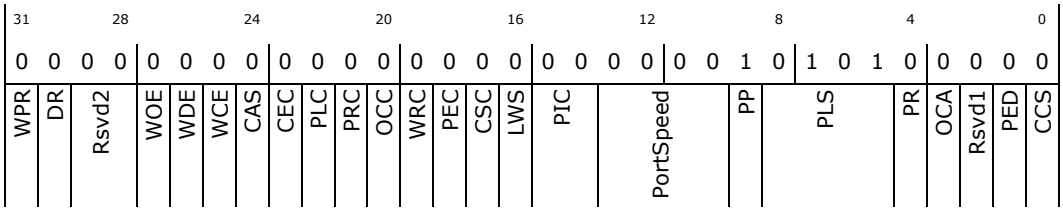
7.2.33 Port Status and Control USB2 (PORTSC6)—Offset 4D0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4D0h

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

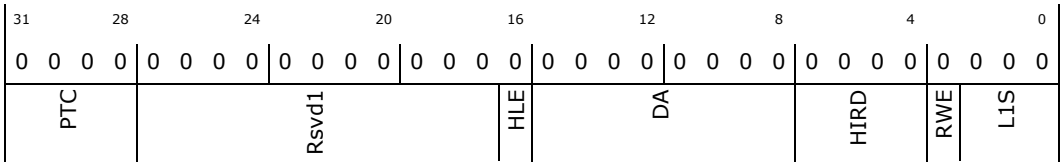
7.2.34 Port Power Management Status and Control USB2 (PORTPMSC6)—Offset 4D4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4D4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
27:17	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0x0 RW	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	0x0 RW	**Device Address (DA):** Note: This register is sticky. **Power Well:** SUS
7:4	0x0 RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0x0 RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0x0 RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

7.2.35 Port X Hardware LPM Control Register (PORTHLPMC6)—Offset 4DCh

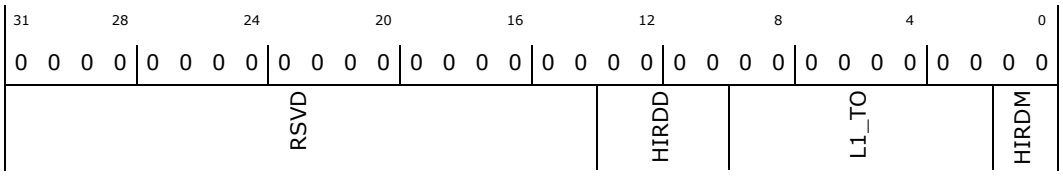
There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4DCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
13:10	0x0 RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS
9:2	0x0 RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0x0 RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky. **Power Well:** SUS

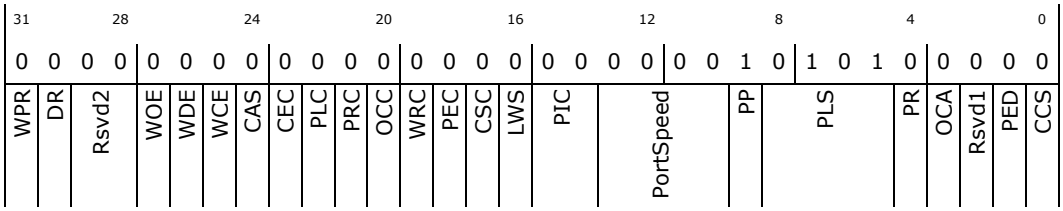
7.2.36 Port Status and Control USB2 (PORTSC7)—Offset 4E0h

Access Method

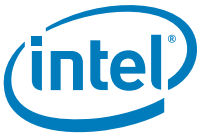
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4E0h

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

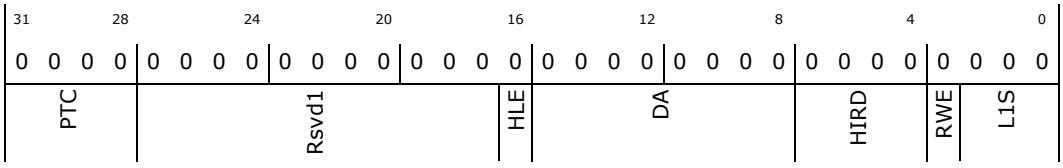
7.2.37 Port Power Management Status and Control USB2 (PORTPMSC7)—Offset 4E4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4E4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
27:17	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0x0 RW	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	0x0 RW	**Device Address (DA):** Note: This register is sticky. **Power Well:** SUS
7:4	0x0 RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0x0 RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0x0 RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

7.2.38 Port X Hardware LPM Control Register (PORTHLPMC7)—Offset 4ECh

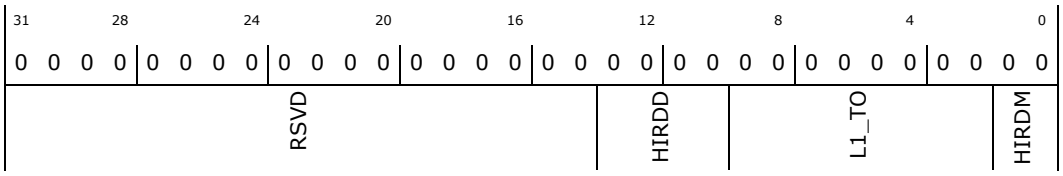
There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4ECh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
13:10	0x0 RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS
9:2	0x0 RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0x0 RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky. **Power Well:** SUS

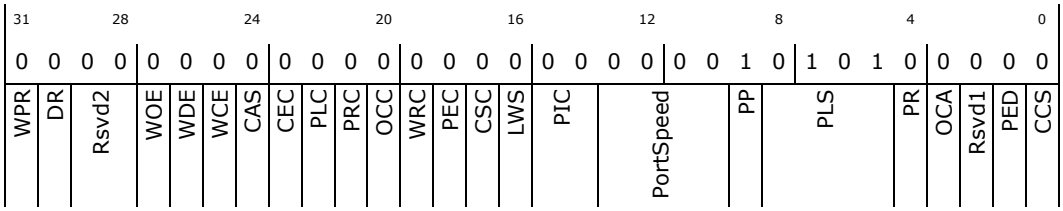
7.2.39 Port Status and Control USB3 (PORTSC8)—Offset 4F0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4F0h

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

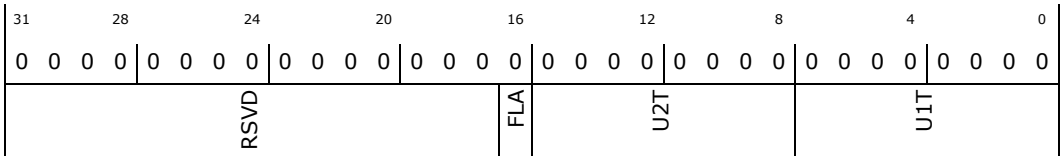
7.2.40 Port Power Management Status and Control USB3 (PORTPMSC8)—Offset 4F4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4F4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW	**Force Link PM Accept (FLA):** Reserved. **Power Well:** SUS
15:8	0x0 RW/S	**U2 Timeout (U2T):** Reserved. **Power Well:** SUS
7:0	0x0 RW/S	**U1 Timeout (U1T):** Reserved. **Power Well:** SUS

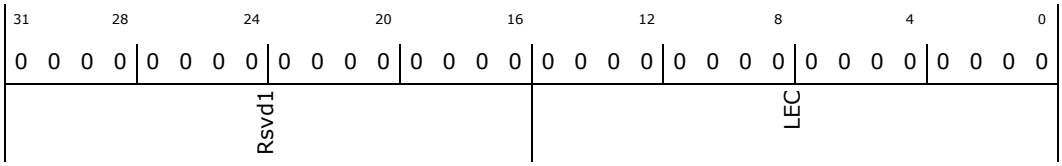
7.2.41 USB3 Port Link Info (PORTLI8)—Offset 4F8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 4F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RO	**Link Error Count (LEC):** Reserved. **Power Well:** Core

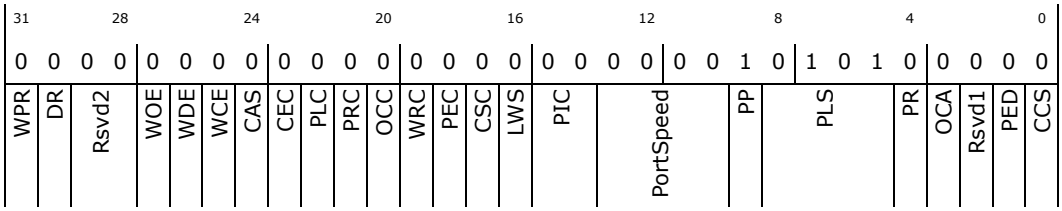
7.2.42 Port Status and Control USB3 (PORTSC9)—Offset 500h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 500h

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

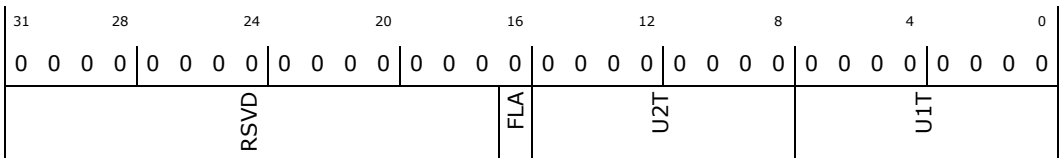
7.2.43 Port Power Management Status and Control USB3 (PORTPMSC9)—Offset 504h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 504h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
16	0x0 RW	**Force Link PM Accept (FLA):** Reserved. **Power Well:** SUS
15:8	0x0 RW/S	**U2 Timeout (U2T):** Reserved. **Power Well:** SUS
7:0	0x0 RW/S	**U1 Timeout (U1T):** Reserved. **Power Well:** SUS

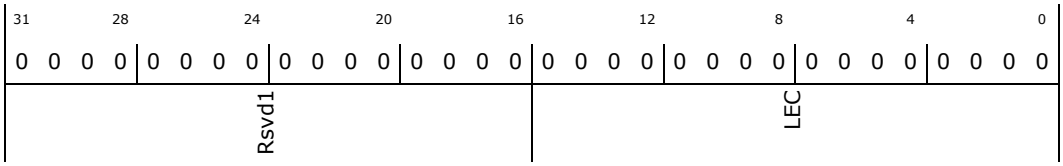
7.2.44 USB3 Port Link Info (PORTLI9)—Offset 508h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 508h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RO	**Link Error Count (LEC):** Reserved. **Power Well:** Core

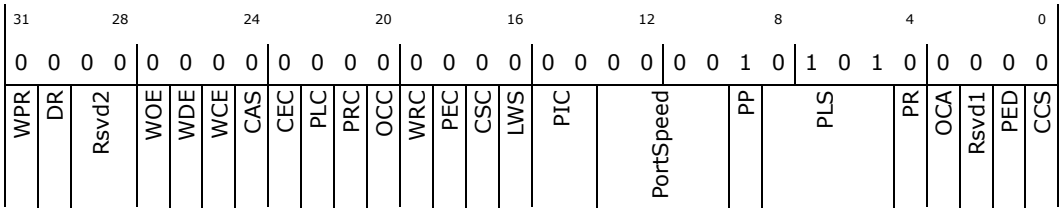
7.2.45 Port Status and Control USB3 (PORTSC10)—Offset 510h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 510h

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

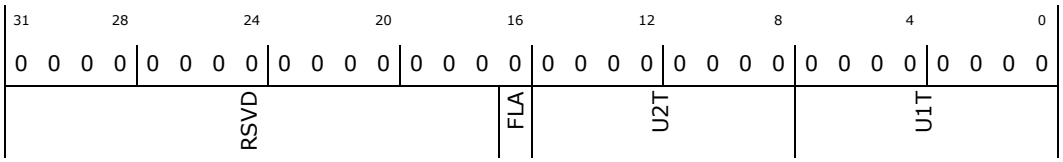
7.2.46 Port Power Management Status and Control USB3 (PORTPMSC10)—Offset 514h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 514h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
16	0x0 RW	**Force Link PM Accept (FLA):** Reserved. **Power Well:** SUS
15:8	0x0 RW/S	**U2 Timeout (U2T):** Reserved. **Power Well:** SUS
7:0	0x0 RW/S	**U1 Timeout (U1T):** Reserved. **Power Well:** SUS

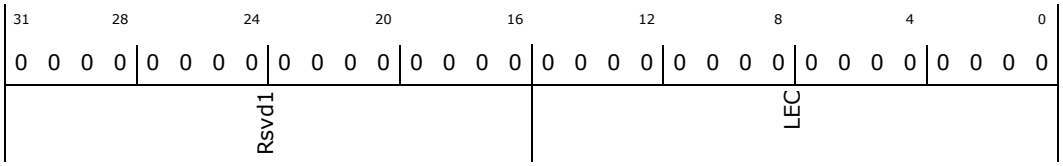
7.2.47 USB3 Port Link Info (PORTLI10)—Offset 518h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 518h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RO	**Link Error Count (LEC):** Reserved. **Power Well:** Core

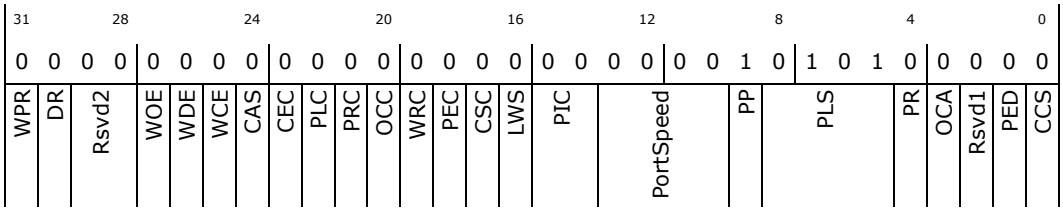
7.2.48 Port Status and Control USB3 (PORTSC11)—Offset 520h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 520h

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

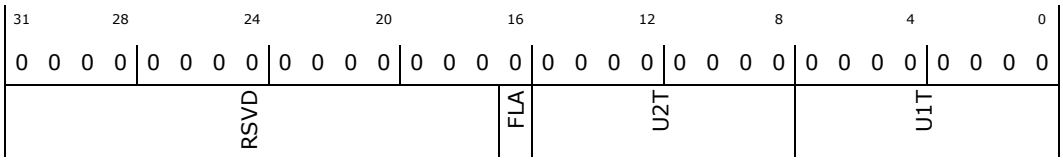
7.2.49 Port Power Management Status and Control USB3 (PORTPMSC11)—Offset 524h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 524h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
16	0x0 RW	**Force Link PM Accept (FLA):** Reserved. **Power Well:** SUS
15:8	0x0 RW/S	**U2 Timeout (U2T):** Reserved. **Power Well:** SUS
7:0	0x0 RW/S	**U1 Timeout (U1T):** Reserved. **Power Well:** SUS

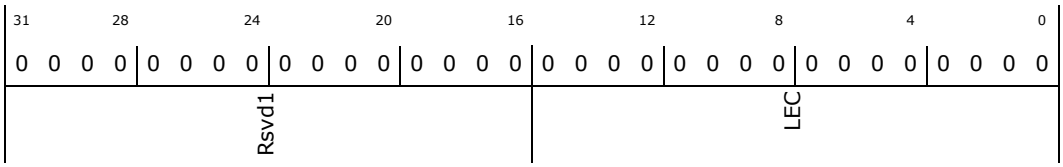
7.2.50 USB3 Port Link Info (PORTLI11)—Offset 528h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 528h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RO	**Link Error Count (LEC):** Reserved. **Power Well:** Core

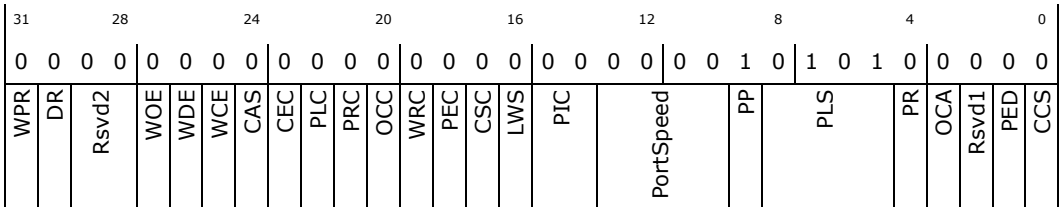
7.2.51 Port Status and Control USB3 (PORTSC12)—Offset 530h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 530h

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

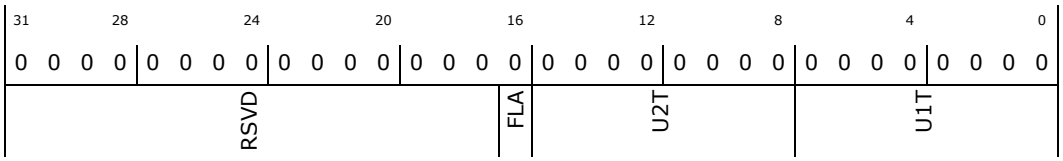
7.2.52 Port Power Management Status and Control USB3 (PORTPMSC12)—Offset 534h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 534h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
16	0x0 RW	**Force Link PM Accept (FLA):** Reserved. **Power Well:** SUS
15:8	0x0 RW/S	**U2 Timeout (U2T):** Reserved. **Power Well:** SUS
7:0	0x0 RW/S	**U1 Timeout (U1T):** Reserved. **Power Well:** SUS

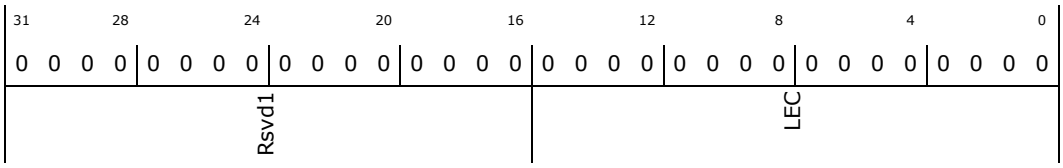
7.2.53 USB3 Port Link Info (PORTLI12)—Offset 538h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 538h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RO	**Link Error Count (LEC):** Reserved. **Power Well:** Core

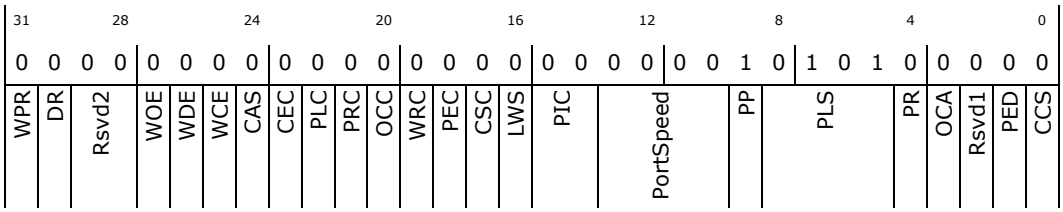
7.2.54 Port Status and Control USB3 (PORTSC13)—Offset 540h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 540h

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

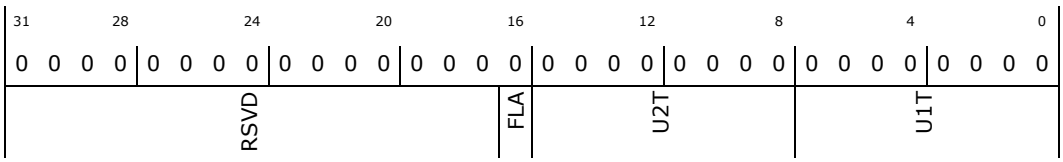
7.2.55 Port Power Management Status and Control USB3 (PORTPMSC13)—Offset 544h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 544h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
16	0x0 RW	**Force Link PM Accept (FLA):** Reserved. **Power Well:** SUS
15:8	0x0 RW/S	**U2 Timeout (U2T):** Reserved. **Power Well:** SUS
7:0	0x0 RW/S	**U1 Timeout (U1T):** Reserved. **Power Well:** SUS

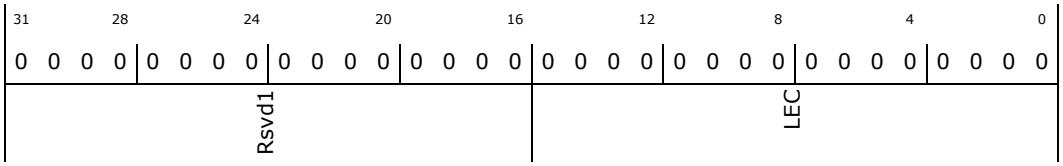
7.2.56 USB3 Port Link Info (PORTLI13)—Offset 548h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 548h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RO	**Link Error Count (LEC):** Reserved. **Power Well:** Core

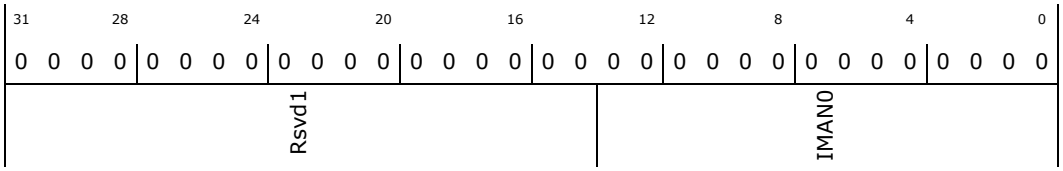
7.2.57 Microframe Index (RTMFINDEX)—Offset 2000h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2000h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
13:0	0x0 RO	**Microframe Index (IMAN0):** Reserved. **Power Well:** Core

7.2.58 Interrupter 1 Management (IMAN0)—Offset 2020h

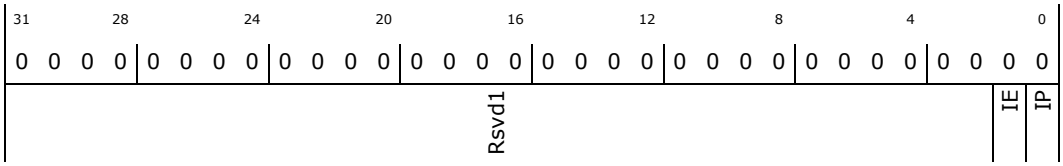
There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2020h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0x0 RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

7.2.59 Interrupter 1 Moderation (IMOD0)—Offset 2024h

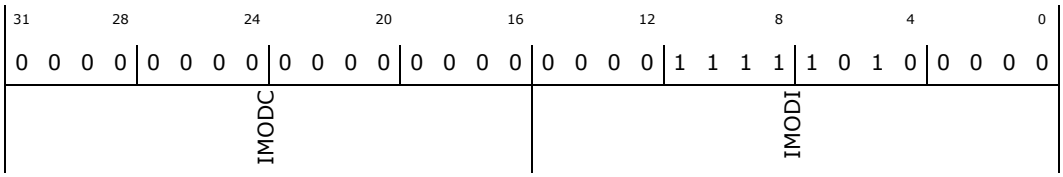
There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2024h

Default: 00000FA0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Interrupt Moderation Counter (IMODC):** Reserved. **Power Well:** Core
15:0	0xfa0 RW	**Interrupt Moderation Interval (IMODI):** Reserved. **Power Well:** Core

7.2.60 Event Ring Segment Table Size 1 (ERSTSZ0)—Offset 2028h

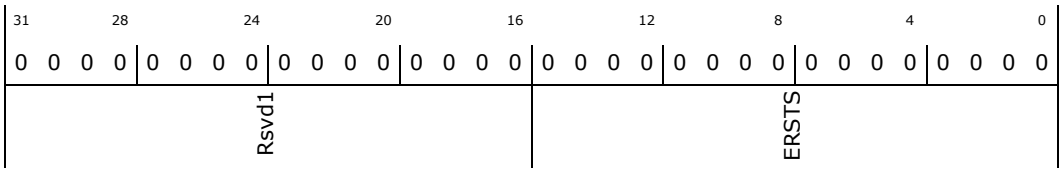
There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2028h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RW	**Event Ring Segment Table Size (ERSTS):** Reserved. **Power Well:** Core

7.2.61 Event Ring Segment Table Base Address Low 1 (ERSTBA_LO0)—Offset 2030h

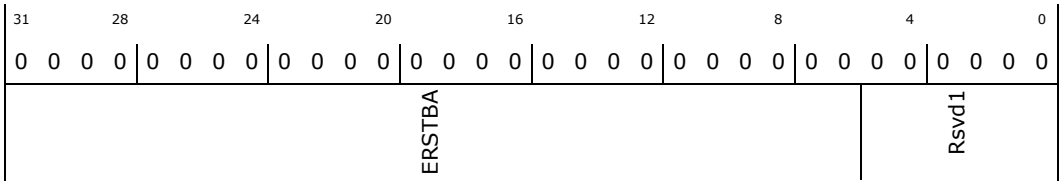
There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2030h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

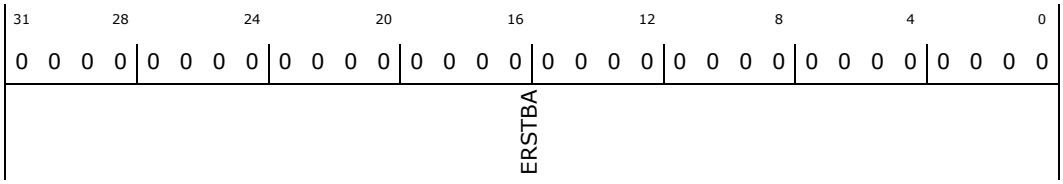
7.2.62 Event Ring Segment Table Base Address High 1 (ERSTBA_HI0)—Offset 2034h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2034h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Segment Table Base Address (ERSTBA):** Reserved. **Power Well:** Core

7.2.63 Event Ring Dequeue Pointer Low 1 (ERDP_LO0)—Offset 2038h

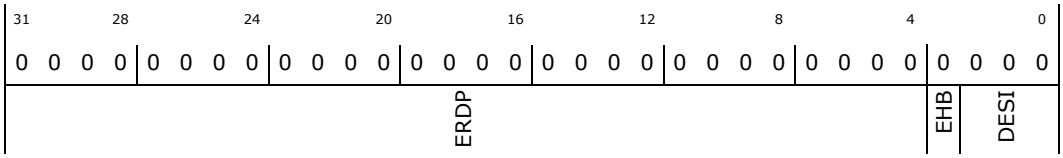
There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2038h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW/C	**Event Handler Busy (EHB):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Dequeue ERST Segment Index (DESI):** Reserved. **Power Well:** Core

7.2.64 Event Ring Dequeue Pointer High 1 (ERDP_HI0)—Offset 203Ch

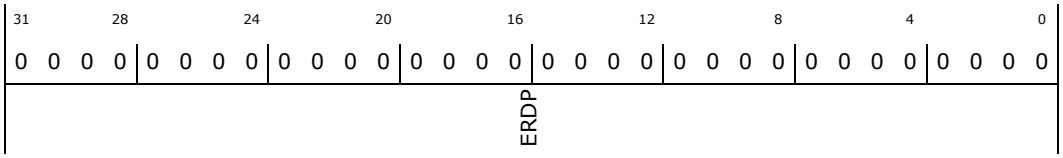
There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 203Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

7.2.65 Interrupter 2 Management (IMAN1)—Offset 2040h

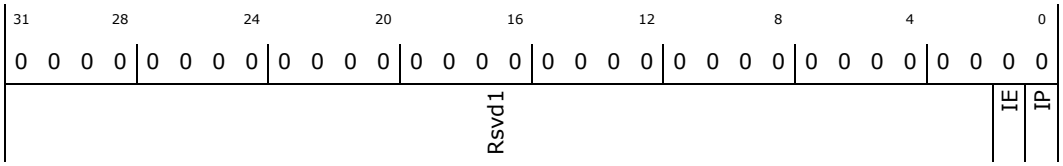
There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2040h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0x0 RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

7.2.66 Interrupter 2 Moderation (IMOD1)—Offset 2044h

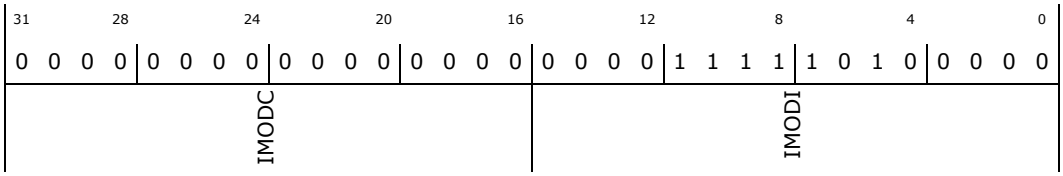
There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2044h

Default: 00000FA0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Interrupt Moderation Counter (IMODC):** Reserved. **Power Well:** Core
15:0	0xfa0 RW	**Interrupt Moderation Interval (IMODI):** Reserved. **Power Well:** Core

7.2.67 Event Ring Segment Table Size 2 (ERSTSZ1)—Offset 2048h

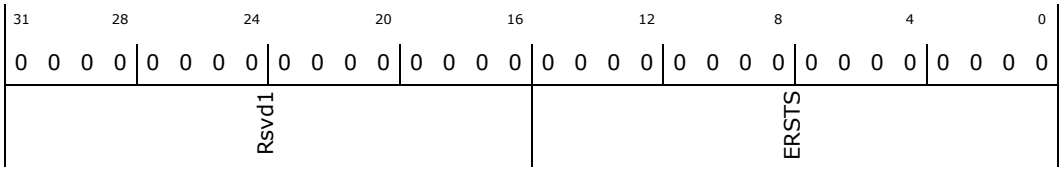
There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2048h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RW	**Event Ring Segment Table Size (ERSTS):** Reserved. **Power Well:** Core

7.2.68 Event Ring Segment Table Base Address Low 2 (ERSTBA_LO1)—Offset 2050h

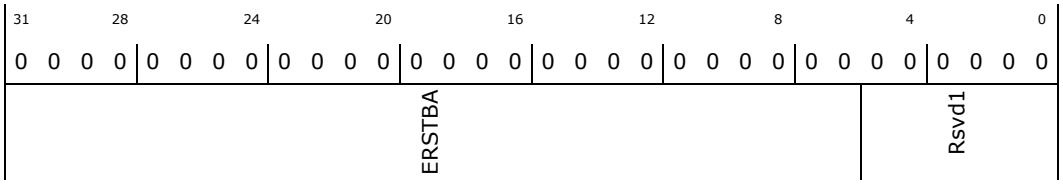
There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2050h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Reserved. **Power Well:** Core
5:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

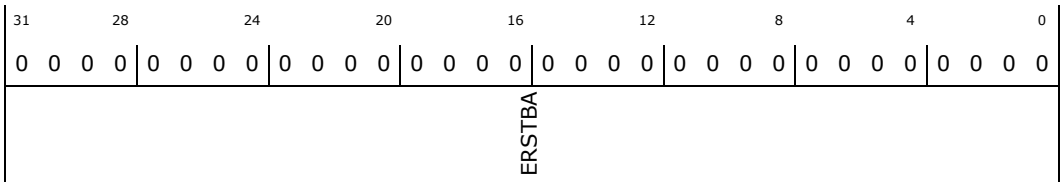
7.2.69 Event Ring Segment Table Base Address High 2 (ERSTBA_HI1)—Offset 2054h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2054h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Segment Table Base Address (ERSTBA):** Reserved. **Power Well:** Core

7.2.70 Event Ring Dequeue Pointer Low 2 (ERDP_LO1)—Offset 2058h

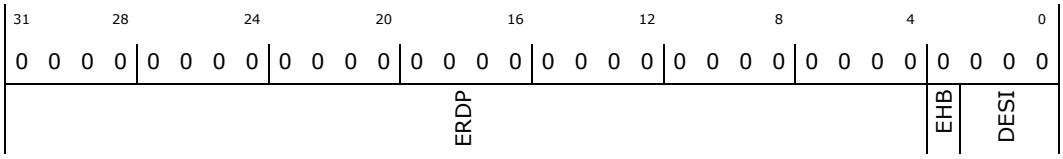
There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2058h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core
3	0x0 RW/C	**Event Handler Busy (EHB):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Dequeue ERST Segment Index (DESI):** Reserved. **Power Well:** Core

7.2.71 Event Ring Dequeue Pointer High 2 (ERDP_HI1)—Offset 205Ch

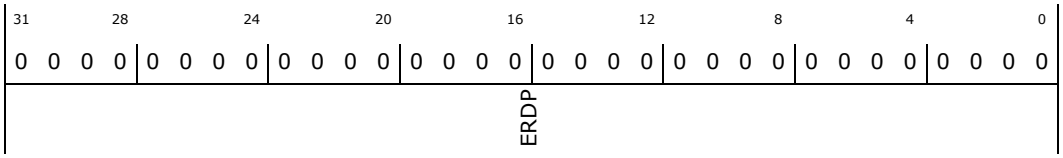
There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 205Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

7.2.72 Interrupter 3 Management (IMAN2)—Offset 2060h

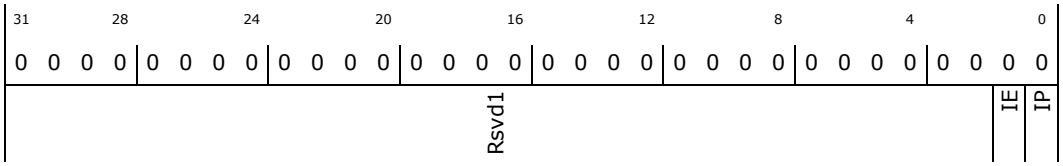
There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2060h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0x0 RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

7.2.73 Interrupter 3 Moderation (IMOD2)—Offset 2064h

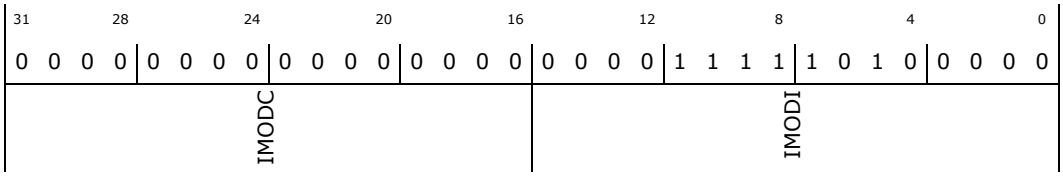
There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2064h

Default: 00000FA0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Interrupt Moderation Counter (IMODC):** Reserved. **Power Well:** Core
15:0	0xfa0 RW	**Interrupt Moderation Interval (IMODI):** Reserved. **Power Well:** Core

7.2.74 Event Ring Segment Table Size 3 (ERSTSZ2)—Offset 2068h

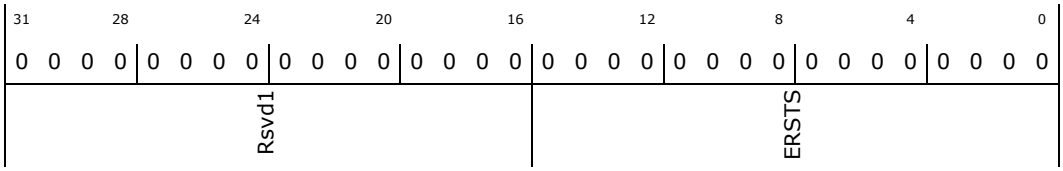
There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2068h

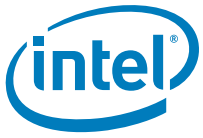
Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RW	**Event Ring Segment Table Size (ERSTS):** Reserved. **Power Well:** Core

7.2.75 Event Ring Segment Table Base Address Low 3 (ERSTBA_LO2)—Offset 2070h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

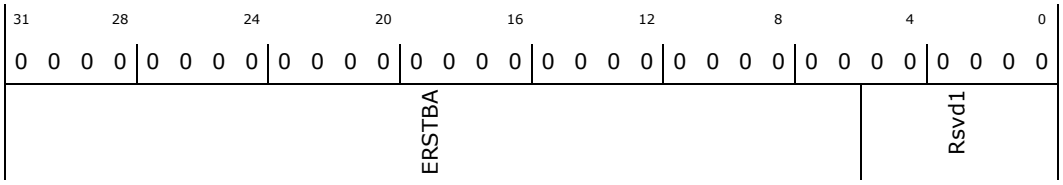


Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2070h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Reserved. **Power Well:** Core
5:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

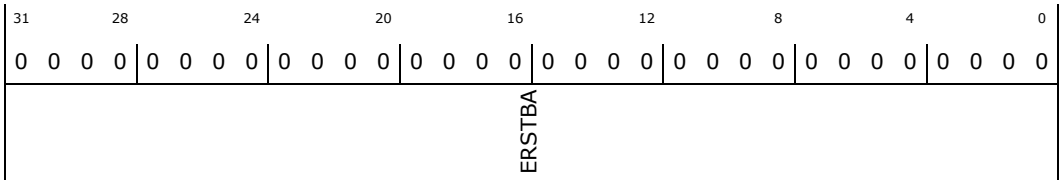
7.2.76 Event Ring Segment Table Base Address High 3 (ERSTBA_HI2)—Offset 2074h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2074h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Segment Table Base Address (ERSTBA):** Reserved. **Power Well:** Core

7.2.77 Event Ring Dequeue Pointer Low 3 (ERDP_LO2)—Offset 2078h

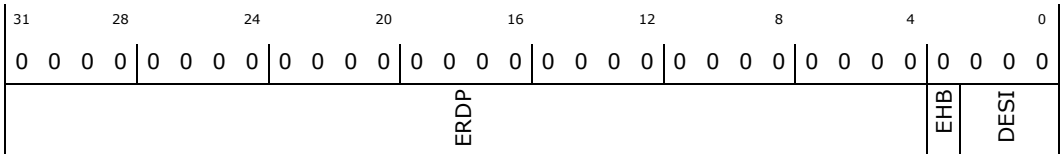
There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2078h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core
3	0x0 RW/C	**Event Handler Busy (EHB):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Dequeue ERST Segment Index (DESI):** Reserved. **Power Well:** Core

7.2.78 Event Ring Dequeue Pointer High 3 (ERDP_HI2)—Offset 207Ch

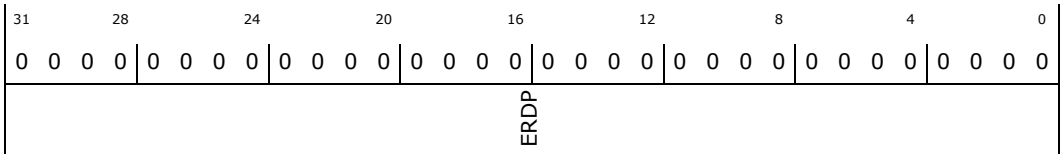
There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 207Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

7.2.79 Interrupter 4 Management (IMAN3)—Offset 2080h

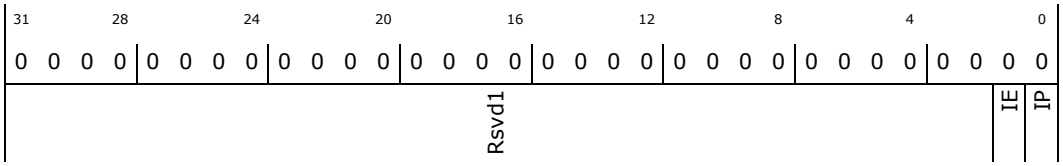
There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2080h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0x0 RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

7.2.80 Interrupter 4 Moderation (IMOD3)—Offset 2084h

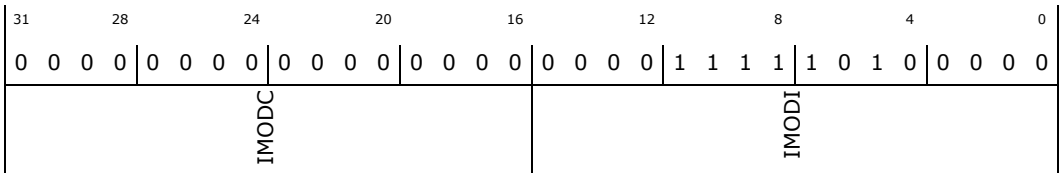
There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2084h

Default: 00000FA0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Interrupt Moderation Counter (IMODC):** Reserved. **Power Well:** Core
15:0	0xfa0 RW	**Interrupt Moderation Interval (IMODI):** Reserved. **Power Well:** Core

7.2.81 Event Ring Segment Table Size 4 (ERSTSZ3)—Offset 2088h

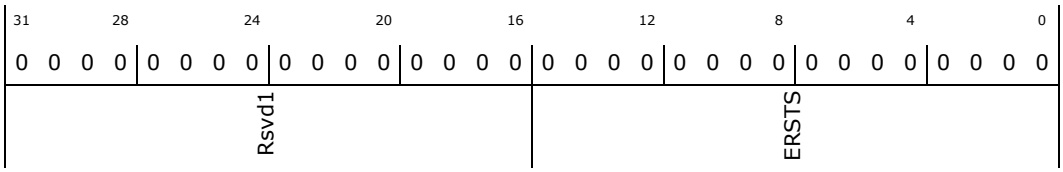
There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2088h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RW	**Event Ring Segment Table Size (ERSTS):** Reserved. **Power Well:** Core

7.2.82 Event Ring Segment Table Base Address Low 4 (ERSTBA_LO3)—Offset 2090h

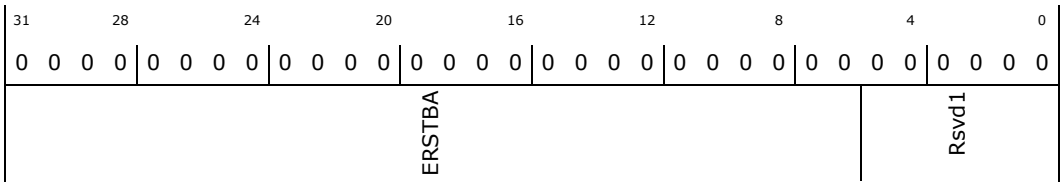
There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2090h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

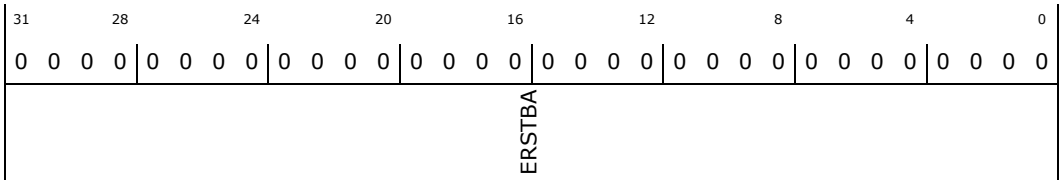
7.2.83 Event Ring Segment Table Base Address High 4 (ERSTBA_HI3)—Offset 2094h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2094h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Segment Table Base Address (ERSTBA):** Reserved. **Power Well:** Core

7.2.84 Event Ring Dequeue Pointer Low 4 (ERDP_LO3)—Offset 2098h

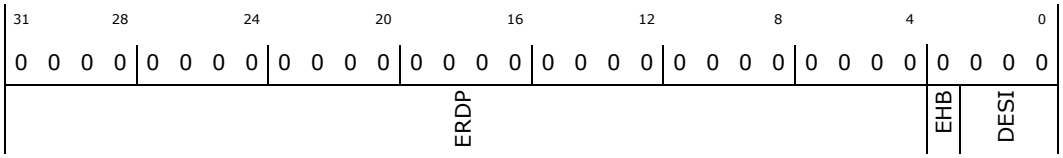
There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2098h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW/C	**Event Handler Busy (EHB):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Dequeue ERST Segment Index (DESI):** Reserved. **Power Well:** Core

7.2.85 Event Ring Dequeue Pointer High 4 (ERDP_HI3)—Offset 209Ch

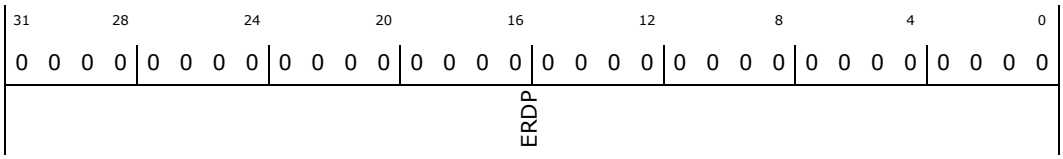
There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 209Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

7.2.86 Interrupter 5 Management (IMAN4)—Offset 20A0h

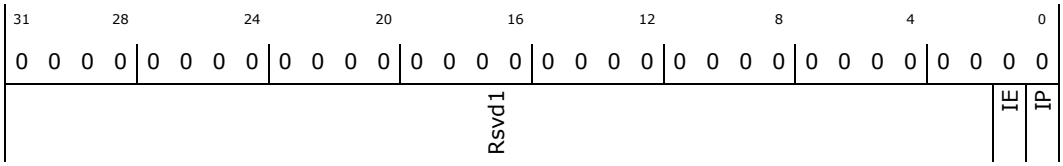
There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0x0 RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

7.2.87 Interrupter 5 Moderation (IMOD4)—Offset 20A4h

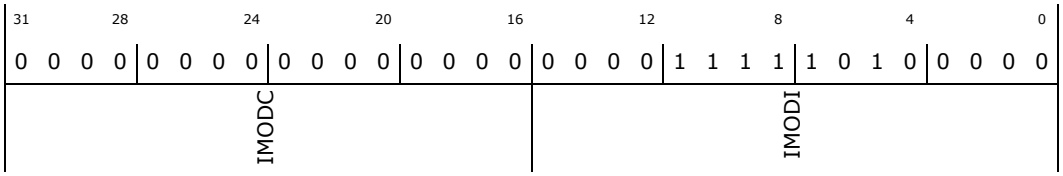
There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20A4h

Default: 00000FA0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Interrupt Moderation Counter (IMODC):** Reserved. **Power Well:** Core
15:0	0xfa0 RW	**Interrupt Moderation Interval (IMODI):** Reserved. **Power Well:** Core

7.2.88 Event Ring Segment Table Size 5 (ERSTSZ4)—Offset 20A8h

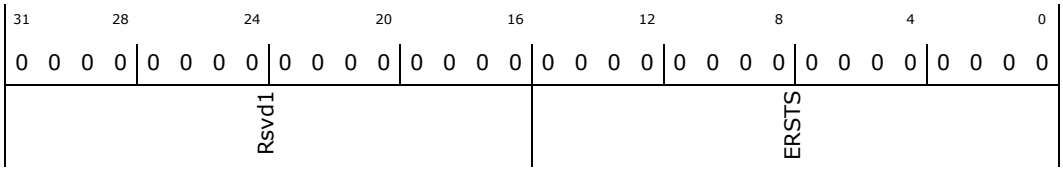
There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RW	**Event Ring Segment Table Size (ERSTS):** Reserved. **Power Well:** Core

7.2.89 Event Ring Segment Table Base Address Low 5 (ERSTBA_LO4)—Offset 20B0h

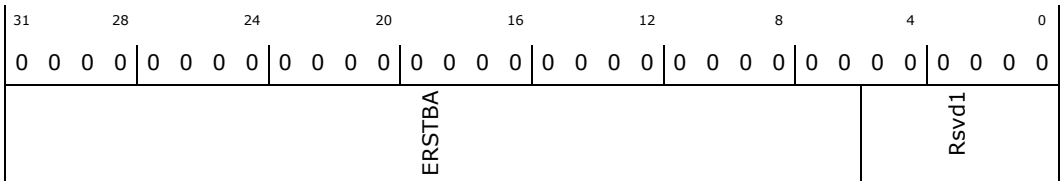
There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Reserved. **Power Well:** Core
5:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

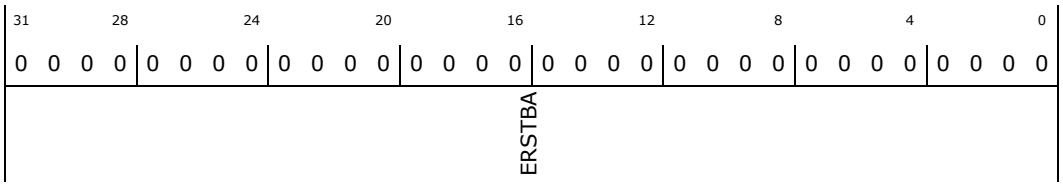
7.2.90 Event Ring Segment Table Base Address High 5 (ERSTBA_HI4)—Offset 20B4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20B4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Segment Table Base Address (ERSTBA):** Reserved. **Power Well:** Core

7.2.91 Event Ring Dequeue Pointer Low 5 (ERDP_LO4)—Offset 20B8h

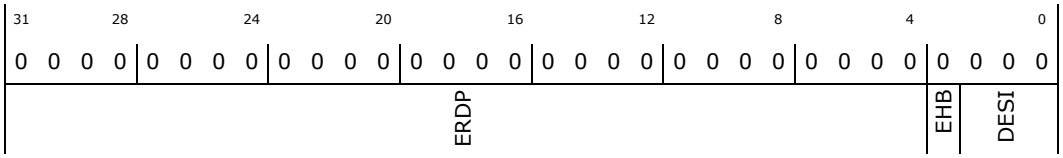
There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core
3	0x0 RW/C	**Event Handler Busy (EHB):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Dequeue ERST Segment Index (DESI):** Reserved. **Power Well:** Core

7.2.92 Event Ring Dequeue Pointer High 5 (ERDP_HI4)—Offset 20BCh

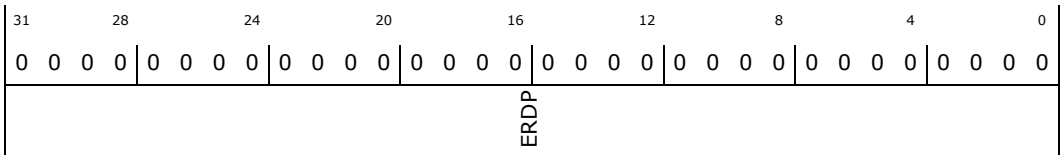
There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20BCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

7.2.93 Interrupter 6 Management (IMAN5)—Offset 20C0h

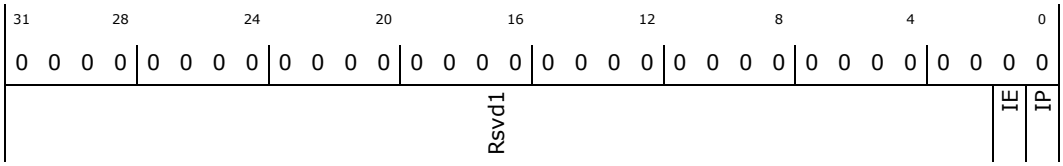
There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0x0 RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

7.2.94 Interrupter 6 Moderation (IMOD5)—Offset 20C4h

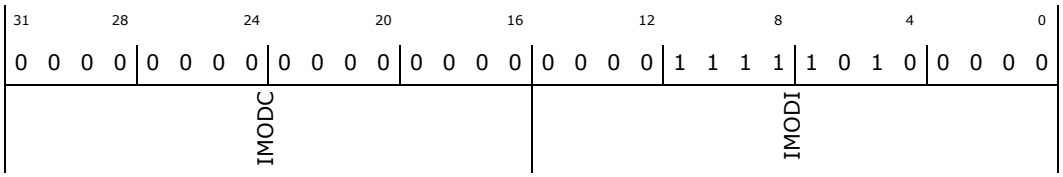
There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20C4h

Default: 00000FA0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Interrupt Moderation Counter (IMODC):** Reserved. **Power Well:** Core
15:0	0xfa0 RW	**Interrupt Moderation Interval (IMODI):** Reserved. **Power Well:** Core

7.2.95 Event Ring Segment Table Size 6 (ERSTSZ5)—Offset 20C8h

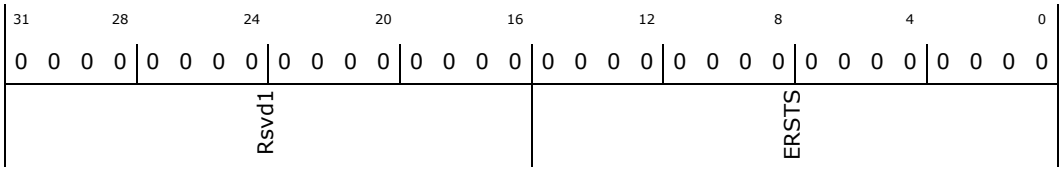
There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20C8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RW	**Event Ring Segment Table Size (ERSTS):** Reserved. **Power Well:** Core

7.2.96 Event Ring Segment Table Base Address Low 6 (ERSTBA_LO5)—Offset 20D0h

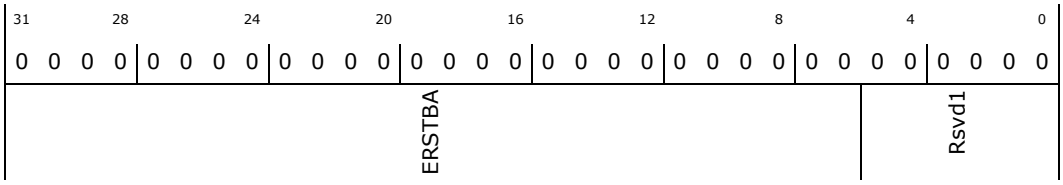
There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Reserved. **Power Well:** Core
5:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

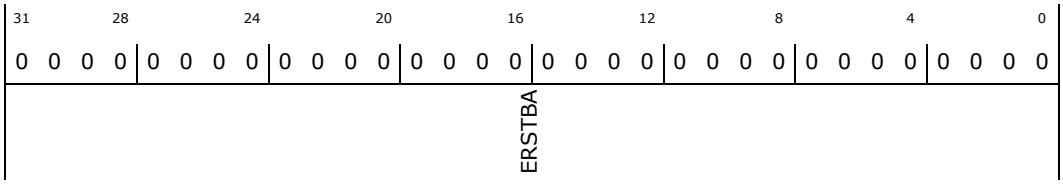
7.2.97 Event Ring Segment Table Base Address High 6 (ERSTBA_HI5)—Offset 20D4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20D4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Segment Table Base Address (ERSTBA):** Reserved. **Power Well:** Core

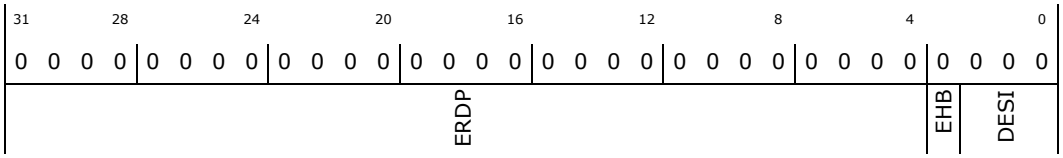
7.2.98 Event Ring Dequeue Pointer Low 6 (ERDP_LO5)—Offset 20D8h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** [MBAR] + 20D8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core
3	0x0 RW/C	**Event Handler Busy (EHB):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Dequeue ERST Segment Index (DESI):** Reserved. **Power Well:** Core

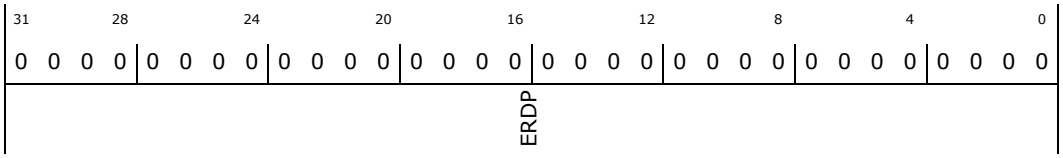
7.2.99 Event Ring Dequeue Pointer High 6 (ERDP_HI5)—Offset 20DCh

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** [MBAR] + 20DCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

7.2.100 Interrupter 7 Management (IMAN6)—Offset 20E0h

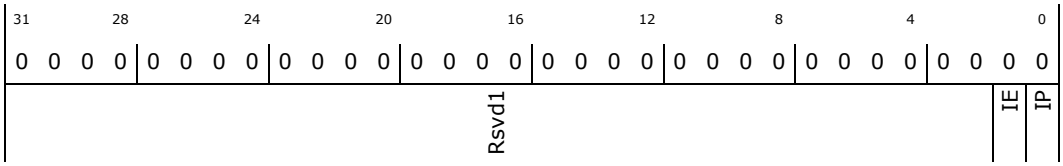
There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20E0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0x0 RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

7.2.101 Interrupter 7 Moderation (IMOD6)—Offset 20E4h

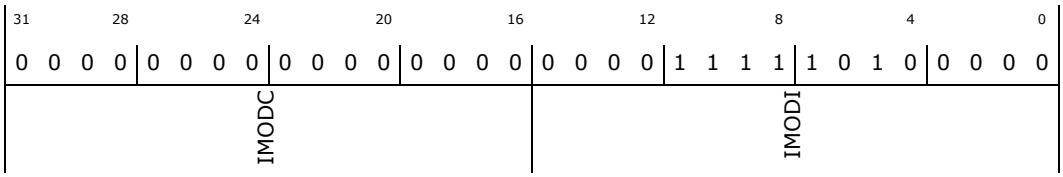
There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20E4h

Default: 00000FA0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Interrupt Moderation Counter (IMODC):** Reserved. **Power Well:** Core
15:0	0xfa0 RW	**Interrupt Moderation Interval (IMODI):** Reserved. **Power Well:** Core

7.2.102 Event Ring Segment Table Size 7 (ERSTSZ6)—Offset 20E8h

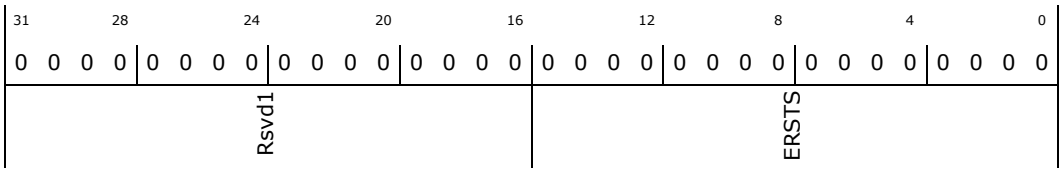
There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20E8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RW	**Event Ring Segment Table Size (ERSTS):** Reserved. **Power Well:** Core

7.2.103 Event Ring Segment Table Base Address Low 7 (ERSTBA_LO6)—Offset 20F0h

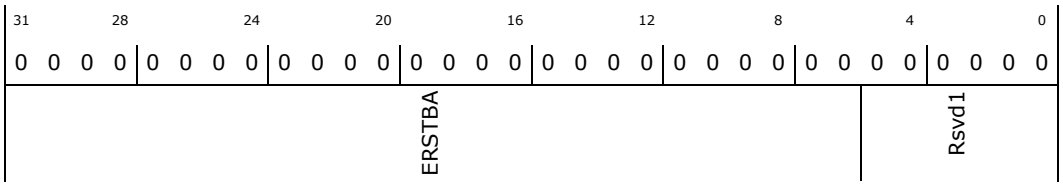
There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20F0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

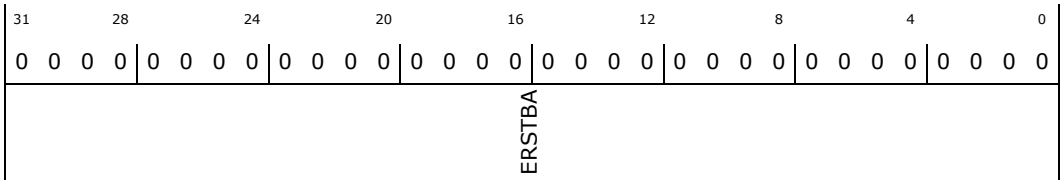
7.2.104 Event Ring Segment Table Base Address High 7 (ERSTBA_HI6)—Offset 20F4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20F4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Segment Table Base Address (ERSTBA):** Reserved. **Power Well:** Core

7.2.105 Event Ring Dequeue Pointer Low 7 (ERDP_LO6)—Offset 20F8h

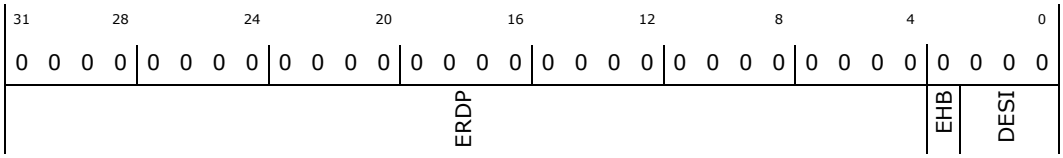
There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW/C	**Event Handler Busy (EHB):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Dequeue ERST Segment Index (DESI):** Reserved. **Power Well:** Core

7.2.106 Event Ring Dequeue Pointer High 7 (ERDP_HI6)—Offset 20FCh

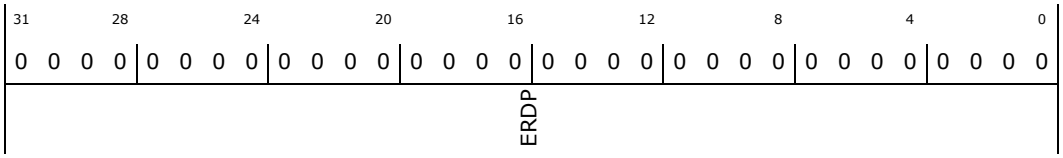
There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 20FCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

7.2.107 Interrupter 8 Management (IMAN7)—Offset 2100h

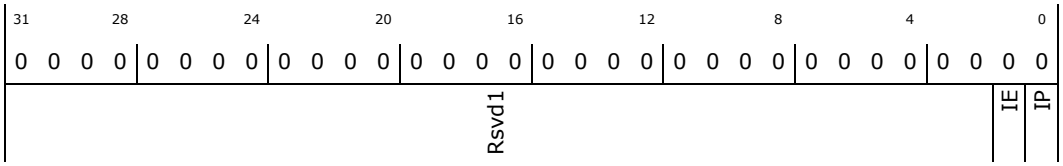
There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2100h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0x0 RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

7.2.108 Interrupter 8 Moderation (IMOD7)—Offset 2104h

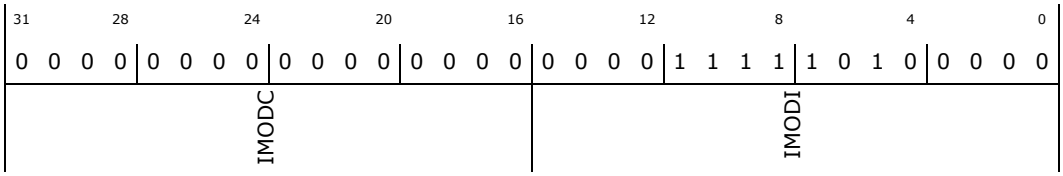
There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2104h

Default: 00000FA0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Interrupt Moderation Counter (IMODC):** Reserved. **Power Well:** Core
15:0	0xfa0 RW	**Interrupt Moderation Interval (IMODI):** Reserved. **Power Well:** Core

7.2.109 Event Ring Segment Table Size 8 (ERSTSZ7)—Offset 2108h

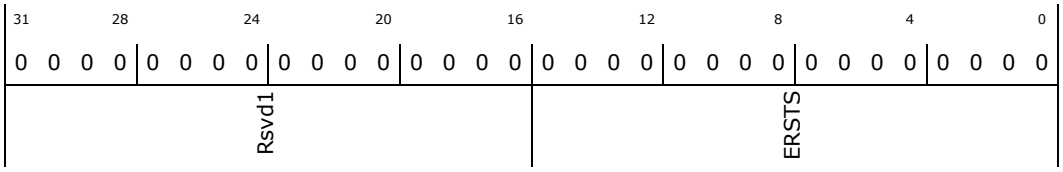
There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2108h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RW	**Event Ring Segment Table Size (ERSTS):** Reserved. **Power Well:** Core

7.2.110 Event Ring Segment Table Base Address Low 8 (ERSTBA_LO7)—Offset 2110h

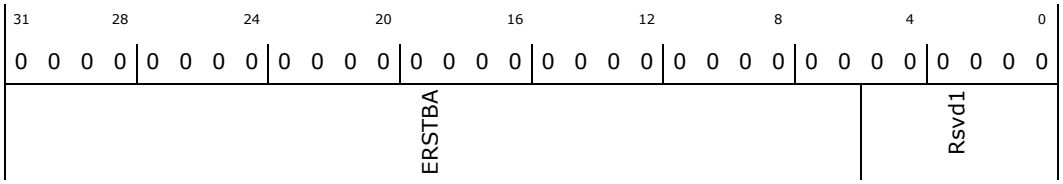
There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2110h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Reserved. **Power Well:** Core
5:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

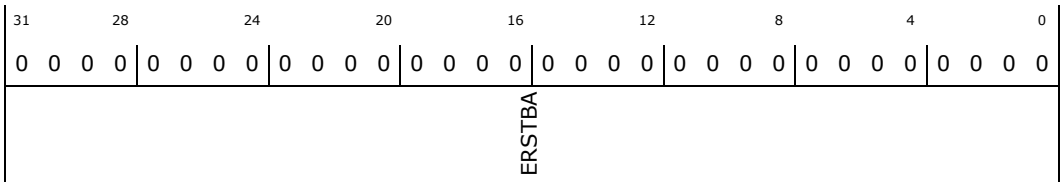
7.2.111 Event Ring Segment Table Base Address High 8 (ERSTBA_HI7)—Offset 2114h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2114h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Segment Table Base Address (ERSTBA):** Reserved. **Power Well:** Core

7.2.112 Event Ring Dequeue Pointer Low 8 (ERDP_LO7)—Offset 2118h

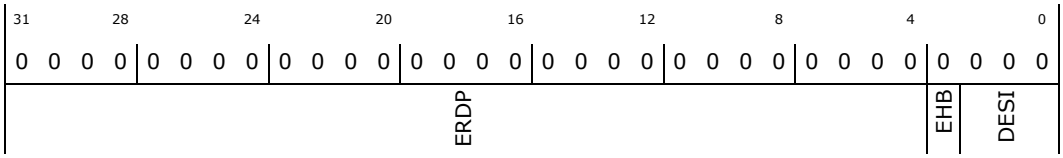
There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 2118h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core
3	0x0 RW/C	**Event Handler Busy (EHB):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Dequeue ERST Segment Index (DESI):** Reserved. **Power Well:** Core

7.2.113 Event Ring Dequeue Pointer High 8 (ERDP_HI7)—Offset 211Ch

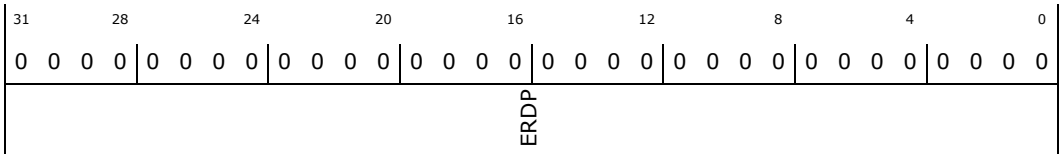
There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 211Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

7.2.114 Door Bell 1 (DB0)—Offset 3000h

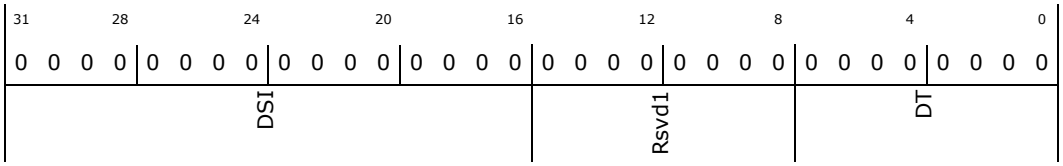
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3000h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.115 Door Bell 2 (DB1)—Offset 3004h

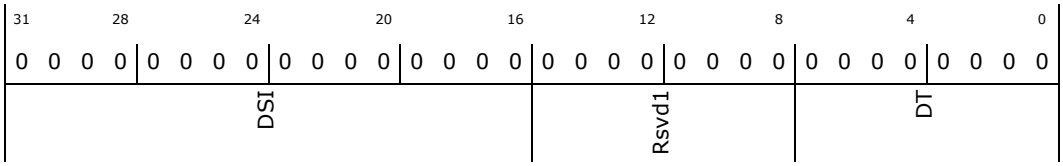
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3004h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.116 Door Bell 3 (DB2)—Offset 3008h

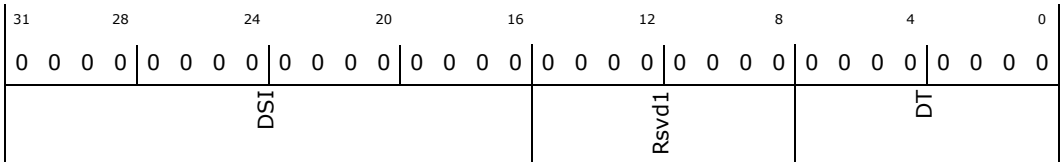
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3008h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.117 Door Bell 4 (DB3)—Offset 300Ch

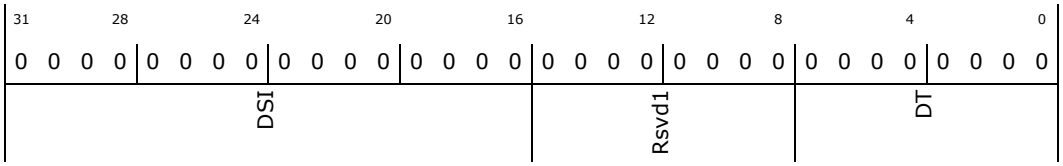
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 300Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.118 Door Bell 5 (DB4)—Offset 3010h

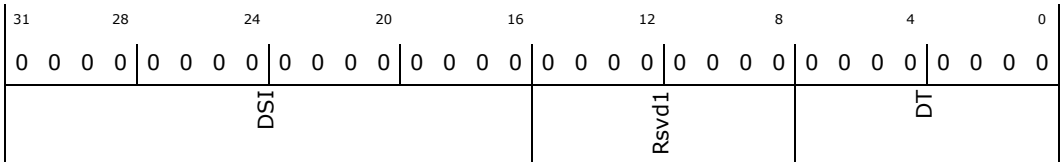
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3010h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.119 Door Bell 6 (DB5)—Offset 3014h

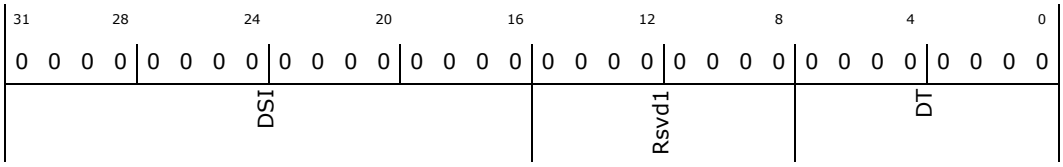
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3014h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.120 Door Bell 7 (DB6)—Offset 3018h

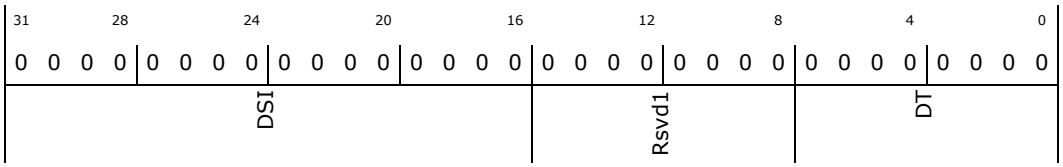
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3018h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.121 Door Bell 8 (DB7)—Offset 301Ch

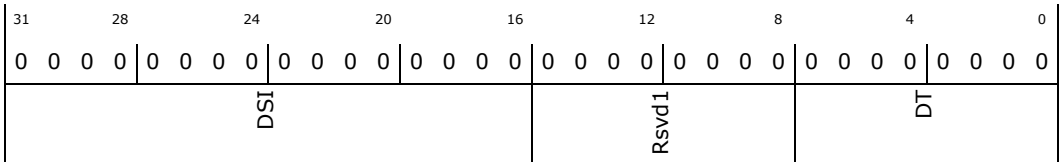
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 301Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.122 Door Bell 9 (DB8)—Offset 3020h

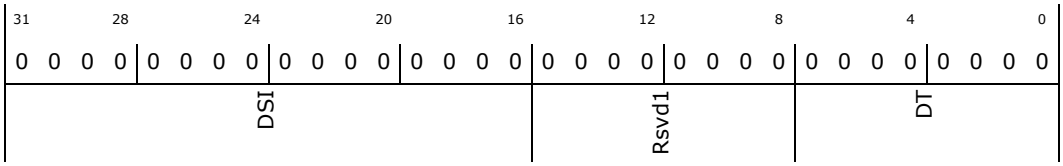
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3020h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.123 Door Bell 10 (DB9)—Offset 3024h

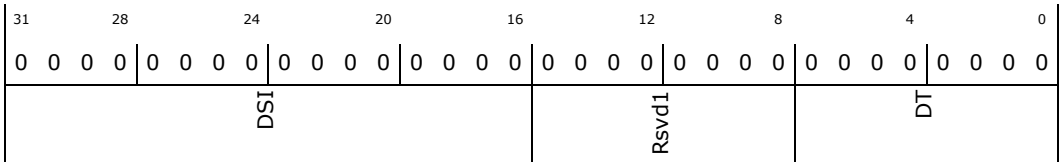
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3024h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.124 Door Bell 11 (DB10)—Offset 3028h

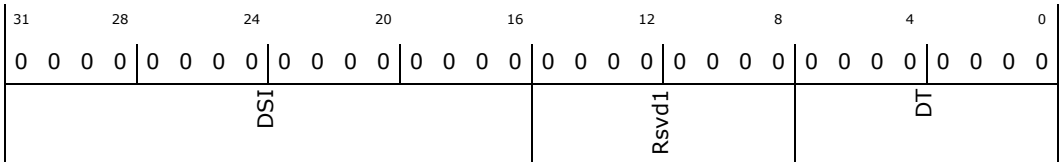
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3028h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.125 Door Bell 12 (DB11)—Offset 302Ch

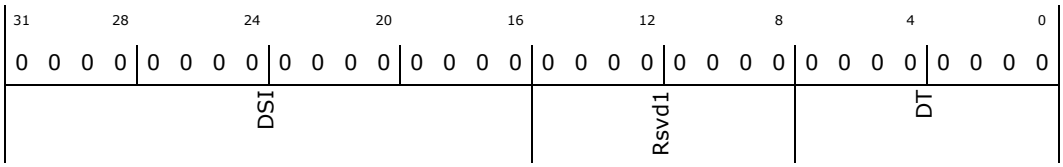
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 302Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.126 Door Bell 13 (DB12)—Offset 3030h

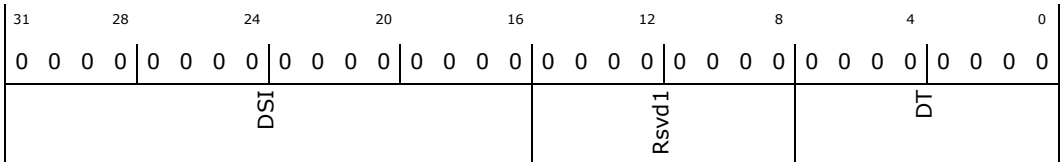
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3030h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.127 Door Bell 14 (DB13)—Offset 3034h

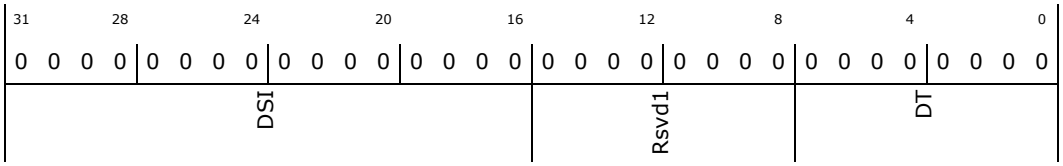
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3034h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.128 Door Bell 15 (DB14)—Offset 3038h

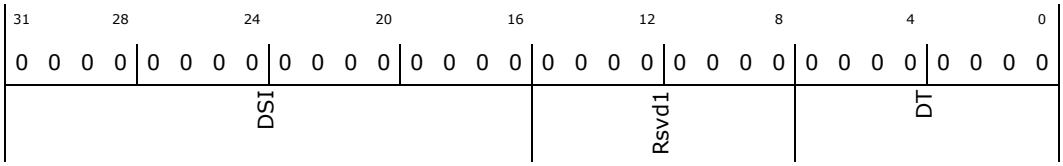
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3038h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.129 Door Bell 16 (DB15)—Offset 303Ch

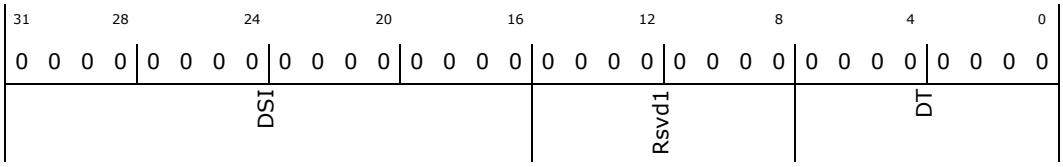
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 303Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.130 Door Bell 17 (DB16)—Offset 3040h

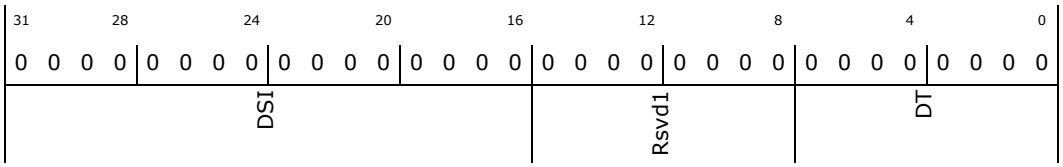
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3040h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.131 Door Bell 18 (DB17)—Offset 3044h

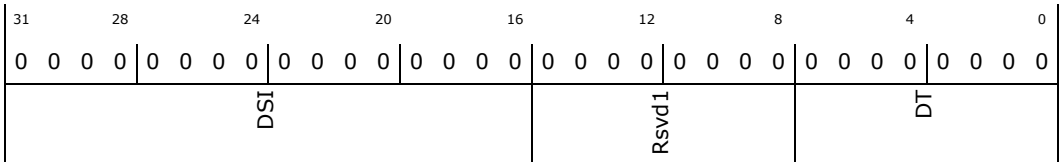
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3044h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.132 Door Bell 19 (DB18)—Offset 3048h

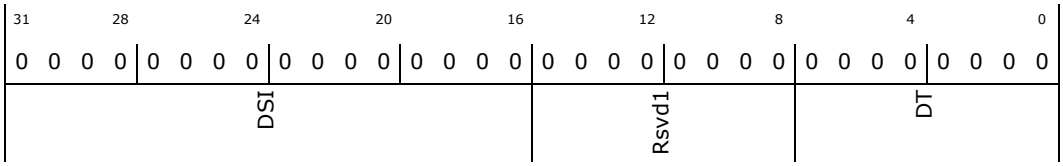
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3048h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.133 Door Bell 20 (DB19)—Offset 304Ch

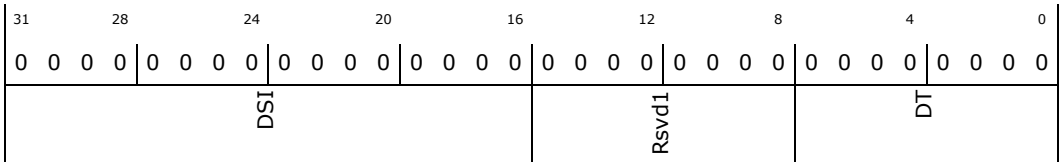
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 304Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.134 Door Bell 21 (DB20)—Offset 3050h

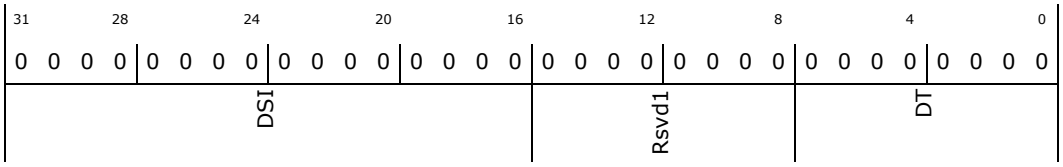
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3050h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.135 Door Bell 22 (DB21)—Offset 3054h

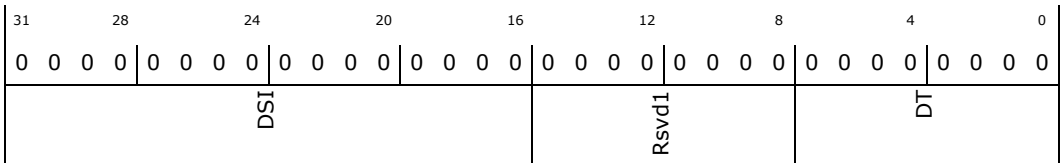
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3054h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.136 Door Bell 23 (DB22)—Offset 3058h

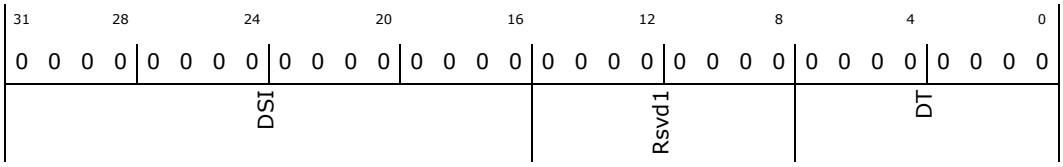
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3058h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.137 Door Bell 24 (DB23)—Offset 305Ch

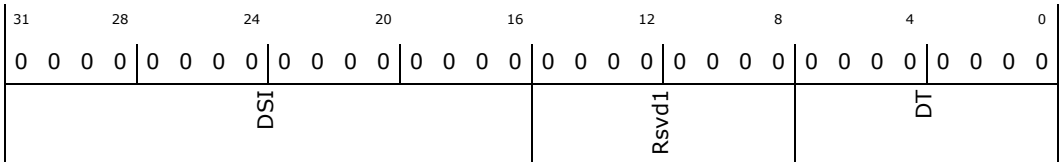
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 305Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.138 Door Bell 25 (DB24)—Offset 3060h

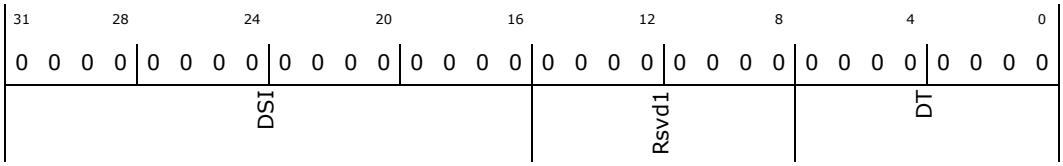
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3060h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.139 Door Bell 26 (DB25)—Offset 3064h

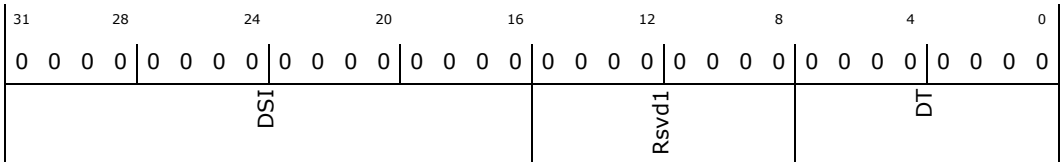
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3064h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.140 Door Bell 27 (DB26)—Offset 3068h

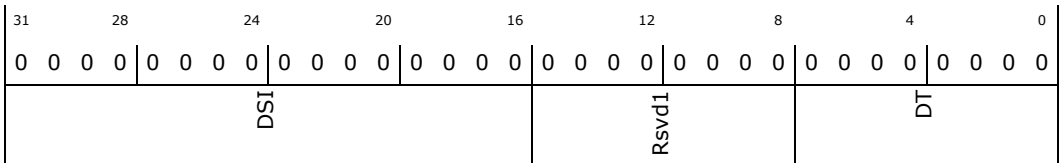
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3068h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.141 Door Bell 28 (DB27)—Offset 306Ch

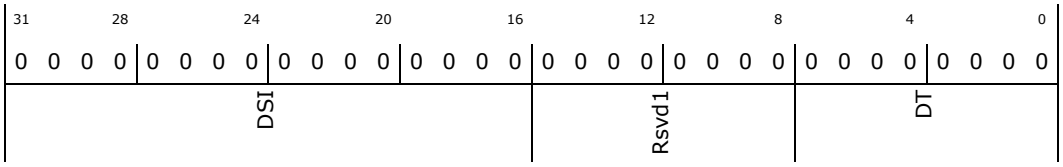
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 306Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.142 Door Bell 29 (DB28)—Offset 3070h

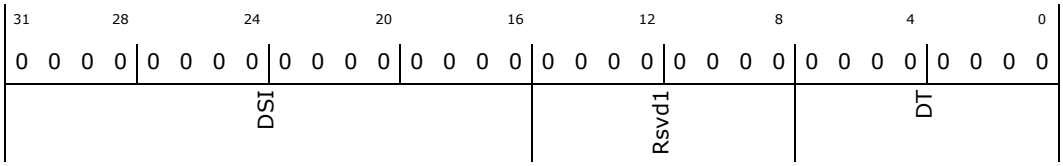
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3070h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.143 Door Bell 30 (DB29)—Offset 3074h

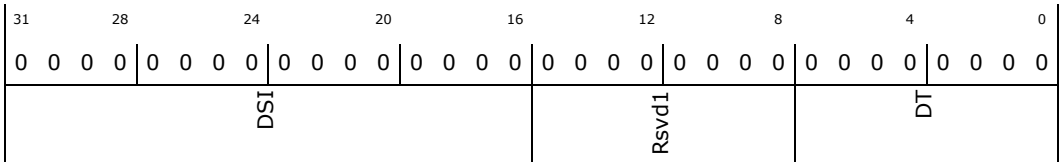
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3074h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.144 Door Bell 31 (DB30)—Offset 3078h

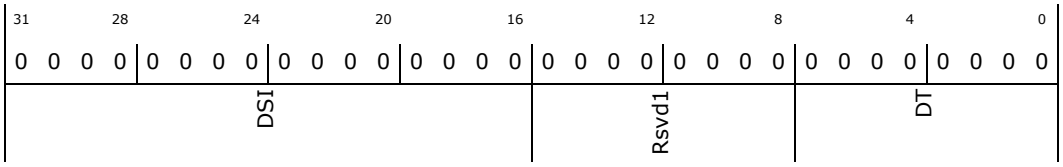
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3078h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.145 Door Bell 32 (DB31)—Offset 307Ch

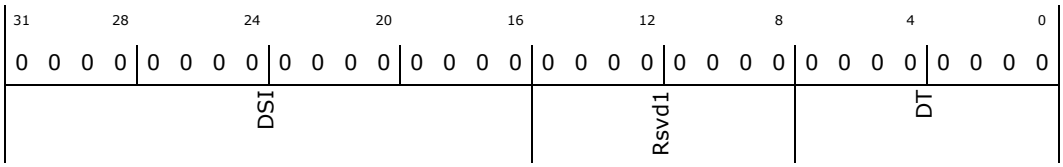
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 307Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.2.146 Door Bell 32 (DB32)—Offset 3080h

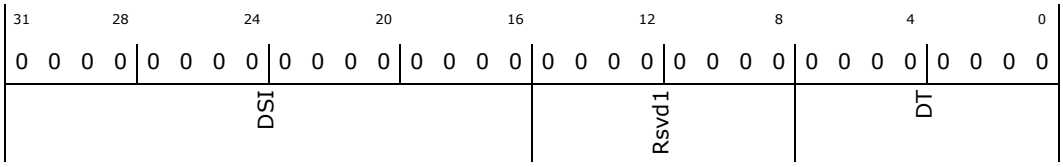
Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 3080h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

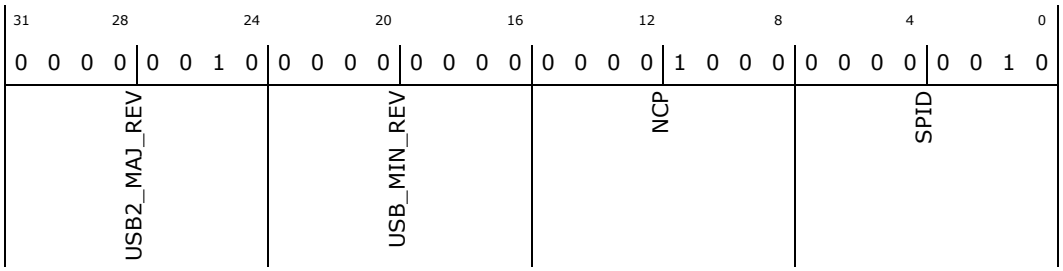
7.2.147 XECP_SUPP_USB2_0—Offset 8000h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8000h

Default: 02000802h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x2 RO	**USB Major Revision: 2.0 (USB2_MAJ_REV):** Reserved. **Power Well:** Core
23:16	0x0 RO	**USB Minor Revision (USB_MIN_REV):** Reserved. **Power Well:** Core
15:8	0x8 RO	**Next Capability Pointer (NCP):** **Power Well:** Core
7:0	0x2 RO	**Supported Protocol ID (SPID):** Reserved. **Power Well:** Core

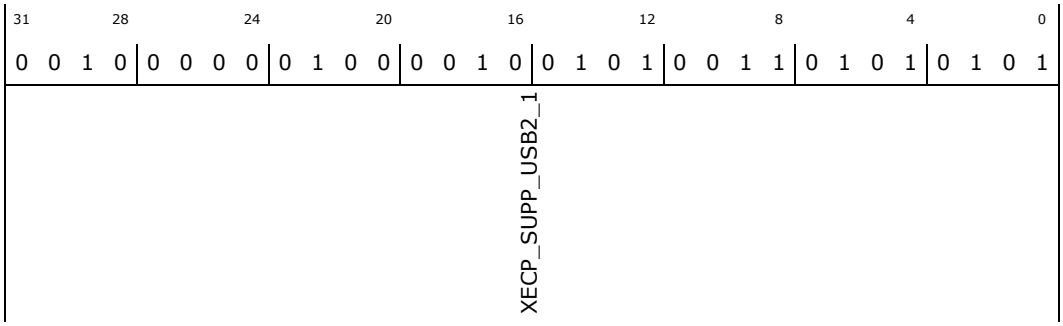
7.2.148 XECP_SUPP_USB2_1—Offset 8004h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8004h

Default: 20425355h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x20425355 RO	**XECP_SUPP_USB2_1:** Namestring USB **Power Well:** Core

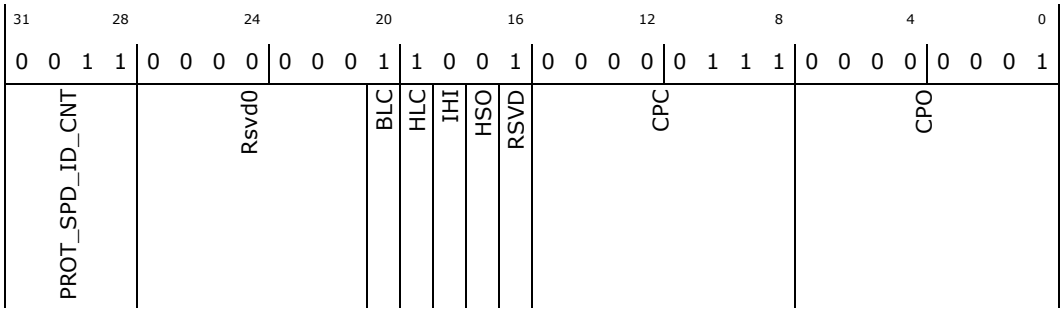
7.2.149 XECP_SUPP_USB2_2—Offset 8008h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8008h

Default: 30190701h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x3 RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT):** 3 USB 2.0 Speed (High, Full, Low) **Power Well:** Core
27:21	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
20	0x1 RO	**BESL LPM Capability (BLC):** Bit is set to 1 to indicate that the the ports described by this xHCI Supported Protocol Capability will apply BESL timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMCC registers. **Power Well:** Core
19	0x1 RO	**Protocol Defined - Hardware LMP Capability (HLC):** Reserved. **Power Well:** Core
18	0x0 RO	**Protocol Defined - Integrated Hub Implementation (IHI):** Reserved. **Power Well:** Core
17	0x0 RO	**Protocol Defined - High SPeed Only (HSO):** Reserved. **Power Well:** Core
16	0x1 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
15:8	0x7 RO	**Compatible Port Count (CPC):** **Power Well:** Core
7:0	0x1 RO	**Compatible Port Offset (CPO):** Reserved. **Power Well:** Core

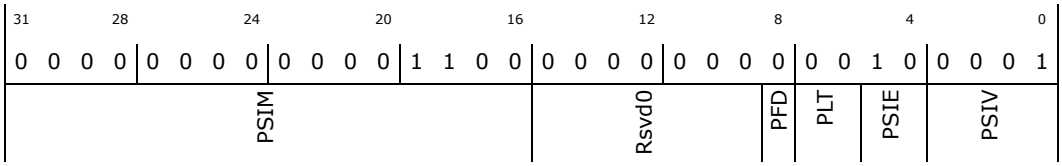
7.2.150 XECP_SUPP_USB2_3 (Full Speed) (XECP_SUPP_USB2_3)—Offset 8010h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8010h

Default: 000C0021h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xc RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x0 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	0x2 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x1 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

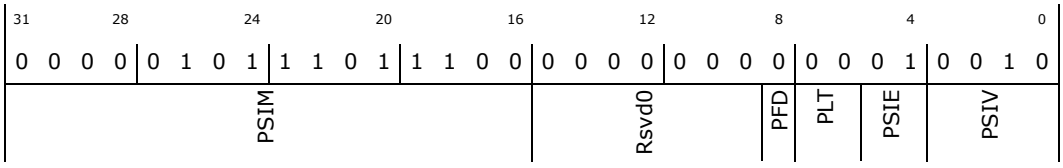
7.2.151 XECP_SUPP_USB2_4 (Low Speed) (XECP_SUPP_USB2_4)—Offset 8014h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8014h

Default: 05DC0012h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x5dc RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x0 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5:4	0x1 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x2 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

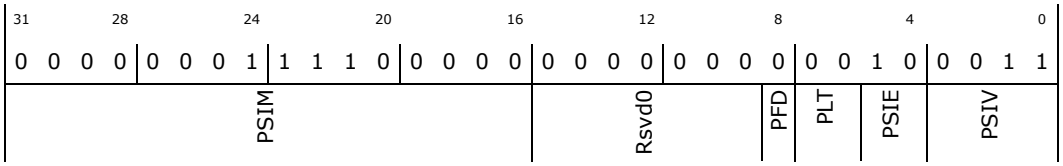
7.2.152 XECP_SUPP_USB2_5 (High Speed) (XECP_SUPP_USB2_5)—Offset 8018h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8018h

Default: 01E00023h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x1e0 RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x0 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	0x2 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x3 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

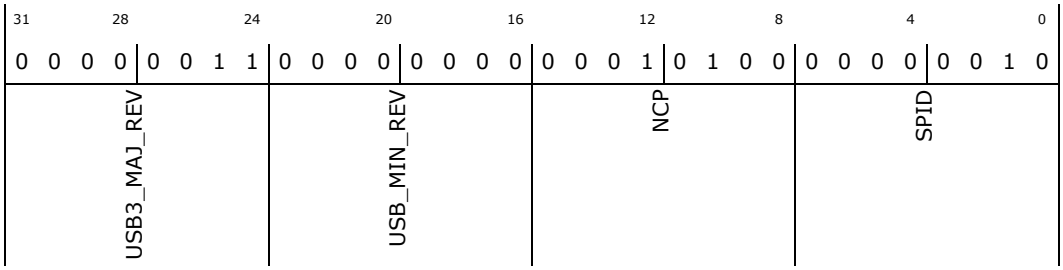
7.2.153 XECP_SUPP_USB3_0—Offset 8020h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8020h

Default: 03001402h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x3 RO	**USB Major Revision: 3.0 (USB3_MAJ_REV):** Reserved. **Power Well:** Core
23:16	0x0 RO	**USB Minor Revision (USB_MIN_REV):** Reserved. **Power Well:** Core
15:8	0x14 RO	**Next Capability Pointer (NCP):** Reserved. **Power Well:** Core
7:0	0x2 RO	**Supported Protocol ID (SPID):** Reserved. **Power Well:** Core

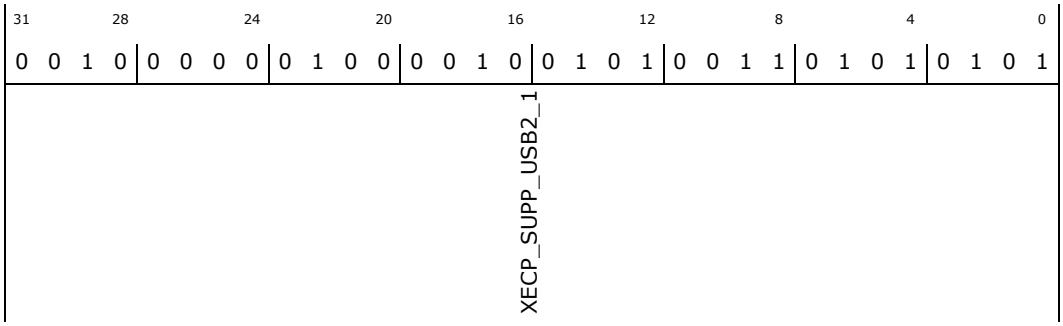
7.2.154 XECP_SUPP_USB3_1—Offset 8024h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8024h

Default: 20425355h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x20425355 RO	**XECP_SUPP_USB2_1:** Namestring USB **Power Well:** Core

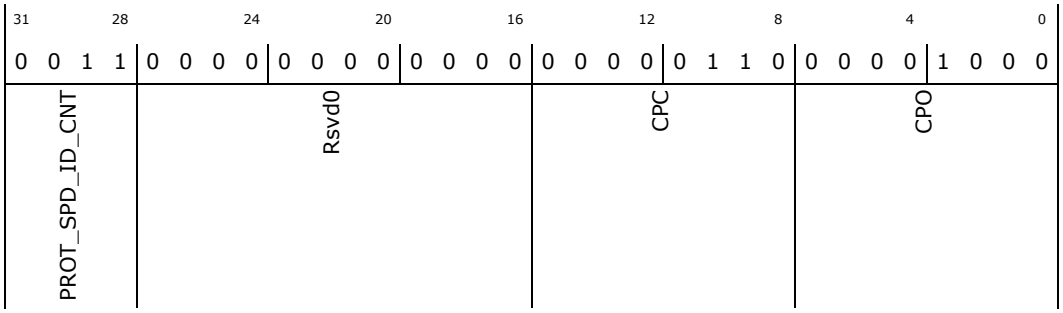
7.2.155 XECP_SUPP_USB3_2—Offset 8028h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8028h

Default: 30000608h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x3 RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT):** 1 USB 3.0 Speed (Supper Speed) **Power Well:** Core
27:16	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
15:8	0x6 RO	**Compatible Port Count (CPC):** **Power Well:** Core
7:0	0x8 RO	**Compatible Port Offset (CPO):** Reserved. **Power Well:** Core

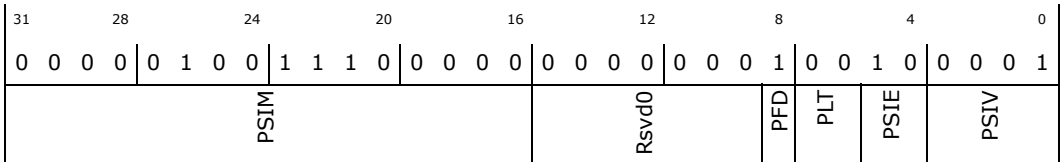
7.2.156 XECP_SUPP_USB3_3—Offset 8030h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8030h

Default: 04E00121h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x4e0 RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x1 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	0x2 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x1 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

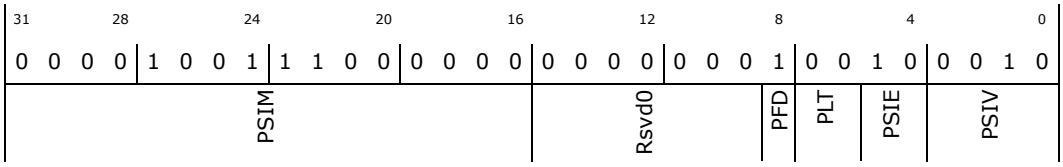
7.2.157 XECP_SUPP_USB3_4—Offset 8034h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8034h

Default: 09C00122h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x9c0 RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x1 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	0x2 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x2 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

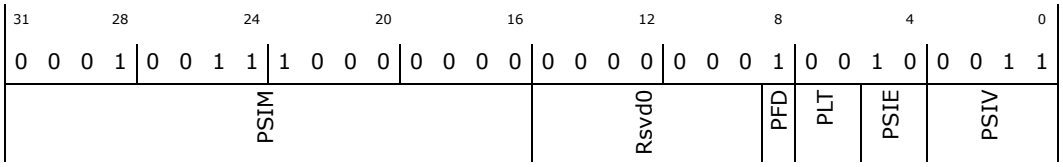
7.2.158 XECP_SUPP_USB3_5—Offset 8038h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8038h

Default: 13800123h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x1380 RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x1 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5:4	0x2 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x3 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

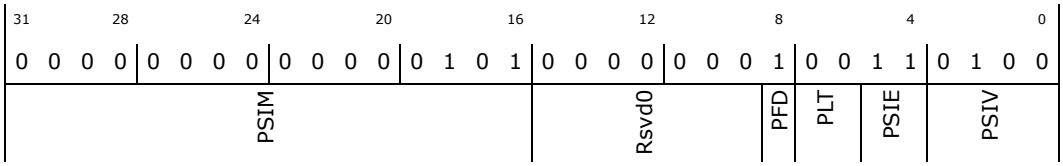
7.2.159 XECP_SUPP_USB3_6—Offset 803Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 803Ch

Default: 00050134h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x5 RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x1 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	0x3 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x4 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

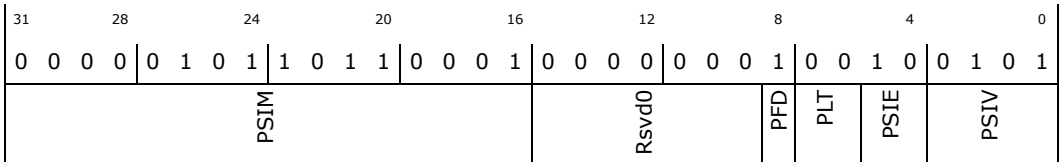
7.2.160 XECP_SUPP_USB3_7—Offset 8040h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8040h

Default: 05B10125h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x5b1 RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x1 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	0x2 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x5 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

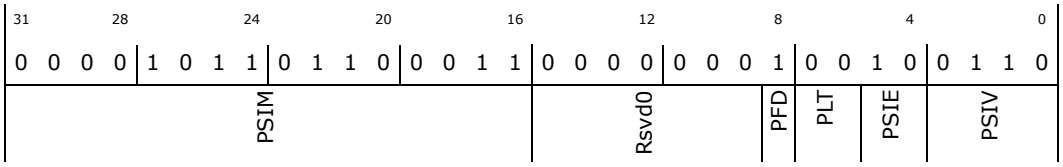
7.2.161 XECP_SUPP_USB3_8—Offset 8044h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8044h

Default: 0B630126h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xb63 RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x1 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	0x2 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x6 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

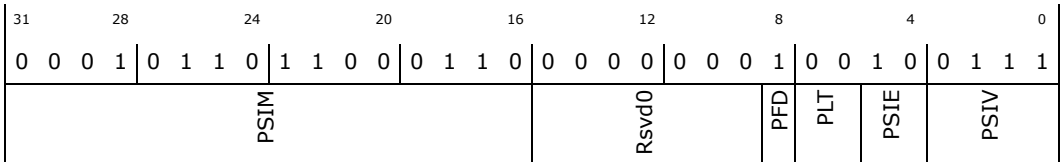
7.2.162 XECP_SUPP_USB3_9—Offset 8048h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8048h

Default: 16C60127h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x16c6 RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x1 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	0x2 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x7 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

7.2.163 Host Controller Capability (HOST_CTRL_CAP_REG)—Offset 8070h

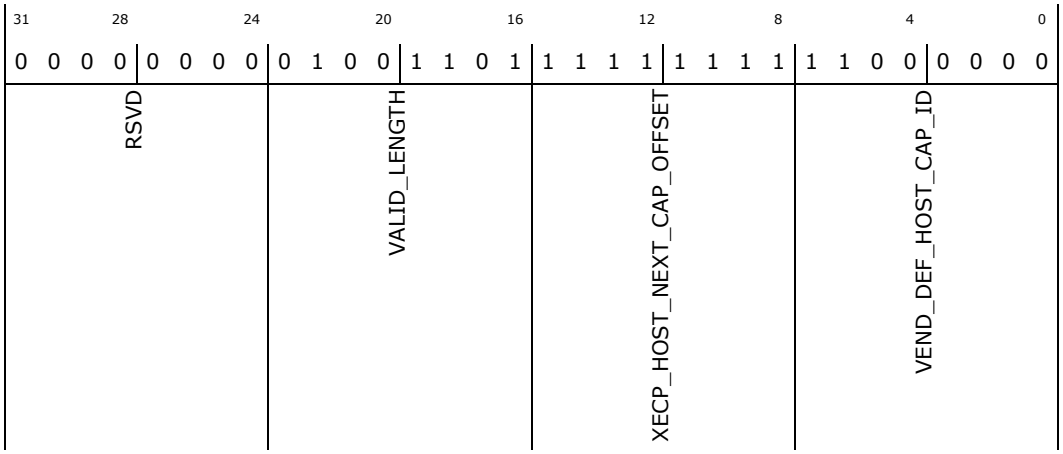
This is a register that describe the host controller the extended cap location. It includes the , XECP_HOST_NEXT_CAP_OFFSET and VEND_DEF_HOST_CAP_ID_192. This register is not subject to HW save and restore.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8070h

Default: 004DFFC0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
23:16	0x4d RO	**Valid Length (VALID_LENGTH):** Indicates the number of valid DWords in the capability, that need to be saved and restored This value needs to be updated as new chicken bit registers are added. 47h -) 818Bh is the last valid byte **Power Well:** Core
15:8	0xff RO	**Next Capability Pointer (XECP_HOST_NEXT_CAP_OFFSET):** Reserved. **Power Well:** Core
7:0	0xc0 RO	**Supported Protocol ID (VEND_DEF_HOST_CAP_ID):** Reserved. **Power Well:** Core

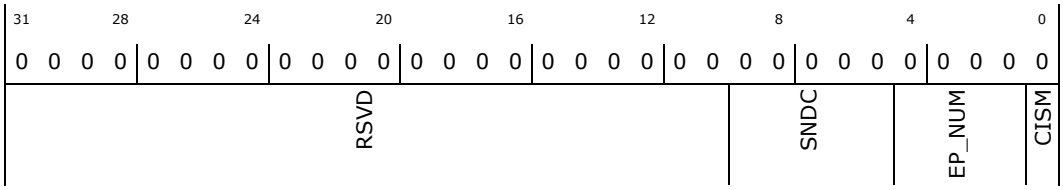
7.2.164 Override EP Flow Control (HOST_CLR_MASK_REG)—Offset 8078h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8078h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
9:5	0x0 RW	**Slot Number Default Config (SNDC):** 5bits of slot number as a default configuration. It can scale to max of 128 slots **Power Well:** Core
4:1	0x0 RW	**EP Number (EP_NUM):** 4bits of EP number **Power Well:** Core
0	0x0 RW	**Clear Internal Scheduler's Mask (CISM):** This is a register that is used to clear the internal scheduler's mask that is used to stop scheduling a particular EP. Bit0 indicates the direction of the EP **Power Well:** Core

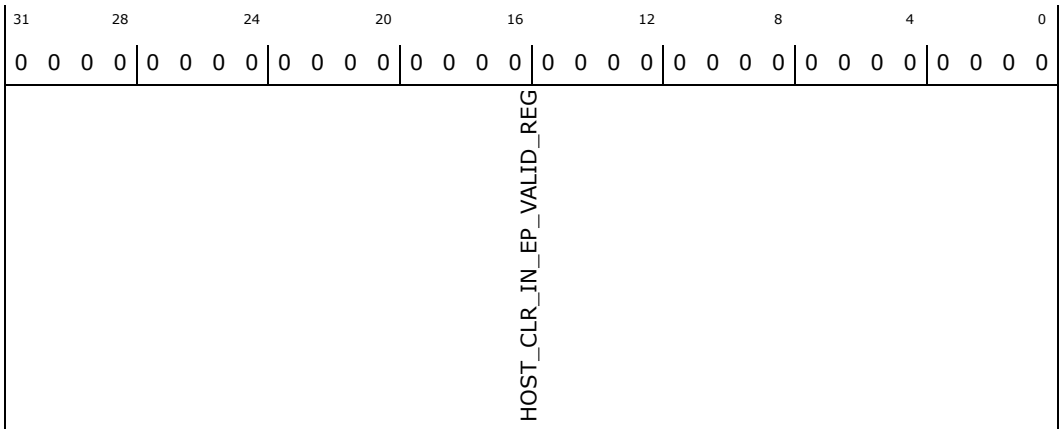
7.2.165 Clear Active IN EP ID Control (HOST_CLR_IN_EP_VALID_REG)—Offset 807Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 807Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Clear Active IN EP ID Control (HOST_CLR_IN_EP_VALID_REG):** This register is used to clear the internal valid IN EP array that TRM stored in order to guarantee one IN EP per port. This register allows software to clear the valid bit of each port IN EP. This field indicates the port number. For a 2port configuration, only bit1:0 are valid. It can scale for the max number of ports that we support. **Power Well:** Core

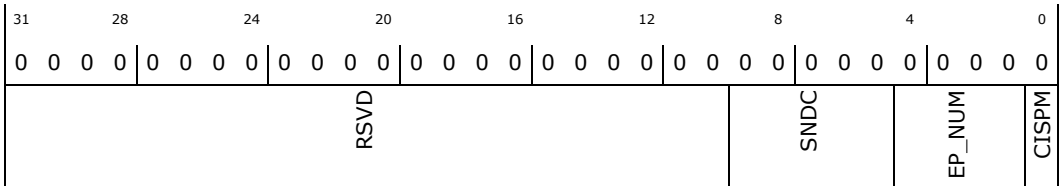
7.2.166 Clear Poll Mask Control (HOST_CLR_PMASK_REG)—Offset 8080h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8080h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
9:5	0x0 RW	**Slot Number Default Config (SNDC):** 5bits of slot number as a default configuration. It can scale to max of 128 slots **Power Well:** Core
4:1	0x0 RW	**EP Number (EP_NUM):** 4bits of EP number **Power Well:** Core
0	0x0 RW	**Clear Internal Scheduler's Poll Mask (CISPM):** This is a register that is used to clear the internal scheduler's poll mask that is used to indicate whether we need to poll this EP. This is used for USB2. Bit0 indicates the direction of the EP **Power Well:** Core

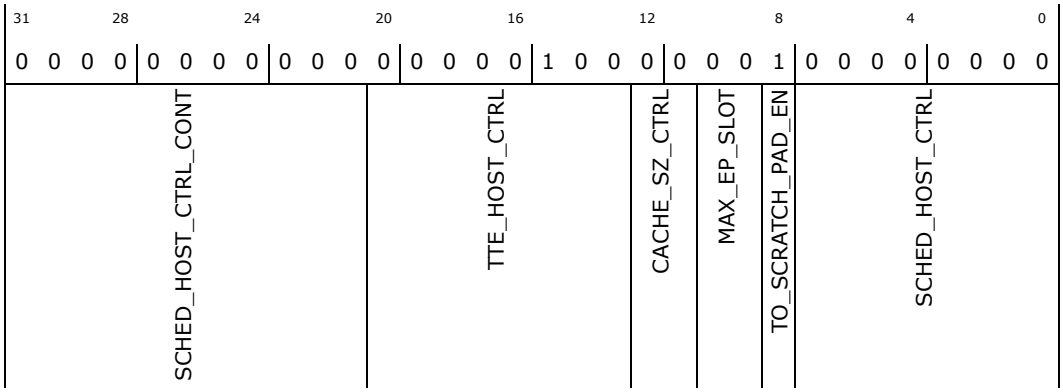
7.2.167 Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8094h

Default: 00008100h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RW	**Scheduler Host Control Reg Cont (SCHED_HOST_CTRL_CONT):** method of USB2 port periodic done check (off by default) **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
20:13	0x4 RW	**TTE Host Control (TTE_HOST_CTRL):** (0): disable interrupt complete split limit to 3 microframes (1): disable checking of missed microframes (2): disable split error request w/NULL pointer on speculative INs with data payload and no TRB. (3): disable deferred split error request on speculative IN with data payload and no TRB. (7:4): reserved **Power Well:** Core
12:11	0x0 RW	**Cache Size Control Reg (CACHE_SZ_CTRL):** 0: 64 1: 32 2,3: 16 **Power Well:** Core
10:9	0x0 RW	**Maximum EP Per Slot (MAX_EP_SLOT):** 0: 32 1: 16 2: 8 3: 4 **Power Well:** Core
8	0x1 RW	**Turn on scratch_pad_en (TO_SCRATCH_PAD_EN):** Reserved. **Power Well:** Core
7:0	0x0 RW	**Scheduler Host Control Reg (SCHED_HOST_CTRL):** (0): disable poll delay (1): disable TRM active in EP valid check (2): enable TTE overlap prevention on interrupt IN EPs (at cost of possible service interval slip) (3) enable TTE overlap prevention on interrupt OUT EPs (at cost of possible service interval slip) (5:4) scheduler sort pattern 00 (default) search ISO ahead of interrupt within each service interval 01 - search USB2-ISO, USB3-ISO, USB2-Interrupt, USB3-Interrupt within each service interval 10 - search strictly by interval 11 - search all ISO intervals ahead interrupt intervals and within each interval, USB2 ahead of USB3 (6): disable 1 pack scheduling limit when ISO pending in present microframe (7): enable check to stop scheduling on port that are not connected **Power Well:** Core

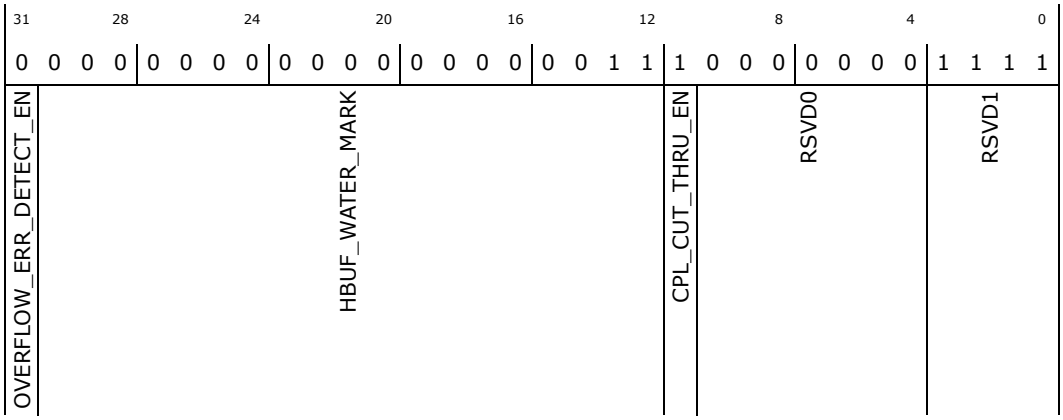
7.2.168 Global Port Control (HOST_CTRL_PORT_CTRL)—Offset 80A0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80A0h

Default: 0000380Fh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**OVERFLOW ERROR DETECTION ENABLE (OVERFLOW_ERR_DETECT_EN):** Reserved. **Power Well:** Core
30:12	0x3 RW	**HBUF_WATER_MARK:** Reserved. **Power Well:** Core
11	0x1 RW	**CPL Cut Thru Enable (CPL_CUT_THRU_EN):** Reserved. **Power Well:** Core
10:4	0x0 RW	**RESERVED (RSVD0):** Reserved. **Power Well:** Core
3:0	0xf RW	**RESERVED (RSVD1):** Reserved. **Power Well:** Core

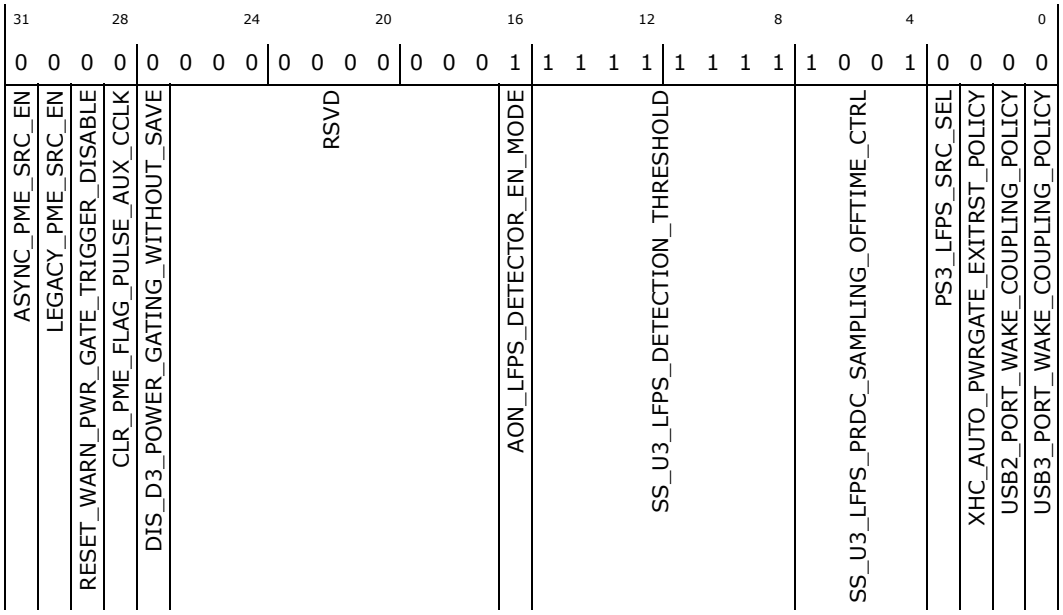
7.2.169 Power Management Control (PMCTRL_REG)—Offset 80A4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80A4h

Default: 0001FF90h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Async PME Source Enable (ASYNC_PME_SRC_EN):** This field allows the async PME source to be allowed to generate PME. This is specifically required for SOCs that do not allow for any clock other than RTC to be available during RTD3. **Power Well:** SUS
30	0x0 RW	**Legacy PME Source Enable (LEGACY_PME_SRC_EN):** This field allows the legacy PME source to be used in PME generation. The legacy source in in reference to the source prior to the RTD3 changes. **Power Well:** SUS
29	0x0 RW	**Reset Warn Power Gate Trigger Disable (RESET_WARN_PWR_GATE_TRIGGER_DISABLE):** This field controls the actions taken for due to reset warn. 0 - Reset Warn will trigger a HW autonomous Power Gate 1 - Reset Warn will not trigger a HW autonomous Power Gate **Power Well:** SUS
28	0x0 RW	**CLR_PME_FLAG_PULSE_AUX_CCLK:** Reserved. **Power Well:** SUS
27	0x0 RW	**DIS_D3_POWER_GATING_WITHOUT_SAVE:** Disable D3 Power Gating Without Save 0 D3 Power Gating is enabled 1 D3 Power Gating is disabled when Save is not done. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
26:17	0x0 RW	**RESERVED (RSVD):** Reserved. **Power Well:** SUS
16	0x1 RW	**AON LFPS Detector Enable Mode (AON_LFPS_DETECTOR_EN_MODE):** 1 - Allow the LFSP Detector in AON to own LFPS detection when the port is in PS3 for U2/U3 - not RxD regardless of port ownership. 0 - Allow the LFPS Detector in AON to own the LFPS detection only when the AON owns the port and in U2/U3 - not RxD **Power Well:** SUS
15:8	0xff RW	**SS U3 LFPS Detection Threshold (SS_U3_LFPS_DETECTION_THRESHOLD):** This field controls the threshold used to determine when a valid U3 Wake is detected through when using the unfiltered LFPS source. The value on this field will reflect the binary count required to have been detected on the counter being clocked by the unfiltered lfps source to result in a valid U3 wake detection. **Power Well:** SUS
7:4	0x9 RW	**SS_U3_LFPS_PRDC_SAMPLING_OFFTIME_CTRL:** This field controls the OFF time for the LFPS periodic sampling for USB3 Ports 0x0 periodic sampling is disabled. 0x1 OFF time is 1ms 0x2 OFF time is 2ms 0xF OFF time is 15ms The ON Time is determined by the amount of time required to reliably determine if there is a valid LFPS and is HW implementation specific. A speed up mode shall be implemented where this field is in units of us. i.e. 0x1 = 1 us OFF time, 0x2 = 2 us OFF time, etc. **Power Well:** SUS
3	0x0 RW	**PS3 LFPS Source Select (PS3_LFPS_SRC_SEL):** 0 LFPS Source is unfiltered 1 LFPS Source is filtered (Rx-Elec-Idle) LFPS Source is Rx-Elec-Idle for any non PS3 state. **Power Well:** SUS
2	0x0 RW	**XHCI Engine Autonomous Power Gate Exit Reset Policy (XHC_AUTO_PWRGATE_EXITRST_POLICY):** Controls when the xHCI engine is brought out of reset due to a power ungate. 0 Engine is brought out of reset when D3 to D0 is triggered. This allows for a quick power up sequence while leaving the virtual PCIe LTSSM in L23 is power ungate is not due to D3 to D0. 1 Engine is brought out of reset along with the rest of the IP. This is required for PMC save/restore flow. **Power Well:** SUS
1	0x0 RW	**USB2 Port Wake Unit Coupling Policy (USB2_PORT_WAKE_COUPLING_POLICY):** Controls the trigger for USB2 Port Wake Units to initiate Port Level Power Off Preparation. 0 RTD3 triggered 1 - Port Triggered when in L1, L2 or Disabled, Disconnected **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**USB3 Port Wake Unit Coupling Policy (USB3_PORT_WAKE_COUPLING_POLICY):** Controls the trigger for USB3 Port Wake Units to initiate Port Level Power Off Preparation. 0 - RTD3 Triggered 1 - Port Triggered when in PS3 due to RxDetect, U3, U2 or Disabled **Power Well:** SUS

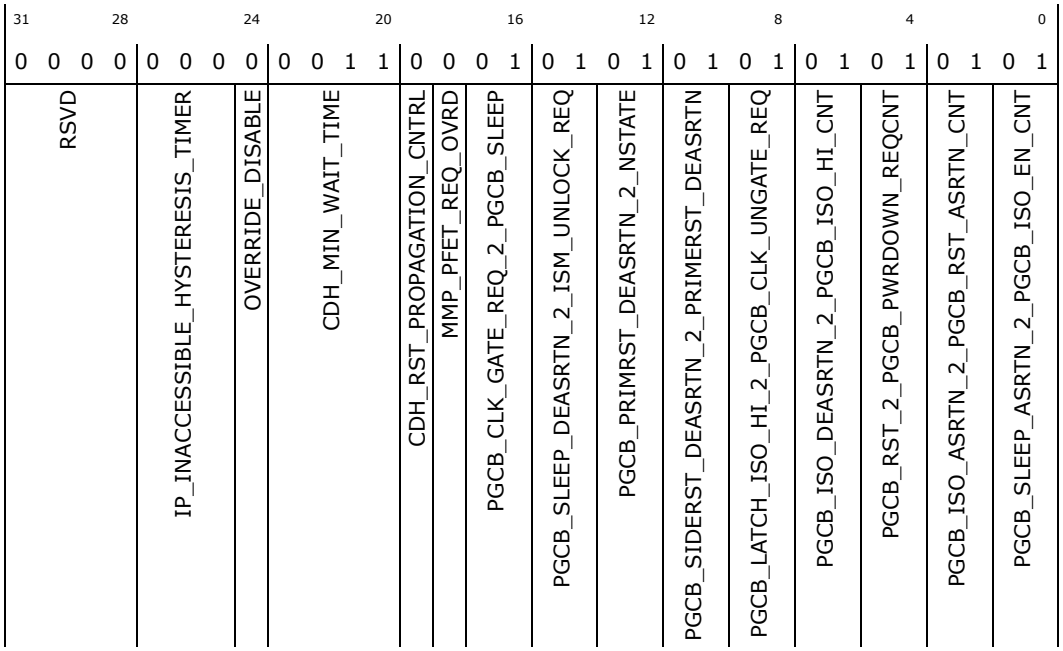
7.2.170 PGCB Control (PGCBCTRL_REG)—Offset 80A8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80A8h

Default: 00315555h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** SUS
27:25	0x0 RW	**IP_INACCESSIBLE_HYSTERESIS_TIMER:** 000 ? 50us 001 ? 100us 010 ? 150us 011 ? 200us 000 ? 250us 001 ? 300us 010 ? 350us 111 ? 400us **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
24	0x0 RW	**Override_Disable (OVERRIDE_DISABLE):** Reserved. **Power Well:** SUS
23:20	0x3 RW	**CDH Aggregation Minimum Wait Time (CDH_MIN_WAIT_TIME):** This field controls the minimum time that we must wait for resets to propagate before allowing Power Up flow to complete. The Power Up flow requires special handling of clocks, reset and sleep signaling which requires the CDH to monitor reset propagation. This timer allow for flexibility on when we consider all resets propagated. 0h Disabled 1h 2 clocks 2h 4 clocks 3h 8 clocks 4h 16 clocks 5h 32 clocks 6h 64 clocks 7h 128 clocks **Power Well:** SUS
19	0x0 RW	**RESERVED (CDH_RST_PROPAGATION_CNTRL):** This bit will indicate the mode of operation for the CDH Reset Propagation Aggregator. It allows for a mode where the aggregation will wait for an indication from each CDH before proceeding OR ignore the CDH indication before proceeding. Regardless of the mode, the aggregator will enforce the CDH Aggregation Mini Wait Time. 0 Aggregate all the CDH indications before triggering the CDH Aggregation Mini Wait Time. Once the Min Wait Time is met a notification to the Power Sequencer/Control will be initiated 1 Trigger the CDH Aggregation Mini Wait Time w/o waiting for CDH indication. Once the Min Wait time is met a notification to the Power Sequencer/Control will be initiated. **Power Well:** SUS
18	0x0 RW	**MMP_PFET_REQ_OVRD:** This bit will disable the MMP PFET request condition for PGCB control. 1 MMP PFET Request Ignored 0 Default **Power Well:** SUS
17:16	0x1 RW	**PGCB Clock Gate Request to PGCB Sleep (PGCB_CLK_GATE_REQ_2_PGCB_SLEEP):** Value representing the minimum number of delay clocks required between the assertion of pgcb_ip_clkgate_b to the deassertion of pgcb_sleep on PG exit. (This is only applicable for IP-Accessible PG with state-retention enabled.) Please see the description of cfg_tsleepact for more details. **Power Well:** SUS
15:14	0x1 RW	**PGCB Sleep Deassertion to PGCB ISM Unlock Req (PGCB_SLEEP_DEASRTN_2_ISM_UNLOCK_REQ):** For IP-Accessible PG (with state retention): Value representing the minimum number of delay clocks required between the deassertion of gcb_sleepto the deassertion of pgcb_ip_*_lock_req_b. For IP-Inaccessible PG (or with state-retention disabled): Value representing the minimum number of delay clocks required between the deassertion of pgcb_sleep to the deassertion of pgcb_isol_en_b. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
13:12	0x1 RW	**PGCB Prim Reset Deassertion to PGCB Next State (PGCB_PRIMRST_DEASRTN_2_NSTATE):** For IP-Accessible PG (with state retention): Value representing the minimum number of delay clocks required between the deassertion of pgcb_sleep to the deassertion of pgcb_ip_*_lock_req_b. For IP-Inaccessible PG (or with state-retention disabled): Value representing the minimum number of delay clocks required between the deassertion of pgcb_sleep to the deassertion of pgcb_isol_en_b. **Power Well:** SUS
11:10	0x1 RW	**PGCB Side Reset Deassertion to PGCB Prim Reset Deassertion (PGCB_SIDERST_DEASRTN_2_PRIMERST_DEASRTN):** Value representing the number of delay clocks required between the deassertion of gcb_force_rst_bto the deassertion of gcb_force_prim_rst_b (This is only applicable for IP-Accessible PG.) Please see the description of cfg_tsleepact for more details. **Power Well:** SUS
9:8	0x1 RW	**PGCB Latch Isolation High to PGCB Clock Ungate Request (PGCB_LATCH_ISO_HI_2_PGCB_CLK_UNGATE_REQ):** Value representing the number of delay clocks required between the assertion of pgcb_isol_latchen to the deassertion of pgcb_ip_clkgate_req_b. Please see the description of cfg_tsleepact for more details. **Power Well:** SUS
7:6	0x1 RW	**PGCB Isolation Deassertion to PGCB Latch Isolation High Count (PGCB_ISO_DEASRTN_2_PGCB_ISO_HI_CNT):** Value representing the minimum number of delay clocks required between the deassertion of pgcb_isol_en_b to the assertion of gcb_isol_latchen. Please see the description of cfg_tsleepact for more details. **Power Well:** SUS
5:4	0x1 RW	**PGCB Reset Assertion to PGCB Power Down Request Count (PGCB_RST_2_PGCB_PWRDOWN_REQCNT):** For IP-Accessible PG (with state retention): Value representing the minimum number of delay clocks required between the assertion of pgcb_force_prim_rst_b and pgcb_force_rst_b to the assertion of pgcb_pmc_pg_req_b. For IP-Inaccessible PG (or with state-retention disabled): Value representing the minimum number of delay clocks required between the assertion of pgcb_force_prim_rst_b and pgcb_force_rst_b to the assertion of pgcb_sleep. Please see the description of cfg_tsleepact for more details. **Power Well:** SUS
3:2	0x1 RW	**PGCB Isolation Assertion to PGCB Reset Assertion Count (PGCB_ISO_ASRTN_2_PGCB_RST_ASRTN_CNT):** Value representing the minimum number of delay clocks required between the assertion of gcb_isol_en_bto the assertion of gcb_force_prim_rst_band gcb_force_rst_b Please see the description of [1:0] for more details. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
1:0	0x1 RW	**PGCB Sleep Assertion to PGCB Isolation Enable Count (PGCB_SLEEP_ASRTN_2_PGCB_ISO_EN_CNT):** For IP-Accessible PG (with state retention): Value representing the minimum number of delay clocks required between the assertion of pgcb_sleep (and the deassertion of pgcb_isol_latchen) to the assertion of pgcb_isol_en_b. For IP-Inaccessible PG (or with state-retention disabled): Value representing the minimum number of delay clocks required between the deassertion of pgcb_isol_latchen to the assertion of pgcb_isol_en_b, as well as the minimum number of delay clocks required between the assertion of pgcb_sleep to the assertion of pgcb_pmc_pg_req_b. Common for all cfg_t* inputs: 0 1 clock 1 2 clocks 0 8 clocks 1 256 clocks For any of the cfg_t* inputs that an IP may feel are a don-care and the IP does not feel they will be useful for post-silicon debug, the recommendation is to tie the input to 201 (2 clocks). Otherwise, the inputs may be tied to another relevant value or connected to a configuration register. Note: These signals may only change while pgcb_pwrupidle is asserted, if pgcb_pwrupidle is deasserted it should be valid and stable. (It may change the same cycle that ip_pgcb_pg_rdy_req_b asserts.) **Power Well:** SUS

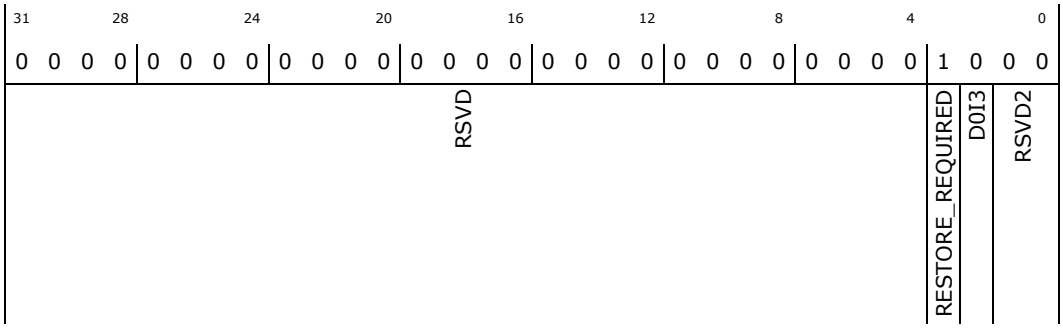
7.2.171 D0I3 Control (DOI3CTRL_REG)—Offset 80ACh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80ACh

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
3	0x1 RW/1C	**RestoreRequired (RESTORE_REQUIRED):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up. **Power Well:** SUS
2	0x0 RW	**D0I3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0). **Power Well:** SUS
1:0	0x0 RO	**RESERVED (RSVD2):** Reserved. **Power Well:** SUS

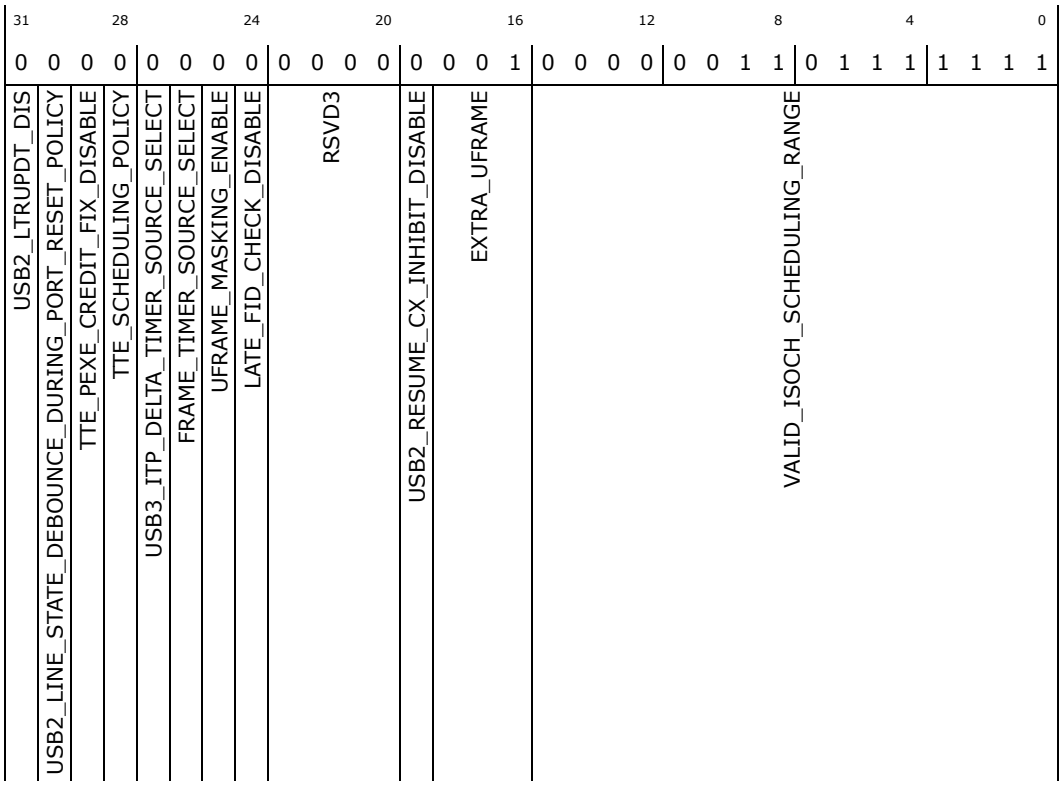
7.2.172 HOST_CTRL_MISC_REG—Offset 80B0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80B0h

Default: 0001037Fh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**USB2_LTRUPDT_DIS:** Reserved. **Power Well:** Core
30	0x0 RW	**USB2 Line State Debounce During Port Reset Policy (USB2_LINE_STATE_DEBOUNCE_DURING_PORT_RESET_POLICY):** This register controls how the debounce is enforced during the Port Reset phase. 0 do not enable the line state debounce during port reset. 1 enable the line state debounce during port reset. **Power Well:** Core
29	0x0 RW	**TTE PEXE Credit Fix Disable (TTE_PEXE_CREDIT_FIX_DISABLE):** When set, it disables a fix implemented to re-deem PEXE credits when a port is disconnected **Power Well:** Core
28	0x0 RW	**TTE Scheduling policy (TTE_SCHEDULING_POLICY):** This register controls a fix made to prevent over-scheduling by not account for 188B in each uFrame. Setting this bit will disable the fix and allow for over-scheduling. **Power Well:** Core
27	0x0 RW	**USB3 ITP Delta Timer Source Select (USB3_ITP_DELTA_TIMER_SOURCE_SELECT):** This register selects the source for the delta timer tracking used for ITP generation. 0 the source is a 16.666 ns tick generated from a crystal reference clock 1 - the source is a 16.666 ns tick generated from the aux_cclk. This field needs to remain in sync with Frame Timer Source Select to ensure the are both set or both cleared. There is no support for any other combination. **Power Well:** Core
26	0x0 RW	**Frame Timer Source Select (FRAME_TIMER_SOURCE_SELECT):** This register controls the source for the frame timer. 0 the source for the frame timer is a crystal reference clock 1 the source for the frame timer is the aux_cclk. **Power Well:** Core
25	0x0 RW	**uFrame Masking Enable (UFRAME_MASKING_ENABLE):** If set, enables the uFrame tick to be masked due to ports being in U3/NC. This controls a fix made to disable the auto masking of uFrame tick due to port state w/o any pipeline idle condition. When cleared, we rely on gating of frame timer due to proper port state and idleness tracking from the pipeline. **Power Well:** Core
24	0x0 RW	**Late FID Check Disable (LATE_FID_CHECK_DISABLE):** This register disables the Late FID Check performed when starting an ISOCH stream. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
23:20	0x0 RW	**RESERVED (RSVD3):** Reserved. **Power Well:** Core
19	0x0 RW	**USB2 Resume Cx Inhibit Disable (USB2_RESUME_CX_INHIBIT_DISABLE):** Controls if USB2 L1 Resume is allowed to contribute to DMA Active which will inhibit Cx state. 0 USB2 L1 Resume is allowed to inhibit Cx via DMA Active 1 USB2 L1 Resume is NOT allowed to inhibit Cx via DMA Active When cleared, Cx will only be inhibited when the DMA traffic for the port begins. **Power Well:** Core
18:16	0x1 RW	**Extra uFrame (EXTRA_UFRAME):** This register controls the extra number of uFrames added onto the advancing of late FID check. **Power Well:** Core
15:0	0x37f RW	**Valid Isoch Scheduling Range (VALID_ISOCH_SCHEDULING_RANGE):** This register defines the window in miliseconds from the current Frame that will be considered for scheduling in an upcoming Frame. Anything scheduled outside of this window will be considered as late and will trigger the Missed Service Error. **Power Well:** Core

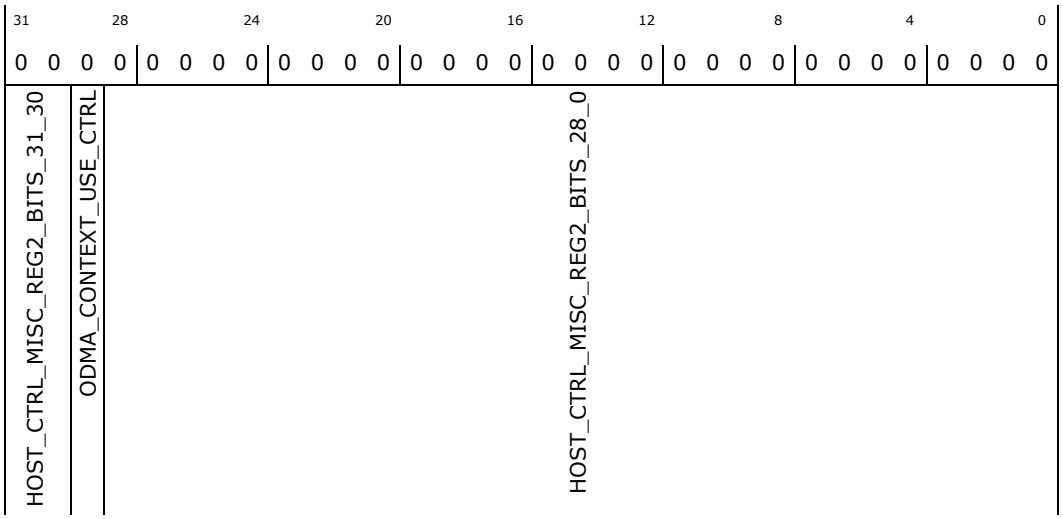
7.2.173 HOST_CTRL_MISC_REG2—Offset 80B4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80B4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**HOST_CTRL_MISC_REG2_BITS_31_30:** Reserved. **Power Well:** Core
29	0x0 RW	**ODMA_CONTEXT_USE_CTRL:** Reserved. **Power Well:** Core
28:0	0x0 RW	**HOST_CTRL_MISC_REG2_BITS_28_0:** Reserved. **Power Well:** Core

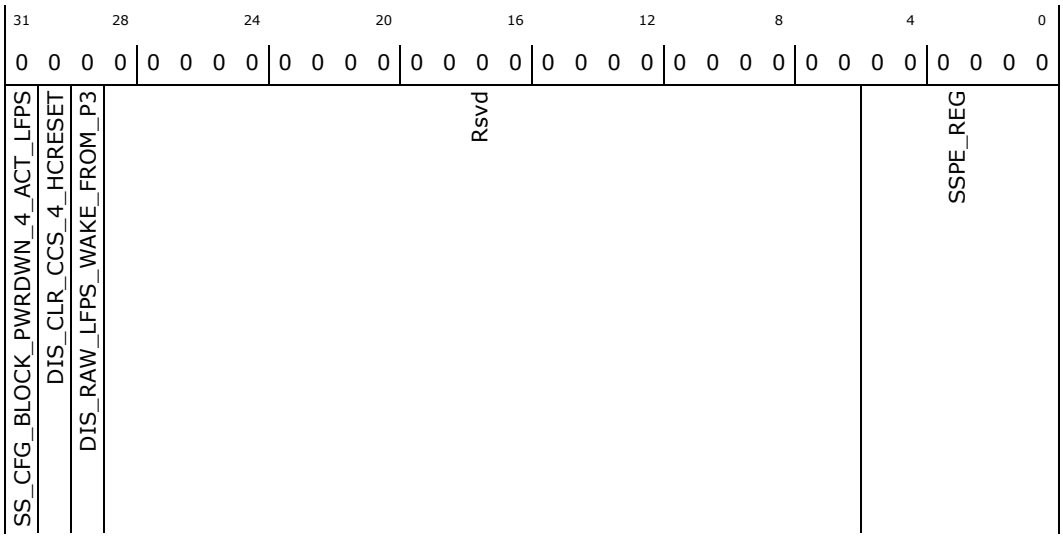
7.2.174 SSPE_REG—Offset 80B8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**ssCfgBlockPwrDwn4ActLFPS (SS_CFG_BLOCK_PWRDWN_4_ACT_LFPS):** Reserved. **Power Well:** SUS
30	0x0 RW	**dis_clr_ccs_4hcreset (DIS_CLR_CCS_4_HCRESET):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
29	0x0 RW	**DIS_RAW_LFPS_WAKE_FROM_P3:** This bit is used to disable RTL fix provided to separate RawLFPS and RxElecIDle detection Default 0: RTL fix is Enable 1 : Write to 1 to Disable the Fix **Power Well:** SUS
28:6	0x0 RO	**Rsvd:** Reserved. **Power Well:** SUS
5:0	0x0 RW	**SSPE_REG:** Reserved. **Power Well:** SUS

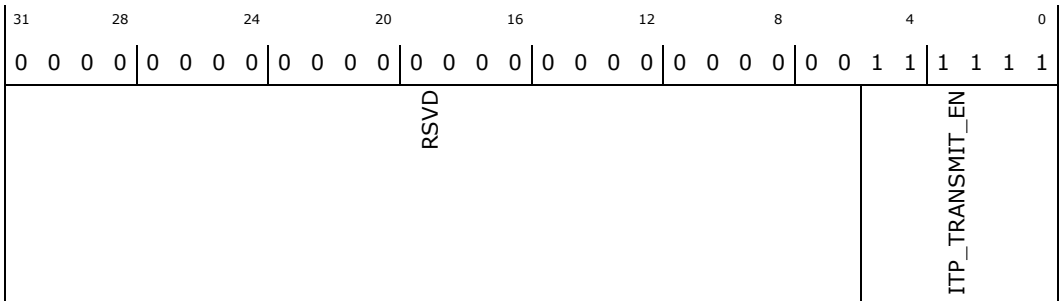
7.2.175 reg_SSPITPE_type (SSPITPE)—Offset 80BCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80BCh

Default: 0000003Fh



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**RSVD:** Reserved. **Power Well:** Core
5:0	0x3f RW	**ITP Transmit Enable (ITP_TRANSMIT_EN):** Width is scaled with USB3 Port Count PortCount=4 **Power Well:** Core

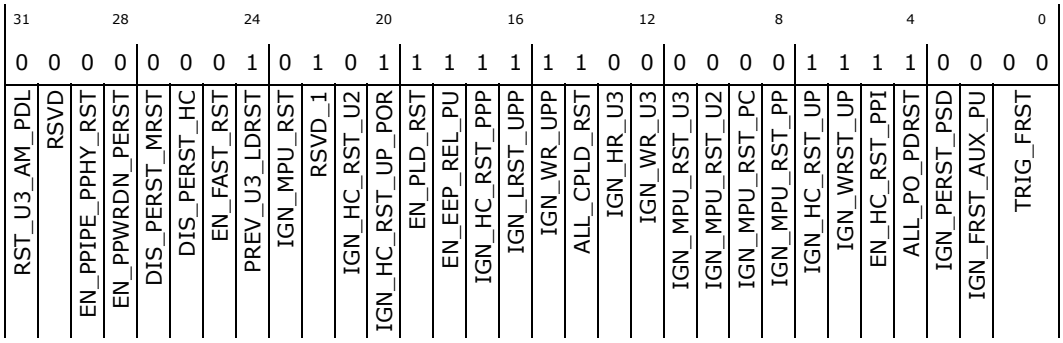
7.2.176 AUX Reset Control (AUX_CTRL_REG)—Offset 80C0h

Access Method

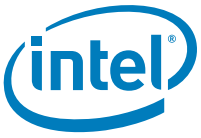
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80C0h

Default: 015FC0F0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Reset USB3 AUX/Main PD Logic (RST_U3_AM_PDL):** A reset that is designed to reset all USB3 port AUX + Main power domain logic. This is a debug function. It is called cold reset. Write 1 to this register will issue a cold reset to USB3 ports. **Power Well:** SUS
30	0x0 RW	**RESERVED (RSVD):** Reserved. **Power Well:** SUS
29	0x0 RW	**Enable PCIe PIPE Reset As PCIe PHY Reset (EN_PPIPE_PPHY_RST):** This bit set to 1 selects the PCIe PIPE reset as a PCIe PHY power on reset. 0 selects the AUX powerup reset as a PCIe PHY powerup reset. **Power Well:** SUS
28	0x0 RW	**Ensure PIPE Powerdown On PERST# (EN_PPWRDN_PERST):** This bit ensures any PERST# being asserted will cause PIPE powerdown state transition to P1. **Power Well:** SUS
27	0x0 RW	**Disable PERST# Main RST (DIS_PERST_MRST):** There is a feature where we only allow PERST# to be treated as a main powerdown reset when it is asserted during the state that is not in D3. This bit disables this feature when it is set to 1. If this bit is set to 1, it means that any PERST# will be treated as a main power domain reset regardless of its Dstate. **Power Well:** SUS
26	0x0 RW	**Disable PCIe PERST# Host Controller (DIS_PERST_HC):** There is a feature where we can disable PCIe PERST# from reset the host controller until power management control module has done its clock switching. This is for a case where PM entered L23 and immediately PERST# asserted. This bit is designed to enable this feature when set to 1. **Power Well:** SUS



Bit Range	Default & Access	Field Name (ID): Description
25	0x0 RW	**Enable Fast Simulation Reset Mode (EN_FAST_RST):** Enable a fast simulation mode for reset function. This is a feature for GLS **Power Well:** SUS
24	0x1 RW	**Prevent USB3 Link Down Reset (PREV_U3_LDRST):** When set to 1 prevent a reset being generated due to the USB3 port link down condition. **Power Well:** SUS
23	0x0 RW	**Ignore Main Power Up Reset (IGN_MPU_RST):** When set to 1 ignore the main power up reset for USB3 PIPE PHY reset. **Power Well:** SUS
22	0x1 RW	**RESERVED (RSVD_1):** Reserved. **Power Well:** SUS
21	0x0 RW	**Ignore HC Reset USB2 (IGN_HC_RST_U2):** When set to '1' ignore HC reset to reset the USB2 Port logic **Power Well:** SUS
20	0x1 RW	**Ignore HC Reset USB PHY (IGN_HC_RST_UP_POR):** When set to '1' ignore HC reset to the USB PHY power-on reset **Power Well:** SUS
19	0x1 RW	**Enable PCIe Link-Down Reset (EN_PLD_RST):** Enable a reset due to a PCIe link-down condition. The PCIe link down condition will cause a HC reset liked. If this bit is set 1, the PCIe link down condition will only reset the PCIe core. **Power Well:** SUS
18	0x1 RW	**Enable EEPROM Reload On Power Up (EN_EEP_REL_PU):** When set to '1' enable EEPROM reload on every main power-up **Power Well:** SUS
17	0x1 RW	**Ignore HC Reset PCIe PHY PIPE (IGN_HC_RST_PPP):** When set to '1' ignore HC reset to the PCIe PHY PIPE reset **Power Well:** SUS
16	0x1 RW	**Ignore LTSSM Reset USB PHY PIPE (IGN_LRST_UPP):** When set to '1' ignore the LTSSM of USB link state transition caused reset to USB PHY PIPE reset **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
15	0x1 RW	**Ignore Warm Reset USB PHY Power (IGN_WR_UPP):** When set to '1' ignore warm reset the USB PHY power on reset **Power Well:** SUS
14	0x1 RW	**Allow Core PCIe Link Down Reset (ALL_CPLD_RST):** When set to '1' allow PCIe link down to cause a reset to the rest of the core **Power Well:** SUS
13	0x0 RW	**Ignore Hot Reset USB3 (IGN_HR_U3):** When set to '1' ignore hot reset to the USB3 port logic **Power Well:** SUS
12	0x0 RW	**Ignore Warm Reset USB3 (IGN_WR_U3):** When set to '1' ignore warm reset to the USB3 port logic **Power Well:** SUS
11	0x0 RW	**Ignore Main Power Up Reset USB3 (IGN_MPU_RST_U3):** When set to '1' ignore main power up reset to USB3 port logic **Power Well:** SUS
10	0x0 RW	**Ignore Main Power Up Reset USB2 (IGN_MPU_RST_U2):** When set to '1' ignore main power up reset to USB2 port logic **Power Well:** SUS
9	0x0 RW	**Ignore Main Power Up Reset PCIe Core (IGN_MPU_RST_PC):** When set to '1' ignore main power up reset to PCIe core **Power Well:** SUS
8	0x0 RW	**Ignore Main Power Up Reset PCIe PHY (IGN_MPU_RST_PP):** When set to '1' ignore main power up reset to PCIe PHY **Power Well:** SUS
7	0x1 RW	**Ignore HC Reset USB PHY (IGN_HC_RST_UP):** When set to '1' ignore HC reset to the USB PHY **Power Well:** SUS
6	0x1 RW	**Ignore Warm Reset USB PHY (IGN_WRST_UP):** When set to '1' ignore warm reset to the USB PHY **Power Well:** SUS
5	0x1 RW	**Enable HC Reset Per Port Isolation (EN_HC_RST_PPI):** Enables the HC reset or per port reset isolation function **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
4	0x1 RW	**Allow Power Off Power Domain Reset (ALL_PO_PDRST):** When set to '1' allow main power off condition to trigger a main power domain reset **Power Well:** SUS
3	0x0 RW	**Ignore Wait For PERST# During Power Show Down (IGN_PERST_PSD):** When set to '1' ignore waiting for PERST# deassertion during main power show down. **Power Well:** SUS
2	0x0 RW	**Ignore Fundamental Reset During AUX Power Up (IGN_FRST_AUX_PU):** When fundamental reset is asserted during AUX power up, if this bit is set, then we will ignore PERST# such that purely wait for timeout to deassert fundamental reset. **Power Well:** SUS
1:0	0x0 RW	**Trigger Fundamental Reset (TRIG_FRST):** Writing to bit(1:0) to value of 2'b11 will cause a fundamental reset **Power Well:** SUS

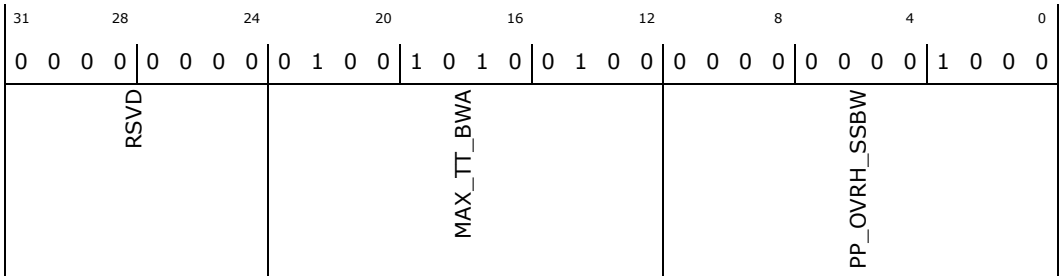
7.2.177 Super Speed Bandwidth Overload (HOST_BW_OV_SS_REG)—Offset 80C4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80C4h

Default: 004A4008h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
23:12	0x4a4 RW	**Max. TT BW Allowed (MAX_TT_BWA):** see white paper **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11:0	0x8 RW	**Per Packet Overhead SS BW (PP_OVRH_SSBW):** BW calculation: Overhead per packet for SS BW calculations. see white paper. **Power Well:** Core

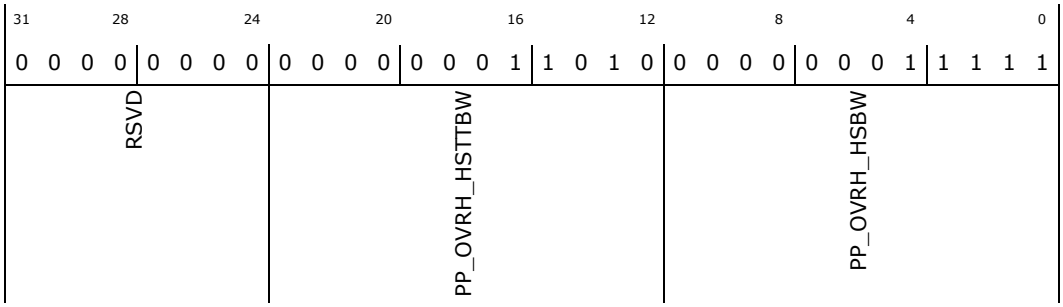
7.2.178 High Speed TT Bandwidth Overload (HOST_BW_OV_HS_REG)—Offset 80C8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80C8h

Default: 0001A01Fh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
23:12	0x1a RW	**Per Packet Overhead HS-TT BW (PP_OVRH_HSTTBW):** BW calculation: Overhead per packet for HS-TT BW calculations. see white paper. **Power Well:** Core
11:0	0x1f RW	**Per Packet Overhead HS BW (PP_OVRH_HSBW):** BW calculation: Overhead per packet for HS BW calculations. see white paper. **Power Well:** Core

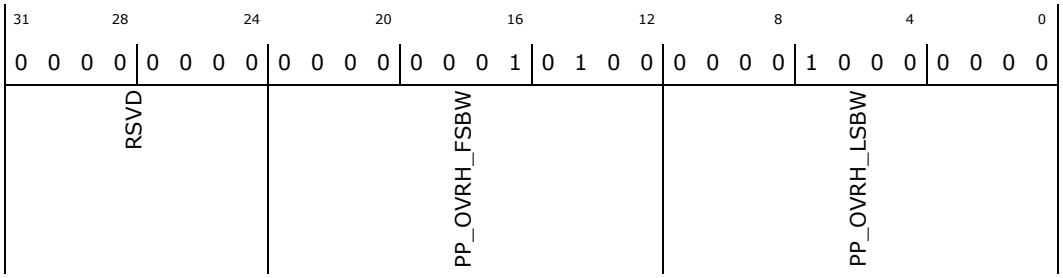
7.2.179 Bandwidth Overload Full Low Speed (HOST_BW_OV_FS_LS_REG)—Offset 80CCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80CCh

Default: 00014080h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
23:12	0x14 RW	**Per Packet Overhead FS BW (PP_OVRH_FSBW):** BW calculation: Overhead per packet for FS BW calculations. see white paper. **Power Well:** Core
11:0	0x80 RW	**Per Packet Overhead LS BW (PP_OVRH_LSBW):** BW calculation: Overhead per packet for LS BW calculations. see white paper. **Power Well:** Core

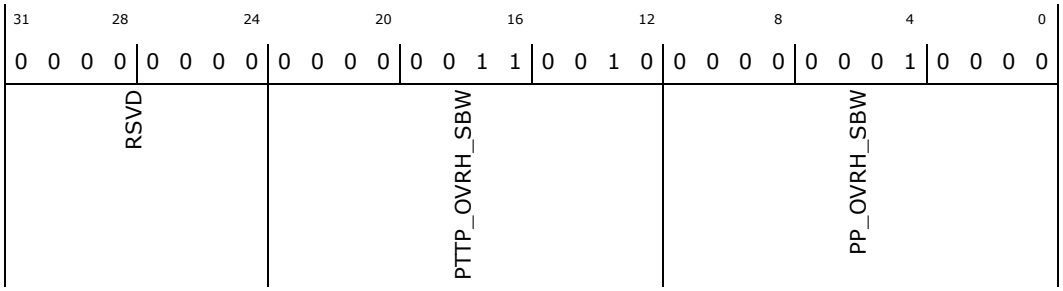
7.2.180 System Bandwidth Overload (HOST_BW_OV_SYS_REG)—Offset 80D0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80D0h

Default: 00032010h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
23:12	0x32 RW	**Per TT Packet Overhead System BW (PTTP_OVRH_SBW):** BW calculation: Overhead per TT packet for System BW calculations. see white paper. **Power Well:** Core
11:0	0x10 RW	**Per Packet Overhead System BW (PP_OVRH_SBW):** BW calculation: Overhead per packet for System BW calculations. see white paper. **Power Well:** Core

7.2.181 Scheduler Async Delay (HOST_CTRL_SCH_ASYNC_DELAY_REG)—Offset 80D4h

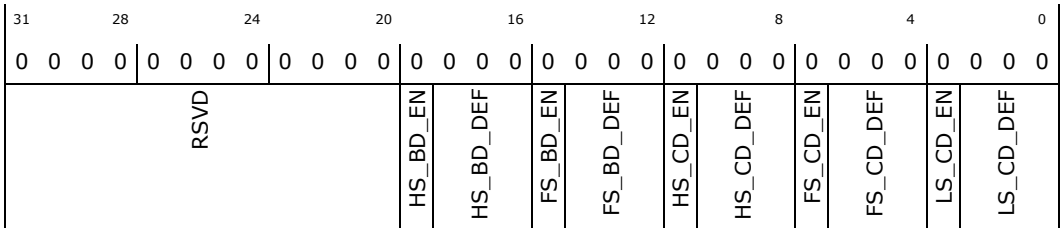
Global defaults for inserting delays between packets in the scheduler for async. types.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80D4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
19	0x0 RW	**High-Speed Bulk Delay Enable (HS_BD_EN):** Reserved. **Power Well:** Core
18:16	0x0 RW	**High-Speed Bulk Delay Default (HS_BD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...) **Power Well:** Core
15	0x0 RW	**Full-Speed Bulk Delay Enable (FS_BD_EN):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14:12	0x0 RW	**Full-Speed Bulk Delay Default (FS_BD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...) **Power Well:** Core
11	0x0 RW	**High-Speed Control Delay Enable (HS_CD_EN):** Reserved. **Power Well:** Core
10:8	0x0 RW	**High-Speed Control Delay Default (HS_CD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...) **Power Well:** Core
7	0x0 RW	**Full-Speed Control Delay Enable (FS_CD_EN):** Reserved. **Power Well:** Core
6:4	0x0 RW	**Full-Speed Control Default (FS_CD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...) **Power Well:** Core
3	0x0 RW	**Low-Speed Control Delay Enable (LS_CD_EN):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Low-Speed Control Delay Default (LS_CD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...) **Power Well:** Core

7.2.182 DEVICE MODE CONTROL REG 0 (DUAL_ROLE_CFG_REG0)—Offset 80D8h

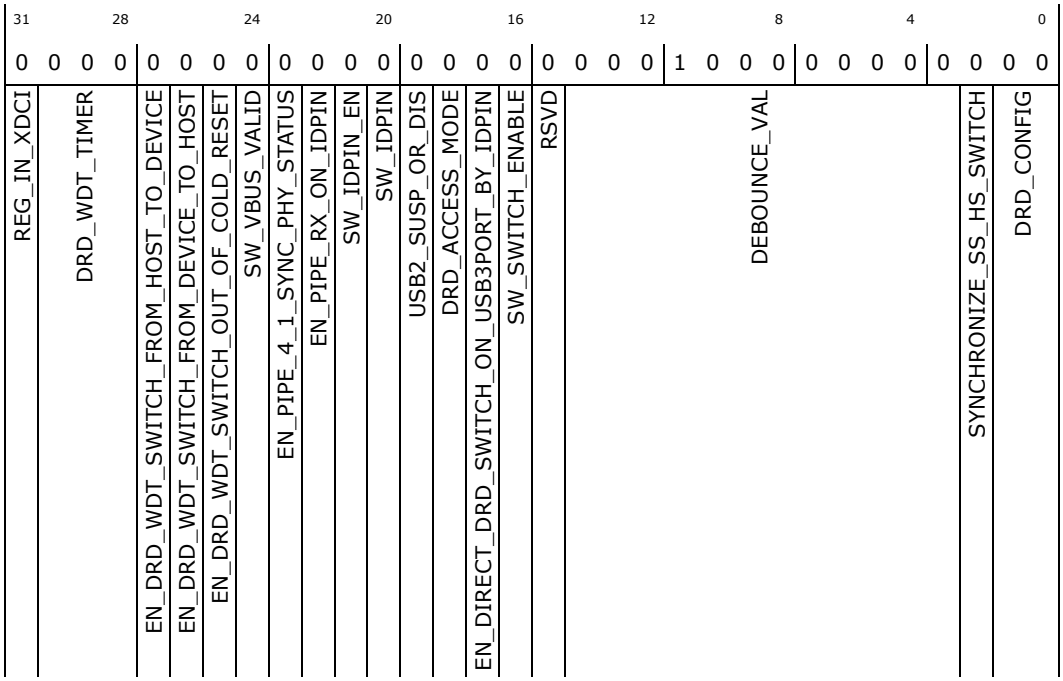
All bits in this register must be in the Always ON Power domain (ungated SUS or AON as appropriate)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80D8h

Default: 00000800h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**XDCI_DRD_CTRL_EN (REG_IN_XDCI):** When DRD_ACCESS_MODE (bit 18) =1, 0 -- The policies below is controlled by register in the XHCI MMIO 1 -- The policies below is controlled by register in the XDCI MMIO When DRD_ACCESS_MODE =0, this bit is a don't care. **Power Well:** SUS
30:28	0x0 RW	**DRD_WDT_TIMER:** 0-based incremental of 500ms **Power Well:** SUS
27	0x0 RW	**EN_DRD_WDT_SWITCH_FROM_HOST_TO_DEVICE:** Reserved. **Power Well:** SUS
26	0x0 RW	**EN_DRD_WDT_SWITCH_FROM_DEVICE_TO_HOST:** Reserved. **Power Well:** SUS
25	0x0 RW	**EN_DRD_WDT_SWITCH_OUT_OF_COLD_RESET:** Reserved. **Power Well:** SUS
24	0x0 RW	**SW_VBUS_VALID:** if SW_IDPIN_EN (bit 21) is 1, 0 ? deassert sw vbus valid 1 ? assert sw vbus valid **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
23	0x0 RW	**EN_PIPE_4_1_SYNC_PHY_STATUS:** Reserved. **Power Well:** SUS
22	0x0 RW	**EN_PIPE_RX_ON_IDPIN:** During the connection to a device, there may be a delay in DRD switch from XDCI to XHCI mode,the rx term can be low after idpin deasserts. If this bit is 0, the rx term will be assert immediately after idpin toggle. Otherwise, the device may fall back to USB2 mode. 1 -- drive 0s on utmi rx signals to controller if not connected. **Power Well:** SUS
21	0x0 RW	**SW_IDPIN_EN:** SW_IDPIN_EN 1 -- enable SW id pin (pre DRD) 0 -- disable SW id pin. **Power Well:** SUS
20	0x0 RW	**SW_IDPIN:** if SW_IDPIN_EN (bit 21) is 1, 0 - host mode 1 - device mode **Power Well:** SUS
19	0x0 RW	**USB2_SUSP_OR_DIS:** 1 - The DRD UTMI suspendm will be controlled by host/device based on the DRD switch. 0 - whenever device or host deassert suspendm, the DRD UTMI suspendm will be deasserted. **Power Well:** SUS
18	0x0 RW	**DRD_ACCESS_MODE:** 0 - The DUAL_ROLE register from host and device are ORed to control DRD 1 - The DUAL_ROLE register from host and device are selected by XDCI_DRD_CTRL_EN (bit 31) to control DRD **Power Well:** SUS
17	0x0 RW	**EN_DIRECT_DRD_SWITCH_ON_USB3PORT_BY_IDPIN:** 0 enable the direct DRD switch on USB3 port by idpin 1 disable the direct DRD switch **Power Well:** SUS
16	0x0 RW	**SW_SWITCH_ENABLE:** SW switch enable 0 (default) ID pin HW controlled DRD. 1 -- SW controlled DRD (ignore idpin), switch based on the DRD_CONFIG. **Power Well:** SUS
15	0x0 RW	**RSVD:** Reserved. **Power Well:** SUS
14:3	0x100 RW	**DEBOUNCE_VAL:** ID ping debounce timer (DEBOUNCE_VAL): in the unit of RTC clock (33us) default to 8.448 ms **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**SYNCHRONIZE_SS_HS_SWITCH:** Synchronize the SS and HS switch: 0 (default) Does not synchronize. i.e. HS switch on the debounced id pin, while SS switch independently controlled by the sequencer. 1 synchronize HS and SS switch. Both speeds switch when sequencer switch. **Power Well:** SUS
1:0	0x0 RW	**DRD_CONFIG:** 00 Dynamic DRD switch mode 01 static host mode 10 static device mode 11 -- reserved **Power Well:** SUS

7.2.183 DEVICE MODE CONTROL REG 1 (DUAL_ROLE_CFG_REG1)—Offset 80DCh

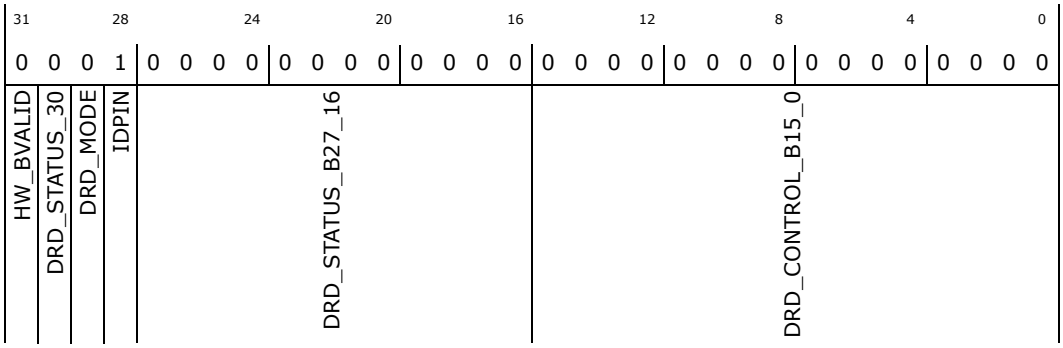
All bits in this register must be in the Always ON Power domain (ungated SUS or AON as appropriate)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80DCh

Default: 10000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**BVALID_HW (HW_BVALID):** hardware bvalid **Power Well:** SUS
30	0x0 RO	**DRD_STATUS_B31_30 (DRD_STATUS_30):** Reserved. **Power Well:** SUS
29	0x0 RO	**DRD_MODE:** SS DRD mode 0 device mode 1 host mode **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
28	0x1 RO	**IDPIN:** IDPIN value hw version **Power Well:** SUS
27:16	0x0 RO	**DRD_STATUS_B27_16:** Reserved. **Power Well:** SUS
15:0	0x0 RW	**DRD_CONTROL_B15_0:** Reserved. **Power Well:** SUS

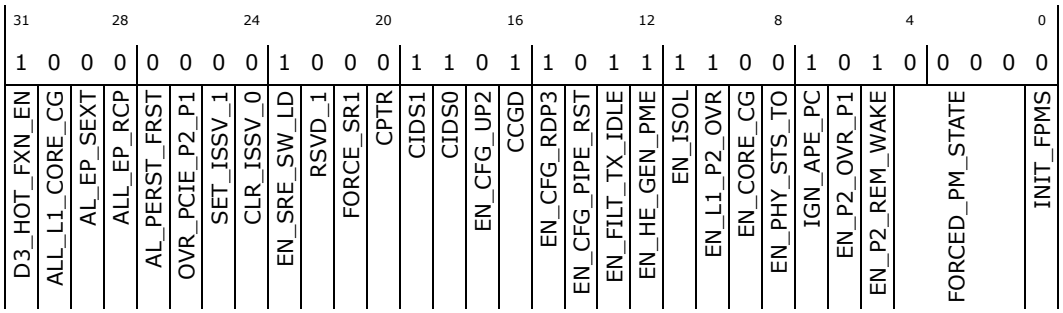
7.2.184 AUX Power Management Control (AUX_CTRL_REG1)—Offset 80E0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

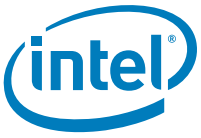
Offset: [MBAR] + 80E0h

Default: 808DBCA0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**D3 Hot function enable register (D3_HOT_FXN_EN):** This bit is from pin input which is set 1. But we allow software to alter it if it is needed. 1: D3 hot enabled 0: D3 hot not abled. **Power Well:** SUS
30	0x0 RW	**Allow L1 Core Clock Gating (ALL_L1_CORE_CG):** When set to 1 allows core clock being gated during L1 state. **Power Well:** SUS
29	0x0 RW	**Allow Engine PHY Status Extension (AL_EP_SEXT):** When set to 1 allows the engine to extend PHY status of PCIe PIPE for one more cycle. This is due to the fact that our rate change function has a potential of not being able to sample the phystatus signal. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
28	0x0 RW	**Allow Engine PCIe Rate Change Passing (ALL_EP_RCP):** When set to 1 allows the engine to pass PCIe rate change signal as it is from PCIe core to PCIe PHY. **Power Well:** SUS
27	0x0 RW	**Allow Engine PERST Fundamental Reset (AL_PERST_FRST):** When set to 1 allow engine to treat PERST# as a fundamental reset **Power Well:** SUS
26	0x0 RW	**Overwrite PCIe P2 to P1 (OVR_PCIE_P2_P1):** When set to 1 will overwrite a PCIe powerdown state of P2 to P1. **Power Well:** SUS
25	0x0 RW	**Set Internal SSV 1 (SET_ISSV_1):** When set to 1 set the internal SSV to 1. **Power Well:** SUS
24	0x0 RW	**Clear Internal SSV 0 (CLR_ISSV_0):** When set to 1 clear the internal SSV to 0. **Power Well:** SUS
23	0x1 RW	**Enable save_restore_enable SW Loading (EN_SRE_SW_LD):** This is a bit that enables the save_restore_enable signal being loaded when a software command has set Save bit. This is a debug function. **Power Well:** SUS
22	0x0 RW	**RESERVED (RSVD_1):** Reserved. **Power Well:** SUS
21	0x0 RW	**Force save_restore 1 (FORCE_SR1):** When set to 1, it will force the save_restore flag to 1. This flag is an bit to ensure that we have masked the update during low power state. If software write this bit to 1, it must write it to 0 in order to resume the normal save and restore function. **Power Well:** SUS
20	0x0 RW	**cfg pcie txreg rd (CPTR):** Reserved. **Power Well:** SUS
19	0x1 RW	**cfg iob drivestrength[1] (CIDS1):** Reserved. **Power Well:** SUS
18	0x1 RW	**cfg iob drivestrength[0] (CIDS0):** Reserved. **Power Well:** SUS



Bit Range	Default & Access	Field Name (ID): Description
17	0x0 RW	**Enable CFG USB P2 (EN_CFG_UP2):** When set to '1' enable cfg usb p2 **Power Well:** SUS
16	0x1 RW	**cfg clk gate dis (CCGD):** Reserved. **Power Well:** SUS
15	0x1 RW	**Enable CFG RXDET P3 (EN_CFG_RDP3):** When set to '1' enable cfg rxdet p3 **Power Well:** SUS
14	0x0 RW	**Enable CFG PIPE Reset (EN_CFG_PIPE_RST):** When set to '1' enable cfg pipe rst **Power Well:** SUS
13	0x1 RW	**Enable Filter TX Idle (EN_FILT_TX_IDLE):** When set to 1 enables a filter function to TX electrical idle signal at PCie PIPE. We have a filter that will set TXelecidle signal of PCIe PIPE to 1 whenever we are in isolation state or power down transition states. **Power Well:** SUS
12	0x1 RW	**Enable Host Engine Generate PME (EN_HE_GEN_PME):** This is a global switch to whether or not enable this host engine to generate PME message. **Power Well:** SUS
11	0x1 RW	**Enable Isolation (EN_ISOL):** When set to '1' enable isolation **Power Well:** SUS
10	0x1 RW	**Enable L1 Caused P2 Overwrite (EN_L1_P2_OVR):** Set 1 to enable a new feature. This new feature is designed to use L1 as a state to identify whether we should do P2 Overwrite or not. We used to use P1 state to identify whether or not to invoke P2 overwrite function. **Power Well:** SUS
9	0x0 RW	**Enable Core Clock Gating (EN_CORE_CG):** When set to '1' enable core clock gating based on low power state entered **Power Well:** SUS
8	0x0 RW	**Enable PHY Status Timeout (EN_PHY_STS_TO):** When set to '1' enable PHY status timeout function which is designed to cover the PCIePHY issue that we may have not able to detect the PHY status toggle. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
7	0x1 RW	**Ignore aux_pm_en PCIe Core (IGN_APE_PC):** When set to '1' ignore the aux_pm_en reg from PCIe core to continue the remote wake/clock switching support **Power Well:** SUS
6	0x0 RW	**Enable P2 Overwrite P1 (EN_P2_OVR_P1):** When set to '1' enable P2 overwrite P1 when PCIe core has indicated the transition from P0 to P1. This is to enable entering the even lower power state. **Power Well:** SUS
5	0x1 RW	**Enable P2 Remote Wake (EN_P2_REM_WAKE):** When set 1 '1' enable the remote wake function by allowing P2 clock/switching and P2 entering **Power Well:** SUS
4:1	0x0 RW	**Forced PM State (FORCED_PM_STATE):** Reserved. **Power Well:** SUS
0	0x0 RW	**Initiate Force PM State (INIT_FPMS):** When set to '1' force PM state to go to the state indicated in bit 4:1 **Power Well:** SUS

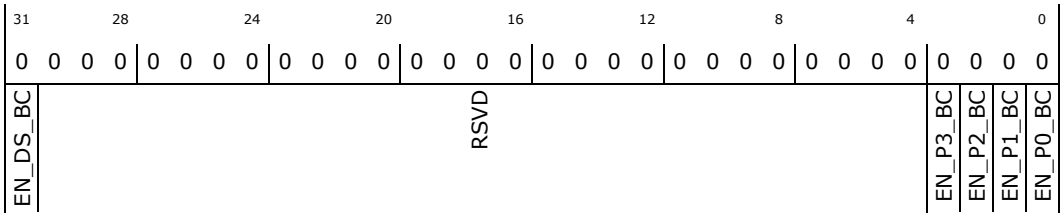
7.2.185 Battery Charge (BATTERY_CHARGE_REG)—Offset 80E4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80E4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Enable DM_SRC Battery Charge (EN_DS_BC):** 1 - Always enable battery charge DM_SRC if not connected. Don't wait for portable device detect. (spec. ver. 1.2) 0 - Battery charge spec ver. 1.1. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
30:4	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
3	0x0 RW	**Enable Port 3 Battery Charging (EN_P3_BC):** 0 - Battery charging disabled (Physical Port #3) 1 - Battery charging enabled (Physical Port #3) **Power Well:** SUS
2	0x0 RW	**Enable Port 2 Battery Charging (EN_P2_BC):** 0 - Battery charging disabled (Physical Port #2) 1 - Battery charging enabled (Physical Port #2) **Power Well:** SUS
1	0x0 RW	**Enable Port 1 Battery Charging (EN_P1_BC):** 0 - Battery charging disabled (Physical Port #1) 1 - Battery charging enabled (Physical Port #1) **Power Well:** SUS
0	0x0 RW	**Enable Port 0 Battery Charging (EN_P0_BC):** 0 - Battery charging disabled (Physical Port #0) 1 - Battery charging enabled (Physical Port #0) **Power Well:** SUS

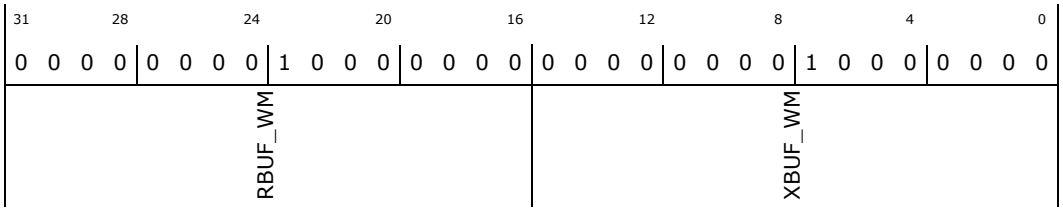
7.2.186 Port Watermark (HOST_CTRL_WATERMARK_REG)—Offset 80E8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80E8h

Default: 00800080h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x80 RW	**RBUF water mark (RBUF_WM):** Reserved. **Power Well:** Core
15:0	0x80 RW	**XBUF water mark (XBUF_WM):** Reserved. **Power Well:** Core

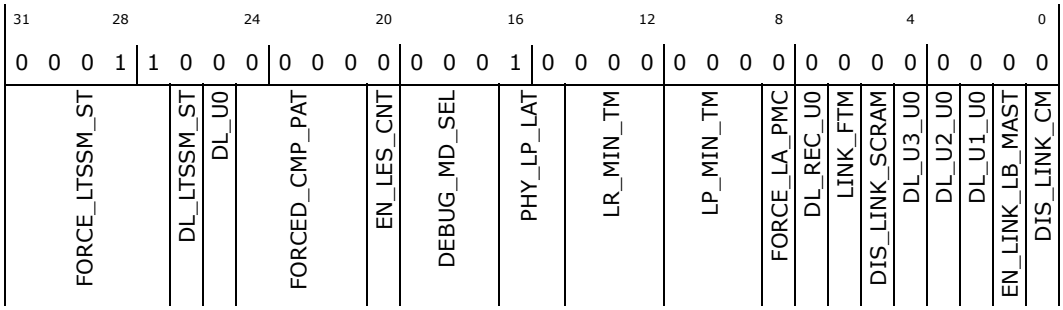
7.2.187 SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)—Offset 80ECh

Access Method

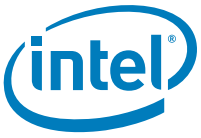
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80ECh

Default: 18010000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x3 RW	**Force LTSSM State (FORCE_LTSSM_ST):** LTSSM state to be forced This value is for test purpose only. **Power Well:** Core
26	0x0 RW	**Direct Link LTSSM State (DL_LTSSM_ST):** 0: Normal operation mode 1: Direct link to a specific state specified by bit 31:27 This bit is for test purpose only. It shall be written 0 in normal operation mode. **Power Well:** Core
25	0x0 RW	**Direct Link To U0 (DL_U0):** 0: Normal operation mode 1: Direct link to U0 This bit is for test purpose only. It shall be written 0 in normal operation mode. **Power Well:** Core
24:21	0x0 RW	**Forced Compliance Pattern (FORCED_CMP_PAT):** Compliance pattern to be forced to enter compliance mode This value is for test purpose only. **Power Well:** Core
20	0x0 RW	**Enable Link Error Slave Count (EN_LES_CNT):** 0: Disable link error slave count 1: Enable link error slave count **Power Well:** Core
19:17	0x0 RW	**Debug Mode Select (DEBUG_MD_SEL):** Reserved. **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
16:15	0x2 RW	**PHY Low Power Latency (PHY_LP_LAT):** This field defines the latency to drive the PHY to enter low power mode 0: 4 cycles 1: 8 cycles 2: 16 cycles 3: 32 cycles **Power Well:** Core
14:12	0x0 RW	**Link Recovery Minimum Time (LR_MIN_TM):** This value defines the minimum time for the link to stay in Recovery.Active other than from U3. The granuity is 128us. **Power Well:** Core
11:9	0x0 RW	**Link Polling Minimum Time (LP_MIN_TM):** This value defines the minimum time for the link to stay in Polling.Active and Recovery.Active from U3. The granuity is 128us. **Power Well:** Core
8	0x0 RW	**Force Link Accept PM Command (FORCE_LA_PMC):** 0: Normal operation mode 1: Force link to accept power management command **Power Well:** Core
7	0x0 RW	**Direct Link Recovery U0 (DL_REC_U0):** 0: Normal operation mode 1: Direct link to Recovery from U0 **Power Well:** Core
6	0x0 RW	**Link Fast Training Mode (LINK_FTM):** 0: Normal operation mode 1: Link fast training mode This bit should be written 0 in normal operation. **Power Well:** Core
5	0x0 RW	**Disable Link Scrambler (DIS_LINK_SCRAM):** 0: Enable link scrambler 1: Disable link scramber **Power Well:** Core
4	0x0 RW	**Direct Link U3 From U0 (DL_U3_U0):** 0: Normal operation mode 1: Direct link to U3 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode. **Power Well:** Core
3	0x0 RW	**Direct Link U3 From U0 (DL_U2_U0):** 0: Normal operation mode 1: Direct link to U2 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode. **Power Well:** Core
2	0x0 RW	**Direct Link U3 From U0 (DL_U1_U0):** 0: Normal operation mode 1: Direct link to U1 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**Enable Link Loopback Master Mode (EN_LINK_LB_MAST):** 0: Disable link loopback master mode 1: Enable link loopback master mode **Power Well:** Core
0	0x0 RW	**Disable Link Compliance Mode (DIS_LINK_CM):** 0: Enable link compliance mode 1: Disable link compliance mode **Power Well:** Core

7.2.188 USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)—Offset 80F0h

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80F0h

Default: 310803A0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0
FSLS_SE0_DIS_DEL_7_0								RSVD0			L1_EXIT_RECOVERY_MODE	L1_TO_INCR_MODE	RSVD3	EN_DETECT_NOMINAL_PKT_EOP	DIS_CHIRP_RESPONSE	DIS_192B_LIM	EXT_FSLS_DIS	UTMI_RST_SEL		DIS_HS_DIS_WIN	DIS_PERR_DET	DIS_PF_IOUT	DRV_RESK_FSLS_SER	EN_U2_DROP_PING	EN_U2_FORCE_PING	EN_U2_AUTO_PING	DIS_PHY_SUSM	UTMI_INT_CG_DIS	DIS_PSUSM_DS	FORCE_PHY_RST	U2_ACC_SIM_TIM

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x31 RW	**FS/LS Mode SE0 Disconnect Delay[7:0] (FSLS_SE0_DIS_DEL_7_0):** # of microseconds of SE0 in FS/LS mode to register disconnect had occurred. **Power Well:** SUS
23:21	0x0 RW	**Reserved (RSVD0):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
20	0x0 RW	**L1_EXIT_RECOVERY_MODE:** Mode for extended L1 Exit recovery delay: 0: 12us 1: 50us **Power Well:** SUS
19	0x1 RW	**L1_TO_INCR_MODE:** Mode select for L1 Timeout increments: 0: time out increments are in 125us 1: L1 Timeout increments are in 256us. Refer to USB2 PORTHLPMC.L1 Timeout in XHCI Spec for additional details **Power Well:** SUS
18	0x0 RW	**Reserved (RSVD3):** Reserved. **Power Well:** SUS
17	0x0 RW	**EN_DETECT_NOMINAL_PKT_EOP:** 0: Detect minimal packet EOP. 1: Detect nominal packet EOP. **Power Well:** SUS
16	0x0 RW	**Disable Chirp Response (DIS_CHIRP_RESPONSE):** 0: Normal 1: Force full speed on host ports (disable chirp response) **Power Well:** SUS
15	0x0 RW	**Disable 192 Byte Limit Check (DIS_192B_LIM):** 0: Enforce 192 byte limit on complete-split INs. Treat any packet) 192 as babble case. 1: Disable 192 byte limit check. **Power Well:** SUS
14	0x0 RW	**External Provided FS/LS Disconnect (EXT_FSLS_DIS):** 0: Internal FS/LS Disconnect from linestate(1:0) 1: External provided FS/LS Disconnect from hostdisconnect input **Power Well:** SUS
13:12	0x0 RW	**UTMI Reset Source Select (UTMI_RST_SEL):** Select UTMI Reset Source (FRD UTMI Reset Only) 00: HCReset or Force PHY Reset or internal reset after disconnect/suspend for restart (default) 01,11: UTMI reset = ~UTMI suspendm 10: UTMI reset = ~UTMI suspendm and synchronization to port clk. **Power Well:** SUS
11	0x0 RW	**Disable HS Disconnect Window (DIS_HS_DIS_WIN):** 0: Enable HS Disconnect Window Function 1: Disable HS Disconnect Window Function **Power Well:** SUS
10	0x0 RW	**Disable Port Error Detection (DIS_PERR_DET):** 0: Enable Port Error Detection (default) 1: Disable Port Error Detection **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
9	0x1 RW	**Disable Peek Function for ISO-OUT (DIS_PF_IOUT):** 0: Enable Peek function for ISO-OUT (default) 1: Disable Peek function for ISO-OUT **Power Well:** SUS
8	0x1 RW	**Drive Resume-K FS/LS Serial Interface (DRV_RESK_FSLS_SER):** 0: Drive Resume-K on parallel Interface 1: Drive Resume-K directly on FS/LS Serial Interface (default) **Power Well:** SUS
7	0x1 RW	**Enable USB2 Drop-Ping (EN_U2_DROP_PING):** 0: Disable Drop-Ping Function in USB2 Protocol (default) 1: Enable Drop-Ping Function in USB2 Protocol **Power Well:** SUS
6	0x0 RW	**Enable USB2 Force-Ping (EN_U2_FORCE_PING):** 0: Disable Force-Ping Function in USB2 Protocol (default) 1: Enable Force-Ping Function in USB2 Protocol **Power Well:** SUS
5	0x1 RW	**Enable USB2 Auto-Ping (EN_U2_AUTO_PING):** 0: Disable Auto-Ping Function 1: Enable Auto-Ping Function in USB2 Protocol (default) **Power Well:** SUS
4	0x0 RW	**Disable PHY SuspendM (DIS_PHY_SUSM):** 0: PHY is suspend=U3,U2,disconnect (default) 1: Disable PHY SuspendM in All States **Power Well:** SUS
3	0x0 RW	**UTMI Internal Clock Gate Disable (UTMI_INT_CG_DIS):** 0: Normal operation (internal clock gated in U2,U3,disconnect) 1: UTMI Internal Clock Gate Disable **Power Well:** SUS
2	0x0 RW	**Disable PHY SuspendM in Disconnect State (DIS_PSUSM_DS):** 0: PHY is suspendM=0 in Disconnect State (default) 1: Disable PHY SuspendM in Disconnect State **Power Well:** SUS
1	0x0 RW	**Force PHY Reset (FORCE_PHY_RST):** 0: Normal Operation (default) 1: Force PHY Reset **Power Well:** SUS
0	0x0 RW	**USB2 Accelerated Simulation Timing (U2_ACC_SIM_TIM):** 0: Normal Operation (default - FPGA/ASIC) 1: USB2 Accelerated Simulation Timing (default - simulation) **Power Well:** SUS

7.2.189 USB2 Port Link Control 2 (USB2_LINK_MGR_CTRL_REG2)—Offset 80F4h

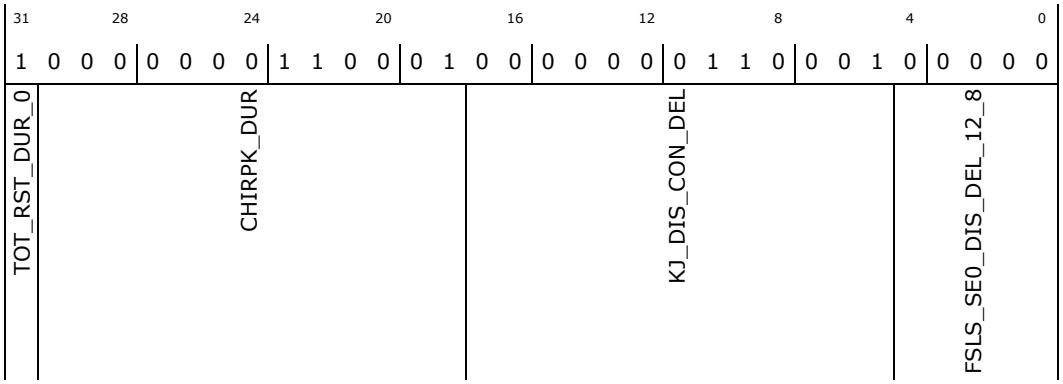
These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80F4h

Default: 80C40620h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**Total Reset Duration[0] (TOT_RST_DUR_0):** # of microseconds for total reset duration **Power Well:** SUS
30:18	0x31 RW	**Chirp-K Duration (CHIRPK_DUR):** # of microseconds of Chirp-K to register that a device is chirping **Power Well:** SUS
17:5	0x31 RW	**K/J Disconnect Connect Delay (KJ_DIS_CON_DEL):** # of microseconds of K/J in disconnected state to register connect has occurred. **Power Well:** SUS
4:0	0x0 RW	**FS/LS Mode SE0 Disconnect Delay[12:8] (FSLS_SE0_DIS_DEL_12_8):** # of microseconds of SE0 in FS/LS mode to register disconnect had occurred. **Power Well:** SUS

7.2.190 USB2 Port Link Control 3 (USB2_LINK_MGR_CTRL_REG3)—Offset 80F8h

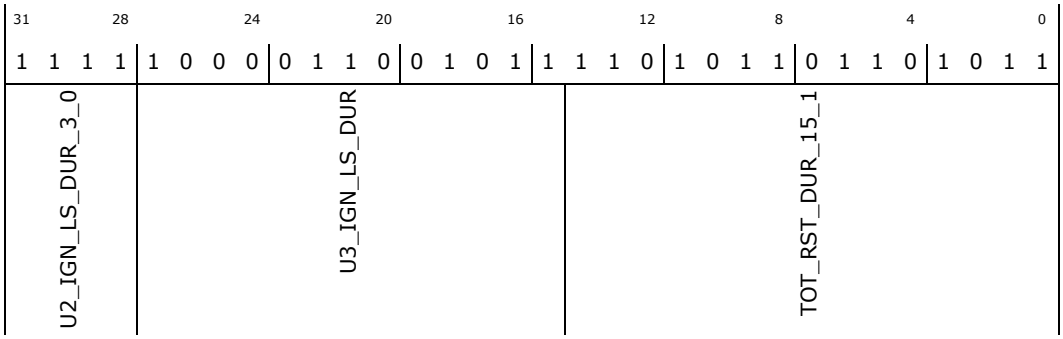
These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80F8h

Default: F865EB6Bh



Bit Range	Default & Access	Field Name (ID): Description
31:28	0xf RW	**U2 Entry Ignore Linestate Changes Duration[3:0] (U2_IGN_LS_DUR_3_0):** # of microseconds after entering U2, linestate changes are ignored as bus settles **Power Well:** SUS
27:15	0x10cb RW	**U3 Entry Ignore Linestate Changes Duration (U3_IGN_LS_DUR):** # of microseconds after entering U3, linestate changes are ignored as bus settles **Power Well:** SUS
14:0	0x6b6b RW	**Total Reset Duration[15:1] (TOT_RST_DUR_15_1):** # of microseconds for total reset duration **Power Well:** SUS

7.2.191 USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)—Offset 80FCh

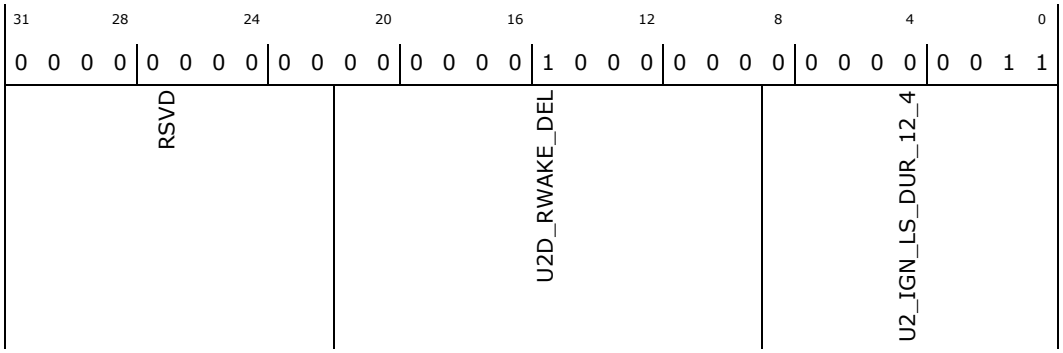
These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 80FCh

Default: 00008003h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
21:9	0x40 RW	**U2 Detect Remote Wake Delay (U2D_RWAKE_DEL):** #of microseconds after detecting U2 remote wake condition to reflect K **Power Well:** SUS
8:0	0x3 RW	**U2 Entry Ignore Linestate Changes Duration[12:4] (U2_IGN_LS_DUR_12_4):** # of microseconds after entering U2, linestate changes are ignored as bus settles **Power Well:** SUS

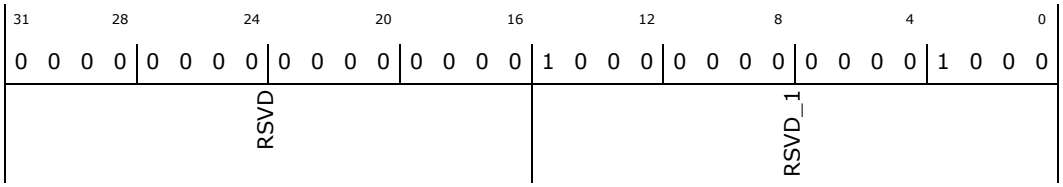
7.2.192 Bandwidth Calc Control (HOST_CTRL_BW_CTRL_REG)—Offset 8100h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8100h

Default: 00008008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:0	0x8008 RW	**Reserved (RSVD_1):** Reserved. **Power Well:** Core

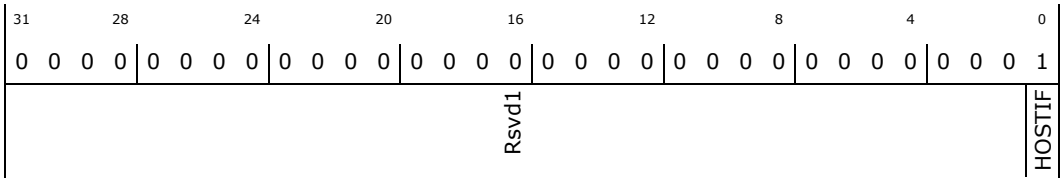
7.2.193 Host Interface Control (HOST_IF_CTRL_REG)—Offset 8108h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8108h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Rsvd1:** Reserved. **Power Well:** Core
0	0x1 RW	**Host IF (HOSTIF):** Reserved. **Power Well:** Core

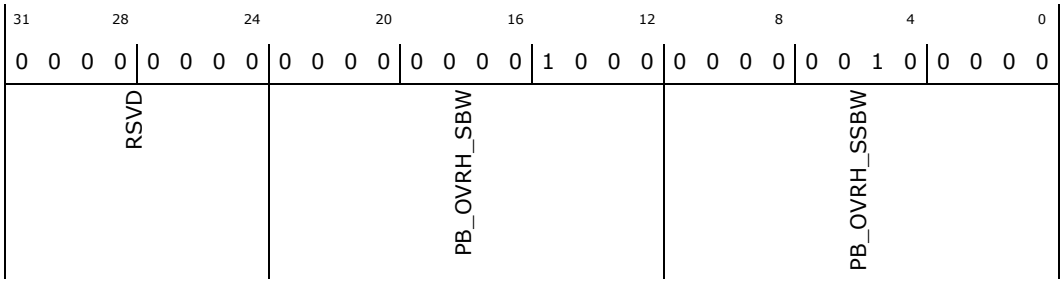
7.2.194 Bandwidth Overload Burst (HOST_BW_OV_BURST_REG)—Offset 810Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 810Ch

Default: 00008020h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
23:12	0x8 RW	**Per Burst Overhead System BW (PB_OVRH_SBW):** BW calculation: Overhead per burst for system BW calculations. see white paper. **Power Well:** Core
11:0	0x20 RW	**Per Burst Overhead System BW (PB_OVRH_SSBW):** BW calculation: Overhead per burst for SS BW calculations. see white paper. **Power Well:** Core

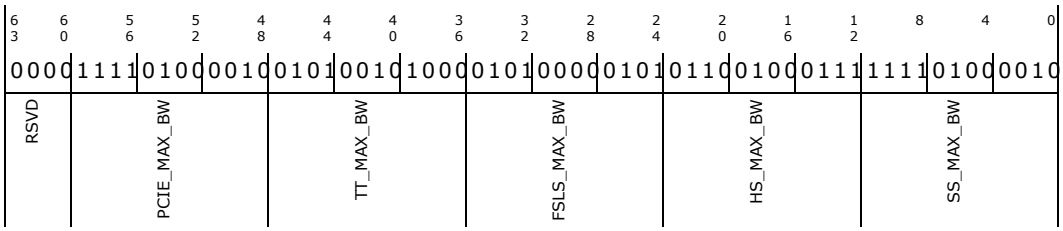
7.2.195 USB Max Bandwidth Control 4 (HOST_CTRL_BW_MAX_REG)—Offset 8128h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [MBAR] + 8128h

Default: 0F42528505647F42h



Bit Range	Default & Access	Field Name (ID): Description
63:60	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
59:48	0xf42 RW	**PCIe Max BW Units (PCIE_MAX_BW):** Max. Number of BW units for PCIe (system interface) (denominator in 90% calculation) **Power Well:** Core
47:36	0x528 RW	**TT Max BW Units (TT_MAX_BW):** Max. Number of BW units for TTs. (denominator in 90% calculation) **Power Well:** Core
35:24	0x505 RW	**FS/LS Max BW Units (FSLS_MAX_BW):** Max. Number of BW units for FS/LS ports. (denominator in 90% calculation) **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
23:12	0x647 RW	**HS Max BW Units (HS_MAX_BW):** Max. Number of BW units for HS ports. (denominator in 80% calculation) **Power Well:** Core
11:0	0xf42 RW	**SS Max BW Units (SS_MAX_BW):** Max. Number of BW units for SS ports. (denominator in 90% calculation) **Power Well:** Core

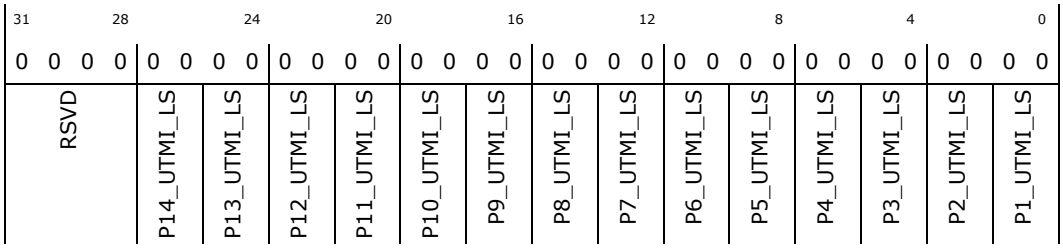
7.2.196 USB2 Linestate Debug (LINESTATE_DEBUG_REG)—Offset 8130h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8130h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
27:26	0x0 RO	**Port 14 UTMI Linestate (P14_UTMI_LS):** Reserved. **Power Well:** Core
25:24	0x0 RO	**Port 13 UTMI Linestate (P13_UTMI_LS):** Reserved. **Power Well:** Core
23:22	0x0 RO	**Port 12 UTMI Linestate (P12_UTMI_LS):** Reserved. **Power Well:** Core
21:20	0x0 RO	**Port 11 UTMI Linestate (P11_UTMI_LS):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
19:18	0x0 RO	**Port 10 UTMI Linestate (P10_UTMI_LS):** Reserved. **Power Well:** Core
17:16	0x0 RO	**Port 9 UTMI Linestate (P9_UTMI_LS):** Reserved. **Power Well:** Core
15:14	0x0 RO	**Port 8 UTMI Linestate (P8_UTMI_LS):** Reserved. **Power Well:** Core
13:12	0x0 RO	**Port 7 UTMI Linestate (P7_UTMI_LS):** Reserved. **Power Well:** Core
11:10	0x0 RO	**Port 6 UTMI Linestate (P6_UTMI_LS):** Reserved. **Power Well:** Core
9:8	0x0 RO	**Port 5 UTMI Linestate (P5_UTMI_LS):** Reserved. **Power Well:** Core
7:6	0x0 RO	**Port 4 UTMI Linestate (P4_UTMI_LS):** Reserved. **Power Well:** Core
5:4	0x0 RO	**Port 3 UTMI Linestate (P3_UTMI_LS):** Reserved. **Power Well:** Core
3:2	0x0 RO	**Port 2 UTMI Linestate (P2_UTMI_LS):** Reserved. **Power Well:** Core
1:0	0x0 RO	**Port 1 UTMI Linestate (P1_UTMI_LS):** Reserved. **Power Well:** Core

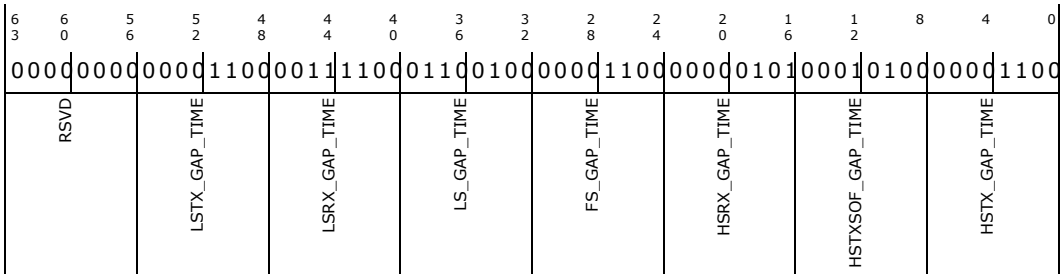
7.2.197 USB2 Protocol Gap Timer (USB2_PROTOCOL_GAP_TIMER_REG)—Offset 8134h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [MBAR] + 8134h

Default: 000C3C640C05140Ch



Bit Range	Default & Access	Field Name (ID): Description
63:56	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
55:48	0xc RW	**GAP time after LS TX thru FS hub (LSTX_GAP_TIME):** Reserved. **Power Well:** Core
47:40	0x3c RW	**GAP time after LS RX thru FS hub (LSRX_GAP_TIME):** Reserved. **Power Well:** Core
39:32	0x64 RW	**GAP timer after LS (LS_GAP_TIME):** Reserved. **Power Well:** Core
31:24	0xc RW	**GAP time after FS (FS_GAP_TIME):** Reserved. **Power Well:** Core
23:16	0x5 RW	**GAP time after HS RX (HSRX_GAP_TIME):** Reserved. **Power Well:** Core
15:8	0x14 RW	**GAP time after HS TX SOF (HSTXSOF_GAP_TIME):** Reserved. **Power Well:** Core
7:0	0xc RW	**GAP time HS TX Packet (HSTX_GAP_TIME):** Reserved. **Power Well:** Core

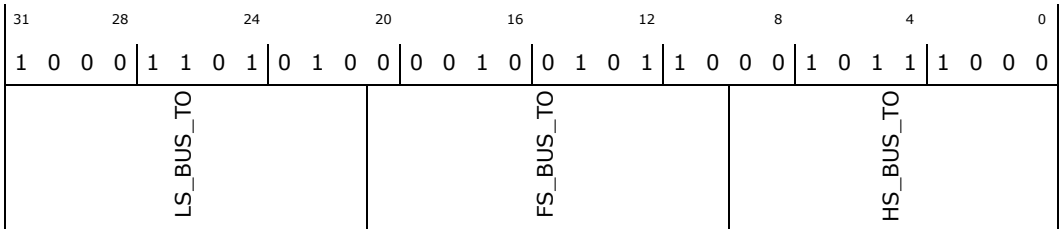
7.2.198 USB2 Protocol Bus Timeout Timer (USB2_PROTOCOL_BTO_TIMER_REG)—Offset 813Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 813Ch

Default: 8D4258B8h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x46a RW	**Bus timeout count for LS (LS_BUS_TO):** Reserved. **Power Well:** Core
20:10	0x96 RW	**Bus timeout count for FS (FS_BUS_TO):** Reserved. **Power Well:** Core
9:0	0xb8 RW	**Bus timeout count for HS (HS_BUS_TO):** Reserved. **Power Well:** Core

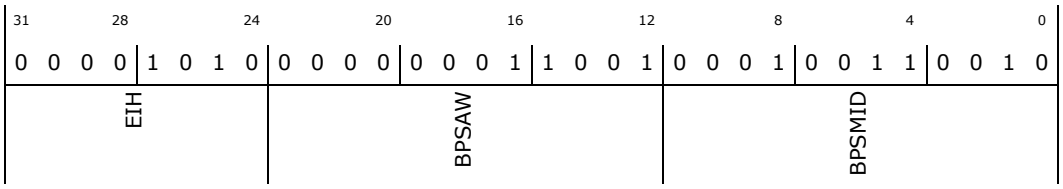
7.2.199 Power Scheduler Control-0 (PWR_SCHED_CTRL0)—Offset 8140h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8140h

Default: 0A019132h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0xa RW	**Engine Idle Hysteresis (EIH):** This register controls the min. idle span that has to be observed from the engine idle indicators before the power state flags (xhc_*_idle) will indicate a 1. **Power Well:** Core
23:12	0x19 RW	**Backbone PLL Shutdown Advance Wake (BPSAW):** This register controls the time before the next scheduled transaction where the Backbone PLL request will assert. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124) **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11:0	0x132 RW	**Backbone PLL Shutdown Min. Idle Duration (BPSMID):** The sum of this register plus the Backbone PLL Shutdown Advance Wake form to a Total Idle time. When the next scheduled periodic transaction is after present time + Total Idle, the Backbone PLL request will de-assert, allowing the PLL to shutdown. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124) **Power Well:** Core

7.2.200 Power Scheduler Control-2 (PWR_SCHED_CTRL2)—Offset 8144h

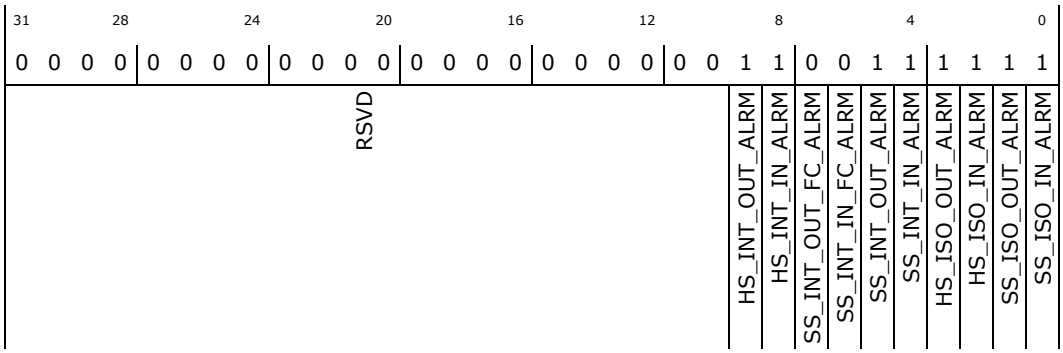
These bit enable by EP type those EPs classes that are considered for determining next periodic active interval for pre-wake of the periodic_active signal. EP classes that are disabled may never be observed in setting of the periodic_active signal.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8144h

Default: 0000033Fh



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
9	0x1 RW	**HS Interrupt-OUT Alarm (HS_INT_OUT_ALRM):** Reserved. **Power Well:** Core
8	0x1 RW	**HS Interrupt-IN Alarm (HS_INT_IN_ALRM):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW	**SS Interrupt-OUT FC Alarm (SS_INT_OUT_FC_ALRM):** Reserved. **Power Well:** Core
6	0x0 RW	**SS Interrupt-IN Alarm (SS_INT_IN_FC_ALRM):** Reserved. **Power Well:** Core
5	0x1 RW	**SS Interrupt-OUT & not in FC Alarm (SS_INT_OUT_ALRM):** Reserved. **Power Well:** Core
4	0x1 RW	**SS Interrupt-IN & not in FC Alarm (SS_INT_IN_ALRM):** Reserved. **Power Well:** Core
3	0x1 RW	**HS ISO-OUT Alarm (HS_ISO_OUT_ALRM):** Reserved. **Power Well:** Core
2	0x1 RW	**HS ISO-IN Alarm (HS_ISO_IN_ALRM):** Reserved. **Power Well:** Core
1	0x1 RW	**SS ISO-OUT Alarm (SS_ISO_OUT_ALRM):** Reserved. **Power Well:** Core
0	0x1 RW	**SS ISO-IN Alarm (SS_ISO_IN_ALRM):** Reserved. **Power Well:** Core

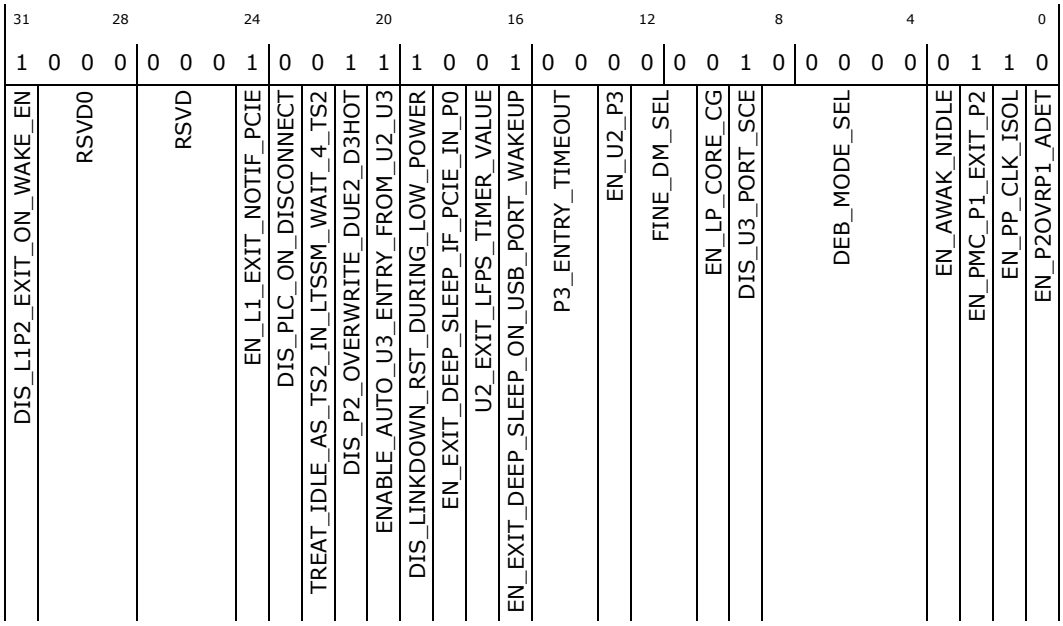
7.2.201 AUX Power Management Control (AUX_CTRL_REG2)—Offset 8154h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8154h

Default: 81390206h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**DIS_L1P2_EXIT_ON_WAKE_EN:** This bit disables the dependency on Wake Enables defined in PORTSC for L1P2 exit when in D0 **Power Well:** SUS
30:28	0x0 RW	**RESERVED0 (RSVD0):** Reserved. **Power Well:** SUS
27:25	0x0 RW	**RESERVED (RSVD):** Reserved. **Power Well:** SUS
24	0x1 RW	**Enable L1 exit notification to SNPS PCIe core (EN_L1_EXIT_NOTIF_PCIE):** This bit enables a L1 exit notification to SNPS PCIe core. There is a case where USB ports have waked up and AUX PM module has started the wakeup process. The AUX PM control state got into a wait for P0 state because it needs to wait until PCie core to signal powerdown state change. Due to the fact that the core is in D3Hot, there is no run_stop bit set such that no internal interrupt will be fired. This causes the LTSSM of PCIe stayed in L1 even though AUX PM has known that it needs an L1 exit. This bit works together with bit21 of this register. 1: enables this feature 0: disables this feature. **Power Well:** SUS
23	0x0 RW	**DISABLE PLC ON DISCONNECT (DIS_PLC_ON_DISCONNECT):** 1: do not assert PLC for disconnection 0: assert PLC for disconnection **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
22	0x0 RW	**TREAT_IDLE_AS_TS2_IN_LTSSM_WAIT_4_TS2:** This bit enables a feature in PCie core LTSSM to treat IDLE received as TS2 when LTSSM is in wait for TS2 receive state. This is a function requested from PHY where it is possible to not able to receive TS2 without error. 1: treat Logic IDLE as TS2 received when in some PCIe LTSSM state. 0: disable this feature. **Power Well:** SUS
21	0x1 RW	**Disable p2 overwrite due to the D3HOT where PCIe core enters the L1 (DIS_P2_OVERWRITE_DUE2_D3HOT):** We added a feature where if PCIe core LTSSM enters L1 due to the D3hot, the aux PM control will not start a P2 overwrite function in anticipating for the next L23 enter. 1: disables p2 overwrite due to the D3HOT where PCIe core enters the L1. 0: enables P2 overwrite even if we are in D3Hot. **Power Well:** SUS
20	0x1 RW	**Enable the port to enter U3 automatically when in U1/U2 (ENABLE_AUTO_U3_ENTRY_FROM_U2_U3):** 1: enables the port to enter U3 automatically when in U1/U2 0: disables the port to enter U3 automatically when in U1/U2 **Power Well:** SUS
19	0x1 RW	**No linkdown reset is issue during low power state (DIS_LINKDOWN_RST_DURING_LOW_POWER):** No linkdown reset is issue during low power state **Power Well:** SUS
18	0x0 RW	**EN_EXIT_DEEP_SLEEP_IF_PCIE_IN_P0:** This bit enables a feature in AUX PM module where if PCIe core LTSSM is in P0 for a duration of time, we will exit the deep sleep state. This is for failure control in case. 1: enables this feature 0: disable this feature **Power Well:** SUS
17	0x0 RW	**U2_EXIT_LFPS_TIMER_VALUE:** This bit selects U2 exit LFPS timer value 0: 320ns 400ns in 25MHz domain 1: 240ns 320ns in 25MHz domain **Power Well:** SUS
16	0x1 RW	**EN_EXIT_DEEP_SLEEP_ON_USB_PORT_WAKEUP:** This bit enables a function that AUX PM module exits from the deep sleep state due to the USB ports wakeup level signal. We have added this feature where USB ports will generated a wakeup level signal to wakeup the AUX PM module if it is in deep sleep state and this level signal will be cleared if the change bits are updated by software. 1: enables this function 0: disables this function which means that a wakeup pulse generated from each USB PortSC event will wake up the AUX PM module from deep sleep if the D3 state is programmed. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RW	**P3_ENTRY_TIMEOUT:** This field defines the timeout value to enter P3 mode in U2. 00: 7us 8us 01: 511us 512us 10: disables the timer (0us) 11: disables the timer (0us) **Power Well:** SUS
13	0x0 RW	**Enable U2 P3 Mode (EN_U2_P3):** 0: Disable U2 P3 mode 1: Enable U2 P3 mode **Power Well:** SUS
12:11	0x0 RW	**Fine Debug Mode Select (FINE_DM_SEL):** Reserved. **Power Well:** SUS
10	0x0 RW	**Enable Low Power State Based Core Clock Gating (EN_LP_CORE_CG):** When set to '1' enable core clock gating based on low power state entered **Power Well:** SUS
9	0x1 RW	**Disable USB3 Port Status Changed Event (DIS_U3_PORT_SCE):** 0: Enable USB3 port status change event generation if any change bit is not cleared 1: Disable USB3 port status change event generation if any change bit is not cleared Bit 12 default 0 **Power Well:** SUS
8:4	0x0 RW	**Debug Mode Select Register (DEB_MODE_SEL):** Reserved. **Power Well:** SUS
3	0x0 RW	**Enable Auto Wakeup Non-IDLE (EN_AWAK_NIDLE):** When set to 1 enables the auto wakeup function when engine has identified non IDLE condition. **Power Well:** SUS
2	0x1 RW	**Enable PM Control P1 Exit P2 (EN_PMC_P1_EXIT_P2):** When set 1 enables the PM control module to transition to P1 instead of P0 when exit P2. **Power Well:** SUS
1	0x1 RW	**Enable PCIe PIPE CLK Isolation (EN_PP_CLK_ISOL):** When set to 1 enables the PCIe PIPE CLK to be isolated when main power is removed. **Power Well:** SUS
0	0x0 RW	**Enable P2 Overwrite P1 Allowed Detect (EN_P2OVRP1_ADET):** When set to 1 enables a function that can detect whether or not enable P2 overwrite P1 function. The condition to get to P2 overwrite is when engine is in idle conditions. This means that there is no ISO EP pending. **Power Well:** SUS

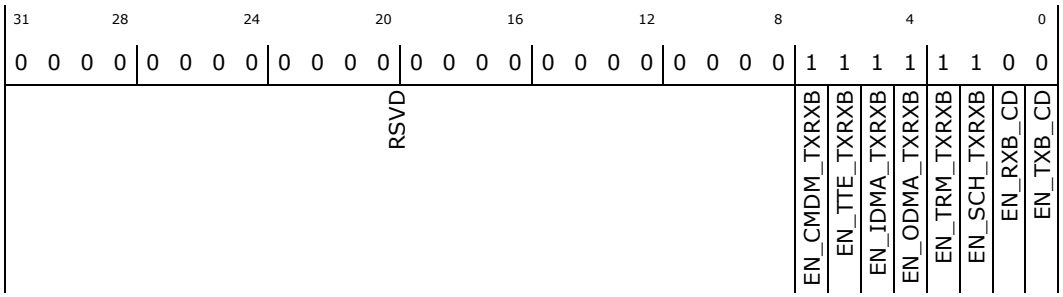
7.2.202 USB2 PHY Power Management Control (USB2_PHY_PMC)—Offset 8164h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8164h

Default: 000000FCh



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
7	0x1 RW	**EN_CMDM_TXRXB:** Enable Command Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy **Power Well:** Core
6	0x1 RW	**EN_TTE_TXRXB:** Enable TTE Active indication for Tx/Rx Bias circuit HS Phy PM Policy **Power Well:** Core
5	0x1 RW	**EN_IDMA_TXRXB:** Enable IDMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy **Power Well:** Core
4	0x1 RW	**EN_ODMA_TXRXB:** Enable ODMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy **Power Well:** Core
3	0x1 RW	**EN_TRM_TXRXB:** Enable Transfer Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy **Power Well:** Core
2	0x1 RW	**EN_SCH_TXRXB:** Enable Scheduler Active indication for Tx/Rx Bias circuit HS Phy PM Policy **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**Enable Rx Bias ckt disable (EN_RXB_CD):** When set enables the Rx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits) **Power Well:** Core
0	0x0 RW	**Enable Tx Bias ckt disable (EN_TXB_CD):** When set enables the Tx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits) **Power Well:** Core

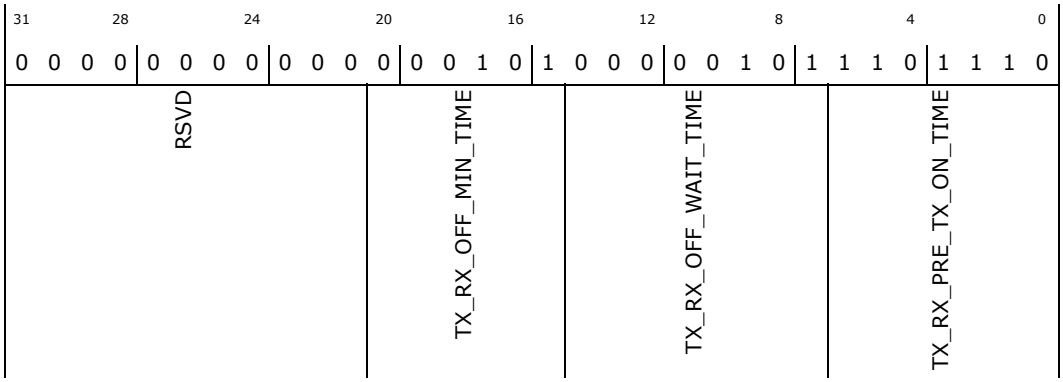
7.2.203 USB2 Phy Power Management Control 2 (USB2_PHY_PMC2)—Offset 8168h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8168h

Default: 000282EEh



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
20:15	0x5 RW	**Tx/Rx Off Min Time (TX_RX_OFF_MIN_TIME):** Minimum number of clocks (uclk60x) for which Tx/Rx shall be switched off. This is used to decide if bias circuits can be switched off in the current micro-frame ahead of the next Tx/Rx. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14:7	0x5 RW	**Tx/Rx Off Wait Time (TX_RX_OFF_WAIT_TIME):** Guardband time in number of clocks (uclk60x) before which Tx/Rx can be turned off when there is no activity **Power Well:** Core
6:0	0x6e RW	**Tx/Rx Pre Tx ON Time (TX_RX_PRE_TX_ON_TIME):** This is the time (in uclk60 clock periods) when Tx/Rx Bias needs to be turned on ahead of Transmit or Receive. This is based on the AFE requirement when bias needs to be ON before the transmit/receive occurs on the bus. **Power Well:** Core

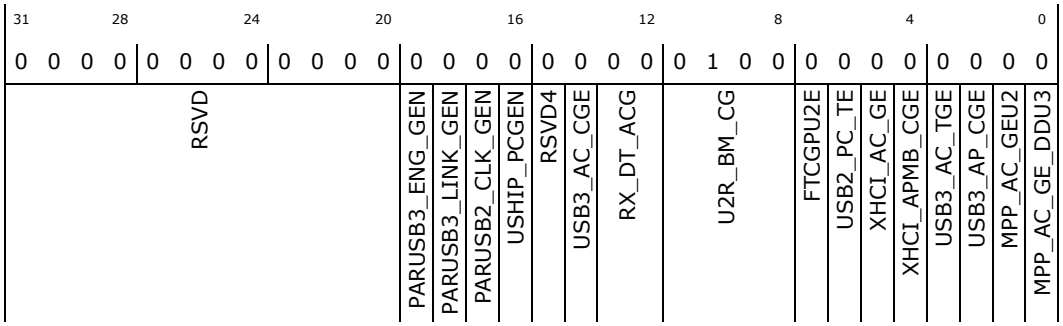
7.2.204 xHCI Aux Clock Control Register (XHCI_AUX_CCR)—Offset 816Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 816Ch

Default: 00000400h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**Reserved (RSVD):** Reserved.
19	0x0 RW	**USB3 Partition Engine/Link trunk gating Enable (PARUSB3_ENG_GEN):** When set to 1 enables gating of the SOSC trunk to the XHCI engine and link in the PARUSB3 partition. **Power Well:** SUS
18	0x0 RW	**USB3 Partition Frame Timer trunk gating Enable (PARUSB3_LINK_GEN):** When set to 1 enables gating of the SOSC trunk to the Frame timer in the PARUSB3 partition. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
17	0x0 RW	**USB2 link partition clock gating enable (PARUSB2_CLK_GEN):** When set to 1 enables gating of the SOSC trunk to the USB2 link and Phy logic in the PARUSB2 partition. **Power Well:** SUS
16	0x0 RW	**USB2/USHIP 12.5 MHz partition clock gating enable (USHIP_PCGEN):** When set to 1 enables gating of the 12.5 MHz SOSC trunk to the USB2 and USHIP logic in the PARUSB2 partition. **Power Well:** SUS
15	0x0 RO	**Reserved1 (RSVD4):** Reserved
14	0x0 RW	**USB3 Port Aux/Core clock gating enable (USB3_AC_CGE):** When set, allows the aux_cclk clock into the USB3 port to be gated when conditions are met. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS
13:12	0x0 RW	**Rx Detect Timer when port Aux Clock is Gated (RX_DT_ACG):** This field defines the value of the timer used to perform Rx Detect when port Aux Clock has been gated. 0x0: 100ms 0x1: 12ms Others: Reserved Note: This timer shall use the Fast Training Timer Tick (about 1us tick) for simulation purposes. For Fast Training mode, the above timeouts will become about 11us and about 100us, +/- implementation uncertainty, respectively. **Power Well:** SUS
11:8	0x4 RW	**U2 Residency Before ModPHY Clock Gating (U2R_BM_CG):** Before gating ModPHY Aux clock, Host Controller shall wait for this time in U2. This time is meant to ensure that the attached device has entered U2 as well. 0x0: 1us 0x1: 128us 0x2: 256us 0x3: 512us 0x4: 640us 0x5: 768us 0x6: 896us 0x7: 1024us Others: Reserved Note: This counter shall start counting once pipe has entered PS3 state in response to link in U2. **Power Well:** SUS
7	0x0 RW	**Frame Timer Clock Gating Ports in U2 Enable (FTCGPU2E):** This bit, when set, allows Host Controller to gate the clock to the Frame Timer when ports are in U2. **Power Well:** SUS
6	0x0 RW	**USB2 port clock throttle enable (USB2_PC_TE):** When set, allows the Aux clock into the USB2 ports to be throttled when conditions allow. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**XHCI Engine Aux clock gating enable (XHCI_AC_GE):** When set, allows the aux clock into the XHCI engine to be gated when idle. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS
4	0x0 RW	**XHCI Aux PM block clock gating enable (XHCI_APMB_CGE):** When set, allows the aux clock into the Aux PM block to be gated when idle. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS
3	0x0 RW	**USB3 Aux Clock Trunk Gating Enable (USB3_AC_TGE):** When set, allows Aux Clock Trunk feeding to USB3.0 ports to be gated when port Aux clock is gated at all USB3.0 ports and all USB3.0 modPHY instances. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS
2	0x0 RW	**USB3 Port Aux/Port clock gating enable (USB3_AP_CGE):** When set, allows the aux_pclk clock into the USB3 port to be gated when conditions are met. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS
1	0x0 RW	**ModPHY port Aux clock gating enable in U2 (MPP_AC_GEU2):** When set, allows the aux clock into the ModPhy to be gated when Link is in U2 and pipe has been in PS3 for at least the time defined by U2 Residency Before ModPHY Clock Gating field. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**ModPHY port Aux clock gating enable in Disconnected, U3 or Disabled (MPP_AC_GE_DDU3):** When set, allows the aux clock into the ModPHY to be gated when Link is in Disconnected, U3 or Disabled state. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS

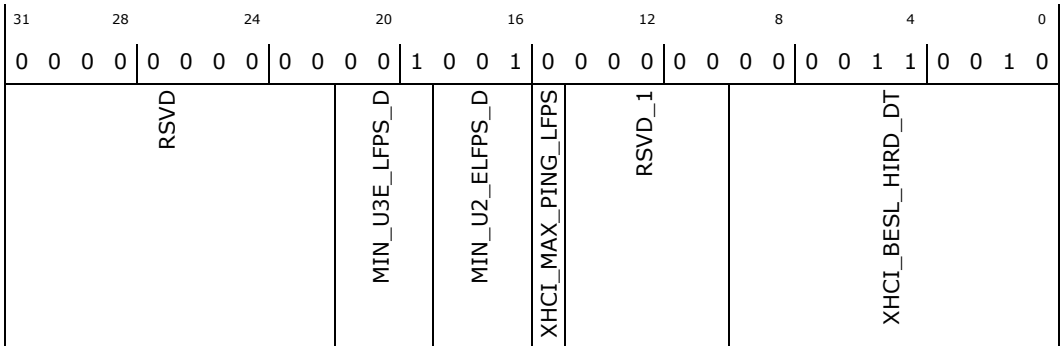
7.2.205 USB LPM Parameters (USB_LPM_PARAM)—Offset 8170h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8170h

Default: 00090032h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
21:19	0x1 RW	**Min U3 Exit LFPS Duration (MIN_U3E_LFPS_D):** Min U3 Exit LFPS Duration This field defines the minimum duration of LFPS driven by Host Controller upon U3 exit LFPS handshake. Note that theres an uncertainty of +-16us in actual duration driven by the Host Controller. 0b000: 96us 0b001: 160us 0b010: 224us 0b011: 288us 0b100: 352us 0b101: 416us 0b110: 480us 0b111: 544us **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
18:16	0x1 RW	**Min U2 Exit LFPS Duration (MIN_U2_ELFPS_D):** Min U2 Exit LFPS Duration This field defines the minimum duration of LFPS driven by Host Controller upon U2 exit LFPS handshake. Note that theres an uncertainty of +-16us in actual duration driven by the Host Controller. 0b000: 96us 0b001: 160us 0b010: 224us 0b011: 288us 0b100: 352us 0b101: 416us 0b110: 480us 0b111: 544us **Power Well:** SUS
15	0x0 RW	**Max PING LFPS Rx Detection (XHCI_MAX_PING_LFPS):** This field defines the maximum timing for PING LFPS. If an incoming LFPS will be considered a PING if it has a timing such that it is less than or equal to the selected value. Otherwise it will be considered for the other types of LFPS. 0b Max PING LFPS timing set to 256 ns (32 link clocks) 1b Max PING LFPS timing set to 320 ns (40 link clocks) **Power Well:** SUSe
14:10	0x0 RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core
9:0	0x32 RW	**xHCI BESL to HIRD Distance (XHCI_BESL_HIRD_DT):** This field defines the gap between BESL and duration of Resume signalling from Host upon Host Initiated Resume from USB2.0 LPM. Default value of this register corresponds to xHCI spec defined 50us value. Value BESL to HIRD Distance 000h 0us 001h 1us 002h 2us 3FFh 1023us **Power Well:** SUS

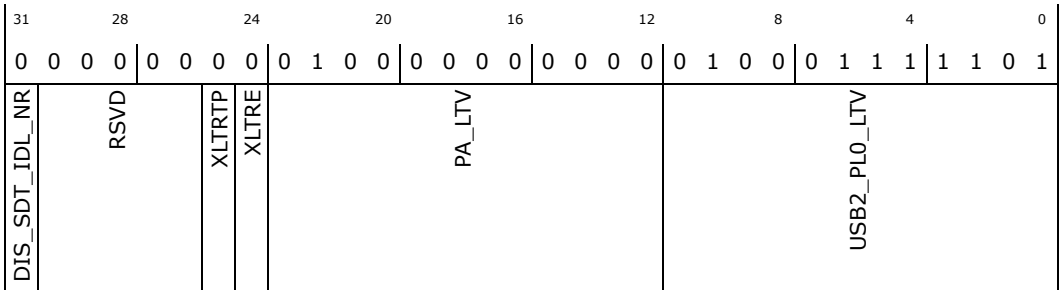
7.2.206 xHC Latency Tolerance Parameters - LTV Control (XLTP_LTV1)—Offset 8174h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8174h

Default: 0040047Dh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Disable scheduler direct transition from IDLE to NO requirement (DIS_SDT_IDL_NR):** 0: (default) allow scheduler direct transition from IDLE to NO requirement 1: Disable scheduler direct transition from IDLE to NO requirement **Power Well:** Core
30:26	0x0 RW	**Reserved (RSVD):** Reserved. **Power Well:** Core
25	0x0 RW	**XHCI LTR Transition Policy (XLTRTP):** When '0', LTR messaging state machine transitions from High, Medium, or Low LTR states to Active state upon the Alarm Timer timout and stays in Active until the next service boundary. When '1', the LTR messaging state machine transitions through High ? Med ? Low ? Active states assuming enough latency is available for each transition. **Power Well:** Core
24	0x0 RW	**XHCI LTR Enable (XLTRE):** This bit must be set to enable LTV messaging from XHCI to the PMC. **Power Well:** Core
23:12	0x400 RW	**Periodic Active LTV (PA_LTV):** 23:22 Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 21:12 Latency Value (ns) Defaults to 0 micro seconds **Power Well:** Core
11:0	0x47d RW	**USB2 Port L0 LTV (USB2_PL0_LTV):** 11:10 Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 9:0 Latency Value (ns) Defaults to 128 Micro Seconds **Power Well:** Core

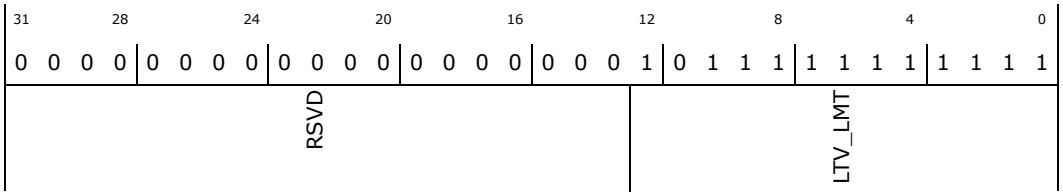
7.2.207 xHC Latency Tolerance Parameters LTV Control 2 (XLTP_LTV2)—Offset 8178h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8178h

Default: 000017FFh



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
12:0	0x17ff RW	**LTV Limit (LTV_LMT):** This register defines a maximum LTR value that is allowed to be advertised to the PMC. This is meant to be used as a workaround or mitigation if issues are discovered with the LTR values generated by the XHC using the defined algorithms. If the LTR value of the XHC is larger than the value in this register field, the value in this field is sent to the PMC instead. Default value is the highest possible - 101b 12:10: Latency Multiplier Field 000b - Value times 1 ns 001b - Value times 32 ns 010b - Value times 1,024 ns 011b - Value times 32,768 ns 100b - Value times 1,048,576 ns 101b - Value times 33,554,432 ns 110b-111b - Not Permitted 9:0: Latency Value Default = 3FFh **Power Well:** Core

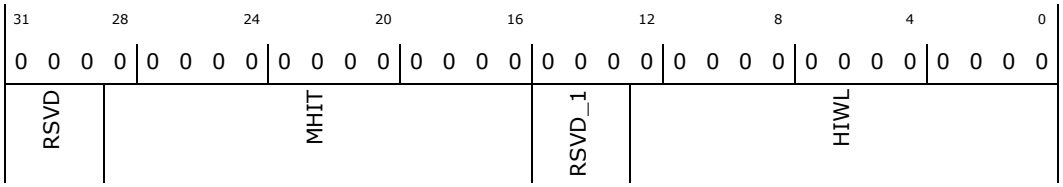
7.2.208 xHC Latency Tolerance Parameters - High Idle Time Control (XLTP_HITC)—Offset 817Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 817Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
28:16	0x0 RW	**Minimum High Idle Time (MHIT):** LTR value can be indicated. This value must be larger than HIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds) **Power Well:** Core
15:13	0x0 RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core
12:0	0x0 RW	**High Idle Wake Latency (HIWL):** This is the latency to access memory from the High Idle Latency state. This value must be larger than MIWL and LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds) **Power Well:** Core

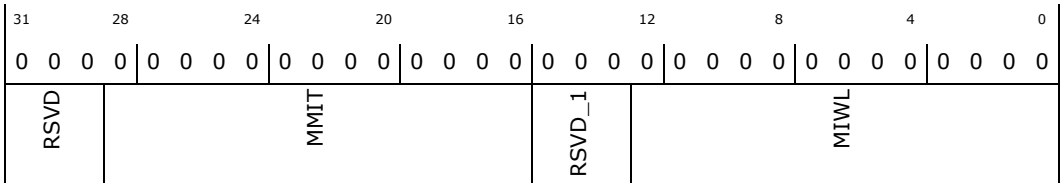
7.2.209 xHC Latency Tolerance Parameters - Medium Idle Time Control (XLTP_MITC)—Offset 8180h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8180h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
28:16	0x0 RW	**Minimum Medium Idle Time (MMIT):** LTR value can be indicated. This value must be larger than MIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds) **Power Well:** Core
15:13	0x0 RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12:0	0x0 RW	**Medium Idle Wake Latency (MIWL):** This is the latency to access memory from the Medium Idle Latency state. This value must be larger than LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds) **Power Well:** Core

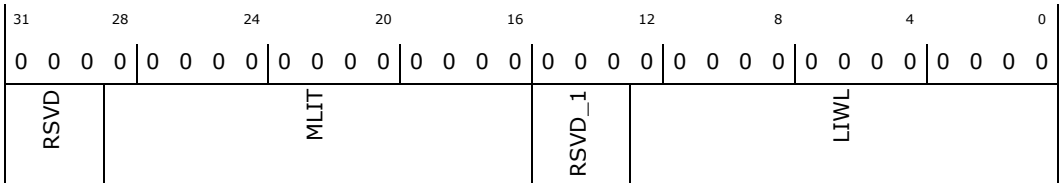
7.2.210 xHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)—Offset 8184h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8184h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
28:16	0x0 RW	**Minimum Low Idle Time (MLIT):** LTR value can be indicated. This value must be larger than LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds) **Power Well:** Core
15:13	0x0 RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core
12:0	0x0 RW	**Low Idle Wake Latency (LIWL):** This is the latency to access memory from the Medium Idle Latency state. 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds) **Power Well:** Core

7.2.211 HOST_CTRL_BW_MAX3_REG—Offset 8188h

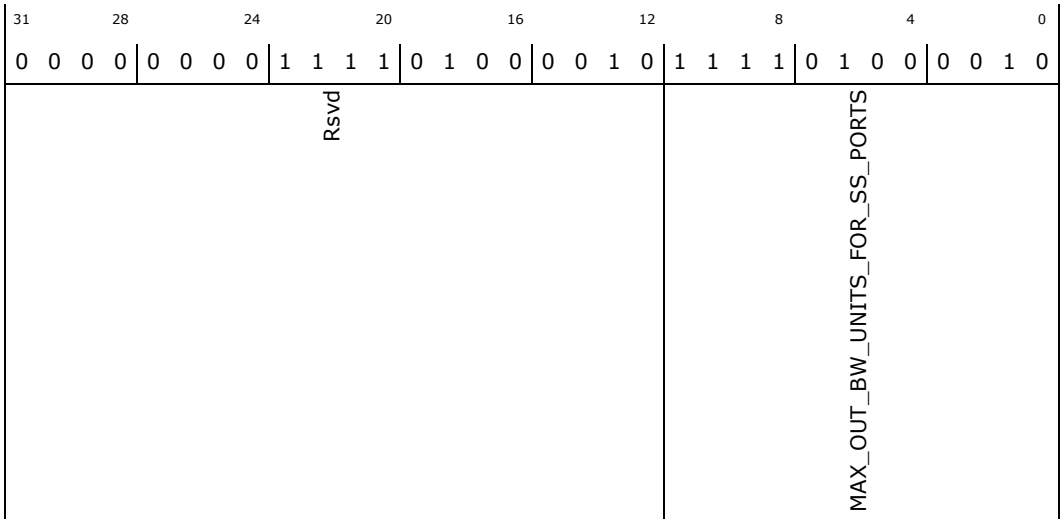
Added for SoC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8188h

Default: 00F42F42h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0xf42 RO	**Rsvd:** Reserved. **Power Well:** Core
11:0	0xf42 RW	**MAX_OUT_BW_UNITS_FOR_SS_PORTS:** Max. Number of OUT BW units for SS ports - denominator in 90% calculation **Power Well:** Core

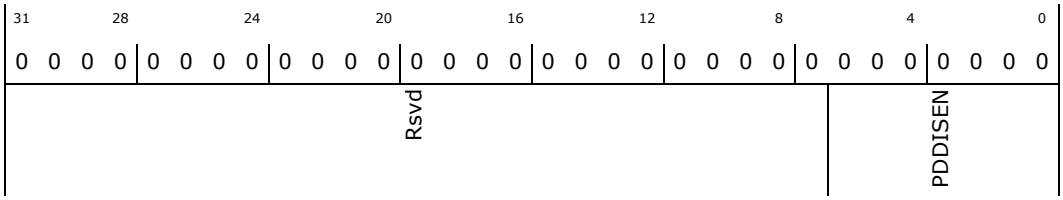
7.2.212 PDDIS_REG—Offset 8198h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8198h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**Rsvd:** Reserved. **Power Well:** SUS
6:0	0x0 RW	**PDDISEN:** Reserved. **Power Well:** SUS

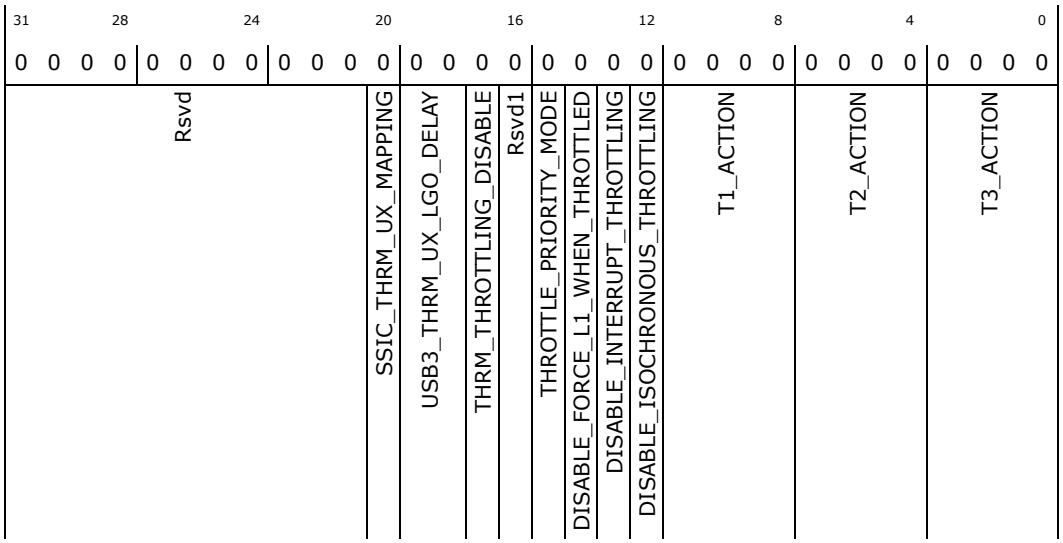
7.2.213 THRM_HOST_CTRL_REG—Offset 819Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 819Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core
20	0x0 RW	**SSIC Thermal Throttle Ux Mapping (SSIC_THRM_UX_MAPPING):** Controls if U1 or U2 is forced upon the start of thermal throttle OFF period. 0 Force ports into U2 during Thermal Throttle triggered Ux entry. 1 Force ports into U1 during Thermal Throttle triggered Ux entry. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
19:18	0x0 RW	**USB3 Thermal Throttle Ux LGO delay (USB3_THRM_UX_LGO_DELAY):** Controls the delay enforced between LMP for FLPMA and LMP for Ux LGO. After sending LPMA ON , wait for pre-defined number of clocks to initiate LGO_U1/LGO_U2 00: 8 clocks 01: 32 clocks 10: 128 clocks 11: 0 clocks This field does not apply to ports that are not operating in the mode required to issue FLMA ON. **Power Well:** Core
17	0x0 RW	**THRM_THROTTLING_DISABLE:** 0: Thermal throttling is enabled. 1: Thermal throttling is disabled. The host controller ignores the TT control inputs and does not throttle. **Power Well:** Core
16	0x0 RO	**Rsvd (Rsvd1):** Reserved. **Power Well:** Core
15	0x0 RW	**THROTTLE_PRIORITY_MODE:** 0: Off period has priority: In this case, when the throttle signal is asserted, the host controller enters the off state on the next uframe boundary, and stays in the off state for the prescribed duration or until the end of the 16 uframe throttle period whichever occurs first. On subsequent throttle periods, the off period occurs first and then the on period. 1: The On period has priority: In this case, when the throttle signal is asserted, the host controller completes the required On period first before entering the off period. If the required number of uFrames has already been executed in a 16 uframe throttle window, the controller enters the off period immediately. **Power Well:** Core
14	0x0 RW	**DISABLE_FORCE_L1_WHEN_THROTTLED:** 0: USB2 port will not force L1 entry on throttled ports. L1 entry will be based on the normal idle timeout 1: USB2 ports will attempt to enter L1 immediately after throttled ports are idle. **Power Well:** Core
13	0x0 RW	**DISABLE_INTERRUPT_THROTTLING:** 0: Interrupt traffic is throttled 1: Interrupt traffic is not throttled **Power Well:** Core
12	0x0 RW	**DISABLE_ISOCHRONOUS_THROTTLING:** 0: Isochronous traffic is throttled 1: Isochronous traffic is not throttled **Power Well:** Core
11:8	0x0 RW	**T1_ACTION:** # bus intervals to be idle for async traffic out of the 16 interval master period; from 0 to 15. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**T2_ACTION:** # bus intervals to be idle for async traffic out of the 16 interval master period; from 0 to 15. **Power Well:** Core
3:0	0x0 RW	**T3_ACTION:** # bus intervals to be idle for async traffic out of the 16 interval master period; from 0 to 15. **Power Well:** Core

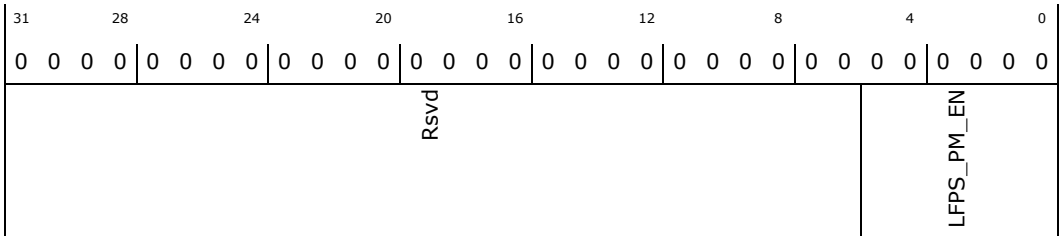
7.2.214 LFPS_PM_CTRL_REG—Offset 81A0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 81A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**Rsvd:** Reserved. **Power Well:** SUS
5:0	0x0 RW	**LFPS_PM_EN:** Reserved. **Power Well:** SUS

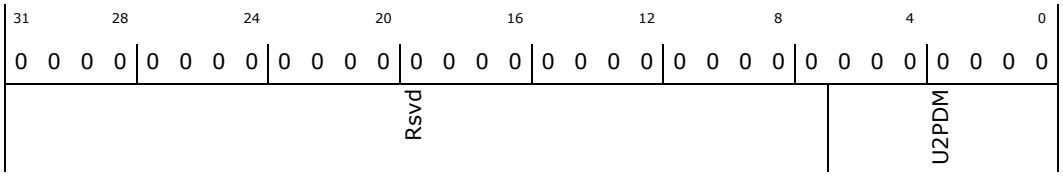
7.2.215 U2PDM—Offset 81A4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 81A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core
6:0	0x0 RW	**U2PDM:** Reserved. **Power Well:** Core

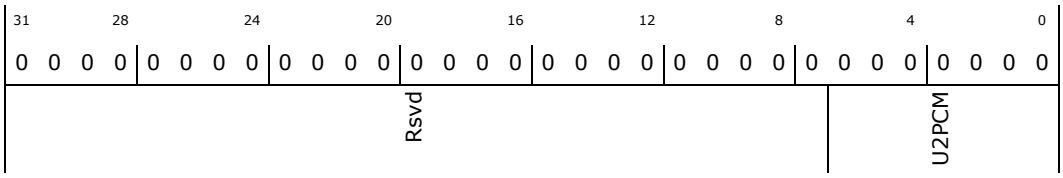
7.2.216 U2PCM—Offset 81A8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 81A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core
6:0	0x0 RW	**U2PCM:** Reserved. **Power Well:** Core

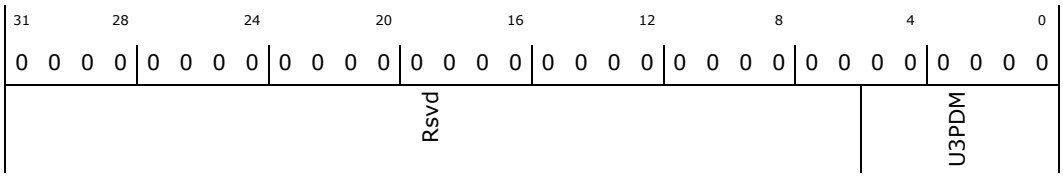
7.2.217 U3PDM—Offset 81ACh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 81ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core
5:0	0x0 RW	**U3PDM:** Reserved. **Power Well:** Core

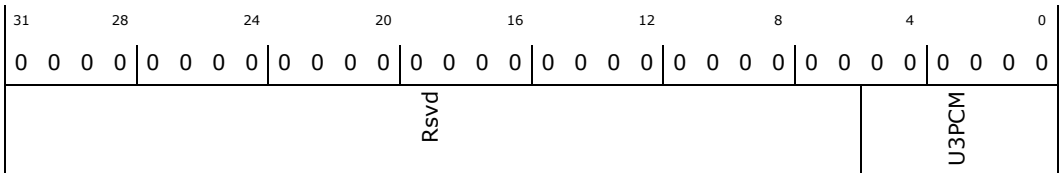
7.2.218 U3PCM—Offset 81B0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 81B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core
5:0	0x0 RW	**U3PCM:** Reserved. **Power Well:** Core

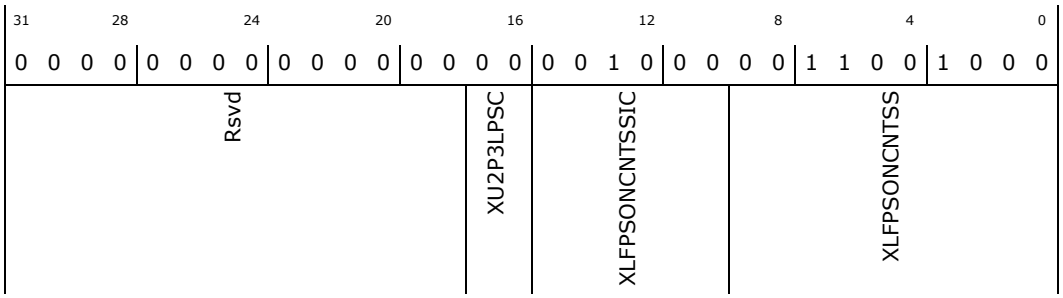
7.2.219 LFPSONCOUNT_REG—Offset 81B8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 81B8h

Default: 000020C8h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0x0 RO	**Rsvd:** Reserved. **Power Well:** SUS
17:16	0x0 RW	**U2P3 LFPS Periodic Sampling Control (XU2P3LPSC):** This field controls the OFF time for the LFPS periodic sampling for SS and SSIC ports in U2P3. If LFPSPM for a port is 1, it will override the OFF time and LFPS receiver will remain OFF permanently. For Fast Sim mode, 500us will be equivalent to 5us. 0x0 Polling Disable. (RXDET Polling will become 100ms.) 0x1 500us OFF Time 0x2 1ms OFF Time 0x3 1.5ms OFF Time **Power Well:** SUS
15:10	0x8 RW	**XLFPSONCNTSSIC:** This time would describe the number of clocks SSIC LFPS will remain ON. SSIC LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 8. **Power Well:** SUS
9:0	0xc8 RW	**XLFPSONCNTSS:** This time would describe the number of clocks LFPS will remain ON. LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 200. **Power Well:** SUS

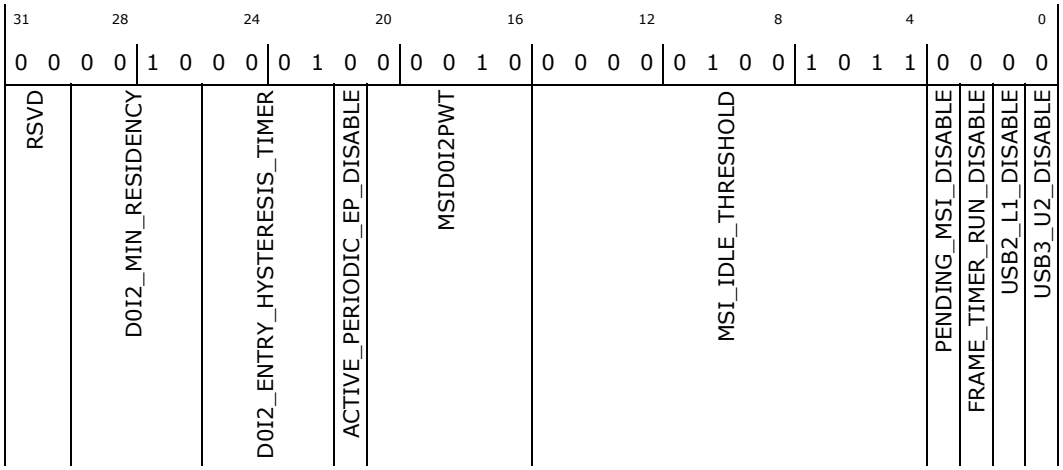
7.2.220 reg_D0i2_CTRL_REG_type (D0i2_CTRL_REG)—Offset 81BCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 81BCh

Default: 084204B0h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
29:26	0x2 RW	**D0i2 Minimum Residency (D0I2_MIN_RESIDENCY):** This field controls the minimum time that we must stay in D0i2 to ensure that the entry sequence has settled before we attempt to exit. 0h Disabled 1h 8 clocks 2h 16 clocks 3h 32 clocks 4h 128 clocks 5h 256 clocks 6h 512 clocks 7h 1024 clocks **Power Well:** SUS
25:22	0x1 RW	**D0i2 Entry Hysteresis Timer (D0I2_ENTRY_HYSTERESIS_TIMER):** This field allows for a hysteresis timer to be implemented specifically for D0i2. This will allow for D0i2 entry to be controlled independently from the timer used for D0i3 and D3. 0h Disabled 1h 8 clocks 2h 16 clocks 3h 32 clocks 4h 64 clocks 5h 128 clocks 6h 256 clocks 7h 512 clocks **Power Well:** SUS
21	0x0 RW	**Active Periodic EP Disable (ACTIVE_PERIODIC_EP_DISABLE):** This field allows the xHC to control how aggressive it enters D0i2 in the presence of active Periodic EPs. Setting this field will allow D0i2 only when there are no active Periodic EPs on the schedule. Either there are no active DB or any active Interrupt EP is flow controlled. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
20:16	0x2 RW	**MSI D0i2 Pre Wake Time (MSID0I2PWT):** This is the latency that is expected to be incurred to exit the D0i2 state. This wake latency is the latency to be added to the tracked D0i2 wake by the MSI module. Example: If while allowing D0i2 there is an MSI generation that will trigger in 250 us from now ,the MSI module will trigger a D0i2 wake up 250 us MSI D0i2 Pre Wake Time. The D0I2WL is to ensure that the act of D0i2 exit does not impact the action(s) required by the alarm(s) that was enabled prior to D0i2. 3:0 250 ns ticks 0h 0 ns 1h 250 ns . 1Fh 3750 ns **Power Well:** SUS
15:4	0x4b RW	**MSI Idle Threshold (MSI_IDLE_THRESHOLD):** This field allows the xHC to control how aggressive it enters D0i2 in the presence of pending MSI. This field is valid only if Pending MSI Disable is 0, allowing D0i2 in the presence of pending MSIs. D0i2 will be prevented if the amount of idle time between Event Ring being idle to the time an MSI will be generated does not exceed this time. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124) **Power Well:** SUS
3	0x0 RW	**Pending MSI Disable (PENDING_MSI_DISABLE):** This field allows the xHC to disable D0i2 when there are pending MSIs in the event manager. Setting this field will require all IMOD counters to be 0h and all MSIs delivered. Clearing this field will allow for D0i2 power gating while there are 1 or more IMOD counters decrementing which implies that an MSI is pending and will be generated once the corresponding IMOD counter reaches 0h. **Power Well:** SUS
2	0x0 RW	**Frame Timer Run Disable (FRAME_TIMER_RUN_DISABLE):** This field allows the xHC to disable D0i2 when the frame timer is running. Clearing this field will allow D0i2 when the frame timer is required as defined in the XHCI Spec. Setting this field will not allow D0i2 when the frame timer is required and will limit D0i2 for the condition where the frame timer is not required. **Power Well:** SUS
1	0x0 RW	**USB2 L1 Disable (USB2_L1_DISABLE):** This field allows the xHC to disable D0i2 when USB2 ports are in L1. This implies that D0i2 will only be triggered when ports are in L2 or deeper. **Power Well:** SUS
0	0x0 RW	**USB3 U2 Disable (USB3_U2_DISABLE):** This field allows the xHC to disable D0i2 when USB3 ports are in U2. This implies that D0i2 will only be triggered when ports are in U3 or deeper. **Power Well:** SUS

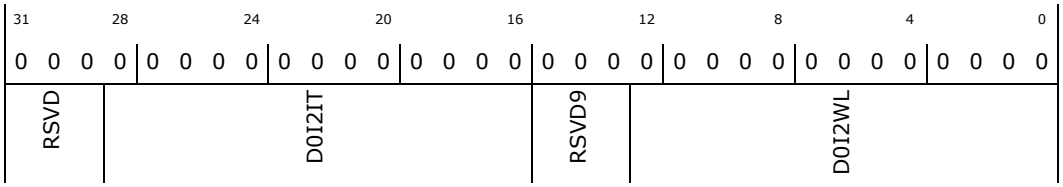
7.2.221 reg_D0i2_SCH_ALARM_CTRL_REG_type (D0i2_SCH_ALARM_CTRL_REG)—Offset 81C0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 81C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** SUS
28:16	0x0 RO	**D0i2 Idle Time (D0I2IT):** This is the minimum schedule idle time that must be available before D0i2 can allowed. 12:7 Time value in # of 125s Bus Intervals (0 8ms) 6:0 Fractional BI Time value in s (0 124s) This field controls how much scheduler idle time is required to trigger D0i2. The scheduler idle time is the same idle time that is used by other functions implementing alarm timers such as PLL shutdown, LTR and USB2 L1 override. If there is a need to require other alarm timers to have been set such as LTR has triggered a Low Idle time, then this field needs to be as aggressive as LTR Low Min Idle Time to ensure D0i2 is triggered once the scheduler has detected IDLE in the schedule. This is only to be used as alternate modes of operation or back up modes. **Power Well:** SUS
15:13	0x0 RO	**Reserved (RSVD9):** Reserved. **Power Well:** SUS
12:0	0x0 RW	**D0i2 Wake Latency (D0I2WL):** This is the latency that is expected to be incurred to exit the D0i2 state. This wake latency is the latency to be added to the tracked D0i2 wake by the scheduler. Example: If while allowing D0i2 there is an alarm that will trigger in 250 us from now , the scheduler will allow D0i2 and track this alarm with an adjustment to wake up 250ns D0I2WL) from. The D0I2WL is to ensure that the act of D0i2 exit does not impact the action(s) required by the alarm(s) that was enabled prior to D0i2. 12:7 Time value in # of 125s Bus Intervals (0 8ms) 6:0 Fractional BI Time value in s (0124s) **Power Well:** SUS

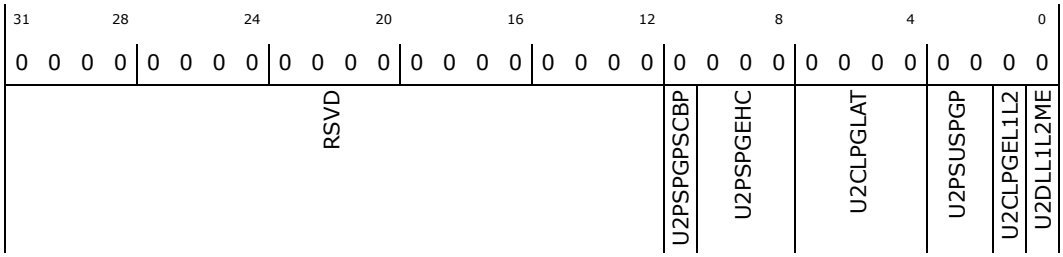
7.2.222 reg_USB2PMCTRL_REG_type (USB2PMCTRL_REG)—Offset 81C4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 81C4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** SUS
11	0x0 RW	**USB2 PHY SUS Power Gate PORTSC Block Policy (U2PSPGPSCBP):** This controls the policy for blocking PORTSC Updates while the USB2 PHY SUS Well is power gated. When set, the controller will block any updates to the PORTSC caused by port status change if the USB2 PHY SUS is power gated. 0 Do not **Power Well:** SUS
10:8	0x0 RW	**USB2 PHY SUS Well Power Gate Entry Hysteresis Count (U2PSPGEHC):** This controls the amount of hysteresis time the controller will enforce after detecting the USB2 PHY SUS Power Gate entry condition. 0h 0 clocks 1h 32 clocks 2h 64 clocks 3h 128 clocks 4h 256 clocks 5h 512 clocks 6h 1024 clocks 7h 2048 clocks **Power Well:** SUS
7:4	0x0 RW	**USB2 PHY SUS Power Gate PORTSC Block Policy (U2CLPGLAT):** This field represents the worst case latency for the USB2 Common Lane to enter and exit its power gate state. This fields is required to be compared to a ports HIRD/HIRD value for the ports that have allowed L1 to L2 mapping to determine if the Common Lane can be allowed to power off. If the power gate entry/exit latency is greater than the HIRD/HIRDD then the common lane should not be allowed to power gate as this will result in a L1 exit violation. 0h 100 us 1h 200 us 2h 300 us Eh 1500us Fh 1600 us **Power Well:** SUS
3:2	0x0 RW	**USB2 PHY SUS Well Power Gate Policy (U2PSUSPGP):** This field controls when to enable the USB2 PHY SUS Well Power Gating when the proper conditions are met. 00 USB2 PHY SUS Power Gating is Disabled. 01 USB2 PHY SUS Power Gating is Enabled in Only D0 and D0i2 (Excludes D0i3 and D3) 10 USB2 PHY SUS Power Gating is Enabled in only in D0, D0i2 and D0i3 (Excludes D3) 11 USB2 PHY SUS Power Gating is Enabled in D0/D0i2/ D0i3/D3 **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**USB2 Common Lane Power Gating Enable During L1 to L2 Mapping for USB2 PHY Power Gating (U2CLPGEL1L2):** This field when set enables the controller to allow for the common lane power gating to be enabled when all ports are exposed as in L2 to the USB2 PHY while at least 1 port has been mapped to L2 from L1. This field alone does not guarantee power gating since the L1 HIRD/HIRDD Value must be compared with the PHYs power gate exit latency (U2CLPGLAT) held in this register to ensure that L1 exit is not violated. 0 USB2 Common Lane Power Gating is disabled when any port has been mapped from L1 to L2. 1 USB2 Common Lane Power Gating is allowed when any port has been mapped to L2 from L1 with the additional condition that the HIRD/HIRDD is greater than the PHYs Power Gate exit latency. **Power Well:** SUS
0	0x0 RW	**USB2 Data Lane L1 to L2 Mapping Enable for USB2 PHY Power Gating (U2DLL1L2ME):** This field when set enables the controller to map an L1 entry directly to L2 to allow the USB2 PHY to trigger its Autonomous Power Gating. The USB2 PHY will trigger PG only when in L2 since it does not fully understand the requirements for L1. 0 USB2 L1 to L2 mapping is disabled for all ports 1 USB2 L1 to L2 mapping is enabled for all ports **Power Well:** SUS

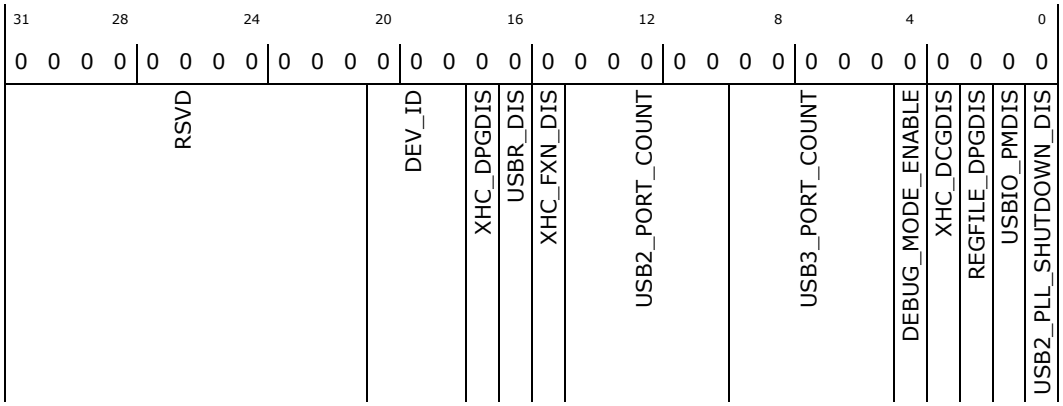
7.2.223 FUS1_REG—Offset 8410h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8410h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RO	**RSVD:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
20:18	0x0 RO	**DEV_ID:** Provides a fuse over-ride for the lower 3 bits of device ID. **Power Well:** Core
17	0x0 RO	**XHC_DPGDIS:** When asserted, it indicates that the xHCI will not dynamically power gate the controller. **Power Well:** Core
16	0x0 RO	**USBR_DIS:** When asserted, it indicates that xHCI does not support USBr **Power Well:** Core
15	0x0 RO	**XHC_FXN_DIS:** When asserted, it indicates the xHCI is fused to function disabled. **Power Well:** Core
14:10	0x0 RO	**USB2_PORT_COUNT:** 0x0 = MAX USB2 Ports enabled 0x1 = Max USB2 Ports -1 enabled 0x1F = All ports disabled **Power Well:** Core
9:5	0x0 RO	**USB3_PORT_COUNT:** 0x0 = MAX USB3 Ports enabled 0x1 = Max USB3 Ports -1 enabled 0x1F = All ports disabled **Power Well:** Core
4	0x0 RO	**DEBUG_MODE_ENABLE:** 0 = USB debug mode disabled 1 = USB debug mode enabled. **Power Well:** Core
3	0x0 RO	**XHC_DCGDIS:** 0= USB3 (xHC) dynamic clock gating enabled 1= USB3 (xHC) dynamic clock gating disabled **Power Well:** Core
2	0x0 RO	**REGFILE_DPGDIS:** 0 = USB3 (xHC) dynamic RF power gating enabled 1 = USB3 (xHC) dynamic RF power gating disabled **Power Well:** Core
1	0x0 RO	**USBIO_PMDIS:** 0=USB2 HW LPM and USB3 HW Ux under xHC enabled 1= USB2 HW LPM and USB3 HW Ux under xHC disabled **Power Well:** Core
0	0x0 RO	**USB2_PLL_SHUTDOWN_DIS:** 0= USB2 PLL Shutdown enabled 1= USB2 PLL Shutdown disabled **Power Well:** Core

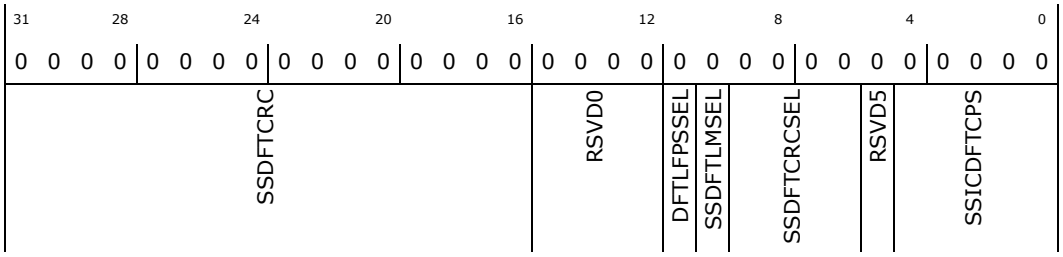
7.2.224 DFT_REG1—Offset 8430h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8430h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**SS/SSIC DFT CRC (SSDFTCRC):** These register bits contain the value of SS DFT CRC **Power Well:** Core
15:12	0x0 RO	**RSVD0:** RSVD0 **Power Well:** Core
11	0x0 RW	**DFTLFPSSEL:** DFTLFPSSEL 0: Rxelecidle is driven from GPIO Pin 1: Rxelecidle is Driven as specified by Super Speed DFT LFPS Mode Select **Power Well:** Core
10	0x0 RW	**Super Speed DFT LFPS Mode Select (SSDFTLMSEL):** This bit selects the Super Speed DFT LFPS mode, and will only take effect when Super Speed HBP mode is enabled. 0b: HBP logic will internally loopback TX LFPS as RX LFPS and AFE RX LFPS path to the controller is disconnected. 1b: RX LFPS path works normally **Power Well:** Core
9:6	0x0 RW	**SS/SSIC DFT CRC Select (SSDFTCRCSEL):** These bits select which Super Speed DFT CRC value is reflected in SSDFTCRC bits. In addition, these bits also select which SuperSpeed DFT CRC MSB value is sent to GPIO monitor pin, i.e. sata3gp_gp37 to aid silicon debug. Live version of selected CRC's MSB will be- sent to GPIO monitor pin, i.e. sata3gp_gp37. 0h (default): No SuperSpeed DFT CRC is selected. 1h: Data Payload CRC 2h: Link Management Packet CRC 3h: Transaction Packet CRC 4h: Isochronous Timestamp Packet CRC 5h: Data Packet Header CRC 6h: Link Command Packet CRC 7h: RRAP Packet CRC 8h: Tx/Rx Cfg CRC Others: Reserved Note : CRC types 7 and 8 are only applicable if Port is SSIC Port **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RO	**RSVD5:** RSVD5 **Power Well:** Core
4:0	0x0 RW	**SS/SSIC DFT CRC Port Select (SSICDFTCPS):** One CRC per packet type is shared for all the Super Speed ports. These bits select the Super Speed port for which CRC data will be updated. 000b: (default) No SuperSpeed Port is selected 001b: SS/SSIC Port 0 010b: SS/SSIC Port 1 011b: SS/SSIC Port 2 100b: SS/SSIC Port 3 101b: SS/SSIC PORT4 110b :SS/SSIC Port 5 others : Rsvd **Power Well:** Core

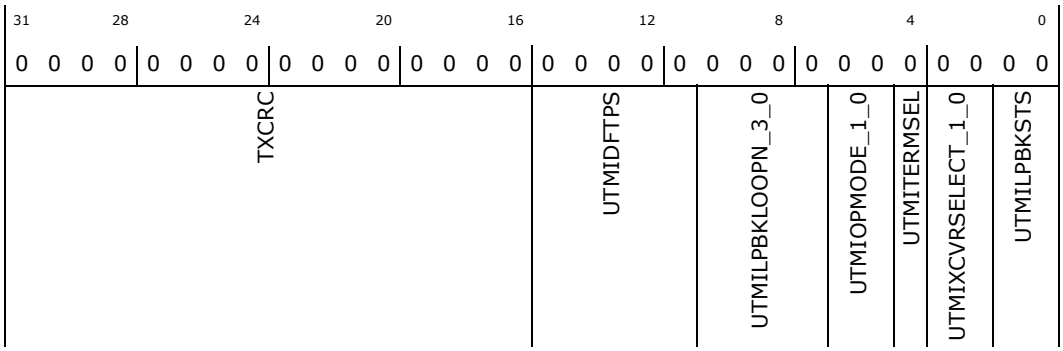
7.2.225 DFT_REG2—Offset 8434h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8434h

Default: 00000000h



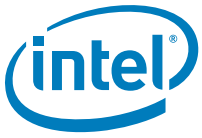
Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**HS/HSIC TX CRC (TXCRC):** These register bits contain the value of TX CRC. This TX CRC is placed right after the 480MHz XCLKQ. **Power Well:** Core
15:11	0x0 RW	**HSIC/UTMI+ DFT Port Select (UTMIDFTPS):** One CRC is shared for all the UTMI+ ports. These bits select the UTMI+ port for which CRC data will be updated and loopback status reflected in UTMILPBKSTS. 0h: (default) No UTMI+ Port is selected 1h: UTMI+ Port 0 2h: UTMI+ Port 1 3h: UTMI+ Port 2 4h: UTMI+ Port 3 5h: UTMI+ Port 4 6h: UTMI+ Port 5 7h: UTMI+ Port 6 8h: UTMI+ Port 7 9h: UTMI+ Port 8 Ah: UTMI+ Port 9 Bh: UTMI+ Port 10 Ch: UTMI+ Port 11 Dh: UTMI+ Port 12 Eh: UTMI+ Port 13 Others: Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
10:7	0x0 RW	**Loop Number (UTMILPBKLOOPN_3_0):** Number of repeatable fixed pattern within a packet Note: Connect register bit 3 to counter bit 7, register bit 2 to counter bit 5, register bit 1 to counter bit 3, register bit 0 to counter bit 1. Counter bits 6, 4, 2 and 0 will be tied off to 0. Hence, the programmable loop number shall be: 0000b: 0 loop 0001b: 2 loops 0010b: 8 loops 0011b: 10 loops 1100b: 160 loops 1101b: 162 loops 1110b: 168 loops 1111b: 170 loops (max) +E27 **Power Well:** Core
6:5	0x0 RW	**Operational Mode (UTMIOPMODE_1_0):** Operational Mode in test mode. These signals select between various operational modes: 00b: Normal Operation 01b: Non-Driving 10b: Disable Bit Stuffing and NRZI encoding 11b: Reserved **Power Well:** Core
4	0x0 RW	**Termination Select (UTMITERMSEL):** Termination Select in test mode. This signal selects between the FS and HS terminations: 0b: HS termination enabled 1b: FS termination enabled **Power Well:** Core
3:2	0x0 RW	**Transceiver Select (UTMIXCVRSELECT_1_0):** Transceiver Select in test mode. This signal selects between the LS, FS and HS transceivers: 00b: HS transceiver enabled 01b: FS transceiver enabled 10b: LS transceiver enabled 11b: Reserved **Power Well:** Core
1:0	0x0 RW	**UTMI+ Loopback Status (UTMILPBKSTS):** Loopback Status for port selected by UTMIDFTPS 00b: Reset condition 01b: Comparator has started receiving data and the received data matches with the TX pattern. 10b: Comparator has started receiving data the received data does not match with the TX pattern but there was no assertion of RC error from UTMI. 11b: Comparator has started receiving data and RX ERROR was asserted for at least one clock by UTMI. Note that this does not reflect the status of pattern comparison since RX error from UTMI is unexpected for loopback. **Power Well:** Core

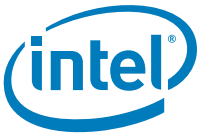
7.3 USB xHCI Memory Mapped I/O Registers Address Map

Table 39. Summary of Memory Mapped I/O Registers—MBAR

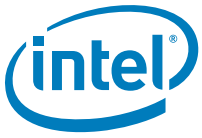
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8438–843Bh	4	"DFT_REG3—Offset 8438h" on page 2714	00000000h
843C–843Fh	4	"dft_reg4 (DFT_REG4)—Offset 843Ch" on page 2299	00000000h
8440–8443h	4	"dft_reg5 (DFT_REG5)—Offset 8440h" on page 2299	00000000h
8448–844Bh	4	"XECP_CMDM_STS0—Offset 8448h" on page 2300	00000000h
844C–844Fh	4	"XECP_CMDM_STS1—Offset 844Ch" on page 2303	03FC0000h
8450–8453h	4	"XECP_CMDM_STS2—Offset 8450h" on page 2303	00000000h
8454–8457h	4	"XECP_CMDM_STS3—Offset 8454h" on page 2304	00000000h
8458–845Bh	4	"XECP_CMDM_STS4—Offset 8458h" on page 2304	00000000h
845C–845Fh	4	"XECP_CMDM_STS5—Offset 845Ch" on page 2305	00000000h
8460–8463h	4	"AUX Power PHY Reset (UPORTS_PON_RST_REG)—Offset 8460h" on page 2305	00000000h
8464–8467h	4	"Latency Tolerance Control 0 (HOST_IF_LAT_TOL_CTRL_REG0)—Offset 8464h" on page 2306	000D0000h
846C–846Fh	4	"USB Legacy Support Capability (USBLEGSUP)—Offset 846Ch" on page 2307	00002501h
8470–8473h	4	"USB Legacy Support Control Status (USBLEGCTLSTS)—Offset 8470h" on page 2308	00000000h
84F4–84F7h	4	"Port Disable Override capability register (PDO_CAPABILITY)—Offset 84F4h" on page 2309	000003C6h
84F8–84FBh	4	"USB2 Port Disable Override (USB2PDO)—Offset 84F8h" on page 2310	00000000h
84FC–84FFh	4	"USB3 Port Disable Override (USB3PDO)—Offset 84FCh" on page 2310	00000000h
8500–8503h	4	"HW state capability register (HW_STATE_CAPABILITY)—Offset 8500h" on page 2311	001D40C7h
8504–8507h	4	"HW state register 1 (HW_STATE_REG1)—Offset 8504h" on page 2311	00000000h
8508–850Bh	4	"HW state register 2 (HW_STATE_REG2)—Offset 8508h" on page 2312	00000000h
850C–850Fh	4	"HW state register 3 (HW_STATE_REG3)—Offset 850Ch" on page 2312	00000000h
8510–8513h	4	"HW state register 4 (HW_STATE_REG4)—Offset 8510h" on page 2313	00000000h
8600–8603h	4	"CONFIG mirror capability register (CONFIG_MIRROR_CAPABILITY)—Offset 8600h" on page 2314	000040C2h
8604–8605h	2	"Command (CMD_MMIO)—Offset 8604h" on page 2314	0000h



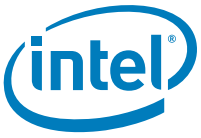
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8606–8607h	2	"Device Status (STS_MMIO)—Offset 8606h" on page 2316	0290h
8608–8608h	1	"Revision ID (RID_MMIO)—Offset 8608h" on page 2317	00h
8609–8609h	1	"Programming Interface (PI_MMIO)—Offset 8609h" on page 2318	30h
860A–860Ah	1	"Sub Class Code (SCC_MMIO)—Offset 860Ah" on page 2318	03h
860B–860Ch	2	"Base Class Code (BCC_MMIO)—Offset 860Bh" on page 2318	0Ch
860D–860Dh	1	"Master Latency Timer (MLT_MMIO)—Offset 860Dh" on page 2319	00h
860E–860Fh	2	"Header Type (HT_MMIO)—Offset 860Eh" on page 2319	00h
8610–8617h	8	"Memory Base Address (MBAR_MMIO)—Offset 8610h" on page 2320	0000000000000004h
862C–862Dh	2	"USB Subsystem Vendor ID (SSVID_MMIO)—Offset 862Ch" on page 2321	0000h
862E–862Fh	2	"USB Subsystem ID (SSID_MMIO)—Offset 862Eh" on page 2321	0000h
8634–8634h	1	"Capabilities Pointer (CAP_PTR_MMIO)—Offset 8634h" on page 2322	70h
863C–863Ch	1	"Interrupt Line (ILINE_MMIO)—Offset 863Ch" on page 2322	00h
863D–863Fh	3	"Interrupt Pin (IPIN_MMIO)—Offset 863Dh" on page 2323	00h
8658–865Bh	4	"Audio Time Synchronization (AUDSYNC_MMIO)—Offset 8658h" on page 2323	00000000h
8660–8660h	1	"Serial Bus Release Number (SBRN_MMIO)—Offset 8660h" on page 2324	30h
8661–8661h	1	"Frame Length Adjustment (FLADJ_MMIO)—Offset 8661h" on page 2324	60h
8662–8662h	1	"Best Effort Service Latency (BESL_MMIO)—Offset 8662h" on page 2326	00h
8670–8670h	1	"PCI Power Management Capability ID (PM_CID_MMIO)—Offset 8670h" on page 2326	01h
8671–8671h	1	"Next Item Pointer #1 (PM_NEXT_MMIO)—Offset 8671h" on page 2327	80h
8672–8673h	2	"Power Management Capabilities (PM_CAP_MMIO)—Offset 8672h" on page 2327	C1C2h
8674–8675h	2	"Power Management Control/Status (PM_CS_MMIO)—Offset 8674h" on page 2328	0008h
8680–8680h	1	"Message Signaled Interrupt CID (MSI_CID_MMIO)—Offset 8680h" on page 2330	05h
8681–8681h	1	"Next item pointer (MSI_NEXT_MMIO)—Offset 8681h" on page 2330	00h
8682–8683h	2	"Message Signaled Interrupt Message Control (MSI_MCTL_MMIO)—Offset 8682h" on page 2331	0086h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8684–8687h	4	"Message Signaled Interrupt Message Address (MSI_MAD_MMIO)—Offset 8684h" on page 2332	00000000h
8688–868Bh	4	"Message Signaled Interrupt Upper Address (MSI_MUAD_MMIO)—Offset 8688h" on page 2332	00000000h
868C–868Dh	2	"Message Signaled Interrupt Message Data (MSI_MD_MMIO)—Offset 868Ch" on page 2333	0000h
8694–8697h	4	"Fuse and Strap (FUS_MMIO)—Offset 8694h" on page 2333	00000000h
86A4–86A7h	4	"High Speed Configuration 2 (HSCFG2_MMIO)—Offset 86A4h" on page 2335	00002000h
86B0–86B3h	4	"XHCI USB2 Overcurrent Pin Mapping 1 (U2OCM1_MMIO)—Offset 86B0h" on page 2337	00000000h
86B4–86B7h	4	"XHCI USB2 Overcurrent Pin Mapping 2 (U2OCM2_MMIO)—Offset 86B4h" on page 2337	00000000h
86D0–86D3h	4	"XHCI USB3 Overcurrent Pin Mapping 1 (U3OCM1_MMIO)—Offset 86D0h" on page 2338	00000000h
86D4–86D7h	4	"XHCI USB3 Overcurrent Pin Mapping 2 (U3OCM2_MMIO)—Offset 86D4h" on page 2339	00000000h
8700–8703h	4	"Debug Capability ID Register (DCID)—Offset 8700h" on page 2339	0005100Ah
8704–8707h	4	"Debug Capability Doorbell Register (DCDB)—Offset 8704h" on page 2340	00000000h
8708–870Bh	4	"Debug Capability Event Ring Segment Table Size Register (DCERSTSZ)—Offset 8708h" on page 2341	00000000h
8710–8717h	8	"Debug Capability Event Ring Segment Table Base Address Register (DCERSTBA)—Offset 8710h" on page 2341	0000000000000000h
8718–871Fh	8	"Debug Capability Event Ring Dequeue Pointer Register (DCERDP)—Offset 8718h" on page 2342	0000000000000000h
8720–8723h	4	"Debug Capability Control Register (DCCTRL)—Offset 8720h" on page 2342	00000000h
8724–8727h	4	"Debug Capability Status Register (DCST)—Offset 8724h" on page 2343	00000000h
8728–872Bh	4	"Debug Capability Port Status and Control Register (DCPORTSC)—Offset 8728h" on page 2344	00000080h
8730–8737h	8	"Debug Capability Context Pointer Register (DCCP)—Offset 8730h" on page 2347	0000000000000000h
8738–873Bh	4	"Debug Capability Device Descriptor Info Register 1 (DCDDI1)—Offset 8738h" on page 2347	00000000h
873C–873Fh	4	"Debug Capability Device Descriptor Info Register 2 (DCDDI2)—Offset 873Ch" on page 2348	00000000h
8740–8743h	4	"Debug Capability Descriptor Parameters (DCDP)—Offset 8740h" on page 2348	000030C3h
8748–874Bh	4	"Debug Device Control ODMA (DBGDEV_CTRL_ODMA_REG)—Offset 8748h" on page 2349	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8800–8803h	4	"SSIC Policy and Implementation Specific Registers Capability ID register (SSIC_IMPLEMENTATION_CAPABILITY_ID_REG)—Offset 8800h" on page 2351	000040C4h
8804–8807h	4	"SSIC global configuration control register (SSIC_GLOBAL_CONFIG_CONTROL_REG)—Offset 8804h" on page 2351	00000000h
8808–880Bh	4	"reg_SSIC_CONFIG_REG1_type (PORT1_SSIC_CONFIG_REG1)—Offset 8808h" on page 2353	82286000h
880C–880Fh	4	"reg_SSIC_CONFIG_REG2_type (PORT1_SSIC_CONFIG_REG2)—Offset 880Ch" on page 2354	04821F46h
8810–8813h	4	"reg_SSIC_CONFIG_REG3_type (PORT1_SSIC_CONFIG_REG3)—Offset 8810h" on page 2356	40480000h
8814–8817h	4	"reg_SSIC_CONFIG_REG4_type (PORT1_SSIC_CONFIG_REG4)—Offset 8814h" on page 2357	64796464h
8818–881Bh	4	"reg_SSIC_LOOPBACK_CONFIG_REG_type (PORT1_SSIC_LOOPBACK_CONFIG_REG)—Offset 8818h" on page 2358	00000000h
881C–881Fh	4	"reg_SSIC_LOOPBACK_BURST_COUNT_REG_type (PORT1_SSIC_LOOPBACK_BURST_COUNT_REG)—Offset 881Ch" on page 2359	00000000h
8820–8823h	4	"reg_SSIC_LOOPBACK_ERROR_COUNT_REG_type (PORT1_SSIC_LOOPBACK_ERROR_COUNT_REG)—Offset 8820h" on page 2360	00000000h
8838–883Bh	4	"reg_SSIC_CONFIG_REG1_type (PORT2_SSIC_CONFIG_REG1)—Offset 8838h" on page 2361	82286000h
883C–883Fh	4	"reg_SSIC_CONFIG_REG2_type (PORT2_SSIC_CONFIG_REG2)—Offset 883Ch" on page 2363	04821F46h
8840–8843h	4	"reg_SSIC_CONFIG_REG3_type (PORT2_SSIC_CONFIG_REG3)—Offset 8840h" on page 2364	40480000h
8844–8847h	4	"reg_SSIC_CONFIG_REG4_type (PORT2_SSIC_CONFIG_REG4)—Offset 8844h" on page 2365	64796464h
8848–884Bh	4	"reg_SSIC_LOOPBACK_CONFIG_REG_type (PORT2_SSIC_LOOPBACK_CONFIG_REG)—Offset 8848h" on page 2366	00000000h
884C–884Fh	4	"reg_SSIC_LOOPBACK_BURST_COUNT_REG_type (PORT2_SSIC_LOOPBACK_BURST_COUNT_REG)—Offset 884Ch" on page 2367	00000000h
8850–8853h	4	"reg_SSIC_LOOPBACK_ERROR_COUNT_REG_type (PORT2_SSIC_LOOPBACK_ERROR_COUNT_REG)—Offset 8850h" on page 2368	00000000h
8900–8903h	4	"SSIC Local and Remote Profile Registers Capability ID register (SSIC_PROFILE_CAPABILITY_ID_REG)—Offset 8900h" on page 2369	000000C5h



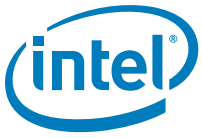
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8904–8907h	4	"SSIC Port N Register Access Control (PORT1_REGISTER_ACCESS_CONTROL)—Offset 8904h" on page 2370	00C00000h
8908–890Bh	4	"SSIC Port N Register Access Status (PORT1_REGISTER_ACCESS_STATUS)—Offset 8908h" on page 2371	00000000h
890C–890Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG0)—Offset 890Ch" on page 2372	00000000h
8910–8913h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG1)—Offset 8910h" on page 2373	00000000h
8914–8917h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG2)—Offset 8914h" on page 2374	00000000h
8918–891Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG3)—Offset 8918h" on page 2374	00000000h
891C–891Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG4)—Offset 891Ch" on page 2375	00000000h
8920–8923h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG5)—Offset 8920h" on page 2376	00000000h
8924–8927h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG6)—Offset 8924h" on page 2377	00000000h
8928–892Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG7)—Offset 8928h" on page 2378	00000000h
892C–892Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG8)—Offset 892Ch" on page 2379	00000000h
8930–8933h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG9)—Offset 8930h" on page 2380	00000000h
8934–8937h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG10)—Offset 8934h" on page 2380	00000000h
8938–893Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG11)—Offset 8938h" on page 2381	00000000h
893C–893Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG12)—Offset 893Ch" on page 2382	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8940–8943h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG13)—Offset 8940h" on page 2383	00000000h
8944–8947h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG14)—Offset 8944h" on page 2384	00000000h
8948–894Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG15)—Offset 8948h" on page 2385	00000000h
894C–894Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG16)—Offset 894Ch" on page 2386	00000000h
8950–8953h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG17)—Offset 8950h" on page 2386	00000000h
8954–8957h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG18)—Offset 8954h" on page 2387	00000000h
8958–895Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG19)—Offset 8958h" on page 2388	00000000h
895C–895Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG20)—Offset 895Ch" on page 2389	00000000h
8960–8963h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG21)—Offset 8960h" on page 2390	00000000h
8964–8967h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG22)—Offset 8964h" on page 2391	00000000h
8968–896Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG23)—Offset 8968h" on page 2392	00000000h
896C–896Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG24)—Offset 896Ch" on page 2392	00000000h
8970–8973h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG25)—Offset 8970h" on page 2393	00000000h
8974–8977h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG26)—Offset 8974h" on page 2394	00000000h
8978–897Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG27)—Offset 8978h" on page 2395	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
897C–897Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG28)—Offset 897Ch" on page 2396	00000000h
8980–8983h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG29)—Offset 8980h" on page 2397	00000000h
8984–8987h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG30)—Offset 8984h" on page 2398	00000000h
8988–898Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG31)—Offset 8988h" on page 2398	00000000h
898C–898Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG32)—Offset 898Ch" on page 2399	00000000h
8990–8993h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG33)—Offset 8990h" on page 2400	00000000h
8994–8997h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG34)—Offset 8994h" on page 2401	00000000h
8998–899Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG35)—Offset 8998h" on page 2402	00000000h
899C–899Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG36)—Offset 899Ch" on page 2403	00000000h
89A0–89A3h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG37)—Offset 89A0h" on page 2404	00000000h
89A4–89A7h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG38)—Offset 89A4h" on page 2404	00000000h
89A8–89ABh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG39)—Offset 89A8h" on page 2405	00000000h
89AC–89AFh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG40)—Offset 89ACh" on page 2406	00000000h
89B0–89B3h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG41)—Offset 89B0h" on page 2407	00000000h
89B4–89B7h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG42)—Offset 89B4h" on page 2408	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
89B8–89BBh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG43)—Offset 89B8h" on page 2409	00000000h
89BC–89BFh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG44)—Offset 89BCh" on page 2410	00000000h
89C0–89C3h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG45)—Offset 89C0h" on page 2410	00000000h
89C4–89C7h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG46)—Offset 89C4h" on page 2411	00000000h
89C8–89CBh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG47)—Offset 89C8h" on page 2412	00000000h
89CC–89CFh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG48)—Offset 89CCh" on page 2413	00000000h
89D0–89D3h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG49)—Offset 89D0h" on page 2414	00000000h
89D4–89D7h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG50)—Offset 89D4h" on page 2415	00000000h
89D8–89DBh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG51)—Offset 89D8h" on page 2416	00000000h
89DC–89DFh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG52)—Offset 89DCh" on page 2416	00000000h
89E0–89E3h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG53)—Offset 89E0h" on page 2417	00000000h
89E4–89E7h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG54)—Offset 89E4h" on page 2418	00000000h
89E8–89EBh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG55)—Offset 89E8h" on page 2419	00000000h
89EC–89EFh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG56)—Offset 89ECh" on page 2420	00000000h
89F0–89F3h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG57)—Offset 89F0h" on page 2421	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
89F4–89F7h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG58)—Offset 89F4h" on page 2422	00000000h
89F8–89FBh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG59)—Offset 89F8h" on page 2422	00000000h
89FC–89FFh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG60)—Offset 89FCh" on page 2423	00000000h
8A00–8A03h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG61)—Offset 8A00h" on page 2424	00000000h
8A04–8A07h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG62)—Offset 8A04h" on page 2425	00000000h
8A08–8A0Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG63)—Offset 8A08h" on page 2426	00000000h
8A14–8A17h	4	"SSIC Port N Register Access Control (PORT2_REGISTER_ACCESS_CONTROL)—Offset 8A14h" on page 2427	00C00000h
8A18–8A1Bh	4	"SSIC Port N Register Access Status (PORT2_REGISTER_ACCESS_STATUS)—Offset 8A18h" on page 2428	00000000h
8A1C–8A1Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG0)—Offset 8A1Ch" on page 2429	00000000h
8A20–8A23h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG1)—Offset 8A20h" on page 2430	00000000h
8A24–8A27h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG2)—Offset 8A24h" on page 2430	00000000h
8A28–8A2Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG3)—Offset 8A28h" on page 2431	00000000h
8A2C–8A2Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG4)—Offset 8A2Ch" on page 2432	00000000h
8A30–8A33h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG5)—Offset 8A30h" on page 2433	00000000h
8A34–8A37h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG6)—Offset 8A34h" on page 2434	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8A38–8A3Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG7)—Offset 8A38h" on page 2435	00000000h
8A3C–8A3Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG8)—Offset 8A3Ch" on page 2436	00000000h
8A40–8A43h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG9)—Offset 8A40h" on page 2436	00000000h
8A44–8A47h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG10)—Offset 8A44h" on page 2437	00000000h
8A48–8A4Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG11)—Offset 8A48h" on page 2438	00000000h
8A4C–8A4Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG12)—Offset 8A4Ch" on page 2439	00000000h
8A50–8A53h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG13)—Offset 8A50h" on page 2440	00000000h
8A54–8A57h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG14)—Offset 8A54h" on page 2441	00000000h
8A58–8A5Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG15)—Offset 8A58h" on page 2442	00000000h
8A5C–8A5Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG16)—Offset 8A5Ch" on page 2442	00000000h
8A60–8A63h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG17)—Offset 8A60h" on page 2443	00000000h
8A64–8A67h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG18)—Offset 8A64h" on page 2444	00000000h
8A68–8A6Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG19)—Offset 8A68h" on page 2445	00000000h
8A6C–8A6Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG20)—Offset 8A6Ch" on page 2446	00000000h
8A70–8A73h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG21)—Offset 8A70h" on page 2447	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8A74–8A77h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG22)—Offset 8A74h" on page 2448	00000000h
8A78–8A7Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG23)—Offset 8A78h" on page 2448	00000000h
8A7C–8A7Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG24)—Offset 8A7Ch" on page 2449	00000000h
8A80–8A83h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG25)—Offset 8A80h" on page 2450	00000000h
8A84–8A87h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG26)—Offset 8A84h" on page 2451	00000000h
8A88–8A8Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG27)—Offset 8A88h" on page 2452	00000000h
8A8C–8A8Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG28)—Offset 8A8Ch" on page 2453	00000000h
8A90–8A93h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG29)—Offset 8A90h" on page 2454	00000000h
8A94–8A97h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG30)—Offset 8A94h" on page 2454	00000000h
8A98–8A9Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG31)—Offset 8A98h" on page 2455	00000000h
8A9C–8A9Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG32)—Offset 8A9Ch" on page 2456	00000000h
8AA0–8AA3h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG33)—Offset 8AA0h" on page 2457	00000000h
8AA4–8AA7h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG34)—Offset 8AA4h" on page 2458	00000000h
8AA8–8AABh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG35)—Offset 8AA8h" on page 2459	00000000h
8AAC–8AAFh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG36)—Offset 8AACh" on page 2460	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8AB0–8AB3h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG37)—Offset 8AB0h" on page 2460	00000000h
8AB4–8AB7h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG38)—Offset 8AB4h" on page 2461	00000000h
8AB8–8ABBh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG39)—Offset 8AB8h" on page 2462	00000000h
8ABC–8ABFh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG40)—Offset 8ABCh" on page 2463	00000000h
8AC0–8AC3h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG41)—Offset 8AC0h" on page 2464	00000000h
8AC4–8AC7h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG42)—Offset 8AC4h" on page 2465	00000000h
8AC8–8ACBh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG43)—Offset 8AC8h" on page 2466	00000000h
8ACC–8ACFh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG44)—Offset 8ACCh" on page 2466	00000000h
8AD0–8AD3h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG45)—Offset 8AD0h" on page 2467	00000000h
8AD4–8AD7h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG46)—Offset 8AD4h" on page 2468	00000000h
8AD8–8ADBh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG47)—Offset 8AD8h" on page 2469	00000000h
8ADC–8ADFh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG48)—Offset 8ADCh" on page 2470	00000000h
8AE0–8AE3h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG49)—Offset 8AE0h" on page 2471	00000000h
8AE4–8AE7h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG50)—Offset 8AE4h" on page 2472	00000000h
8AE8–8AEBh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG51)—Offset 8AE8h" on page 2472	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8AEC–8AEFh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG52)—Offset 8AECh" on page 2473	00000000h
8AF0–8AF3h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG53)—Offset 8AF0h" on page 2474	00000000h
8AF4–8AF7h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG54)—Offset 8AF4h" on page 2475	00000000h
8AF8–8AFBh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG55)—Offset 8AF8h" on page 2476	00000000h
8AFC–8AFFh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG56)—Offset 8AFCh" on page 2477	00000000h
8B00–8B03h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG57)—Offset 8B00h" on page 2478	00000000h
8B04–8B07h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG58)—Offset 8B04h" on page 2478	00000000h
8B08–8B0Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG59)—Offset 8B08h" on page 2479	00000000h
8B0C–8B0Fh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG60)—Offset 8B0Ch" on page 2480	00000000h
8B10–8B13h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG61)—Offset 8B10h" on page 2481	00000000h
8B14–8B17h	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG62)—Offset 8B14h" on page 2482	00000000h
8B18–8B1Bh	4	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG63)—Offset 8B18h" on page 2483	00000000h

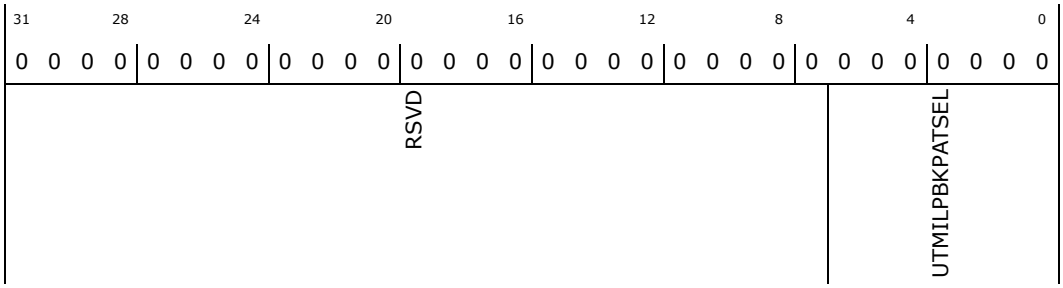
7.3.1 dft_reg4 (DFT_REG4)—Offset 843Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 843Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RW	**RSVD:** Reserved. **Power Well:** Core
6:0	0x0 RW	**Loopback Pattern (UTMILPBKPATSEL):** Loopback Lane Select (UTMILPBKSEL): Port is selected if the corresponding bit (zero based) is selected Bit 0 = Port 1 Bit 1 = Port 2 Etc. **Power Well:** Core

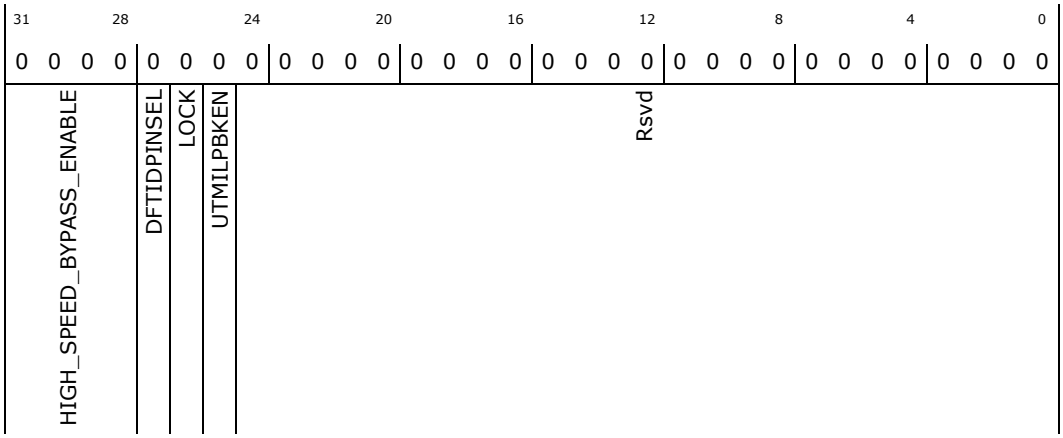
7.3.2 dft_reg5 (DFT_REG5)—Offset 8440h

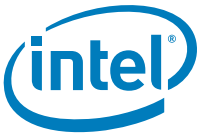
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8440h

Default: 00000000h





Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW/L	**High Speed Bypass Enable (HIGH_SPEED_BYPASS_ENABLE):** 0000 - Disable all HBP 0001 - Enable SS HBP 0010 - Enable HS HBP 0011 - Enable HSIC HBP 0100 - Enable SSIC HBP Others - Reserved **Power Well:** Core
27	0x0 RW	**DFTIDPINSEL (DFTIDPINSEL):** Select Between Device and Host Controller in HBP mode 0h : Device Controller is selected 1h : Host Controller is selected **Power Well:** Core
26	0x0 RW/O	**Lock Bit (LOCK):** This bit is used by BIOS to lock/unlock lockable bits. When set to '1' the write access to HBP Enable is disabled (locked state). When set to '0', the write access to bit locked are enable (unlocked state). Writable once after platform reset. **Power Well:** Core
25	0x0 RW	**Loopback Enable (UTMILPBKEN):** Enable loopback test mode. If asserted, loopback test mode is enabled **Power Well:** Core
24:0	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core

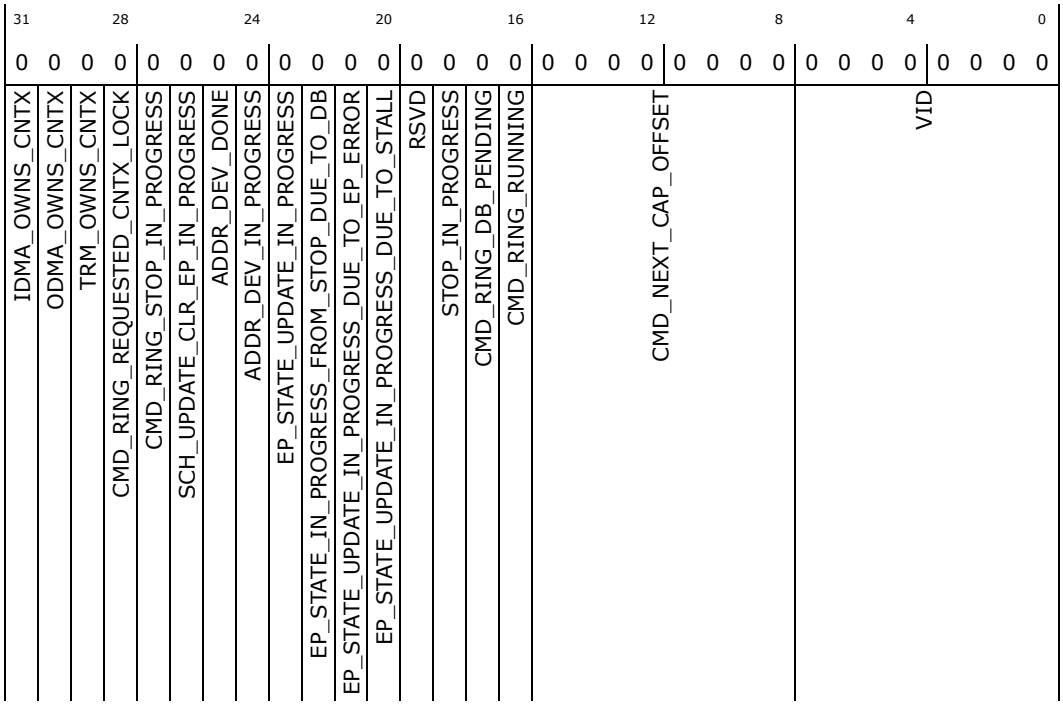
7.3.3 XECP_CMDM_STS0—Offset 8448h

Access Method

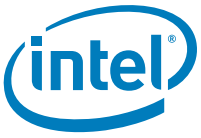
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8448h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**IDMA_OWNS_CNTX:** Indicates that IDMA module owns the context access currently **Power Well:** Core
30	0x0 RO	**ODMA_OWNS_CNTX:** Indicates that ODMA module owns the context access currently **Power Well:** Core
29	0x0 RO	**TRM_OWNS_CNTX:** Indicates that TRM modules owns the context access currently **Power Well:** Core
28	0x0 RO	**CMD_RING_REQUESTED_CNTX_LOCK:** Indicates that Command Manager has requested a context lock **Power Well:** Core
27	0x0 RO	**CMD_RING_STOP_IN_PROGRESS:** Indicates that Command Ring stop command is in progress **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
26	0x0 RO	**SCH_UPDATE_CLR_EP_IN_PROGRESS:** Indicates that clearing an EP out of schedule is in progress **Power Well:** Core
25	0x0 RO	**ADDR_DEV_DONE:** Indicates that current address device command is done by ODMA **Power Well:** Core
24	0x0 RO	**ADDR_DEV_IN_PROGRESS:** Indicates that ODMA has an address device command in progress **Power Well:** Core
23	0x0 RO	**EP_STATE_UPDATE_IN_PROGRESS:** Indicates that updating of EP state is in progress **Power Well:** Core
22	0x0 RO	**EP_STATE_IN_PROGRESS_FROM_STOP_DUE_TO_DB:** Indicates that doorbell manager is issuing and EP update due to a doorbell ring on an EP that is in stop state **Power Well:** Core
21	0x0 RO	**EP_STATE_UPDATE_IN_PROGRESS_DUE_TO_EP_ERROR:** Indicates that transfer ring manager is issuing and EP update due to an EP error condition detected **Power Well:** Core
20	0x0 RO	**EP_STATE_UPDATE_IN_PROGRESS_DUE_TO_STALL:** Indicates that transfer ring manager is issuing an EP state update due to stall received **Power Well:** Core
19	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
18	0x0 RO	**STOP in progress (STOP_IN_PROGRESS):** Indicates that a STOP on the Command Ring is in progress **Power Well:** Core
17	0x0 RO	**commend ring has doorbell pending (CMD_RING_DB_PENDING):** Indicates that the commend ring has doorbell pending **Power Well:** Core
16	0x0 RO	**commend ring running (CMD_RING_RUNNING):** Indicates that the commend ring is running **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Command next capability offset (CMD_NEXT_CAP_OFFSET):** Reserved. **Power Well:** Core
7:0	0x0 RO	**Vendor defined capability ID (VID):** Reserved. **Power Well:** Core

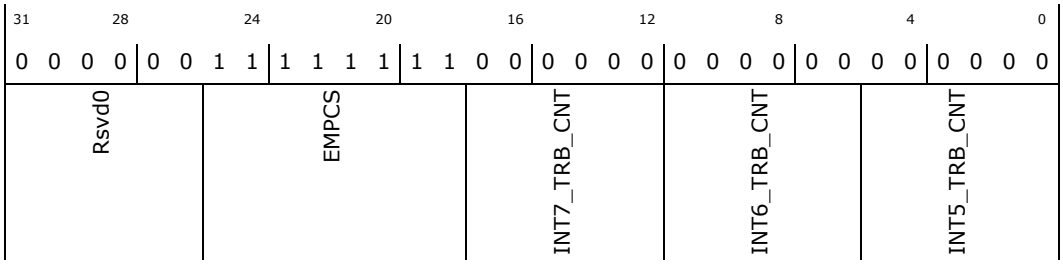
7.3.4 XECP_CMDM_STS1—Offset 844Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 844Ch

Default: 03FC0000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
25:18	0xff RO	**Event manager Producer Cycle State (EMPCS):** Reserved. **Power Well:** Core
17:12	0x0 RO	**Interrupter 7 TRB Count [5:0] (INT7_TRB_CNT):** Reserved. **Power Well:** Core
11:6	0x0 RO	**Interrupter 6 TRB Count [5:0] (INT6_TRB_CNT):** Reserved. **Power Well:** Core
5:0	0x0 RO	**Interrupter 5 TRB Count [5:0] (INT5_TRB_CNT):** Reserved. **Power Well:** Core

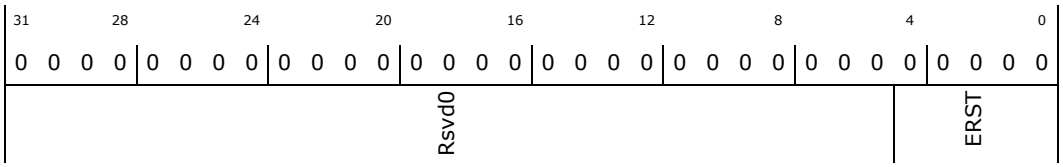
7.3.5 XECP_CMDM_STS2—Offset 8450h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8450h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
4:0	0x0 RO	**Event Ring Segment Table (ERST):** count low **Power Well:** Core

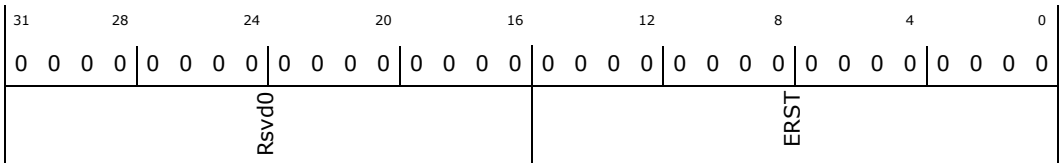
7.3.6 XECP_CMDM_STS3—Offset 8454h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8454h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
15:0	0x0 RO	**Event Ring Segment Table (ERST):** count high **Power Well:** Core

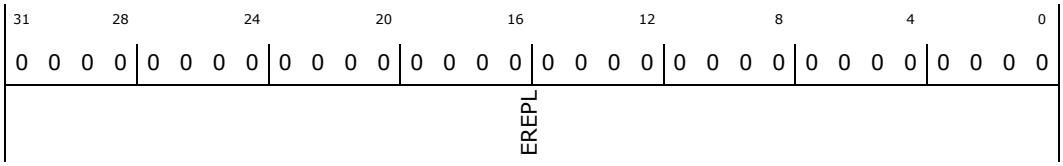
7.3.7 XECP_CMDM_STS4—Offset 8458h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8458h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Event Ring Enqueue Pointer Low (EREPL):** Reserved. **Power Well:** Core

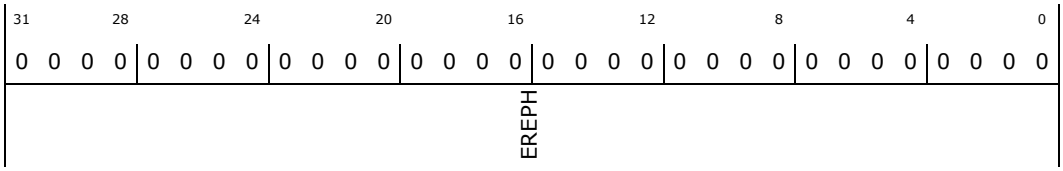
7.3.8 XECP_CMDM_STS5—Offset 845Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 845Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Event Ring Enqueue Pointer High (EREPH):** Reserved. **Power Well:** Core

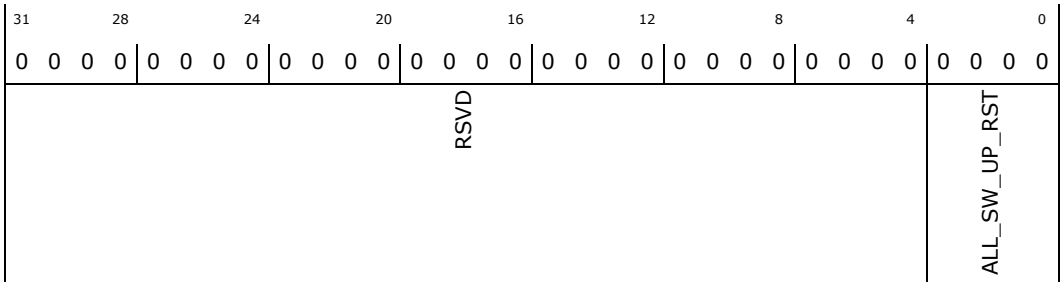
7.3.9 AUX Power PHY Reset (UPORTS_PON_RST_REG)—Offset 8460h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8460h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
3:0	0x0 WO	**Allow Software USB PHY RST (ALL_SW_UP_RST):** Allow a USB PHY reset being issued by software. Writing to this register with bit set to 1 will reset the USB PHY that is connected to the port. Bit3:0 indicates the port number of the USB PHY **Power Well:** SUS

7.3.10 Latency Tolerance Control 0 (HOST_IF_LAT_TOL_CTRL_REG0)—Offset 8464h

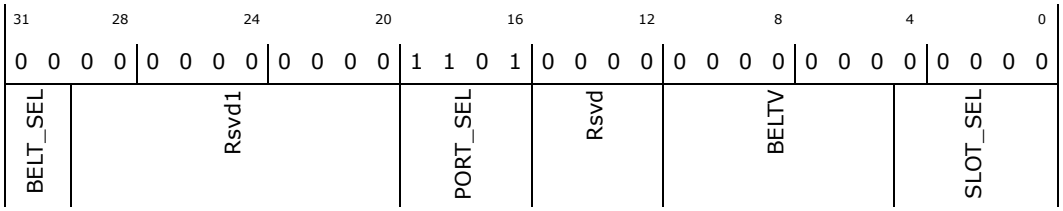
The Latency Tolerance Control Register is used by SW to control which BELT is returned when this register is read. SW shall write to this register to program a Slot-ID, Port-ID and BELT Select to determine which BELT is selected. When this register is read the selected BELT is returned.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8464h

Default: 000D0000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 WO	**BELT Select (BELT_SEL):** This field determines what value will be selected to read back from SW when reading this register 0: Returns the SW programmed Latency Tolerance Value 1: Returns the Lowest BELT in the Host 2: Returns the BELT for the requested Slot-ID (Slot Select) 3: Returns the BELT for the requested Port-ID (Port Select) **Power Well:** Core
29:20	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
19:16	0xd WO	**Port Select (PORT_SEL):** Used to select the BELT for a given Port # when the BELT Select is programmed to select the Port-ID (this field is 0 based) **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:12	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core
11:5	0x0 RO	**BELT Value (BELTV):** Value of selected BELT is return in this field **Power Well:** Core
4:0	0x0 RW	**Slot Select (SLOT_SEL):** Reads will return: BELT Value (BELTV) [4:0]: Value of selected BELT is return in this field Writes will control : Slot Select (): Used to select the BELT for a given Slot # when the BELT Select is programmed to select the Slot-ID (this field is zero based) **Power Well:** Core

7.3.11 USB Legacy Support Capability (USBLEGSUP)—Offset 846Ch

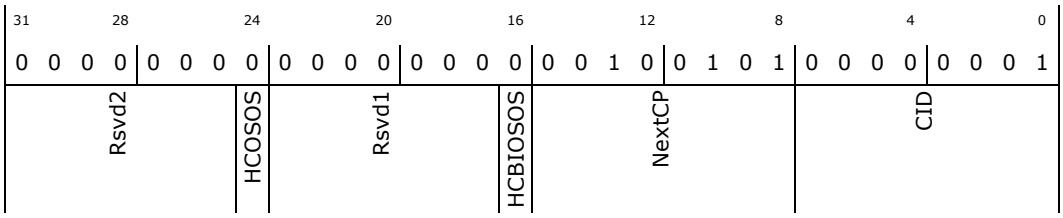
This register is modified and maintained by BIOS

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 846Ch

Default: 00002501h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
24	0x0 RW	**HC OS Owned Semaphore (HCOSOS):** Reserved. **Power Well:** SUS
23:17	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0x0 RW	**HC BIOS Owned Semaphore (HCBIOSOS):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x25 RW/S	**Next Capability Pointer (NextCP):** Reserved. **Power Well:** SUS
7:0	0x1 RW/L	**Capability ID (CID):** Reserved. **Power Well:** SUS

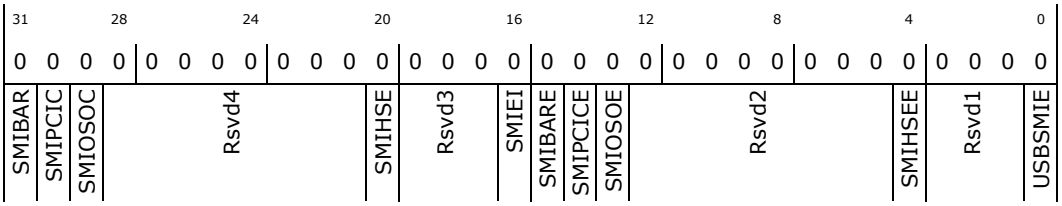
7.3.12 USB Legacy Support Control Status (USBLEGCTLSTS)—Offset 8470h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8470h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/C	**SMI on BAR (SMIBAR):** Reserved. **Power Well:** SUS
30	0x0 RW/C	**SMI on PCI Command (SMIPCIC):** Reserved. **Power Well:** SUS
29	0x0 RW/C	**SMI on OS Ownership Change (SMIOSOC):** Reserved. **Power Well:** SUS
28:21	0x0 RO	**Rsvd4:** Reserved. **Power Well:** Core
20	0x0 RO	**SMI on Host System Error (SMIHSE):** Reserved. **Power Well:** SUS
19:17	0x0 RO	**Rsvd3:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RO	**SMI on Event Interrupt (SMIEI):** Reserved. **Power Well:** SUS
15	0x0 RW	**SMI on BAR Enable (SMIBARE):** Reserved. **Power Well:** SUS
14	0x0 RW	**SMI on PCI Command Enable (SMIPCICE):** Reserved. **Power Well:** SUS
13	0x0 RW	**SMI on OS Ownership Enable (SMIOSOE):** Reserved. **Power Well:** SUS
12:5	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
4	0x0 RW	**SMI on Host System Error Enable (SMIHSEE):** Reserved. **Power Well:** SUS
3:1	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
0	0x0 RW	**USB SMI Enable (USBSMIE):** Reserved. **Power Well:** SUS

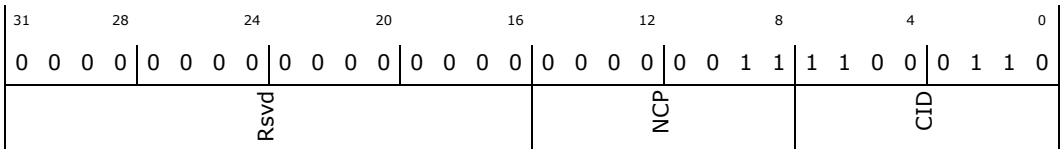
7.3.13 Port Disable Override capability register (PDO_CAPABILITY)—Offset 84F4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 84F4h

Default: 000003C6h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x3 RW/S	**Next Capability Pointer (NCP):** Reserved. **Power Well:** Core
7:0	0xc6 RW/S	**Capability ID (CID):** Reserved. **Power Well:** Core

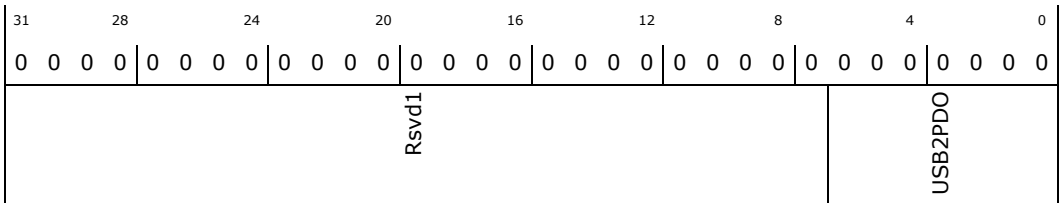
7.3.14 USB2 Port Disable Override (USB2PDO)—Offset 84F8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 84F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
6:0	0x0 RW/O	**USB2PDO:** Reserved. **Power Well:** SUS

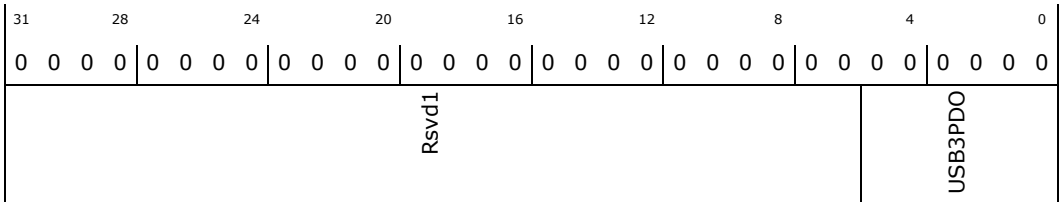
7.3.15 USB3 Port Disable Override (USB3PDO)—Offset 84FCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 84FCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
5:0	0x0 RW/O	**USB3 Port Disable Override (USB3PDO):** A '1' in a bit position prevents the corresponding USB3 port from reporting a Device Connection to the XHC. **Power Well:** SUS

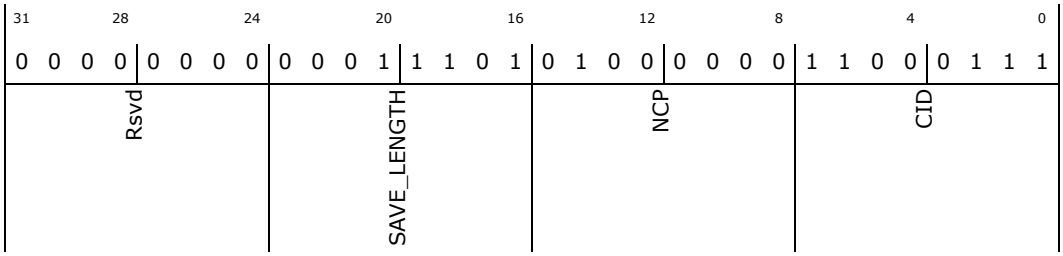
7.3.16 HW state capability register (HW_STATE_CAPABILITY)—Offset 8500h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8500h

Default: 001D40C7h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core
23:16	0x1d RO	**Save Length (SAVE_LENGTH):** Indicates the number of DWords in this capability starting at offset 04h, that need to be saved and restored **Power Well:** Core
15:8	0x40 RO	**Next Capability Pointer (NCP):** Reserved. **Power Well:** Core
7:0	0xc7 RO	**Capability ID (CID):** Reserved. **Power Well:** Core

7.3.17 HW state register 1 (HW_STATE_REG1)—Offset 8504h

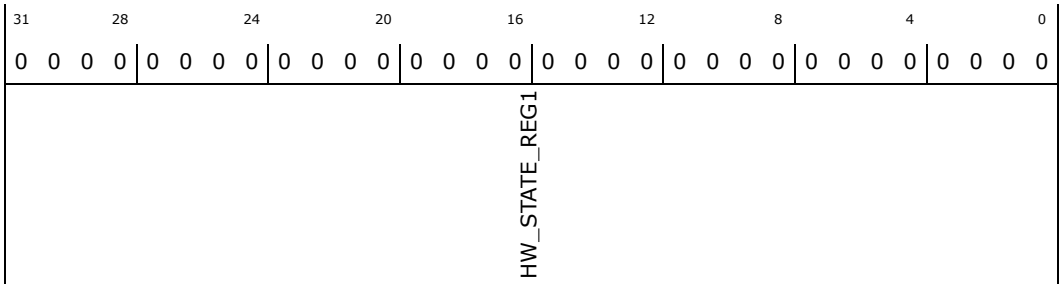
Implementation defined HW state: SW must not access this register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8504h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**HW_STATE_REG1:** Reserved. **Power Well:** Core

7.3.18 HW state register 2 (HW_STATE_REG2)—Offset 8508h

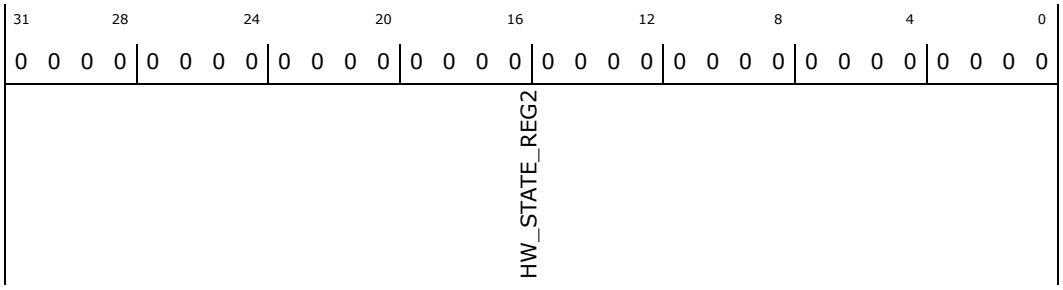
Implementation defined HW state: SW must not access this register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8508h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**HW_STATE_REG2:** Reserved. **Power Well:** Core

7.3.19 HW state register 3 (HW_STATE_REG3)—Offset 850Ch

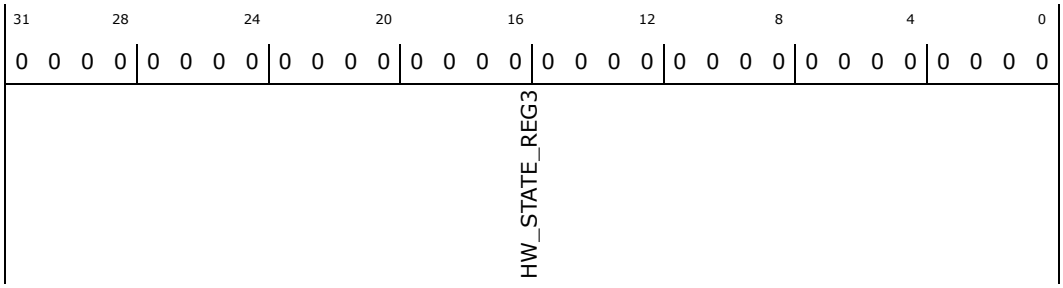
Implementation defined HW state: SW must not access this register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 850Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**HW_STATE_REG3:** Reserved. **Power Well:** Core

7.3.20 HW state register 4 (HW_STATE_REG4)—Offset 8510h

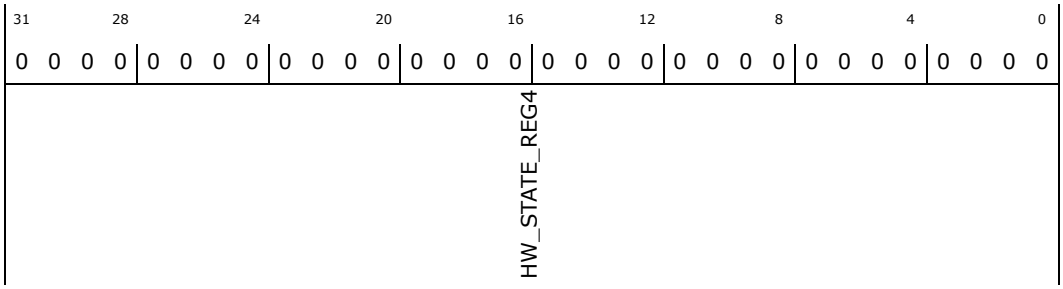
Implementation defined HW state: SW must not access this register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8510h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**HW_STATE_REG4:** Reserved. **Power Well:** Core

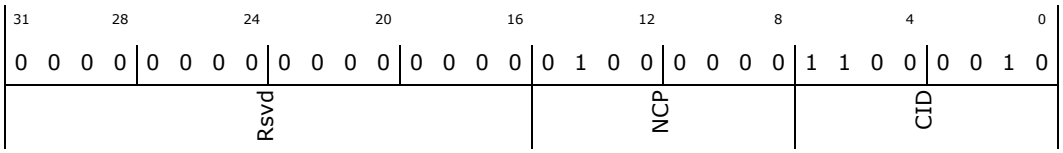
7.3.21 CONFIG mirror capability register (CONFIG_MIRROR_CAPABILITY)—Offset 8600h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8600h

Default: 000040C2h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core
15:8	0x40 RW/S	**Next Capability Pointer (NCP):** Reserved. **Power Well:** Core
7:0	0xc2 RW/S	**Capability ID (CID):** Reserved. **Power Well:** Core

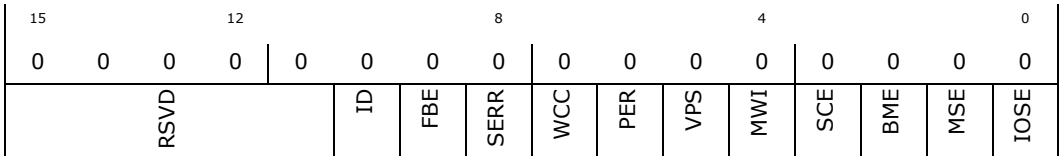
7.3.22 Command (CMD_MMIO)—Offset 8604h

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [MBAR] + 8604h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:11	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RW	**Interrupt Disable (ID):** When cleared to 0, the function is capable of generating interrupts. When 1, the function can not generate its interrupt to the interrupt controller. Note that the corresponding Interrupt Status bit is not affected by the interrupt enable. **Power Well:** Core
9	0x0 RO	**Fast Back to Back Enable (FBE):** Reserved. **Power Well:** Core
8	0x0 RW	**SERR# Enable (SERR):** When set to 1, the XHC is capable of generating (internally) SERR#. Refer section on error handling. **Power Well:** Core
7	0x0 RO	**Wait Cycle Control (WCC):** Reserved. **Power Well:** Core
6	0x0 RW	**Parity Error Response (PER):** When set to 1, the XHCI Host Controller will check for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase as recommended by the XHCI specification. Note that this applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#. **Power Well:** Core
4	0x0 RO	**Memory Write Invalidate (MWI):** Reserved. **Power Well:** Core
3	0x0 RO	**Special Cycle Enable (SCE):** Reserved. **Power Well:** Core
2	0x0 RW	**Bus Master Enable (BME):** When set, it allows XHC to act as a bus master. When cleared, it disable XHC from initiating transactions on the system bus. **Power Well:** Core
1	0x0 RW	**Memory Space Enable (MSE):** This bit controls access to the XHC Memory Space registers. If this bit is set, accesses to the XHC registers are enabled. The Base Address register for the XHC should be programmed before this bit is set. **Power Well:** Core
0	0x0 RO	**I/O Space Enable (IOSE):** Reserved as 0. Read-Only. **Power Well:** Core

7.3.23 Device Status (STS_MMIO)—Offset 8606h

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [MBAR] + 8606h

Default: 0290h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0
DPE	SSE	RMA	RTA	STA	DEVT		MDPED	FBBC	UDF	MC	CL	IS	RSVD		

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW/1C	**Detected Parity Error (DPE):** This bit is set by the Intel PCH whenever a parity error is seen on the internal interface to the XHC host controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
14	0x0 RW/1C	**Signaled System Error (SSE):** This bit is set by the Intel PCH whenever it signals SERR# (internally). The SERR_EN bit (bit 8 in the Command Register) must be 1 for this bit to be set. Refer error handling section for complete list of conditions handled. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
13	0x0 RW/1C	**Received Master-Abort Status (RMA):** This bit is set when XHC, as a master, receives a master-abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
12	0x0 RW/1C	**Received Target Abort Status (RTA):** This bit is set when XHC, as a master, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
11	0x0 RW/1C	**Signaled Target-Abort Status (STA):** This bit is used to indicate when the XHC function responds to a cycle with a target abort. **Power Well:** Core
10:9	0x1 RO	**DEVSEL# Timing Status (DEVT):** This 2-bit field defines the timing for DEVSEL# assertion. Read-Only. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW/1C	**Master Data Parity Error Detected (MDPED):** This bit is set by the Intel PCH whenever a data parity error is detected on a XHC read completion packet on the internal interface to the XHC host controller and bit 6 of the Command register is set to 1. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
7	0x1 RO	**Fast Back-to-Back Capable (FBBC):** Reserved as 1 Read-Only. **Power Well:** Core
6	0x0 RO	**User Definable Features (UDF):** Reserved as 0. Read-Only. **Power Well:** Core
5	0x0 RO	**66 MHz Capable (MC):** Reserved as 0. Read-Only. **Power Well:** Core
4	0x1 RO	**Capabilities List (CL):** Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer. **Power Well:** Core
3	0x0 RO/V	**Interrupt Status (IS):** This read-only bit reflects the state of this function's interrupt at the input of the enable/disable logic. This bit is a 1 when the interrupt is asserted. This bit will be 0 when the interrupt is deasserted. The value reported in this bit is independent of the value in the Interrupt Enable bit. **Power Well:** Core
2:0	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

7.3.24 Revision ID (RID_MMIO)—Offset 8608h

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [MBAR] + 8608h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RID							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO/V	**Revision ID (RID):** Refer Chap 6 for value. **Power Well:** Core

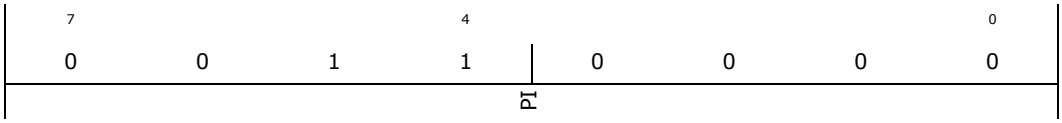
7.3.25 Programming Interface (PI_MMIO)—Offset 8609h

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [MBAR] + 8609h

Default: 30h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x30 RO	**Programming Interface (PI):** A value of 30h indicates that this USB Host Controller conforms to the XHCI specification. **Power Well:** Core

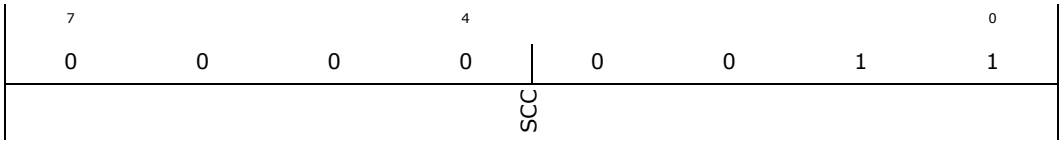
7.3.26 Sub Class Code (SCC_MMIO)—Offset 860Ah

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [MBAR] + 860Ah

Default: 03h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x3 RO	**Sub Class Code (SCC):** A value of 03h indicates that this is a Universal Serial Bus Host Controller. **Power Well:** Core

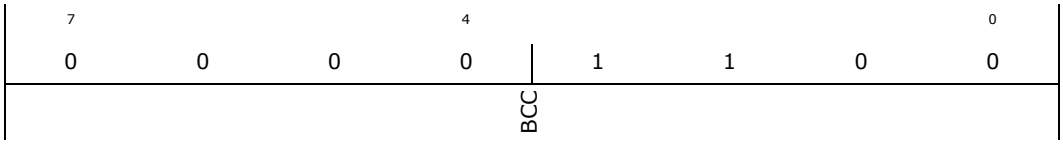
7.3.27 Base Class Code (BCC_MMIO)—Offset 860Bh

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [MBAR] + 860Bh

Default: 0Ch



Bit Range	Default & Access	Field Name (ID): Description
7:0	0xc RO	**Base Class Code (BCC):** A value of 0Ch indicates that this is a Serial Bus controller. **Power Well:** Core

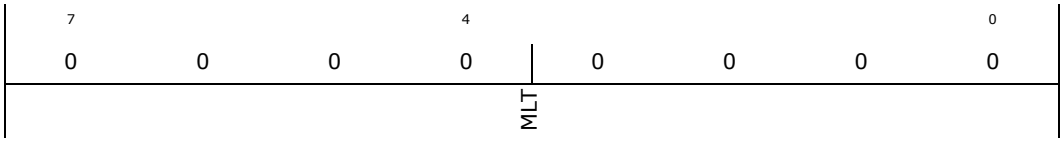
7.3.28 Master Latency Timer (MLT_MMIO)—Offset 860Dh

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [MBAR] + 860Dh

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**Master Latency Timer (MLT):** Because the XHC controller is internally implemented with arbitration on an internal interface, it does not need a master latency timer. The bits will be fixed at 0. **Power Well:** Core

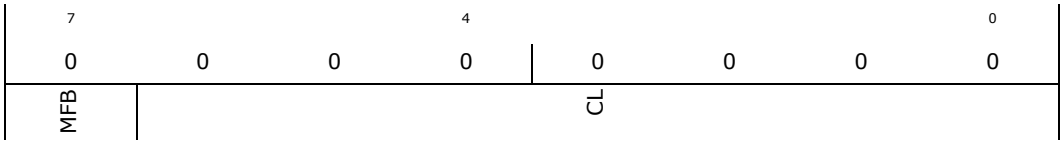
7.3.29 Header Type (HT_MMIO)—Offset 860Eh

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [MBAR] + 860Eh

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**Multi-Function Bit (MFB):** Read only indicating single function device. **Power Well:** Core
6:0	0x0 RO	**Configuration layout (CL):** Hardwired to 0 to indicate a standard PCI configuration layout. **Power Well:** Core

7.3.30 Memory Base Address (MBAR_MMIO)—Offset 8610h

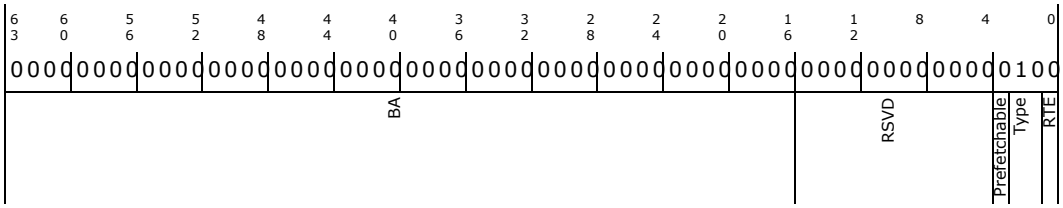
Value in this register will be different after the enumeration process.

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [MBAR] + 8610h

Default: 0000000000000004h



Bit Range	Default & Access	Field Name (ID): Description
63:16	0x0 RW	**Base Address (BA):** Bits (63:16) correspond to memory address signals (63:16), respectively. This gives 64 KB of relocatable memory space aligned to 64 KB boundaries. **Power Well:** Core
15:4	0x0 RO	**Reserved (RSVD):** Reserved. Read-Only 0, this indicates that this function is requesting an 64KB block of memory. **Power Well:** Core
3	0x0 RO	**Prefetchable:** This bit is hardwired to 0 indicating that this range should not be prefetched. **Power Well:** Core
2:1	0x2 RO	**Type:** If this field is hardwired to 00 it indicates that this range can be mapped anywhere within 32-bit address space. If this field is hardwired to 10 it indicates that this range can be mapped anywhere within 64-bit address space. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RO	**Resource Type Indicator (RTE):** This bit is hardwired to 0 indicating that the base address field in this register maps to memory space **Power Well:** Core

7.3.31 USB Subsystem Vendor ID (SSVID_MMIO)—Offset 862Ch

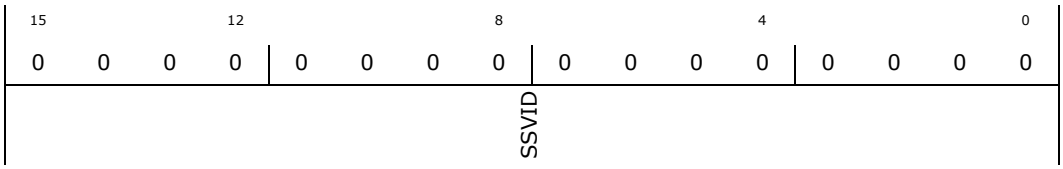
This register is modified and maintained by BIOS

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [MBAR] + 862Ch

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW/L	**USB Subsystem Vendor ID (SSVID):** This register, in combination with the USB Subsystem ID register, enables the operating system to distinguish each subsystem from the others. **Power Well:** Core

7.3.32 USB Subsystem ID (SSID_MMIO)—Offset 862Eh

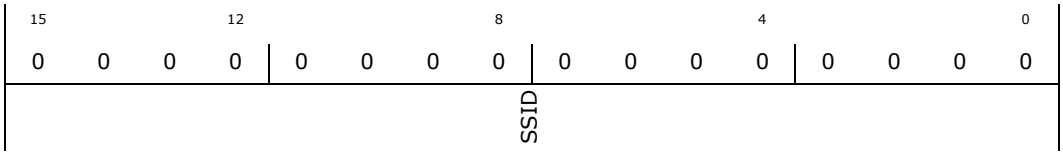
This register is modified and maintained by BIOS

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [MBAR] + 862Eh

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW/L	**USB Subsystem ID (SSID):** BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s). **Power Well:** Core

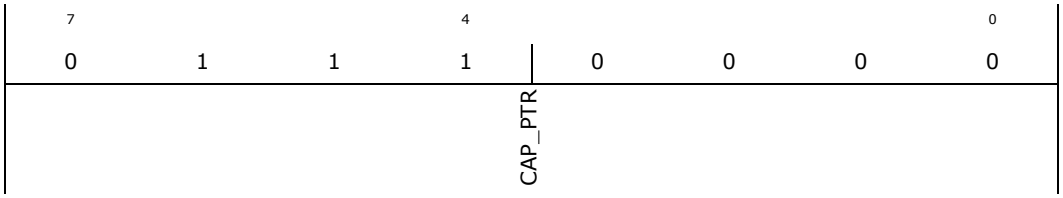
7.3.33 Capabilities Pointer (CAP_PTR_MMIO)—Offset 8634h

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [MBAR] + 8634h

Default: 70h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x70 RO	**Capabilities Pointer (CAP_PTR):** This register points to the starting offset of the capabilities ranges. **Power Well:** Core

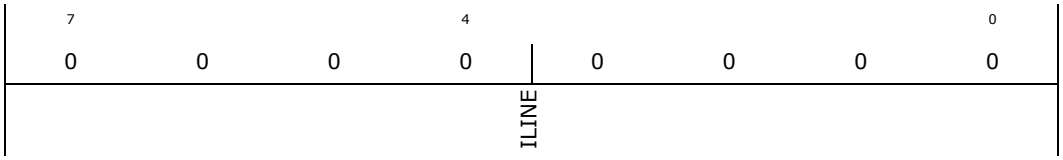
7.3.34 Interrupt Line (ILINE_MMIO)—Offset 863Ch

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [MBAR] + 863Ch

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**Interrupt Line (ILINE):** This data is not used by the Intel PCH. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to. **Power Well:** Core

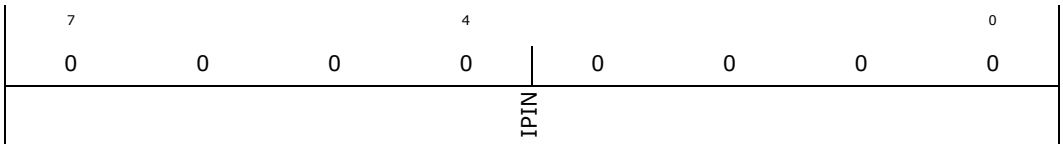
7.3.35 Interrupt Pin (IPIN_MMIO)—Offset 863Dh

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [MBAR] + 863Dh

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**Interrupt pin (IPIN):** Bits 7:0 reflect the Interrupt Pin assigned to the host controller by the platform (and are hardwired). **Power Well:** Core

7.3.36 Audio Time Synchronization (AUDSYNC_MMIO)—Offset 8658h

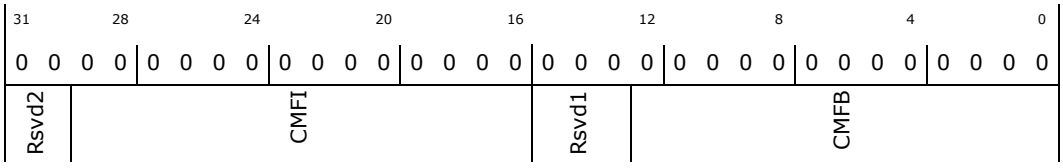
This 32 bit register is used for audio stream synchronization across different devices. Global signal sample_now captures a value in AUDSYNC register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8658h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
29:16	0x0 RO/V	**Captured Frame List Current Index/Frame Number (CMFI):** The value in this register is updated in response to sample_now signal. Bits (29:16) reflect state of bits (13:0) of FRINDEX **Power Well:** Core
15:13	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
12:0	0x0 RO/V	**Captured Micro-frame BLIF (CMFB):** The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done in FLA. **Power Well:** Core

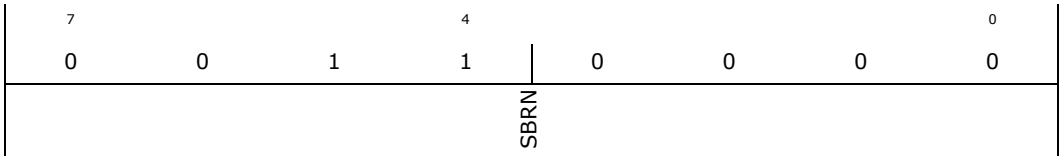
7.3.37 Serial Bus Release Number (SBRN_MMIO)—Offset 8660h

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [MBAR] + 8660h

Default: 30h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x30 RO	**Serial Bus Release Number (SBRN):** A value of 30h indicates that this controller follows USB release 3.0. **Power Well:** SUS

7.3.38 Frame Length Adjustment (FLADJ_MMIO)—Offset 8661h

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register

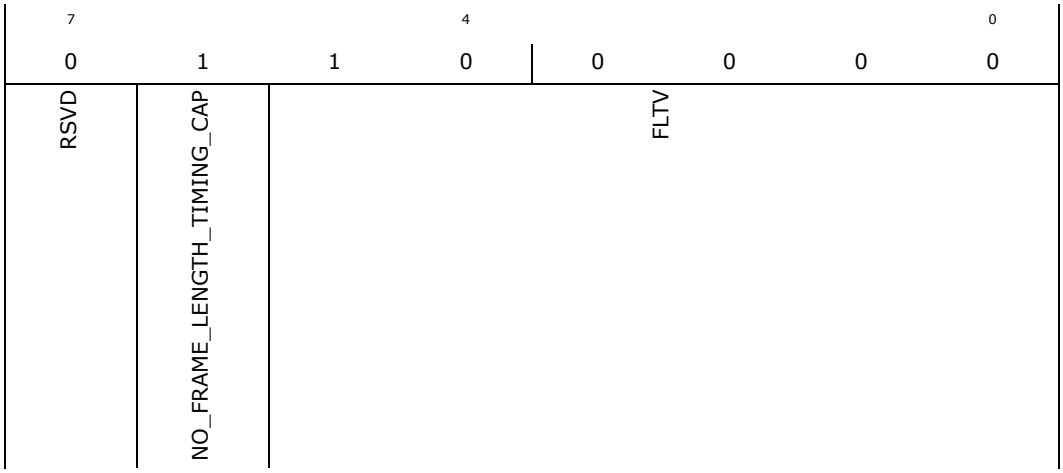
should only be modified when the HChalted bit in the USBSTS register is a one. Changing value of this register while the host controller is operating yields undefined results.

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [MBAR] + 8661h

Default: 60h



Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**Reserved (RSVD):** . **Power Well:** SUS
6	0x1 RO	**No Frame Length Timing Capability (NO_FRAME_LENGTH_TIMING_CAP):** This flag is set to 1 to indicate that the host controller does not support a programmable Frame Length Timing Value field. **Power Well:** Core
5:0	0x20 RO	**Frame Length Timing Value (FLTV):** SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (number of High Speed bit times) FLADJ Value (decimal) (decimal) 59488 0 (00h) 59504 1 (01h) 59520 2 (02h) ... 59984 31 (1Fh) 60000 32 (20h) ... 60480 62 (3Eh) 60496 63 (3Fh) Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (# High Speed bit times) FLADJ Value **Power Well:** SUS

7.3.39 Best Effort Service Latency (BESL_MMIO)—Offset 8662h

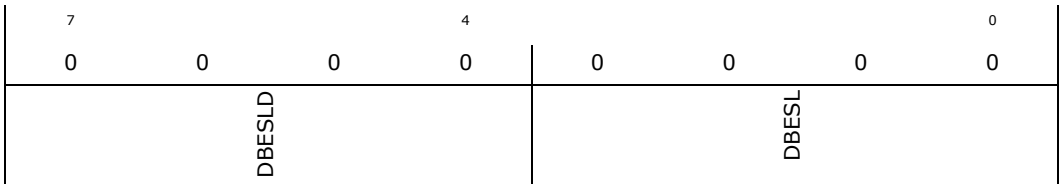
Bset Effort Service Latency.

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [MBAR] + 8662h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW/L	**Default Best Effort Service Latency Deep (DBESLD):** Default Best Effort Service Latency (DBESLD) If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESLD field. This is programmed by BIOS based on platform parameters. **Power Well:** Core
3:0	0x0 RW/L	**Default Best Effort Service Latency (DBESL):** If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESL field. This is programmed by BIOS based on platform parameters. **Power Well:** Core

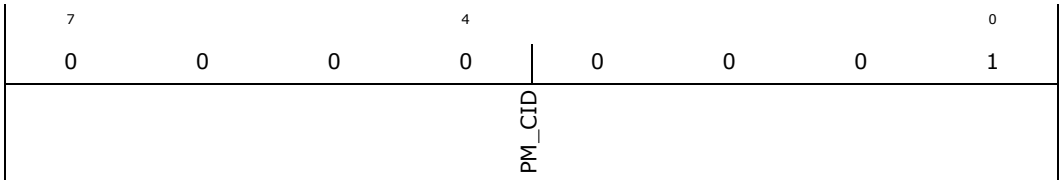
7.3.40 PCI Power Management Capability ID (PM_CID_MMIO)—Offset 8670h

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [MBAR] + 8670h

Default: 01h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x1 RO	**PCI Power Management Capability ID (PM_CID):** A value of 01h indicates that this is a PCI Power Management capabilities field. **Power Well:** Core

7.3.41 Next Item Pointer #1 (PM_NEXT_MMIO)—Offset 8671h

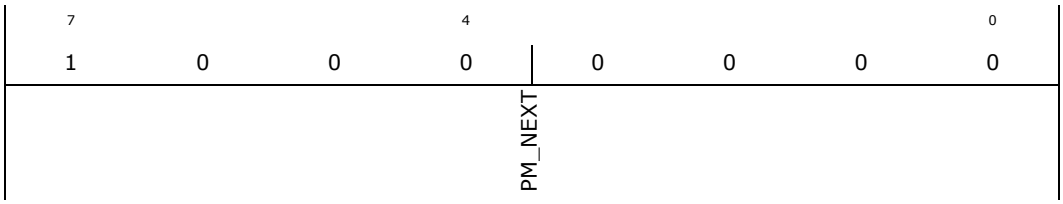
This register is modified and maintained by BIOS

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [MBAR] + 8671h

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x80 RW/L	**Next Item Pointer #1 (PM_NEXT):** This register defaults to 80h, which indicates that the next capability registers begin at configuration offset 80h. This register is writable when the Access Control bit is set to '0'. This allows BIOS to effectively hide the next capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Values of: 80h implies next capability is MSI 00h implies that MSI capability is hidden. Note: This value is never expected to be programmed. **Power Well:** Core

7.3.42 Power Management Capabilities (PM_CAP_MMIO)—Offset 8672h

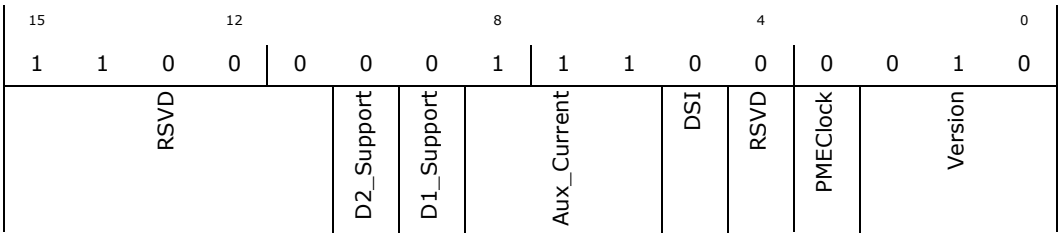
Normally, this register is read-only to report capabilities to the power management software. In order to report different power management capabilities depending on the system in which the Intel PCH is used, the write access to this register is controlled by the Access Control bit (ACCTRL). The value written to this register does not affect the hardware other than changing the value returned during a read. This register is modified and maintained by BIOS

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [MBAR] + 8672h

Default: C1C2h



Bit Range	Default & Access	Field Name (ID): Description
15:11	0x18 RO	**Reserved (RSVD):** Reserved.
10	0x0 RW/L	**D2_Support:** The D2 state is not supported. **Power Well:** Core
9	0x0 RW/L	**D1_Support:** The D1 state is not supported. **Power Well:** Core
8:6	0x7 RW/L	**Aux_Current:** The Intel PCH XHC reports 375mA maximum Suspend well current required when in the D3cold state. This value can be written by BIOS when a more accurate value is known. **Power Well:** Core
5	0x0 RW/L	**DSI:** The Intel PCH reports 0, indicating that no device-specific initialization is required. **Power Well:** Core
4	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
3	0x0 RW/L	**PME Clock (PMEClock):** The Intel PCH reports 0, indicating that no PCI clock is required to generate PME#. **Power Well:** Core
2:0	0x2 RW/L	**Version:** The Intel PCH reports 010, indicating that it complies with Revision 1.1 of the PCI Power Management Specification. **Power Well:** Core

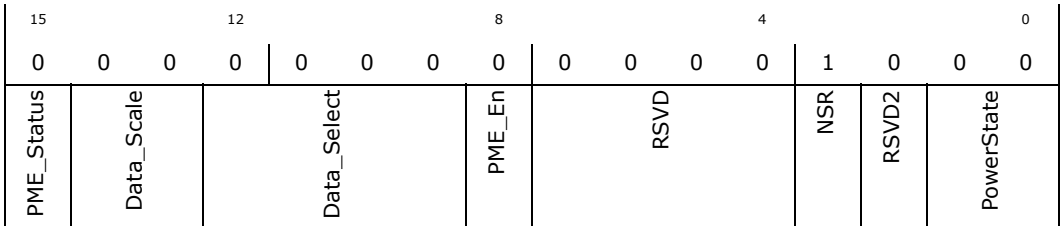
7.3.43 Power Management Control/Status (PM_CS_MMIO)—Offset 8674h

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [MBAR] + 8674h

Default: 0008h



Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW/1C	**PME_Status:** This bit is set when the Intel PCH XHC would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). Writing a 0 has no effect. This bit must be explicitly cleared by the operating system each time the operating system is loaded. **Power Well:** SUS
14:13	0x0 RO	**Data_Scale:** The Intel PCH hardwires these bits to 00 because it does not support the associated Data register. **Power Well:** Core
12:9	0x0 RO	**Data_Select:** The Intel PCH hardwires these bits to 0000 because it does not support the associated Data register. **Power Well:** Core
8	0x0 RW	**PME_En:** A 1 enables the Intel PCH XHC to generate an internal PME signal when PME_Status is 1. This bit must be explicitly cleared by the operating system each time it is initially loaded. **Power Well:** SUS
7:4	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
3	0x1 RO	**No Soft Reset (NSR):**), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. Transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. **Power Well:** Core
2	0x0 RO	**Reserved (RSVD2):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1:0	0x0 RW	**PowerState:** This 2-bit field is used both to determine the current power state of XHC function and to set a new power state. The definition of the field values are: 00b - D0 state 11b - D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3hot state, the Intel PCH must not accept accesses to the XHC memory range, but the configuration space must still be accessible. **Power Well:** Core

7.3.44 Message Signaled Interrupt CID (MSI_CID_MMIO)—Offset 8680h

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [MBAR] + 8680h

Default: 05h

7			4				0
0	0	0	0	0	1	0	1
CID							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x5 RO	**Capability ID (CID):** Indicates that this is an MSI capability **Power Well:** Core

7.3.45 Next item pointer (MSI_NEXT_MMIO)—Offset 8681h

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [MBAR] + 8681h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
NEXT							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**Next Pointer (NEXT):** Indicates that this is the last item on the capability list **Power Well:** Core

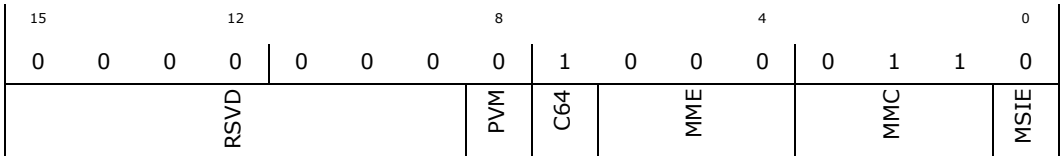
7.3.46 Message Signaled Interrupt Message Control (MSI_MCTL_MMIO)—Offset 8682h

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [MBAR] + 8682h

Default: 0086h



Bit Range	Default & Access	Field Name (ID): Description
15:9	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
8	0x0 RO	**Per-Vector Masking Capable (PVM):** Specifies whether controller supports MSI per vector masking. Not supported **Power Well:** Core
7	0x1 RO	**64 Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages. This device is 64-bit capable. **Power Well:** Core
6:4	0x0 RW	**Multiple Message Enable (MME):** Indicates the number of messages the controller should assert. This device supports multiple message MSI. **Power Well:** Core
3:1	0x3 RO	**Multiple Message Capable (MMC):** Indicates the number of messages the controller wishes to assert. This field must be set by HW to reflect the number of Interrupters supported. Encoding number of Vectors requested (number of Interrupters) 000 1 001 2 010 4 011 8 100 16 101 32 110-111 Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**MSI Enable (MSIE):** If set to 1, MSI is enabled and the traditional interrupt pins are not used to generate interrupts. If cleared to 0, MSI operation is disabled and the traditional interrupt pins are used. **Power Well:** Core

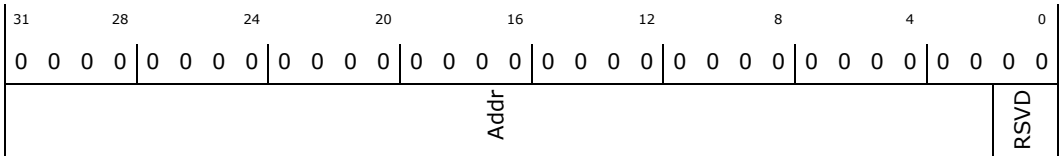
7.3.47 Message Signaled Interrupt Message Address (MSI_MAD_MMIO)—Offset 8684h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8684h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Addr:** Lower DW of system specified message address, always DWORD aligned **Power Well:** Core
1:0	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

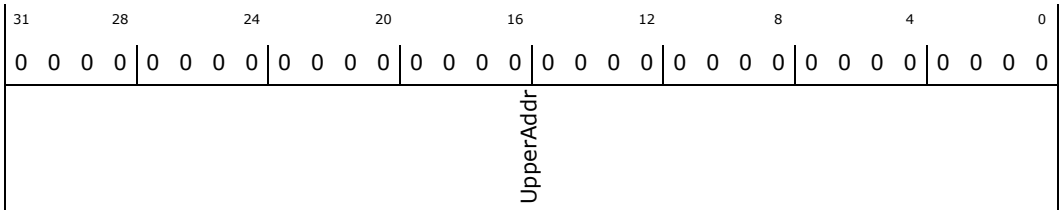
7.3.48 Message Signaled Interrupt Upper Address (MSI_MUAD_MMIO)—Offset 8688h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8688h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Upper Addr (UpperAddr):** Upper DW of system specified message address. **Power Well:** Core

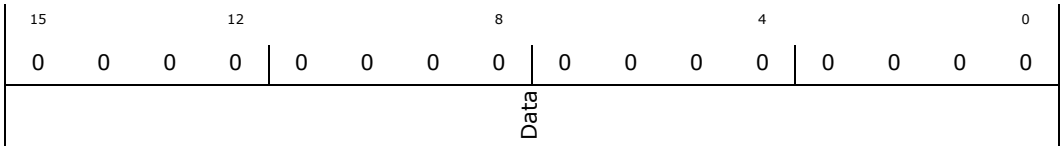
7.3.49 Message Signaled Interrupt Message Data (MSI_MD_MMIO)—Offset 868Ch

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [MBAR] + 868Ch

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW	**Data:** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD(15:0)) during the data phase of the MSI memory write transaction. The Multiple Message Enable field (bits 6-4 of the Message Control register) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010 indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000, the function is not permitted to modify the message data. **Power Well:** Core

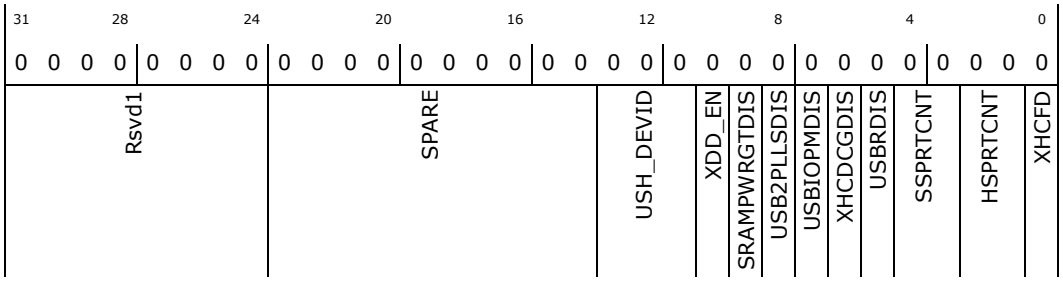
7.3.50 Fuse and Strap (FUS_MMIO)—Offset 8694h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8694h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
23:14	0x0 RO/V	**Spare Fuses (SPARE)** **Power Well:** SUS
13:11	0x0 RO/V	**USH DevID (USH_DEVID):** LSB bits of USH PCIe Device ID The 3 LSB bits enable defining up to 8 separate USH SKUs if required **Power Well:** SUS
10	0x0 RO/V	**Debug Device Enable (XDD_EN):** 0 : Debug Device is Enabled 1: Debug Device is Disabled **Power Well:** SUS
9	0x0 RO/V	**SRAM Power Gating Disable (SRAMPWRGTDIS):** 0: SRAM Power Gating Enabled 1: SRAM Power Gating Disabled **Power Well:** SUS
8	0x0 RO/V	**USB2 PLL Shutdown Disable (USB2PLLSDIS):** 0: USB2 PLL shutdown enabled 1: USB2 PLL shutdown disabled **Power Well:** SUS
7	0x0 RO/V	**USB I/O Power Management Disable (USBIOPMDIS):** 0: USB2 HW LPM and USB3 HW Ux under XHC enabled 1: USB2 HW LPM and USB3 HW Ux under XHC disabled **Power Well:** SUS
6	0x0 RO/V	**XHC Dynamic Clock Gating Disable (XHCDCGDIS):** 0: USB3 (XHC) dynamic clock gating enabled 1: USB3 (XHC) dynamic clock gating disabled **Power Well:** SUS
5	0x0 RO/V	**USBr Disable (USBRDIS):** 0: USBr enabled 1: USBr disabled **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
4:3	0x0 RO/V	**SS Port Count (SSPRTCNT):** This field specifies number of SS ports present. Supported combinations are: 00: 6 SS ports 01: 4 SS ports 10: 2 SS ports 11: 0 SS ports **Power Well:** SUS
2:1	0x0 RO/V	**HS Port Count (HSPRTCNT):** This field specifies number HS ports present. Supported combinations are: 00: 14 HS ports 01: 12 HS ports 10: 10 HS ports 11: N/A (reserved) **Power Well:** SUS
0	0x0 RO/V	**XHCI Function Disable (XHCFD):** When asserted, it indicates the XHCI is fused to function disabled. **Power Well:** SUS

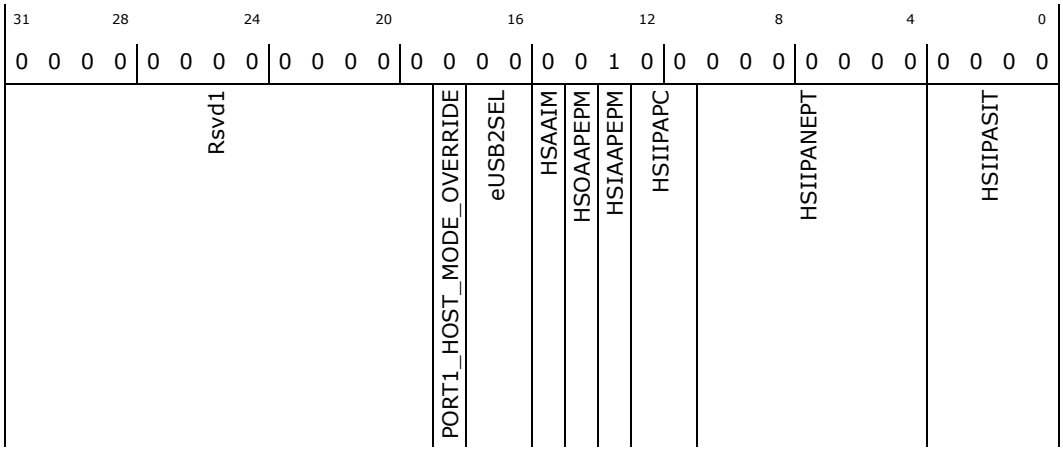
7.3.51 High Speed Configuration 2 (HSCFG2_MMIO)—Offset 86A4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 86A4h

Default: 00002000h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
18	0x0 RW	**PORT1_HOST_MODE_OVERRIDE:** When set, this bit causes the Host_Device mux on port 1 to be forced into the Host mode. **Power Well:** Core
17:16	0x0 RW	**eUSB2SEL:** The two bits are associate with USB2 ports 1 - bit 16 and 2 - bit 2 0: Port is mapped to USB2 1: Port is mapped to eUSB2 **Power Well:** Core
15	0x0 RW	**HS ASYNC Active IN Mask (HSAAIM):** Determines if the Async Active will mask/ignore IN EP s. 0 HS ASYNC Active will include IN EP s. 1 HS ASYNC Active will mask/ignore IN EP s. **Power Well:** Core
14	0x0 RW	**HS OUT ASYNC Active Polling EP Mask (HSOAAPEPM):** Determines if the Async Active for OUT HS/FS/LS masks/ignores EP s that are polling/ PINGing (HS) due to NAK. 0 HS OUT ASYNC Active will include EP s that are polling. 1 HS OUT ASYNC Active will mask/ignore EP s that are polling. **Power Well:** Core
13	0x1 RW	**HS IN ASYNC Active Polling EP Mask (HSIAAPEPM):** Determines if the Async Active for IN HS/FS/LS masks/ignores EP s that are polling due to NAK. 0 HS IN ASYNC Active will include EP s that are polling. 1 HS IN ASYNC Active will mask/ignore EP s that are polling. **Power Well:** Core
12:11	0x0 RW	**HS INTR IN Periodic Active Policy Control (HSIIPAPC):** Controls how the HS INTR IN periodic active is used to generate the global periodic active. This will determine how the smallest service interval among active EP s and number of active EP s are used. 0 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold OR Numb of EP Threshold values meet the requirement. 1 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold AND Numb of EP Threshold values meet the requirement. 2 Always allow HS INTR EP s to be used in the generation of the global Periodic Active indication. 3 Never allow HS INTR EP s to be used in the generation of the global Periodic Active indication **Power Well:** Core
10:4	0x0 RW	**HS INTR IN Periodic Active Num of EP Threshold (HSIIPANEPT):** Defines the threshold used to determine if Periodic Active may include HS/ FS/LS INTR IN EP active indication. If there are more than NumEPThreshold active HS/FS/LS INTR EP s then they may be included as part of the periodic active generation. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x0 RW	**HS INTR IN Periodic Active Service Interval Threshold (HSIIPASIT):** Defines the Service Interval threshold used to determine if Periodic Active will include HS/FS/LS INTR IN EP active indication. If there are any active HS/FS/LS INTR EP s with a service interval less than or equal to this threshold then they may be included as part of the periodic active generation. **Power Well:** Core

7.3.52 XHCI USB2 Overcurrent Pin Mapping 1 (U2OCM1_MMIO)—Offset 86B0h

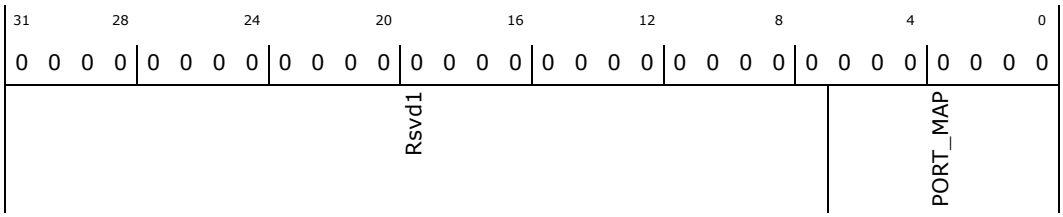
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 86B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**Rsvd (Rsvd1):** Reserved **Power Well:** Core
6:0	0x0 RW/L	**Port mapping (PORT_MAP):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std **Power Well:** Core

7.3.53 XHCI USB2 Overcurrent Pin Mapping 2 (U2OCM2_MMIO)—Offset 86B4h

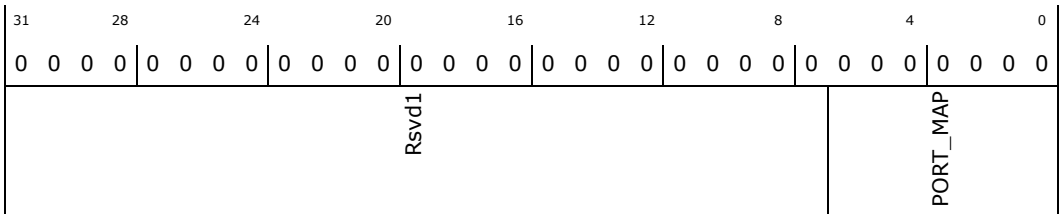
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 86B4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**Rsvd (Rsvd1):** Reserved **Power Well:** Core
6:0	0x0 RW/L	**Port mapping (PORT_MAP):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std **Power Well:** Core

7.3.54 XHCI USB3 Overcurrent Pin Mapping 1 (U3OCM1_MMIO)—Offset 86D0h

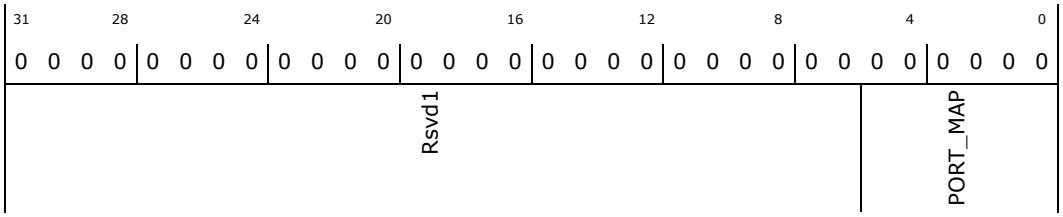
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 86D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**Rsvd (Rsvd1):** Reserved **Power Well:** Core
5:0	0x0 RW/L	**Port mapping (PORT_MAP):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std **Power Well:** Core

7.3.55 XHCI USB3 Overcurrent Pin Mapping 2 (U3OCM2_MMIO)—Offset 86D4h

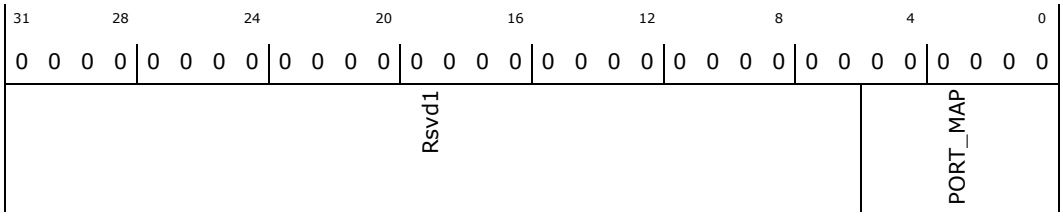
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 86D4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**Rsvd (Rsvd1):** Reserved **Power Well:** Core
5:0	0x0 RW/L	**Port mapping (PORT_MAP):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std **Power Well:** Core

7.3.56 Debug Capability ID Register (DCID)—Offset 8700h

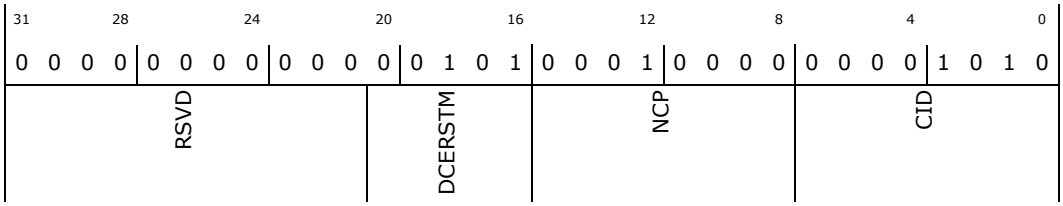
This register is modified and maintained by BIOS

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8700h

Default: 0005100Ah



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
20:16	0x5 RW	**Debug Capability Event Ring Segment Table Max (DCERSTM):** Note: This register is sticky. **Power Well:** Core
15:8	0x10 RW	**Next Capability Pointer (NCP):** Note: This register is sticky. **Power Well:** Core
7:0	0xa RW	**Capability ID (CID):** Note: This register is sticky. **Power Well:** Core

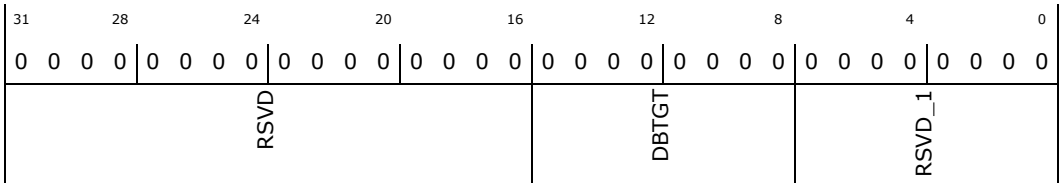
7.3.57 Debug Capability Doorbell Register (DCDB)—Offset 8704h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8704h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (RSVD):** Reserved. **Power Well:** Core
15:8	0x0 RW	**Doorbell Target (DBTGT):** This field defines the target of the doorbell reference. The table below defines the Debug Capability notification that is generated by ringing the doorbell. Value Definition 0 Data EP 1 OUT Enqueue Pointer Update 1 Data EP 1 IN Enqueue Pointer Update 2:255 Reserved This field returns '0' when read and the value should be treated as undefined by software. **Power Well:** Core
7:0	0x0 RW	**Reserved (RSVD_1):** Reserved. **Power Well:** Core

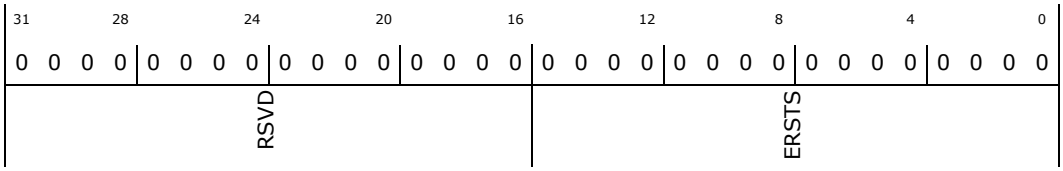
7.3.58 Debug Capability Event Ring Segment Table Size Register (DCERSTSZ)—Offset 8708h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8708h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (RSVD):** Reserved. **Power Well:** Core
15:0	0x0 RW	**Event Ring Segment Table Size (ERSTS):** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Debug Capability Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the DCERST Max field in the DCID register Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'. **Power Well:** Core

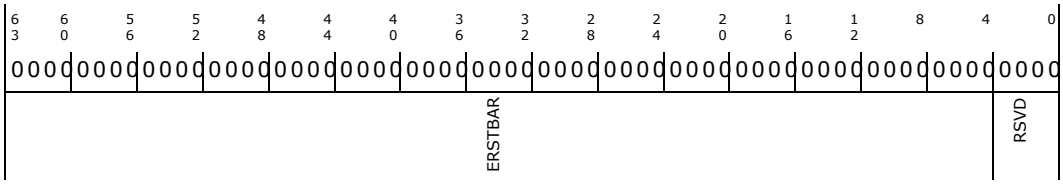
7.3.59 Debug Capability Event Ring Segment Table Base Address Register (DCERSTBA)—Offset 8710h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [MBAR] + 8710h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:4	0x0 RW	**Event Ring Segment Table Base Address Register (ERSTBAR):** This field defines the high order bits of the start address of the Debug Capability Event Ring Segment Table. Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'. **Power Well:** Core
3:0	0x0 RW	**Reserved (RSVD):** Reserved. **Power Well:** Core

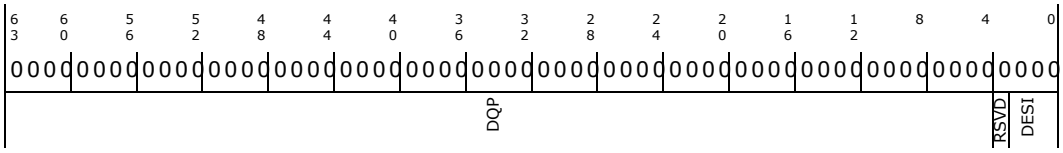
7.3.60 Debug Capability Event Ring Dequeue Pointer Register (DCERDP)—Offset 8718h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [MBAR] + 8718h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:4	0x0 RW	**Dequeue Pointer (DQP):** This field defines the high order bits of the 64-bit address of the current Debug Capability Event Ring Dequeue Pointer. Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'. **Power Well:** Core
3	0x0 RW	**Reserved (RSVD):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Dequeue ERST Segment Index (DESI):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. **Power Well:** Core

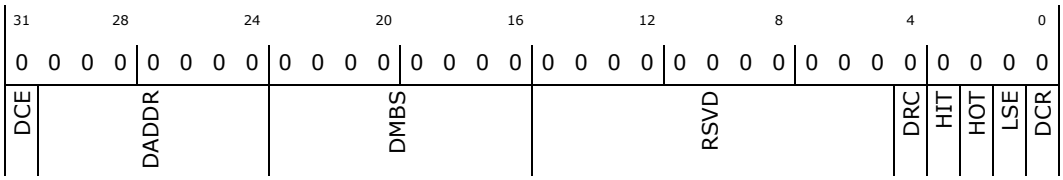
7.3.61 Debug Capability Control Register (DCCTRL)—Offset 8720h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8720h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Debug Capability Enable (DCE):** Reserved. **Power Well:** Core
30:24	0x0 RO	**Device Address (DADDR):** Reserved. **Power Well:** Core
23:16	0x0 RO	**Debug Max Burst Size (DMBS):** USB Debug Device does not support bursting. **Power Well:** Core
15:5	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
4	0x0 RW/C	**DbC Run Change (DRC):** Reserved. **Power Well:** Core
3	0x0 RW/1S	**Halt IN TR (HIT):** Reserved. **Power Well:** Core
2	0x0 RW/1S	**Halt OUT TR (HOT):** Reserved. **Power Well:** Core
1	0x0 RW	**Link Status Event Enable (LSE):** Reserved. **Power Well:** Core
0	0x0 RO	**DbC Run (DCR):** Reserved. **Power Well:** Core

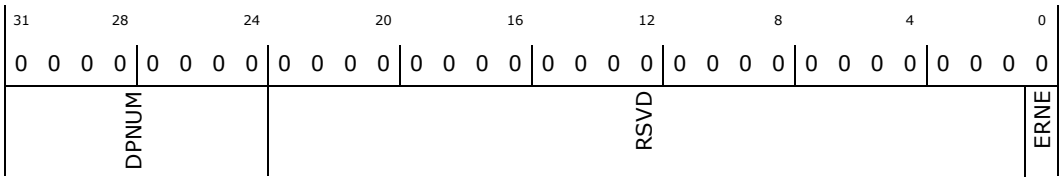
7.3.62 Debug Capability Status Register (DCST)—Offset 8724h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8724h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Debug Port Number (DPNUM):** This field provides the ID of the Root Hub port that the Debug Capability has been automatically attached to. The value is '0' when the Debug Capability is not attached to a Root Hub port. **Power Well:** Core
23:1	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
0	0x0 RO	**Event Ring Not Empty (ERNE):** When '1', this field indicates that the Debug Capability Event Ring has a Transfer Event on it. It is automatically cleared to '0' by the xHC when the Debug Capability Event Ring is empty, i.e. the Debug Capability Enqueue Pointer is equal to the Debug Capability Event Ring Dequeue Pointer register. **Power Well:** Core

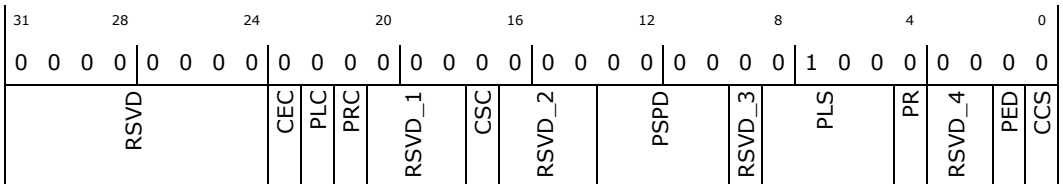
7.3.63 Debug Capability Port Status and Control Register (DCPORTSC)—Offset 8728h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8728h

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
23	0x0 RW/C	**Port Config Error Change (CEC):** This flag indicates that the port failed to configure its link partner. 0 = No change. 1 = Port Config Error detected. Software shall clear this bit by writing a '1' to it. **Power Well:** Core
22	0x0 RW/C	**Port Link Status Change (PLC):** This flag is set to '1' due to the following PLS transitions: U0 -) U3 Suspend signaling detected from Debug Host U3 -) U0 Resume complete Polling -) Disabled Training Error Ux or Recovery -) Inactive Error Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0' **Power Well:** Core
21	0x0 RW/C	**Port Reset Change (PRC):** This bit is set when reset processing on this port is complete (i.e. a '1' to '0' transition of PR). '0' = No change. '1' = Reset complete.Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'. **Power Well:** Core
20:18	0x0 RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core
17	0x0 RW/C	**Connect Status Change (CSC):** an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'. **Power Well:** Core
16:14	0x0 RO	**Reserved (RSVD_2):** Reserved. **Power Well:** Core
13:10	0x0 RO	**Port Speed (PSPD):** This field identifies the speed of the port. This field is only relevant when a Debug Host is attached (CCS = '1') in all other cases this field shall indicate Undefined Speed. 0 Undefined Speed 1-15 Protocol Speed ID (PSI) Note: The Debug Capability only does not supports LS, FS, or HS operation. **Power Well:** Core
9	0x0 RO	**Reserved (RSVD_3):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
8:5	0x4 RO	**Port Link State (PLS):** This field reflects its current link state. This field is only relevant when a Debug Host is attached (Debug Port Number) '0'). Value Meaning 0 Link is in the U0 State 1 Link is in the U1 State 2 Link is in the U2 State 3 Link is in the U3 State (Device Suspended) 4 Link is in the Disabled State 5 Link is in the RxDetect State 6 Link is in the Inactive State 7 Link is in the Polling State 8 Link is in the Recovery State 9 Link is in the Hot Reset State 15:10 Reserved Note: Transitions between different states are not reflected until the transition is complete. **Power Well:** Core
4	0x0 RO	**Port Reset (PR):** '1' = Port is in Reset. '0' = Port is not in Reset. This bit is set to '1' when the bus reset sequence as defined in the USB Specification is detected on the Root Hub port assigned to the Debug capability. It is cleared when the bus reset sequence is completed by the Debug Host, and the DbC shall transition to the USB Default state. A '0' to '1' transition of this bit shall clear DCPORTSC PED ('0'). This field is '0' if DCE or CCS are '0'. **Power Well:** Core
3:2	0x0 RO	**Reserved (RSVD_4):** Reserved. **Power Well:** Core
1	0x0 RW	**Port Enabled/Disabled (PED):** Default = '0'. '1' = Enabled. '0' = Disabled. This flag shall be set to '1' by a '0' to '1' transition of CCS or a '1' to '0' transition of the PR. When PED transitions from '1' to '0' due to the assertion of PR, the port's link shall transition to the Rx.Detect state. This flag may be used by software to enable or disable the operation of the Root Hub port assigned to the Debug Capability. The Debug Capability Root Hub port operation may be disabled by a fault condition (disconnect event or other fault condition, e.g. a LTSSM Polling sub state time out, tPortConfiguration timeout error, etc.), the assertion of DCPORTSC PR, or by software. 0 = Debug Capability Root Hub port is disabled. 1 = Debug Capability Root Hub port is enabled. When the port is disabled (PED = '0') the port's link shall enter the SS.Disabled state and remain there until PED is reasserted ('1') or DCE is negated ('0'). Note that the Root Hub port is remains mapped to Debug Capability while PED = '0'. While PED = '0' the Debug Capability will appear to be disconnected to the Debug Host. Note, this bit is not affected by PORTSC PR bit transitions. This field is '0' if DCE or CCS are '0'. **Power Well:** Core
0	0x0 RO	**Current Connect Status (CCS):** '1' = A Root Hub port is connected to a Debug Host and assigned to the Debug Capability. '0' = No Debug Host is present. This value reflects the current state of the port, and may not correspond to the value reported by the Connect Status Change (CSC) field in the Port Status Change Event that was generated by a '0' to '1' transition of this bit. This flag is '0' if Debug Capability Enable (DCE) is '0'. **Power Well:** Core

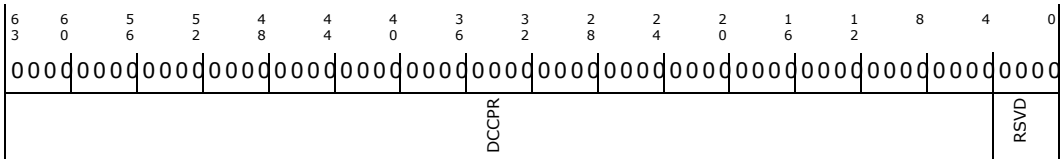
7.3.64 Debug Capability Context Pointer Register (DCCP)—Offset 8730h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [MBAR] + 8730h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:4	0x0 RW	**Debug Capability Context Pointer Register (DCCPR):** This field defines the high order bits of the start address of the Debug Capability Context data structure associated with the Debug Capability. Software shall initialize this register before setting the Debug Capability Enable bit in the Debug Capability Control Register to '1'. **Power Well:** Core
3:0	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

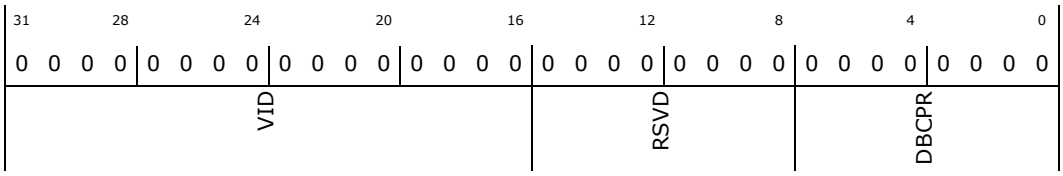
7.3.65 Debug Capability Device Descriptor Info Register 1 (DCDDI1)—Offset 8738h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8738h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Vendor ID (VID):** This field is presented by the Debug Device in the USB Device Descriptor idVendor field. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
7:0	0x0 RW	**DbC Protocol (DBCPR):** This field is presented by the Debug Device in the USB Interface Descriptor bInterfaceProtocol field. Value Function 0 Debug Target vendor defined. 1 GNU Remote Debug Command Set supported. 2-255 Reserved. **Power Well:** Core

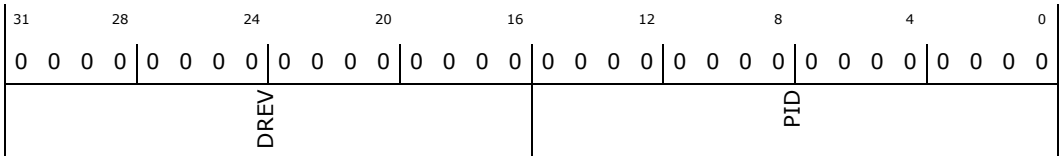
7.3.66 Debug Capability Device Descriptor Info Register 2 (DCDDI2)—Offset 873Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 873Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Device Revision (DREV):** This field is presented by the Debug Device in the USB Device Descriptor bcdDevice field. **Power Well:** Core
15:0	0x0 RW	**Product ID (PID):** This field is presented by the Debug Device in the USB Device Descriptor idProduct field. **Power Well:** Core

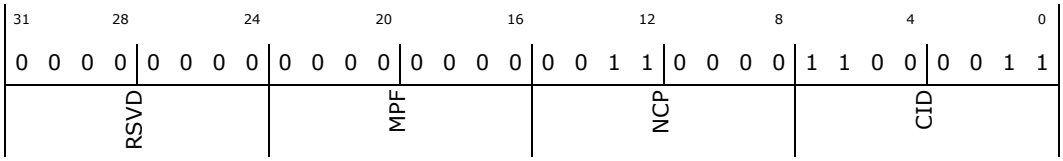
7.3.67 Debug Capability Descriptor Parameters (DCDP)—Offset 8740h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8740h

Default: 000030C3h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
23:16	0x0 RW	**Max Power Field (MPF):** This field will be used by USB Debug Device to report maximum power consumption when the device is fully operational. This value is returned by bMaxPower field in response to Configuration Descriptor read from the debug device. Note: bU1DevExitLat and bU2DevExitLat fields returned in BOS Descriptor read will be taken from the corresponding fields from the Host Controller space. **Power Well:** Core
15:8	0x30 RW/S	**NEXT CAPABILITY POINTER (NCP):** Reserved. **Power Well:** Core
7:0	0xc3 RW/S	**Capability ID (CID):** Reserved. **Power Well:** Core

7.3.68 Debug Device Control ODMA (DBGDEV_CTRL_ODMA_REG)—Offset 8748h

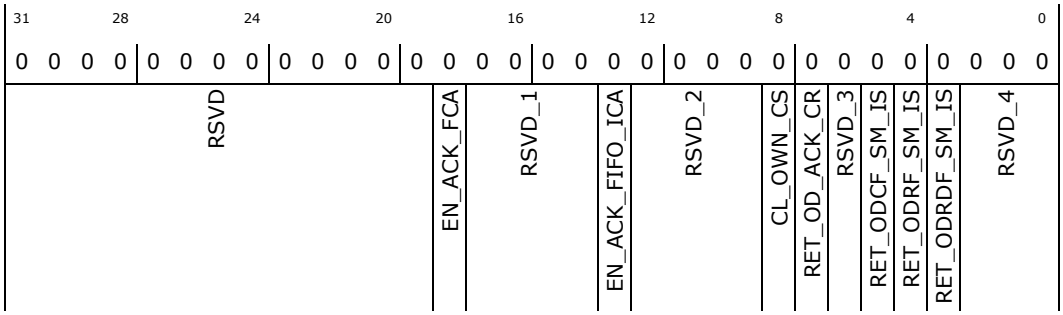
This register contains a number of fields that provide a specific level of configurability for the OUT DMA that is part of Debug Device logic. This configurability is above and beyond that defined in the xHCI specification.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8748h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0x0 RW	**Reserved (RSVD):** Reserved. **Power Well:** Core
18	0x0 RW	**Enable ACK FIFO credit accounting (EN_ACK_FCA):** Setting this field will enable ACK FIFO credit accounting. ODMA will ensure that ample room exists in the ACK FIFO for expected device responses prior to initiating a given DP **Power Well:** Core
17:14	0x0 RW	**Reserved (RSVD_1):** Reserved. **Power Well:** Core
13	0x0 RW	**Enable ACK FIFO ICA mechanisms (EN_ACK_FIFO_ICA):** Setting this field will enable ACK FIFO individual credit accounting mechanisms for Async vs. Periodic Endpoints. ODMA will ensure that ample room exists in the ACK FIFO for expected device responses prior to initiating a given DP **Power Well:** Core
12:9	0x0 RW	**Reserved (RSVD_2):** Reserved. **Power Well:** Core
8	0x0 RW	**Clear ownership of context semaphore (CL_OWN_CS):** Setting this field generates a pulse that clears the ownership of the context semaphore that is shared between the Out DMA Response and Completion Finite State Machines **Power Well:** Core
7	0x0 RW	**Return OD ACK credits (RET_OD_ACK_CR):** Setting this field generates a pulse that implicitly returns all of the Out DMA ACK credits on all ports **Power Well:** Core
6	0x0 RW	**Reserved (RSVD_3):** Reserved. **Power Well:** Core
5	0x0 RW	**Return ODCF SM to idle state (RET_ODCF_SM_IS):** Setting this field generates a pulse that returns the Out DMA Completion Finite State Machine into the IDLE state **Power Well:** Core
4	0x0 RW	**Return ODRF SM to idle state (RET_ODRF_SM_IS):** Setting this field generates a pulse that returns the Out DMA Response Finite State Machine into the IDLE state **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**Return ODRDF SM to idle state (RET_ODRDF_SM_IS):** Setting this field generates a pulse that returns the Out DMA Read Finite State Machine into the IDLE state **Power Well:** Core
2:0	0x0 RW	**Reserved (RSVD_4):** Reserved. **Power Well:** Core

7.3.69 SSIC Policy and Implementation Specific Registers Capability ID register (SSIC_IMPLEMENTATION_CAPABILITY_ID_REG)—Offset 8800h

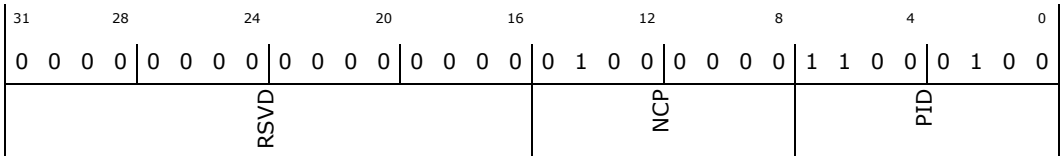
Chicken bits and Policy bits associated with SSIC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8800h

Default: 000040C4h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
15:8	0x40 RO	**Next Capability Pointer (NCP):** Reserved. **Power Well:** Core
7:0	0xc4 RO	**Supported Protocol ID (PID):** Reserved. **Power Well:** Core

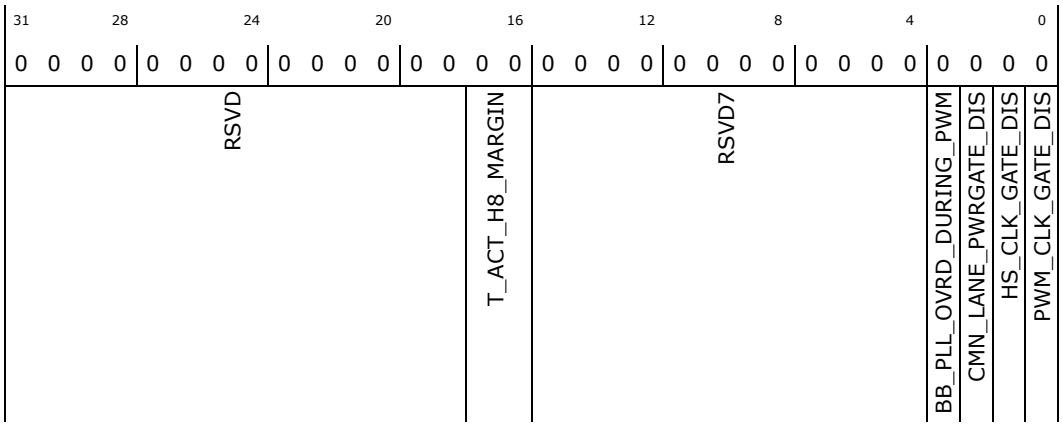
7.3.70 SSIC global configuration control register (SSIC_GLOBAL_CONFIG_CONTROL_REG)—Offset 8804h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8804h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
17:16	0x0 RW	**T_ACT_H8_MARGIN:** Specifies the margin time added to the tActivate spec time of 100us in T_ACT_H8_TIME. 11: Reserved 10: 50us 01: 20us (default for ModPHY) 00: 10us (default for MIPI MPHY) **Power Well:** Core
15:4	0x0 RO	**Reserved1 (RSVD7):** Reserved. **Power Well:** Core
3	0x0 RW	**BB_PLL_OVRD_DURING_PWM:** Reserved. **Power Well:** Core
2	0x0 RW	**CMN_LANE_PWRGATE_DIS:** This will disable the MPHY common lane power gate. **Power Well:** Core
1	0x0 RW	**HS_CLK_GATE_DIS:** This will disable the HS Clock gate request from XHCI to MIPI PLL. **Power Well:** Core
0	0x0 RW	**PWM_CLK_GATE_DIS:** This will disable the PWM Clock gate request from XHCI to MIPI PLL. **Power Well:** Core

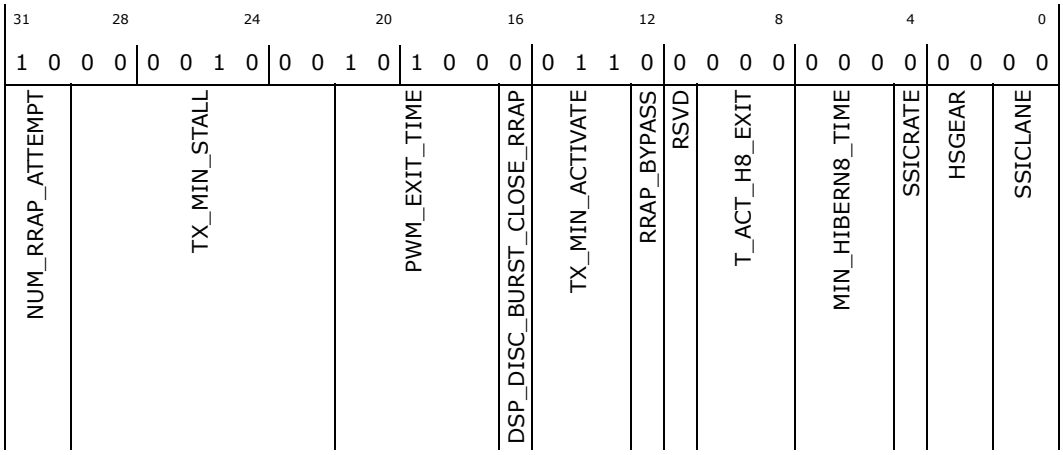
7.3.71 reg_SSIC_CONFIG_REG1_type (PORT1_SSIC_CONFIG_REG1)—Offset 8808h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8808h

Default: 82286000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x2 RW	**NUM_RRAP_ATTEMPT:** Specify the number of RRAP access attempt if there was tRRAPInitiatorResponse timeout. **Power Well:** Core
29:22	0x8 RW	**TX_MIN_STALL:** (TX_Min_STALL_NoConfig_Time_Capability in MIPI PHY Spec). PA will ensure TX_MIN_STALL time in STALL before entering HS-BURST or HIBERN8. Specifies minimum time in SI in STALL state. **Power Well:** Core
21:17	0x14 RW	**PWM_EXIT_TIME:** This will be max of RX_Min_ActivateTime_Capability and TX_Min_SAVE_Config_Time_Capability in MIPI PHY Specs) Specifies minimum activate time needed in 5us steps. PA will wait PWM_EXIT_TIME time after exiting PWM to start HS-BURST. SSIC spec requires it to be at 100us. For speedup mode this time would be in 1us steps. **Power Well:** Core
16	0x0 RW	**DSP_DISC_BURST_CLOSE_RRAP:** 0 - Send BURST Closure RRAP for DSP Disconnect 1 - Dont send Burst Closure RRAP for DSP Disconnect. For device PWM exit would be indication for DSP Disconnect. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:13	0x3 RW	**TX_MIN_ACTIVATE:** (TX_Min_ActivateTime in MIPI PHY Spec) Specifies minimum activate time needed in 100us steps. PA will wait TX_MIN_ACTIVATE time after H8 exit to start of PWM Burst. SSIC spec requires it to be at 1.5ms. For speedup mode this time would be 10us to 150us in steps of 10us. **Power Well:** Core
12	0x0 RW	**RRAP_BYPASS:** Enables DFx Loopback test mode where RRAP command / response is bypassed for HS_CONFIG and PWM_BURST_CLOSURE. Host will still perform initial enter and exit PWM mode with no RRAP transfers. **Power Well:** Core
11	0x0 RW	**Reserved (RSVD):** Reserved. **Power Well:** Core
10:8	0x0 RW	**T_ACT_H8_EXIT:** Specifies minimum time in 100us steps for T_ACTIVATE_TIME to exit H8. Val: Si Time / Fast Sim Time 000: 110us / 10us 001: 210us / 20us 110: 710us / 70us 111: 5ms / 500us Spec required timing is 100us. **Power Well:** Core
7:5	0x0 RW	**MIN_HIBERN8_TIME:** Minimum time in HIBERN8 state 0 110us 1 210us .. 7 810us PA will ensure MIN_HIBERN8_TIME in its TX HIBERN8. For speedup mode this time will be from 10us to 80us in steps of 10us. **Power Well:** Core
4	0x0 RW	**SSICRATE:** 0 A Series 1 B Series **Power Well:** Core
3:2	0x0 RW	**HSGEAR:** 0=HS-G1 1=HS-G2 2=HS-G3 **Power Well:** Core
1:0	0x0 RW	**SSICLANE:** 0=Single lane 1=Bi-lane 2=Quad-lane **Power Well:** Core

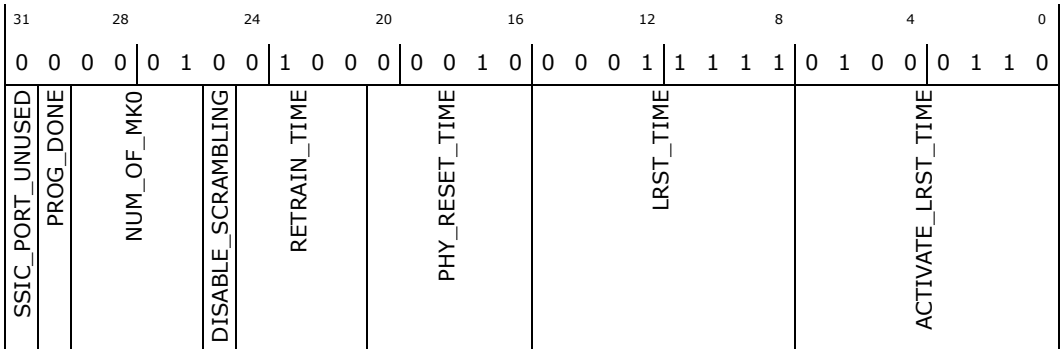
7.3.72 reg_SSIC_CONFIG_REG2_type (PORT1_SSIC_CONFIG_REG2)—Offset 880Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 880Ch

Default: 04821F46h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SSIC_PORT_UNUSED:** This indicates that no SSIC device is connected to the port and PORTSC register would always reflect DISCONNECTED. **Power Well:** Core
30	0x0 RW	**PROG_DONE:** BIOS will program this bit once SSIC profile programming is done. SSIC will enable the MPHY and local PLL once this bit is set. **Power Well:** Core
29:26	0x1 RW	**NUM_OF_MK0:** Number of MK0 which transmitter will send before sending any data. **Power Well:** Core
25	0x0 RW	**DISABLE_SCRAMBLING:** This bit will disable scrambling in HS-BURST **Power Well:** Core
24:21	0x4 RW	**RETRAIN_TIME:** Corresponds to time in 10us to detect improper training of the local and remote M-RX as part of HS-BURST entry. SSIC Spec specific 40 to 50us **Power Well:** Core
20:16	0x2 RW	**PHY_RESET_TIME:** Corresponds to time in 100ns, PA will drive PHY RESET for MIPI PHY. **Power Well:** Core
15:8	0x1f RW	**LRST_TIME:** Corresponds to time in 100us PA will drive DIF-P for line reset. MIPI PHY specifies 3.1 ms Minimum. For speedup mode this time will be in steps of 5us. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x46 RW	**ACTIVATE_LRST_TIME:** (Corresponds to tResetDIFN) Specifies in step of 1ms period of time a DSP is required to drive a DIF-N prior to a LINE-RESET. SSIC spec defined range is 60-80ms. For speedup mode this time will be from 5us to 400us in steps of 5us. **Power Well:** Core

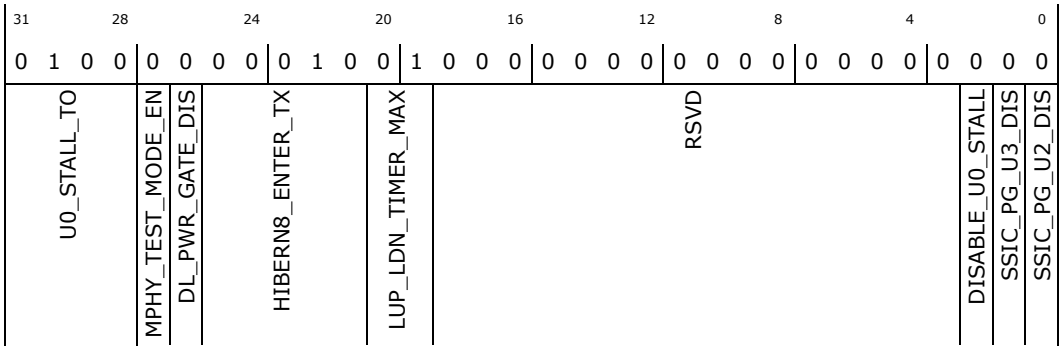
7.3.73 reg_SSIC_CONFIG_REG3_type (PORT1_SSIC_CONFIG_REG3)—Offset 8810h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8810h

Default: 40480000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x4 RW	**U0_STALL_TO:** Time in 2^[U-STALL_TO] clock for U0 STALL entry. If there is no packet in arbiter for U0_STALL_TO time, PA will enable U0 STALL if DISABLE_U0_STALL is not set. 0000 0011 (Not recommended) 0100 16 SSIC HS CLK . 1111 32768 SSIC HS CLK **Power Well:** Core
27	0x0 RW	**MPHY_TEST_MODE_EN:** When this bit is set, controller would not initiate any PWM once it enters PWM Mode. It will wait for tester to send Loopback RRAP Command. **Power Well:** Core
26	0x0 RW	**DL_PWR_GATE_DIS:** Reserved. **Power Well:** Core
25:21	0x2 RW	**HIBERN8_ENTER_TX:** The time PA will drive DIF-N after last bit of Line-CFG before entering H8. In steps of 50ns. Legal range is 50 to 1000ns. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
20:19	0x1 RW	**LUP_LDN_TIMER_MAX:** 00: 10 us 01: 100 us 10: 1000us /1ms 11: (Timer is disable and dont transmit LDN) **Power Well:** Core
18:3	0x0 RW	**RESERVED (RSVD):** rsvd **Power Well:** Core
2	0x0 RW	**DISABLE_U0_STALL:** This bit will disable the STALL entry in U0 **Power Well:** Core
1	0x0 RW	**SSIC_PG_U3_DIS:** This disables MPHY DL PG during U3. **Power Well:** Core
0	0x0 RW	**SSIC_PG_U2_DIS:** This disables MPHY DL PG during U2. **Power Well:** Core

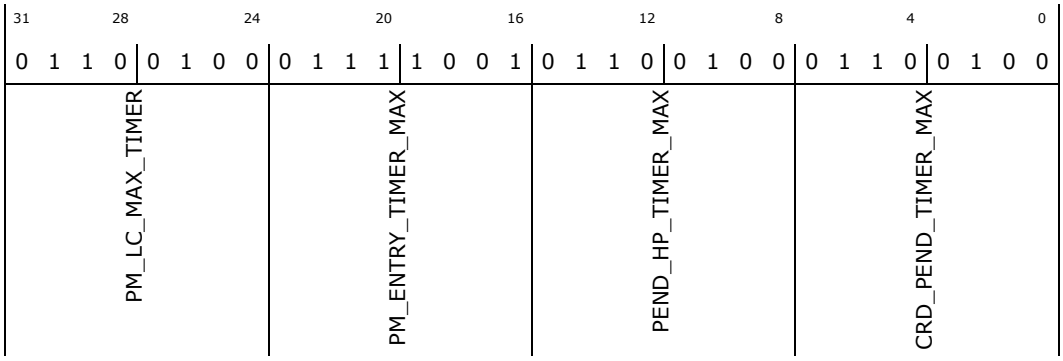
7.3.74 reg_SSIC_CONFIG_REG4_type (PORT1_SSIC_CONFIG_REG4)—Offset 8814h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8814h

Default: 64796464h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x64 RW	**PM_LC_MAX_TIMER:** In steps of 1us. Default 100us **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
23:16	0x79 RW	**PM_ENTRY_TIMER_MAX:** In steps of 1us. Default 100us **Power Well:** Core
15:8	0x64 RW	**PEND_HP_TIMER_MAX:** In steps of 1us. Default 100us **Power Well:** Core
7:0	0x64 RW	**CRD_PEND_TIMER_MAX:** In steps of 1us. Default 100us **Power Well:** Core

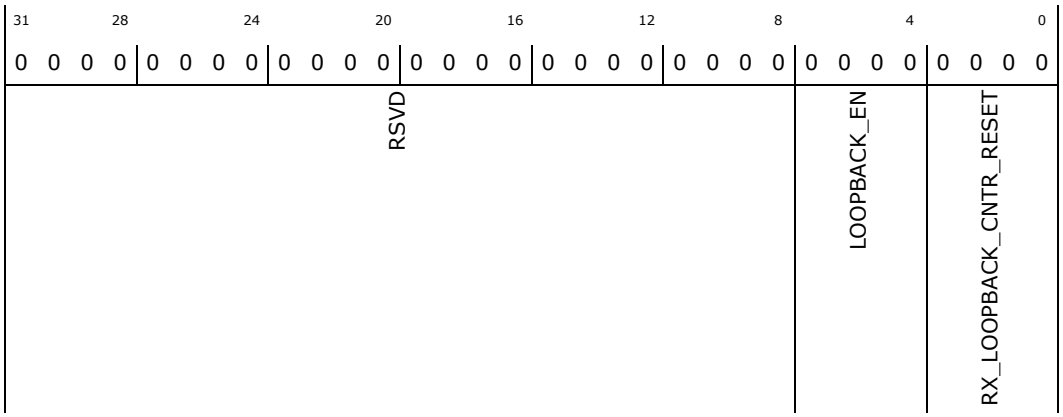
7.3.75 reg_SSIC_LOOPBACK_CONFIG_REG_type (PORT1_SSIC_LOOPBACK_CONFIG_REG)—Offset 8818h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8818h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
7:4	0x0 RO	**LOOPBACK_EN:** This Register is used to enable Conformance Loopback in the Target in the specified PAIR.. Bit [0]: Writing 1b1 enables the loopback mode in PAIR0. Writing 1b0 shall have no effect. Bit [1]: Writing 1b1 enables the loopback mode in PAIR1. Writing 1b0 shall have no effect. Bit [2]: Writing 1b1 enables the loopback mode in PAIR2. Writing 1b0 shall have no effect. Bit [3]: Writing 1b1 enables the loopback mode in PAIR3. Writing 1b0 shall have no effect. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x0 RO	**RX LOOPBACK CNTR RESET (RX_LOOPBACK_CNTR_RESET):** Reset RX_BURST_COUNT and RX_ERR_COUNT, write only, self-clearing. Bit [0] for PAIR0 Bit [1] for PAIR1 Bit [2] for PAIR2 Bit [3] for PAIR3 **Power Well:** Core

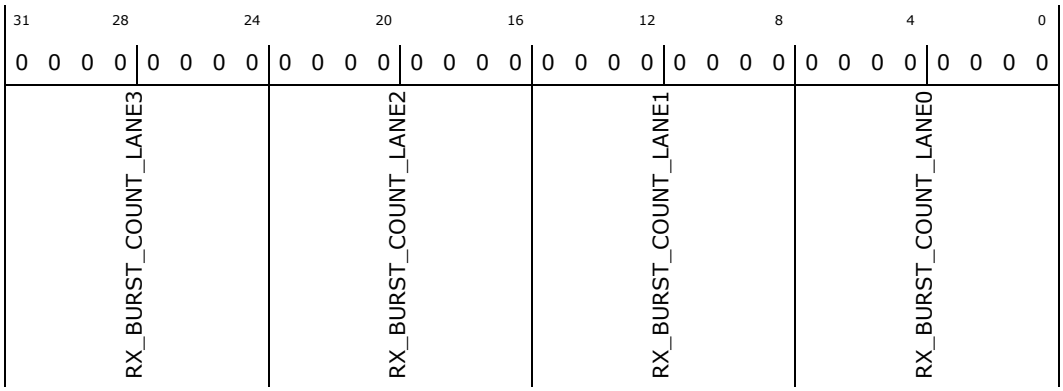
7.3.76 reg_SSIC_LOOPBACK_BURST_COUNT_REG_type (PORT1_SSIC_LOOPBACK_BURST_COUNT_REG)—Offset 881Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 881Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RX_BURST_COUNT_LANE3:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
23:16	0x0 RO	**RX_BURST_COUNT_LANE2:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**RX_BURST_COUNT_LANE1:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
7:0	0x0 RO	**RX_BURST_COUNT_LANE0:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core

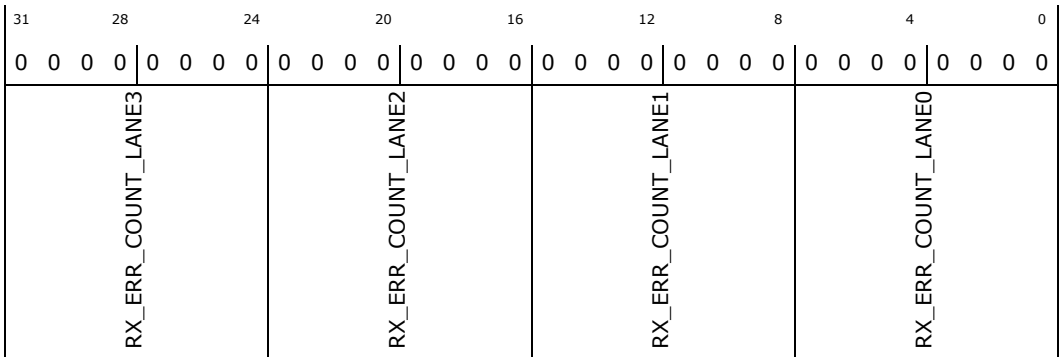
7.3.77 reg_SSIC_LOOPBACK_ERROR_COUNT_REG_type (PORT1_SSIC_LOOPBACK_ERROR_COUNT_REG)—Offset 8820h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8820h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RX_ERR_COUNT_LANE3:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
23:16	0x0 RO	**RX_ERR_COUNT_LANE2:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
15:8	0x0 RO	**RX_ERR_COUNT_LANE1:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
7:0	0x0 RO	**RX_ERR_COUNT_LANE0:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core

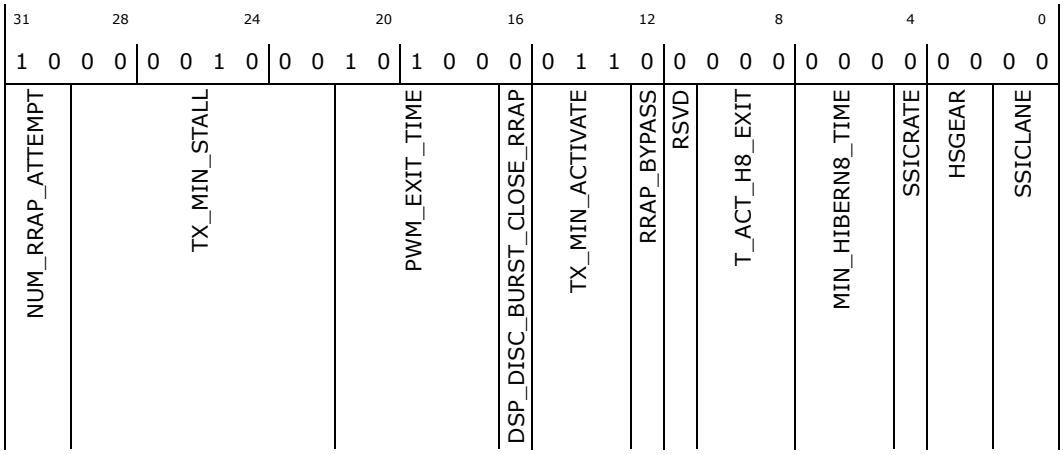
7.3.78 reg_SSIC_CONFIG_REG1_type (PORT2_SSIC_CONFIG_REG1)—Offset 8838h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8838h

Default: 82286000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x2 RW	**NUM_RRAP_ATTEMPT:** Specify the number of RRAP access attempt if there was tRRAPInitiatorResponse timeout. **Power Well:** Core
29:22	0x8 RW	**TX_MIN_STALL:** (TX_Min_STALL_NoConfig_Time_Capability in MIPI PHY Spec). PA will ensure TX_MIN_STALL time in STALL before entering HS-BURST or HIBERN8. Specifies minimum time in SI in STALL state. **Power Well:** Core
21:17	0x14 RW	**PWM_EXIT_TIME:** This will be max of RX_Min_ActivateTime_Capability and TX_Min_SAVE_Config_Time_Capability in MIPI PHY Specs) Specifies minimum activate time needed in 5us steps. PA will wait PWM_EXIT_TIME time after exiting PWM to start HS-BURST. SSIC spec requires it to be at 100us. For speedup mode this time would be in 1us steps. **Power Well:** Core
16	0x0 RW	**DSP_DISC_BURST_CLOSE_RRAP:** 0 - Send BURST Closure RRAP for DSP Disconnect 1 - Dont send Burst Closure RRAP for DSP Disconnect. For device PWM exit would be indication for DSP Disconnect. **Power Well:** Core
15:13	0x3 RW	**TX_MIN_ACTIVATE:** (TX_Min_ActivateTime in MIPI PHY Spec) Specifies minimum activate time needed in 100us steps. PA will wait TX_MIN_ACTIVATE time after H8 exit to start of PWM Burst. SSIC spec requires it to be at 1.5ms. For speedup mode this time would be 10us to 150us in steps of 10us. **Power Well:** Core
12	0x0 RW	**RRAP_BYPASS:** Enables DFx Loopback test mode where RRAP command / response is bypassed for HS_CONFIG and PWM_BURST_CLOSURE. Host will still perform initial enter and exit PWM mode with no RRAP transfers. **Power Well:** Core
11	0x0 RW	**Reserved (RSVD):** Reserved. **Power Well:** Core
10:8	0x0 RW	**T_ACT_H8_EXIT:** Specifies minimum time in 100us steps for T_ACTIVATE_TIME to exit H8. Val: Si Time / Fast Sim Time 000: 110us / 10us 001: 210us / 20us 110: 710us / 70us 111: 5ms / 500us Spec required timing is 100us. **Power Well:** Core
7:5	0x0 RW	**MIN_HIBERN8_TIME:** Minimum time in HIBERN8 state 0 110us 1 210us .. 7 810us PA will ensure MIN_HIBERN8_TIME in its TX HIBERN8. For speedup mode this time will be from 10us to 80us in steps of 10us. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**SSICRATE:** 0 A Series 1 B Series **Power Well:** Core
3:2	0x0 RW	**HSGEAR:** 0=HS-G1 1=HS-G2 2=HS-G3 **Power Well:** Core
1:0	0x0 RW	**SSICLANE:** 0=Single lane 1=Bi-lane 2=Quad-lane **Power Well:** Core

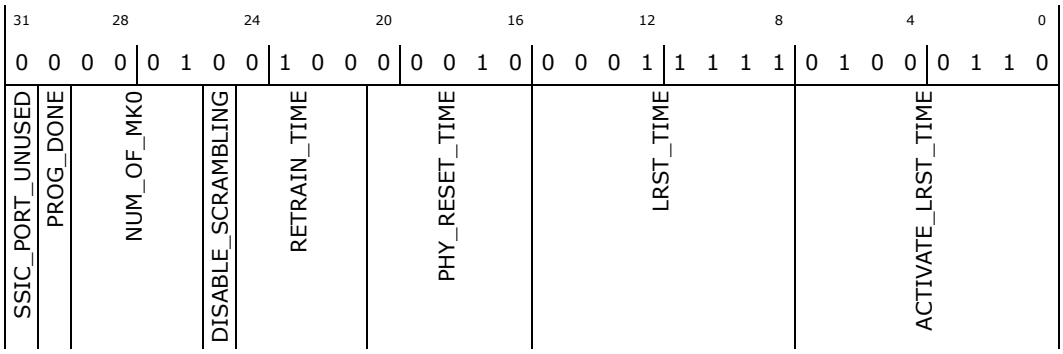
7.3.79 reg_SSIC_CONFIG_REG2_type (PORT2_SSIC_CONFIG_REG2)—Offset 883Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 883Ch

Default: 04821F46h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SSIC_PORT_UNUSED:** This indicates that no SSIC device is connected to the port and PORTSC register would always reflect DISCONNECTED. **Power Well:** Core
30	0x0 RW	**PROG_DONE:** BIOS will program this bit once SSIC profile programming is done. SSIC will enable the MPHY and local PLL once this bit is set. **Power Well:** Core
29:26	0x1 RW	**NUM_OF_MK0:** Number of MK0 which transmitter will send before sending any data. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
25	0x0 RW	**DISABLE_SCRAMBLING:** This bit will disable scrambling in HS-BURST **Power Well:** Core
24:21	0x4 RW	**RETRAIN_TIME:** Corresponds to time in 10us to detect improper training of the local and remote M-RX as part of HS-BURST entry. SSIC Spec specific 40 to 50us **Power Well:** Core
20:16	0x2 RW	**PHY_RESET_TIME:** Corresponds to time in 100ns, PA will drive PHY RESET for MIPI PHY. **Power Well:** Core
15:8	0x1f RW	**LRST_TIME:** Corresponds to time in 100us PA will drive DIF-P for line reset. MIPI PHY specifies 3.1 ms Minimum. For speedup mode this time will be in steps of 5us. **Power Well:** Core
7:0	0x46 RW	**ACTIVATE_LRST_TIME:** (Corresponds to tResetDIFN) Specifies in step of 1ms period of time a DSP is required to drive a DIF-N prior to a LINE-RESET. SSIC spec defined range is 60-80ms. For speedup mode this time will be from 5us to 400us in steps of 5us. **Power Well:** Core

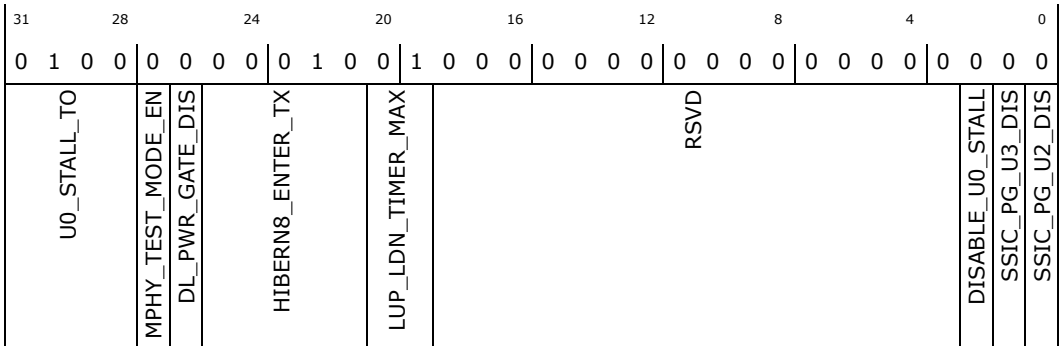
7.3.80 reg_SSIC_CONFIG_REG3_type (PORT2_SSIC_CONFIG_REG3)—Offset 8840h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8840h

Default: 40480000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x4 RW	**U0_STALL_TO:** Time in 2^[U-STALL_TO] clock for U0 STALL entry. If there is no packet in arbiter for U0_STALL_TO time, PA will enable U0 STALL if DISABLE_U0_STALL is not set. 0000 0011 (Not recommended) 0100 16 SSIC HS CLK . 1111 32768 SSIC HS CLK **Power Well:** Core
27	0x0 RW	**MPHY_TEST_MODE_EN:** When this bit is set, controller would not initiate any PWM once it enters PWM Mode. It will wait for tester to send Loopback RRAP Command. **Power Well:** Core
26	0x0 RW	**DL_PWR_GATE_DIS:** Reserved. **Power Well:** Core
25:21	0x2 RW	**HIBERN8_ENTER_TX:** The time PA will drive DIF-N after last bit of Line-CFG before entering H8. In steps of 50ns. Legal range is 50 to 1000ns. **Power Well:** Core
20:19	0x1 RW	**LUP_LDN_TIMER_MAX:** 00: 10 us 01: 100 us 10: 1000us /1ms 11: (Timer is disable and dont transmit LDN) **Power Well:** Core
18:3	0x0 RW	**RESERVED (RSVD):** rsvd **Power Well:** Core
2	0x0 RW	**DISABLE_U0_STALL:** This bit will disable the STALL entry in U0 **Power Well:** Core
1	0x0 RW	**SSIC_PG_U3_DIS:** This disables MPHY DL PG during U3. **Power Well:** Core
0	0x0 RW	**SSIC_PG_U2_DIS:** This disables MPHY DL PG during U2. **Power Well:** Core

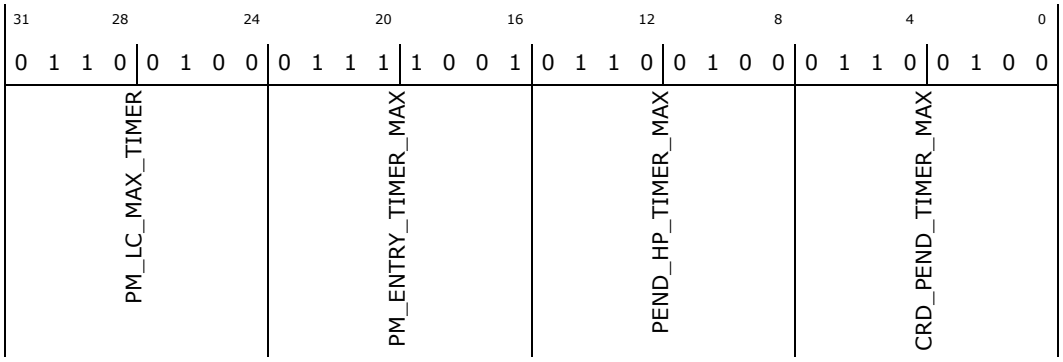
7.3.81 reg_SSIC_CONFIG_REG4_type (PORT2_SSIC_CONFIG_REG4)—Offset 8844h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8844h

Default: 64796464h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x64 RW	**PM_LC_MAX_TIMER:** In steps of 1us. Default 100us **Power Well:** Core
23:16	0x79 RW	**PM_ENTRY_TIMER_MAX:** In steps of 1us. Default 100us **Power Well:** Core
15:8	0x64 RW	**PEND_HP_TIMER_MAX:** In steps of 1us. Default 100us **Power Well:** Core
7:0	0x64 RW	**CRD_PEND_TIMER_MAX:** In steps of 1us. Default 100us **Power Well:** Core

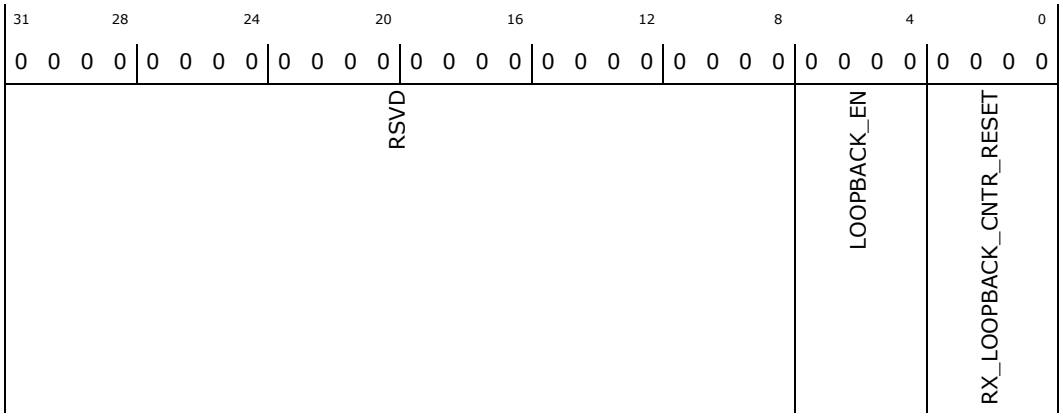
7.3.82 reg_SSIC_LOOPBACK_CONFIG_REG_type (PORT2_SSIC_LOOPBACK_CONFIG_REG)—Offset 8848h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8848h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
7:4	0x0 RO	**LOOPBACK_EN:** This Register is used to enable Conformance Loopback in the Target in the specified PAIR.. Bit [0]: Writing 1b1 enables the loopback mode in PAIR0. Writing 1b0 shall have no effect. Bit [1]: Writing 1b1 enables the loopback mode in PAIR1. Writing 1b0 shall have no effect. Bit [2]: Writing 1b1 enables the loopback mode in PAIR2. Writing 1b0 shall have no effect. Bit [3]: Writing 1b1 enables the loopback mode in PAIR3. Writing 1b0 shall have no effect. **Power Well:** Core
3:0	0x0 RO	**RX LOOPBACK CNTR RESET (RX_LOOPBACK_CNTR_RESET):** Reset RX_BURST_COUNT and RX_ERR_COUNT, write only, self-clearing. Bit [0] for PAIR0 Bit [1] for PAIR1 Bit [2] for PAIR2 Bit [3] for PAIR3 **Power Well:** Core

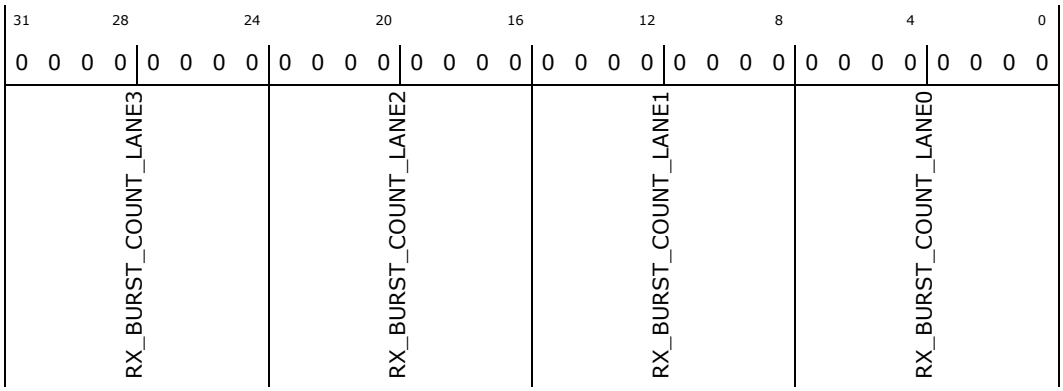
7.3.83 reg_SSIC_LOOPBACK_BURST_COUNT_REG_type (PORT2_SSIC_LOOPBACK_BURST_COUNT_REG)—Offset 884Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 884Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RX_BURST_COUNT_LANE3:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
23:16	0x0 RO	**RX_BURST_COUNT_LANE2:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
15:8	0x0 RO	**RX_BURST_COUNT_LANE1:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
7:0	0x0 RO	**RX_BURST_COUNT_LANE0:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core

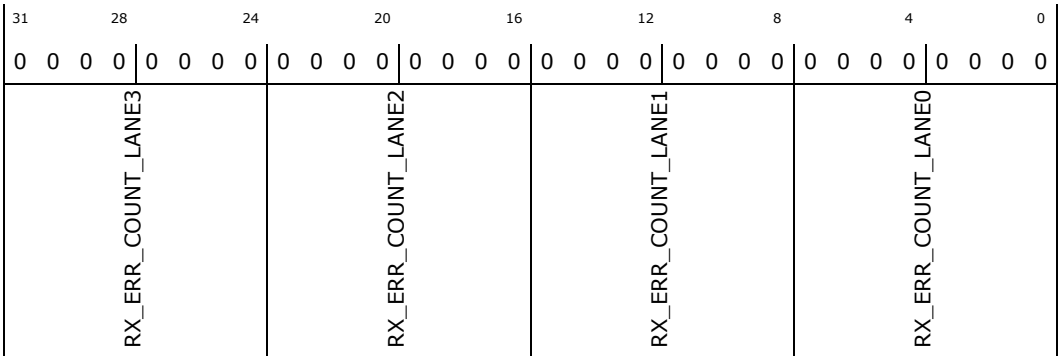
7.3.84 reg_SSIC_LOOPBACK_ERROR_COUNT_REG_type (PORT2_SSIC_LOOPBACK_ERROR_COUNT_REG)—Offset 8850h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8850h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RX_ERR_COUNT_LANE3:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
23:16	0x0 RO	**RX_ERR_COUNT_LANE2:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
15:8	0x0 RO	**RX_ERR_COUNT_LANE1:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
7:0	0x0 RO	**RX_ERR_COUNT_LANE0:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core

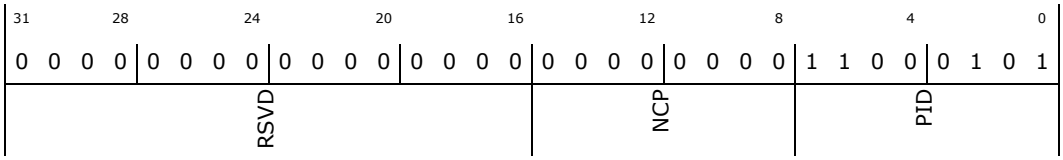
7.3.85 SSIC Local and Remote Profile Registers Capability ID register (SSIC_PROFILE_CAPABILITY_ID_REG)—Offset 8900h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8900h

Default: 000000C5h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RW/S	**Next Capability Pointer (NCP):** Reserved. **Power Well:** Core
7:0	0xc5 RW/S	**Supported Protocol ID (PID):** Reserved. **Power Well:** Core

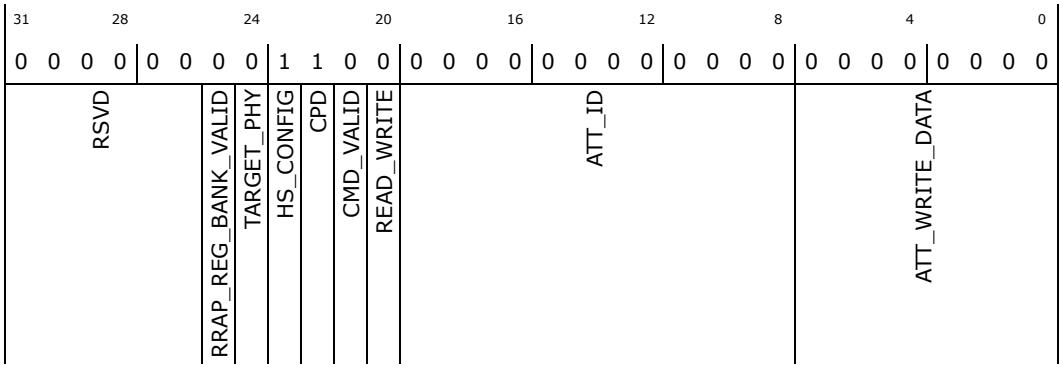
7.3.86 SSIC Port N Register Access Control (PORT1_REGISTER_ACCESS_CONTROL)—Offset 8904h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8904h

Default: 00C00000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
25	0x0 RW	**RRAP Register Bank Valid (RRAP_REG_BANK_VALID):** 0 = No valid Commands in the Lane N register bank. Host Controller can close the PWM burst once commands from this register are completed. 1 = Valid commands present in the Lane N register bank. Host controller must complete commands from the register bank before closing the burst. **Power Well:** Core
24	0x0 RW	**Target Phy (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy Setting this bit to 1 allows the use of this command mechanism to write to local Phy profile and AFE tuning registers Primarily as a back up option. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
23	0x1 RW	**HS_Config (HS_CONFIG):** When this bit is set to 1 the host controller will issue an RRAP write with HS_Config=1 once it sees Command Phase Done = 1 **Power Well:** Core
22	0x1 RW	**Command Phase Done (CPD):** When set to 1, this indicates that SW has completed performing RRAP cycles through the command register. **Power Well:** Core
21	0x0 RW	**Command Valid (CMD_VALID):** When written to 1 indicates that the Attribute ID and Attribute Data for writes fields are valid. **Power Well:** Core
20	0x0 RW	**Read_Write (READ_WRITE):** 0 = Write 1= Read **Power Well:** Core
19:8	0x0 RW	**Attribute ID (ATT_ID):** Attribute ID that is being written or read **Power Well:** Core
7:0	0x0 RW	**Attribute Write Data (ATT_WRITE_DATA):** Data byte that is required to be written to either the local phy or the remote phy **Power Well:** Core

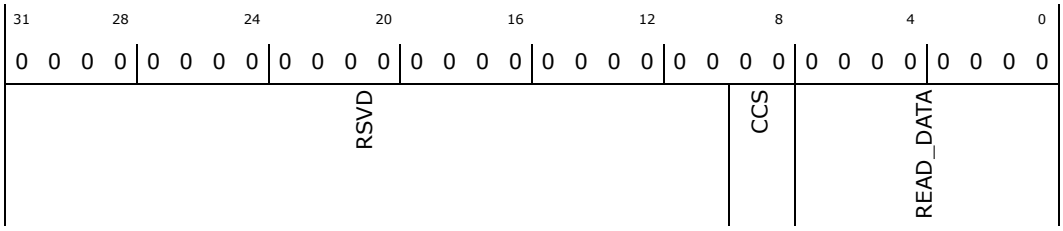
7.3.87 SSIC Port N Register Access Status (PORT1_REGISTER_ACCESS_STATUS)—Offset 8908h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8908h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
9:8	0x0 RW	**Command Completion Status (CCS):** 00 = Command not complete 01 = Command complete with Success 10 = Command complete with Error These bits must be cleared before a new command is initiated. **Power Well:** Core
7:0	0x0 RO	**Read data (READ_DATA):** Data read as a result of the RRAP operation **Power Well:** Core

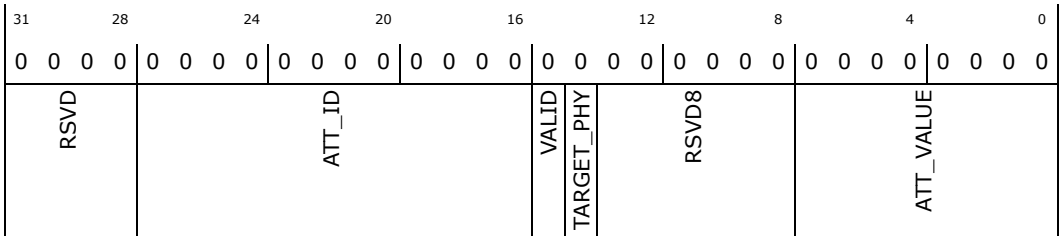
7.3.88 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG0)—Offset 890Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 890Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

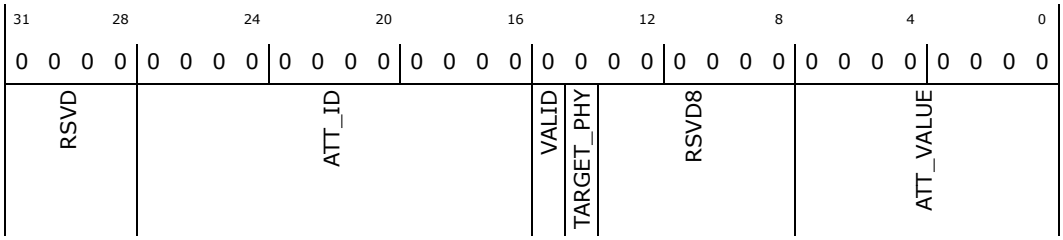
7.3.89 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG1)—Offset 8910h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8910h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

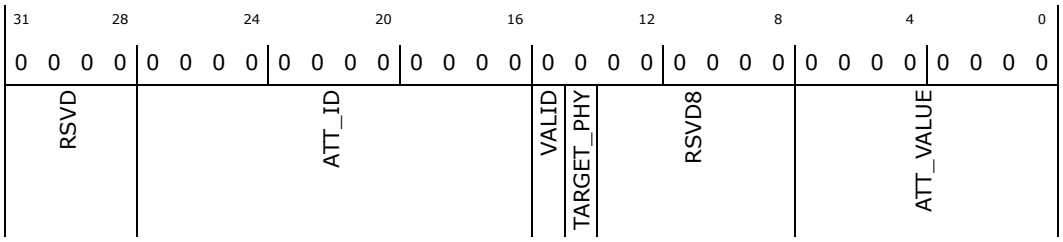
7.3.90 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG2)—Offset 8914h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8914h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

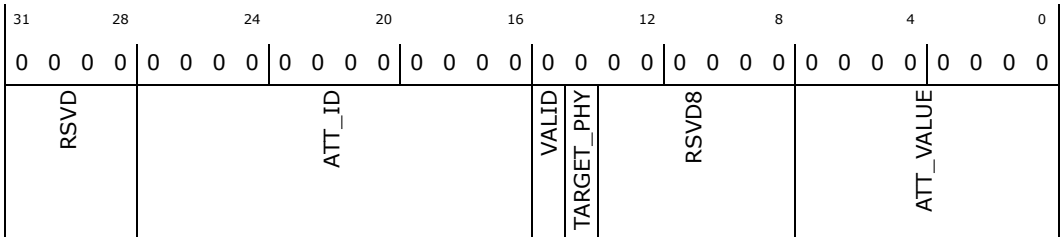
7.3.91 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG3)—Offset 8918h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8918h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

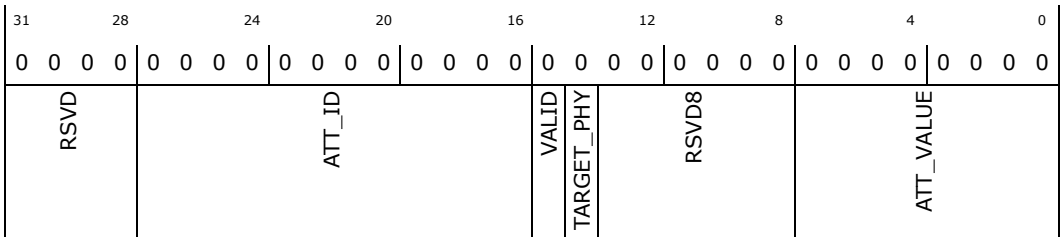
7.3.92 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG4)—Offset 891Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 891Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

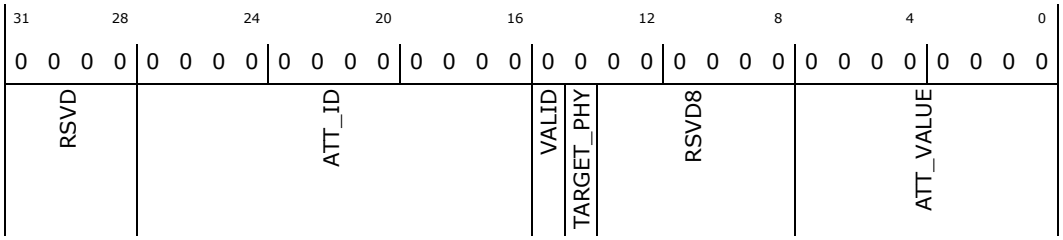
7.3.93 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG5)—Offset 8920h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8920h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

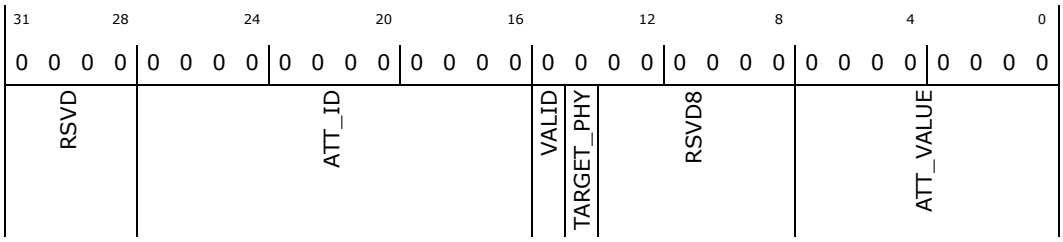
7.3.94 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG6)—Offset 8924h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8924h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

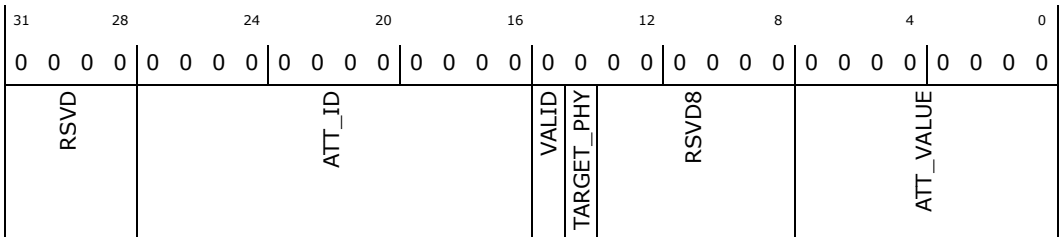
7.3.95 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG7)—Offset 8928h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8928h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

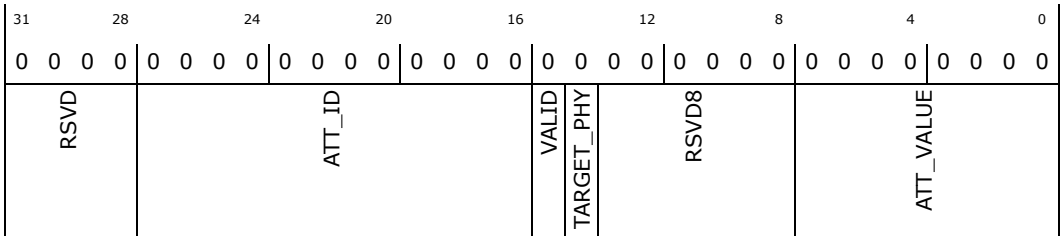
7.3.96 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG8)—Offset 892Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 892Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

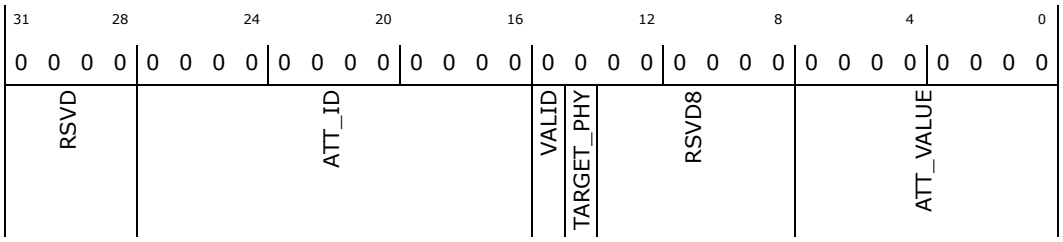
7.3.97 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG9)—Offset 8930h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8930h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

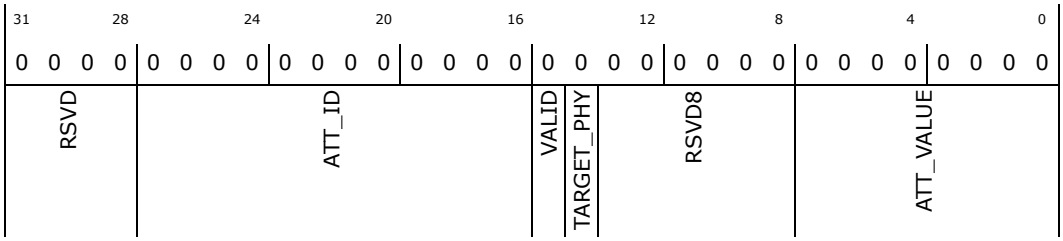
7.3.98 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG10)—Offset 8934h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8934h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

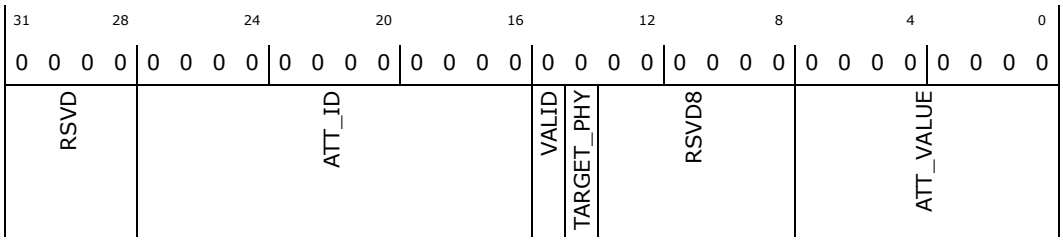
7.3.99 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG11)—Offset 8938h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8938h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

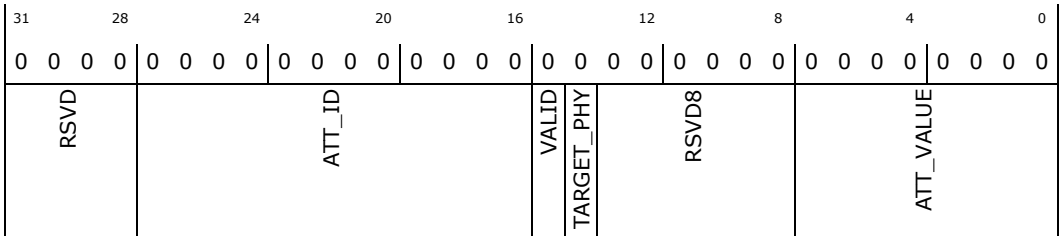
7.3.100 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG12)—Offset 893Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 893Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

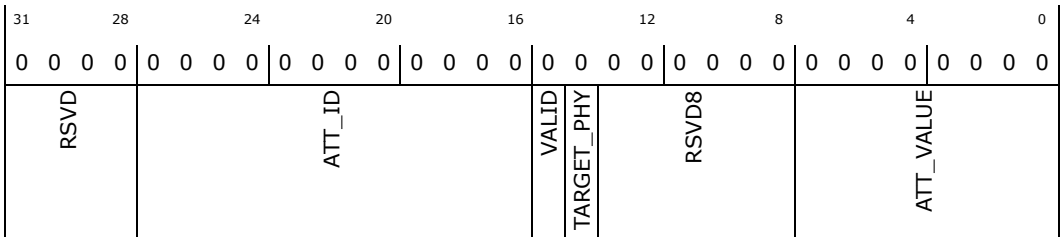
7.3.101 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG13)—Offset 8940h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8940h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

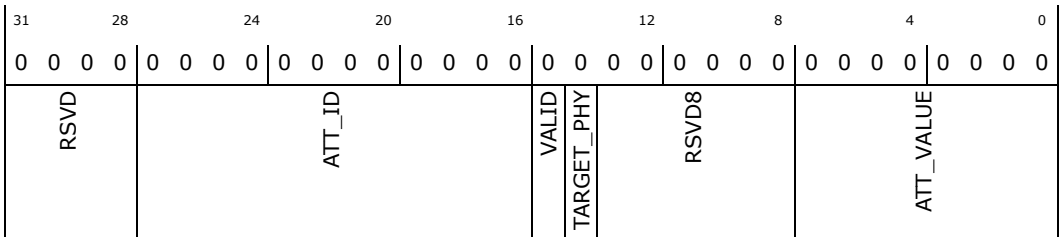
7.3.102 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG14)—Offset 8944h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8944h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

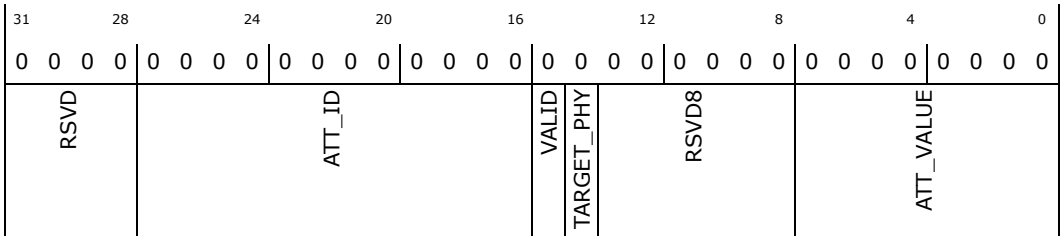
7.3.103 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG15)—Offset 8948h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8948h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

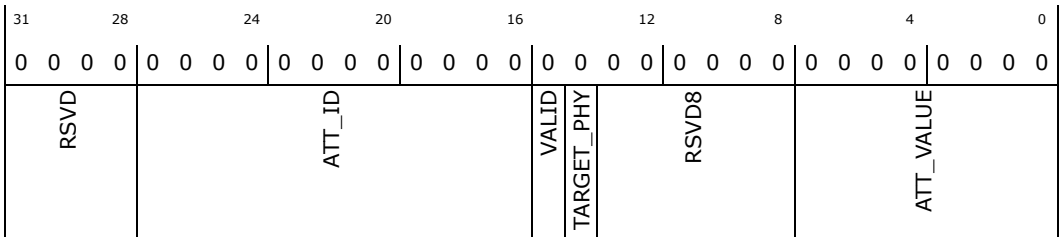
7.3.104 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG16)—Offset 894Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 894Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

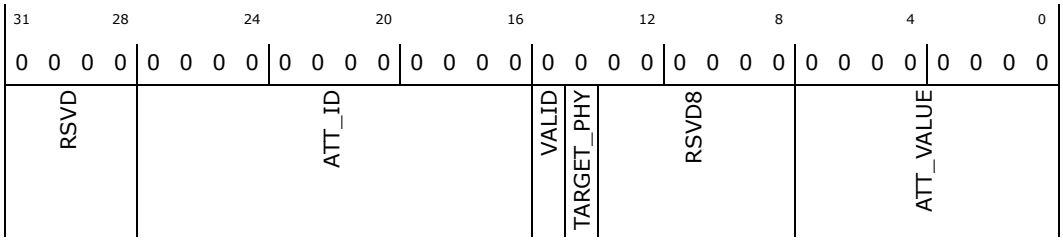
7.3.105 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG17)—Offset 8950h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8950h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

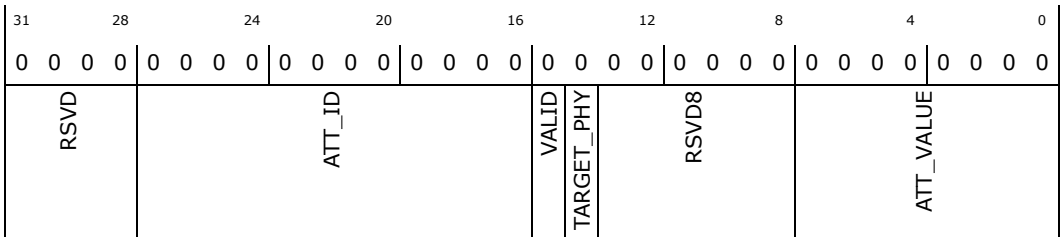
7.3.106 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG18)—Offset 8954h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8954h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

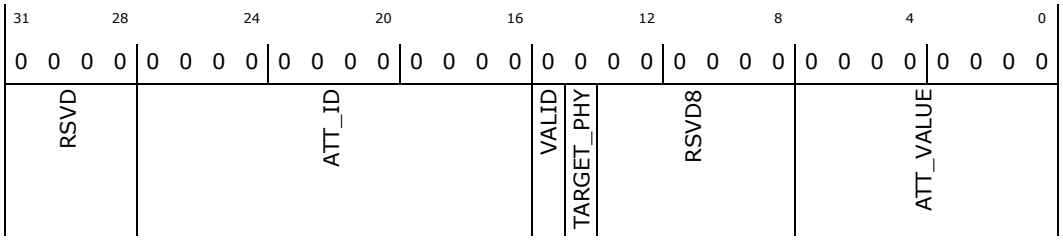
7.3.107 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG19)—Offset 8958h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8958h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

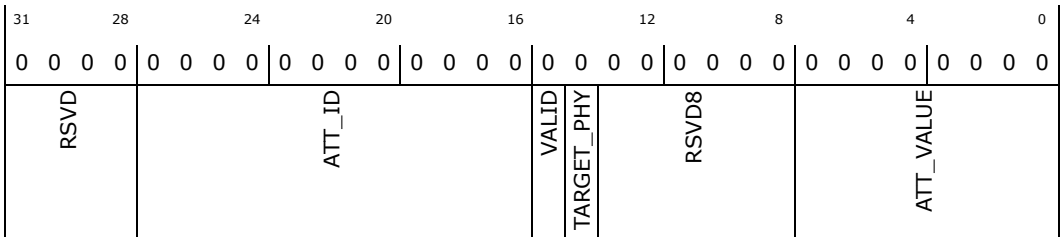
7.3.108 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG20)—Offset 895Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 895Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

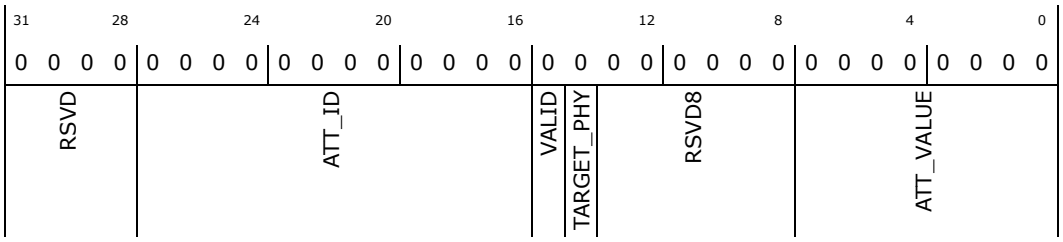
7.3.109 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG21)—Offset 8960h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8960h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

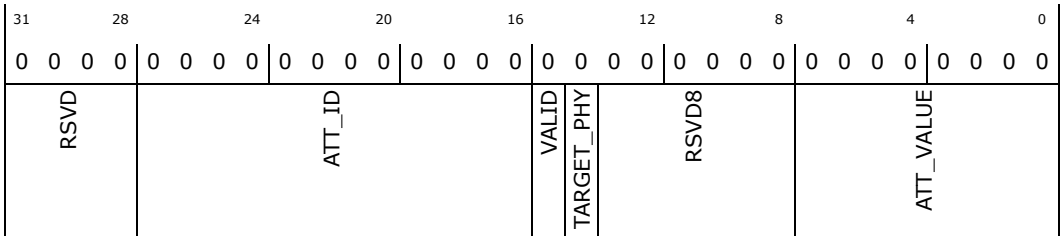
7.3.110 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG22)—Offset 8964h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8964h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

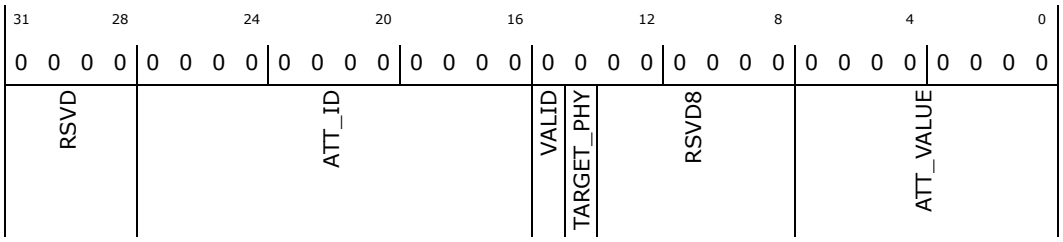
7.3.111 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG23)—Offset 8968h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8968h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

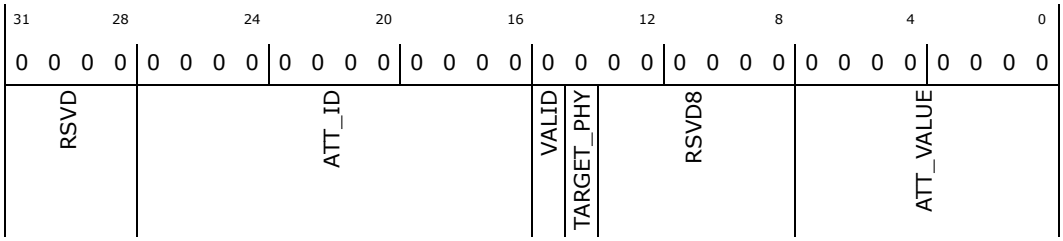
7.3.112 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG24)—Offset 896Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 896Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

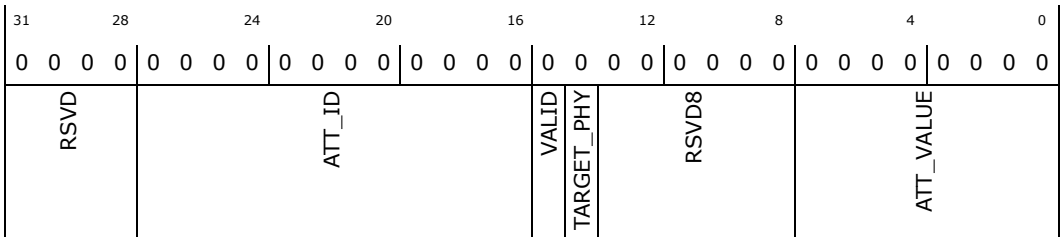
7.3.113 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG25)—Offset 8970h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8970h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

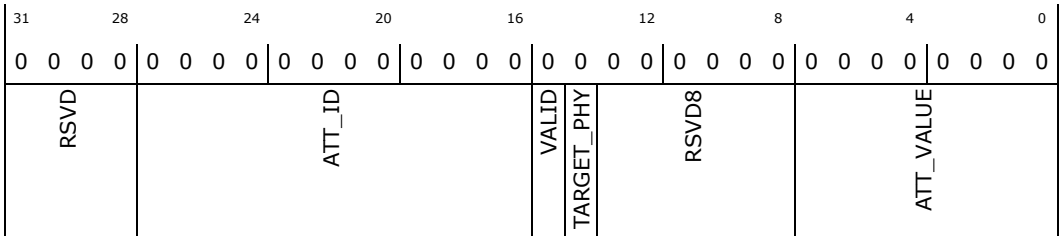
7.3.114 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG26)—Offset 8974h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8974h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

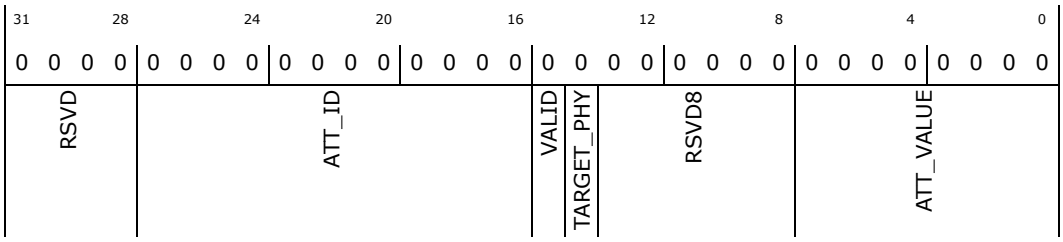
7.3.115 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG27)—Offset 8978h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8978h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

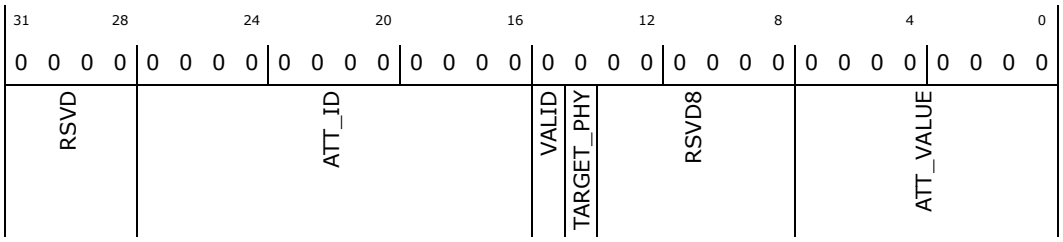
7.3.116 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG28)—Offset 897Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 897Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

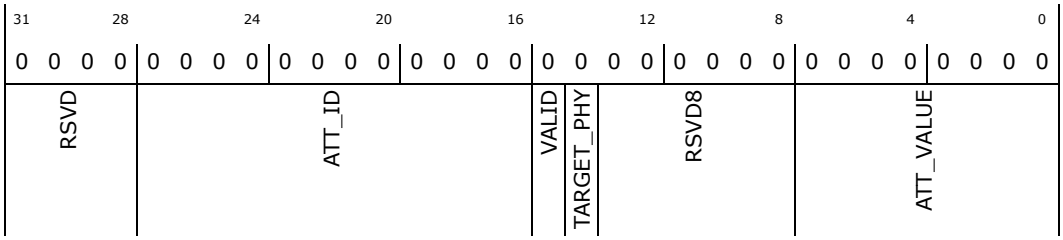
7.3.117 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG29)—Offset 8980h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8980h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

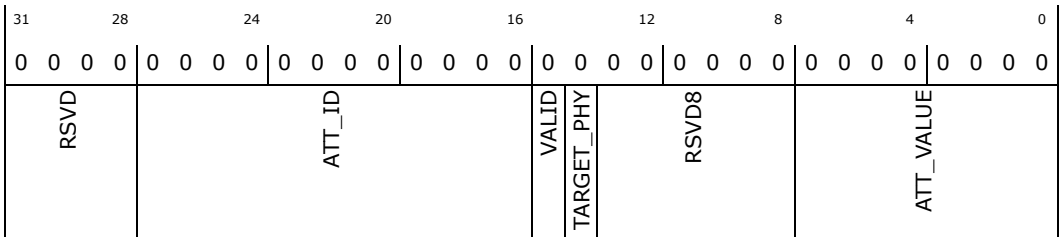
7.3.118 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG30)—Offset 8984h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8984h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

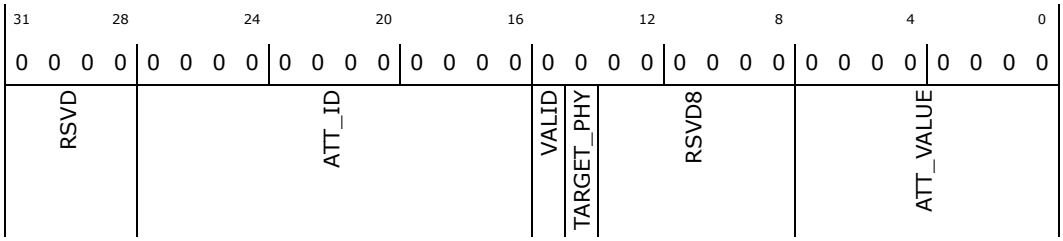
7.3.119 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG31)—Offset 8988h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8988h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

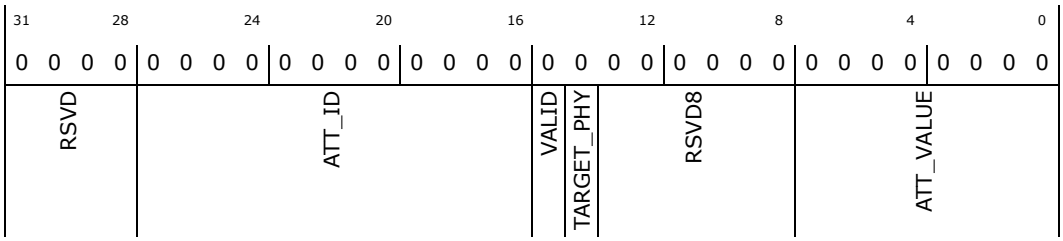
7.3.120 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG32)—Offset 898Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 898Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

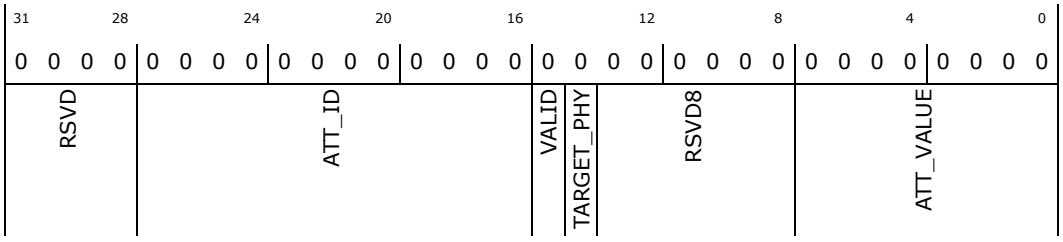
7.3.121 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG33)—Offset 8990h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8990h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

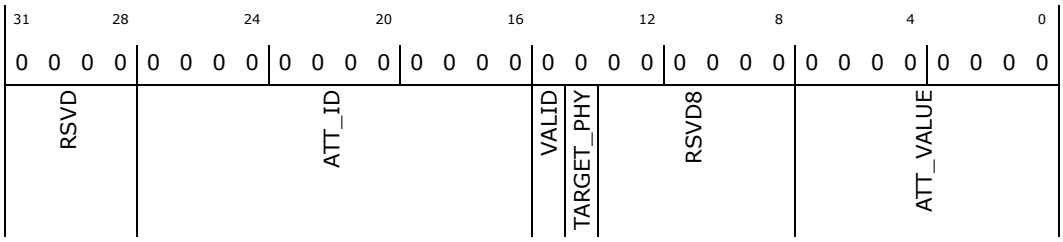
7.3.122 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG34)—Offset 8994h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8994h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

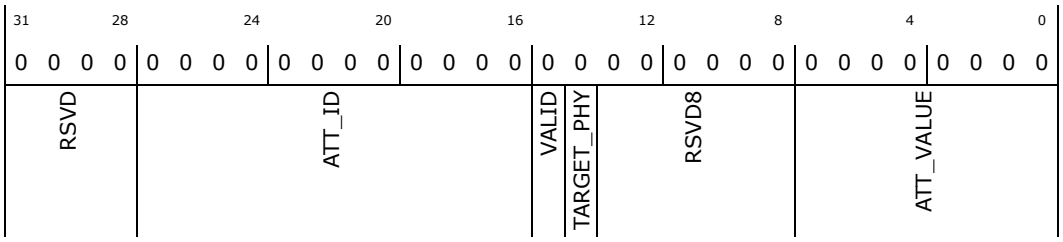
7.3.123 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG35)—Offset 8998h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8998h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

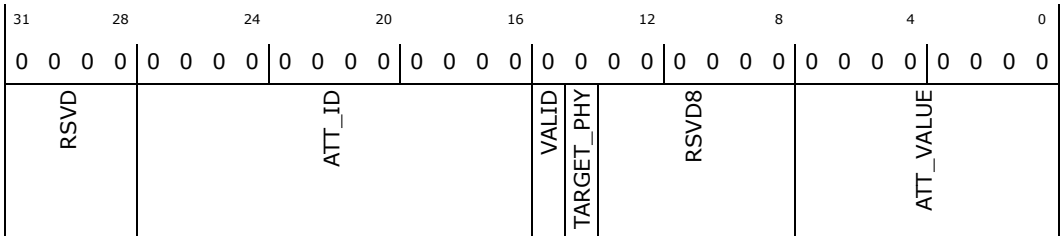
7.3.124 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG36)—Offset 899Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 899Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

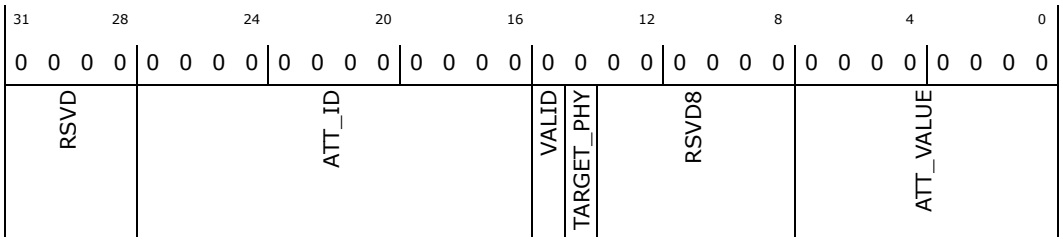
7.3.125 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG37)—Offset 89A0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

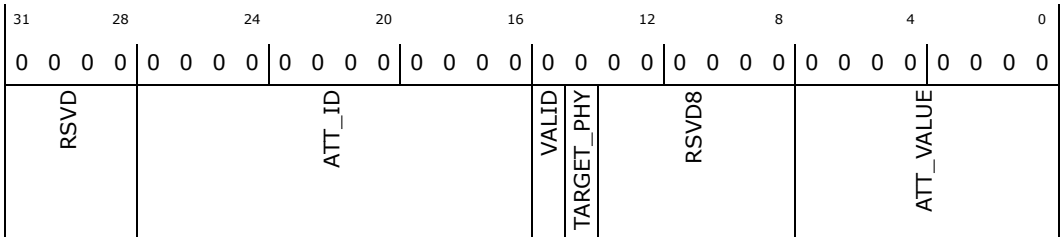
7.3.126 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG38)—Offset 89A4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

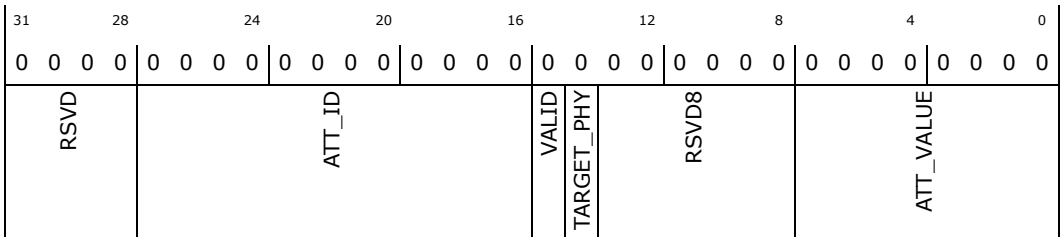
7.3.127 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG39)—Offset 89A8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

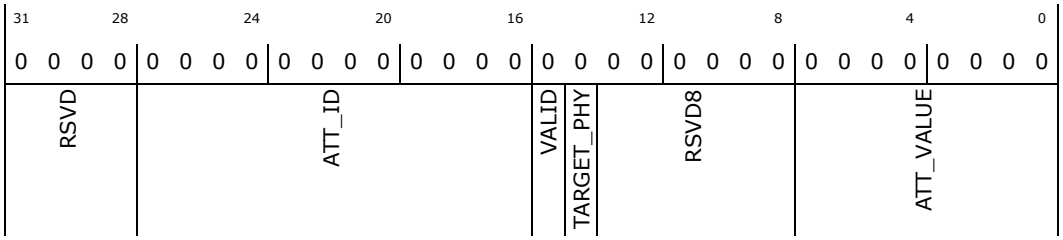
7.3.128 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG40)—Offset 89ACh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

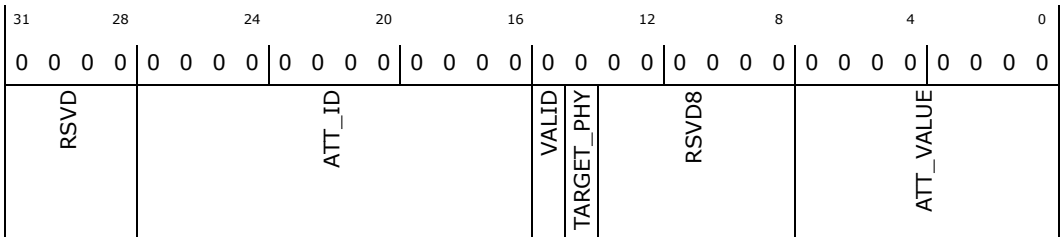
7.3.129 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG41)—Offset 89B0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

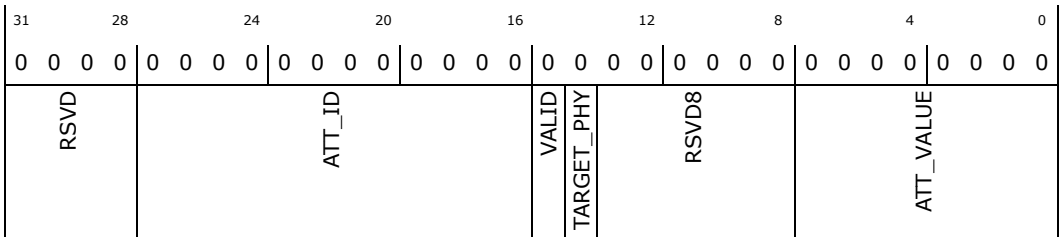
7.3.130 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG42)—Offset 89B4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89B4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

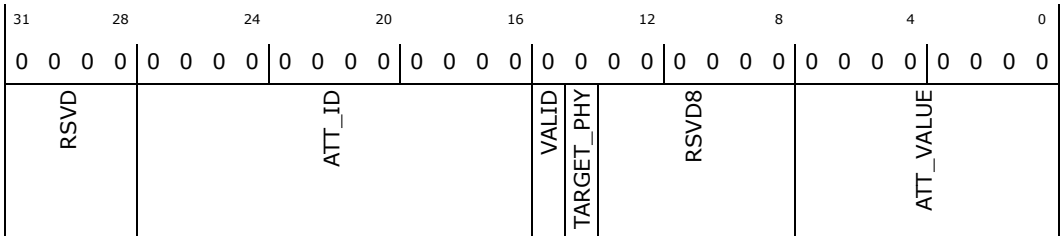
7.3.131 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG43)—Offset 89B8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

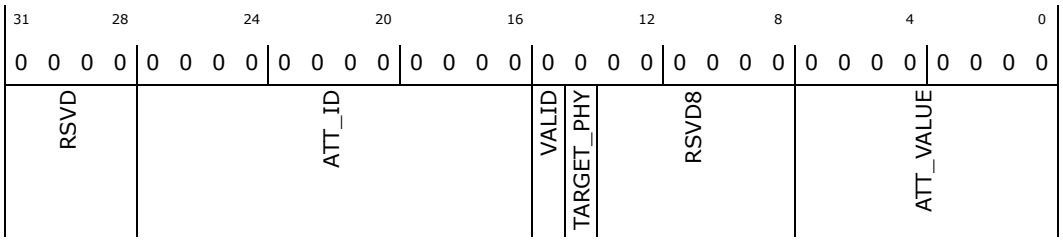
7.3.132 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG44)—Offset 89BCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89BCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

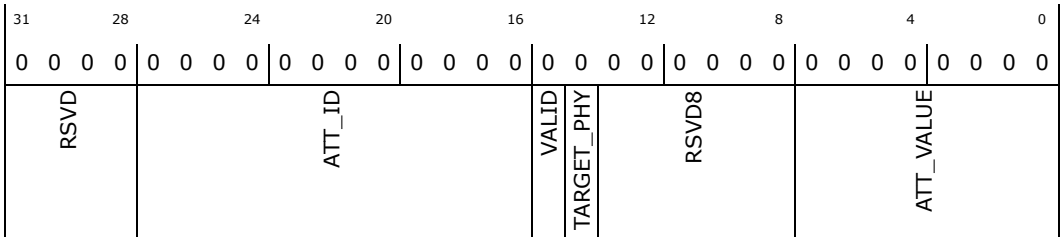
7.3.133 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG45)—Offset 89C0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

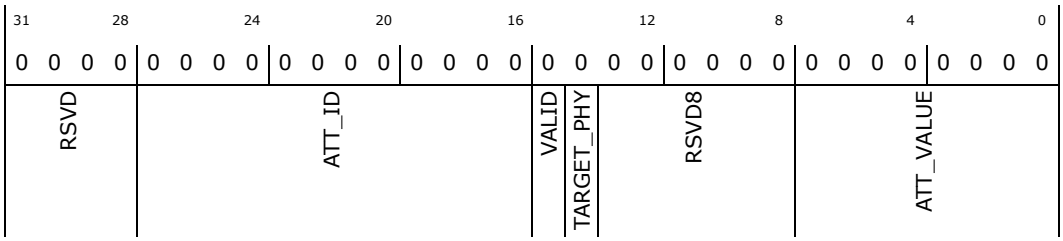
7.3.134 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG46)—Offset 89C4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89C4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

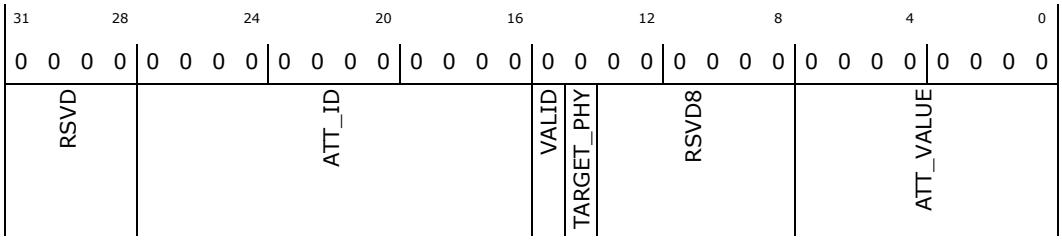
7.3.135 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG47)—Offset 89C8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89C8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

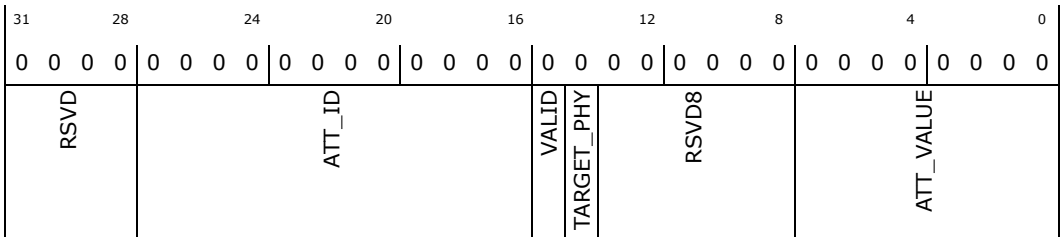
7.3.136 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG48)—Offset 89CCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89CCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

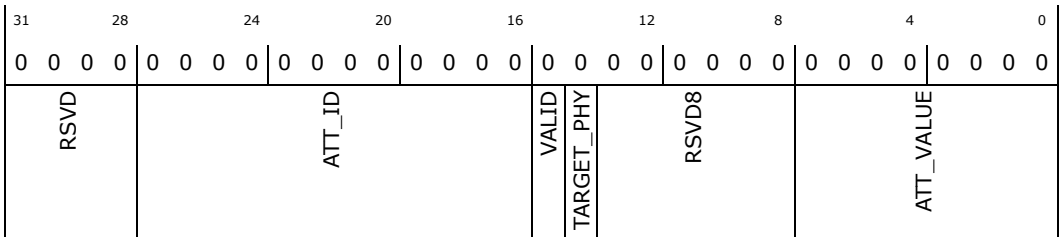
7.3.137 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG49)—Offset 89D0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

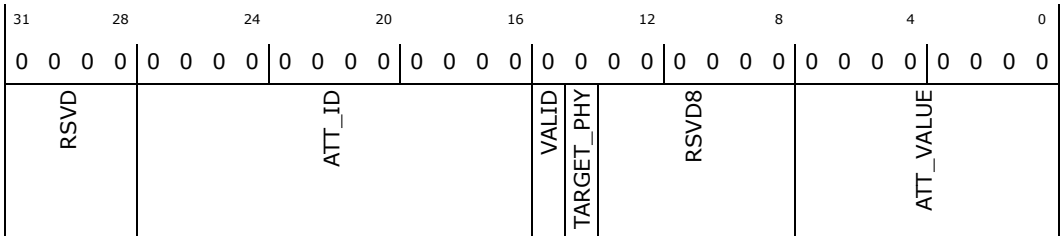
7.3.138 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG50)—Offset 89D4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89D4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

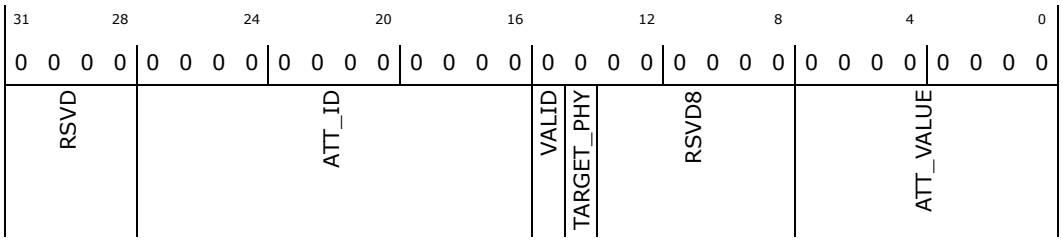
7.3.139 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG51)—Offset 89D8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89D8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

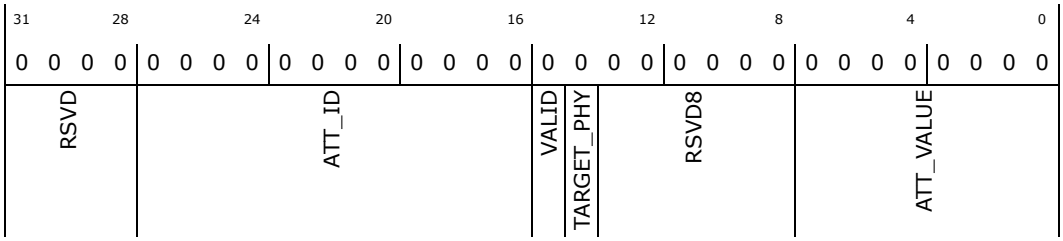
7.3.140 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG52)—Offset 89DCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89DCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

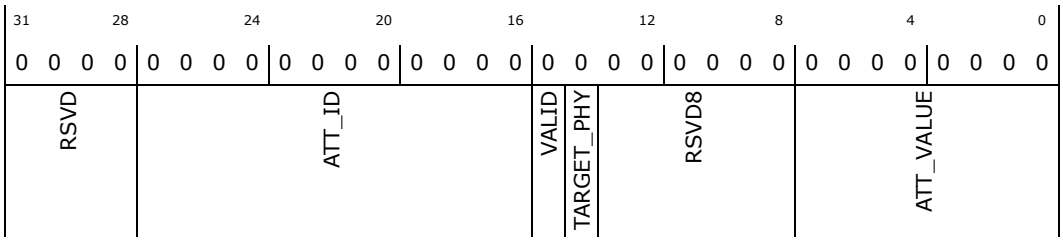
7.3.141 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG53)—Offset 89E0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89E0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

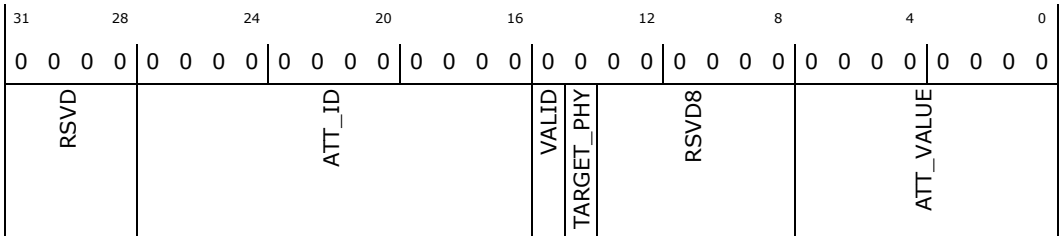
7.3.142 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG54)—Offset 89E4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89E4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

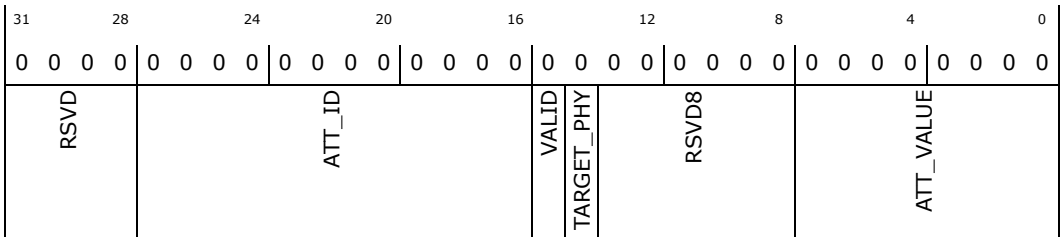
7.3.143 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG55)—Offset 89E8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89E8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

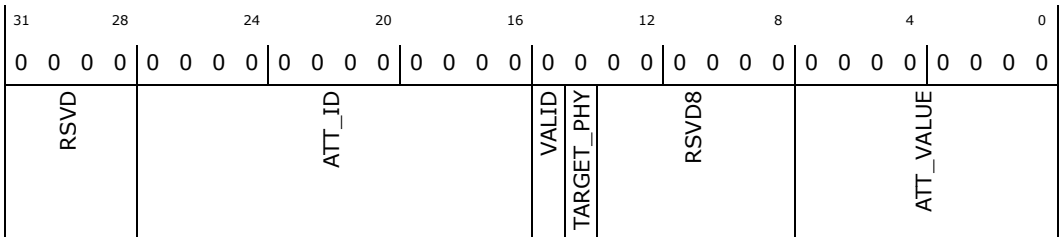
7.3.144 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG56)—Offset 89ECh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89ECh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

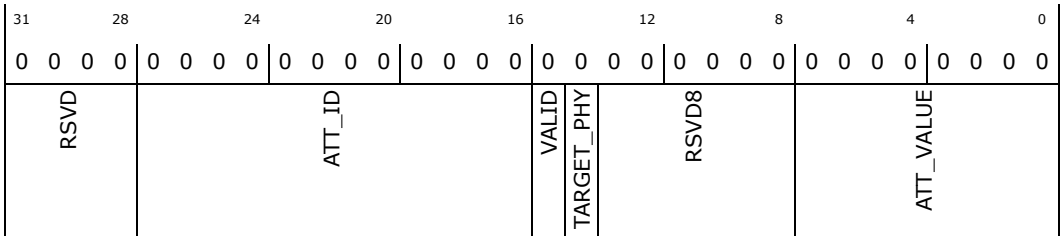
7.3.145 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG57)—Offset 89F0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89F0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

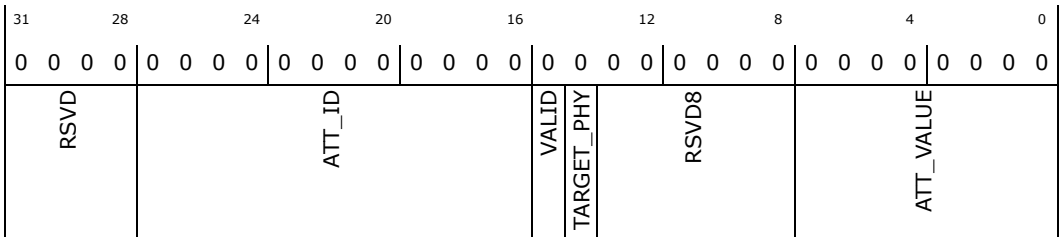
7.3.146 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG58)—Offset 89F4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89F4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

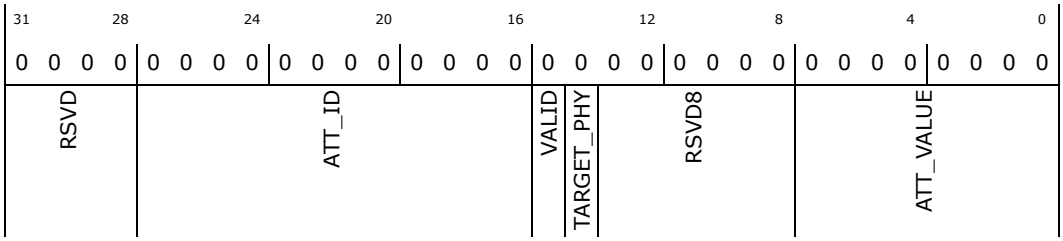
7.3.147 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG59)—Offset 89F8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

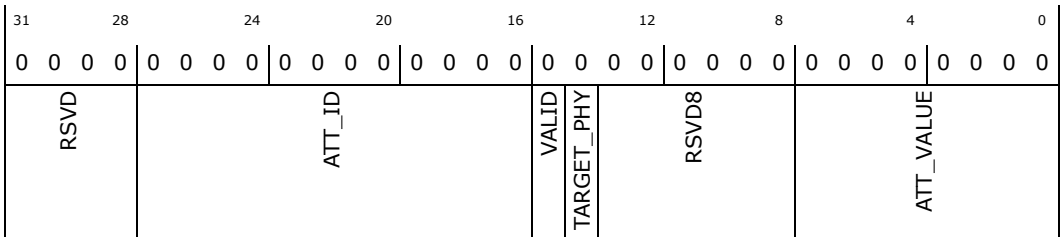
7.3.148 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG60)—Offset 89FCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 89FCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

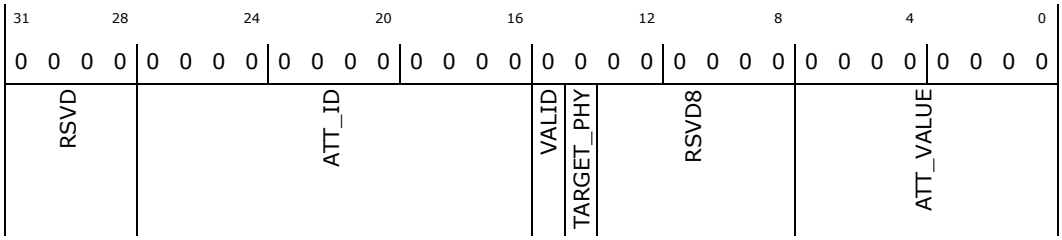
7.3.149 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG61)—Offset 8A00h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A00h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

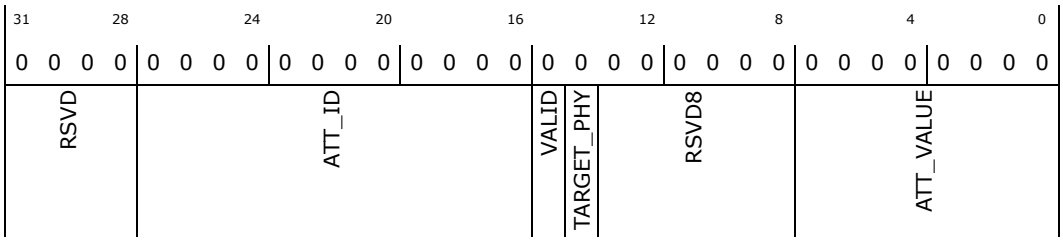
7.3.150 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG62)—Offset 8A04h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A04h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

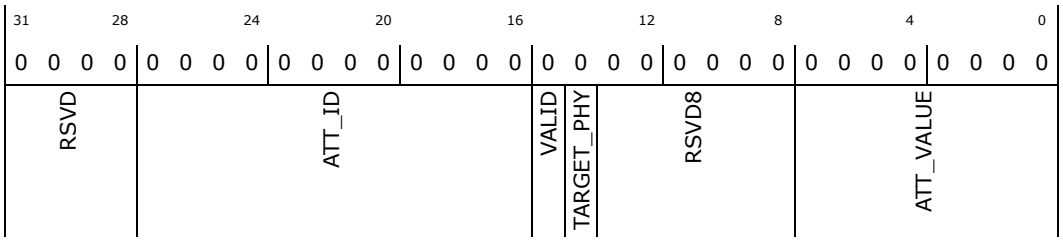
7.3.151 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG63)—Offset 8A08h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A08h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

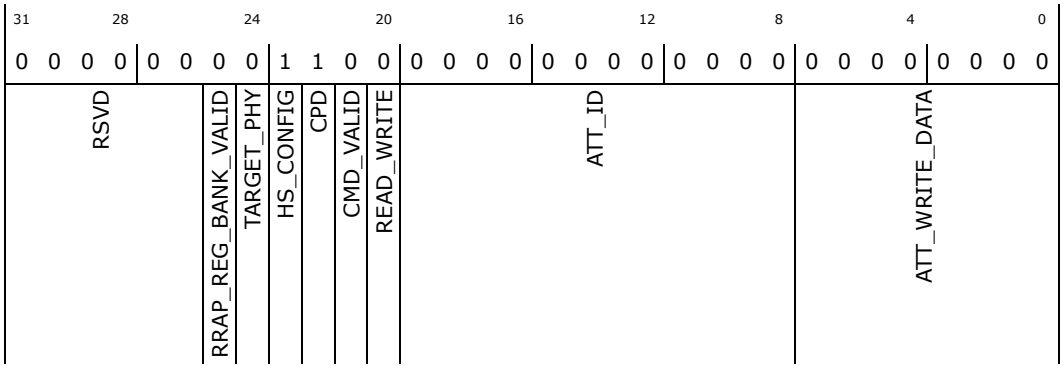
7.3.152 SSIC Port N Register Access Control (PORT2_REGISTER_ACCESS_CONTROL)—Offset 8A14h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A14h

Default: 00C00000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
25	0x0 RW	**RRAP Register Bank Valid (RRAP_REG_BANK_VALID):** 0 = No valid Commands in the Lane N register bank. Host Controller can close the PWM burst once commands from this register are completed. 1 = Valid commands present in the Lane N register bank. Host controller must complete commands from the register bank before closing the burst. **Power Well:** Core
24	0x0 RW	**Target Phy (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy Setting this bit to 1 allows the use of this command mechanism to write to local Phy profile and AFE tuning registers Primarily as a back up option. **Power Well:** Core
23	0x1 RW	**HS_Config (HS_CONFIG):** When this bit is set to 1 the host controller will issue an RRAP write with HS_Config=1 once it sees Command Phase Done = 1 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
22	0x1 RW	**Command Phase Done (CPD):** When set to 1, this indicates that SW has completed performing RRAP cycles through the command register. **Power Well:** Core
21	0x0 RW	**Command Valid (CMD_VALID):** When written to 1 indicates that the Attribute ID and Attribute Data for writes fields are valid. **Power Well:** Core
20	0x0 RW	**Read_Write (READ_WRITE):** 0 = Write 1= Read **Power Well:** Core
19:8	0x0 RW	**Attribute ID (ATT_ID):** Attribute ID that is being written or read **Power Well:** Core
7:0	0x0 RW	**Attribute Write Data (ATT_WRITE_DATA):** Data byte that is required to be written to either the local phy or the remote phy **Power Well:** Core

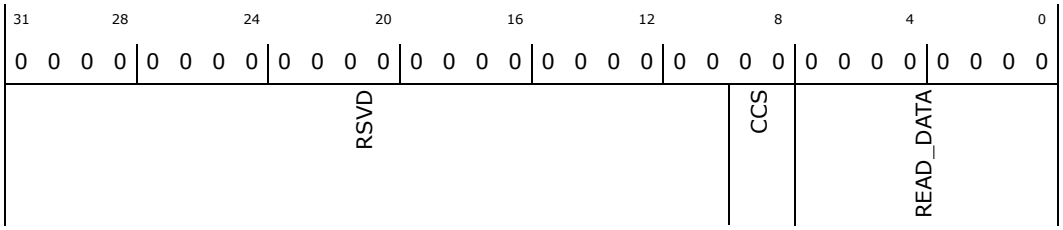
7.3.153 SSIC Port N Register Access Status (PORT2_REGISTER_ACCESS_STATUS)—Offset 8A18h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A18h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
9:8	0x0 RW	**Command Completion Status (CCS):** 00 = Command not complete 01 = Command complete with Success 10 = Command complete with Error These bits must be cleared before a new command is initiated. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**Read data (READ_DATA):** Data read as a result of the RRAP operation **Power Well:** Core

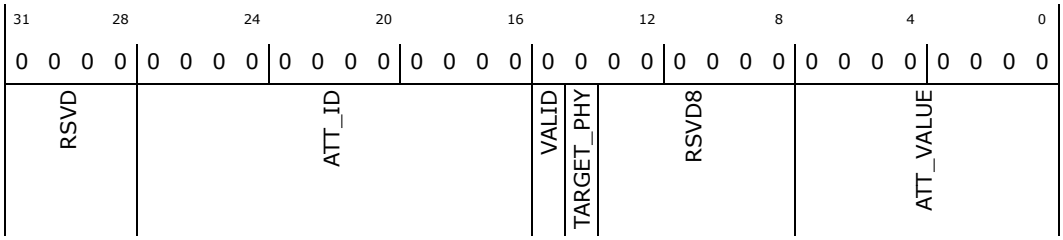
7.3.154 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG0)—Offset 8A1Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A1Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

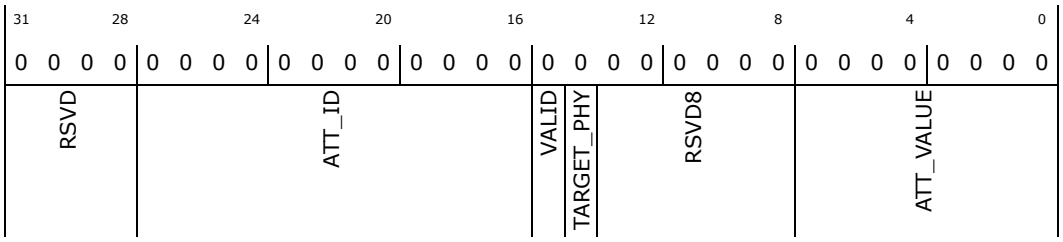
7.3.155 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG1)—Offset 8A20h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A20h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

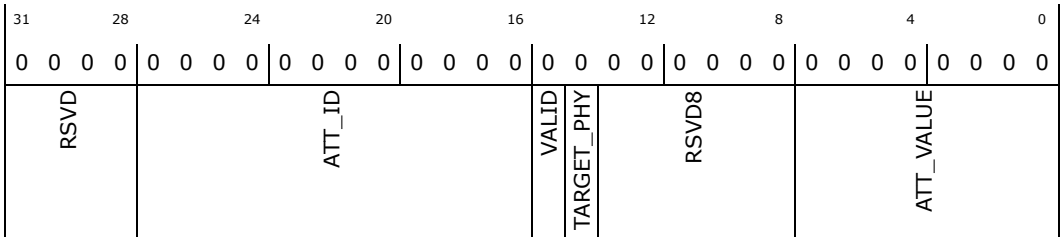
7.3.156 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG2)—Offset 8A24h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A24h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

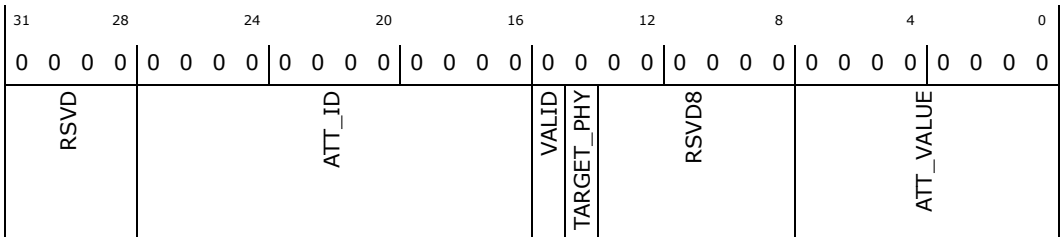
7.3.157 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG3)—Offset 8A28h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A28h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

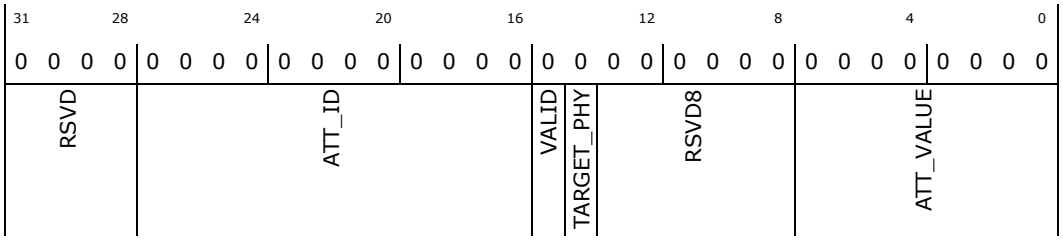
7.3.158 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG4)—Offset 8A2Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

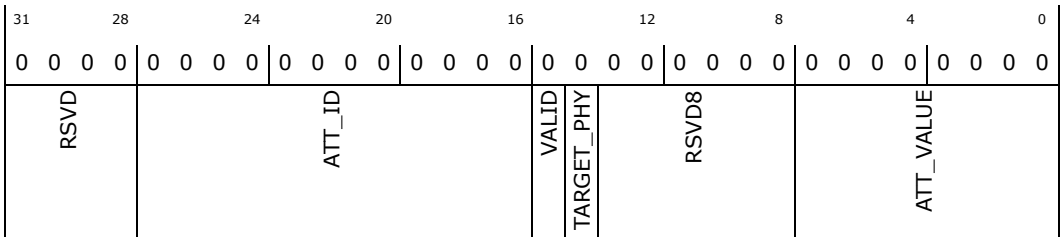
7.3.159 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG5)—Offset 8A30h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

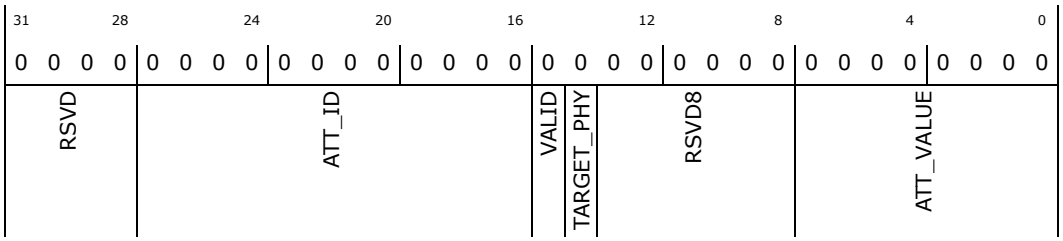
7.3.160 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG6)—Offset 8A34h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

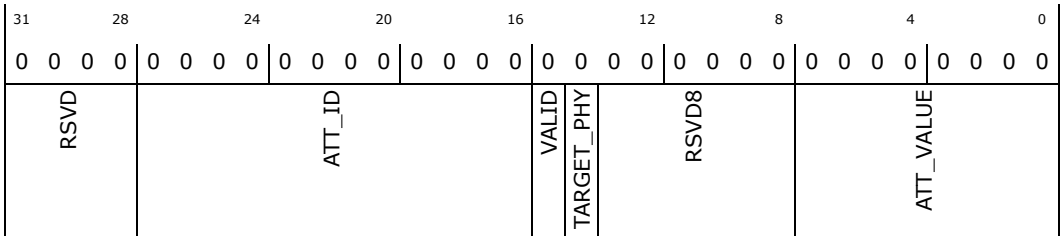
7.3.161 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG7)—Offset 8A38h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A38h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

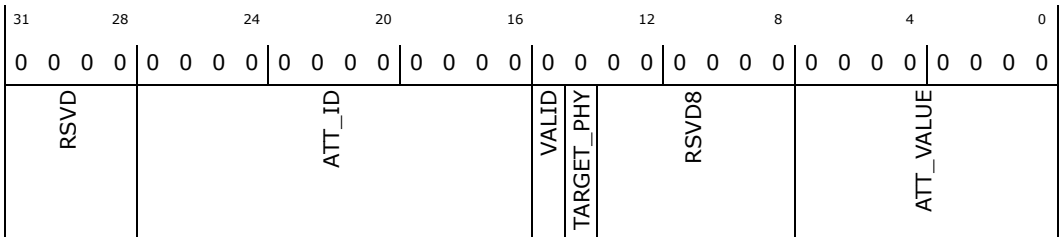
7.3.162 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG8)—Offset 8A3Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A3Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

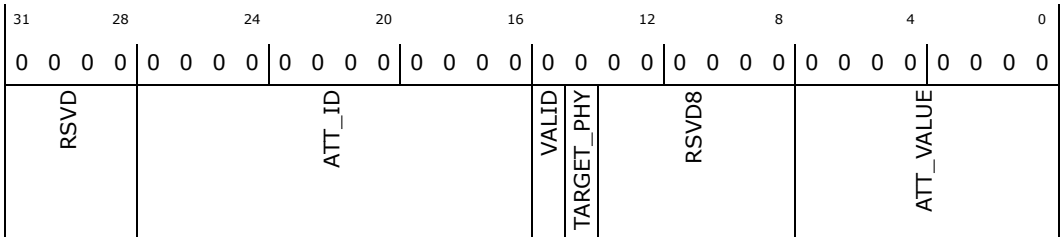
7.3.163 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG9)—Offset 8A40h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A40h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

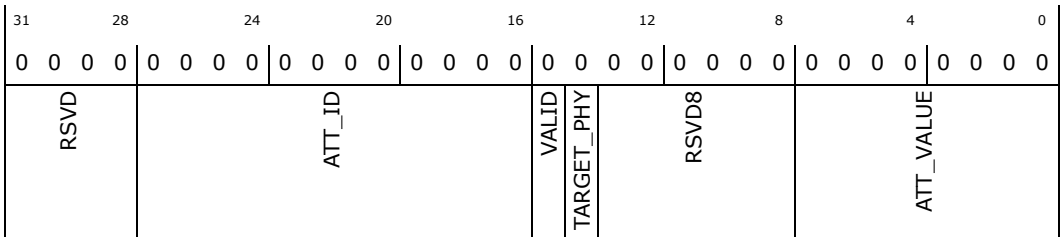
7.3.164 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG10)—Offset 8A44h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A44h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

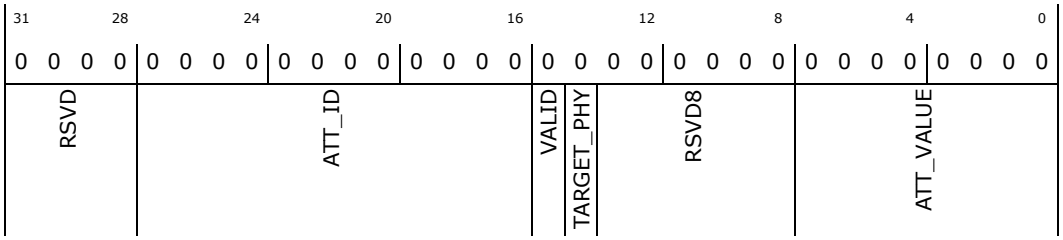
7.3.165 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG11)—Offset 8A48h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A48h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

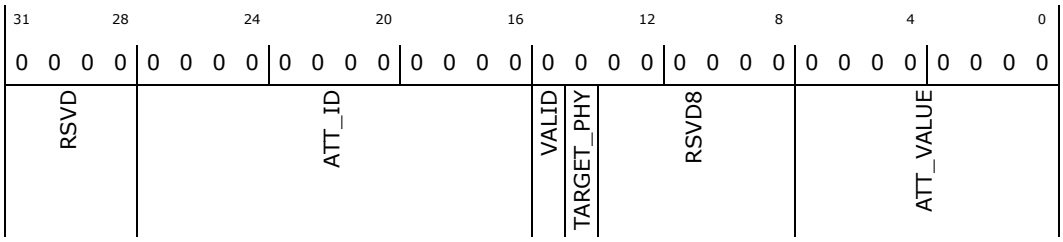
7.3.166 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG12)—Offset 8A4Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A4Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

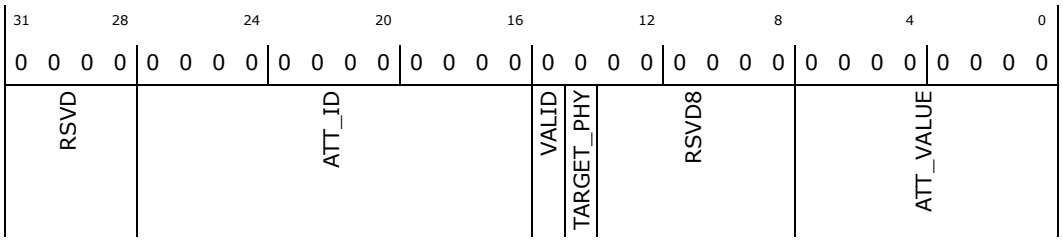
7.3.167 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG13)—Offset 8A50h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A50h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

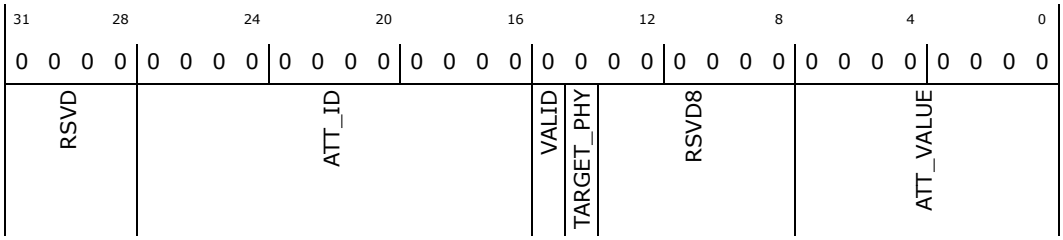
7.3.168 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG14)—Offset 8A54h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A54h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

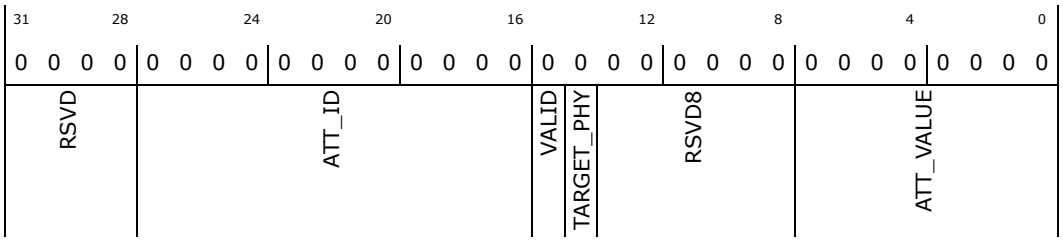
7.3.169 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG15)—Offset 8A58h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A58h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

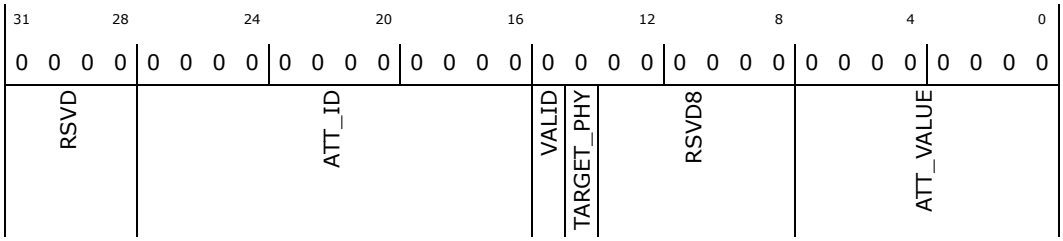
7.3.170 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG16)—Offset 8A5Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A5Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

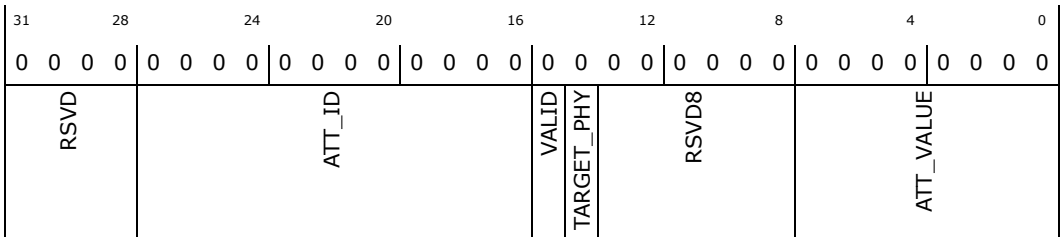
7.3.171 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG17)—Offset 8A60h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A60h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

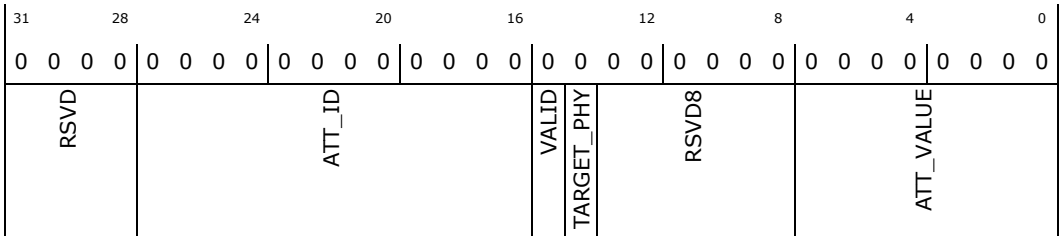
7.3.172 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG18)—Offset 8A64h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A64h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

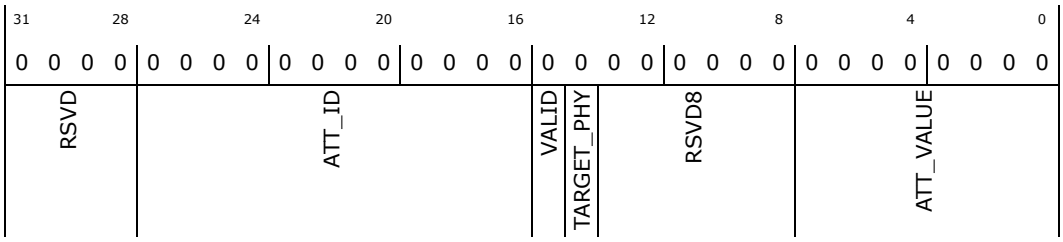
7.3.173 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG19)—Offset 8A68h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A68h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

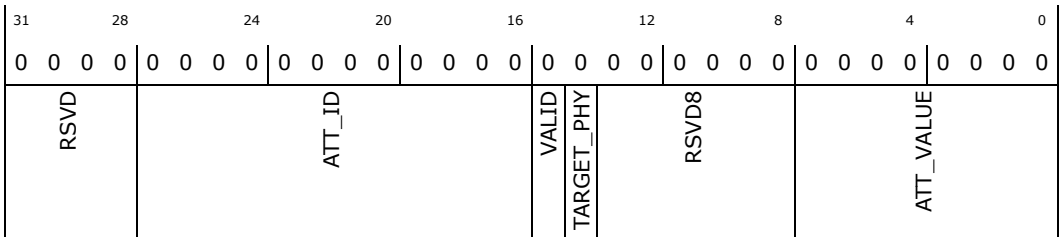
7.3.174 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG20)—Offset 8A6Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A6Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

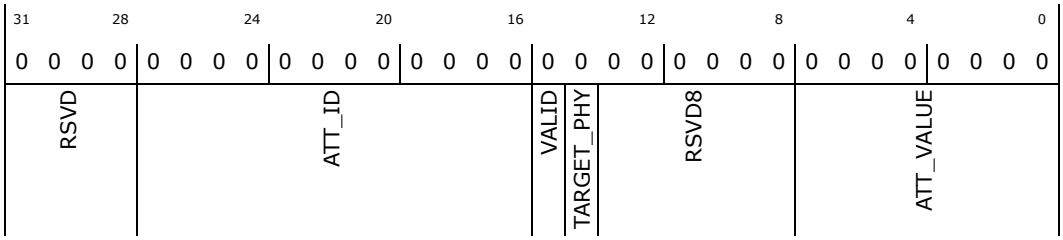
7.3.175 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG21)—Offset 8A70h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A70h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

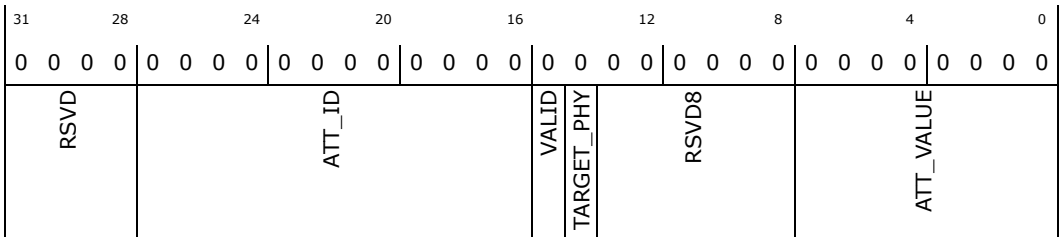
7.3.176 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG22)—Offset 8A74h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A74h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

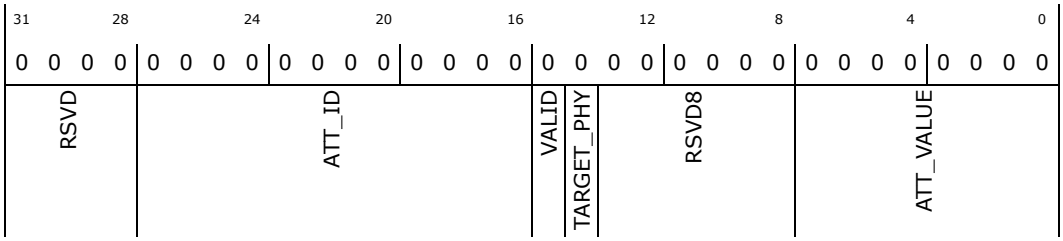
7.3.177 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG23)—Offset 8A78h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A78h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

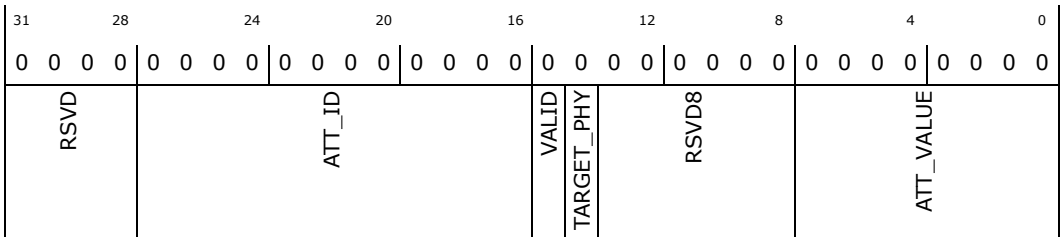
7.3.178 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG24)—Offset 8A7Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A7Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

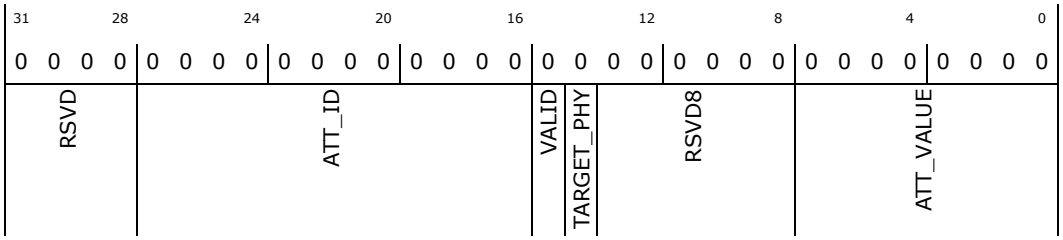
7.3.179 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG25)—Offset 8A80h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A80h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

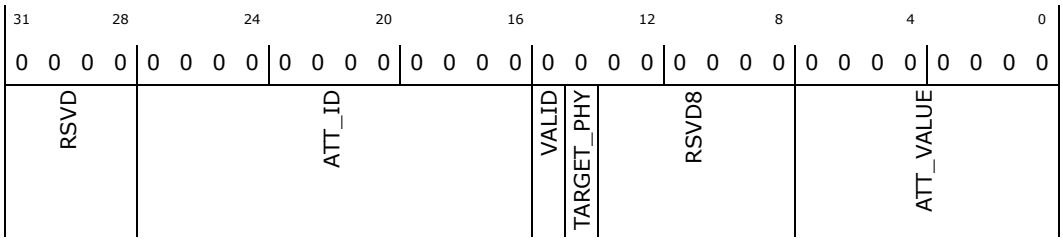
7.3.180 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG26)—Offset 8A84h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A84h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

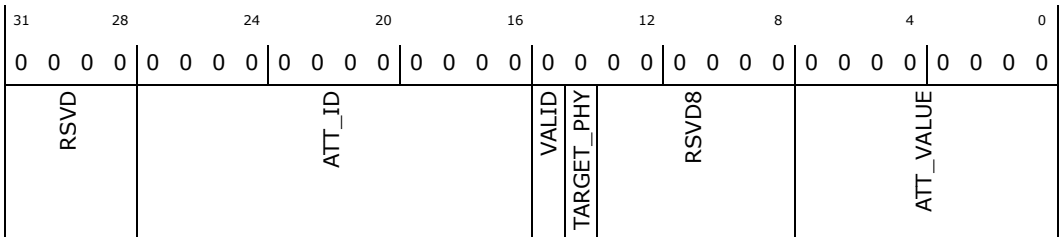
7.3.181 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG27)—Offset 8A88h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A88h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

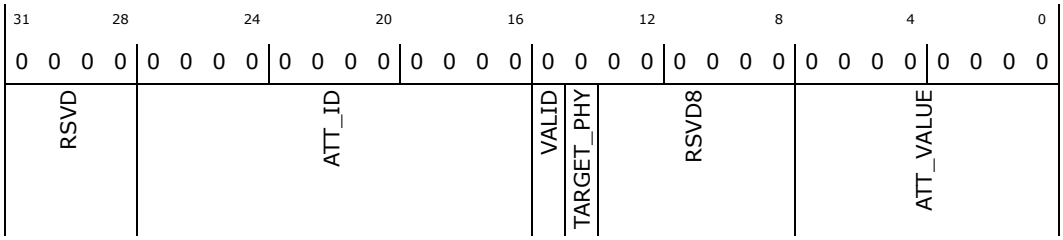
7.3.182 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG28)—Offset 8A8Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A8Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

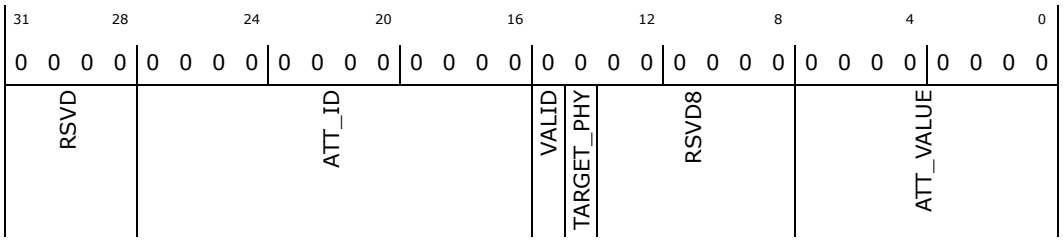
7.3.183 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG29)—Offset 8A90h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A90h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

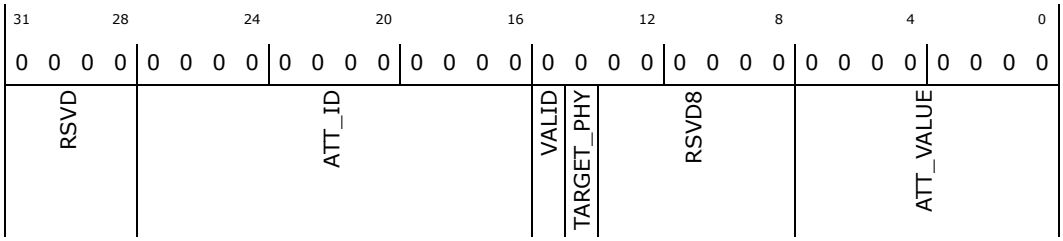
7.3.184 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG30)—Offset 8A94h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A94h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

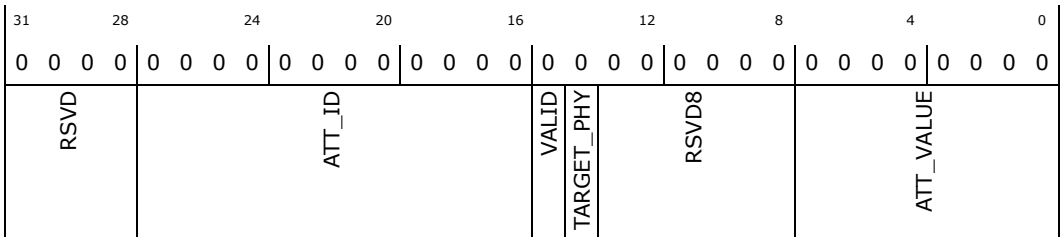
7.3.185 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG31)—Offset 8A98h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A98h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

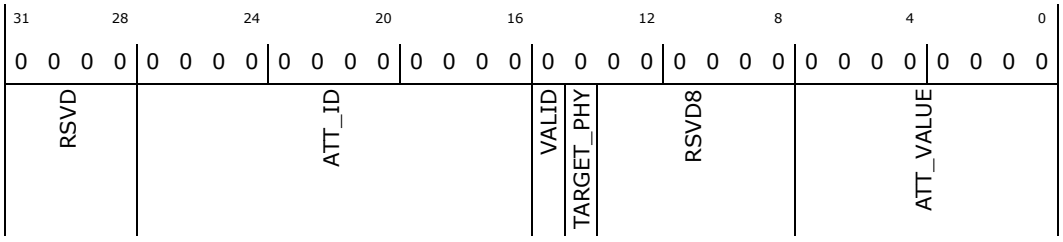
7.3.186 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG32)—Offset 8A9Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8A9Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

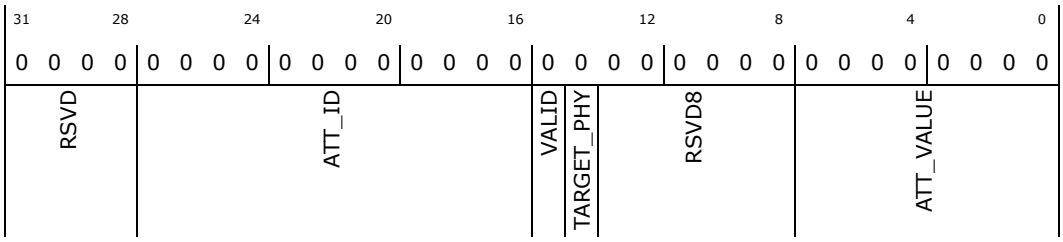
7.3.187 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG33)—Offset 8AA0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AA0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

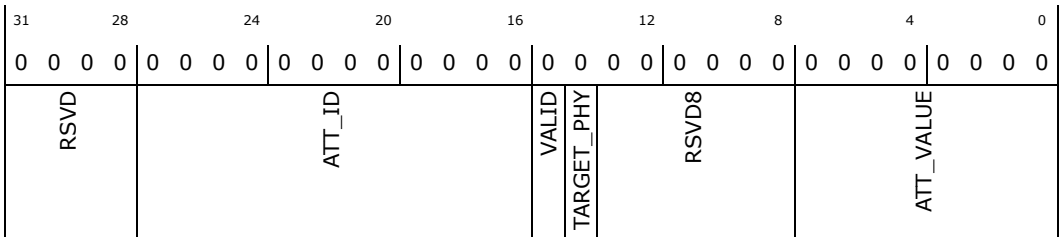
7.3.188 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG34)—Offset 8AA4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AA4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

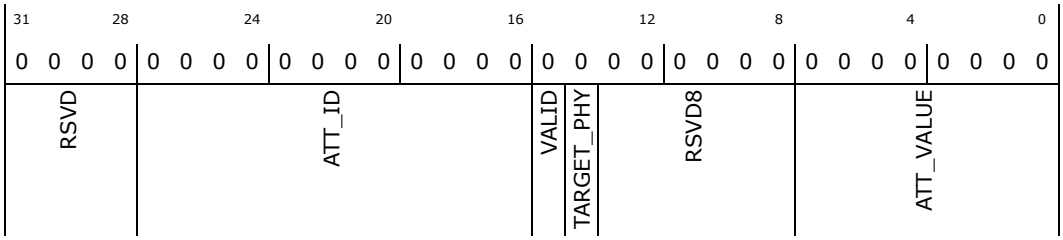
7.3.189 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG35)—Offset 8AA8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AA8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

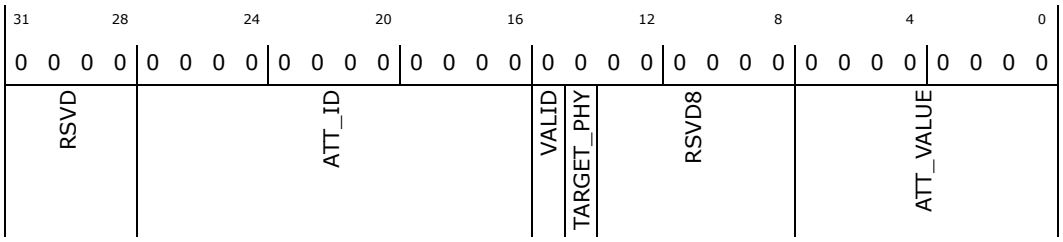
7.3.190 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG36)—Offset 8AACh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

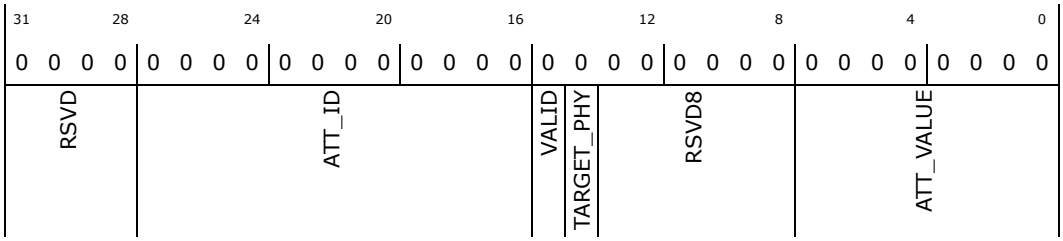
7.3.191 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG37)—Offset 8AB0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AB0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

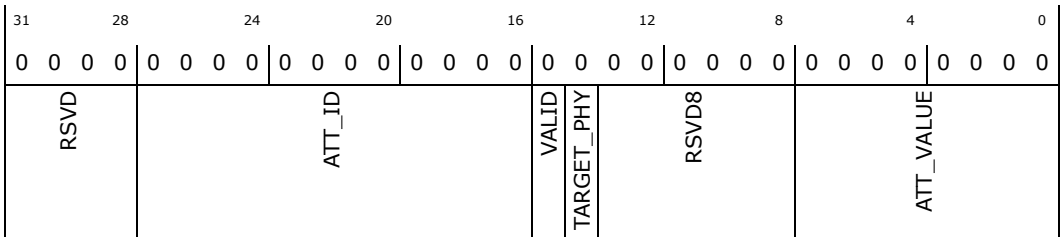
7.3.192 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG38)—Offset 8AB4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AB4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

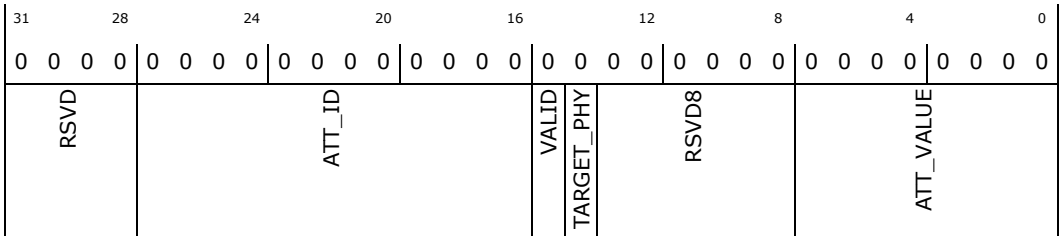
7.3.193 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG39)—Offset 8AB8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AB8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

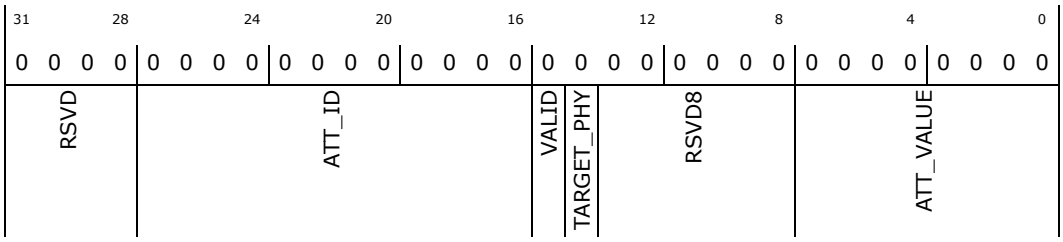
7.3.194 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG40)—Offset 8ABCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8ABCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

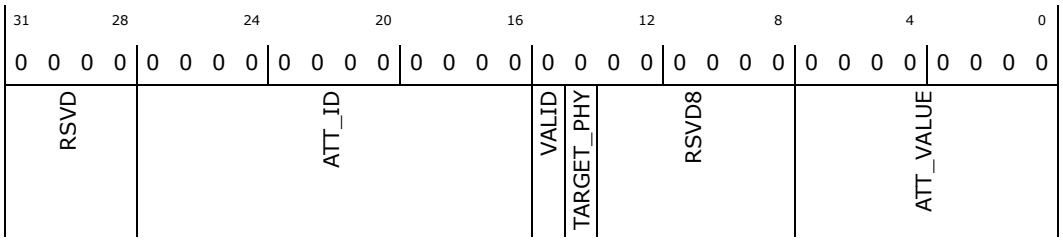
7.3.195 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG41)—Offset 8AC0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AC0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

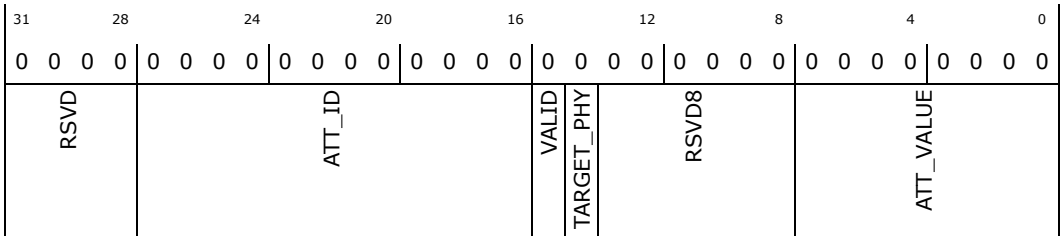
7.3.196 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG42)—Offset 8AC4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AC4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

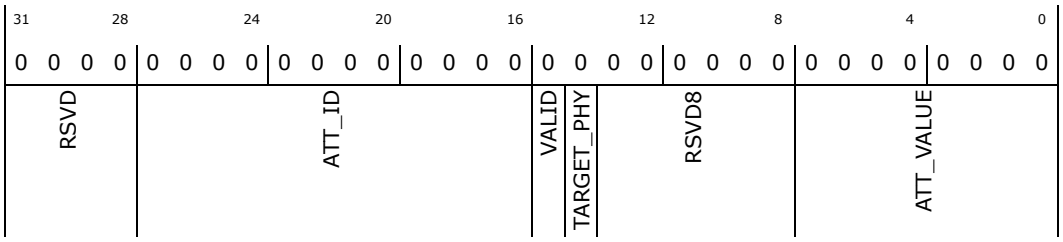
7.3.197 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG43)—Offset 8AC8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AC8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

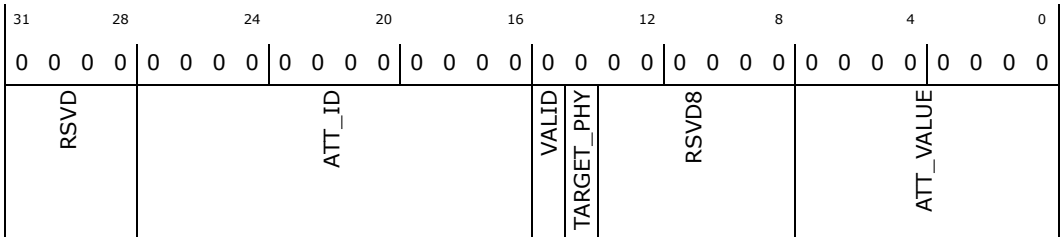
7.3.198 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG44)—Offset 8ACCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8ACCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

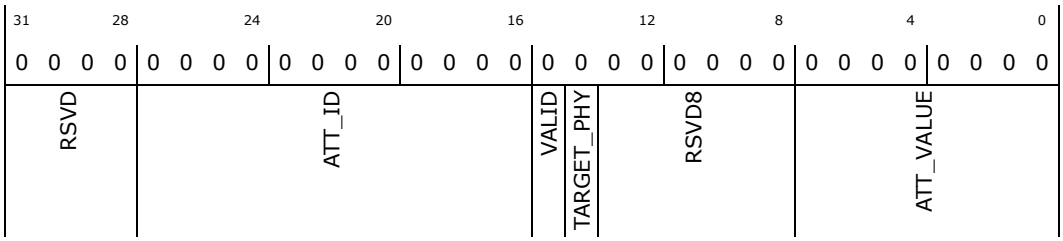
7.3.199 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG45)—Offset 8AD0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AD0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

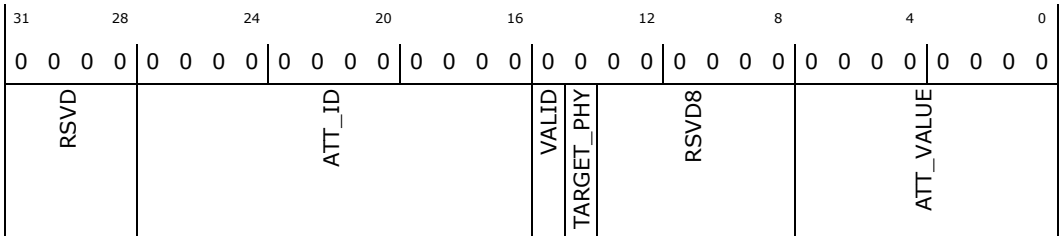
7.3.200 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG46)—Offset 8AD4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AD4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

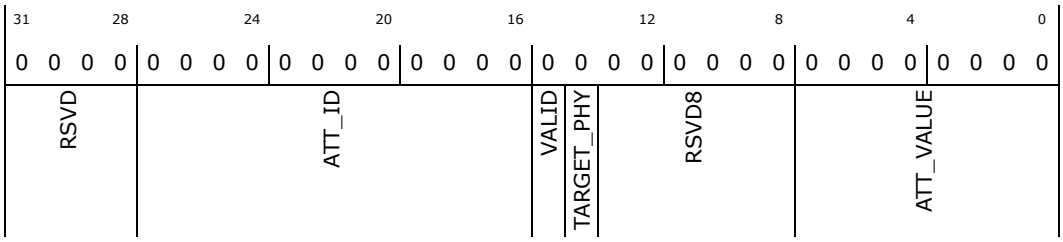
7.3.201 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG47)—Offset 8AD8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AD8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

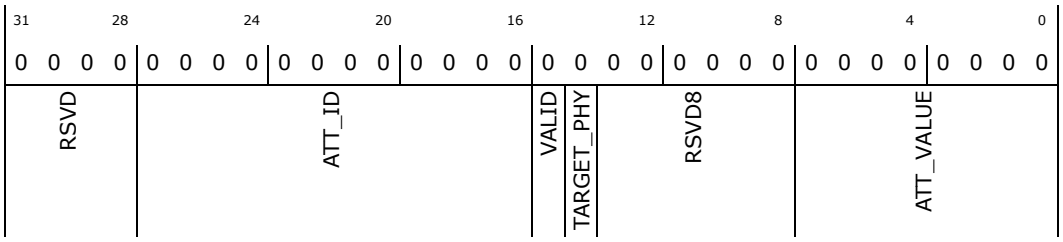
7.3.202 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG48)—Offset 8ADCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8ADCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

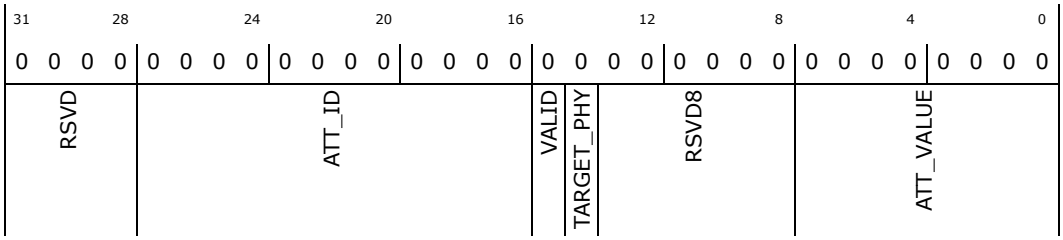
7.3.203 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG49)—Offset 8AE0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AE0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

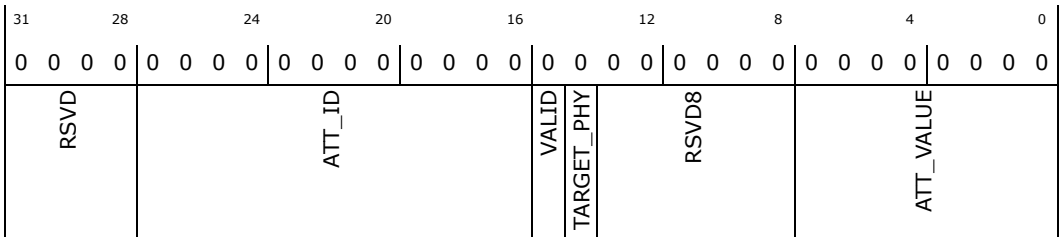
7.3.204 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG50)—Offset 8AE4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AE4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

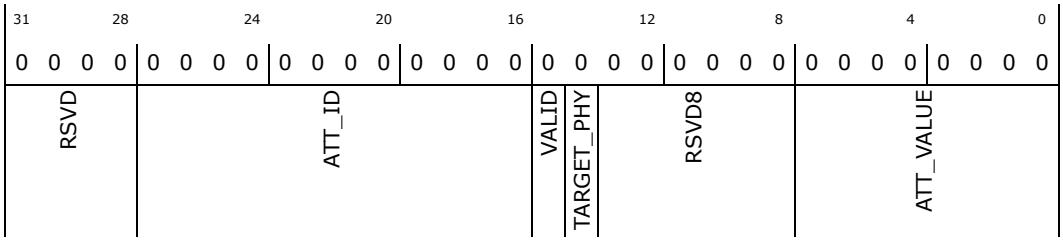
7.3.205 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG51)—Offset 8AE8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AE8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

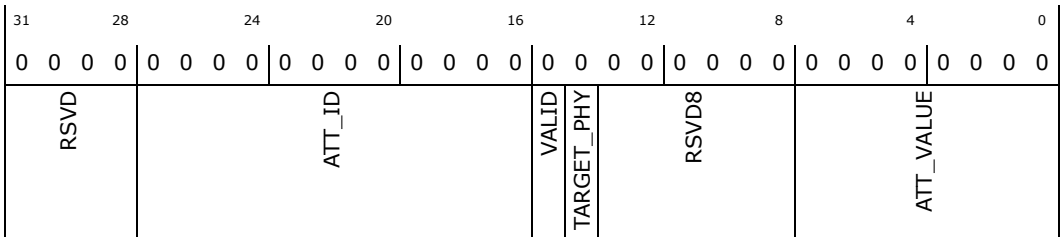
7.3.206 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG52)—Offset 8AECh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AECh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

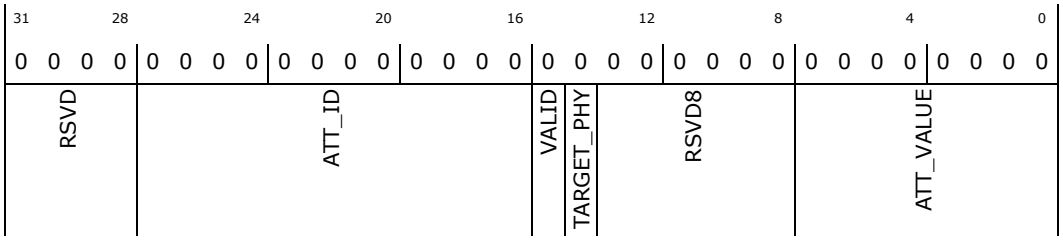
7.3.207 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG53)—Offset 8AF0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AF0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

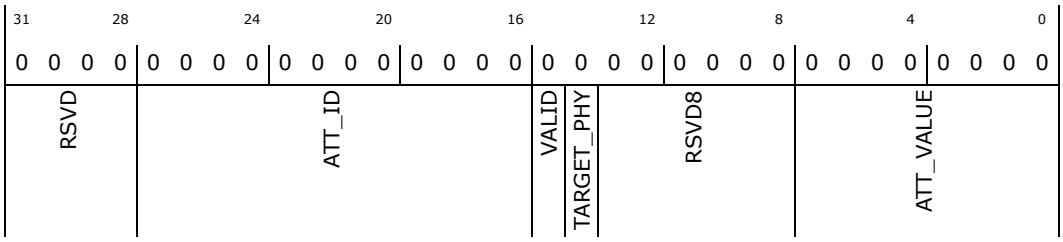
7.3.208 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG54)—Offset 8AF4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AF4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

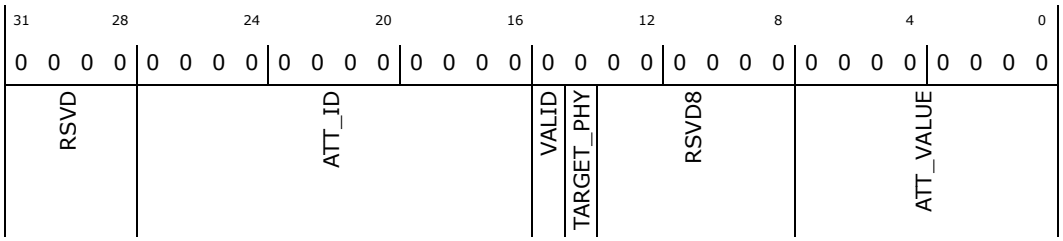
7.3.209 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG55)—Offset 8AF8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AF8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

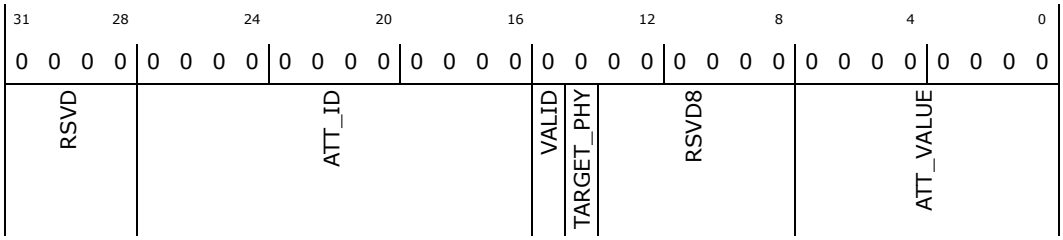
7.3.210 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG56)—Offset 8AFCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8AFCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

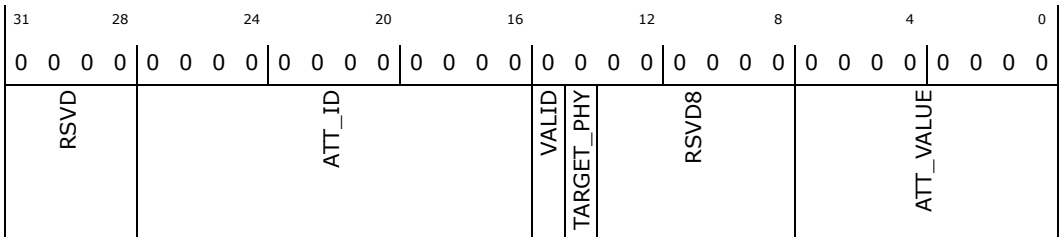
7.3.211 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG57)—Offset 8B00h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8B00h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

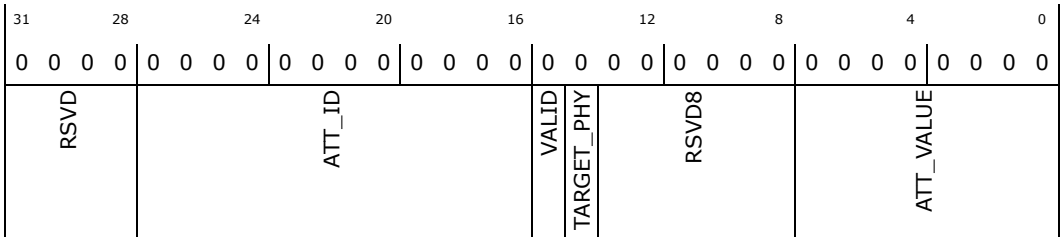
7.3.212 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG58)—Offset 8B04h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8B04h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

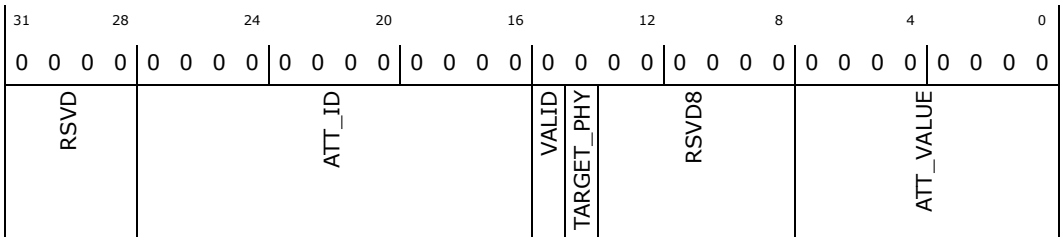
7.3.213 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG59)—Offset 8B08h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8B08h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

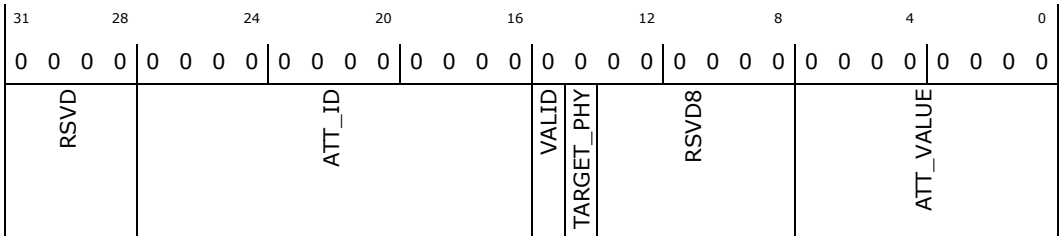
7.3.214 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG60)—Offset 8B0Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8B0Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

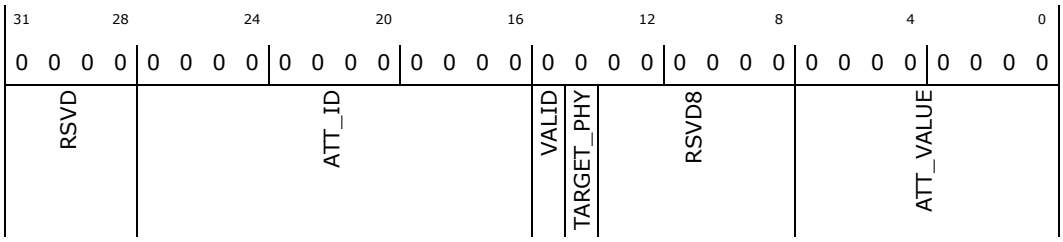
7.3.215 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG61)—Offset 8B10h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8B10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

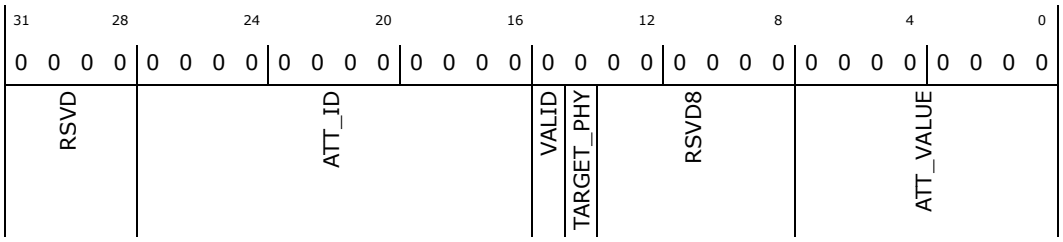
7.3.216 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG62)—Offset 8B14h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8B14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

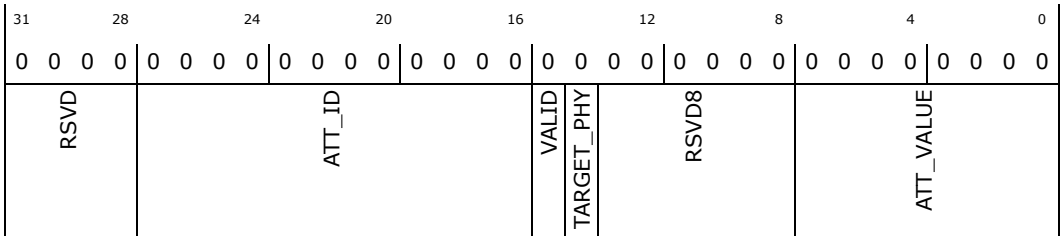
7.3.217 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG63)—Offset 8B18h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [MBAR] + 8B18h

Default: 00000000h

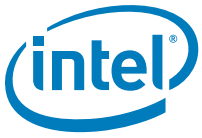


Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4 USB xHCI Memory Mapped I/O Registers Address Map

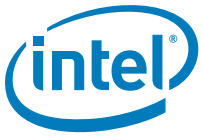
Table 40. Summary of Message Bus Registers—0x5A

Offset	Register Name (Register Symbol)	Default Value
0–1h	"Capability Registers Length (CAPLENGTH)—Offset 0h" on page 2504	80h
2–3h	"Host Controller Interface Version Number (HCIVERSION)—Offset 2h" on page 2504	0100h
4–7h	"Structural Parameters 1 (HCSPARAMS1)—Offset 4h" on page 2505	0D000820h
8–Bh	"Structural Parameters 2 (HCSPARAMS2)—Offset 8h" on page 2505	94000054h
C–Fh	"Structural Parameters 3 (HCSPARAMS3)—Offset Ch" on page 2506	00040001h
10–13h	"Capability Parameters (HCCPARAMS)—Offset 10h" on page 2507	200077C1h
14–17h	"Doorbell Offset (DBOFF)—Offset 14h" on page 2508	00003000h
18–1Bh	"Runtime Register Space Offset (RTSOFF)—Offset 18h" on page 2509	00002000h
80–83h	"USB Command (USBCMD)—Offset 80h" on page 2509	00000000h
84–87h	"USB Status (USBSTS)—Offset 84h" on page 2511	00000001h
88–8Bh	"Page Size (PAGESIZE)—Offset 88h" on page 2512	00000001h
94–97h	"Device Notification Control (DNCTRL)—Offset 94h" on page 2512	00000000h
98–9Bh	"Command Ring Low (CRCR_LO)—Offset 98h" on page 2513	00000000h
9C–9Fh	"Command Ring High (CRCR_HI)—Offset 9Ch" on page 2514	00000000h
B0–B3h	"Device Context Base Address Array Pointer Low (DCBAAP_LO)—Offset B0h" on page 2514	00000000h
B4–B7h	"Device Context Base Address Array Pointer High (DCBAAP_HI)—Offset B4h" on page 2515	00000000h
B8–BBh	"Configure (CONFIG)—Offset B8h" on page 2515	00000000h
480–483h	"Port Status and Control USB2 (PORTSC1)—Offset 480h" on page 2516	000002A0h
484–487h	"Port Power Management Status and Control USB2 (PORTPMSC1)—Offset 484h" on page 2518	00000000h
48C–48Fh	"Port X Hardware LPM Control Register (PORTHLPMC1)—Offset 48Ch" on page 2519	00000000h
490–493h	"Port Status and Control USB2 (PORTSC2)—Offset 490h" on page 2520	000002A0h
494–497h	"Port Power Management Status and Control USB2 (PORTPMSC2)—Offset 494h" on page 2522	00000000h
49C–49Fh	"Port X Hardware LPM Control Register (PORTHLPMC2)—Offset 49Ch" on page 2523	00000000h
4A0–4A3h	"Port Status and Control USB2 (PORTSC3)—Offset 4A0h" on page 2524	000002A0h
4A4–4A7h	"Port Power Management Status and Control USB2 (PORTPMSC3)—Offset 4A4h" on page 2526	00000000h
4AC–4AFh	"Port X Hardware LPM Control Register (PORTHLPMC3)—Offset 4ACh" on page 2527	00000000h



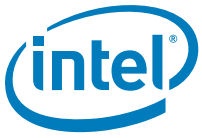
Offset	Register Name (Register Symbol)	Default Value
4B0–4B3h	"Port Status and Control USB2 (PORTSC4)—Offset 4B0h" on page 2528	000002A0h
4B4–4B7h	"Port Power Management Status and Control USB2 (PORTPMSC4)—Offset 4B4h" on page 2530	00000000h
4BC–4BFh	"Port X Hardware LPM Control Register (PORTHLPMC4)—Offset 4BCh" on page 2531	00000000h
4C0–4C3h	"Port Status and Control USB2 (PORTSC5)—Offset 4C0h" on page 2532	000002A0h
4C4–4C7h	"Port Power Management Status and Control USB2 (PORTPMSC5)—Offset 4C4h" on page 2534	00000000h
4CC–4CFh	"Port X Hardware LPM Control Register (PORTHLPMC5)—Offset 4CCh" on page 2535	00000000h
4D0–4D3h	"Port Status and Control USB2 (PORTSC6)—Offset 4D0h" on page 2536	000002A0h
4D4–4D7h	"Port Power Management Status and Control USB2 (PORTPMSC6)—Offset 4D4h" on page 2538	00000000h
4DC–4DFh	"Port X Hardware LPM Control Register (PORTHLPMC6)—Offset 4DCh" on page 2539	00000000h
4E0–4E3h	"Port Status and Control USB2 (PORTSC7)—Offset 4E0h" on page 2540	000002A0h
4E4–4E7h	"Port Power Management Status and Control USB2 (PORTPMSC7)—Offset 4E4h" on page 2542	00000000h
4EC–4EFh	"Port X Hardware LPM Control Register (PORTHLPMC7)—Offset 4ECh" on page 2543	00000000h
4F0–4F3h	"Port Status and Control USB3 (PORTSC8)—Offset 4F0h" on page 2544	000002A0h
4F4–4F7h	"Port Power Management Status and Control USB3 (PORTPMSC8)—Offset 4F4h" on page 2546	00000000h
4F8–4FBh	"USB3 Port Link Info (PORTLI8)—Offset 4F8h" on page 2547	00000000h
500–503h	"Port Status and Control USB3 (PORTSC9)—Offset 500h" on page 2547	000002A0h
504–507h	"Port Power Management Status and Control USB3 (PORTPMSC9)—Offset 504h" on page 2550	00000000h
508–50Bh	"USB3 Port Link Info (PORTLI9)—Offset 508h" on page 2550	00000000h
510–513h	"Port Status and Control USB3 (PORTSC10)—Offset 510h" on page 2551	000002A0h
514–517h	"Port Power Management Status and Control USB3 (PORTPMSC10)—Offset 514h" on page 2553	00000000h
518–51Bh	"USB3 Port Link Info (PORTLI10)—Offset 518h" on page 2554	00000000h
520–523h	"Port Status and Control USB3 (PORTSC11)—Offset 520h" on page 2554	000002A0h

Offset	Register Name (Register Symbol)	Default Value
524–527h	"Port Power Management Status and Control USB3 (PORTPMSC11)—Offset 524h" on page 2556	00000000h
528–52Bh	"USB3 Port Link Info (PORTLI11)—Offset 528h" on page 2557	00000000h
530–533h	"Port Status and Control USB3 (PORTSC12)—Offset 530h" on page 2557	000002A0h
534–537h	"Port Power Management Status and Control USB3 (PORTPMSC12)—Offset 534h" on page 2560	00000000h
538–53Bh	"USB3 Port Link Info (PORTLI12)—Offset 538h" on page 2560	00000000h
540–543h	"Port Status and Control USB3 (PORTSC13)—Offset 540h" on page 2561	000002A0h
544–547h	"Port Power Management Status and Control USB3 (PORTPMSC13)—Offset 544h" on page 2563	00000000h
548–54Bh	"USB3 Port Link Info (PORTLI13)—Offset 548h" on page 2564	00000000h
2000–2003h	"Microframe Index (RTMFINDEX)—Offset 2000h" on page 2564	00000000h
2020–2023h	"Interrupter 1 Management (IMAN0)—Offset 2020h" on page 2565	00000000h
2024–2027h	"Interrupter 1 Moderation (IMOD0)—Offset 2024h" on page 2565	00000FA0h
2028–202Bh	"Event Ring Segment Table Size 1 (ERSTSZ0)—Offset 2028h" on page 2566	00000000h
2030–2033h	"Event Ring Segment Table Base Address Low 1 (ERSTBA_LO0)—Offset 2030h" on page 2566	00000000h
2034–2037h	"Event Ring Segment Table Base Address High 1 (ERSTBA_HI0)—Offset 2034h" on page 2567	00000000h
2038–203Bh	"Event Ring Dequeue Pointer Low 1 (ERDP_LO0)—Offset 2038h" on page 2567	00000000h
203C–203Fh	"Event Ring Dequeue Pointer High 1 (ERDP_HI0)—Offset 203Ch" on page 2568	00000000h
2040–2043h	"Interrupter 2 Management (IMAN1)—Offset 2040h" on page 2569	00000000h
2044–2047h	"Interrupter 2 Moderation (IMOD1)—Offset 2044h" on page 2569	00000FA0h
2048–204Bh	"Event Ring Segment Table Size 2 (ERSTSZ1)—Offset 2048h" on page 2570	00000000h
2050–2053h	"Event Ring Segment Table Base Address Low 2 (ERSTBA_LO1)—Offset 2050h" on page 2570	00000000h
2054–2057h	"Event Ring Segment Table Base Address High 2 (ERSTBA_HI1)—Offset 2054h" on page 2571	00000000h
2058–205Bh	"Event Ring Dequeue Pointer Low 2 (ERDP_LO1)—Offset 2058h" on page 2571	00000000h

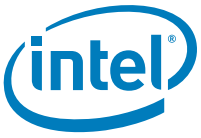


Offset	Register Name (Register Symbol)	Default Value
205C–205Fh	"Event Ring Dequeue Pointer High 2 (ERDP_HI1)—Offset 205Ch" on page 2572	00000000h
2060–2063h	"Interrupter 3 Management (IMAN2)—Offset 2060h" on page 2573	00000000h
2064–2067h	"Interrupter 3 Moderation (IMOD2)—Offset 2064h" on page 2573	00000FA0h
2068–206Bh	"Event Ring Segment Table Size 3 (ERSTSZ2)—Offset 2068h" on page 2574	00000000h
2070–2073h	"Event Ring Segment Table Base Address Low 3 (ERSTBA_LO2)—Offset 2070h" on page 2574	00000000h
2074–2077h	"Event Ring Segment Table Base Address High 3 (ERSTBA_HI2)—Offset 2074h" on page 2575	00000000h
2078–207Bh	"Event Ring Dequeue Pointer Low 3 (ERDP_LO2)—Offset 2078h" on page 2575	00000000h
207C–207Fh	"Event Ring Dequeue Pointer High 3 (ERDP_HI2)—Offset 207Ch" on page 2576	00000000h
2080–2083h	"Interrupter 4 Management (IMAN3)—Offset 2080h" on page 2577	00000000h
2084–2087h	"Interrupter 4 Moderation (IMOD3)—Offset 2084h" on page 2577	00000FA0h
2088–208Bh	"Event Ring Segment Table Size 4 (ERSTSZ3)—Offset 2088h" on page 2578	00000000h
2090–2093h	"Event Ring Segment Table Base Address Low 4 (ERSTBA_LO3)—Offset 2090h" on page 2578	00000000h
2094–2097h	"Event Ring Segment Table Base Address High 4 (ERSTBA_HI3)—Offset 2094h" on page 2579	00000000h
2098–209Bh	"Event Ring Dequeue Pointer Low 4 (ERDP_LO3)—Offset 2098h" on page 2579	00000000h
209C–209Fh	"Event Ring Dequeue Pointer High 4 (ERDP_HI3)—Offset 209Ch" on page 2580	00000000h
20A0–20A3h	"Interrupter 5 Management (IMAN4)—Offset 20A0h" on page 2581	00000000h
20A4–20A7h	"Interrupter 5 Moderation (IMOD4)—Offset 20A4h" on page 2581	00000FA0h
20A8–20ABh	"Event Ring Segment Table Size 5 (ERSTSZ4)—Offset 20A8h" on page 2582	00000000h
20B0–20B3h	"Event Ring Segment Table Base Address Low 5 (ERSTBA_LO4)—Offset 20B0h" on page 2582	00000000h
20B4–20B7h	"Event Ring Segment Table Base Address High 5 (ERSTBA_HI4)—Offset 20B4h" on page 2583	00000000h
20B8–20BBh	"Event Ring Dequeue Pointer Low 5 (ERDP_LO4)—Offset 20B8h" on page 2583	00000000h
20BC–20BFh	"Event Ring Dequeue Pointer High 5 (ERDP_HI4)—Offset 20BCh" on page 2584	00000000h

Offset	Register Name (Register Symbol)	Default Value
20C0–20C3h	"Interrupter 6 Management (IMAN5)—Offset 20C0h" on page 2585	00000000h
20C4–20C7h	"Interrupter 6 Moderation (IMOD5)—Offset 20C4h" on page 2585	00000FA0h
20C8–20CBh	"Event Ring Segment Table Size 6 (ERSTSZ5)—Offset 20C8h" on page 2586	00000000h
20D0–20D3h	"Event Ring Segment Table Base Address Low 6 (ERSTBA_LO5)—Offset 20D0h" on page 2586	00000000h
20D4–20D7h	"Event Ring Segment Table Base Address High 6 (ERSTBA_HI5)—Offset 20D4h" on page 2587	00000000h
20D8–20DBh	"Event Ring Dequeue Pointer Low 6 (ERDP_LO5)—Offset 20D8h" on page 2587	00000000h
20DC–20DFh	"Event Ring Dequeue Pointer High 6 (ERDP_HI5)—Offset 20DCh" on page 2588	00000000h
20E0–20E3h	"Interrupter 7 Management (IMAN6)—Offset 20E0h" on page 2589	00000000h
20E4–20E7h	"Interrupter 7 Moderation (IMOD6)—Offset 20E4h" on page 2589	00000FA0h
20E8–20EBh	"Event Ring Segment Table Size 7 (ERSTSZ6)—Offset 20E8h" on page 2590	00000000h
20F0–20F3h	"Event Ring Segment Table Base Address Low 7 (ERSTBA_LO6)—Offset 20F0h" on page 2590	00000000h
20F4–20F7h	"Event Ring Segment Table Base Address High 7 (ERSTBA_HI6)—Offset 20F4h" on page 2591	00000000h
20F8–20FBh	"Event Ring Dequeue Pointer Low 7 (ERDP_LO6)—Offset 20F8h" on page 2591	00000000h
20FC–20FFh	"Event Ring Dequeue Pointer High 7 (ERDP_HI6)—Offset 20FCh" on page 2592	00000000h
2100–2103h	"Interrupter 8 Management (IMAN7)—Offset 2100h" on page 2593	00000000h
2104–2107h	"Interrupter 8 Moderation (IMOD7)—Offset 2104h" on page 2593	00000FA0h
2108–210Bh	"Event Ring Segment Table Size 8 (ERSTSZ7)—Offset 2108h" on page 2594	00000000h
2110–2113h	"Event Ring Segment Table Base Address Low 8 (ERSTBA_LO7)—Offset 2110h" on page 2594	00000000h
2114–2117h	"Event Ring Segment Table Base Address High 8 (ERSTBA_HI7)—Offset 2114h" on page 2595	00000000h
2118–211Bh	"Event Ring Dequeue Pointer Low 8 (ERDP_LO7)—Offset 2118h" on page 2595	00000000h
211C–211Fh	"Event Ring Dequeue Pointer High 8 (ERDP_HI7)—Offset 211Ch" on page 2596	00000000h
3000–3003h	"Door Bell 1 (DB0)—Offset 3000h" on page 2597	00000000h

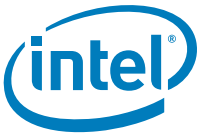


Offset	Register Name (Register Symbol)	Default Value
3004–3007h	"Door Bell 2 (DB1)—Offset 3004h" on page 2597	00000000h
3008–300Bh	"Door Bell 3 (DB2)—Offset 3008h" on page 2598	00000000h
300C–300Fh	"Door Bell 4 (DB3)—Offset 300Ch" on page 2598	00000000h
3010–3013h	"Door Bell 5 (DB4)—Offset 3010h" on page 2599	00000000h
3014–3017h	"Door Bell 6 (DB5)—Offset 3014h" on page 2600	00000000h
3018–301Bh	"Door Bell 7 (DB6)—Offset 3018h" on page 2600	00000000h
301C–301Fh	"Door Bell 8 (DB7)—Offset 301Ch" on page 2601	00000000h
3020–3023h	"Door Bell 9 (DB8)—Offset 3020h" on page 2602	00000000h
3024–3027h	"Door Bell 10 (DB9)—Offset 3024h" on page 2602	00000000h
3028–302Bh	"Door Bell 11 (DB10)—Offset 3028h" on page 2603	00000000h
302C–302Fh	"Door Bell 12 (DB11)—Offset 302Ch" on page 2604	00000000h
3030–3033h	"Door Bell 13 (DB12)—Offset 3030h" on page 2604	00000000h
3034–3037h	"Door Bell 14 (DB13)—Offset 3034h" on page 2605	00000000h
3038–303Bh	"Door Bell 15 (DB14)—Offset 3038h" on page 2606	00000000h
303C–303Fh	"Door Bell 16 (DB15)—Offset 303Ch" on page 2606	00000000h
3040–3043h	"Door Bell 17 (DB16)—Offset 3040h" on page 2607	00000000h
3044–3047h	"Door Bell 18 (DB17)—Offset 3044h" on page 2608	00000000h
3048–304Bh	"Door Bell 19 (DB18)—Offset 3048h" on page 2608	00000000h
304C–304Fh	"Door Bell 20 (DB19)—Offset 304Ch" on page 2609	00000000h
3050–3053h	"Door Bell 21 (DB20)—Offset 3050h" on page 2610	00000000h
3054–3057h	"Door Bell 22 (DB21)—Offset 3054h" on page 2610	00000000h
3058–305Bh	"Door Bell 23 (DB22)—Offset 3058h" on page 2611	00000000h

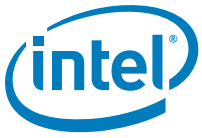


Offset	Register Name (Register Symbol)	Default Value
305C–305Fh	"Door Bell 24 (DB23)—Offset 305Ch" on page 2612	00000000h
3060–3063h	"Door Bell 25 (DB24)—Offset 3060h" on page 2612	00000000h
3064–3067h	"Door Bell 26 (DB25)—Offset 3064h" on page 2613	00000000h
3068–306Bh	"Door Bell 27 (DB26)—Offset 3068h" on page 2614	00000000h
306C–306Fh	"Door Bell 28 (DB27)—Offset 306Ch" on page 2614	00000000h
3070–3073h	"Door Bell 29 (DB28)—Offset 3070h" on page 2615	00000000h
3074–3077h	"Door Bell 30 (DB29)—Offset 3074h" on page 2616	00000000h
3078–307Bh	"Door Bell 31 (DB30)—Offset 3078h" on page 2616	00000000h
307C–307Fh	"Door Bell 32 (DB31)—Offset 307Ch" on page 2617	00000000h
3080–3083h	"Door Bell 32 (DB32)—Offset 3080h" on page 2618	00000000h
8000–8003h	"XECP_SUPP_USB2_0—Offset 8000h" on page 2618	02000802h
8004–8007h	"XECP_SUPP_USB2_1—Offset 8004h" on page 2619	20425355h
8008–800Bh	"XECP_SUPP_USB2_2—Offset 8008h" on page 2620	30190701h
8010–8013h	"XECP_SUPP_USB2_3 (Full Speed) (XECP_SUPP_USB2_3)—Offset 8010h" on page 2621	000C0021h
8014–8017h	"XECP_SUPP_USB2_4 (Low Speed) (XECP_SUPP_USB2_4)—Offset 8014h" on page 2622	05DC0012h
8018–801Bh	"XECP_SUPP_USB2_5 (High Speed) (XECP_SUPP_USB2_5)—Offset 8018h" on page 2623	01E00023h
8020–8023h	"XECP_SUPP_USB3_0—Offset 8020h" on page 2623	03001402h
8024–8027h	"XECP_SUPP_USB3_1—Offset 8024h" on page 2624	20425355h
8028–802Bh	"XECP_SUPP_USB3_2—Offset 8028h" on page 2625	30000608h
8030–8033h	"XECP_SUPP_USB3_3—Offset 8030h" on page 2625	04E00121h
8034–8037h	"XECP_SUPP_USB3_4—Offset 8034h" on page 2626	09C00122h
8038–803Bh	"XECP_SUPP_USB3_5—Offset 8038h" on page 2627	13800123h

Offset	Register Name (Register Symbol)	Default Value
803C–803Fh	"XECP_SUPP_USB3_6—Offset 803Ch" on page 2628	00050134h
8040–8043h	"XECP_SUPP_USB3_7—Offset 8040h" on page 2629	05B10125h
8044–8047h	"XECP_SUPP_USB3_8—Offset 8044h" on page 2630	0B630126h
8048–804Bh	"XECP_SUPP_USB3_9—Offset 8048h" on page 2630	16C60127h
8070–8073h	"Host Controller Capability (HOST_CTRL_CAP_REG)—Offset 8070h" on page 2631	004DFFC0h
8078–807Bh	"Override EP Flow Control (HOST_CLR_MASK_REG)—Offset 8078h" on page 2632	00000000h
807C–807Fh	"Clear Active IN EP ID Control (HOST_CLR_IN_EP_VALID_REG)—Offset 807Ch" on page 2633	00000000h
8080–8083h	"Clear Poll Mask Control (HOST_CLR_PMASK_REG)—Offset 8080h" on page 2634	00000000h
8094–8097h	"Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h" on page 2635	00008100h
80A0–80A3h	"Global Port Control (HOST_CTRL_PORT_CTRL)—Offset 80A0h" on page 2636	0000380Fh
80A4–80A7h	"Power Management Control (PMCTRL_REG)—Offset 80A4h" on page 2637	0001FF90h
80A8–80ABh	"PGCB Control (PGCBCTRL_REG)—Offset 80A8h" on page 2639	00315555h
80AC–80AFh	"D0I3 Control (DOI3CTRL_REG)—Offset 80ACh" on page 2643	00000008h
80B0–80B3h	"HOST_CTRL_MISC_REG—Offset 80B0h" on page 2644	0001037Fh
80B4–80B7h	"HOST_CTRL_MISC_REG2—Offset 80B4h" on page 2647	00000000h
80B8–80BBh	"SSPE_REG—Offset 80B8h" on page 2647	00000000h
80BC–80BFh	"reg_SSPITPE_type (SSPITPE)—Offset 80BCh" on page 2648	0000003Fh
80C0–80C3h	"AUX Reset Control (AUX_CTRL_REG)—Offset 80C0h" on page 2649	015FC0F0h
80C4–80C7h	"Super Speed Bandwidth Overload (HOST_BW_OV_SS_REG)—Offset 80C4h" on page 2653	004A4008h
80C8–80CBh	"High Speed TT Bandwidth Overload (HOST_BW_OV_HS_REG)—Offset 80C8h" on page 2654	0001A01Fh
80CC–80CFh	"Bandwidth Overload Full Low Speed (HOST_BW_OV_FS_LS_REG)—Offset 80CCh" on page 2654	00014080h
80D0–80D3h	"System Bandwidth Overload (HOST_BW_OV_SYS_REG)—Offset 80D0h" on page 2655	00032010h

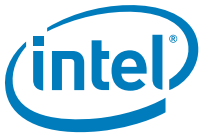


Offset	Register Name (Register Symbol)	Default Value
80D4–80D7h	"Scheduler Async Delay (HOST_CTRL_SCH_ASYNC_DELAY_REG)—Offset 80D4h" on page 2656	00000000h
80D8–80DBh	"DEVICE MODE CONTROL REG 0 (DUAL_ROLE_CFG_REG0)—Offset 80D8h" on page 2657	00000800h
80DC–80DFh	"DEVICE MODE CONTROL REG 1 (DUAL_ROLE_CFG_REG1)—Offset 80DCh" on page 2660	10000000h
80E0–80E3h	"AUX Power Management Control (AUX_CTRL_REG1)—Offset 80E0h" on page 2661	808DBCA0h
80E4–80E7h	"Battery Charge (BATTERY_CHARGE_REG)—Offset 80E4h" on page 2664	00000000h
80E8–80EBh	"Port Watermark (HOST_CTRL_WATERMARK_REG)—Offset 80E8h" on page 2665	00800080h
80EC–80EFh	"SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)—Offset 80ECh" on page 2666	18010000h
80F0–80F3h	"USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)—Offset 80F0h" on page 2668	310803A0h
80F4–80F7h	"USB2 Port Link Control 2 (USB2_LINK_MGR_CTRL_REG2)—Offset 80F4h" on page 2671	80C40620h
80F8–80FBh	"USB2 Port Link Control 3 (USB2_LINK_MGR_CTRL_REG3)—Offset 80F8h" on page 2672	F865EB6Bh
80FC–80FFh	"USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)—Offset 80FCh" on page 2673	00008003h
8100–8103h	"Bandwidth Calc Control (HOST_CTRL_BW_CTRL_REG)—Offset 8100h" on page 2674	00008008h
8108–810Bh	"Host Interface Control (HOST_IF_CTRL_REG)—Offset 8108h" on page 2675	00000001h
810C–810Fh	"Bandwidth Overload Burst (HOST_BW_OV_BURST_REG)—Offset 810Ch" on page 2675	00008020h
8128–812Fh	"USB Max Bandwidth Control 4 (HOST_CTRL_BW_MAX_REG)—Offset 8128h" on page 2676	0F42528505647F42h
8130–8133h	"USB2 Linestate Debug (LINESTATE_DEBUG_REG)—Offset 8130h" on page 2677	00000000h
8134–813Bh	"USB2 Protocol Gap Timer (USB2_PROTOCOL_GAP_TIMER_REG)—Offset 8134h" on page 2679	000C3C640C05140Ch
813C–813Fh	"USB2 Protocol Bus Timeout Timer (USB2_PROTOCOL_BTO_TIMER_REG)—Offset 813Ch" on page 2680	8D4258B8h
8140–8143h	"Power Scheduler Control-0 (PWR_SCHED_CTRL0)—Offset 8140h" on page 2680	0A019132h
8144–8147h	"Power Scheduler Control-2 (PWR_SCHED_CTRL2)—Offset 8144h" on page 2681	0000033Fh
8154–8157h	"AUX Power Management Control (AUX_CTRL_REG2)—Offset 8154h" on page 2683	81390206h
8164–8167h	"USB2 PHY Power Management Control (USB2_PHY_PMC)—Offset 8164h" on page 2686	000000FCh

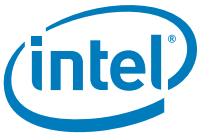


Offset	Register Name (Register Symbol)	Default Value
8168–816Bh	"USB2 Phy Power Management Control 2 (USB2_PHY_PMC2)—Offset 8168h" on page 2687	000282EEh
816C–816Fh	"xHCI Aux Clock Control Register (XHCI_AUX_CCR)—Offset 816Ch" on page 2688	00000400h
8170–8173h	"USB LPM Parameters (USB_LPM_PARAM)—Offset 8170h" on page 2691	00090032h
8174–8177h	"xHC Latency Tolerance Parameters - LTV Control (XLTP_LTV1)—Offset 8174h" on page 2693	0040047Dh
8178–817Bh	"xHC Latency Tolerance Parameters LTV Control 2 (XLTP_LTV2)—Offset 8178h" on page 2694	000017FFh
817C–817Fh	"xHC Latency Tolerance Parameters - High Idle Time Control (XLTP_HITC)—Offset 817Ch" on page 2695	00000000h
8180–8183h	"xHC Latency Tolerance Parameters - Medium Idle Time Control (XLTP_MITC)—Offset 8180h" on page 2696	00000000h
8184–8187h	"xHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)—Offset 8184h" on page 2697	00000000h
8188–818Bh	"HOST_CTRL_BW_MAX3_REG—Offset 8188h" on page 2697	00F42F42h
8198–819Bh	"PDDIS_REG—Offset 8198h" on page 2698	00000000h
819C–819Fh	"THRM_HOST_CTRL_REG—Offset 819Ch" on page 2699	00000000h
81A0–81A3h	"LFPS_PM_CTRL_REG—Offset 81A0h" on page 2701	00000000h
81A4–81A7h	"U2PDM—Offset 81A4h" on page 2701	00000000h
81A8–81ABh	"U2PCM—Offset 81A8h" on page 2702	00000000h
81AC–81AFh	"U3PDM—Offset 81ACh" on page 2702	00000000h
81B0–81B3h	"U3PCM—Offset 81B0h" on page 2703	00000000h
81B8–81BBh	"LFPSONCOUNT_REG—Offset 81B8h" on page 2703	000020C8h
81BC–81BFh	"reg_D0i2_CTRL_REG_type (D0i2_CTRL_REG)—Offset 81BCh" on page 2704	084204B0h
81C0–81C3h	"reg_D0i2_SCH_ALARM_CTRL_REG_type (D0i2_SCH_ALARM_CTRL_REG)—Offset 81C0h" on page 2706	00000000h
81C4–81C7h	"reg_USB2PMCTRL_REG_type (USB2PMCTRL_REG)—Offset 81C4h" on page 2707	00000000h
8410–8413h	"FUS1_REG—Offset 8410h" on page 2709	00000000h
8430–8433h	"DFT_REG1—Offset 8430h" on page 2711	00000000h

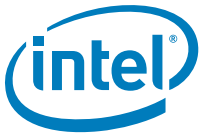
Offset	Register Name (Register Symbol)	Default Value
8434–8437h	"DFT_REG2—Offset 8434h" on page 2712	00000000h
8438–843Bh	"DFT_REG3—Offset 8438h" on page 2714	00000000h
843C–843Fh	"dft_reg4 (DFT_REG4)—Offset 843Ch" on page 2715	00000000h
8440–8443h	"dft_reg5 (DFT_REG5)—Offset 8440h" on page 2716	00000000h
8448–844Bh	"XECP_CMDM_STS0—Offset 8448h" on page 2717	00000000h
844C–844Fh	"XECP_CMDM_STS1—Offset 844Ch" on page 2719	03FC0000h
8450–8453h	"XECP_CMDM_STS2—Offset 8450h" on page 2720	00000000h
8454–8457h	"XECP_CMDM_STS3—Offset 8454h" on page 2720	00000000h
8458–845Bh	"XECP_CMDM_STS4—Offset 8458h" on page 2721	00000000h
845C–845Fh	"XECP_CMDM_STS5—Offset 845Ch" on page 2721	00000000h
8460–8463h	"AUX Power PHY Reset (UPORTS_PON_RST_REG)—Offset 8460h" on page 2722	00000000h
8464–8467h	"Latency Tolerance Control 0 (HOST_IF_LAT_TOL_CTRL_REG0)—Offset 8464h" on page 2722	000D0000h
846C–846Fh	"USB Legacy Support Capability (USBLEGSUP)—Offset 846Ch" on page 2723	00002501h
8470–8473h	"USB Legacy Support Control Status (USBLEGCTLSTS)—Offset 8470h" on page 2724	00000000h
84F4–84F7h	"Port Disable Override capability register (PDO_CAPABILITY)—Offset 84F4h" on page 2726	000003C6h
84F8–84FBh	"USB2 Port Disable Override (USB2PDO)—Offset 84F8h" on page 2726	00000000h
84FC–84FFh	"USB3 Port Disable Override (USB3PDO)—Offset 84FCh" on page 2727	00000000h
8500–8503h	"HW state capability register (HW_STATE_CAPABILITY)—Offset 8500h" on page 2727	001D40C7h
8504–8507h	"HW state register 1 (HW_STATE_REG1)—Offset 8504h" on page 2728	00000000h
8508–850Bh	"HW state register 2 (HW_STATE_REG2)—Offset 8508h" on page 2729	00000000h
850C–850Fh	"HW state register 3 (HW_STATE_REG3)—Offset 850Ch" on page 2729	00000000h
8510–8513h	"HW state register 4 (HW_STATE_REG4)—Offset 8510h" on page 2730	00000000h



Offset	Register Name (Register Symbol)	Default Value
8600–8603h	"CONFIG mirror capability register (CONFIG_MIRROR_CAPABILITY)—Offset 8600h" on page 2731	000040C2h
8604–8605h	"Command (CMD_MMIO)—Offset 8604h" on page 2731	0000h
8606–8607h	"Device Status (STS_MMIO)—Offset 8606h" on page 2733	0290h
8608–8608h	"Revision ID (RID_MMIO)—Offset 8608h" on page 2734	00h
8609–8609h	"Programming Interface (PI_MMIO)—Offset 8609h" on page 2735	30h
860A–860Ah	"Sub Class Code (SCC_MMIO)—Offset 860Ah" on page 2735	03h
860B–860Ch	"Base Class Code (BCC_MMIO)—Offset 860Bh" on page 2736	0Ch
860D–860Dh	"Master Latency Timer (MLT_MMIO)—Offset 860Dh" on page 2736	00h
860E–860Fh	"Header Type (HT_MMIO)—Offset 860Eh" on page 2736	00h
8610–8617h	"Memory Base Address (MBAR_MMIO)—Offset 8610h" on page 2737	0000000000000004h
862C–862Dh	"USB Subsystem Vendor ID (SSVID_MMIO)—Offset 862Ch" on page 2738	0000h
862E–862Fh	"USB Subsystem ID (SSID_MMIO)—Offset 862Eh" on page 2739	0000h
8634–8634h	"Capabilities Pointer (CAP_PTR_MMIO)—Offset 8634h" on page 2739	70h
863C–863Ch	"Interrupt Line (ILINE_MMIO)—Offset 863Ch" on page 2740	00h
863D–863Fh	"Interrupt Pin (IPIN_MMIO)—Offset 863Dh" on page 2740	00h
8658–865Bh	"Audio Time Synchronization (AUDSYNC_MMIO)—Offset 8658h" on page 2741	00000000h
8660–8660h	"Serial Bus Release Number (SBRN_MMIO)—Offset 8660h" on page 2741	30h
8661–8661h	"Frame Length Adjustment (FLADJ_MMIO)—Offset 8661h" on page 2742	60h
8662–8662h	"Best Effort Service Latency (BESL_MMIO)—Offset 8662h" on page 2743	00h
8670–8670h	"PCI Power Management Capability ID (PM_CID_MMIO)—Offset 8670h" on page 2744	01h
8671–8671h	"Next Item Pointer #1 (PM_NEXT_MMIO)—Offset 8671h" on page 2744	80h
8672–8673h	"Power Management Capabilities (PM_CAP_MMIO)—Offset 8672h" on page 2745	C1C2h

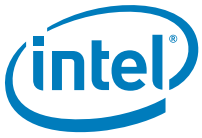


Offset	Register Name (Register Symbol)	Default Value
8674–8675h	"Power Management Control/Status (PM_CS_MMIO)—Offset 8674h" on page 2746	0008h
8680–8680h	"Message Signaled Interrupt CID (MSI_CID_MMIO)—Offset 8680h" on page 2748	05h
8681–8681h	"Next item pointer (MSI_NEXT_MMIO)—Offset 8681h" on page 2748	00h
8682–8683h	"Message Signaled Interrupt Message Control (MSI_MCTL_MMIO)—Offset 8682h" on page 2749	0086h
8684–8687h	"Message Signaled Interrupt Message Address (MSI_MAD_MMIO)—Offset 8684h" on page 2750	00000000h
8688–868Bh	"Message Signaled Interrupt Upper Address (MSI_MUAD_MMIO)—Offset 8688h" on page 2750	00000000h
868C–868Dh	"Message Signaled Interrupt Message Data (MSI_MD_MMIO)—Offset 868Ch" on page 2751	0000h
8694–8697h	"Fuse and Strap (FUS_MMIO)—Offset 8694h" on page 2752	00000000h
86A4–86A7h	"High Speed Configuration 2 (HSCFG2_MMIO)—Offset 86A4h" on page 2753	00002000h
86B0–86B3h	"XHCI USB2 Overcurrent Pin Mapping 1 (U2OCM1_MMIO)—Offset 86B0h" on page 2755	00000000h
86B4–86B7h	"XHCI USB2 Overcurrent Pin Mapping 2 (U2OCM2_MMIO)—Offset 86B4h" on page 2756	00000000h
86D0–86D3h	"XHCI USB3 Overcurrent Pin Mapping 1 (U3OCM1_MMIO)—Offset 86D0h" on page 2757	00000000h
86D4–86D7h	"XHCI USB3 Overcurrent Pin Mapping 2 (U3OCM2_MMIO)—Offset 86D4h" on page 2757	00000000h
8700–8703h	"Debug Capability ID Register (DCID)—Offset 8700h" on page 2758	0005100Ah
8704–8707h	"Debug Capability Doorbell Register (DCDB)—Offset 8704h" on page 2759	00000000h
8708–870Bh	"Debug Capability Event Ring Segment Table Size Register (DCERSTSZ)—Offset 8708h" on page 2760	00000000h
8710–8717h	"Debug Capability Event Ring Segment Table Base Address Register (DCERSTBA)—Offset 8710h" on page 2760	0000000000000000h
8718–871Fh	"Debug Capability Event Ring Dequeue Pointer Register (DCERDP)—Offset 8718h" on page 2761	0000000000000000h
8720–8723h	"Debug Capability Control Register (DCCTRL)—Offset 8720h" on page 2762	00000000h
8724–8727h	"Debug Capability Status Register (DCST)—Offset 8724h" on page 2763	00000000h
8728–872Bh	"Debug Capability Port Status and Control Register (DCPORTSC)—Offset 8728h" on page 2763	00000080h
8730–8737h	"Debug Capability Context Pointer Register (DCCP)—Offset 8730h" on page 2766	0000000000000000h



Offset	Register Name (Register Symbol)	Default Value
8738–873Bh	"Debug Capability Device Descriptor Info Register 1 (DCDDI1)—Offset 8738h" on page 2766	00000000h
873C–873Fh	"Debug Capability Device Descriptor Info Register 2 (DCDDI2)—Offset 873Ch" on page 2767	00000000h
8740–8743h	"Debug Capability Descriptor Parameters (DCDP)—Offset 8740h" on page 2767	000030C3h
8748–874Bh	"Debug Device Control ODMA (DBGDEV_CTRL_ODMA_REG)—Offset 8748h" on page 2768	00000000h
8800–8803h	"SSIC Policy and Implementation Specific Registers Capability ID register (SSIC_IMPLEMENTATION_CAPABILITY_ID_REG)—Offset 8800h" on page 2770	000040C4h
8804–8807h	"SSIC global configuration control register (SSIC_GLOBAL_CONFIG_CONTROL_REG)—Offset 8804h" on page 2771	00000000h
8808–880Bh	"reg_SSIC_CONFIG_REG1_type (PORT1_SSIC_CONFIG_REG1)—Offset 8808h" on page 2772	82286000h
880C–880Fh	"reg_SSIC_CONFIG_REG2_type (PORT1_SSIC_CONFIG_REG2)—Offset 880Ch" on page 2774	04821F46h
8810–8813h	"reg_SSIC_CONFIG_REG3_type (PORT1_SSIC_CONFIG_REG3)—Offset 8810h" on page 2775	40480000h
8814–8817h	"reg_SSIC_CONFIG_REG4_type (PORT1_SSIC_CONFIG_REG4)—Offset 8814h" on page 2777	64796464h
8818–881Bh	"reg_SSIC_LOOPBACK_CONFIG_REG_type (PORT1_SSIC_LOOPBACK_CONFIG_REG)—Offset 8818h" on page 2777	00000000h
881C–881Fh	"reg_SSIC_LOOPBACK_BURST_COUNT_REG_type (PORT1_SSIC_LOOPBACK_BURST_COUNT_REG)—Offset 881Ch" on page 2778	00000000h
8820–8823h	"reg_SSIC_LOOPBACK_ERROR_COUNT_REG_type (PORT1_SSIC_LOOPBACK_ERROR_COUNT_REG)—Offset 8820h" on page 2779	00000000h
8838–883Bh	"reg_SSIC_CONFIG_REG1_type (PORT2_SSIC_CONFIG_REG1)—Offset 8838h" on page 2780	82286000h
883C–883Fh	"reg_SSIC_CONFIG_REG2_type (PORT2_SSIC_CONFIG_REG2)—Offset 883Ch" on page 2782	04821F46h
8840–8843h	"reg_SSIC_CONFIG_REG3_type (PORT2_SSIC_CONFIG_REG3)—Offset 8840h" on page 2784	40480000h
8844–8847h	"reg_SSIC_CONFIG_REG4_type (PORT2_SSIC_CONFIG_REG4)—Offset 8844h" on page 2785	64796464h
8848–884Bh	"reg_SSIC_LOOPBACK_CONFIG_REG_type (PORT2_SSIC_LOOPBACK_CONFIG_REG)—Offset 8848h" on page 2786	00000000h
884C–884Fh	"reg_SSIC_LOOPBACK_BURST_COUNT_REG_type (PORT2_SSIC_LOOPBACK_BURST_COUNT_REG)—Offset 884Ch" on page 2787	00000000h
8850–8853h	"reg_SSIC_LOOPBACK_ERROR_COUNT_REG_type (PORT2_SSIC_LOOPBACK_ERROR_COUNT_REG)—Offset 8850h" on page 2788	00000000h
8900–8903h	"SSIC Local and Remote Profile Registers Capability ID register (SSIC_PROFILE_CAPABILITY_ID_REG)—Offset 8900h" on page 2789	000000C5h
8904–8907h	"SSIC Port N Register Access Control (PORT1_REGISTER_ACCESS_CONTROL)—Offset 8904h" on page 2790	00C00000h

Offset	Register Name (Register Symbol)	Default Value
8908–890Bh	"SSIC Port N Register Access Status (PORT1_REGISTER_ACCESS_STATUS)—Offset 8908h" on page 2791	00000000h
890C–890Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG0)—Offset 890Ch" on page 2792	00000000h
8910–8913h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG1)—Offset 8910h" on page 2793	00000000h
8914–8917h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG2)—Offset 8914h" on page 2794	00000000h
8918–891Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG3)—Offset 8918h" on page 2795	00000000h
891C–891Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG4)—Offset 891Ch" on page 2796	00000000h
8920–8923h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG5)—Offset 8920h" on page 2797	00000000h
8924–8927h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG6)—Offset 8924h" on page 2798	00000000h
8928–892Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG7)—Offset 8928h" on page 2798	00000000h
892C–892Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG8)—Offset 892Ch" on page 2799	00000000h
8930–8933h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG9)—Offset 8930h" on page 2800	00000000h
8934–8937h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG10)—Offset 8934h" on page 2801	00000000h
8938–893Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG11)—Offset 8938h" on page 2802	00000000h
893C–893Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG12)—Offset 893Ch" on page 2803	00000000h
8940–8943h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG13)—Offset 8940h" on page 2804	00000000h
8944–8947h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG14)—Offset 8944h" on page 2805	00000000h
8948–894Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG15)—Offset 8948h" on page 2806	00000000h
894C–894Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG16)—Offset 894Ch" on page 2807	00000000h
8950–8953h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG17)—Offset 8950h" on page 2808	00000000h
8954–8957h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG18)—Offset 8954h" on page 2809	00000000h
8958–895Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG19)—Offset 8958h" on page 2810	00000000h
895C–895Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG20)—Offset 895Ch" on page 2811	00000000h



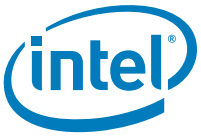
Offset	Register Name (Register Symbol)	Default Value
8960–8963h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG21)—Offset 8960h" on page 2812	00000000h
8964–8967h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG22)—Offset 8964h" on page 2813	00000000h
8968–896Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG23)—Offset 8968h" on page 2814	00000000h
896C–896Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG24)—Offset 896Ch" on page 2815	00000000h
8970–8973h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG25)—Offset 8970h" on page 2816	00000000h
8974–8977h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG26)—Offset 8974h" on page 2817	00000000h
8978–897Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG27)—Offset 8978h" on page 2818	00000000h
897C–897Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG28)—Offset 897Ch" on page 2819	00000000h
8980–8983h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG29)—Offset 8980h" on page 2820	00000000h
8984–8987h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG30)—Offset 8984h" on page 2821	00000000h
8988–898Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG31)—Offset 8988h" on page 2822	00000000h
898C–898Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG32)—Offset 898Ch" on page 2823	00000000h
8990–8993h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG33)—Offset 8990h" on page 2824	00000000h
8994–8997h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG34)—Offset 8994h" on page 2825	00000000h
8998–899Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG35)—Offset 8998h" on page 2826	00000000h
899C–899Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG36)—Offset 899Ch" on page 2827	00000000h
89A0–89A3h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG37)—Offset 89A0h" on page 2828	00000000h
89A4–89A7h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG38)—Offset 89A4h" on page 2829	00000000h
89A8–89ABh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG39)—Offset 89A8h" on page 2830	00000000h
89AC–89AFh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG40)—Offset 89ACh" on page 2831	00000000h
89B0–89B3h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG41)—Offset 89B0h" on page 2832	00000000h
89B4–89B7h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG42)—Offset 89B4h" on page 2833	00000000h

Offset	Register Name (Register Symbol)	Default Value
89B8–89BBh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG43)—Offset 89B8h" on page 2834	00000000h
89BC–89BFh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG44)—Offset 89BCh" on page 2835	00000000h
89C0–89C3h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG45)—Offset 89C0h" on page 2836	00000000h
89C4–89C7h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG46)—Offset 89C4h" on page 2837	00000000h
89C8–89CBh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG47)—Offset 89C8h" on page 2838	00000000h
89CC–89CFh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG48)—Offset 89CCh" on page 2839	00000000h
89D0–89D3h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG49)—Offset 89D0h" on page 2840	00000000h
89D4–89D7h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG50)—Offset 89D4h" on page 2841	00000000h
89D8–89DBh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG51)—Offset 89D8h" on page 2842	00000000h
89DC–89DFh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG52)—Offset 89DCh" on page 2843	00000000h
89E0–89E3h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG53)—Offset 89E0h" on page 2844	00000000h
89E4–89E7h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG54)—Offset 89E4h" on page 2845	00000000h
89E8–89EBh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG55)—Offset 89E8h" on page 2846	00000000h
89EC–89EFh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG56)—Offset 89ECh" on page 2847	00000000h
89F0–89F3h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG57)—Offset 89F0h" on page 2848	00000000h
89F4–89F7h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG58)—Offset 89F4h" on page 2849	00000000h
89F8–89FBh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG59)—Offset 89F8h" on page 2850	00000000h
89FC–89FFh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG60)—Offset 89FCh" on page 2851	00000000h
8A00–8A03h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG61)—Offset 8A00h" on page 2852	00000000h
8A04–8A07h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG62)—Offset 8A04h" on page 2853	00000000h
8A08–8A0Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG63)—Offset 8A08h" on page 2854	00000000h
8A14–8A17h	"SSIC Port N Register Access Control (PORT2_REGISTER_ACCESS_CONTROL)—Offset 8A14h" on page 2855	00C00000h

Offset	Register Name (Register Symbol)	Default Value
8A18–8A1Bh	"SSIC Port N Register Access Status (PORT2_REGISTER_ACCESS_STATUS)—Offset 8A18h" on page 2857	00000000h
8A1C–8A1Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG0)—Offset 8A1Ch" on page 2857	00000000h
8A20–8A23h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG1)—Offset 8A20h" on page 2858	00000000h
8A24–8A27h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG2)—Offset 8A24h" on page 2859	00000000h
8A28–8A2Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG3)—Offset 8A28h" on page 2860	00000000h
8A2C–8A2Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG4)—Offset 8A2Ch" on page 2861	00000000h
8A30–8A33h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG5)—Offset 8A30h" on page 2862	00000000h
8A34–8A37h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG6)—Offset 8A34h" on page 2863	00000000h
8A38–8A3Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG7)—Offset 8A38h" on page 2864	00000000h
8A3C–8A3Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG8)—Offset 8A3Ch" on page 2865	00000000h
8A40–8A43h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG9)—Offset 8A40h" on page 2866	00000000h
8A44–8A47h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG10)—Offset 8A44h" on page 2867	00000000h
8A48–8A4Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG11)—Offset 8A48h" on page 2868	00000000h
8A4C–8A4Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG12)—Offset 8A4Ch" on page 2869	00000000h
8A50–8A53h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG13)—Offset 8A50h" on page 2870	00000000h
8A54–8A57h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG14)—Offset 8A54h" on page 2871	00000000h
8A58–8A5Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG15)—Offset 8A58h" on page 2872	00000000h
8A5C–8A5Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG16)—Offset 8A5Ch" on page 2873	00000000h
8A60–8A63h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG17)—Offset 8A60h" on page 2874	00000000h
8A64–8A67h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG18)—Offset 8A64h" on page 2875	00000000h
8A68–8A6Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG19)—Offset 8A68h" on page 2876	00000000h
8A6C–8A6Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG20)—Offset 8A6Ch" on page 2877	00000000h

Offset	Register Name (Register Symbol)	Default Value
8A70–8A73h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG21)—Offset 8A70h" on page 2878	00000000h
8A74–8A77h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG22)—Offset 8A74h" on page 2879	00000000h
8A78–8A7Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG23)—Offset 8A78h" on page 2880	00000000h
8A7C–8A7Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG24)—Offset 8A7Ch" on page 2881	00000000h
8A80–8A83h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG25)—Offset 8A80h" on page 2882	00000000h
8A84–8A87h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG26)—Offset 8A84h" on page 2883	00000000h
8A88–8A8Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG27)—Offset 8A88h" on page 2884	00000000h
8A8C–8A8Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG28)—Offset 8A8Ch" on page 2885	00000000h
8A90–8A93h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG29)—Offset 8A90h" on page 2886	00000000h
8A94–8A97h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG30)—Offset 8A94h" on page 2887	00000000h
8A98–8A9Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG31)—Offset 8A98h" on page 2888	00000000h
8A9C–8A9Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG32)—Offset 8A9Ch" on page 2889	00000000h
8AA0–8AA3h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG33)—Offset 8AA0h" on page 2890	00000000h
8AA4–8AA7h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG34)—Offset 8AA4h" on page 2891	00000000h
8AA8–8AABh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG35)—Offset 8AA8h" on page 2892	00000000h
8AAC–8AAFh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG36)—Offset 8AACh" on page 2893	00000000h
8AB0–8AB3h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG37)—Offset 8AB0h" on page 2894	00000000h
8AB4–8AB7h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG38)—Offset 8AB4h" on page 2895	00000000h
8AB8–8ABBh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG39)—Offset 8AB8h" on page 2896	00000000h
8ABC–8ABFh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG40)—Offset 8ABCh" on page 2897	00000000h
8AC0–8AC3h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG41)—Offset 8AC0h" on page 2898	00000000h
8AC4–8AC7h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG42)—Offset 8AC4h" on page 2899	00000000h

Offset	Register Name (Register Symbol)	Default Value
8AC8–8ACBh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG43)—Offset 8AC8h" on page 2900	00000000h
8ACC–8ACFh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG44)—Offset 8ACCh" on page 2901	00000000h
8AD0–8AD3h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG45)—Offset 8AD0h" on page 2902	00000000h
8AD4–8AD7h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG46)—Offset 8AD4h" on page 2903	00000000h
8AD8–8ADBh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG47)—Offset 8AD8h" on page 2904	00000000h
8ADC–8ADFh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG48)—Offset 8ADCh" on page 2905	00000000h
8AE0–8AE3h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG49)—Offset 8AE0h" on page 2906	00000000h
8AE4–8AE7h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG50)—Offset 8AE4h" on page 2907	00000000h
8AE8–8AEBh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG51)—Offset 8AE8h" on page 2908	00000000h
8AEC–8AEFh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG52)—Offset 8AECh" on page 2909	00000000h
8AF0–8AF3h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG53)—Offset 8AF0h" on page 2910	00000000h
8AF4–8AF7h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG54)—Offset 8AF4h" on page 2911	00000000h
8AF8–8AFBh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG55)—Offset 8AF8h" on page 2912	00000000h
8AFC–8AFFh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG56)—Offset 8AFCh" on page 2913	00000000h
8B00–8B03h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG57)—Offset 8B00h" on page 2914	00000000h
8B04–8B07h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG58)—Offset 8B04h" on page 2915	00000000h
8B08–8B0Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG59)—Offset 8B08h" on page 2916	00000000h
8B0C–8B0Fh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG60)—Offset 8B0Ch" on page 2917	00000000h
8B10–8B13h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG61)—Offset 8B10h" on page 2918	00000000h
8B14–8B17h	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG62)—Offset 8B14h" on page 2919	00000000h
8B18–8B1Bh	"reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG63)—Offset 8B18h" on page 2920	00000000h



7.4.1 Capability Registers Length (CAPLENGTH)—Offset 0h

This register is modified and maintained by BIOS

Access Method

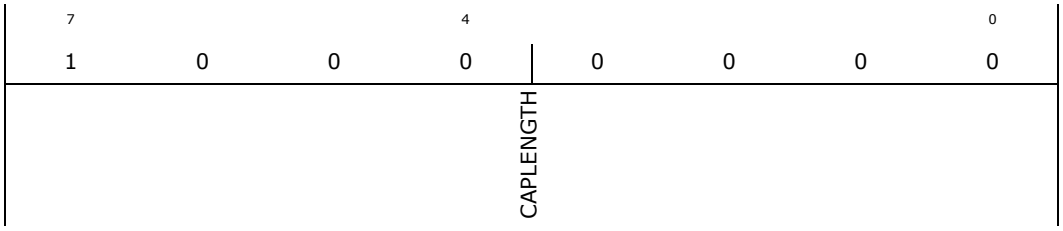
Type: Message Bus Register (Size: 8 bits)

Offset: [Port: 0x5A] + 0h

Op Codes:

h - Read, h - Write

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x80 RW/L	**Capability Registers Length (CAPLENGTH):** Reserved. **Power Well:** Core

7.4.2 Host Controller Interface Version Number (HCIVERSION)—Offset 2h

This register is modified and maintained by BIOS

Access Method

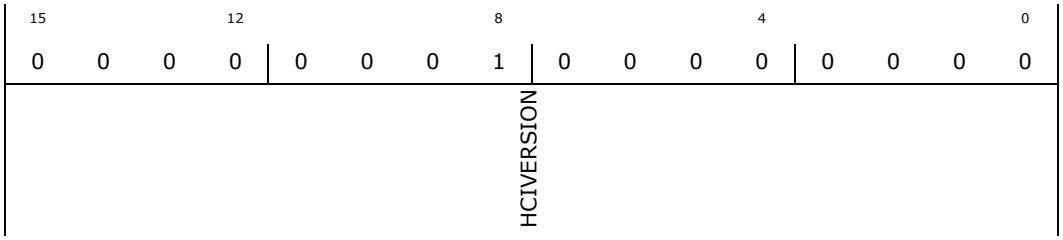
Type: Message Bus Register (Size: 16 bits)

Offset: [Port: 0x5A] + 2h

Op Codes:

h - Read, h - Write

Default: 0100h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0x100 RO	**Host Controller Interface Version Number (HCIVERSION):** Reserved. **Power Well:** Core

7.4.3 Structural Parameters 1 (HCSPARAMS1)—Offset 4h

This register is modified and maintained by BIOS

Access Method

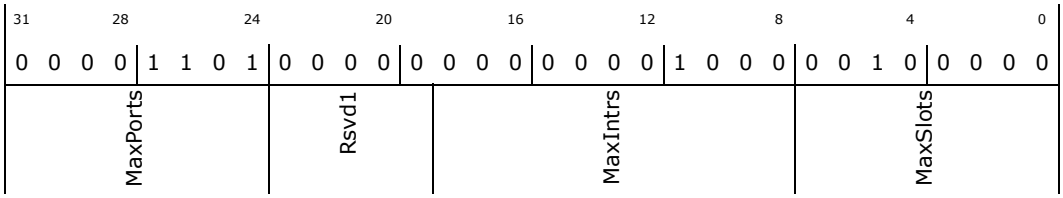
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4h

Op Codes:

h - Read, h - Write

Default: 0D000820h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0xd RO	**Number of Ports (MaxPorts):** Reserved. **Power Well:** Core
23:19	0x0 RW/L	**Rsvd1:** Reserved. **Power Well:** Core
18:8	0x8 RW/L	**Number of Interrupters (MaxIntrs):** Reserved. **Power Well:** Core
7:0	0x20 RW/L	**Number of Device Slots (MaxSlots):** Reserved. **Power Well:** Core

7.4.4 Structural Parameters 2 (HCSPARAMS2)—Offset 8h

This register is modified and maintained by BIOS

Access Method

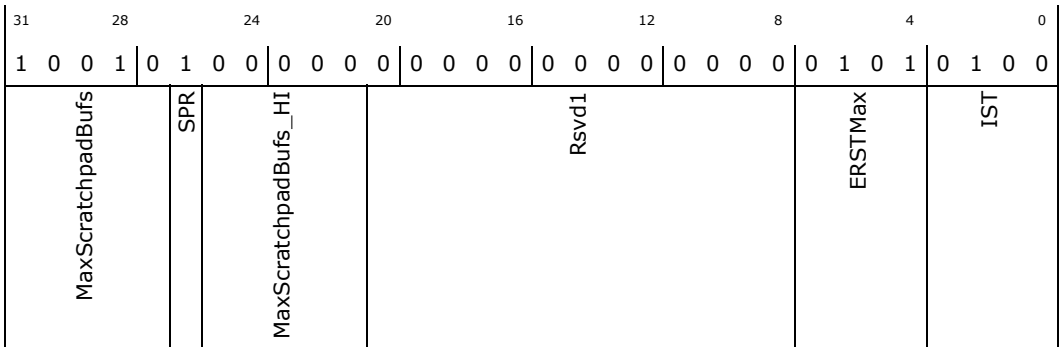
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8h

Op Codes:

h - Read, h - Write

Default: 94000054h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x12 RW/L	**Max Scratchpad Buffers LO (MaxScratchpadBufs):** Reserved. **Power Well:** Core
26	0x1 RW/L	**Scratchpad Restore (SPR):** Reserved. **Power Well:** Core
25:21	0x0 RW/L	**Max Scratchpad Buffers HI (MaxScratchpadBufs_HI):** Reserved. **Power Well:** Core
20:8	0x0 RW/L	**Rsvd1:** Reserved. **Power Well:** Core
7:4	0x5 RW/L	**Event Ring Segment Table Max (ERSTMax):** Reserved. **Power Well:** Core
3:0	0x4 RW/L	**Isochronous Scheduling Threshold (IST):** Reserved. **Power Well:** Core

7.4.5 Structural Parameters 3 (HCSPARAMS3)—Offset Ch

This register is modified and maintained by BIOS

Access Method

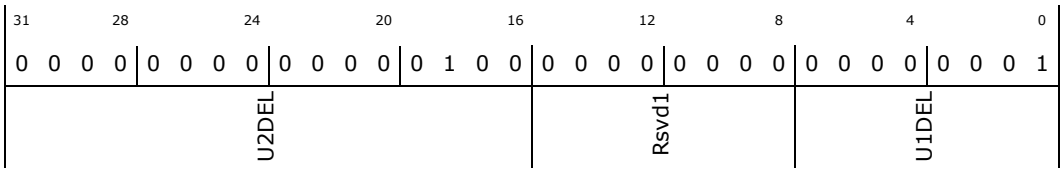
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + Ch

Op Codes:

h - Read, h - Write

Default: 00040001h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x4 RW/L	**U2 Device Exit Latency (U2DEL):** Reserved. **Power Well:** Core
15:8	0x0 RW/L	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x1 RW/L	**U1 Device Exit Latency (U1DEL):** Reserved. **Power Well:** Core

7.4.6 Capability Parameters (HCCPARAMS)—Offset 10h

This register is modified and maintained by BIOS

Access Method

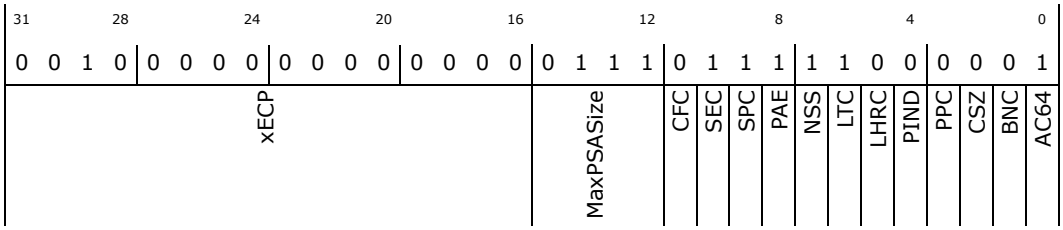
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 10h

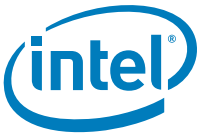
Op Codes:

h - Read, h - Write

Default: 200077C1h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x2000 RW/L	**xHCI Extended Capabilities Pointer (xECP):** Reserved. **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x7 RW/L	**Maximum Primary Stream Array Size (MaxPSASize):** Reserved. **Power Well:** Core
11	0x0 RW/L	**Contiguous Frame ID Capability (CFC):** Reserved. **Power Well:** Core
10	0x1 RW/L	**Stopped EDLTA Capabilty (SEC):** Reserved. **Power Well:** Core
9	0x1 RW/L	**Stopped - Short Packet Capability (SPC):** Reserved. **Power Well:** Core
8	0x1 RW/L	**Parst All Event Data (PAE):** Reserved. **Power Well:** Core
7	0x1 RW/L	**No Secondary SID Support (NSS):** Reserved. **Power Well:** Core
6	0x1 RW/L	**Latency Tolerance Messaging Capability (LTC):** Reserved. **Power Well:** Core
5	0x0 RW/L	**Light HC Reset Capability (LHRC):** Reserved. **Power Well:** Core
4	0x0 RW/L	**Port Indicators (PIND):** Reserved. **Power Well:** Core
3	0x0 RW/L	**Port Power Control (PPC):** Reserved. **Power Well:** Core
2	0x0 RW/L	**Context Size (CSZ):** Reserved. **Power Well:** Core
1	0x0 RW/L	**BW Negotiation Capability (BNC):** Reserved. **Power Well:** Core
0	0x1 RW/L	**64-bit Addressing Capability (AC64):** Reserved. **Power Well:** Core

7.4.7 Doorbell Offset (DBOFF)—Offset 14h

Access Method

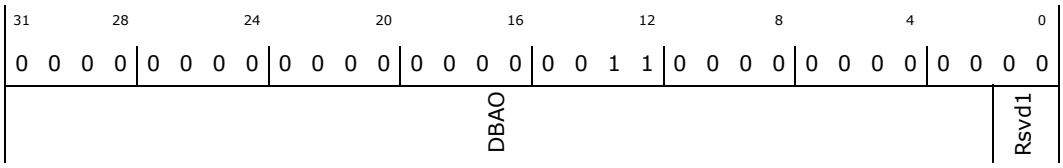
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 14h

Op Codes:

h - Read, h - Write

Default: 00003000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0xc00 RO	**Doorbell Array Offset (DBAO):** Reserved. **Power Well:** Core
1:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

7.4.8 Runtime Register Space Offset (RTSOFF)—Offset 18h

Access Method

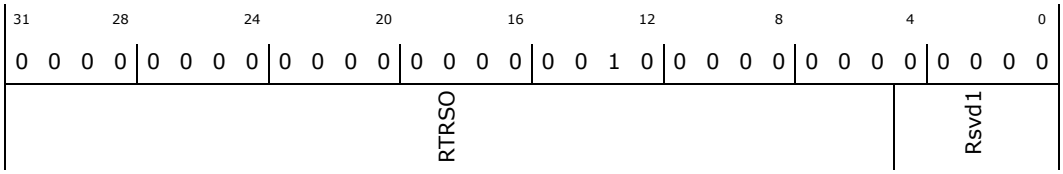
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 18h

Op Codes:

h - Read, h - Write

Default: 00002000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x100 RO	**Runtime Register Space Offset (RTRSO):** Reserved. **Power Well:** Core
4:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

7.4.9 USB Command (USBCMD)—Offset 80h

Access Method

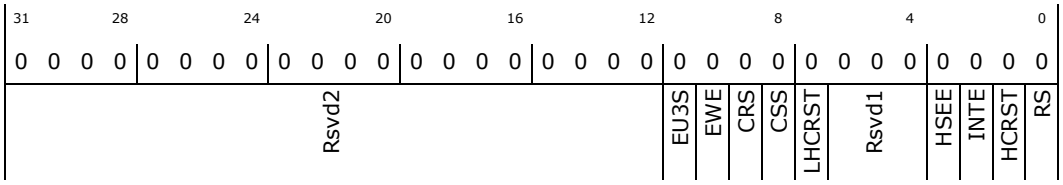
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
11	0x0 RW	**Enable U3 MFINDEX Stop (EU3S):** Reserved. **Power Well:** Core
10	0x0 RW	**Enable Wrap Event (EWE):** Reserved. **Power Well:** Core
9	0x0 RW	**Controller Restore State (CRS):** Reserved. **Power Well:** Core
8	0x0 RW	**Controller Save State (CSS):** Reserved. **Power Well:** Core
7	0x0 RW	**Light Host Controller Reset (LHCRST):** Reserved. **Power Well:** Core
6:4	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
3	0x0 RW	**Host System Error Enable (HSEE):** Reserved. **Power Well:** Core
2	0x0 RW	**Interrupter Enable (INTE):** Reserved. **Power Well:** Core
1	0x0 RW	**Host Controller Reset (HCRST):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**Run/Stop (RS):** Reserved. **Power Well:** Core

7.4.10 USB Status (USBSTS)—Offset 84h

Access Method

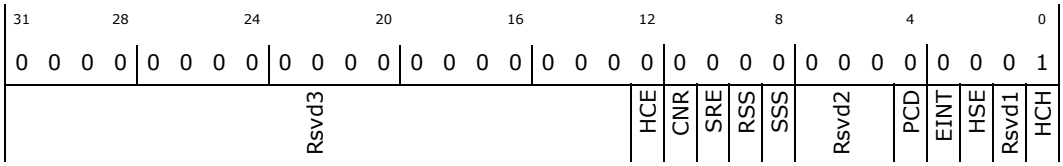
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 84h

Op Codes:

h - Read, h - Write

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**Rsvd3:** Reserved. **Power Well:** Core
12	0x0 RO	**Host Controller Error (HCE):** This bit is not preset in HC, this is deviation from XHCI 1.0 spec. **Power Well:** Core
11	0x0 RO	**Controller Not Ready (CNR):** This is deviation from XHCI 1.0 spec. **Power Well:** Core
10	0x0 RW/C	**Save/Restore Error (SRE):** Reserved. **Power Well:** Core
9	0x0 RO	**Restore State Status (RSS):** Reserved. **Power Well:** Core
8	0x0 RO	**Save State Status (SSS):** Reserved. **Power Well:** Core
7:5	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW/C	**Port Change Detect (PCD):** Reserved. **Power Well:** Core
3	0x0 RW/C	**Event Interrupt (EINT):** Reserved. **Power Well:** Core
2	0x0 RW/C	**Host System Error (HSE):** Reserved. **Power Well:** Core
1	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
0	0x1 RO	**HCHalted (HCH):** Reserved. **Power Well:** Core

7.4.11 Page Size (PAGESIZE)—Offset 88h

Access Method

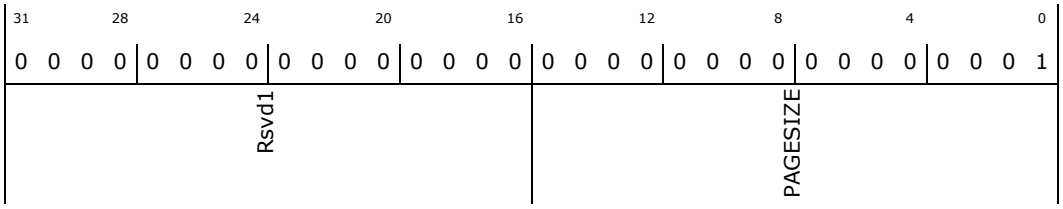
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 88h

Op Codes:

h - Read, h - Write

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x1 RO	**Page Size (PAGESIZE):** Reserved. **Power Well:** Core

7.4.12 Device Notification Control (DNCTRL)—Offset 94h

Access Method

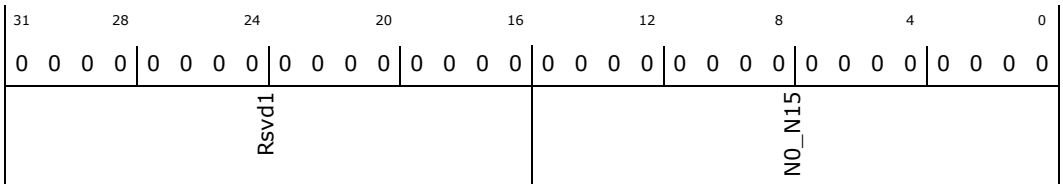
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 94h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RW	**Notification Enable (N0_N15):** Reserved. **Power Well:** Core

7.4.13 Command Ring Low (CRCR_LO)—Offset 98h

Access Method

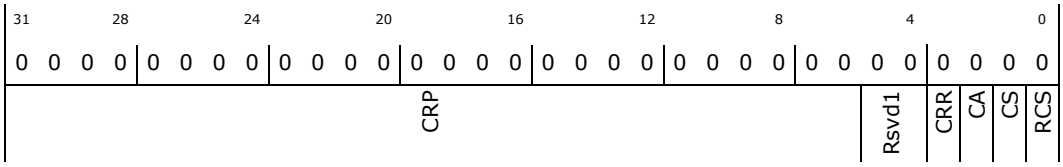
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 98h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Command Ring Pointer (CRP):** Reserved. **Power Well:** Core
5:4	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
3	0x0 RO	**Command Ring Running (CRR):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW/1S	**Command Abort (CA):** Reserved. **Power Well:** Core
1	0x0 RW/1S	**Command Stop (CS):** Reserved. **Power Well:** Core
0	0x0 RW	**Ring Cycle State (RCS):** Reserved. **Power Well:** Core

7.4.14 Command Ring High (CRCR_HI)—Offset 9Ch

Access Method

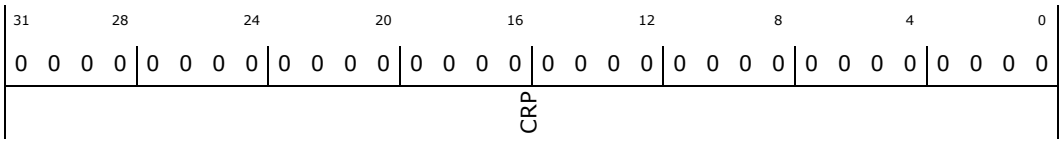
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 9Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Command Ring Pointer (CRP):** Reserved. **Power Well:** Core

7.4.15 Device Context Base Address Array Pointer Low (DCBAAP_LO)—Offset B0h

Access Method

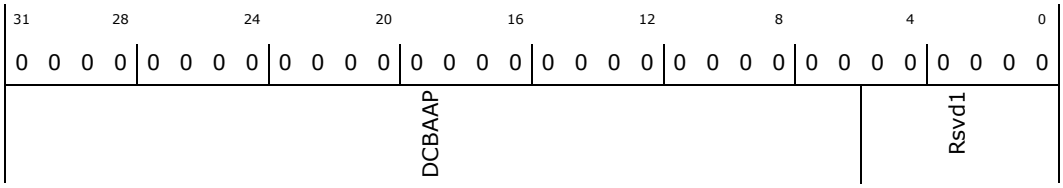
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + B0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Device Context Base Address Array Pointer (DCBAAP):** Reserved. **Power Well:** Core
5:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

7.4.16 Device Context Base Address Array Pointer High (DCBAAP_HI)—Offset B4h

Access Method

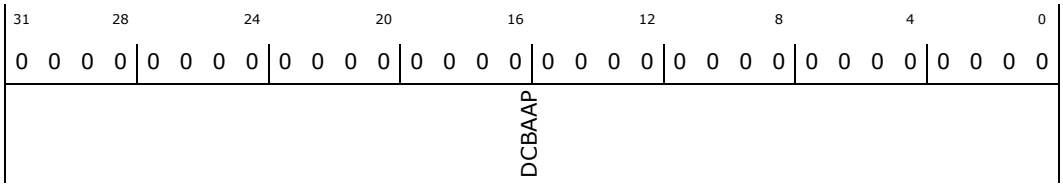
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + B4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Device Context Base Address Array Pointer (DCBAAP):** Reserved. **Power Well:** Core

7.4.17 Configure (CONFIG)—Offset B8h

Access Method

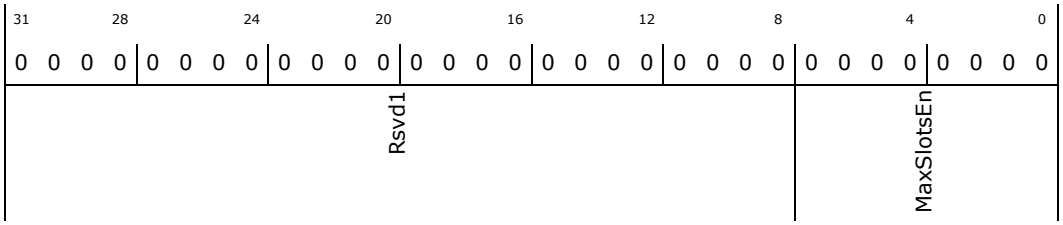
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + B8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**Max Device Slots Enabled (MaxSlotsEn):** Reserved. **Power Well:** Core

7.4.18 Port Status and Control USB2 (PORTSC1)—Offset 480h

Access Method

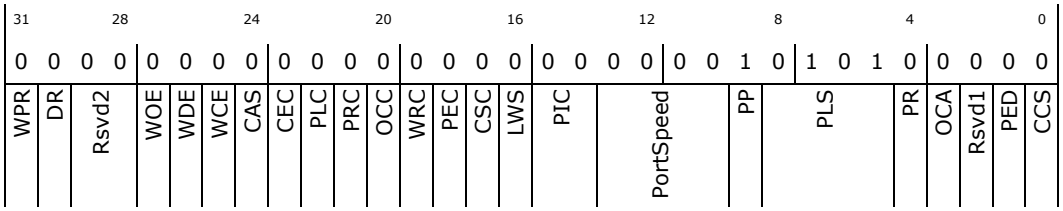
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 480h

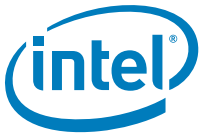
Op Codes:

h - Read, h - Write

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS



Bit Range	Default & Access	Field Name (ID): Description
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

7.4.19 Port Power Management Status and Control USB2 (PORTPMSC1)—Offset 484h

Access Method

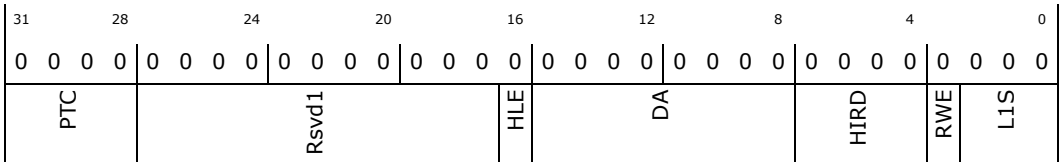
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 484h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS
27:17	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	0x0 RW	**Device Address (DA):** Note: This register is sticky. **Power Well:** SUS
7:4	0x0 RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0x0 RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0x0 RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

7.4.20 Port X Hardware LPM Control Register (PORTHLPMC1)—Offset 48Ch

There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

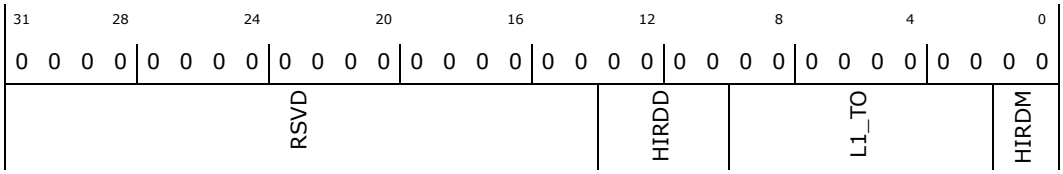
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 48Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
13:10	0x0 RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS
9:2	0x0 RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0x0 RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky. **Power Well:** SUS

7.4.21 Port Status and Control USB2 (PORTSC2)—Offset 490h

Access Method

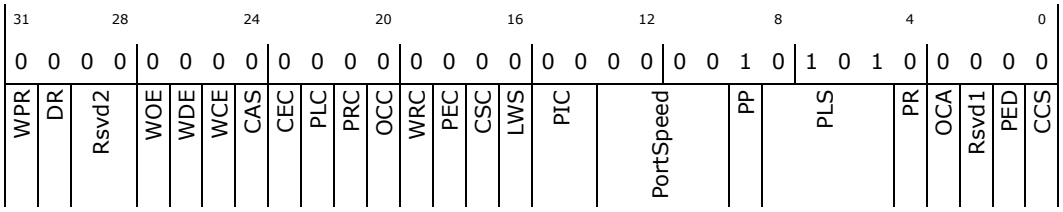
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 490h

Op Codes:

h - Read, h - Write

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

7.4.22 Port Power Management Status and Control USB2 (PORTPMSC2)—Offset 494h

Access Method

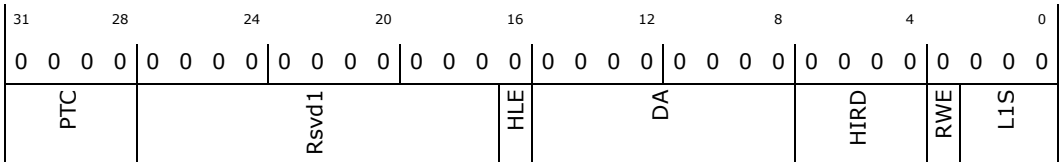
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 494h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS
27:17	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0x0 RW	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	0x0 RW	**Device Address (DA):** Note: This register is sticky. **Power Well:** SUS
7:4	0x0 RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0x0 RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0x0 RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

7.4.23 Port X Hardware LPM Control Register (PORTHLPMC2)—Offset 49Ch

There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

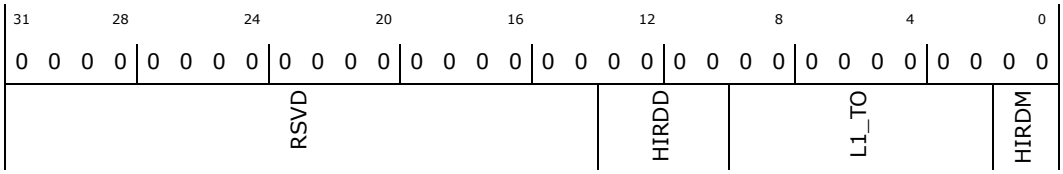
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 49Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
13:10	0x0 RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS
9:2	0x0 RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0x0 RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky. **Power Well:** SUS

7.4.24 Port Status and Control USB2 (PORTSC3)—Offset 4A0h

Access Method

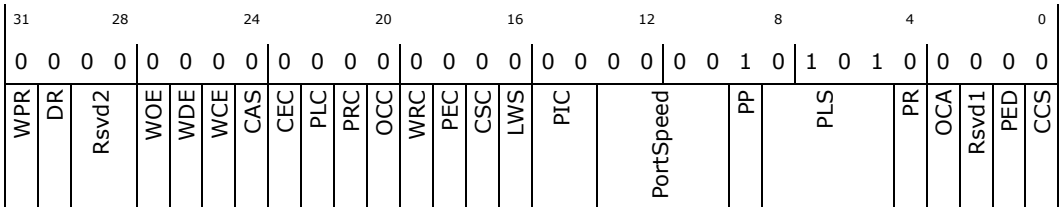
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4A0h

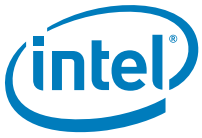
Op Codes:

h - Read, h - Write

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS



Bit Range	Default & Access	Field Name (ID): Description
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

7.4.25 Port Power Management Status and Control USB2 (PORTPMSC3)—Offset 4A4h

Access Method

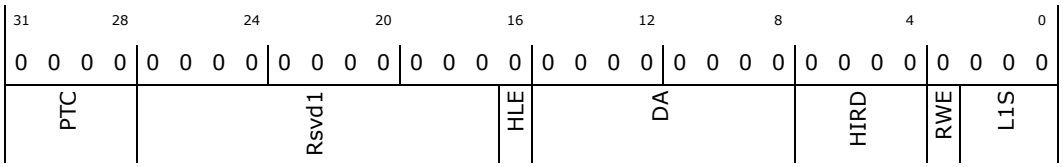
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4A4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS
27:17	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0x0 RW	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	0x0 RW	**Device Address (DA):** Note: This register is sticky. **Power Well:** SUS
7:4	0x0 RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0x0 RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0x0 RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

7.4.26 Port X Hardware LPM Control Register (PORTHLPMC3)—Offset 4ACh

There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

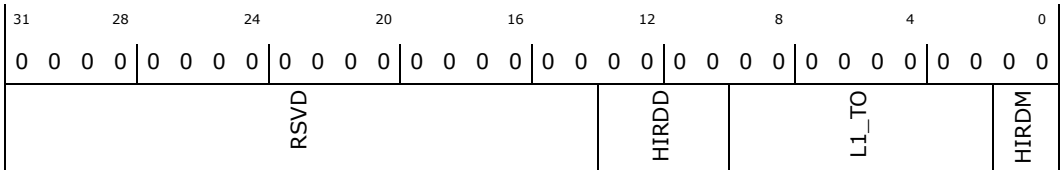
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4ACh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
13:10	0x0 RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS
9:2	0x0 RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0x0 RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky. **Power Well:** SUS

7.4.27 Port Status and Control USB2 (PORTSC4)—Offset 4B0h

Access Method

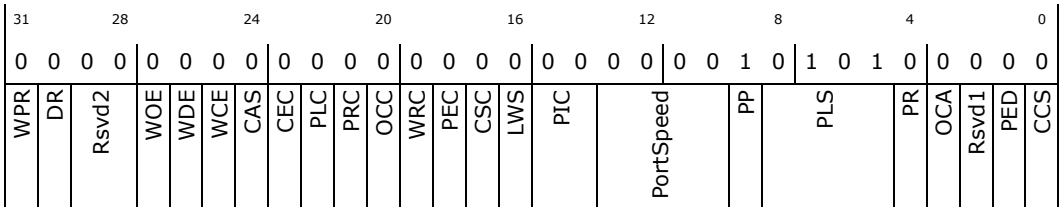
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4B0h

Op Codes:

h - Read, h - Write

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

7.4.28 Port Power Management Status and Control USB2 (PORTPMSC4)—Offset 4B4h

Access Method

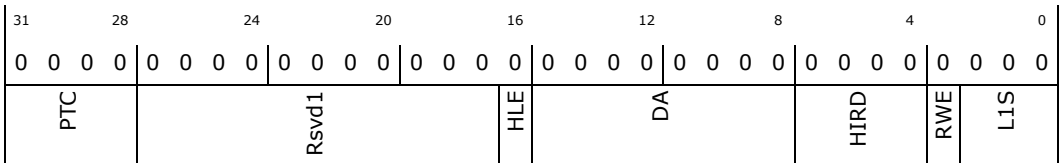
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4B4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS
27:17	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0x0 RW	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	0x0 RW	**Device Address (DA):** Note: This register is sticky. **Power Well:** SUS
7:4	0x0 RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0x0 RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0x0 RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

7.4.29 Port X Hardware LPM Control Register (PORTHLPMC4)—Offset 4BCh

There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

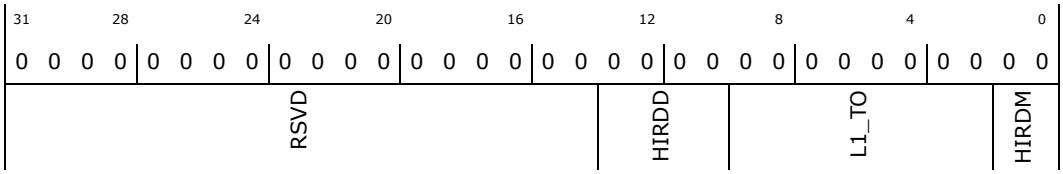
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4BCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
13:10	0x0 RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS
9:2	0x0 RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0x0 RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky. **Power Well:** SUS

7.4.30 Port Status and Control USB2 (PORTSC5)—Offset 4C0h

Access Method

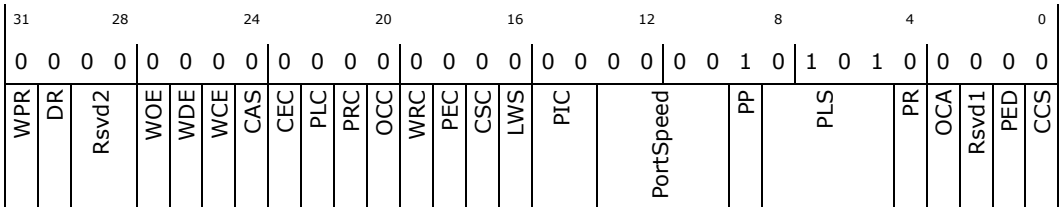
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4C0h

Op Codes:

h - Read, h - Write

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

7.4.31 Port Power Management Status and Control USB2 (PORTPMSC5)—Offset 4C4h

Access Method

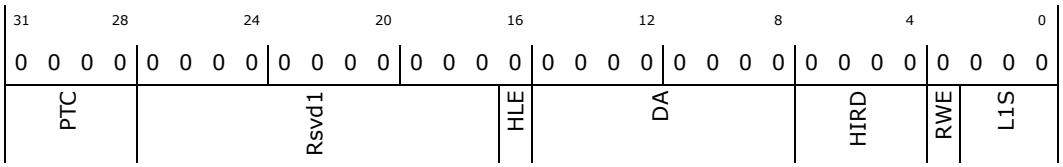
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4C4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS
27:17	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0x0 RW	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	0x0 RW	**Device Address (DA):** Note: This register is sticky. **Power Well:** SUS
7:4	0x0 RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0x0 RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0x0 RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

7.4.32 Port X Hardware LPM Control Register (PORTHLPMC5)—Offset 4CCh

There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

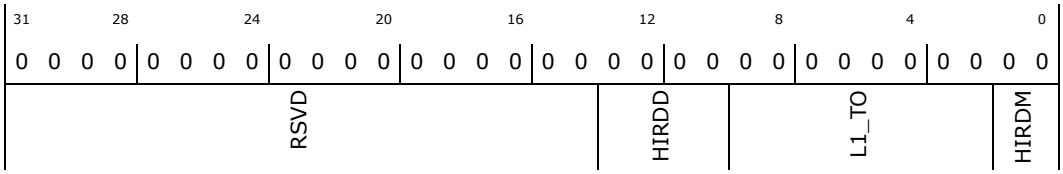
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4CCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
13:10	0x0 RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS
9:2	0x0 RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0x0 RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky. **Power Well:** SUS

7.4.33 Port Status and Control USB2 (PORTSC6)—Offset 4D0h

Access Method

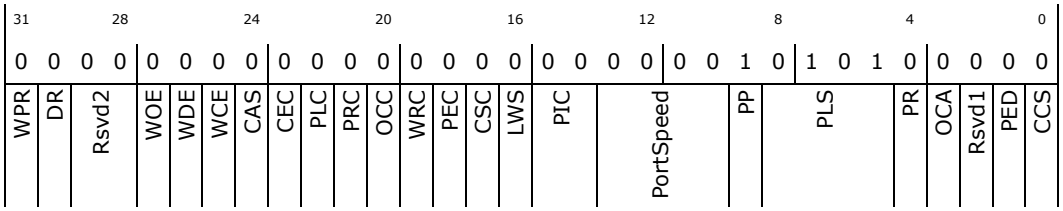
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4D0h

Op Codes:

h - Read, h - Write

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

7.4.34 Port Power Management Status and Control USB2 (PORTPMSC6)—Offset 4D4h

Access Method

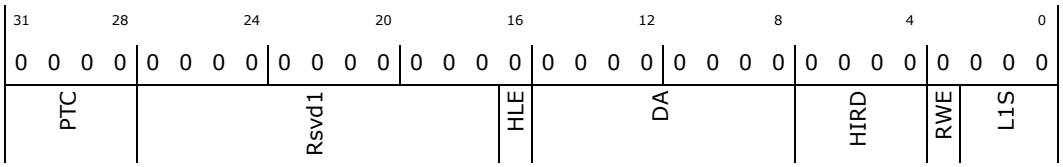
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4D4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS
27:17	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0x0 RW	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	0x0 RW	**Device Address (DA):** Note: This register is sticky. **Power Well:** SUS
7:4	0x0 RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0x0 RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0x0 RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

7.4.35 Port X Hardware LPM Control Register (PORTHLPMC6)—Offset 4DCh

There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

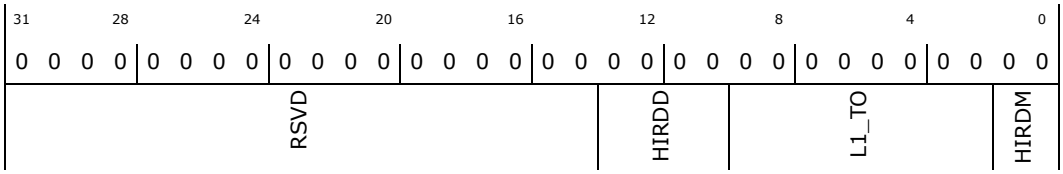
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4DCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
13:10	0x0 RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS
9:2	0x0 RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0x0 RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky. **Power Well:** SUS

7.4.36 Port Status and Control USB2 (PORTSC7)—Offset 4E0h

Access Method

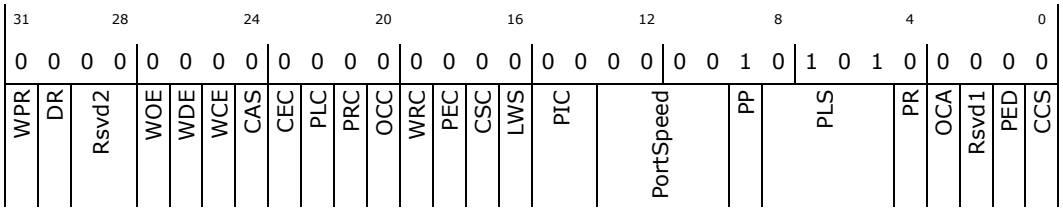
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4E0h

Op Codes:

h - Read, h - Write

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

7.4.37 Port Power Management Status and Control USB2 (PORTPMSC7)—Offset 4E4h

Access Method

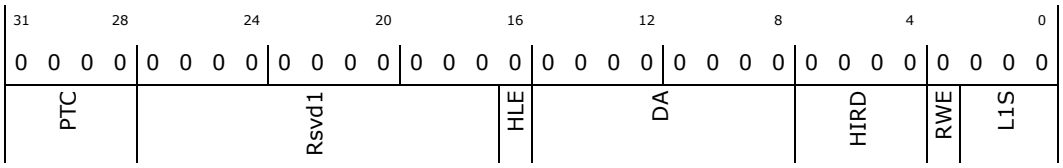
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4E4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW	**Port Test Control (PTC):** Note: This register is sticky. **Power Well:** SUS
27:17	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0x0 RW	**Hardware LPM Enable (HLE):** Reserved. **Power Well:** SUS
15:8	0x0 RW	**Device Address (DA):** Note: This register is sticky. **Power Well:** SUS
7:4	0x0 RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky. **Power Well:** SUS
3	0x0 RW	**Remote Wake Enable (RWE):** Note: This register is sticky. **Power Well:** SUS
2:0	0x0 RW	**L1 Status (L1S):** Note: This register is sticky. **Power Well:** SUS

7.4.38 Port X Hardware LPM Control Register (PORTHLPMC7)—Offset 4ECh

There are 9 PORTHLPMC registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

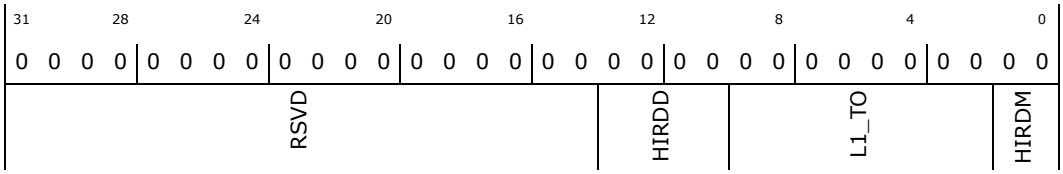
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4ECh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
13:10	0x0 RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value. **Power Well:** SUS
9:2	0x0 RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky. **Power Well:** SUS
1:0	0x0 RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky. **Power Well:** SUS

7.4.39 Port Status and Control USB3 (PORTSC8)—Offset 4F0h

Access Method

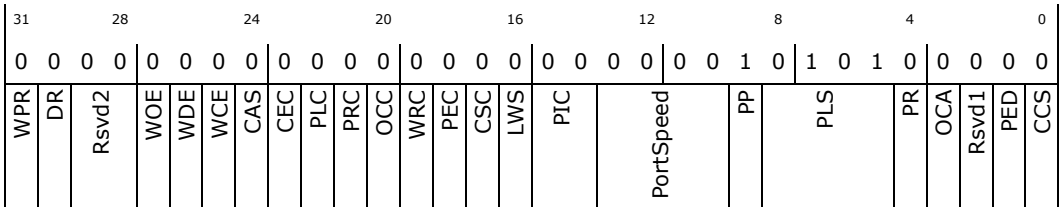
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4F0h

Op Codes:

h - Read, h - Write

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

7.4.40 Port Power Management Status and Control USB3 (PORTPMSC8)—Offset 4F4h

Access Method

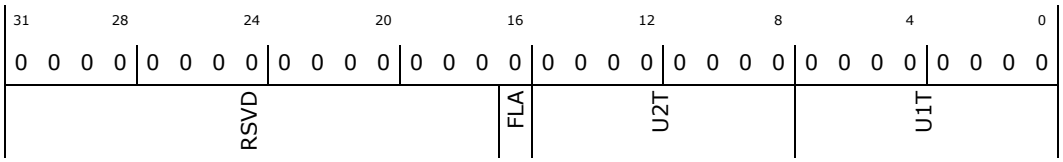
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4F4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
16	0x0 RW	**Force Link PM Accept (FLA):** Reserved. **Power Well:** SUS
15:8	0x0 RW/S	**U2 Timeout (U2T):** Reserved. **Power Well:** SUS
7:0	0x0 RW/S	**U1 Timeout (U1T):** Reserved. **Power Well:** SUS

7.4.41 USB3 Port Link Info (PORTLI8)—Offset 4F8h

Access Method

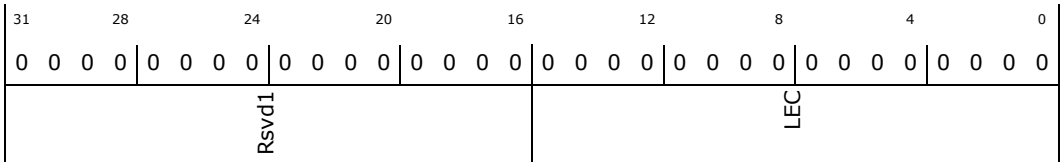
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 4F8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RO	**Link Error Count (LEC):** Reserved. **Power Well:** Core

7.4.42 Port Status and Control USB3 (PORTSC9)—Offset 500h

Access Method

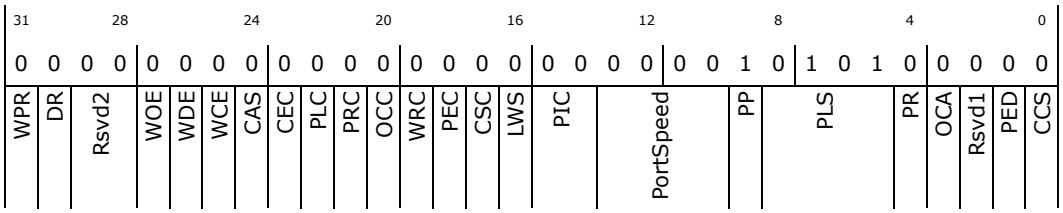
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 500h

Op Codes:

h - Read, h - Write

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

7.4.43 Port Power Management Status and Control USB3 (PORTPMSC9)—Offset 504h

Access Method

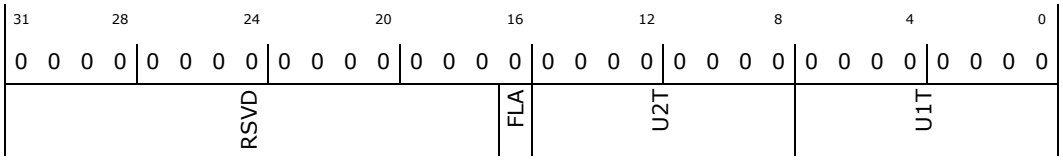
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 504h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
16	0x0 RW	**Force Link PM Accept (FLA):** Reserved. **Power Well:** SUS
15:8	0x0 RW/S	**U2 Timeout (U2T):** Reserved. **Power Well:** SUS
7:0	0x0 RW/S	**U1 Timeout (U1T):** Reserved. **Power Well:** SUS

7.4.44 USB3 Port Link Info (PORTLI9)—Offset 508h

Access Method

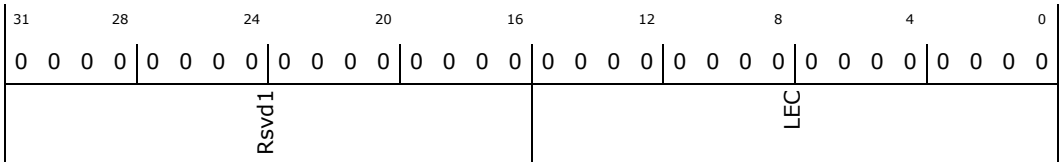
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 508h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RO	**Link Error Count (LEC):** Reserved. **Power Well:** Core

7.4.45 Port Status and Control USB3 (PORTSC10)—Offset 510h

Access Method

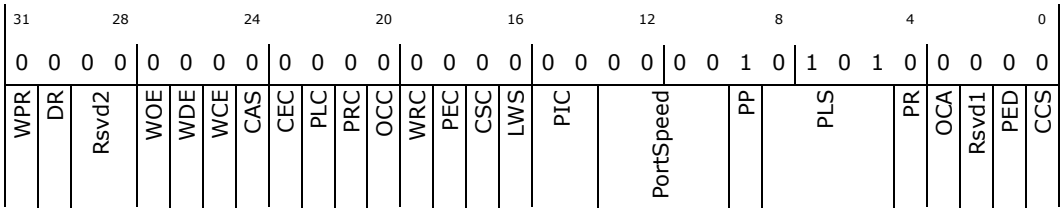
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 510h

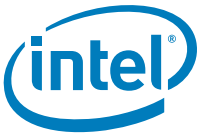
Op Codes:

h - Read, h - Write

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS



Bit Range	Default & Access	Field Name (ID): Description
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

7.4.46 Port Power Management Status and Control USB3 (PORTPMSC10)—Offset 514h

Access Method

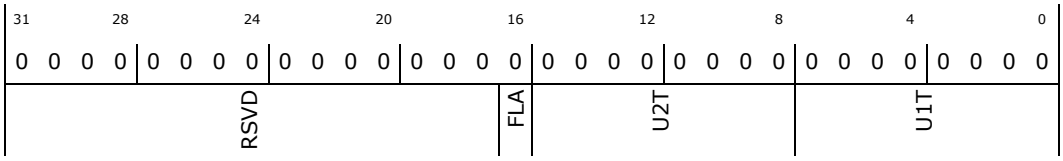
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 514h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
16	0x0 RW	**Force Link PM Accept (FLA):** Reserved. **Power Well:** SUS
15:8	0x0 RW/S	**U2 Timeout (U2T):** Reserved. **Power Well:** SUS
7:0	0x0 RW/S	**U1 Timeout (U1T):** Reserved. **Power Well:** SUS

7.4.47 USB3 Port Link Info (PORTLI10)—Offset 518h

Access Method

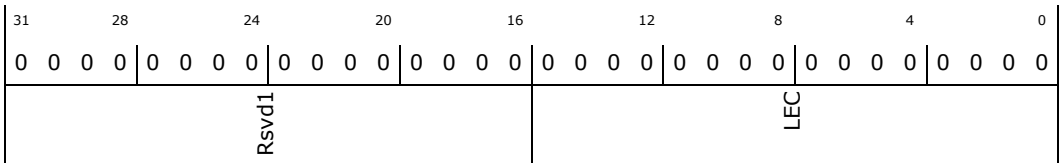
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 518h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RO	**Link Error Count (LEC):** Reserved. **Power Well:** Core

7.4.48 Port Status and Control USB3 (PORTSC11)—Offset 520h

Access Method

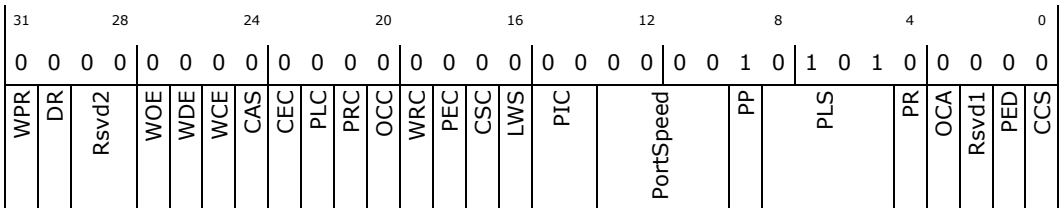
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 520h

Op Codes:

h - Read, h - Write

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

7.4.49 Port Power Management Status and Control USB3 (PORTPMSC11)—Offset 524h

Access Method

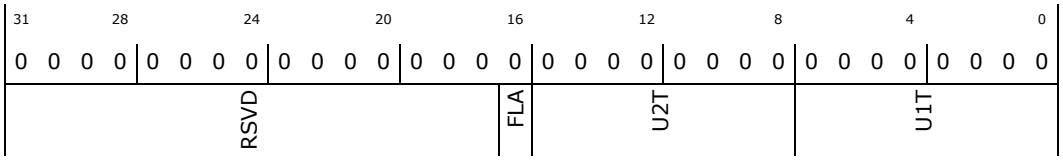
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 524h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
16	0x0 RW	**Force Link PM Accept (FLA):** Reserved. **Power Well:** SUS
15:8	0x0 RW/S	**U2 Timeout (U2T):** Reserved. **Power Well:** SUS
7:0	0x0 RW/S	**U1 Timeout (U1T):** Reserved. **Power Well:** SUS

7.4.50 USB3 Port Link Info (PORTLI11)—Offset 528h

Access Method

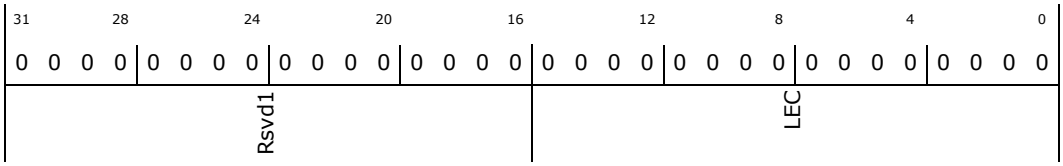
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 528h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RO	**Link Error Count (LEC):** Reserved. **Power Well:** Core

7.4.51 Port Status and Control USB3 (PORTSC12)—Offset 530h

Access Method

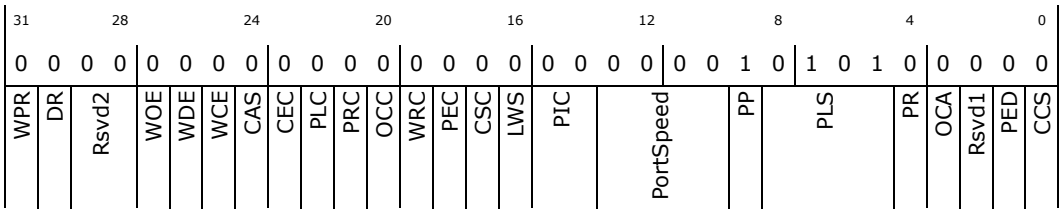
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 530h

Op Codes:

h - Read, h - Write

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

7.4.52 Port Power Management Status and Control USB3 (PORTPMSC12)—Offset 534h

Access Method

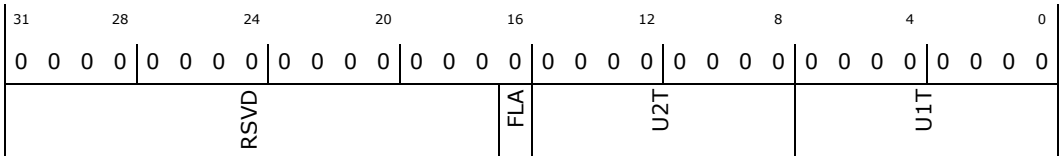
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 534h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
16	0x0 RW	**Force Link PM Accept (FLA):** Reserved. **Power Well:** SUS
15:8	0x0 RW/S	**U2 Timeout (U2T):** Reserved. **Power Well:** SUS
7:0	0x0 RW/S	**U1 Timeout (U1T):** Reserved. **Power Well:** SUS

7.4.53 USB3 Port Link Info (PORTLI12)—Offset 538h

Access Method

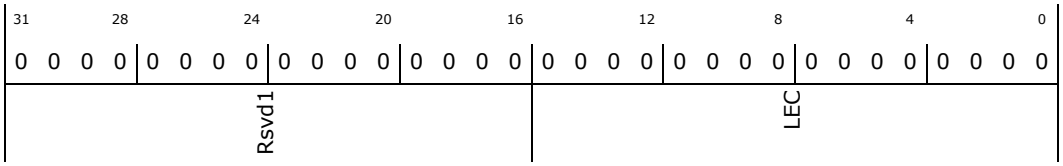
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 538h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RO	**Link Error Count (LEC):** Reserved. **Power Well:** Core

7.4.54 Port Status and Control USB3 (PORTSC13)—Offset 540h

Access Method

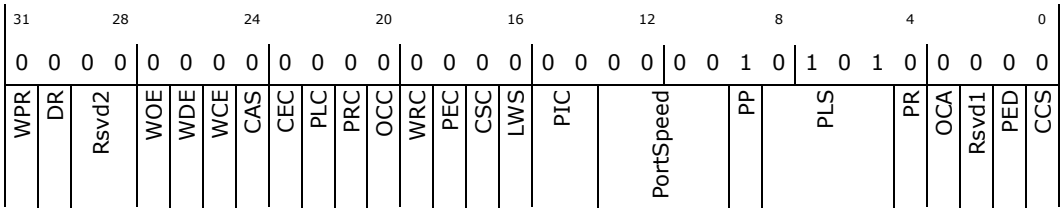
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 540h

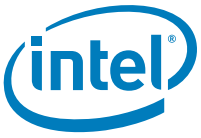
Op Codes:

h - Read, h - Write

Default: 000002A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1S	**Warm Port Reset (WPR):** Reserved. **Power Well:** SUS
30	0x0 RW/L	**Device Removable (DR):** Reserved. **Power Well:** Core
29:28	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
27	0x0 RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky. **Power Well:** SUS
26	0x0 RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky. **Power Well:** SUS
25	0x0 RW	**Wake on Connect Enable (WCE):** Note: This register is sticky. **Power Well:** SUS



Bit Range	Default & Access	Field Name (ID): Description
24	0x0 RO	**Cold Attach Status (CAS):** Reserved. **Power Well:** SUS
23	0x0 RW/C	**Port Config Error Change (CEC):** Note: This register is sticky. **Power Well:** SUS
22	0x0 RW/C	**Port Link State Change (PLC):** Note: This register is sticky. **Power Well:** SUS
21	0x0 RW/C	**Port Reset Change (PRC):** Note: This register is sticky. **Power Well:** SUS
20	0x0 RW/C	**Over-current Change (OCC):** Note: This register is sticky. **Power Well:** SUS
19	0x0 RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky. **Power Well:** SUS
18	0x0 RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky. **Power Well:** SUS
17	0x0 RW/C	**Connect Status Change (CSC):** Note: This register is sticky. **Power Well:** SUS
16	0x0 RW	**Port Link State Write Strobe (LWS):** Reserved. **Power Well:** SUS
15:14	0x0 RW	**Port Indicator Control (PIC):** Note: This register is sticky. **Power Well:** SUS
13:10	0x0 RW	**Port Speed (PortSpeed):** Note: This register is sticky. **Power Well:** SUS
9	0x1 RW	**Port Power (PP):** Note: This register is sticky. **Power Well:** SUS
8:5	0x5 RW	**Port Link State (PLS):** Note: This register is sticky. **Power Well:** SUS
4	0x0 RW/1S	**Port Reset (PR):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**Over-current Active (OCA):** Note: This register is sticky. **Power Well:** SUS
2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky. **Power Well:** SUS
0	0x0 RW	**Current Connect Status (CCS):** Note: This register is sticky. **Power Well:** SUS

7.4.55 Port Power Management Status and Control USB3 (PORTPMSC13)—Offset 544h

Access Method

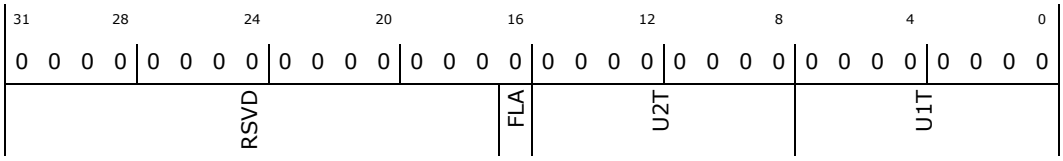
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 544h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
16	0x0 RW	**Force Link PM Accept (FLA):** Reserved. **Power Well:** SUS
15:8	0x0 RW/S	**U2 Timeout (U2T):** Reserved. **Power Well:** SUS
7:0	0x0 RW/S	**U1 Timeout (U1T):** Reserved. **Power Well:** SUS

7.4.56 USB3 Port Link Info (PORTLI13)—Offset 548h

Access Method

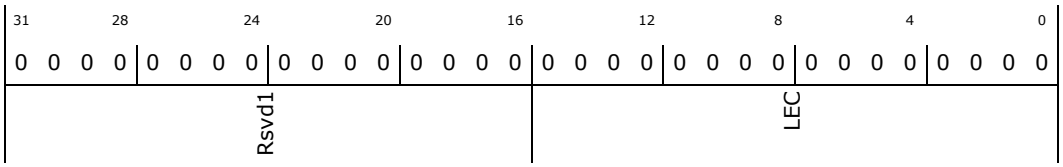
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 548h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RO	**Link Error Count (LEC):** Reserved. **Power Well:** Core

7.4.57 Microframe Index (RTMFINDEX)—Offset 2000h

Access Method

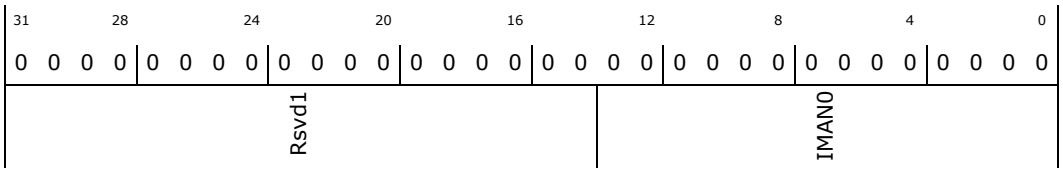
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2000h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
13:0	0x0 RO	**Microframe Index (IMAN0):** Reserved. **Power Well:** Core

7.4.58 Interrupter 1 Management (IMAN0)—Offset 2020h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

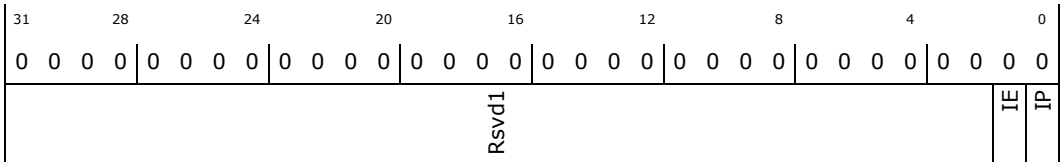
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2020h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0x0 RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

7.4.59 Interrupter 1 Moderation (IMOD0)—Offset 2024h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

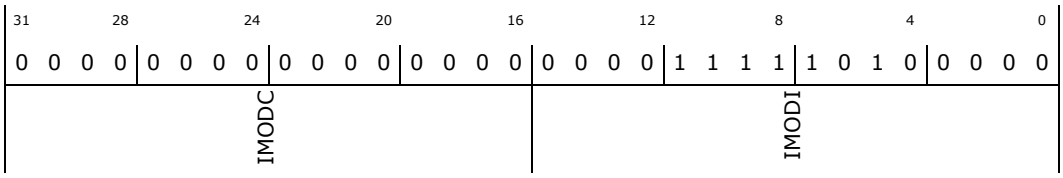
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2024h

Op Codes:

h - Read, h - Write

Default: 00000FA0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Interrupt Moderation Counter (IMODC):** Reserved. **Power Well:** Core
15:0	0xfa0 RW	**Interrupt Moderation Interval (IMODI):** Reserved. **Power Well:** Core

7.4.60 Event Ring Segment Table Size 1 (ERSTSZ0)—Offset 2028h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

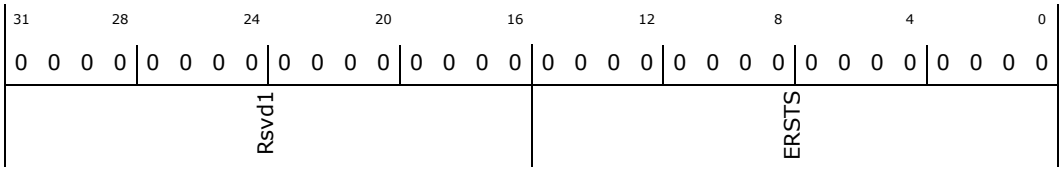
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2028h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RW	**Event Ring Segment Table Size (ERSTS):** Reserved. **Power Well:** Core

7.4.61 Event Ring Segment Table Base Address Low 1 (ERSTBA_LO0)—Offset 2030h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

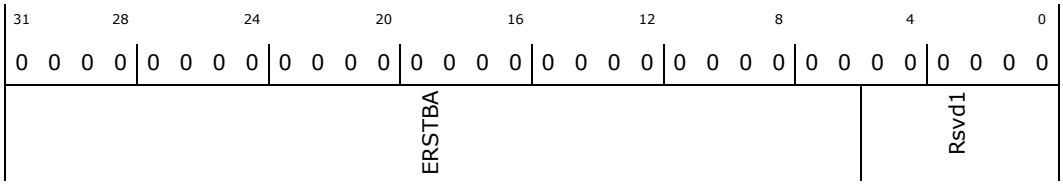
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2030h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Reserved. **Power Well:** Core
5:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

7.4.62 Event Ring Segment Table Base Address High 1 (ERSTBA_HI0)—Offset 2034h

Access Method

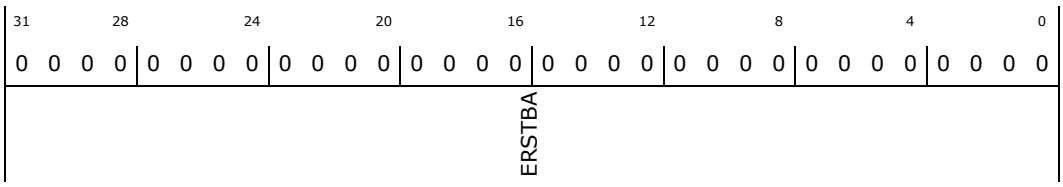
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2034h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Segment Table Base Address (ERSTBA):** Reserved. **Power Well:** Core

7.4.63 Event Ring Dequeue Pointer Low 1 (ERDP_LO0)—Offset 2038h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

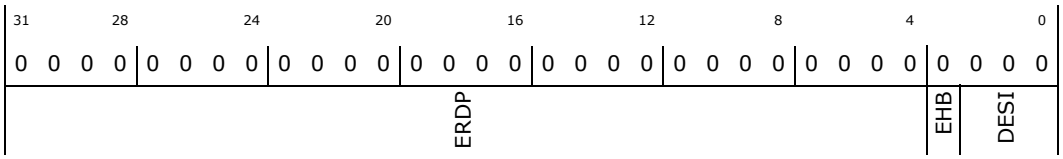
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2038h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core
3	0x0 RW/C	**Event Handler Busy (EHB):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Dequeue ERST Segment Index (DESI):** Reserved. **Power Well:** Core

7.4.64 Event Ring Dequeue Pointer High 1 (ERDP_HI0)—Offset 203Ch

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

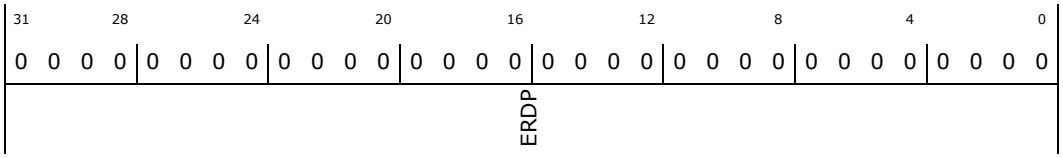
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 203Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

7.4.65 Interrupter 2 Management (IMAN1)—Offset 2040h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

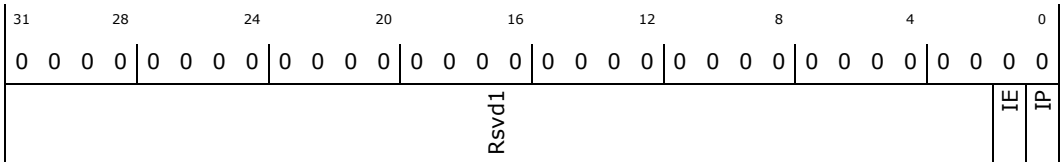
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2040h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0x0 RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

7.4.66 Interrupter 2 Moderation (IMOD1)—Offset 2044h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

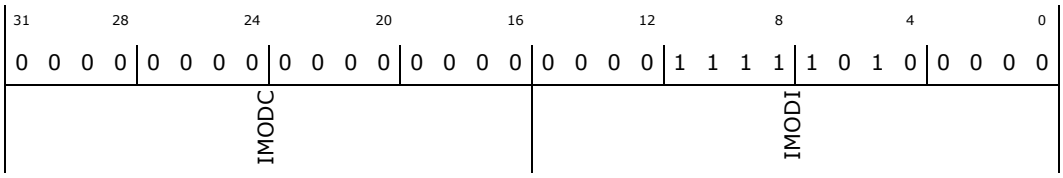
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2044h

Op Codes:

h - Read, h - Write

Default: 00000FA0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Interrupt Moderation Counter (IMODC):** Reserved. **Power Well:** Core
15:0	0xfa0 RW	**Interrupt Moderation Interval (IMODI):** Reserved. **Power Well:** Core

7.4.67 Event Ring Segment Table Size 2 (ERSTSZ1)—Offset 2048h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

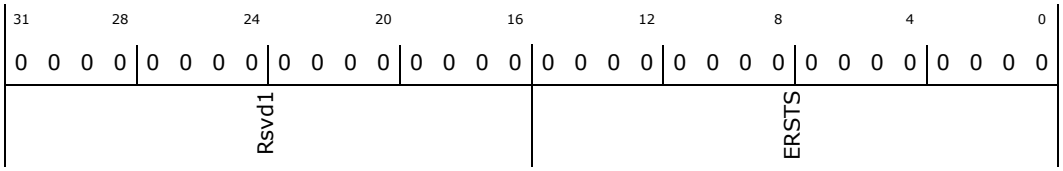
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2048h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RW	**Event Ring Segment Table Size (ERSTS):** Reserved. **Power Well:** Core

7.4.68 Event Ring Segment Table Base Address Low 2 (ERSTBA_LO1)—Offset 2050h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

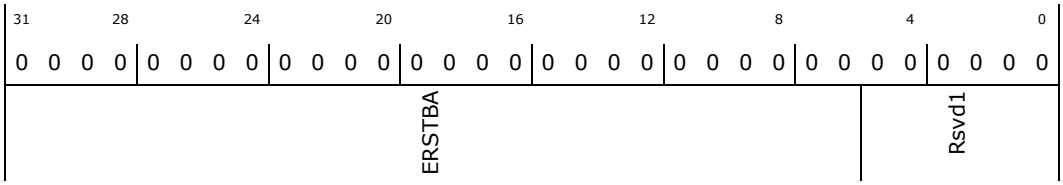
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2050h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Reserved. **Power Well:** Core
5:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

7.4.69 Event Ring Segment Table Base Address High 2 (ERSTBA_HI1)—Offset 2054h

Access Method

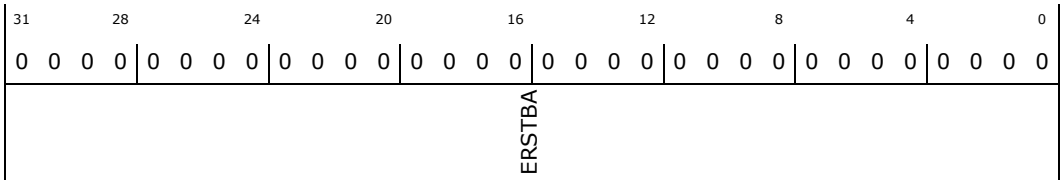
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2054h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Segment Table Base Address (ERSTBA):** Reserved. **Power Well:** Core

7.4.70 Event Ring Dequeue Pointer Low 2 (ERDP_LO1)—Offset 2058h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

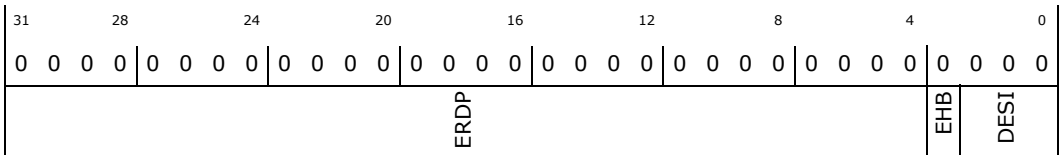
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2058h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core
3	0x0 RW/C	**Event Handler Busy (EHB):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Dequeue ERST Segment Index (DESI):** Reserved. **Power Well:** Core

7.4.71 Event Ring Dequeue Pointer High 2 (ERDP_HI1)—Offset 205Ch

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

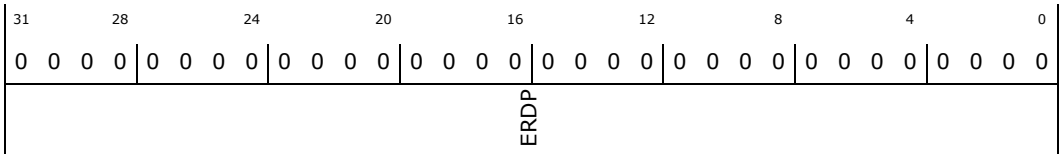
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 205Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

7.4.72 Interrupter 3 Management (IMAN2)—Offset 2060h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

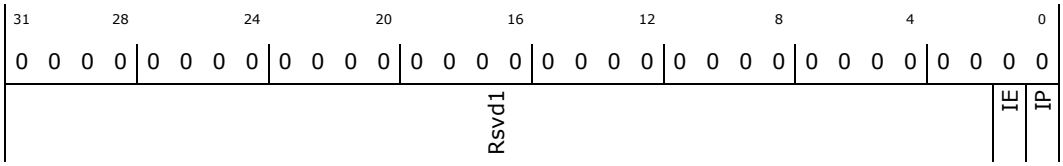
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2060h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0x0 RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

7.4.73 Interrupter 3 Moderation (IMOD2)—Offset 2064h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

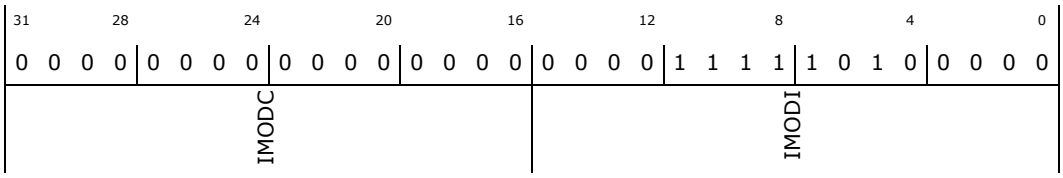
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2064h

Op Codes:

h - Read, h - Write

Default: 00000FA0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Interrupt Moderation Counter (IMODC):** Reserved. **Power Well:** Core
15:0	0xfa0 RW	**Interrupt Moderation Interval (IMODI):** Reserved. **Power Well:** Core

7.4.74 Event Ring Segment Table Size 3 (ERSTSZ2)—Offset 2068h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

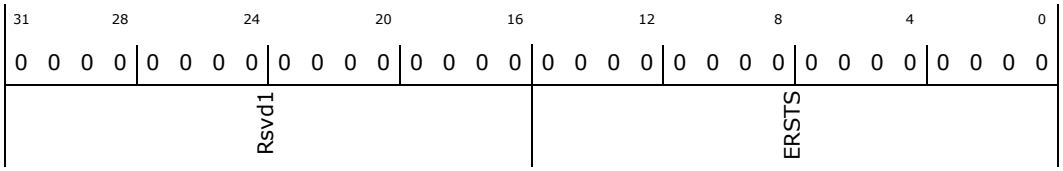
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2068h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RW	**Event Ring Segment Table Size (ERSTS):** Reserved. **Power Well:** Core

7.4.75 Event Ring Segment Table Base Address Low 3 (ERSTBA_LO2)—Offset 2070h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

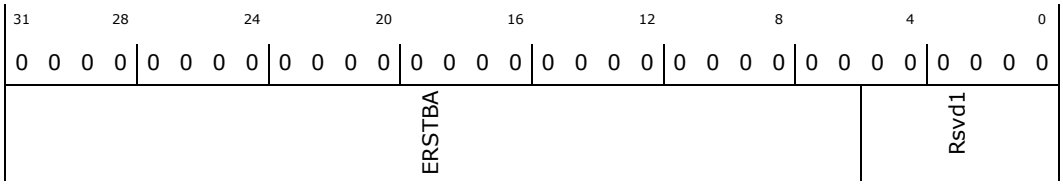
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2070h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Reserved. **Power Well:** Core
5:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

7.4.76 Event Ring Segment Table Base Address High 3 (ERSTBA_HI2)—Offset 2074h

Access Method

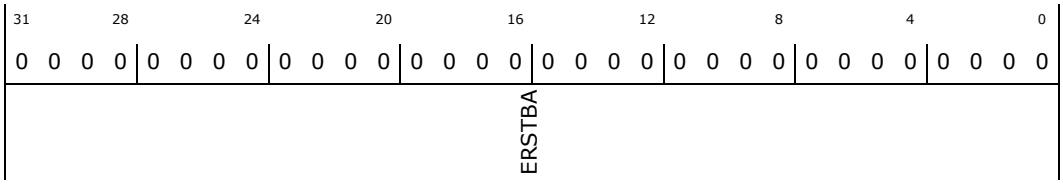
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2074h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Segment Table Base Address (ERSTBA):** Reserved. **Power Well:** Core

7.4.77 Event Ring Dequeue Pointer Low 3 (ERDP_LO2)—Offset 2078h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

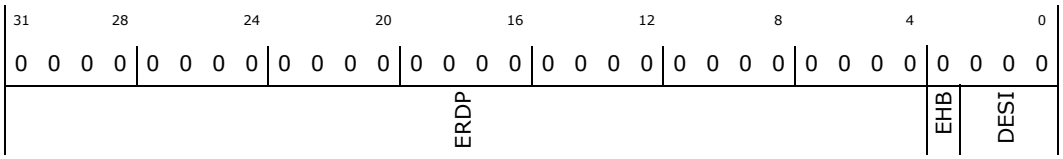
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2078h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core
3	0x0 RW/C	**Event Handler Busy (EHB):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Dequeue ERST Segment Index (DESI):** Reserved. **Power Well:** Core

7.4.78 Event Ring Dequeue Pointer High 3 (ERDP_HI2)—Offset 207Ch

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

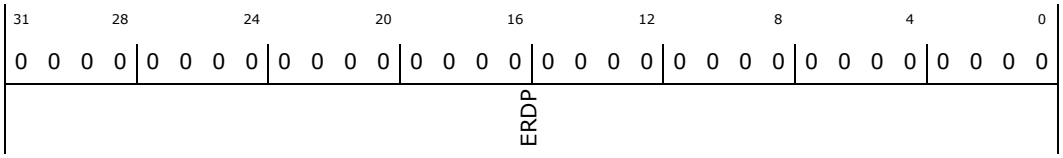
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 207Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

7.4.79 Interrupter 4 Management (IMAN3)—Offset 2080h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

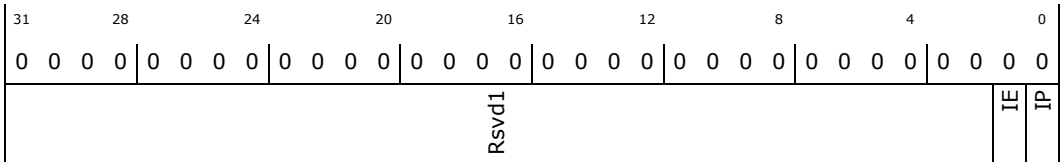
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2080h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0x0 RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

7.4.80 Interrupter 4 Moderation (IMOD3)—Offset 2084h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

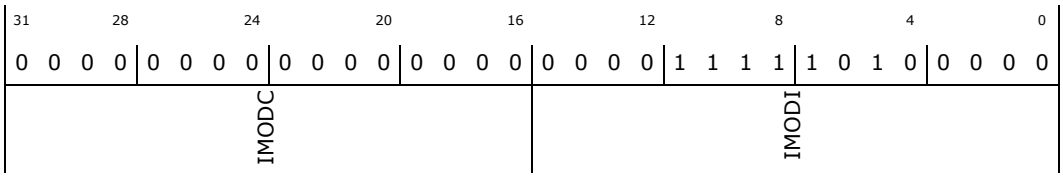
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2084h

Op Codes:

h - Read, h - Write

Default: 00000FA0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Interrupt Moderation Counter (IMODC):** Reserved. **Power Well:** Core
15:0	0xfa0 RW	**Interrupt Moderation Interval (IMODI):** Reserved. **Power Well:** Core

7.4.81 Event Ring Segment Table Size 4 (ERSTSZ3)—Offset 2088h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

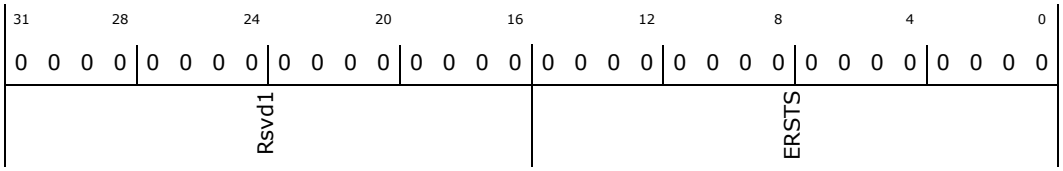
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2088h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RW	**Event Ring Segment Table Size (ERSTS):** Reserved. **Power Well:** Core

7.4.82 Event Ring Segment Table Base Address Low 4 (ERSTBA_LO3)—Offset 2090h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

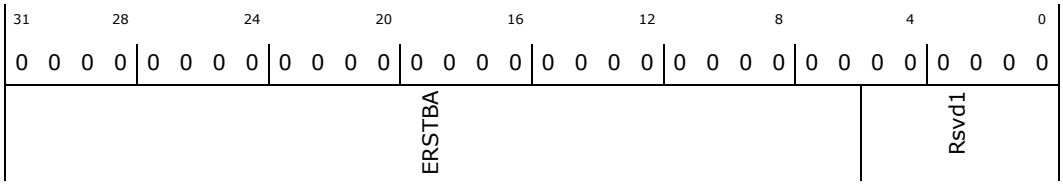
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2090h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Reserved. **Power Well:** Core
5:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

7.4.83 Event Ring Segment Table Base Address High 4 (ERSTBA_HI3)—Offset 2094h

Access Method

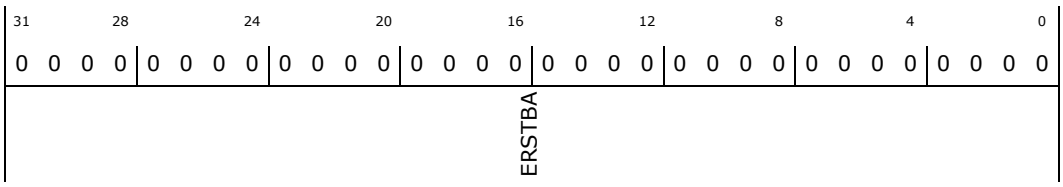
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2094h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Segment Table Base Address (ERSTBA):** Reserved. **Power Well:** Core

7.4.84 Event Ring Dequeue Pointer Low 4 (ERDP_LO3)—Offset 2098h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

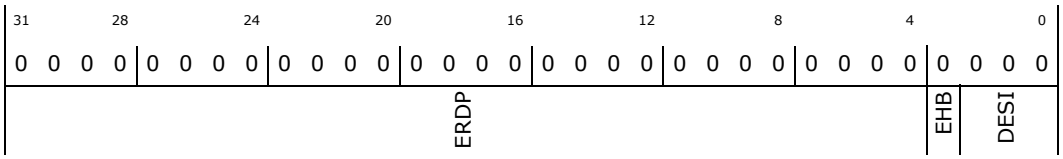
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2098h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core
3	0x0 RW/C	**Event Handler Busy (EHB):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Dequeue ERST Segment Index (DESI):** Reserved. **Power Well:** Core

7.4.85 Event Ring Dequeue Pointer High 4 (ERDP_HI3)—Offset 209Ch

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

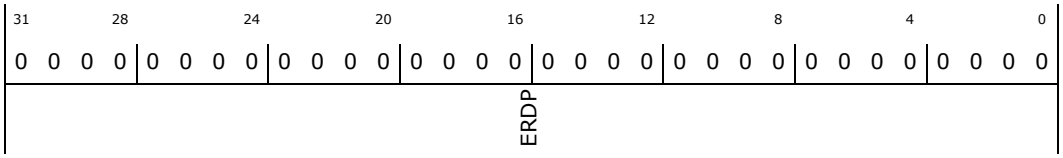
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 209Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

7.4.86 Interrupter 5 Management (IMAN4)—Offset 20A0h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

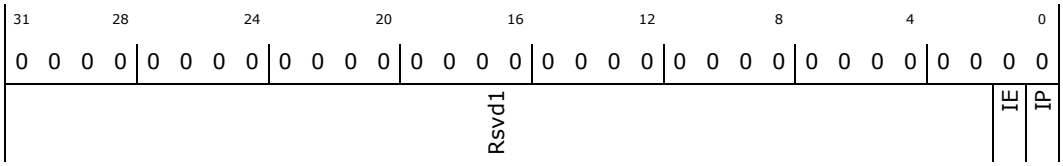
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20A0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0x0 RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

7.4.87 Interrupter 5 Moderation (IMOD4)—Offset 20A4h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

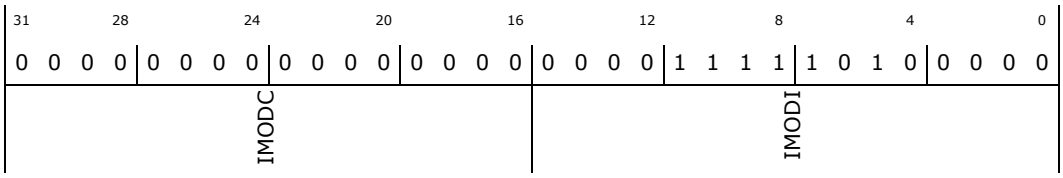
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20A4h

Op Codes:

h - Read, h - Write

Default: 00000FA0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Interrupt Moderation Counter (IMODC):** Reserved. **Power Well:** Core
15:0	0xfa0 RW	**Interrupt Moderation Interval (IMODI):** Reserved. **Power Well:** Core

7.4.88 Event Ring Segment Table Size 5 (ERSTSZ4)—Offset 20A8h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

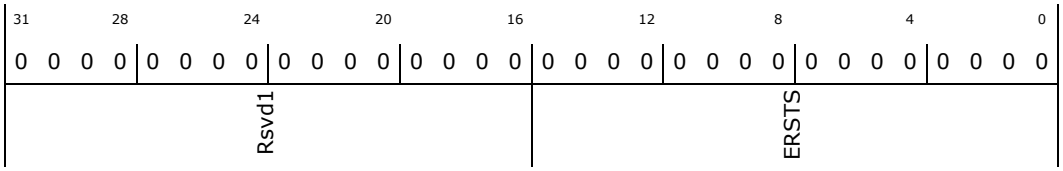
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20A8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RW	**Event Ring Segment Table Size (ERSTS):** Reserved. **Power Well:** Core

7.4.89 Event Ring Segment Table Base Address Low 5 (ERSTBA_LO4)—Offset 20B0h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

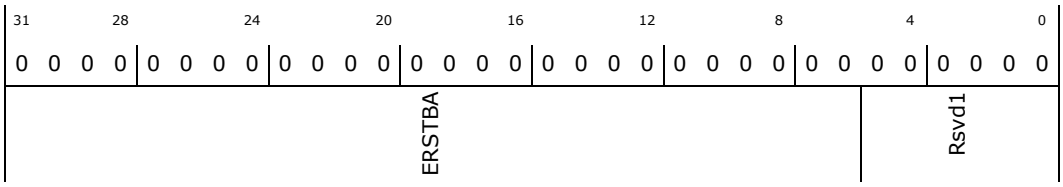
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20B0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Reserved. **Power Well:** Core
5:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

7.4.90 Event Ring Segment Table Base Address High 5 (ERSTBA_HI4)—Offset 20B4h

Access Method

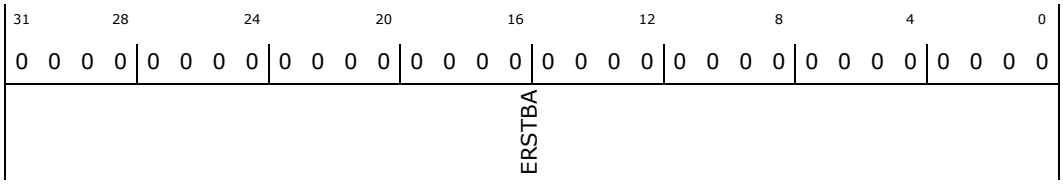
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20B4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Segment Table Base Address (ERSTBA):** Reserved. **Power Well:** Core

7.4.91 Event Ring Dequeue Pointer Low 5 (ERDP_LO4)—Offset 20B8h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

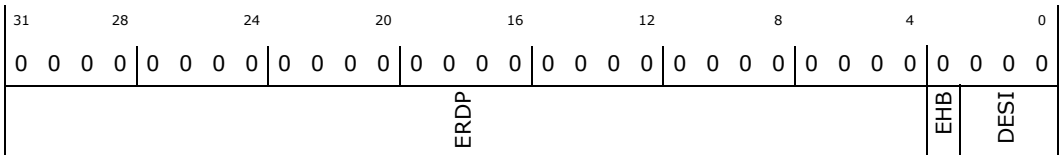
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20B8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core
3	0x0 RW/C	**Event Handler Busy (EHB):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Dequeue ERST Segment Index (DESI):** Reserved. **Power Well:** Core

7.4.92 Event Ring Dequeue Pointer High 5 (ERDP_HI4)—Offset 20BCh

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

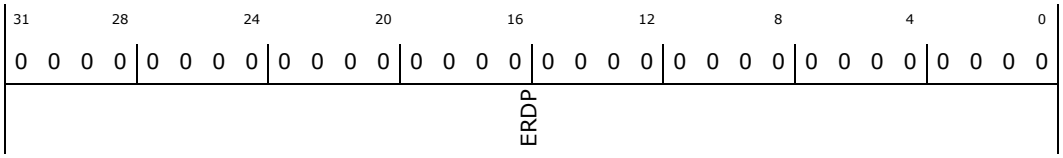
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20BCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

7.4.93 Interrupter 6 Management (IMAN5)—Offset 20C0h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

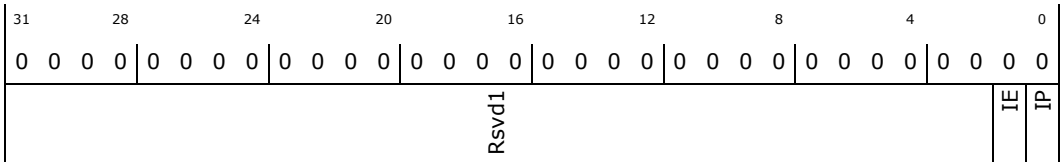
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20C0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0x0 RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

7.4.94 Interrupter 6 Moderation (IMOD5)—Offset 20C4h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

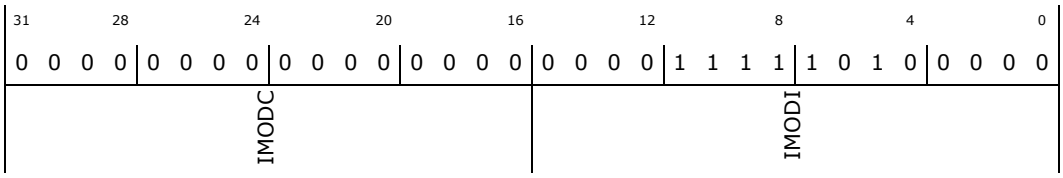
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20C4h

Op Codes:

h - Read, h - Write

Default: 00000FA0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Interrupt Moderation Counter (IMODC):** Reserved. **Power Well:** Core
15:0	0xfa0 RW	**Interrupt Moderation Interval (IMODI):** Reserved. **Power Well:** Core

7.4.95 Event Ring Segment Table Size 6 (ERSTSZ5)—Offset 20C8h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

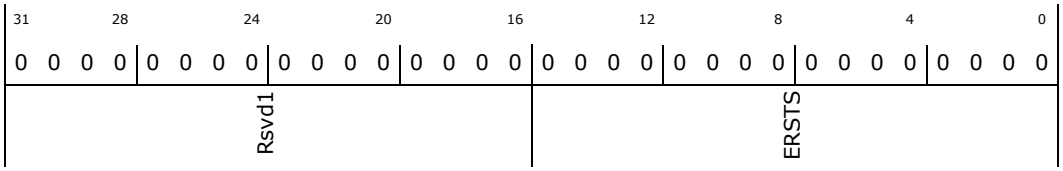
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20C8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RW	**Event Ring Segment Table Size (ERSTS):** Reserved. **Power Well:** Core

7.4.96 Event Ring Segment Table Base Address Low 6 (ERSTBA_LO5)—Offset 20D0h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

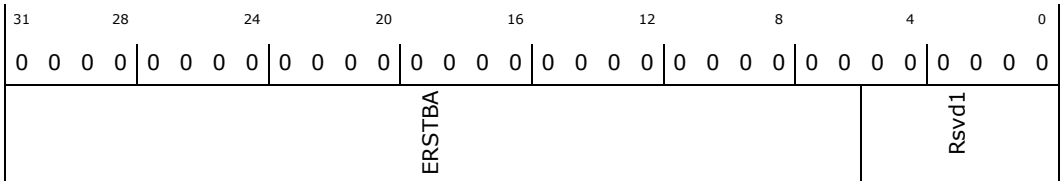
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20D0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Reserved. **Power Well:** Core
5:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

7.4.97 Event Ring Segment Table Base Address High 6 (ERSTBA_HI5)—Offset 20D4h

Access Method

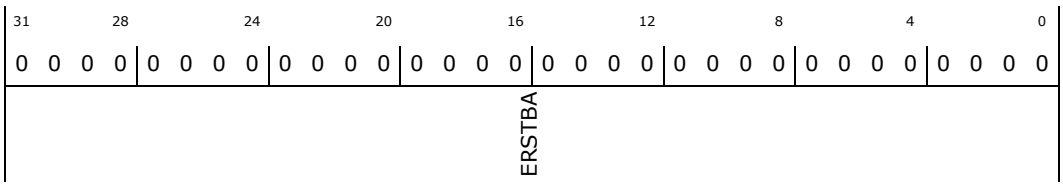
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20D4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Segment Table Base Address (ERSTBA):** Reserved. **Power Well:** Core

7.4.98 Event Ring Dequeue Pointer Low 6 (ERDP_LO5)—Offset 20D8h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

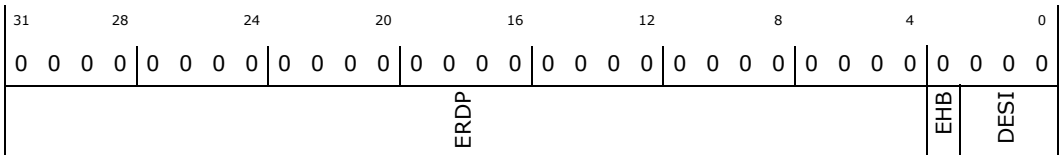
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20D8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core
3	0x0 RW/C	**Event Handler Busy (EHB):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Dequeue ERST Segment Index (DESI):** Reserved. **Power Well:** Core

7.4.99 Event Ring Dequeue Pointer High 6 (ERDP_HI5)—Offset 20DCh

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

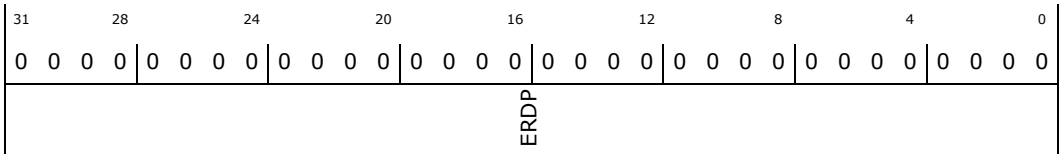
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20DCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

7.4.100 Interrupter 7 Management (IMAN6)—Offset 20E0h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

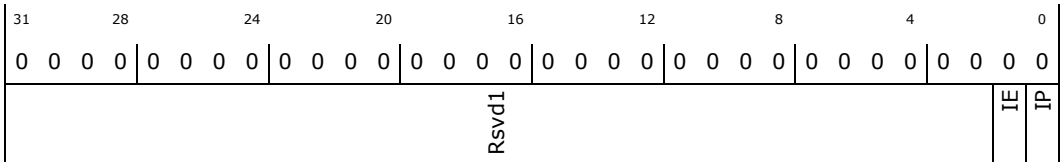
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20E0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0x0 RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

7.4.101 Interrupter 7 Moderation (IMOD6)—Offset 20E4h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

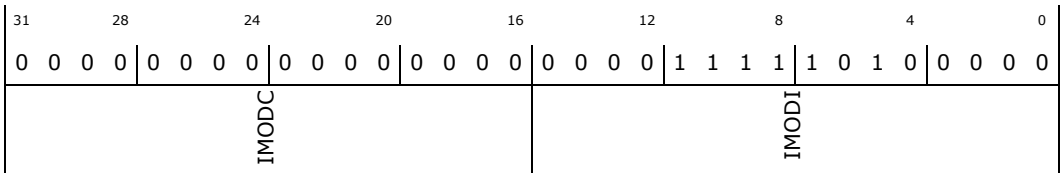
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20E4h

Op Codes:

h - Read, h - Write

Default: 00000FA0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Interrupt Moderation Counter (IMODC):** Reserved. **Power Well:** Core
15:0	0xfa0 RW	**Interrupt Moderation Interval (IMODI):** Reserved. **Power Well:** Core

7.4.102 Event Ring Segment Table Size 7 (ERSTSZ6)—Offset 20E8h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

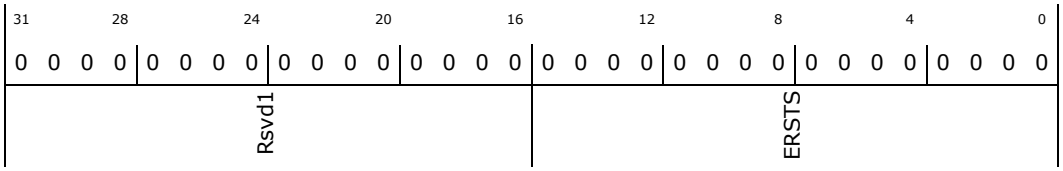
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20E8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RW	**Event Ring Segment Table Size (ERSTS):** Reserved. **Power Well:** Core

7.4.103 Event Ring Segment Table Base Address Low 7 (ERSTBA_LO6)—Offset 20F0h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

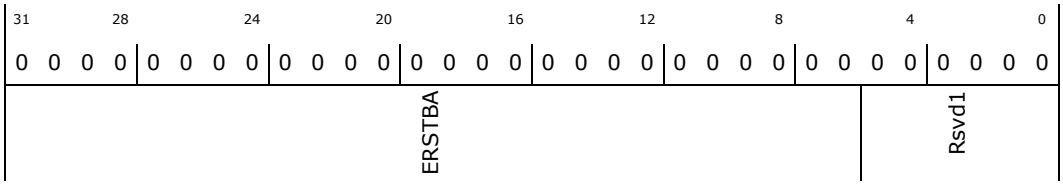
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20F0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Reserved. **Power Well:** Core
5:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

7.4.104 Event Ring Segment Table Base Address High 7 (ERSTBA_HI6)—Offset 20F4h

Access Method

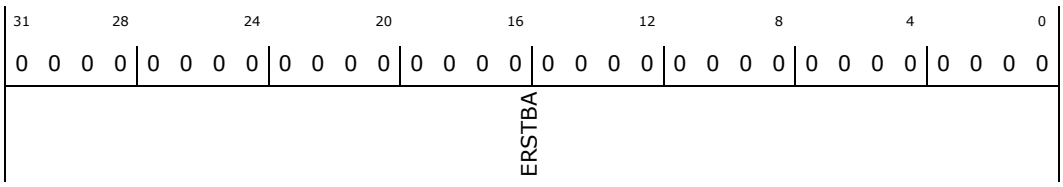
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20F4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Segment Table Base Address (ERSTBA):** Reserved. **Power Well:** Core

7.4.105 Event Ring Dequeue Pointer Low 7 (ERDP_LO6)—Offset 20F8h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

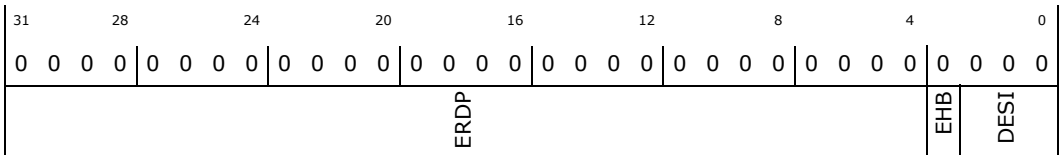
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20F8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core
3	0x0 RW/C	**Event Handler Busy (EHB):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Dequeue ERST Segment Index (DESI):** Reserved. **Power Well:** Core

7.4.106 Event Ring Dequeue Pointer High 7 (ERDP_HI6)—Offset 20FCh

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

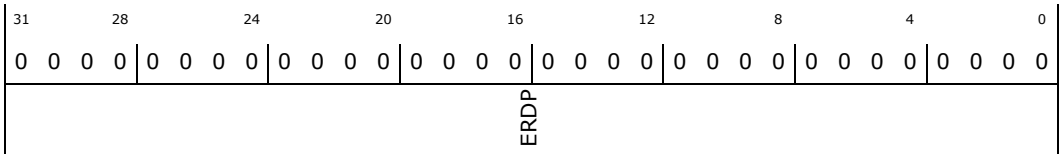
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 20FCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

7.4.107 Interrupter 8 Management (IMAN7)—Offset 2100h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

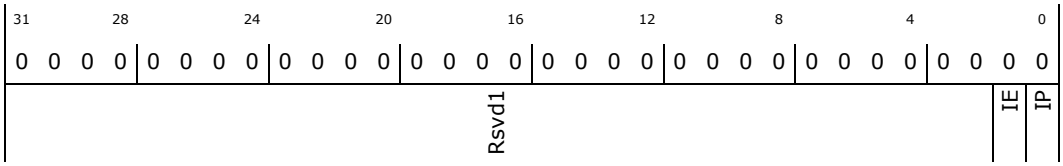
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2100h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
1	0x0 RW	**Interrupt Enable (IE):** Reserved. **Power Well:** Core
0	0x0 RW/C	**Interrupt Pending (IP):** Reserved. **Power Well:** Core

7.4.108 Interrupter 8 Moderation (IMOD7)—Offset 2104h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

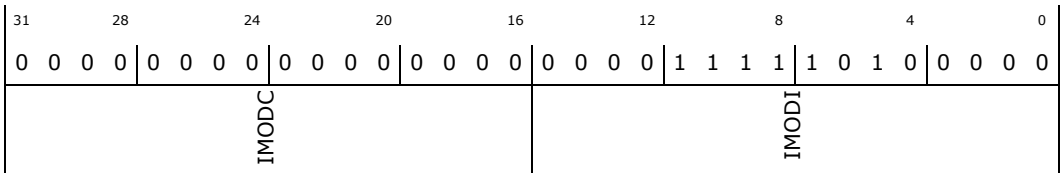
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2104h

Op Codes:

h - Read, h - Write

Default: 00000FA0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Interrupt Moderation Counter (IMODC):** Reserved. **Power Well:** Core
15:0	0xfa0 RW	**Interrupt Moderation Interval (IMODI):** Reserved. **Power Well:** Core

7.4.109 Event Ring Segment Table Size 8 (ERSTSZ7)—Offset 2108h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

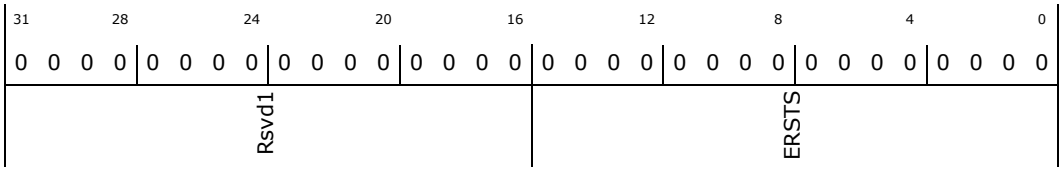
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2108h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
15:0	0x0 RW	**Event Ring Segment Table Size (ERSTS):** Reserved. **Power Well:** Core

7.4.110 Event Ring Segment Table Base Address Low 8 (ERSTBA_LO7)—Offset 2110h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

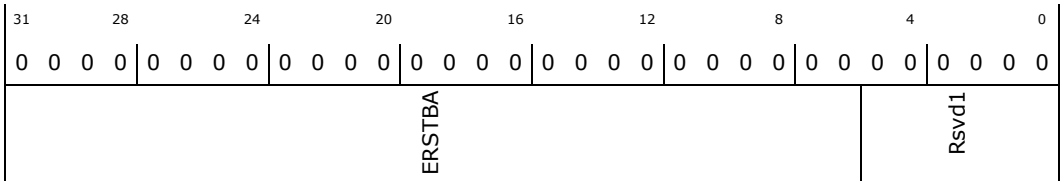
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2110h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**Event Ring Segment Table Base Address Register (ERSTBA):** Reserved. **Power Well:** Core
5:0	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core

7.4.111 Event Ring Segment Table Base Address High 8 (ERSTBA_HI7)—Offset 2114h

Access Method

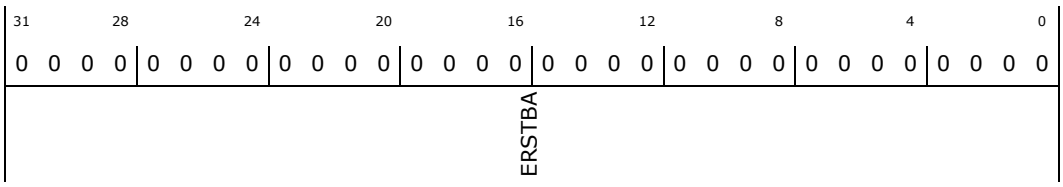
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2114h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Segment Table Base Address (ERSTBA):** Reserved. **Power Well:** Core

7.4.112 Event Ring Dequeue Pointer Low 8 (ERDP_LO7)—Offset 2118h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

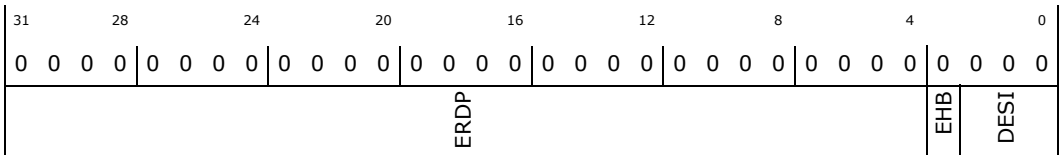
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 2118h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core
3	0x0 RW/C	**Event Handler Busy (EHB):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Dequeue ERST Segment Index (DESI):** Reserved. **Power Well:** Core

7.4.113 Event Ring Dequeue Pointer High 8 (ERDP_HI7)—Offset 211Ch

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

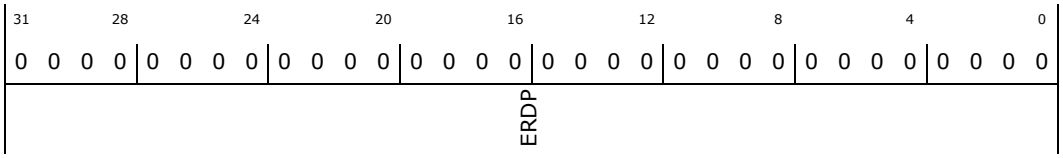
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 211Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Event Ring Dequeue Pointer (ERDP):** Reserved. **Power Well:** Core

7.4.114 Door Bell 1 (DB0)—Offset 3000h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

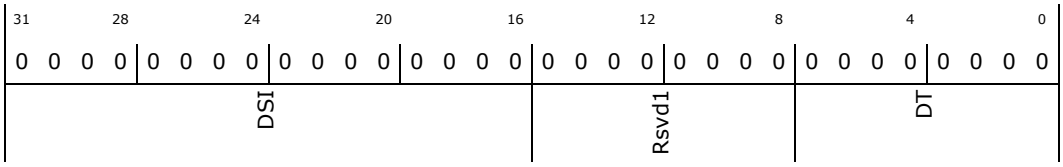
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3000h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.115 Door Bell 2 (DB1)—Offset 3004h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

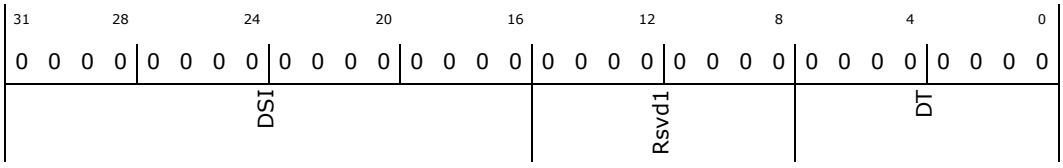
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3004h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.116 Door Bell 3 (DB2)—Offset 3008h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

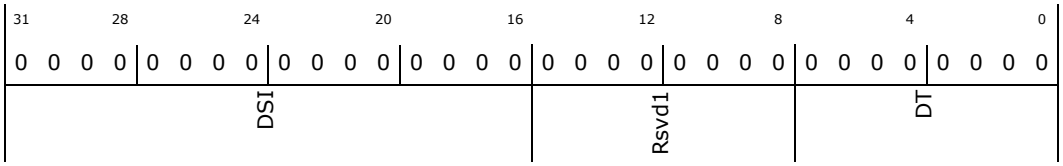
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3008h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.117 Door Bell 4 (DB3)—Offset 300Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

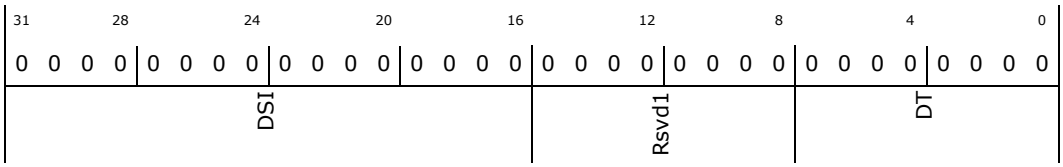
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 300Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.118 Door Bell 5 (DB4)—Offset 3010h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

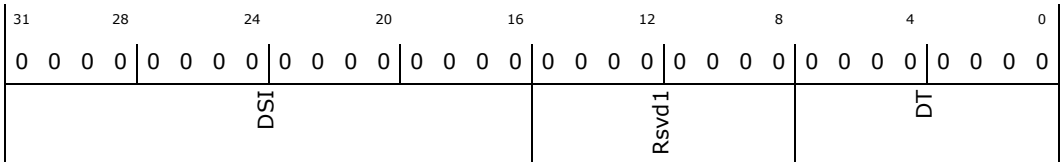
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3010h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.119 Door Bell 6 (DB5)—Offset 3014h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

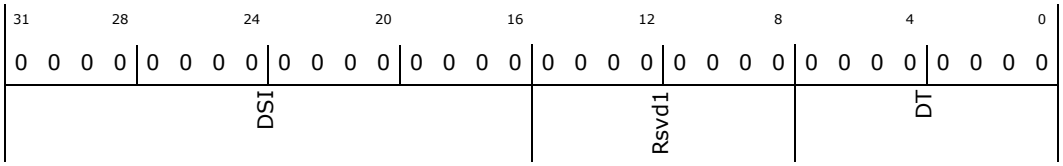
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3014h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.120 Door Bell 7 (DB6)—Offset 3018h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

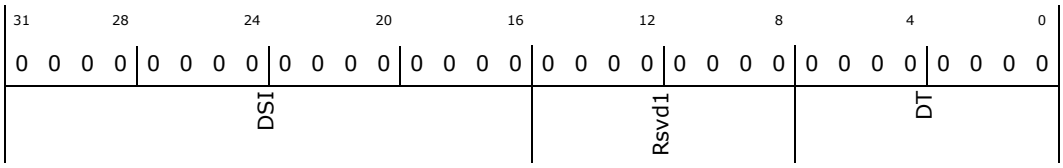
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3018h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.121 Door Bell 8 (DB7)—Offset 301Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

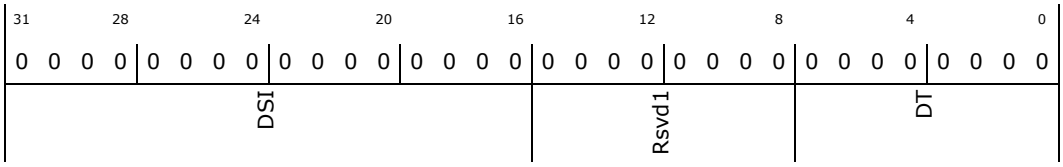
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 301Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.122 Door Bell 9 (DB8)—Offset 3020h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

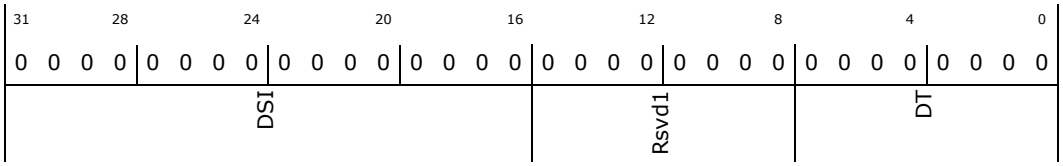
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3020h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.123 Door Bell 10 (DB9)—Offset 3024h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

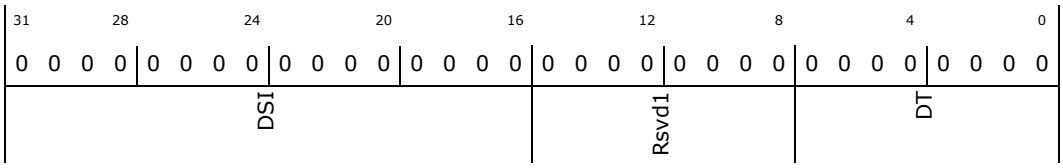
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3024h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.124 Door Bell 11 (DB10)—Offset 3028h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

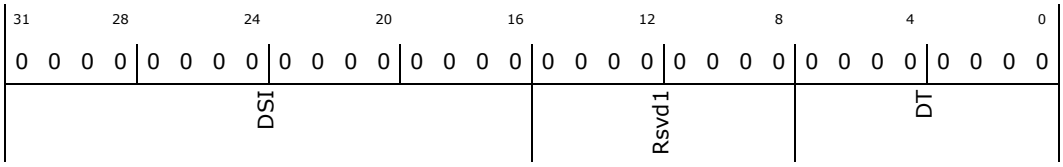
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3028h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.125 Door Bell 12 (DB11)—Offset 302Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

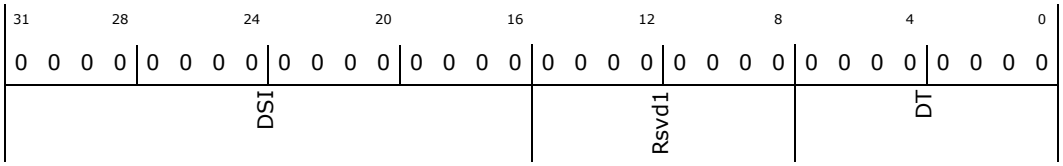
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 302Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.126 Door Bell 13 (DB12)—Offset 3030h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

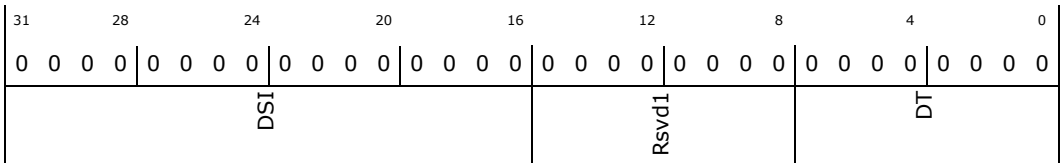
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3030h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.127 Door Bell 14 (DB13)—Offset 3034h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

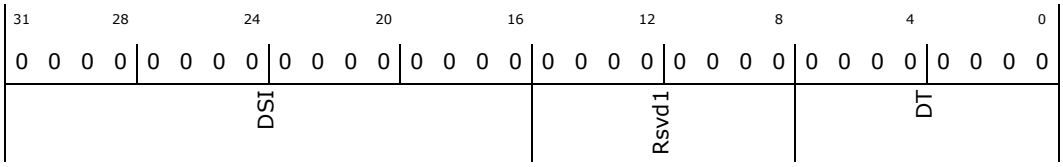
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3034h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.128 Door Bell 15 (DB14)—Offset 3038h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

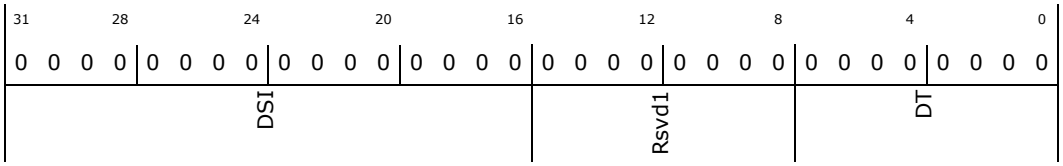
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3038h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.129 Door Bell 16 (DB15)—Offset 303Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

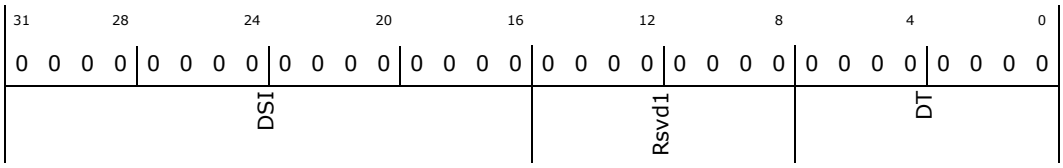
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 303Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.130 Door Bell 17 (DB16)—Offset 3040h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

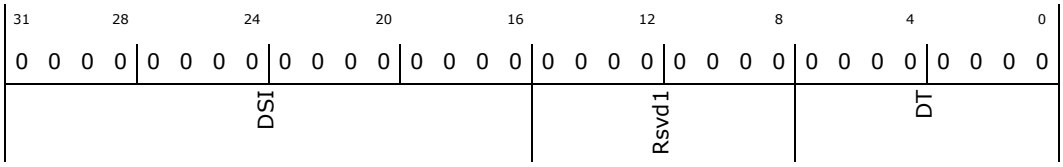
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3040h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.131 Door Bell 18 (DB17)—Offset 3044h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

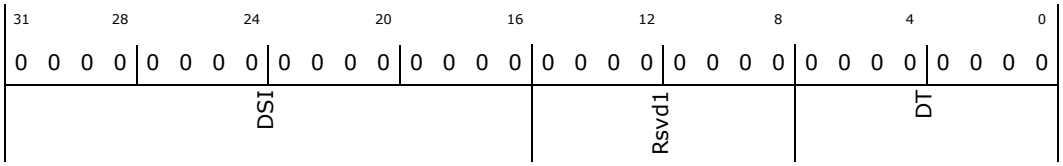
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3044h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.132 Door Bell 19 (DB18)—Offset 3048h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

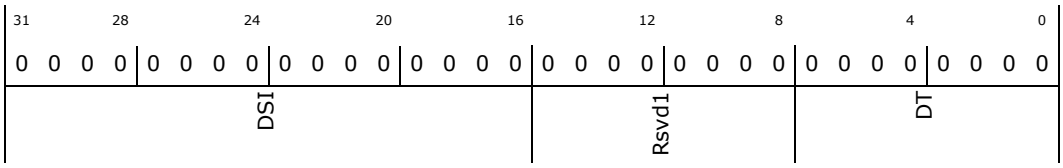
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3048h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.133 Door Bell 20 (DB19)—Offset 304Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

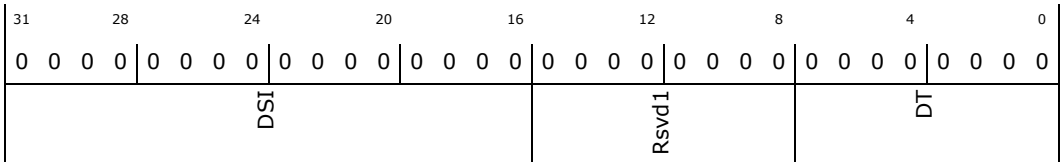
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 304Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.134 Door Bell 21 (DB20)—Offset 3050h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

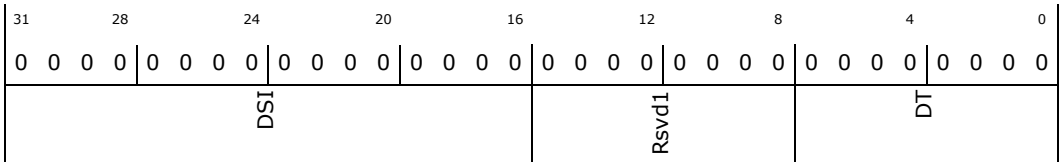
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3050h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.135 Door Bell 22 (DB21)—Offset 3054h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

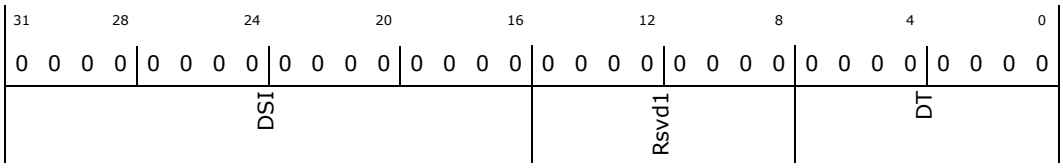
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3054h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.136 Door Bell 23 (DB22)—Offset 3058h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

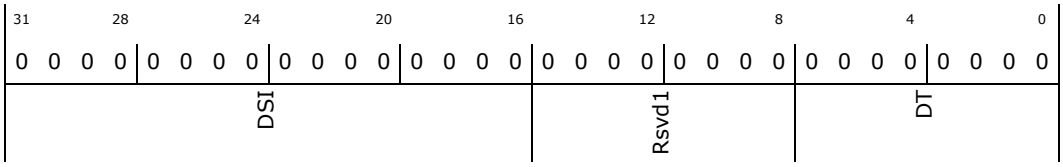
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3058h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.137 Door Bell 24 (DB23)—Offset 305Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

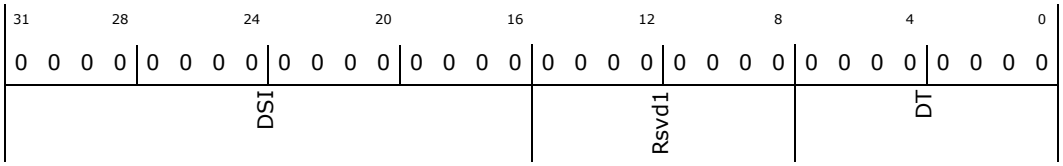
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 305Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.138 Door Bell 25 (DB24)—Offset 3060h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

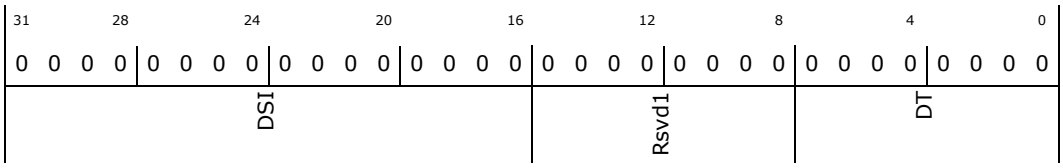
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3060h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.139 Door Bell 26 (DB25)—Offset 3064h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

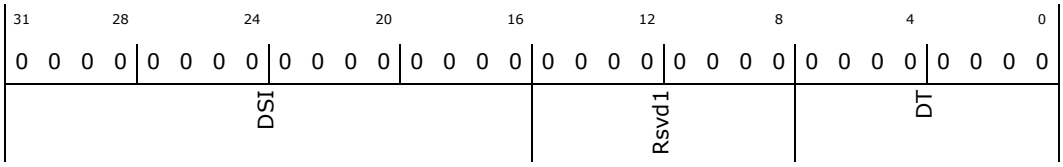
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3064h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.140 Door Bell 27 (DB26)—Offset 3068h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

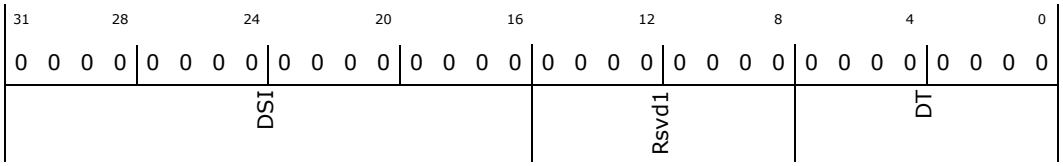
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3068h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.141 Door Bell 28 (DB27)—Offset 306Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

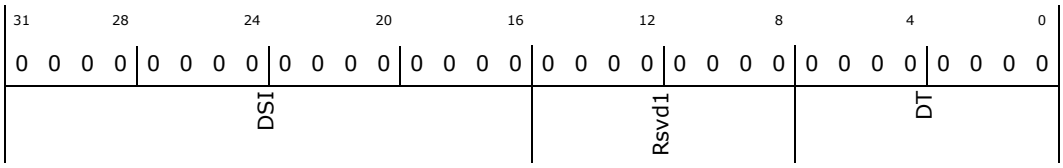
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 306Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.142 Door Bell 29 (DB28)—Offset 3070h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

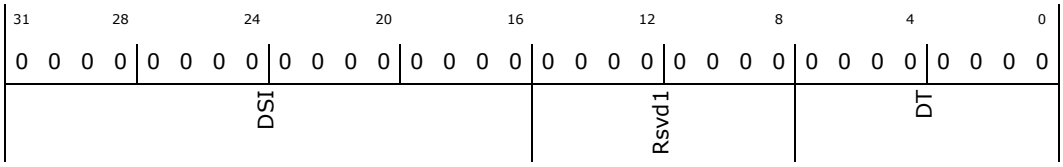
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3070h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.143 Door Bell 30 (DB29)—Offset 3074h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

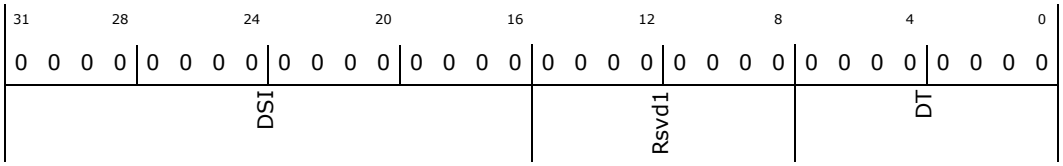
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3074h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.144 Door Bell 31 (DB30)—Offset 3078h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

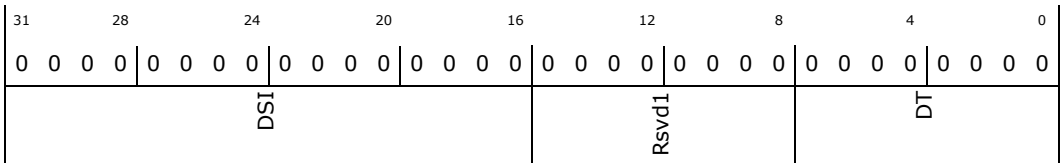
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3078h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.145 Door Bell 32 (DB31)—Offset 307Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

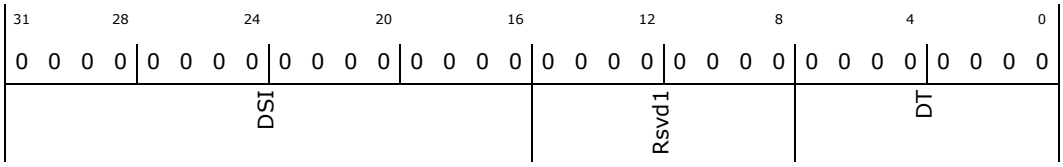
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 307Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.146 Door Bell 32 (DB32)—Offset 3080h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

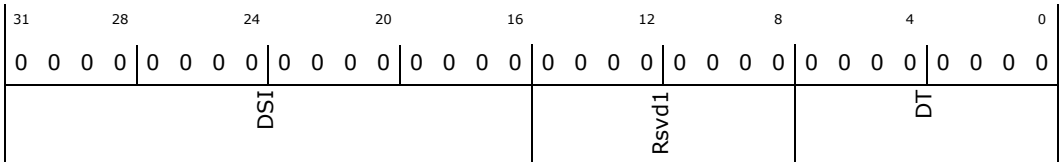
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 3080h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**DB Stream ID (DSI):** Reserved. **Power Well:** Core
15:8	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
7:0	0x0 RW	**DB Target (DT):** Reserved. **Power Well:** Core

7.4.147 XECP_SUPP_USB2_0—Offset 8000h

Access Method

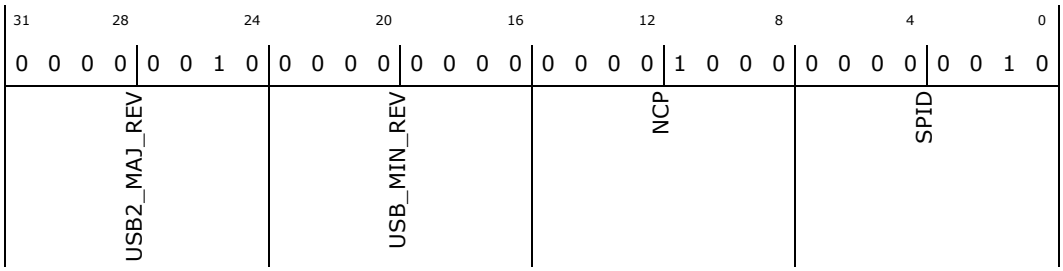
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8000h

Op Codes:

h - Read, h - Write

Default: 02000802h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x2 RO	**USB Major Revision: 2.0 (USB2_MAJ_REV):** Reserved. **Power Well:** Core
23:16	0x0 RO	**USB Minor Revision (USB_MIN_REV):** Reserved. **Power Well:** Core
15:8	0x8 RO	**Next Capability Pointer (NCP):** **Power Well:** Core
7:0	0x2 RO	**Supported Protocol ID (SPID):** Reserved. **Power Well:** Core

7.4.148 XECP_SUPP_USB2_1—Offset 8004h

Access Method

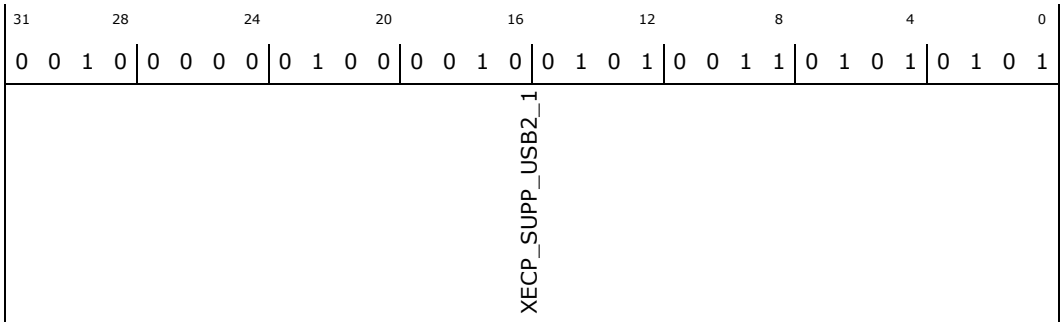
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8004h

Op Codes:

h - Read, h - Write

Default: 20425355h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x20425355 RO	**XECP_SUPP_USB2_1:** Namestring USB **Power Well:** Core

7.4.149 XECP_SUPP_USB2_2—Offset 8008h

Access Method

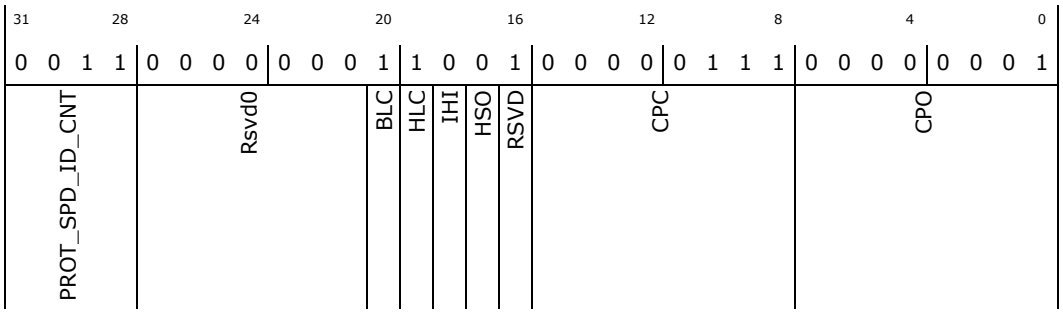
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8008h

Op Codes:

h - Read, h - Write

Default: 30190701h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x3 RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT):** 3 USB 2.0 Speed (High, Full, Low) **Power Well:** Core
27:21	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
20	0x1 RO	**BESL LPM Capability (BLC):** Bit is set to 1 to indicate that the the ports described by this xHCI Supported Protocol Capability will apply BESL timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMCC registers. **Power Well:** Core
19	0x1 RO	**Protocol Defined - Hardware LMP Capability (HLC):** Reserved. **Power Well:** Core
18	0x0 RO	**Protocol Defined - Integrated Hub Implementation (IHI):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
17	0x0 RO	**Protocol Defined - High SPeed Only (HSO):** Reserved. **Power Well:** Core
16	0x1 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
15:8	0x7 RO	**Compatible Port Count (CPC):** **Power Well:** Core
7:0	0x1 RO	**Compatible Port Offset (CPO):** Reserved. **Power Well:** Core

7.4.150 XECP_SUPP_USB2_3 (Full Speed) (XECP_SUPP_USB2_3)—Offset 8010h

Access Method

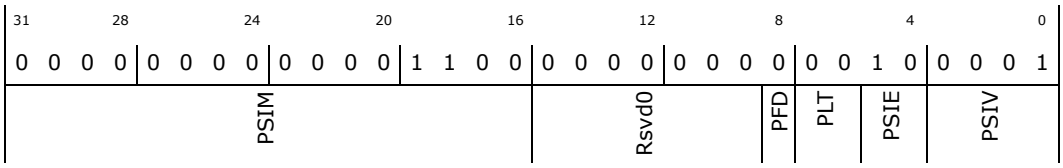
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8010h

Op Codes:

h - Read, h - Write

Default: 000C0021h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xc RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x0 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5:4	0x2 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x1 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

7.4.151 XECP_SUPP_USB2_4 (Low Speed) (XECP_SUPP_USB2_4)—Offset 8014h

Access Method

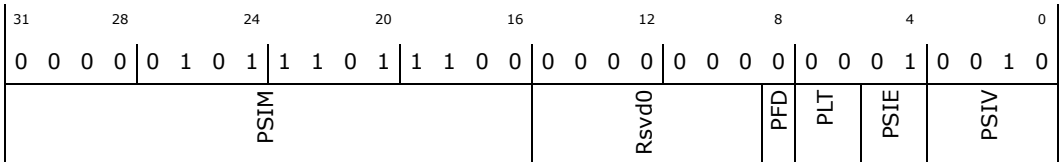
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8014h

Op Codes:

h - Read, h - Write

Default: 05DC0012h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x5dc RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x0 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	0x1 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x2 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

7.4.152 XECP_SUPP_USB2_5 (High Speed) (XECP_SUPP_USB2_5)—Offset 8018h

Access Method

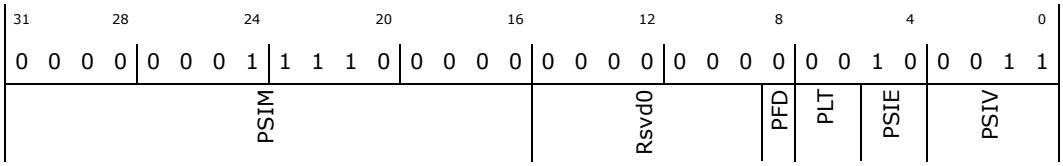
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8018h

Op Codes:

h - Read, h - Write

Default: 01E00023h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x1e0 RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x0 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	0x2 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x3 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

7.4.153 XECP_SUPP_USB3_0—Offset 8020h

Access Method

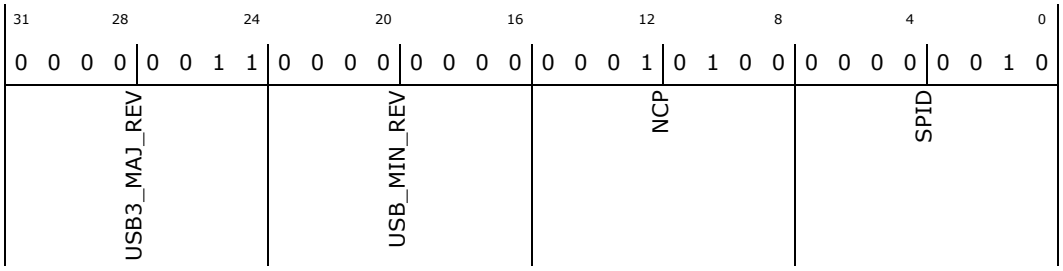
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8020h

Op Codes:

h - Read, h - Write

Default: 03001402h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x3 RO	**USB Major Revision: 3.0 (USB3_MAJ_REV):** Reserved. **Power Well:** Core
23:16	0x0 RO	**USB Minor Revision (USB_MIN_REV):** Reserved. **Power Well:** Core
15:8	0x14 RO	**Next Capability Pointer (NCP):** Reserved. **Power Well:** Core
7:0	0x2 RO	**Supported Protocol ID (SPID):** Reserved. **Power Well:** Core

7.4.154 XECP_SUPP_USB3_1—Offset 8024h

Access Method

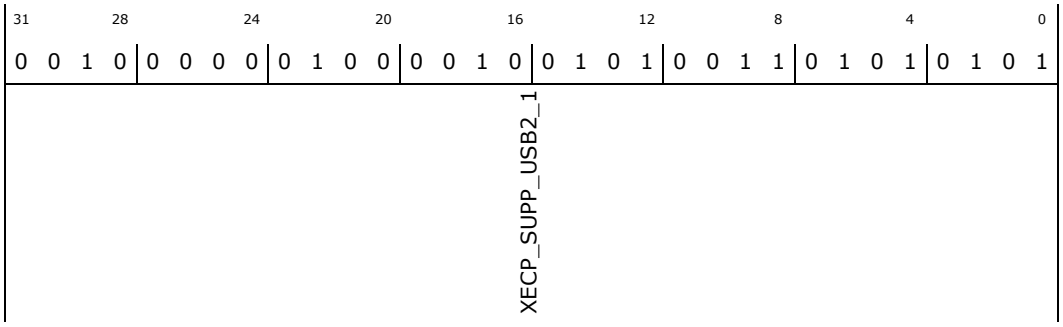
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8024h

Op Codes:

h - Read, h - Write

Default: 20425355h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x20425355 RO	**XECP_SUPP_USB2_1:** Namestring USB **Power Well:** Core

7.4.155 XECP_SUPP_USB3_2—Offset 8028h

Access Method

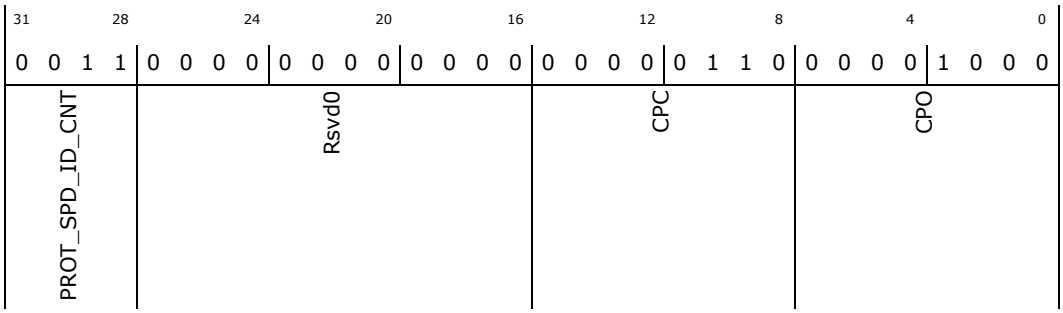
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8028h

Op Codes:

h - Read, h - Write

Default: 30000608h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x3 RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT):** 1 USB 3.0 Speed (Supper Speed) **Power Well:** Core
27:16	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
15:8	0x6 RO	**Compatible Port Count (CPC):** **Power Well:** Core
7:0	0x8 RO	**Compatible Port Offset (CPO):** Reserved. **Power Well:** Core

7.4.156 XECP_SUPP_USB3_3—Offset 8030h

Access Method

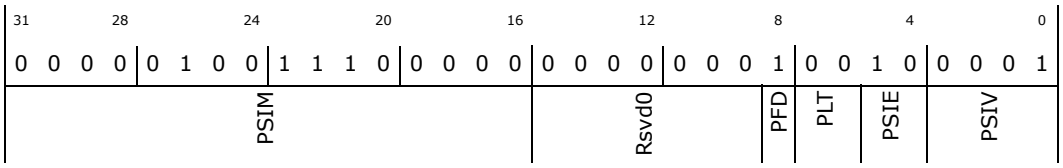
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8030h

Op Codes:

h - Read, h - Write

Default: 04E00121h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x4e0 RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x1 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	0x2 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x1 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

7.4.157 XECP_SUPP_USB3_4—Offset 8034h

Access Method

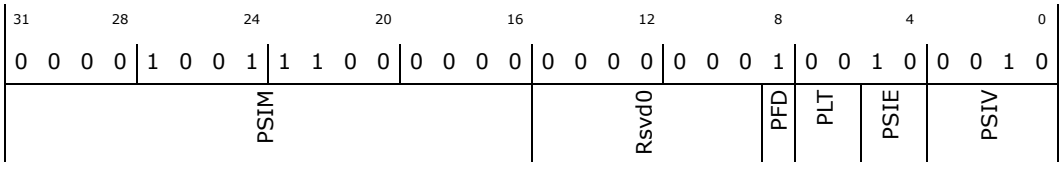
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8034h

Op Codes:

h - Read, h - Write

Default: 09C00122h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x9c0 RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x1 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	0x2 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x2 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

7.4.158 XECP_SUPP_USB3_5—Offset 8038h

Access Method

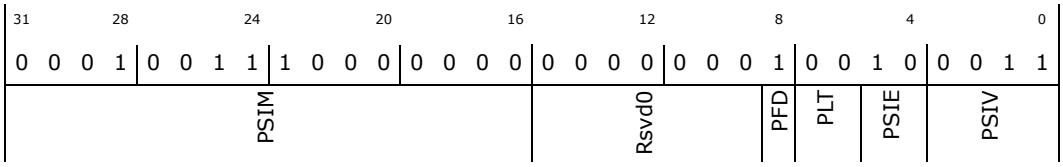
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8038h

Op Codes:

h - Read, h - Write

Default: 13800123h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x1380 RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
8	0x1 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	0x2 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x3 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

7.4.159 XECP_SUPP_USB3_6—Offset 803Ch

Access Method

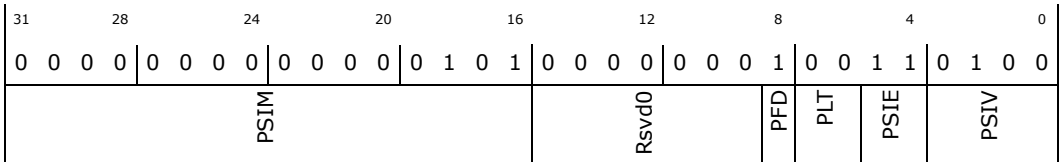
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 803Ch

Op Codes:

h - Read, h - Write

Default: 00050134h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x5 RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x1 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5:4	0x3 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x4 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

7.4.160 XECP_SUPP_USB3_7—Offset 8040h

Access Method

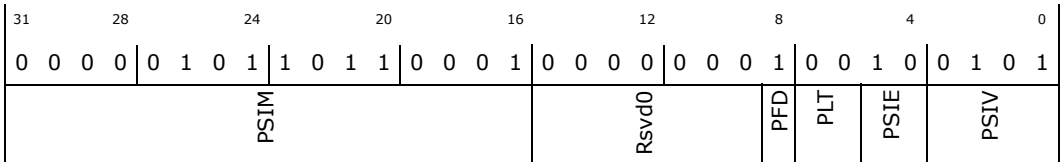
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8040h

Op Codes:

h - Read, h - Write

Default: 05B10125h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x5b1 RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x1 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	0x2 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x5 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

7.4.161 XECP_SUPP_USB3_8—Offset 8044h

Access Method

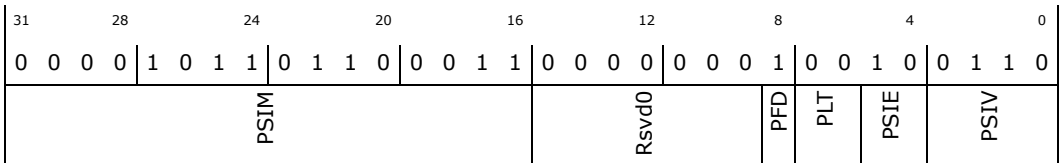
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8044h

Op Codes:

h - Read, h - Write

Default: 0B630126h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xb63 RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x1 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	0x2 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x6 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

7.4.162 XECP_SUPP_USB3_9—Offset 8048h

Access Method

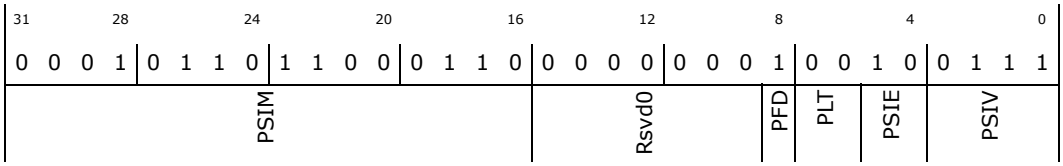
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8048h

Op Codes:

h - Read, h - Write

Default: 16C60127h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x16c6 RO	**Protocol Speed ID Mantissa (PSIM):** Reserved. **Power Well:** Core
15:9	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
8	0x1 RO	**PSI Full Duplex (PFD):** Reserved. **Power Well:** Core
7:6	0x0 RO	**PSI Type (PLT):** Reserved. **Power Well:** Core
5:4	0x2 RO	**Protocol Speed ID Exponent (PSIE):** Reserved. **Power Well:** Core
3:0	0x7 RO	**Protocol Speed ID Value (PSIV):** Reserved. **Power Well:** Core

7.4.163 Host Controller Capability (HOST_CTRL_CAP_REG)—Offset 8070h

This is a register that describe the host controller the extended cap location. It includes the , XECP_HOST_NEXT_CAP_OFFSET and VEND_DEF_HOST_CAP_ID_192. This register is not subject to HW save and restore.

Access Method

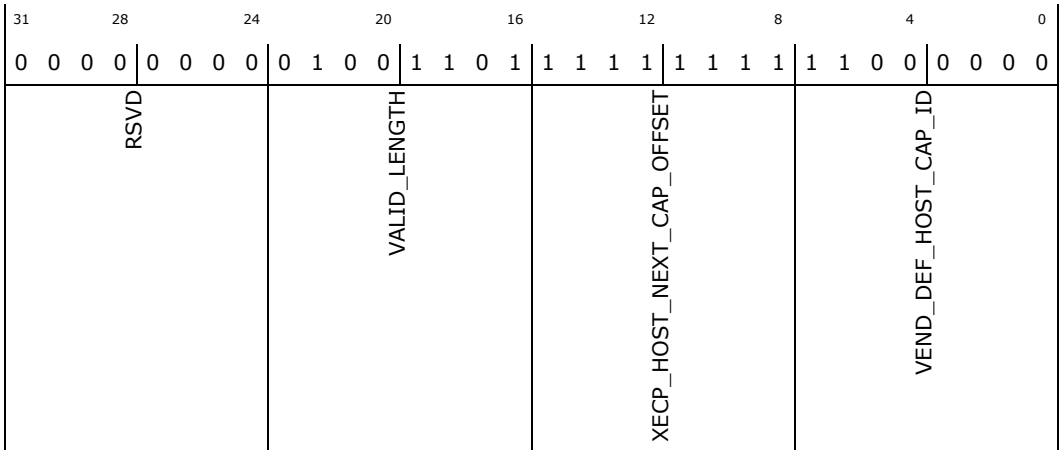
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8070h

Op Codes:

h - Read, h - Write

Default: 004DFFC0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
23:16	0x4d RO	**Valid Length (VALID_LENGTH):** Indicates the number of valid DWords in the capability, that need to be saved and restored This value needs to be updated as new chicken bit registers are added. 47h -) 818Bh is the last valid byte **Power Well:** Core
15:8	0xff RO	**Next Capability Pointer (XECP_HOST_NEXT_CAP_OFFSET):** Reserved. **Power Well:** Core
7:0	0xc0 RO	**Supported Protocol ID (VEND_DEF_HOST_CAP_ID):** Reserved. **Power Well:** Core

7.4.164 Override EP Flow Control (HOST_CLR_MASK_REG)—Offset 8078h

Access Method

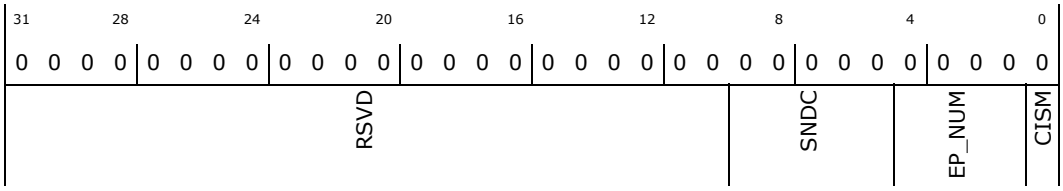
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8078h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
9:5	0x0 RW	**Slot Number Default Config (SNDC):** 5bits of slot number as a default configuration. It can scale to max of 128 slots **Power Well:** Core
4:1	0x0 RW	**EP Number (EP_NUM):** 4bits of EP number **Power Well:** Core
0	0x0 RW	**Clear Internal Scheduler's Mask (CISM):** This is a register that is used to clear the internal scheduler's mask that is used to stop scheduling a particular EP. Bit0 indicates the direction of the EP **Power Well:** Core

7.4.165 Clear Active IN EP ID Control (HOST_CLR_IN_EP_VALID_REG)—Offset 807Ch

Access Method

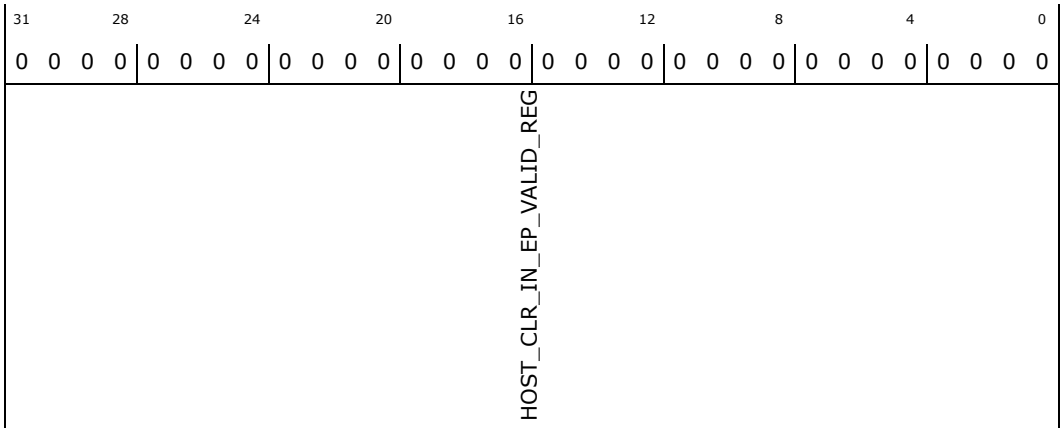
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 807Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Clear Active IN EP ID Control (HOST_CLR_IN_EP_VALID_REG):** This register is used to clear the internal valid IN EP array that TRM stored in order to guarantee one IN EP per port. This register allows software to clear the valid bit of each port IN EP. This field indicates the port number. For a 2port configuration, only bit1:0 are valid. It can scale for the max number of ports that we support. **Power Well:** Core

7.4.166 Clear Poll Mask Control (HOST_CLR_PMASK_REG)—Offset 8080h

Access Method

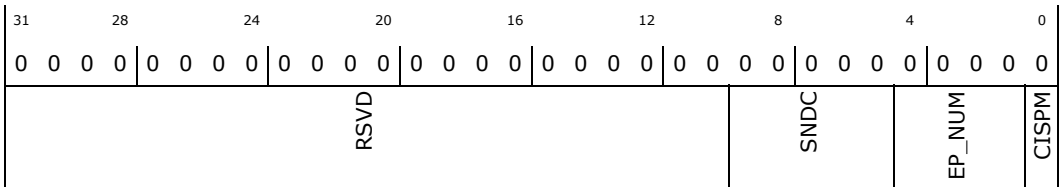
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8080h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
9:5	0x0 RW	**Slot Number Default Config (SNDC):** 5bits of slot number as a default configuration. It can scale to max of 128 slots **Power Well:** Core
4:1	0x0 RW	**EP Number (EP_NUM):** 4bits of EP number **Power Well:** Core
0	0x0 RW	**Clear Internal Scheduler's Poll Mask (CISPM):** This is a register that is used to clear the internal scheduler's poll mask that is used to indicate whether we need to poll this EP. This is used for USB2. Bit0 indicates the direction of the EP **Power Well:** Core

7.4.167 Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h

Access Method

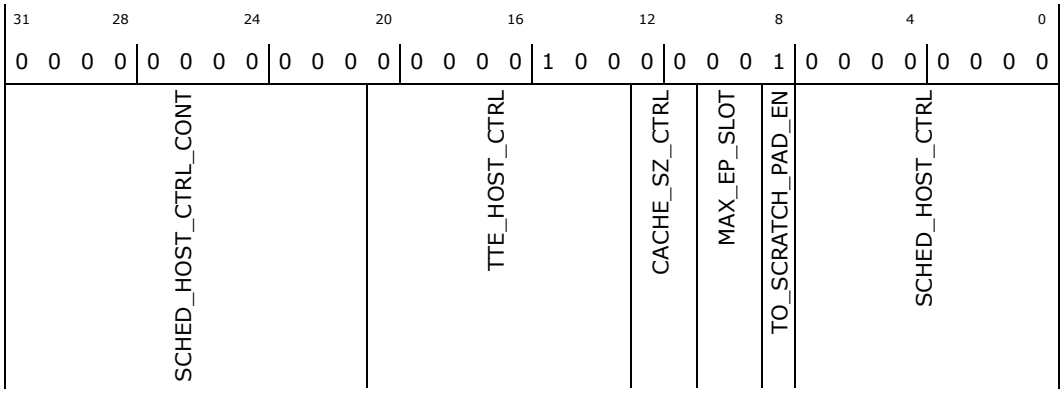
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8094h

Op Codes:

h - Read, h - Write

Default: 00008100h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RW	**Scheduler Host Control Reg Cont (SCHED_HOST_CTRL_CONT):** method of USB2 port periodic done check (off by default) **Power Well:** Core
20:13	0x4 RW	**TTE Host Control (TTE_HOST_CTRL):** (0): disable interrupt complete split limit to 3 microframes (1): disable checking of missed microframes (2): disable split error request w/NULL pointer on speculative INs with data payload and no TRB. (3): disable deferred split error request on speculative IN with data payload and no TRB. (7:4): reserved **Power Well:** Core
12:11	0x0 RW	**Cache Size Control Reg (CACHE_SZ_CTRL):** 0: 64 1: 32 2,3: 16 **Power Well:** Core
10:9	0x0 RW	**Maximum EP Per Slot (MAX_EP_SLOT):** 0: 32 1: 16 2: 8 3: 4 **Power Well:** Core
8	0x1 RW	**Turn on scratch_pad_en (TO_SCRATCH_PAD_EN):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**Scheduler Host Control Reg (SCHED_HOST_CTRL):** (0): disable poll delay (1): disable TRM active in EP valid check (2): enable TTE overlap prevention on interrupt IN EPs (at cost of possible service interval slip) (3) enable TTE overlap prevention on interrupt OUT EPs (at cost of possible service interval slip) (5:4) scheduler sort pattern 00 (default) search ISO ahead of interrupt within each service interval 01 - search USB2-ISO, USB3-ISO, USB2-Interrupt, USB3-Interrupt within each service interval 10 - search strictly by interval 11 - search all ISO intervals ahead interrupt intervals and within each interval, USB2 ahead of USB3 (6): disable 1 pack scheduling limit when ISO pending in present microframe (7): enable check to stop scheduling on port that are not connected **Power Well:** Core

7.4.168 Global Port Control (HOST_CTRL_PORT_CTRL)—Offset 80A0h

Access Method

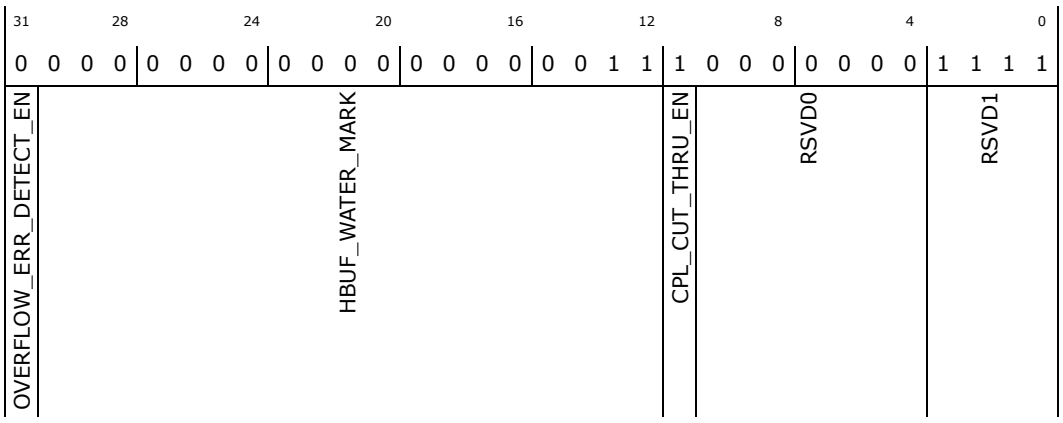
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80A0h

Op Codes:

h - Read, h - Write

Default: 0000380Fh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**OVERFLOW ERROR DETECTION ENABLE (OVERFLOW_ERR_DETECT_EN):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
30:12	0x3 RW	**HBUF_WATER_MARK:** Reserved. **Power Well:** Core
11	0x1 RW	**CPL Cut Thru Enable (CPL_CUT_THRU_EN):** Reserved. **Power Well:** Core
10:4	0x0 RW	**RESERVED (RSVD0):** Reserved. **Power Well:** Core
3:0	0xf RW	**RESERVED (RSVD1):** Reserved. **Power Well:** Core

7.4.169 Power Management Control (PMCTRL_REG)—Offset 80A4h

Access Method

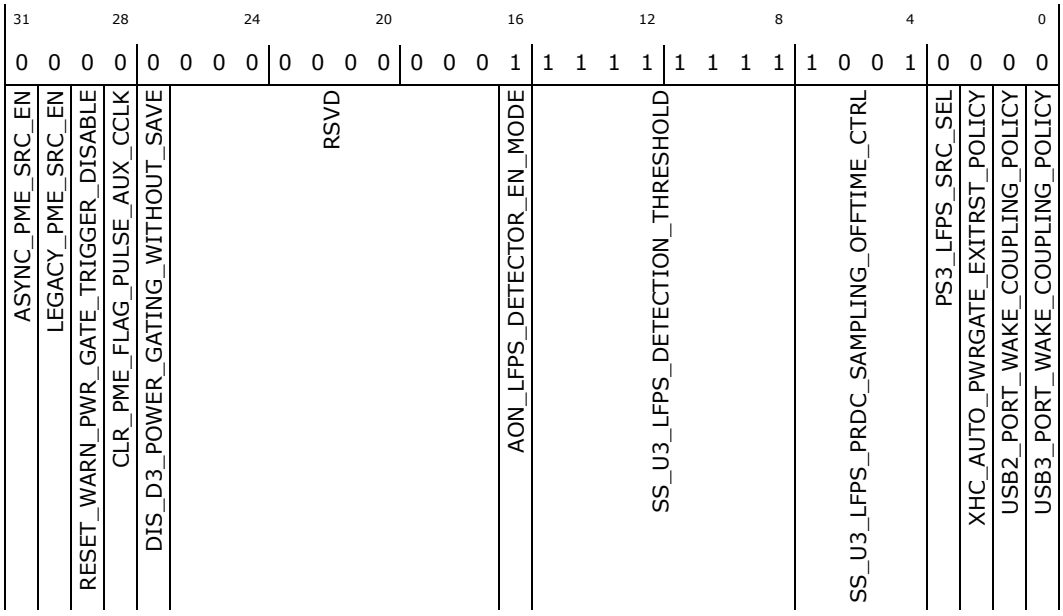
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80A4h

Op Codes:

h - Read, h - Write

Default: 0001FF90h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Async PME Source Enable (ASYNC_PME_SRC_EN):** This field allows the async PME source to be allowed to generate PME. This is specifically required for SOCs that do not allow for any clock other than RTC to be available during RTD3. **Power Well:** SUS
30	0x0 RW	**Legacy PME Source Enable (LEGACY_PME_SRC_EN):** This field allows the legacy PME source to be used in PME generation. The legacy source in in reference to the source prior to the RTD3 changes. **Power Well:** SUS
29	0x0 RW	**Reset Warn Power Gate Trigger Disable (RESET_WARN_PWR_GATE_TRIGGER_DISABLE):** This field controls the actions taken for due to reset warn. 0 - Reset Warn will trigger a HW autonomous Power Gate 1 - Reset Warn will not trigger a HW autonomous Power Gate **Power Well:** SUS
28	0x0 RW	**CLR_PME_FLAG_PULSE_AUX_CCLK:** Reserved. **Power Well:** SUS
27	0x0 RW	**DIS_D3_POWER_GATING_WITHOUT_SAVE:** Disable D3 Power Gating Without Save 0 D3 Power Gating is enabled 1 D3 Power Gating is disabled when Save is not done. **Power Well:** SUS
26:17	0x0 RW	**RESERVED (RSVD):** Reserved. **Power Well:** SUS
16	0x1 RW	**AON LFPS Detector Enable Mode (AON_LFPS_DETECTOR_EN_MODE):** 1 - Allow the LFSP Detector in AON to own LFPS detection when the port is in PS3 for U2/U3 - not RxD regardless of port ownership. 0 - Allow the LFPS Detector in AON to own the LFPS detection only when the AON owns the port and in U2/U3 - not RxD **Power Well:** SUS
15:8	0xff RW	**SS U3 LFPS Detection Threshold (SS_U3_LFPS_DETECTION_THRESHOLD):** This field controls the threshold used to determine when a valid U3 Wake is detected through when using the unfiltered LFPS source. The value on this field will reflect the binary count required to have been detected on the counter being clocked by the unfiltered lfps source to result in a valid U3 wake detection. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x9 RW	**SS_U3_LFPS_PRDC_SAMPLING_OFFTIME_CTRL:** This field controls the OFF time for the LFPS periodic sampling for USB3 Ports 0x0 periodic sampling is disabled. 0x1 OFF time is 1ms 0x2 OFF time is 2ms 0xF OFF time is 15ms The ON Time is determined by the amount of time required to reliably determine if there is a valid LFPS and is HW implementation specific. A speed up mode shall be implemented where this field is in units of us. i.e. 0x1 = 1 us OFF time, 0x2 = 2 us OFF time, etc. **Power Well:** SUS
3	0x0 RW	**PS3 LFPS Source Select (PS3_LFPS_SRC_SEL):** 0 LFPS Source is unfiltered 1 LFPS Source is filtered (Rx-Elec-Idle) LFPS Source is Rx-Elec-Idle for any non PS3 state. **Power Well:** SUS
2	0x0 RW	**XHCI Engine Autonomous Power Gate Exit Reset Policy (XHC_AUTO_PWRGATE_EXITRST_POLICY):** Controls when the xHCI engine is brought out of reset due to a power ungate. 0 Engine is brought out of reset when D3 to D0 is triggered. This allows for a quick power up sequence while leaving the virtual PCIe LTSSM in L23 is power ungate is not due to D3 to D0. 1 Engine is brought out of reset along with the rest of the IP. This is required for PMC save/restore flow. **Power Well:** SUS
1	0x0 RW	**USB2 Port Wake Unit Coupling Policy (USB2_PORT_WAKE_COUPLING_POLICY):** Controls the trigger for USB2 Port Wake Units to initiate Port Level Power Off Preparation. 0 RTD3 triggered 1 - Port Triggered when in L1, L2 or Disabled, Disconnected **Power Well:** SUS
0	0x0 RW	**USB3 Port Wake Unit Coupling Policy (USB3_PORT_WAKE_COUPLING_POLICY):** Controls the trigger for USB3 Port Wake Units to initiate Port Level Power Off Preparation. 0 - RTD3 Triggered 1 - Port Triggered when in PS3 due to RxDetect, U3, U2 or Disabled **Power Well:** SUS

7.4.170 PGCB Control (PGCBCTRL_REG)—Offset 80A8h

Access Method

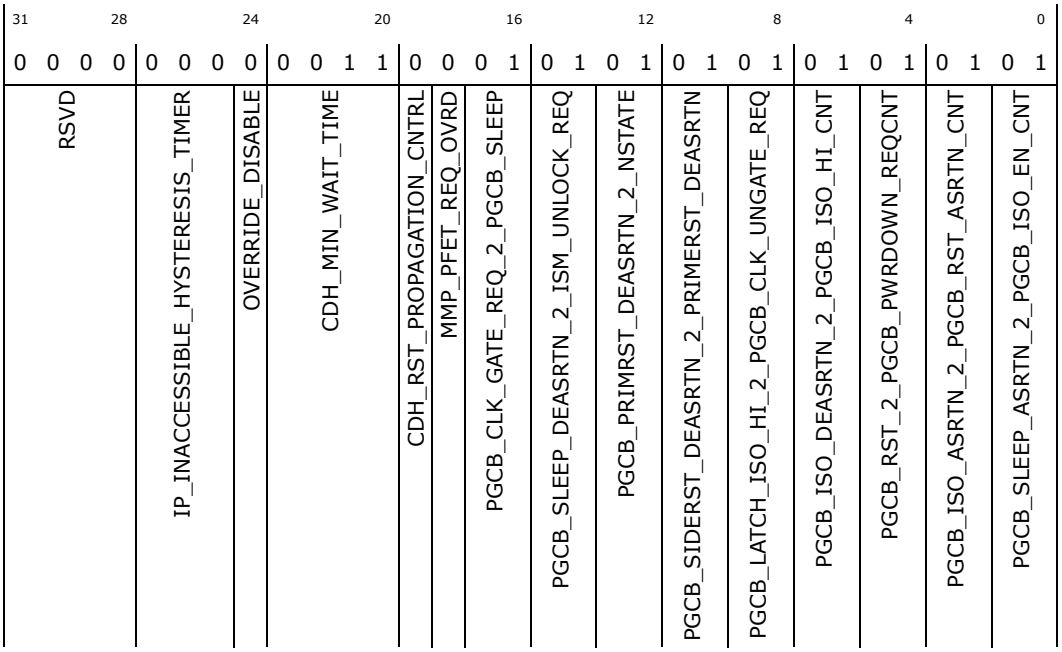
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80A8h

Op Codes:

h - Read, h - Write

Default: 00315555h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** SUS
27:25	0x0 RW	**IP_INACCESSIBLE_HYSTERESIS_TIMER:** 000 ? 50us 001 ? 100us 010 ? 150us 011 ? 200us 000 ? 250us 001 ? 300us 010 ? 350us 111 ? 400us **Power Well:** SUS
24	0x0 RW	**Override_Disable (OVERRIDE_DISABLE):** Reserved. **Power Well:** SUS
23:20	0x3 RW	**CDH Aggregation Minimum Wait Time (CDH_MIN_WAIT_TIME):** This field controls the minimum time that we must wait for resets to propagate before allowing Power Up flow to complete. The Power Up flow requires special handling of clocks, reset and sleep signaling which requires the CDH to monitor reset propagation. This timer allow for flexibility on when we consider all resets propagated. 0h Disabled 1h 2 clocks 2h 4 clocks 3h 8 clocks 4h 16 clocks 5h 32 clocks 6h 64 clocks 7h 128 clocks **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RW	**RESERVED (CDH_RST_PROPAGATION_CNTRL):** This bit will indicate the mode of operation for the CDH Reset Propagation Aggregator. It allows for a mode where the aggregation will wait for an indication from each CDH before proceeding OR ignore the CDH indication before proceeding. Regardless of the mode, the aggregator will enforce the CDH Aggregation Mini Wait Time. 0 Aggregate all the CDH indications before triggering the CDH Aggregation Mini Wait Time. Once the Min Wait Time is met a notification to the Power Sequencer/Control will be initiated 1 Trigger the CDH Aggregation Mini Wait Time w/o waiting for CDH indication. Once the Min Wait time is met a notification to the Power Sequencer/Control will be initiated. **Power Well:** SUS
18	0x0 RW	**MMP_PFET_REQ_OVRD:** This bit will disable the MMP PFET request condition for PGCB control. 1 MMP PFET Request Ignored 0 Default **Power Well:** SUS
17:16	0x1 RW	**PGCB Clock Gate Request to PGCB Sleep (PGCB_CLK_GATE_REQ_2_PGCB_SLEEP):** Value representing the minimum number of delay clocks required between the assertion of pgcb_ip_clkgate_b to the deassertion of pgcb_sleep on PG exit. (This is only applicable for IP-Accessible PG with state-retention enabled.) Please see the description of cfg_tsleepact for more details. **Power Well:** SUS
15:14	0x1 RW	**PGCB Sleep Deassertion to PGCB ISM Unlock Req (PGCB_SLEEP_DEASRTN_2_ISM_UNLOCK_REQ):** For IP-Accessible PG (with state retention): Value representing the minimum number of delay clocks required between the deassertion of gcb_sleepto the deassertion of pgcb_ip_*_lock_req_b. For IP-Inaccessible PG (or with state-retention disabled): Value representing the minimum number of delay clocks required between the deassertion of pgcb_sleep to the deassertion of pgcb_isol_en_b. **Power Well:** SUS
13:12	0x1 RW	**PGCB Prim Reset Deassertion to PGCB Next State (PGCB_PRIMRST_DEASRTN_2_NSTATE):** For IP-Accessible PG (with state retention): Value representing the minimum number of delay clocks required between the deassertion of pgcb_sleep to the deassertion of pgcb_ip_*_lock_req_b. For IP-Inaccessible PG (or with state-retention disabled): Value representing the minimum number of delay clocks required between the deassertion of pgcb_sleep to the deassertion of pgcb_isol_en_b. **Power Well:** SUS
11:10	0x1 RW	**PGCB Side Reset Deassertion to PGCB Prim Reset Deassertion (PGCB_SIDERST_DEASRTN_2_PRIMERST_DEASRTN):** Value representing the number of delay clocks required between the deassertion of gcb_force_rst_bto the deassertion of gcb_force_prim_rst_b (This is only applicable for IP-Accessible PG.) Please see the description of cfg_tsleepact for more details. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
9:8	0x1 RW	**PGCB Latch Isolation High to PGCB Clock Ungate Request (PGCB_LATCH_ISO_HI_2_PGCB_CLK_UNGATE_REQ):** Value representing the number of delay clocks required between the assertion of pgcb_isol_latchen to the deassertion of pgcb_ip_clkgate_req_b. Please see the description of cfg_tsleepact for more details. **Power Well:** SUS
7:6	0x1 RW	**PGCB Isolation Deassertion to PGCB Latch Isolation High Count (PGCB_ISO_DEASRTN_2_PGCB_ISO_HI_CNT):** Value representing the minimum number of delay clocks required between the deassertion of pgcb_isol_en_b to the assertion of gcb_isol_latchen. Please see the description of cfg_tsleepact for more details. **Power Well:** SUS
5:4	0x1 RW	**PGCB Reset Assertion to PGCB Power Down Request Count (PGCB_RST_2_PGCB_PWRDOWN_REQCNT):** For IP-Accessible PG (with state retention): Value representing the minimum number of delay clocks required between the assertion of pgcb_force_prim_rst_b and pgcb_force_rst_b to the assertion of pgcb_pmc_pg_req_b. For IP-Inaccessible PG (or with state-retention disabled): Value representing the minimum number of delay clocks required between the assertion of pgcb_force_prim_rst_b and pgcb_force_rst_b to the assertion of pgcb_sleep. Please see the description of cfg_tsleepact for more details. **Power Well:** SUS
3:2	0x1 RW	**PGCB Isolation Assertion to PGCB Reset Assertion Count (PGCB_ISO_ASRTN_2_PGCB_RST_ASRTN_CNT):** Value representing the minimum number of delay clocks required between the assertion of gcb_isol_en_bto the assertion of gcb_force_prim_rst_band gcb_force_rst_b Please see the description of [1:0] for more details. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
1:0	0x1 RW	**PGCB Sleep Assertion to PGCB Isolation Enable Count (PGCB_SLEEP_ASRTN_2_PGCB_ISO_EN_CNT):** For IP-Accessible PG (with state retention): Value representing the minimum number of delay clocks required between the assertion of pgcb_sleep (and the deassertion of pgcb_isol_latchen) to the assertion of pgcb_isol_en_b. For IP-Inaccessible PG (or with state-retention disabled): Value representing the minimum number of delay clocks required between the deassertion of pgcb_isol_latchen to the assertion of pgcb_isol_en_b, as well as the minimum number of delay clocks required between the assertion of pgcb_sleep to the assertion of pgcb_pmc_pg_req_b. Common for all cfg_t* inputs: 0 1 clock 1 2 clocks 0 8 clocks 1 256 clocks For any of the cfg_t* inputs that an IP may feel are a don-care and the IP does not feel they will be useful for post-silicon debug, the recommendation is to tie the input to 201 (2 clocks). Otherwise, the inputs may be tied to another relevant value or connected to a configuration register. Note: These signals may only change while pgcb_pwrupidle is asserted, if pgcb_pwrupidle is deasserted it should be valid and stable. (It may change the same cycle that ip_pgcb_pg_rdy_req_b asserts.) **Power Well:** SUS

7.4.171 D0I3 Control (DOI3CTRL_REG)—Offset 80ACh

Access Method

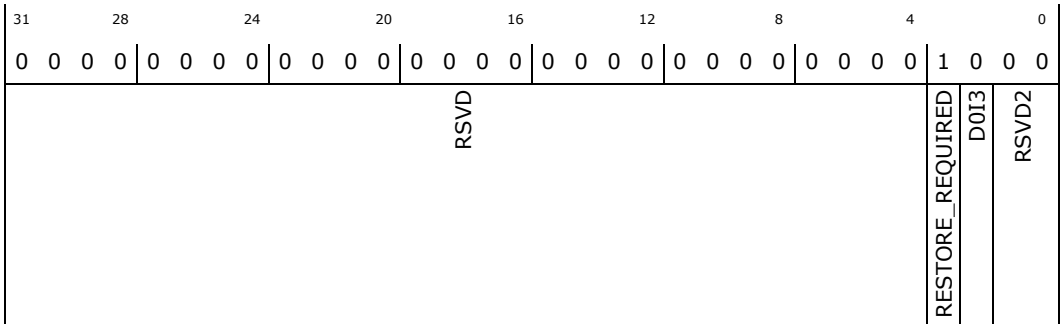
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80ACh

Op Codes:

h - Read, h - Write

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
3	0x1 RW/1C	**RestoreRequired (RESTORE_REQUIRED):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up. **Power Well:** SUS
2	0x0 RW	**D0I3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0). **Power Well:** SUS
1:0	0x0 RO	**RESERVED (RSVD2):** Reserved. **Power Well:** SUS

7.4.172 HOST_CTRL_MISC_REG—Offset 80B0h

Access Method

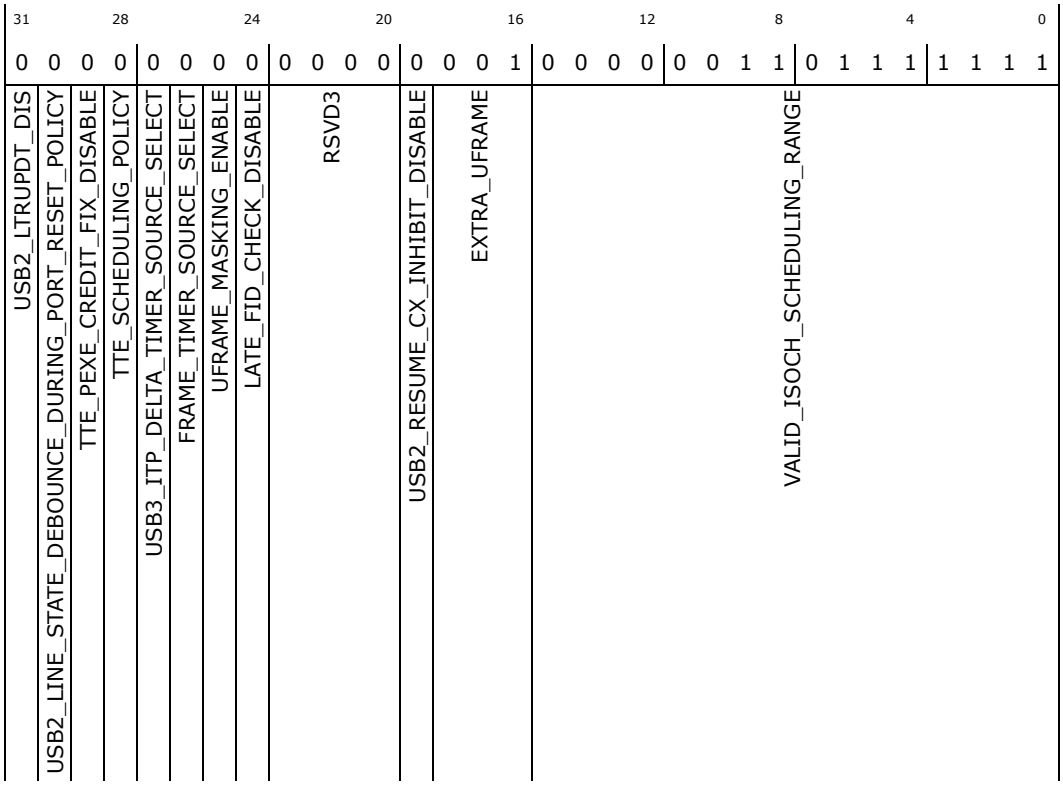
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80B0h

Op Codes:

h - Read, h - Write

Default: 0001037Fh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**USB2_LTRUPDT_DIS:** Reserved. **Power Well:** Core
30	0x0 RW	**USB2 Line State Debounce During Port Reset Policy (USB2_LINE_STATE_DEBOUNCE_DURING_PORT_RESET_POLICY):** This register controls how the debounce is enforced during the Port Reset phase. 0 do not enable the line state debounce during port reset. 1 enable the line state debounce during port reset. **Power Well:** Core
29	0x0 RW	**TTE PEXE Credit Fix Disable (TTE_PEXE_CREDIT_FIX_DISABLE):** When set, it disables a fix implemented to re-deem PEXE credits when a port is disconnected **Power Well:** Core
28	0x0 RW	**TTE Scheduling policy (TTE_SCHEDULING_POLICY):** This register controls a fix made to prevent over-scheduling by not account for 188B in each uFrame. Setting this bit will disable the fix and allow for over-scheduling. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
27	0x0 RW	**USB3 ITP Delta Timer Source Select (USB3_ITP_DELTA_TIMER_SOURCE_SELECT):** This register selects the source for the delta timer tracking used for ITP generation. 0 the source is a 16.666 ns tick generated from a crystal reference clock 1 - the source is a 16.666 ns tick generated from the aux_cclk. This field needs to remain in sync with Frame Timer Source Select to ensure the are both set or both cleared. There is no support for any other combination. **Power Well:** Core
26	0x0 RW	**Frame Timer Source Select (FRAME_TIMER_SOURCE_SELECT):** This register controls the source for the frame timer. 0 the source for the frame timer is a crystal reference clock 1 the source for the frame timer is the aux_cclk. **Power Well:** Core
25	0x0 RW	**uFrame Masking Enable (UFRAME_MASKING_ENABLE):** If set, enables the uFrame tick to be masked due to ports being in U3/NC. This controls a fix made to disable the auto masking of uFrame tick due to port state w/o any pipeline idle condition. When cleared, we rely on gating of frame timer due to proper port state and idleness tracking from the pipeline. **Power Well:** Core
24	0x0 RW	**Late FID Check Disable (LATE_FID_CHECK_DISABLE):** This register disables the Late FID Check performed when starting an ISOCH stream. **Power Well:** Core
23:20	0x0 RW	**RESERVED (RSVD3):** Reserved. **Power Well:** Core
19	0x0 RW	**USB2 Resume Cx Inhibit Disable (USB2_RESUME_CX_INHIBIT_DISABLE):** Controls if USB2 L1 Resume is allowed to contribute to DMA Active which will inhibit Cx state. 0 USB2 L1 Resume is allowed to inhibit Cx via DMA Active 1 USB2 L1 Resume is NOT allowed to inhibit Cx via DMA Active When cleared, Cx will only be inhibited when the DMA traffic for the port begins. **Power Well:** Core
18:16	0x1 RW	**Extra uFrame (EXTRA_UFRAME):** This register controls the extra number of uFrames added onto the advancing of late FID check. **Power Well:** Core
15:0	0x37f RW	**Valid Isoch Scheduling Range (VALID_ISOCH_SCHEDULING_RANGE):** This register defines the window in miliseconds from the current Frame that will be considered for scheduling in an upcoming Frame. Anything scheduled outside of this window will be considered as late and will trigger the Missed Service Error. **Power Well:** Core

7.4.173 HOST_CTRL_MISC_REG2—Offset 80B4h

Access Method

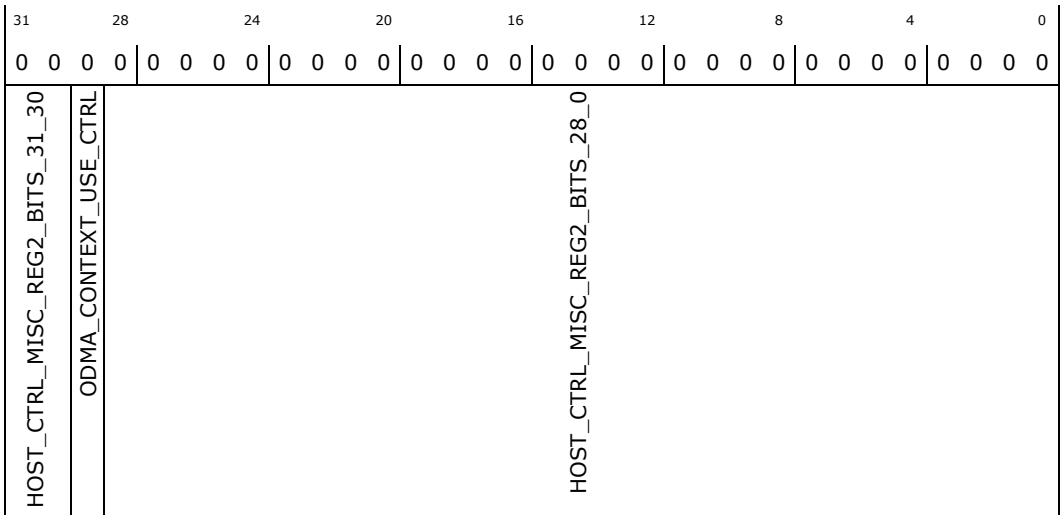
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80B4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**HOST_CTRL_MISC_REG2_BITS_31_30:** Reserved. **Power Well:** Core
29	0x0 RW	**ODMA_CONTEXT_USE_CTRL:** Reserved. **Power Well:** Core
28:0	0x0 RW	**HOST_CTRL_MISC_REG2_BITS_28_0:** Reserved. **Power Well:** Core

7.4.174 SSPE_REG—Offset 80B8h

Access Method

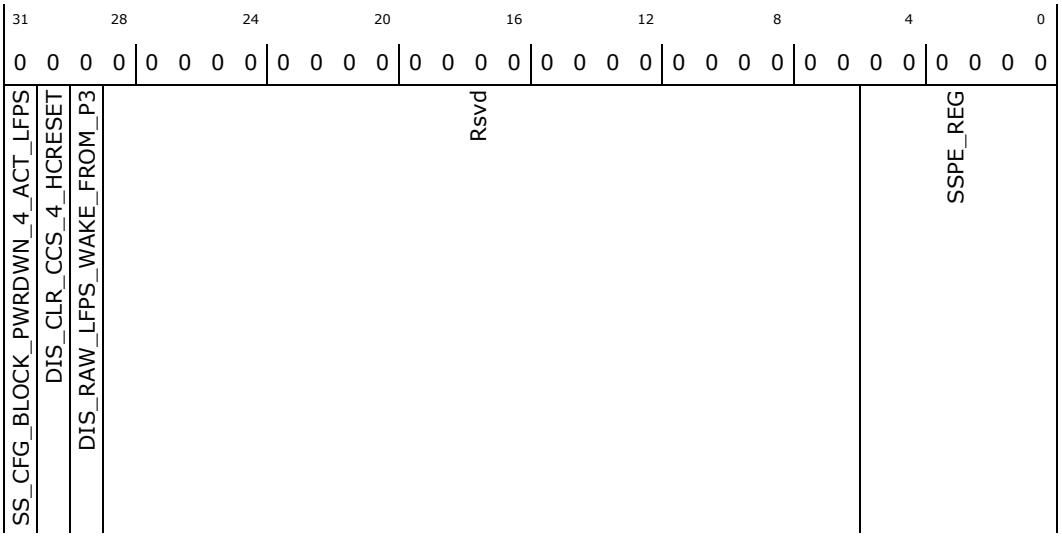
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80B8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**ssCfgBlockPwrDwn4ActLFPS (SS_CFG_BLOCK_PWRDWN_4_ACT_LFPS):** Reserved. **Power Well:** SUS
30	0x0 RW	**dis_clr_ccs_4hcreset (DIS_CLR_CCS_4_HCRESET):** Reserved. **Power Well:** SUS
29	0x0 RW	**DIS_RAW_LFPS_WAKE_FROM_P3:** This bit is used to disable RTL fix provided to separate RawLFPS and RxElecIDle detection Default 0: RTL fix is Enable 1 : Write to 1 to Disable the Fix **Power Well:** SUS
28:6	0x0 RO	**Rsvd:** Reserved. **Power Well:** SUS
5:0	0x0 RW	**SSPE_REG:** Reserved. **Power Well:** SUS

7.4.175 reg_SSPITPE_type (SSPITPE)—Offset 80BCh

Access Method

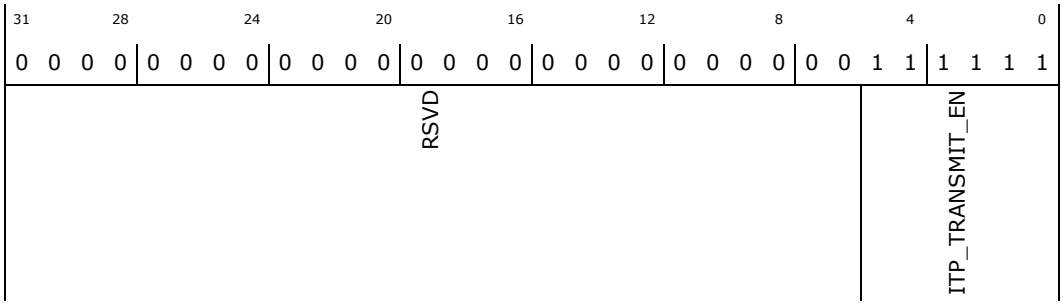
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80BCh

Op Codes:

h - Read, h - Write

Default: 0000003Fh



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**RSVD:** Reserved. **Power Well:** Core
5:0	0x3f RW	**ITP Transmit Enable (ITP_TRANSMIT_EN):** Width is scaled with USB3 Port Count PortCount=4 **Power Well:** Core

7.4.176 AUX Reset Control (AUX_CTRL_REG)—Offset 80C0h

Access Method

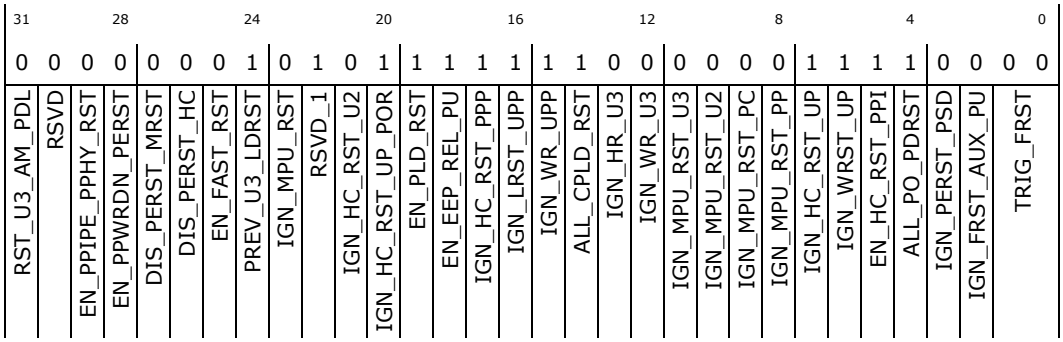
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80C0h

Op Codes:

h - Read, h - Write

Default: 015FC0F0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Reset USB3 AUX/Main PD Logic (RST_U3_AM_PDL):** A reset that is designed to reset all USB3 port AUX + Main power domain logic. This is a debug function. It is called cold reset. Write 1 to this register will issue a cold reset to USB3 ports. **Power Well:** SUS
30	0x0 RW	**RESERVED (RSVD):** Reserved. **Power Well:** SUS
29	0x0 RW	**Enable PCIe PIPE Reset As PCIe PHY Reset (EN_PPIPE_PPHY_RST):** This bit set to 1 selects the PCIe PIPE reset as a PCIe PHY power on reset. 0 selects the AUX powerup reset as a PCIe PHY powerup reset. **Power Well:** SUS
28	0x0 RW	**Ensure PIPE Powerdown On PERST# (EN_PPWRDN_PERST):** This bit ensures any PERST# being asserted will cause PIPE powerdown state transition to P1. **Power Well:** SUS
27	0x0 RW	**Disable PERST# Main RST (DIS_PERST_MRST):** There is a feature where we only allow PERST# to be treated as a main powerdown reset when it is asserted during the state that is not in D3. This bit disables this feature when it is set to 1. If this bit is set to 1, it means that any PERST# will be treated as a main power domain reset regardless of its Dstate. **Power Well:** SUS
26	0x0 RW	**Disable PCIe PERST# Host Controller (DIS_PERST_HC):** There is a feature where we can disable PCIe PERST# from reset the host controller until power management control module has done its clock switching. This is for a case where PM entered L23 and immediately PERST# asserted. This bit is designed to enable this feature when set to 1. **Power Well:** SUS
25	0x0 RW	**Enable Fast Simulation Reset Mode (EN_FAST_RST):** Enable a fast simulation mode for reset function. This is a feature for GLS **Power Well:** SUS
24	0x1 RW	**Prevent USB3 Link Down Reset (PREV_U3_LDRST):** When set to 1 prevent a reset being generated due to the USB3 port link down condition. **Power Well:** SUS
23	0x0 RW	**Ignore Main Power Up Reset (IGN_MPU_RST):** When set to 1 ignore the main power up reset for USB3 PIPE PHY reset. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
22	0x1 RW	**RESERVED (RSVD_1):** Reserved. **Power Well:** SUS
21	0x0 RW	**Ignore HC Reset USB2 (IGN_HC_RST_U2):** When set to '1' ignore HC reset to reset the USB2 Port logic **Power Well:** SUS
20	0x1 RW	**Ignore HC Reset USB PHY (IGN_HC_RST_UP_POR):** When set to '1' ignore HC reset to the USB PHY power-on reset **Power Well:** SUS
19	0x1 RW	**Enable PCIe Link-Down Reset (EN_PLD_RST):** Enable a reset due to a PCIe link-down condition. The PCIe link down condition will cause a HC reset liked. If this bit is set 1, the PCIe link down condition will only reset the PCIe core. **Power Well:** SUS
18	0x1 RW	**Enable EEPROM Reload On Power Up (EN_EEP_REL_PU):** When set to '1' enable EEPROM reload on every main power-up **Power Well:** SUS
17	0x1 RW	**Ignore HC Reset PCIe PHY PIPE (IGN_HC_RST_PPP):** When set to '1' ignore HC reset to the PCIe PHY PIPE reset **Power Well:** SUS
16	0x1 RW	**Ignore LTSSM Reset USB PHY PIPE (IGN_LRST_UPP):** When set to '1' ignore the LTSSM of USB link state transition caused reset to USB PHY PIPE reset **Power Well:** SUS
15	0x1 RW	**Ignore Warm Reset USB PHY Power (IGN_WR_UPP):** When set to '1' ignore warm reset the USB PHY power on reset **Power Well:** SUS
14	0x1 RW	**Allow Core PCIe Link Down Reset (ALL_CPLD_RST):** When set to '1' allow PCIe link down to cause a reset to the rest of the core **Power Well:** SUS
13	0x0 RW	**Ignore Hot Reset USB3 (IGN_HR_U3):** When set to '1' ignore hot reset to the USB3 port logic **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
12	0x0 RW	**Ignore Warm Reset USB3 (IGN_WR_U3):** When set to '1' ignore warm reset to the USB3 port logic **Power Well:** SUS
11	0x0 RW	**Ignore Main Power Up Reset USB3 (IGN_MPU_RST_U3):** When set to '1' ignore main power up reset to USB3 port logic **Power Well:** SUS
10	0x0 RW	**Ignore Main Power Up Reset USB2 (IGN_MPU_RST_U2):** When set to '1' ignore main power up reset to USB2 port logic **Power Well:** SUS
9	0x0 RW	**Ignore Main Power Up Reset PCIe Core (IGN_MPU_RST_PC):** When set to '1' ignore main power up reset to PCIe core **Power Well:** SUS
8	0x0 RW	**Ignore Main Power Up Reset PCIe PHY (IGN_MPU_RST_PP):** When set to '1' ignore main power up reset to PCIe PHY **Power Well:** SUS
7	0x1 RW	**Ignore HC Reset USB PHY (IGN_HC_RST_UP):** When set to '1' ignore HC reset to the USB PHY **Power Well:** SUS
6	0x1 RW	**Ignore Warm Reset USB PHY (IGN_WRST_UP):** When set to '1' ignore warm reset to the USB PHY **Power Well:** SUS
5	0x1 RW	**Enable HC Reset Per Port Isolation (EN_HC_RST_PPI):** Enables the HC reset or per port reset isolation function **Power Well:** Core
4	0x1 RW	**Allow Power Off Power Domain Reset (ALL_PO_PDRST):** When set to '1' allow main power off condition to trigger a main power domain reset **Power Well:** SUS
3	0x0 RW	**Ignore Wait For PERST# During Power Show Down (IGN_PERST_PSD):** When set to '1' ignore waiting for PERST# deassertion during main power show down. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**Ignore Fundamental Reset During AUX Power Up (IGN_FRST_AUX_PU):** When fundamental reset is asserted during AUX power up, if this bit is set, then we will ignore PERST# such that purely wait for timeout to deassert fundamental reset. **Power Well:** SUS
1:0	0x0 RW	**Trigger Fundamental Reset (TRIG_FRST):** Writing to bit(1:0) to value of 2'b11 will cause a fundamental reset **Power Well:** SUS

7.4.177 Super Speed Bandwidth Overload (HOST_BW_OV_SS_REG)—Offset 80C4h

Access Method

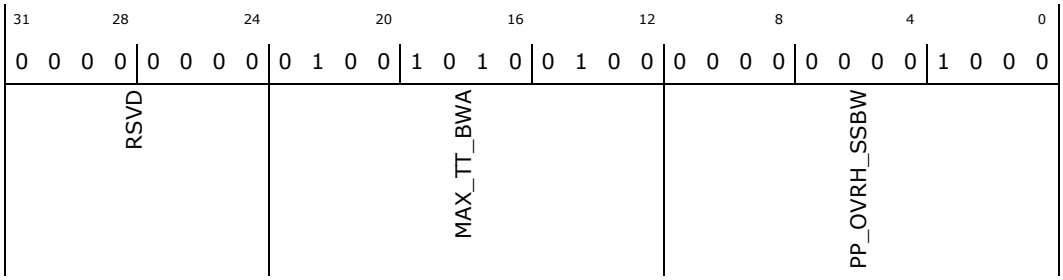
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80C4h

Op Codes:

h - Read, h - Write

Default: 004A4008h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
23:12	0x4a4 RW	**Max. TT BW Allowed (MAX_TT_BWA):** see white paper **Power Well:** Core
11:0	0x8 RW	**Per Packet Overhead SS BW (PP_OVRH_SSBW):** BW calculation: Overhead per packet for SS BW calculations. see white paper. **Power Well:** Core

7.4.178 High Speed TT Bandwidth Overload (HOST_BW_OV_HS_REG)—Offset 80C8h

Access Method

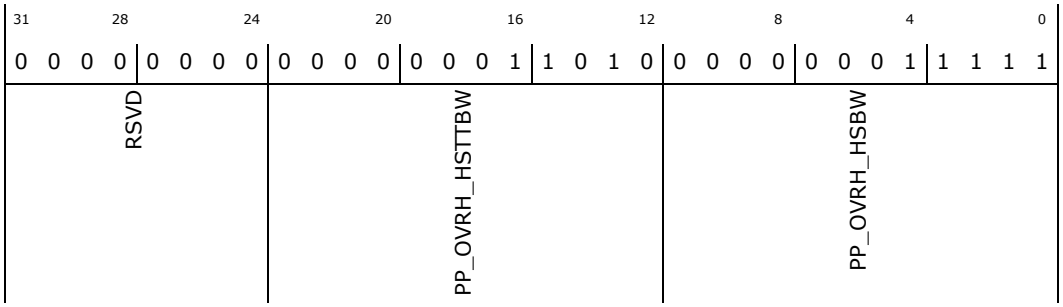
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80C8h

Op Codes:

h - Read, h - Write

Default: 0001A01Fh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
23:12	0x1a RW	**Per Packet Overhead HS-TT BW (PP_OVRH_HSTTBW):** BW calculation: Overhead per packet for HS-TT BW calculations. see white paper. **Power Well:** Core
11:0	0x1f RW	**Per Packet Overhead HS BW (PP_OVRH_HSBW):** BW calculation: Overhead per packet for HS BW calculations. see white paper. **Power Well:** Core

7.4.179 Bandwidth Overload Full Low Speed (HOST_BW_OV_FS_LS_REG)—Offset 80CCh

Access Method

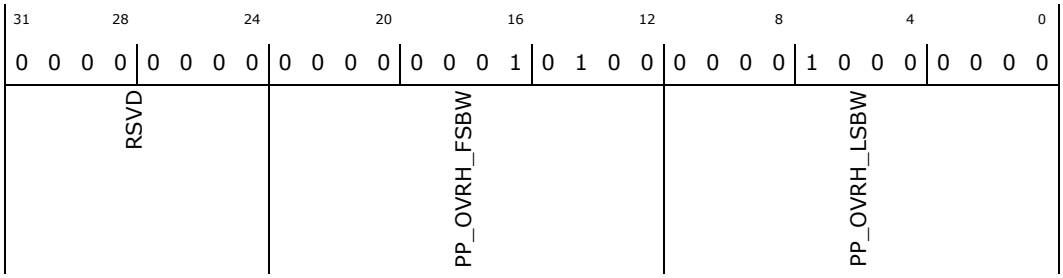
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80CCh

Op Codes:

h - Read, h - Write

Default: 00014080h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
23:12	0x14 RW	**Per Packet Overhead FS BW (PP_OVRH_FSBW):** BW calculation: Overhead per packet for FS BW calculations. see white paper. **Power Well:** Core
11:0	0x80 RW	**Per Packet Overhead LS BW (PP_OVRH_LSBW):** BW calculation: Overhead per packet for LS BW calculations. see white paper. **Power Well:** Core

7.4.180 System Bandwidth Overload (HOST_BW_OV_SYS_REG)—Offset 80D0h

Access Method

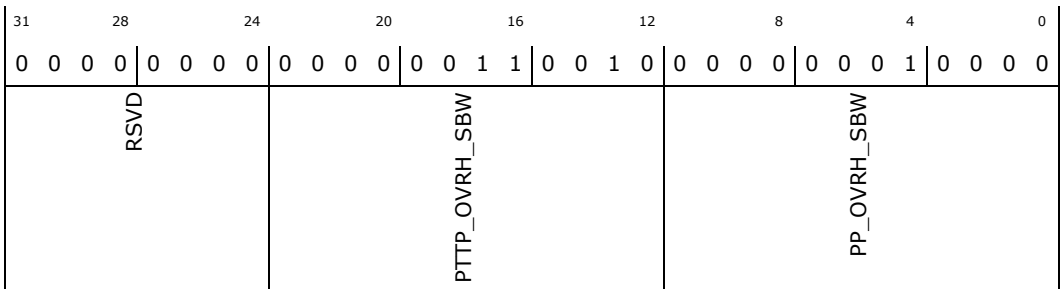
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80D0h

Op Codes:

h - Read, h - Write

Default: 00032010h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
23:12	0x32 RW	**Per TT Packet Overhead System BW (PTTP_OVRH_SBW):** BW calculation: Overhead per TT packet for System BW calculations. see white paper. **Power Well:** Core
11:0	0x10 RW	**Per Packet Overhead System BW (PP_OVRH_SBW):** BW calculation: Overhead per packet for System BW calculations. see white paper. **Power Well:** Core

7.4.181 Scheduler Async Delay (HOST_CTRL_SCH_ASYNC_DELAY_REG)—Offset 80D4h

Global defaults for inserting delays between packets in the scheduler for async. types.

Access Method

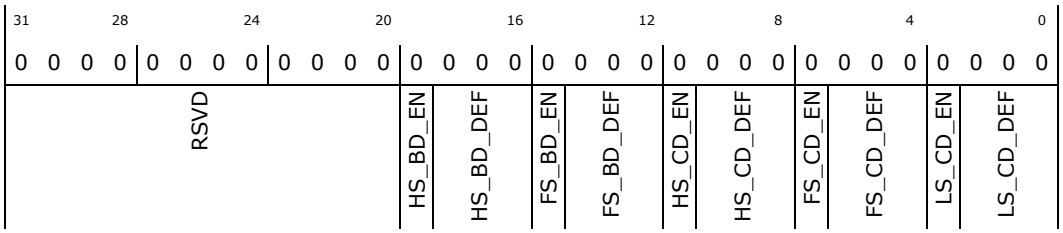
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80D4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
19	0x0 RW	**High-Speed Bulk Delay Enable (HS_BD_EN):** Reserved. **Power Well:** Core
18:16	0x0 RW	**High-Speed Bulk Delay Default (HS_BD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...) **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Full-Speed Bulk Delay Enable (FS_BD_EN):** Reserved. **Power Well:** Core
14:12	0x0 RW	**Full-Speed Bulk Delay Default (FS_BD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...) **Power Well:** Core
11	0x0 RW	**High-Speed Control Delay Enable (HS_CD_EN):** Reserved. **Power Well:** Core
10:8	0x0 RW	**High-Speed Control Delay Default (HS_CD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...) **Power Well:** Core
7	0x0 RW	**Full-Speed Control Delay Enable (FS_CD_EN):** Reserved. **Power Well:** Core
6:4	0x0 RW	**Full-Speed Control Default (FS_CD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...) **Power Well:** Core
3	0x0 RW	**Low-Speed Control Delay Enable (LS_CD_EN):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Low-Speed Control Delay Default (LS_CD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...) **Power Well:** Core

7.4.182 DEVICE MODE CONTROL REG 0 (DUAL_ROLE_CFG_REG0)—Offset 80D8h

All bits in this register must be in the Always ON Power domain (ungated SUS or AON as appropriate)

Access Method

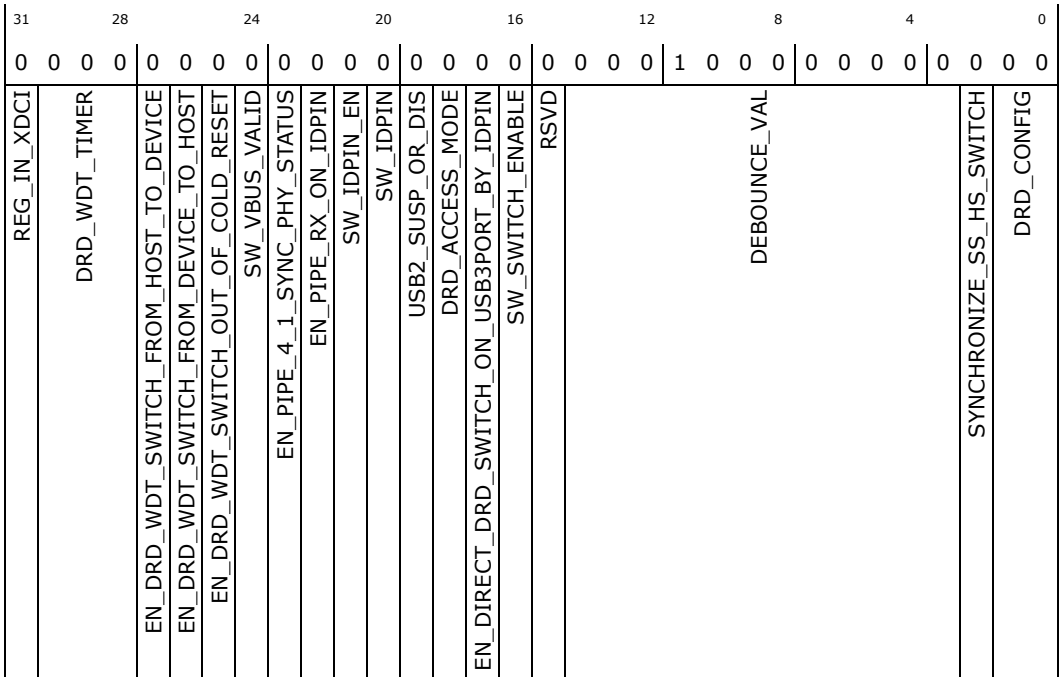
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80D8h

Op Codes:

h - Read, h - Write

Default: 00000800h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**XDCI_DRD_CTRL_EN (REG_IN_XDCI):** When DRD_ACCESS_MODE (bit 18) =1, 0 -- The policies below is controlled by register in the XHCI MMIO 1 -- The policies below is controlled by register in the XDCI MMIO When DRD_ACCESS_MODE =0, this bit is a don?t care. **Power Well:** SUS
30:28	0x0 RW	**DRD_WDT_TIMER:** 0-based incremental of 500ms **Power Well:** SUS
27	0x0 RW	**EN_DRD_WDT_SWITCH_FROM_HOST_TO_DEVICE:** Reserved. **Power Well:** SUS
26	0x0 RW	**EN_DRD_WDT_SWITCH_FROM_DEVICE_TO_HOST:** Reserved. **Power Well:** SUS
25	0x0 RW	**EN_DRD_WDT_SWITCH_OUT_OF_COLD_RESET:** Reserved. **Power Well:** SUS
24	0x0 RW	**SW_VBUS_VALID:** if SW_IDPIN_EN (bit 21) is 1, 0 ? deassert sw vbus valid 1 ? assert sw vbus valid **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
23	0x0 RW	**EN_PIPE_4_1_SYNC_PHY_STATUS:** Reserved. **Power Well:** SUS
22	0x0 RW	**EN_PIPE_RX_ON_IDPIN:** During the connection to a device, there may be a delay in DRD switch from XDCI to XHCI mode,the rx term can be low after idpin deasserts. If this bit is 0, the rx term will be assert immediately after idpin toggle. Otherwise, the device may fall back to USB2 mode. 1 -- drive 0s on utmi rx signals to controller if not connected. **Power Well:** SUS
21	0x0 RW	**SW_IDPIN_EN:** SW_IDPIN_EN 1 -- enable SW id pin (pre DRD) 0 -- disable SW id pin. **Power Well:** SUS
20	0x0 RW	**SW_IDPIN:** if SW_IDPIN_EN (bit 21) is 1, 0 - host mode 1 - device mode **Power Well:** SUS
19	0x0 RW	**USB2_SUSP_OR_DIS:** 1 - The DRD UTMI suspendm will be controlled by host/device based on the DRD switch. 0 - whenever device or host deassert suspendm, the DRD UTMI suspendm will be deasserted. **Power Well:** SUS
18	0x0 RW	**DRD_ACCESS_MODE:** 0 - The DUAL_ROLE register from host and device are ORed to control DRD 1 - The DUAL_ROLE register from host and device are selected by XDCI_DRD_CTRL_EN (bit 31) to control DRD **Power Well:** SUS
17	0x0 RW	**EN_DIRECT_DRD_SWITCH_ON_USB3PORT_BY_IDPIN:** 0 enable the direct DRD switch on USB3 port by idpin 1 disable the direct DRD switch **Power Well:** SUS
16	0x0 RW	**SW_SWITCH_ENABLE:** SW switch enable 0 (default) ID pin HW controlled DRD. 1 -- SW controlled DRD (ignore idpin), switch based on the DRD_CONFIG. **Power Well:** SUS
15	0x0 RW	**RSVD:** Reserved. **Power Well:** SUS
14:3	0x100 RW	**DEBOUNCE_VAL:** ID ping debounce timer (DEBOUNCE_VAL): in the unit of RTC clock (33us) default to 8.448 ms **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**SYNCHRONIZE_SS_HS_SWITCH:** Synchronize the SS and HS switch: 0 (default) Does not synchronize. i.e. HS switch on the debounced id pin, while SS switch independently controlled by the sequencer. 1 synchronize HS and SS switch. Both speeds switch when sequencer switch. **Power Well:** SUS
1:0	0x0 RW	**DRD_CONFIG:** 00 Dynamic DRD switch mode 01 static host mode 10 static device mode 11 -- reserved **Power Well:** SUS

7.4.183 DEVICE MODE CONTROL REG 1 (DUAL_ROLE_CFG_REG1)—Offset 80DCh

All bits in this register must be in the Always ON Power domain (ungated SUS or AON as appropriate)

Access Method

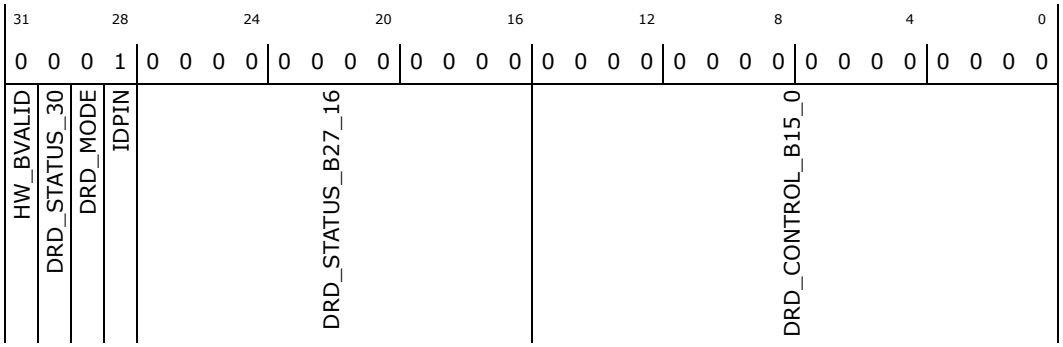
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80DCh

Op Codes:

h - Read, h - Write

Default: 10000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**BVALID_HW (HW_BVALID):** hardware bvalid **Power Well:** SUS
30	0x0 RO	**DRD_STATUS_B31_30 (DRD_STATUS_30):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
29	0x0 RO	**DRD_MODE:** SS DRD mode 0 device mode 1 host mode **Power Well:** SUS
28	0x1 RO	**IDPIN:** IDPIN value hw version **Power Well:** SUS
27:16	0x0 RO	**DRD_STATUS_B27_16:** Reserved. **Power Well:** SUS
15:0	0x0 RW	**DRD_CONTROL_B15_0:** Reserved. **Power Well:** SUS

7.4.184 AUX Power Management Control (AUX_CTRL_REG1)—Offset 80E0h

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80E0h

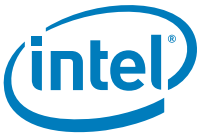
Op Codes:

h - Read, h - Write

Default: 808DBCA0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	0	1	0	0	0	1	1	0	1	1	0	1	1	1	1	0	0	1	0	1	0	0	0	0	0
D3_HOT_FXN_EN	ALL_L1_CORE_CG	AL_EP_SEXT	ALL_EP_RCP	AL_PERST_FRST	OVR_PCIE_P2_P1	SET_ISSV_1	CLR_ISSV_0	EN_SRE_SW_LD	RSVD_1	FORCE_SR1	CPTR	CIDS1	CIDS0	EN_CFG_UP2	CCGD	EN_CFG_RDP3	EN_CFG_PIPE_RST	EN_FILT_TX_IDLE	EN_HE_GEN_PME	EN_ISOL	EN_L1_P2_OVR	EN_CORE_CG	EN_PHY_STS_TO	IGN_APE_PC	EN_P2_OVR_P1	EN_P2_REM_WAKE	FORCED_PM_STATE				INIT_FPMS

Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**D3 Hot function enable register (D3_HOT_FXN_EN):** This bit is from pin input which is set 1. But we allow software to alter it if it is needed. 1: D3 hot enabled 0: D3 hot not abled. **Power Well:** SUS
30	0x0 RW	**Allow L1 Core Clock Gating (ALL_L1_CORE_CG):** When set to 1 allows core clock being gated during L1 state. **Power Well:** SUS



Bit Range	Default & Access	Field Name (ID): Description
29	0x0 RW	**Allow Engine PHY Status Extension (AL_EP_SEXT):** When set to 1 allows the engine to extend PHY status of PCIe PIPE for one more cycle. This is due to the fact that our rate change function has a potential of not being able to sample the phystatus signal. **Power Well:** SUS
28	0x0 RW	**Allow Engine PCIe Rate Change Passing (ALL_EP_RCP):** When set to 1 allows the engine to pass PCIe rate change signal as it is from PCIe core to PCIe PHY. **Power Well:** SUS
27	0x0 RW	**Allow Engine PERST Fundamental Reset (AL_PERST_FRST):** When set to 1 allow engine to treat PERST# as a foundamental reset **Power Well:** SUS
26	0x0 RW	**Overwrite PCIe P2 to P1 (OVR_PCIE_P2_P1):** When set to 1 will overwrite a PCIe powerdown state of P2 to P1. **Power Well:** SUS
25	0x0 RW	**Set Internal SSV 1 (SET_ISSV_1):** When set to 1 set the internal SSV to 1. **Power Well:** SUS
24	0x0 RW	**Clear Internal SSV 0 (CLR_ISSV_0):** When set to 1 clear the internal SSV to 0. **Power Well:** SUS
23	0x1 RW	**Enable save_restore_enable SW Loading (EN_SRE_SW_LD):** This is a bit that enables the save_restore_enable signal being loaded when a software command has set Save bit. This is a debug function. **Power Well:** SUS
22	0x0 RW	**RESERVED (RSVD_1):** Reserved. **Power Well:** SUS
21	0x0 RW	**Force save_restore 1 (FORCE_SR1):** When set to 1, it will force the save_restore flag to 1. This flag is an bit to ensure that we have masked the update during low power state. If software write this bit to 1, it must write it to 0 in order to resume the normal save and restore function. **Power Well:** SUS
20	0x0 RW	**cfg pcie txreg rd (CPTR):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
19	0x1 RW	**cfg iob drivestrength[1] (CIDS1):** Reserved. **Power Well:** SUS
18	0x1 RW	**cfg iob drivestrength[0] (CIDS0):** Reserved. **Power Well:** SUS
17	0x0 RW	**Enable CFG USB P2 (EN_CFG_UP2):** When set to '1' enable cfg usb p2 **Power Well:** SUS
16	0x1 RW	**cfg clk gate dis (CCGD):** Reserved. **Power Well:** SUS
15	0x1 RW	**Enable CFG RXDET P3 (EN_CFG_RDP3):** When set to '1' enable cfg rxdet p3 **Power Well:** SUS
14	0x0 RW	**Enable CFG PIPE Reset (EN_CFG_PIPE_RST):** When set to '1' enable cfg pipe rst **Power Well:** SUS
13	0x1 RW	**Enable Filter TX Idle (EN_FILT_TX_IDLE):** When set to 1 enables a filter function to TX electrical idle signal at PCie PIPE. We have a filter that will set TXelecidle signal of PCIe PIPE to 1 whenever we are in isolation state or power down transition states. **Power Well:** SUS
12	0x1 RW	**Enable Host Engine Generate PME (EN_HE_GEN_PME):** This is a global switch to whether or not eable this host engine to generate PME message. **Power Well:** SUS
11	0x1 RW	**Enable Isolation (EN_ISOL):** When set to '1' enable isolation **Power Well:** SUS
10	0x1 RW	**Enable L1 Caused P2 Overwrite (EN_L1_P2_OVR):** Set 1 to enable a new feature. This new feature is designed to use L1 as a state to identify whether we should do P2 Overwrite or not. We used to use P1 state to identify whether or not to invoke P2 overwrite function. **Power Well:** SUS
9	0x0 RW	**Enable Core Clock Gating (EN_CORE_CG):** When set to '1' enable core clock gating based on low power state entered **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**Enable PHY Status Timeout (EN_PHY_STS_TO):** When set to '1' enable PHY status timeout function which is designed to cover the PCIePHY issue that we may have not able to detect the PHY status toggle. **Power Well:** SUS
7	0x1 RW	**Ignore aux_pm_en PCIe Core (IGN_APE_PC):** When set to '1' ignore the aux_pm_en reg from PCIe core to continue the remote wake/clock switching support **Power Well:** SUS
6	0x0 RW	**Enable P2 Overwrite P1 (EN_P2_OVR_P1):** When set to '1' enable P2 overwrite P1 when PCIe core has indicated the transition from P0 to P1. This is to enable entering the even lower power state. **Power Well:** SUS
5	0x1 RW	**Enable P2 Remote Wake (EN_P2_REM_WAKE):** When set 1 '1' enable the remote wake function by allowing P2 clock/switching and P2 entering **Power Well:** SUS
4:1	0x0 RW	**Forced PM State (FORCED_PM_STATE):** Reserved. **Power Well:** SUS
0	0x0 RW	**Initiate Force PM State (INIT_FPMS):** When set to '1' force PM state to go to the state indicated in bit 4:1 **Power Well:** SUS

7.4.185 Battery Charge (BATTERY_CHARGE_REG)—Offset 80E4h

Access Method

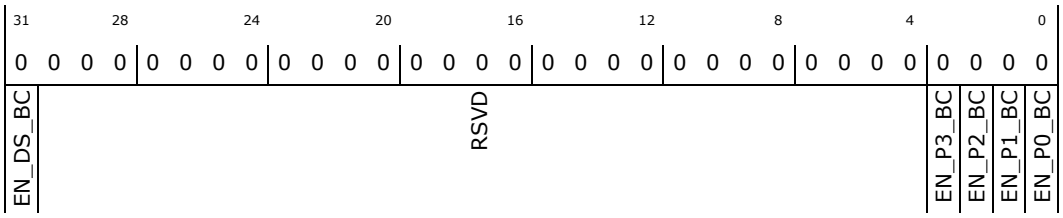
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80E4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Enable DM_SRC Battery Charge (EN_DS_BC):** 1 - Always enable battery charge DM_SRC if not connected. Don't wait for portable device detect. (spec. ver. 1.2) 0 - Battery charge spec ver. 1.1. **Power Well:** SUS
30:4	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
3	0x0 RW	**Enable Port 3 Battery Charging (EN_P3_BC):** 0 - Battery charging disabled (Physical Port #3) 1 - Battery charging enabled (Physical Port #3) **Power Well:** SUS
2	0x0 RW	**Enable Port 2 Battery Charging (EN_P2_BC):** 0 - Battery charging disabled (Physical Port #2) 1 - Battery charging enabled (Physical Port #2) **Power Well:** SUS
1	0x0 RW	**Enable Port 1 Battery Charging (EN_P1_BC):** 0 - Battery charging disabled (Physical Port #1) 1 - Battery charging enabled (Physical Port #1) **Power Well:** SUS
0	0x0 RW	**Enable Port 0 Battery Charging (EN_P0_BC):** 0 - Battery charging disabled (Physical Port #0) 1 - Battery charging enabled (Physical Port #0) **Power Well:** SUS

7.4.186 Port Watermark (HOST_CTRL_WATERMARK_REG)—Offset 80E8h

Access Method

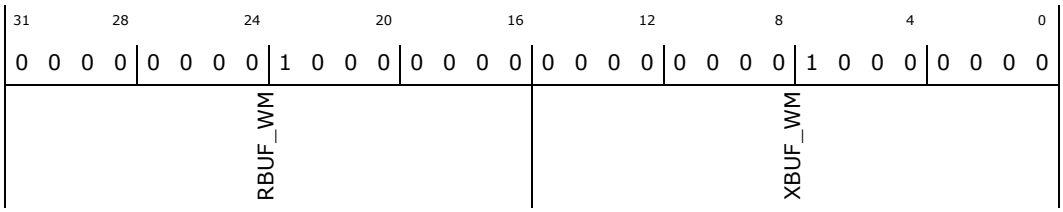
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80E8h

Op Codes:

h - Read, h - Write

Default: 00800080h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x80 RW	**RBUF water mark (RBUF_WM):** Reserved. **Power Well:** Core
15:0	0x80 RW	**XBUF water mark (XBUF_WM):** Reserved. **Power Well:** Core

7.4.187 SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)—Offset 80ECh

Access Method

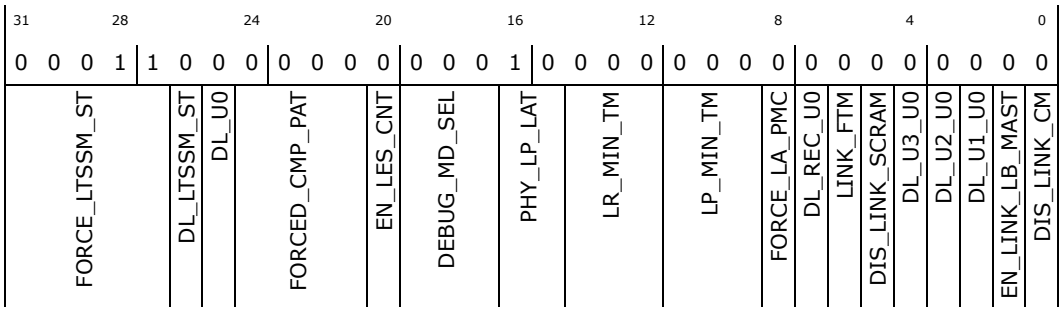
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80ECh

Op Codes:

h - Read, h - Write

Default: 18010000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x3 RW	**Force LTSSM State (FORCE_LTSSM_ST):** LTSSM state to be forced This value is for test purpose only. **Power Well:** Core
26	0x0 RW	**Direct Link LTSSM State (DL_LTSSM_ST):** 0: Normal operation mode 1: Direct link to a specific state specified by bit 31:27 This bit is for test purpose only. It shall be written 0 in normal operation mode. **Power Well:** Core
25	0x0 RW	**Direct Link To U0 (DL_U0):** 0: Normal operation mode 1: Direct link to U0 This bit is for test purpose only. It shall be written 0 in normal operation mode. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
24:21	0x0 RW	**Forced Compliance Pattern (FORCED_CMP_PAT):** Compliance pattern to be forced to enter compliance mode This value is for test purpose only. **Power Well:** Core
20	0x0 RW	**Enable Link Error Slave Count (EN_LES_CNT):** 0: Disable link error slave count 1: Enable link error slave count **Power Well:** Core
19:17	0x0 RW	**Debug Mode Select (DEBUG_MD_SEL):** Reserved. **Power Well:** Core
16:15	0x2 RW	**PHY Low Power Latency (PHY_LP_LAT):** This field defines the latency to drive the PHY to enter low power mode 0: 4 cycles 1: 8 cycles 2: 16 cycles 3: 32 cycles **Power Well:** Core
14:12	0x0 RW	**Link Recovery Minimum Time (LR_MIN_TM):** This value defines the minimum time for the link to stay in Recovery.Active other than from U3. The granuity is 128us. **Power Well:** Core
11:9	0x0 RW	**Link Polling Minimum Time (LP_MIN_TM):** This value defines the minimum time for the link to stay in Polling.Active and Recovery.Active from U3. The granuity is 128us. **Power Well:** Core
8	0x0 RW	**Force Link Accept PM Command (FORCE_LA_PMC):** 0: Normal operation mode 1: Force link to accept power management command **Power Well:** Core
7	0x0 RW	**Direct Link Recovery U0 (DL_REC_U0):** 0: Normal operation mode 1: Direct link to Recovery from U0 **Power Well:** Core
6	0x0 RW	**Link Fast Training Mode (LINK_FTM):** 0: Normal operation mode 1: Link fast training mode This bit should be written 0 in normal operation. **Power Well:** Core
5	0x0 RW	**Disable Link Scrambler (DIS_LINK_SCRAM):** 0: Enable link scrambler 1: Disable link scramber **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**Direct Link U3 From U0 (DL_U3_U0):** 0: Normal operation mode 1: Direct link to U3 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode. **Power Well:** Core
3	0x0 RW	**Direct Link U3 From U0 (DL_U2_U0):** 0: Normal operation mode 1: Direct link to U2 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode. **Power Well:** Core
2	0x0 RW	**Direct Link U3 From U0 (DL_U1_U0):** 0: Normal operation mode 1: Direct link to U1 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode. **Power Well:** Core
1	0x0 RW	**Enable Link Loopback Master Mode (EN_LINK_LB_MAST):** 0: Disable link loopback master mode 1: Enable link loopback master mode **Power Well:** Core
0	0x0 RW	**Disable Link Compliance Mode (DIS_LINK_CM):** 0: Enable link compliance mode 1: Disable link compliance mode **Power Well:** Core

7.4.188 USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)—Offset 80F0h

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

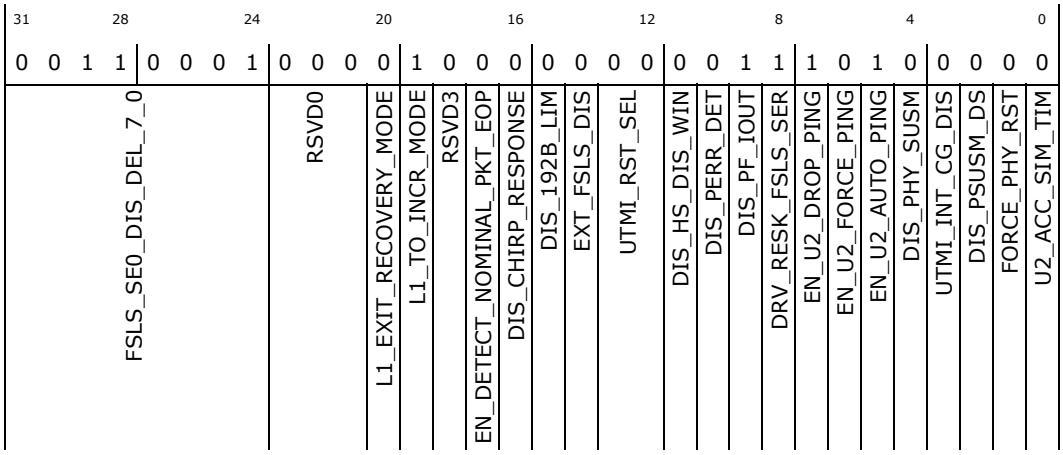
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80F0h

Op Codes:

h - Read, h - Write

Default: 310803A0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x31 RW	**FS/LS Mode SE0 Disconnect Delay[7:0] (FSLS_SE0_DIS_DEL_7_0):** # of microseconds of SE0 in FS/LS mode to register disconnect had occurred. **Power Well:** SUS
23:21	0x0 RW	**Reserved (RSVD0):** Reserved. **Power Well:** SUS
20	0x0 RW	**L1_EXIT_RECOVERY_MODE:** Mode for extended L1 Exit recovery delay: 0: 12us 1: 50us **Power Well:** SUS
19	0x1 RW	**L1_TO_INCR_MODE:** Mode select for L1 Timeout increments: 0: time out increments are in 125us 1: L1 Timeout increments are in 256us. Refer to USB2 PORTHLPMC.L1 Timeout in XHCI Spec for additional details **Power Well:** SUS
18	0x0 RW	**Reserved (RSVD3):** Reserved. **Power Well:** SUS
17	0x0 RW	**EN_DETECT_NOMINAL_PKT_EOP:** 0: Detect minimal packet EOP. 1: Detect nominal packet EOP. **Power Well:** SUS
16	0x0 RW	**Disable Chirp Response (DIS_CHIRP_RESPONSE):** 0: Normal 1: Force full speed on host ports (disable chirp response) **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Disable 192 Byte Limit Check (DIS_192B_LIM):** 0: Enforce 192 byte limit on complete-split INs. Treat any packet) 192 as babble case. 1: Disable 192 byte limit check. **Power Well:** SUS
14	0x0 RW	**External Provided FS/LS Disconnect (EXT_FSLS_DIS):** 0: Internal FS/LS Disconnect from linestate(1:0) 1: External provided FS/LS Disconnect from hostdisconnect input **Power Well:** SUS
13:12	0x0 RW	**UTMI Reset Source Select (UTMI_RST_SEL):** Select UTMI Reset Source (FRD UTMI Reset Only) 00: HCReset or Force PHY Reset or internal reset after disconnect/suspend for restart (default) 01,11: UTMI reset = ~UTMI suspendm 10: UTMI reset = ~UTMI suspendm and synchronization to port clk. **Power Well:** SUS
11	0x0 RW	**Disable HS Disconnect Window (DIS_HS_DIS_WIN):** 0: Enable HS Disconnect Window Function 1: Disable HS Disconnect Window Function **Power Well:** SUS
10	0x0 RW	**Disable Port Error Detection (DIS_PERR_DET):** 0: Enable Port Error Detection (default) 1: Disable Port Error Detection **Power Well:** SUS
9	0x1 RW	**Disable Peek Function for ISO-OUT (DIS_PF_IOUT):** 0: Enable Peek function for ISO-OUT (default) 1: Disable Peek function for ISO-OUT **Power Well:** SUS
8	0x1 RW	**Drive Resume-K FS/LS Serial Interface (DRV_RESK_FSLS_SER):** 0: Drive Resume-K on parallel Interface 1: Drive Resume-K directly on FS/LS Serial Interface (default) **Power Well:** SUS
7	0x1 RW	**Enable USB2 Drop-Ping (EN_U2_DROP_PING):** 0: Disable Drop-Ping Function in USB2 Protocol (default) 1: Enable Drop-Ping Function in USB2 Protocol **Power Well:** SUS
6	0x0 RW	**Enable USB2 Force-Ping (EN_U2_FORCE_PING):** 0: Disable Force-Ping Function in USB2 Protocol (default) 1: Enable Force-Ping Function in USB2 Protocol **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
5	0x1 RW	**Enable USB2 Auto-Ping (EN_U2_AUTO_PING):** 0: Disable Auto-Ping Function 1: Enable Auto-Ping Function in USB2 Protocol (default) **Power Well:** SUS
4	0x0 RW	**Disable PHY SuspendM (DIS_PHY_SUSM):** 0: PHY is suspend=U3,U2,disconnect (default) 1: Disable PHY SuspendM in All States **Power Well:** SUS
3	0x0 RW	**UTMI Internal Clock Gate Disable (UTMI_INT_CG_DIS):** 0: Normal operation (internal clock gated in U2,U3,disconnect) 1: UTMI Internal Clock Gate Disable **Power Well:** SUS
2	0x0 RW	**Disable PHY SuspendM in Disconnect State (DIS_PSUSM_DS):** 0: PHY is suspendM=0 in Disconnect State (default) 1: Disable PHY SuspendM in Disconnect State **Power Well:** SUS
1	0x0 RW	**Force PHY Reset (FORCE_PHY_RST):** 0: Normal Operation (default) 1: Force PHY Reset **Power Well:** SUS
0	0x0 RW	**USB2 Accelerated Simulation Timing (U2_ACC_SIM_TIM):** 0: Normal Operation (default - FPGA/ASIC) 1: USB2 Accelerated Simulation Timing (default - simulation) **Power Well:** SUS

7.4.189 USB2 Port Link Control 2 (USB2_LINK_MGR_CTRL_REG2)—Offset 80F4h

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

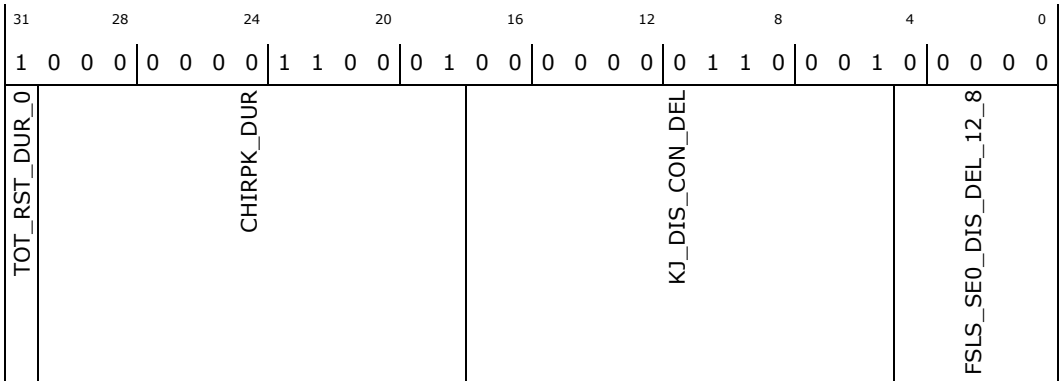
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80F4h

Op Codes:

h - Read, h - Write

Default: 80C40620h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**Total Reset Duration[0] (TOT_RST_DUR_0):** # of microseconds for total reset duration **Power Well:** SUS
30:18	0x31 RW	**Chirp-K Duration (CHIRPK_DUR):** # of microseconds of Chirp-K to register that a device is chirping **Power Well:** SUS
17:5	0x31 RW	**K/J Disconnect Connect Delay (KJ_DIS_CON_DEL):** # of microseconds of K/J in disconnected state to register connect has occurred. **Power Well:** SUS
4:0	0x0 RW	**FS/LS Mode SE0 Disconnect Delay[12:8] (FSLS_SE0_DIS_DEL_12_8):** # of microseconds of SE0 in FS/LS mode to register disconnect had occurred. **Power Well:** SUS

7.4.190 USB2 Port Link Control 3 (USB2_LINK_MGR_CTRL_REG3)—Offset 80F8h

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

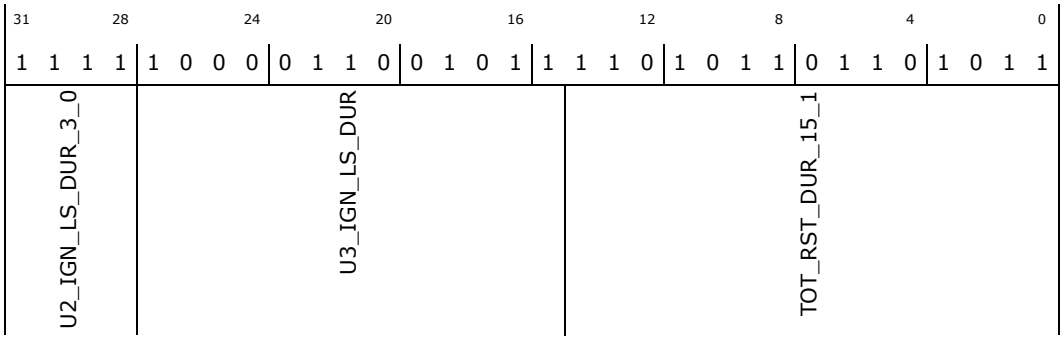
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80F8h

Op Codes:

h - Read, h - Write

Default: F865EB6Bh



Bit Range	Default & Access	Field Name (ID): Description
31:28	0xf RW	**U2 Entry Ignore Linestate Changes Duration[3:0] (U2_IGN_LS_DUR_3_0):** # of microseconds after entering U2, linestate changes are ignored as bus settles **Power Well:** SUS
27:15	0x10cb RW	**U3 Entry Ignore Linestate Changes Duration (U3_IGN_LS_DUR):** # of microseconds after entering U3, linestate changes are ignored as bus settles **Power Well:** SUS
14:0	0x6b6b RW	**Total Reset Duration[15:1] (TOT_RST_DUR_15_1):** # of microseconds for total reset duration **Power Well:** SUS

7.4.191 USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)—Offset 80FCh

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

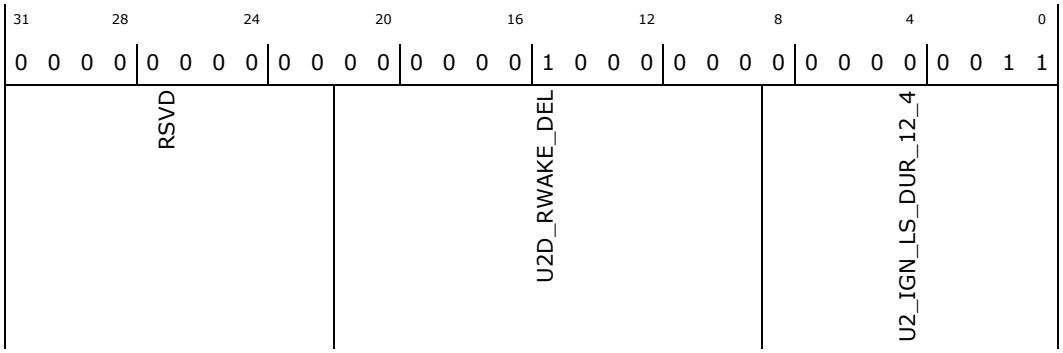
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 80FCh

Op Codes:

h - Read, h - Write

Default: 00008003h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
21:9	0x40 RW	**U2 Detect Remote Wake Delay (U2D_RWAKE_DEL):** #of microseconds after detecting U2 remote wake condition to reflect K **Power Well:** SUS
8:0	0x3 RW	**U2 Entry Ignore Linestate Changes Duration[12:4] (U2_IGN_LS_DUR_12_4):** # of microseconds after entering U2, linestate changes are ignored as bus settles **Power Well:** SUS

7.4.192 Bandwidth Calc Control (HOST_CTRL_BW_CTRL_REG)—Offset 8100h

Access Method

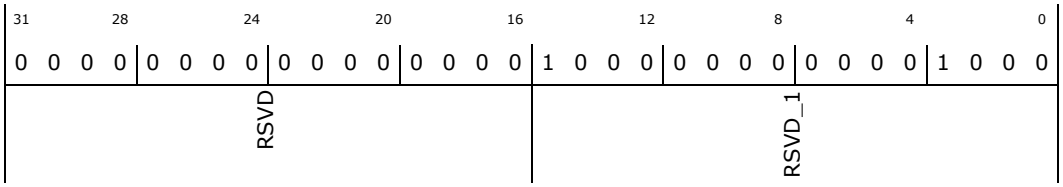
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8100h

Op Codes:

h - Read, h - Write

Default: 00008008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
15:0	0x8008 RW	**Reserved (RSVD_1):** Reserved. **Power Well:** Core

7.4.193 Host Interface Control (HOST_IF_CTRL_REG)—Offset 8108h

Access Method

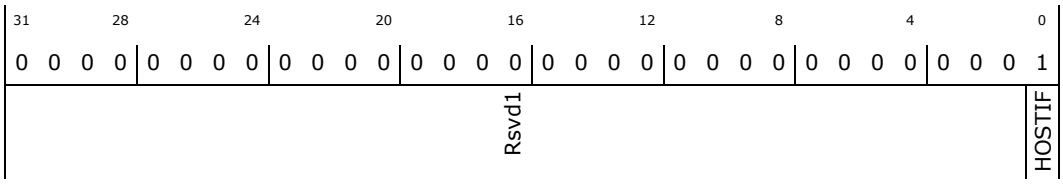
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8108h

Op Codes:

h - Read, h - Write

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Rsvd1:** Reserved. **Power Well:** Core
0	0x1 RW	**Host IF (HOSTIF):** Reserved. **Power Well:** Core

7.4.194 Bandwidth Overload Burst (HOST_BW_OV_BURST_REG)—Offset 810Ch

Access Method

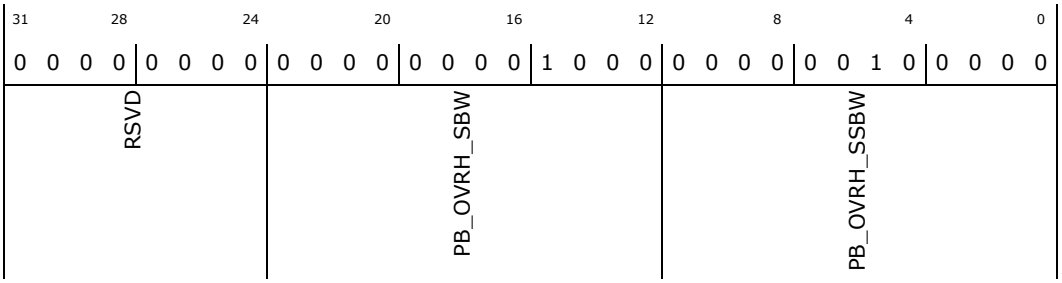
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 810Ch

Op Codes:

h - Read, h - Write

Default: 00008020h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
23:12	0x8 RW	**Per Burst Overhead System BW (PB_OVRH_SBW):** BW calculation: Overhead per burst for system BW calculations. see white paper. **Power Well:** Core
11:0	0x20 RW	**Per Burst Overhead System BW (PB_OVRH_SSBW):** BW calculation: Overhead per burst for SS BW calculations. see white paper. **Power Well:** Core

7.4.195 USB Max Bandwidth Control 4 (HOST_CTRL_BW_MAX_REG)—Offset 8128h

Access Method

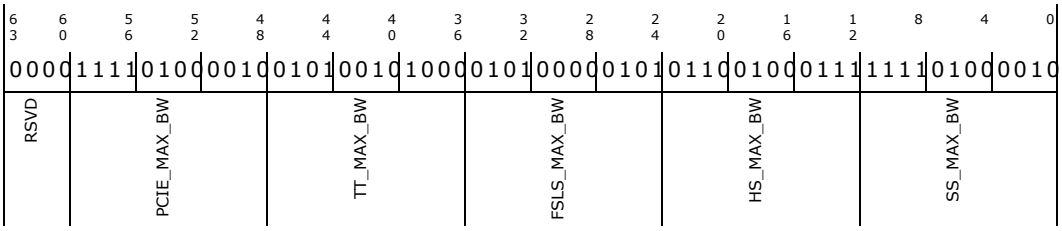
Type: Message Bus Register (Size: 64 bits)

Offset: [Port: 0x5A] + 8128h

Op Codes:

h - Read, h - Write

Default: 0F42528505647F42h



Bit Range	Default & Access	Field Name (ID): Description
63:60	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
59:48	0xf42 RW	**PCIe Max BW Units (PCIE_MAX_BW):** Max. Number of BW units for PCIe (system interface) (denominator in 90% calculation) **Power Well:** Core
47:36	0x528 RW	**TT Max BW Units (TT_MAX_BW):** Max. Number of BW units for TTs. (denominator in 90% calculation) **Power Well:** Core
35:24	0x505 RW	**FS/LS Max BW Units (FSLS_MAX_BW):** Max. Number of BW units for FS/LS ports. (denominator in 90% calculation) **Power Well:** Core
23:12	0x647 RW	**HS Max BW Units (HS_MAX_BW):** Max. Number of BW units for HS ports. (denominator in 80% calculation) **Power Well:** Core
11:0	0xf42 RW	**SS Max BW Units (SS_MAX_BW):** Max. Number of BW units for SS ports. (denominator in 90% calculation) **Power Well:** Core

7.4.196 USB2 Linestate Debug (LINESTATE_DEBUG_REG)—Offset 8130h

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8130h

Op Codes:

h - Read, h - Write

Default: 00000000h

31 28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RSVD	P14_UTMI_LS, P13_UTMI_LS	P12_UTMI_LS, P11_UTMI_LS	P10_UTMI_LS, P9_UTMI_LS	P8_UTMI_LS, P7_UTMI_LS	P6_UTMI_LS, P5_UTMI_LS	P4_UTMI_LS, P3_UTMI_LS	P2_UTMI_LS, P1_UTMI_LS

Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
27:26	0x0 RO	**Port 14 UTMI Linestate (P14_UTMI_LS):** Reserved. **Power Well:** Core
25:24	0x0 RO	**Port 13 UTMI Linestate (P13_UTMI_LS):** Reserved. **Power Well:** Core
23:22	0x0 RO	**Port 12 UTMI Linestate (P12_UTMI_LS):** Reserved. **Power Well:** Core
21:20	0x0 RO	**Port 11 UTMI Linestate (P11_UTMI_LS):** Reserved. **Power Well:** Core
19:18	0x0 RO	**Port 10 UTMI Linestate (P10_UTMI_LS):** Reserved. **Power Well:** Core
17:16	0x0 RO	**Port 9 UTMI Linestate (P9_UTMI_LS):** Reserved. **Power Well:** Core
15:14	0x0 RO	**Port 8 UTMI Linestate (P8_UTMI_LS):** Reserved. **Power Well:** Core
13:12	0x0 RO	**Port 7 UTMI Linestate (P7_UTMI_LS):** Reserved. **Power Well:** Core
11:10	0x0 RO	**Port 6 UTMI Linestate (P6_UTMI_LS):** Reserved. **Power Well:** Core
9:8	0x0 RO	**Port 5 UTMI Linestate (P5_UTMI_LS):** Reserved. **Power Well:** Core
7:6	0x0 RO	**Port 4 UTMI Linestate (P4_UTMI_LS):** Reserved. **Power Well:** Core
5:4	0x0 RO	**Port 3 UTMI Linestate (P3_UTMI_LS):** Reserved. **Power Well:** Core
3:2	0x0 RO	**Port 2 UTMI Linestate (P2_UTMI_LS):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1:0	0x0 RO	**Port 1 UTMI Linestate (P1_UTMI_LS):** Reserved. **Power Well:** Core

7.4.197 USB2 Protocol Gap Timer (USB2_PROTOCOL_GAP_TIMER_REG)—Offset 8134h

Access Method

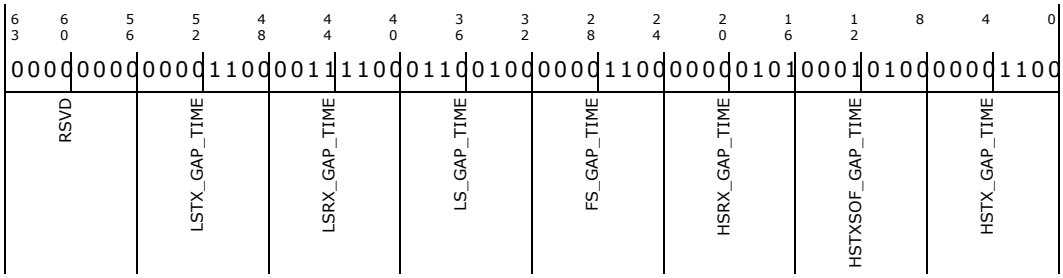
Type: Message Bus Register (Size: 64 bits)

Offset: [Port: 0x5A] + 8134h

Op Codes:

h - Read, h - Write

Default: 000C3C640C05140Ch



Bit Range	Default & Access	Field Name (ID): Description
63:56	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
55:48	0xc RW	**GAP time after LS TX thru FS hub (LSTX_GAP_TIME):** Reserved. **Power Well:** Core
47:40	0x3c RW	**GAP time after LS RX thru FS hub (LSRX_GAP_TIME):** Reserved. **Power Well:** Core
39:32	0x64 RW	**GAP timer after LS (LS_GAP_TIME):** Reserved. **Power Well:** Core
31:24	0xc RW	**GAP time after FS (FS_GAP_TIME):** Reserved. **Power Well:** Core
23:16	0x5 RW	**GAP time after HS RX (HSRX_GAP_TIME):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x14 RW	**GAP time after HS TX SOF (HSTXSOF_GAP_TIME):** Reserved. **Power Well:** Core
7:0	0xc RW	**GAP time HS TX Packet (HSTX_GAP_TIME):** Reserved. **Power Well:** Core

7.4.198 USB2 Protocol Bus Timeout Timer (USB2_PROTOCOL_BTO_TIMER_REG)—Offset 813Ch

Access Method

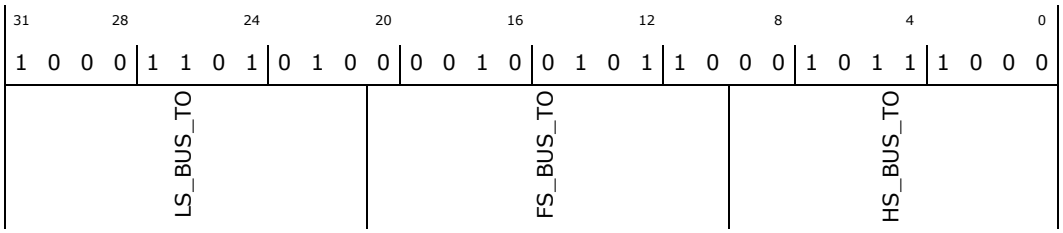
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 813Ch

Op Codes:

h - Read, h - Write

Default: 8D4258B8h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x46a RW	**Bus timeout count for LS (LS_BUS_TO):** Reserved. **Power Well:** Core
20:10	0x96 RW	**Bus timeout count for FS (FS_BUS_TO):** Reserved. **Power Well:** Core
9:0	0xb8 RW	**Bus timeout count for HS (HS_BUS_TO):** Reserved. **Power Well:** Core

7.4.199 Power Scheduler Control-0 (PWR_SCHED_CTRL0)—Offset 8140h

Access Method

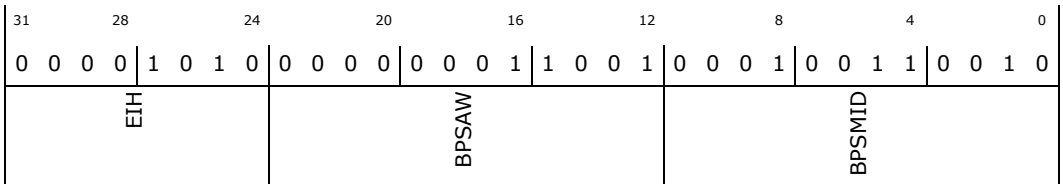
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8140h

Op Codes:

h - Read, h - Write

Default: 0A019132h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0xa RW	**Engine Idle Hysteresis (EIH):** This register controls the min. idle span that has to be observed from the engine idle indicators before the power state flags (xhc_*_idle) will indicate a 1. **Power Well:** Core
23:12	0x19 RW	**Backbone PLL Shutdown Advance Wake (BPSAW):** This register controls the time before the next scheduled transaction where the Backbone PLL request will assert. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124) **Power Well:** Core
11:0	0x132 RW	**Backbone PLL Shutdown Min. Idle Duration (BPSMID):** The sum of this register plus the Backbone PLL Shutdown Advance Wake form to a Total Idle time. When the next scheduled periodic transaction is after present time + Total Idle, the Backbone PLL request will de-assert, allowing the PLL to shutdwon. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124) **Power Well:** Core

7.4.200 Power Scheduler Control-2 (PWR_SCHED_CTRL2)—Offset 8144h

These bit enable by EP type those EPs classes that are considered for determining next periodic active interval for pre-wake of the periodic_active signal. EP classes that are disabled may never be observed in setting of the periodic_active signal.

Access Method

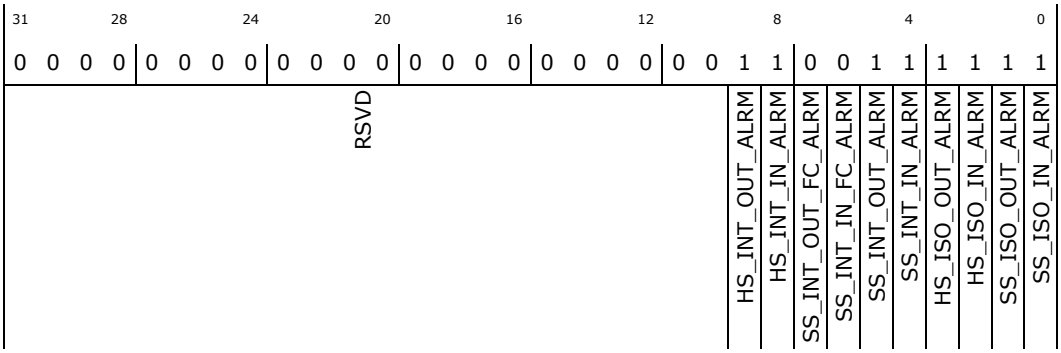
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8144h

Op Codes:

h - Read, h - Write

Default: 0000033Fh



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
9	0x1 RW	**HS Interrupt-OUT Alarm (HS_INT_OUT_ALRM):** Reserved. **Power Well:** Core
8	0x1 RW	**HS Interrupt-IN Alarm (HS_INT_IN_ALRM):** Reserved. **Power Well:** Core
7	0x0 RW	**SS Interrupt-OUT FC Alarm (SS_INT_OUT_FC_ALRM):** Reserved. **Power Well:** Core
6	0x0 RW	**SS Interrupt-IN Alarm (SS_INT_IN_FC_ALRM):** Reserved. **Power Well:** Core
5	0x1 RW	**SS Interrupt-OUT & not in FC Alarm (SS_INT_OUT_ALRM):** Reserved. **Power Well:** Core
4	0x1 RW	**SS Interrupt-IN & not in FC Alarm (SS_INT_IN_ALRM):** Reserved. **Power Well:** Core
3	0x1 RW	**HS ISO-OUT Alarm (HS_ISO_OUT_ALRM):** Reserved. **Power Well:** Core
2	0x1 RW	**HS ISO-IN Alarm (HS_ISO_IN_ALRM):** Reserved. **Power Well:** Core
1	0x1 RW	**SS ISO-OUT Alarm (SS_ISO_OUT_ALRM):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**SS ISO-IN Alarm (SS_ISO_IN_ALRM):** Reserved. **Power Well:** Core

7.4.201 AUX Power Management Control (AUX_CTRL_REG2)—Offset 8154h

Access Method

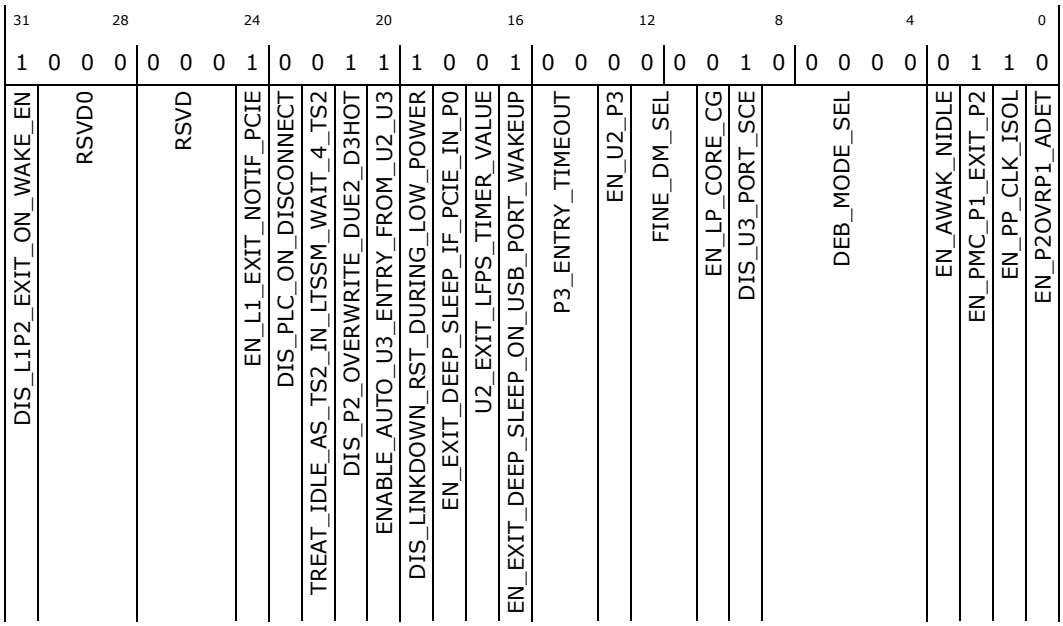
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8154h

Op Codes:

h - Read, h - Write

Default: 81390206h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**DIS_L1P2_EXIT_ON_WAKE_EN:** This bit disables the dependency on Wake Enables defined in PORTSC for L1P2 exit when in D0 **Power Well:** SUS
30:28	0x0 RW	**RESERVED0 (RSVD0):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
27:25	0x0 RW	**RESERVED (RSVD):** Reserved. **Power Well:** SUS
24	0x1 RW	**Enable L1 exit notification to SNPS PCIe core (EN_L1_EXIT_NOTIF_PCIE):** This bit enables a L1 exit notification to SNPS PCIe core. There is a case where USB ports have waked up and AUX PM module has started the wakeup process. The AUX PM control state got into a wait for P0 state because it needs to wait until PCie core to signal powerdown state change. Due to the fact that the core is in D3Hot, there is no run_stop bit set such that no internal interrupt will be fired. This causes the LTSSM of PCIe stayed in L1 even though AUX PM has known that it needs an L1 exit. This bit works together with bit21 of this register. 1: enables this feature 0: disables this feature. **Power Well:** SUS
23	0x0 RW	**DISABLE PLC ON DISCONNECT (DIS_PLC_ON_DISCONNECT):** 1: do not assert PLC for disconnection 0: assert PLC for disconnection **Power Well:** SUS
22	0x0 RW	**TREAT_IDLE_AS_TS2_IN_LTSSM_WAIT_4_TS2:** This bit enables a feature in PCie core LTSSM to treat IDLE received as TS2 when LTSSM is in wait for TS2 receive state. This is a function requested from PHY where it is possible to not able to receive TS2 without error. 1: treat Logic IDLE as TS2 received when in some PCIe LTSSM state. 0: disable this feature. **Power Well:** SUS
21	0x1 RW	**Disable p2 overwrite due to the D3HOT where PCIe core enters the L1 (DIS_P2_OVERWRITE_DUE2_D3HOT):** We added a feature where if PCIe core LTSSM enters L1 due to the D3hot, the aux PM control will not start a P2 overwrite function in anticipating for the next L23 enter. 1: disables p2 overwrite due to the D3HOT where PCIe core enters the L1. 0: enables P2 overwrite even if we are in D3Hot. **Power Well:** SUS
20	0x1 RW	**Enable the port to enter U3 automatically when in U1/U2 (ENABLE_AUTO_U3_ENTRY_FROM_U2_U3):** 1: enables the port to enter U3 automatically when in U1/U2 0: disables the port to enter U3 automatically when in U1/U2 **Power Well:** SUS
19	0x1 RW	**No linkdown reset is issue during low power state (DIS_LINKDOWN_RST_DURING_LOW_POWER):** No linkdown reset is issue during low power state **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
18	0x0 RW	**EN_EXIT_DEEP_SLEEP_IF_PCIE_IN_P0:** This bit enables a feature in AUX PM module where if PCIe core LTSSM is in P0 for a duration of time, we will exit the deep sleep state. This is for failure control in case. 1: enables this feature 0: disable this feature **Power Well:** SUS
17	0x0 RW	**U2_EXIT_LFPS_TIMER_VALUE:** This bit selects U2 exit LFPS timer value 0: 320ns 400ns in 25MHz domain 1: 240ns 320ns in 25MHz domain **Power Well:** SUS
16	0x1 RW	**EN_EXIT_DEEP_SLEEP_ON_USB_PORT_WAKEUP:** This bit enables a function that AUX PM module exits from the deep sleep state due to the USB ports wakeup level signal. We have added this feature where USB ports will generated a wakeup level signal to wakeup the AUX PM module if it is in deep sleep state and this level signal will be cleared if the change bits are updated by software. 1: enables this function 0: disables this function which means that a wakeup pulse generated from each USB PortSC event will wake up the AUX PM module from deep sleep if the D3 state is programmed. **Power Well:** SUS
15:14	0x0 RW	**P3_ENTRY_TIMEOUT:** This field defines the timeout value to enter P3 mode in U2. 00: 7us 8us 01: 511us 512us 10: disables the timer (0us) 11: disables the timer (0us) **Power Well:** SUS
13	0x0 RW	**Enable U2 P3 Mode (EN_U2_P3):** 0: Disable U2 P3 mode 1: Enable U2 P3 mode **Power Well:** SUS
12:11	0x0 RW	**Fine Debug Mode Select (FINE_DM_SEL):** Reserved. **Power Well:** SUS
10	0x0 RW	**Enable Low Power State Based Core Clock Gating (EN_LP_CORE_CG):** When set to '1' enable core clock gating based on low power state entered **Power Well:** SUS
9	0x1 RW	**Disable USB3 Port Status Changed Event (DIS_U3_PORT_SCE):** 0: Enable USB3 port status change event generation if any change bit is not cleared 1: Disable USB3 port status change event generation if any change bit is not cleared Bit 12 default 0 **Power Well:** SUS
8:4	0x0 RW	**Debug Mode Select Register (DEB_MODE_SEL):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**Enable Auto Wakeup Non-IDLE (EN_AWAK_NIDLE):** When set to 1 enables the auto wakeup function when engine has identified non IDLE condition. **Power Well:** SUS
2	0x1 RW	**Enable PM Control P1 Exit P2 (EN_PMC_P1_EXIT_P2):** When set 1 enables the PM control module to transition to P1 instead of P0 when exit P2. **Power Well:** SUS
1	0x1 RW	**Enable PCIe PIPE CLK Isolation (EN_PP_CLK_ISOL):** When set to 1 enables the PCIe PIPE CLK to be isolated when main power is removed. **Power Well:** SUS
0	0x0 RW	**Enable P2 Overwrite P1 Allowed Detect (EN_P2OVRP1_ADET):** When set to 1 enables a function that can detect whether or not enable P2 overwrite P1 function. The condition to get to P2 overwrite is when engine is in idle conditions. This means that there is no ISO EP pending. **Power Well:** SUS

7.4.202 USB2 PHY Power Management Control (USB2_PHY_PMC)—Offset 8164h

Access Method

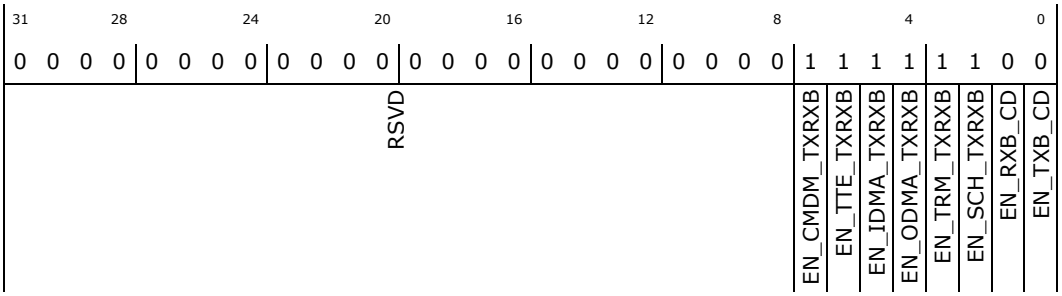
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8164h

Op Codes:

h - Read, h - Write

Default: 000000FCh



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7	0x1 RW	**EN_CMDM_TXRXB:** Enable Command Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy **Power Well:** Core
6	0x1 RW	**EN_TTE_TXRXB:** Enable TTE Active indication for Tx/Rx Bias circuit HS Phy PM Policy **Power Well:** Core
5	0x1 RW	**EN_IDMA_TXRXB:** Enable IDMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy **Power Well:** Core
4	0x1 RW	**EN_ODMA_TXRXB:** Enable ODMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy **Power Well:** Core
3	0x1 RW	**EN_TRM_TXRXB:** Enable Transfer Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy **Power Well:** Core
2	0x1 RW	**EN_SCH_TXRXB:** Enable Scheduler Active indication for Tx/Rx Bias circuit HS Phy PM Policy **Power Well:** Core
1	0x0 RW	**Enable Rx Bias ckt disable (EN_RXB_CD):** When set enables the Rx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits) **Power Well:** Core
0	0x0 RW	**Enable Tx Bias ckt disable (EN_TXB_CD):** When set enables the Tx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits) **Power Well:** Core

7.4.203 USB2 Phy Power Management Control 2 (USB2_PHY_PMC2)—Offset 8168h

Access Method

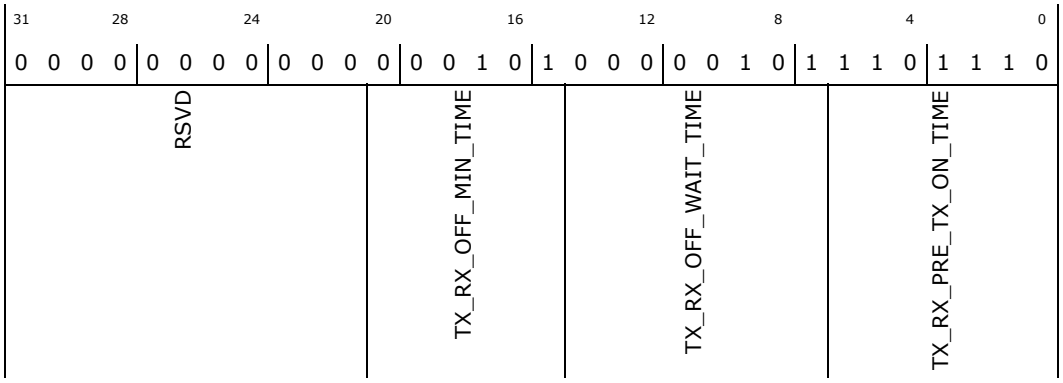
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8168h

Op Codes:

h - Read, h - Write

Default: 000282EEh



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
20:15	0x5 RW	**Tx/Rx Off Min Time (TX_RX_OFF_MIN_TIME):** Minimum number of clocks (uclk60x) for which Tx/Rx shall be switched off. This is used to decide if bias circuits can be switched off in the current micro-frame ahead of the next Tx/Rx. **Power Well:** Core
14:7	0x5 RW	**Tx/Rx Off Wait Time (TX_RX_OFF_WAIT_TIME):** Guardband time in number of clocks (uclk60x) before which Tx/Rx can be turned off when there is no activity **Power Well:** Core
6:0	0x6e RW	**Tx/Rx Pre Tx ON Time (TX_RX_PRE_TX_ON_TIME):** This is the time (in uclk60 clock periods) when Tx/Rx Bias needs to be turned on ahead of Transmit or Receive. This is based on the AFE requirement when bias needs to be ON before the transmit/receive occurs on the bus. **Power Well:** Core

7.4.204 xHCI Aux Clock Control Register (XHCI_AUX_CCR)—Offset 816Ch

Access Method

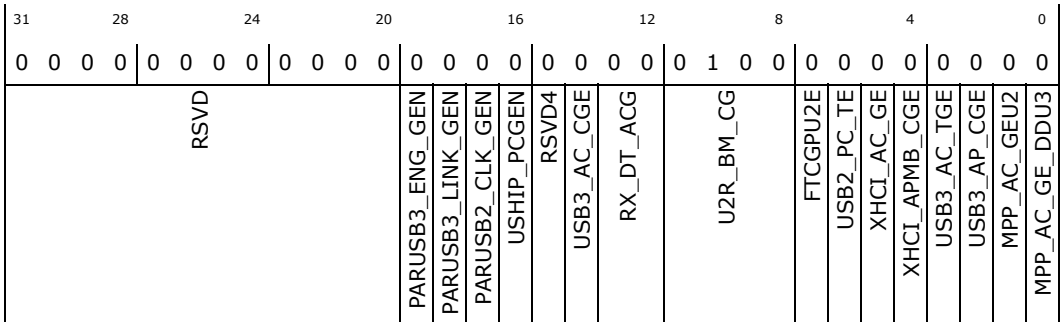
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 816Ch

Op Codes:

h - Read, h - Write

Default: 00000400h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**Reserved (RSVD):** Reserved.
19	0x0 RW	**USB3 Partition Engine/Link trunk gating Enable (PARUSB3_ENG_GEN):** When set to 1 enables gating of the SOSC trunk to the XHCI engine and link in the PARUSB3 partition. **Power Well:** SUS
18	0x0 RW	**USB3 Partition Frame Timer trunk gating Enable (PARUSB3_LINK_GEN):** When set to 1 enables gating of the SOSC trunk to the Frame timer in the PARUSB3 partition. **Power Well:** SUS
17	0x0 RW	**USB2 link partition clock gating enable (PARUSB2_CLK_GEN):** When set to 1 enables gating of the SOSC trunk to the USB2 link and Phy logic in the PARUSB2 partition. **Power Well:** SUS
16	0x0 RW	**USB2/USHIP 12.5 MHz partition clock gating enable (USHIP_PCGEN):** When set to 1 enables gating of the 12.5 MHz SOSC trunk to the USB2 and USHIP logic in the PARUSB2 partition. **Power Well:** SUS
15	0x0 RO	**Reserved1 (RSVD4):** Reserved
14	0x0 RW	**USB3 Port Aux/Core clock gating enable (USB3_AC_CGE):** When set, allows the aux_cclk clock into the USB3 port to be gated when conditions are met. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
13:12	0x0 RW	**Rx Detect Timer when port Aux Clock is Gated (RX_DT_ACG):** This field defines the value of the timer used to perform Rx Detect when port Aux Clock has been gated. 0x0: 100ms 0x1: 12ms Others: Reserved Note: This timer shall use the Fast Training Timer Tick (about 1us tick) for simulation purposes. For Fast Training mode, the above timeouts will become about 11us and about 100us, +/- implementation uncertainty, respectively. **Power Well:** SUS
11:8	0x4 RW	**U2 Residency Before ModPHY Clock Gating (U2R_BM_CG):** Before gating ModPHY Aux clock, Host Controller shall wait for this time in U2. This time is meant to ensure that the attached device has entered U2 as well. 0x0: 1us 0x1: 128us 0x2: 256us 0x3: 512us 0x4: 640us 0x5: 768us 0x6: 896us 0x7: 1024us Others: Reserved Note: This counter shall start counting once pipe has entered PS3 state in response to link in U2. **Power Well:** SUS
7	0x0 RW	**Frame Timer Clock Gating Ports in U2 Enable (FTCGPU2E):** This bit, when set, allows Host Controller to gate the clock to the Frame Timer when ports are in U2. **Power Well:** SUS
6	0x0 RW	**USB2 port clock throttle enable (USB2_PC_TE):** When set, allows the Aux clock into the USB2 ports to be throttled when conditions allow. **Power Well:** SUS
5	0x0 RW	**XHCI Engine Aux clock gating enable (XHCI_AC_GE):** When set, allows the aux clock into the XHCI engine to be gated when idle. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS
4	0x0 RW	**XHCI Aux PM block clock gating enable (XHCI_APMB_CGE):** When set, allows the aux clock into the Aux PM block to be gated when idle. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**USB3 Aux Clock Trunk Gating Enable (USB3_AC_TGE):** When set, allows Aux Clock Trunk feeding to USB3.0 ports to be gated when port Aux clock is gated at all USB3.0 ports and all USB3.0 modPHY instances. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS
2	0x0 RW	**USB3 Port Aux/Port clock gating enable (USB3_AP_CGE):** When set, allows the aux_pclk clock into the USB3 port to be gated when conditions are met. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS
1	0x0 RW	**ModPHY port Aux clock gating enable in U2 (MPP_AC_GEU2):** When set, allows the aux clock into the ModPhy to be gated when Link is in U2 and pipe has been in PS3 for at least the time defined by U2 Residency Before ModPHY Clock Gating field. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS
0	0x0 RW	**ModPHY port Aux clock gating enable in Disconnected, U3 or Disabled (MPP_AC_GE_DDU3):** When set, allows the aux clock into the ModPHY to be gated when Link is in Disconnected, U3 or Disabled state. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse. **Power Well:** SUS

7.4.205 USB LPM Parameters (USB_LPM_PARAM)—Offset 8170h

Access Method

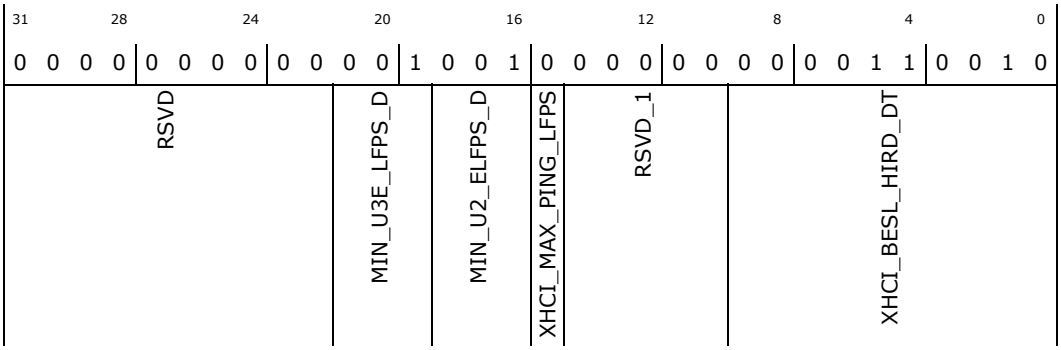
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8170h

Op Codes:

h - Read, h - Write

Default: 00090032h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
21:19	0x1 RW	**Min U3 Exit LFPS Duration (MIN_U3E_LFPS_D):** Min U3 Exit LFPS Duration This field defines the minimum duration of LFPS driven by Host Controller upon U3 exit LFPS handshake. Note that theres an uncertainty of +-16us in actual duration driven by the Host Controller. 0b000: 96us 0b001: 160us 0b010: 224us 0b011: 288us 0b100: 352us 0b101: 416us 0b110: 480us 0b111: 544us **Power Well:** SUS
18:16	0x1 RW	**Min U2 Exit LFPS Duration (MIN_U2_ELFPS_D):** Min U2 Exit LFPS Duration This field defines the minimum duration of LFPS driven by Host Controller upon U2 exit LFPS handshake. Note that theres an uncertainty of +-16us in actual duration driven by the Host Controller. 0b000: 96us 0b001: 160us 0b010: 224us 0b011: 288us 0b100: 352us 0b101: 416us 0b110: 480us 0b111: 544us **Power Well:** SUS
15	0x0 RW	**Max PING LFPS Rx Detection (XHCI_MAX_PING_LFPS):** This field defines the maximum timing for PING LFPS. If an incoming LFPS will be considered a PING if it has a timing such that it is less than or equal to the selected value. Otherwise it will be considered for the other types of LFPS. 0b Max PING LFPS timing set to 256 ns (32 link clocks) 1b Max PING LFPS timing set to 320 ns (40 link clocks) **Power Well:** SUSe
14:10	0x0 RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
9:0	0x32 RW	**xHCI BESL to HIRD Distance (XHCI_BESL_HIRD_DT):** This field defines the gap between BESL and duration of Resume signalling from Host upon Host Initiated Resume from USB2.0 LPM. Default value of this register corresponds to xHCI spec defined 50us value. Value BESL to HIRD Distance 000h 0us 001h 1us 002h 2us 3FFh 1023us **Power Well:** SUS

7.4.206 xHC Latency Tolerance Parameters - LTV Control (XLTP_LTV1)—Offset 8174h

Access Method

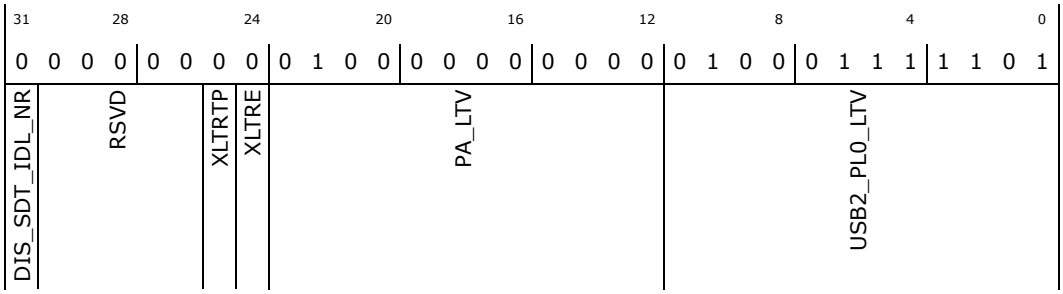
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8174h

Op Codes:

h - Read, h - Write

Default: 0040047Dh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Disable scheduler direct transition from IDLE to NO requirement (DIS_SDT_IDL_NR):** 0: (default) allow scheduler direct transition from IDLE to NO requirement 1: Disable scheduler direct transition from IDLE to NO requirement **Power Well:** Core
30:26	0x0 RW	**Reserved (RSVD):** Reserved. **Power Well:** Core
25	0x0 RW	**XHCI LTR Transition Policy (XLTRTP):** When '0', LTR messaging state machine transitions from High, Medium, or Low LTR states to Active state upon the Alarm Timer timout and stays in Active until the next service boundary. When '1', the LTR messaging state machine transitions through High ? Med ? Low ? Active states assuming enough latency is available for each transition. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
24	0x0 RW	**XHCI LTR Enable (XLTRE):** This bit must be set to enable LTV messaging from XHCI to the PMC. **Power Well:** Core
23:12	0x400 RW	**Periodic Active LTV (PA_LTV):** 23:22 Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 21:12 Latency Value (ns) Defaults to 0 micro seconds **Power Well:** Core
11:0	0x47d RW	**USB2 Port L0 LTV (USB2_PL0_LTV):** 11:10 Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 9:0 Latency Value (ns) Defaults to 128 Micro Seconds **Power Well:** Core

7.4.207 xHC Latency Tolerance Parameters LTV Control 2 (XLTP_LTV2)—Offset 8178h

Access Method

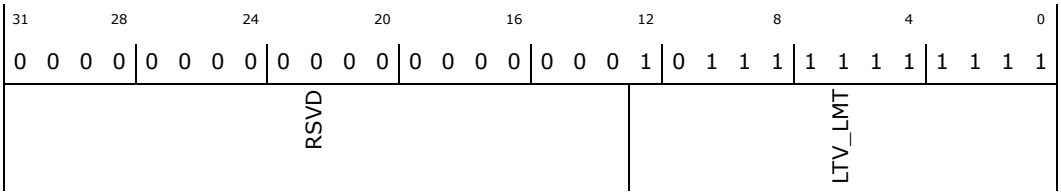
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8178h

Op Codes:

h - Read, h - Write

Default: 000017FFh



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12:0	0x17ff RW	**LTV Limit (LTV_LMT):** This register defines a maximum LTR value that is allowed to be advertised to the PMC. This is meant to be used as a workaround or mitigation if issues are discovered with the LTR values generated by the XHC using the defined algorithms. If the LTR value of the XHC is larger than the value in this register field, the value in this field is sent to the PMC instead. Default value is the highest possible - 101b 12:10: Latency Multiplier Field 000b - Value times 1 ns 001b - Value times 32 ns 010b - Value times 1,024 ns 011b - Value times 32,768 ns 100b - Value times 1,048,576 ns 101b - Value times 33,554,432 ns 110b-111b - Not Permitted 9:0: Latency Value Default = 3FFh **Power Well:** Core

7.4.208 xHC Latency Tolerance Parameters - High Idle Time Control (XLTP_HITC)—Offset 817Ch

Access Method

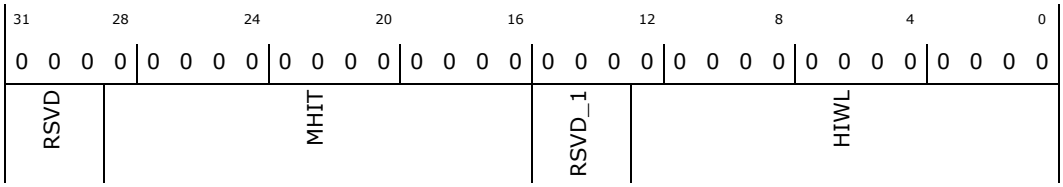
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 817Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
28:16	0x0 RW	**Minimum High Idle Time (MHIT):** LTR value can be indicated. This value must be larger than HIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds) **Power Well:** Core
15:13	0x0 RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12:0	0x0 RW	**High Idle Wake Latency (HIWL):** This is the latency to access memory from the High Idle Latency state. This value must be larger than MIWL and LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds) **Power Well:** Core

7.4.209 xHC Latency Tolerance Parameters - Medium Idle Time Control (XLTP_MITC)—Offset 8180h

Access Method

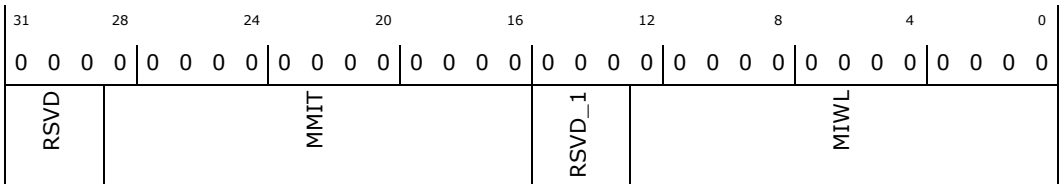
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8180h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
28:16	0x0 RW	**Minimum Medium Idle Time (MMIT):** LTR value can be indicated. This value must be larger than MIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds) **Power Well:** Core
15:13	0x0 RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core
12:0	0x0 RW	**Medium Idle Wake Latency (MIWL):** This is the latency to access memory from the Medium Idle Latency state. This value must be larger than LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds) **Power Well:** Core

7.4.210 xHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)—Offset 8184h

Access Method

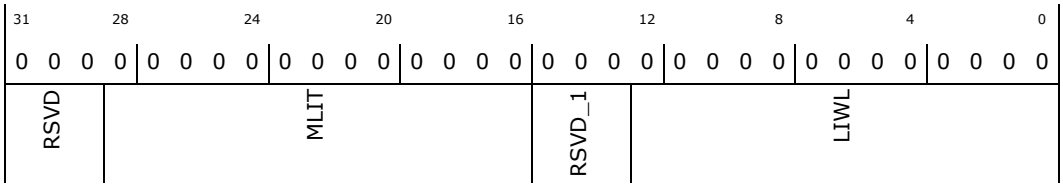
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8184h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
28:16	0x0 RW	**Minimum Low Idle Time (MLIT):** LTR value can be indicated. This value must be larger than LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds) **Power Well:** Core
15:13	0x0 RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core
12:0	0x0 RW	**Low Idle Wake Latency (LIWL):** This is the latency to access memory from the Medium Idle Latency state. 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds) **Power Well:** Core

7.4.211 HOST_CTRL_BW_MAX3_REG—Offset 8188h

Added for SoC

Access Method

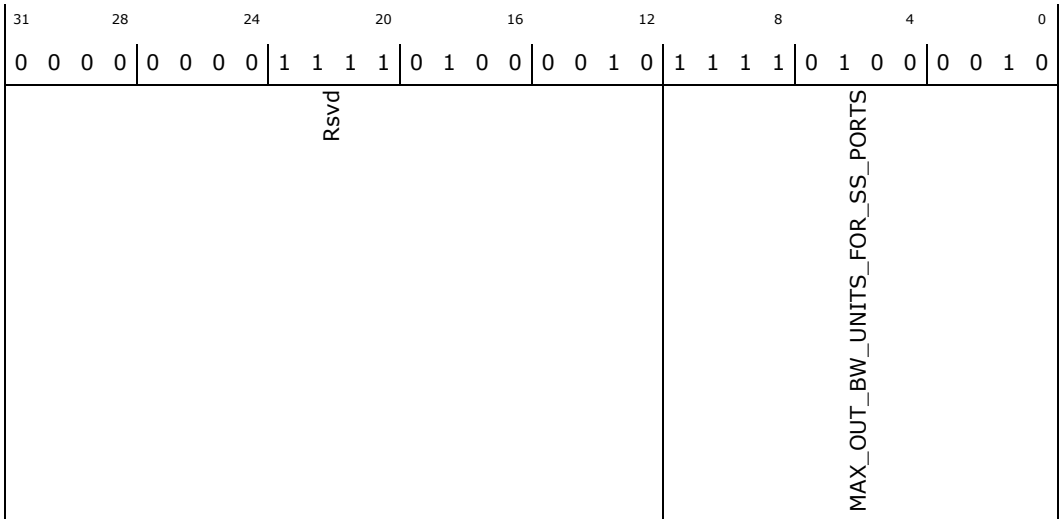
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8188h

Op Codes:

h - Read, h - Write

Default: 00F42F42h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0xf42 RO	**Rsvd:** Reserved. **Power Well:** Core
11:0	0xf42 RW	**MAX_OUT_BW_UNITS_FOR_SS_PORTS:** Max. Number of OUT BW units for SS ports - denominator in 90% calculation **Power Well:** Core

7.4.212 PDDIS_REG—Offset 8198h

Access Method

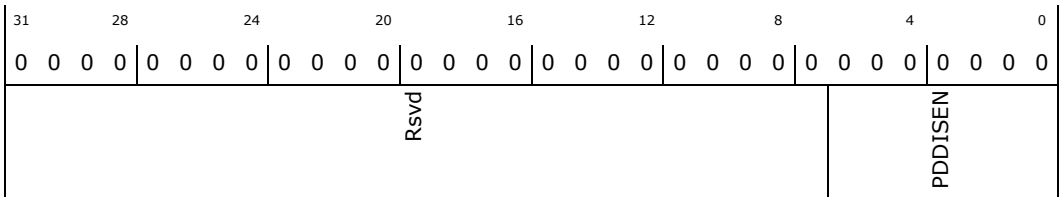
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8198h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**Rsvd:** Reserved. **Power Well:** SUS
6:0	0x0 RW	**PDDISEN:** Reserved. **Power Well:** SUS

7.4.213 THRM_HOST_CTRL_REG—Offset 819Ch

Access Method

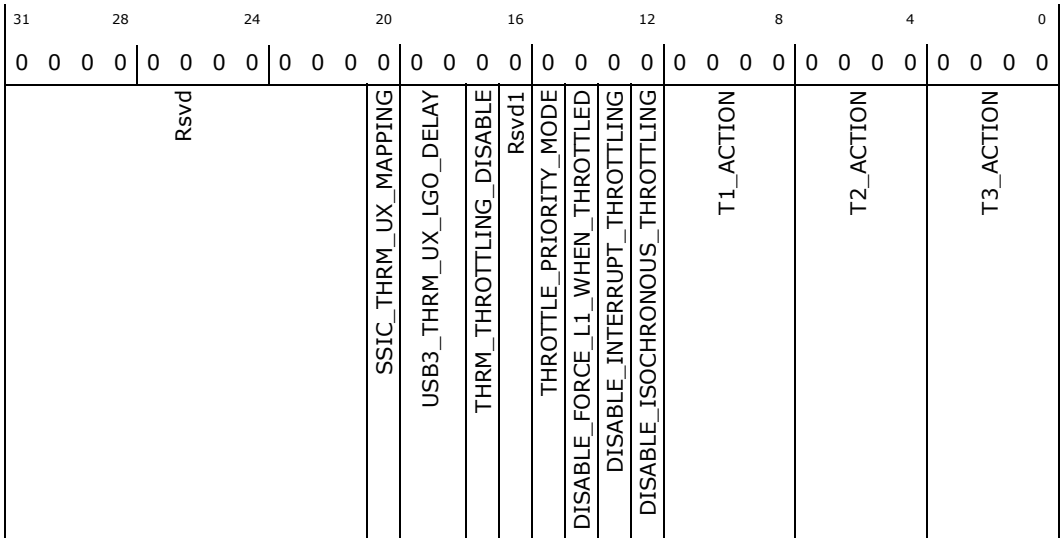
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 819Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core
20	0x0 RW	**SSIC Thermal Throttle Ux Mapping (SSIC_THRM_UX_MAPPING):** Controls if U1 or U2 is forced upon the start of thermal throttle OFF period. 0 Force ports into U2 during Thermal Throttle triggered Ux entry. 1 Force ports into U1 during Thermal Throttle triggered Ux entry. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
19:18	0x0 RW	**USB3 Thermal Throttle Ux LGO delay (USB3_THRM_UX_LGO_DELAY):** Controls the delay enforced between LMP for FLPMA and LMP for Ux LGO. After sending LPMA ON , wait for pre-defined number of clocks to initiate LGO_U1/LGO_U2 00: 8 clocks 01: 32 clocks 10: 128 clocks 11: 0 clocks This field does not apply to ports that are not operating in the mode required to issue FLMA ON. **Power Well:** Core
17	0x0 RW	**THRM_THROTTLING_DISABLE:** 0: Thermal throttling is enabled. 1: Thermal throtling is disabled. The host controller ignores the TT control inputs and does not throttle. **Power Well:** Core
16	0x0 RO	**Rsvd (Rsvd1):** Reserved. **Power Well:** Core
15	0x0 RW	**THROTTLE_PRIORITY_MODE:** 0: Off period has priority: In this case, when the throttle signal is asserted, the host controller enters the off state on the next uframe boundary, and stays in the off state for the prescribed duration or until the end of the 16 uframe throttle period whichever occurs first. On subsequent throttle periods, the off period occurs first and then the on period. 1: The On period has priority: In this case, when the throttle signal is asserted, the host controller completes the required On period first before entering the off period. If the required number of uFrames has already been executed in a 16 uframe throttle window, the controller enters the off period immediately. **Power Well:** Core
14	0x0 RW	**DISABLE_FORCE_L1_WHEN_THROTTLED:** 0: USB2 port will not force L1 entry on throttled ports. L1 entry will be based on the normal idle timeout 1: USB2 ports will attempt to enter L1 immediately after throttled ports are idle. **Power Well:** Core
13	0x0 RW	**DISABLE_INTERRUPT_THROTTLING:** 0: Interrupt traffic is throttled 1: Interrupt traffic is not throttled **Power Well:** Core
12	0x0 RW	**DISABLE_ISOCHRONOUS_THROTTLING:** 0: Isochronous traffic is throttled 1: Isochronous traffic is not throttled **Power Well:** Core
11:8	0x0 RW	**T1_ACTION:** # bus intervals to be idle for async traffic out of the 16 interval master period; from 0 to 15. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**T2_ACTION:** # bus intervals to be idle for async traffic out of the 16 interval master period; from 0 to 15. **Power Well:** Core
3:0	0x0 RW	**T3_ACTION:** # bus intervals to be idle for async traffic out of the 16 interval master period; from 0 to 15. **Power Well:** Core

7.4.214 LFPS_PM_CTRL_REG—Offset 81A0h

Access Method

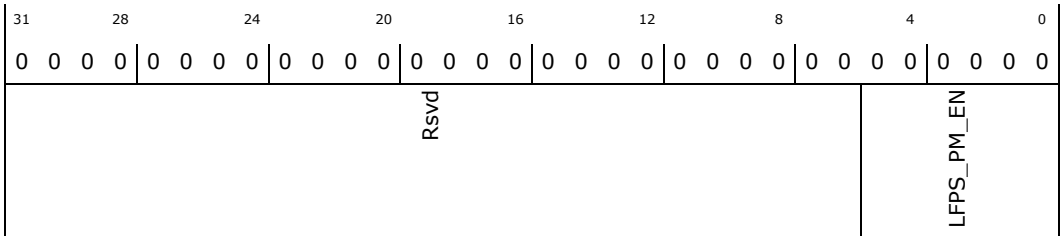
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 81A0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**Rsvd:** Reserved. **Power Well:** SUS
5:0	0x0 RW	**LFPS_PM_EN:** Reserved. **Power Well:** SUS

7.4.215 U2PDM—Offset 81A4h

Access Method

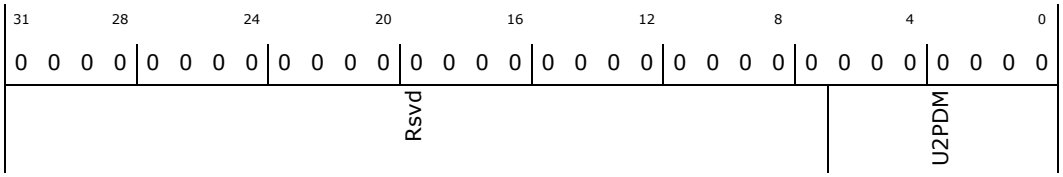
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 81A4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core
6:0	0x0 RW	**U2PDM:** Reserved. **Power Well:** Core

7.4.216 U2PCM—Offset 81A8h

Access Method

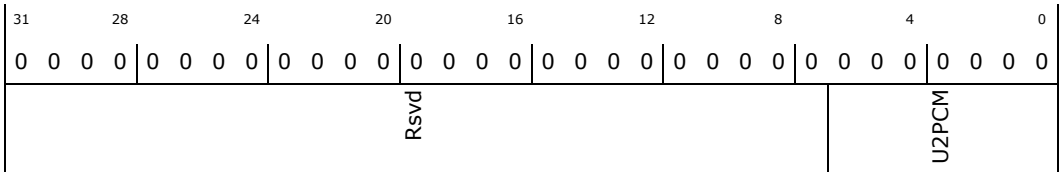
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 81A8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core
6:0	0x0 RW	**U2PCM:** Reserved. **Power Well:** Core

7.4.217 U3PDM—Offset 81ACh

Access Method

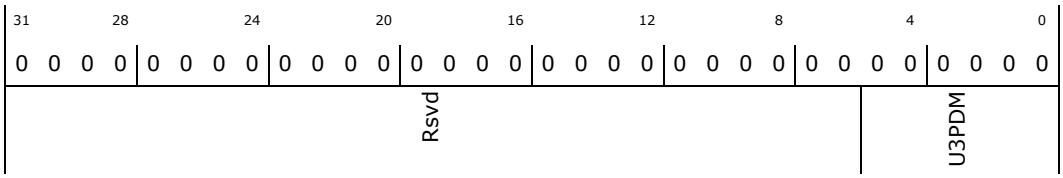
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 81ACh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core
5:0	0x0 RW	**U3PDM:** Reserved. **Power Well:** Core

7.4.218 U3PCM—Offset 81B0h

Access Method

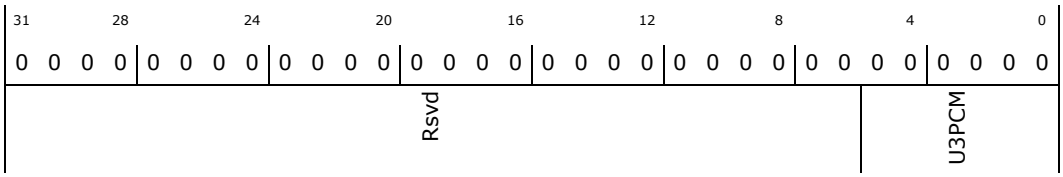
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 81B0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core
5:0	0x0 RW	**U3PCM:** Reserved. **Power Well:** Core

7.4.219 LFPSONCOUNT_REG—Offset 81B8h

Access Method

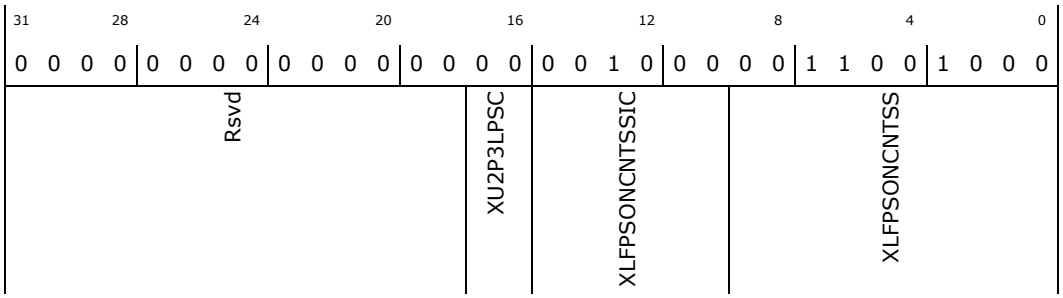
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 81B8h

Op Codes:

h - Read, h - Write

Default: 000020C8h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0x0 RO	**Rsvd:** Reserved. **Power Well:** SUS
17:16	0x0 RW	**U2P3 LFPS Periodic Sampling Control (XU2P3LPSC):** This field controls the OFF time for the LFPS periodic sampling for SS and SSIC ports in U2P3. If LFPSPM for a port is 1, it will override the OFF time and LFPS receiver will remain OFF permanently. For Fast Sim mode, 500us will be equivalent to 5us. 0x0 Polling Disable. (RXDET Polling will become 100ms.) 0x1 500us OFF Time 0x2 1ms OFF Time 0x3 1.5ms OFF Time **Power Well:** SUS
15:10	0x8 RW	**XLFPSONCNTSSIC:** This time would describe the number of clocks SSIC LFPS will remain ON. SSIC LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 8. **Power Well:** SUS
9:0	0xc8 RW	**XLFPSONCNTSS:** This time would describe the number of clocks LFPS will remain ON. LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 200. **Power Well:** SUS

7.4.220 reg_D0i2_CTRL_REG_type (D0i2_CTRL_REG)—Offset 81BCh

Access Method

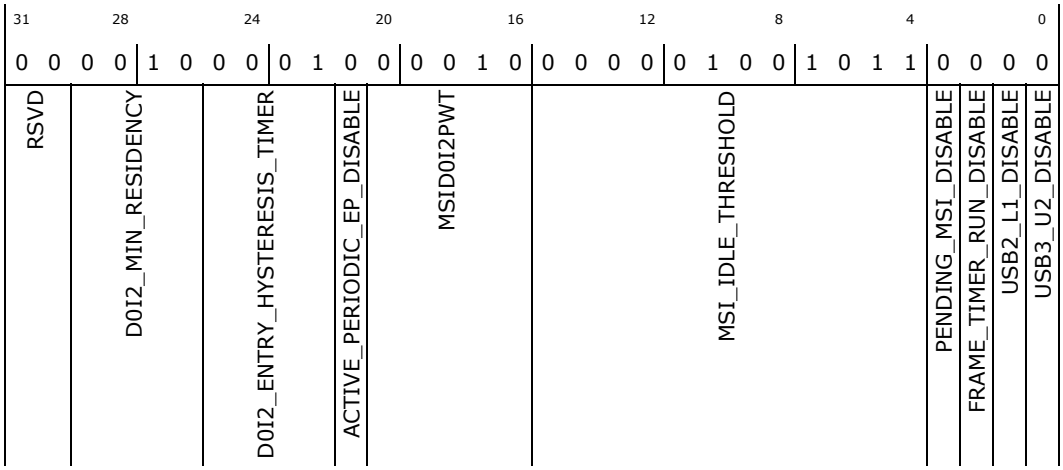
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 81BCh

Op Codes:

h - Read, h - Write

Default: 084204B0h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
29:26	0x2 RW	**D0i2 Minimum Residency (D0I2_MIN_RESIDENCY):** This field controls the minimum time that we must stay in D0i2 to ensure that the entry sequence has settled before we attempt to exit. 0h Disabled 1h 8 clocks 2h 16 clocks 3h 32 clocks 4h 128 clocks 5h 256 clocks 6h 512 clocks 7h 1024 clocks **Power Well:** SUS
25:22	0x1 RW	**D0i2 Entry Hysteresis Timer (D0I2_ENTRY_HYSTERESIS_TIMER):** This field allows for a hysteresis timer to be implemented specifically for D0i2. This will allow for D0i2 entry to be controlled independently from the timer used for D0i3 and D3. 0h Disabled 1h 8 clocks 2h 16 clocks 3h 32 clocks 4h 64 clocks 5h 128 clocks 6h 256 clocks 7h 512 clocks **Power Well:** SUS
21	0x0 RW	**Active Periodic EP Disable (ACTIVE_PERIODIC_EP_DISABLE):** This field allows the xHC to control how aggressive it enters D0i2 in the presence of active Periodic EPs. Setting this field will allow D0i2 only when there are no active Periodic EPs on the schedule. Either there are no active DB or any active Interrupt EP is flow controlled. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
20:16	0x2 RW	**MSI D0i2 Pre Wake Time (MSID0I2PWT):** This is the latency that is expected to be incurred to exit the D0i2 state. This wake latency is the latency to be added to the tracked D0i2 wake by the MSI module. Example: If while allowing D0i2 there is an MSI generation that will trigger in 250 us from now ,the MSI module will trigger a D0i2 wake up 250 us MSI D0i2 Pre Wake Time. The D0I2WL is to ensure that the act of D0i2 exit does not impact the action(s) required by the alarm(s) that was enabled prior to D0i2. 3:0 250 ns ticks 0h 0 ns 1h 250 ns . 1Fh 3750 ns **Power Well:** SUS
15:4	0x4b RW	**MSI Idle Threshold (MSI_IDLE_THRESHOLD):** This field allows the xHC to control how aggressive it enters D0i2 in the presence of pending MSI. This field is valid only if Pending MSI Disable is 0, allowing D0i2 in the presence of pending MSIs. D0i2 will be prevented if the amount of idle time between Event Ring being idle to the time an MSI will be generated does not exceed this time. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124) **Power Well:** SUS
3	0x0 RW	**Pending MSI Disable (PENDING_MSI_DISABLE):** This field allows the xHC to disable D0i2 when there are pending MSIs in the event manager. Setting this field will require all IMOD counters to be 0h and all MSIs delivered. Clearing this field will allow for D0i2 power gating while there are 1 or more IMOD counters decrementing which implies that an MSI is pending and will be generated once the corresponding IMOD counter reaches 0h. **Power Well:** SUS
2	0x0 RW	**Frame Timer Run Disable (FRAME_TIMER_RUN_DISABLE):** This field allows the xHC to disable D0i2 when the frame timer is running. Clearing this field will allow D0i2 when the frame timer is required as defined in the XHCI Spec. Setting this field will not allow D0i2 when the frame timer is required and will limit D0i2 for the condition where the frame timer is not required. **Power Well:** SUS
1	0x0 RW	**USB2 L1 Disable (USB2_L1_DISABLE):** This field allows the xHC to disable D0i2 when USB2 ports are in L1. This implies that D0i2 will only be triggered when ports are in L2 or deeper. **Power Well:** SUS
0	0x0 RW	**USB3 U2 Disable (USB3_U2_DISABLE):** This field allows the xHC to disable D0i2 when USB3 ports are in U2. This implies that D0i2 will only be triggered when ports are in U3 or deeper. **Power Well:** SUS

7.4.221 reg_D0i2_SCH_ALARM_CTRL_REG_type (D0i2_SCH_ALARM_CTRL_REG)—Offset 81C0h

Access Method

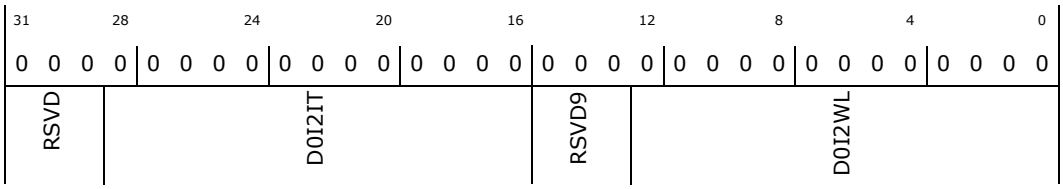
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 81C0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** SUS
28:16	0x0 RO	**D0i2 Idle Time (D0I2IT):** This is the minimum schedule idle time that must be available before D0i2 can allowed. 12:7 Time value in # of 125s Bus Intervals (0 8ms) 6:0 Fractional BI Time value in s (0 124s) This field controls how much scheduler idle time is required to trigger D0i2. The scheduler idle time is the same idle time that is used by other functions implementing alarm timers such as PLL shutdown, LTR and USB2 L1 override. If there is a need to require other alarm timers to have been set such as LTR has triggered a Low Idle time, then this field needs to be as aggressive as LTR Low Min Idle Time to ensure D0i2 is triggered once the scheduler has detected IDLE in the schedule. This is only to be used as alternate modes of operation or back up modes. **Power Well:** SUS
15:13	0x0 RO	**Reserved (RSVD9):** Reserved. **Power Well:** SUS
12:0	0x0 RW	**D0i2 Wake Latency (D0I2WL):** This is the latency that is expected to be incurred to exit the D0i2 state. This wake latency is the latency to be added to the tracked D0i2 wake by the scheduler. Example: If while allowing D0i2 there is an alarm that will trigger in 250 us from now , the scheduler will allow D0i2 and track this alarm with an adjustment to wake up 250ns D0I2WL) from. The D0I2WL is to ensure that the act of D0i2 exit does not impact the action(s) required by the alarm(s) that was enabled prior to D0i2. 12:7 Time value in # of 125s Bus Intervals (0 8ms) 6:0 Fractional BI Time value in s (0124s) **Power Well:** SUS

7.4.222 reg_USB2PMCTRL_REG_type (USB2PMCTRL_REG)—Offset 81C4h

Access Method

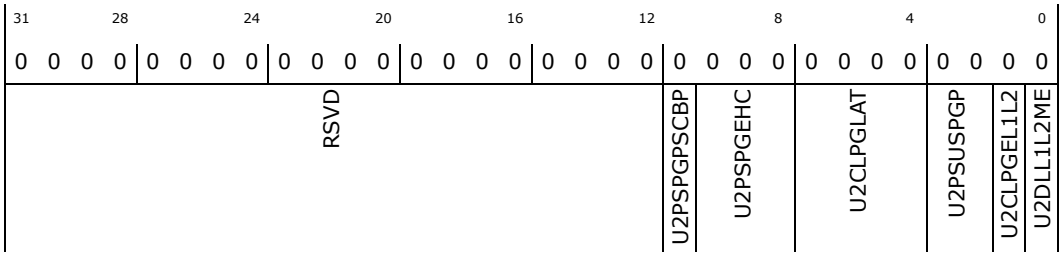
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 81C4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** SUS
11	0x0 RW	**USB2 PHY SUS Power Gate PORTSC Block Policy (U2PSPGPSCBP):** This controls the policy for blocking PORTSC Updates while the USB2 PHY SUS Well is power gated. When set, the controller will block any updates to the PORTSC caused by port status change if the USB2 PHY SUS is power gated. 0 Do not **Power Well:** SUS
10:8	0x0 RW	**USB2 PHY SUS Well Power Gate Entry Hysteresis Count (U2PSPGEHC):** This controls the amount of hysteresis time the controller will enforce after detecting the USB2 PHY SUS Power Gate entry condition. 0h 0 clocks 1h 32 clocks 2h 64 clocks 3h 128 clocks 4h 256 clocks 5h 512 clocks 6h 1024 clocks 7h 2048 clocks **Power Well:** SUS
7:4	0x0 RW	**USB2 PHY SUS Power Gate PORTSC Block Policy (U2CLPGLAT):** This field represents the worst case latency for the USB2 Common Lane to enter and exit its power gate state. This fields is required to be compared to a ports HIRD/HIRD value for the ports that have allowed L1 to L2 mapping to determine if the Common Lane can be allowed to power off. If the power gate entry/exit latency is greater than the HIRD/HIRDD then the common lane should not be allowed to power gate as this will result in a L1 exit violation. 0h 100 us 1h 200 us 2h 300 us Eh 1500us Fh 1600 us **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
3:2	0x0 RW	**USB2 PHY SUS Well Power Gate Policy (U2PSUSPGP):** This field controls when to enable the USB2 PHY SUS Well Power Gating when the proper conditions are met. 00 USB2 PHY SUS Power Gating is Disabled. 01 USB2 PHY SUS Power Gating is Enabled in Only D0 and D0i2 (Excludes D0i3 and D3) 10 USB2 PHY SUS Power Gating is Eanabled in only in D0, D0i2 and D0i3 (Excludes D3) 11 USB2 PHY SUS Power Gating is Eanabled in D0/D0i2/ D0i3/D3 **Power Well:** SUS
1	0x0 RW	**USB2 Common Lane Power Gating Enable During L1 to L2 Mapping for USB2 PHY Power Gating (U2CLPGEL1L2):** This field when set enables the controller to allow for the common lane power gating to be enabled when all ports are exposed as in L2 to the USB2 PHY while at least 1 port has been mapped to L2 from L1. This field alone does not guarantee power gating since the L1 HIRD/HIRDD Value must be compared with the PHYs power gate exit latency (U2CLPGLAT) held in this register to ensure that L1 exit is not violated. 0 USB2 Common Lane Power Gating is disabled when any port has been mapped from L1 to L2. 1 USB2 Common Lane Power Gating is allowed when any port has been mapped to L2 from L1 with the additional condition that the HIRD/HIRDD is greater than the PHYs Power Gate exit latency. **Power Well:** SUS
0	0x0 RW	**USB2 Data Lane L1 to L2 Mapping Enable for USB2 PHY Power Gating (U2DLL1L2ME):** This field when set enables the controller to map an L1 entry directly to L2 to allow the USB2 PHY to trigger its Autonomous Power Gating. The USB2 PHY will trigger PG only when in L2 since it does not fully understand the requirements for L1. 0 USB2 L1 to L2 mapping is disabled for all ports 1 USB2 L1 to L2 mapping is enabled for all ports **Power Well:** SUS

7.4.223 FUS1_REG—Offset 8410h

Access Method

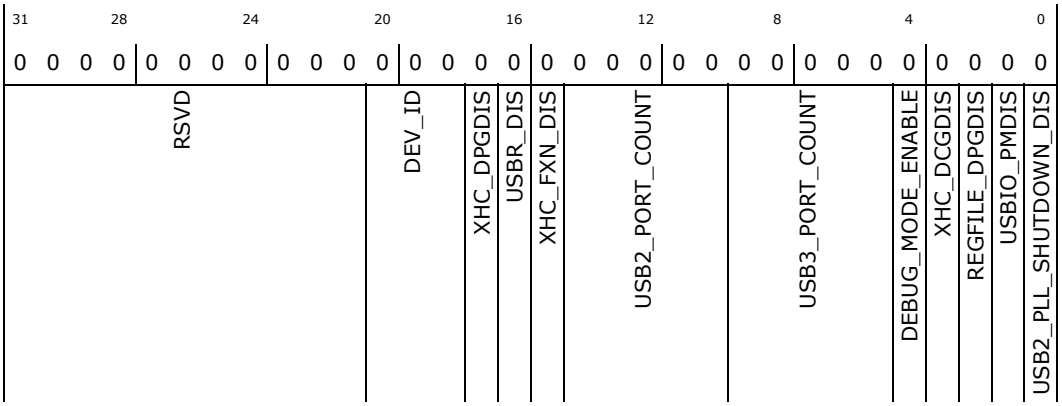
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8410h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RO	**RSVD:** Reserved. **Power Well:** Core
20:18	0x0 RO	**DEV_ID:** Provides a fuse over-ride for the lower 3 bits of device ID. **Power Well:** Core
17	0x0 RO	**XHC_DPGDIS:** When asserted, it indicates that the xHCI will not dynamically power gate the controller. **Power Well:** Core
16	0x0 RO	**USBR_DIS:** When asserted, it indicates that xHCI does not support USBr **Power Well:** Core
15	0x0 RO	**XHC_FXN_DIS:** When asserted, it indicates the xHCI is fused to function disabled. **Power Well:** Core
14:10	0x0 RO	**USB2_PORT_COUNT:** 0x0 = MAX USB2 Ports enabled 0x1 = Max USB2 Ports -1 enabled 0x1F = All ports disabled **Power Well:** Core
9:5	0x0 RO	**USB3_PORT_COUNT:** 0x0 = MAX USB3 Ports enabled 0x1 = Max USB3 Ports -1 enabled 0x1F = All ports disabled **Power Well:** Core
4	0x0 RO	**DEBUG_MODE_ENABLE:** 0 = USB debug mode disabled 1 = USB debug mode enabled. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RO	**XHC_DCGDIS:** 0= USB3 (xHC) dynamic clock gating enabled 1= USB3 (xHC) dynamic clock gating disabled **Power Well:** Core
2	0x0 RO	**REGFILE_DPGDIS:** 0 = USB3 (xHC) dynamic RF power gating enabled 1 = USB3 (xHC) dynamic RF power gating disabled **Power Well:** Core
1	0x0 RO	**USBIO_PMDIS:** 0=USB2 HW LPM and USB3 HW Ux under xHC enabled 1= USB2 HW LPM and USB3 HW Ux under xHC disabled **Power Well:** Core
0	0x0 RO	**USB2_PLL_SHUTDOWN_DIS:** 0= USB2 PLL Shutdown enabled 1= USB2 PLL Shutdown disabled **Power Well:** Core

7.4.224 DFT_REG1—Offset 8430h

Access Method

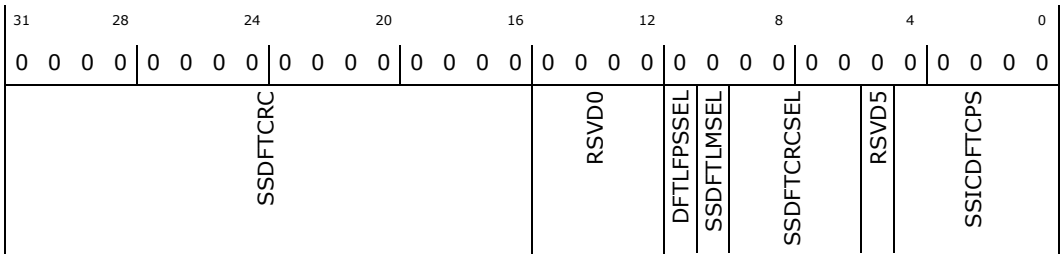
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8430h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**SS/SSIC DFT CRC (SSDFTCRC):** These register bits contain the value of SS DFT CRC **Power Well:** Core
15:12	0x0 RO	**RSVD0:** RSVD0 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11	0x0 RW	**DFTLFPSSEL:** DFTLFPSSEL 0: Rxelecidle is driven from GPIO Pin 1: Rxelecidle is Driven as specified by Super Speed DFT LFPS Mode Select **Power Well:** Core
10	0x0 RW	**Super Speed DFT LFPS Mode Select (SSDFTLMSEL):** This bit selects the Super Speed DFT LFPS mode, and will only take effect when Super Speed HBP mode is enabled. 0b: HBP logic will internally loopback TX LFPS as RX LFPS and AFE RX LFPS path to the controller is disconnected. 1b: RX LFPS path works normally **Power Well:** Core
9:6	0x0 RW	**SS/SSIC DFT CRC Select (SSDFTCRCSEL):** These bits select which Super Speed DFT CRC value is reflected in SSDFTCRC bits. In addition, these bits also select which SuperSpeed DFT CRC MSB value is sent to GPIO monitor pin, i.e. sata3gp_gp37 to aid silicon debug. Live version of selected CRC's MSB will be- sent to GPIO monitor pin, i.e. sata3gp_gp37. 0h (default): No SuperSpeed DFT CRC is selected. 1h: Data Payload CRC 2h: Link Management Packet CRC 3h: Transaction Packet CRC 4h: Isochronous Timestamp Packet CRC 5h: Data Packet Header CRC 6h: Link Command Packet CRC 7h: RRAP Packet CRC 8h: Tx/Rx Cfg CRC Others: Reserved Note : CRC types 7 and 8 are onlyapplicable if Port is SSIC Port **Power Well:** Core
5	0x0 RO	**RSVD5:** RSVD5 **Power Well:** Core
4:0	0x0 RW	**SS/SSIC DFT CRC Port Select (SSICDFTCPS):** One CRC per packet type is shared for all the Super Speed ports. These bits select the Super Speed port for which CRC data will be updated. 000b: (default) No SuperSpeed Port is selected 001b: SS/SSIC Port 0 010b: SS/SSIC Port 1 011b: SS/SSIC Port 2 100b: SS/SSIC Port 3 101b: SS/SSIC PORT4 110b :SS/SSIC Port 5 others : Rsvd **Power Well:** Core

7.4.225 DFT_REG2—Offset 8434h

Access Method

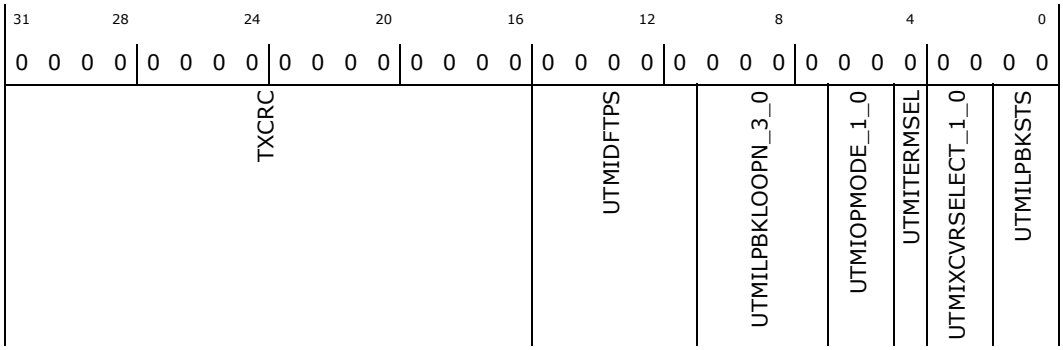
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8434h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**HS/HSIC TX CRC (TXCRC):** These register bits contain the value of TX CRC. This TX CRC is placed right after the 480MHz XCLKQ. **Power Well:** Core
15:11	0x0 RW	**HSIC/UTMI+ DFT Port Select (UTMIDFTPS):** One CRC is shared for all the UTMI+ ports. These bits select the UTMI+ port for which CRC data will be updated and loopback status reflected in UTMILPBKSTS. 0h: (default) No UTMI+ Port is selected 1h: UTMI+ Port 0 2h: UTMI+ Port 1 3h: UTMI+ Port 2 4h: UTMI+ Port 3 5h: UTMI+ Port 4 6h: UTMI+ Port 5 7h: UTMI+ Port 6 8h: UTMI+ Port 7 9h: UTMI+ Port 8 Ah: UTMI+ Port 9 Bh: UTMI+ Port 10 Ch: UTMI+ Port 11 Dh: UTMI+ Port 12 Eh: UTMI+ Port 13 Others: Reserved **Power Well:** Core
10:7	0x0 RW	**Loop Number (UTMILPBKLOOPN_3_0):** Number of repeatable fixed pattern within a packet Note: Connect register bit 3 to counter bit 7, register bit 2 to counter bit 5, register bit 1 to counter bit 3, register bit 0 to counter bit 1. Counter bits 6, 4, 2 and 0 will be tied off to 0. Hence, the programmable loop number shall be: 0000b: 0 loop 0001b: 2 loops 0010b: 8 loops 0011b: 10 loops 1100b: 160 loops 1101b: 162 loops 1110b: 168 loops 1111b: 170 loops (max) +E27 **Power Well:** Core
6:5	0x0 RW	**Operational Mode (UTMIOPMODE_1_0):** Operational Mode in test mode. These signals select between various operational modes: 00b: Normal Operation 01b: Non-Driving 10b: Disable Bit Stuffing and NRZI encoding 11b: Reserved **Power Well:** Core
4	0x0 RW	**Termination Select (UTMITERMSEL):** Termination Select in test mode. This signal selects between the FS and HS terminations: 0b: HS termination enabled 1b: FS termination enabled **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3:2	0x0 RW	**Transceiver Select (UTMIXCVRSELECT_1_0):** Transceiver Select in test mode. This signal selects between the LS, FS and HS transceivers: 00b: HS transceiver enabled 01b: FS transceiver enabled 10b: LS transceiver enabled 11b: Reserved **Power Well:** Core
1:0	0x0 RW	**UTMI+ Loopback Status (UTMILPBKSTS):** Loopback Status for port selected by UTMIDFTPS 00b: Reset condition 01b: Comparator has started receiving data and the received data matches with the TX pattern. 10b: Comparator has started receiving data the received data does not match with the TX pattern but there was no assertion of RC error from UTMI. 11b: Comparator has started receiving data and RX ERROR was asserted for at least one clock by UTMI. Note that this does not reflect the status of pattern comparison since RX error from UTMI is unexpected for loopback. **Power Well:** Core

7.4.226 DFT_REG3—Offset 8438h

Access Method

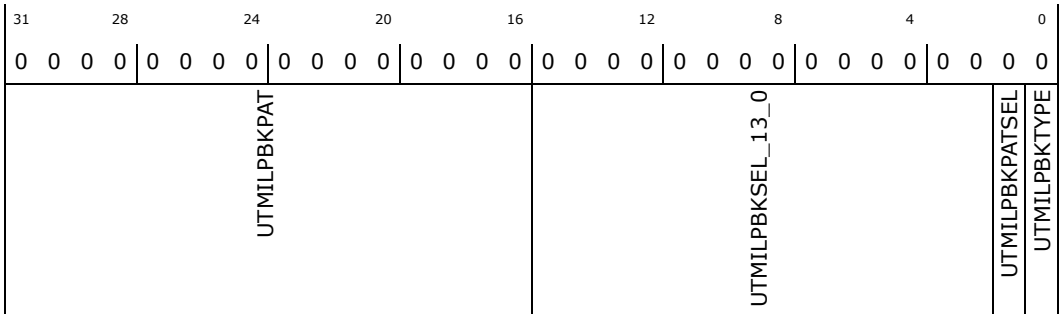
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8438h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Loopback Pattern (UTMILPBKPAT):** 2-byte pattern for loopback Note: This 2-byte pattern will be replicated to the upper 2-byte to form the DW pattern **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:2	0x0 RW	**Loopback Lane Select (UTMILPBKSEL_13_0):** Port is selected if the corresponding bit is selected Note: MSB is for UTMI+ Port13, LSB is for UTMI+ Port0 **Power Well:** Core
1	0x0 RW	**Loopback Pattern (UTMILPBKPATSEL):** Near end loopback pattern generation type: 0b: Fixed pattern 1b: USB2 test packet **Power Well:** Core
0	0x0 RW	**Loopback Type (UTMILPBKTYPE):** Loopback Type in test mode. This signal selects between DNELB and ANELB, and will only take effect if DTUTMILPBKEN is set. 0b: Digital Near-End Loopback (DNELB) 1b: Analog Near-End Loopback (ANELB) Note: Analog Far-End Loopback (AFELB) is not supported **Power Well:** Core

7.4.227 dft_reg4 (DFT_REG4)—Offset 843Ch

Access Method

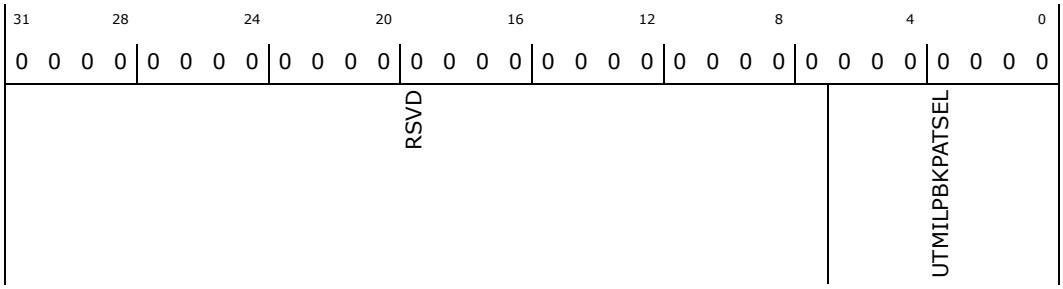
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 843Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RW	**RSVD:** Reserved. **Power Well:** Core
6:0	0x0 RW	**Loopback Pattern (UTMILPBKPATSEL):** Loopback Lane Select (UTMILPBKSEL): Port is selected if the corresponding bit (zero based) is selected Bit 0 = Port 1 Bit 1 = Port 2 Etc. **Power Well:** Core

7.4.228 dft_reg5 (DFT_REG5)—Offset 8440h

Access Method

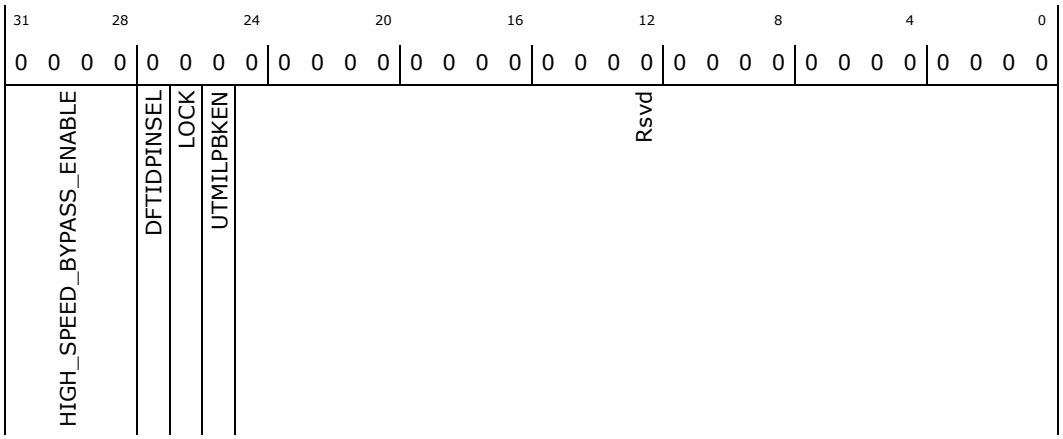
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8440h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RW/L	**High Speed Bypass Enable (HIGH_SPEED_BYPASS_ENABLE):** 0000 - Disable all HBP 0001 - Enable SS HBP 0010 - Enable HS HBP 0011 - Enable HSIC HBP 0100 - Enable SSIC HBP Others - Reserved **Power Well:** Core
27	0x0 RW	**DFTIDPINSEL (DFTIDPINSEL):** Select Between Device and Host Controller in HBP mode 0h : Device Controller is selected 1h : Host Controller is selected **Power Well:** Core
26	0x0 RW/O	**Lock Bit (LOCK):** This bit is used by BIOS to lock/unlock lockable bits. When set to '1' the write access to HBP Enable is disabled (locked state). When set to '0', the write access to bit locked are enable (unlocked state). Writable once after platform reset. **Power Well:** Core
25	0x0 RW	**Loopback Enable (UTMILPBKEN):** Enable loopback test mode. If asserted, loopback test mode is enabled **Power Well:** Core
24:0	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core

7.4.229 XECP_CMDM_STS0—Offset 8448h

Access Method

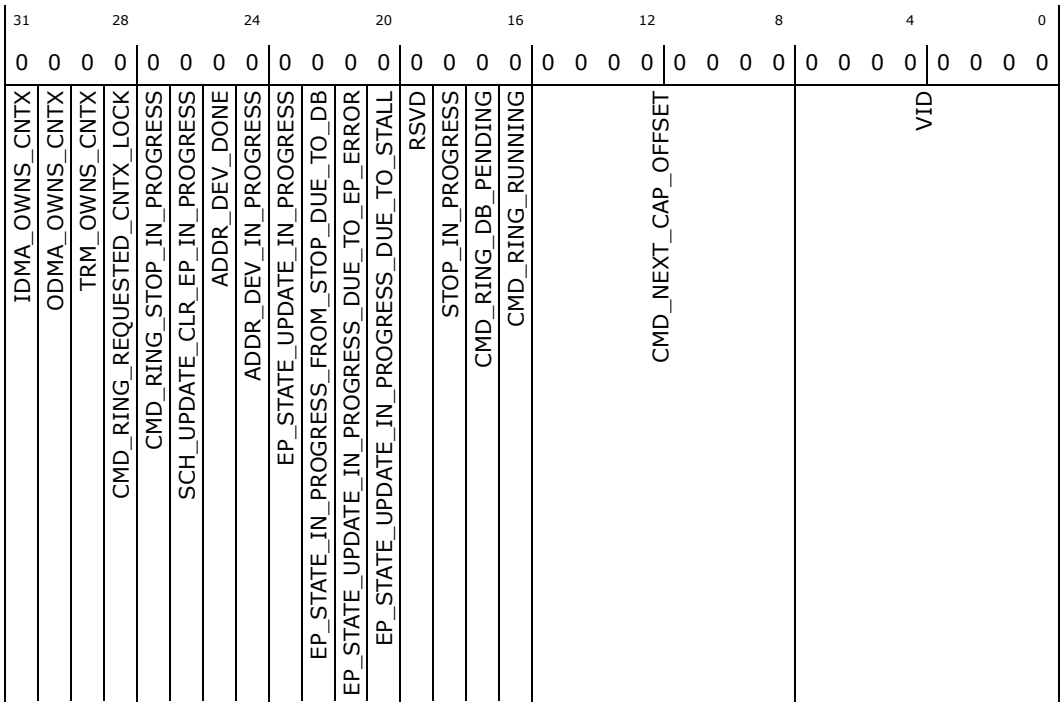
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8448h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**IDMA_OWNS_CNTX:** Indicates that IDMA module owns the context access currently **Power Well:** Core
30	0x0 RO	**ODMA_OWNS_CNTX:** Indicates that ODMA module owns the context access currently **Power Well:** Core
29	0x0 RO	**TRM_OWNS_CNTX:** Indicates that TRM modules owns the context access currently **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
28	0x0 RO	**CMD_RING_REQUESTED_CNTX_LOCK:** Indicates that Command Manager has requested a context lock **Power Well:** Core
27	0x0 RO	**CMD_RING_STOP_IN_PROGRESS:** Indicates that Command Ring stop command is in progress **Power Well:** Core
26	0x0 RO	**SCH_UPDATE_CLR_EP_IN_PROGRESS:** Indicates that clearing an EP out of schedule is in progress **Power Well:** Core
25	0x0 RO	**ADDR_DEV_DONE:** Indicates that current address device command is done by ODMA **Power Well:** Core
24	0x0 RO	**ADDR_DEV_IN_PROGRESS:** Indicates that ODMA has an address device command in progress **Power Well:** Core
23	0x0 RO	**EP_STATE_UPDATE_IN_PROGRESS:** Indicates that updating of EP state is in progress **Power Well:** Core
22	0x0 RO	**EP_STATE_IN_PROGRESS_FROM_STOP_DUE_TO_DB:** Indicates that doorbell manager is issuing and EP update due to a doorbell ring on an EP that is in stop state **Power Well:** Core
21	0x0 RO	**EP_STATE_UPDATE_IN_PROGRESS_DUE_TO_EP_ERROR:** Indicates that transfer ring manager is isuing and EP update due to an EP error condition detected **Power Well:** Core
20	0x0 RO	**EP_STATE_UPDATE_IN_PROGRESS_DUE_TO_STALL:** Indicates that transfere ring manager is issuing an EP state update due to stall received **Power Well:** Core
19	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
18	0x0 RO	**STOP in progress (STOP_IN_PROGRESS):** Indicates that a STOP on the Command Ring is in progress **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
17	0x0 RO	**commend ring has doorbell pending (CMD_RING_DB_PENDING):** Indicates that the commend ring has doorbell pending **Power Well:** Core
16	0x0 RO	**commend ring running (CMD_RING_RUNNING):** Indicates that the commend ring is running **Power Well:** Core
15:8	0x0 RO	**Command next capability offset (CMD_NEXT_CAP_OFFSET):** Reserved. **Power Well:** Core
7:0	0x0 RO	**Vendor defined capability ID (VID):** Reserved. **Power Well:** Core

7.4.230 XECP_CMDM_STS1—Offset 844Ch

Access Method

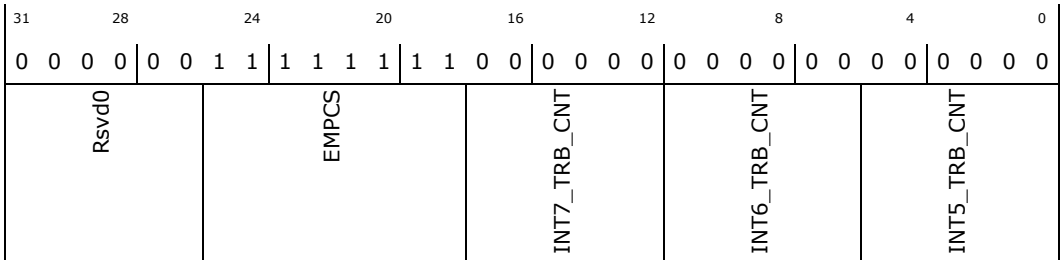
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 844Ch

Op Codes:

h - Read, h - Write

Default: 03FC0000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
25:18	0xff RO	**Event manager Producer Cycle State (EMPCS):** Reserved. **Power Well:** Core
17:12	0x0 RO	**Interrupter 7 TRB Count [5:0] (INT7_TRB_CNT):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11:6	0x0 RO	**Interrupter 6 TRB Count [5:0] (INT6_TRB_CNT):** Reserved. **Power Well:** Core
5:0	0x0 RO	**Interrupter 5 TRB Count [5:0] (INT5_TRB_CNT):** Reserved. **Power Well:** Core

7.4.231 XECP_CMDM_STS2—Offset 8450h

Access Method

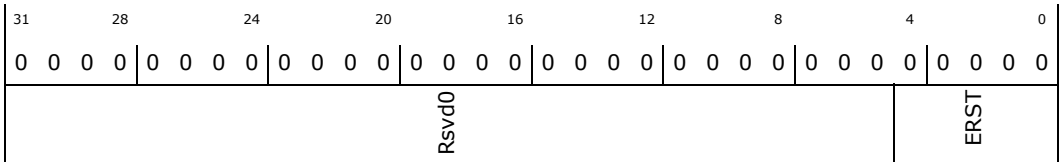
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8450h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
4:0	0x0 RO	**Event Ring Segment Table (ERST):** count low **Power Well:** Core

7.4.232 XECP_CMDM_STS3—Offset 8454h

Access Method

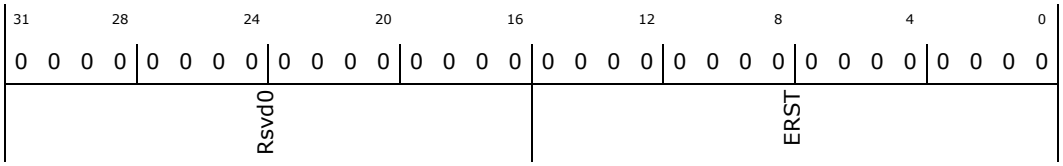
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8454h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd0:** Reserved. **Power Well:** Core
15:0	0x0 RO	**Event Ring Segment Table (ERST):** count high **Power Well:** Core

7.4.233 XECP_CMDM_STS4—Offset 8458h

Access Method

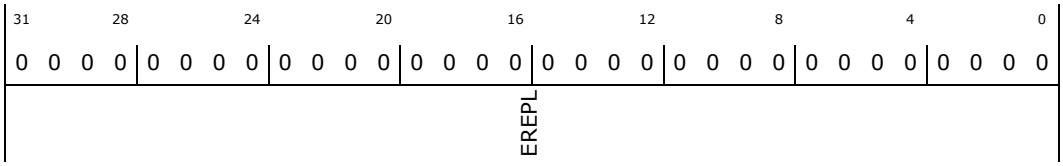
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8458h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Event Ring Enqueue Pointer Low (EREPL):** Reserved. **Power Well:** Core

7.4.234 XECP_CMDM_STS5—Offset 845Ch

Access Method

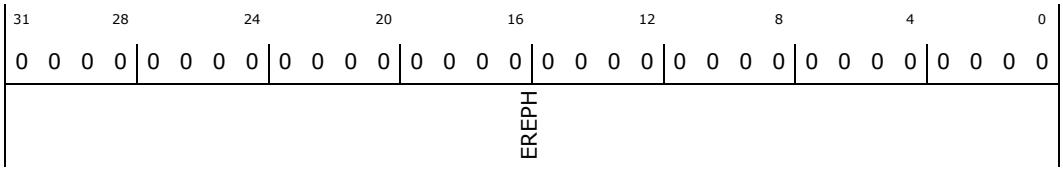
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 845Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Event Ring Enqueue Pointer High (EREPH):** Reserved. **Power Well:** Core

7.4.235 AUX Power PHY Reset (UPORTS_PON_RST_REG)—Offset 8460h

Access Method

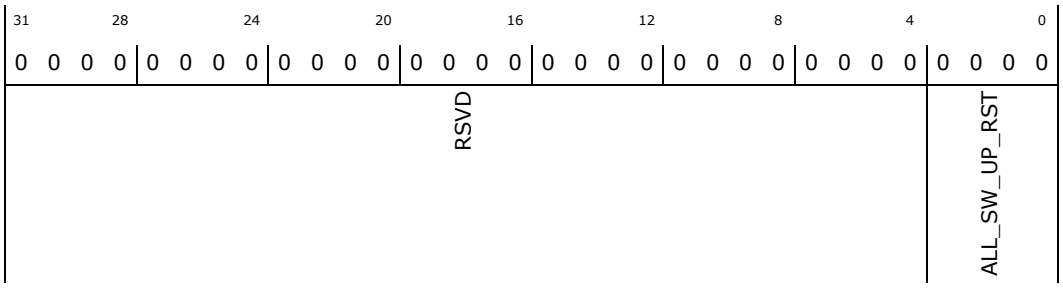
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8460h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
3:0	0x0 WO	**Allow Software USB PHY RST (ALL_SW_UP_RST):** Allow a USB PHY reset being issued by software. Writing to this register with bit set to 1 will reset the USB PHY that is connected to the port. Bit3:0 indicates the port number of the USB PHY **Power Well:** SUS

7.4.236 Latency Tolerance Control 0 (HOST_IF_LAT_TOL_CTRL_REG0)—Offset 8464h

The Latency Tolerance Control Register is used by SW to control which BELT is returned when this register is read. SW shall write to this register to program a Slot-ID, Port-ID and BELT Select to determine which BELT is selected. When this register is read the selected BELT is returned.

Access Method

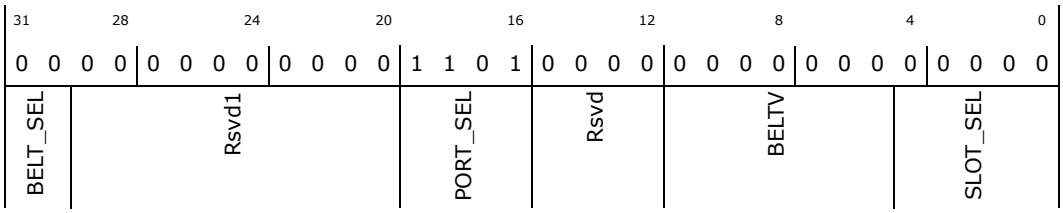
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8464h

Op Codes:

h - Read, h - Write

Default: 000D0000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 WO	**BELT Select (BELT_SEL):** This field determines what value will be selected to read back from SW when reading this register 0: Returns the SW programmed Latency Tolerance Value 1: Returns the Lowest BELT in the Host 2: Returns the BELT for the requested Slot-ID (Slot Select) 3: Returns the BELT for the requested Port-ID (Port Select) **Power Well:** Core
29:20	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
19:16	0xd WO	**Port Select (PORT_SEL):** Used to select the BELT for a given Port # when the BELT Select is programmed to select the Port-ID (this field is 0 based) **Power Well:** Core
15:12	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core
11:5	0x0 RO	**BELT Value (BELTV):** Value of selected BELT is return in this field **Power Well:** Core
4:0	0x0 RW	**Slot Select (SLOT_SEL):** Reads will return: BELT Value (BELTV) [4:0]: Value of selected BELT is return in this field Writes will control : Slot Select (): Used to select the BELT for a given Slot # when the BELT Select is programmed to select the Slot-ID (this field is zero based) **Power Well:** Core

7.4.237 USB Legacy Support Capability (USBLEGSUP)—Offset 846Ch

This register is modified and maintained by BIOS

Access Method

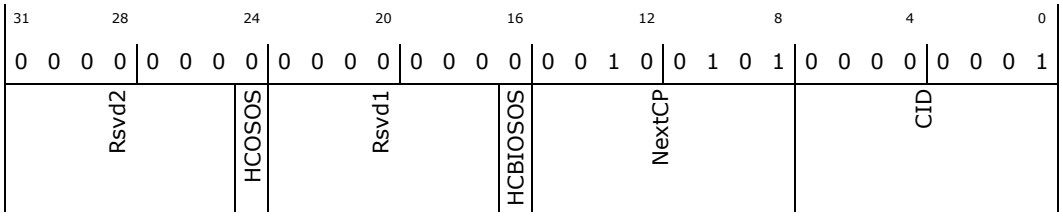
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 846Ch

Op Codes:

h - Read, h - Write

Default: 00002501h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
24	0x0 RW	**HC OS Owned Semaphore (HCOSOS):** Reserved. **Power Well:** SUS
23:17	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
16	0x0 RW	**HC BIOS Owned Semaphore (HCBIOSOS):** Reserved. **Power Well:** SUS
15:8	0x25 RW/S	**Next Capability Pointer (NextCP):** Reserved. **Power Well:** SUS
7:0	0x1 RW/L	**Capability ID (CID):** Reserved. **Power Well:** SUS

7.4.238 USB Legacy Support Control Status (USBLEGCTLSTS)—Offset 8470h

Access Method

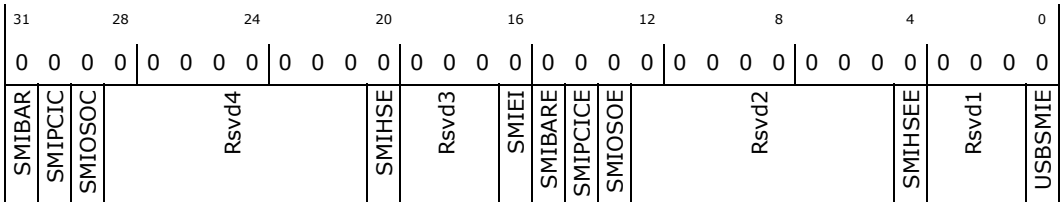
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8470h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/C	**SMI on BAR (SMIBAR):** Reserved. **Power Well:** SUS
30	0x0 RW/C	**SMI on PCI Command (SMIPCIC):** Reserved. **Power Well:** SUS
29	0x0 RW/C	**SMI on OS Ownership Change (SMIOSOC):** Reserved. **Power Well:** SUS
28:21	0x0 RO	**Rsvd4:** Reserved. **Power Well:** Core
20	0x0 RO	**SMI on Host System Error (SMIHSE):** Reserved. **Power Well:** SUS
19:17	0x0 RO	**Rsvd3:** Reserved. **Power Well:** Core
16	0x0 RO	**SMI on Event Interrupt (SMIEI):** Reserved. **Power Well:** SUS
15	0x0 RW	**SMI on BAR Enable (SMIBARE):** Reserved. **Power Well:** SUS
14	0x0 RW	**SMI on PCI Command Enable (SMIPCICE):** Reserved. **Power Well:** SUS
13	0x0 RW	**SMI on OS Ownership Enable (SMIOSOE):** Reserved. **Power Well:** SUS
12:5	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
4	0x0 RW	**SMI on Host System Error Enable (SMIHSEE):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
3:1	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
0	0x0 RW	**USB SMI Enable (USBSMIE):** Reserved. **Power Well:** SUS

7.4.239 Port Disable Override capability register (PDO_CAPABILITY)—Offset 84F4h

Access Method

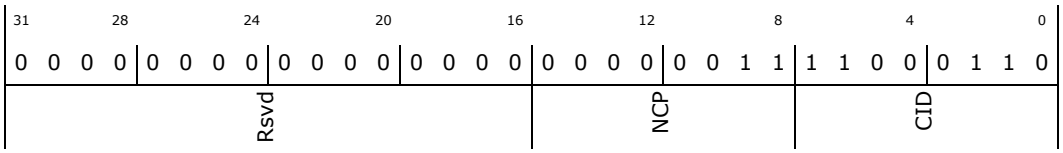
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 84F4h

Op Codes:

h - Read, h - Write

Default: 000003C6h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core
15:8	0x3 RW/S	**Next Capability Pointer (NCP):** Reserved. **Power Well:** Core
7:0	0xc6 RW/S	**Capability ID (CID):** Reserved. **Power Well:** Core

7.4.240 USB2 Port Disable Override (USB2PDO)—Offset 84F8h

Access Method

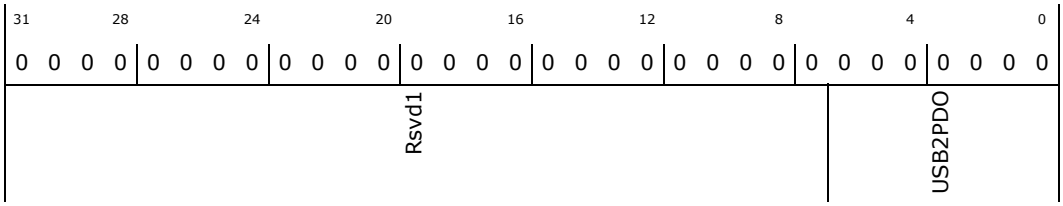
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 84F8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
6:0	0x0 RW/O	**USB2PDO:** Reserved. **Power Well:** SUS

7.4.241 USB3 Port Disable Override (USB3PDO)—Offset 84FCh

Access Method

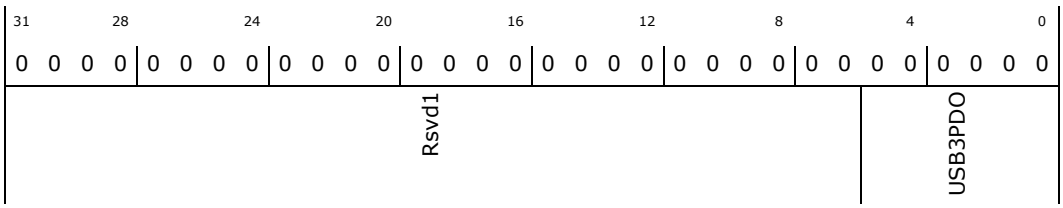
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 84FCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
5:0	0x0 RW/O	**USB3 Port Disable Override (USB3PDO):** A '1' in a bit position prevents the corresponding USB3 port from reporting a Device Connection to the XHC. **Power Well:** SUS

7.4.242 HW state capability register (HW_STATE_CAPABILITY)—Offset 8500h

Access Method

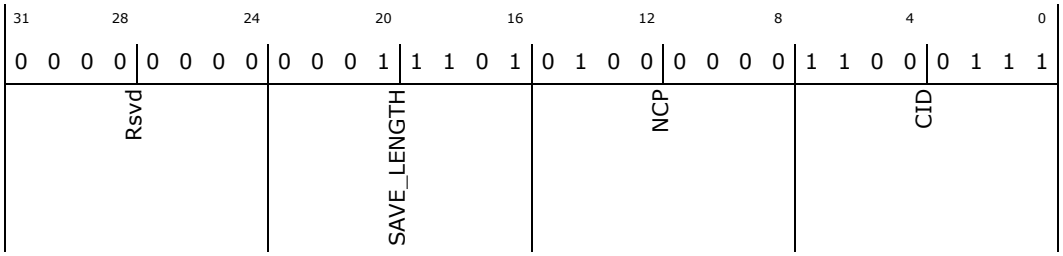
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8500h

Op Codes:

h - Read, h - Write

Default: 001D40C7h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core
23:16	0x1d RO	**Save Length (SAVE_LENGTH):** Indicates the number of DWords in this capability starting at offset 04h, that need to be saved and restored **Power Well:** Core
15:8	0x40 RO	**Next Capability Pointer (NCP):** Reserved. **Power Well:** Core
7:0	0xc7 RO	**Capability ID (CID):** Reserved. **Power Well:** Core

7.4.243 HW state register 1 (HW_STATE_REG1)—Offset 8504h

Implementation defined HW state: SW must not access this register.

Access Method

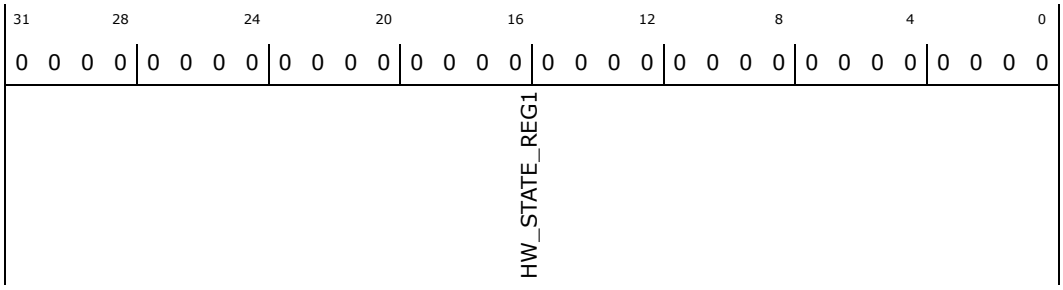
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8504h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**HW_STATE_REG1:** Reserved. **Power Well:** Core

7.4.244 HW state register 2 (HW_STATE_REG2)—Offset 8508h

Implementation defined HW state: SW must not access this register.

Access Method

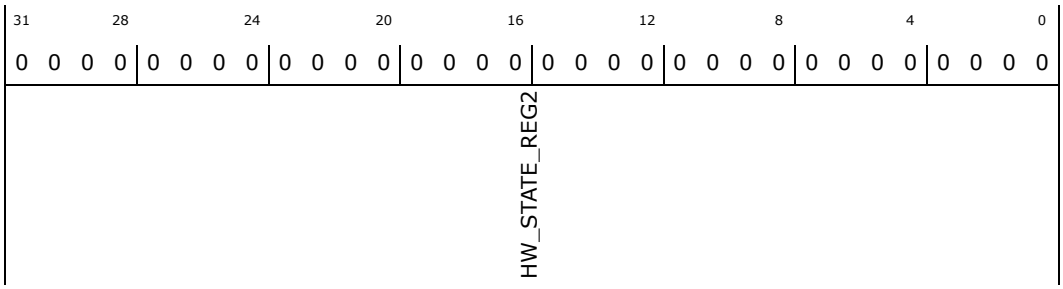
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8508h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**HW_STATE_REG2:** Reserved. **Power Well:** Core

7.4.245 HW state register 3 (HW_STATE_REG3)—Offset 850Ch

Implementation defined HW state: SW must not access this register.

Access Method

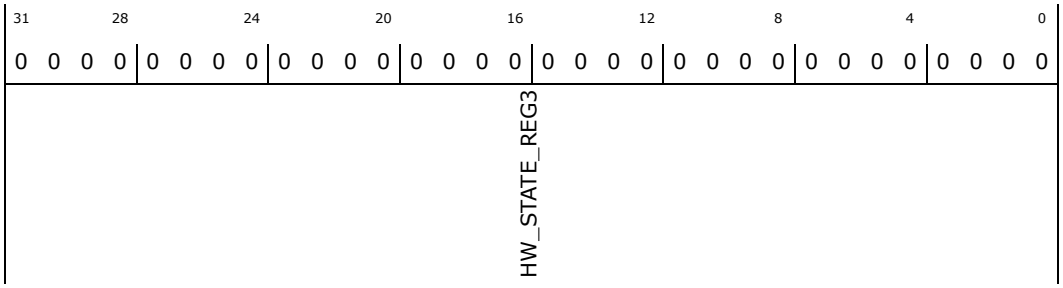
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 850Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**HW_STATE_REG3:** Reserved. **Power Well:** Core

7.4.246 HW state register 4 (HW_STATE_REG4)—Offset 8510h

Implementation defined HW state: SW must not access this register.

Access Method

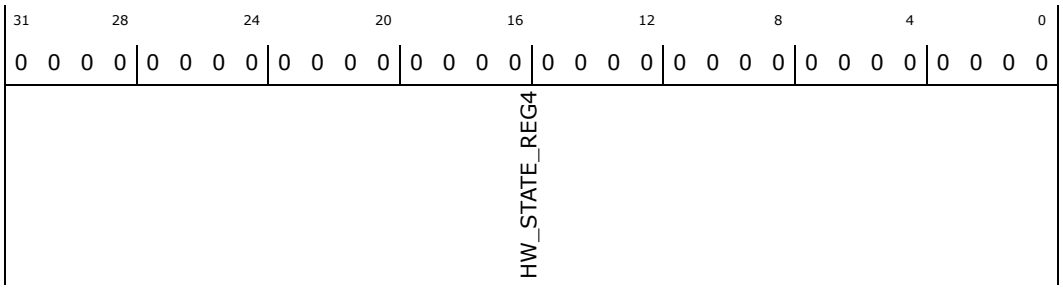
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8510h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**HW_STATE_REG4:** Reserved. **Power Well:** Core

7.4.247 CONFIG mirror capability register (CONFIG_MIRROR_CAPABILITY)—Offset 8600h

Access Method

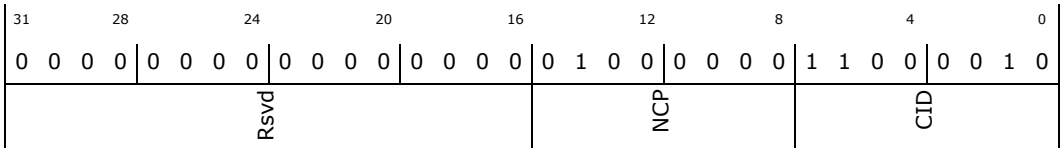
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8600h

Op Codes:

h - Read, h - Write

Default: 000040C2h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Rsvd:** Reserved. **Power Well:** Core
15:8	0x40 RW/S	**Next Capability Pointer (NCP):** Reserved. **Power Well:** Core
7:0	0xc2 RW/S	**Capability ID (CID):** Reserved. **Power Well:** Core

7.4.248 Command (CMD_MMIO)—Offset 8604h

Access Method

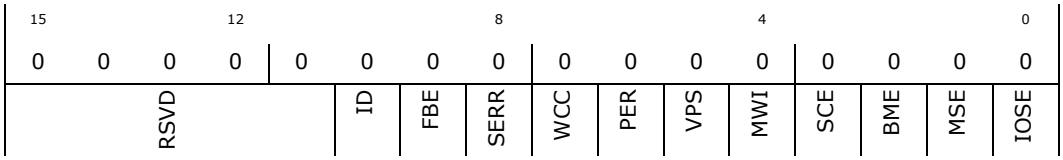
Type: Message Bus Register (Size: 16 bits)

Offset: [Port: 0x5A] + 8604h

Op Codes:

h - Read, h - Write

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:11	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RW	**Interrupt Disable (ID):** When cleared to 0, the function is capable of generating interrupts. When 1, the function can not generate its interrupt to the interrupt controller. Note that the corresponding Interrupt Status bit is not affected by the interrupt enable. **Power Well:** Core
9	0x0 RO	**Fast Back to Back Enable (FBE):** Reserved. **Power Well:** Core
8	0x0 RW	**SERR# Enable (SERR):** When set to 1, the XHC is capable of generating (internally) SERR#. Refer section on error handling. **Power Well:** Core
7	0x0 RO	**Wait Cycle Control (WCC):** Reserved. **Power Well:** Core
6	0x0 RW	**Parity Error Response (PER):** When set to 1, the XHCI Host Controller will check for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase as recommended by the XHCI specification. Note that this applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#. **Power Well:** Core
4	0x0 RO	**Memory Write Invalidate (MWI):** Reserved. **Power Well:** Core
3	0x0 RO	**Special Cycle Enable (SCE):** Reserved. **Power Well:** Core
2	0x0 RW	**Bus Master Enable (BME):** When set, it allows XHC to act as a bus master. When cleared, it disable XHC from initiating transactions on the system bus. **Power Well:** Core
1	0x0 RW	**Memory Space Enable (MSE):** This bit controls access to the XHC Memory Space registers. If this bit is set, accesses to the XHC registers are enabled. The Base Address register for the XHC should be programmed before this bit is set. **Power Well:** Core
0	0x0 RO	**I/O Space Enable (IOSE):** Reserved as 0. Read-Only. **Power Well:** Core

7.4.249 Device Status (STS_MMIO)—Offset 8606h

Access Method

Type: Message Bus Register (Size: 16 bits)

Offset: [Port: 0x5A] + 8606h

Op Codes:

h - Read, h - Write

Default: 0290h

15			12				8				4				0
0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0
DPE	SSE	RMA	RTA	STA	DEVT		MDPED	FBBC	UDF	MC	CL	IS	RSVD		

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW/1C	**Detected Parity Error (DPE):** This bit is set by the Intel PCH whenever a parity error is seen on the internal interface to the XHC host controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
14	0x0 RW/1C	**Signaled System Error (SSE):** This bit is set by the Intel PCH whenever it signals SERR# (internally). The SERR_EN bit (bit 8 in the Command Register) must be 1 for this bit to be set. Refer error handling section for complete list of conditions handled. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
13	0x0 RW/1C	**Received Master-Abort Status (RMA):** This bit is set when XHC, as a master, receives a master-abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
12	0x0 RW/1C	**Received Target Abort Status (RTA):** This bit is set when XHC, as a master, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
11	0x0 RW/1C	**Signaled Target-Abort Status (STA):** This bit is used to indicate when the XHC function responds to a cycle with a target abort. **Power Well:** Core
10:9	0x1 RO	**DEVSEL# Timing Status (DEVT):** This 2-bit field defines the timing for DEVSEL# assertion. Read-Only. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW/1C	**Master Data Parity Error Detected (MDPED):** This bit is set by the Intel PCH whenever a data parity error is detected on a XHC read completion packet on the internal interface to the XHC host controller and bit 6 of the Command register is set to 1. Software clears this bit by writing a 1 to this bit location. **Power Well:** Core
7	0x1 RO	**Fast Back-to-Back Capable (FBBC):** Reserved as 1 Read-Only. **Power Well:** Core
6	0x0 RO	**User Definable Features (UDF):** Reserved as 0. Read-Only. **Power Well:** Core
5	0x0 RO	**66 MHz Capable (MC):** Reserved as 0. Read-Only. **Power Well:** Core
4	0x1 RO	**Capabilities List (CL):** Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer. **Power Well:** Core
3	0x0 RO/V	**Interrupt Status (IS):** This read-only bit reflects the state of this function's interrupt at the input of the enable/disable logic. This bit is a 1 when the interrupt is asserted. This bit will be 0 when the interrupt is deasserted. The value reported in this bit is independent of the value in the Interrupt Enable bit. **Power Well:** Core
2:0	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

7.4.250 Revision ID (RID_MMIO)—Offset 8608h

Access Method

Type: Message Bus Register (Size: 8 bits)

Offset: [Port: 0x5A] + 8608h

Op Codes:

h - Read, h - Write

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RID							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO/V	**Revision ID (RID):** Refer Chap 6 for value. **Power Well:** Core

7.4.251 Programming Interface (PI_MMIO)—Offset 8609h

Access Method

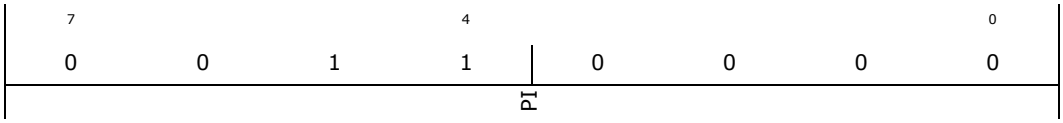
Type: Message Bus Register (Size: 8 bits)

Offset: [Port: 0x5A] + 8609h

Op Codes:

h - Read, h - Write

Default: 30h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x30 RO	**Programming Interface (PI):** A value of 30h indicates that this USB Host Controller conforms to the XHCI specification. **Power Well:** Core

7.4.252 Sub Class Code (SCC_MMIO)—Offset 860Ah

Access Method

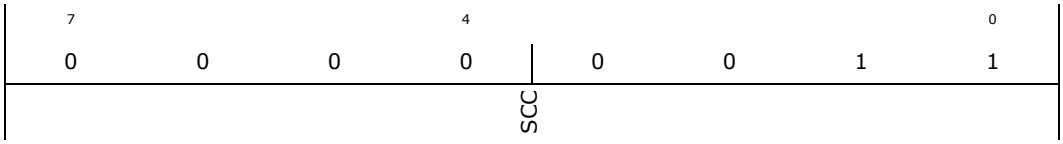
Type: Message Bus Register (Size: 8 bits)

Offset: [Port: 0x5A] + 860Ah

Op Codes:

h - Read, h - Write

Default: 03h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x3 RO	**Sub Class Code (SCC):** A value of 03h indicates that this is a Universal Serial Bus Host Controller. **Power Well:** Core

7.4.253 Base Class Code (BCC_MMIO)—Offset 860Bh

Access Method

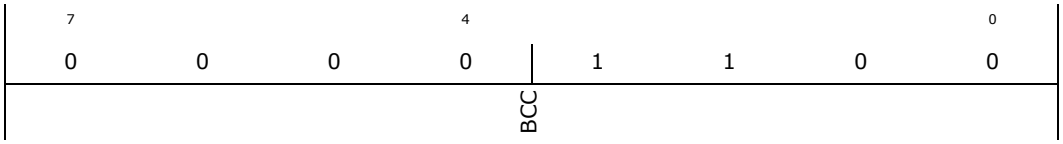
Type: Message Bus Register (Size: 8 bits)

Offset: [Port: 0x5A] + 860Bh

Op Codes:

h - Read, h - Write

Default: 0Ch



Bit Range	Default & Access	Field Name (ID): Description
7:0	0xc RO	**Base Class Code (BCC):** A value of 0Ch indicates that this is a Serial Bus controller. **Power Well:** Core

7.4.254 Master Latency Timer (MLT_MMIO)—Offset 860Dh

Access Method

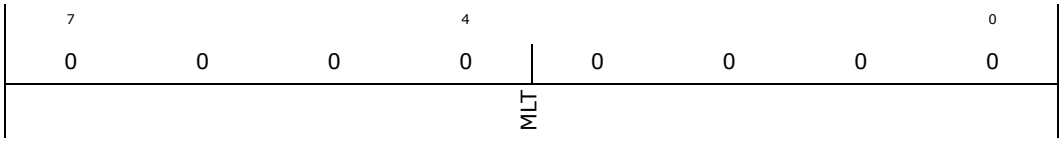
Type: Message Bus Register (Size: 8 bits)

Offset: [Port: 0x5A] + 860Dh

Op Codes:

h - Read, h - Write

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**Master Latency Timer (MLT):** Because the XHC controller is internally implemented with arbitration on an internal interface, it does not need a master latency timer. The bits will be fixed at 0. **Power Well:** Core

7.4.255 Header Type (HT_MMIO)—Offset 860Eh

Access Method

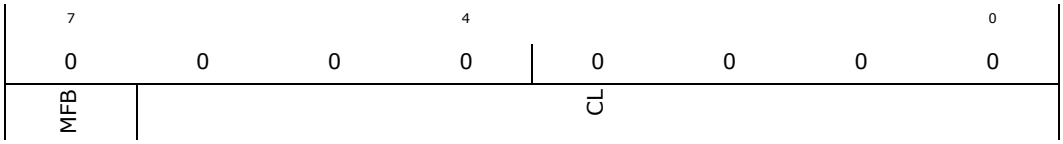
Type: Message Bus Register (Size: 8 bits)

Offset: [Port: 0x5A] + 860Eh

Op Codes:

h - Read, h - Write

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**Multi-Function Bit (MFB):** Read only indicating single function device. **Power Well:** Core
6:0	0x0 RO	**Configuration layout (CL):** Hardwired to 0 to indicate a standard PCI configuration layout. **Power Well:** Core

7.4.256 Memory Base Address (MBAR_MMIO)—Offset 8610h

Value in this register will be different after the enumeration process.

Access Method

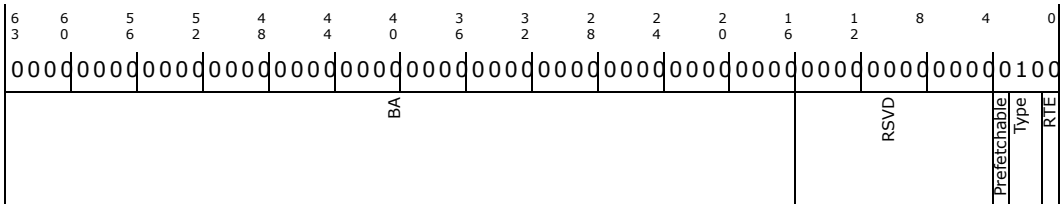
Type: Message Bus Register (Size: 64 bits)

Offset: [Port: 0x5A] + 8610h

Op Codes:

h - Read, h - Write

Default: 0000000000000004h



Bit Range	Default & Access	Field Name (ID): Description
63:16	0x0 RW	**Base Address (BA):** Bits (63:16) correspond to memory address signals (63:16), respectively. This gives 64 KB of relocatable memory space aligned to 64 KB boundaries. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:4	0x0 RO	**Reserved (RSVD):** Reserved. Read-Only 0, this indicates that this function is requesting an 64KB block of memory. **Power Well:** Core
3	0x0 RO	**Prefetchable:** This bit is hardwired to 0 indicating that this range should not be prefetched. **Power Well:** Core
2:1	0x2 RO	**Type:** If this field is hardwired to 00 it indicates that this range can be mapped anywhere within 32-bit address space. If this field is hardwired to 10 it indicates that this range can be mapped anywhere within 64-bit address space. **Power Well:** Core
0	0x0 RO	**Resource Type Indicator (RTE):** This bit is hardwired to 0 indicating that the base address field in this register maps to memory space **Power Well:** Core

7.4.257 USB Subsystem Vendor ID (SSVID_MMIO)—Offset 862Ch

This register is modified and maintained by BIOS

Access Method

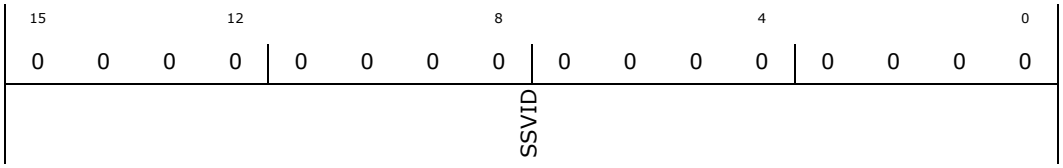
Type: Message Bus Register (Size: 16 bits)

Offset: [Port: 0x5A] + 862Ch

Op Codes:

h - Read, h - Write

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW/L	**USB Subsystem Vendor ID (SSVID):** This register, in combination with the USB Subsystem ID register, enables the operating system to distinguish each subsystem from the others. **Power Well:** Core

7.4.258 USB Subsystem ID (SSID_MMIO)—Offset 862Eh

This register is modified and maintained by BIOS

Access Method

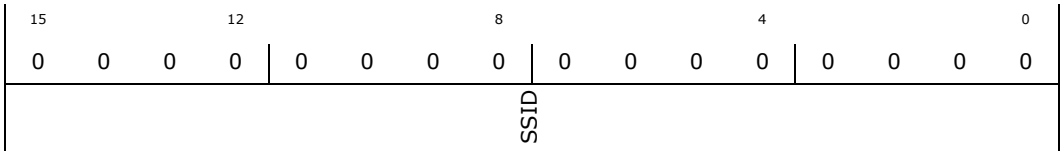
Type: Message Bus Register (Size: 16 bits)

Offset: [Port: 0x5A] + 862Eh

Op Codes:

h - Read, h - Write

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW/L	**USB Subsystem ID (SSID):** BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s). **Power Well:** Core

7.4.259 Capabilities Pointer (CAP_PTR_MMIO)—Offset 8634h

Access Method

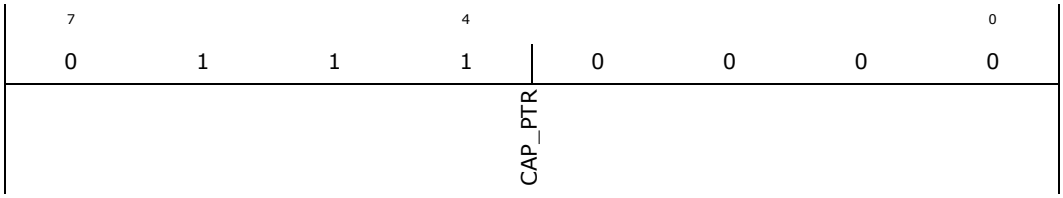
Type: Message Bus Register (Size: 8 bits)

Offset: [Port: 0x5A] + 8634h

Op Codes:

h - Read, h - Write

Default: 70h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x70 RO	**Capabilities Pointer (CAP_PTR):** This register points to the starting offset of the capabilities ranges. **Power Well:** Core

7.4.260 Interrupt Line (ILINE_MMIO)—Offset 863Ch

Access Method

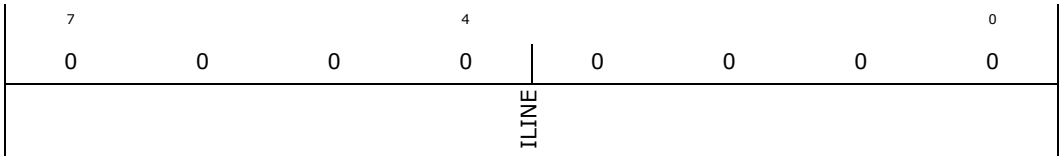
Type: Message Bus Register (Size: 8 bits)

Offset: [Port: 0x5A] + 863Ch

Op Codes:

h - Read, h - Write

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**Interrupt Line (ILINE):** This data is not used by the Intel PCH. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to. **Power Well:** Core

7.4.261 Interrupt Pin (IPIN_MMIO)—Offset 863Dh

Access Method

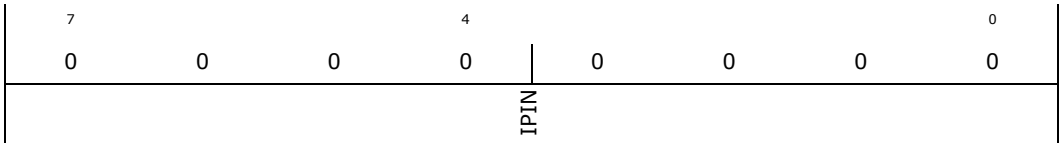
Type: Message Bus Register (Size: 8 bits)

Offset: [Port: 0x5A] + 863Dh

Op Codes:

h - Read, h - Write

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**Interrupt pin (IPIN):** Bits 7:0 reflect the Interrupt Pin assigned to the host controller by the platform (and are hardwired). **Power Well:** Core

7.4.262 Audio Time Synchronization (AUDSYNC_MMIO)—Offset 8658h

This 32 bit register is used for audio stream synchronization across different devices. Global signal sample_now captures a value in AUDSYNC register.

Access Method

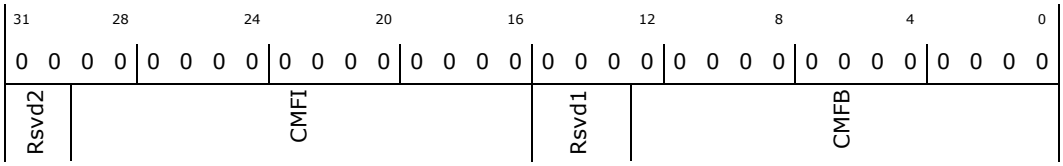
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8658h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**Rsvd2:** Reserved. **Power Well:** Core
29:16	0x0 RO/V	**Captured Frame List Current Index/Frame Number (CMFI):** The value in this register is updated in response to sample_now signal. Bits (29:16) reflect state of bits (13:0) of FRINDEX **Power Well:** Core
15:13	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
12:0	0x0 RO/V	**Captured Micro-frame BLIF (CMFB):** The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done in FLA. **Power Well:** Core

7.4.263 Serial Bus Release Number (SBRN_MMIO)—Offset 8660h

Access Method

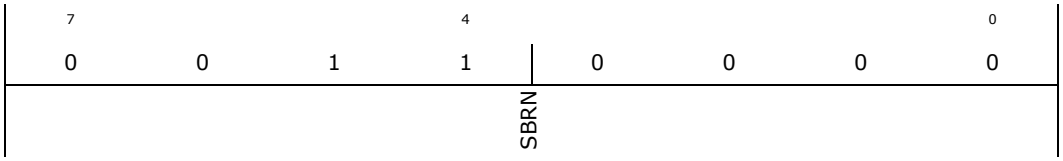
Type: Message Bus Register (Size: 8 bits)

Offset: [Port: 0x5A] + 8660h

Op Codes:

h - Read, h - Write

Default: 30h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x30 RO	**Serial Bus Release Number (SBRN):** A value of 30h indicates that this controller follows USB release 3.0. **Power Well:** SUS

7.4.264 Frame Length Adjustment (FLADJ_MMIO)—Offset 8661h

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register should only be modified when the HChalted bit in the USBSTS register is a one. Changing value of this register while the host controller is operating yields undefined results.

Access Method

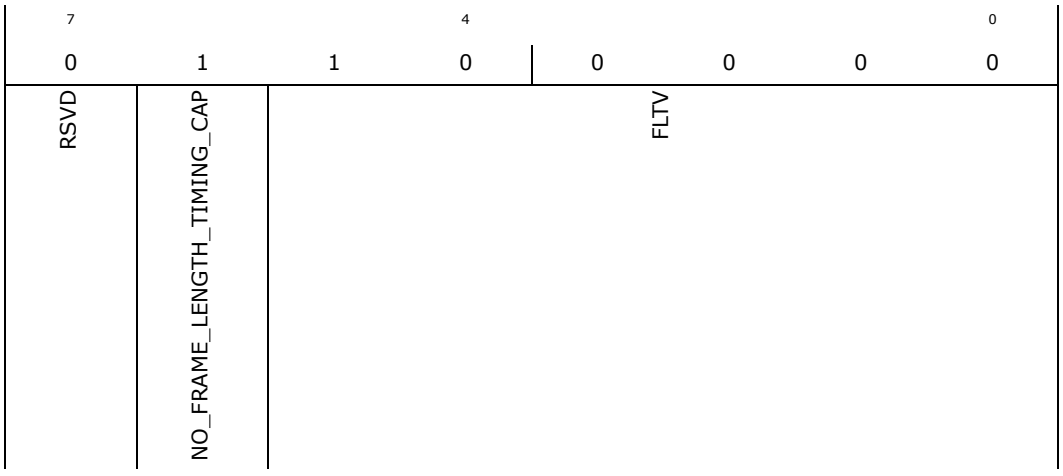
Type: Message Bus Register (Size: 8 bits)

Offset: [Port: 0x5A] + 8661h

Op Codes:

h - Read, h - Write

Default: 60h



Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**Reserved (RSVD):** . **Power Well:** SUS
6	0x1 RO	**No Frame Length Timing Capability (NO_FRAME_LENGTH_TIMING_CAP):** This flag is set to 1 to indicate that the host controller does not support a programmable Frame Length Timing Value field. **Power Well:** Core
5:0	0x20 RO	**Frame Length Timing Value (FLTV):** SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (number of High Speed bit times) FLADJ Value (decimal) (decimal) 59488 0 (00h) 59504 1 (01h) 59520 2 (02h) ... 59984 31 (1Fh) 60000 32 (20h) ... 60480 62 (3Eh) 60496 63 (3Fh) Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (# High Speed bit times) FLADJ Value **Power Well:** SUS

7.4.265 Best Effort Service Latency (BESL_MMIO)—Offset 8662h

Bset Effort Service Latency.

Access Method

Type: Message Bus Register (Size: 8 bits)

Offset: [Port: 0x5A] + 8662h

Op Codes:

h - Read, h - Write

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
DBESLD				DBESL			

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW/L	**Default Best Effort Service Latency Deep (DBESLD):** Default Best Effort Service Latency (DBESLD) If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESLD field. This is programmed by BIOS based on platform parameters. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x0 RW/L	**Default Best Effort Service Latency (DBESL):** If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESL field. This is programmed by BIOS based on platform parameters. **Power Well:** Core

7.4.266 PCI Power Management Capability ID (PM_CID_MMIO)—Offset 8670h

Access Method

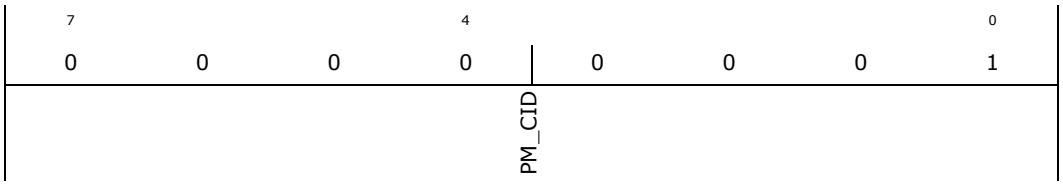
Type: Message Bus Register (Size: 8 bits)

Offset: [Port: 0x5A] + 8670h

Op Codes:

h - Read, h - Write

Default: 01h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x1 RO	**PCI Power Management Capability ID (PM_CID):** A value of 01h indicates that this is a PCI Power Management capabilities field. **Power Well:** Core

7.4.267 Next Item Pointer #1 (PM_NEXT_MMIO)—Offset 8671h

This register is modified and maintained by BIOS

Access Method

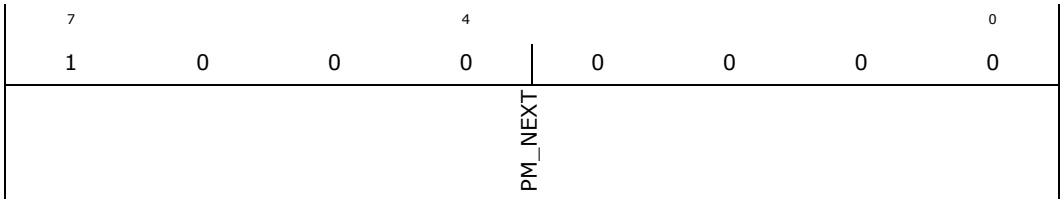
Type: Message Bus Register (Size: 8 bits)

Offset: [Port: 0x5A] + 8671h

Op Codes:

h - Read, h - Write

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x80 RW/L	**Next Item Pointer #1 (PM_NEXT):** This register defaults to 80h, which indicates that the next capability registers begin at configuration offset 80h. This register is writable when the Access Control bit is set to '0'. This allows BIOS to effectively hide the next capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Values of: 80h implies next capability is MSI 00h implies that MSI capability is hidden. Note: This value is never expected to be programmed. **Power Well:** Core

7.4.268 Power Management Capabilities (PM_CAP_MMIO)—Offset 8672h

Normally, this register is read-only to report capabilities to the power management software. In order to report different power management capabilities depending on the system in which the Intel PCH is used, the write access to this register is controlled by the Access Control bit (ACCTRL). The value written to this register does not affect the hardware other than changing the value returned during a read. This register is modified and maintained by BIOS

Access Method

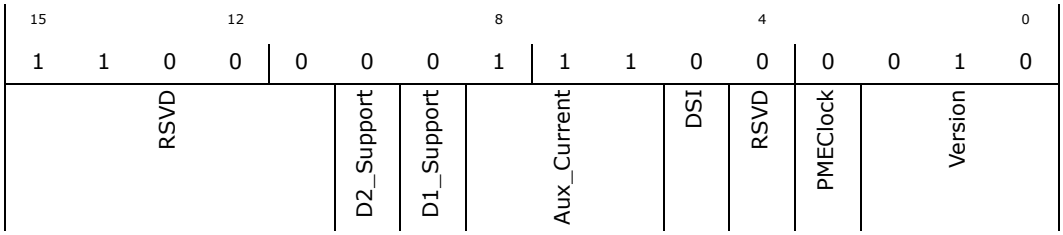
Type: Message Bus Register (Size: 16 bits)

Offset: [Port: 0x5A] + 8672h

Op Codes:

h - Read, h - Write

Default: C1C2h



Bit Range	Default & Access	Field Name (ID): Description
15:11	0x18 RO	**Reserved (RSVD):** Reserved.
10	0x0 RW/L	**D2_Support:** The D2 state is not supported. **Power Well:** Core
9	0x0 RW/L	**D1_Support:** The D1 state is not supported. **Power Well:** Core
8:6	0x7 RW/L	**Aux_Current:** The Intel PCH XHC reports 375mA maximum Suspend well current required when in the D3cold state. This value can be written by BIOS when a more accurate value is known. **Power Well:** Core
5	0x0 RW/L	**DSI:** The Intel PCH reports 0, indicating that no device-specific initialization is required. **Power Well:** Core
4	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
3	0x0 RW/L	**PME Clock (PMEClock):** The Intel PCH reports 0, indicating that no PCI clock is required to generate PME#. **Power Well:** Core
2:0	0x2 RW/L	**Version:** The Intel PCH reports 010, indicating that it complies with Revision 1.1 of the PCI Power Management Specification. **Power Well:** Core

7.4.269 Power Management Control/Status (PM_CS_MMIO)—Offset 8674h

Access Method

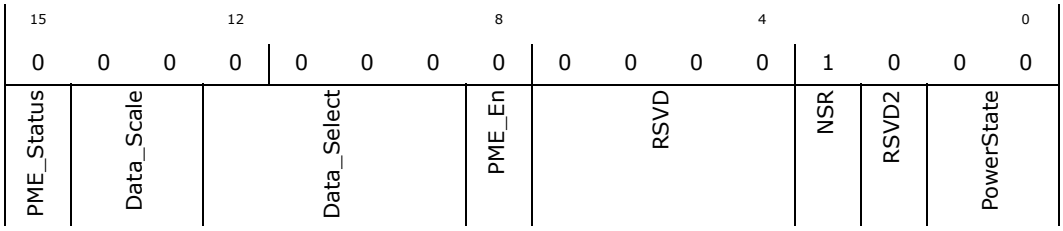
Type: Message Bus Register (Size: 16 bits)

Offset: [Port: 0x5A] + 8674h

Op Codes:

h - Read, h - Write

Default: 0008h



Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW/1C	**PME_Status:** This bit is set when the Intel PCH XHC would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). Writing a 0 has no effect. This bit must be explicitly cleared by the operating system each time the operating system is loaded. **Power Well:** SUS
14:13	0x0 RO	**Data_Scale:** The Intel PCH hardwires these bits to 00 because it does not support the associated Data register. **Power Well:** Core
12:9	0x0 RO	**Data_Select:** The Intel PCH hardwires these bits to 0000 because it does not support the associated Data register. **Power Well:** Core
8	0x0 RW	**PME_En:** A 1 enables the Intel PCH XHC to generate an internal PME signal when PME_Status is 1. This bit must be explicitly cleared by the operating system each time it is initially loaded. **Power Well:** SUS
7:4	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
3	0x1 RO	**No Soft Reset (NSR):**), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. Transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. **Power Well:** Core
2	0x0 RO	**Reserved (RSVD2):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1:0	0x0 RW	**PowerState:** This 2-bit field is used both to determine the current power state of XHC function and to set a new power state. The definition of the field values are: 00b - D0 state 11b - D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3hot state, the Intel PCH must not accept accesses to the XHC memory range, but the configuration space must still be accessible. **Power Well:** Core

7.4.270 Message Signaled Interrupt CID (MSI_CID_MMIO)—Offset 8680h

Access Method

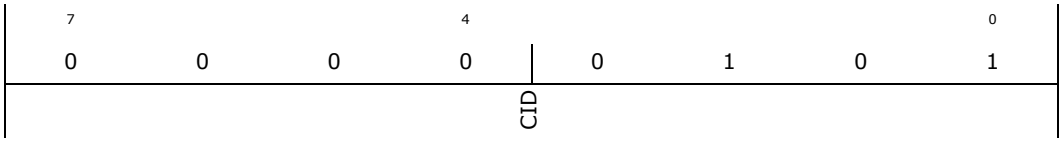
Type: Message Bus Register (Size: 8 bits)

Offset: [Port: 0x5A] + 8680h

Op Codes:

h - Read, h - Write

Default: 05h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x5 RO	**Capability ID (CID):** Indicates that this is an MSI capability **Power Well:** Core

7.4.271 Next item pointer (MSI_NEXT_MMIO)—Offset 8681h

Access Method

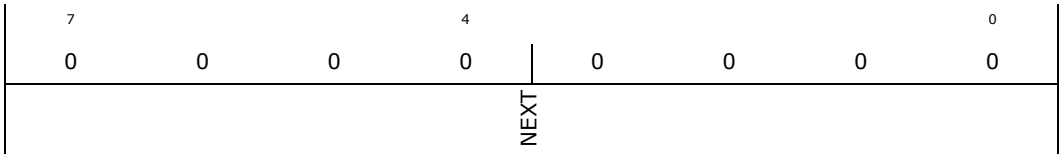
Type: Message Bus Register (Size: 8 bits)

Offset: [Port: 0x5A] + 8681h

Op Codes:

h - Read, h - Write

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**Next Pointer (NEXT):** Indicates that this is the last item on the capability list **Power Well:** Core

7.4.272 Message Signaled Interrupt Message Control (MSI_MCTL_MMIO)—Offset 8682h

Access Method

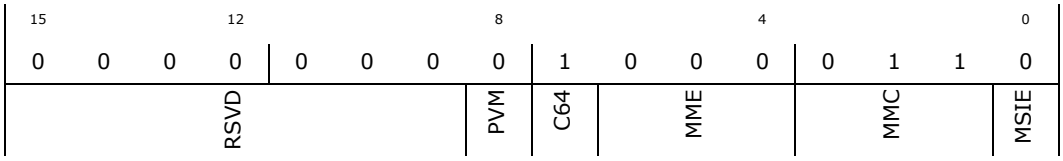
Type: Message Bus Register (Size: 16 bits)

Offset: [Port: 0x5A] + 8682h

Op Codes:

h - Read, h - Write

Default: 0086h



Bit Range	Default & Access	Field Name (ID): Description
15:9	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
8	0x0 RO	**Per-Vector Masking Capable (PVM):** Specifies whether controller supports MSI per vector masking. Not supported **Power Well:** Core
7	0x1 RO	**64 Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages. This device is 64-bit capable. **Power Well:** Core
6:4	0x0 RW	**Multiple Message Enable (MME):** Indicates the number of messages the controller should assert. This device supports multiple message MSI. **Power Well:** Core
3:1	0x3 RO	**Multiple Message Capable (MMC):** Indicates the number of messages the controller wishes to assert. This field must be set by HW to reflect the number of Interrupters supported. Encoding number of Vectors requested (number of Interrupters) 000 1 001 2 010 4 011 8 100 16 101 32 110-111 Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**MSI Enable (MSIE):** If set to 1, MSI is enabled and the traditional interrupt pins are not used to generate interrupts. If cleared to 0, MSI operation is disabled and the traditional interrupt pins are used. **Power Well:** Core

7.4.273 Message Signaled Interrupt Message Address (MSI_MAD_MMIO)—Offset 8684h

Access Method

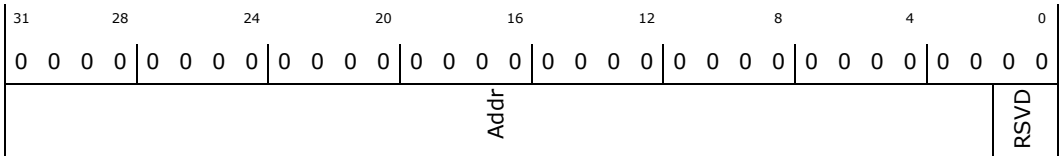
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8684h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Addr:** Lower DW of system specified message address, always DWORD aligned **Power Well:** Core
1:0	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

7.4.274 Message Signaled Interrupt Upper Address (MSI_MUAD_MMIO)—Offset 8688h

Access Method

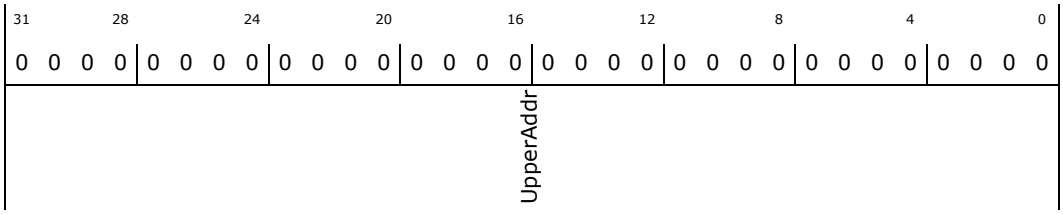
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8688h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Upper Addr (UpperAddr):** Upper DW of system specified message address. **Power Well:** Core

7.4.275 Message Signaled Interrupt Message Data (MSI_MD_MMIO)—Offset 868Ch

Access Method

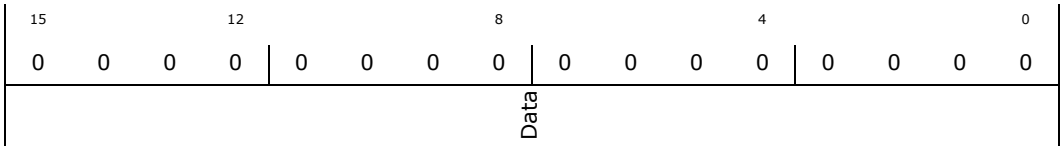
Type: Message Bus Register (Size: 16 bits)

Offset: [Port: 0x5A] + 868Ch

Op Codes:

h - Read, h - Write

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW	**Data:** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD(15:0)) during the data phase of the MSI memory write transaction. The Multiple Message Enable field (bits 6-4 of the Message Control register) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010 indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000, the function is not permitted to modify the message data. **Power Well:** Core

7.4.276 Fuse and Strap (FUS_MMIO)—Offset 8694h

Access Method

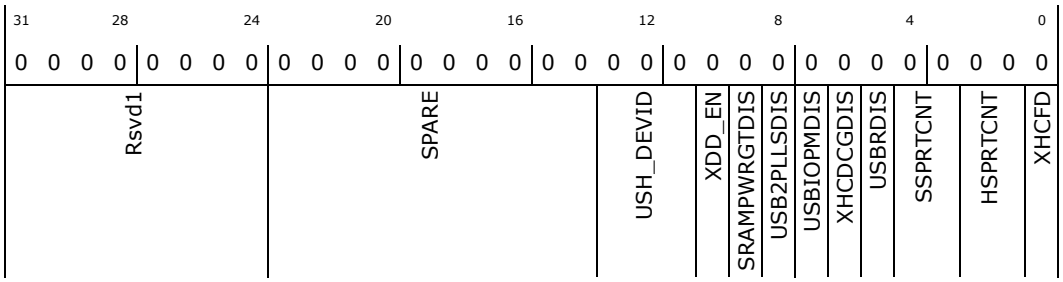
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8694h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
23:14	0x0 RO/V	**Spare Fuses (SPARE):** **Power Well:** SUS
13:11	0x0 RO/V	**USH DevID (USH_DEVID):** LSB bits of USH PCIe Device ID The 3 LSB bits enable defining up to 8 separate USH SKUs if required **Power Well:** SUS
10	0x0 RO/V	**Debug Device Enable (XDD_EN):** 0 : Debug Device is Enabled 1: Debug Device is Disabled **Power Well:** SUS
9	0x0 RO/V	**SRAM Power Gating Disable (SRAMPWRGTDIS):** 0: SRAM Power Gating Enabled 1: SRAM Power Gating Disabled **Power Well:** SUS
8	0x0 RO/V	**USB2 PLL Shutdown Disable (USB2PLLSDIS):** 0: USB2 PLL shutdown enabled 1: USB2 PLL shutdown disabled **Power Well:** SUS
7	0x0 RO/V	**USB I/O Power Management Disable (USBIOPMDIS):** 0: USB2 HW LPM and USB3 HW Ux under XHC enabled 1: USB2 HW LPM and USB3 HW Ux under XHC disabled **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
6	0x0 RO/V	**XHC Dynamic Clock Gating Disable (XHCDCGDIS):** 0: USB3 (XHC) dynamic clock gating enabled 1: USB3 (XHC) dynamic clock gating disabled **Power Well:** SUS
5	0x0 RO/V	**USBr Disable (USBRDIS):** 0: USBr enabled 1: USBr disabled **Power Well:** SUS
4:3	0x0 RO/V	**SS Port Count (SSPRTCNT):** This field specifies number of SS ports present. Supported combinations are: 00: 6 SS ports 01: 4 SS ports 10: 2 SS ports 11: 0 SS ports **Power Well:** SUS
2:1	0x0 RO/V	**HS Port Count (HSPRTCNT):** This field specifies number HS ports present. Supported combinations are: 00: 14 HS ports 01: 12 HS ports 10: 10 HS ports 11: N/A (reserved) **Power Well:** SUS
0	0x0 RO/V	**XHCI Function Disable (XHCFD):** When asserted, it indicates the XHCI is fused to function disabled. **Power Well:** SUS

7.4.277 High Speed Configuration 2 (HSCFG2_MMIO)—Offset 86A4h

Access Method

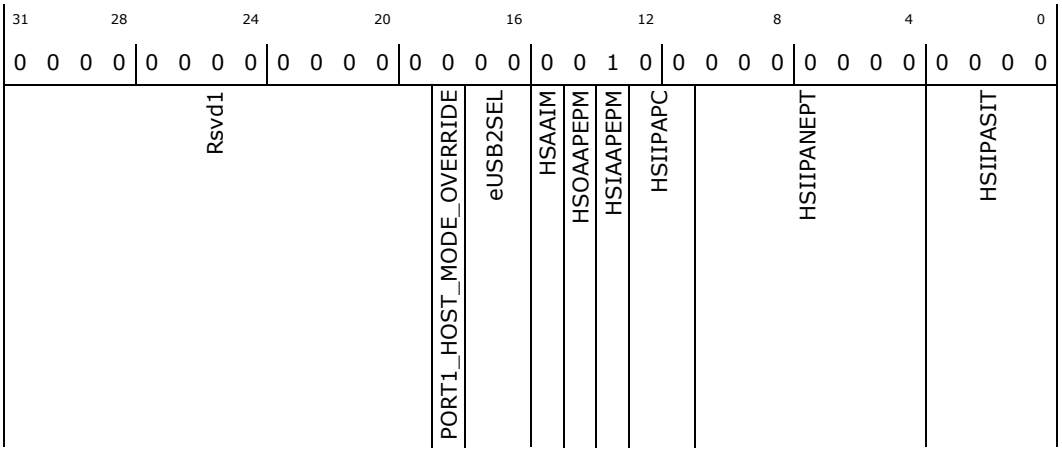
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 86A4h

Op Codes:

h - Read, h - Write

Default: 00002000h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0x0 RO	**Rsvd1:** Reserved. **Power Well:** Core
18	0x0 RW	**PORT1_HOST_MODE_OVERRIDE:** When set, this bit causes the Host_Device mux on port 1 to be forced into the Host mode. **Power Well:** Core
17:16	0x0 RW	**eUSB2SEL:** The two bits are associate with USB2 ports 1 - bit 16 and 2 - bit 2 0: Port is mapped to USB2 1: Port is mapped to eUSB2 **Power Well:** Core
15	0x0 RW	**HS ASYNC Active IN Mask (HSAAIM):** Determines if the Async Active will mask/ignore IN EP s. 0 HS ASYNC Active will include IN EP s. 1 HS ASYNC Active will mask/ignore IN EP s. **Power Well:** Core
14	0x0 RW	**HS OUT ASYNC Active Polling EP Mask (HSOAAPEPM):** Determines if the Async Active for OUT HS/FS/LS masks/ignores EP s that are polling/ PINGing (HS) due to NAK. 0 HS OUT ASYNC Active will include EP s that are polling. 1 HS OUT ASYNC Active will mask/ignore EP s that are polling. **Power Well:** Core
13	0x1 RW	**HS IN ASYNC Active Polling EP Mask (HSIAAPEPM):** Determines if the Async Active for IN HS/FS/LS masks/ignores EP s that are polling due to NAK. 0 HS IN ASYNC Active will include EP s that are polling. 1 HS IN ASYNC Active will mask/ignore EP s that are polling. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12:11	0x0 RW	**HS INTR IN Periodic Active Policy Control (HSIIPAPC):** Controls how the HS INTR IN periodic active is used to generate the global periodic active. This will determine how the smallest service interval among active EP s and number of active EP s are used. 0 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold OR Numb of EP Threshold values meet the requirement. 1 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold AND Numb of EP Threshold values meet the requirement. 2 Always allow HS INTR EP s to be used in the generation of the global Periodic Active indication. 3 Never allow HS INTR EP s to be used in the generation of the global Periodic Active indicaiton **Power Well:** Core
10:4	0x0 RW	**HS INTR IN Periodic Active Num of EP Threshold (HSIIPANEPT):** Defines the threshold used to determine if Periodic Acive may include HS/FS/LS INTR IN EP active indication. If there are more than NumEPThreshold active HS/FS/LS INTR EP s then they may be included as part of the periodic active generation. **Power Well:** Core
3:0	0x0 RW	**HS INTR IN Periodic Active Service Interval Threshold (HSIIPASIT):** Defines the Service Interval threshold used to determine if Periodic Acive will include HS/FS/LS INTR IN EP active indication. If there are any active HS/FS/LS INTR EP s with a service interval less than or equal to this threshold then they may be included as part of the periodic active generation. **Power Well:** Core

7.4.278 XHCI USB2 Overcurrent Pin Mapping 1 (U2OCM1_MMIO)—Offset 86B0h

Reserved

Access Method

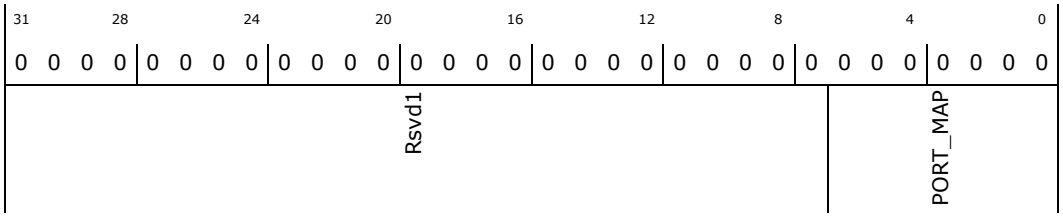
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 86B0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**Rsvd (Rsvd1):** Reserved **Power Well:** Core
6:0	0x0 RW/L	**Port mapping (PORT_MAP):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std **Power Well:** Core

7.4.279 XHCI USB2 Overcurrent Pin Mapping 2 (U2OCM2_MMIO)—Offset 86B4h

Reserved

Access Method

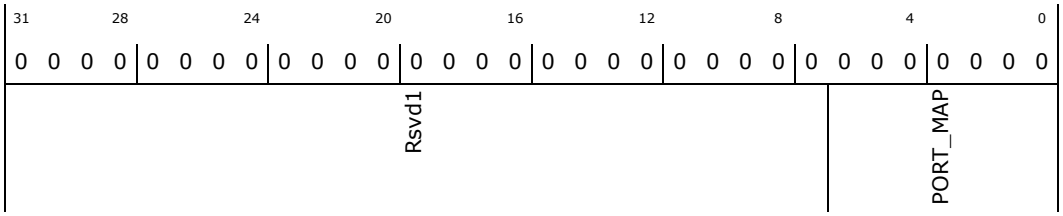
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 86B4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**Rsvd (Rsvd1):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
6:0	0x0 RW/L	**Port mapping (PORT_MAP):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std **Power Well:** Core

7.4.280 XHCI USB3 Overcurrent Pin Mapping 1 (U3OCM1_MMIO)—Offset 86D0h

Reserved

Access Method

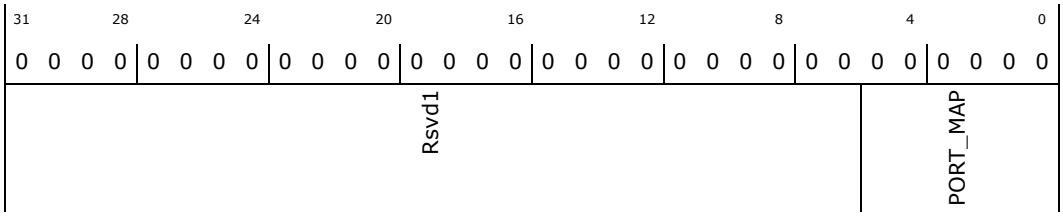
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 86D0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**Rsvd (Rsvd1):** Reserved **Power Well:** Core
5:0	0x0 RW/L	**Port mapping (PORT_MAP):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std **Power Well:** Core

7.4.281 XHCI USB3 Overcurrent Pin Mapping 2 (U3OCM2_MMIO)—Offset 86D4h

Reserved

Access Method

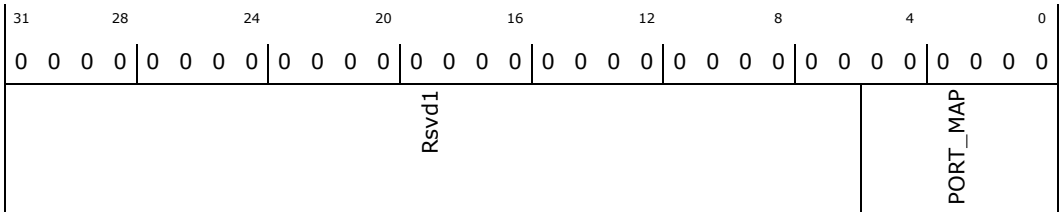
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 86D4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**Rsvd (Rsvd1):** Reserved **Power Well:** Core
5:0	0x0 RW/L	**Port mapping (PORT_MAP):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std **Power Well:** Core

7.4.282 Debug Capability ID Register (DCID)—Offset 8700h

This register is modified and maintained by BIOS

Access Method

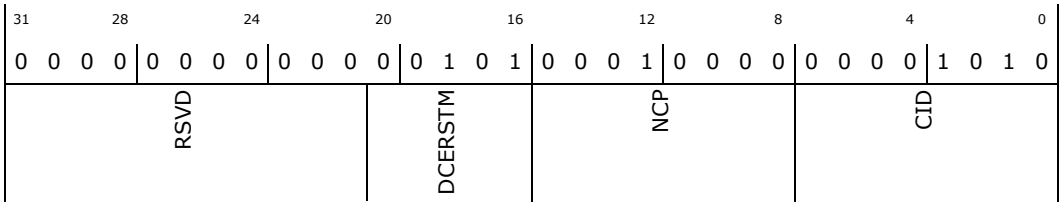
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8700h

Op Codes:

h - Read, h - Write

Default: 0005100Ah



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
20:16	0x5 RW	**Debug Capability Event Ring Segment Table Max (DCERSTM):** Note: This register is sticky. **Power Well:** Core
15:8	0x10 RW	**Next Capability Pointer (NCP):** Note: This register is sticky. **Power Well:** Core
7:0	0xa RW	**Capability ID (CID):** Note: This register is sticky. **Power Well:** Core

7.4.283 Debug Capability Doorbell Register (DCDB)—Offset 8704h

Access Method

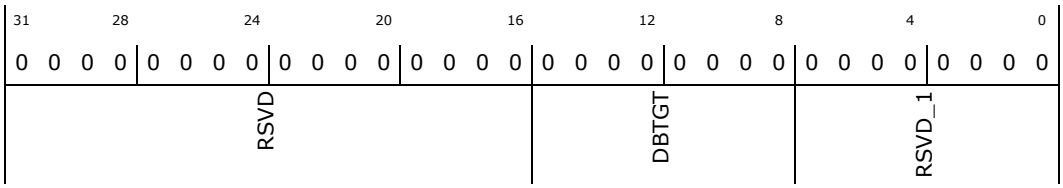
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8704h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (RSVD):** Reserved. **Power Well:** Core
15:8	0x0 RW	**Doorbell Target (DBTGT):** This field defines the target of the doorbell reference. The table below defines the Debug Capability notification that is generated by ringing the doorbell. Value Definition 0 Data EP 1 OUT Enqueue Pointer Update 1 Data EP 1 IN Enqueue Pointer Update 2:255 Reserved This field returns '0' when read and the value should be treated as undefined by software. **Power Well:** Core
7:0	0x0 RW	**Reserved (RSVD_1):** Reserved. **Power Well:** Core

7.4.284 Debug Capability Event Ring Segment Table Size Register (DCERSTSZ)—Offset 8708h

Access Method

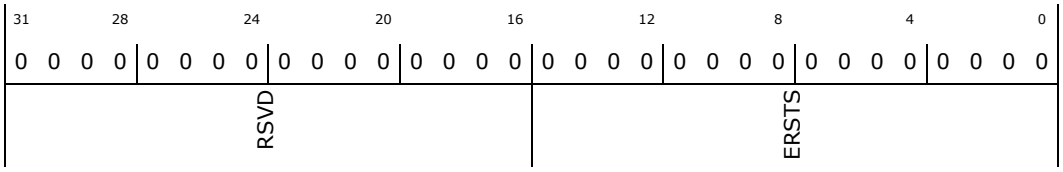
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8708h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved (RSVD):** Reserved. **Power Well:** Core
15:0	0x0 RW	**Event Ring Segment Table Size (ERSTS):** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Debug Capability Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the DCERST Max field in the DCID register Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'. **Power Well:** Core

7.4.285 Debug Capability Event Ring Segment Table Base Address Register (DCERSTBA)—Offset 8710h

Access Method

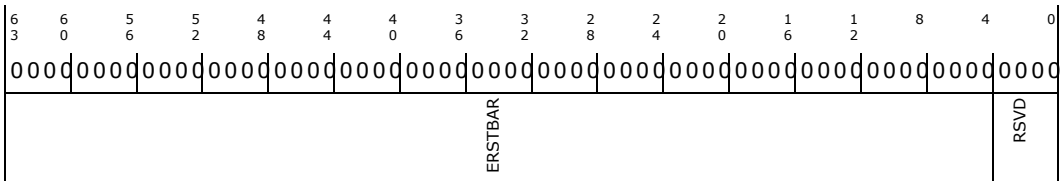
Type: Message Bus Register (Size: 64 bits)

Offset: [Port: 0x5A] + 8710h

Op Codes:

h - Read, h - Write

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:4	0x0 RW	**Event Ring Segment Table Base Address Register (ERSTBAR):** This field defines the high order bits of the start address of the Debug Capability Event Ring Segment Table. Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'. **Power Well:** Core
3:0	0x0 RW	**Reserved (RSVD):** Reserved. **Power Well:** Core

7.4.286 Debug Capability Event Ring Dequeue Pointer Register (DCERDP)—Offset 8718h

Access Method

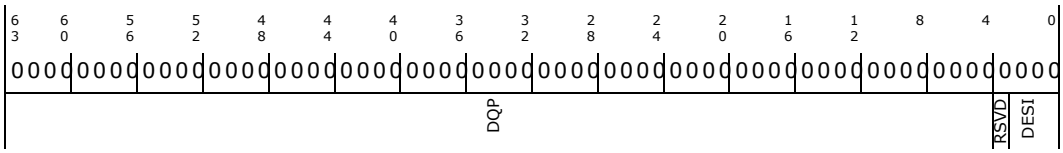
Type: Message Bus Register (Size: 64 bits)

Offset: [Port: 0x5A] + 8718h

Op Codes:

h - Read, h - Write

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:4	0x0 RW	**Dequeue Pointer (DQP):** This field defines the high order bits of the 64-bit address of the current Debug Capability Event Ring Dequeue Pointer. Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'. **Power Well:** Core
3	0x0 RW	**Reserved (RSVD):** Reserved. **Power Well:** Core
2:0	0x0 RW	**Dequeue ERST Segment Index (DESI):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. **Power Well:** Core

7.4.287 Debug Capability Control Register (DCCTRL)—Offset 8720h

Access Method

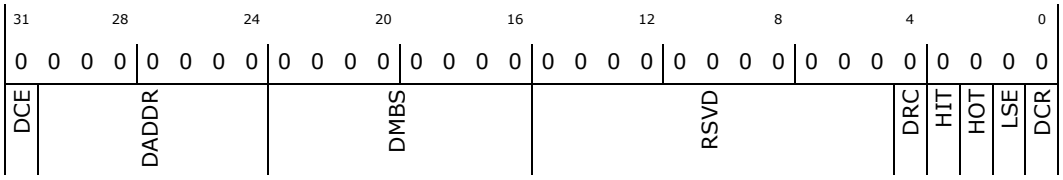
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8720h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Debug Capability Enable (DCE):** Reserved. **Power Well:** Core
30:24	0x0 RO	**Device Address (DADDR):** Reserved. **Power Well:** Core
23:16	0x0 RO	**Debug Max Burst Size (DMBS):** USB Debug Device does not support bursting. **Power Well:** Core
15:5	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
4	0x0 RW/C	**DbC Run Change (DRC):** Reserved. **Power Well:** Core
3	0x0 RW/1S	**Halt IN TR (HIT):** Reserved. **Power Well:** Core
2	0x0 RW/1S	**Halt OUT TR (HOT):** Reserved. **Power Well:** Core
1	0x0 RW	**Link Status Event Enable (LSE):** Reserved. **Power Well:** Core
0	0x0 RO	**DbC Run (DCR):** Reserved. **Power Well:** Core

7.4.288 Debug Capability Status Register (DCST)—Offset 8724h

Access Method

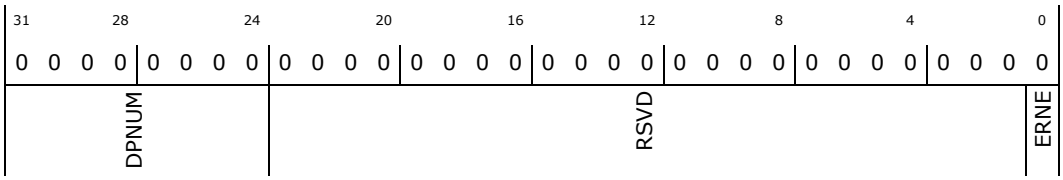
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8724h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Debug Port Number (DPNUM):** This field provides the ID of the Root Hub port that the Debug Capability has been automatically attached to. The value is '0' when the Debug Capability is not attached to a Root Hub port. **Power Well:** Core
23:1	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
0	0x0 RO	**Event Ring Not Empty (ERNE):** When '1', this field indicates that the Debug Capability Event Ring has a Transfer Event on it. It is automatically cleared to '0' by the xHC when the Debug Capability Event Ring is empty, i.e. the Debug Capability Enqueue Pointer is equal to the Debug Capability Event Ring Dequeue Pointer register. **Power Well:** Core

7.4.289 Debug Capability Port Status and Control Register (DCPORTSC)—Offset 8728h

Access Method

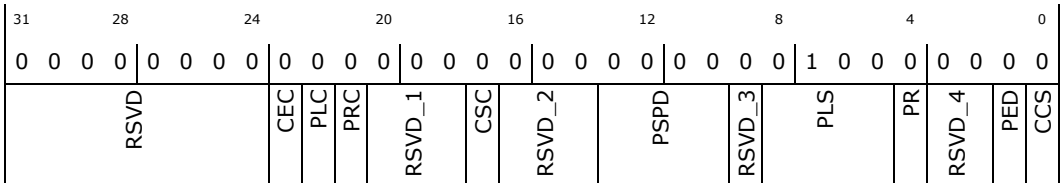
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8728h

Op Codes:

h - Read, h - Write

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
23	0x0 RW/C	**Port Config Error Change (CEC):** This flag indicates that the port failed to configure its link partner. 0 = No change. 1 = Port Config Error detected. Software shall clear this bit by writing a '1' to it. **Power Well:** Core
22	0x0 RW/C	**Port Link Status Change (PLC):** This flag is set to '1' due to the following PLS transitions: U0 -) U3 Suspend signaling detected from Debug Host U3 -) U0 Resume complete Polling -) Disabled Training Error Ux or Recovery -) Inactive Error Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0' **Power Well:** Core
21	0x0 RW/C	**Port Reset Change (PRC):** This bit is set when reset processing on this port is complete (i.e. a '1' to '0' transition of PR). '0' = No change. '1' = Reset complete.Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'. **Power Well:** Core
20:18	0x0 RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core
17	0x0 RW/C	**Connect Status Change (CSC):** an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'. **Power Well:** Core
16:14	0x0 RO	**Reserved (RSVD_2):** Reserved. **Power Well:** Core
13:10	0x0 RO	**Port Speed (PSPD):** This field identifies the speed of the port. This field is only relevant when a Debug Host is attached (CCS = '1') in all other cases this field shall indicate Undefined Speed. 0 Undefined Speed 1-15 Protocol Speed ID (PSI) Note: The Debug Capability onlydoes not supports LS, FS, or HS operation. **Power Well:** Core
9	0x0 RO	**Reserved (RSVD_3):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
8:5	0x4 RO	**Port Link State (PLS):** This field reflects its current link state. This field is only relevant when a Debug Host is attached (Debug Port Number) '0'). Value Meaning 0 Link is in the U0 State 1 Link is in the U1 State 2 Link is in the U2 State 3 Link is in the U3 State (Device Suspended) 4 Link is in the Disabled State 5 Link is in the RxDetect State 6 Link is in the Inactive State 7 Link is in the Polling State 8 Link is in the Recovery State 9 Link is in the Hot Reset State 15:10 Reserved Note: Transitions between different states are not reflected until the transition is complete. **Power Well:** Core
4	0x0 RO	**Port Reset (PR):** '1' = Port is in Reset. '0' = Port is not in Reset. This bit is set to '1' when the bus reset sequence as defined in the USB Specification is detected on the Root Hub port assigned to the Debug capability. It is cleared when the bus reset sequence is completed by the Debug Host, and the DbC shall transition to the USB Default state. A '0' to '1' transition of this bit shall clear DCPORTSC PED ('0'). This field is '0' if DCE or CCS are '0'. **Power Well:** Core
3:2	0x0 RO	**Reserved (RSVD_4):** Reserved. **Power Well:** Core
1	0x0 RW	**Port Enabled/Disabled (PED):** Default = '0'. '1' = Enabled. '0' = Disabled. This flag shall be set to '1' by a '0' to '1' transition of CCS or a '1' to '0' transition of the PR. When PED transitions from '1' to '0' due to the assertion of PR, the port's link shall transition to the Rx.Detect state. This flag may be used by software to enable or disable the operation of the Root Hub port assigned to the Debug Capability. The Debug Capability Root Hub port operation may be disabled by a fault condition (disconnect event or other fault condition, e.g. a LTSSM Polling substate timeout, tPortConfiguration timeout error, etc.), the assertion of DCPORTSC PR, or by software. 0 = Debug Capability Root Hub port is disabled. 1 = Debug Capability Root Hub port is enabled. When the port is disabled (PED = '0') the port's link shall enter the SS.Disabled state and remain there until PED is reasserted ('1') or DCE is negated ('0'). Note that the Root Hub port is remains mapped to Debug Capability while PED = '0'. While PED = '0' the Debug Capability will appear to be disconnected to the Debug Host. Note, this bit is not affected by PORTSC PR bit transitions. This field is '0' if DCE or CCS are '0'. **Power Well:** Core
0	0x0 RO	**Current Connect Status (CCS):** '1' = A Root Hub port is connected to a Debug Host and assigned to the Debug Capability. '0' = No Debug Host is present. This value reflects the current state of the port, and may not correspond to the value reported by the Connect Status Change (CSC) field in the Port Status Change Event that was generated by a '0' to '1' transition of this bit. This flag is '0' if Debug Capability Enable (DCE) is '0'. **Power Well:** Core

7.4.290 Debug Capability Context Pointer Register (DCCP)—Offset 8730h

Access Method

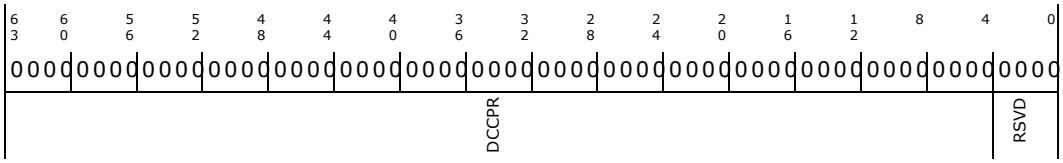
Type: Message Bus Register (Size: 64 bits)

Offset: [Port: 0x5A] + 8730h

Op Codes:

h - Read, h - Write

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:4	0x0 RW	**Debug Capability Context Pointer Register (DCCPR):** This field defines the high order bits of the start address of the Debug Capability Context data structure associated with the Debug Capability. Software shall initialize this register before setting the Debug Capability Enable bit in the Debug Capability Control Register to '1'. **Power Well:** Core
3:0	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

7.4.291 Debug Capability Device Descriptor Info Register 1 (DCDDI1)—Offset 8738h

Access Method

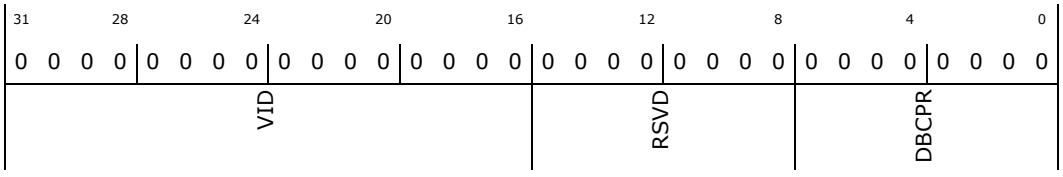
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8738h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Vendor ID (VID):** This field is presented by the Debug Device in the USB Device Descriptor idVendor field. **Power Well:** Core
15:8	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
7:0	0x0 RW	**DbC Protocol (DBCPR):** This field is presented by the Debug Device in the USB Interface Descriptor bInterfaceProtocol field. Value Function 0 Debug Target vendor defined. 1 GNU Remote Debug Command Set supported. 2-255 Reserved. **Power Well:** Core

7.4.292 Debug Capability Device Descriptor Info Register 2 (DCDDI2)—Offset 873Ch

Access Method

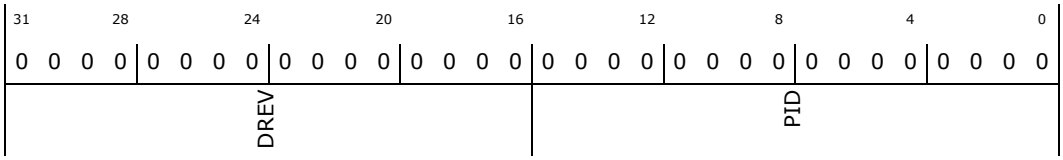
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 873Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Device Revision (DREV):** This field is presented by the Debug Device in the USB Device Descriptor bcdDevice field. **Power Well:** Core
15:0	0x0 RW	**Product ID (PID):** This field is presented by the Debug Device in the USB Device Descriptor idProduct field. **Power Well:** Core

7.4.293 Debug Capability Descriptor Parameters (DCDP)—Offset 8740h

Access Method

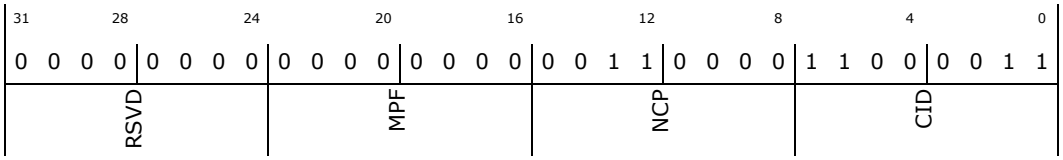
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8740h

Op Codes:

h - Read, h - Write

Default: 000030C3h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
23:16	0x0 RW	**Max Power Field (MPF):** This field will be used by USB Debug Device to report maximum power consumption when the device is fully operational. This value is returned by bMaxPower field in response to Configuration Descriptor read from the debug device. Note: bU1DevExitLat and bU2DevExitLat fields returned in BOS Descriptor read will be taken from the corresponding fields from the Host Controller space. **Power Well:** Core
15:8	0x30 RW/S	**NEXT CAPABILITY POINTER (NCP):** Reserved. **Power Well:** Core
7:0	0xc3 RW/S	**Capability ID (CID):** Reserved. **Power Well:** Core

7.4.294 Debug Device Control ODMA (DBGDEV_CTRL_ODMA_REG)—Offset 8748h

This register contains a number of fields that provide a specific level of configurability for the OUT DMA that is part of Debug Device logic. This configurability is above and beyond that defined in the xHCI specification.

Access Method

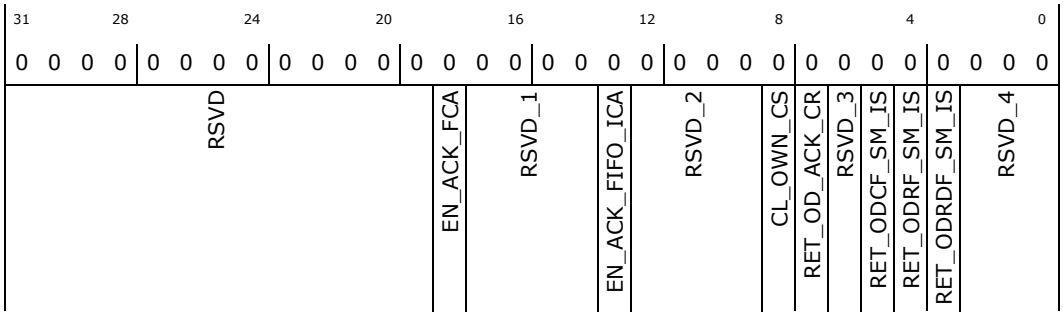
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8748h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0x0 RW	**Reserved (RSVD):** Reserved. **Power Well:** Core
18	0x0 RW	**Enable ACK FIFO credit accounting (EN_ACK_FCA):** Setting this field will enable ACK FIFO credit accounting. ODMA will ensure that ample room exists in the ACK FIFO for expected device responses prior to initiating a given DP **Power Well:** Core
17:14	0x0 RW	**Reserved (RSVD_1):** Reserved. **Power Well:** Core
13	0x0 RW	**Enable ACK FIFO ICA mechanisms (EN_ACK_FIFO_ICA):** Setting this field will enable ACK FIFO individual credit accounting mechanisms for Async vs. Periodic Endpoints. ODMA will ensure that ample room exists in the ACK FIFO for expected device responses prior to initiating a given DP **Power Well:** Core
12:9	0x0 RW	**Reserved (RSVD_2):** Reserved. **Power Well:** Core
8	0x0 RW	**Clear ownership of context semaphore (CL_OWN_CS):** Setting this field generates a pulse that clears the ownership of the context semaphore that is shared between the Out DMA Response and Completion Finite State Machines **Power Well:** Core
7	0x0 RW	**Return OD ACK credits (RET_OD_ACK_CR):** Setting this field generates a pulse that implicitly returns all of the Out DMA ACK credits on all ports **Power Well:** Core
6	0x0 RW	**Reserved (RSVD_3):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**Return ODCF SM to idle state (RET_ODCF_SM_IS):** Setting this field generates a pulse that returns the Out DMA Completion Finite State Machine into the IDLE state **Power Well:** Core
4	0x0 RW	**Return ODRF SM to idle state (RET_ODRF_SM_IS):** Setting this field generates a pulse that returns the Out DMA Response Finite State Machine into the IDLE state **Power Well:** Core
3	0x0 RW	**Return ODRDF SM to idle state (RET_ODRDF_SM_IS):** Setting this field generates a pulse that returns the Out DMA Read Finite State Machine into the IDLE state **Power Well:** Core
2:0	0x0 RW	**Reserved (RSVD_4):** Reserved. **Power Well:** Core

7.4.295 SSIC Policy and Implementation Specific Registers Capability ID register (SSIC_IMPLEMENTATION_CAPABILITY_ID_REG)—Offset 8800h

Chicken bits and Policy bits associated with SSIC

Access Method

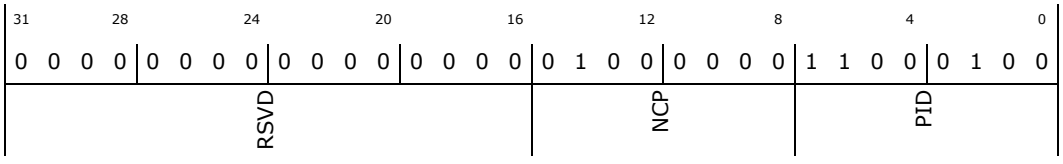
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8800h

Op Codes:

h - Read, h - Write

Default: 000040C4h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
15:8	0x40 RO	**Next Capability Pointer (NCP):** Reserved. **Power Well:** Core
7:0	0xc4 RO	**Supported Protocol ID (PID):** Reserved. **Power Well:** Core

7.4.296 SSIC global configuration control register (SSIC_GLOBAL_CONFIG_CONTROL_REG)—Offset 8804h

Access Method

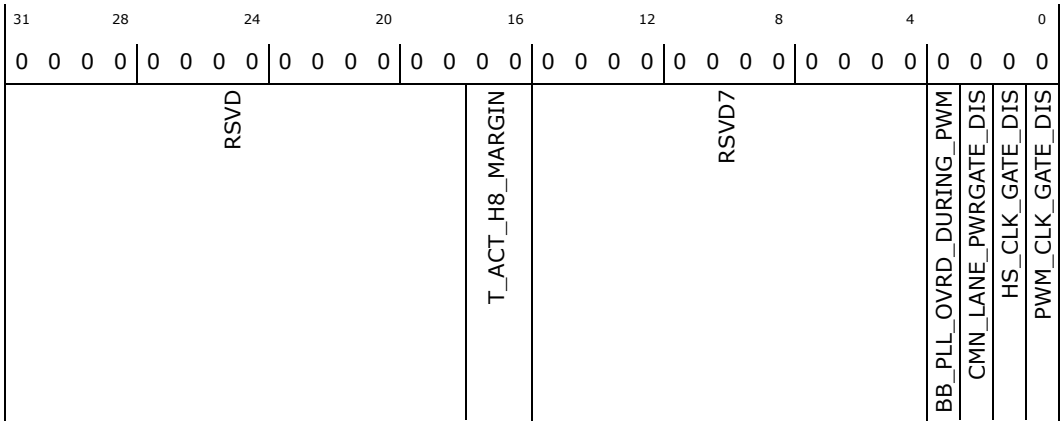
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8804h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
17:16	0x0 RW	**T_ACT_H8_MARGIN:** Specifies the margin time added to the tActivate spec time of 100us in T_ACT_H8_TIME. 11: Reserved 10: 50us 01: 20us (default for ModPHY) 00: 10us (default for MIPI MPHY) **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:4	0x0 RO	**Reserved1 (RSVD7):** Reserved. **Power Well:** Core
3	0x0 RW	**BB_PLL_OVRD_DURING_PWM:** Reserved. **Power Well:** Core
2	0x0 RW	**CMN_LANE_PWRGATE_DIS:** This will disable the MPHY common lane power gate. **Power Well:** Core
1	0x0 RW	**HS_CLK_GATE_DIS:** This will disable the HS Clock gate request from XHCI to MIPI PLL. **Power Well:** Core
0	0x0 RW	**PWM_CLK_GATE_DIS:** This will disable the PWM Clock gate request from XHCI to MIPI PLL. **Power Well:** Core

7.4.297 reg_SSIC_CONFIG_REG1_type (PORT1_SSIC_CONFIG_REG1)—Offset 8808h

Access Method

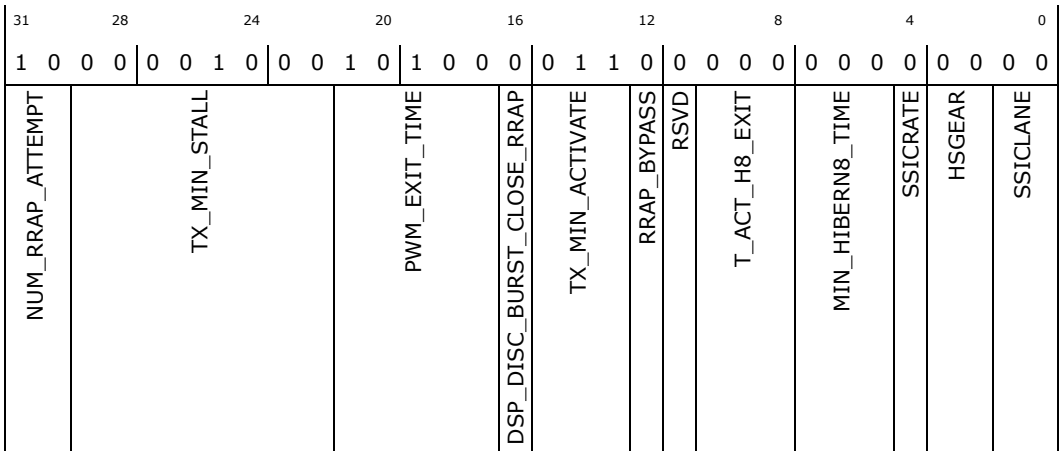
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8808h

Op Codes:

h - Read, h - Write

Default: 82286000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x2 RW	**NUM_RRAP_ATTEMPT:** Specify the number of RRAP access attempt if there was tRRAPInitiatorResponse timeout. **Power Well:** Core
29:22	0x8 RW	**TX_MIN_STALL:** (TX_Min_STALL_NoConfig_Time_Capability in MIPI PHY Spec). PA will ensure TX_MIN_STALL time in STALL before entering HS-BURST or HIBERN8. Specifies minimum time in SI in STALL state. **Power Well:** Core
21:17	0x14 RW	**PWM_EXIT_TIME:** This will be max of RX_Min_ActivateTime_Capability and TX_Min_SAVE_Config_Time_Capability in MIPI PHY Specs) Specifies minimum activate time needed in 5us steps. PA will wait PWM_EXIT_TIME time after exiting PWM to start HS-BURST. SSIC spec requires it to be at 100us. For speedup mode this time would be in 1us steps. **Power Well:** Core
16	0x0 RW	**DSP_DISC_BURST_CLOSE_RRAP:** 0 - Send BURST Closure RRAP for DSP Disconnect 1 - Dont send Burst Closure RRAP for DSP Disconnect. For device PWM exit would be indication for DSP Disconnect. **Power Well:** Core
15:13	0x3 RW	**TX_MIN_ACTIVATE:** (TX_Min_ActivateTime in MIPI PHY Spec) Specifies minimum activate time needed in 100us steps. PA will wait TX_MIN_ACTIVATE time after H8 exit to start of PWM Burst. SSIC spec requires it to be at 1.5ms. For speedup mode this time would be 10us to 150us in steps of 10us. **Power Well:** Core
12	0x0 RW	**RRAP_BYPASS:** Enables DFx Loopback test mode where RRAP command / response is bypassed for HS_CONFIG and PWM_BURST_CLOSURE. Host will still perform initial enter and exit PWM mode with no RRAP transfers. **Power Well:** Core
11	0x0 RW	**Reserved (RSVD):** Reserved. **Power Well:** Core
10:8	0x0 RW	**T_ACT_H8_EXIT:** Specifies minimum time in 100us steps for T_ACTIVATE_TIME to exit H8. Val: Si Time / Fast Sim Time 000: 110us / 10us 001: 210us / 20us 110: 710us / 70us 111: 5ms / 500us Spec required timing is 100us. **Power Well:** Core
7:5	0x0 RW	**MIN_HIBERN8_TIME:** Minimum time in HIBERN8 state 0 110us 1 210us .. 7 810us PA will ensure MIN_HIBERN8_TIME in its TX HIBERN8. For speedup mode this time will be from 10us to 80us in steps of 10us. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**SSICRATE:** 0 A Series 1 B Series **Power Well:** Core
3:2	0x0 RW	**HSGEAR:** 0=HS-G1 1=HS-G2 2=HS-G3 **Power Well:** Core
1:0	0x0 RW	**SSICLANE:** 0=Single lane 1=Bi-lane 2=Quad-lane **Power Well:** Core

7.4.298 reg_SSIC_CONFIG_REG2_type (PORT1_SSIC_CONFIG_REG2)—Offset 880Ch

Access Method

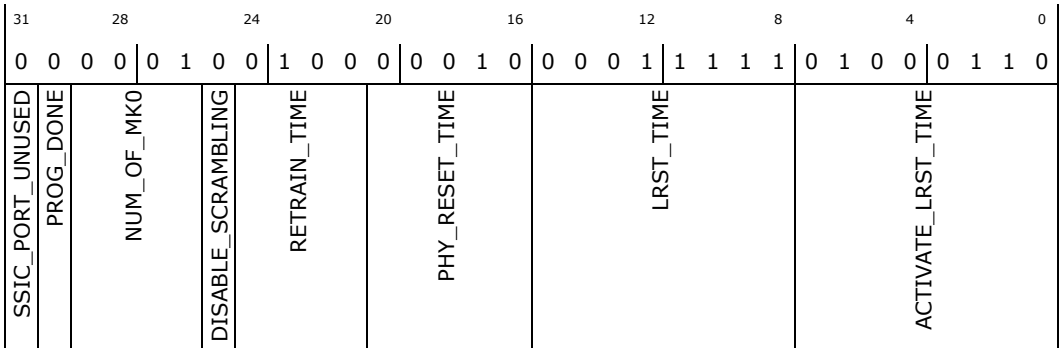
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 880Ch

Op Codes:

h - Read, h - Write

Default: 04821F46h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SSIC_PORT_UNUSED:** This indicates that no SSIC device is connected to the port and PORTSC register would always reflect DISCONNECTED. **Power Well:** Core
30	0x0 RW	**PROG_DONE:** BIOS will program this bit once SSIC profile programming is done. SSIC will enable the MPHY and local PLL once this bit is set. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
29:26	0x1 RW	**NUM_OF_MK0:** Number of MK0 which transmitter will send before sending any data. **Power Well:** Core
25	0x0 RW	**DISABLE_SCRAMBLING:** This bit will disable scrambling in HS-BURST **Power Well:** Core
24:21	0x4 RW	**RETRAIN_TIME:** Corresponds to time in 10us to detect improper training of the local and remote M-RX as part of HS-BURST entry. SSIC Spec specific 40 to 50us **Power Well:** Core
20:16	0x2 RW	**PHY_RESET_TIME:** Corresponds to time in 100ns, PA will drive PHY RESET for MIPI PHY. **Power Well:** Core
15:8	0x1f RW	**LRST_TIME:** Corresponds to time in 100us PA will drive DIF-P for line reset. MIPI PHY specifies 3.1 ms Minimum. For speedup mode this time will be in steps of 5us. **Power Well:** Core
7:0	0x46 RW	**ACTIVATE_LRST_TIME:** (Corresponds to tResetDIFN) Specifies in step of 1ms period of time a DSP is required to drive a DIF-N prior to a LINE-RESET. SSIC spec defined range is 60-80ms. For speedup mode this time will be from 5us to 400us in steps of 5us. **Power Well:** Core

7.4.299 reg_SSIC_CONFIG_REG3_type (PORT1_SSIC_CONFIG_REG3)—Offset 8810h

Access Method

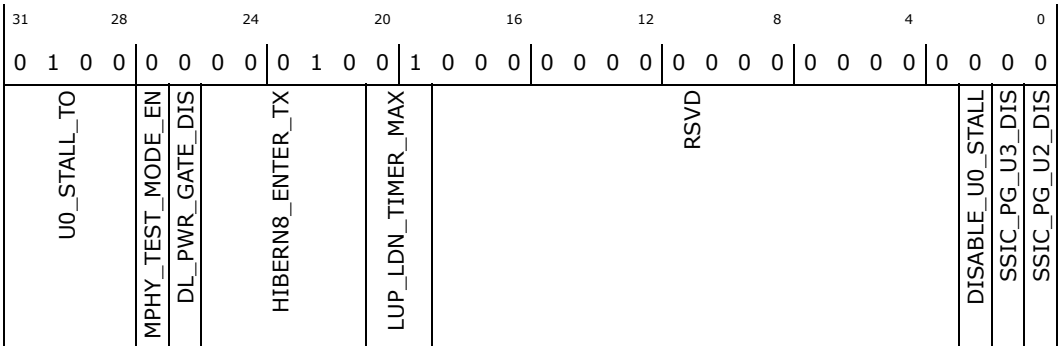
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8810h

Op Codes:

h - Read, h - Write

Default: 40480000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x4 RW	**U0_STALL_TO:** Time in 2^[U-STALL_TO] clock for U0 STALL entry. If there is no packet in arbiter for U0_STALL_TO time, PA will enable U0 STALL if DISABLE_U0_STALL is not set. 0000 0011 (Not recommended) 0100 16 SSIC HS CLK . 1111 32768 SSIC HS CLK **Power Well:** Core
27	0x0 RW	**MPHY_TEST_MODE_EN:** When this bit is set, controller would not initiate any PWM once it enters PWM Mode. It will wait for tester to send Loopback RRAP Command. **Power Well:** Core
26	0x0 RW	**DL_PWR_GATE_DIS:** Reserved. **Power Well:** Core
25:21	0x2 RW	**HIBERN8_ENTER_TX:** The time PA will drive DIF-N after last bit of Line-CFG before entering H8. In steps of 50ns. Legal range is 50 to 1000ns. **Power Well:** Core
20:19	0x1 RW	**LUP_LDN_TIMER_MAX:** 00: 10 us 01: 100 us 10: 1000us /1ms 11: (Timer is disable and dont transmit LDN) **Power Well:** Core
18:3	0x0 RW	**RESERVED (RSVD):** rsvd **Power Well:** Core
2	0x0 RW	**DISABLE_U0_STALL:** This bit will disable the STALL entry in U0 **Power Well:** Core
1	0x0 RW	**SSIC_PG_U3_DIS:** This disables MPHY DL PG during U3. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**SSIC_PG_U2_DIS:** This disables MPHY DL PG during U2. **Power Well:** Core

7.4.300 reg_SSIC_CONFIG_REG4_type (PORT1_SSIC_CONFIG_REG4)—Offset 8814h

Access Method

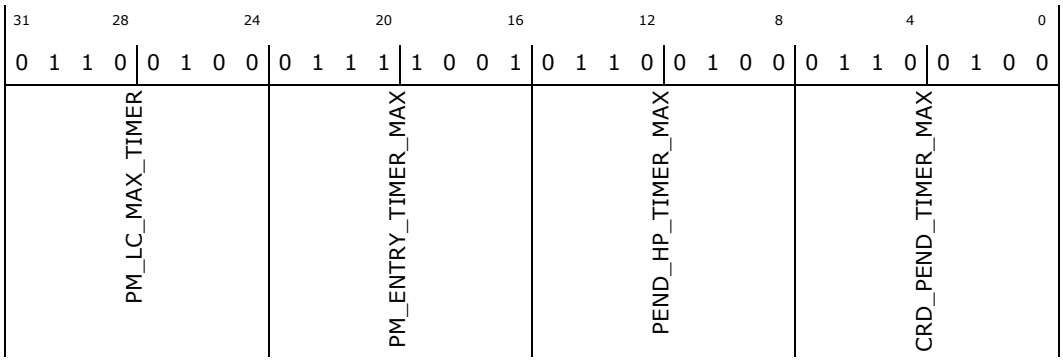
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8814h

Op Codes:

h - Read, h - Write

Default: 64796464h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x64 RW	**PM_LC_MAX_TIMER:** In steps of 1us. Default 100us **Power Well:** Core
23:16	0x79 RW	**PM_ENTRY_TIMER_MAX:** In steps of 1us. Default 100us **Power Well:** Core
15:8	0x64 RW	**PEND_HP_TIMER_MAX:** In steps of 1us. Default 100us **Power Well:** Core
7:0	0x64 RW	**CRD_PEND_TIMER_MAX:** In steps of 1us. Default 100us **Power Well:** Core

7.4.301 reg_SSIC_LOOPBACK_CONFIG_REG_type (PORT1_SSIC_LOOPBACK_CONFIG_REG)—Offset 8818h

Access Method

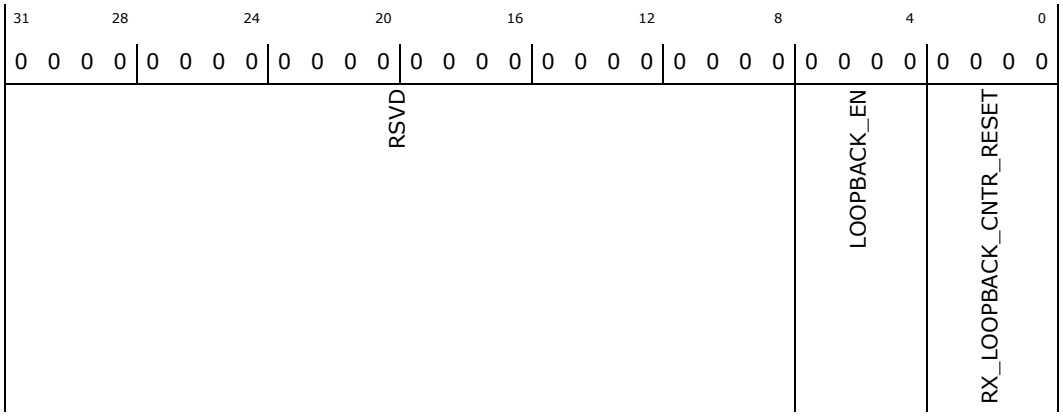
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8818h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core
7:4	0x0 RO	**LOOPBACK_EN:** This Register is used to enable Conformance Loopback in the Target in the specified PAIR.. Bit [0]: Writing 1b1 enables the loopback mode in PAIR0. Writing 1b0 shall have no effect. Bit [1]: Writing 1b1 enables the loopback mode in PAIR1. Writing 1b0 shall have no effect. Bit [2]: Writing 1b1 enables the loopback mode in PAIR2. Writing 1b0 shall have no effect. Bit [3]: Writing 1b1 enables the loopback mode in PAIR3. Writing 1b0 shall have no effect. **Power Well:** Core
3:0	0x0 RO	**RX LOOPBACK CNTR RESET (RX_LOOPBACK_CNTR_RESET):** Reset RX_BURST_COUNT and RX_ERR_COUNT, write only, self-clearing. Bit [0] for PAIR0 Bit [1] for PAIR1 Bit [2] for PAIR2 Bit [3] for PAIR3 **Power Well:** Core

7.4.302 reg_SSIC_LOOPBACK_BURST_COUNT_REG_type (PORT1_SSIC_LOOPBACK_BURST_COUNT_REG)—Offset 881Ch

Access Method

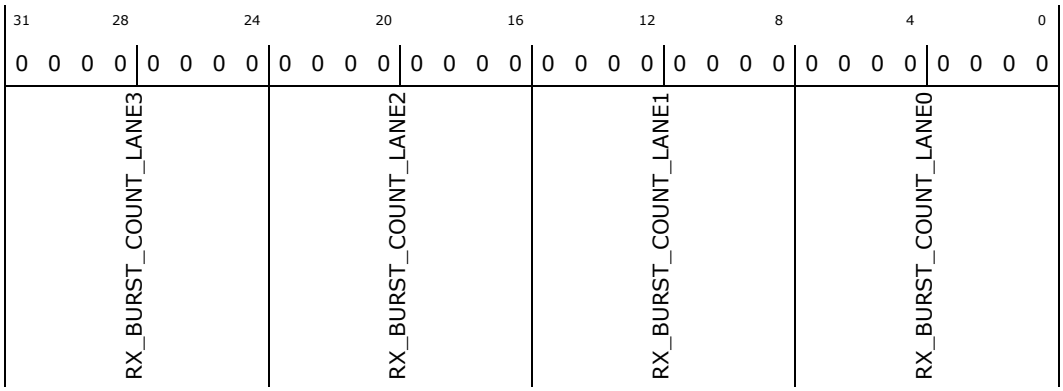
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 881Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RX_BURST_COUNT_LANE3:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
23:16	0x0 RO	**RX_BURST_COUNT_LANE2:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
15:8	0x0 RO	**RX_BURST_COUNT_LANE1:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
7:0	0x0 RO	**RX_BURST_COUNT_LANE0:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core

7.4.303 reg_SSIC_LOOPBACK_ERROR_COUNT_REG_type (PORT1_SSIC_LOOPBACK_ERROR_COUNT_REG)—Offset 8820h

Access Method

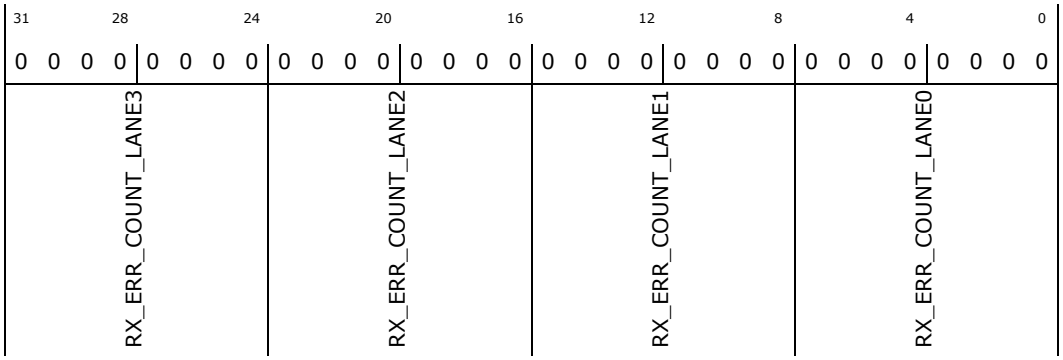
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8820h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RX_ERR_COUNT_LANE3:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
23:16	0x0 RO	**RX_ERR_COUNT_LANE2:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
15:8	0x0 RO	**RX_ERR_COUNT_LANE1:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
7:0	0x0 RO	**RX_ERR_COUNT_LANE0:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core

7.4.304 reg_SSIC_CONFIG_REG1_type (PORT2_SSIC_CONFIG_REG1)—Offset 8838h

Access Method

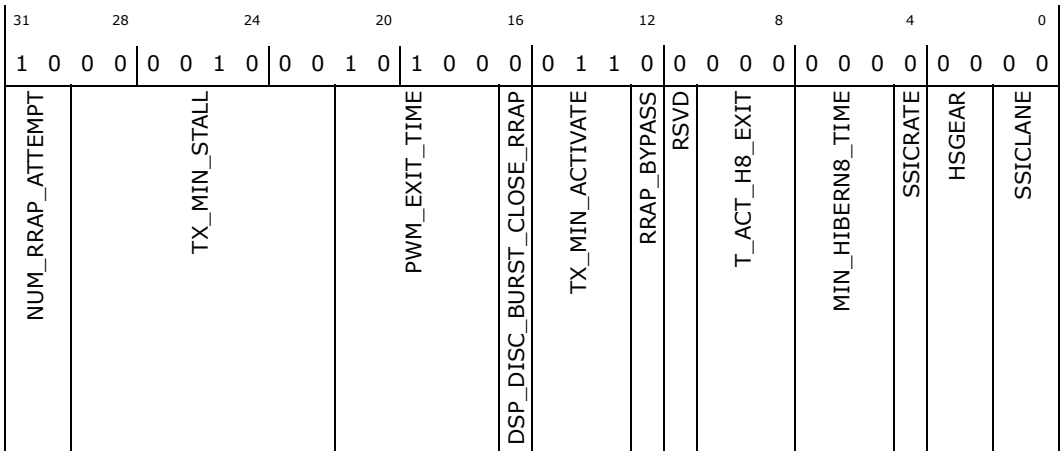
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8838h

Op Codes:

h - Read, h - Write

Default: 82286000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x2 RW	**NUM_RRAP_ATTEMPT:** Specify the number of RRAP access attempt if there was tRRAPInitiatorResponse timeout. **Power Well:** Core
29:22	0x8 RW	**TX_MIN_STALL:** (TX_Min_STALL_NoConfig_Time_Capability in MIPI PHY Spec). PA will ensure TX_MIN_STALL time in STALL before entering HS-BURST or HIBERN8. Specifies minimum time in SI in STALL state. **Power Well:** Core
21:17	0x14 RW	**PWM_EXIT_TIME:** This will be max of RX_Min_ActivateTime_Capability and TX_Min_SAVE_Config_Time_Capability in MIPI PHY Specs) Specifies minimum activate time needed in 5us steps. PA will wait PWM_EXIT_TIME time after exiting PWM to start HS-BURST. SSIC spec requires it to be at 100us. For speedup mode this time would be in 1us steps. **Power Well:** Core
16	0x0 RW	**DSP_DISC_BURST_CLOSE_RRAP:** 0 - Send BURST Closure RRAP for DSP Disconnect 1 - Dont send Burst Closure RRAP for DSP Disconnect. For device PWM exit would be indication for DSP Disconnect. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:13	0x3 RW	**TX_MIN_ACTIVATE:** (TX_Min_ActivateTime in MIPI PHY Spec) Specifies minimum activate time needed in 100us steps. PA will wait TX_MIN_ACTIVATE time after H8 exit to start of PWM Burst. SSIC spec requires it to be at 1.5ms. For speedup mode this time would be 10us to 150us in steps of 10us. **Power Well:** Core
12	0x0 RW	**RRAP_BYPASS:** Enables DFx Loopback test mode where RRAP command / response is bypassed for HS_CONFIG and PWM_BURST_CLOSURE. Host will still perform initial enter and exit PWM mode with no RRAP transfers. **Power Well:** Core
11	0x0 RW	**Reserved (RSVD):** Reserved. **Power Well:** Core
10:8	0x0 RW	**T_ACT_H8_EXIT:** Specifies minimum time in 100us steps for T_ACTIVATE_TIME to exit H8. Val: Si Time / Fast Sim Time 000: 110us / 10us 001: 210us / 20us 110: 710us / 70us 111: 5ms / 500us Spec required timing is 100us. **Power Well:** Core
7:5	0x0 RW	**MIN_HIBERN8_TIME:** Minimum time in HIBERN8 state 0 110us 1 210us .. 7 810us PA will ensure MIN_HIBERN8_TIME in its TX HIBERN8. For speedup mode this time will be from 10us to 80us in steps of 10us. **Power Well:** Core
4	0x0 RW	**SSICRATE:** 0 A Series 1 B Series **Power Well:** Core
3:2	0x0 RW	**HSGEAR:** 0=HS-G1 1=HS-G2 2=HS-G3 **Power Well:** Core
1:0	0x0 RW	**SSICLANE:** 0=Single lane 1=Bi-lane 2=Quad-lane **Power Well:** Core

7.4.305 reg_SSIC_CONFIG_REG2_type (PORT2_SSIC_CONFIG_REG2)—Offset 883Ch

Access Method

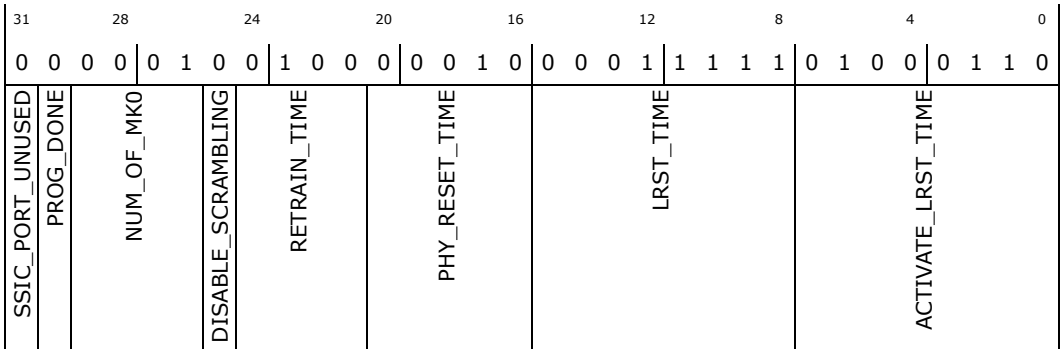
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 883Ch

Op Codes:

h - Read, h - Write

Default: 04821F46h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**SSIC_PORT_UNUSED:** This indicates that no SSIC device is connected to the port and PORTSC register would always reflect DISCONNECTED. **Power Well:** Core
30	0x0 RW	**PROG_DONE:** BIOS will program this bit once SSIC profile programming is done. SSIC will enable the MPHY and local PLL once this bit is set. **Power Well:** Core
29:26	0x1 RW	**NUM_OF_MK0:** Number of MK0 which transmitter will send before sending any data. **Power Well:** Core
25	0x0 RW	**DISABLE_SCRAMBLING:** This bit will disable scrambling in HS-BURST **Power Well:** Core
24:21	0x4 RW	**RETRAIN_TIME:** Corresponds to time in 10us to detect improper training of the local and remote M-RX as part of HS-BURST entry. SSIC Spec specific 40 to 50us **Power Well:** Core
20:16	0x2 RW	**PHY_RESET_TIME:** Corresponds to time in 100ns, PA will drive PHY RESET for MIPI PHY. **Power Well:** Core
15:8	0x1f RW	**LRST_TIME:** Corresponds to time in 100us PA will drive DIF-P for line reset. MIPI PHY specifies 3.1 ms Minimum. For speedup mode this time will be in steps of 5us. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x46 RW	**ACTIVATE_LRST_TIME:** (Corresponds to tResetDIFN) Specifies in step of 1ms period of time a DSP is required to drive a DIF-N prior to a LINE-RESET. SSIC spec defined range is 60-80ms. For speedup mode this time will be from 5us to 400us in steps of 5us. **Power Well:** Core

7.4.306 reg_SSIC_CONFIG_REG3_type (PORT2_SSIC_CONFIG_REG3)—Offset 8840h

Access Method

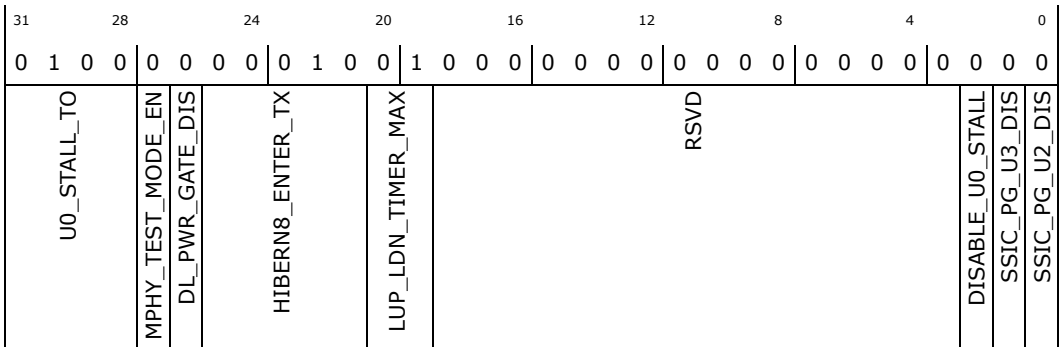
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8840h

Op Codes:

h - Read, h - Write

Default: 40480000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x4 RW	**U0_STALL_TO:** Time in 2^[U-STALL_TO] clock for U0 STALL entry. If there is no packet in arbiter for U0_STALL_TO time, PA will enable U0 STALL if DISABLE_U0_STALL is not set. 0000 0011 (Not recommended) 0100 16 SSIC HS CLK . 1111 32768 SSIC HS CLK **Power Well:** Core
27	0x0 RW	**MPHY_TEST_MODE_EN:** When this bit is set, controller would not initiate any PWM once it enters PWM Mode. It will wait for tester to send Loopback RRAP Command. **Power Well:** Core
26	0x0 RW	**DL_PWR_GATE_DIS:** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
25:21	0x2 RW	**HIBERN8_ENTER_TX:** The time PA will drive DIF-N after last bit of Line-CFG before entering H8. In steps of 50ns. Legal range is 50 to 1000ns. **Power Well:** Core
20:19	0x1 RW	**LUP_LDN_TIMER_MAX:** 00: 10 us 01: 100 us 10: 1000us /1ms 11: (Timer is disable and dont transmit LDN) **Power Well:** Core
18:3	0x0 RW	**RESERVED (RSVD):** rsvd **Power Well:** Core
2	0x0 RW	**DISABLE_U0_STALL:** This bit will disable the STALL entry in U0 **Power Well:** Core
1	0x0 RW	**SSIC_PG_U3_DIS:** This disables MPHY DL PG during U3. **Power Well:** Core
0	0x0 RW	**SSIC_PG_U2_DIS:** This disables MPHY DL PG during U2. **Power Well:** Core

7.4.307 reg_SSIC_CONFIG_REG4_type (PORT2_SSIC_CONFIG_REG4)—Offset 8844h

Access Method

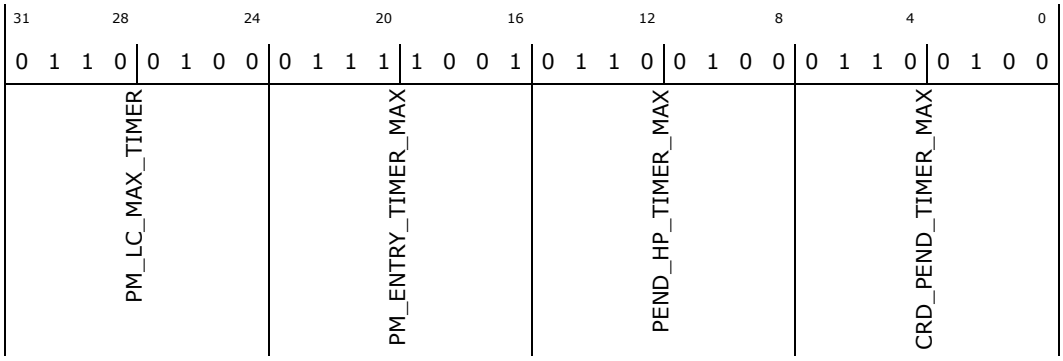
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8844h

Op Codes:

h - Read, h - Write

Default: 64796464h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x64 RW	**PM_LC_MAX_TIMER:** In steps of 1us. Default 100us **Power Well:** Core
23:16	0x79 RW	**PM_ENTRY_TIMER_MAX:** In steps of 1us. Default 100us **Power Well:** Core
15:8	0x64 RW	**PEND_HP_TIMER_MAX:** In steps of 1us. Default 100us **Power Well:** Core
7:0	0x64 RW	**CRD_PEND_TIMER_MAX:** In steps of 1us. Default 100us **Power Well:** Core

7.4.308 reg_SSIC_LOOPBACK_CONFIG_REG_type (PORT2_SSIC_LOOPBACK_CONFIG_REG)—Offset 8848h

Access Method

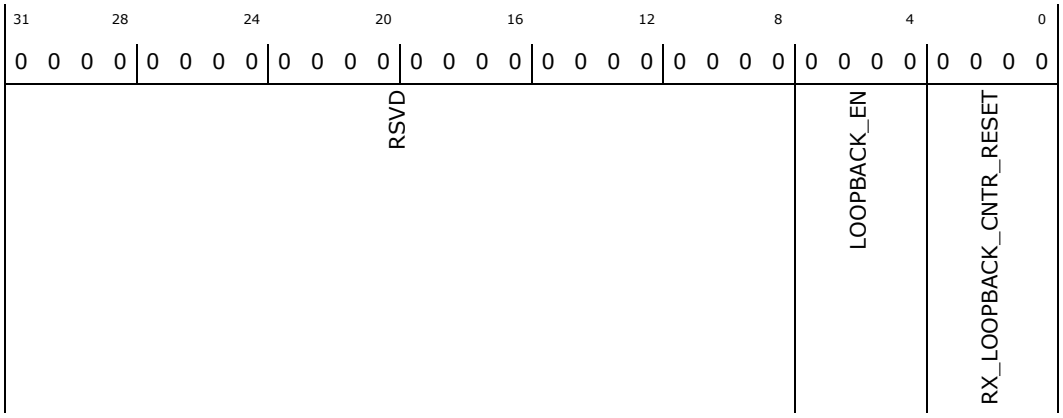
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8848h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RO	**LOOPBACK_EN:** This Register is used to enable Conformance Loopback in the Target in the specified PAIR.. Bit [0]: Writing 1b1 enables the loopback mode in PAIR0. Writing 1b0 shall have no effect. Bit [1]: Writing 1b1 enables the loopback mode in PAIR1. Writing 1b0 shall have no effect. Bit [2]: Writing 1b1 enables the loopback mode in PAIR2. Writing 1b0 shall have no effect. Bit [3]: Writing 1b1 enables the loopback mode in PAIR3. Writing 1b0 shall have no effect. **Power Well:** Core
3:0	0x0 RO	**RX LOOPBACK CNTR RESET (RX_LOOPBACK_CNTR_RESET):** Reset RX_BURST_COUNT and RX_ERR_COUNT, write only, self-clearing. Bit [0] for PAIR0 Bit [1] for PAIR1 Bit [2] for PAIR2 Bit [3] for PAIR3 **Power Well:** Core

7.4.309 reg_SSIC_LOOPBACK_BURST_COUNT_REG_type (PORT2_SSIC_LOOPBACK_BURST_COUNT_REG)—Offset 884Ch

Access Method

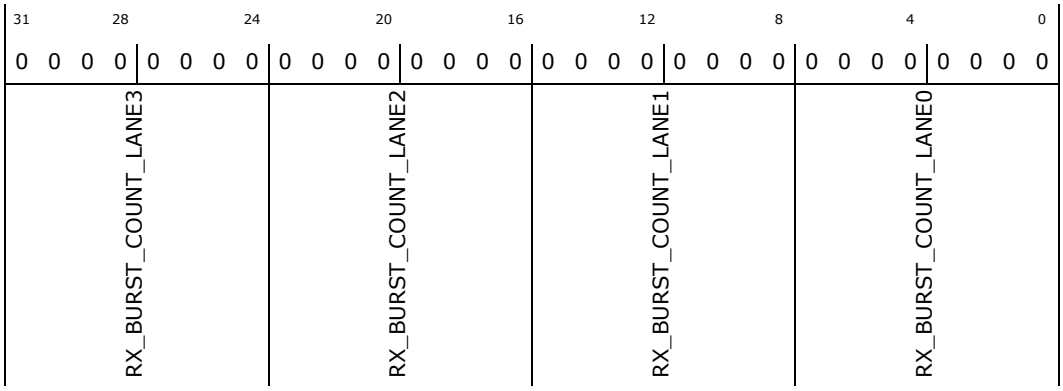
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 884Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RX_BURST_COUNT_LANE3:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
23:16	0x0 RO	**RX_BURST_COUNT_LANE2:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
15:8	0x0 RO	**RX_BURST_COUNT_LANE1:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
7:0	0x0 RO	**RX_BURST_COUNT_LANE0:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core

7.4.310 reg_SSIC_LOOPBACK_ERROR_COUNT_REG_type (PORT2_SSIC_LOOPBACK_ERROR_COUNT_REG)—Offset 8850h

Access Method

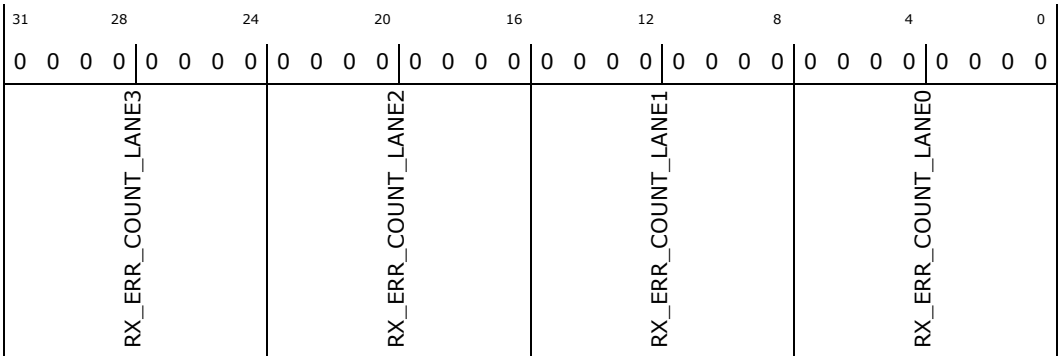
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8850h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RX_ERR_COUNT_LANE3:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
23:16	0x0 RO	**RX_ERR_COUNT_LANE2:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
15:8	0x0 RO	**RX_ERR_COUNT_LANE1:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core
7:0	0x0 RO	**RX_ERR_COUNT_LANE0:** RX_BURST_COUNT shall increment each time the M-RX of the PAIR under test detects a prepare time DIF-P. This shall be reset when the DUT receives a Write Command with rx_count_reset set to one. These counters shall not be reset when the DUT receives a LINE-RESET. **Power Well:** Core

7.4.311 SSIC Local and Remote Profile Registers Capability ID register (SSIC_PROFILE_CAPABILITY_ID_REG)—Offset 8900h

Access Method

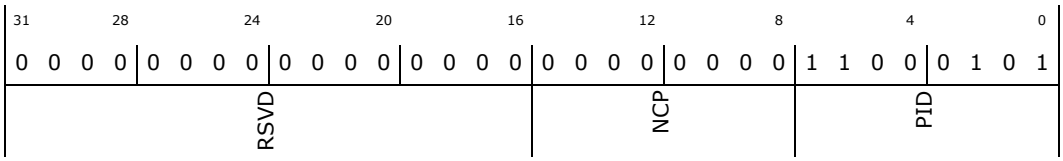
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8900h

Op Codes:

h - Read, h - Write

Default: 000000C5h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RW/S	**Next Capability Pointer (NCP):** Reserved. **Power Well:** Core
7:0	0xc5 RW/S	**Supported Protocol ID (PID):** Reserved. **Power Well:** Core

7.4.312 SSIC Port N Register Access Control (PORT1_REGISTER_ACCESS_CONTROL)—Offset 8904h

Access Method

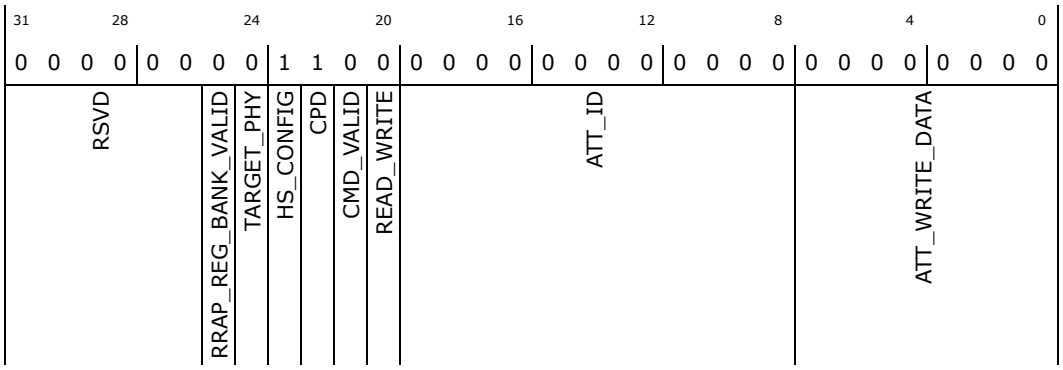
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8904h

Op Codes:

h - Read, h - Write

Default: 00C00000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
25	0x0 RW	**RRAP Register Bank Valid (RRAP_REG_BANK_VALID):** 0 = No valid Commands in the Lane N register bank. Host Controller can close the PWM burst once commands from this register are completed. 1 = Valid commands present in the Lane N register bank. Host controller must complete commands from the register bank before closing the burst. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
24	0x0 RW	**Target Phy (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy Setting this bit to 1 allows the use of this command mechanism to write to local Phy profile and AFE tuning registers Primarily as a back up option. **Power Well:** Core
23	0x1 RW	**HS_Config (HS_CONFIG):** When this bit is set to 1 the host controller will issue an RRAP write with HS_Config=1 once it sees Command Phase Done = 1 **Power Well:** Core
22	0x1 RW	**Command Phase Done (CPD):** When set to 1, this indicates that SW has completed performing RRAP cycles through the command register. **Power Well:** Core
21	0x0 RW	**Command Valid (CMD_VALID):** When written to 1 indicates that the Attribute ID and Attribute Data for writes fields are valid. **Power Well:** Core
20	0x0 RW	**Read_Write (READ_WRITE):** 0 = Write 1= Read **Power Well:** Core
19:8	0x0 RW	**Attribute ID (ATT_ID):** Attribute ID that is being written or read **Power Well:** Core
7:0	0x0 RW	**Attribute Write Data (ATT_WRITE_DATA):** Data byte that is required to be written to either the local phy or the remote phy **Power Well:** Core

7.4.313 SSIC Port N Register Access Status (PORT1_REGISTER_ACCESS_STATUS)—Offset 8908h

Access Method

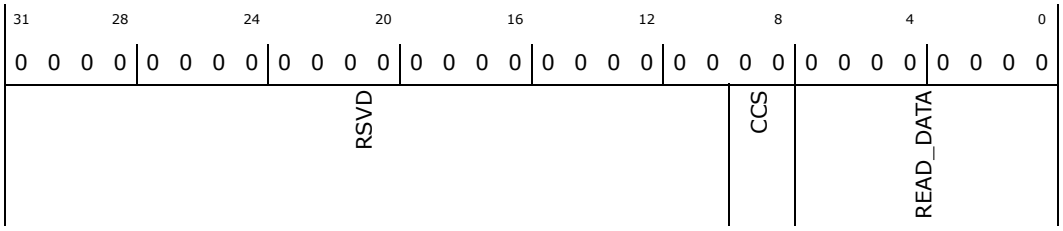
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8908h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
9:8	0x0 RW	**Command Completion Status (CCS):** 00 = Command not complete 01 = Command complete with Success 10 = Command complete with Error These bits must be cleared before a new command is initiated. **Power Well:** Core
7:0	0x0 RO	**Read data (READ_DATA):** Data read as a result of the RRAP operation **Power Well:** Core

7.4.314 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG0)—Offset 890Ch

Access Method

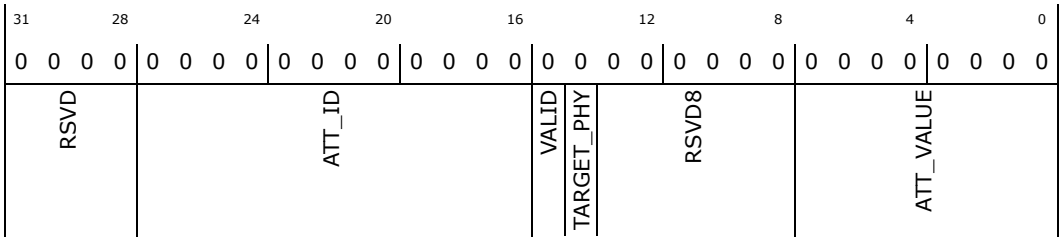
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 890Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.315 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG1)—Offset 8910h

Access Method

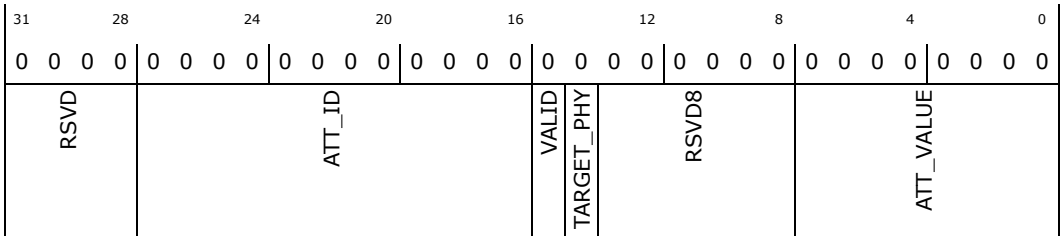
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8910h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.316 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG2)—Offset 8914h

Access Method

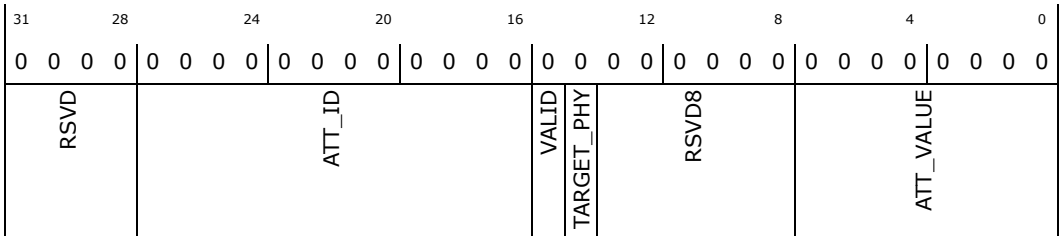
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8914h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.317 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG3)—Offset 8918h

Access Method

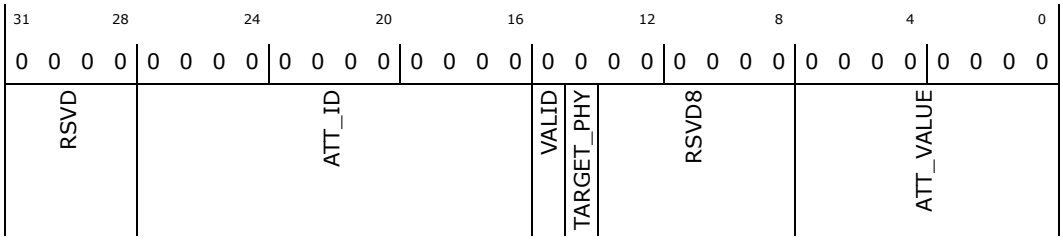
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8918h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.318 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG4)—Offset 891Ch

Access Method

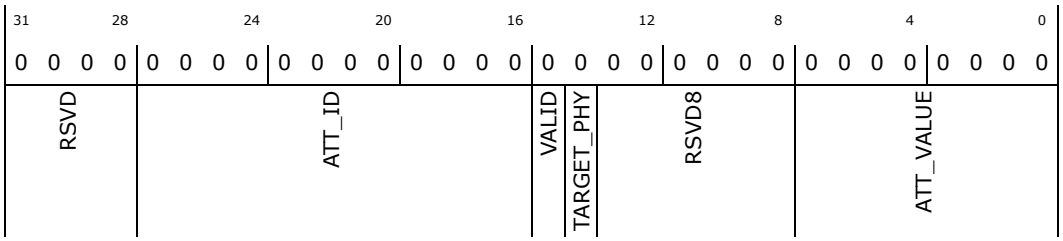
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 891Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.319 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG5)—Offset 8920h

Access Method

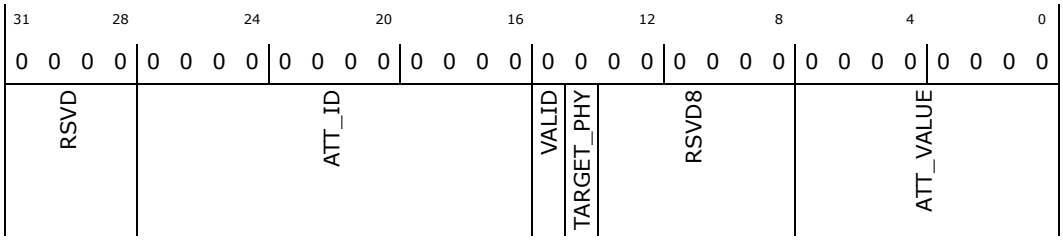
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8920h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.320 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG6)—Offset 8924h

Access Method

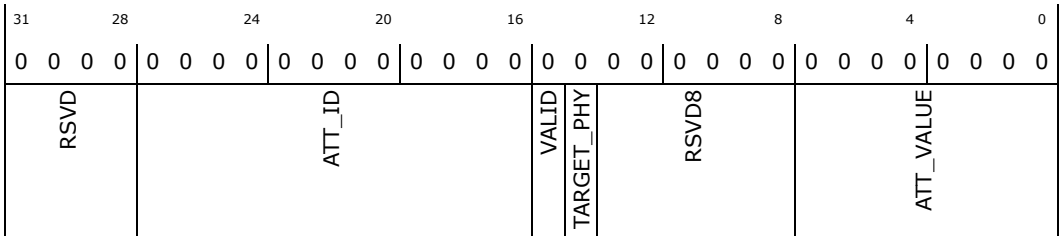
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8924h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.321 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG7)—Offset 8928h

Access Method

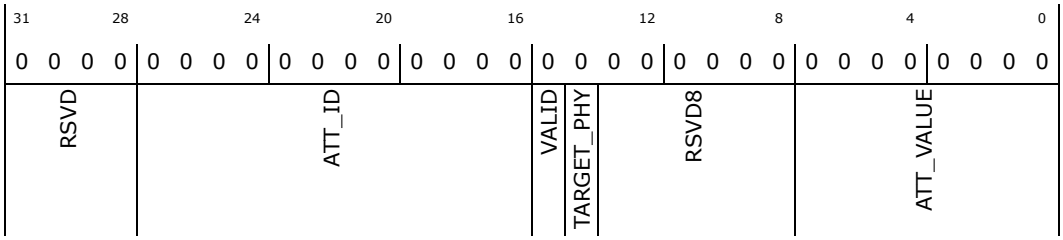
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8928h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.322 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG8)—Offset 892Ch

Access Method

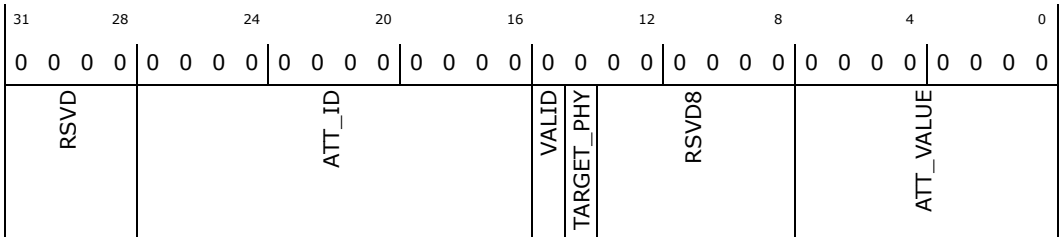
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 892Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.323 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG9)—Offset 8930h

Access Method

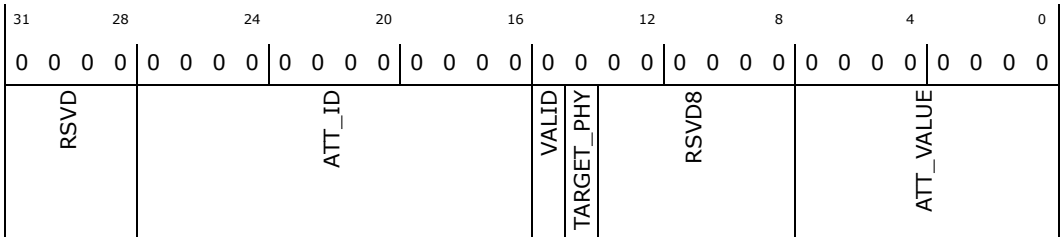
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8930h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.324 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG10)—Offset 8934h

Access Method

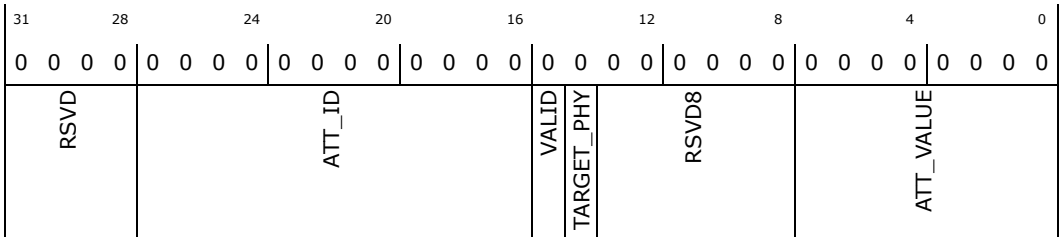
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8934h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.325 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG11)—Offset 8938h

Access Method

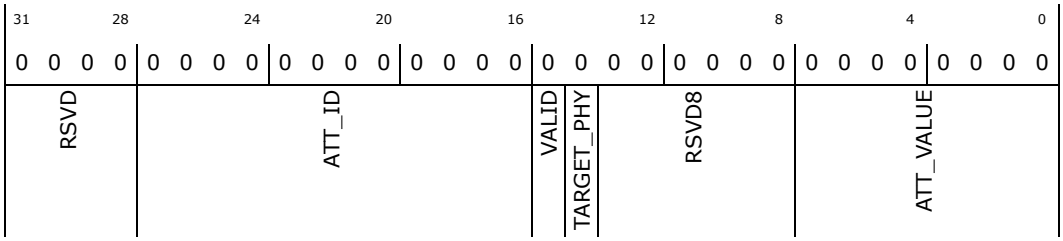
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8938h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.326 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG12)—Offset 893Ch

Access Method

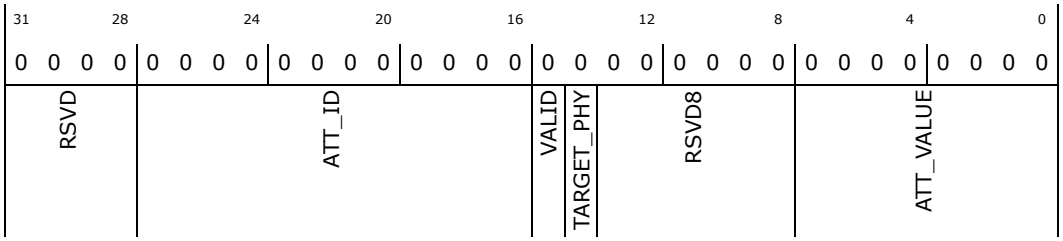
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 893Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.327 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG13)—Offset 8940h

Access Method

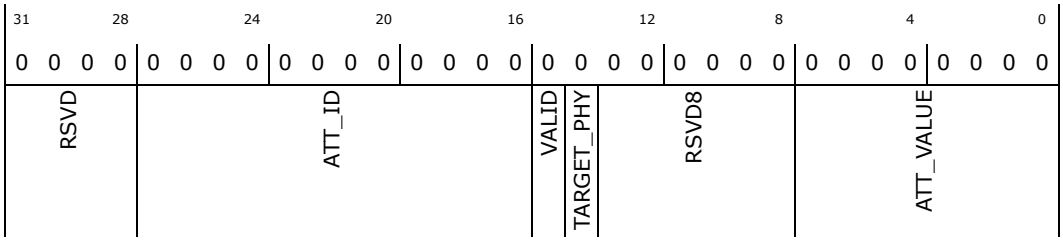
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8940h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.328 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG14)—Offset 8944h

Access Method

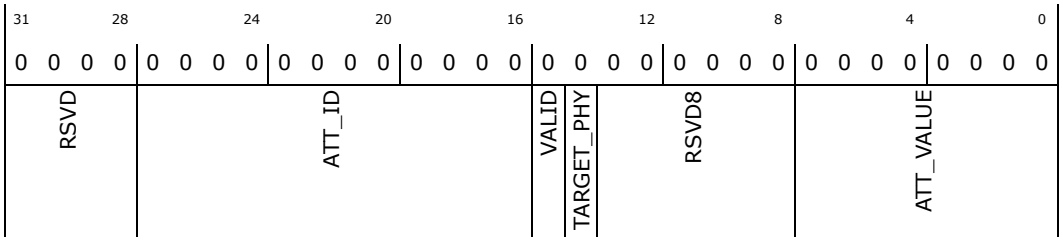
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8944h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.329 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG15)—Offset 8948h

Access Method

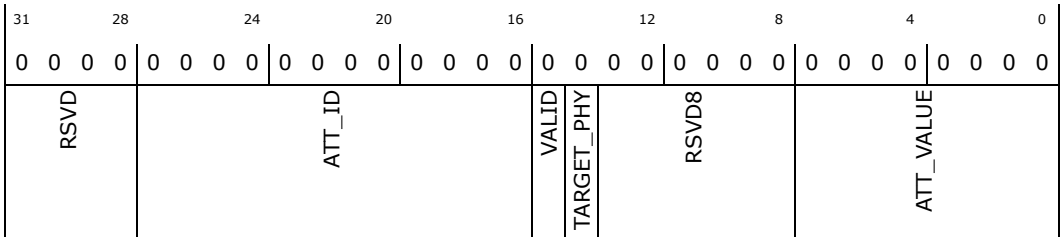
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8948h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.330 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG16)—Offset 894Ch

Access Method

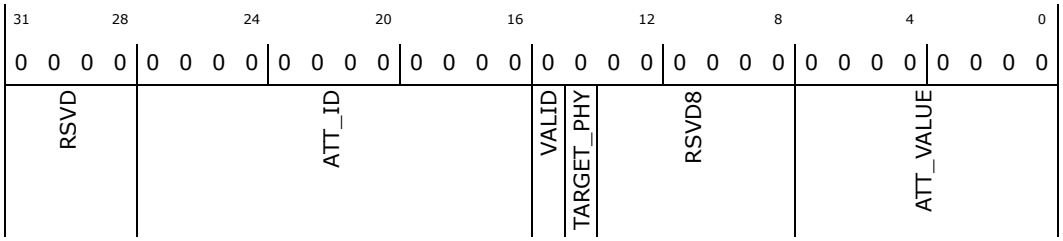
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 894Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.331 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG17)—Offset 8950h

Access Method

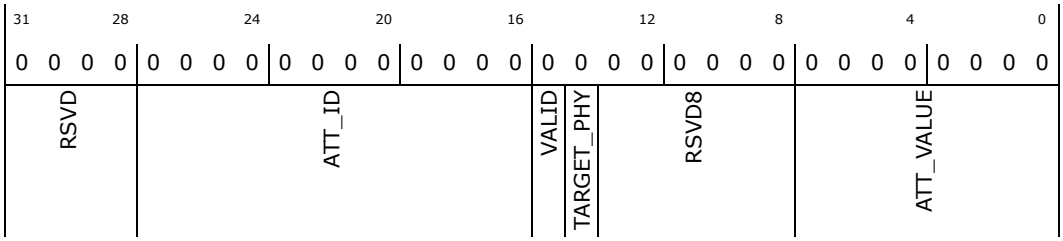
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8950h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.332 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG18)—Offset 8954h

Access Method

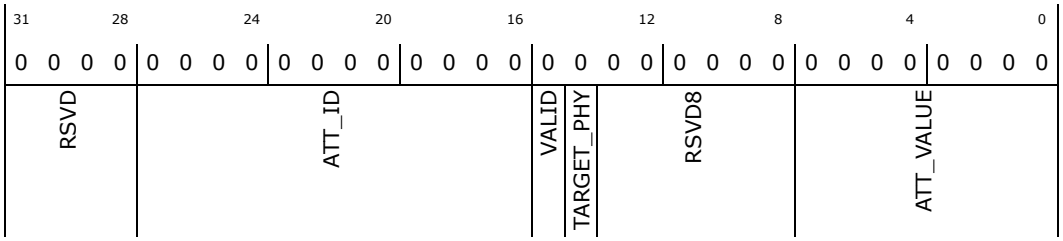
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8954h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.333 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG19)—Offset 8958h

Access Method

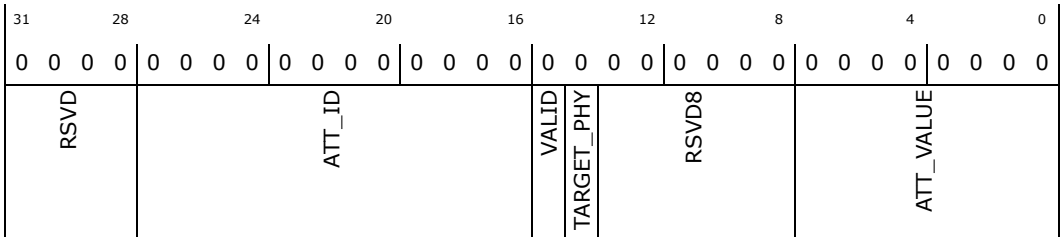
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8958h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.334 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG20)—Offset 895Ch

Access Method

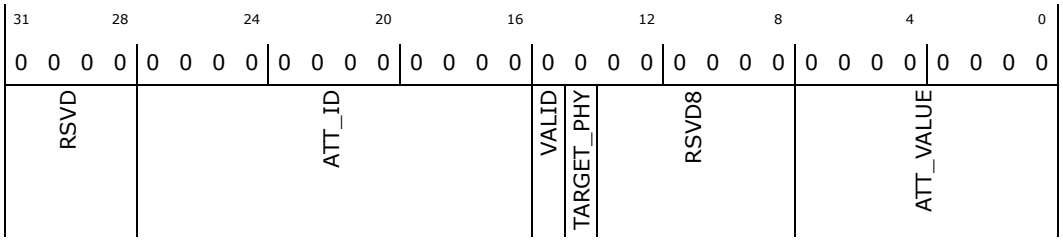
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 895Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.335 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG21)—Offset 8960h

Access Method

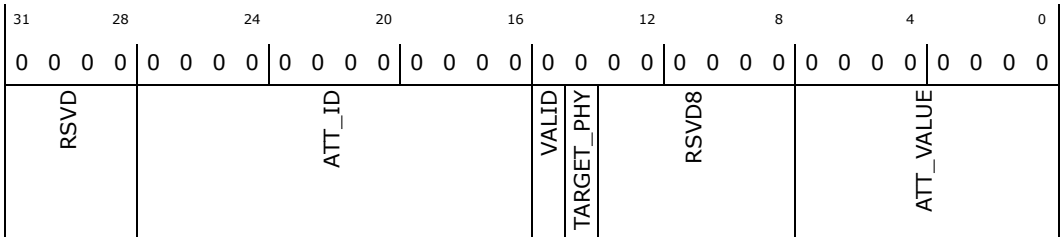
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8960h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.336 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG22)—Offset 8964h

Access Method

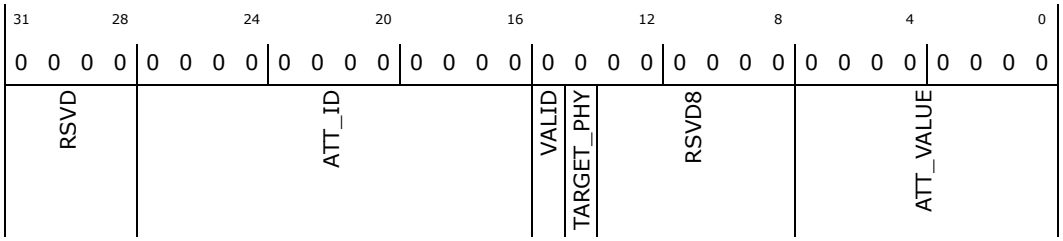
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8964h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.337 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG23)—Offset 8968h

Access Method

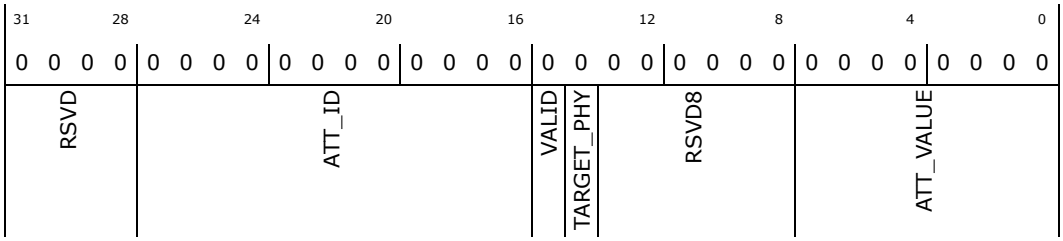
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8968h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.338 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG24)—Offset 896Ch

Access Method

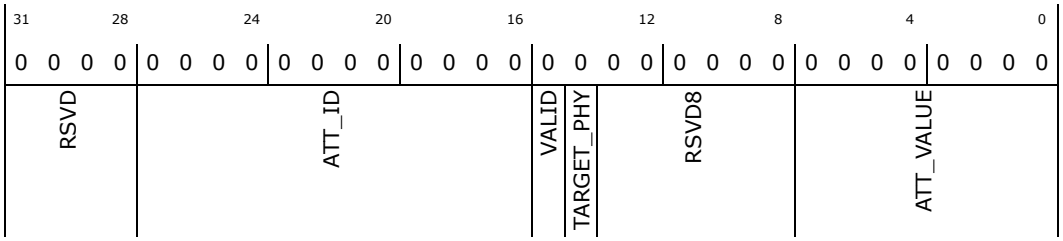
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 896Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.339 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG25)—Offset 8970h

Access Method

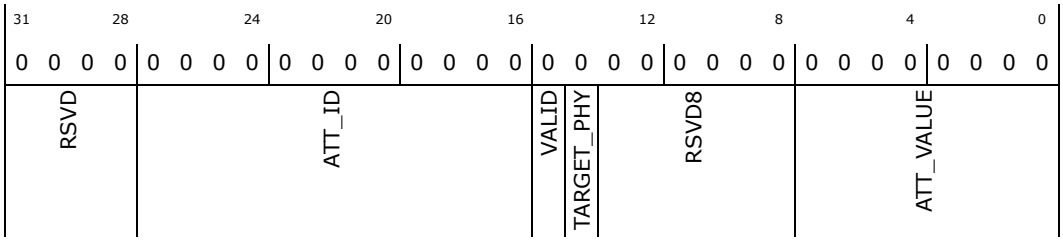
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8970h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.340 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG26)—Offset 8974h

Access Method

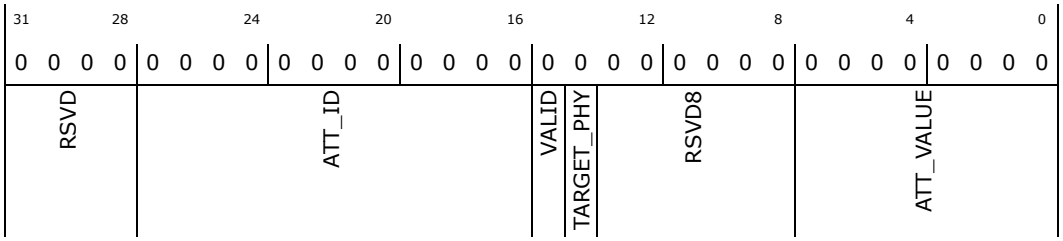
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8974h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.341 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG27)—Offset 8978h

Access Method

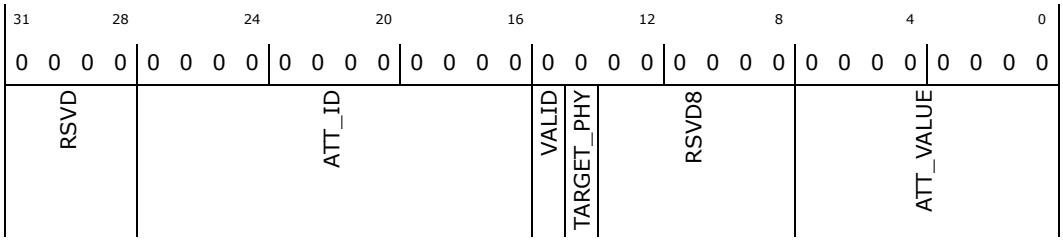
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8978h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.342 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG28)—Offset 897Ch

Access Method

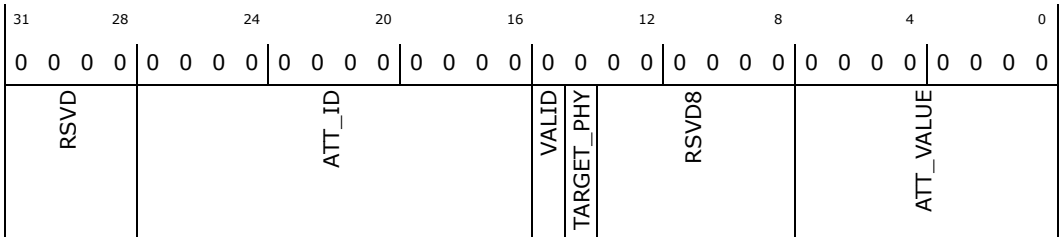
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 897Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.343 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG29)—Offset 8980h

Access Method

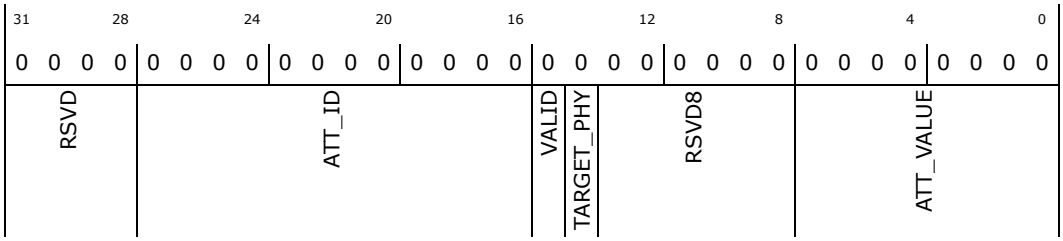
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8980h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.344 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG30)—Offset 8984h

Access Method

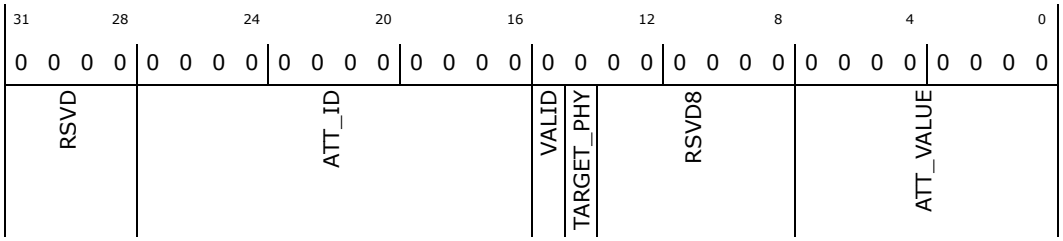
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8984h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.345 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG31)—Offset 8988h

Access Method

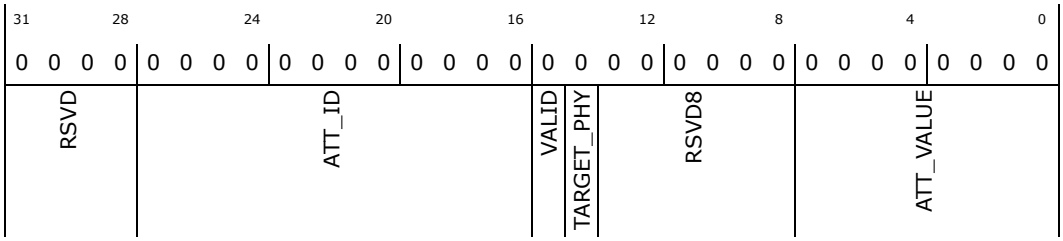
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8988h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.346 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG32)—Offset 898Ch

Access Method

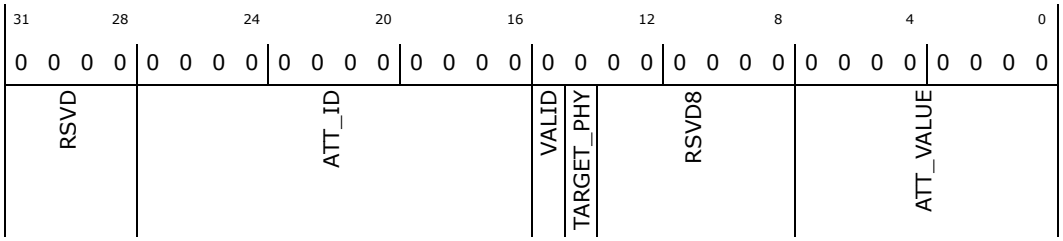
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 898Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.347 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG33)—Offset 8990h

Access Method

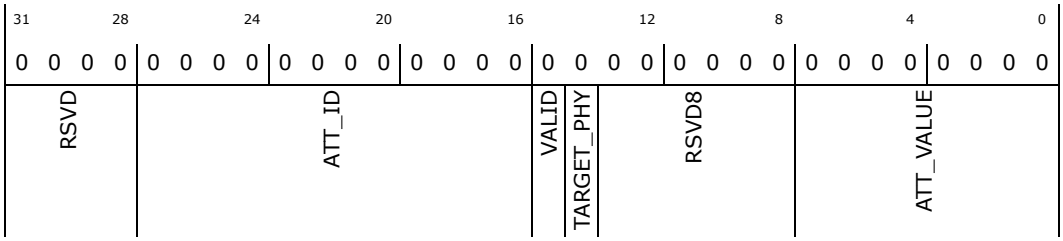
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8990h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.348 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG34)—Offset 8994h

Access Method

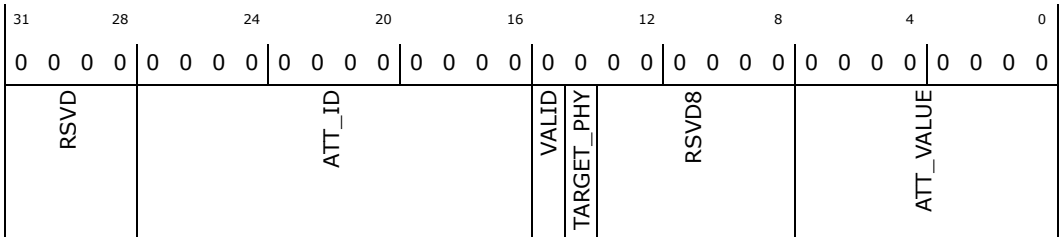
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8994h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.349 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG35)—Offset 8998h

Access Method

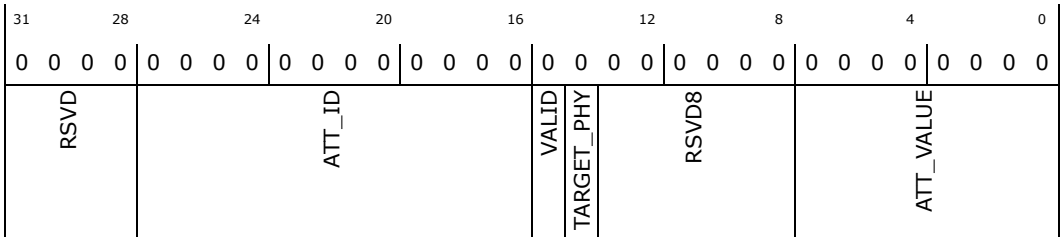
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8998h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.350 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG36)—Offset 899Ch

Access Method

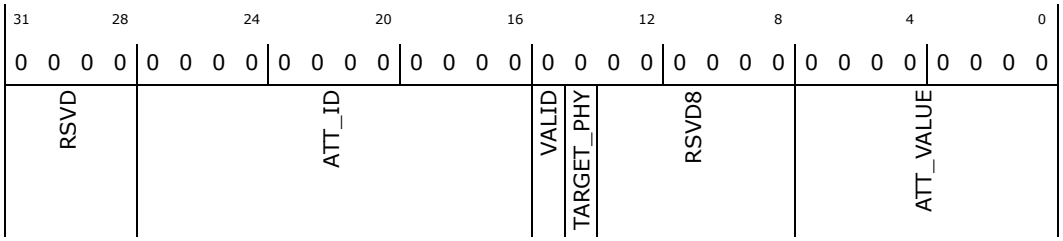
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 899Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.351 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG37)—Offset 89A0h

Access Method

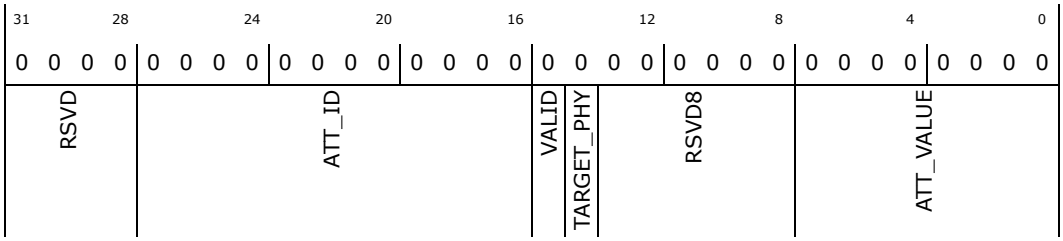
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89A0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.352 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG38)—Offset 89A4h

Access Method

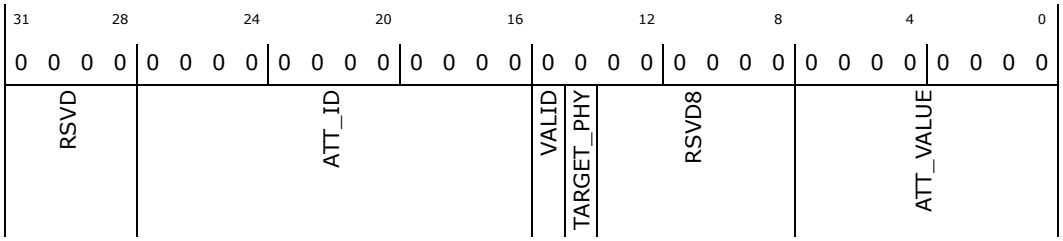
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89A4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.353 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG39)—Offset 89A8h

Access Method

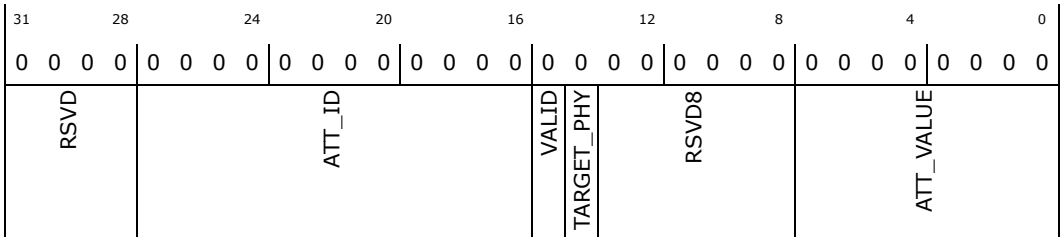
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89A8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.354 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG40)—Offset 89ACh

Access Method

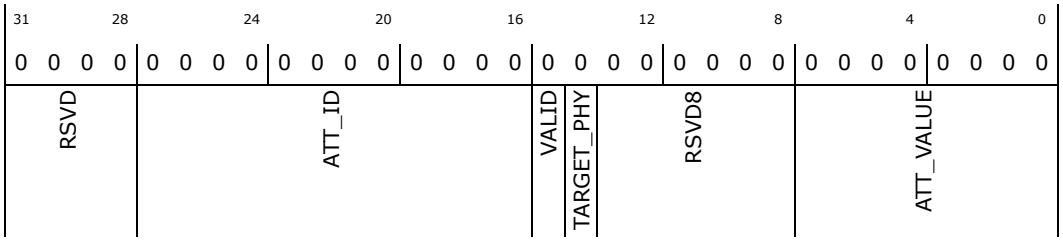
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89ACh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.355 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG41)—Offset 89B0h

Access Method

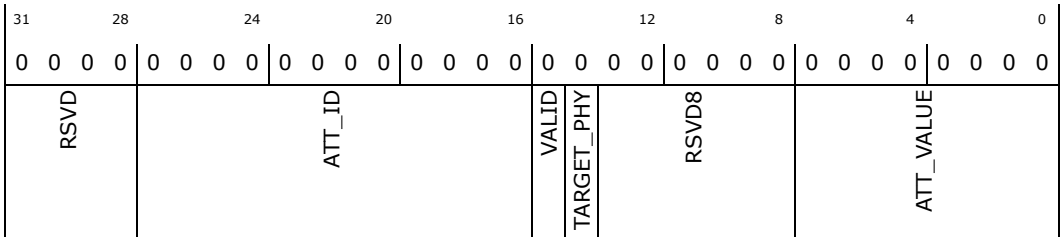
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89B0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.356 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG42)—Offset 89B4h

Access Method

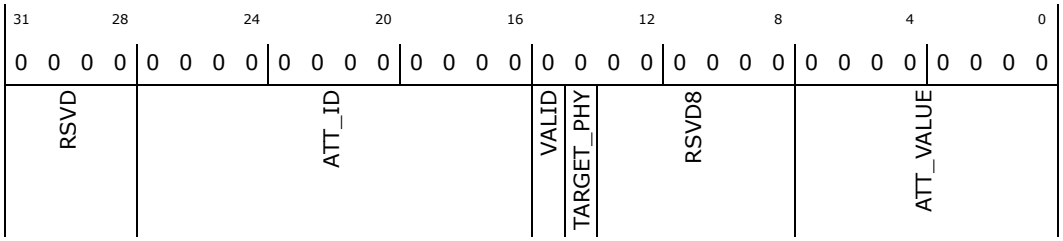
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89B4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.357 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG43)—Offset 89B8h

Access Method

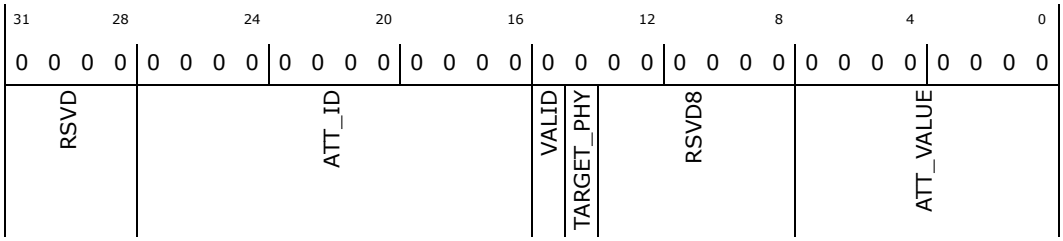
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89B8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.358 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG44)—Offset 89BCh

Access Method

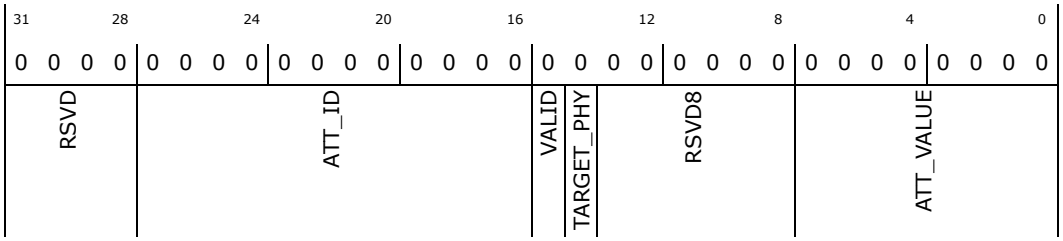
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89BCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.359 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG45)—Offset 89C0h

Access Method

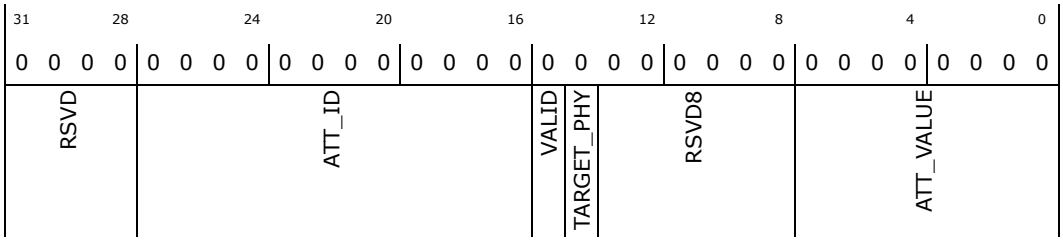
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89C0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.360 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG46)—Offset 89C4h

Access Method

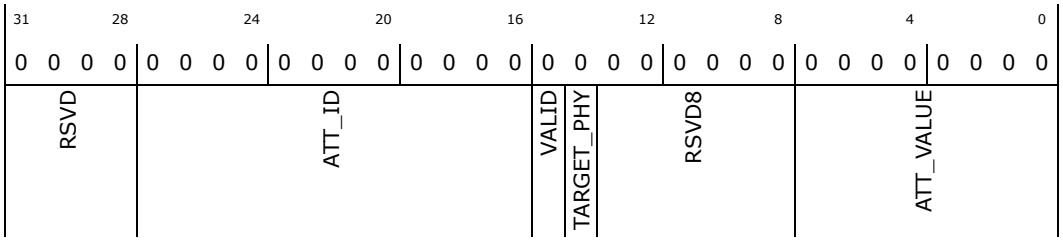
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89C4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.361 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG47)—Offset 89C8h

Access Method

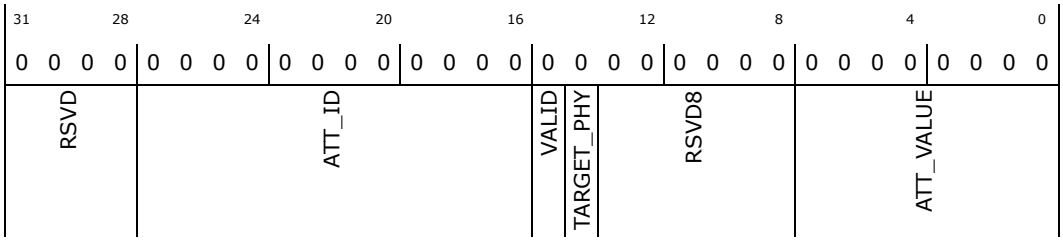
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89C8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.362 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG48)—Offset 89CCh

Access Method

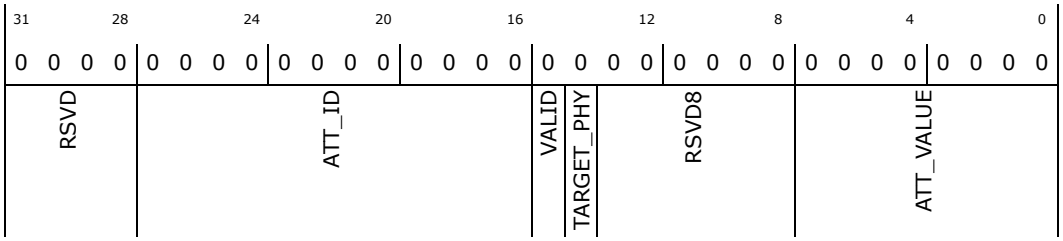
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89CCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.363 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG49)—Offset 89D0h

Access Method

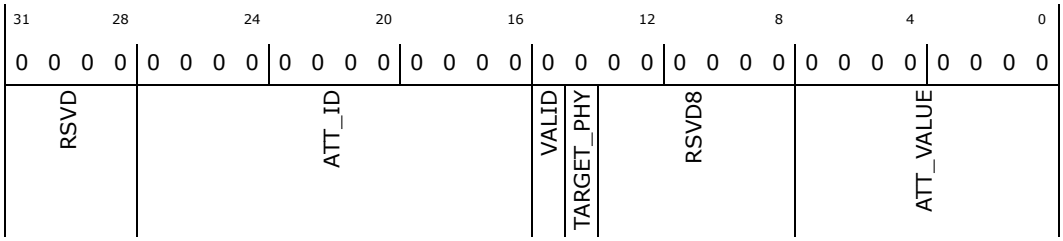
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89D0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.364 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG50)—Offset 89D4h

Access Method

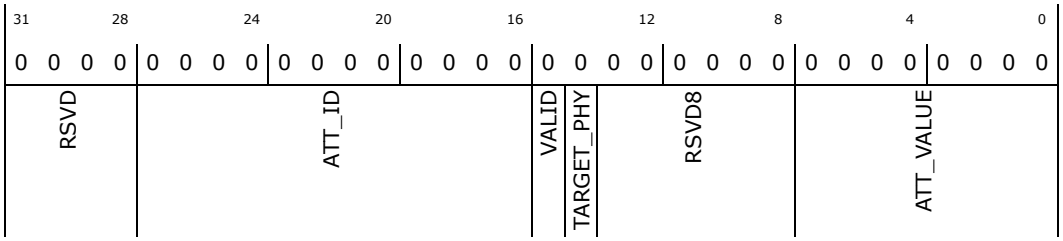
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89D4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.365 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG51)—Offset 89D8h

Access Method

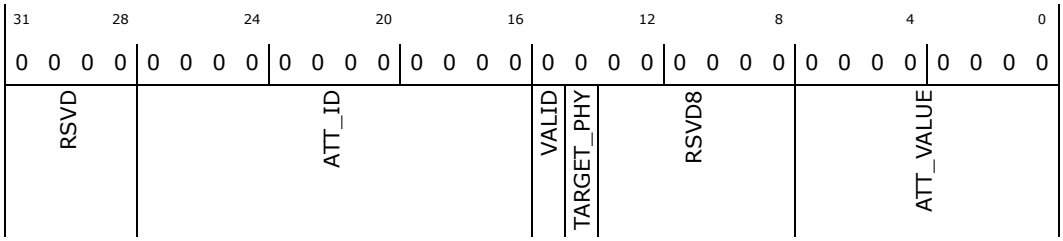
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89D8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.366 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG52)—Offset 89DCh

Access Method

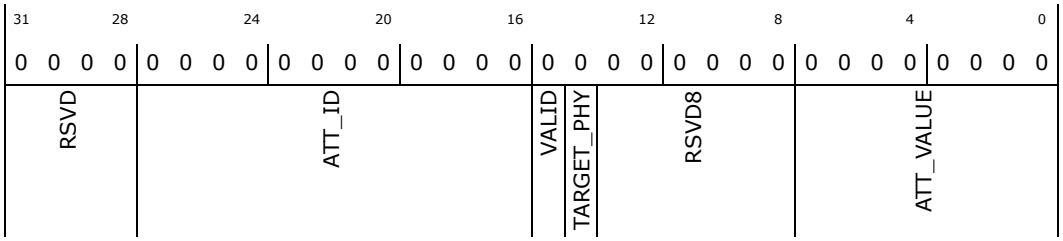
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89DCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.367 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG53)—Offset 89E0h

Access Method

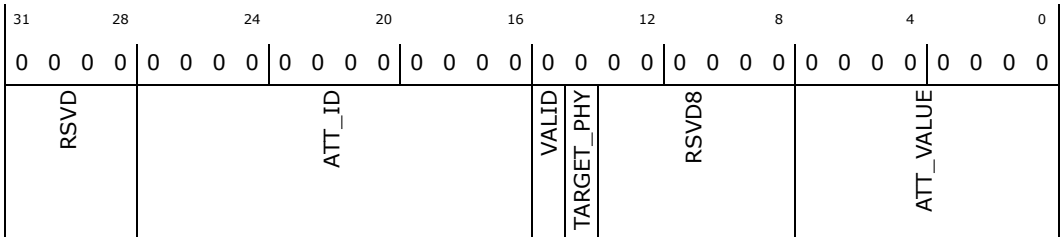
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89E0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.368 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG54)—Offset 89E4h

Access Method

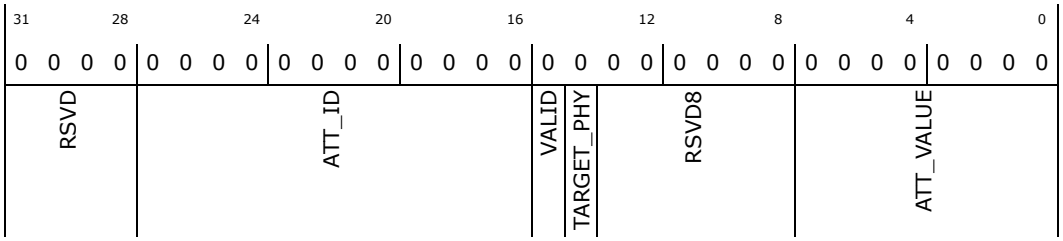
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89E4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.369 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG55)—Offset 89E8h

Access Method

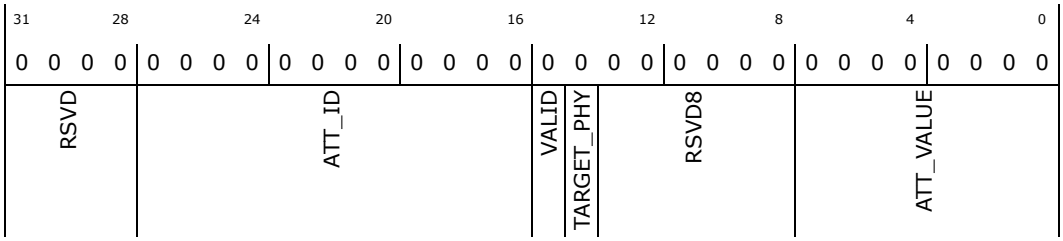
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89E8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.370 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG56)—Offset 89ECh

Access Method

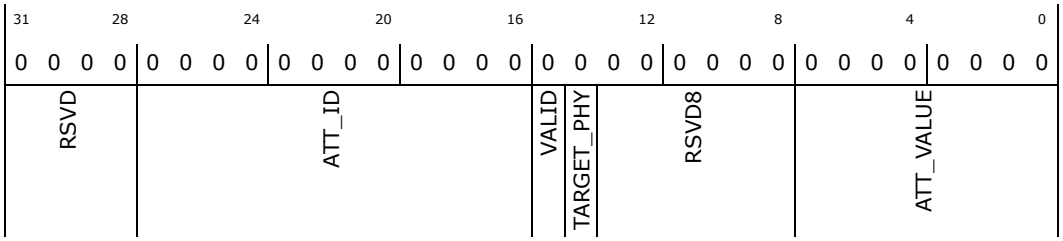
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89ECh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.371 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG57)—Offset 89F0h

Access Method

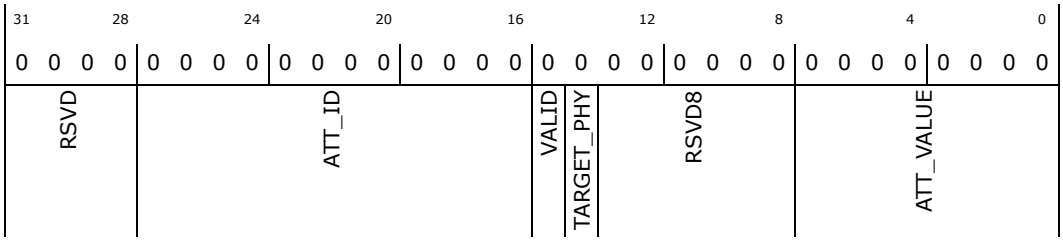
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89F0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.372 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG58)—Offset 89F4h

Access Method

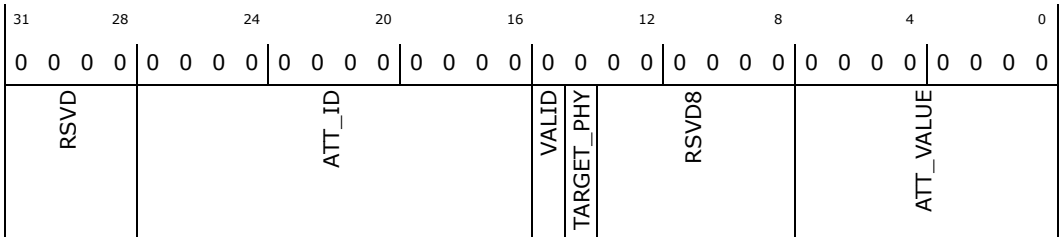
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89F4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.373 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG59)—Offset 89F8h

Access Method

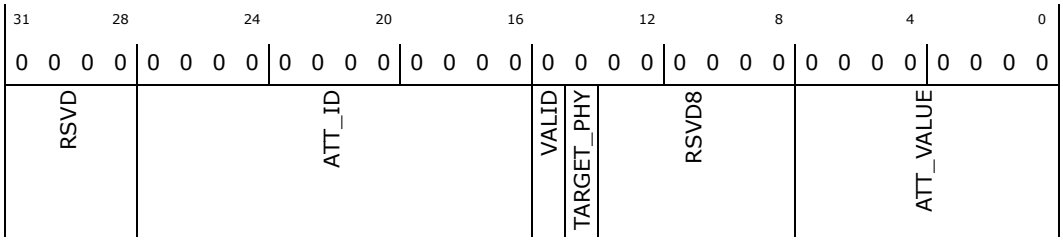
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89F8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.374 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG60)—Offset 89FCh

Access Method

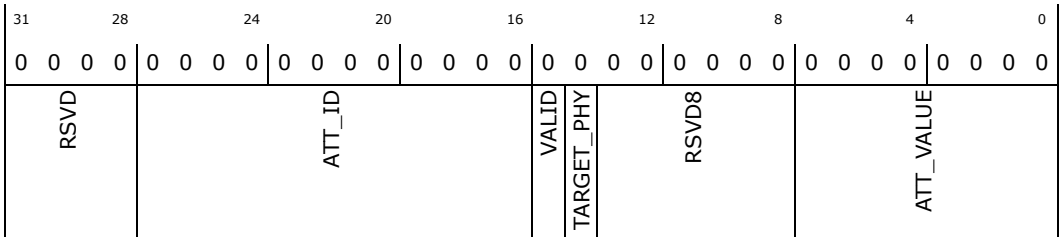
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 89FCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.375 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG61)—Offset 8A00h

Access Method

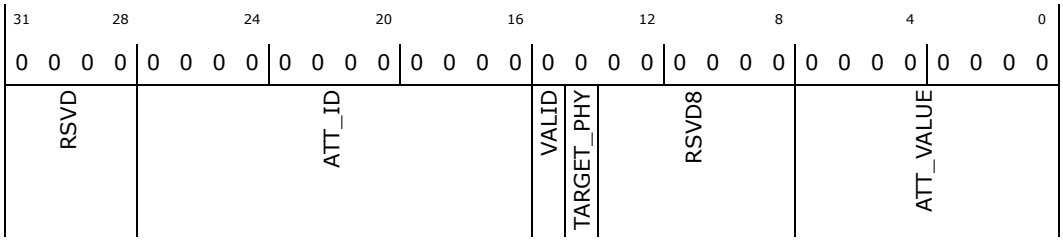
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A00h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.376 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG62)—Offset 8A04h

Access Method

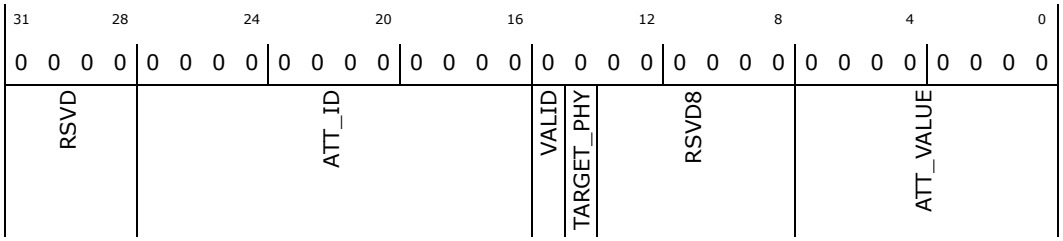
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A04h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.377 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT1_PROFILE_ATTRIBUTES_REG63)—Offset 8A08h

Access Method

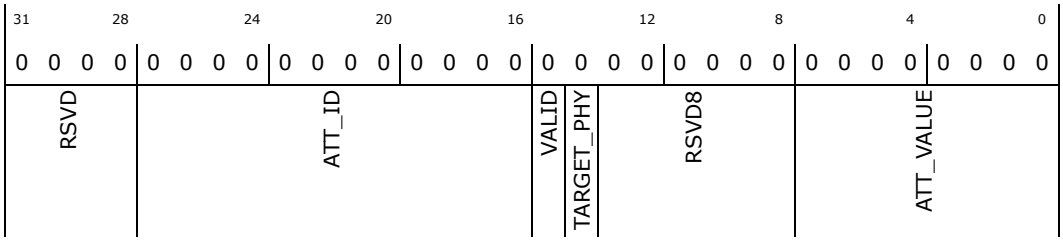
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A08h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.378 SSIC Port N Register Access Control (PORT2_REGISTER_ACCESS_CONTROL)—Offset 8A14h

Access Method

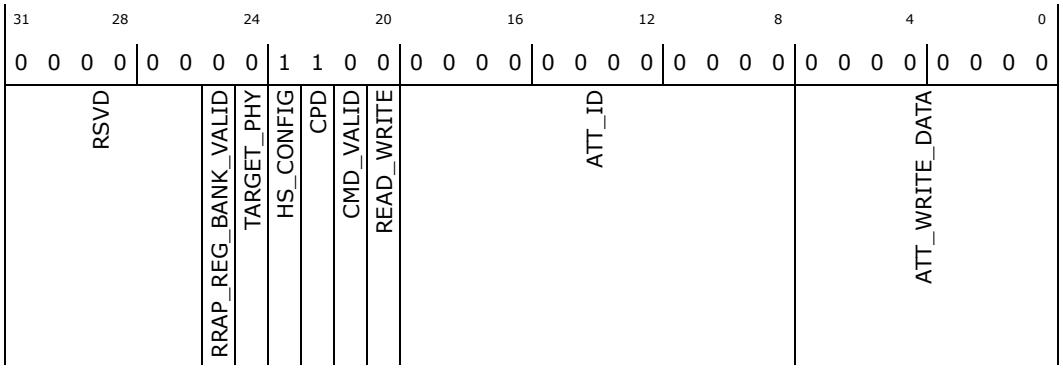
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A14h

Op Codes:

h - Read, h - Write

Default: 00C00000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
25	0x0 RW	**RRAP Register Bank Valid (RRAP_REG_BANK_VALID):** 0 = No valid Commands in the Lane N register bank. Host Controller can close the PWM burst once commands from this register are completed. 1 = Valid commands present in the Lane N register bank. Host controller must complete commands from the register bank before closing the burst. **Power Well:** Core
24	0x0 RW	**Target Phy (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy Setting this bit to 1 allows the use of this command mechanism to write to local Phy profile and AFE tuning registers Primarily as a back up option. **Power Well:** Core
23	0x1 RW	**HS_Config (HS_CONFIG):** When this bit is set to 1 the host controller will issue an RRAP write with HS_Config=1 once it sees Command Phase Done = 1 **Power Well:** Core
22	0x1 RW	**Command Phase Done (CPD):** When set to 1, this indicates that SW has completed performing RRAP cycles through the command register. **Power Well:** Core
21	0x0 RW	**Command Valid (CMD_VALID):** When written to 1 indicates that the Attribute ID and Attribute Data for writes fields are valid. **Power Well:** Core
20	0x0 RW	**Read_Write (READ_WRITE):** 0 = Write 1= Read **Power Well:** Core
19:8	0x0 RW	**Attribute ID (ATT_ID):** Attribute ID that is being written or read **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**Attribute Write Data (ATT_WRITE_DATA):** Data byte that is required to be written to either the local phy or the remote phy **Power Well:** Core

7.4.379 SSIC Port N Register Access Status (PORT2_REGISTER_ACCESS_STATUS)—Offset 8A18h

Access Method

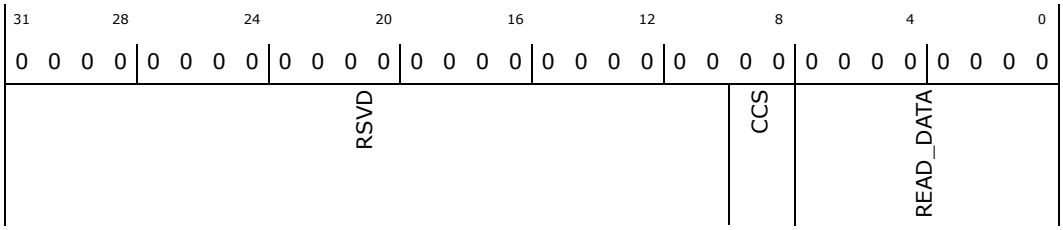
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A18h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
9:8	0x0 RW	**Command Completion Status (CCS):** 00 = Command not complete 01 = Command complete with Success 10 = Command complete with Error These bits must be cleared before a new command is initiated. **Power Well:** Core
7:0	0x0 RO	**Read data (READ_DATA):** Data read as a result of the RRAP operation **Power Well:** Core

7.4.380 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG0)—Offset 8A1Ch

Access Method

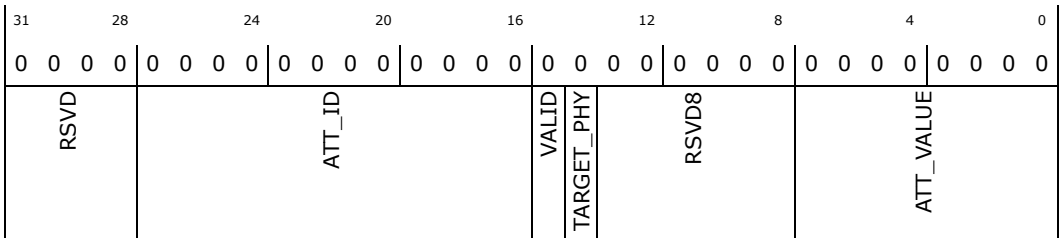
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A1Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.381 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG1)—Offset 8A20h

Access Method

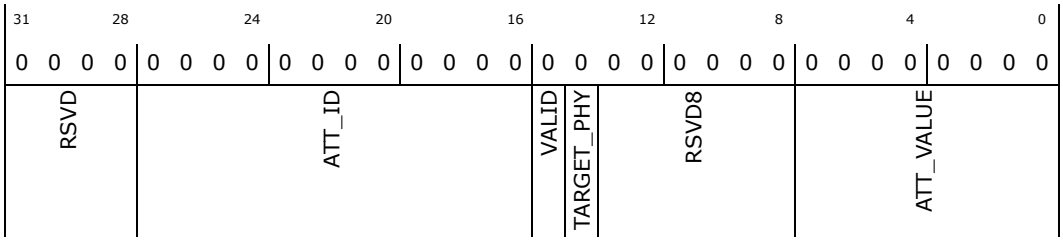
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A20h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.382 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG2)—Offset 8A24h

Access Method

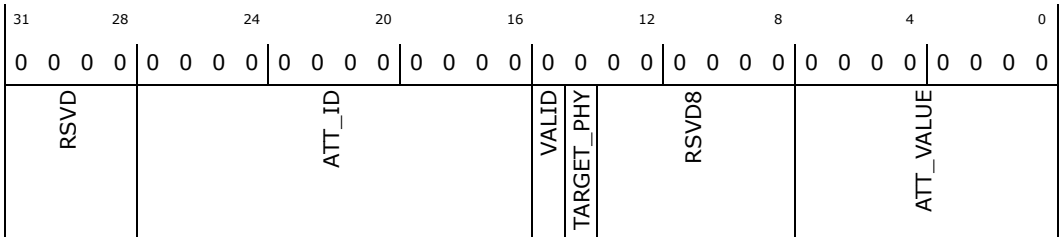
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A24h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.383 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG3)—Offset 8A28h

Access Method

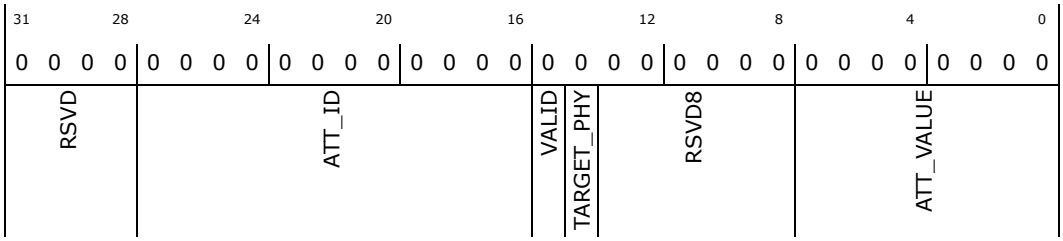
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A28h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.384 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG4)—Offset 8A2Ch

Access Method

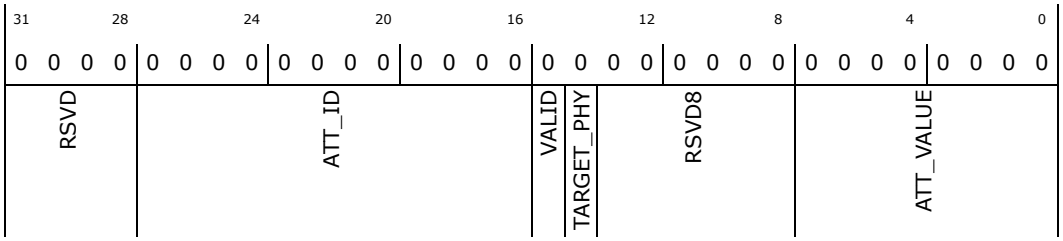
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A2Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.385 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG5)—Offset 8A30h

Access Method

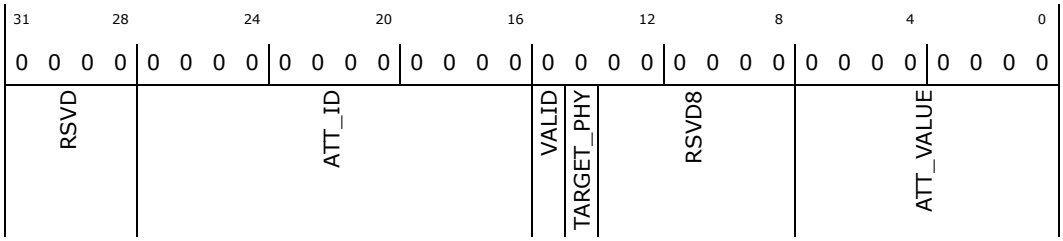
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A30h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.386 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG6)—Offset 8A34h

Access Method

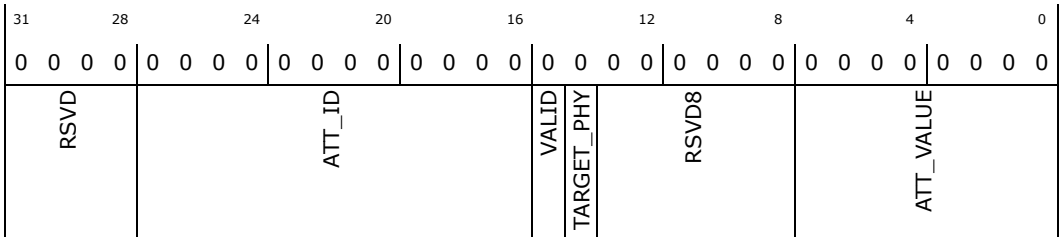
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A34h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.387 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG7)—Offset 8A38h

Access Method

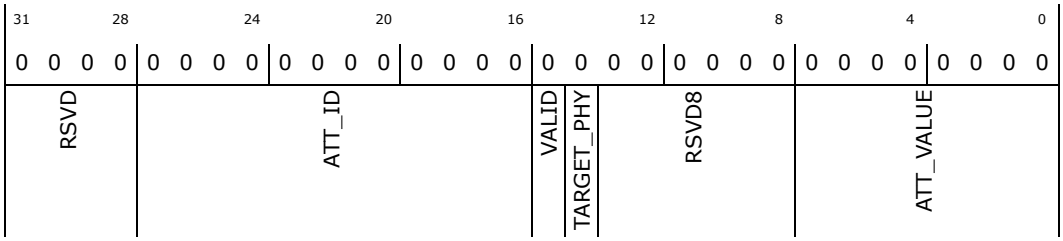
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A38h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.388 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG8)—Offset 8A3Ch

Access Method

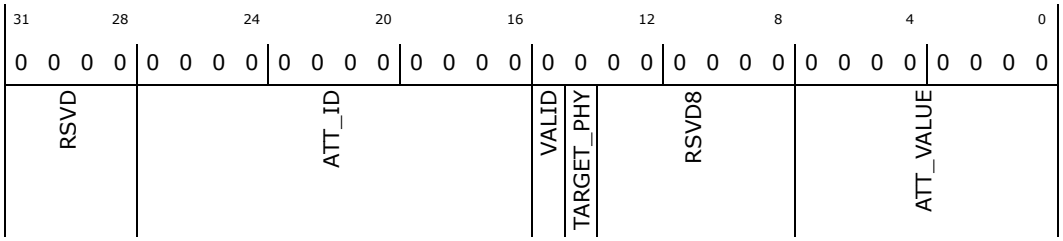
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A3Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.389 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG9)—Offset 8A40h

Access Method

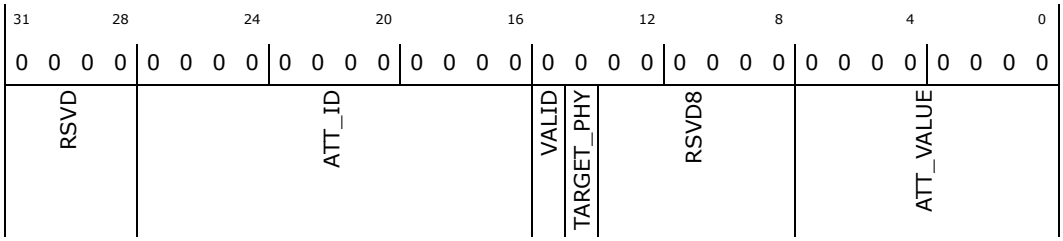
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A40h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.390 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG10)—Offset 8A44h

Access Method

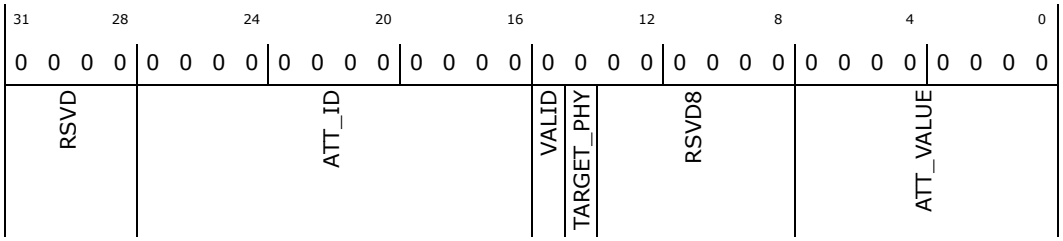
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A44h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.391 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG11)—Offset 8A48h

Access Method

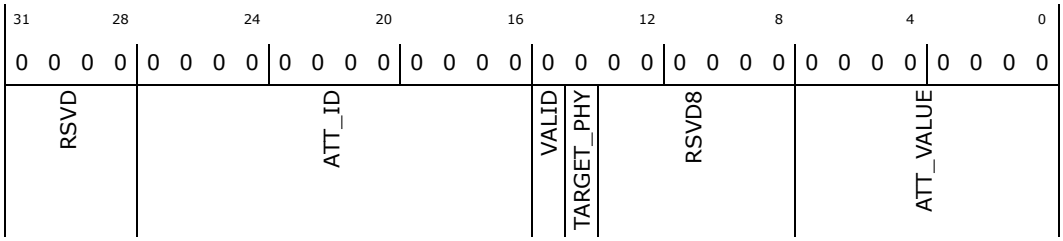
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A48h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.392 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG12)—Offset 8A4Ch

Access Method

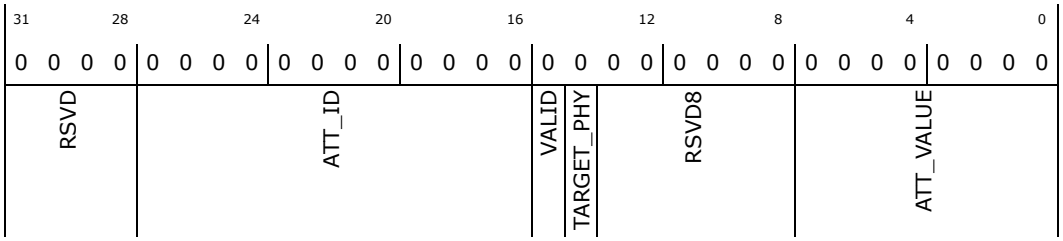
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A4Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.393 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG13)—Offset 8A50h

Access Method

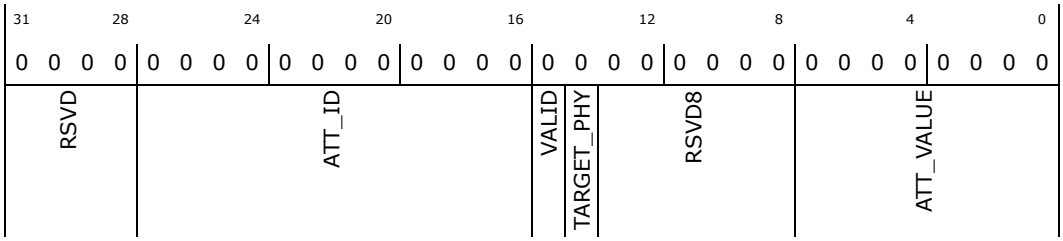
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A50h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.394 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG14)—Offset 8A54h

Access Method

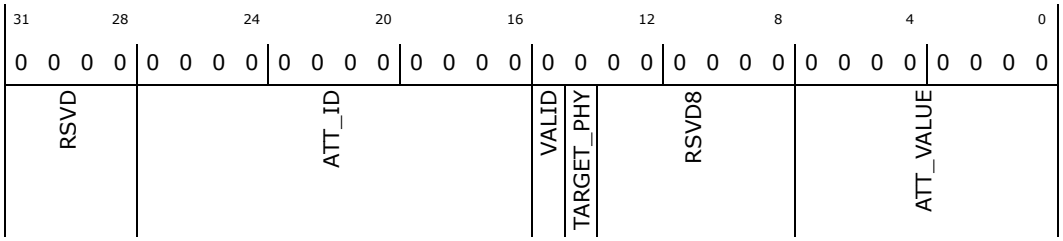
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A54h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.395 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG15)—Offset 8A58h

Access Method

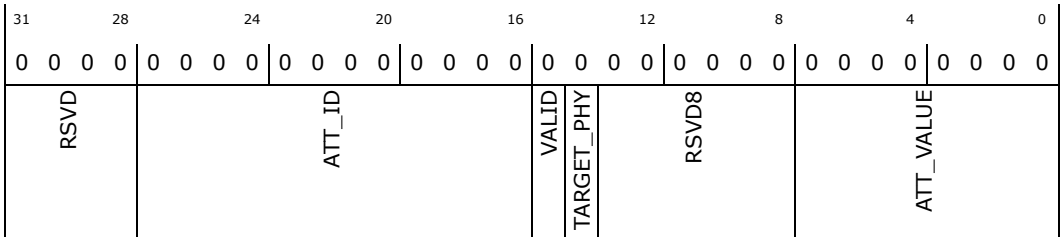
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A58h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.396 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG16)—Offset 8A5Ch

Access Method

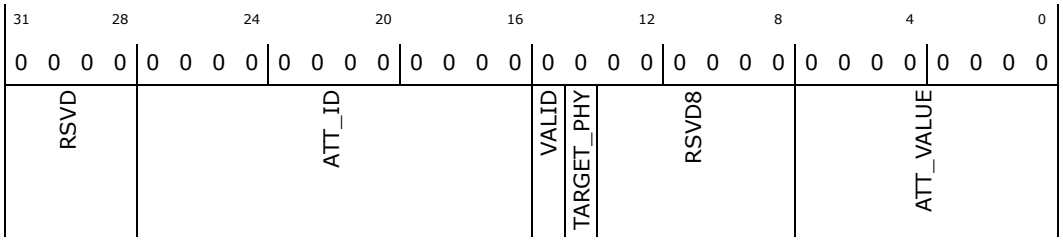
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A5Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.397 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG17)—Offset 8A60h

Access Method

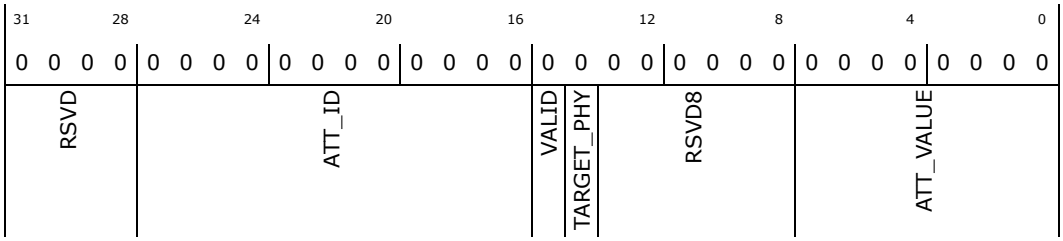
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A60h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.398 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG18)—Offset 8A64h

Access Method

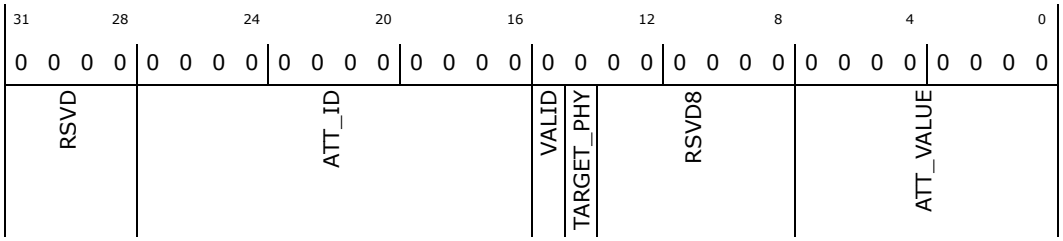
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A64h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.399 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG19)—Offset 8A68h

Access Method

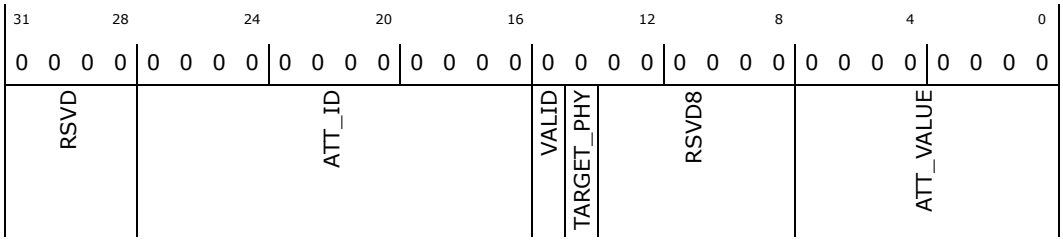
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A68h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.400 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG20)—Offset 8A6Ch

Access Method

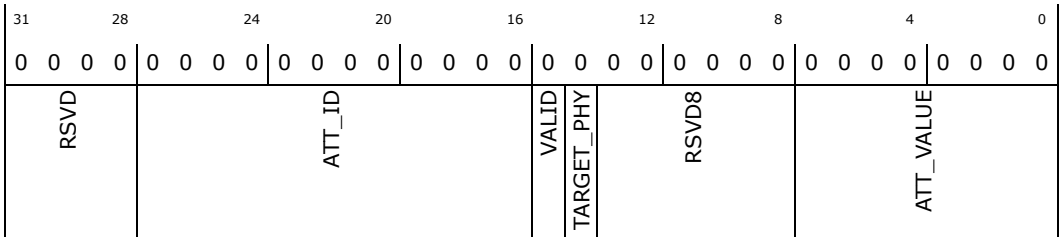
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A6Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.401 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG21)—Offset 8A70h

Access Method

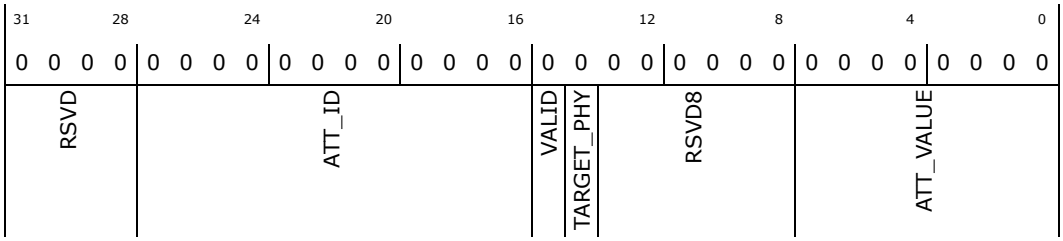
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A70h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.402 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG22)—Offset 8A74h

Access Method

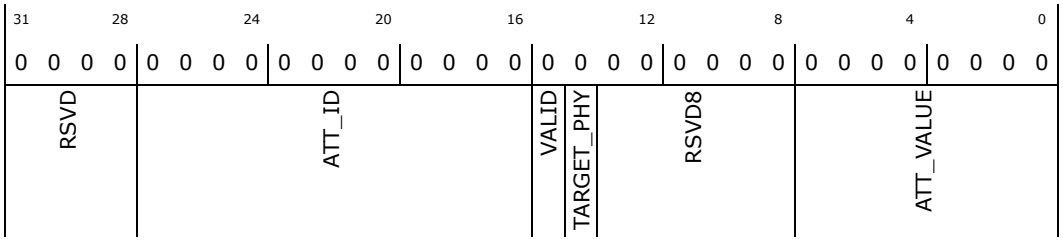
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A74h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.403 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG23)—Offset 8A78h

Access Method

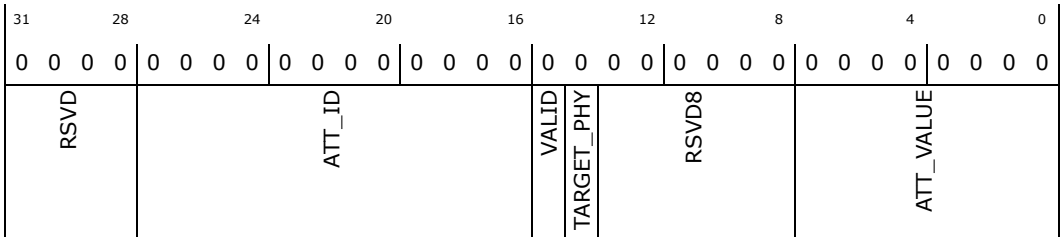
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A78h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.404 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG24)—Offset 8A7Ch

Access Method

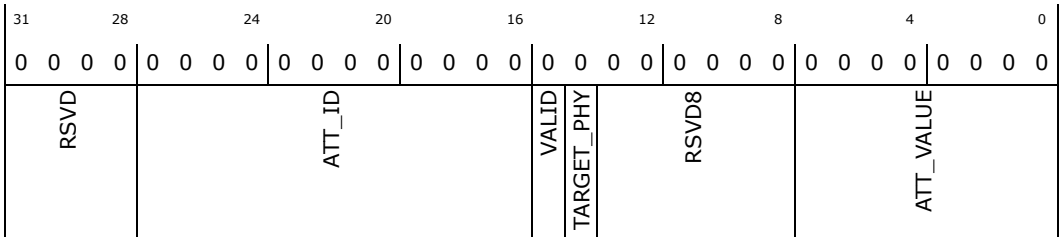
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A7Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.405 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG25)—Offset 8A80h

Access Method

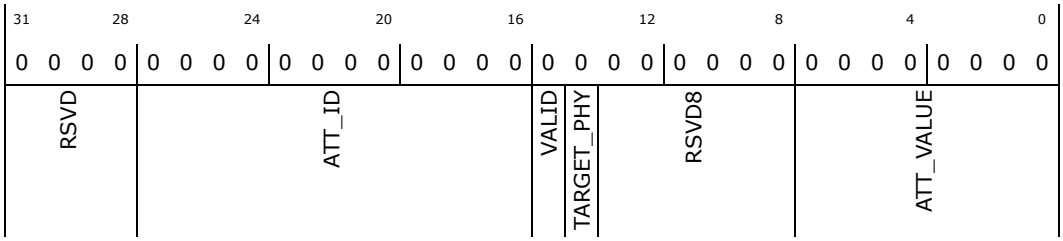
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A80h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.406 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG26)—Offset 8A84h

Access Method

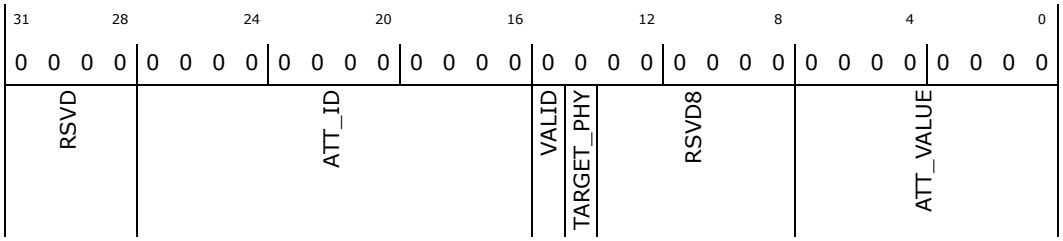
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A84h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.407 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG27)—Offset 8A88h

Access Method

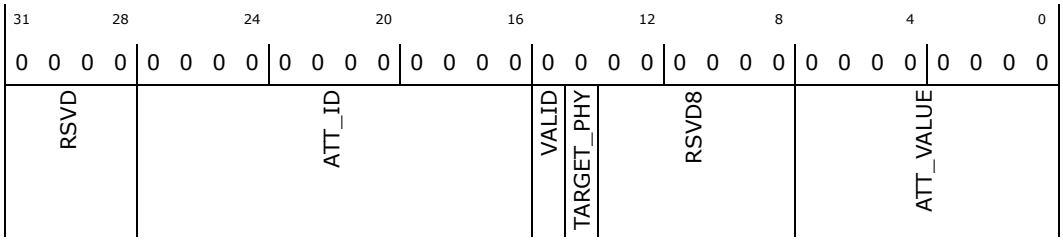
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A88h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.408 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG28)—Offset 8A8Ch

Access Method

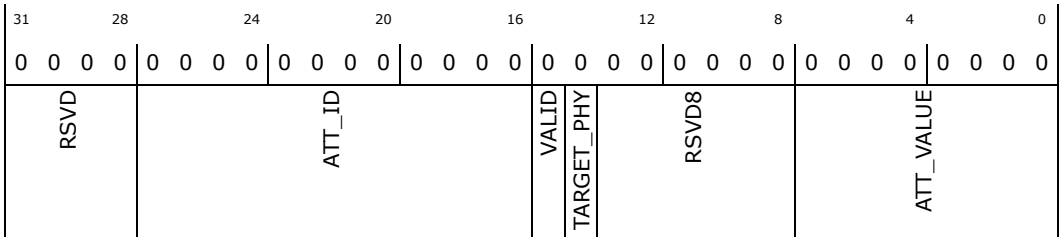
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A8Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.409 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG29)—Offset 8A90h

Access Method

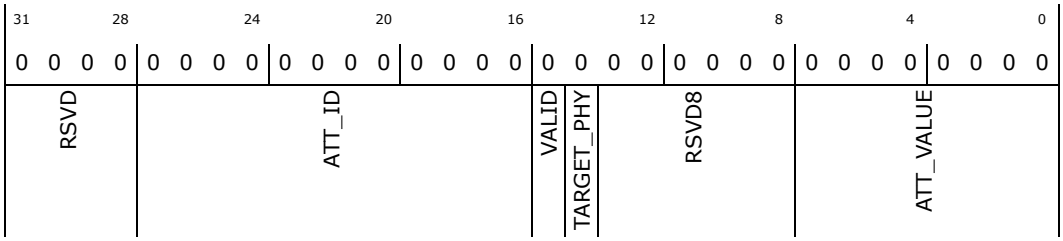
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A90h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.410 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG30)—Offset 8A94h

Access Method

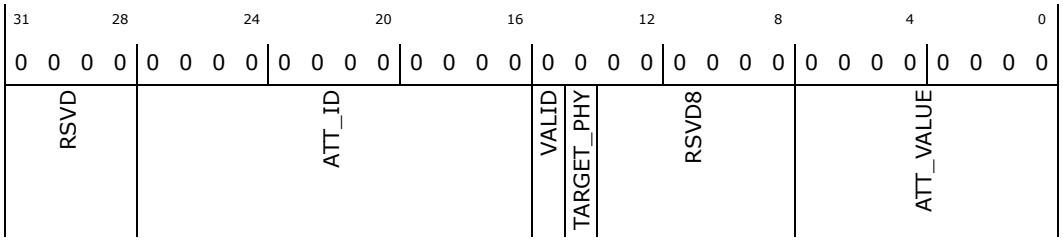
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A94h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.411 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG31)—Offset 8A98h

Access Method

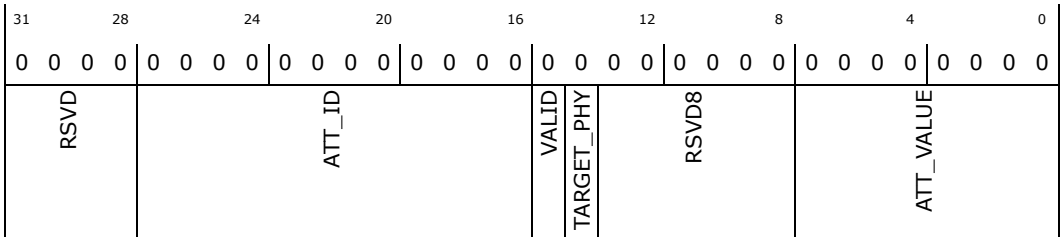
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A98h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.412 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG32)—Offset 8A9Ch

Access Method

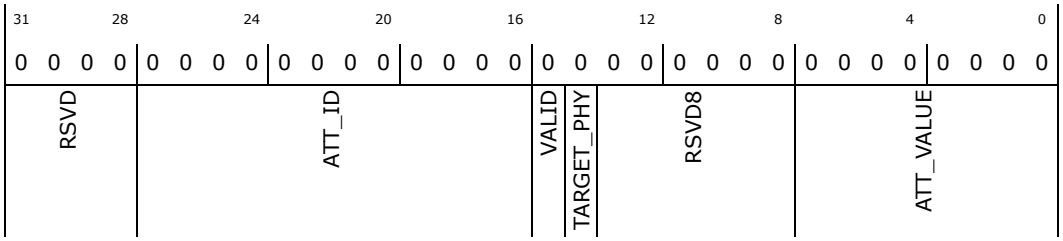
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8A9Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.413 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG33)—Offset 8AA0h

Access Method

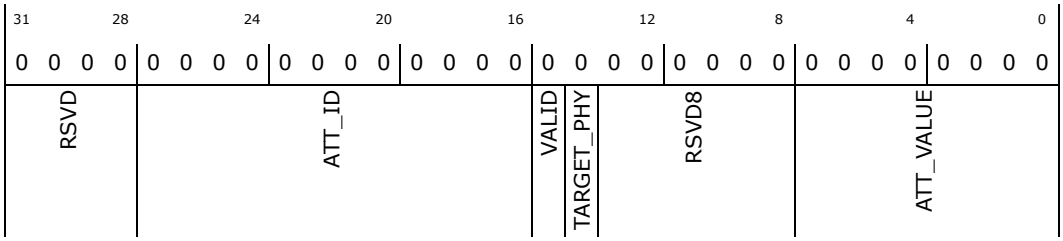
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AA0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.414 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG34)—Offset 8AA4h

Access Method

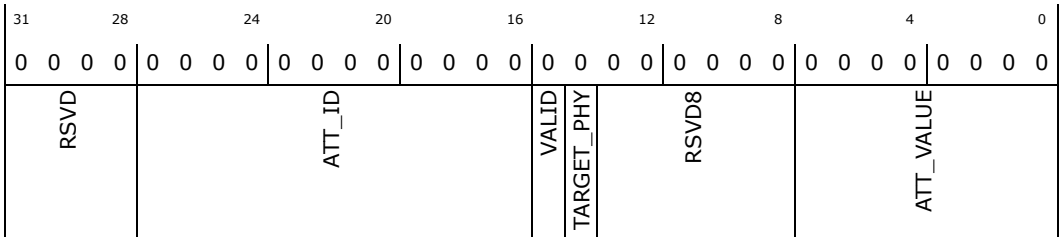
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AA4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.415 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG35)—Offset 8AA8h

Access Method

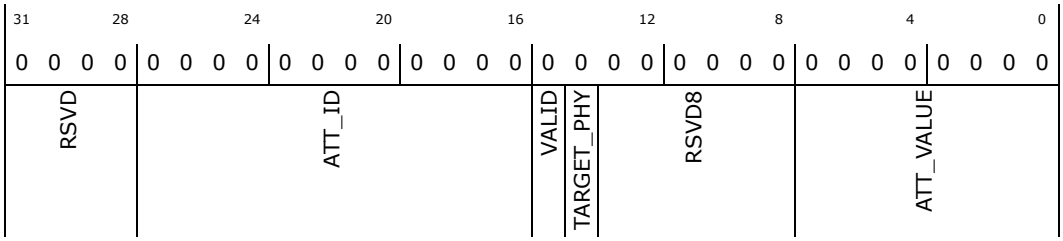
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AA8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.416 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG36)—Offset 8AACh

Access Method

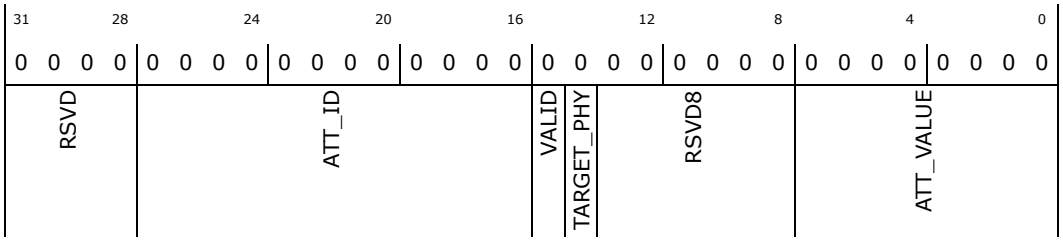
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AACh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.417 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG37)—Offset 8AB0h

Access Method

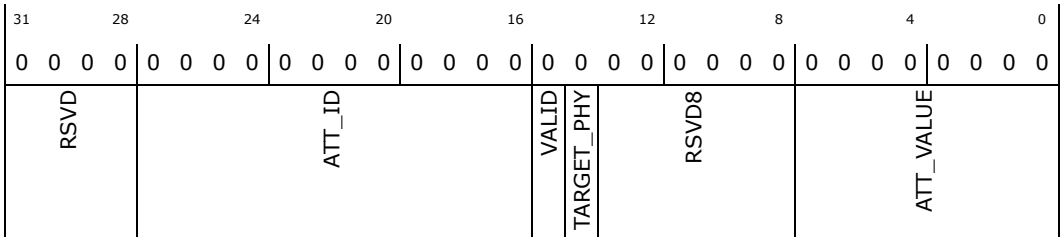
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AB0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.418 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG38)—Offset 8AB4h

Access Method

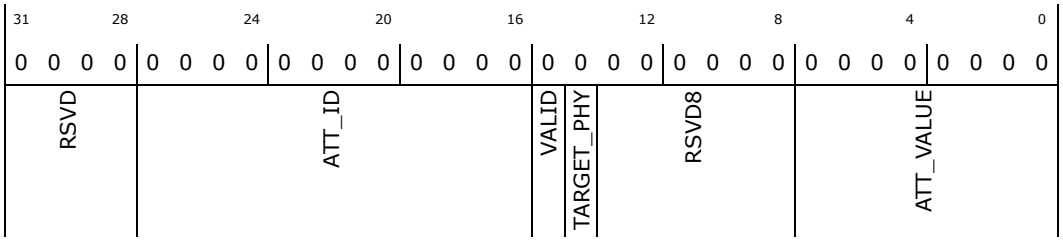
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AB4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.419 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG39)—Offset 8AB8h

Access Method

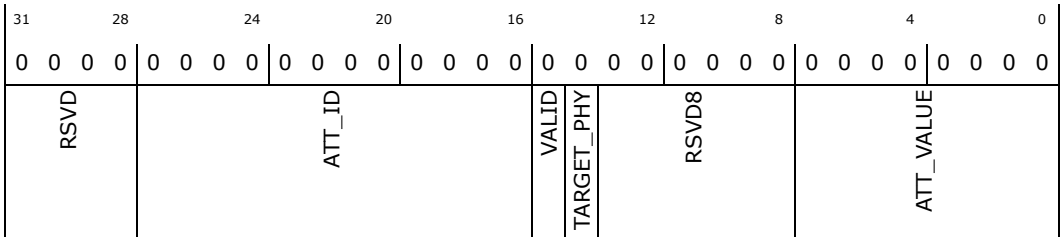
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AB8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.420 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG40)—Offset 8ABCh

Access Method

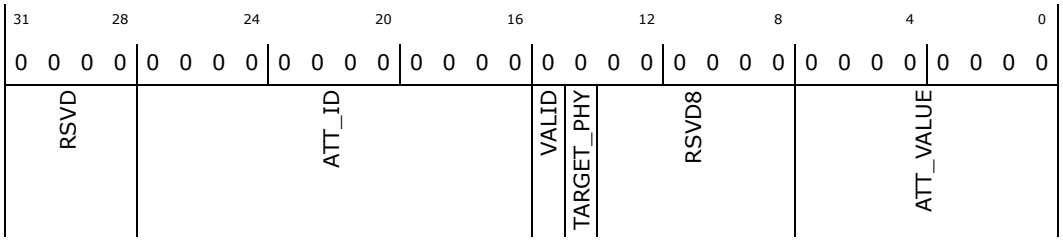
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8ABCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.421 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG41)—Offset 8AC0h

Access Method

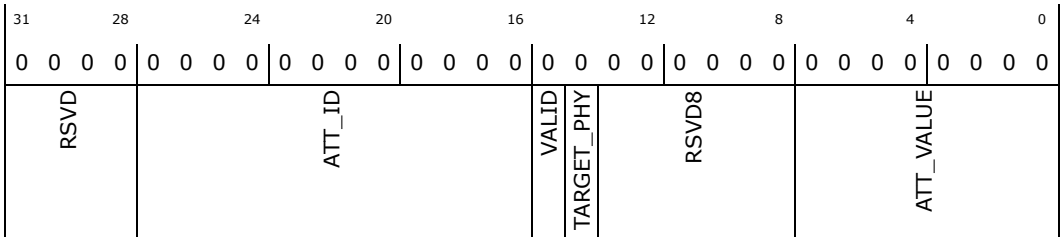
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AC0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.422 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG42)—Offset 8AC4h

Access Method

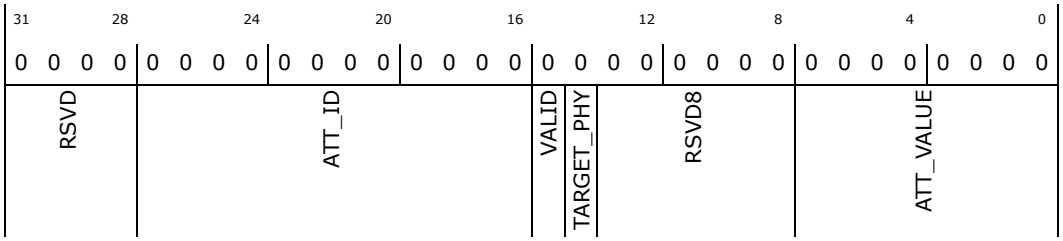
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AC4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.423 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG43)—Offset 8AC8h

Access Method

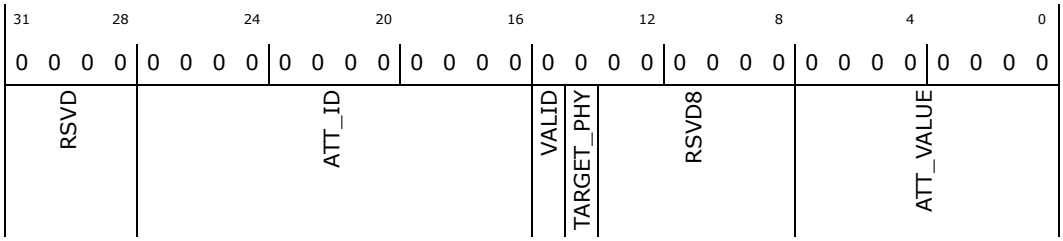
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AC8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.424 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG44)—Offset 8ACCh

Access Method

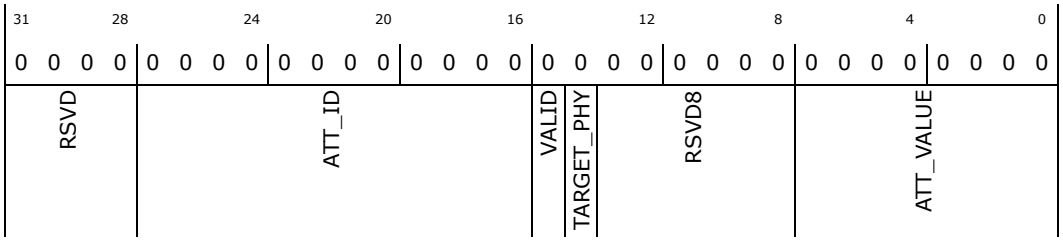
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8ACCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.425 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG45)—Offset 8AD0h

Access Method

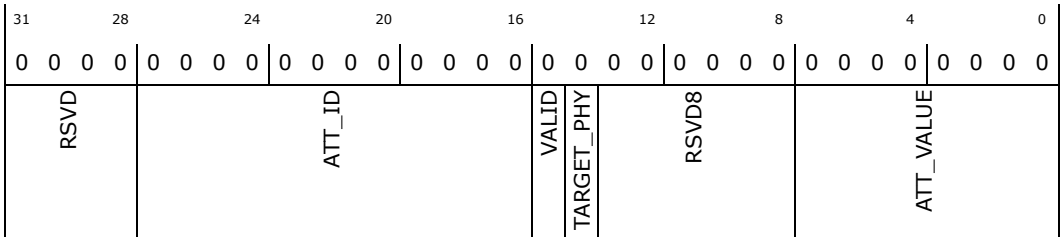
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AD0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.426 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG46)—Offset 8AD4h

Access Method

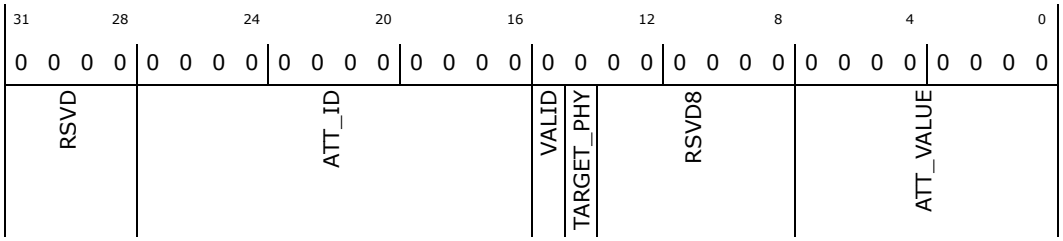
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AD4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.427 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG47)—Offset 8AD8h

Access Method

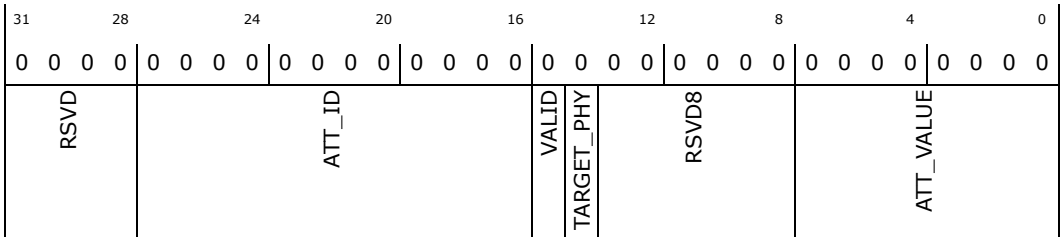
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AD8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.428 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG48)—Offset 8ADCh

Access Method

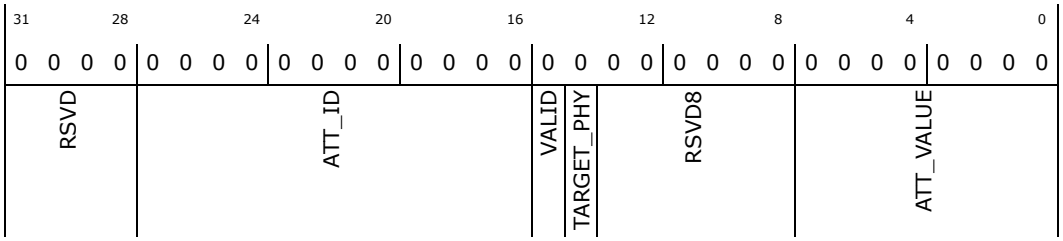
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8ADCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.429 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG49)—Offset 8AE0h

Access Method

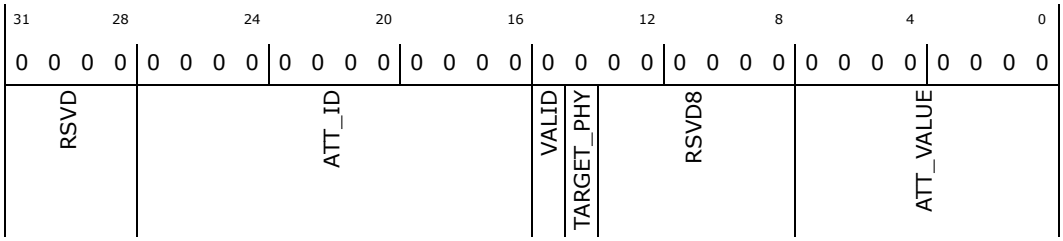
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AE0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.430 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG50)—Offset 8AE4h

Access Method

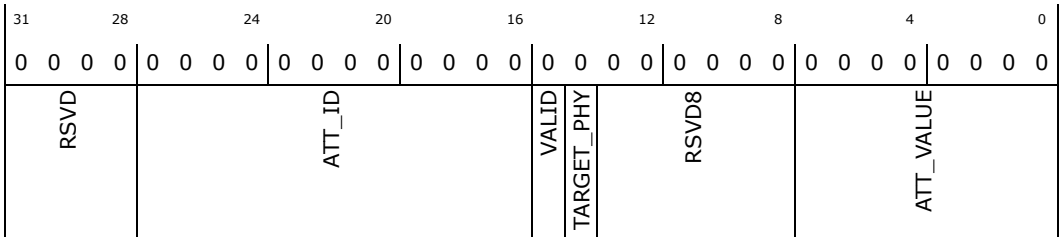
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AE4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.431 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG51)—Offset 8AE8h

Access Method

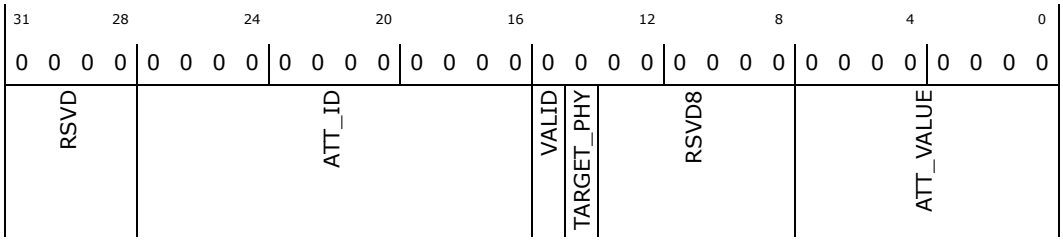
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AE8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.432 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG52)—Offset 8AECh

Access Method

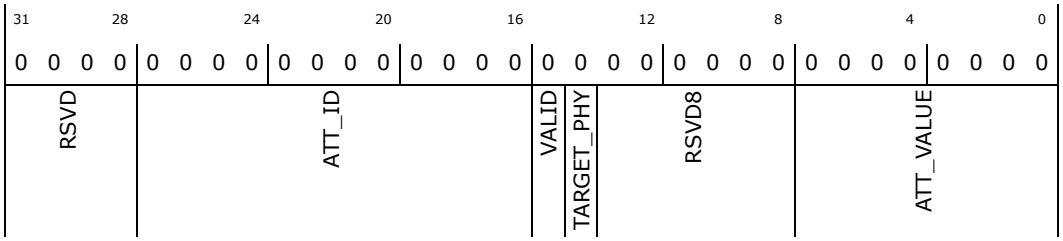
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AECh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.433 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG53)—Offset 8AF0h

Access Method

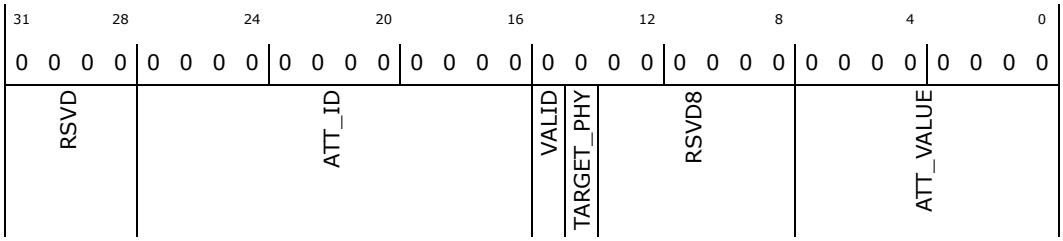
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AF0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.434 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG54)—Offset 8AF4h

Access Method

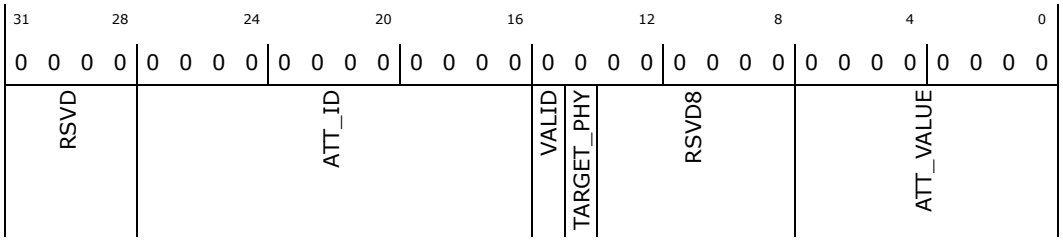
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AF4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.435 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG55)—Offset 8AF8h

Access Method

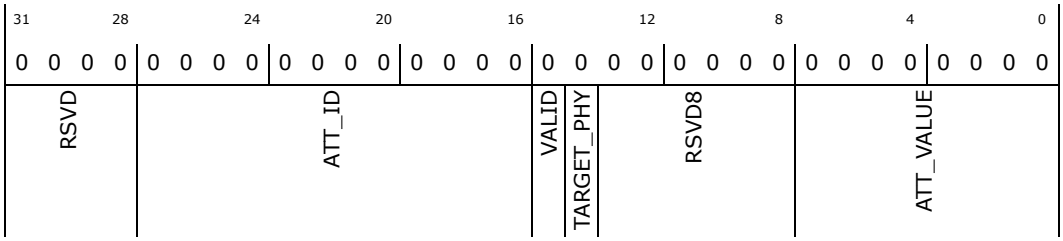
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AF8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.436 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG56)—Offset 8AFCh

Access Method

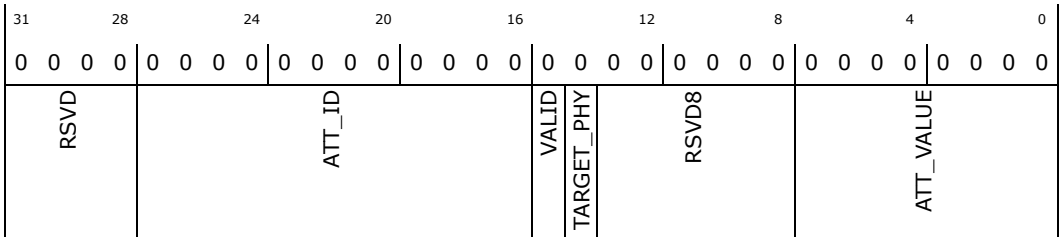
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8AFCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.437 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG57)—Offset 8B00h

Access Method

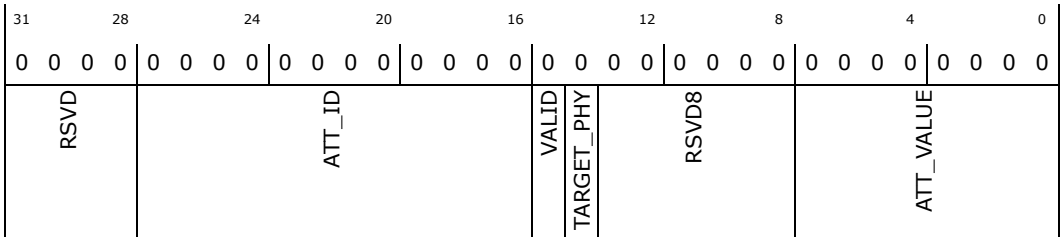
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8B00h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.438 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG58)—Offset 8B04h

Access Method

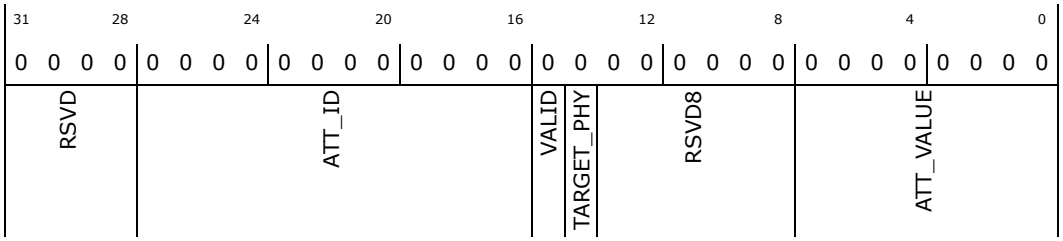
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8B04h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.439 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG59)—Offset 8B08h

Access Method

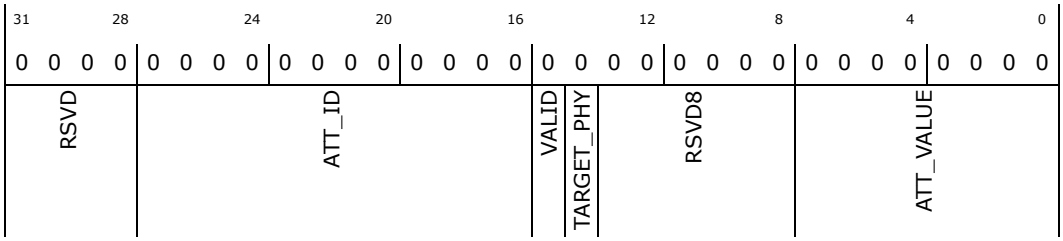
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8B08h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.440 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG60)—Offset 8B0Ch

Access Method

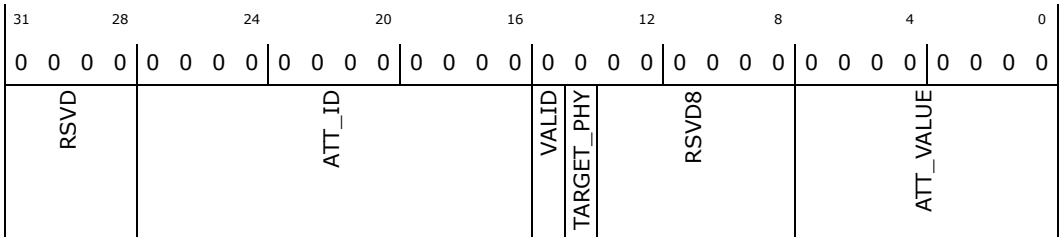
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8B0Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.441 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG61)—Offset 8B10h

Access Method

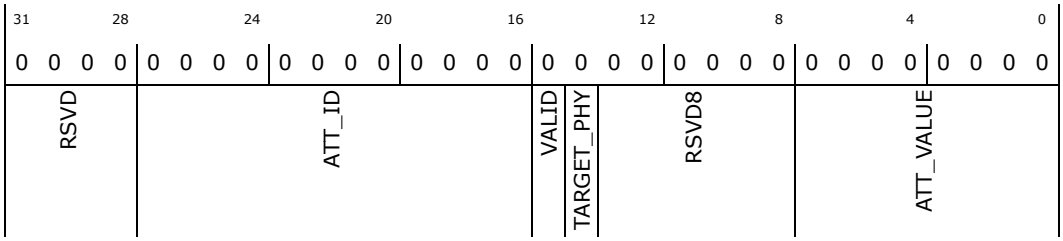
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8B10h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.442 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG62)—Offset 8B14h

Access Method

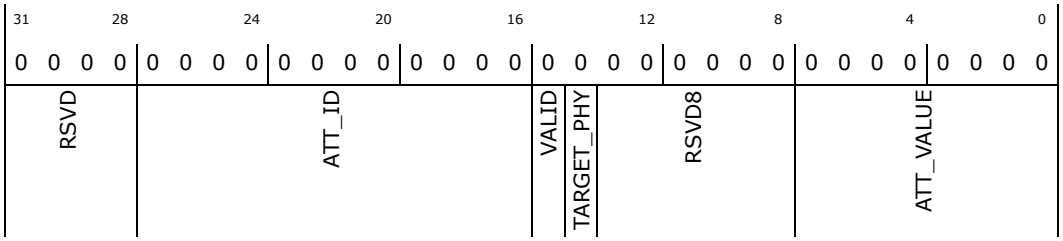
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8B14h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core

7.4.443 reg_SSIC_PORT_PROFILE_ATTRIBUTES_REG_type (PORT2_PROFILE_ATTRIBUTES_REG63)—Offset 8B18h

Access Method

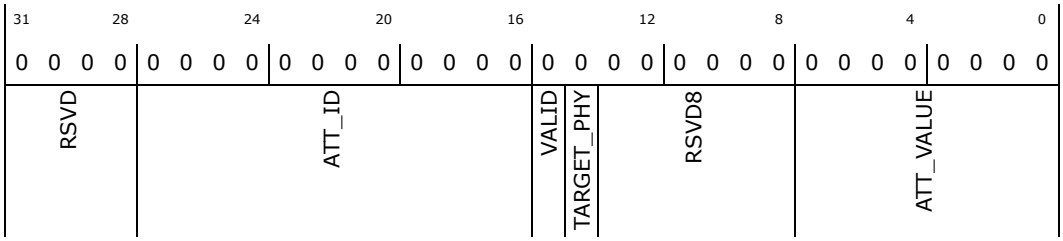
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x5A] + 8B18h

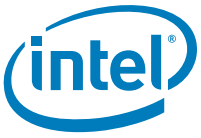
Op Codes:

h - Read, h - Write

Default: 00000000h



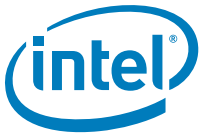
Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
27:16	0x0 RW	**Attribute ID (ATT_ID):** Reserved. **Power Well:** Core
15	0x0 RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16 **Power Well:** Core
14	0x0 RW	**TARGET_PHY:** 0 = Remote Phy 1 = Local Phy **Power Well:** Core
13:8	0x0 RO	**Reserved (RSVD8):** Reserved. **Power Well:** Core
7:0	0x0 RW	**ATTRIBUTE VALUE (ATT_VALUE):** Reserved. **Power Well:** Core



7.5 USB3 Memory Mapped I/O Common Registers

Table 41. Summary of Memory Mapped I/O Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
F000–F003h	4	"reg_CMNREG1_type (CMNREG1)—Offset F000h" on page 2924	1B000101h
F004–F007h	4	"reg_CMNREG2_type (CMNREG2)—Offset F004h" on page 2924	00000130h
F008–F00Bh	4	"reg_CMNREG3_type (CMNREG3)—Offset F008h" on page 2925	00000000h
F00C–F00Fh	4	"reg_CMNREG4_type (CMNREG4)—Offset F00Ch" on page 2926	00000000h
F010–F013h	4	"reg_CMNREG5_type (CMNREG5)—Offset F010h" on page 2927	00000802h
F014–F017h	4	"reg_CMNREG6_type (CMNREG6)—Offset F014h" on page 2928	4100052Ch
F018–F01Bh	4	"reg_CMNREG7_type (CMNREG7)—Offset F018h" on page 2928	00000000h
F01C–F01Fh	4	"reg_CMNREG8_type (CMNREG8)—Offset F01Ch" on page 2929	00000001h
F020–F023h	4	"reg_CMNREG9_type (CMNREG9)—Offset F020h" on page 2930	00040000h
F024–F027h	4	"reg_CMNREG10_type (CMNREG10)—Offset F024h" on page 2931	00000000h
F028–F02Bh	4	"reg_CMNREG11_type (CMNREG11)—Offset F028h" on page 2932	00000000h
F02C–F02Fh	4	"reg_CMNREG12_type (CMNREG12)—Offset F02Ch" on page 2932	00000000h
F030–F033h	4	"reg_CMNREG13_type (CMNREG13)—Offset F030h" on page 2933	00000000h
F034–F037h	4	"reg_CMNREG14_type (CMNREG14)—Offset F034h" on page 2934	00000000h
F038–F03Bh	4	"reg_CMNREG15_type (CMNREG15)—Offset F038h" on page 2935	00000000h
F03C–F03Fh	4	"reg_CMNREG16_type (CMNREG16)—Offset F03Ch" on page 2935	00000000h
F040–F043h	4	"reg_DFXREG0_type (DFXREG0)—Offset F040h" on page 2936	00000000h
F044–F047h	4	"reg_DFXREG1_type (DFXREG1)—Offset F044h" on page 2937	00000000h
F048–F04Bh	4	"reg_DFXREG2_type (DFXREG2)—Offset F048h" on page 2937	00000000h
F04C–F04Fh	4	"reg_DFXREG3_type (DFXREG3)—Offset F04Ch" on page 2938	00000000h
F050–F053h	4	"reg_DFXREG4_type (DFXREG4)—Offset F050h" on page 2939	00000000h
F054–F057h	4	"reg_DFXREG5_type (DFXREG5)—Offset F054h" on page 2939	00000013h
F058–F05Bh	4	"reg_DFXREG6_type (DFXREG6)—Offset F058h" on page 2940	00060000h
F05C–F05Fh	4	"reg_DFXREG7_type (DFXREG7)—Offset F05Ch" on page 2941	00060000h
F060–F063h	4	"reg_DFXREG8_type (DFXREG8)—Offset F060h" on page 2942	00000000h
F064–F067h	4	"reg_DFXREG9_type (DFXREG9)—Offset F064h" on page 2943	00000000h
F068–F06Bh	4	"reg_DFXREG10_type (DFXREG10)—Offset F068h" on page 2943	00000000h
F06C–F06Fh	4	"reg_DFXREG11_type (DFXREG11)—Offset F06Ch" on page 2944	00000000h
F070–F073h	4	"reg_DFXREG12_type (DFXREG12)—Offset F070h" on page 2945	00000000h
F074–F077h	4	"reg_CMNREG17_type (CMNREG17)—Offset F074h" on page 2946	FA21BE2Ch
F078–F07Bh	4	"reg_CMNREG18_type (CMNREG18)—Offset F078h" on page 2946	00000000h
F07C–F07Fh	4	"reg_CMNREG19_type (CMNREG19)—Offset F07Ch" on page 2947	16010C0Ch



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
F080–F083h	4	"reg_CMNREG20_type (CMNREG20)—Offset F080h" on page 2948	00000000h
F084–F087h	4	"reg_CMNREG21_type (CMNREG21)—Offset F084h" on page 2948	00000000h
F088–F08Bh	4	"reg_CMNREG22_type (CMNREG22)—Offset F088h" on page 2949	00000000h

7.5.1 reg_CMNREG1_type (CMNREG1)—Offset F000h

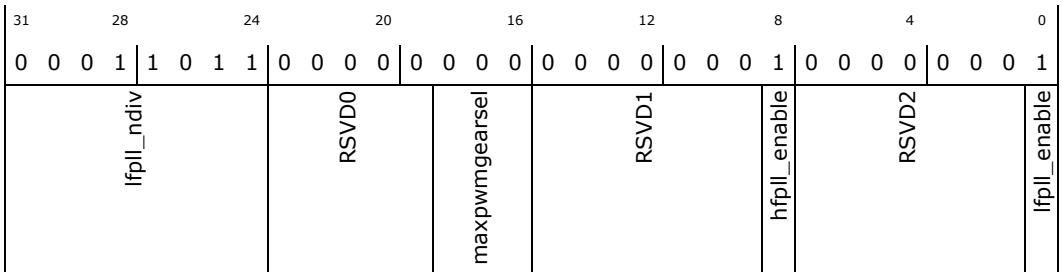
CMNREG1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F000h

Default: 1B000101h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x1b RW	**lfpll_ndiv:** Low Frequency Divider Setting sets divide ratio to generate pwmck from hsck. For 19.2Mhz refclk: Rate A=0x17, Rate B=0x1b; For 26Mhz refclk: Rate A=0x17; Rate B=0x1A
23:19	0x0 RO	**RSVD0:** Reserved
18:16	0x0 RW	**maxpwmgearsel:** Select divisor value for max PWM trunk clock. For functional mode this setting must be set to 0 at all times.
15:9	0x0 RO	**RSVD1:** Reserved
8	0x1 RW	**hfpll_enable:** Enable PLL Enables VCO bias and VCO outputs Enables analog circuits inside PLL
7:1	0x0 RO	**RSVD2:** Reserved
0	0x1 RW	**lfpll_enable:** Enable LF PLL for trunk clock.

7.5.2 reg_CMNREG2_type (CMNREG2)—Offset F004h

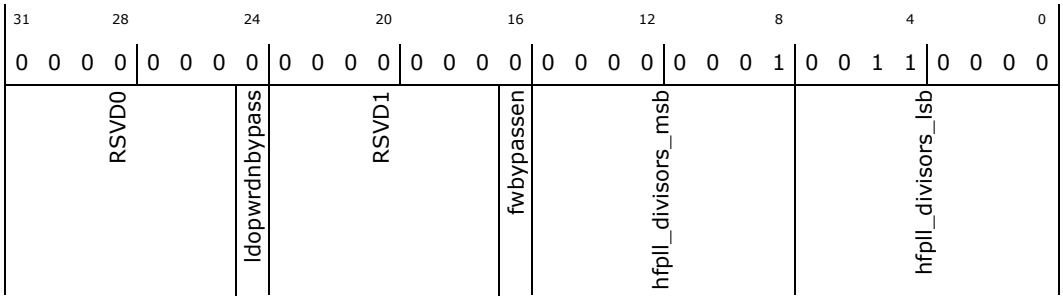
CMNREG2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F004h

Default: 00000130h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**ldopwrdnbypass:** LDO bypass mode enable for debug.
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RW	**fwbypassen:** Overrides the FW logic
15:8	0x1 RW	**hfpll_divisors_msb:** HFPLL feedback divisors. For 19.2Mhz refclk, set to 1. For 26Mhz and 25MHz(HBP), set to 0.
7:0	0x30 RW	**hfpll_divisors_lsb:** HFPLL feedback divisors. For 19.2Mhz refclk: Rate A=0x04; Rate B=0x30. For 26Mhz refclk: Rate A=0xc0; Rate B=0xe0; For 25Mhz refclk(HBP): Rate A=0xc8; Rate B=0xF0

7.5.3 reg_CMNREG3_type (CMNREG3)—Offset F008h

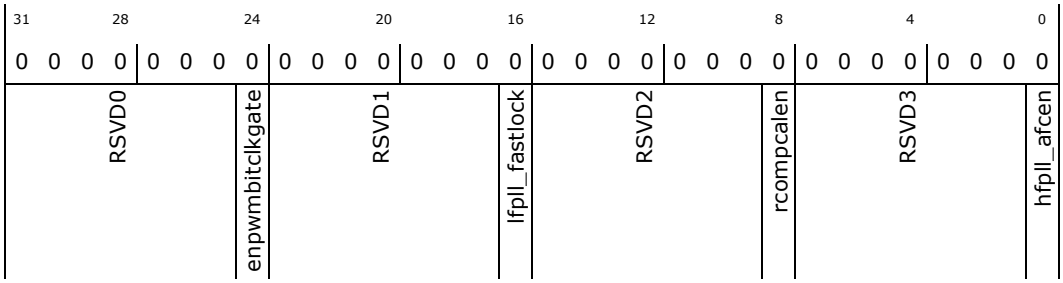
CMNREG3

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F008h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**enpwmbitclkgate:** pwm bit clock gating enable (1=enable ck, 0=ck gated).
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RW	**lfpll_fastlock:** Enable fast lock using previously calibrated values
15:9	0x0 RO	**RSVD2:** Reserved
8	0x0 RW	**rcompcalen:** RCOMP Calibration enable
7:1	0x0 RO	**RSVD3:** Reserved
0	0x0 RW	**hfpll_afcen:** Enable automatic frequency counter. Default should be enabled (=1). Only disable in debug mode.

7.5.4 reg_CMNREG4_type (CMNREG4)—Offset F00Ch

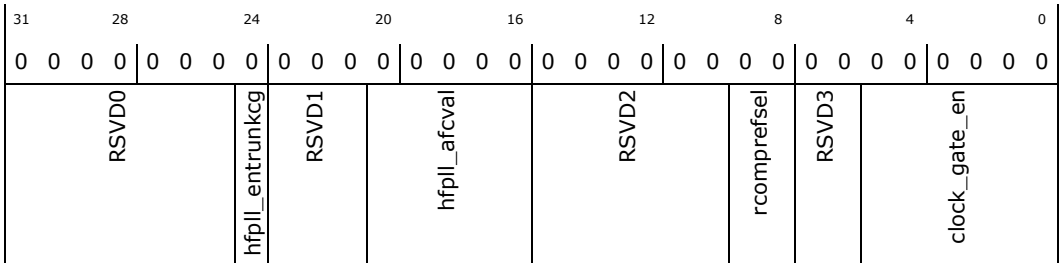
CMNREG4

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F00Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**hfpll_entrunkcg:** Enable maxhsck (trunck clock). 1=enabled, 0=gated.
23:21	0x0 RO	**RSVD1:** Reserved
20:16	0x0 RW	**hfpll_afcval:** AFC tuning bits used to force coarse fequency setting when the AFC is disabled, Used in debug only.

Bit Range	Default & Access	Field Name (ID): Description
15:10	0x0 RO	**RSVD2:** Reserved
9:8	0x0 RW	**rcomprefsel:** NA
7:6	0x0 RO	**RSVD3:** Reserved
5:0	0x0 RW	**clock_gate_en:** [0]: MaxHSClk High speed trunk clock gate enable; [1] MaxPWMClk trunk clock gate enable; [2] pll_ref_clk clock gate enable; [3] rmmi_ref_clk clock gate enable; [4] pll_ref_clk trunk clock gate enable; [5] rmmi_cfg_clk trunk clock gate en;

7.5.5 reg_CMNREG5_type (CMNREG5)—Offset F010h

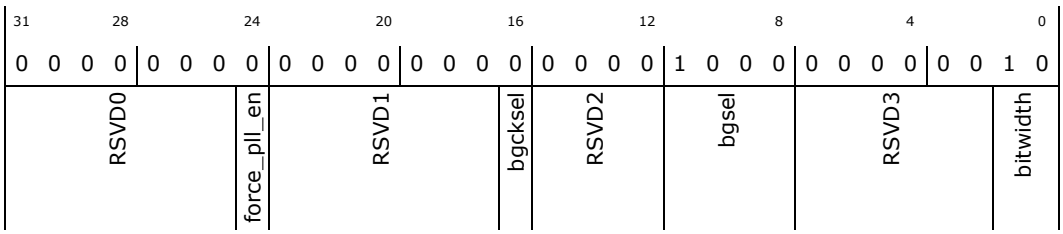
CMNREG5

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F010h

Default: 00000802h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**force_pll_en:** Enable the PLL after power up and reset de-assertion. When set, PLL will not be shutdown unless common lane core is being powered down.
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RW	**bgcksel:** band gap clock select. 0- Reference clock:: 1- Reference Clock/2.
15:12	0x0 RO	**RSVD2:** Reserved
11:8	0x8 RW	**bgsel:** Bandgap voltage trim.
7:2	0x0 RO	**RSVD3:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
1:0	0x2 RW	**bitwidth:** Divider setting for trunk clocks. 01: divide by 2 (10bit RMMI); 10: divide by 4 (20bit RMMI); 11: divide by 8 (40bit RMMI); 00: reserved

7.5.6 reg_CMNREG6_type (CMNREG6)—Offset F014h

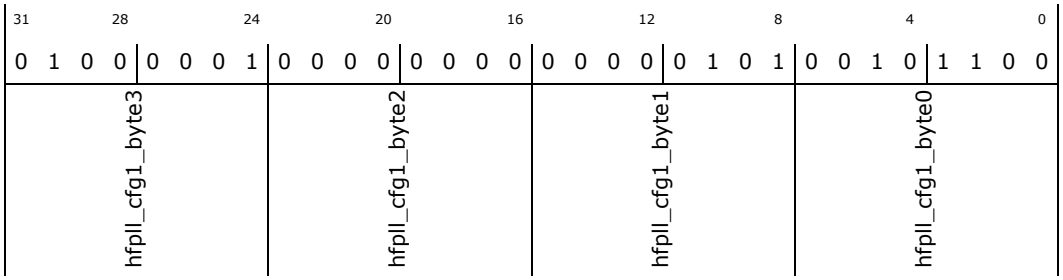
CMNREG6

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F014h

Default: 4100052Ch



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x41 RW	**hfpll_cfg1_byte3:** HFPLL configuration register as required by AFE bits [31:24]. ANN: [31:30]=lockthresh[1:0], [29:25]=lpf_gain[4:0], [24]=lfp_maxstep[4]. Initialize to 0x81. SoC: [30]=lockthresh[0], [29]=lpfrstmode, [28:26]=pfdchop[2:0], [25]=pfdchopen, [24]=pfdresipw
23:16	0x0 RW	**hfpll_cfg1_byte2:** HFPLL configuration register as required by AFE bits [23:16]. ANN: [23:20]=lfp_maxstep[3:0], [19:16]=cselext[8:5]. Initialize to 0xF0. SoC: [23:22]=pfdresipw[1:0], [21:16]=tcompcode[7:2]. Initialize to 0.
15:8	0x5 RW	**hfpll_cfg1_byte1:** HFPLL configuration register as required by AFE bits [15:8]. ANN: [15:11]=cselext[4:0], [10:8]=vcoamp[3:1]. Initialize to 0. SoC: [15:14]=tcompcode[1:0], [13]=tcompen, [12:11]=tcomprange[1:0], [10:8]=ivco[3:1]. Initial setting Rate A: 0x03 Rate B: 0x
7:0	0x2c RW	**hfpll_cfg1_byte0:** HFPLL configuration register as required by AFE bits [7:0]. ANN: [7]=vcoamp[0], [6:5]=reserved, [4:3]=lpf_avg[1:0], [2:0]=pllmodesel[2:0]. Initialize to 0x15. SoC: [7]=ivco[0], [6]=ivcoextra, [5:3]=vcovarcm1[2:0], [2:0]=vcovarcm2[2:0]. Initialize to 0

7.5.7 reg_CMNREG7_type (CMNREG7)—Offset F018h

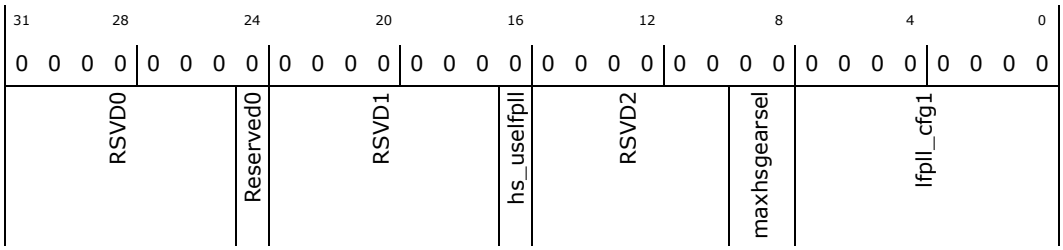
CMNREG7

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F018h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RO	**Reserved0:** Reserved
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RW	**hs_uselfpll:** Use LFPLL for high speed clocks.
15:10	0x0 RO	**RSVD2:** Reserved
9:8	0x0 RW	**maxhsgearsel:** Sets max trunk clock frequency for HS supported on a product. 00: divide by 1 (Gear3) 01: divide by 2 (Gear2) 10: divide by 4 (Gear1) 11: divide by 8 (NA)
7:0	0x0 RW	**lfpll_cfg1:** [2:0] - lockctr: [4:3] - lockdiv: [7:5] - lockthresh.

7.5.8 reg_CMNREG8_type (CMNREG8)—Offset F01Ch

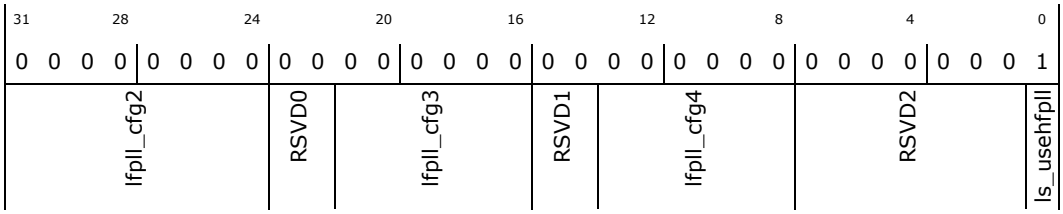
CMNREG8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F01Ch

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**lfpll_cfg2:** [2:0] - adaptivemin: [3] - adaptivethresh: [5:4] - pdgain: [6]-relocken: [7] - shiften.

Bit Range	Default & Access	Field Name (ID): Description
23:22	0x0 RO	**RSVD0:** Reserved
21:16	0x0 RW	**lfpll_cfg3:** [2:0] - shiftki[2:0]: [5:3] - shfitkii.
15:14	0x0 RO	**RSVD1:** Reserved
13:8	0x0 RW	**lfpll_cfg4:** [2:0] - shiftp[2:0]: [5:3] - shfitpi.
7:1	0x0 RO	**RSVD2:** Reserved
0	0x1 RW	**ls_usehfpll:** Use HFPLL for PWM clocks. For ANN this must be 1 at all times. For SoC the POR is set to 1.

7.5.9 reg_CMNREG9_type (CMNREG9)—Offset F020h

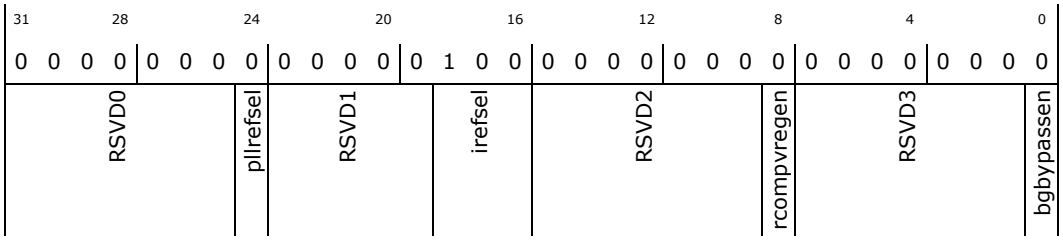
CMNREG9

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F020h

Default: 00040000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**pllrefsel:** Reference clock select 1'b0 - From SoC: 1'b1 - From external bumps. In functional mode only clock from SoC is supported
23:19	0x0 RO	**RSVD1:** Reserved
18:16	0x4 RW	**irefsel:** Reference current amplitude select
15:9	0x0 RO	**RSVD2:** Reserved
8	0x0 RW	**rcompvregen:** enable vreg for RCOMP driver

Bit Range	Default & Access	Field Name (ID): Description
7:1	0x0 RO	**RSVD3:** Reserved
0	0x0 RW	**bgbypassen:** Bandgap bypass enable.

7.5.10 reg_CMNREG10_type (CMNREG10)—Offset F024h

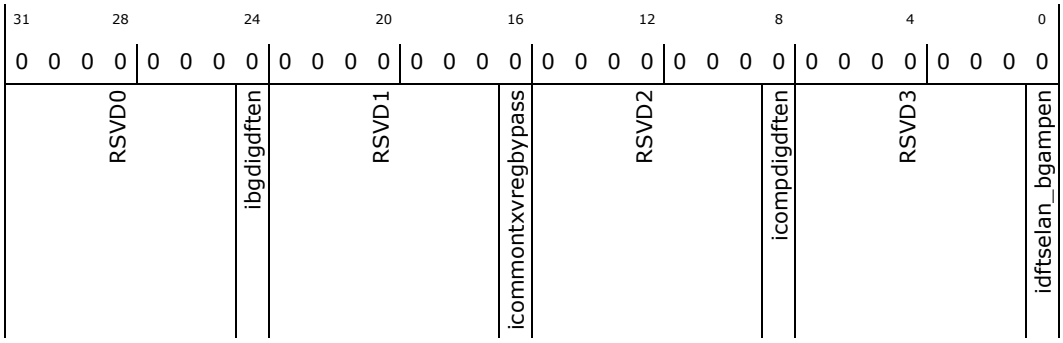
CMNREG10

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F024h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**ibgdigdften:** BG DFT enable.
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RW	**icommontxvregbypass:** bypass vreg for RCOMP driver
15:9	0x0 RO	**RSVD2:** Reserved
8	0x0 RW	**icompdigdften:** COMP DFT enable
7:1	0x0 RO	**RSVD3:** Reserved
0	0x0 RW	**idftselan_bgampen:** DFT select, analog, one hot

7.5.11 reg_CMNREG11_type (CMNREG11)—Offset F028h

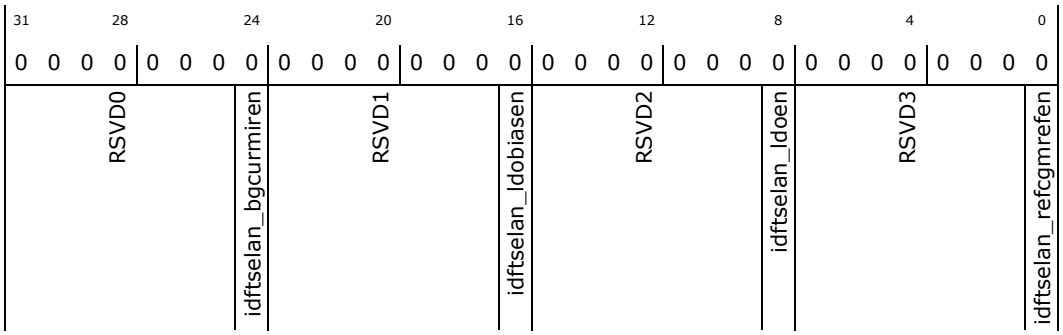
CMNREG11

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F028h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**idftselan_bgcurmiren:** DFT select, analog, one hot.
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RW	**idftselan_ldobiasen:** DFT select, analog, one hot.
15:9	0x0 RO	**RSVD2:** Reserved
8	0x0 RW	**idftselan_ldoen:** DFT select, analog, one hot.
7:1	0x0 RO	**RSVD3:** Reserved
0	0x0 RW	**idftselan_refcgmrefen:** DFT select, analog, one hot

7.5.12 reg_CMNREG12_type (CMNREG12)—Offset F02Ch

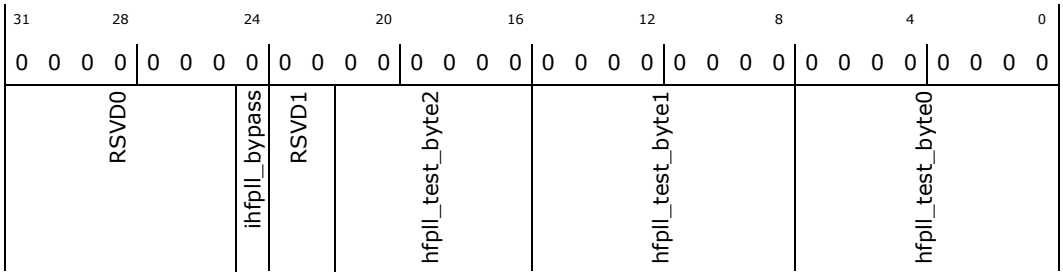
CMNREG12

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F02Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**ihfpll_bypass:** HFPLL Bypass Passes refclk PLL input directly onto PLL output
23:22	0x0 RO	**RSVD1:** Reserved
21:16	0x0 RW	**hfpll_test_byte2:** HFPLL Test Control Placeholder for HFPLL test control vcoidven, vctlobsen
15:8	0x0 RW	**hfpll_test_byte1:** HFPLL Test Control Placeholder for HFPLL test control vcoidven, vctlobsen
7:0	0x0 RW	**hfpll_test_byte0:** HFPLL Test Control Placeholder for HFPLL test control vcoidven, vctlobsen

7.5.13 reg_CMNREG13_type (CMNREG13)—Offset F030h

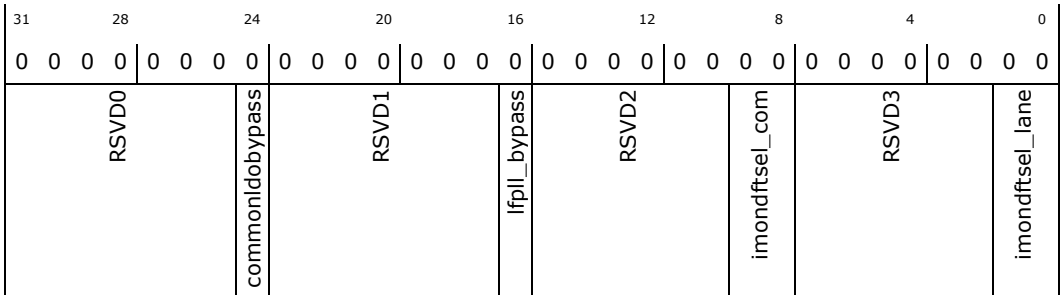
CMNREG13

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F030h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
24	0x0 RW	**commonldobypass:** bypass LDO in COMMON lane.
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RW	**lfpll_bypass:** Low Frequency Bypass . Drives refclk onto pwmckp/n .
15:10	0x0 RO	**RSVD2:** Reserved
9:8	0x0 RW	**imondftsel_com:** DFT select. Select common lane digital signals
7:2	0x0 RO	**RSVD3:** Reserved
1:0	0x0 RW	**imondftsel_lane:** DFT select. Select left or right lanes digital signals

7.5.14 reg_CMNREG14_type (CMNREG14)—Offset F034h

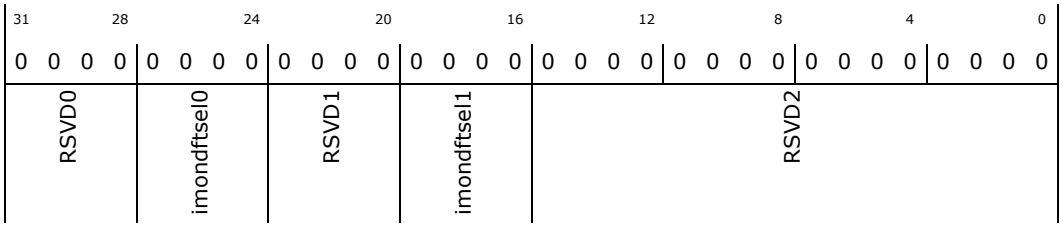
CMNREG14

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F034h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RSVD0:** Reserved
27:24	0x0 RW	**imondftsel0:** select which internal digital signals in COMMON
23:20	0x0 RO	**RSVD1:** Reserved
19:16	0x0 RW	**imondftsel1:** select which internal digital signals in COMMON
15:0	0x0 RO	**RSVD2:** Reserved

7.5.15 reg_CMNREG15_type (CMNREG15)—Offset F038h

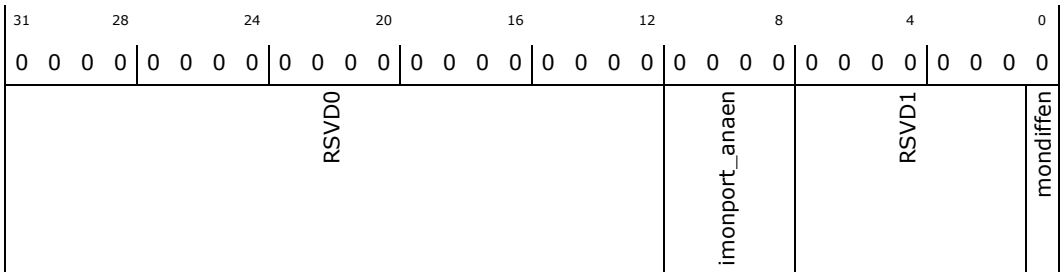
CMNREG15

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F038h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RSVD0:** Reserved
11:8	0x0 RW	**imonport_anaen:** enable analog monitor paths. Choose mapping between 2 analog buses and 2 monitor ports.
7:1	0x0 RO	**RSVD1:** Reserved
0	0x0 RW	**mondiffen:** enable differential monitoring mode

7.5.16 reg_CMNREG16_type (CMNREG16)—Offset F03Ch

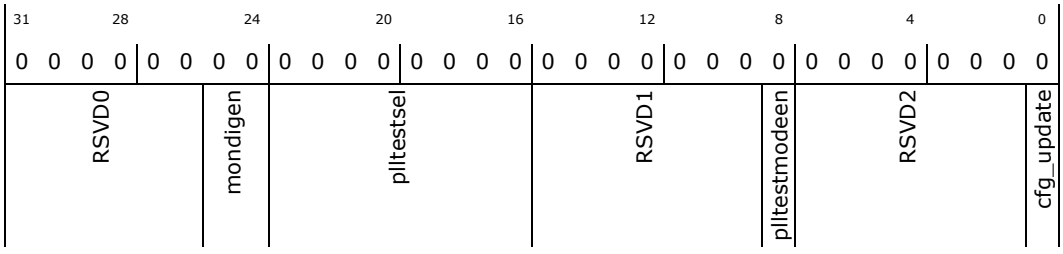
CMNREG16

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F03Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD0:** Reserved
25:24	0x0 RW	**mondigen:** enable digital monitor drivers.
23:16	0x0 RW	**plltestsel:** select which internal signal in the PLL to send to monitor bumps.
15:9	0x0 RO	**RSVD1:** Reserved
8	0x0 RW	**plltestmodeen:** mask test config bits.
7:1	0x0 RO	**RSVD2:** Reserved
0	0x0 RW	**cfg_update:** Configuration update to copy the shadow register contents to the effective register

7.5.17 reg_DFXREG0_type (DFXREG0)—Offset F040h

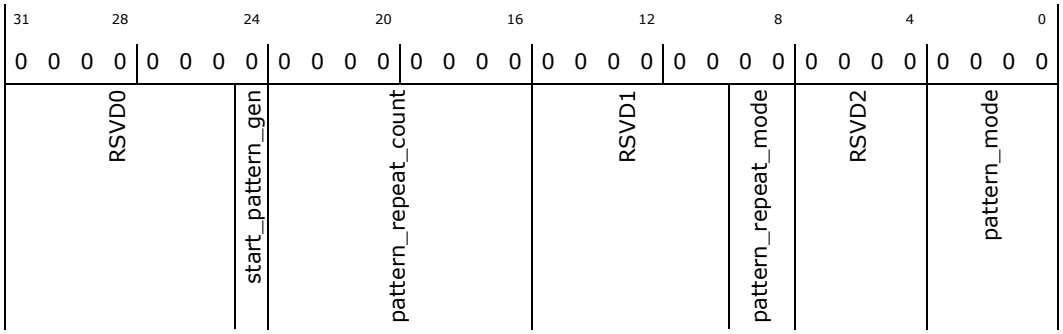
DFXREG0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F040h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**start_pattern_gen:** 1'b1 = Starts pattern gen in continous mode , 1'b0 = stop the continous burst.
23:16	0x0 RW	**pattern_repeat_count:** The count for which pattern repeats. Any 8 bit non zero value
15:10	0x0 RO	**RSVD1:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
9:8	0x0 RW	**pattern_repeat_mode:** 8h1 8bit repeat count, 8h2 11bit repeat count, 8h3 continuous mode
7:4	0x0 RO	**RSVD2:** Reserved
3:0	0x0 RW	**pattern_mode:** 8h1 CJTPAT, 8h2 CRPAT, 8h3 UserDefined

7.5.18 reg_DFXREG1_type (DFXREG1)—Offset F044h

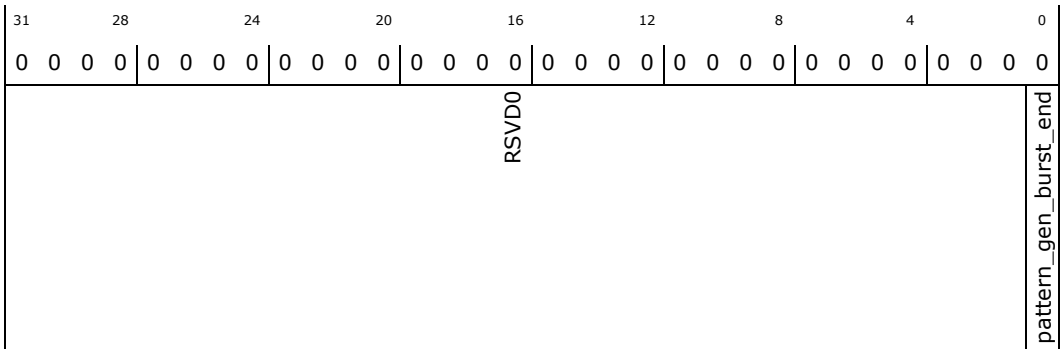
DFXREG1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F044h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RW/1C	**pattern_gen_burst_end:** Set by hardware to indicate that the pattern generation burst has completed.The software has to then write 1 into patter_gen_burst_end field to clear this.

7.5.19 reg_DFXREG2_type (DFXREG2)—Offset F048h

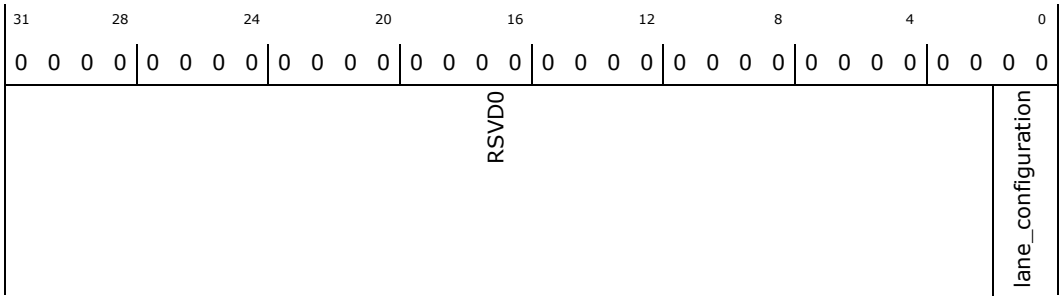
DFXREG2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F048h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RW	**lane_configuration:** 0: lane0 only 1: lane0, lane1 only 2: lane0, lane1, lane2 only 3: All lanes present

7.5.20 reg_DFXREG3_type (DFXREG3)—Offset F04Ch

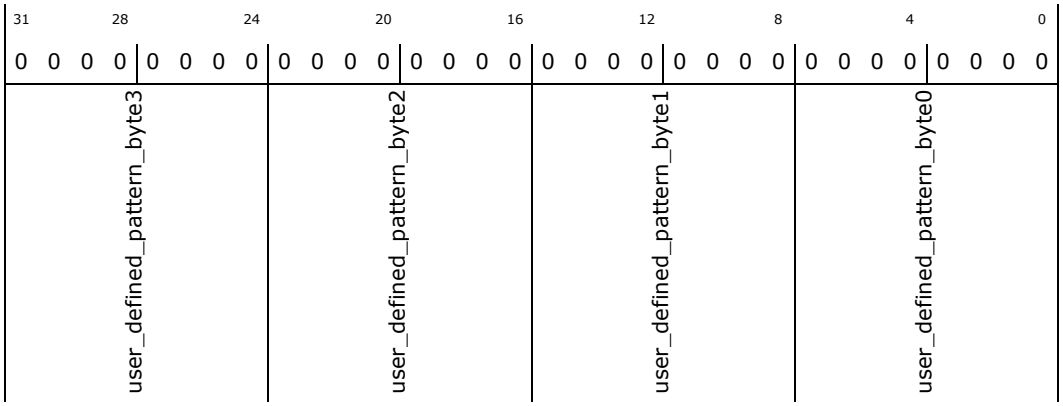
DFXREG3

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F04Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**user_defined_pattern_byte3:** Register value of user defined pattern .Upper 8 bits are not sent - reserved.
23:16	0x0 RW	**user_defined_pattern_byte2:** Register value of user defined pattern Upper 8 bits are not sent - reserved.
15:8	0x0 RW	**user_defined_pattern_byte1:** Register value of user defined pattern

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**user_defined_pattern_byte0:** Register value of user defined pattern

7.5.21 reg_DFXREG4_type (DFXREG4)—Offset F050h

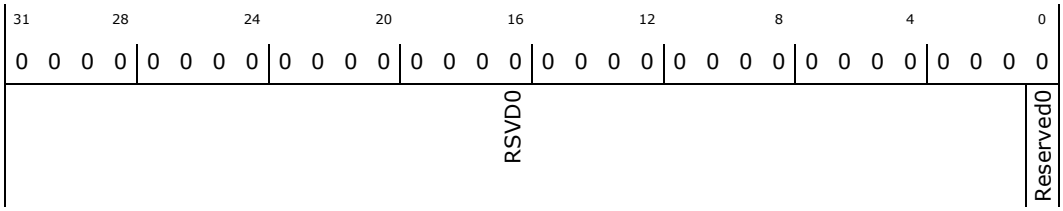
DFXREG4

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F050h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RO	**Reserved0:** reserved.

7.5.22 reg_DFXREG5_type (DFXREG5)—Offset F054h

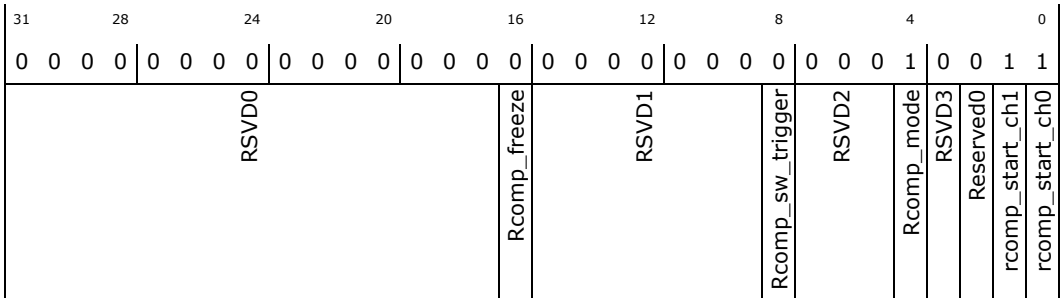
DFXREG5

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F054h

Default: 00000013h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RSVD0:** Reserved
16	0x0 RW	**Rcomp_freeze:** Writing 1'b1 will cause RCOMP FSM and controller to freeze at the point in the FSM. It wont respond to AFE.
15:9	0x0 RO	**RSVD1:** Reserved
8	0x0 RW	**Rcomp_sw_trigger:** 1'b1 trigger's RCOMP FSM via software. Write 0 to clear it.
7:5	0x0 RO	**RSVD2:** Reserved
4	0x1 RW	**Rcomp_mode:** 1: AUTO-RCOMP mode. 0: SW-RCOMP
3	0x0 RO	**RSVD3:** Reserved
2	0x0 RO	**Reserved0:** reserved.
1	0x1 RW	**rcomp_start_ch1:** This bit set would indicate the RCOMP to be enabled. Setting it to zero, RCOMP would be turned off for channle1.
0	0x1 RW	**rcomp_start_ch0:** This bit set would indicate the RCOMP to be enabled. Setting it to zero, RCOMP would be turned off for channel0

7.5.23 reg_DFXREG6_type (DFXREG6)—Offset F058h

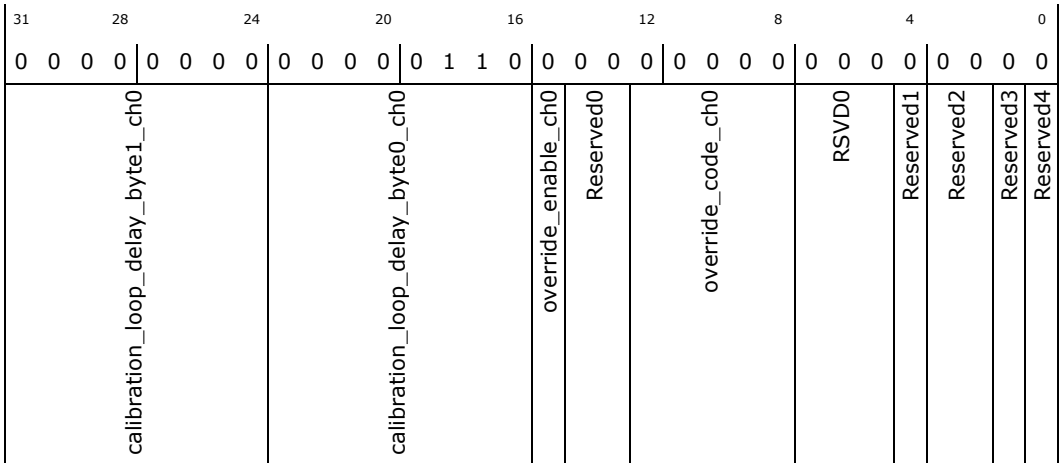
DFXREG6

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F058h

Default: 00060000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**calibration_loop_delay_byte1_ch0:** Specifies number of clock cycles to be used for sampling the upcount from AFE.
23:16	0x6 RW	**calibration_loop_delay_byte0_ch0:** Specifies number of clock cycles to be used for sampling the upcount from AFE.
15	0x0 RW	**override_enable_ch0:** Rcomp override enable for CH0
14:13	0x0 RO	**Reserved0:** reserved.
12:8	0x0 RW	**override_code_ch0:** Rcomp override code for CH0
7:5	0x0 RO	**RSVD0:** Reserved
4	0x0 RO	**Reserved1:** reserved.
3:2	0x0 RO	**Reserved2:** reserved.
1	0x0 RO	**Reserved3:** reserved.
0	0x0 RO	**Reserved4:** reserved.

7.5.24 reg_DFXREG7_type (DFXREG7)—Offset F05Ch

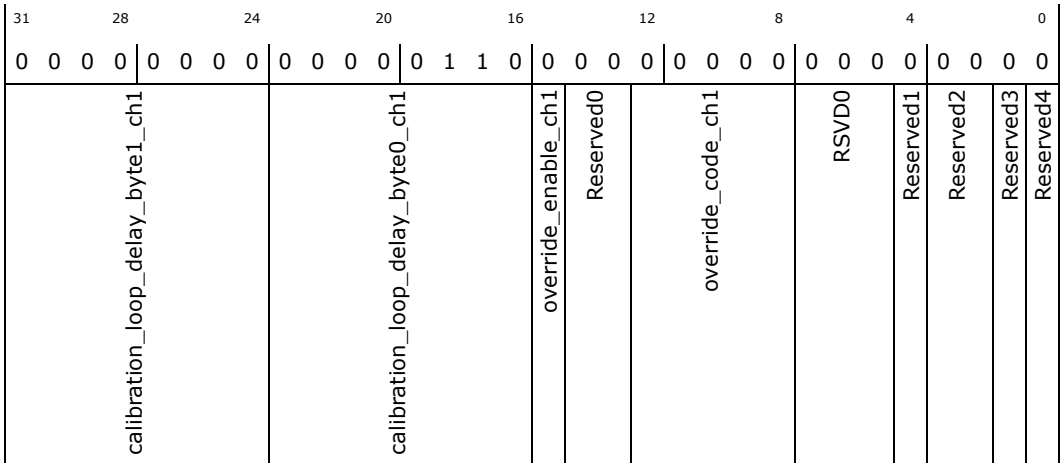
DFXREG7

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F05Ch

Default: 00060000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**calibration_loop_delay_byte1_ch1:** Specifies number of clock cycles to be used for sampling the upcount from AFE.
23:16	0x6 RW	**calibration_loop_delay_byte0_ch1:** Specifies number of clock cycles to be used for sampling the upcount from AFE.
15	0x0 RW	**override_enable_ch1:** Rcomp override enable for CH1
14:13	0x0 RO	**Reserved0:** reserved.
12:8	0x0 RW	**override_code_ch1:** Rcomp override code for CH1
7:5	0x0 RO	**RSVD0:** Reserved
4	0x0 RO	**Reserved1:** reserved.
3:2	0x0 RO	**Reserved2:** reserved.
1	0x0 RO	**Reserved3:** reserved.
0	0x0 RO	**Reserved4:** reserved.

7.5.25 reg_DFXREG8_type (DFXREG8)—Offset F060h

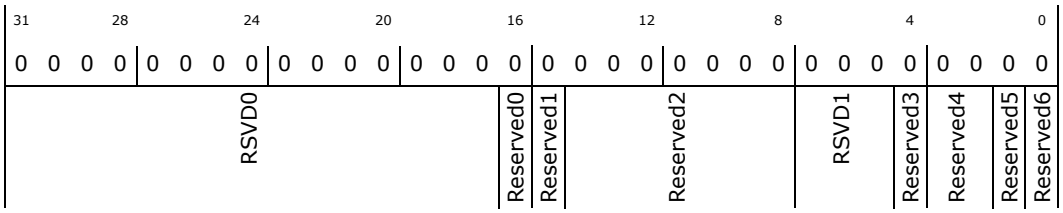
DFXREG8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F060h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RSVD0:** Reserved
16	0x0 RO	**Reserved0:** reserved.
15	0x0 RO	**Reserved1:** reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:8	0x0 RO	**Reserved2:** reserved.
7:5	0x0 RO	**RSVD1:** Reserved
4	0x0 RO	**Reserved3:** reserved.
3:2	0x0 RO	**Reserved4:** reserved.
1	0x0 RO	**Reserved5:** reserved.
0	0x0 RO	**Reserved6:** reserved.

7.5.26 reg_DFXREG9_type (DFXREG9)—Offset F064h

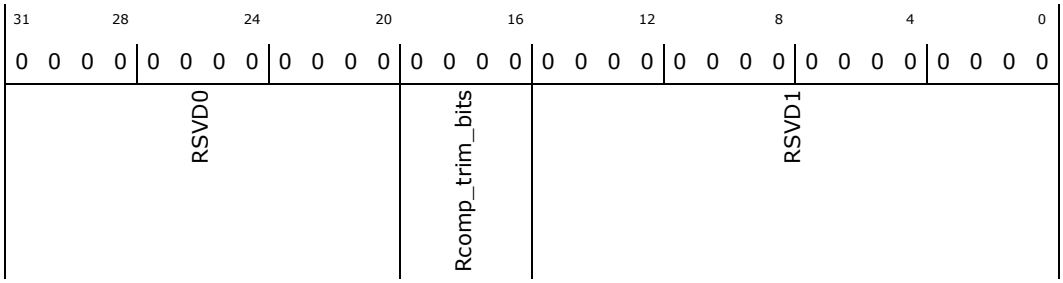
DFXREG9

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F064h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RSVD0:** Reserved
19:16	0x0 RW	**Rcomp_trim_bits:** select reference voltage for RCOMP comparator. Adjustments for +5,+10 or -5 %.
15:0	0x0 RO	**RSVD1:** Reserved

7.5.27 reg_DFXREG10_type (DFXREG10)—Offset F068h

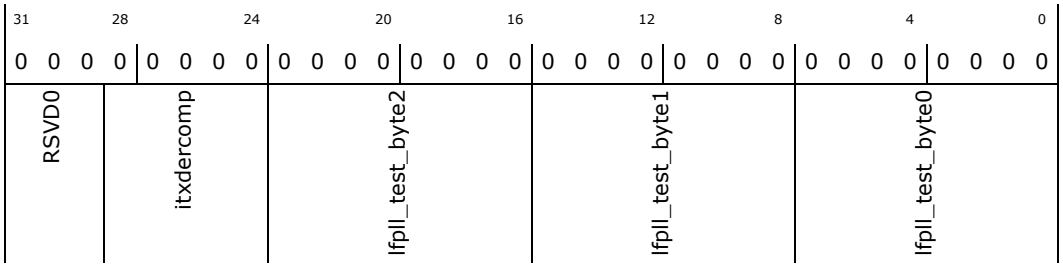
DFXREG10

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F068h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD0:** Reserved
28:24	0x0 RW	**itxdercomp:** de-emphasis RCOMP codes
23:16	0x0 RW	**lfpll_test_byte2:** LFPLL Test Control Placeholder coarseovrd and fineovrd and dcoovrd[15:0] and viewsel[2:0].
15:8	0x0 RW	**lfpll_test_byte1:** LFPLL Test Control Placeholder coarseovrd and fineovrd and dcoovrd[15:0] and viewsel[2:0].
7:0	0x0 RW	**lfpll_test_byte0:** LFPLL Test Control Placeholder coarseovrd and fineovrd and dcoovrd[15:0] and viewsel[2:0].

7.5.28 reg_DFXREG11_type (DFXREG11)—Offset F06Ch

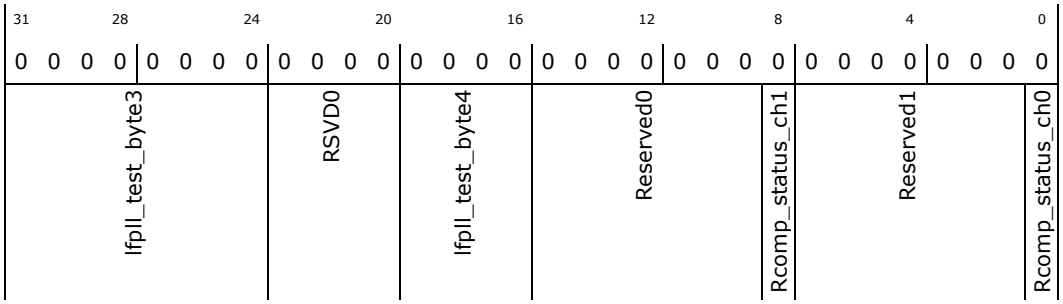
DFXREG11

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F06Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**lfpll_test_byte3:** LFPLL test placeholder.
23:20	0x0 RO	**RSVD0:** Reserved
19:16	0x0 RW	**lfpll_test_byte4:** LFPLL test placeholder.
15:9	0x0 RO	**Reserved0:** reserved.
8	0x0 RW/1C	**Rcomp_status_ch1:** Poll for 1'b1 to check if Rcomp is done. write 1 to clear.
7:1	0x0 RO	**Reserved1:** reserved.
0	0x0 RW/1C	**Rcomp_status_ch0:** Poll for 1'b1 to check if Rcomp is done. write 1 to clear.

7.5.29 reg_DFXREG12_type (DFXREG12)—Offset F070h

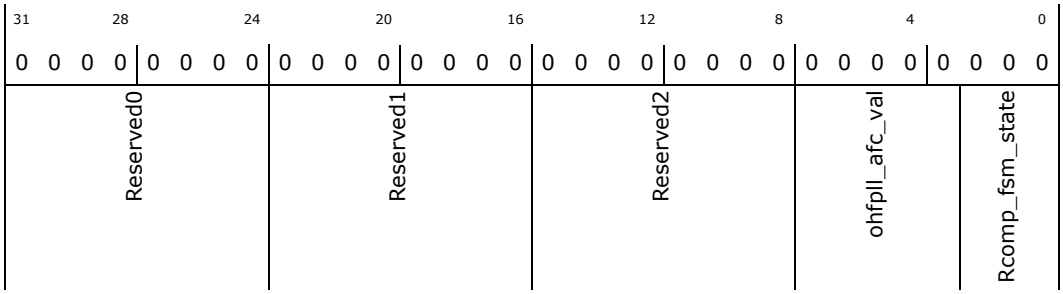
DFXREG12

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F070h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** reserved.
23:16	0x0 RO	**Reserved1:** reserved.
15:8	0x0 RO	**Reserved2:** reserved.
7:3	0x0 RO	**ohfpll_afc_val:** AFC lock values. When the AFC is enabled, the AFC value after PLL locked is captured here and can be read out for debug purposes

Bit Range	Default & Access	Field Name (ID): Description
2:0	0x0 RO	**Rcomp_fsm_state:** Read out Rcomp FSM current state. RCOMP FSM State 3'b000 = s_RCOMP_FSM_IDLE 3'b001 = s_RCOMP_CALIB_LOOP_TIMER 3'b010 = s_RCOMP_SAMPLE_UPCOUNT 3'b011 = s_RCOMP_INCR_CODE 3'b100 = s_RCOMP_FSM_DONE_TIMER OTHERS = Return to s_RCOMP_FSM_IDLE

7.5.30 reg_CMNREG17_type (CMNREG17)—Offset F074h

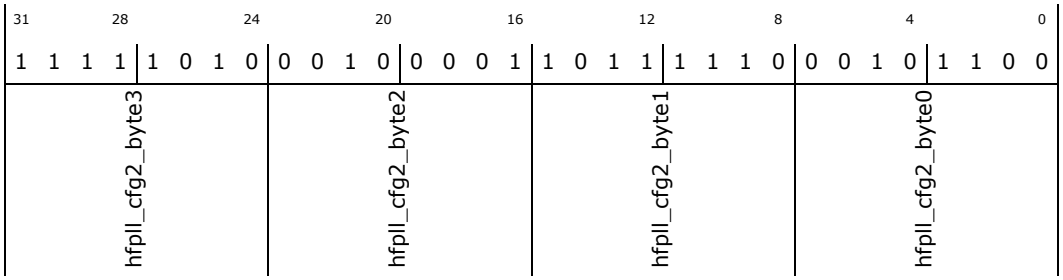
CMNREG17

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F074h

Default: FA21BE2Ch



Bit Range	Default & Access	Field Name (ID): Description
31:24	0xfa RW	**hfpll_cfg2_byte3:** HFPLL configuration register as required by AFE bits [63:32]. 19.2MHz Rate A: 0x45 19.2MHz Rate B: 0x7C 26MHz Rate A: 0xF0 26MHz Rate B: 0x18 25MHz Rate A: 0xFA 25MHz Rate B: 0x2C
23:16	0x21 RW	**hfpll_cfg2_byte2:** HFPLL configuration register as required by AFE bits [63:32]. Always 0x01
15:8	0xbe RW	**hfpll_cfg2_byte1:** HFPLL configuration register as required by AFE bits [63:32]. Always 0xAC
7:0	0x2c RW	**hfpll_cfg2_byte0:** HFPLL configuration register as required by AFE bits [63:32]. Adjust lock threshold. 0x0C normally. 0x0D during debug.

7.5.31 reg_CMNREG18_type (CMNREG18)—Offset F078h

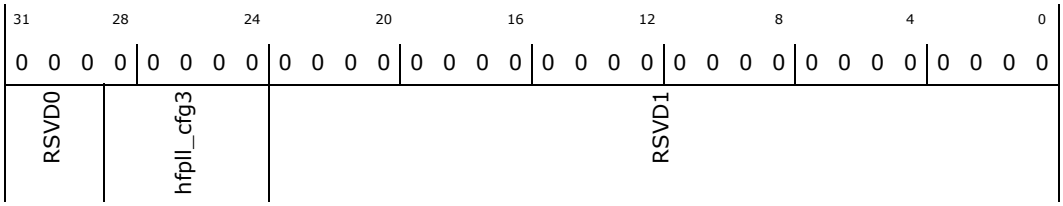
CMNREG18

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F078h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD0:** Reserved
28:24	0x0 RW	**hfpll_cfg3:** HFPLL configuration register as required by AFE bits [67:64]. 19.2MHz Rate A: 0x1 19.2MHz Rate B: 0x1 26MHz Rate A: 0 26MHz Rate B: 0x1 25MHz Rate A: 0 25MHz Rate B: 0x1
23:0	0x0 RO	**RSVD1:** Reserved

7.5.32 reg_CMNREG19_type (CMNREG19)—Offset F07Ch

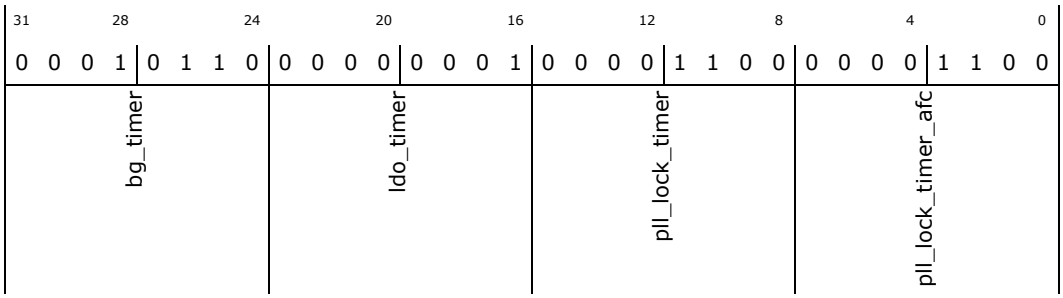
CMNREG19

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F07Ch

Default: 16010C0Ch



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x16 RW	**bg_timer:** Band gap timer. Counts in multiple of 32 reference clock cycles. Though BG is not present in ANN, the timer delay is still honored.
23:16	0x1 RW	**ldo_timer:** LDO timer. Counts in 1us granularity. Though LDO is not present in SoC, the timer delay is still honored.
15:8	0xc RW	**pll_lock_timer:** PLL lock timer without the AFC counter enabled. Counts in 1us granularity
7:0	0xc RW	**pll_lock_timer_afc:** PLL lock timer with the AFC counter enabled. Counts in 1us granularity

7.5.33 reg_CMNREG20_type (CMNREG20)—Offset F080h

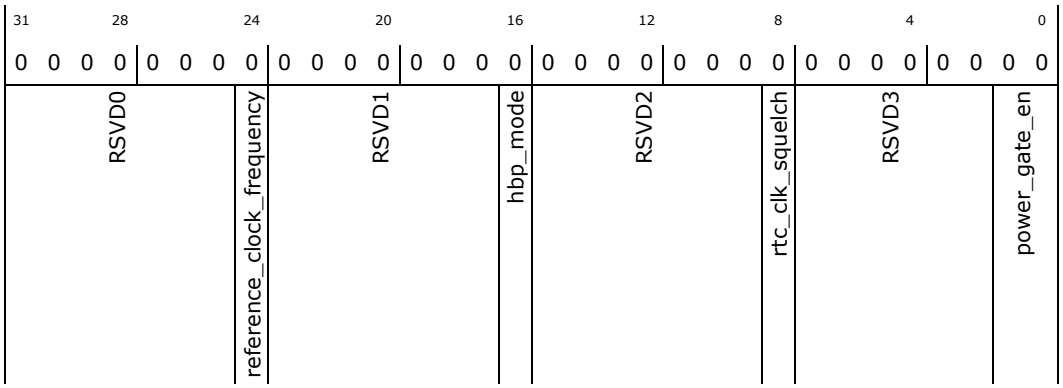
CMNREG20

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F080h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**reference_clock_frequency:** 1'b0 - 19.2 MHz reference clock;; 1'b1 - 26 MHz reference clock
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RW	**hbp_mode:** HBP Mode clocking. The MaxHSClk will be set to 500 MHz when HBP mode is enabled. The MaxHSClk gating should be disabled in this mode.
15:9	0x0 RO	**RSVD2:** Reserved
8	0x0 RW	**rtc_clk_squelch:** The squelch detection circuit in data lane RX will use the RTC clk (32 KHz) instead of the local ring oscillator
7:2	0x0 RO	**RSVD3:** Reserved
1:0	0x0 RW	**power_gate_en:** Enable Power gating [0] - Common Lane core power gating; [1] - Common Lane SUS power gating enable.

7.5.34 reg_CMNREG21_type (CMNREG21)—Offset F084h

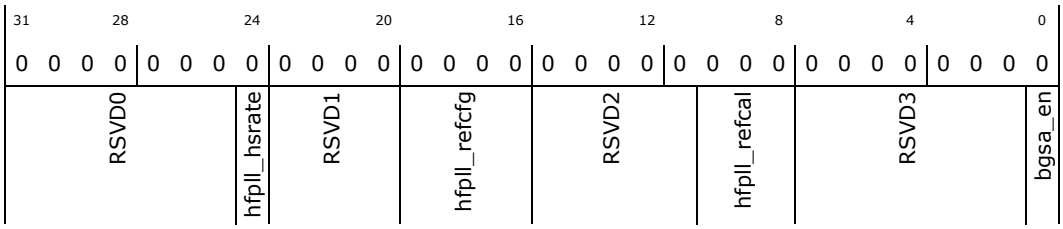
CMNREG21

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD + F000h] + F084h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**hfpll_hsrate:** 1=Rate A, 0=Rate B
23:20	0x0 RO	**RSVD1:** Reserved
19:16	0x0 RW	**hfpll_refcfg:** NA
15:11	0x0 RO	**RSVD2:** Reserved
10:8	0x0 RW	**hfpll_refcal:** PLL Reference current amplitude select
7:1	0x0 RO	**RSVD3:** Reserved
0	0x0 RW	**bgsa_en:** Enables small amplitude mode for BG on SoC. Selects small amplitude reference voltage in voltage divider in ANN.

7.5.35 reg_CMNREG22_type (CMNREG22)—Offset F088h

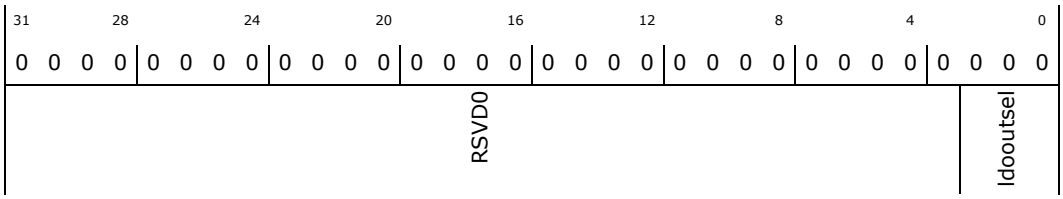
CMNREG22

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

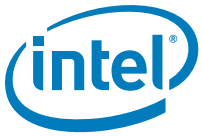
Offset: [TBD + F000h] + F088h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
2:0	0x0 RW	**ldooutsel:** LDO output fine tuning setting. Step size = ~10mV.



7.6 USB3 Memory Mapped RX Registers

Table 42. Summary of Memory Mapped I/O Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
80–83h	4	"reg_RXCAPREG1_type (RXCAPREG1)—Offset 80h" on page 2953	00020100h
84–87h	4	"reg_RXCAPREG2_type (RXCAPREG2)—Offset 84h" on page 2953	0F010005h
88–8Bh	4	"reg_RXCAPREG3_type (RXCAPREG3)—Offset 88h" on page 2954	44017D08h
8C–8Fh	4	"reg_RXCAPREG4_type (RXCAPREG4)—Offset 8Ch" on page 2955	01070804h
90–93h	4	"reg_RXCAPREG5_type (RXCAPREG5)—Offset 90h" on page 2956	15010020h
94–97h	4	"reg_RXCAPREG6_type (RXCAPREG6)—Offset 94h" on page 2957	04044645h
A0–A3h	4	"reg_RXREG2_type (RXREG2)—Offset A0h" on page 2958	01020100h
A4–A7h	4	"reg_RXREG3_type (RXREG3)—Offset A4h" on page 2959	0F000001h
A8–ABh	4	"reg_RXREG4_type (RXREG4)—Offset A8h" on page 2960	00000000h
C0–C3h	4	"reg_RXREG5_type (RXREG5)—Offset C0h" on page 2961	00000000h

7.6.1 reg_RXCAPREG1_type (RXCAPREG1)—Offset 80h

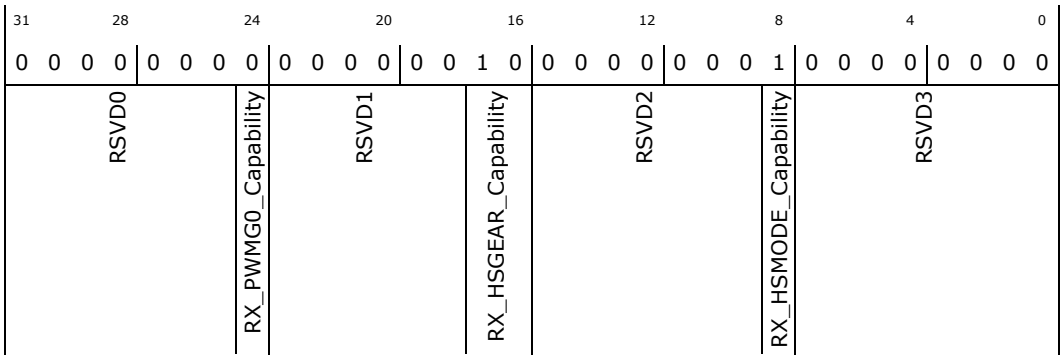
RXCAPREG1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 80h

Default: 00020100h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**RX_PWMG0_Capability:** Specifies support for PWM-G0. NO = 0, YES = 1
23:18	0x0 RO	**RSVD1:** Reserved
17:16	0x2 RW	**RX_HSGEAR_Capability:** Specifies supported HS-GEARs. Existence depends on: RX_HSMODE_Capability HS_G1_ONLY = 1, HS_G1_TO_G2 = 2, HS_G1_TO_G3 = 3
15:9	0x0 RO	**RSVD2:** Reserved
8	0x1 RW	**RX_HSMODE_Capability:** Specifies support for HS-MODE. FALSE = 0, TRUE = 1
7:0	0x0 RO	**RSVD3:** Reserved

7.6.2 reg_RXCAPREG2_type (RXCAPREG2)—Offset 84h

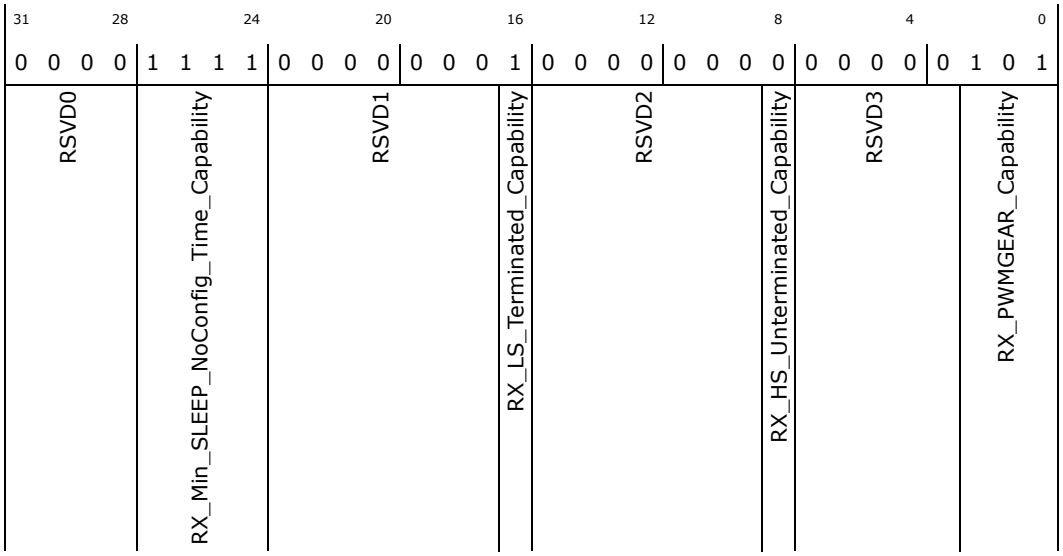
RXCAPREG2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 84h

Default: 0F010005h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RSVD0:** Reserved
27:24	0xf RW	**RX_Min_SLEEP_NoConfig_Time_Capability:** Specifies minimum time(in SI) in SLEEP state needed when inline configuration was not performed. 1 to 15
23:17	0x0 RO	**RSVD1:** Reserved
16	0x1 RW	**RX_LS_Terminated_Capability:** Specifies support for enabling resistive termination in LS-MODE. NO = 0, YES = 1
15:9	0x0 RO	**RSVD2:** Reserved
8	0x0 RW	**RX_HS_Unterminated_Capability:** Specifies support for disconnection of resistive termination in HS-MODE. Existence depends on: RX_HSMODE_Capability NO = 0, YES = 1
7:3	0x0 RO	**RSVD3:** Reserved
2:0	0x5 RW	**RX_PWMGEAR_Capability:** Specifies supported PWM-GEARs other than PWM-G0. PWM_G1_ONLY = 1, PWM_G1_TO_G2 = 2, PWM_G1_TO_G3 = 3, PWM_G1_TO_G4 = 4, PWM_G1_TO_G5 = 5, PWM_G1_TO_G6 = 6, PWM_G1_TO_G7 = 7

7.6.3 reg_RXCAPREG3_type (RXCAPREG3)—Offset 88h

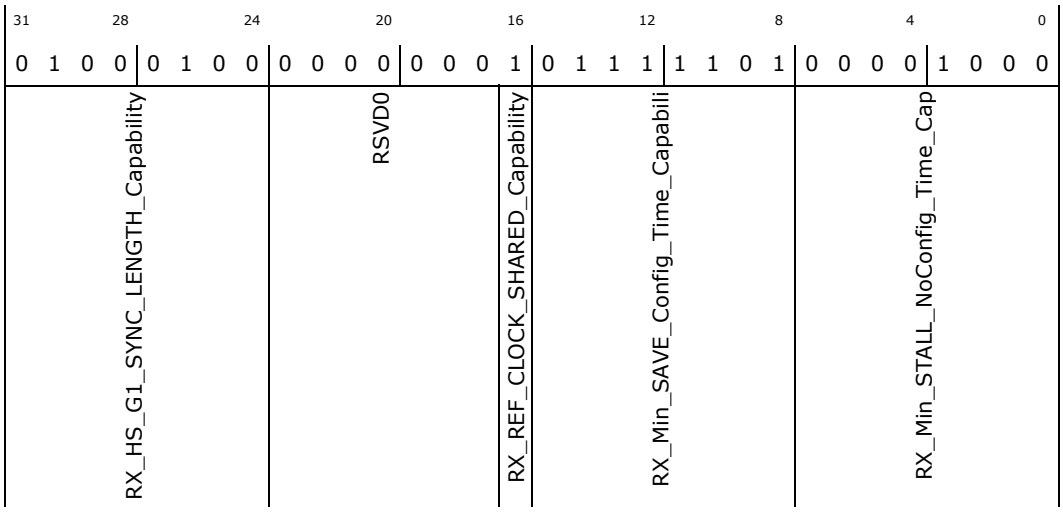
RXCAPREG3

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 88h

Default: 44017D08h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x44 RW	**RX_HS_G1_SYNC_LENGTH_Capability:** High Speed GEAR 1 Synchronization pattern length in SI. Existence depends on: RX_HSMODE_Capability B[7:6] SYNC_range FINE = 0, COARSE = 1 B[5:0] SYNC_length 1 to 15 for FINE, 0 to 15 for COARSE
23:17	0x0 RO	**RSVD0:** Reserved
16	0x1 RW	**RX_REF_CLOCK_SHARED_Capability:** Specifies support for a shared reference clock. B[0] NO = 0, YES = 1
15:8	0x7d RW	**RX_Min_SAVE_Config_Time_Capabili:** (Spec Name, RX_Min_SAVE_Config_Time_Capability) Specifies minimum reconfiguration time (in 40 ns steps). This applies only to SLEEP and STALL states. Both Int B[7:0] 1 to 250 (10000 ns) RX_REF_CLOCK_SHARED_Capability 0x8A Specifies support for a shared reference clock. NO = 0, YES = 1
7:0	0x8 RW	**RX_Min_STALL_NoConfig_Time_Cap:** (Spec Name RX_Min_STALL_NoConfig_Time_Capability) Specifies minimum time(in SI) in STALL state needed when inline configuration was not performed. 1 to 255

7.6.4 reg_RXCAPREG4_type (RXCAPREG4)—Offset 8Ch

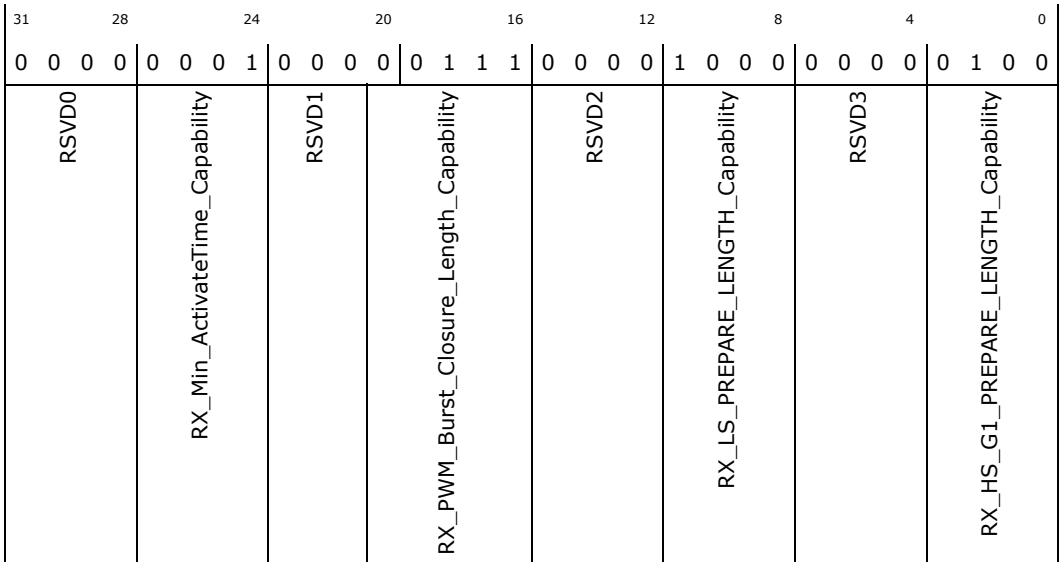
RXCAPREG4

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 8Ch

Default: 01070804h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RSVD0:** Reserved
27:24	0x1 RW	**RX_Min_ActivateTime_Capability:** Specifies minimum activate time needed in 100s steps. B[3:0] 1 to 9
23:21	0x0 RO	**RSVD1:** Reserved
20:16	0x7 RW	**RX_PWM_Burst_Closure_Length_Capability:** Specifies minimum burst closure time (in SI) necessary to guarantee complete data processing inside M-RX. B[4:0] 0 to 31
15:12	0x0 RO	**RSVD2:** Reserved
11:8	0x8 RW	**RX_LS_PREPARE_LENGTH_Capability:** PWM-BURST or SYS-BURST PREPARE length multiplier for M-RX. B[3:0]0 to 15
7:4	0x0 RO	**RSVD3:** Reserved
3:0	0x4 RW	**RX_HS_G1_PREPARE_LENGTH_Capability:** HS-G1 PREPARE length multiplier for M-RX. Existence depends on: RX_HSMODE_Capability B[3:0] 0 to 15

7.6.5 reg_RXCAPREG5_type (RXCAPREG5)—Offset 90h

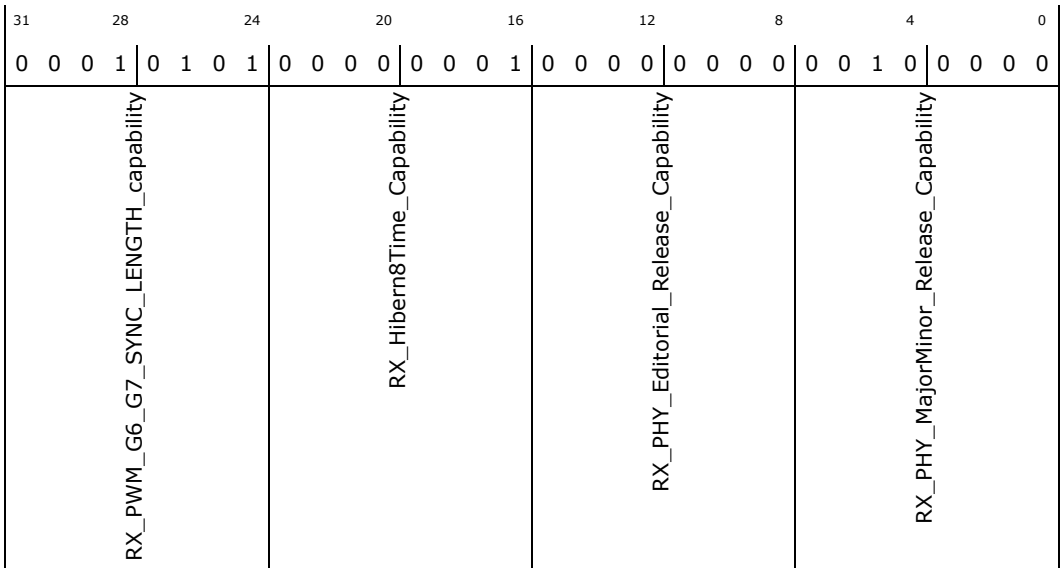
RXCAPREG5

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 90h

Default: 15010020h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x15 RW	**RX_PWM_G6_G7_SYNC_LENGTH_capability:** Synchronization pattern length, in SI, for PWM-G6 and PWM-G7 in LS-MODE . Existence depends on: RX_PWMGEAR_Capability B[7:6] SYNC_range FINE = 0, COARSE = 1 B[5:0] SYNC_length 0 to 15
23:16	0x1 RW	**RX_Hibern8Time_Capability:** Specifies minimum time (in 100s steps) in HIBERN8 state. B[7:0] 1 to 128 (100s to 12.8 ms)
15:8	0x0 RW	**RX_PHY_Editorial_Release_Capability:** Specifies the sequence number of the M-PHY version supported by the M-RX. B[7:0] 1 to 99
7:0	0x20 RW	**RX_PHY_MajorMinor_Release_Capability:** Specifies the major and minor numbers of the M-PHY version supported by the M-RX. B[7:4] Major version number, 0 to 9 B[3:0] Minor version number, 0 to 9

7.6.6 reg_RXCAPREG6_type (RXCAPREG6)—Offset 94h

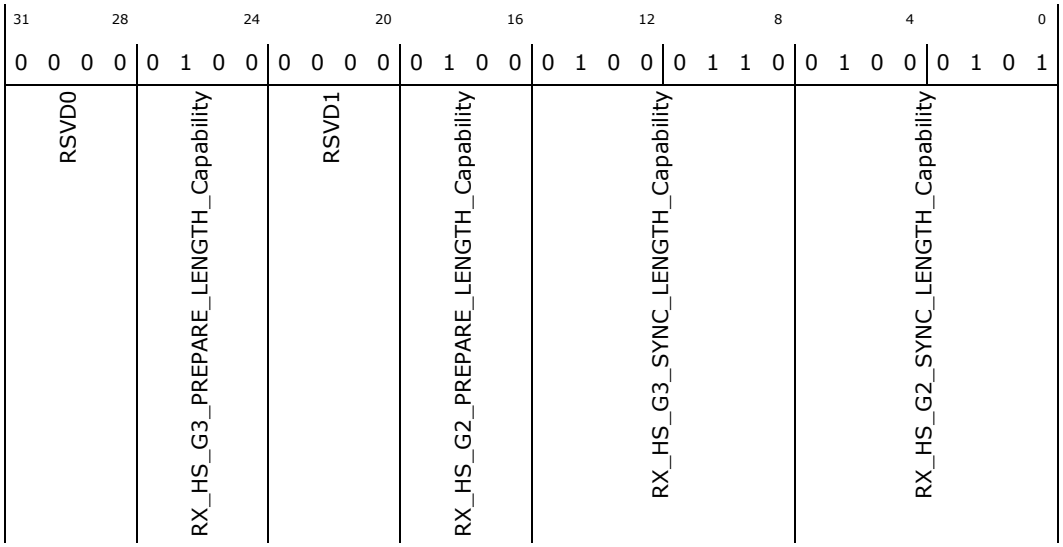
RXCAPREG6

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 94h

Default: 04044645h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RSVD0:** Reserved
27:24	0x4 RW	**RX_HS_G3_PREPARE_LENGTH_Capability:** HS-G3 PREPARE length multiplier for M-RX. Existence depends on: RX_HSGEAR_Capability B[3:0] 0 to 15
23:20	0x0 RO	**RSVD1:** Reserved
19:16	0x4 RW	**RX_HS_G2_PREPARE_LENGTH_Capability:** HS-G2 PREPARE length multiplier for M-RX. Existence depends on: RX_HSGEAR_Capability B[3:0] 0 to 15
15:8	0x46 RW	**RX_HS_G3_SYNC_LENGTH_Capability:** High Speed GEAR 3Synchronization pattern length in SI. Existence depends on: RX_HSGEAR_Capability B[7:6] SYNC_range FINE = 0, COARSE = 1 B[5:0] SYNC_length 1 to 15 for FINE, 0 to 15 for COARSE
7:0	0x45 RW	**RX_HS_G2_SYNC_LENGTH_Capability:** High Speed GEAR 2 Synchronization pattern length in SI. Existence depends on: RX_HSGEAR_Capability B[7:6] SYNC_range FINE = 0, COARSE = 1 B[5:0] SYNC_length 1 to 15 for FINE, 0 to 15 for COARSE

7.6.7 reg_RXREG2_type (RXREG2)—Offset A0h

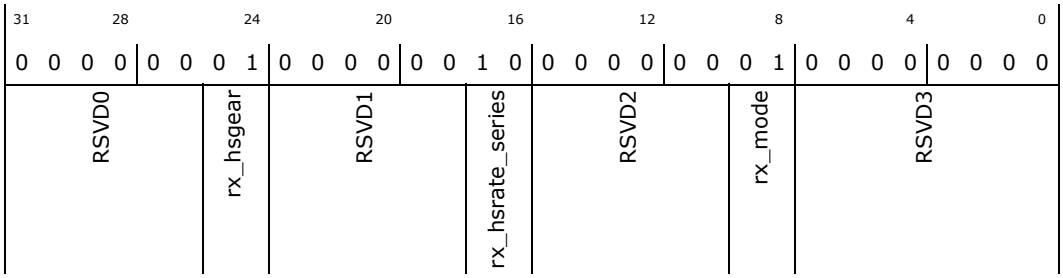
RXREG2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + A0h

Default: 01020100h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD0:** Reserved
25:24	0x1 RW	**rx_hsgear:** Current HS-GEAR. Existence depends on: RX_HSMODE_Capability Value depends on: RX_HSGEAR_Capability Reqd Value: HS_G1 Reset Value: HS_G1 B[1:0] HS_G1 = 1, HS_G2 = 2, HS_G3 = 3
23:18	0x0 RO	**RSVD1:** Reserved
17:16	0x2 RW	**rx_hsrate_series:** HS mode RATE series value. Existence depends on: RX_HSMODE_Capability Reqd Values: A and B Reset Value: A B[1:0] A = 1, B = 2
15:10	0x0 RO	**RSVD2:** Reserved
9:8	0x1 RW	**rx_mode:** Operating mode. Existence depends on: RX_HSMODE_Capability Reqd Value: LS_MODE Reset Value: LS_MODE B[1:0] LS_MODE = 1, HS_MODE = 2
7:0	0x0 RO	**RSVD3:** Reserved

7.6.8 reg_RXREG3_type (RXREG3)—Offset A4h

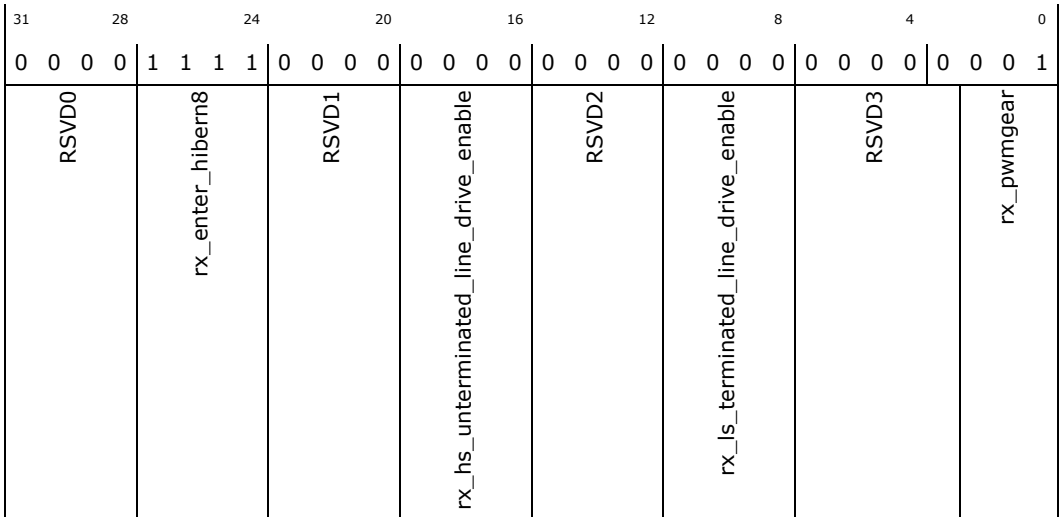
RXREG3

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + A4h

Default: 0F000001h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RSVD0:** Reserved
27:24	0xf RW	**rx_enter_hibern8:** M-RX entry to HIBERN8 state control. Reqd Values: YES, NO Reset Value: YES for Local RESET, NO for LINE-RESET B[0] NO = 0: Protocol Layer shall not set the value of this attribute to NO. When the M-RX is in HIBERN8 state, upon squelch detection the M-RX exits HIBERN8 state (to SLEEP or STALL state) and resets this attribute value to NO, YES = 1: Can be set by the Protocol. The M-RX enters from SLEEP or STALL state to HIBERN8 state, if it is not already in HIBERN8 state.
23:20	0x0 RO	**RSVD1:** Reserved
19:16	0x0 RW	**rx_hs_unterminated_line_drive_enable:** Reserved.
15:12	0x0 RO	**RSVD2:** Reserved
11:8	0x0 RW	**rx_ls_terminated_line_drive_enable:** Reserved.
7:3	0x0 RO	**RSVD3:** Reserved
2:0	0x1 RW	**rx_pwmgear:** Current PWM-GEAR. Reqd Value: PWM_G1 Reset Value: PWM_G1 B[2:0] PWM_G0 = 0, PWM_G1 = 1, PWM_G2 = 2, PWM_G3 = 3, PWM_G4 = 4, PWM_G5 = 5, PWM_G6 = 6, PWM_G7 = 7

7.6.9 reg_RXREG4_type (RXREG4)—Offset A8h

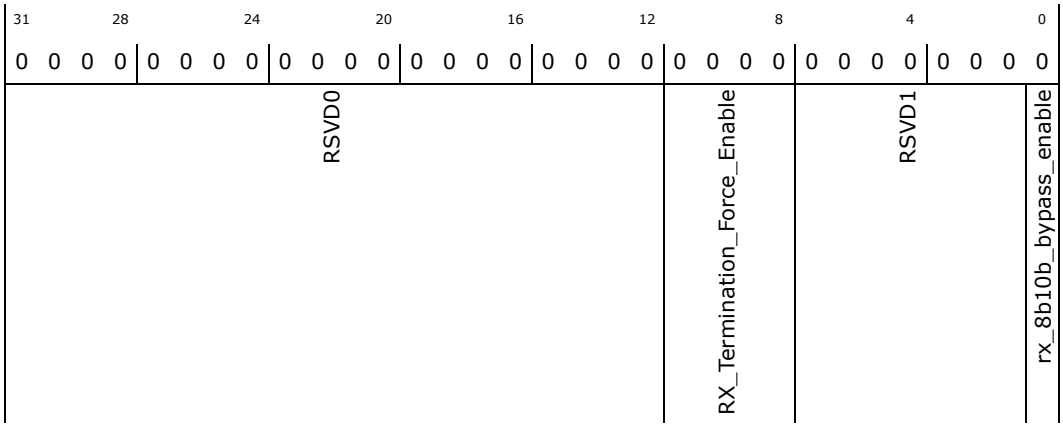
RXREG4

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RSVD0:** Reserved
11:8	0x0 RW	**RX_Termination_Force_Enable:** Force connection of differential termination resistance, RDIF_RX, to enabled state, for RX S-Parameter test purposes. B[0] NO = 0, YES = 1
7:1	0x0 RO	**RSVD1:** Reserved
0	0x0 RW	**rx_8b10b_bypass_enable:** RX_BYPASS_8B10B_Enable Bypass 8b10b Decoding at the M-RX. Reqd Value: FALSE Reset Value: FALSE B[0] FALSE = 0, TRUE = 1

7.6.10 reg_RXREG5_type (RXREG5)—Offset C0h

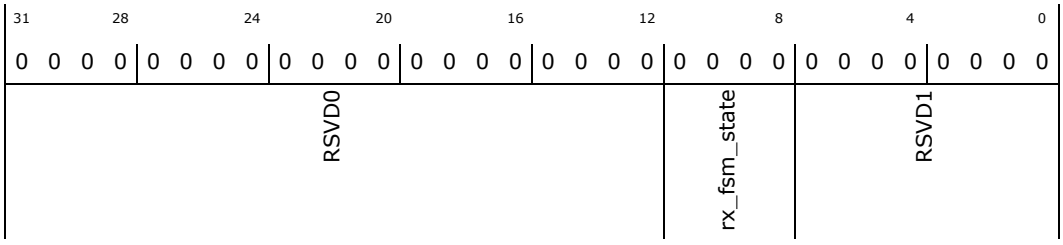
RXREG5

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RSVD0:** Reserved
11:8	0x0 RO	**rx_fsm_state:** To read out the current state of M-RX B[3:0] DISABLED = 0, HIBERN8 = 1, SLEEP = 2, STALL = 3, LS-BURST = 4, HS-BURST = 5, LINE-CFG = 6 LINE-RESET = 7
7:0	0x0 RO	**RSVD1:** Reserved

7.7 USB3 Memory Mapped TX Registers

Table 43. Summary of Memory Mapped I/O Registers—TBD

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"reg_TXCAPREG1_type (TXCAPREG1)—Offset 0h" on page 2965	00020100h
4–7h	4	"reg_TXCAPREG2_type (TXCAPREG2)—Offset 4h" on page 2965	01010305h
8–Bh	4	"reg_TXCAPREG3_type (TXCAPREG3)—Offset 8h" on page 2966	6F080F01h
C–Fh	4	"reg_TXCAPREG4_type (TXCAPREG4)—Offset Ch" on page 2967	01002001h
20–23h	4	"reg_TXREG1_type (TXREG1)—Offset 20h" on page 2968	01020100h
24–27h	4	"reg_TXREG2_type (TXREG2)—Offset 24h" on page 2969	00000201h
28–2Bh	4	"reg_TXREG3_type (TXREG3)—Offset 28h" on page 2970	0F080444h
2C–2Fh	4	"reg_TXREG4_type (TXREG4)—Offset 2Ch" on page 2971	00000701h
30–33h	4	"reg_TXREG5_type (TXREG5)—Offset 30h" on page 2972	01000000h
40–43h	4	"reg_TXREG6_type (TXREG6)—Offset 40h" on page 2973	00000000h

7.7.1 reg_TXCAPREG1_type (TXCAPREG1)—Offset 0h

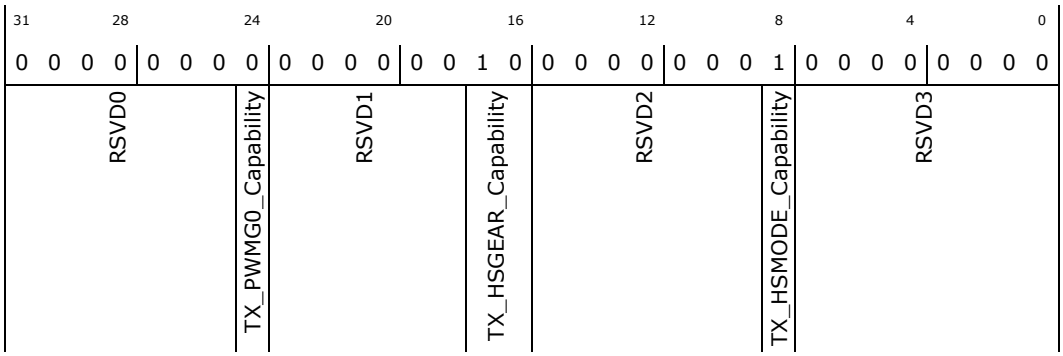
TXCAPREG1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 0h

Default: 00020100h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**TX_PWMG0_Capability:** Specifies support for PWM-G0. NO = 0,YES = 1
23:18	0x0 RO	**RSVD1:** Reserved
17:16	0x2 RW	**TX_HSGEAR_Capability:** TX_HSGEAR_Capability 0x02 Specifies supported HS-GEARs. Existence depends on: TX_HSMODE_Capability. HS_G1_ONLY = 1, HS_G1_TO_G2 = 2, HS_G1_TO_G3 = 3
15:9	0x0 RO	**RSVD2:** Reserved
8	0x1 RW	**TX_HSMODE_Capability:** Specifies support for HS-MODE. FALSE = 0, TRUE = 1
7:0	0x0 RO	**RSVD3:** Reserved

7.7.2 reg_TXCAPREG2_type (TXCAPREG2)—Offset 4h

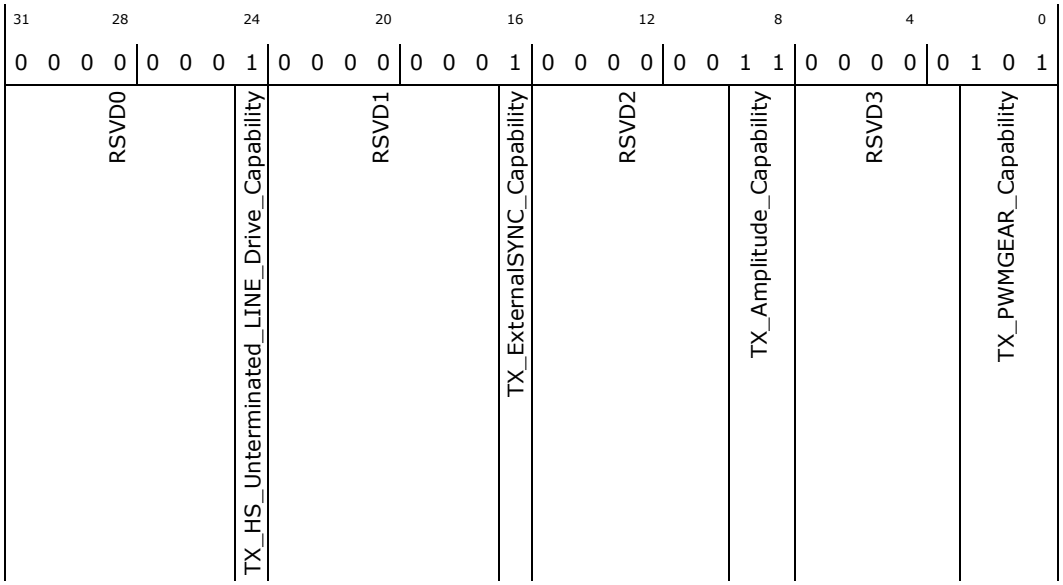
TXCAPREG2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 4h

Default: 01010305h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x1 RW	**TX_HS_Unterminated_LINE_Drive_Capability:** Specifies whether or not M-TX supports driving an unterminated LINE in HS-MODE. Existence depends on:TX_HSMODE_Capability. NO = 0, YES = 1
23:17	0x0 RO	**RSVD1:** Reserved
16	0x1 RW	**TX_ExternalSYNC_Capability:** Specifies support for external SYNC pattern. FALSE = 0, TRUE = 1
15:10	0x0 RO	**RSVD2:** Reserved
9:8	0x3 RW	**TX_Amplitude_Capability:** Specifies supported signal amplitude levels. SMALL_AMPLITUDE_ONLY = 1, LARGE_AMPLITUDE_ONLY = 2, LARGE_AND_SMALL_AMPLITUDE = 3
7:3	0x0 RO	**RSVD3:** Reserved
2:0	0x5 RW	**TX_PWMGEAR_Capability:** Specifies support for PWM-GEARs other than PWM-G0. PWM_G1_ONLY = 1, PWM_G1_TO_G2 = 2, PWM_G1_TO_G3 = 3, PWM_G1_TO_G4 = 4, PWM_G1_TO_G5 = 5, PWM_G1_TO_G6 = 6, PWM_G1_TO_G7 = 7

7.7.3 reg_TXCAPREG3_type (TXCAPREG3)—Offset 8h

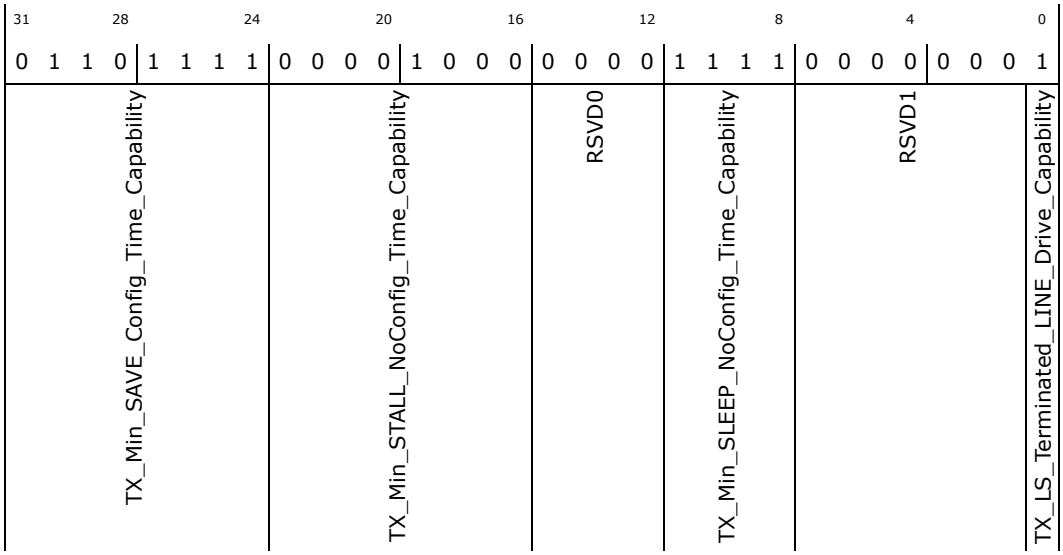
TXCAPREG3

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 8h

Default: 6F080F01h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x6f RW	**TX_Min_SAVE_Config_Time_Capability:** Specifies minimum reconfiguration time (in 40 ns steps) plus an additional 20 SI in the GEAR from which the configuration change was initiated. This applies only to SLEEP and STALL states. 1 to 250 (10000 ns) plus an additional 20 SI
23:16	0x8 RW	**TX_Min_STALL_NoConfig_Time_Capability:** Specifies minimum time (in SI) in STALL state needed when inline configuration was not performed. 1 to 255
15:12	0x0 RO	**RSVD0:** Reserved
11:8	0xf RW	**TX_Min_SLEEP_NoConfig_Time_Capability:** Specifies minimum time (in SI) in SLEEP state needed when inline configuration was not performed. 1 to 15
7:1	0x0 RO	**RSVD1:** Reserved
0	0x1 RW	**TX_LS_Terminated_LINE_Drive_Capability:** Specifies whether or not M-TX supports driving a terminated LINE in LS-MODE. NO = 0, YES = 1

7.7.4 reg_TXCAPREG4_type (TXCAPREG4)—Offset Ch

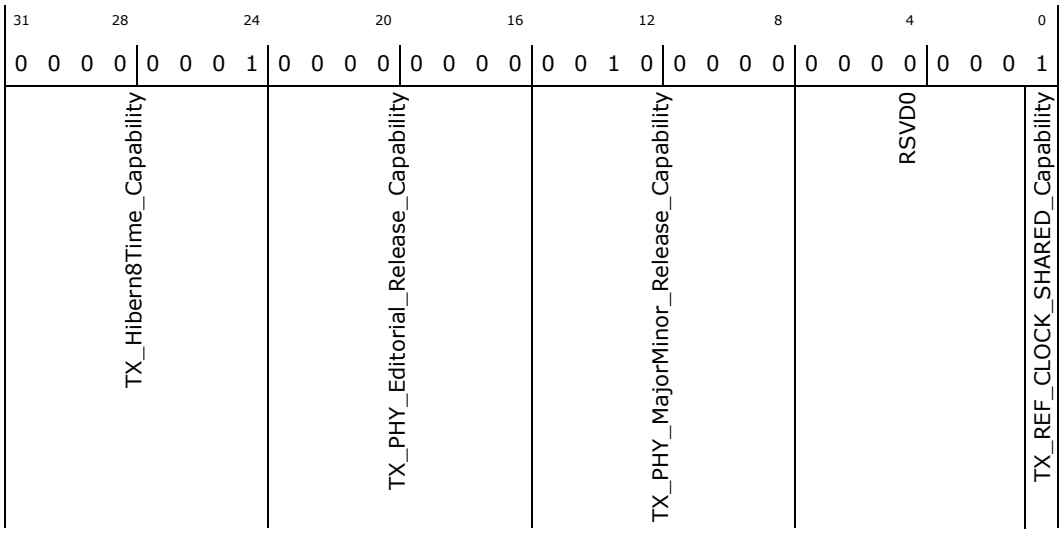
TXCAPREG4

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + Ch

Default: 01002001h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x1 RW	**TX_Hibern8Time_Capability:** Specifies minimum time (in 100s steps) in HIBERN8 state. B[7:0] 1 to 128 (100s to 12.8 ms)
23:16	0x0 RW	**TX_PHY_Editorial_Release_Capability:** Specifies the sequence number of the M-PHY version supported by the M-TX. Both Int B[7:0] 1 to 99
15:8	0x20 RW	**TX_PHY_MajorMinor_Release_Capability:** Specifies the major and minor numbers of the M-PHY version supported by the M-TX. B[7:4] Major version number, 0 to 9 B[3:0] Minor version number, 0 to 9
7:1	0x0 RO	**RSVD0:** Reserved
0	0x1 RW	**TX_REF_CLOCK_SHARED_Capability:** Specifies support for a shared reference clock. NO = 0, YES = 1

7.7.5 reg_TXREG1_type (TXREG1)—Offset 20h

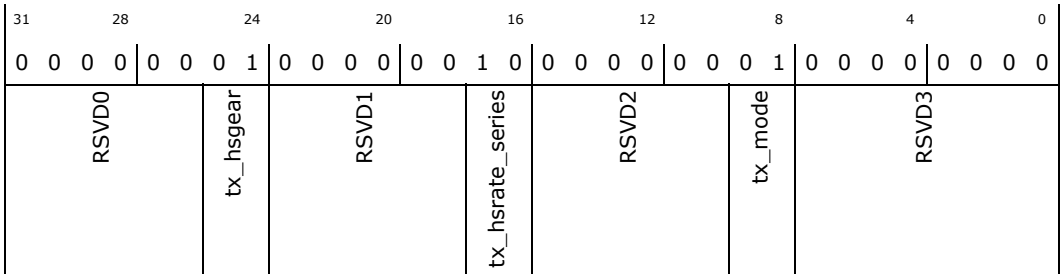
TXREG1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 20h

Default: 01020100h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD0:** Reserved
25:24	0x1 RW	**tx_hsgear:** HS-GEAR value of M-TX. Existence depends on: TX_HSMODE_Capability Value depends on: TX_HSGEAR_Capability Reqd Value: HS_G1 Reset Value: HS_G1 HS_G1 = 1, HS_G2 = 2, HS_G3 = 3
23:18	0x0 RO	**RSVD1:** Reserved
17:16	0x2 RW	**tx_hsrate_series:** HS mode RATE series value of M-TX. Existence depends on: TX_HSMODE_Capability Reqd Value: A and B Reset Value: A A = 1, B = 2
15:10	0x0 RO	**RSVD2:** Reserved
9:8	0x1 RW	**tx_mode:** M-TX operating mode. Existence depends on: TX_HSMODE_Capability Reqd Value: LS_MODE Reset Value: LS_MODE LS_MODE = 1, HS_MODE = 2
7:0	0x0 RO	**RSVD3:** Reserved

7.7.6 reg_TXREG2_type (TXREG2)—Offset 24h

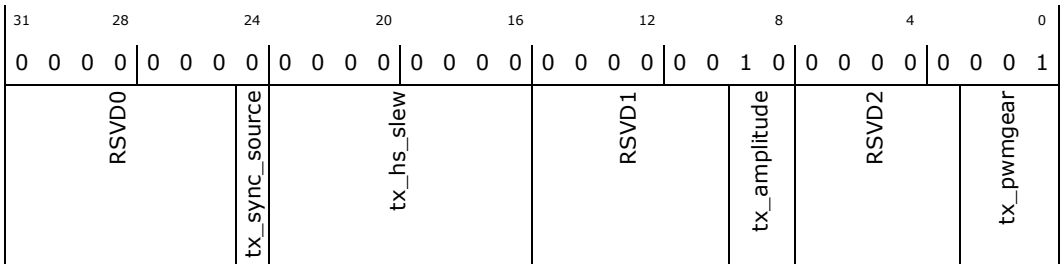
TXREG2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 24h

Default: 00000201h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**tx_sync_source:** Source of synchronization pattern at M-TX. Existence depends on: (TX_HSMODE_Capability OR TX_PWMGEAR_Capability = 6 OR TX_PWMGEAR_Capability = 7) AND TX_ExternalSync_Capability Reqd Value:INTERNAL_SYNC Reset Value:INTERNAL_SYNC INTERNAL_SYNC = 0, EXTERNAL_SYNC = 1
23:16	0x0 RW	**tx_hs_slew:** (Spec Name, TX_HS_SlewRate) Slew Rate control of M-TX output driver. Existence depends on: TX_HSMODE_Capability 0 to 255
15:10	0x0 RO	**RSVD1:** Reserved
9:8	0x2 RW	**tx_amplitude:** Type of drive strength on PINs at M-TX. Value depends on: TX_Amplitude_Capability Reset Value:LARGE_AMPLITUDE 1 SMALL_AMPLITUDE = 1, LARGE_AMPLITUDE = 2
7:3	0x0 RO	**RSVD2:** Reserved
2:0	0x1 RW	**tx_pwmgear:** PWM-GEAR value of M-TX. Value depends on: TX_PWMGEAR_Capability, TX_PWMG0_Capability Reqd Value: PWM_G1 Reset Value: PWM_G1 PWM_G0 = 0, PWM_G1 = 1, PWM_G2 = 2, PWM_G3 = 3, PWM_G4 = 4, PWM_G5 = 5, PWM_G6 = 6, PWM_G7 = 7

7.7.7 reg_TXREG3_type (TXREG3)—Offset 28h

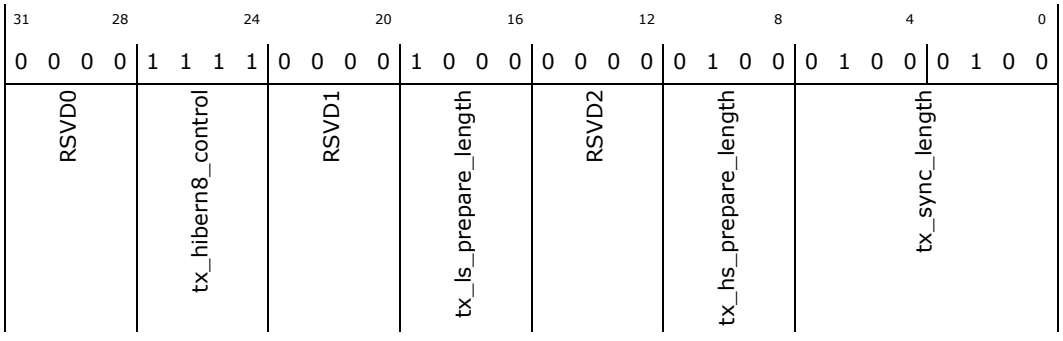
TXREG3

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 28h

Default: 0F080444h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
27:24	0xf RW	**tx_hibern8_control:** M-TX HIBERN8 state control. 1 bit per lane for 4 lanes (EXIT = 0, ENTER = 1)
23:20	0x0 RO	**RSVD1:** Reserved
19:16	0x8 RW	**tx_ls_prepare_length:** PWM-BURST or SYS-BURST PREPARE length multiplier for M-TX. Reqd Values: 0 to 15 Reset Value: 10 0 to 15
15:12	0x0 RO	**RSVD2:** Reserved
11:8	0x4 RW	**tx_hs_prepare_length:** HS PREPARE length multiplier for M-TX. Existence depends on: TX_HSMODE_Capability Reqd Values: 0 to 15 Reset Value: 15 0 to 15
7:0	0x44 RW	**tx_sync_length:** High Speed Synchronization pattern length of M-TX in SI. B[7:6] - 2'h0 Fine: 2'h1 Coarse: B[5:0] - Sync Length

7.7.8 reg_TXREG4_type (TXREG4)—Offset 2Ch

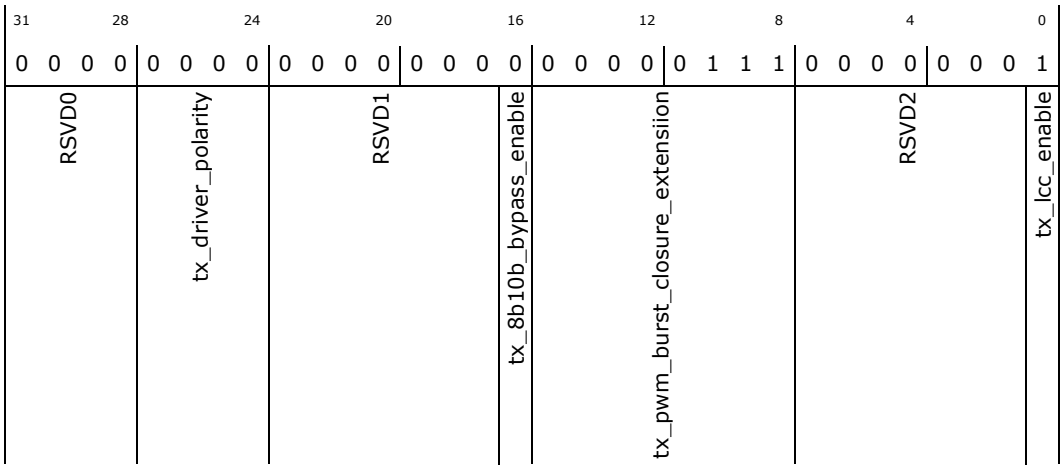
TXREG4

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 2Ch

Default: 00000701h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RSVD0:** Reserved
27:24	0x0 RW	**tx_driver_polarity:** M-TX output driver polarity. Reqd Values: NORMAL, INVERTED Reset Value: NORMAL for local RESET. LINE-RESET shall not reset the value of this attribute. NORMAL = 0, INVERTED = 1

Bit Range	Default & Access	Field Name (ID): Description
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RW	**tx_8b10b_bypass_enable:** (Spec Name, TX_BYPASS_8B10B_Enable) Bypass 8b10b encoding operation at M-TX. Reqd Value: FALSE Reset Value: FALSE FALSE = 0, TRUE = 1
15:8	0x7 RW	**tx_pwm_burst_closure_extensiion:** (Spec Name, TX_PWM_BURST_Closure_Extension) BURST CLOSURE sequence duration in SI. The value shall be greater than, or equal to, the value of RX_PWM_Burst_Closure_Length_Capability. Reqd Values: 0 to 255 Reset Value: 32 0 to 255
7:1	0x0 RO	**RSVD2:** Reserved
0	0x1 RW	**tx_lcc_enable:** LCCs support by the M-TX. Reqd Values: YES, NO Reset Value: YES NO = 0, YES = 1

7.7.9 reg_TXREG5_type (TXREG5)—Offset 30h

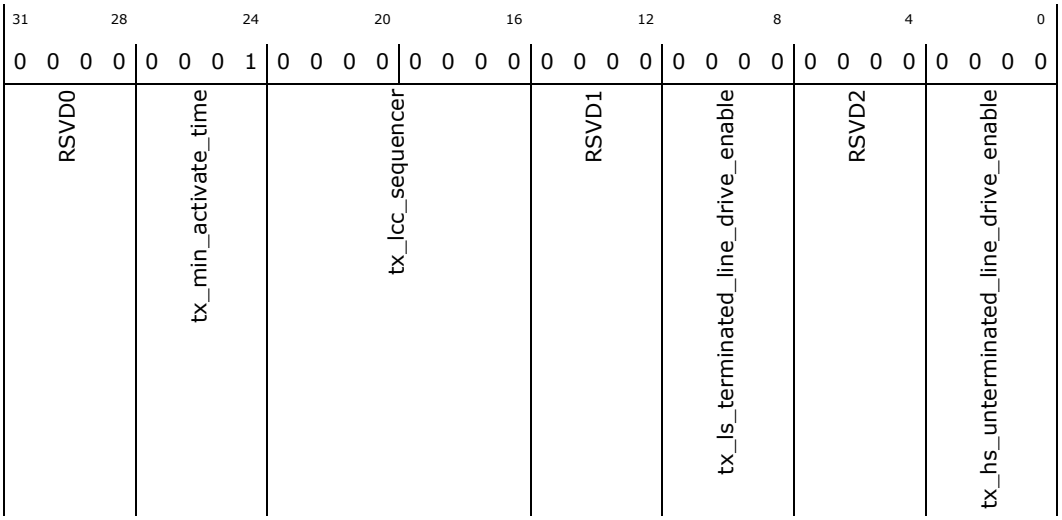
TXREG5

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 30h

Default: 01000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
27:24	0x1 RW	**tx_min_activate_time:** (Spec Name TX_Min_ActivateTime) Specifies minimum activate time needed in 100 s steps. If an OMC is not present, this value must be greater than or equal to the smaller of RX_Min_ActivateTime_Capability or RX_Advanced_Min_ActivateTime_ Capability from the remote M-RX. If an OMC is present, this value must be greater than or equal to the smaller of RX_Min_ActivateTime_Capability + 1 (i.e., the Protocol Layer shall add 100 s when an OMC is present) or RX_Advanced_Min_ActivateTime_Capability + 100 ms. Reset Values: 15 1 to 15
23:16	0x0 RW	**tx_lcc_sequencer:** To set bits for carrying out multiple LCC-READ or LCC-WRITE operations. To perform an LCC operation the corresponding bit for this attribute shall be set. TX_LCC_Sequencer bits are cleared by M-TX when it issues the associated LCC request. Reqd Values: READ-CAPABILITY, READ-MFG-INFO, READ-VEND-INFO, WRITE-ATTRIBUTE Reset Values: 0 (no READ or WRITE operation requested) B[0] = 1: LCC READ-CAPABILITY requested, B[0] = 0: LCC READ-CAPABILITY not requested, B[1] = 1: LCC READ-MFG-INFO requested, B[1] = 0: LCC READ-MFG-INFO not requested, B[2] = 1: LCC READ-VEND-INFO requested, B[2] = 0: LCC READ-VEND-INFO not requested, B[6:3]: Reserved and shall be set to 0b0000, B[7] = 1: LCC WRITE-ATTRIBUTE requested, B[7] = 0: LCC WRITE-ATTRIBUTE not requested.
15:12	0x0 RO	**RSVD1:** Reserved
11:8	0x0 RW	**tx_ls_terminated_line_drive_enable:** Enable M-TX to drive terminated LINE in LS-MODE. Existence depends on: TX_LS_Terminated_LINE_Drive_Capability Reqd Values: NO, YES Reset Value: NO NO = 0, YES = 1
7:4	0x0 RO	**RSVD2:** Reserved
3:0	0x0 RW	**tx_hs_unterminated_line_drive_enable:** Enable M-TX to drive unterminated LINE in HS-MODE. Existence depends on: TX_HSMODE_Capability AND TX_HS_Unterminated_LINE_Drive_Capability Reqd Values: NO, YES Reset Value: NO NO = 0, YES = 1

7.7.10 reg_TXREG6_type (TXREG6)—Offset 40h

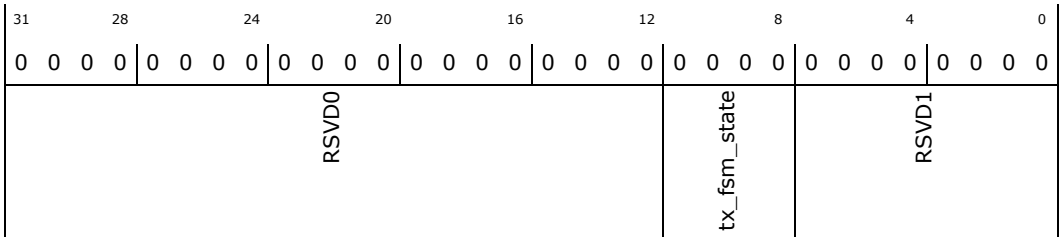
TXREG6

Access Method

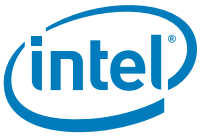
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 40h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RSVD0:** Reserved
11:8	0x0 RO	**tx_fsm_state:** To read out the current state of M-TX DISABLED = 0, HIBERN8 = 1, SLEEP = 2, STALL = 3, LS-BURST = 4, HS-BURST = 5, LINE-CFG = 6 LINE-RESET = 7
7:0	0x0 RO	**RSVD1:** Reserved



7.8 USB3 Memory Mapped Private Registers

Table 44. Summary of Memory Mapped I/O Registers—TBD

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1000–1003h	4	"reg_IMPREG1_type (IMPREG1)—Offset 1000h" on page 2977	00000000h
1004–1007h	4	"reg_IMPREG2_type (IMPREG2)—Offset 1004h" on page 2977	00000000h
1008–100Bh	4	"reg_IMPREG3_type (IMPREG3)—Offset 1008h" on page 2978	FFFF0000h
100C–100Fh	4	"reg_IMPREG4_type (IMPREG4)—Offset 100Ch" on page 2979	10000000h
1010–1013h	4	"reg_IMPREG5_type (IMPREG5)—Offset 1010h" on page 2980	0000020Fh
1014–1017h	4	"reg_IMPREG6_type (IMPREG6)—Offset 1014h" on page 2981	001E0A00h
1018–101Bh	4	"reg_IMPREG7_type (IMPREG7)—Offset 1018h" on page 2981	00030008h
101C–101Fh	4	"reg_IMPREG8_type (IMPREG8)—Offset 101Ch" on page 2982	00000000h
1020–1023h	4	"reg_IMPREG9_type (IMPREG9)—Offset 1020h" on page 2983	00000000h
1024–1027h	4	"reg_IMPREG10_type (IMPREG10)—Offset 1024h" on page 2984	00000000h
1028–102Bh	4	"reg_IMPREG11_type (IMPREG11)—Offset 1028h" on page 2984	0000FFFFh
102C–102Fh	4	"reg_IMPREG12_type (IMPREG12)—Offset 102Ch" on page 2985	0A000000h
1030–1033h	4	"reg_IMPREG13_type (IMPREG13)—Offset 1030h" on page 2986	00000000h
1034–1037h	4	"reg_IMPREG14_type (IMPREG14)—Offset 1034h" on page 2987	00000000h
1038–103Bh	4	"reg_IMPREG15_type (IMPREG15)—Offset 1038h" on page 2988	00000000h
103C–103Fh	4	"reg_IMPREG16_type (IMPREG16)—Offset 103Ch" on page 2988	00000000h
1040–1043h	4	"reg_IMPREG17_type (IMPREG17)—Offset 1040h" on page 2989	00000000h
1044–1047h	4	"reg_IMPREG18_type (IMPREG18)—Offset 1044h" on page 2990	00000000h
1048–104Bh	4	"reg_IMPREG19_type (IMPREG19)—Offset 1048h" on page 2991	00000000h
104C–104Fh	4	"reg_IMPREG20_type (IMPREG20)—Offset 104Ch" on page 2992	00000000h
1050–1053h	4	"reg_IMPREG21_type (IMPREG21)—Offset 1050h" on page 2992	000F0000h
1054–1057h	4	"reg_IMPREG22_type (IMPREG22)—Offset 1054h" on page 2993	00020000h
1058–105Bh	4	"reg_IMPREG23_type (IMPREG23)—Offset 1058h" on page 2994	00000000h
105C–105Fh	4	"reg_IMPREG24_type (IMPREG24)—Offset 105Ch" on page 2995	00000000h
1060–1063h	4	"reg_IMPREG25_type (IMPREG25)—Offset 1060h" on page 2996	00000020h

7.8.1 reg_IMPREG1_type (IMPREG1)—Offset 1000h

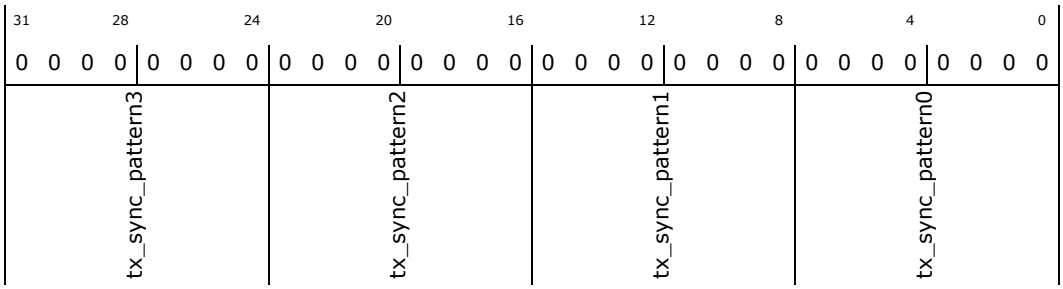
IMPREG1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1000h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**tx_sync_pattern3:** User Specified SYNC patterns. The sync pattern is 4 bytes. 8b10b data encoding is done in HW
23:16	0x0 RW	**tx_sync_pattern2:** Refer Above
15:8	0x0 RW	**tx_sync_pattern1:** Refer Above
7:0	0x0 RW	**tx_sync_pattern0:** Refer Above

7.8.2 reg_IMPREG2_type (IMPREG2)—Offset 1004h

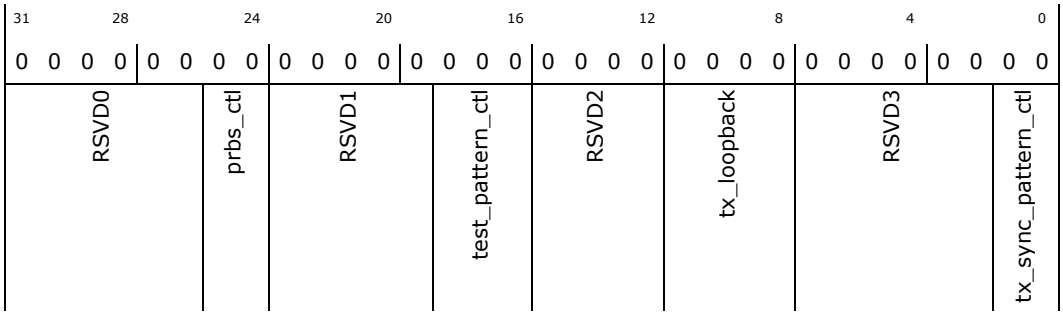
IMPREG2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1004h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD0:** Reserved
25:24	0x0 RW	**prbs_ctl:** 2'h0: Disable PRBS Generation 2'h1: PRBS Generation enable.
23:19	0x0 RO	**RSVD1:** Reserved
18:16	0x0 RW	**test_pattern_ctl:** B[2]: PRBS Pattern Generation B[1:0]: CJTPAT/CRPAT Pattern generation
15:12	0x0 RO	**RSVD2:** Reserved
11:8	0x0 RW	**tx_loopback:** TX2RX loopback in MPHY digital. 1 bit per lane. Supports upto 4 lanes
7:2	0x0 RO	**RSVD3:** Reserved
1:0	0x0 RW	**tx_sync_pattern_ctl:** Defines source of the SYNC Pattern 2'b00 : D10.5, D26.5 2'bX1 : tx_sync_pattern3, tx_sync_pattern2, tx_sync_pattern1, tx_sync_pattern0 2'b10 : 16'h0000

7.8.3 reg_IMPREG3_type (IMPREG3)—Offset 1008h

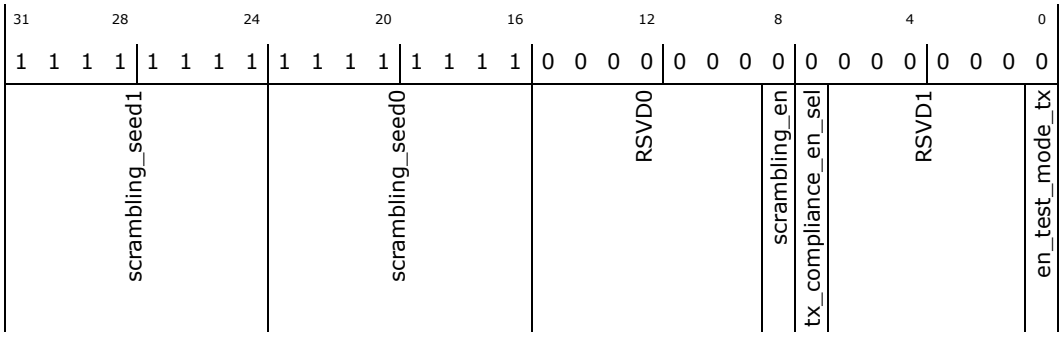
IMPREG3

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1008h

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0xff RW	**scrambling_seed1:** Higher 8 bits of LFSR initial value. When test mode is enabled, burst will be sent with data from LFSR register (which is internal to design).

Bit Range	Default & Access	Field Name (ID): Description
23:16	0xff RW	**scrambling_seed0:** Lower 8 bits of LFSR initial value. When test mode is enabled, burst will be sent with data from LFSR register (which is internal to design).
15:9	0x0 RO	**RSVD0:** Reserved
8	0x0 RW	**scrambling_en:** Enables and disables scrambling of the 16 bit data from the controller. 1'b0 : No Data Scrambling 1'b1 : Enable Data Scrambling
7	0x0 RW	**tx_compliance_en_sel:** Used as part of the MPHY TEST for SSIC. Setting this bit to a 1, will select the top level hc_mphy_test_tx_compli_en, otherwise it will select bit0 of IMPREG3.
6:1	0x0 RO	**RSVD1:** Reserved
0	0x0 RW	**en_test_mode_tx:** Enables test mode operation. Setting this bit 1, will make M-TX to start new burst with LFSR data. Hibern8/Sleep/Stall state will be exited.

7.8.4 reg_IMPREG4_type (IMPREG4)—Offset 100Ch

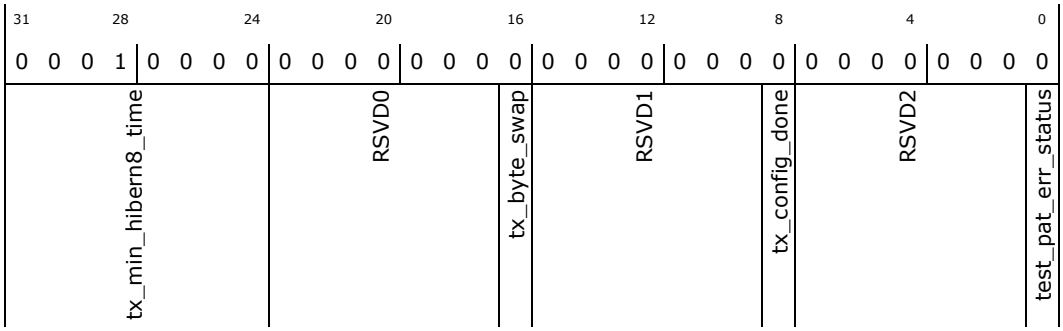
IMPREG4

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 100Ch

Default: 10000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x10 RW	**tx_min_hibern8_time:** Min time in hibern8 in terms of no of reference clocks.
23:17	0x0 RO	**RSVD0:** Reserved
16	0x0 RW	**tx_byte_swap:** Swap the byte ordering for the pair of bytes on RMMI.

Bit Range	Default & Access	Field Name (ID): Description
15:9	0x0 RO	**RSVD1:** Reserved
8	0x0 RW	**tx_config_done:** Indicates completion of configuration writes
7:1	0x0 RO	**RSVD2:** Reserved
0	0x0 RW/1C	**test_pat_err_status:** Error detected on LFSR pattern checking. This is set on the first mismatch.

7.8.5 reg_IMPREG5_type (IMPREG5)—Offset 1010h

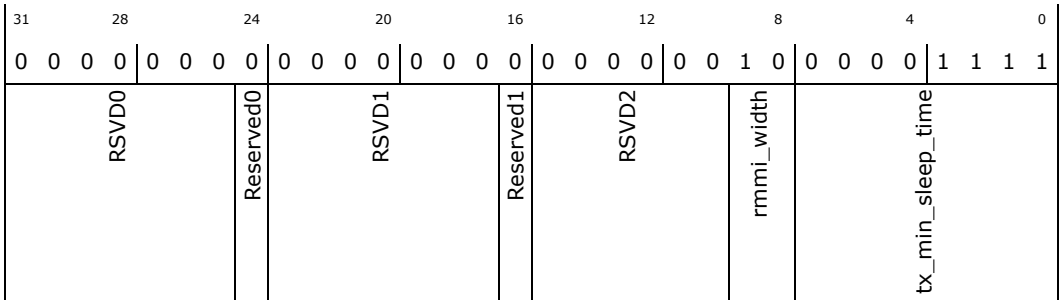
IMPREG5

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1010h

Default: 0000020Fh



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RO	**Reserved0:** Reserved
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RO	**Reserved1:** Reserved
15:10	0x0 RO	**RSVD2:** Reserved
9:8	0x2 RW	**rmmi_width:** RMMI interface width. 2'b00 : Reserved; 2'b01: 2 Symbol (16 bits); 2'h2 4 Symbols (32 bits); 2'b11 : Reserved
7:0	0xf RW	**tx_min_sleep_time:** Min time in sleep in terms of no of reference clocks.

7.8.6 reg_IMPREG6_type (IMPREG6)—Offset 1014h

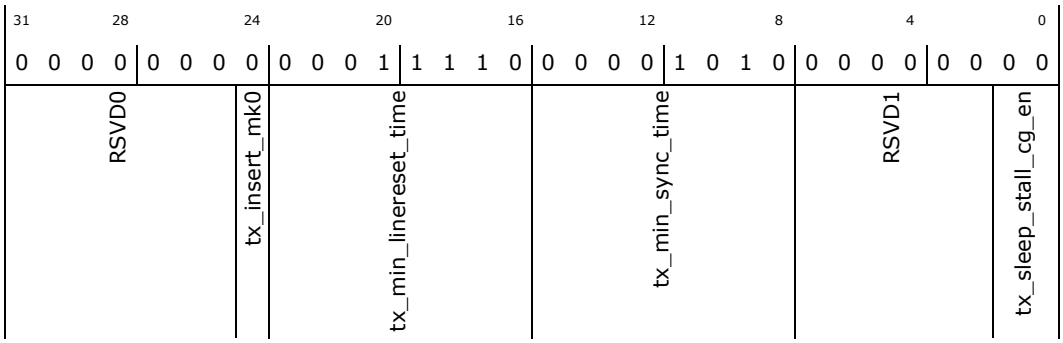
IMPREG6

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1014h

Default: 001E0A00h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**tx_insert_mk0:** Insert MK0 after sync duration when starting a new burst
23:16	0x1e RW	**tx_min_linereset_time:** Drive DIF-P for this duration on line reset in steps of 100s
15:8	0xa RW	**tx_min_sync_time:** NO CONNECT
7:2	0x0 RO	**RSVD1:** Reserved
1:0	0x0 RW	**tx_sleep_stall_cg_en:** Enable TX Symbol clock Gating: [0] Sleep state clock gating; [1] Stall state clock gating

7.8.7 reg_IMPREG7_type (IMPREG7)—Offset 1018h

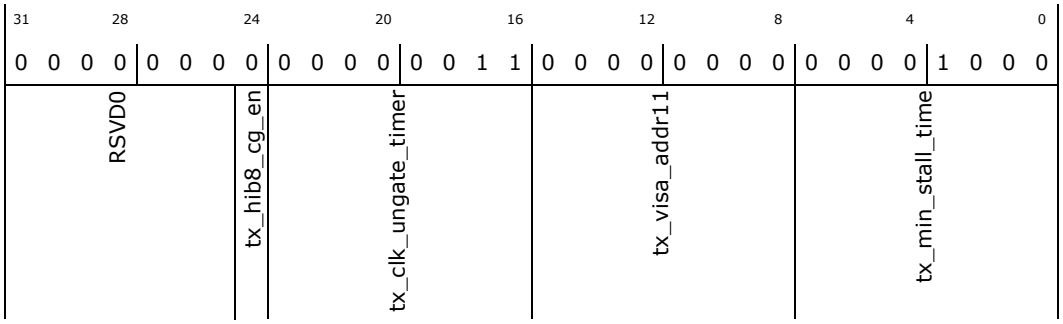
IMPREG7

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1018h

Default: 00030008h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**tx_hib8_cg_en:** Enable TX Symbol clock gating in HIBERN8 state.
23:16	0x3 RW	**tx_clk_ungate_timer:** NO CONNECT
15:8	0x0 RW	**tx_visa_addr11:** NO CONNECT
7:0	0x8 RW	**tx_min_stall_time:** Delay starting a new high burst to satisfy the tx minimum stal requirement.

7.8.8 reg_IMPREG8_type (IMPREG8)—Offset 101Ch

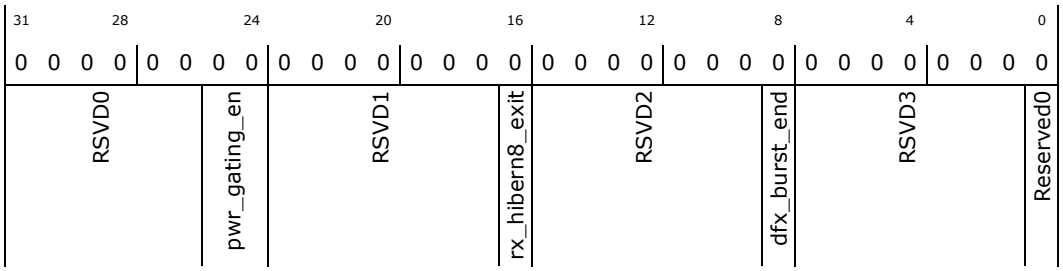
IMPREG8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 101Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
25:24	0x0 RW	**pwr_gating_en:** Enable Power gating [0] : Enable Power gating feature for data lane core power well [1]: Enable power gating feature for data lane SUS power well
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RW	**rx_hibern8_exit:** SW controlled RX H8 mechanism. Programming this bit to 1 brinss the RX out of H8. It does not wait for DIF-N detection
15:9	0x0 RO	**RSVD2:** Reserved
8	0x0 RW	**dfx_burst_end:** Force close the TX burst. This is not an offline register. Programming this register has an immediate effect.
7:1	0x0 RO	**RSVD3:** Reserved
0	0x0 RO	**Reserved0:** Reserved

7.8.9 reg_IMPREG9_type (IMPREG9)—Offset 1020h

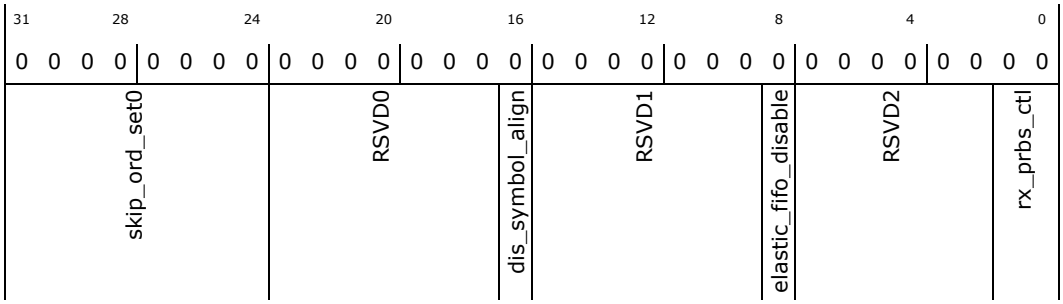
IMPREG9

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1020h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**skip_ord_set0:** Not Used
23:17	0x0 RO	**RSVD0:** Reserved
16	0x0 RW	**dis_symbol_align:** NO CONNECT
15:9	0x0 RO	**RSVD1:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**elastic_fifo_disable:** Disable Elastic FIFO Feature. In this mode, it acts as clock domain crossing FIFO only.
7:2	0x0 RO	**RSVD2:** Reserved
1:0	0x0 RW	**rx_prbs_ctl:** NO CONNECT

7.8.10 reg_IMPREG10_type (IMPREG10)—Offset 1024h

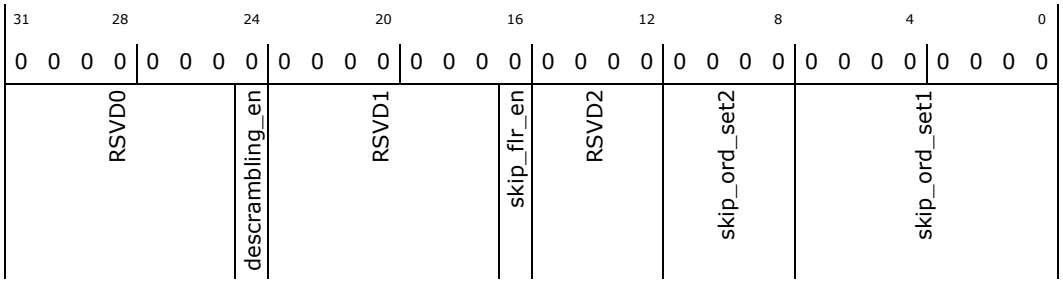
IMPREG10

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1024h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**descrambling_en:** NO CONNECT
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RW	**skip_flr_en:** Not Used
15:12	0x0 RO	**RSVD2:** Reserved
11:8	0x0 RW	**skip_ord_set2:** Not Used
7:0	0x0 RW	**skip_ord_set1:** Not Used

7.8.11 reg_IMPREG11_type (IMPREG11)—Offset 1028h

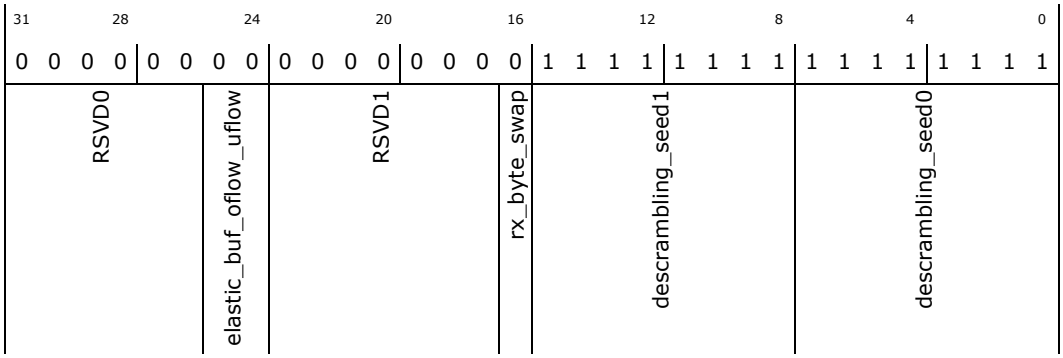
IMPREG11

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1028h

Default: 0000FFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD0:** Reserved
25:24	0x0 RW/1C	**elastic_buf_oflow_uflow:** Elastic Buffer overflow/underflow indication [0] - EB Overflow; [1] - EB Underflow
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RW	**rx_byte_swap:** 1'b0 : Maintain Symbol Order 1'b1 : Swap Most Significan and Least Significant Symbols in a 20 bit Word
15:8	0xff RW	**descrambling_seed1:** De-Scrambling Seed. Reset to this value on detection of MK0
7:0	0xff RW	**descrambling_seed0:** Same as above. Part of 16 bit value

7.8.12 reg_IMPREG12_type (IMPREG12)—Offset 102Ch

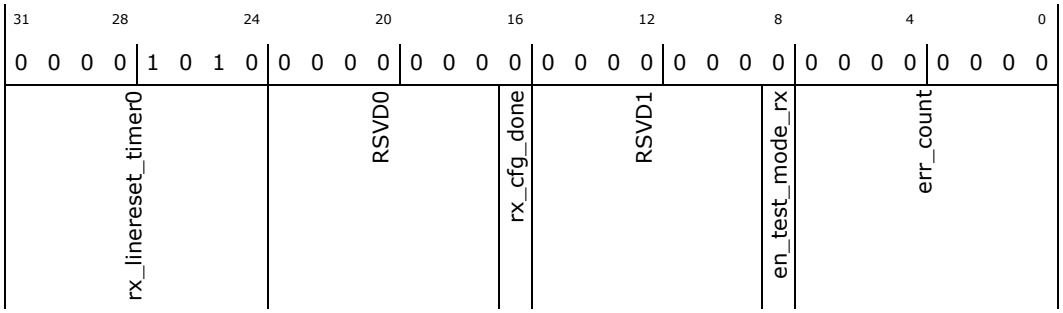
IMPREG12

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 102Ch

Default: 0A000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0xa RW	**rx_linereset_timer0:** Indicate RX_Line_reset on detection DIF-P for this duration in steps of 100s
23:17	0x0 RO	**RSVD0:** Reserved
16	0x0 RW	**rx_cfg_done:** Indicates completion of configuration writes.
15:9	0x0 RO	**RSVD1:** Reserved
8	0x0 RW	**en_test_mode_rx:** Enables RX PRBS Pattern Test Mode 1'b0 : Test Mode Disabled 1'b1 : Test Mode Enabled
7:0	0x0 RW/1C	**err_count:** Saturatin error count. Count is incremented by 1 for each cycle there is a mismatch

7.8.13 reg_IMPREG13_type (IMPREG13)—Offset 1030h

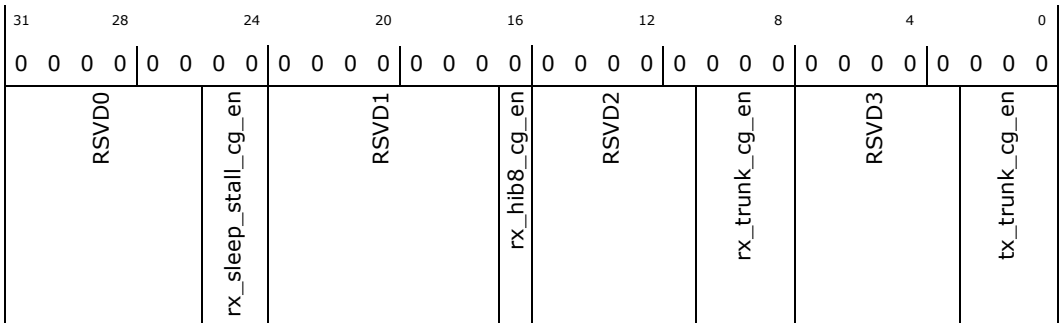
IMPREG13

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1030h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD0:** Reserved
25:24	0x0 RW	**rx_sleep_stall_cg_en:** Enable RX Symbol clock Gating: [0] Sleep state clock gating; [1] Stall state clock gating
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RW	**rx_hib8_cg_en:** Enable RX Symbol clock gating in HIBERN8 state.
15:11	0x0 RO	**RSVD2:** Reserved
10:8	0x0 RW	**rx_trunk_cg_en:** RX Symbol Clock trunk clock gating enable in different states. [0] Enable RXSymbolClk gating in Sleep state; [1] Enable RXSymbolClk gating in STALL state; [2] Enable RXSymbolClk gating in HIBERN8 state.
7:3	0x0 RO	**RSVD3:** Reserved
2:0	0x0 RW	**tx_trunk_cg_en:** TX Symbol Clock trunk clock gating enable in different states. [0] Enable TXSymbolClk gating in Sleep state; [1] Enable TXSymbolClk gating in STALL state; [2] Enable TXSymbolClk gating in HIBERN8 state.

7.8.14 reg_IMPREG14_type (IMPREG14)—Offset 1034h

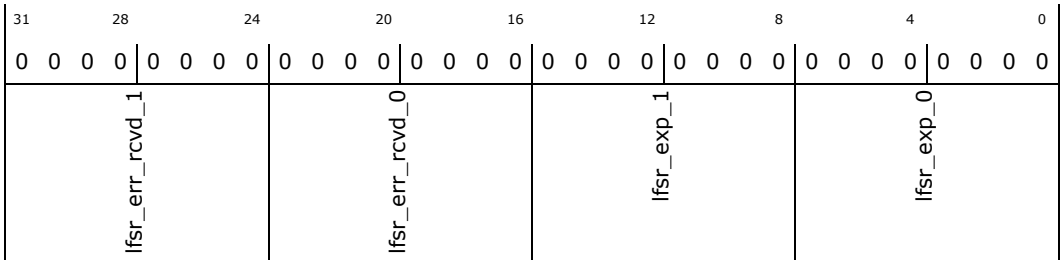
IMPREG14

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1034h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW/1C	**lfsr_err_rcvd_1:** First mismatch pattern. This field remains locked until the test_pat_err_status bit is cleared
23:16	0x0 RW/1C	**lfsr_err_rcvd_0:** LSB of the above field

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RW/1C	**lfsr_exp_1:** Expected pattern when the first mismatch detected. This field remains locked until the test_pat_err_status bit is cleared
7:0	0x0 RW/1C	**lfsr_exp_0:** LSB of the above field

7.8.15 reg_IMPREG15_type (IMPREG15)—Offset 1038h

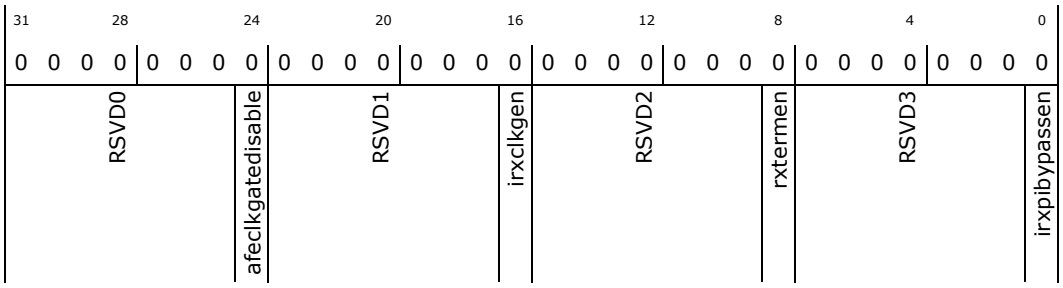
IMPREG15

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1038h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**afeclkgatedisable:** per lane divider clock input gate. 0=gated.
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RW	**irxclkgen:** enables input quad clocks to PI. Disable to save power in STALL (may need to keep them running for extra SI's to clear FIFO)
15:9	0x0 RO	**RSVD2:** Reserved
8	0x0 RW	**rxtermen:** enable RXTERM
7:1	0x0 RO	**RSVD3:** Reserved
0	0x0 RW	**irxpibypassen:** Park PI. Debug use only

7.8.16 reg_IMPREG16_type (IMPREG16)—Offset 103Ch

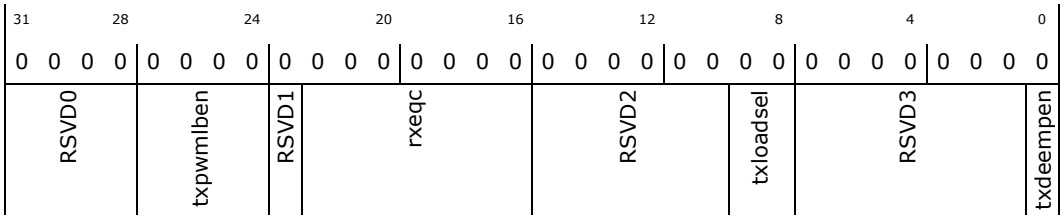
IMPREG16

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 103Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RSVD0:** Reserved
27:24	0x0 RW	**txpwmlben:** Internal RX2TX loopback for PWM mode. Not supported.
23	0x0 RO	**RSVD1:** Reserved
22:16	0x0 RW	**rxeqc:** RX Equalization output to the AFE
15:10	0x0 RO	**RSVD2:** Reserved
9:8	0x0 RW	**txloadsel:** TX symbol clock CDC tuning bits. 4 possible phases to allow post silicon adjustment.
7:1	0x0 RO	**RSVD3:** Reserved
0	0x0 RW	**txdeempen:** TX de-emphasis enable

7.8.17 reg_IMPREG17_type (IMPREG17)—Offset 1040h

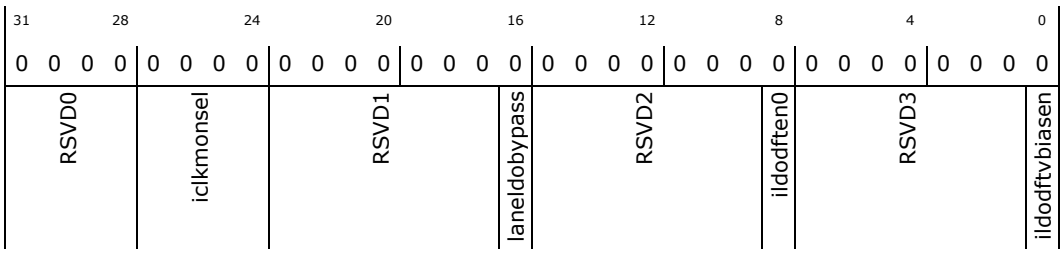
IMPREG17

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1040h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RSVD0:** Reserved
27:24	0x0 RW	**iclkmonsel:** selects which clock net in lane clock block to monitor
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RW	**laneldobypass:** per lane LDO bypass. 1 = bypass.
15:9	0x0 RO	**RSVD2:** Reserved
8	0x0 RW	**ildodften0:** LDO monitor enable.
7:1	0x0 RO	**RSVD3:** Reserved
0	0x0 RW	**ildodftvbiasen:** enable LDO bias node monitor.

7.8.18 reg_IMPREG18_type (IMPREG18)—Offset 1044h

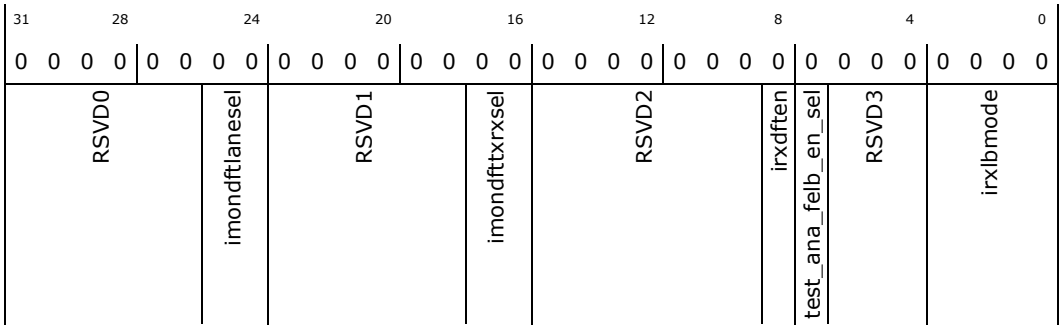
IMPREG18

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1044h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD0:** Reserved
25:24	0x0 RW	**imondftlanesel:** selects which digital net in lane to monitor
23:18	0x0 RO	**RSVD1:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
17:16	0x0 RW	**imondfttxrxsel:** selects TX or RX digital nets to monitor
15:9	0x0 RO	**RSVD2:** Reserved
8	0x0 RW	**irxdften:** Enables monitor paths to internal nodes in HS RX.
7	0x0 RW	**test_ana_felb_en_sel:** Used as part of the MPHY TEST for SSIC. Setting this bit to a 1, will select the top level hc_mphy_test_ana_felb_en. Otherwise irxlbmode will be selected.
6:4	0x0 RO	**RSVD3:** Reserved
3:0	0x0 RW	**irxlbmode:** Analog FELB loopback mode. HS Serial RX data is looped back to TX.

7.8.19 reg_IMPREG19_type (IMPREG19)—Offset 1048h

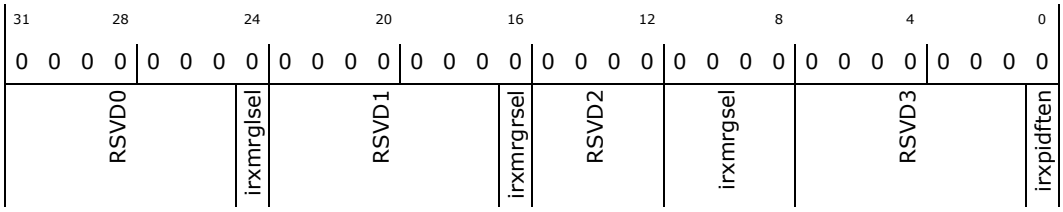
IMPREG19

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1048h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**irxmrglsel:** CDR logic margin left mode
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RW	**irxmrgrsel:** CDR logic margin right mode
15:12	0x0 RO	**RSVD2:** Reserved
11:8	0x0 RW	**irxmrgsel:** CDR logic margin selects

Bit Range	Default & Access	Field Name (ID): Description
7:1	0x0 RO	**RSVD3:** Reserved
0	0x0 RW	**irxpidften:** PI DFT enable. Enables PI margining.

7.8.20 reg_IMPREG20_type (IMPREG20)—Offset 104Ch

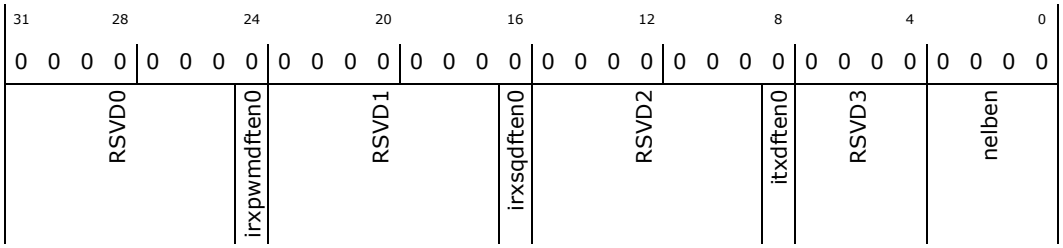
IMPREG20

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 104Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**irxpwmdften0:** RX PWM DFT mode. Enables monitoring of internal nodes in PWM RX.
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RW	**irxsqdften0:** Squelch DFT enable. Enables monitoring of internal nodes in SQ.
15:9	0x0 RO	**RSVD2:** Reserved
8	0x0 RW	**itxdften0:** TX DFT enable. Enables monitoring of internal digital nodes in TX.
7:4	0x0 RO	**RSVD3:** Reserved
3:0	0x0 RW	**nelben:** enable TX to RX NELB muxes. Not supported

7.8.21 reg_IMPREG21_type (IMPREG21)—Offset 1050h

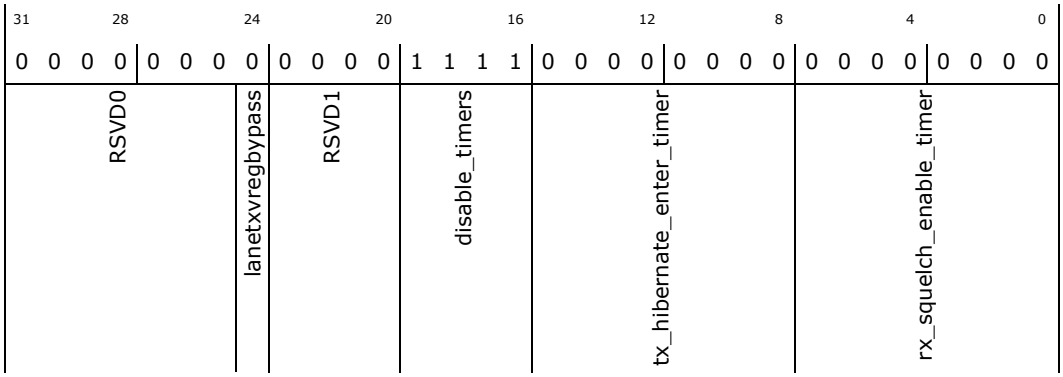
IMPREG21

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1050h

Default: 000F0000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**lanetxvregbypass:** bypass TX vreg
23:20	0x0 RO	**RSVD1:** Reserved
19:16	0xf RW	**disable_timers:** [0] - Disable tx_min_hibernate timer; [1] - Disable tx_min_sleep_time; [2] - Disable tx_min_stall_time; [3] tx_min_activate
15:8	0x0 RW	**tx_hibernate_enter_timer:** Hibernate enter timer. M-TX drives DIF-N after TOB for this timer duration before turning off TX driver. This timer is implemented in config clock.
7:0	0x0 RW	**rx_squelch_enable_timer:** RX squelch detection is enabled after this timer is expired. The timer is started when detecting TOB. It's implemented in config clock

7.8.22 reg_IMPREG22_type (IMPREG22)—Offset 1054h

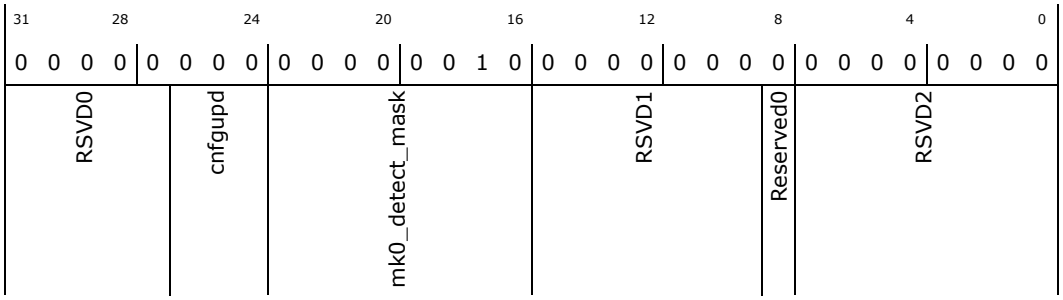
IMPREG22

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1054h

Default: 00020000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RSVD0:** Reserved
26:24	0x0 RW	**cnfgupd:** Update effective configuration registers from shadow registers [2] - Update Private Registers: [1] - Update RX registers: [0] - Update TX Registers
23:16	0x2 RW	**mk0_detect_mask:** Delay MK0 detection after DIF-P detection to prevent false MK0 detection. Counted in pairs of symbols
15:9	0x0 RO	**RSVD1:** Reserved
8	0x0 RO	**Reserved0:** Reserved.
7:0	0x0 RO	**RSVD2:** Reserved

7.8.23 reg_IMPREG23_type (IMPREG23)—Offset 1058h

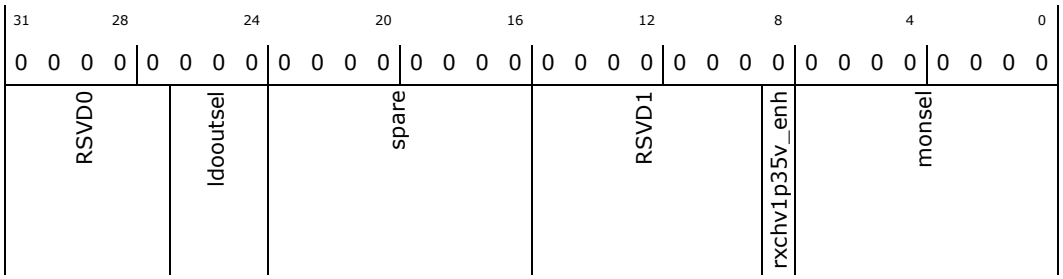
IMPREG23

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1058h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RSVD0:** Reserved
26:24	0x0 RW	**ldooutsel:** LDO output fine tune setting. Step size=10mV.
23:16	0x0 RW	**spare:** Reserved.
15:9	0x0 RO	**RSVD1:** Reserved
8	0x0 RW	**rxchv1p35v_enh:** indicates 1.35V supply is used for Squelch.
7:0	0x0 RW	**monsel:** High speed analog monitor select

7.8.24 reg_IMPREG24_type (IMPREG24)—Offset 105Ch

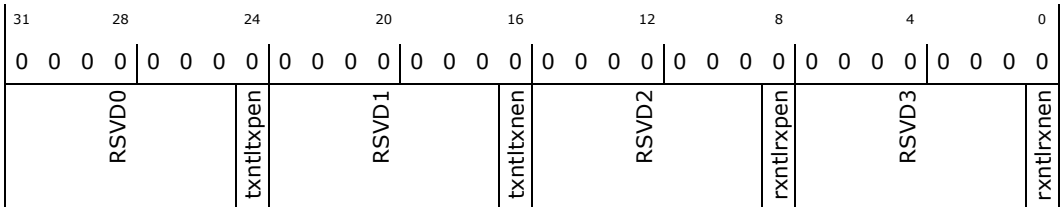
IMPREG24

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 105Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD0:** Reserved
24	0x0 RW	**txntltxpen:** NTL control. Not supported.
23:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RW	**txntltxnen:** NTL control. Not supported.
15:9	0x0 RO	**RSVD2:** Reserved
8	0x0 RW	**rxntlrxpen:** NTL control. Not supported.

Bit Range	Default & Access	Field Name (ID): Description
7:1	0x0 RO	**RSVD3:** Reserved
0	0x0 RW	**rxntlrxnen:** NTL control. Not supported.

7.8.25 reg_IMPREG25_type (IMPREG25)—Offset 1060h

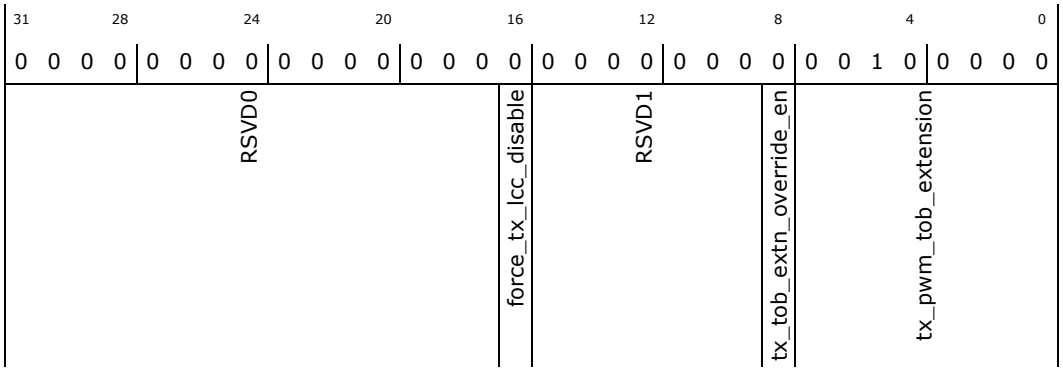
IMPREG25

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [TBD] + 1060h

Default: 00000020h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RSVD0:** Reserved
16	0x0 RW	**force_tx_lcc_disable:** TX LCC Disable 1: TX LCC is disabled 0: TX LCC is enabled as per the TX Register bit
15:9	0x0 RO	**RSVD1:** Reserved
8	0x0 RW	**tx_tob_extn_override_en:** If set the TX TOB Extension value will be taken from the Private space instead of the TX registers else it will be taken from TX register bank
7:0	0x20 RW	**tx_pwm_tob_extension:** TX PWM TOB Extension value

7.9 USB OTG Device PCI Configuration Registers

Table 45. Summary of PCI Configuration Registers—0/22/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"reg_DEVVENDID_type (DEVVENDID)—Offset 0h" on page 2999	22B78086h
4–7h	4	"reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h" on page 2999	00100000h
8–Bh	4	"reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h" on page 3000	0C03FE00h
C–Fh	4	"reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch" on page 3001	00000000h
10–13h	4	"reg_BAR_type (BAR)—Offset 10h" on page 3001	00000000h
14–17h	4	"reg_BAR1_type (BAR1)—Offset 14h" on page 3002	00000000h
2C–2Fh	4	"reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch" on page 3003	00000000h
30–33h	4	"reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 3003	00000000h
34–37h	4	"reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h" on page 3004	00000080h
3C–3Fh	4	"reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch" on page 3004	00000100h
80–83h	4	"reg_POWERCAPID_type (POWERCAPID)—Offset 80h" on page 3005	48030001h
84–87h	4	"reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h" on page 3006	00000008h
F8–FBh	4	"reg_MANID_type (MANID)—Offset F8h" on page 3006	0000000Fh

7.9.1 reg_DEVVENDID_type (DEVVENDID)—Offset 0h

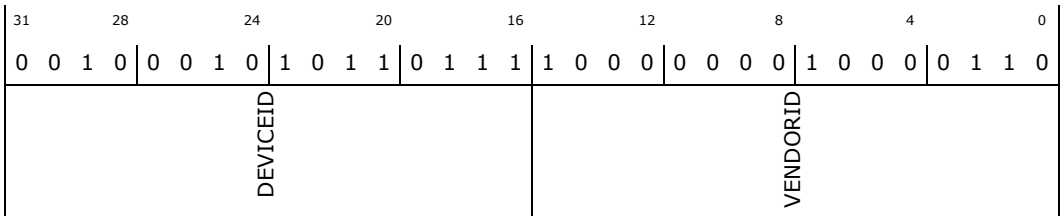
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:22, F:0] + 0h

Default: 22B78086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x22b7 RO	**DEVICEID:** Reserved.
15:0	0x8086 RO	**VENDORID:** Reserved.

7.9.2 reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h

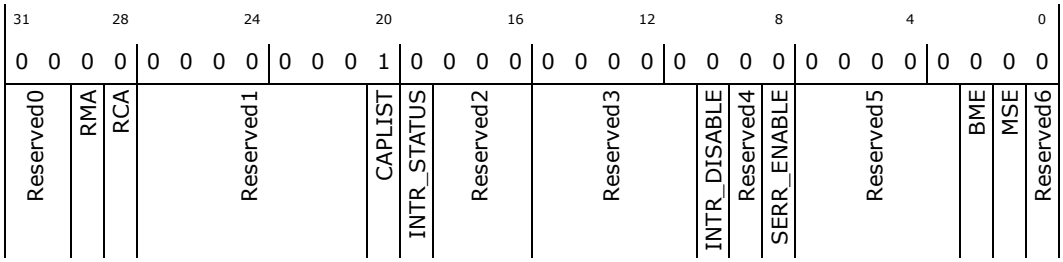
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:22, F:0] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved0:** Reserved.
29	0x0 RW/1C	**RMA:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
28	0x0 RW/1C	**RCA:** Reserved.
27:21	0x0 RO	**Reserved1:** Reserved.
20	0x1 RO	**CAPLIST:** Reserved.
19	0x0 RO	**INTR_STATUS:** Reserved.
18:16	0x0 RO	**Reserved2:** Reserved.
15:11	0x0 RO	**Reserved3:** Reserved.
10	0x0 RW	**INTR_DISABLE:** Reserved.
9	0x0 RO	**Reserved4:** Reserved.
8	0x0 RW	**SERR_ENABLE:** Reserved.
7:3	0x0 RO	**Reserved5:** Reserved.
2	0x0 RW	**BME:** Reserved.
1	0x0 RW	**MSE:** Reserved.
0	0x0 RO	**Reserved6:** Reserved.

7.9.3 reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h

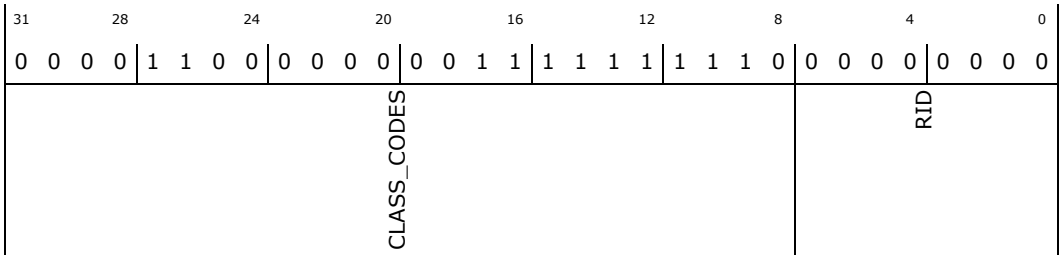
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:22, F:0] + 8h

Default: 0C03FE00h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0xc03fe RO	**CLASS_CODES:** Reserved.
7:0	0x0 RO	**RID:** Reserved.

7.9.4 reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch

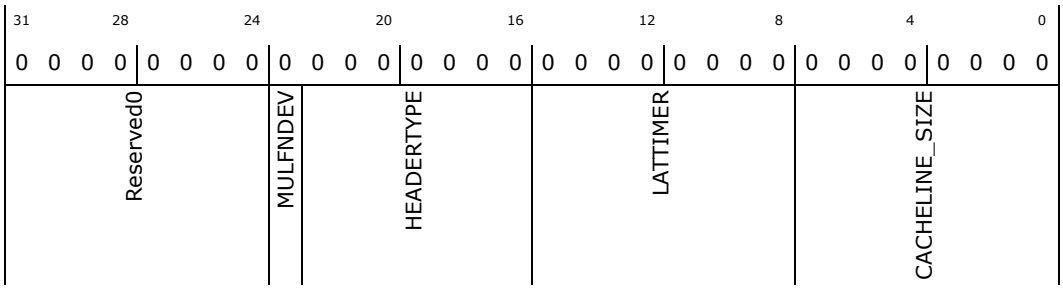
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:22, F:0] + Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved.
23	0x0 RO	**MULFNDEV:** Reserved.
22:16	0x0 RO	**HEADERTYPE:** Reserved.
15:8	0x0 RO	**LATTIMER:** Reserved.
7:0	0x0 RW	**CACHELINE_SIZE:** Reserved.

7.9.5 reg_BAR_type (BAR)—Offset 10h

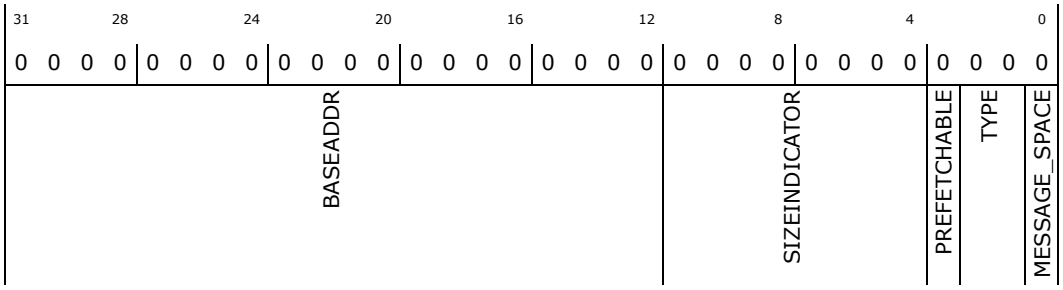
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:22, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Reserved.
11:4	0x0 RO	**SIZEINDICATOR:** Reserved.
3	0x0 RO	**PREFETCHABLE:** Reserved.
2:1	0x0 RO	**TYPE:** Reserved.
0	0x0 RO	**MESSAGE_SPACE:** Reserved.

7.9.6 reg_BAR1_type (BAR1)—Offset 14h

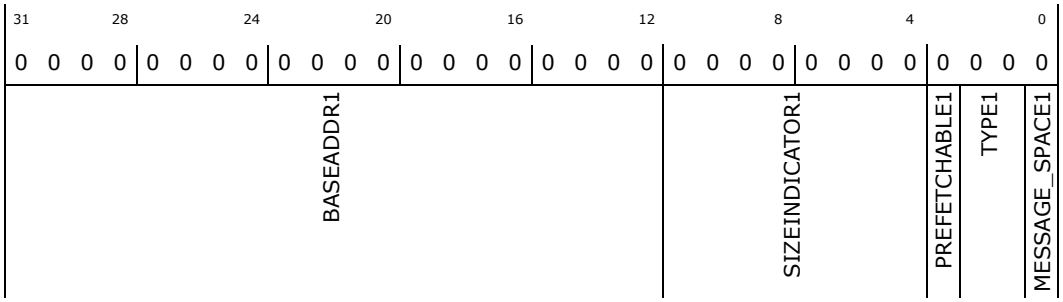
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:22, F:0] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Reserved.
11:4	0x0 RO	**SIZEINDICATOR1:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RO	**PREFETCHABLE1:** Reserved.
2:1	0x0 RO	**TYPE1:** Reserved.
0	0x0 RO	**MESSAGE_SPACE1:** Reserved.

7.9.7 reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch

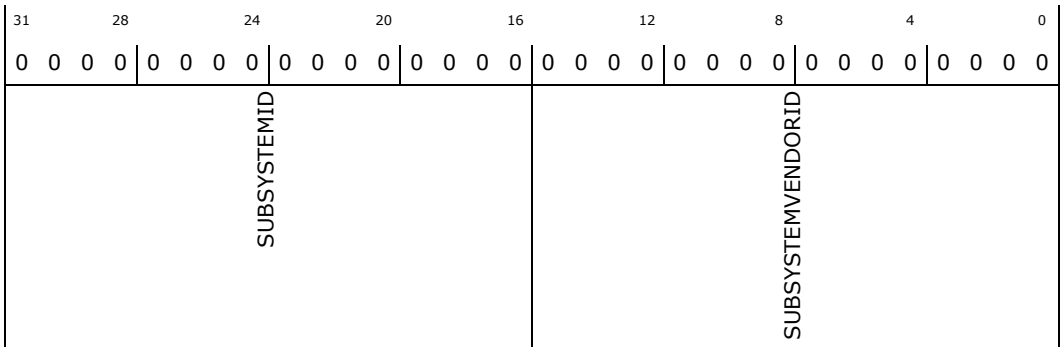
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:22, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Reserved.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Reserved.

7.9.8 reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h

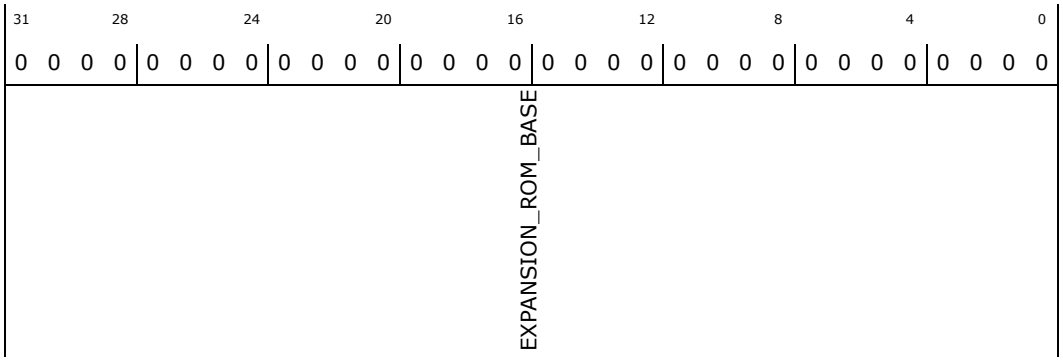
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:22, F:0] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** Reserved.

7.9.9 reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h

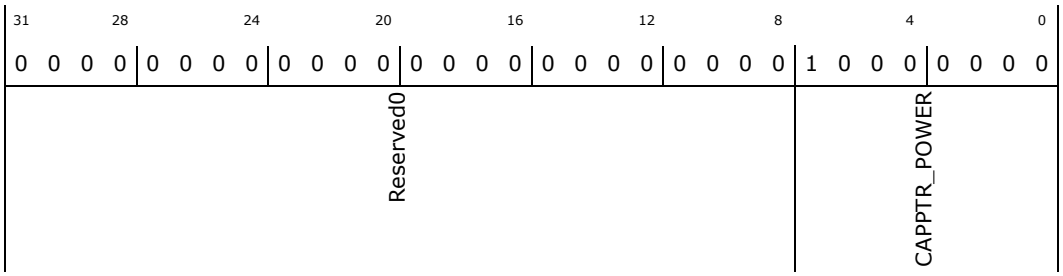
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:22, F:0] + 34h

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved.
7:0	0x80 RO	**CAPPTR_POWER:** Reserved.

7.9.10 reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch

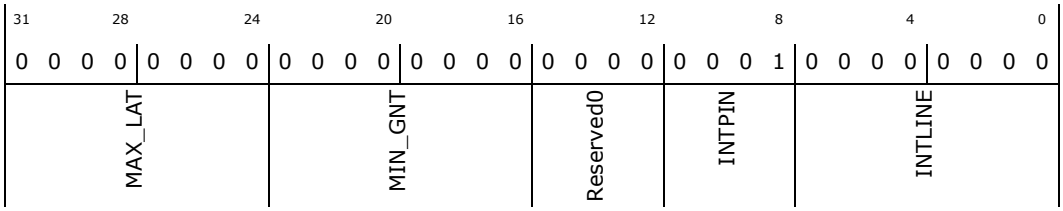
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:22, F:0] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Reserved.
23:16	0x0 RO	**MIN_GNT:** Reserved.
15:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x1 RO	**INTPIN:** Reserved.
7:0	0x0 RW	**INTLINE:** Reserved.

7.9.11 reg_POWERCAPID_type (POWERCAPID)—Offset 80h

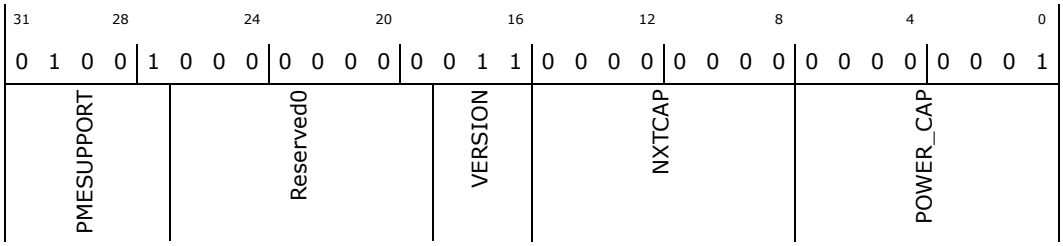
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:22, F:0] + 80h

Default: 48030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x9 RO	**PMESUPPORT:** Reserved.
26:19	0x0 RO	**Reserved0:** Reserved.
18:16	0x3 RO	**VERSION:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**NXTCAP:** Reserved.
7:0	0x1 RO	**POWER_CAP:** Reserved.

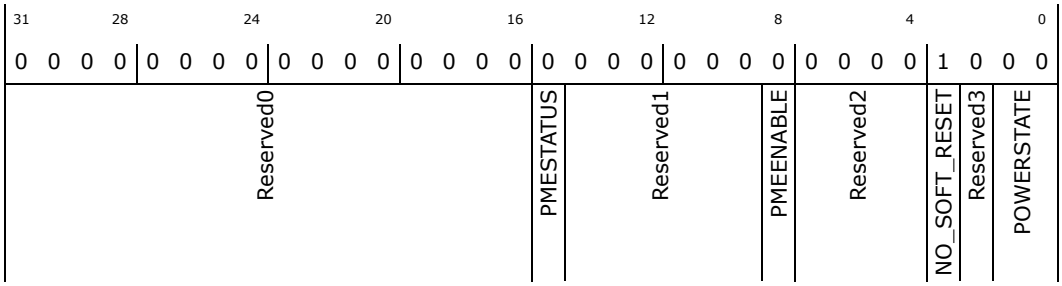
7.9.12 reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:22, F:0] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved.
15	0x0 RW/1C	**PMESTATUS:** Reserved.
14:9	0x0 RO	**Reserved1:** Reserved.
8	0x0 RW	**PMEENABLE:** Reserved.
7:4	0x0 RO	**Reserved2:** Reserved.
3	0x1 RO	**NO_SOFT_RESET:** Reserved.
2	0x0 RO	**Reserved3:** Reserved.
1:0	0x0 RW	**POWERSTATE:** Reserved.

7.9.13 reg_MANID_type (MANID)—Offset F8h

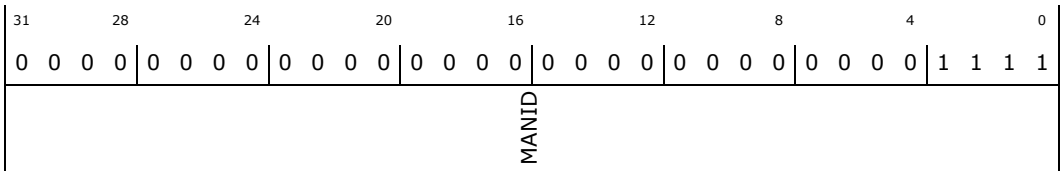
Manufacturers ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:22, F:0] + F8h

Default: 0000000Fh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xf RO	**MANID:** Reserved.

7.10 USB OTG Device PCI Message Bus Registers

Table 46. Summary of Message Bus Registers—0x59

Offset	Register Name (Register Symbol)	Default Value
0–3h	"reg_DEVVENDID_type (DEVVENDID)—Offset 0h" on page 3009	22B78086h
4–7h	"reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h" on page 3009	00100000h
8–Bh	"reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h" on page 3010	0C03FE00h
C–Fh	"reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch" on page 3011	00000000h
10–13h	"reg_BAR_type (BAR)—Offset 10h" on page 3012	00000000h
14–17h	"reg_BAR1_type (BAR1)—Offset 14h" on page 3012	00000000h
2C–2Fh	"reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch" on page 3013	00000000h
30–33h	"reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 3014	00000000h
34–37h	"reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h" on page 3014	00000080h
3C–3Fh	"reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch" on page 3015	00000100h
80–83h	"reg_POWERCAPID_type (POWERCAPID)—Offset 80h" on page 3016	48030001h
84–87h	"reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h" on page 3016	00000008h
F8–FBh	"reg_MANID_type (MANID)—Offset F8h" on page 3017	0000000Fh

7.10.1 reg_DEVVENDID_type (DEVVENDID)—Offset 0h

DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

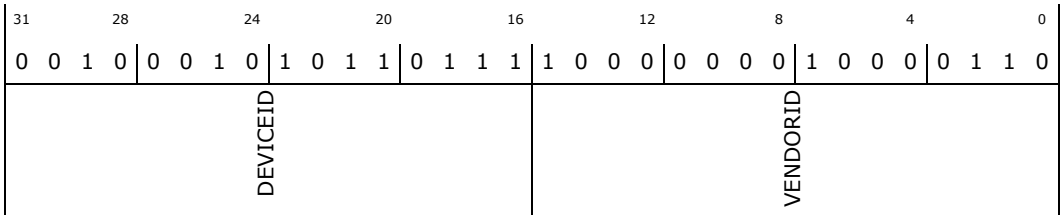
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 0h

Op Codes:

h - Read, h - Write

Default: 22B78086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x22b7 RO	**DEVICEID:** Reserved.
15:0	0x8086 RO	**VENDORID:** Reserved.

7.10.2 reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h

STATUSCOMMAND- Status and Command

Access Method

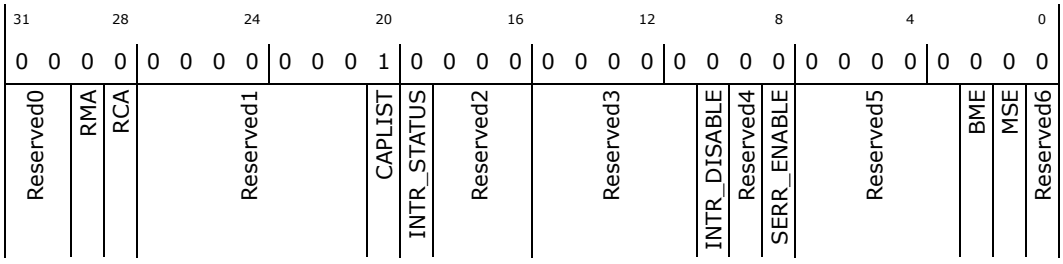
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 4h

Op Codes:

h - Read, h - Write

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved0:** Reserved.
29	0x0 RW/1C	**RMA:** Reserved.
28	0x0 RW/1C	**RCA:** Reserved.
27:21	0x0 RO	**Reserved1:** Reserved.
20	0x1 RO	**CAPLIST:** Reserved.
19	0x0 RO	**INTR_STATUS:** Reserved.
18:16	0x0 RO	**Reserved2:** Reserved.
15:11	0x0 RO	**Reserved3:** Reserved.
10	0x0 RW	**INTR_DISABLE:** Reserved.
9	0x0 RO	**Reserved4:** Reserved.
8	0x0 RW	**SERR_ENABLE:** Reserved.
7:3	0x0 RO	**Reserved5:** Reserved.
2	0x0 RW	**BME:** Reserved.
1	0x0 RW	**MSE:** Reserved.
0	0x0 RO	**Reserved6:** Reserved.

7.10.3 reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h

REVCLASSCODE - Revision ID and Class Code

Access Method

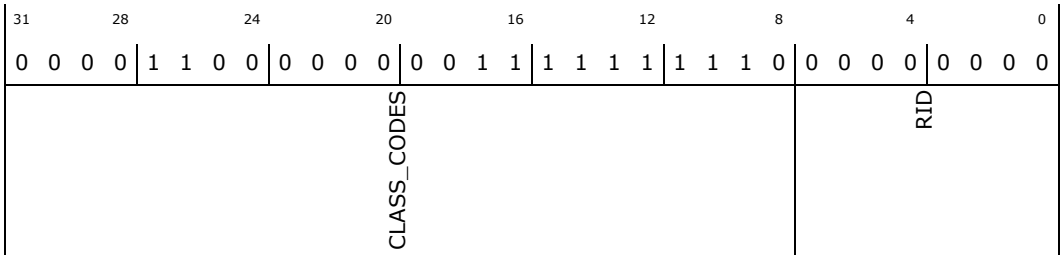
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 8h

Op Codes:

h - Read, h - Write

Default: 0C03FE00h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0xc03fe RO	**CLASS_CODES:** Reserved.
7:0	0x0 RO	**RID:** Reserved.

7.10.4 reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch

CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

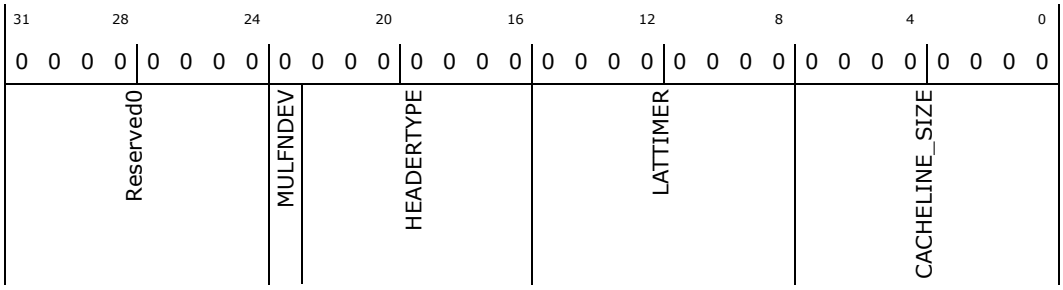
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved.
23	0x0 RO	**MULFNDEV:** Reserved.
22:16	0x0 RO	**HEADERTYPE:** Reserved.
15:8	0x0 RO	**LATTIMER:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**CACHELINE_SIZE:** Reserved.

7.10.5 reg_BAR_type (BAR)—Offset 10h

BAR -Base Address Register

Access Method

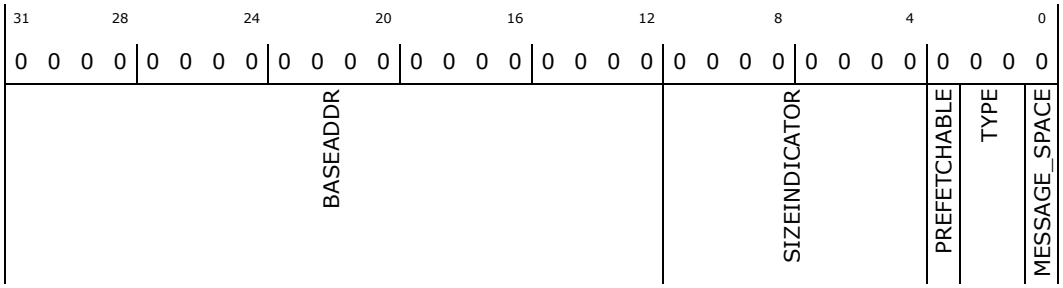
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 10h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Reserved.
11:4	0x0 RO	**SIZEINDICATOR:** Reserved.
3	0x0 RO	**PREFETCHABLE:** Reserved.
2:1	0x0 RO	**TYPE:** Reserved.
0	0x0 RO	**MESSAGE_SPACE:** Reserved.

7.10.6 reg_BAR1_type (BAR1)—Offset 14h

BAR1 -Base Address Register1

Access Method

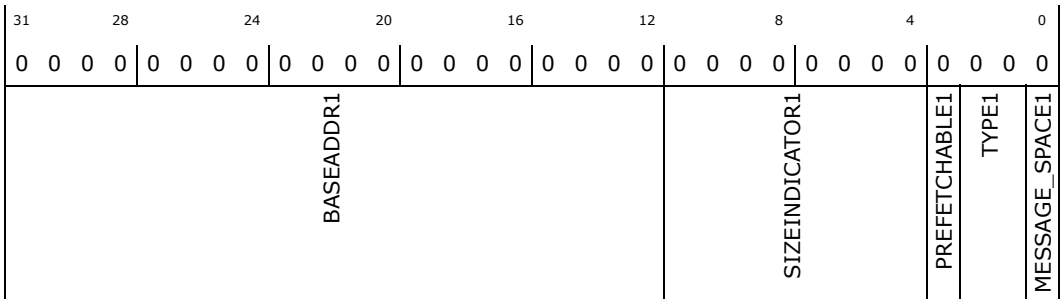
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 14h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Reserved.
11:4	0x0 RO	**SIZEINDICATOR1:** Reserved.
3	0x0 RO	**PREFETCHABLE1:** Reserved.
2:1	0x0 RO	**TYPE1:** Reserved.
0	0x0 RO	**MESSAGE_SPACE1:** Reserved.

7.10.7 reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch

SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

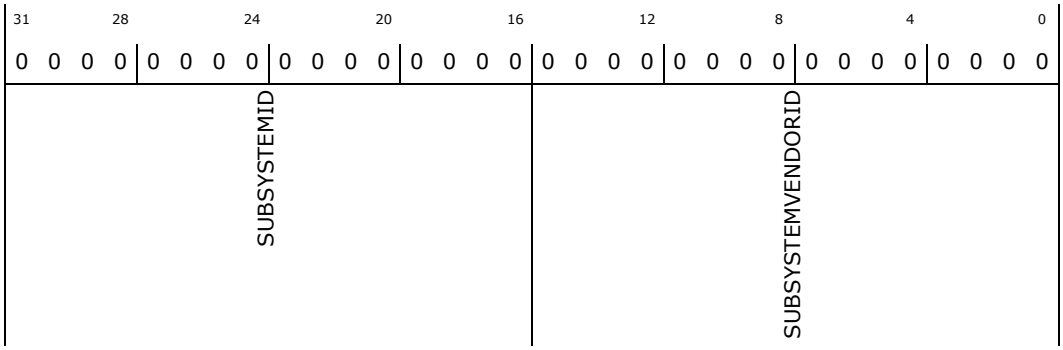
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 2Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Reserved.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Reserved.

7.10.8 reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address

Access Method

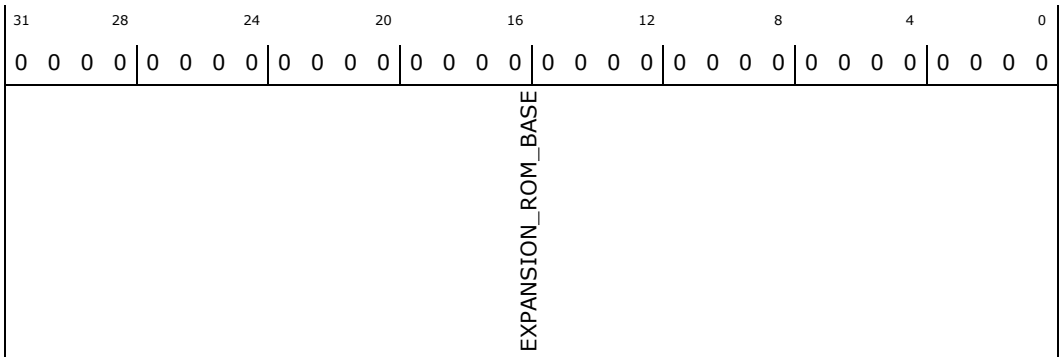
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 30h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** Reserved.

7.10.9 reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h

CAPABILITYPTR - Capabilities Pointer

Access Method

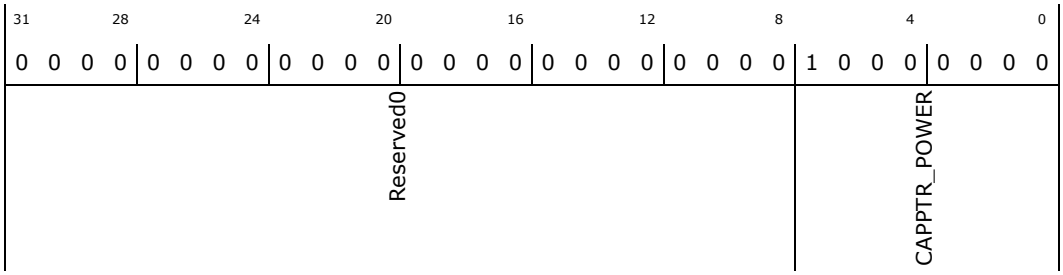
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 34h

Op Codes:

h - Read, h - Write

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved.
7:0	0x80 RO	**CAPPTR_POWER:** Reserved.

7.10.10 reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch

INTERRUPTREG - Interrupt Register

Access Method

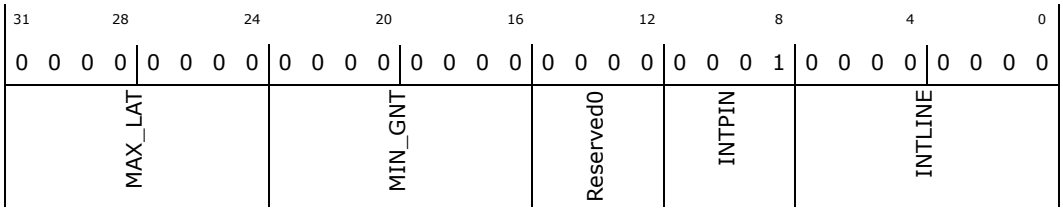
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 3Ch

Op Codes:

h - Read, h - Write

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Reserved.
23:16	0x0 RO	**MIN_GNT:** Reserved.
15:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x1 RO	**INTPIN:** Reserved.
7:0	0x0 RW	**INTLINE:** Reserved.

7.10.11 reg_POWERCAPID_type (POWERCAPID)—Offset 80h

POWERCAPID - PowerManagement Capability ID

Access Method

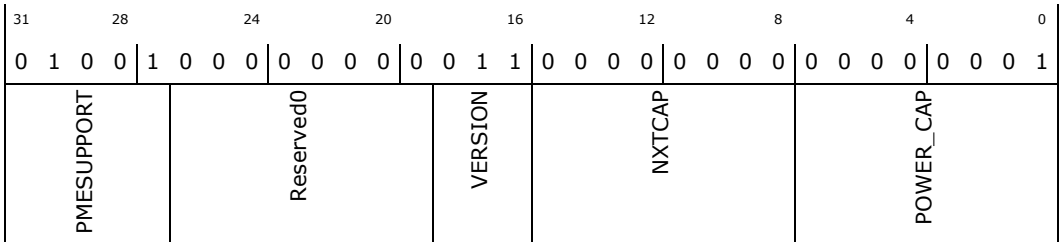
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 80h

Op Codes:

h - Read, h - Write

Default: 48030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x9 RO	**PMESUPPORT:** Reserved.
26:19	0x0 RO	**Reserved0:** Reserved.
18:16	0x3 RO	**VERSION:** Reserved.
15:8	0x0 RO	**NXTCAP:** Reserved.
7:0	0x1 RO	**POWER_CAP:** Reserved.

7.10.12 reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h

Access Method

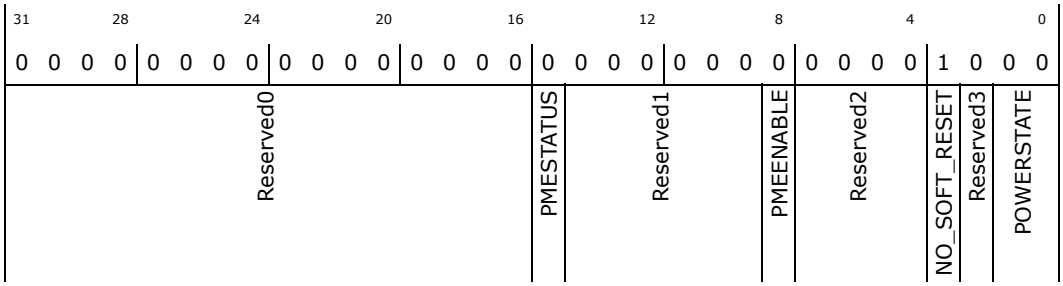
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 84h

Op Codes:

h - Read, h - Write

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved.
15	0x0 RW/1C	**PMESTATUS:** Reserved.
14:9	0x0 RO	**Reserved1:** Reserved.
8	0x0 RW	**PMEENABLE:** Reserved.
7:4	0x0 RO	**Reserved2:** Reserved.
3	0x1 RO	**NO_SOFT_RESET:** Reserved.
2	0x0 RO	**Reserved3:** Reserved.
1:0	0x0 RW	**POWERSTATE:** Reserved.

7.10.13 reg_MANID_type (MANID)—Offset F8h

Manufacturers ID

Access Method

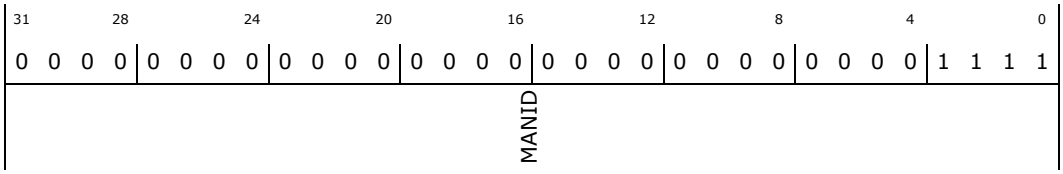
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + F8h

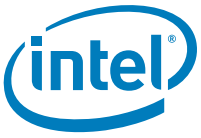
Op Codes:

h - Read, h - Write

Default: 0000000Fh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xf RO	**MANID:** Reserved.

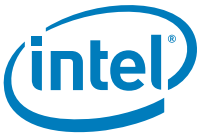


7.11 USB OTG Device Private Message Bus Registers

Table 47. Summary of Message Bus Registers—0x59

Offset	Register Name (Register Symbol)	Default Value
0–3h	"reg_IOSFCTL_type (IOSFCTL)—Offset 0h" on page 3024	0000000Fh
8–Bh	"reg_IOSFSTS_type (IOSFSTS)—Offset 8h" on page 3024	00000000h
10–13h	"reg_OCPCTL_type (OCPCTL)—Offset 10h" on page 3025	000000F1h
20–23h	"reg_FLSH_type (FLSH)—Offset 20h" on page 3026	00000000h
30–33h	"reg_RID_type (RID)—Offset 30h" on page 3027	00000000h
34–37h	"reg_CAPID_type (CAPID)—Offset 34h" on page 3027	00000000h
50–53h	"reg_SPARE_type (SPARE)—Offset 50h" on page 3028	00000000h
60–63h	"reg_IOSFSBA_type (IOSFSBA)—Offset 60h" on page 3028	00000000h
68–6Bh	"reg_UPARBGNTCNTVC0_type (UPARBGNTCNTVC0)—Offset 68h" on page 3029	00000001h
6C–6Fh	"reg_UPARBGNTCNTVC1_type (UPARBGNTCNTVC1)—Offset 6Ch" on page 3029	00000000h
70–73h	"reg_UPARBGNTCNTVC2_type (UPARBGNTCNTVC2)—Offset 70h" on page 3030	00000000h
74–77h	"reg_DNARBGNTCNT_T0_type (DNARBGNTCNT_T0)—Offset 74h" on page 3030	00000001h
78–7Bh	"reg_DNARBGNTCNT_T1_type (DNARBGNTCNT_T1)—Offset 78h" on page 3031	00000000h
7C–7Fh	"reg_DNARBGNTCNT_T2_type (DNARBGNTCNT_T2)—Offset 7Ch" on page 3032	00000000h
C0–C3h	"reg_APICBASE_type (APICBASE)—Offset C0h" on page 3032	00000000h
C4–C7h	"reg_SRAMBASE_type (SRAMBASE)—Offset C4h" on page 3033	00000000h
C8–CBh	"reg_IOREGSELBASE_type (IOREGSELBASE)—Offset C8h" on page 3033	00000000h
CC–CFh	"reg_IOREGSELLIMIT_type (IOREGSELLIMIT)—Offset CCh" on page 3034	00000000h
100–103h	"reg_PWBASE0_type (PWBASE0)—Offset 100h" on page 3035	00000000h
104–107h	"reg_PWLIMIT0_type (PWLIMIT0)—Offset 104h" on page 3035	00000000h
108–10Bh	"reg_PWBASE1_type (PWBASE1)—Offset 108h" on page 3036	00000000h
10C–10Fh	"reg_PWLIMIT1_type (PWLIMIT1)—Offset 10Ch" on page 3037	00000000h
110–113h	"reg_PWBASE2_type (PWBASE2)—Offset 110h" on page 3037	00000000h
114–117h	"reg_PWLIMIT2_type (PWLIMIT2)—Offset 114h" on page 3038	00000000h
118–11Bh	"reg_PWBASE3_type (PWBASE3)—Offset 118h" on page 3039	00000000h
11C–11Fh	"reg_PWLIMIT3_type (PWLIMIT3)—Offset 11Ch" on page 3040	00000000h
150–153h	"reg_MMIOSCUASSISTREG0_type (MMIOSCUASSISTREG0)—Offset 150h" on page 3040	00000000h
154–157h	"reg_MMIOSCUASSISTREG1_type (MMIOSCUASSISTREG1)—Offset 154h" on page 3041	00000000h

Offset	Register Name (Register Symbol)	Default Value
158–15Bh	"reg_MMIOSCUASSISTREG2_type (MMIOSCUASSISTREG2)—Offset 158h" on page 3042	00000000h
15C–15Fh	"reg_MMIOSCUASSISTREG3_type (MMIOSCUASSISTREG3)—Offset 15Ch" on page 3043	00000000h
1E0–1E3h	"reg_PMCTL_type (PMCTL)—Offset 1E0h" on page 3044	00000000h
200–203h	"reg_DEBUGCTL_type (DEBUGCTL)—Offset 200h" on page 3045	00000000h
280–283h	"reg_DEBUGSTS_type (DEBUGSTS)—Offset 280h" on page 3046	00000000h
400–403h	"reg_IOCFGCTL_type (IOCFGCTL)—Offset 400h" on page 3046	00000000h
408–40Bh	"reg_UPBRIDGEDATA_type (UPBRIDGEDATA)—Offset 408h" on page 3047	00000000h
410–413h	"reg_UPBRIDGECMD_type (UPBRIDGECMD)—Offset 410h" on page 3048	00000000h
414–417h	"reg_ILBCTL_type (ILBCTL)—Offset 414h" on page 3049	00000000h
418–41Bh	"reg_INTACKBASE_type (INTACKBASE)—Offset 418h" on page 3049	00000000h
420–423h	"reg_SMICMD_type (SMICMD)—Offset 420h" on page 3050	00000000h
424–427h	"reg_SMIADDR_type (SMIADDR)—Offset 424h" on page 3051	00000000h
428–42Bh	"reg_SMIDATA_type (SMIDATA)—Offset 428h" on page 3051	00000000h
42C–42Fh	"reg_SMISTS_type (SMISTS)—Offset 42Ch" on page 3051	00000002h
430–433h	"reg_IOSCUASSISTREG0_type (IOSCUASSISTREG0)—Offset 430h" on page 3052	FFFF0000h
434–437h	"reg_IOSCUASSISTREG1_type (IOSCUASSISTREG1)—Offset 434h" on page 3053	FFFF0000h
438–43Bh	"reg_IOSCUASSISTREG2_type (IOSCUASSISTREG2)—Offset 438h" on page 3054	FFFF0000h
43C–43Fh	"reg_IOSCUASSISTREG3_type (IOSCUASSISTREG3)—Offset 43Ch" on page 3055	FFFF0000h
440–443h	"reg_IOSCUASSISTREG4_type (IOSCUASSISTREG4)—Offset 440h" on page 3055	FFFF0000h
444–447h	"reg_IOSCUASSISTREG5_type (IOSCUASSISTREG5)—Offset 444h" on page 3056	FFFF0000h
448–44Bh	"reg_IOSCUASSISTREG6_type (IOSCUASSISTREG6)—Offset 448h" on page 3057	FFFF0000h
44C–44Fh	"reg_IOSCUASSISTREG7_type (IOSCUASSISTREG7)—Offset 44Ch" on page 3058	FFFF0000h



Offset	Register Name (Register Symbol)	Default Value
500–503h	"reg_PCICFGCTR1_type (PCICFGCTR1)—Offset 500h" on page 3058	00000100h
504–507h	"reg_PCICFGCTR2_type (PCICFGCTR2)—Offset 504h" on page 3059	00000100h
508–50Bh	"reg_PCICFGCTR3_type (PCICFGCTR3)—Offset 508h" on page 3060	00000100h
50C–50Fh	"reg_PCICFGCTR4_type (PCICFGCTR4)—Offset 50Ch" on page 3061	00000100h
510–513h	"reg_PCICFGCTR5_type (PCICFGCTR5)—Offset 510h" on page 3062	00000100h
514–517h	"reg_PCICFGCTR6_type (PCICFGCTR6)—Offset 514h" on page 3063	00000100h
518–51Bh	"reg_PCICFGCTR7_type (PCICFGCTR7)—Offset 518h" on page 3064	00000100h
51C–51Fh	"reg_PCICFGCTR8_type (PCICFGCTR8)—Offset 51Ch" on page 3064	00000100h
520–523h	"reg_CHCTRL_type (CHCTRL)—Offset 520h" on page 3065	00000000h
600–603h	"reg_PRI_GEN_REGRW1_type (PRI_GEN_REGRW1)—Offset 600h" on page 3066	00000000h
604–607h	"reg_PRI_GEN_REGRW2_type (PRI_GEN_REGRW2)—Offset 604h" on page 3066	00000000h
608–60Bh	"reg_PRI_GEN_REGRW3_type (PRI_GEN_REGRW3)—Offset 608h" on page 3067	00000000h
60C–60Fh	"reg_PRI_GEN_REGRW4_type (PRI_GEN_REGRW4)—Offset 60Ch" on page 3067	00000000h
610–613h	"reg_PRI_GEN_REGRW5_type (PRI_GEN_REGRW5)—Offset 610h" on page 3068	00000000h
614–617h	"reg_PRI_GEN_REGRW6_type (PRI_GEN_REGRW6)—Offset 614h" on page 3069	00000000h
618–61Bh	"reg_PRI_GEN_REGRW7_type (PRI_GEN_REGRW7)—Offset 618h" on page 3069	00000000h
61C–61Fh	"reg_PRI_GEN_REGRW8_type (PRI_GEN_REGRW8)—Offset 61Ch" on page 3070	00000000h
620–623h	"reg_PRI_GEN_REGRWO1_type (PRI_GEN_REGRWO1)—Offset 620h" on page 3070	00000000h
624–627h	"reg_PRI_GEN_REGRWO2_type (PRI_GEN_REGRWO2)—Offset 624h" on page 3071	00000000h
628–62Bh	"reg_PRI_GEN_REGRWO3_type (PRI_GEN_REGRWO3)—Offset 628h" on page 3072	00000000h
62C–62Fh	"reg_PRI_GEN_REGRWO4_type (PRI_GEN_REGRWO4)—Offset 62Ch" on page 3072	00000000h
630–633h	"reg_PRI_GEN_REGRWO5_type (PRI_GEN_REGRWO5)—Offset 630h" on page 3073	00000000h

Offset	Register Name (Register Symbol)	Default Value
634–637h	"reg_PRI_GEN_REGRWO6_type (PRI_GEN_REGRWO6)—Offset 634h" on page 3073	00000000h
638–63Bh	"reg_PRI_GEN_REGRWO7_type (PRI_GEN_REGRWO7)—Offset 638h" on page 3074	00000000h
63C–63Fh	"reg_PRI_GEN_REGRWO8_type (PRI_GEN_REGRWO8)—Offset 63Ch" on page 3075	00000000h

7.11.1 reg_IOSFCTL_type (IOSFCTL)—Offset 0h

This register controls some of the behaviors of IOSF interface.

Access Method

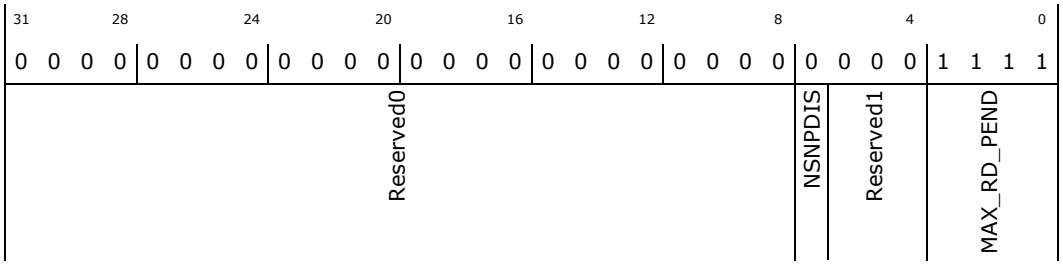
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 0h

Op Codes:

h - Read, h - Write

Default: 0000000Fh



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved.
7	0x0 RW	**NSNPDIS:** Non-snoop Disable. When set, all requests from Bridge on IOSF Primary are snooped. When reset, Bridge obeys MReqInfo attribute on OCP faric to generate snoop or non-snoop transactions.
6:4	0x0 RO	**Reserved1:** Reserved.
3:0	0xf RW	**MAX_RD_PEND:** Maximum number of upstream outstanding reads from Bridge towards IOSF Primary Channel. In reality, number of outstanding read requests towards IOSF could be less than this number depending on resource availability inside IOSF fabric. S/W Programming Model restriction: S/W must ensure there is no upstream DMA traffic is going on when this field is being programmed. Note: This only exists for Channel0. This represents only the upper 4b of the vector. Lowest 2 bits are assumed to be 1's. So max number of reads are x*4+3 where x is the value programmed in this field.

7.11.2 reg_IOSFSTS_type (IOSFSTS)—Offset 8h

This register provides status of some of the events inside OCP Bridge.

Access Method

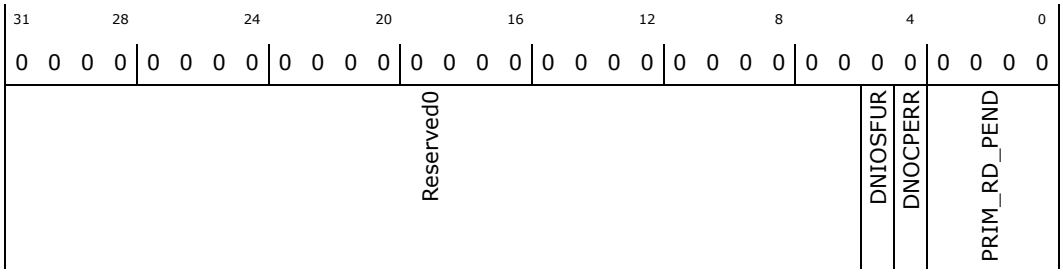
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**Reserved0:** Reserved.
5	0x0 RW/1C	**DNIOSFUR:** Error response received from IOSF for Bridges requests.
4	0x0 RW/1C	**DNOCPERR:** ERR response received from OCP and forwarded to IOSF Primary or Sideband Channels. S/W writes a 1 to clear this
3:0	0x0 RO	**PRIM_RD_PEND:** Number of upstream outstanding reads inside Bridge on IOSF Channel 0. This field does not exist for other IOSF Channels. This field only shows upper 4b of the 6b vector.

7.11.3 reg_OCPCTL_type (OCPCTL)—Offset 10h

This register controls some of the behaviors of OCP interface.

Access Method

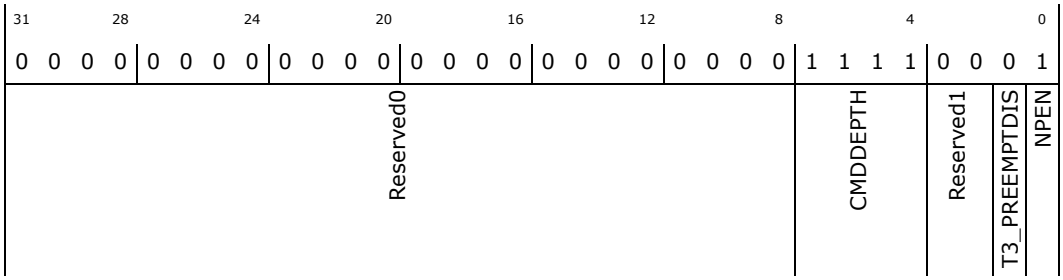
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 10h

Op Codes:

h - Read, h - Write

Default: 000000F1h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0xf RW	**CMDDEPTH:** Effective depth of upstream unified command buffer. Any value more than actual physical depth has no impact on behavior. If this field is programmed with a lesser value, say x, unpstream buffer could have commands upto a max of x + 2. This can be used for debug of performance issues if latency becomes an issue.
3:2	0x0 RO	**Reserved1:** Reserved.
1	0x0 RW	**T3_PREEMPTDIS:** Requests and data transfers on Thread3 are always fixed high priority over requests and data transfers on Thread0. So a Thread3 request can preempt data transfer on Thread0. When this bit is set, Thread3 requests cannot preempt Thread0 data transfers.
0	0x1 RW	**NPEN:** Enable downstream non-posted memory write capability. When clear, Bridge does not generate downstream non-posted memory write requests. When set, all downstream memory write requests are non-posted with exception of those that fall into ranges defined by PWBASE and PWLIMIT registers. S/W could change this bit on the fly while downstream traffic is in progress.

7.11.4 reg_FLSH_type (FLSH)—Offset 20h

This register can be used by OCP agents on Thread 0 to flush any of its writes to global observation point.

Access Method

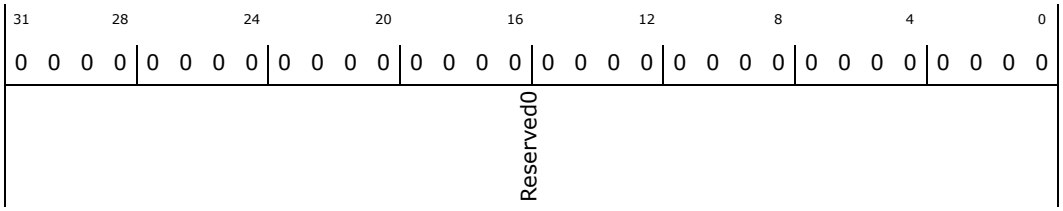
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 20h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved0:** Reserved. This register exists so that agents on OCP fabric can read or write to this register to flush any outstanding transactions in the OCP fabric to Bridge. Read or write to this register does not have any side-effect inside the Bridge and request is terminated gracefully. This register definition also enables firmware or device driver of other IPs to have a permanent hook that it can use to cause a flush. Since all transactions are strictly ordered, any read or write transaction to this register pushes all previous transactions from that agent to the Bridge.

7.11.5 reg_RID_type (RID)—Offset 30h

This register contains Revision ID of Bridge.

Access Method

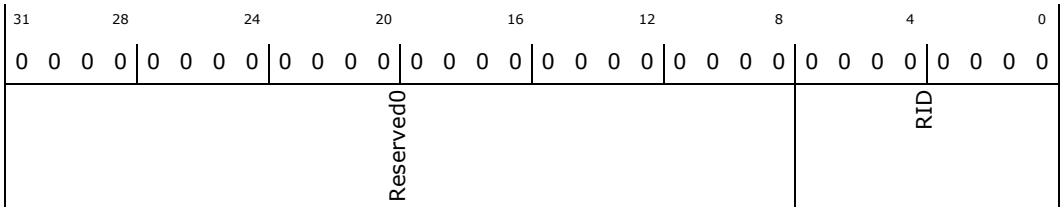
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 30h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved.
7:0	0x0 RO	**RID:** Revision ID of the Bridge.

7.11.6 reg_CAPID_type (CAPID)—Offset 34h

This register describes capabilities of Bridge.

Access Method

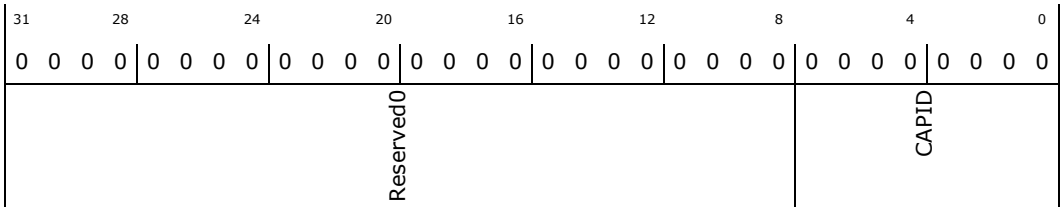
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 34h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved.
7:0	0x0 RO	**CAPID:** For future use.

7.11.7 reg_SPARE_type (SPARE)—Offset 50h

This is a space register.

Access Method

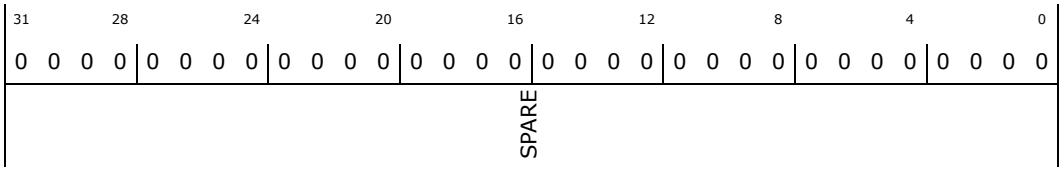
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 50h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SPARE:** This register defines spare configuration bits and reserved for future use

7.11.8 reg_IOSFSBA_type (IOSFSBA)—Offset 60h

There is no physical hardware structure for this register. This is used by SCU to initiated a message on IOSF Sideband Channel. This is same as cDMI_MSG_LNG register with same offset in Langwell for backwards compatibility of SCU firmware. This is a Write-Only location and is accessible only to SCU. A read request to this location by SCU will result in undefined Bridge behavior. This is a 64b register.

Access Method

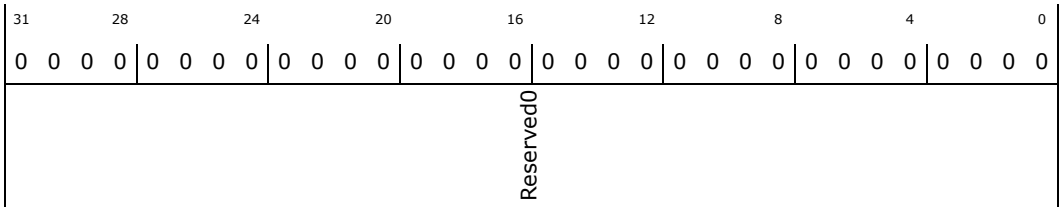
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 60h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved0:** Reserved.

7.11.9 reg_UPARBGNTCNTVC0_type (UPARBGNTCNTVC0)—Offset 68h

This contains Upstream Arbitration Grant counter value for VC0.

Access Method

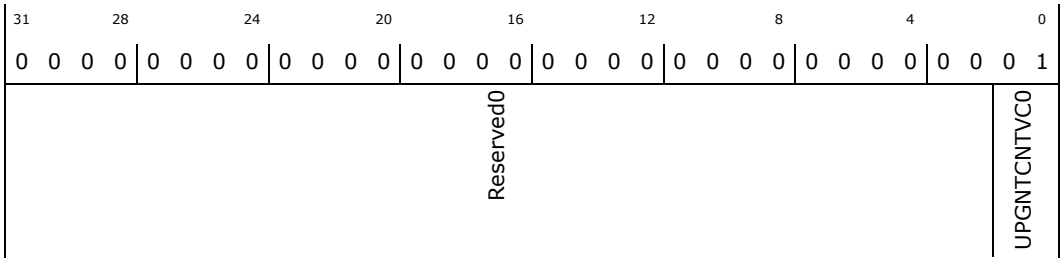
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 68h

Op Codes:

h - Read, h - Write

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved0:** Reserved.
1:0	0x1 RW	**UPGNTCNTVC0:** This determines how many upstream VC0 requests can be launched before a new arbitration session starts. Value of '0' implies no bound, '1' implies 2 requests, '2' implies 4 requests and '3' implies 8 requests.

7.11.10 reg_UPARBGNTCNTVC1_type (UPARBGNTCNTVC1)—Offset 6Ch

This contains Upstream Arbitration Grant counter value for VC1.

Access Method

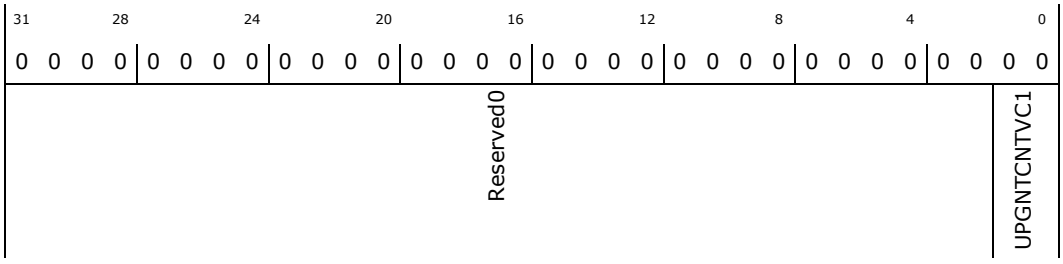
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 6Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved0:** Reserved.
1:0	0x0 RW	**UPGNTCNTVC1:** This determines how many upstream VC1 requests can be launched before it is masked to prevent starvation of lower priority requests. Value of '0' implies no bound, '1' implies 2 requests, '2' implies 4 requests and '3' implies 8 requests.

7.11.11 reg_UPARBGNTCNTVC2_type (UPARBGNTCNTVC2)—Offset 70h

This contains Upstream Arbitration Grant counter value for VC2.

Access Method

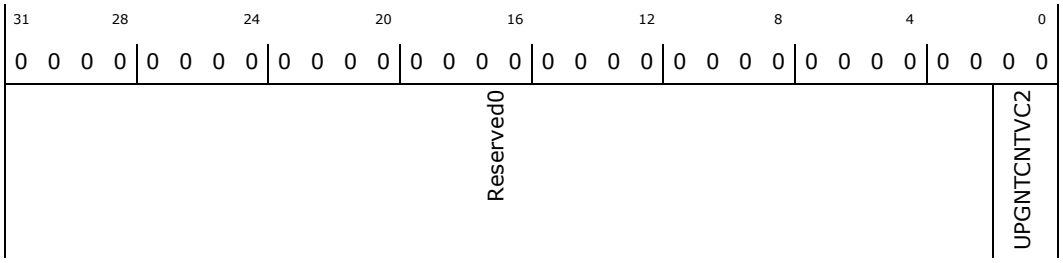
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 70h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved0:** Reserved.
1:0	0x0 RW	**UPGNTCNTVC2:** This determines how many upstream VC2 requests can be launched before it is masked to prevent starvation of lower priority requests. Value of '0' implies no bound, '1' implies 2 requests, '2' implies 4 requests and '3' implies 8 requests.

7.11.12 reg_DNARBGNTCNT_T0_type (DNARBGNTCNT_T0)—Offset 74h

This contains Downstream Arbitration Grant counter value for Thread0.

Access Method

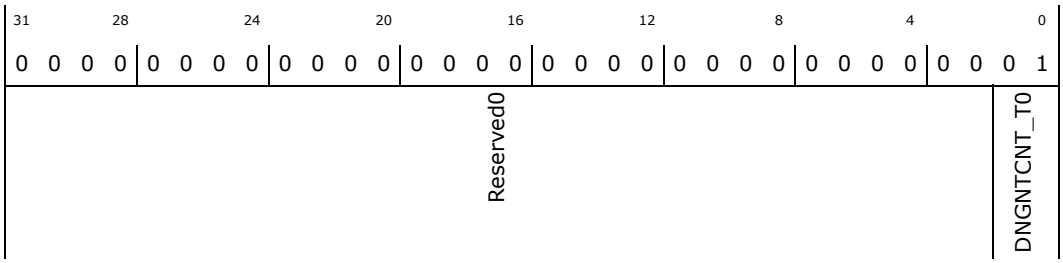
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 74h

Op Codes:

h - Read, h - Write

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved0:** Reserved.
1:0	0x1 RW	**DNGNTCNT_T0:** This determines how many downstream Thread0 data phases can be launched before a new arbitration session starts. Value of '0' implies no bound, '1' implies 8 data phases, '2' implies 16 data phases and '3' implies 24 data phases.

7.11.13 reg_DNARBGNTCNT_T1_type (DNARBGNTCNT_T1)—Offset 78h

This contains Downstream Arbitration Grant counter value for Thread1.

Access Method

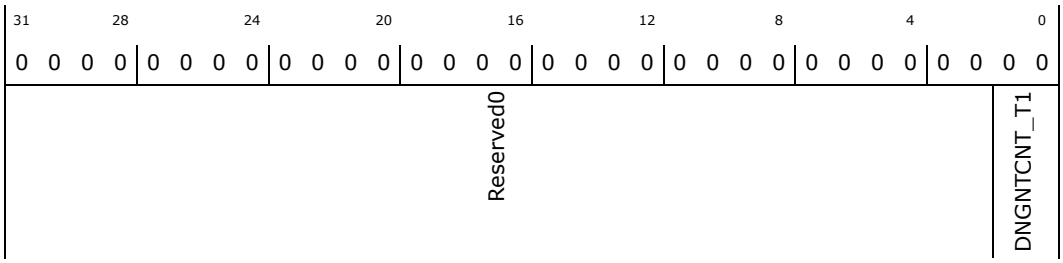
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 78h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved0:** Reserved.
1:0	0x0 RW	**DNGNTCNT_T1:** This determines how many downstream Thread1 data phases can be launched before it is masked to prevent starvation of lower priority responses. Value of '0' implies no bound, '1' implies 8 data phases, '2' implies 16 data phases and '3' implies 24 data phases.

7.11.14 reg_DNARBGNTCNT_T2_type (DNARBGNTCNT_T2)—Offset 7Ch

This contains Downstream Arbitration Grant counter value for Thread2.

Access Method

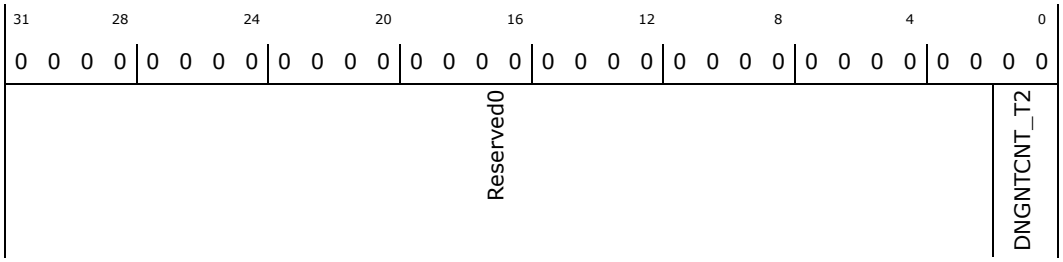
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 7Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved0:** Reserved.
1:0	0x0 RW	**DNGNTCNT_T2:** This determines how many downstream Thread2 data phases can be launched before it is masked to prevent starvation of lower priority responses. Value of '0' implies no bound, '1' implies 8 data phases, '2' implies 16 data phases and '3' implies 24 data phases.

7.11.15 reg_APICBASE_type (APICBASE)—Offset C0h

This register controls IOAPIC related functionality inside Bridge.

Access Method

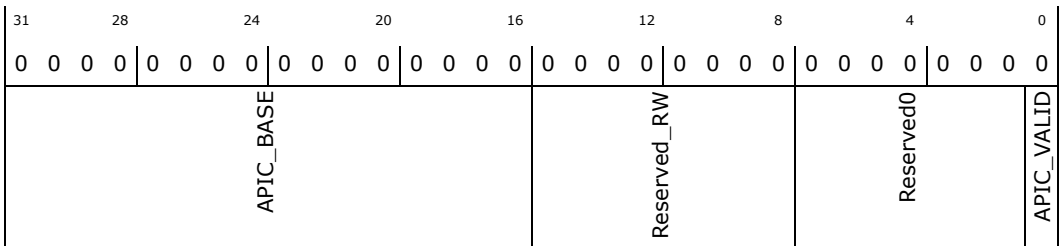
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + C0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**APIC_BASE:** Programmable Base Address for IOAPIC registers
15:8	0x0 RW	**Reserved_RW:** Must be always 0's
7:1	0x0 RO	**Reserved0:** Reserved.
0	0x0 RW	**APIC_VALID:** When set, it indicates IOAPIC support is enabled and address in APIC_BASE is valid.

7.11.16 reg_SRAMBASE_type (SRAMBASE)—Offset C4h

This register controls SRAM related functionality inside Bridge.

Access Method

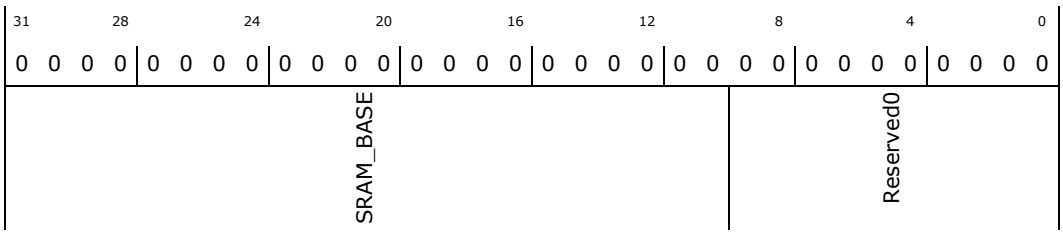
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + C4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**SRAM_BASE:** Programmable Base Address for IOAPIC registers in Shared SRAM
9:0	0x0 RO	**Reserved0:** Reserved.

7.11.17 reg_IOREGSELBASE_type (IOREGSELBASE)—Offset C8h

This register controls IOREGSEL related functionality inside Bridge.

Access Method

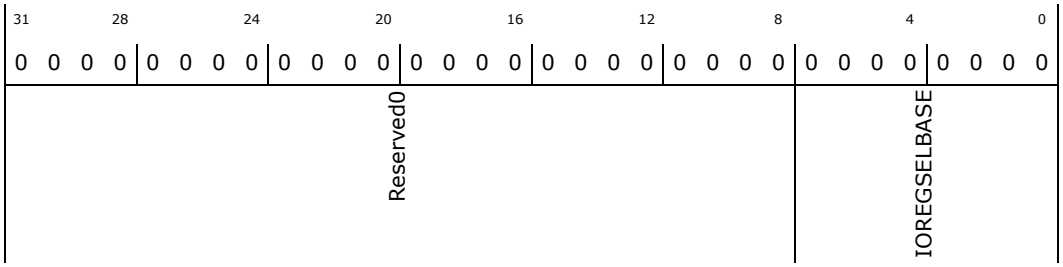
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + C8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved.
7:0	0x0 RW	**IOREGSELBASE:** When a write to IOWIN register occurs, Bridge generates an Interrupt if associated IOREGSEL falls within IOREGSELBASE and IOREGSELLIMIT range and IOWIN_INT_EN is 1.

7.11.18 reg_IOREGSELLIMIT_type (IOREGSELLIMIT)—Offset CCh

This register controls IOREGSEL/IOWIN related functionality inside Bridge.

Access Method

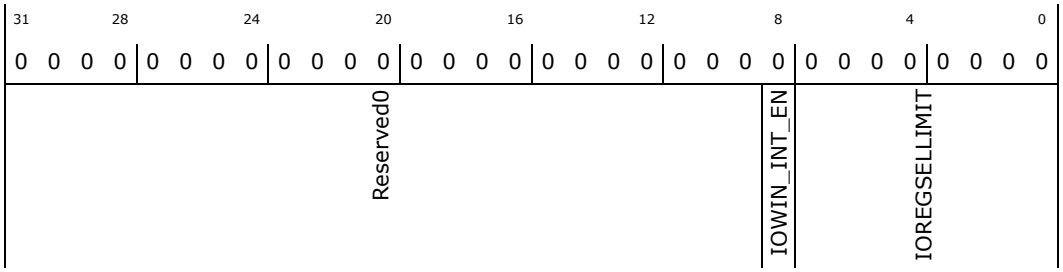
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + CCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**Reserved0:** Reserved.
8	0x0 RW	**IOWIN_INT_EN:** When set, enables generation of Interrupt message to SCU when a write access to APIC IOWIN is made from IOSF Primary Channel and IOREGSEL value falls within IOREGSELBASE and IOREGSELLIMIT values.
7:0	0x0 RW	**IOREGSELLIMIT:** When a write to IOWIN register occurs, Bridge generates an Interrupt if associated IOREGSEL falls within IOREGSELBASE and IOREGSELLIMIT range and IOWIN_INT_EN is 1.

7.11.19 reg_PWBASE0_type (PWBASE0)—Offset 100h

This register contains an address range for downstream posted memory writes.

Access Method

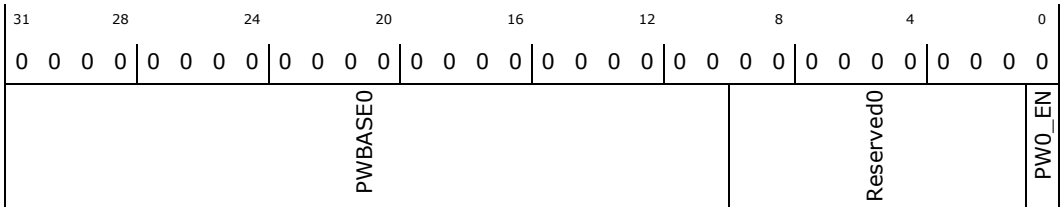
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 100h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**PWBASE0:** Programmable Base Address of 1K memory region to which all downstream memory writes initiated by Bridge towards OCP fabric are launched as posted memory writes. For address comparison purposes, remaining lower bits are assumed to be all 0s. A downstream posted memory write from IOSF will be launched as a downstream posted memory write on OCP fabric if its address is within PWBASE/PWLIMIT range of any of the 4 pairs of registers. Otherwise, the downstream posted memory write is launched as a non-posted memory write on OCP fabric. S/W Programming Model restriction: Address ranges in the four pairs of PWBASE/LIMIT registers can be overlapping. S/W must not update this field when PW0/1/2/3_EN is set.
9:1	0x0 RO	**Reserved0:**
0	0x0 RW	**PW0_EN:** When set, Address region defined by PWBASE0/1/2/3 and PWLIMIT0/1/2/3 is valid. In normal functional mode, all downstream writes are expected to be non-posted and hence, PWBASE and PWLIMIT registers are not used. S/W Programming Model restriction: S/W can change this bit while downstream traffic is in progress.

7.11.20 reg_PWLIMIT0_type (PWLIMIT0)—Offset 104h

This register contains an address range for downstream posted memory writes.

Access Method

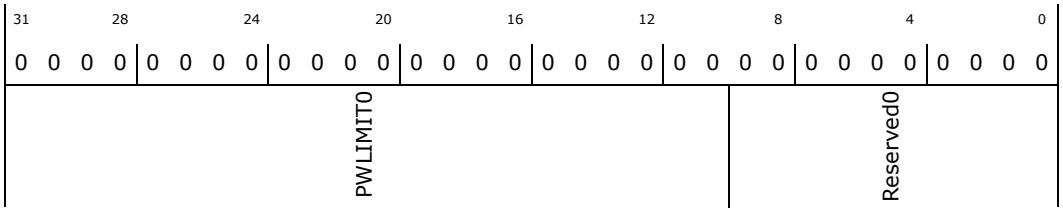
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 104h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**PWLIMIT0:** Programmable Upper Address of 1K memory region to which all downstream writes initiated by Bridge towards OCP fabric are launched as posted memory writes. For address comparison purposes, remaining lower bits are assumed to be all 1s. S/W Programming Model restriction: Address ranges in the four pairs of PWBASE/LIMIT registers can be overlapping. S/W must not update this field when PW0/1/2/3_EN is set
9:0	0x0 RO	**Reserved0:**

7.11.21 reg_PWBASE1_type (PWBASE1)—Offset 108h

This register contains an address range for downstream posted memory writes.

Access Method

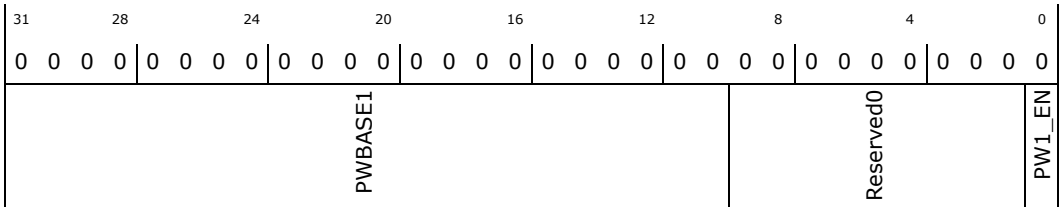
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 108h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**PWBASE1:** Programmable Base Address of 1K memory region to which all downstream writes initiated by Bridge towards OCP fabric are launched as posted memory writes. For address comparison purposes, remaining lower bits are assumed to be all 0s. A downstream posted memory write from IOSF will be launched as a downstream posted memory write on OCP fabric if its address is within PWBASE/PWLIMIT range of any of the 4 pairs of registers. Otherwise, the downstream posted memory write is launched as a non-posted memory write on OCP fabric. S/W Programming Model restriction: Address ranges in the four pairs of PWBASE/LIMIT registers can be overlapping. S/W must not update this field when PW0/1/2/3_EN is set
9:1	0x0 RO	**Reserved0:**

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**PW1_EN:** When set, Address region defined by PWBASE0/1/2/3 and PWLIMIT0/1/2/3 is valid. In normal functional mode, all downstream writes are expected to be non-posted and hence, PWBASE and PWLIMIT registers are not used. S/W Programming Model restriction: S/W can change this bit while downstream traffic is in progress.

7.11.22 reg_PWLIMIT1_type (PWLIMIT1)—Offset 10Ch

This register contains an address range for downstream posted memory writes.

Access Method

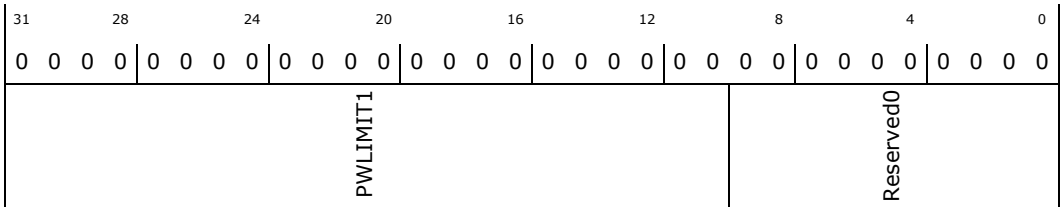
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 10Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**PWLIMIT1:** Programmable Upper Address of 1K memory region to which all downstream writes initiated by Bridge towards OCP fabric are launched as posted memory writes. For address comparison purposes, remaining lower bits are assumed to be all 1s. S/W Programming Model restriction: Address ranges in the four pairs of PWBASE/LIMIT registers can be overlapping. S/W must not update this field when PW0/1/2/3_EN is set.
9:0	0x0 RO	**Reserved0:** Reserved.

7.11.23 reg_PWBASE2_type (PWBASE2)—Offset 110h

This register contains an address range for downstream posted memory writes.

Access Method

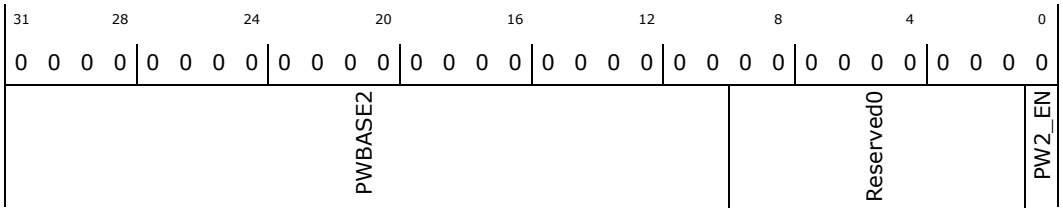
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 110h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**PWBASE2:** Programmable Base Address of 1K memory region to which all downstream writes initiated by Bridge towards OCP fabric are launched as posted memory writes. For address comparison purposes, remaining lower bits are assumed to be all 0s. A downstream posted memory write from IOSF will be launched as a downstream posted memory write on OCP fabric if its address is within PWBASE/PWLIMIT range of any of the 4 pairs of registers. Otherwise, the downstream posted memory write is launched as a non-posted memory write on OCP fabric. S/W Programming Model restriction: Address ranges in the four pairs of PWBASE/LIMIT registers can be overlapping. S/W must not update this field when PW0/1/2/3_EN is set.
9:1	0x0 RO	**Reserved0:**
0	0x0 RW	**PW2_EN:** When set, Address region defined by PWBASE0/1/2/3 and PWLIMIT0/1/2/3 is valid. In normal functional mode, all downstream writes are expected to be non-posted and hence, PWBASE and PWLIMIT registers are not used. S/W Programming Model restriction: S/W can change this bit while downstream traffic is in progress.

7.11.24 reg_PWLIMIT2_type (PWLIMIT2)—Offset 114h

This register contains an address range for downstream posted memory writes.

Access Method

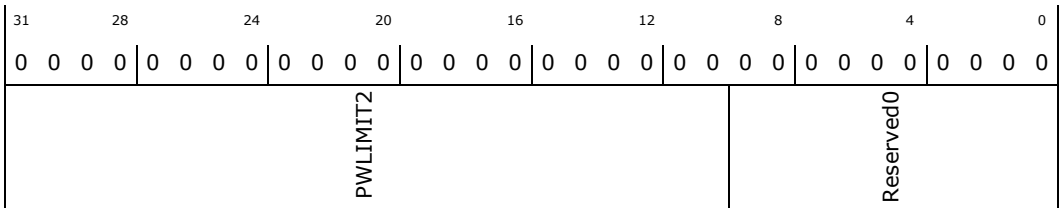
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 114h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**PWLIMIT2:** Programmable Upper Address of 1K memory region to which all downstream writes initiated by Bridge towards OCP fabric are launched as posted memory writes. For address comparison purposes, remaining lower bits are assumed to be all 1s. S/W Programming Model restriction: Address ranges in the four pairs of PWBASE/LIMIT registers can be overlapping. S/W must not update this field when PW0/1/2/3_EN is set.
9:0	0x0 RO	**Reserved0:**

7.11.25 reg_PWBASE3_type (PWBASE3)—Offset 118h

This register contains an address range for downstream posted memory writes.

Access Method

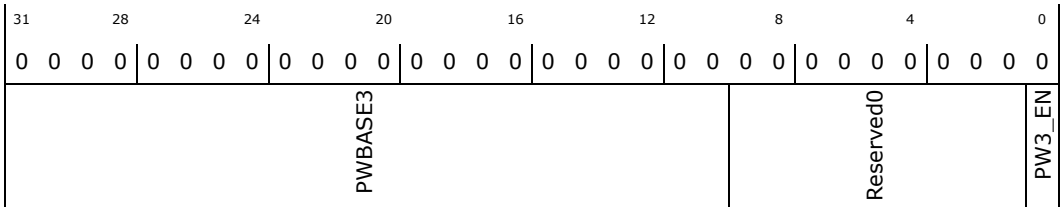
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 118h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**PWBASE3:** Programmable Base Address of 1K memory region to which all downstream writes initiated by Bridge towards OCP fabric are launched as posted memory writes. For address comparison purposes, remaining lower bits are assumed to be all 0s. A downstream posted memory write from IOSF will be launched as a downstream posted memory write on OCP fabric if its address is within PWBASE/PWLIMIT range of any of the 4 pairs of registers. Otherwise, the downstream posted memory write is launched as a non-posted memory write on OCP fabric. S/W Programming Model restriction: Address ranges in the four pairs of PWBASE/LIMIT registers can be overlapping. S/W must not update this field when PW0/1/2/3_EN is set.
9:1	0x0 RO	**Reserved0:**
0	0x0 RW	**PW3_EN:** When set, Address region defined by PWBASE0/1/2/3 and PWLIMIT0/1/2/3 is valid. In normal functional mode, all downstream writes are expected to be non-posted and hence, PWBASE and PWLIMIT registers are not used. S/W Programming Model restriction: S/W can change this bit while downstream traffic is in progress.

7.11.26 reg_PWLIMIT3_type (PWLIMIT3)—Offset 11Ch

This register contains an address range for downstream posted memory writes.

Access Method

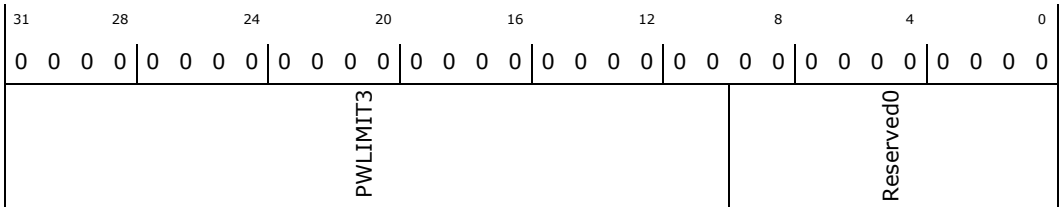
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 11Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**PWLIMIT3:** Programmable Upper Address of 1K memory region to which all downstream writes initiated by Bridge towards OCP fabric are launched as posted memory writes. For address comparison purposes, remaining lower bits are assumed to be all 1s. S/W Programming Model restriction: Address ranges in the four pairs of PWBASE/LIMIT registers can be overlapping. S/W must not update this field when PW0/1/2/3_EN is set.
9:0	0x0 RO	**Reserved0:**

7.11.27 reg_MMIOSCUASSISTREG0_type (MMIOSCUASSISTREG0)—Offset 150h

These Region registers define a set of MMIO ranges that may be handled via SCU assist. The address and size are both 1KB aligned. Each region is enabled by MMIO_SCU_REGION_EN. The regions are used only when MMIO_IPC_EN is set.

Access Method

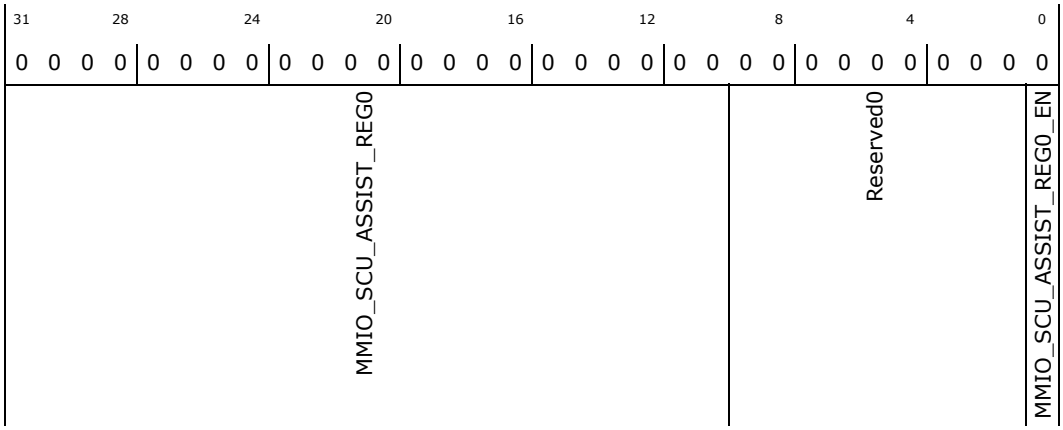
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 150h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**MMIO_SCU_ASSIST_REG0:** Address of 1K size region to which, if an MMIO cycle hits and corresponding MMIO_SCU_REGION_EN 0/1/2/3 is set, the cycle is forwarded to SCU as an IPC message. S/W Programming Model restriction: S/W must not update this field when MMIO_SCU_REGION_EN 0/1/2/3_EN is set.
9:1	0x0 RO	**Reserved0:** Reserved.
0	0x0 RW	**MMIO_SCU_ASSIST_REG0_EN:** When set, Address region defined by MMIO_SCU_ASSIST_REGION 0/1/2/3 is valid. S/W Programming Model restriction: S/W can change this bit while downstream traffic is in progress

7.11.28 reg_MMIOSCUASSISTREG1_type (MMIOSCUASSISTREG1)—Offset 154h

These Region registers define a set of MMIO ranges that may be handled via SCU assist. The address and size are both 1KB aligned. Each region is enabled by MMIO_SCU_REGION_EN. The regions are used only when MMIO_IPC_EN is set.

Access Method

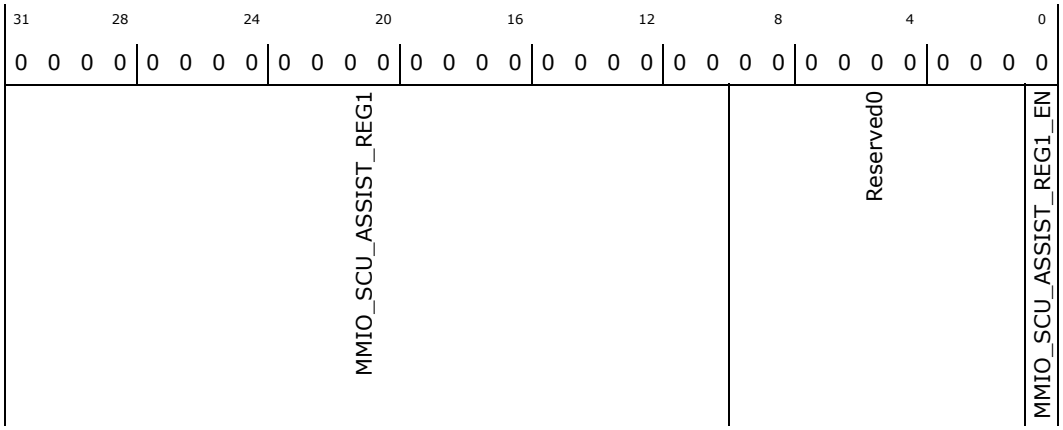
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 154h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**MMIO_SCU_ASSIST_REG1:** Address of 1K size region to which, if an MMIO cycle hits and corresponding MMIO_SCU_REGION_EN 0/1/2/3 is set, the cycle is forwarded to SCU as an IPC message. S/W Programming Model restriction: S/W must not update this field when MMIO_SCU_REGION_EN 0/1/2/3_EN is set.
9:1	0x0 RO	**Reserved0:** Reserved.
0	0x0 RW	**MMIO_SCU_ASSIST_REG1_EN:** When set, Address region defined by MMIO_SCU_ASSIST_REGION 0/1/2/3 is valid. S/W Programming Model restriction: S/W can change this bit while downstream traffic is in progress

7.11.29 reg_MMIOSCUASSISTREG2_type (MMIOSCUASSISTREG2)—Offset 158h

These Region registers define a set of MMIO ranges that may be handled via SCU assist. The address and size are both 1KB aligned. Each region is enabled by MMIO_SCU_REGION_EN. The regions are used only when MMIO_IPC_EN is set.

Access Method

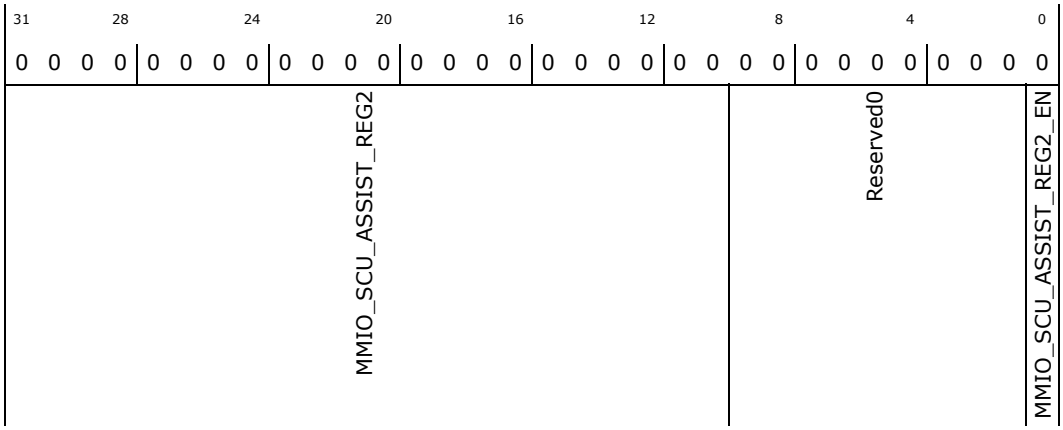
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 158h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**MMIO_SCU_ASSIST_REG2:** Address of 1K size region to which, if an MMIO cycle hits and corresponding MMIO_SCU_REGION_EN 0/1/2/3 is set, the cycle is forwarded to SCU as an IPC message. S/W Programming Model restriction: S/W must not update this field when MMIO_SCU_REGION_EN 0/1/2/3_EN is set.
9:1	0x0 RO	**Reserved0:** Reserved.
0	0x0 RW	**MMIO_SCU_ASSIST_REG2_EN:** When set, Address region defined by MMIO_SCU_ASSIST_REGION 0/1/2/3 is valid. S/W Programming Model restriction: S/W can change this bit while downstream traffic is in progress

7.11.30 reg_MMIOSCUASSISTREG3_type (MMIOSCUASSISTREG3)—Offset 15Ch

These Region registers define a set of MMIO ranges that may be handled via SCU assist. The address and size are both 1KB aligned. Each region is enabled by MMIO_SCU_REGION_EN. The regions are used only when MMIO_IPC_EN is set.

Access Method

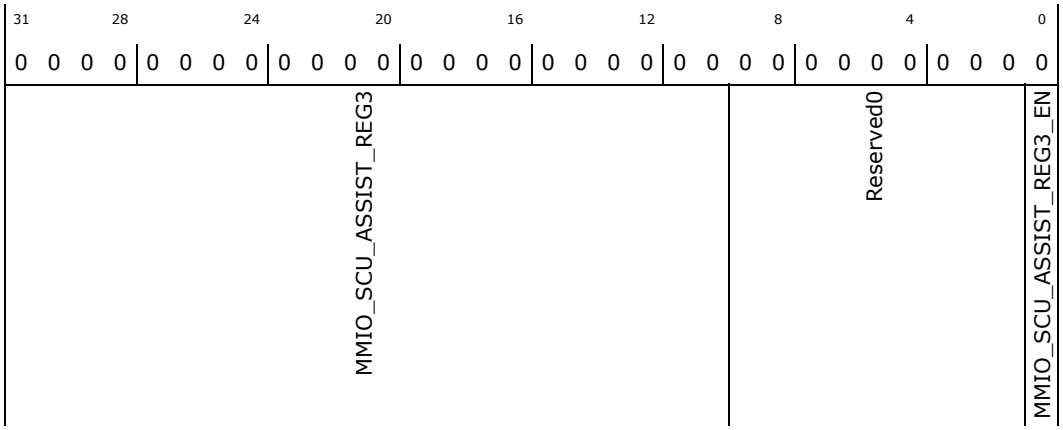
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 15Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**MMIO_SCU_ASSIST_REG3:** Address of 1K size region to which, if an MMIO cycle hits and corresponding MMIO_SCU_REGION_EN 0/1/2/3 is set, the cycle is forwarded to SCU as an IPC message. S/W Programming Model restriction: S/W must not update this field when MMIO_SCU_REGION_EN 0/1/2/3_EN is set.
9:1	0x0 RO	**Reserved0:** Reserved.
0	0x0 RW	**MMIO_SCU_ASSIST_REG3_EN:** When set, Address region defined by MMIO_SCU_ASSIST_REGION 0/1/2/3 is valid. S/W Programming Model restriction: S/W can change this bit while downstream traffic is in progress

7.11.31 reg_PMCTL_type (PMCTL)—Offset 1E0h

This register controls Power Management function of Bridge.

Access Method

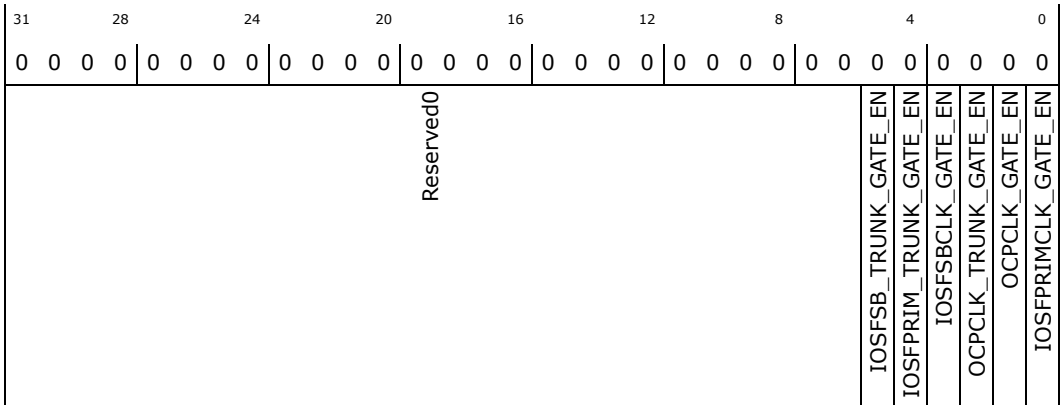
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 1E0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**Reserved0:** Reserved.
5	0x0 RW	**IOSFSB_TRUNK_GATE_EN:** Reserved.
4	0x0 RW	**IOSFPRIM_TRUNK_GATE_EN:** Reserved.
3	0x0 RW	**IOSFSBCLK_GATE_EN:** Reserved.
2	0x0 RW	**OCPCLK_TRUNK_GATE_EN:** Enable OCP clock trunk gating. When set, OCP tunck clock gating functionality is enabled. S/W could change this bit on the fly even when Bridge is servicing cycles.
1	0x0 RW	**OCPCLK_GATE_EN:** Enable OCP clock gating functionality inside Bridge. When set, OCP clock gating functionality is enabled. S/W could change this bit on the fly even when Bridge is servicing cycles
0	0x0 RW	**IOSFPRIMCLK_GATE_EN:** Disable IOSF clock gating functionality inside Bridge. When set, IOSF clock gating functionality is disabled. S/W could change this bit on the fly while downstream traffic is in progress. Note: polarity of this bit is different than that of similar bit for OCP clock.

7.11.32 reg_DEBUGCTL_type (DEBUGCTL)—Offset 200h

This register has bits that controls various debug features.

Access Method

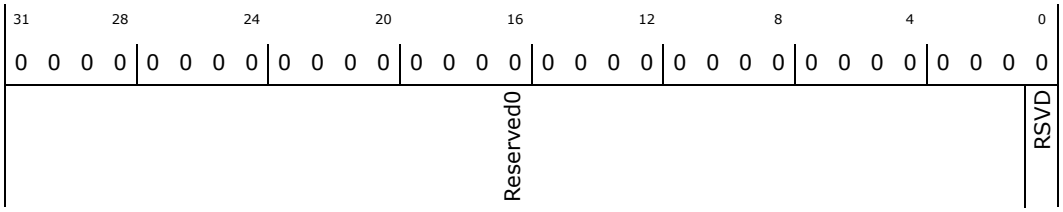
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 200h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**Reserved0:** Reserved.
0	0x0 RO	**Reserved (RSVD):** Reserved.

7.11.33 reg_DEBUGSTS_type (DEBUGSTS)—Offset 280h

Access Method

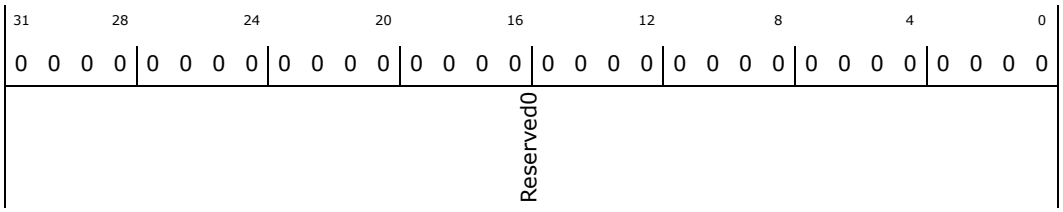
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 280h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved0:** Reserved.

7.11.34 reg_IOCFGCTL_type (IOCFGCTL)—Offset 400h

This register has bits that control various features and mechanisms associated with support for IO and PCI Config cycles functionality. This register is expected to be programmed by SCU during boot time.

Access Method

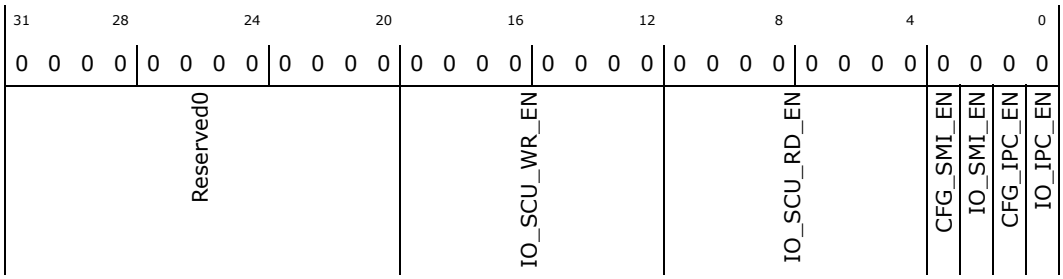
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 400h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**Reserved0:** Reserved.
19:12	0x0 RW	**IO_SCU_WR_EN:** O_SCU_WR_EN: Enable I/O writes that fall in the corresponding IO_SCU_ASSIST_REGION to be handled by the SCU. These bits are only valid when IO_IPC_EN is set. Bit12 corresponds to IO_SCU_ASSIST_REGION0 while bit19 corresponds to IO_SCU_ASSIST_REGION7.
11:4	0x0 RW	**IO_SCU_RD_EN:** IO_SCU_RD_EN: Enable I/O reads that fall in the corresponding IO_SCU_ASSIST_REGION to be handled by the SCU. These bits are only valid when IO_IPC_EN is set. Bit4 corresponds to IO_SCU_ASSIST_REGION0 while bit 11 corresponds to IO_SCU_ASSIST_REGION7.
3	0x0 RW	**CFG_SMI_EN:** When set and when IO_IPC_EN is set, Bridge generates an SMI# as a VLW when SCU writes a Unsuccessful Status (i.e. a 1) in UP_BRIDGE_CMD bit for a Config request. When set and when CFG_IPC_EN is cleared, Bridge generates an SMI# as a VLW when Bridge receives a Config request.
2	0x0 RW	**IO_SMI_EN:** When set and when IO_IPC_EN is set, Bridge generates an SMI# as a VLW when SCU writes a Unsuccessful Status (i.e. a 1) in UP_BRIDGE_CMD bit for an IO request. When set and when IO_IPC_EN is cleared, Bridge generates an SMI# as a VLW when Bridge receives an IO request.
1	0x0 RW	**CFG_IPC_EN:** When set, Bridge sends an IPC message to SCU upon receiving a Config request. When cleared, Bridge returns a completion with Unsuccessful Status on IOSF Primary Channel.
0	0x0 RW	**IO_IPC_EN:** When set, Bridge sends an IPC message to SCU upon receiving an IO request. When cleared, Bridge returns a completion with Unsuccessful Status on IOSF Primary Channel.

7.11.35 reg_UPBRIDGEDATA_type (UPBRIDGEDATA)—Offset 408h

The 32b UP_BRIDGE_DATA is written to by SCU via Thread3 and contains data associated with command written to UP_BRIDGE_CMD register. SCU writes to this register on Thread3 as part of actions it takes for IO or Config read request. When completion status is Successful, Bridge returns this as read data along with IO or Config read completion. It is expected as part of normal usage model that IA never writes or reads this register - though there is no hardware to prevent this. A read to this register from OCP Fabric results in undefined behavior.

Access Method

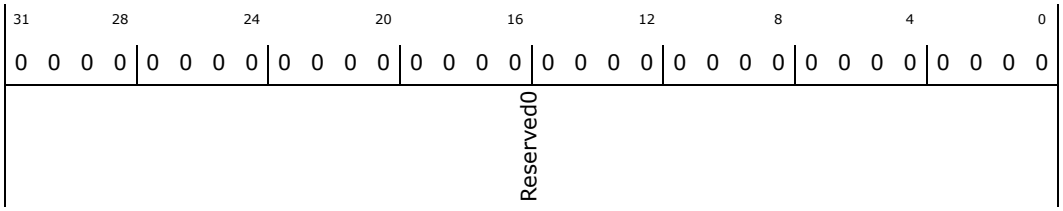
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 408h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved0:** Reserved.

7.11.36 reg_UPBRIDGECMD_type (UPBRIDGECMD)—Offset 410h

This register is written to by SCU and contains command for the Bridge. A read to this register from OCP fabric results in undefined behavior

Access Method

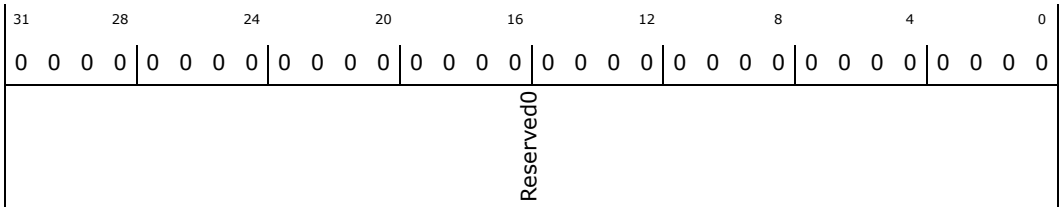
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 410h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 WO	**Reserved0:** SCU writes to this register on Thread3 as part of actions it takes for IO or Config read request. 0x00: Indicates Bridge should return a completion with Successful status for the IO or Config request. 0x01: Indicates Bridge should return a completion with Unsuccessful status for the IO or Config request. Other encodings are reserved. It is expected as part of normal usage model that IA never writes or reads this register - though there is no hardware to prevent this.

7.11.37 reg_ILBCTL_type (ILBCTL)—Offset 414h

This register has bits that control various features and mechanisms associated ILB (Intel Legacy Block). This register is expected to be programmed by SCU during boot time.

Access Method

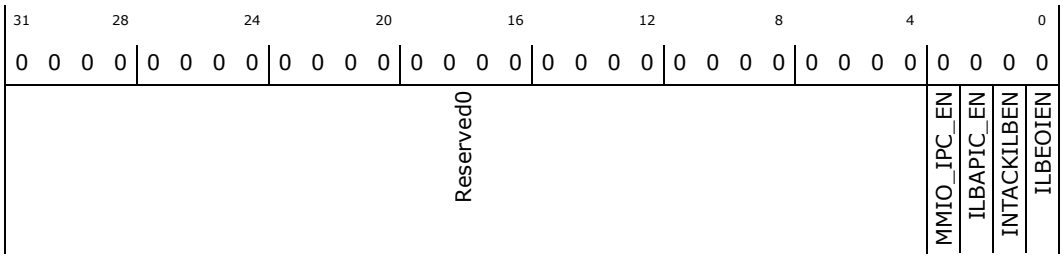
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 414h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved0:** Reserved.
3	0x0 RW	**MMIO_IPC_EN:** When set, Bridge sends an IPC message to SCU upon receiving a MMIO request that hits an enabled regions defined by MMIO_SCU_REGION registers.
2	0x0 RW	**ILBAPIC_EN:** When set, APIC requests are not forwarded to SCU but sent to ILB on Thread0. When reset, APIC requests are forwarded to SCU.
1	0x0 RW	**INTACKILBEN:** When set, Bridge forwards INT_ACK from IA towards ILB on Thread 0 of OCP Fabric. This behavior is independent of setting of IO_IPC_EN bit. When reset, Bridge may forward INT_ACK towards SCU as IPC message if IO_IPC_EN = 1 and IO_SMI_EN = 0.
0	0x0 RW	**ILBEOIEN:** When set, Bridge forwards EOI from IOSF Primary as a memory write on Thread 0 towards ILB on OCP fabric. When reset, Bridge forwards EOI as an IPC to SCU.

7.11.38 reg_INTACKBASE_type (INTACKBASE)—Offset 418h

This register provides memory address to which OCP Bridge forwards INT_ACK cycle from IA as a 1B memory read request. This register is expected to be programmed by SCU during boot time.

Access Method

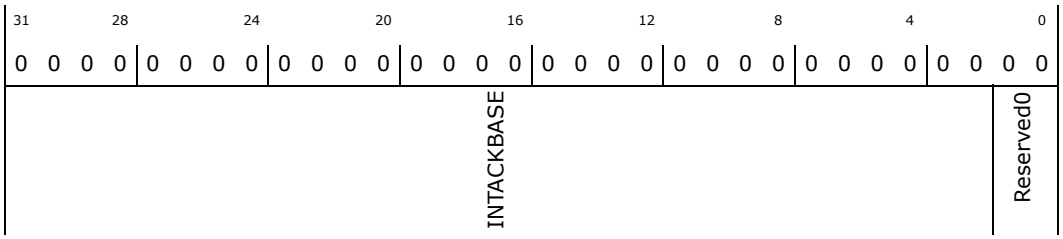
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 418h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**INTACKBASE:** Base memory address to which INT_ACK from IA would be forwarded to as a 1B memory read request. SW Programming Model restriction: Even though register is RW until address bit 2, it is expected that this register would be aligned to 4K address boundary.
1:0	0x0 RO	**Reserved0:** Reserved.

7.11.39 reg_SMICMD_type (SMICMD)—Offset 420h

Bridge stores the command that caused SMI#.

Access Method

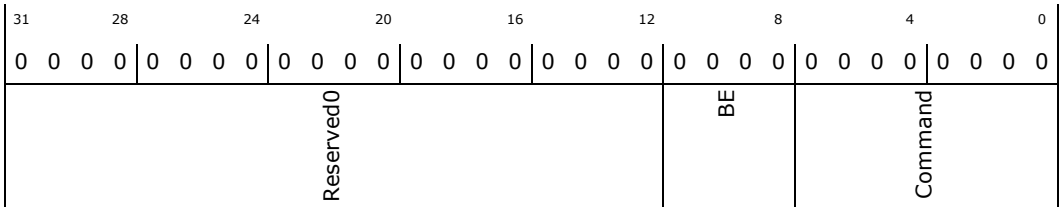
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 420h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x0 RO	**BE:** Bridges stores, in this field, active high First DW Byte Enables associated with the IO or Config request that caused the SMI.
7:0	0x0 RO	**Command:** Bridges stores, in this field, IO or Config request that caused the SMI. Encodings: 0x00: IO read 0x01: IO write 0x02: Config Type0 read 0x03: Config Type0 write 0x04: Config Type1 read 0x05: Config Type1 write

7.11.40 reg_SMIADDR_type (SMIADDR)—Offset 424h

Bridge stores the address of the IO or Config request that caused the SMI#.

Access Method

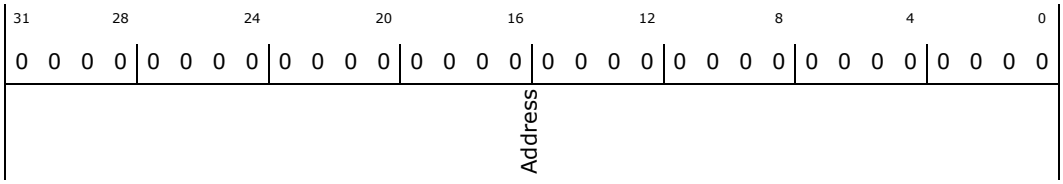
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 424h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Address:** Bridges stores, in this field, address of the IO or Config request that caused the SMI. In case of an IO request, only lower 16b are valid. For Config requests, see table above for information conveyed by various address fields.

7.11.41 reg_SMIDATA_type (SMIDATA)—Offset 428h

Bridge stores the data associated with the IO or Config request that caused the SMI#.

Access Method

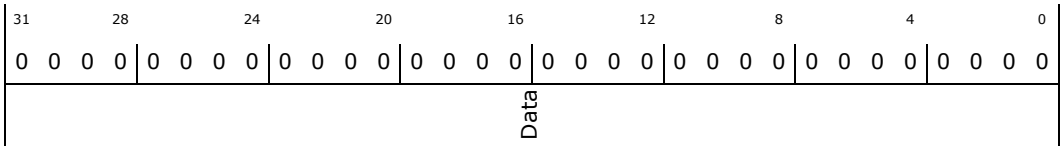
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 428h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Data:** Bridges stores, in this field, data of the IO or Config request that caused the SMI.

7.11.42 reg_SMISTS_type (SMISTS)—Offset 42Ch

Bridge stores the status of SMI#. Refer section Detailed flow of emulation of legacy IO and Config Cycles

Access Method

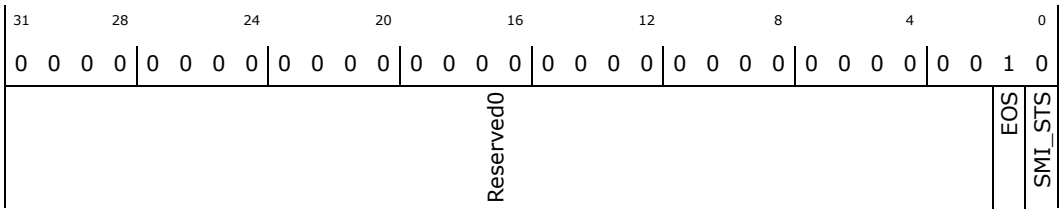
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 42Ch

Op Codes:

h - Read, h - Write

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved0:** Reserved.
1	0x1 RW/S	**EOS:** End of SMI#. Bridge clears this bit when it launches an SMI#. IA-CPU writes a 1 to this bit to set it
0	0x0 RW/1C	**SMI_STS:** This bit is set by h/w. When set and EOS bit is also set, Bridge launches an SMI# on IOSF Sideband Channel. IA-CPU writes a 1 to this bit to clear the bit.

7.11.43 reg_IOSCUASSISTREG0_type (IOSCUASSISTREG0)—Offset 430h

These Region registers define a set of I/O ranges that may be handled via SCU assist. The address is byte granular and the range may be from 1 Byte to the entire 64KB I/O address range. The regions are enabled when IO_IPC_EN is set, IO_SMI_EN is clear and: For writes, corresponding IOCFGCTL. IO_SCU_WR_EN is set For reads, corresponding IOCFGCTL. IO_SCU_RD_EN is set These registers are byte granular. If all the enabled bytes in the incoming IO Cycle fall wholly within the defined region, the IO cycle is a candidate for trapping. If SCU Assist is enabled, and the cycle does not match any of the region registers, it is forwarded onto the ILB - see section on IO and Config handling for PC-Linux support.

Access Method

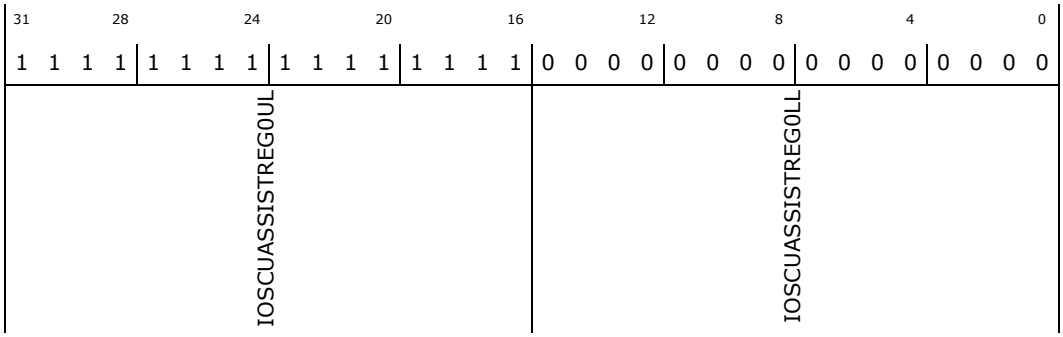
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 430h

Op Codes:

h - Read, h - Write

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RW	**IOSCUASSISTREG0UL:** IO_SCU_ASSIST_REGION_U0: Upper IO Address for Region 0/1/2/3/4/5/6/7
15:0	0x0 RW	**IOSCUASSISTREG0LL:** IO_SCU_ASSIST_REGION_L0: Lower IO Address for Region 0/1/2/3/4/5/6/7

7.11.44 reg_IOSCUASSISTREG1_type (IOSCUASSISTREG1)—Offset 434h

These Region registers define a set of I/O ranges that may be handled via SCU assist. The address is byte granular and the range may be from 1 Byte to the entire 64KB I/O address range. The regions are enabled when IO_IPC_EN is set, IO_SMI_EN is clear and: For writes, corresponding IOCFGCTL. IO_SCU_WR_EN is set For reads, corresponding IOCFGCTL. IO_SCU_RD_EN is set These registers are byte granular. If all the enabled bytes in the incoming IO Cycle fall wholly within the defined region, the IO cycle is a candidate for trapping. If SCU Assist is enabled, and the cycle does not match any of the region registers, it is forwarded onto the ILB - see section on IO and Config handling for PC-Linux support.

Access Method

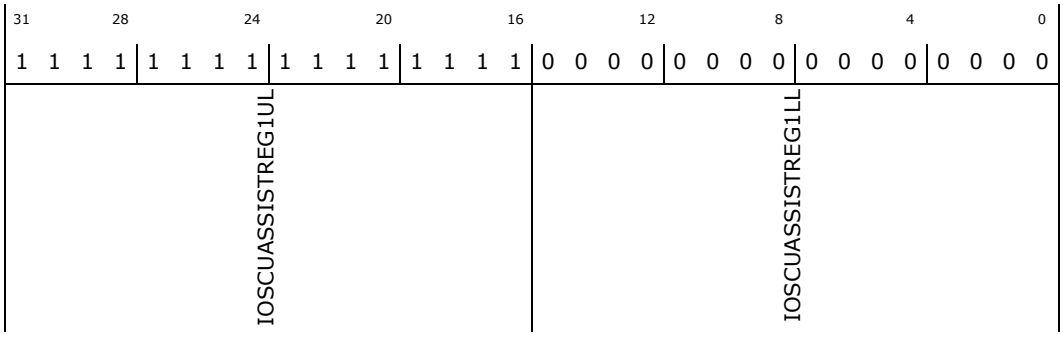
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 434h

Op Codes:

h - Read, h - Write

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RW	**IOSCUASSISTREG1UL:** IO_SCU_ASSIST_REGION_U0: Upper IO Address for Region 0/1/2/3/4/5/6/7
15:0	0x0 RW	**IOSCUASSISTREG1LL:** IO_SCU_ASSIST_REGION_L0: Lower IO Address for Region 0/1/2/3/4/5/6/7

7.11.45 reg_IOSCUASSISTREG2_type (IOSCUASSISTREG2)—Offset 438h

These Region registers define a set of I/O ranges that may be handled via SCU assist. The address is byte granular and the range may be from 1 Byte to the entire 64KB I/O address range. The regions are enabled when IO_IPC_EN is set, IO_SMI_EN is clear and: For writes, corresponding IOCFGCTL. IO_SCU_WR_EN is set For reads, corresponding IOCFGCTL. IO_SCU_RD_EN is set These registers are byte granular. If all the enabled bytes in the incoming IO Cycle fall wholly within the defined region, the IO cycle is a candidate for trapping. If SCU Assist is enabled, and the cycle does not match any of the region registers, it is forwarded onto the ILB - see section on IO and Config handling for PC-Linux support.

Access Method

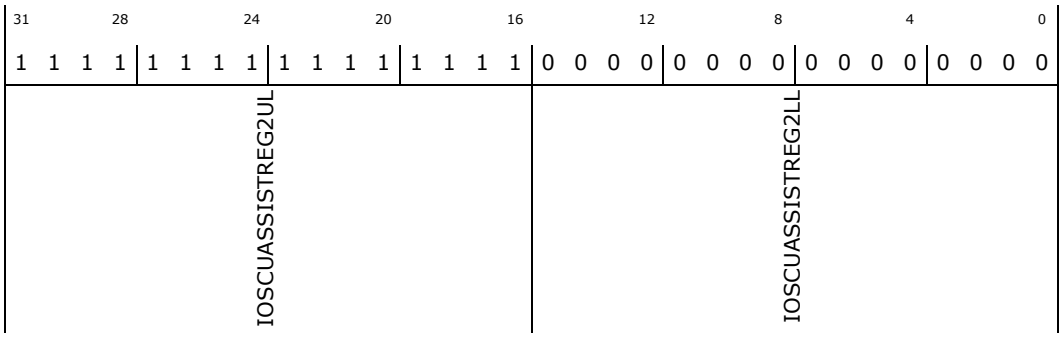
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 438h

Op Codes:

h - Read, h - Write

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RW	**IOSCUASSISTREG2UL:** IO_SCU_ASSIST_REGION_U0: Upper IO Address for Region 0/1/2/3/4/5/6/7
15:0	0x0 RW	**IOSCUASSISTREG2LL:** IO_SCU_ASSIST_REGION_L0: Lower IO Address for Region 0/1/2/3/4/5/6/7

7.11.46 reg_IOSCUASSISTREG3_type (IOSCUASSISTREG3)—Offset 43Ch

These Region registers define a set of I/O ranges that may be handled via SCU assist. The address is byte granular and the range may be from 1 Byte to the entire 64KB I/O address range. The regions are enabled when IO_IPC_EN is set, IO_SMI_EN is clear and: For writes, corresponding IOCFGCTL. IO_SCU_WR_EN is set For reads, corresponding IOCFGCTL. IO_SCU_RD_EN is set These registers are byte granular. If all the enabled bytes in the incoming IO Cycle fall wholly within the defined region, the IO cycle is a candidate for trapping. If SCU Assist is enabled, and the cycle does not match any of the region registers, it is forwarded onto the ILB - see section on IO and Config handling for PC-Linux support.

Access Method

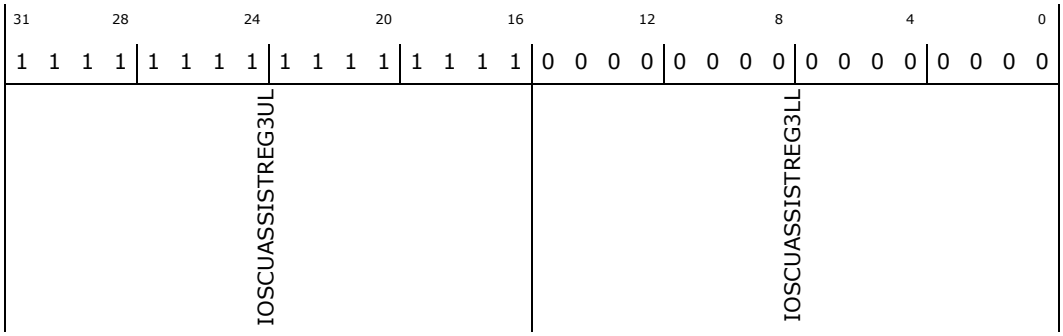
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 43Ch

Op Codes:

h - Read, h - Write

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RW	**IOSCUASSISTREG3UL:** IO_SCU_ASSIST_REGION_U0: Upper IO Address for Region 0/1/2/3/4/5/6/7
15:0	0x0 RW	**IOSCUASSISTREG3LL:** IO_SCU_ASSIST_REGION_L0: Lower IO Address for Region 0/1/2/3/4/5/6/7

7.11.47 reg_IOSCUASSISTREG4_type (IOSCUASSISTREG4)—Offset 440h

These Region registers define a set of I/O ranges that may be handled via SCU assist. The address is byte granular and the range may be from 1 Byte to the entire 64KB I/O address range. The regions are enabled when IO_IPC_EN is set, IO_SMI_EN is clear and: For writes, corresponding IOCFGCTL. IO_SCU_WR_EN is set For reads, corresponding IOCFGCTL. IO_SCU_RD_EN is set These registers are byte granular. If all the enabled bytes in the incoming IO Cycle fall wholly within the defined region, the

IO cycle is a candidate for trapping. If SCU Assist is enabled, and the cycle does not match any of the region registers, it is forwarded onto the ILB - see section on IO and Config handling for PC-Linux support.

Access Method

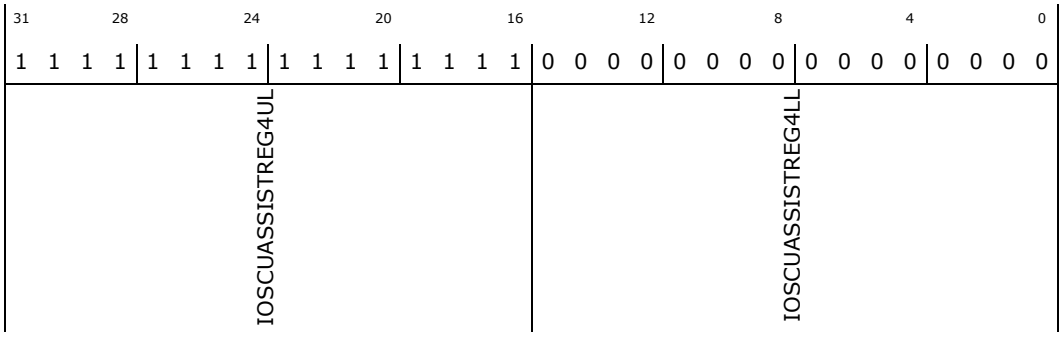
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 440h

Op Codes:

h - Read, h - Write

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RW	**IOSCUASSISTREG4UL:** IO_SCU_ASSIST_REGION_U0: Upper IO Address for Region 0/1/2/3/4/5/6/7
15:0	0x0 RW	**IOSCUASSISTREG4LL:** IO_SCU_ASSIST_REGION_L0: Lower IO Address for Region 0/1/2/3/4/5/6/7

7.11.48 reg_IOSCUASSISTREG5_type (IOSCUASSISTREG5)—Offset 444h

These Region registers define a set of I/O ranges that may be handled via SCU assist. The address is byte granular and the range may be from 1 Byte to the entire 64KB I/O address range. The regions are enabled when IO_IPC_EN is set, IO_SMI_EN is clear and: For writes, corresponding IOCFGCTL. IO_SCU_WR_EN is set For reads, corresponding IOCFGCTL. IO_SCU_RD_EN is set These registers are byte granular. If all the enabled bytes in the incoming IO Cycle fall wholly within the defined region, the IO cycle is a candidate for trapping. If SCU Assist is enabled, and the cycle does not match any of the region registers, it is forwarded onto the ILB - see section on IO and Config handling for PC-Linux support.

Access Method

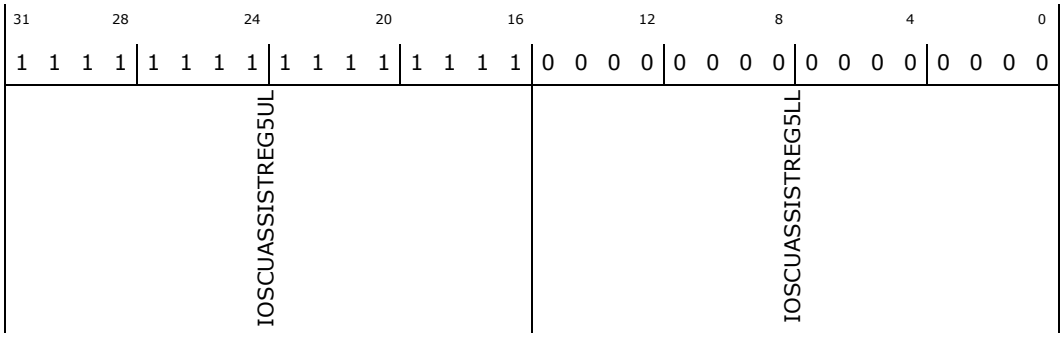
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 444h

Op Codes:

h - Read, h - Write

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RW	**IOSCUASSISTREG5UL:** IO_SCU_ASSIST_REGION_U0: Upper IO Address for Region 0/1/2/3/4/5/6/7
15:0	0x0 RW	**IOSCUASSISTREG5LL:** IO_SCU_ASSIST_REGION_L0: Lower IO Address for Region 0/1/2/3/4/5/6/7

7.11.49 reg_IOSCUASSISTREG6_type (IOSCUASSISTREG6)—Offset 448h

These Region registers define a set of I/O ranges that may be handled via SCU assist. The address is byte granular and the range may be from 1 Byte to the entire 64KB I/O address range. The regions are enabled when IO_IPC_EN is set, IO_SMI_EN is clear and: For writes, corresponding IOCFGCTL. IO_SCU_WR_EN is set For reads, corresponding IOCFGCTL. IO_SCU_RD_EN is set These registers are byte granular. If all the enabled bytes in the incoming IO Cycle fall wholly within the defined region, the IO cycle is a candidate for trapping. If SCU Assist is enabled, and the cycle does not match any of the region registers, it is forwarded onto the ILB - see section on IO and Config handling for PC-Linux support.

Access Method

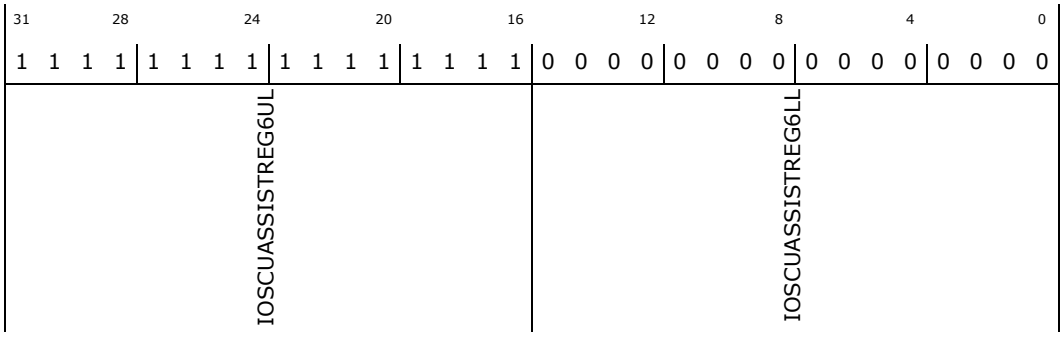
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 448h

Op Codes:

h - Read, h - Write

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RW	**IOSCUASSISTREG6UL:** IO_SCU_ASSIST_REGION_U0: Upper IO Address for Region 0/1/2/3/4/5/6/7
15:0	0x0 RW	**IOSCUASSISTREG6LL:** IO_SCU_ASSIST_REGION_L0: Lower IO Address for Region 0/1/2/3/4/5/6/7

7.11.50 reg_IOSCUASSISTREG7_type (IOSCUASSISTREG7)—Offset 44Ch

These Region registers define a set of I/O ranges that may be handled via SCU assist. The address is byte granular and the range may be from 1 Byte to the entire 64KB I/O address range. The regions are enabled when IO_IPC_EN is set, IO_SMI_EN is clear and: For writes, corresponding IOCFGCTL. IO_SCU_WR_EN is set For reads, corresponding IOCFGCTL. IO_SCU_RD_EN is set These registers are byte granular. If all the enabled bytes in the incoming IO Cycle fall wholly within the defined region, the IO cycle is a candidate for trapping. If SCU Assist is enabled, and the cycle does not match any of the region registers, it is forwarded onto the ILB - see section on IO and Config handling for PC-Linux support.

Access Method

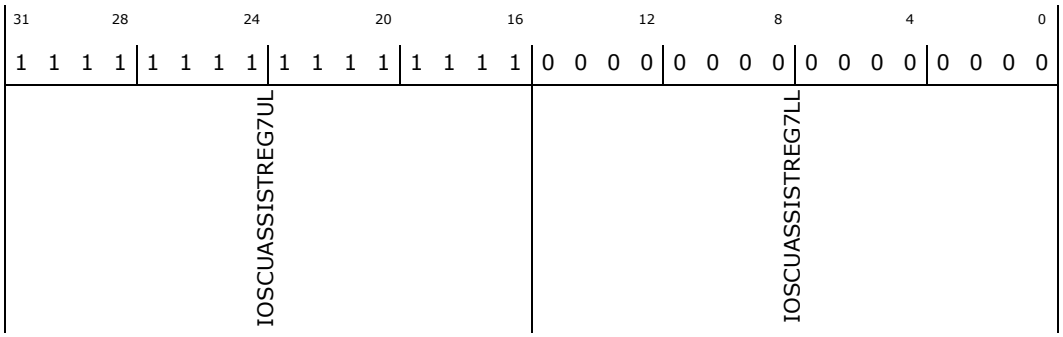
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 44Ch

Op Codes:

h - Read, h - Write

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RW	**IOSCUASSISTREG7UL:** IO_SCU_ASSIST_REGION_U0: Upper IO Address for Region 0/1/2/3/4/5/6/7
15:0	0x0 RW	**IOSCUASSISTREG7LL:** IO_SCU_ASSIST_REGION_L0: Lower IO Address for Region 0/1/2/3/4/5/6/7

7.11.51 reg_PCICFGCTR1_type (PCICFGCTR1)—Offset 500h

This register defines functionality for PCI Config space 1

Access Method

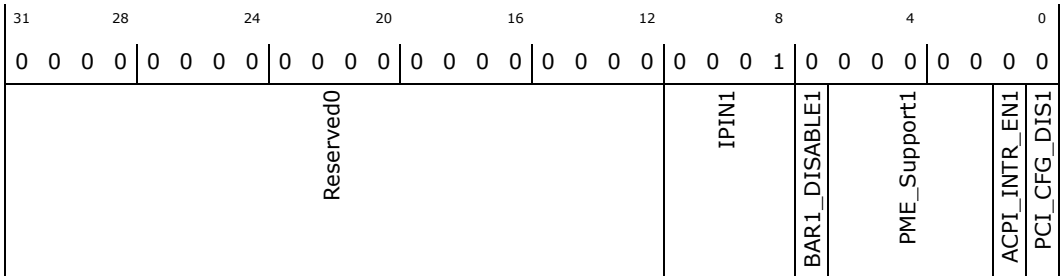
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 500h

Op Codes:

h - Read, h - Write

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x1 RW	**IPIN1:** This register indicates the value to be reflected in the IPIN register of the PCI configuration space. 0- No Interrupt, 1- INTA, 2-INTB, 3-INTC, 4-INTD
7	0x0 RW	**BAR1_DISABLE1:** BAR1 register in the PCI config space will become read only 0 when this bit is set, else this register will be RW. This bit also affects decode for BAR1 accesses
6:2	0x0 RW	**PME_Support1:** The value in this register will be XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space. This register can be used as a mechanism to change the value of the PME_Status PCI config register field
1	0x0 RW	**ACPI_INTR_EN1:** When set, Bridge will use ACPI SB opcodes for messages. When cleared, Bridge will use global IOSF opcodes
0	0x0 RW	**PCI_CFG_DIS1:** When set, PCI configuration accesses return UR response. When 0, PCI configuration accesses are supported

7.11.52 reg_PCICFGCTR2_type (PCICFGCTR2)—Offset 504h

This register defines functionality for PCI Config space 1

Access Method

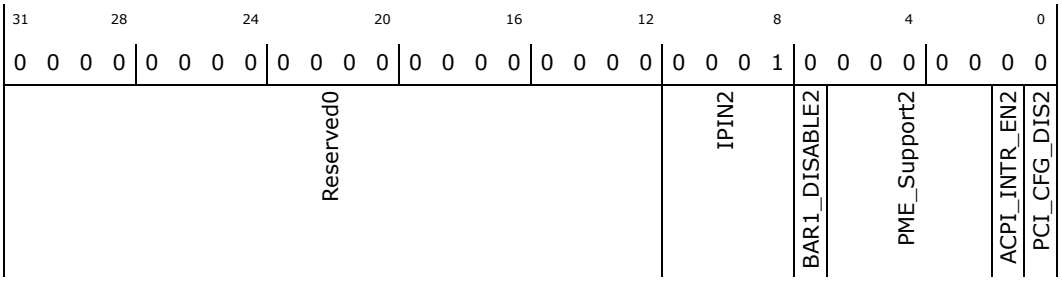
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 504h

Op Codes:

h - Read, h - Write

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x1 RW	**IPIN2:** This register indicates the value to be reflected in the IPIN register of the PCI configuration space. 0- No Interrupt, 1- INTA, 2-INTB, 3-INTC, 4-INTD
7	0x0 RW	**BAR1_DISABLE2:** BAR1 register in the PCI config space will become read only 0 when this bit is set, else this register will be RW. This bit also affects decode for BAR1 accesses
6:2	0x0 RW	**PME_Support2:** The value in this register will be XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space. This register can be used as a mechanism to change the value of the PME_Status PCI config register field
1	0x0 RW	**ACPI_INTR_EN2:** When set, Bridge will use ACPI SB opcodes for messages. When cleared, Bridge will use global IOSF opcodes
0	0x0 RW	**PCI_CFG_DIS2:** When set, PCI configuration accesses return UR response. When 0, PCI configuration accesses are supported

7.11.53 reg_PCICFGCTR3_type (PCICFGCTR3)—Offset 508h

This register defines functionality for PCI Config space 1

Access Method

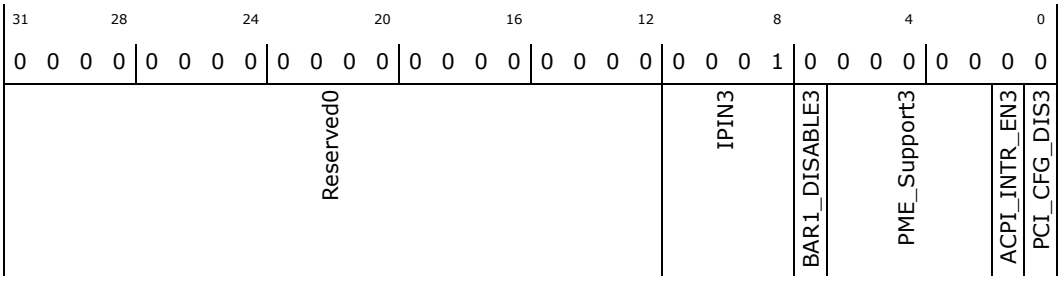
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 508h

Op Codes:

h - Read, h - Write

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x1 RW	**IPIN3:** This register indicates the value to be reflected in the IPIN register of the PCI configuration space. 0- No Interrupt, 1- INTA, 2-INTB, 3-INTC, 4-INTD
7	0x0 RW	**BAR1_DISABLE3:** BAR1 register in the PCI config space will become read only 0 when this bit is set, else this register will be RW. This bit also affects decode for BAR1 accesses
6:2	0x0 RW	**PME_Support3:** The value in this register will be XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space. This register can be used as a mechanism to change the value of the PME_Status PCI config register field
1	0x0 RW	**ACPI_INTR_EN3:** When set, Bridge will use ACPI SB opcodes for messages. When cleared, Bridge will use global IOSF opcodes
0	0x0 RW	**PCI_CFG_DIS3:** When set, PCI configuration accesses return UR response. When 0, PCI configuration accesses are supported

7.11.54 reg_PCICFGCTR4_type (PCICFGCTR4)—Offset 50Ch

This register defines functionality for PCI Config space 1

Access Method

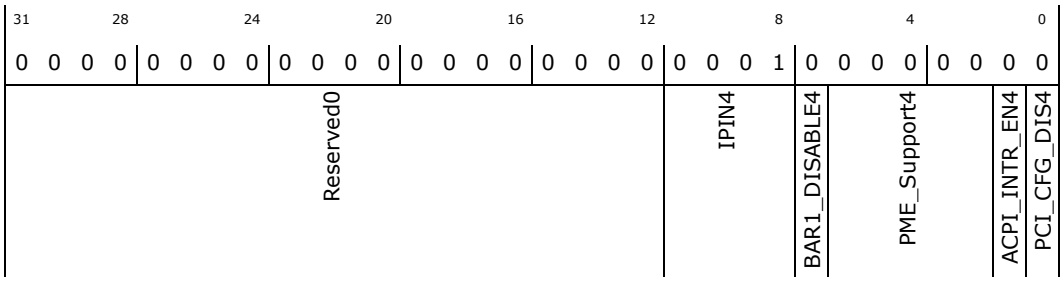
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 50Ch

Op Codes:

h - Read, h - Write

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x1 RW	**IPIN4:** This register indicates the value to be reflected in the IPIN register of the PCI configuration space. 0- No Interrupt, 1- INTA, 2-INTB, 3-INTC, 4-INTD

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW	**BAR1_DISABLE4:** BAR1 register in the PCI config space will become read only 0 when this bit is set, else this register will be RW. This bit also affects decode for BAR1 accesses
6:2	0x0 RW	**PME_Support4:** The value in this register will be XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space. This register can be used as a mechanism to change the value of the PME_Status PCI config register field
1	0x0 RW	**ACPI_INTR_EN4:** When set, Bridge will use ACPI SB opcodes for messages. When cleared, Bridge will use global IOSF opcodes
0	0x0 RW	**PCI_CFG_DIS4:** When set, PCI configuration accesses return UR response. When 0, PCI configuration accesses are supported

7.11.55 reg_PCICFGCTR5_type (PCICFGCTR5)—Offset 510h

This register defines functionality for PCI Config space 1

Access Method

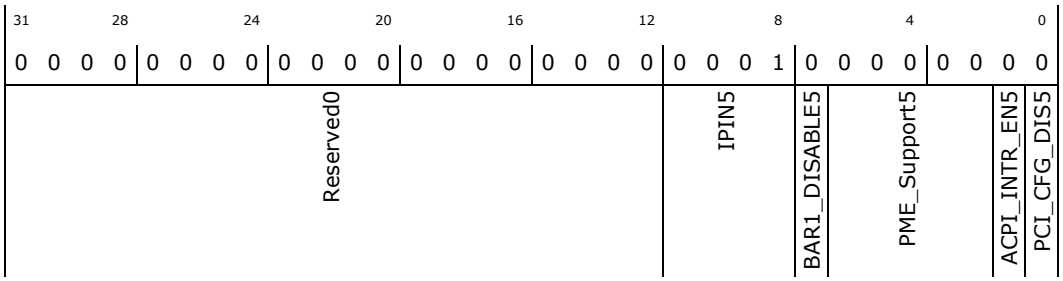
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 510h

Op Codes:

h - Read, h - Write

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x1 RW	**IPIN5:** This register indicates the value to be reflected in the IPIN register of the PCI configuration space. 0- No Interrupt, 1- INTA, 2-INTB, 3-INTC, 4-INTD
7	0x0 RW	**BAR1_DISABLE5:** BAR1 register in the PCI config space will become read only 0 when this bit is set, else this register will be RW. This bit also affects decode for BAR1 accesses
6:2	0x0 RW	**PME_Support5:** The value in this register will be XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space. This register can be used as a mechanism to change the value of the PME_Status PCI config register field

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**ACPI_INTR_EN5:** When set, Bridge will use ACPI SB opcodes for messages. When cleared, Bridge will use global IOSF opcodes
0	0x0 RW	**PCI_CFG_DIS5:** When set, PCI configuration accesses return UR response. When 0, PCI configuration accesses are supported

7.11.56 reg_PCICFGCTR6_type (PCICFGCTR6)—Offset 514h

This register defines functionality for PCI Config space 1

Access Method

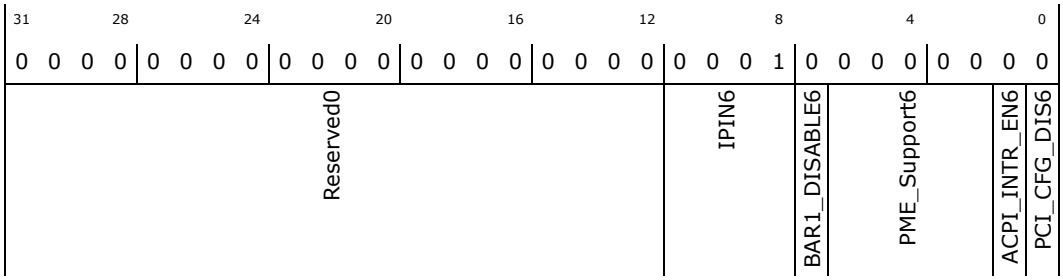
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 514h

Op Codes:

h - Read, h - Write

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x1 RW	**IPIN6:** This register indicates the value to be reflected in the IPIN register of the PCI configuration space. 0- No Interrupt, 1- INTA, 2-INTB, 3-INTC, 4-INTD
7	0x0 RW	**BAR1_DISABLE6:** BAR1 register in the PCI config space will become read only 0 when this bit is set, else this register will be RW. This bit also affects decode for BAR1 accesses
6:2	0x0 RW	**PME_Support6:** The value in this register will be XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space. This register can be used as a mechanism to change the value of the PME_Status PCI config register field
1	0x0 RW	**ACPI_INTR_EN6:** When set, Bridge will use ACPI SB opcodes for messages. When cleared, Bridge will use global IOSF opcodes
0	0x0 RW	**PCI_CFG_DIS6:** When set, PCI configuration accesses return UR response. When 0, PCI configuration accesses are supported

7.11.57 reg_PCICFGCTR7_type (PCICFGCTR7)—Offset 518h

This register defines functionality for PCI Config space 1

Access Method

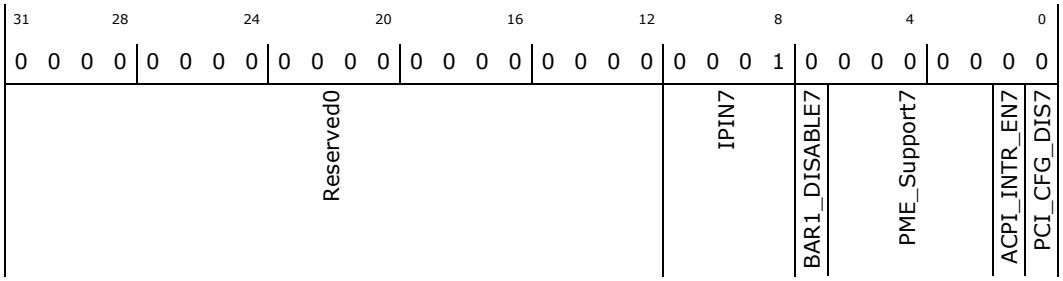
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 518h

Op Codes:

h - Read, h - Write

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x1 RW	**IPIN7:** This register indicates the value to be reflected in the IPIN register of the PCI configuration space. 0- No Interrupt, 1- INTA, 2-INTB, 3-INTC, 4-INTD
7	0x0 RW	**BAR1_DISABLE7:** BAR1 register in the PCI config space will become read only 0 when this bit is set, else this register will be RW. This bit also affects decode for BAR1 accesses
6:2	0x0 RW	**PME_Support7:** The value in this register will be XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space. This register can be used as a mechanism to change the value of the PME_Status PCI config register field
1	0x0 RW	**ACPI_INTR_EN7:** When set, Bridge will use ACPI SB opcodes for messages. When cleared, Bridge will use global IOSF opcodes
0	0x0 RW	**PCI_CFG_DIS7:** When set, PCI configuration accesses return UR response. When 0, PCI configuration accesses are supported

7.11.58 reg_PCICFGCTR8_type (PCICFGCTR8)—Offset 51Ch

This register defines functionality for PCI Config space 1

Access Method

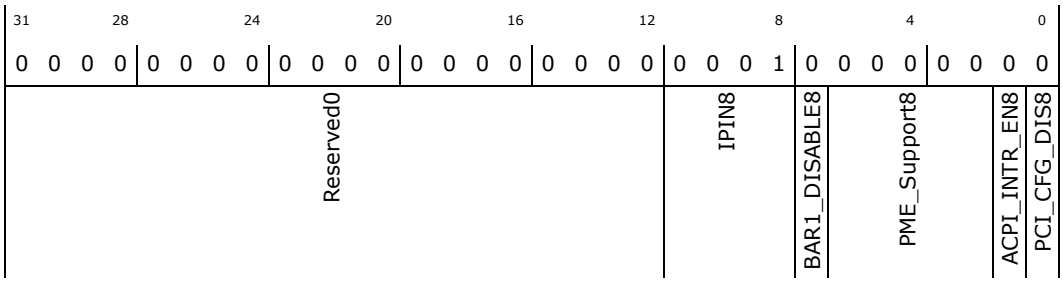
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 51Ch

Op Codes:

h - Read, h - Write

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x1 RW	**IPIN8:** This register indicates the value to be reflected in the IPIN register of the PCI configuration space. 0- No Interrupt, 1- INTA, 2-INTB, 3-INTC, 4-INTD
7	0x0 RW	**BAR1_DISABLE8:** BAR1 register in the PCI config space will become read only 0 when this bit is set, else this register will be RW. This bit also affects decode for BAR1 accesses
6:2	0x0 RW	**PME_Support8:** The value in this register will be XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space. This register can be used as a mechanism to change the value of the PME_Status PCI config register field
1	0x0 RW	**ACPI_INTR_EN8:** When set, Bridge will use ACPI SB opcodes for messages. When cleared, Bridge will use global IOSF opcodes
0	0x0 RW	**PCI_CFG_DIS8:** When set, PCI configuration accesses return UR response. When 0, PCI configuration accesses are supported

7.11.59 reg_CHCTRL_type (CHCTRL)—Offset 520h

Access Method

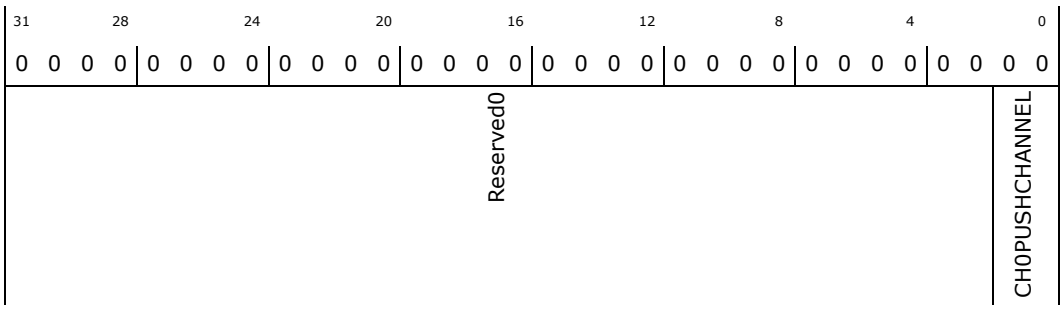
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 520h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved0:** Reserved.
1:0	0x0 RW	**CH0PUSHCHANNEL:** Reserved.

7.11.60 reg_PRI_GEN_REGRW1_type (PRI_GEN_REGRW1)—Offset 600h

General Purpose Read Write Register 1

Access Method

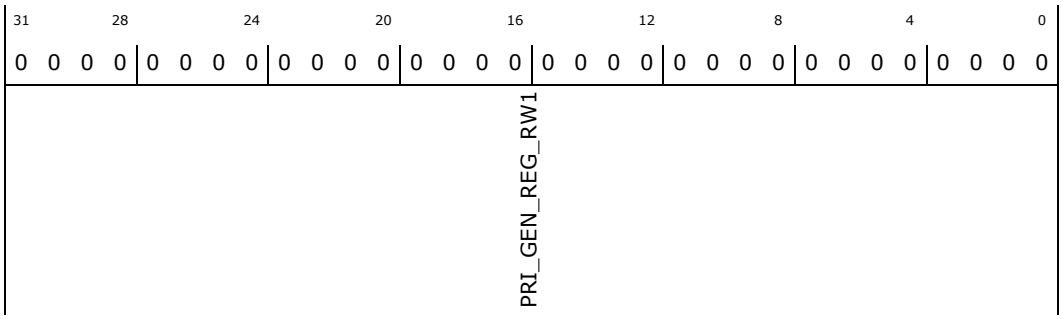
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 600h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**PRI_GEN_REG_RW1:** This is a generic register provided for product specific behavior

7.11.61 reg_PRI_GEN_REGRW2_type (PRI_GEN_REGRW2)—Offset 604h

General Purpose Read Write Register 2

Access Method

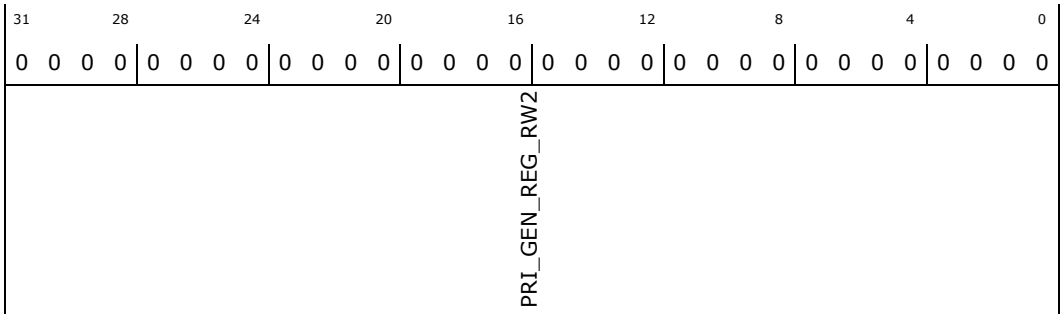
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 604h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**PRI_GEN_REG_RW2:** This is a generic register provided for product specific behavior

7.11.62 reg_PRI_GEN_REGRW3_type (PRI_GEN_REGRW3)—Offset 608h

General Purpose Read Write Register 3

Access Method

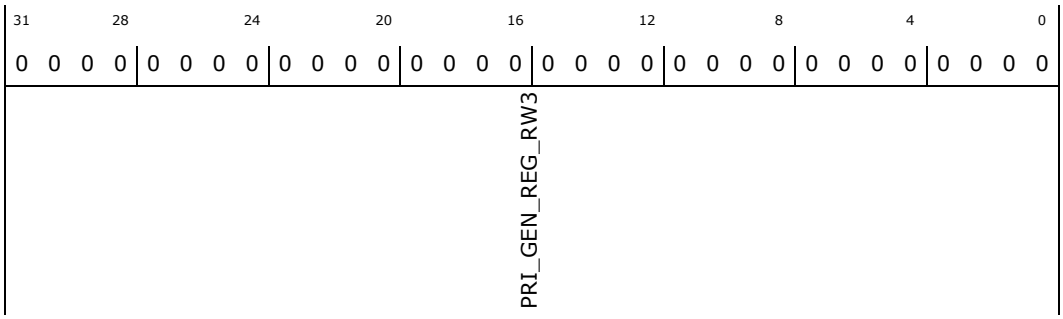
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 608h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**PRI_GEN_REG_RW3:** This is a generic register provided for product specific behavior

7.11.63 reg_PRI_GEN_REGRW4_type (PRI_GEN_REGRW4)—Offset 60Ch

General Purpose Read Write Register 4

Access Method

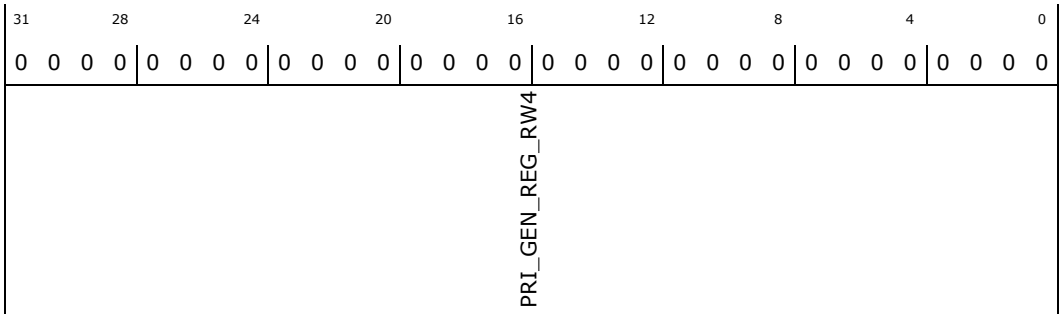
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 60Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**PRI_GEN_REG_RW4:** This is a generic register provided for product specific behavior

7.11.64 reg_PRI_GEN_REGRW5_type (PRI_GEN_REGRW5)—Offset 610h

General Purpose Read Write Register 5

Access Method

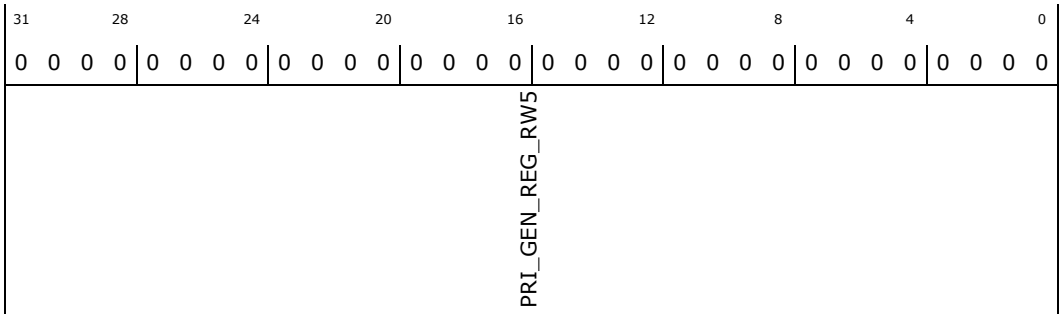
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 610h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**PRI_GEN_REG_RW5:** This is a generic register provided for product specific behavior

7.11.65 reg_PRI_GEN_REGRW6_type (PRI_GEN_REGRW6)—Offset 614h

General Purpose Read Write Register 6

Access Method

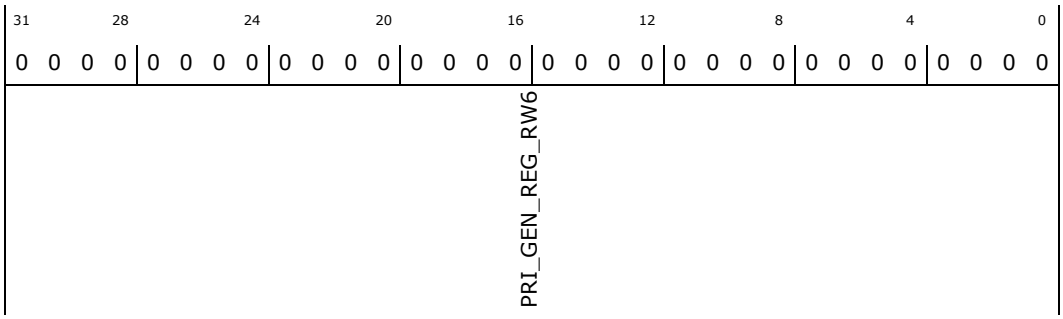
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 614h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**PRI_GEN_REG_RW6:** This is a generic register provided for product specific behavior

7.11.66 reg_PRI_GEN_REGRW7_type (PRI_GEN_REGRW7)—Offset 618h

General Purpose Read Write Register 7

Access Method

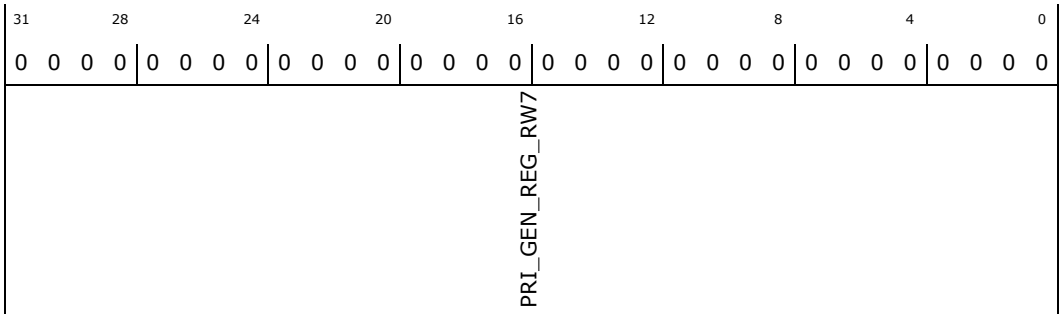
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 618h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**PRI_GEN_REG_RW7:** This is a generic register provided for product specific behavior

7.11.67 reg_PRI_GEN_REGRW8_type (PRI_GEN_REGRW8)—Offset 61Ch

General Purpose Read Write Register 8

Access Method

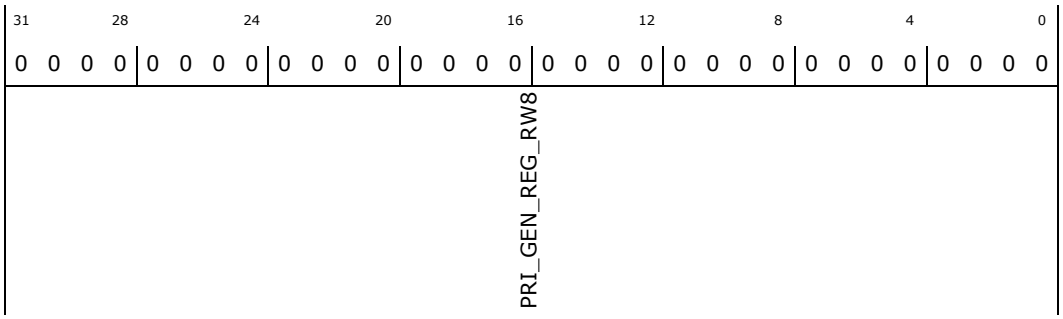
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 61Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**PRI_GEN_REG_RW8:** This is a generic register provided for product specific behavior

7.11.68 reg_PRI_GEN_REGRWO1_type (PRI_GEN_REGRWO1)—Offset 620h

General Purpose Read Write Once Register 1

Access Method

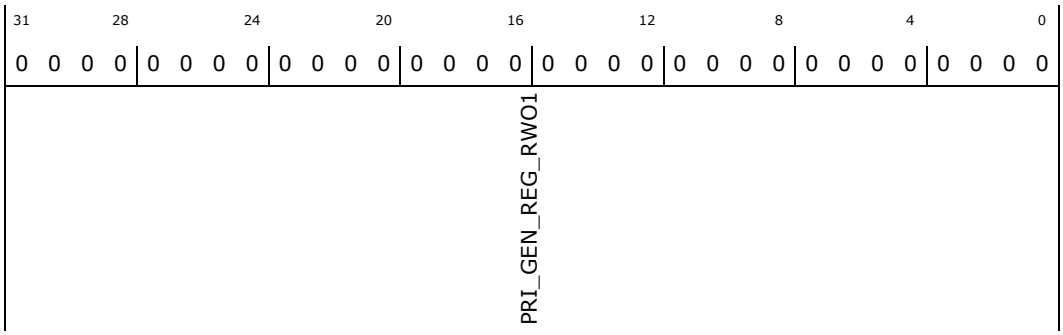
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 620h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/O	**PRI_GEN_REG_RWO1:** This is a generic register provided for product specific behavior

7.11.69 reg_PRI_GEN_REGRWO2_type (PRI_GEN_REGRWO2)—Offset 624h

General Purpose Read Write Once Register 2

Access Method

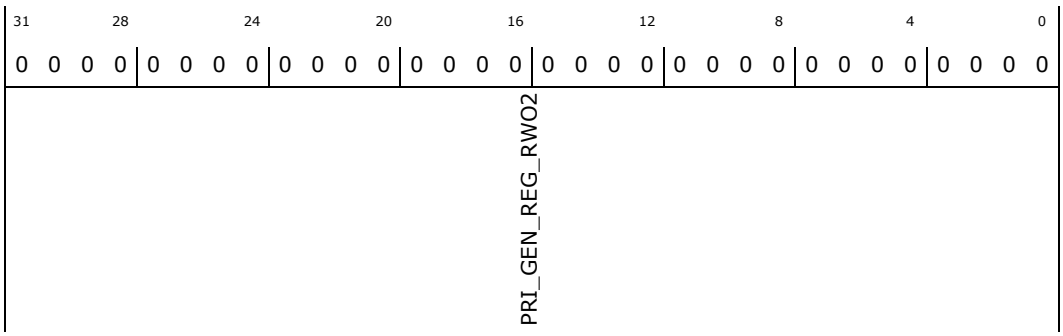
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 624h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/O	**PRI_GEN_REG_RWO2:** This is a generic register provided for product specific behavior

7.11.70 reg_PRI_GEN_REGRWO3_type (PRI_GEN_REGRWO3)—Offset 628h

General Purpose Read Write Once Register 3

Access Method

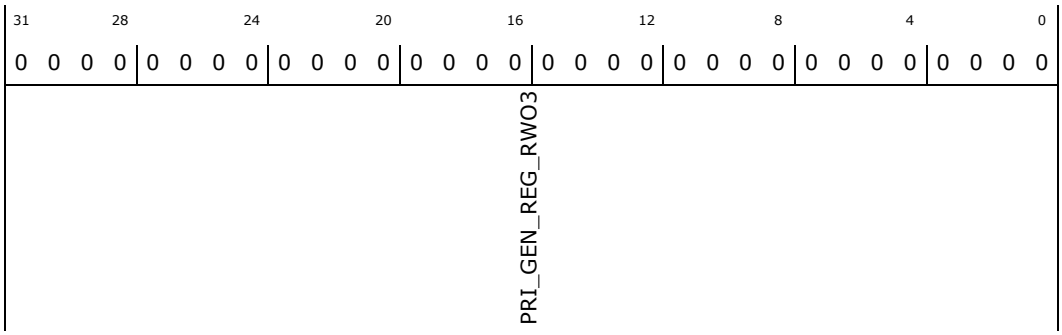
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 628h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/O	**PRI_GEN_REG_RWO3:** This is a generic register provided for product specific behavior

7.11.71 reg_PRI_GEN_REGRWO4_type (PRI_GEN_REGRWO4)—Offset 62Ch

General Purpose Read Write Once Register 4

Access Method

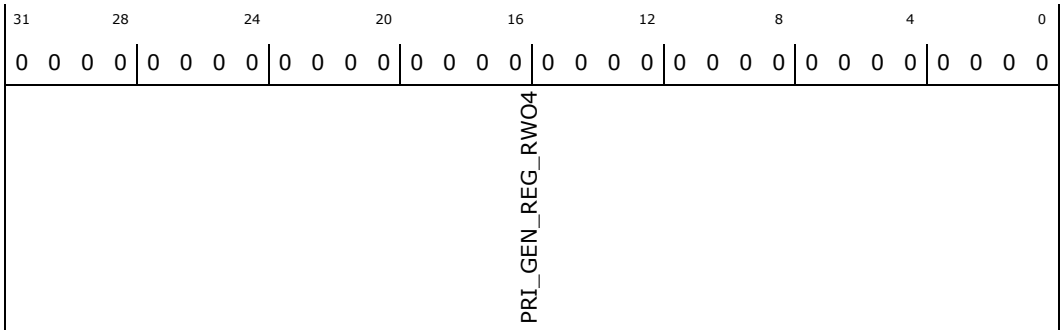
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 62Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/O	**PRI_GEN_REG_RWO4:** This is a generic register provided for product specific behavior

7.11.72 reg_PRI_GEN_REGRWO5_type (PRI_GEN_REGRWO5)—Offset 630h

General Purpose Read Write Once Register 5

Access Method

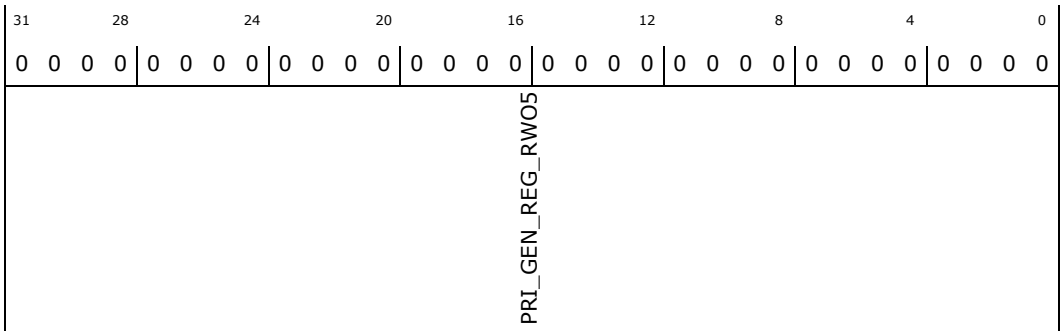
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 630h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/O	**PRI_GEN_REG_RWO5:** This is a generic register provided for product specific behavior

7.11.73 reg_PRI_GEN_REGRWO6_type (PRI_GEN_REGRWO6)—Offset 634h

General Purpose Read Write Once Register 6

Access Method

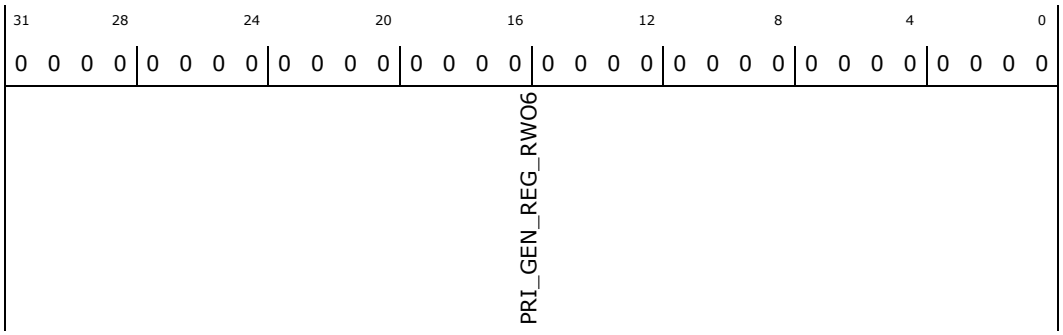
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 634h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/O	**PRI_GEN_REG_RWO6:** This is a generic register provided for product specific behavior

7.11.74 reg_PRI_GEN_REGRWO7_type (PRI_GEN_REGRWO7)—Offset 638h

General Purpose Read Write Once Register 7

Access Method

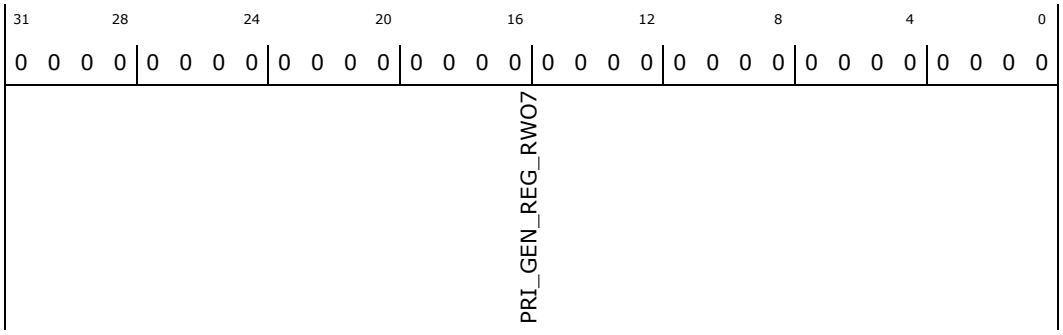
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 638h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/O	**PRI_GEN_REG_RWO7:** This is a generic register provided for product specific behavior

7.11.75 reg_PRI_GEN_REGRWO8_type (PRI_GEN_REGRWO8)—Offset 63Ch

General Purpose Read Write Once Register 8

Access Method

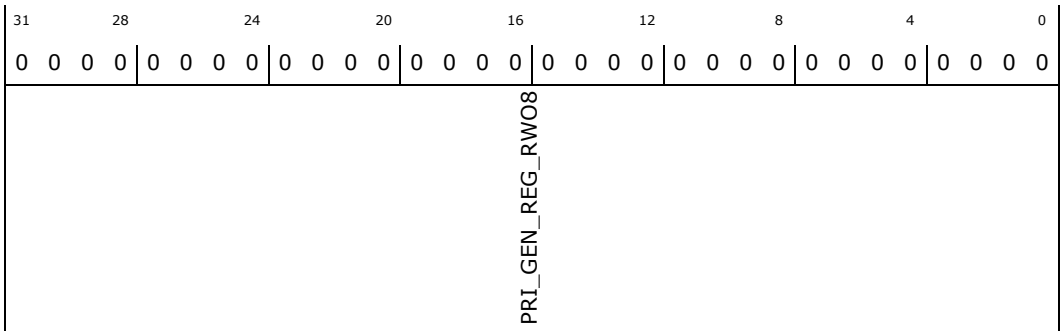
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x59] + 63Ch

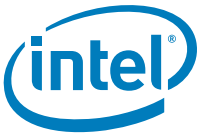
Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/O	**PRI_GEN_REG_RWO8:** This is a generic register provided for product specific behavior



7.12 USB OTG PCI Configuration Registers

Table 48. Summary of PCI Configuration Registers—0/22/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
A0–A3h	4	"reg_GEN_REGRW1_type (GEN_REGRW1)—Offset A0h" on page 3077	00000000h
A4–A7h	4	"reg_GEN_REGRW2_type (GEN_REGRW2)—Offset A4h" on page 3078	00000000h
A8–ABh	4	"reg_GEN_REGRW3_type (GEN_REGRW3)—Offset A8h" on page 3079	00000000h
AC–AFh	4	"reg_GEN_REGRW4_type (GEN_REGRW4)—Offset ACh" on page 3079	00000000h
C0–C3h	4	"reg_GEN_INPUT_REG_type (GEN_INPUT_REGRW)—Offset C0h" on page 3080	1008000Bh

7.12.1 reg_GEN_REGRW1_type (GEN_REGRW1)—Offset A0h

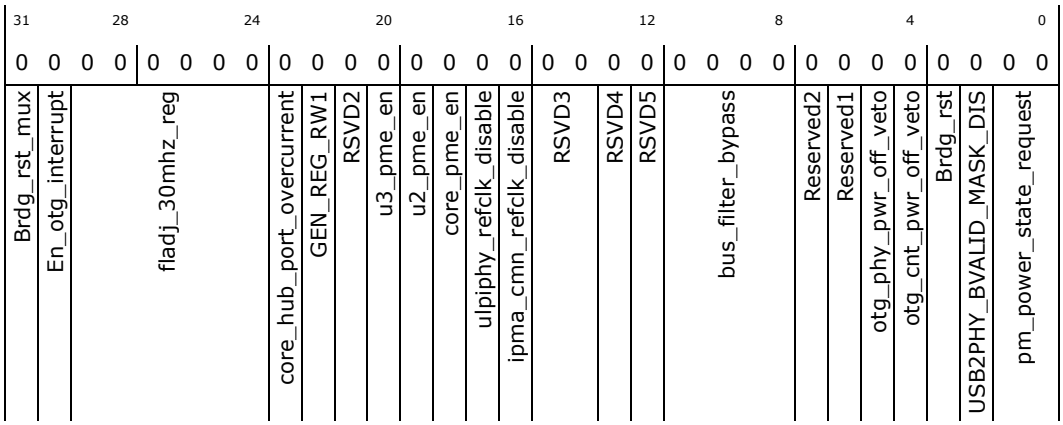
General Purpose Read Write Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:22, F:0] + A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Brdg_rst_mux:** This is a mux the core reset between the normal reset or reset and with bdg_reset regRW1[3]
30	0x0 RW	**En_otg_interrupt:** reserved
29:24	0x0 RW	**fladj_30mhz_reg:** HS jitter adjusment
23	0x0 RW	**core_hub_port_overcurrent:** This is a generic register provided for product specific behavior
22	0x0 RW	**GEN_REG_RW1:** This is a generic register provided for product specific behavior
21	0x0 RW	**RSVD2:** reserved
20	0x0 RW	**u3_pme_en:** Determines whether USB3 flis PME events are allowed to trigger PME events to brige/GPIO
19	0x0 RW	**u2_pme_en:** Determines whether ULPI flis PME events are allowed to trigger PME events to brige/GPIO
18	0x0 RW	**core_pme_en:** Determines whether core PME events are allowed to trigger PME events to brige/GPIO
17	0x0 RW	**ulpiphy_refclk_disable:** Feeds logic that generates the 19.2MHz clkreq signal
16	0x0 RW	**ipma_cmn_refclk_disable:** Feeds through PIMA PHY into 25MHz clkreq signal
15:14	0x0 RW	**RSVD3:** reserved

Bit Range	Default & Access	Field Name (ID): Description
13	0x0 RW	**RSVD4:** reserved
12	0x0 RW	**RSVD5:** reserved
11:8	0x0 RW	**bus_filter_bypass:** Bus Filter Bypass. Disables the internal bus filters that are enabled by DWC_USB3_EN_BUS_FILTERS coreConsultant parameter. This static signal is present only when DWC_USB3_EN_BUS_FILTERS is 1. It is expected that this signal is set or reset at power-on reset and is not changed during the normal operation of the core.
7	0x0 RW	**Reserved2:** reserved
6	0x0 RW	**Reserved1:** reserved
5	0x0 RW	**otg_phy_pwr_off_veto:** Indicates that PHY suspend power should not power off even on RTD3hot (Note that the PHY core power is turned off during RTD3hot in line with the OTG core, as a function of otg_cnt_pwr_off_veto)
4	0x0 RW	**otg_cnt_pwr_off_veto:** Indicates that controller power should not power off even on RTD3hot.Also a veto signal to keep LPPLL on. Note: Currently LPPLL results in a veto for S0iX flows
3	0x0 RW	**Brdg_rst:** reset the core see also regRW1[31]
2	0x0 RW	**USB2PHY_BVALID_MASK_DIS:** 0: enable USB2 PHY BVALID mask 1: disable
1:0	0x0 RW	**pm_power_state_request:** This port defines the PCI power management state requested by the software. When the core is configured with two power rail support (DWC_USB3_EN_PWROPT=2), the valid states are: ? 00: D0 ? 11: D3 Active State

7.12.2 reg_GEN_REGRW2_type (GEN_REGRW2)—Offset A4h

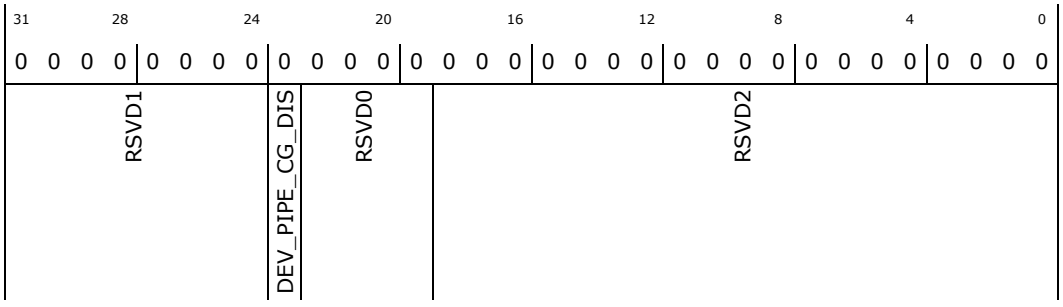
General Purpose Read Write Register2

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:22, F:0] + A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**RSVD1:** RESERVED **Power Well:** SUS
23	0x0 RW	**DEV_PIPE_CG_DIS:** (SoC Only) chicken bit to disable pipe clock gating. 0 ? enable 1- disable This is for debug purpose only.
22:19	0x0 RO	**RSVD0:** Reserved
18:0	0x0 RW	**RSVD2:** RESERVED **Power Well:** SUS

7.12.3 reg_GEN_REGRW3_type (GEN_REGRW3)—Offset A8h

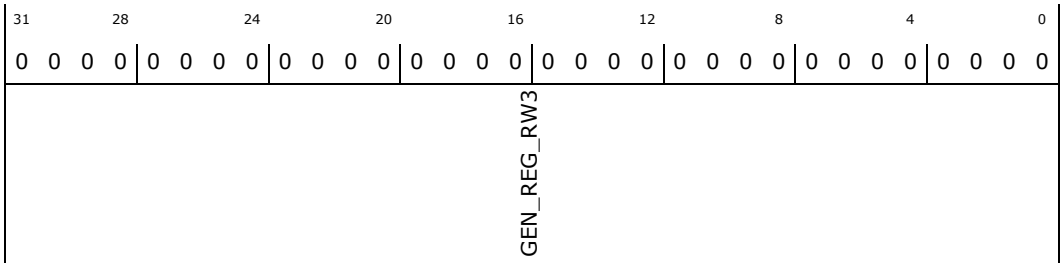
General Purpose Read Write Register3

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:22, F:0] + A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW3:** reserved

7.12.4 reg_GEN_REGRW4_type (GEN_REGRW4)—Offset ACh

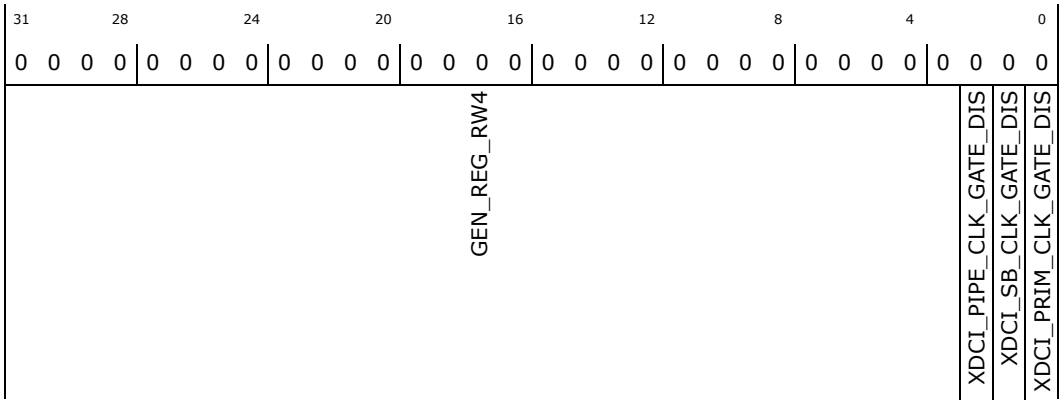
General Purpose Read Write Register4

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:22, F:0] + ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RW	**GEN_REG_RW4:** reserved
2	0x0 RW	**XDCI_PIPE_CLK_GATE_DIS:** xdci pipe clock gating disable
1	0x0 RW	**XDCI_SB_CLK_GATE_DIS:** xdci sideband clock gating disable
0	0x0 RW	**XDCI_PRIM_CLK_GATE_DIS:** xdci primary clock gating disable

7.12.5 reg_GEN_INPUT_REG_type (GEN_INPUT_REGRW)—Offset C0h

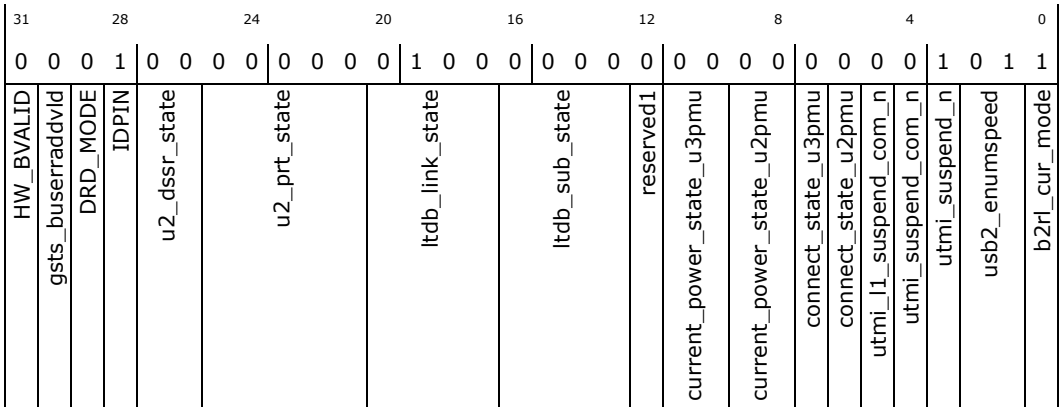
General Purpose Input Register

Access Method

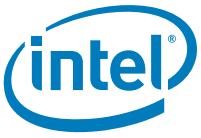
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:22, F:0] + C0h

Default: 1008000Bh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**BVALID_HW (HW_BVALID):** hardware bvalid
30	0x0 RO	**gsts_buserraddvld:** Bus error
29	0x0 RO	**DRD_MODE:** SS DRD mode 0 device mode 1 host mode
28	0x1 RO	**IDPIN:** IDPIN value (debounce)
27:26	0x0 RO	**u2_dssr_state:** USB2 DSSR State
25:21	0x0 RO	**u2_prt_state:** USB2 Port State
20:17	0x4 RO	**ltdb_link_state:** USB3 Link state
16:13	0x0 RO	**ltdb_sub_state:** USB3 Link sub state
12	0x0 RO	**reserved1:** Reserved.
11:10	0x0 RO	**current_power_state_u3pmu:** The current power state of the core. When equal to '3', the PMU is controlling the PHY, and when equal to '0', the core is controlling the PHY
9:8	0x0 RO	**current_power_state_u2pmu:** The current power state of the core. When equal to '3', the PMU is controlling the PHY, and when equal to '0', the core is controlling the PHY
7	0x0 RO	**connect_state_u3pmu:** When '1', indicates the PMU is maintaining at least one connection to the host or a device (the link is in U3). When '0', indicates the PMU has no connection to the host or any device.
6	0x0 RO	**connect_state_u2pmu:** When '1', indicates the PMU is maintaining at least one connection to the host or a device (the link is in L1, L2). When '0', indicates the PMU has no connection to the host or any device
5	0x0 RO	**utmi_l1_suspend_com_n:** Common L1 suspend
4	0x0 RO	**utmi_suspend_com_n:** Common suspend
3	0x1 RO	**utmi_suspend_n:** USB 2.0 Port Suspend
2:1	0x1 RO	**usb2_enumspeed:** Device Enumerated Speed
0	0x1 RO	**b2rl_cur_mode:** Current Mode. Current Mode 1'b0 Host ,1'b1 Device



7.13 USB2 PCI Configuration Registers

Table 49. Summary of PCI Configuration Registers—

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"PLLDIVRATIOS_0—Offset 0h" on page 3083	00640000h
C–Fh	4	"PLLSEQUENCE_1—Offset Ch" on page 3083	00080000h
10–13h	4	"CONFIG_0—Offset 10h" on page 3084	00000000h
14–17h	4	"CONFIG_1—Offset 14h" on page 3085	20000000h
18–1Bh	4	"CONFIG_2—Offset 18h" on page 3086	00000000h
1C–1Fh	4	"CONFIG_3—Offset 1Ch" on page 3086	00000000h
20–23h	4	"FILTER_OBS—Offset 20h" on page 3087	FFE00000h
24–27h	4	"VISA_OUT—Offset 24h" on page 3088	00000000h
28–2Bh	4	"DFT_0—Offset 28h" on page 3088	83FF3F00h
2C–2Fh	4	"DFT_1—Offset 2Ch" on page 3089	30000000h
34–37h	4	"DFT_3—Offset 34h" on page 3090	00022C0Ch
38–3Bh	4	"SFRCONFIG_0—Offset 38h" on page 3091	00880000h

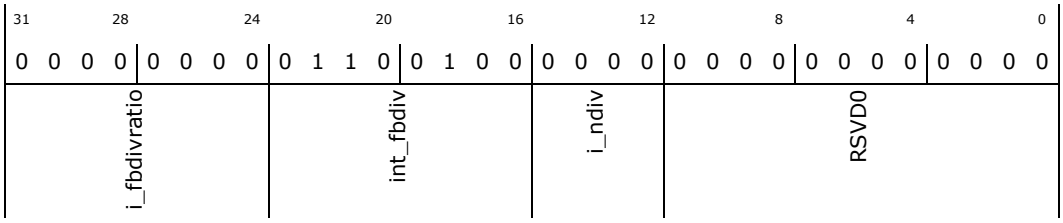
7.13.1 PLLDIVRATIOS_0—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:, D:, F:] + 0h

Default: 00640000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	X RW/Strap	**i_fbdivratio [31:24] (i_fbdivratio):** generic 8bit feedback divider ratio. N=i_fbdivratio
23:16	0x64 RW	**int_fbdiv [23:16] (int_fbdiv):** For external fbclk usage, inserted the expected division ratio.
15:12	X RW/Strap	**i_ndiv [15:12] (i_ndiv):** Currently reserved bits. pre divider control. M=i_ndiv (only 1 to 7 are valid)
11:0	0x0 RO	**RSVD0:** Reserved

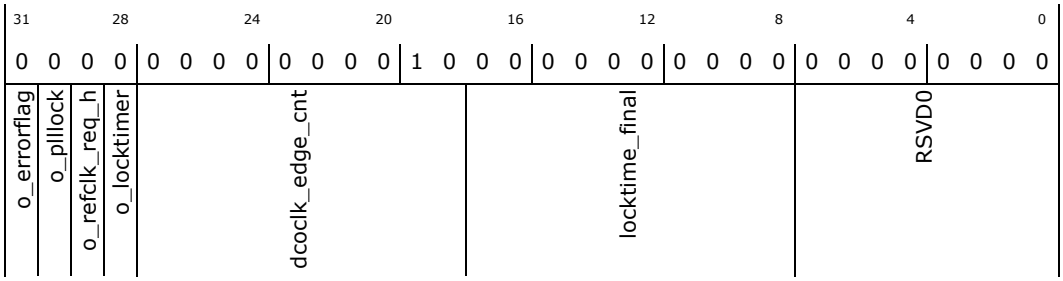
7.13.2 PLLSEQUENCE_1—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:, D:, F:] + Ch

Default: 00080000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**o_errorflag [31:31] (o_errorflag):** General Error flag.
30	0x0 RO	**o_plllock [30:30] (o_plllock):** PLL Lock indicator signal.

Bit Range	Default & Access	Field Name (ID): Description
29	0x0 RO	**o_refclk_req_h [29:29] (o_refclk_req_h):** ADPLL's Refclk request bit.
28	0x0 RO	**o_locktimer [28:28] (o_locktimer):** Lock time expected Indication bit.
27:18	0x2 RO	**dcoclk_edge_cnt [27:18] (dcoclk_edge_cnt):** DCO edge's counter
17:8	0x0 RO	**locktime_final [17:8] (locktime_final):** Locktime counter per refclk cycles, stops at overflow / lock.
7:0	0x0 RO	**RSVD0:** Reserved

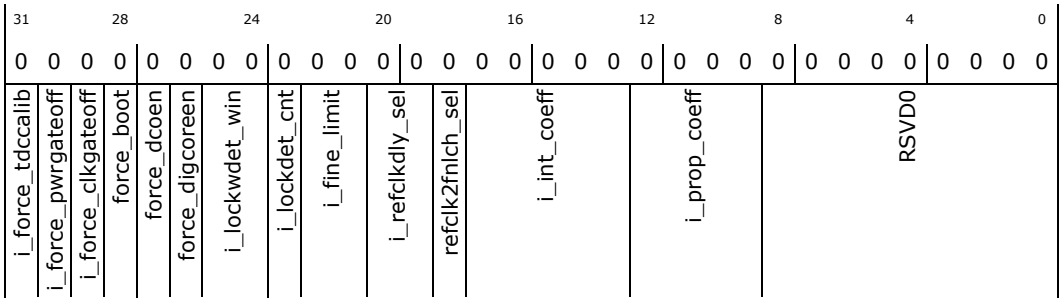
7.13.3 CONFIG_0—Offset 10h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:, D:, F:] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	X RW/Strap	**i_force_tdccalib [31:31] (i_force_tdccalib):** force tdc calibration in c73usb250_normal locking
30	X RW/Strap	**i_force_pwrgateoff [30:30] (i_force_pwrgateoff):** force power gating off in all modes
29	X RW/Strap	**i_force_clkgateoff [29:29] (i_force_clkgateoff):** force clock gating off in all modes
28	0x0 RW	**force_boot [28:28] (force_boot):** EV: forces boot locking instead of c73usb250_normal locking
27	0x0 RW	**force_dcoen [27:27] (force_dcoen):** EV: forces dco enable even if PLL is off. Need this for example in openloop mode
26	0x0 RW	**force_digcoreen [26:26] (force_digcoreen):** EV: forces digital core reset off (unless pwrgood=0)
25:24	X RW/Strap	**i_lockwdet_win [25:24] (i_lockwdet_win):** phase error threshold at which PLL is unlocked (HH max pe allowed)

Bit Range	Default & Access	Field Name (ID): Description
23	X RW/Strap	**i_lockdet_cnt [23:23] (i_lockdet_cnt):** lock counter 32 (L) or 64 (H) cycles
22:21	X RW/Strap	**i_fine_limit [22:21] (i_fine_limit):** defines distance of fine code from edges that would trigger SFR trimming. Distance defined by 2^(fine_limit+5)
20:19	X RW/Strap	**i_refclkdly_sel [20:19] (i_refclkdly_sel):** control delay of refclk_dly clock that is used by DCO latches
18	0x0 RW	**refclk2fnlch_sel [18:18] (refclk2fnlch_sel):** Selects refproc's delayed clock / inverted version of refclk2dig for DCO latches n DS.
17:13	X RW/Strap	**i_int_coeff [17:13] (i_int_coeff):** Ki filter coefficient, 2^n. Two's complement
12:9	X RW/Strap	**i_prop_coeff [12:9] (i_prop_coeff):** Kp filter coefficient, 2^n. Two's complement
8:0	0x0 RO	**RSVD0:** Reserved

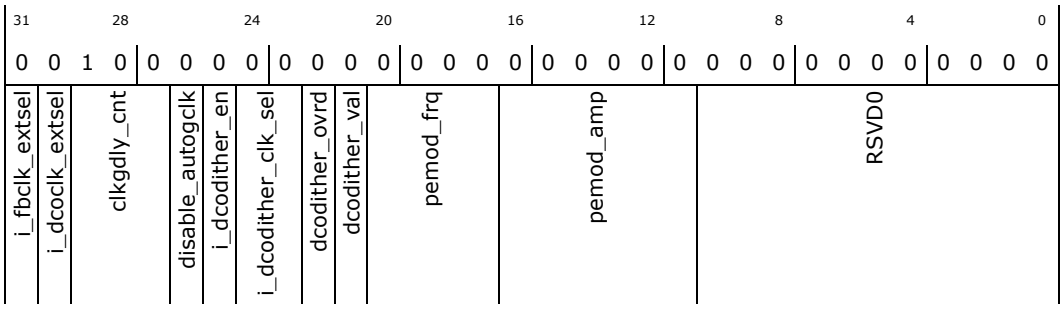
7.13.4 CONFIG_1—Offset 14h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:, D:, F:] + 14h

Default: 20000000h



Bit Range	Default & Access	Field Name (ID): Description
31	X RW/Strap	**i_fbclk_extsel [31:31] (i_fbclk_extsel):** external feedback clock select (allowing use of external feedback divider). In this case, user must set fbdivratio to the feedback ratio he uses
30	X RW/Strap	**i_dcoclk_extsel [30:30] (i_dcoclk_extsel):** long loop clock select through dcoclk_ext clock
29:27	0x4 RW	**clkgdly_cnt [29:27] (clkgdly_cnt):** Delay for clock gating (0 menas no delay).
26	0x0 RW	**disable_autogclk [26:26] (disable_autogclk):** Disables auto-clockgating.
25	X RW/Strap	**i_dcodither_en [25:25] (i_dcodither_en):** enable sigma delta

Bit Range	Default & Access	Field Name (ID): Description
24:23	X RW/Strap	**i_dcodither_clk_sel [24:23] (i_dcodither_clk_sel):** select sigma delta over sampling clock
22	0x0 RW	**dcodither_ovrd [22:22] (dcodither_ovrd):** bypass sigma delta dithering bit with external bit
21	0x0 RW	**dcodither_val [21:21] (dcodither_val):** sigma delta dithering external bit
20:17	0x0 RW	**pemod_frq [20:17] (pemod_frq):** EV: pe modulation frequency
16:11	0x0 RW	**pemod_amp [16:11] (pemod_amp):** EV: pe modulation amplitude. Two's complement
10:0	0x0 RO	**RSVD0:** Reserved

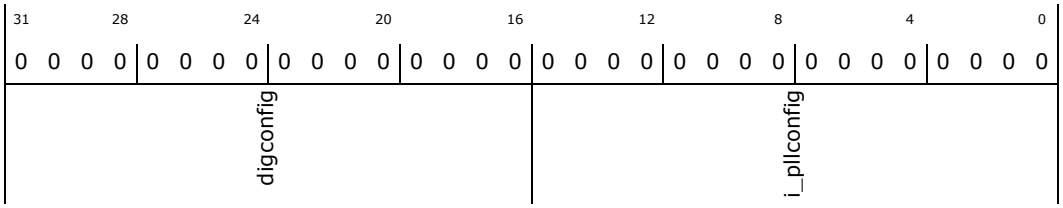
7.13.5 CONFIG_2—Offset 18h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:, D:, F:] + 18h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**digconfig [31:16] (digconfig):** Digital's internal spare config.
15:0	X RW/Strap	**i_pllconfig [15:0] (i_pllconfig):** general configuration bits: quick_phase, coarse_sweepen, tdc_sweepen, use_refclkdel2dcolat

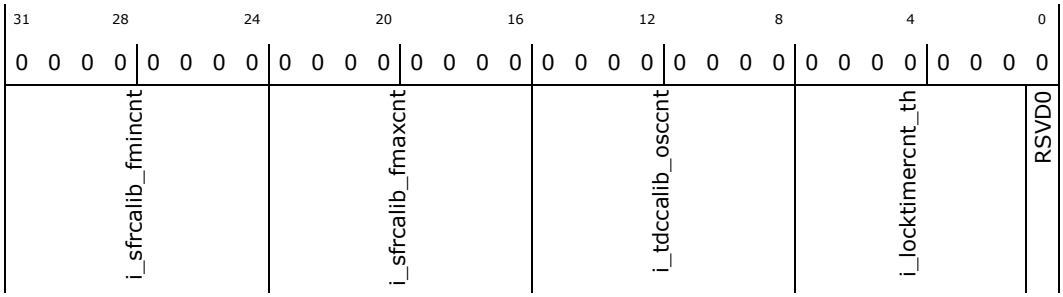
7.13.6 CONFIG_3—Offset 1Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:, D:, F:] + 1Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	X RW/Strap	**i_sfrcalib_fmincnt [31:24] (i_sfrcalib_fmincnt):** set to round(1.1GHz/ Fref)-1 for proper SFR calibration
23:16	X RW/Strap	**i_sfrcalib_fmaxcnt [23:16] (i_sfrcalib_fmaxcnt):** set to round(3.43GHz/Fref)-1 for proper SFR calibration
15:8	X RW/Strap	**i_tdccalib_osccnt [15:8] (i_tdccalib_osccnt):** set to round(1.47GHz/ Frefclk)-1 for proper TDC calibration
7:1	X RW/Strap	**i_locktimercnt_th [7:1] (i_locktimercnt_th):** Set this bus to the number of refclk cycles after which the o_locktimer is asserted,
0	0x0 RO	**RSVD0:** Reserved

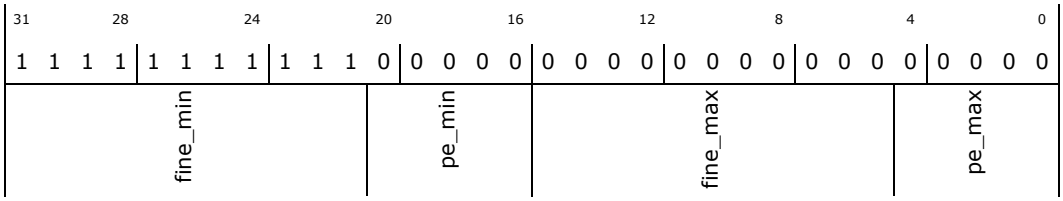
7.13.7 FILTER_OBS—Offset 20h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:, D:, F:] + 20h

Default: FFE00000h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0x7ff RO	**fine_min [31:21] (fine_min):** DCO's fine code min sampled value.
20:16	0x0 RO	**pe_min [20:16] (pe_min):** Phase error min sampled value.
15:5	0x0 RO	**fine_max [15:5] (fine_max):** DCO's fine code max sampled value.
4:0	0x0 RO	**pe_max [4:0] (pe_max):** Phase error max sampled value.

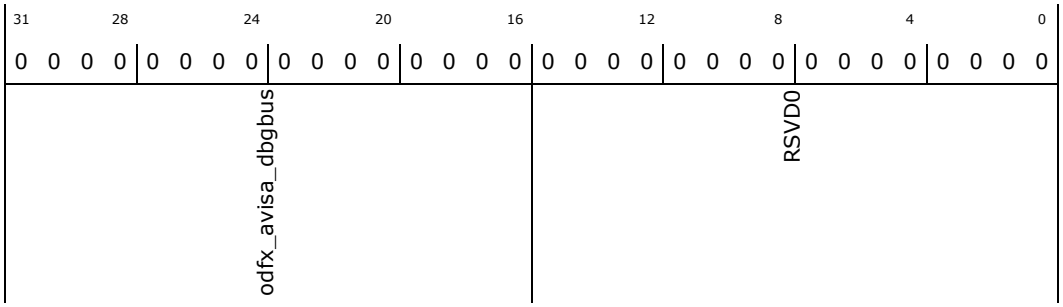
7.13.8 VISA_OUT—Offset 24h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:, D:, F:] + 24h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**odfx_avisa_dbgbus [31:16] (odfx_avisa_dbgbus):** Visa lane's 1 n 0
15:0	0x0 RO	**RSVD0:** Reserved

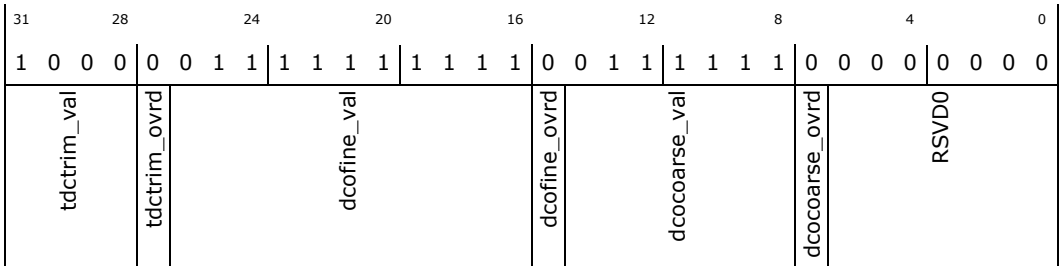
7.13.9 DFT_0—Offset 28h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:, D:, F:] + 28h

Default: 83FF3F00h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x8 RW	**tdctrim_val [31:28] (tdctrim_val):** TDC trim override value
27	0x0 RW	**tdctrim_ovrd [27:27] (tdctrim_ovrd):** TDC trim override select
26:16	0x3ff RW	**dcofine_val [26:16] (dcofine_val):** EV: DCO fine override value

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**dcofine_ovrd [15:15] (dcofine_ovrd):** EV: DCO fine override select
14:8	0x3f RW	**dcocoarse_val [14:8] (dcocoarse_val):** EV: DCO coarse override value
7	0x0 RW	**dcocoarse_ovrd [7:7] (dcocoarse_ovrd):** EV: bypass coarse calibration code with coarse_val
6:0	0x0 RO	**RSVD0:** Reserved

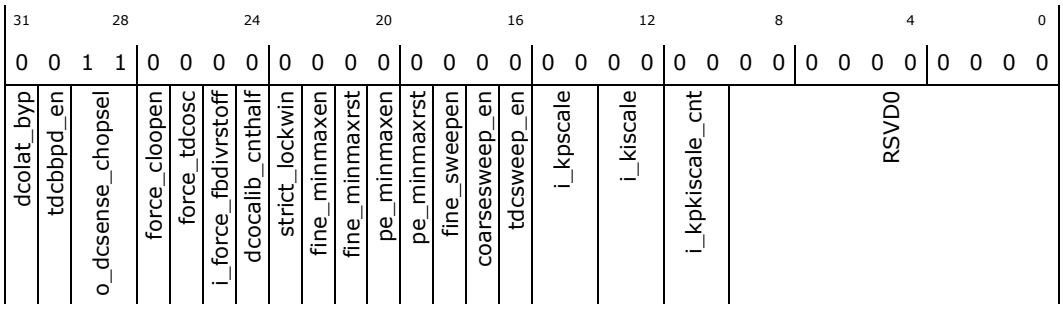
7.13.10 DFT_1—Offset 2Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:, D:, F:] + 2Ch

Default: 30000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**dcolat_byp [31:31] (dcolat_byp):** Makes DCO latches transparent. Allows open loop checks without refclk.
30	0x0 RW	**tdcbbpd_en [30:30] (tdcbbpd_en):** Enable bbpd in the sign bit of the TDC instead of FFPD
29:28	0x3 RW	**o_dcsense_chopsel [29:28] (o_dcsense_chopsel):** div_farm clock chooper: '00' = refclk. '01', '11' = vss, '10' = vcc
27	0x0 RW	**force_cloopen [27:27] (force_cloopen):** EV: forces PLL into close loop mode and final filter coefficient
26	0x0 RW	**force_tdcosc [26:26] (force_tdcosc):** EV: configures TDC chain as ring oscillator
25	X RW/Strap	**i_force_fbdivrstoff [25:25] (i_force_fbdivrstoff):** force feedback divider reset off in all modes
24	0x0 RW	**dcocalib_cnthalf [24:24] (dcocalib_cnthalf):** dco calibration (and tdc calibration?) counter counts half of default count for faster calibration
23	0x0 RW	**strict_lockwin [23:23] (strict_lockwin):** Strict Lock window config. '0' = -1(pe_tdc(0 for 8 cycles. '1' = -2(pe_tdc(1 for 16 cycles.

Bit Range	Default & Access	Field Name (ID): Description
22	0x0 RW	**fine_minmaxen [22:22] (fine_minmaxen):** when '1', min/max values of fine code are monitored (anyway, not when lock=0)
21	0x0 RW	**fine_minmaxrst [21:21] (fine_minmaxrst):** resets the fine minmax value
20	0x0 RW	**pe_minmaxen [20:20] (pe_minmaxen):** when '1', min/max values of TDC output code are monitored (anyway, not when lock=0)
19	0x0 RW	**pe_minmaxrst [19:19] (pe_minmaxrst):** resets the pe_minmax value
18	0x0 RW	**fine_sweepen [18:18] (fine_sweepen):** EV: sweep fine code (triangle sweep)
17	0x0 RW	**coarsesweep_en [17:17] (coarsesweep_en):** Coarse sweep bit.
16	0x0 RW	**tdcsweep_en [16:16] (tdcsweep_en):** TDC sweep bit.
15:14	X RW/Strap	**i_kpscale [15:14] (i_kpscale):** Kp scaling during startup for faster lock (2^n)
13:12	X RW/Strap	**i_kiscale [13:12] (i_kiscale):** Ki scaling during startup for faster lock (2^n)
11:10	X RW/Strap	**i_kpkiscale_cnt [11:10] (i_kpkiscale_cnt):** controls number of refclk cycles at startup at which Kp and Ki are scaled up for faster lock (kpscale, kiscale)
9:0	0x0 RO	**RSVD0:** Reserved

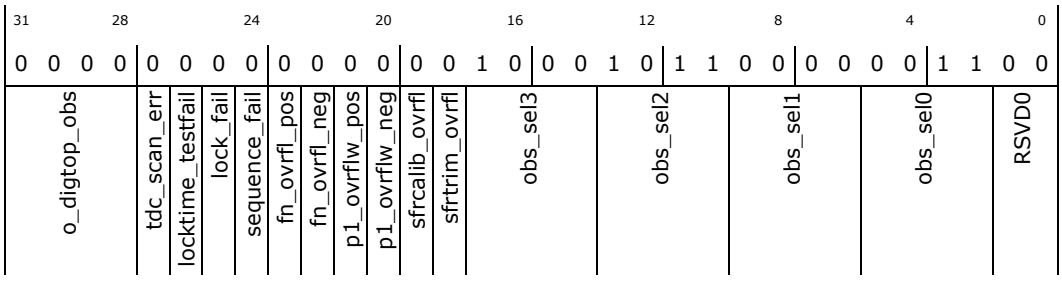
7.13.11 DFT_3—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:, D:, F:] + 34h

Default: 00022C0Ch



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**o_digtop_obs [31:28] (o_digtop_obs):** Digital Obs out.

Bit Range	Default & Access	Field Name (ID): Description
27	0x0 RO	**tdc_scan_err [27:27] (tdc_scan_err):** TDC scan test error flag.
26	0x0 RO	**locktime_testfail [26:26] (locktime_testfail):** Narrow lock window test failed
25	0x0 RO	**lock_fail [25:25] (lock_fail):** PLL went out of lock.
24	0x0 RO	**sequence_fail [24:24] (sequence_fail):** Calib procedure fail flag.
23	0x0 RO	**fn_ovrfl_pos [23:23] (fn_ovrfl_pos):** Fine Positive code overflow.
22	0x0 RO	**fn_ovrfl_neg [22:22] (fn_ovrfl_neg):** Fine Negative code overflow.
21	0x0 RO	**p1_ovrflw_pos [21:21] (p1_ovrflw_pos):** Filter's Integrator Positive code overflow.
20	0x0 RO	**p1_ovrflw_neg [20:20] (p1_ovrflw_neg):** Filter's Integrator Negative code overflow.
19	0x0 RO	**sfrcalib_ovrfl [19:19] (sfrcalib_ovrfl):** SFR calib overflow.
18	0x0 RO	**sfrtrim_ovrfl [18:18] (sfrtrim_ovrfl):** SFR trim overflow.
17:14	0x8 RW	**obs_sel3 [17:14] (obs_sel3):** obs(3) muxing control bits.
13:10	0xb RW	**obs_sel2 [13:10] (obs_sel2):** obs(2) muxing control bits.
9:6	0x0 RW	**obs_sel1 [9:6] (obs_sel1):** obs(1) muxing control bits.
5:2	0x3 RW	**obs_sel0 [5:2] (obs_sel0):** obs(0) muxing control bits.
1:0	0x0 RO	**RSVD0:** Reserved

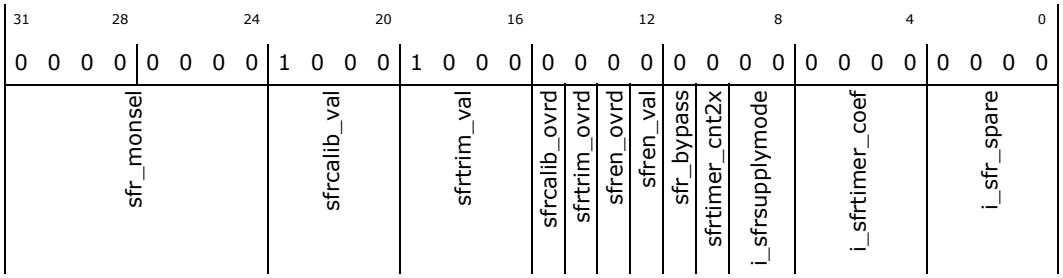
7.13.12 SFRCONFIG_0—Offset 38h

Access Method

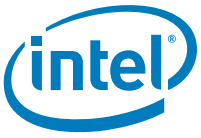
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:, D:, F:] + 38h

Default: 00880000h



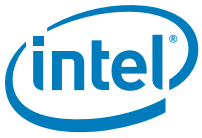
Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**sfr_monsel [31:24] (sfr_monsel):** Select for SFR analog monitor
23:20	0x8 RW	**sfrcalib_val [23:20] (sfrcalib_val):** sfr calibration initial value. Also used as override value when calib_ovrd is 1
19:16	0x8 RW	**sfrtrim_val [19:16] (sfrtrim_val):** EV: sfr trim override value
15	0x0 RW	**sfrcalib_ovrd [15:15] (sfrcalib_ovrd):** EV: sfr calibration is bypassed with sfrcalib_val
14	0x0 RW	**sfrtrim_ovrd [14:14] (sfrtrim_ovrd):** EV: sfr trim override select
13	0x0 RW	**sfren_ovrd [13:13] (sfren_ovrd):** EV: SFR enable override (bypass the power up sequence)
12	0x0 RW	**sfren_val [12:12] (sfren_val):** EV: SFR enable value
11	0x0 RW	**sfr_bypass [11:11] (sfr_bypass):** EV: SFR bypass control
10	0x0 RW	**sfrtimer_cnt2x [10:10] (sfrtimer_cnt2x):** EV: multiplies SFR counters by 2x
9:8	X RW/Strap	**i_sfrsupplymode [9:8] (i_sfrsupplymode):** SFR supply indicator. 01 for 1.35v and 00 for 1.25v
7:4	X RW/Strap	**i_sfrtimer_coef [7:4] (i_sfrtimer_coef):** set this bus to round((Frefclk / 20MHz) - 1) to allow ADPLL generate an absolute timer for SFR trimming, SFR calibration, SFR on and DCO settle
3:0	X RW/Strap	**i_sfr_spare [3:0] (i_sfr_spare):** SFR spare config registers



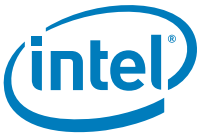
7.14 USB2.0 I/O Configuration Registers

Table 50. Summary of Message Bus Registers—

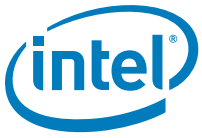
Offset	Register Name (Register Symbol)	Default Value
4100–4103h	"USB2 PER PORT (USB2_PER_PORT_PP0)—Offset 4100h" on page 3101	00055A01h
4200–4203h	"USB2 PER PORT (USB2_PER_PORT_PP1)—Offset 4200h" on page 3104	00055A01h
4300–4303h	"USB2 PER PORT (USB2_PER_PORT_PP2)—Offset 4300h" on page 3108	00055A01h
4400–4403h	"USB2 PER PORT (USB2_PER_PORT_PP3)—Offset 4400h" on page 3111	00055A01h
4500–4503h	"USB2 PER PORT (USB2_PER_PORT_PP4)—Offset 4500h" on page 3115	00055A01h
4001–4004h	"USB2 GLOBAL PORT (USB2_GLOBAL_PORT)—Offset 4001h" on page 3118	0C3D8006h
7F02–7F02h	"USB2 PLL1 (USB2_PLL1)—Offset 7F02h" on page 3122	0E802470h
7F03–7F03h	"USB2 PLL2 (USB2_PLL2)—Offset 7F03h" on page 3124	03000B00h
7F04–7F07h	"USB2 COMPBG (USB2_COMPBG)—Offset 7F04h" on page 3126	00000600h
4105–4105h	"UTMI RX REG1 PER PORT (UTMI_RX_REG1_PER_PORT_PP0)—Offset 4105h" on page 3129	00000000h
4106–4106h	"UTMI RX REG2 PER PORT (UTMI_RX_REG2_PER_PORT_PP0)—Offset 4106h" on page 3129	00000000h
4107–4107h	"UTMI TX REG PER PORT (UTMI_TX_REG_PER_PORT_PP0)—Offset 4107h" on page 3130	00000000h
4108–410Bh	"UTMI MISC REG PER PORT (UTMI_MISC_REG_PER_PORT_PP0)—Offset 4108h" on page 3131	00000050h
4205–4205h	"UTMI RX REG1 PER PORT (UTMI_RX_REG1_PER_PORT_PP1)—Offset 4205h" on page 3133	00000000h
4206–4206h	"UTMI RX REG2 PER PORT (UTMI_RX_REG2_PER_PORT_PP1)—Offset 4206h" on page 3134	00000000h
4207–4207h	"UTMI TX REG PER PORT (UTMI_TX_REG_PER_PORT_PP1)—Offset 4207h" on page 3134	00000000h
4208–420Bh	"UTMI MISC REG PER PORT (UTMI_MISC_REG_PER_PORT_PP1)—Offset 4208h" on page 3135	00000050h
4305–4305h	"UTMI RX REG1 PER PORT (UTMI_RX_REG1_PER_PORT_PP2)—Offset 4305h" on page 3138	00000000h
4306–4306h	"UTMI RX REG2 PER PORT (UTMI_RX_REG2_PER_PORT_PP2)—Offset 4306h" on page 3138	00000000h
4307–4307h	"UTMI TX REG PER PORT (UTMI_TX_REG_PER_PORT_PP2)—Offset 4307h" on page 3138	00000000h



Offset	Register Name (Register Symbol)	Default Value
4308–430Bh	"UTMI MISC REG PER PORT (UTMI_MISC_REG_PER_PORT_PP2)—Offset 4308h" on page 3140	00000050h
4405–4405h	"UTMI RX REG1 PER PORT (UTMI_RX_REG1_PER_PORT_PP3)—Offset 4405h" on page 3142	00000000h
4406–4406h	"UTMI RX REG2 PER PORT (UTMI_RX_REG2_PER_PORT_PP3)—Offset 4406h" on page 3142	00000000h
4407–4407h	"UTMI TX REG PER PORT (UTMI_TX_REG_PER_PORT_PP3)—Offset 4407h" on page 3143	00000000h
4408–440Bh	"UTMI MISC REG PER PORT (UTMI_MISC_REG_PER_PORT_PP3)—Offset 4408h" on page 3144	00000050h
4505–4505h	"UTMI RX REG1 PER PORT (UTMI_RX_REG1_PER_PORT_PP4)—Offset 4505h" on page 3147	00000000h
4506–4506h	"UTMI RX REG2 PER PORT (UTMI_RX_REG2_PER_PORT_PP4)—Offset 4506h" on page 3147	00000000h
4507–4507h	"UTMI TX REG PER PORT (UTMI_TX_REG_PER_PORT_PP4)—Offset 4507h" on page 3147	00000000h
4508–450Bh	"UTMI MISC REG PER PORT (UTMI_MISC_REG_PER_PORT_PP4)—Offset 4508h" on page 3149	00000050h
7F09–7F09h	"RCOMP REGISTER (RCOMP_REGISTER)—Offset 7F09h" on page 3151	81A2040Fh
7F0A–7F0Dh	"ICOMP REGISTER (ICOMP_REGISTER)—Offset 7F0Ah" on page 3152	00008001h
400B–400Bh	"USB2 TEST GLOBAL REG1 (USB2_TEST_GLOBAL_REG1)—Offset 400Bh" on page 3154	00000000h
400C–400Ch	"USB2 TEST GLOBAL REG2 (USB2_TEST_GLOBAL_REG2)—Offset 400Ch" on page 3156	00007FF8h
400D–400Dh	"USB2 TEST GLOBAL REG3 (USB2_TEST_GLOBAL_REG3)—Offset 400Dh" on page 3156	00000000h
400E–400Fh	"USB2 TEST GLOBAL REG4 (USB2_TEST_GLOBAL_REG4)—Offset 400Eh" on page 3157	00000000h
410F–4112h	"ICOMP PERPORT REG (ICOMP_PERPORT_REG_PP0)—Offset 410Fh" on page 3157	00000000h
420F–4212h	"ICOMP PERPORT REG (ICOMP_PERPORT_REG_PP1)—Offset 420Fh" on page 3158	00000000h
430F–4312h	"ICOMP PERPORT REG (ICOMP_PERPORT_REG_PP2)—Offset 430Fh" on page 3158	00000000h
440F–4412h	"ICOMP PERPORT REG (ICOMP_PERPORT_REG_PP3)—Offset 440Fh" on page 3159	00000000h
450F–4512h	"ICOMP PERPORT REG (ICOMP_PERPORT_REG_PP4)—Offset 450Fh" on page 3159	00000000h
4010–4010h	"USB2 TEST GLOBAL REG5 (USB2_TEST_GLOBAL_REG5)—Offset 4010h" on page 3160	00FE00C7h
4011–4011h	"USB2 TEST GLOBAL REG6 (USB2_TEST_GLOBAL_REG6)—Offset 4011h" on page 3161	0003C07Fh

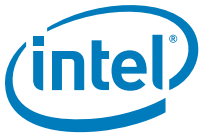


Offset	Register Name (Register Symbol)	Default Value
4012–4015h	"USB2 TEST GLOBAL REG7 (USB2_TEST_GLOBAL_REG7)—Offset 4012h" on page 3163	00000000h
4113–4114h	"USB2 TEST PERPORT REG1 (USB2_TEST_PERPORT_REG1_PP0)—Offset 4113h" on page 3164	00000000h
4213–4214h	"USB2 TEST PERPORT REG1 (USB2_TEST_PERPORT_REG1_PP1)—Offset 4213h" on page 3166	00000000h
4313–4314h	"USB2 TEST PERPORT REG1 (USB2_TEST_PERPORT_REG1_PP2)—Offset 4313h" on page 3168	00000000h
4413–4414h	"USB2 TEST PERPORT REG1 (USB2_TEST_PERPORT_REG1_PP3)—Offset 4413h" on page 3170	00000000h
4513–4514h	"USB2 TEST PERPORT REG1 (USB2_TEST_PERPORT_REG1_PP4)—Offset 4513h" on page 3173	00000000h
7F14–7F17h	"USB2 COMPBG2 (USB2_COMPBG2)—Offset 7F14h" on page 3175	00000080h
4115–4115h	"USB2 VISA PERPORT REG1 (USB2_VISA_PERPORT_REG1_PP0)—Offset 4115h" on page 3176	00000000h
4116–4116h	"USB2 VISA PERPORT REG2 (USB2_VISA_PERPORT_REG2_PP0)—Offset 4116h" on page 3177	00000000h
4117–411Ah	"USB2 VISA PERPORT REG3 (USB2_VISA_PERPORT_REG3_PP0)—Offset 4117h" on page 3178	00000000h
4215–4215h	"USB2 VISA PERPORT REG1 (USB2_VISA_PERPORT_REG1_PP1)—Offset 4215h" on page 3179	00000000h
4216–4216h	"USB2 VISA PERPORT REG2 (USB2_VISA_PERPORT_REG2_PP1)—Offset 4216h" on page 3180	00000000h
4217–421Ah	"USB2 VISA PERPORT REG3 (USB2_VISA_PERPORT_REG3_PP1)—Offset 4217h" on page 3181	00000000h
4315–4315h	"USB2 VISA PERPORT REG1 (USB2_VISA_PERPORT_REG1_PP2)—Offset 4315h" on page 3182	00000000h
4316–4316h	"USB2 VISA PERPORT REG2 (USB2_VISA_PERPORT_REG2_PP2)—Offset 4316h" on page 3183	00000000h
4317–431Ah	"USB2 VISA PERPORT REG3 (USB2_VISA_PERPORT_REG3_PP2)—Offset 4317h" on page 3184	00000000h
4415–4415h	"USB2 VISA PERPORT REG1 (USB2_VISA_PERPORT_REG1_PP3)—Offset 4415h" on page 3185	00000000h
4416–4416h	"USB2 VISA PERPORT REG2 (USB2_VISA_PERPORT_REG2_PP3)—Offset 4416h" on page 3186	00000000h
4417–441Ah	"USB2 VISA PERPORT REG3 (USB2_VISA_PERPORT_REG3_PP3)—Offset 4417h" on page 3187	00000000h
4515–4515h	"USB2 VISA PERPORT REG1 (USB2_VISA_PERPORT_REG1_PP4)—Offset 4515h" on page 3188	00000000h
4516–4516h	"USB2 VISA PERPORT REG2 (USB2_VISA_PERPORT_REG2_PP4)—Offset 4516h" on page 3189	00000000h
4517–451Ah	"USB2 VISA PERPORT REG3 (USB2_VISA_PERPORT_REG3_PP4)—Offset 4517h" on page 3190	00000000h



Offset	Register Name (Register Symbol)	Default Value
4018–4018h	"USB2 VISA GLOBAL REG1 (USB2_VISA_GLOBAL_REG1)—Offset 4018h" on page 3191	00000000h
4019–4019h	"USB2 VISA GLOBAL REG2 (USB2_VISA_GLOBAL_REG2)—Offset 4019h" on page 3192	00000000h
401A–401Dh	"USB2 VISA GLOBAL REG3 (USB2_VISA_GLOBAL_REG3)—Offset 401Ah" on page 3192	00000000h
411B–411Bh	"USB2 SQ DPDM OFFSET PERPORT REG (USB2_SQ_DPDM_OFFSET_PERPORT_REG_PP0)—Offset 411Bh" on page 3193	20404080h
411C–411Ch	"USB2 SQ DMDP OFFSET PERPORT REG (USB2_SQ_DMDP_OFFSET_PERPORT_REG_PP0)—Offset 411Ch" on page 3195	20404080h
411D–4120h	"USB2 DIS OFFSET PERPORT REG (USB2_DIS_OFFSET_PERPORT_REG_PP0)—Offset 411Dh" on page 3197	20408100h
421B–421Bh	"USB2 SQ DPDM OFFSET PERPORT REG (USB2_SQ_DPDM_OFFSET_PERPORT_REG_PP1)—Offset 421Bh" on page 3199	20404080h
421C–421Ch	"USB2 SQ DMDP OFFSET PERPORT REG (USB2_SQ_DMDP_OFFSET_PERPORT_REG_PP1)—Offset 421Ch" on page 3202	20404080h
421D–4220h	"USB2 DIS OFFSET PERPORT REG (USB2_DIS_OFFSET_PERPORT_REG_PP1)—Offset 421Dh" on page 3204	20408100h
431B–431Bh	"USB2 SQ DPDM OFFSET PERPORT REG (USB2_SQ_DPDM_OFFSET_PERPORT_REG_PP2)—Offset 431Bh" on page 3206	20404080h
431C–431Ch	"USB2 SQ DMDP OFFSET PERPORT REG (USB2_SQ_DMDP_OFFSET_PERPORT_REG_PP2)—Offset 431Ch" on page 3208	20404080h
431D–4320h	"USB2 DIS OFFSET PERPORT REG (USB2_DIS_OFFSET_PERPORT_REG_PP2)—Offset 431Dh" on page 3210	20408100h
441B–441Bh	"USB2 SQ DPDM OFFSET PERPORT REG (USB2_SQ_DPDM_OFFSET_PERPORT_REG_PP3)—Offset 441Bh" on page 3212	20404080h
441C–441Ch	"USB2 SQ DMDP OFFSET PERPORT REG (USB2_SQ_DMDP_OFFSET_PERPORT_REG_PP3)—Offset 441Ch" on page 3215	20404080h
441D–4420h	"USB2 DIS OFFSET PERPORT REG (USB2_DIS_OFFSET_PERPORT_REG_PP3)—Offset 441Dh" on page 3217	20408100h
451B–451Bh	"USB2 SQ DPDM OFFSET PERPORT REG (USB2_SQ_DPDM_OFFSET_PERPORT_REG_PP4)—Offset 451Bh" on page 3219	20404080h
451C–451Ch	"USB2 SQ DMDP OFFSET PERPORT REG (USB2_SQ_DMDP_OFFSET_PERPORT_REG_PP4)—Offset 451Ch" on page 3221	20404080h
451D–4520h	"USB2 DIS OFFSET PERPORT REG (USB2_DIS_OFFSET_PERPORT_REG_PP4)—Offset 451Dh" on page 3223	20408100h
7F1E–7F20h	"USB2 SQDIS OFFSET GLOBAL REG (USB2_SQDIS_OFFSET_GLOBAL_REG)—Offset 7F1Eh" on page 3225	00000015h
401F–401Fh	"USB2 DEVICE MODE GLOBAL REG (USB2_DEVICE_MODE_GLOBAL_REG)—Offset 401Fh" on page 3226	00000018h
4020–4023h	"USB2 TEST GLOBAL SERIAL LOOPBACK (USB2_TEST_GLOBAL_SERIAL_LOOPBACK)—Offset 4020h" on page 3228	00000000h
7F21–7F24h	"USB2 GLOBAL COMP CMP OFFSET REG (USB2_GLOBAL_COMP_CMP_OFFSET_REG)—Offset 7F21h" on page 3229	20408100h

Offset	Register Name (Register Symbol)	Default Value
4122–4122h	"PER PORT RCOMP HS PULLUP REGISTER (PER_PORT_RCOMP_HS_PULLUP_REGISTER_PP0)—Offset 4122h" on page 3231	00004011h
4123–4125h	"PER PORT RCOMP HS PULLDOWN REGISTER (PER_PORT_RCOMP_HS_PULLDOWN_REGISTER_PP0)—Offset 4123h" on page 3232	00004011h
4222–4222h	"PER PORT RCOMP HS PULLUP REGISTER (PER_PORT_RCOMP_HS_PULLUP_REGISTER_PP1)—Offset 4222h" on page 3234	00004011h
4223–4225h	"PER PORT RCOMP HS PULLDOWN REGISTER (PER_PORT_RCOMP_HS_PULLDOWN_REGISTER_PP1)—Offset 4223h" on page 3235	00004011h
4322–4322h	"PER PORT RCOMP HS PULLUP REGISTER (PER_PORT_RCOMP_HS_PULLUP_REGISTER_PP2)—Offset 4322h" on page 3237	00004011h
4323–4325h	"PER PORT RCOMP HS PULLDOWN REGISTER (PER_PORT_RCOMP_HS_PULLDOWN_REGISTER_PP2)—Offset 4323h" on page 3238	00004011h
4422–4422h	"PER PORT RCOMP HS PULLUP REGISTER (PER_PORT_RCOMP_HS_PULLUP_REGISTER_PP3)—Offset 4422h" on page 3240	00004011h
4423–4425h	"PER PORT RCOMP HS PULLDOWN REGISTER (PER_PORT_RCOMP_HS_PULLDOWN_REGISTER_PP3)—Offset 4423h" on page 3241	00004011h
4522–4522h	"PER PORT RCOMP HS PULLUP REGISTER (PER_PORT_RCOMP_HS_PULLUP_REGISTER_PP4)—Offset 4522h" on page 3243	00004011h
4523–4525h	"PER PORT RCOMP HS PULLDOWN REGISTER (PER_PORT_RCOMP_HS_PULLDOWN_REGISTER_PP4)—Offset 4523h" on page 3244	00004011h
4024–4024h	"GLOBAL RCOMP CL 45OHM 15K PULLDOWN REGISTER (GLOBAL_RCOMP_CL_45OHM_15K_PULLDOWN_REGISTER)—Offset 4024h" on page 3246	00007F11h
4025–4028h	"GLOBAL RCOMP CL 1POINT5K PULL-UP REGISTER (GLOBAL_RCOMP_CL_1POINT5K_PULLUP_REGISTER)—Offset 4025h" on page 3247	00004011h
4126–4127h	"USB2 PER PORT 2 (USB2_PER_PORT_2_PP0)—Offset 4126h" on page 3249	00829248h
4226–4227h	"USB2 PER PORT 2 (USB2_PER_PORT_2_PP1)—Offset 4226h" on page 3252	00829248h
4326–4327h	"USB2 PER PORT 2 (USB2_PER_PORT_2_PP2)—Offset 4326h" on page 3254	00829248h
4426–4427h	"USB2 PER PORT 2 (USB2_PER_PORT_2_PP3)—Offset 4426h" on page 3257	00829248h
4526–4527h	"USB2 PER PORT 2 (USB2_PER_PORT_2_PP4)—Offset 4526h" on page 3260	00829248h
7F27–7F2Ah	"USB2 PLL3 (USB2_PLL3)—Offset 7F27h" on page 3262	D0413866h
4128–412Bh	"PER PORT LOOPBACK CONTROL (PER_PORT_LOOPBACK_CONTROL_PP0)—Offset 4128h" on page 3264	00000000h
4228–422Bh	"PER PORT LOOPBACK CONTROL (PER_PORT_LOOPBACK_CONTROL_PP1)—Offset 4228h" on page 3265	00000000h
4328–432Bh	"PER PORT LOOPBACK CONTROL (PER_PORT_LOOPBACK_CONTROL_PP2)—Offset 4328h" on page 3267	00000000h



Offset	Register Name (Register Symbol)	Default Value
4428–442Bh	"PER PORT LOOPBACK CONTROL (PER_PORT_LOOPBACK_CONTROL_PP3)—Offset 4428h" on page 3269	00000000h
4528–452Bh	"PER PORT LOOPBACK CONTROL (PER_PORT_LOOPBACK_CONTROL_PP4)—Offset 4528h" on page 3270	00000000h
4029–4029h	"GLB ADP OFFSET REG (GLB_ADP_OFFSET_REG)—Offset 4029h" on page 3272	20408100h
402A–402Ah	"GLB VBUS OFFSET REG (GLB_VBUS_OFFSET_REG)—Offset 402Ah" on page 3274	20408100h
402B–402Bh	"GLB ADP VBUS COMP REG (GLB_ADP_VBUS_COMP_REG)—Offset 402Bh" on page 3276	002A4005h
402C–402Ch	"USB2 GLOBAL PORT 2 (USB2_GLOBAL_PORT_2)—Offset 402Ch" on page 3278	00625000h
402D–402Dh	"GLB CLOCK PORT 0/1 REPEATER (GLB_CLOCK_PORT_0_1_REPEATER)—Offset 402Dh" on page 3281	00000000h
402E–402Eh	"GLB CLOCK PORT 2/3 REPEATER (GLB_CLOCK_PORT_2_3_REPEATER)—Offset 402Eh" on page 3282	00000000h
402F–402Fh	"GLB CLOCK PORT 4/5 REPEATER (GLB_CLOCK_PORT_4_5_REPEATER)—Offset 402Fh" on page 3282	00000000h
4030–4030h	"GLB CLOCK PORT 6/7 REPEATER (GLB_CLOCK_PORT_6_7_REPEATER)—Offset 4030h" on page 3283	00000000h
4031–4031h	"GLB CLOCK PORT 8/9 REPEATER (GLB_CLOCK_PORT_8_9_REPEATER)—Offset 4031h" on page 3283	00000000h
4032–4032h	"GLB CLOCK PORT 10/11 REPEATER (GLB_CLOCK_PORT_10_11_REPEATER)—Offset 4032h" on page 3284	00000000h
4033–4033h	"GLB CLOCK PORT 12/13 REPEATER (GLB_CLOCK_PORT_12_13_REPEATER)—Offset 4033h" on page 3285	00000000h
4034–4034h	"GLB CLOCK PORT 14/15 REPEATER (GLB_CLOCK_PORT_14_15_REPEATER)—Offset 4034h" on page 3285	00000000h
4035–4035h	"GLB LDO MSTR REG 1 (GLB_LDO_MSTR_REG_1)—Offset 4035h" on page 3286	A8000000h
4036–4036h	"GLB LDO MSTR REG 2 (GLB_LDO_MSTR_REG_2)—Offset 4036h" on page 3288	80650F80h
4037–4037h	"GLB LDO SLV REG 1 (GLB_LDO_SLV_REG_1)—Offset 4037h" on page 3290	A8000000h
4038–403Bh	"GLB LDO SLV REG 2 (GLB_LDO_SLV_REG_2)—Offset 4038h" on page 3292	80650F80h
4139–4139h	"PP LDO SLV REG 1 (PP_LDO_SLV_REG_1_PP0)—Offset 4139h" on page 3294	A8000000h
413A–413Dh	"PP LDO SLV REG 2 (PP_LDO_SLV_REG_2_PP0)—Offset 413Ah" on page 3295	80650F80h
4239–4239h	"PP LDO SLV REG 1 (PP_LDO_SLV_REG_1_PP1)—Offset 4239h" on page 3297	A8000000h
423A–423Dh	"PP LDO SLV REG 2 (PP_LDO_SLV_REG_2_PP1)—Offset 423Ah" on page 3299	80650F80h

Offset	Register Name (Register Symbol)	Default Value
4339–4339h	"PP LDO SLV REG 1 (PP_LDO_SLV_REG_1_PP2)—Offset 4339h" on page 3301	A8000000h
433A–433Dh	"PP LDO SLV REG 2 (PP_LDO_SLV_REG_2_PP2)—Offset 433Ah" on page 3303	80650F80h
4439–4439h	"PP LDO SLV REG 1 (PP_LDO_SLV_REG_1_PP3)—Offset 4439h" on page 3305	A8000000h
443A–443Dh	"PP LDO SLV REG 2 (PP_LDO_SLV_REG_2_PP3)—Offset 443Ah" on page 3307	80650F80h
4539–4539h	"PP LDO SLV REG 1 (PP_LDO_SLV_REG_1_PP4)—Offset 4539h" on page 3309	A8000000h
453A–453Dh	"PP LDO SLV REG 2 (PP_LDO_SLV_REG_2_PP4)—Offset 453Ah" on page 3311	80650F80h

7.14.1 USB2 PER PORT (USB2_PER_PORT_PP0)—Offset 4100h

Access Method

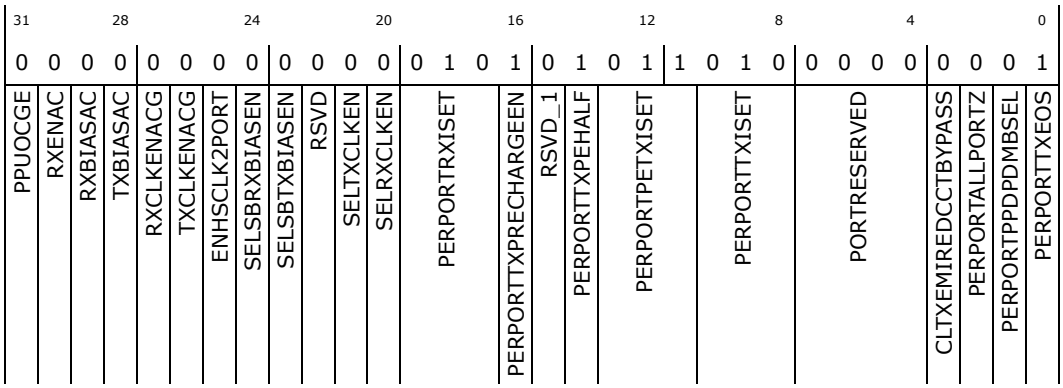
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4100h

Op Codes:

h - Read, h - Write

Default: 00055A01h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Per-Port UTMI_CLK Output Clock Gating Enable (PPUOCGE):** 1: Dynamic Clock Gating is enabled based on L1/L2 suspend indicator. This is the recommended setting for SYNOPSYS based controllers. 0: Output UTMI_CLK is running unless USB PLL is shutdown. This is the recommended setting for FRESCO based controllers. **Power Well:** SUS
30	0x0 RW	**RX EN AFE Control (RXENAC):** 1: Enables the dynamic RX EN behavior. This allows compensation code updates at various boundaries. 0: Disables the dynamic RX EN behavior (function of TXVALID only). RXENAC, RXBIASAC: 00: Legacy mode 01: Illegal 10: Allows additional code update window 11: Allows additional code update window with power saving **Power Well:** SUS
29	0x0 RW	**RX BIAS AFE Control (RXBIASAC):** 1: Enables the AFE bias control 0: Disables the AFE bias control This bit is only valid when internal RXBIAS policy is selected (SELSBRXBIASEN = 0b). **Power Well:** SUS
28	0x0 RW	**TX BIAS AFE Control (TXBIASAC):** 1: Enables the AFE bias control 0: Disables the AFE bias control This bit is only valid when internal TXBIAS policy is selected (SELSBTXBIASEN = 0b). **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
27	0x0 RW	**RX CLKEN AFE Clock Gating (RXCLKENACG):** 1: Enables the AFE clock gating 0: Disables the AFE clock gating This bit is only valid when internal RXCLKEN policy is selected (SELRXCLKEN = 0b). **Power Well:** SUS
26	0x0 RW	**TX CLKEN AFE Clock Gating (TXCLKENACG):** 1: Enables the AFE clock gating 0: Disables the AFE clock gating This bit is only valid when internal TXCLKEN policy is selected (SELTXCLKEN = 0b). **Power Well:** SUS
25	0x0 RW	**ENHSCLK2PORT:** This per-port pin will generate HS clock data pattern for testing purposes for that port and ignore the core data during Tx: 1: The port will transmit 10101..clock data pattern when txen=1. 0: The port will resume to c73usb250_normal operation where data is generated by the controller. **Power Well:** SUS
24	0x0 RW	**SELSBRXBIASEN:** This is to select between the UTMI internal vs. side-band control over the AFE RX bias enable signal. 1 - select side-band control from Intel SIP controller. 0 - select UTMI internally generated control. This is to be used with third party or external controller IP. **Power Well:** SUS
23	0x0 RW	**SELSBTXBIASEN:** This is to select between the UTMI internal vs. side-band control over the AFE TX bias enable signal. 1 - select side-band control from Intel SIP controller. 0 - select UTMI internally generated control. This is to be used with third party or external controller IP. **Power Well:** SUS
22	0x0 WO	**RSVD:** RSVD (RSVD): FORCEPPICOMP (FORCEPPICOMP): Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Testmode When set to 1b, this will force per-port icomp offset cancellation Finite State Machine to start calibrating. BIOS has to wait for sufficient time for the calibration complete. This is a pulse trigger event. **Power Well:** SUS
21	0x0 RW	**SELTXCLKEN:** This is to select between internal mode vs. side-band control on the TX clock enable signal. 0 - override for TXCLKEN to be internally controlled. To be used with third party or external controller IP. 1 - select side-band control from Intel SIP controller. **Power Well:** SUS
20	0x0 RW	**SELRXCLKEN:** This is to select between internal mode vs. side-band control on the RX clock enable signal. 0 - override for RXCLKEN to be internally controlled. To be used with third party or external controller IP. 1 - select side-band control from Intel SIP controller. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
19:17	0x2 RW	**PerPort HS Receiver Bias (PERPORTRXISET):** Config bit (per port) HS Receiver Bias current offset bit (2:0) 000 - 80uA 001 - 90uA 010 (default) - 100uA 011 - 110uA 100 - 120uA 101 - 130uA 110 - 140uA 111 - 150uA **Power Well:** SUS
16	0x1 RW	**PerPort Common Mode Pre-charge (PERPORTTXPRECHARGEEN):** Config bit (per port) To select whether to enable or disable the common mode pre-charge during SOP and EOP. Pre-charge hold for 4 cycles before first data transmission. This is to allow common choke ring back to settle down before driving first data bit to meet eye opening spec. 1 - pre-charge ON 0 - pre-charge OFF **Power Well:** SUS
15	0x0 RW	**RSVD (RSVD_1):** Reserved. **Power Well:** SUS
14	0x1 RW	**PerPort Half Bit Pre-emphasis (PERPORTTXPEHALF):** Config bit (per port) to select between half-bit or full-bit implementation 1 - select half-bit pre-emphasis 0 - select full-bit pre-emphasis. **Power Well:** SUS
13:11	0x3 RW	**PerPort HS Pre-emphasis Bias (PERPORTPETXISET):** Config bit (per port) HS Pre-emphasis Bias current offset bit (2:0) Value Preempen: deempen = 01 (De-emphasis ON) Preempen: deempen = 10 (Pre-emphasis ON) Preempen: deempen = 11 (preemphasis strength/demphasis strength) 000 0mV 0mV 0mV 001 11.25mV 11.25mV 11.25mV/11.25mV 010 16.9mV 16.9mV 16.9mV/16.9mV 011 (default) 28.15mV 28.15mV 28.15mV/ 28.15mV 100 28.15mV 28.15mV 28.15mV/28.15mV 101 39.35mV 39.35mV 39.35mV/39.35mV 110 45mV 45mV 45mV/45mV 111 56.3mV 56.3mV 56.3mV/56.3mV. **Power Well:** SUS
10:8	0x2 RW	**PerPort HS Transmitter Bias (PERPORTTXISET):** Config bit (per port) HS Pre-emphasis Bias current offset bit2 (2:0) Value Preempen: deempen = 01 (De-emphasis ON) Preempen: deempen = 10 (Pre-emphasis ON) Preempen: deempen = 11 (preemphasis strength/demphasis strength) 000 0mV 0mV 0mV 001 11.25mV 11.25mV -11.25mV/11.25mV 010 16.9mV 16.9mV -16.9mV/16.9mV 011 (default) 28.15mV 28.15mV -28.15mV/ 28.15mV 100 28.15mV 28.15mV -28.15mV/28.15mV 101 39.35mV 39.35mV -39.35mV/39.35mV 110 45mV 45mV -45mV/45mV 111 56.3mV 56.3mV -56.3mV/56.3mV **Power Well:** SUS
7:4	0x0 RW	**PORTRESERVED_0123 (PORTRESERVED):** PORTRESERVED (PORTRESERVED): Reserved pin for future functionality of the respective ports **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**CL TX EMI Reduction Circuit Bypass (CLTXEMIREDCCTBYPASS):** Chicken bit for CL TX EMI reduction circuit bypass. Assert 1 to bypass the EMI reduction circuit. Default is 0b. AFE pin remains as PORTRESERVED for this project. **Power Well:** SUS
2	0x0 RW	**PERPORT ALLPORTZ (PERPORTALLPORTZ):** Legacy pin. No longer carries any functionality as the pull-down enable is now controlled by ilane5:0usbpdnen_h **Power Well:** SUS
1	0x0 RW	**PERPORT PPDPDMBSEL (PERPORTPPDPDMBSEL):** Config bit to select comparator 2:1 mux input either dp or dm for HS TX per port current calibration 1 - select dp (for debug purpose only) 0 - select dm (without 1.5K pullup) **Power Well:** SUS
0	0x1 RW	**PERPORT TX EOS protection enable (PERPORTTXEOS):** Set to 1b enables the TX EOS protection. To protect high speed driver passgate. This feature is not required for P1269.8. **Power Well:** SUS

7.14.2 USB2 PER PORT (USB2_PER_PORT_PP1)—Offset 4200h

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4200h

Op Codes:

h - Read, h - Write

Default: 00055A01h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	1
PPUOCGE	RXENAC	RXBIASAC	TXBIASAC	RXCLKENACG	TXCLKENACG	ENHSCLK2PORT	SELSBRXBIASEN	SELSBTXBIASEN	RSVD	SELTXCLKEN	SELRXCLKEN	PERPORTRXISET			PERPORTTXPRECHARGEEN	RSVD_1	PERPORTTXPEHALF	PERPORTPETXISET		PERPORTTXISET		PORTRESERVED				CLTXEMIREDCCTBYPASS	PERPORTALLPORTZ	PERPORTPPDPDMBSEL	PERPORTTXEOS		

Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Per-Port UTMI_CLK Output Clock Gating Enable (PPUOCGE):** 1: Dynamic Clock Gating is enabled based on L1/L2 suspend indicator. This is the recommended setting for SYNOPSYS based controllers. 0: Output UTMI_CLK is running unless USB PLL is shutdown. This is the recommended setting for FRESCO based controllers. **Power Well:** SUS
30	0x0 RW	**RX EN AFE Control (RXENAC):** 1: Enables the dynamic RX EN behavior. This allows compensation code updates at various boundaries. 0: Disables the dynamic RX EN behavior (function of TXVALID only). RXENAC, RXBIASAC: 00: Legacy mode 01: Illegal 10: Allows additional code update window 11: Allows additional code update window with power saving **Power Well:** SUS
29	0x0 RW	**RX BIAS AFE Control (RXBIASAC):** 1: Enables the AFE bias control 0: Disables the AFE bias control This bit is only valid when internal RXBIAS policy is selected (SELSBRXBIASEN = 0b). **Power Well:** SUS
28	0x0 RW	**TX BIAS AFE Control (TXBIASAC):** 1: Enables the AFE bias control 0: Disables the AFE bias control This bit is only valid when internal TXBIAS policy is selected (SELSBTXBIASEN = 0b). **Power Well:** SUS
27	0x0 RW	**RX CLKEN AFE Clock Gating (RXCLKENACG):** 1: Enables the AFE clock gating 0: Disables the AFE clock gating This bit is only valid when internal RXCLKEN policy is selected (SELRXCLKEN = 0b). **Power Well:** SUS
26	0x0 RW	**TX CLKEN AFE Clock Gating (TXCLKENACG):** 1: Enables the AFE clock gating 0: Disables the AFE clock gating This bit is only valid when internal TXCLKEN policy is selected (SELTXCLKEN = 0b). **Power Well:** SUS
25	0x0 RW	**ENHSCLK2PORT:** This per-port pin will generate HS clock data pattern for testing purposes for that port and ignore the core data during Tx: 1: The port will transmit 10101..clock data pattern when txen=1. 0: The port will resume to c73usb250_normal operation where data is generated by the controller. **Power Well:** SUS
24	0x0 RW	**SELSBRXBIASEN:** This is to select between the UTMI internal vs. side-band control over the AFE RX bias enable signal. 1 - select side-band control from Intel SIP controller. 0 - select UTMI internally generated control. This is to be used with third party or external controller IP. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
23	0x0 RW	**SELSBTXBIASEN:** This is to select between the UTMI internal vs. side-band control over the AFE TX bias enable signal. 1 - select side-band control from Intel SIP controller. 0 - select UTMI internally generated control. This is to be used with third party or external controller IP. **Power Well:** SUS
22	0x0 WO	**RSVD:** RSVD (RSVD): FORCEPPICOMP (FORCEPPICOMP): Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Testmode When set to 1b, this will force per-port icomp offset cancellation Finite State Machine to start calibrating. BIOS has to wait for sufficient time for the calibration complete. This is a pulse trigger event. **Power Well:** SUS
21	0x0 RW	**SELTXCLKEN:** This is to select between internal mode vs. side-band control on the TX clock enable signal. 0 - override for TXCLKEN to be internally controlled. To be used with third party or external controller IP. 1 - select side-band control from Intel SIP controller. **Power Well:** SUS
20	0x0 RW	**SELRXCLKEN:** This is to select between internal mode vs. side-band control on the RX clock enable signal. 0 - override for RXCLKEN to be internally controlled. To be used with third party or external controller IP. 1 - select side-band control from Intel SIP controller. **Power Well:** SUS
19:17	0x2 RW	**PerPort HS Receiver Bias (PERPORTRXISET):** Config bit (per port) HS Receiver Bias current offset bit (2:0) 000 - 80uA 001 - 90uA 010 (default) - 100uA 011 - 110uA 100 - 120uA 101 - 130uA 110 - 140uA 111 - 150uA **Power Well:** SUS
16	0x1 RW	**PerPort Common Mode Pre-charge (PERPORTTXPRECHARGEEN):** Config bit (per port) To select whether to enable or disable the common mode pre-charge during SOP and EOP. Pre-charge hold for 4 cycles before first data transmission. This is to allow common choke ring back to settle down before driving first data bit to meet eye opening spec. 1 - pre-charge ON 0 - pre-charge OFF **Power Well:** SUS
15	0x0 RW	**RSVD (RSVD_1):** Reserved. **Power Well:** SUS
14	0x1 RW	**PerPort Half Bit Pre-emphasis (PERPORTTXPEHALF):** Config bit (per port) to select between half-bit or full-bit implementation 1 - select half-bit pre-emphasis 0 - select full-bit pre-emphasis. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
13:11	0x3 RW	**PerPort HS Pre-emphasis Bias (PERPORTPETXISET):** Config bit (per port) HS Pre-emphasis Bias current offset bit (2:0) Value Preempen: deempen = 01 (De-emphasis ON) Preempen: deempen = 10 (Pre-emphasis ON) Preempen: deempen = 11 (preemphasis strength/demphasis strength) 000 0mV 0mV 0mV 001 11.25mV 11.25mV 11.25mV/11.25mV 010 16.9mV 16.9mV 16.9mV/16.9mV 011 (default) 28.15mV 28.15mV 28.15mV/ 28.15mV 100 28.15mV 28.15mV 28.15mV/28.15mV 101 39.35mV 39.35mV 39.35mV/39.35mV 110 45mV 45mV 45mV/45mV 111 56.3mV 56.3mV 56.3mV/56.3mV. **Power Well:** SUS
10:8	0x2 RW	**PerPort HS Transmitter Bias (PERPORTTXISET):** Config bit (per port) HS Pre-emphasis Bias current offset bit2 (2:0) Value Preempen: deempen = 01 (De-emphasis ON) Preempen: deempen = 10 (Pre-emphasis ON) Preempen: deempen = 11 (preemphasis strength/demphasis strength) 000 0mV 0mV 0mV 001 11.25mV 11.25mV -11.25mV/11.25mV 010 16.9mV 16.9mV -16.9mV/16.9mV 011 (default) 28.15mV 28.15mV -28.15mV/ 28.15mV 100 28.15mV 28.15mV -28.15mV/28.15mV 101 39.35mV 39.35mV -39.35mV/39.35mV 110 45mV 45mV -45mV/45mV 111 56.3mV 56.3mV -56.3mV/56.3mV **Power Well:** SUS
7:4	0x0 RW	**PORTRESERVED_0123 (PORTRESERVED):** PORTRESERVED (PORTRESERVED): Reserved pin for future functionality of the respective ports **Power Well:** SUS
3	0x0 RW	**CL TX EMI Reduction Circuit Bypass (CLTXEMIREDCCTBYPASS):** Chicken bit for CL TX EMI reduction circuit bypass. Assert 1 to bypass the EMI reduction circuit. Default is 0b. AFE pin remains as PORTRESERVED for this project. **Power Well:** SUS
2	0x0 RW	**PERPORT ALLPORTZ (PERPORTALLPORTZ):** Legacy pin. No longer carries any functionality as the pull-down enable is now controlled by ilane5:0usbpdnen_h **Power Well:** SUS
1	0x0 RW	**PERPORT PPDPDMBSEL (PERPORTPPDPDMBSEL):** Config bit to select comparator 2:1 mux input either dp or dm for HS TX per port current calibration 1 - select dp (for debug purpose only) 0 - select dm (without 1.5K pullup) **Power Well:** SUS
0	0x1 RW	**PERPORT TX EOS protection enable (PERPORTTXEOS):** Set to 1b enables the TX EOS protection. To protect high speed driver passgate. This feature is not required for P1269.8. **Power Well:** SUS

7.14.3 USB2 PER PORT (USB2_PER_PORT_PP2)—Offset 4300h

Access Method

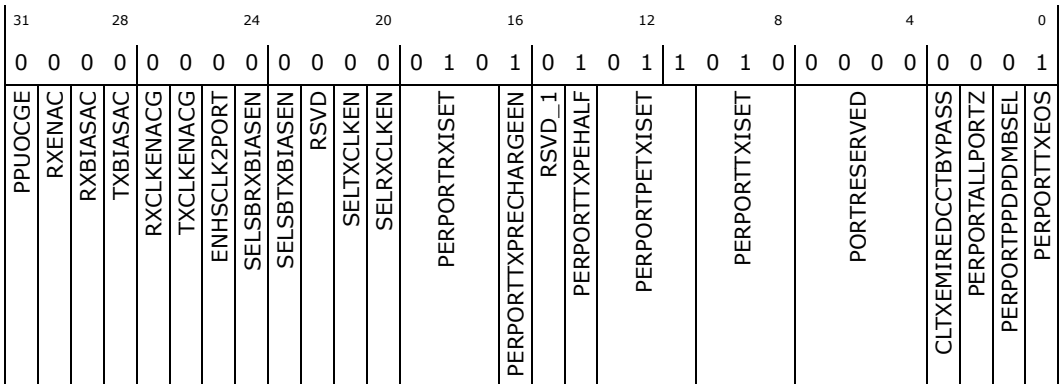
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4300h

Op Codes:

h - Read, h - Write

Default: 00055A01h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Per-Port UTMI_CLK Output Clock Gating Enable (PPUOCGE):** 1: Dynamic Clock Gating is enabled based on L1/L2 suspend indicator. This is the recommended setting for SYNOPSYS based controllers. 0: Output UTMI_CLK is running unless USB PLL is shutdown. This is the recommended setting for FRESCO based controllers. **Power Well:** SUS
30	0x0 RW	**RX EN AFE Control (RXENAC):** 1: Enables the dynamic RX EN behavior. This allows compensation code updates at various boundaries. 0: Disables the dynamic RX EN behavior (function of TXVALID only). RXENAC, RXBIASAC: 00: Legacy mode 01: Illegal 10: Allows additional code update window 11: Allows additional code update window with power saving **Power Well:** SUS
29	0x0 RW	**RX BIAS AFE Control (RXBIASAC):** 1: Enables the AFE bias control 0: Disables the AFE bias control This bit is only valid when internal RXBIAS policy is selected (SELSBRXBIASEN = 0b). **Power Well:** SUS
28	0x0 RW	**TX BIAS AFE Control (TXBIASAC):** 1: Enables the AFE bias control 0: Disables the AFE bias control This bit is only valid when internal TXBIAS policy is selected (SELSBTXBIASEN = 0b). **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
27	0x0 RW	**RX CLKEN AFE Clock Gating (RXCLKENACG):** 1: Enables the AFE clock gating 0: Disables the AFE clock gating This bit is only valid when internal RXCLKEN policy is selected (SELRXCLKEN = 0b). **Power Well:** SUS
26	0x0 RW	**TX CLKEN AFE Clock Gating (TXCLKENACG):** 1: Enables the AFE clock gating 0: Disables the AFE clock gating This bit is only valid when internal TXCLKEN policy is selected (SELTXCLKEN = 0b). **Power Well:** SUS
25	0x0 RW	**ENHSCLK2PORT:** This per-port pin will generate HS clock data pattern for testing purposes for that port and ignore the core data during Tx: 1: The port will transmit 10101..clock data pattern when txen=1. 0: The port will resume to c73usb250_normal operation where data is generated by the controller. **Power Well:** SUS
24	0x0 RW	**SELSBRXBIASEN:** This is to select between the UTMI internal vs. side-band control over the AFE RX bias enable signal. 1 - select side-band control from Intel SIP controller. 0 - select UTMI internally generated control. This is to be used with third party or external controller IP. **Power Well:** SUS
23	0x0 RW	**SELSBTXBIASEN:** This is to select between the UTMI internal vs. side-band control over the AFE TX bias enable signal. 1 - select side-band control from Intel SIP controller. 0 - select UTMI internally generated control. This is to be used with third party or external controller IP. **Power Well:** SUS
22	0x0 WO	**RSVD:** RSVD (RSVD): FORCEPPICOMP (FORCEPPICOMP): Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Testmode When set to 1b, this will force per-port icomp offset cancellation Finite State Machine to start calibrating. BIOS has to wait for sufficient time for the calibration complete. This is a pulse trigger event. **Power Well:** SUS
21	0x0 RW	**SELTXCLKEN:** This is to select between internal mode vs. side-band control on the TX clock enable signal. 0 - override for TXCLKEN to be internally controlled. To be used with third party or external controller IP. 1 - select side-band control from Intel SIP controller. **Power Well:** SUS
20	0x0 RW	**SELRXCLKEN:** This is to select between internal mode vs. side-band control on the RX clock enable signal. 0 - override for RXCLKEN to be internally controlled. To be used with third party or external controller IP. 1 - select side-band control from Intel SIP controller. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
19:17	0x2 RW	**PerPort HS Receiver Bias (PERPORTRXISET):** Config bit (per port) HS Receiver Bias current offset bit (2:0) 000 - 80uA 001 - 90uA 010 (default) - 100uA 011 - 110uA 100 - 120uA 101 - 130uA 110 - 140uA 111 - 150uA **Power Well:** SUS
16	0x1 RW	**PerPort Common Mode Pre-charge (PERPORTTXPRECHARGEEN):** Config bit (per port) To select whether to enable or disable the common mode pre-charge during SOP and EOP. Pre-charge hold for 4 cycles before first data transmission. This is to allow common choke ring back to settle down before driving first data bit to meet eye opening spec. 1 - pre-charge ON 0 - pre-charge OFF **Power Well:** SUS
15	0x0 RW	**RSVD (RSVD_1):** Reserved. **Power Well:** SUS
14	0x1 RW	**PerPort Half Bit Pre-emphasis (PERPORTTXPEHALF):** Config bit (per port) to select between half-bit or full-bit implementation 1 - select half-bit pre-emphasis 0 - select full-bit pre-emphasis. **Power Well:** SUS
13:11	0x3 RW	**PerPort HS Pre-emphasis Bias (PERPORTPETXISET):** Config bit (per port) HS Pre-emphasis Bias current offset bit (2:0) Value Preempen: deempen = 01 (De-emphasis ON) Preempen: deempen = 10 (Pre-emphasis ON) Preempen: deempen = 11 (preemphasis strength/demphasis strength) 000 0mV 0mV 0mV 001 11.25mV 11.25mV 11.25mV/11.25mV 010 16.9mV 16.9mV 16.9mV/16.9mV 011 (default) 28.15mV 28.15mV 28.15mV/ 28.15mV 100 28.15mV 28.15mV 28.15mV/28.15mV 101 39.35mV 39.35mV 39.35mV/39.35mV 110 45mV 45mV 45mV/45mV 111 56.3mV 56.3mV 56.3mV/56.3mV. **Power Well:** SUS
10:8	0x2 RW	**PerPort HS Transmitter Bias (PERPORTTXISET):** Config bit (per port) HS Pre-emphasis Bias current offset bit2 (2:0) Value Preempen: deempen = 01 (De-emphasis ON) Preempen: deempen = 10 (Pre-emphasis ON) Preempen: deempen = 11 (preemphasis strength/demphasis strength) 000 0mV 0mV 0mV 001 11.25mV 11.25mV -11.25mV/11.25mV 010 16.9mV 16.9mV -16.9mV/16.9mV 011 (default) 28.15mV 28.15mV -28.15mV/ 28.15mV 100 28.15mV 28.15mV -28.15mV/28.15mV 101 39.35mV 39.35mV -39.35mV/39.35mV 110 45mV 45mV -45mV/45mV 111 56.3mV 56.3mV -56.3mV/56.3mV **Power Well:** SUS
7:4	0x0 RW	**PORTRESERVED_0123 (PORTRESERVED):** PORTRESERVED (PORTRESERVED): Reserved pin for future functionality of the respective ports **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**CL TX EMI Reduction Circuit Bypass (CLTXEMIREDCCTBYPASS):** Chicken bit for CL TX EMI reduction circuit bypass. Assert 1 to bypass the EMI reduction circuit. Default is 0b. AFE pin remains as PORTRESERVED for this project. **Power Well:** SUS
2	0x0 RW	**PERPORT ALLPORTZ (PERPORTALLPORTZ):** Legacy pin. No longer carries any functionality as the pull-down enable is now controlled by ilane5:0usbpdnen_h **Power Well:** SUS
1	0x0 RW	**PERPORT PPDPDMBSEL (PERPORTPPDPDMBSEL):** Config bit to select comparator 2:1 mux input either dp or dm for HS TX per port current calibration 1 - select dp (for debug purpose only) 0 - select dm (without 1.5K pullup) **Power Well:** SUS
0	0x1 RW	**PERPORT TX EOS protection enable (PERPORTTXEOS):** Set to 1b enables the TX EOS protection. To protect high speed driver passgate. This feature is not required for P1269.8. **Power Well:** SUS

7.14.4 USB2 PER PORT (USB2_PER_PORT_PP3)—Offset 4400h

Access Method

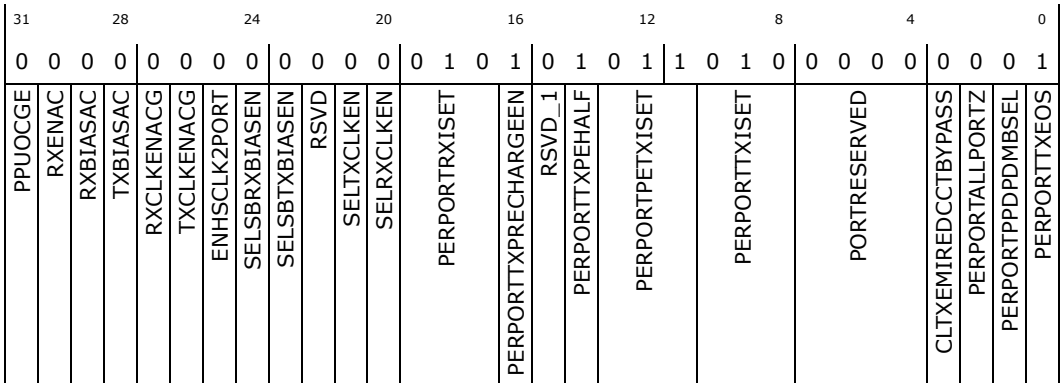
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4400h

Op Codes:

h - Read, h - Write

Default: 00055A01h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Per-Port UTMI_CLK Output Clock Gating Enable (PPUOCGE):** 1: Dynamic Clock Gating is enabled based on L1/L2 suspend indicator. This is the recommended setting for SYNOPSYS based controllers. 0: Output UTMI_CLK is running unless USB PLL is shutdown. This is the recommended setting for FRESCO based controllers. **Power Well:** SUS
30	0x0 RW	**RX EN AFE Control (RXENAC):** 1: Enables the dynamic RX EN behavior. This allows compensation code updates at various boundaries. 0: Disables the dynamic RX EN behavior (function of TXVALID only). RXENAC, RXBIASAC: 00: Legacy mode 01: Illegal 10: Allows additional code update window 11: Allows additional code update window with power saving **Power Well:** SUS
29	0x0 RW	**RX BIAS AFE Control (RXBIASAC):** 1: Enables the AFE bias control 0: Disables the AFE bias control This bit is only valid when internal RXBIAS policy is selected (SELSBRXBIASEN = 0b). **Power Well:** SUS
28	0x0 RW	**TX BIAS AFE Control (TXBIASAC):** 1: Enables the AFE bias control 0: Disables the AFE bias control This bit is only valid when internal TXBIAS policy is selected (SELSBTXBIASEN = 0b). **Power Well:** SUS
27	0x0 RW	**RX CLKEN AFE Clock Gating (RXCLKENACG):** 1: Enables the AFE clock gating 0: Disables the AFE clock gating This bit is only valid when internal RXCLKEN policy is selected (SELRXCLKEN = 0b). **Power Well:** SUS
26	0x0 RW	**TX CLKEN AFE Clock Gating (TXCLKENACG):** 1: Enables the AFE clock gating 0: Disables the AFE clock gating This bit is only valid when internal TXCLKEN policy is selected (SELTXCLKEN = 0b). **Power Well:** SUS
25	0x0 RW	**ENHSCLK2PORT:** This per-port pin will generate HS clock data pattern for testing purposes for that port and ignore the core data during Tx: 1: The port will transmit 10101..clock data pattern when txen=1. 0: The port will resume to c73usb250_normal operation where data is generated by the controller. **Power Well:** SUS
24	0x0 RW	**SELSBRXBIASEN:** This is to select between the UTMI internal vs. side-band control over the AFE RX bias enable signal. 1 - select side-band control from Intel SIP controller. 0 - select UTMI internally generated control. This is to be used with third party or external controller IP. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
23	0x0 RW	**SELSBTXBIASEN:** This is to select between the UTMI internal vs. side-band control over the AFE TX bias enable signal. 1 - select side-band control from Intel SIP controller. 0 - select UTMI internally generated control. This is to be used with third party or external controller IP. **Power Well:** SUS
22	0x0 WO	**RSVD:** RSVD (RSVD): FORCEPPICOMP (FORCEPPICOMP): Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Testmode When set to 1b, this will force per-port icomp offset cancellation Finite State Machine to start calibrating. BIOS has to wait for sufficient time for the calibration complete. This is a pulse trigger event. **Power Well:** SUS
21	0x0 RW	**SELTXCLKEN:** This is to select between internal mode vs. side-band control on the TX clock enable signal. 0 - override for TXCLKEN to be internally controlled. To be used with third party or external controller IP. 1 - select side-band control from Intel SIP controller. **Power Well:** SUS
20	0x0 RW	**SELRXCLKEN:** This is to select between internal mode vs. side-band control on the RX clock enable signal. 0 - override for RXCLKEN to be internally controlled. To be used with third party or external controller IP. 1 - select side-band control from Intel SIP controller. **Power Well:** SUS
19:17	0x2 RW	**PerPort HS Receiver Bias (PERPORTRXISET):** Config bit (per port) HS Receiver Bias current offset bit (2:0) 000 - 80uA 001 - 90uA 010 (default) - 100uA 011 - 110uA 100 - 120uA 101 - 130uA 110 - 140uA 111 - 150uA **Power Well:** SUS
16	0x1 RW	**PerPort Common Mode Pre-charge (PERPORTTXPRECHARGEEN):** Config bit (per port) To select whether to enable or disable the common mode pre-charge during SOP and EOP. Pre-charge hold for 4 cycles before first data transmission. This is to allow common choke ring back to settle down before driving first data bit to meet eye opening spec. 1 - pre-charge ON 0 - pre-charge OFF **Power Well:** SUS
15	0x0 RW	**RSVD (RSVD_1):** Reserved. **Power Well:** SUS
14	0x1 RW	**PerPort Half Bit Pre-emphasis (PERPORTTXPEHALF):** Config bit (per port) to select between half-bit or full-bit implementation 1 - select half-bit pre-emphasis 0 - select full-bit pre-emphasis. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
13:11	0x3 RW	**PerPort HS Pre-emphasis Bias (PERPORTPETXISET):** Config bit (per port) HS Pre-emphasis Bias current offset bit (2:0) Value Preempen: deempen = 01 (De-emphasis ON) Preempen: deempen = 10 (Pre-emphasis ON) Preempen: deempen = 11 (preemphasis strength/demphasis strength) 000 0mV 0mV 0mV 001 11.25mV 11.25mV 11.25mV/11.25mV 010 16.9mV 16.9mV 16.9mV/16.9mV 011 (default) 28.15mV 28.15mV 28.15mV/ 28.15mV 100 28.15mV 28.15mV 28.15mV/28.15mV 101 39.35mV 39.35mV 39.35mV/39.35mV 110 45mV 45mV 45mV/45mV 111 56.3mV 56.3mV 56.3mV/56.3mV. **Power Well:** SUS
10:8	0x2 RW	**PerPort HS Transmitter Bias (PERPORTTXISET):** Config bit (per port) HS Pre-emphasis Bias current offset bit2 (2:0) Value Preempen: deempen = 01 (De-emphasis ON) Preempen: deempen = 10 (Pre-emphasis ON) Preempen: deempen = 11 (preemphasis strength/demphasis strength) 000 0mV 0mV 0mV 001 11.25mV 11.25mV -11.25mV/11.25mV 010 16.9mV 16.9mV -16.9mV/16.9mV 011 (default) 28.15mV 28.15mV -28.15mV/ 28.15mV 100 28.15mV 28.15mV -28.15mV/28.15mV 101 39.35mV 39.35mV -39.35mV/39.35mV 110 45mV 45mV -45mV/45mV 111 56.3mV 56.3mV -56.3mV/56.3mV **Power Well:** SUS
7:4	0x0 RW	**PORTRESERVED_0123 (PORTRESERVED):** PORTRESERVED (PORTRESERVED): Reserved pin for future functionality of the respective ports **Power Well:** SUS
3	0x0 RW	**CL TX EMI Reduction Circuit Bypass (CLTXEMIREDCCTBYPASS):** Chicken bit for CL TX EMI reduction circuit bypass. Assert 1 to bypass the EMI reduction circuit. Default is 0b. AFE pin remains as PORTRESERVED for this project. **Power Well:** SUS
2	0x0 RW	**PERPORT ALLPORTZ (PERPORTALLPORTZ):** Legacy pin. No longer carries any functionality as the pull-down enable is now controlled by ilane5:0usbpdnen_h **Power Well:** SUS
1	0x0 RW	**PERPORT PPDPDMBSEL (PERPORTPPDPDMBSEL):** Config bit to select comparator 2:1 mux input either dp or dm for HS TX per port current calibration 1 - select dp (for debug purpose only) 0 - select dm (without 1.5K pullup) **Power Well:** SUS
0	0x1 RW	**PERPORT TX EOS protection enable (PERPORTTXEOS):** Set to 1b enables the TX EOS protection. To protect high speed driver passgate. This feature is not required for P1269.8. **Power Well:** SUS

7.14.5 USB2 PER PORT (USB2_PER_PORT_PP4)—Offset 4500h

Access Method

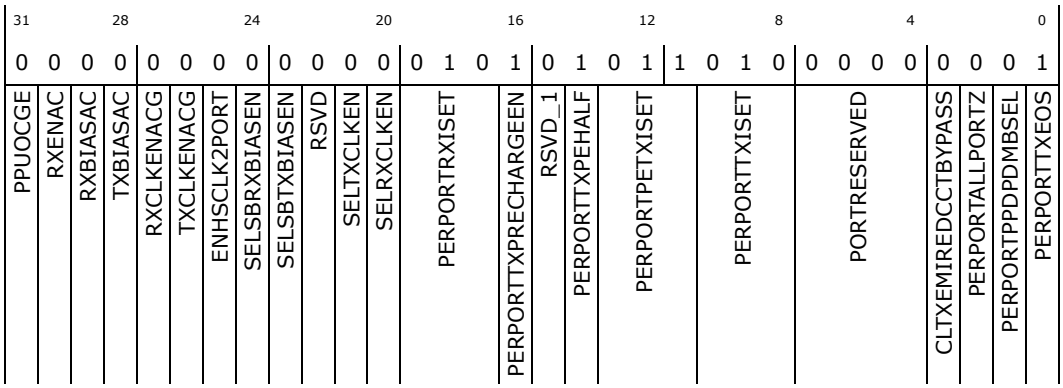
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4500h

Op Codes:

h - Read, h - Write

Default: 00055A01h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Per-Port UTMI_CLK Output Clock Gating Enable (PPUOCGE):** 1: Dynamic Clock Gating is enabled based on L1/L2 suspend indicator. This is the recommended setting for SYNOPSYS based controllers. 0: Output UTMI_CLK is running unless USB PLL is shutdown. This is the recommended setting for FRESCO based controllers. **Power Well:** SUS
30	0x0 RW	**RX EN AFE Control (RXENAC):** 1: Enables the dynamic RX EN behavior. This allows compensation code updates at various boundaries. 0: Disables the dynamic RX EN behavior (function of TXVALID only). RXENAC, RXBIASAC: 00: Legacy mode 01: Illegal 10: Allows additional code update window 11: Allows additional code update window with power saving **Power Well:** SUS
29	0x0 RW	**RX BIAS AFE Control (RXBIASAC):** 1: Enables the AFE bias control 0: Disables the AFE bias control This bit is only valid when internal RXBIAS policy is selected (SELSBRXBIASEN = 0b). **Power Well:** SUS
28	0x0 RW	**TX BIAS AFE Control (TXBIASAC):** 1: Enables the AFE bias control 0: Disables the AFE bias control This bit is only valid when internal TXBIAS policy is selected (SELSBTXBIASEN = 0b). **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
27	0x0 RW	**RX CLKEN AFE Clock Gating (RXCLKENACG):** 1: Enables the AFE clock gating 0: Disables the AFE clock gating This bit is only valid when internal RXCLKEN policy is selected (SELRXCLKEN = 0b). **Power Well:** SUS
26	0x0 RW	**TX CLKEN AFE Clock Gating (TXCLKENACG):** 1: Enables the AFE clock gating 0: Disables the AFE clock gating This bit is only valid when internal TXCLKEN policy is selected (SELTXCLKEN = 0b). **Power Well:** SUS
25	0x0 RW	**ENHSCLK2PORT:** This per-port pin will generate HS clock data pattern for testing purposes for that port and ignore the core data during Tx: 1: The port will transmit 10101..clock data pattern when txen=1. 0: The port will resume to c73usb250_normal operation where data is generated by the controller. **Power Well:** SUS
24	0x0 RW	**SELSBRXBIASEN:** This is to select between the UTMI internal vs. side-band control over the AFE RX bias enable signal. 1 - select side-band control from Intel SIP controller. 0 - select UTMI internally generated control. This is to be used with third party or external controller IP. **Power Well:** SUS
23	0x0 RW	**SELSBTXBIASEN:** This is to select between the UTMI internal vs. side-band control over the AFE TX bias enable signal. 1 - select side-band control from Intel SIP controller. 0 - select UTMI internally generated control. This is to be used with third party or external controller IP. **Power Well:** SUS
22	0x0 WO	**RSVD:** RSVD (RSVD): FORCEPPICOMP (FORCEPPICOMP): Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Testmode When set to 1b, this will force per-port icomp offset cancellation Finite State Machine to start calibrating. BIOS has to wait for sufficient time for the calibration complete. This is a pulse trigger event. **Power Well:** SUS
21	0x0 RW	**SELTXCLKEN:** This is to select between internal mode vs. side-band control on the TX clock enable signal. 0 - override for TXCLKEN to be internally controlled. To be used with third party or external controller IP. 1 - select side-band control from Intel SIP controller. **Power Well:** SUS
20	0x0 RW	**SELRXCLKEN:** This is to select between internal mode vs. side-band control on the RX clock enable signal. 0 - override for RXCLKEN to be internally controlled. To be used with third party or external controller IP. 1 - select side-band control from Intel SIP controller. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
19:17	0x2 RW	**PerPort HS Receiver Bias (PERPORTRXISET):** Config bit (per port) HS Receiver Bias current offset bit (2:0) 000 - 80uA 001 - 90uA 010 (default) - 100uA 011 - 110uA 100 - 120uA 101 - 130uA 110 - 140uA 111 - 150uA **Power Well:** SUS
16	0x1 RW	**PerPort Common Mode Pre-charge (PERPORTTXPRECHARGEEN):** Config bit (per port) To select whether to enable or disable the common mode pre-charge during SOP and EOP. Pre-charge hold for 4 cycles before first data transmission. This is to allow common choke ring back to settle down before driving first data bit to meet eye opening spec. 1 - pre-charge ON 0 - pre-charge OFF **Power Well:** SUS
15	0x0 RW	**RSVD (RSVD_1):** Reserved. **Power Well:** SUS
14	0x1 RW	**PerPort Half Bit Pre-emphasis (PERPORTTXPEHALF):** Config bit (per port) to select between half-bit or full-bit implementation 1 - select half-bit pre-emphasis 0 - select full-bit pre-emphasis . **Power Well:** SUS
13:11	0x3 RW	**PerPort HS Pre-emphasis Bias (PERPORTPETXISET):** Config bit (per port) HS Pre-emphasis Bias current offset bit (2:0) Value Preempen: deempen = 01 (De-emphasis ON) Preempen: deempen = 10 (Pre-emphasis ON) Preempen: deempen = 11 (preemphasis strength/demphasis strength) 000 0mV 0mV 0mV 001 11.25mV 11.25mV 11.25mV/11.25mV 010 16.9mV 16.9mV 16.9mV/16.9mV 011 (default) 28.15mV 28.15mV 28.15mV/ 28.15mV 100 28.15mV 28.15mV 28.15mV/28.15mV 101 39.35mV 39.35mV 39.35mV/39.35mV 110 45mV 45mV 45mV/45mV 111 56.3mV 56.3mV 56.3mV/56.3mV . **Power Well:** SUS
10:8	0x2 RW	**PerPort HS Transmitter Bias (PERPORTTXISET):** Config bit (per port) HS Pre-emphasis Bias current offset bit2 (2:0) Value Preempen: deempen = 01 (De-emphasis ON) Preempen: deempen = 10 (Pre-emphasis ON) Preempen: deempen = 11 (preemphasis strength/demphasis strength) 000 0mV 0mV 0mV 001 11.25mV 11.25mV -11.25mV/11.25mV 010 16.9mV 16.9mV -16.9mV/16.9mV 011 (default) 28.15mV 28.15mV -28.15mV/ 28.15mV 100 28.15mV 28.15mV -28.15mV/28.15mV 101 39.35mV 39.35mV -39.35mV/39.35mV 110 45mV 45mV -45mV/45mV 111 56.3mV 56.3mV -56.3mV/56.3mV **Power Well:** SUS
7:4	0x0 RW	**PORTRESERVED_0123 (PORTRESERVED):** PORTRESERVED (PORTRESERVED): Reserved pin for future functionality of the respective ports **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**CL TX EMI Reduction Circuit Bypass (CLTXEMIREDCCTBYPASS):** Chicken bit for CL TX EMI reduction circuit bypass. Assert 1 to bypass the EMI reduction circuit. Default is 0b. AFE pin remains as PORTRESERVED for this project. **Power Well:** SUS
2	0x0 RW	**PERPORT ALLPORTZ (PERPORTALLPORTZ):** Legacy pin. No longer carries any functionality as the pull-down enable is now controlled by ilane5:0usbpdnen_h **Power Well:** SUS
1	0x0 RW	**PERPORT PPDPDMBSEL (PERPORTPPDPDMBSEL):** Config bit to select comparator 2:1 mux input either dp or dm for HS TX per port current calibration 1 - select dp (for debug purpose only) 0 - select dm (without 1.5K pullup) **Power Well:** SUS
0	0x1 RW	**PERPORT TX EOS protection enable (PERPORTTXEOS):** Set to 1b enables the TX EOS protection. To protect high speed driver passgate. This feature is not required for P1269.8. **Power Well:** SUS

7.14.6 USB2 GLOBAL PORT (USB2_GLOBAL_PORT)—Offset 4001h

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4001h

Op Codes:

h - Read, h - Write

Default: 0C3D8006h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0	0	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
RSVD				DMRXENTOT				HSICCG	UPLLS	HDISCPOL	USBPLLSHYS			BYPRXPSYNC	BYPTXPSYNC	HMRXENTOT				DISCUPLLSHUTEN	L2UPLLSHUTEN	L1UPLLSHUTEN	RSMRST18ENB	CFGDISCROWBARCTL	DRCCLKSTRBGBYPASS	EXTCLKREQEN	SSIDECLKLGE	SSOSCCLKLGE	EOSPROTECTBYPASS	RXDISCSAMPLEBYPASS	TXPEDYNEN	TXDISCPEHALFOFF	LOWPWREN	CLKG

Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS
28:26	0x3 RW	**Device Mode RX EN Turn On Time (DMRXENTOT):** The RX EN turn on time here is wrt to the staggered driven deassertion when operating in Device mode. 000: 8 HS bit time 001: 12 HS bit time 010: 16 HS bit time 011: 20 HS bit time 100: 24 HS bit time 101: 28 HS bit time 110: 32 HS bit time 111: 36 HS bit time This field is only valid when the corresponding per-port field RXENAC is 1b. **Power Well:** SUS
25	0x0 RW	**HSIC Clk480 Gate Enable (HSICCG):** 1: Enables the output HSIC clk480 to be dynamically gated based on L1/L2 HSIC suspend indicators. 0: Disables output HSIC clk480 gating (always ON). **Power Well:** SUS
24	0x0 WO	**USB PLL Startup (UPLLS):** The USB PLL will come out of reset disabled. When set to 1b, it allows the USB PLL to start locking. Writes of 0b has no effect. Reads always return a 0b. **Power Well:** SUS
23	0x0 RW	**Host Disconnect Policy (HDISCPOL):** 1: HS and FS/LS disconnect detect. 0: HS disconnect detect only. **Power Well:** SUS
22:20	0x3 RW	**USB PLL Shutdown Hysteresis (USBPLLSHYS):** Timer to expire before shutting the the USB PLL: 000: 1 s 001: 2 s 010: 4 s 011: 8 s 100: 16 s 101: 32 s 110: 64 s 111: 128 s This field is only valid when EXTCLKREQEN = 0b (internal CLKREQ). **Power Well:** SUS
19	0x1 RW	**Bypass RX Path Synchronizers (BYPRXPSYNC):** 1: Bypasses the 2 stage syncs, and results in faster UNSQ to RXVALID assertion. 0: Allows the 2 stage syncs. **Power Well:** SUS
18	0x1 RW	**Bypass TX Path Synchronizers (BYPTXPSYNC):** 1: Bypasses the 2 stage syncs, and results in faster TXVALID to DRIVEEN assertion. 0: Allows the 2 stage syncs. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
17:15	0x3 RW	**Host Mode RX EN Turn On Time (HMRXENTOT):** The RX EN turn on time here is wrt to the staggered driveen deassertion when operating in Host mode. 000: 8 HS bit time 001: 12 HS bit time 010: 16 HS bit time 011: 20 HS bit time 100: 24 HS bit time 101: 28 HS bit time 110: 32 HS bit time 111: 36 HS bit time This field is only valid when the corresponding per-port field RXENAC is 1b. **Power Well:** SUS
14	0x0 RW	**Disconnect USB PLL Shutdown Enable (DISCUPLLSHUTEN):** 1: Enables USB PLL shutdown on disconnected ports (SE0 detection) 0: Disables USB PLL shutdown on disconnected ports. It is recommended to enable this functionality only on Host only operation (not OTG or Device). This bit is only applicable if EXTCLKREQEN = 0b. This functionality is disabled by default to allow EXTCLKREQEN to be programmed prior to USB PLL shutdown. **Power Well:** SUS
13	0x0 RW	**L2 USB PLL Shutdown Enable (L2UPLLSHUTEN):** 1: Enables USB PLL shutdown during port L2. 0: Disables USB PLL shutdown during port L2. This bit is only applicable if EXTCLKREQEN = 0b. This functionality is disabled by default to allow EXTCLKREQEN to be programmed prior to USB PLL shutdown. **Power Well:** SUS
12	0x0 RW	**L1 USB PLL Shutdown Enable (L1UPLLSHUTEN):** 1: Enables USB PLL shutdown during port L1. 0: Disables USB PLL shutdown during port L1. This bit is only applicable if EXTCLKREQEN = 0b. This functionality is disabled by default to allow EXTCLKREQEN to be programmed prior to USB PLL shutdown. **Power Well:** SUS
11	0x0 RW	**RSMRST18ENB:** - when this pin = 0 power seq is enabled, when 1, rsmrst18 is overridden when all power are up - rsmrst18 is an internally generated signal that goes high during power sequence (ie some or all of the powers are down) - when power up sequence is completed the internal block will assert this rsmrst18 signal to low **Power Well:** SUS
10	0x0 RW	**CFGDISCROWBARCTL:** HIGH to disable crowbar current in driver during Classic Tx **Power Well:** SUS
9	0x0 RW	**DRCCLKSTRBGBYPASS:** Config bit to bypass dynamic clock gating (drcclkstrbsyngb) on drcclk480strb to the SHIP. Set to 1b to bypass the clock gating. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**External USB PLL CLKREQ/ACK Enable (EXTCLKREQEN):** 1: USB PLL shutdown depends on external CLKREQ/ACK. 0: USB PLL shutdown depends on internal CLKREQ/ACK. **Power Well:** SUS
7	0x0 RW	**SHIP side_clk Local Gating Enable (SSIDECLKLGE):** 1: Enables clock gating 0: Disables clock gating **Power Well:** SUS
6	0x0 RW	**SHIP sosc_clk Local Gating Enable (SSOSCCLKLGE):** 1: Enables clock gating 0: Disables clock gating **Power Well:** SUS
5	0x0 RW	**EOSPROTECTBYPASS:** Assert to 1b to disable the EOS protection circuit on the RX HS input passgate. This bit is not applicable to P1269.8. **Power Well:** SUS
4	0x0 RW	**RXDISCSAMPLEBYPASS:** Assert to 1b to override the txdiscsample signal to HS RX disconnect detector for test mode so that HS RX disconnect detector can be tested. **Power Well:** SUS
3	0x0 RW	**Dynamic Pre-emphasis Control Feature (TXPEDYNEN):** Config bit (global to all ports) 1: Assert to 1b to enable the dynamic pre-emphasis jamming control during SOF EOP. Enables dynamic control of txdiscsample from the SIP side, which gives better differential voltage during SOF EOP when asserted during this time, for a more reliable disconnect detection. 0: It is will gate pre-emphasis jamming control iusbtxdiscsample_h signal when set to 0b. This only impacts the TX and not the RX. **Power Well:** SUS
2	0x1 RW	**TXDISCPEHALFOFF:** Config bit (global to all ports) to select the jamming magnitude when TXPEDYNEN is enabled. The jamming magnitude option as below: 1 -- select half pre-emphasis strength 0 - select full pre-emphasis strength **Power Well:** SUS
1	0x1 RW	**Low Power Mode (LOWPWREN):** Assert to 1b to enable the low power mode TX EOS biasing circuit. De-assert to 0b to disable the low power mode as a chicken bit. This bit is not applicable for P1269.8 process which uses 3.3V TG devices but applicable for P1271 process which uses 1.8V TG devices. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**Clock Gating Feature (CLKG):** Clock gating configuration bit (global to all ports). Controls the usbclkgenb signal. 1 - disable clock gating feature 0 - enable clock gating feature **Power Well:** SUS

7.14.7 USB2 PLL1 (USB2_PLL1)—Offset 7F02h

Access Method

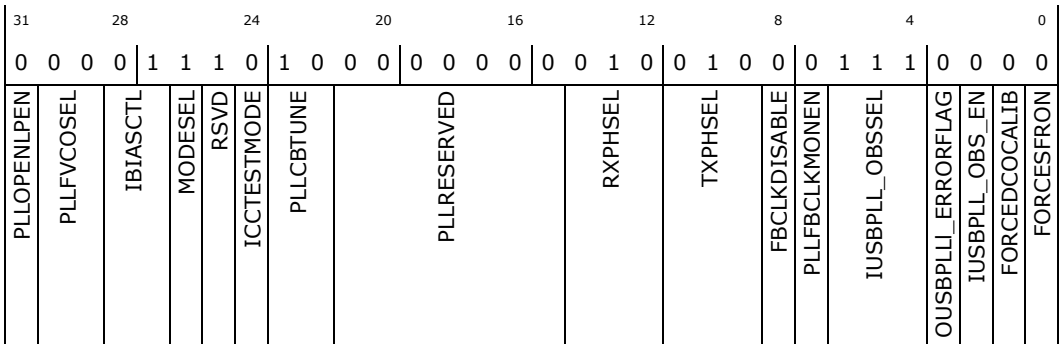
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 7F02h

Op Codes:

h - Read, h - Write

Default: 0E802470h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**PLLOPENLPEN:** Feed directly to SHIP or AFE : AFE Functional or Test Mode : Functional/Test Mode Set to 1b to enter PLL open loop mode. VCO frequency is determined by ipllvrefsel(3:0) bits. Default: 1 b0 **Power Well:** SUS
30:29	0x0 RW	**PLLFVCOSEL:** PLL VCO frequency select bus. These bits should be set by the CORE based on the vco target frequency. That will help optimize PLL performance (Rj and Lock time). Note that this takes effect only when ipllconfig(1:0)=00 ipllfvcosel(1:0) LBW frequency HBW frequency 11 3.3 - 3.6GHz) 3.5GHz 10 2.75 - 3.3GHz 3.0 - 3.5GHz 01 2.3 - 2.75GHz 2.5 - 3.0GHz 00- Default 1.8 - 2.3GHz andlt; 2.5GHz Default: 2 b00 (for 1.92GHz) If only a single VCO frequency is used then set the default according to the table above or even hard tie it (no registers are required) **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
28:27	0x1 RW	**IBIASCTL:** Bias control for the Input Buffer. High Rbias is for lower current. Low Rbias is for better jitter performance (higher current). ibiascntl(1) 0 0 1 1 ibiascntl(0) 0 1 0 1 Rbias 10k 5k 6k 3.75k Default: 2b01 (5k) **Power Well:** SUS
26	0x1 RW	**MODESEL:** Changes the common mode of the reference clock to the input buffer Default for dot0 = 0, for dot1/2 = 1 This will make iusbibiascntl(1:0) default optimum for dot process. (5k for dot0 and 10k for dot1/2) **Power Well:** SUS
25	0x1 RW	**RSVD:** RSVD **Power Well:** SUS
24	0x0 RW	**ICCTESTMODE:** Input from Sus. During icctestmode, diff amp will be disabled. Output irusbclkout will be pulled up to high **Power Well:** SUS
23:22	0x2 RW	**PLLCBTUNE:** This bus is ignored by default. In order to use it, set iusbpllconfig(0) to 1 or iusbpllopenlpen to 1 When ipllconfig(0)= 0 the PLL automatically chooses the best cbtune for best Rj performance and ignores this bus This bus controls the amount of capacitance that loads the VCO. As VCO loaded with more capacitance: 1. Current increases 2. Jitter improves 00 - least capacitance 11 - max capacitance For better performance use these values based on freq range: Default: 2 b11 (for 1.92GHz) ipllcbtune(1:0) LBW frequency HBW frequency 00- Default) 3.1GHz) 3.5GHz 01 2.6 - 3.1GHz 3.0 - 3.5GHz 10 2.2 - 2.6GHz 2.5 - 3.0GHz 11 andlt; 2.2GHz andlt; 2.5GHz **Power Well:** SUS
21:15	0x0 RW	**PLLRESERVED:** Reserved pins for future use **Power Well:** SUS
14:12	0x2 RW	**RXPHSEL:** This bit only selects which HSIO clock phase to send to core. Receiver phase select bits Default is to select ph(2) from 8-phase (ph7:0) clocks. **Power Well:** SUS
11:9	0x2 RW	**TXPHSEL:** Transmit phase select bits. This bit selects which phase to be sent to port TX. Default is to select ph(2) from 8-phase (ph7:0) clocks **Power Well:** SUS
8	0x0 RW	**FBCLKDISABLE:** PLL Feedback Clock Disable - Disable the feedback clock in the PLL FUB, this is intended to simulate and validate the YANK detect circuitry in the PLL analog core: 1 - PLL feedback path disabled 0 - PLL feedback path enabled **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW	**PLLFBCLKMONEN:** To enable PLL feedback monitoring mode during PLL BI 1 - enable monitor mode 0 - disable monitor mode VISA needs to be configured to monitor this feedback clock. **Power Well:** SUS
6:4	0x7 RW	**ADPLL OBS SELECT (IUSBPLL_OBSSEL):** This signal is used to select ADPLL signal for monitoring at local port (used together with iusbpll_obs_en): 000 - o_obs(0) 001 - o_obs(1) 010 - o_obs(2) 011 - o_obs(3) 100 - refclkview 101 - fbclkview others - vss Default = 111 **Power Well:** SUS
3	0x0 RO	**ADPLL ERROR FLAG (OUSBPLLl_ERRORFLAG):** ADPLL ERROR FLAG: indicator for a violation in PLL (overflow issues, PLL lost lock, etc). Routed also to VISA. Details of the violation could be found in VISA outputs **Power Well:** SUS
2	0x0 RW	**ADPLL OBS (IUSBPLL_OBS_EN):** ADPLL: This signal is used to select between pllbypassclk or ADPLL monitor signal to be sent through clock repeater to local port for observation. It needs to be used together with iusbpllbypass (set to 1). 0 - Select pllbypassclk 1 - Select ADPLL signals for monitoring through local port Default = 0 **Power Well:** SUS
1	0x0 RW	**FORCEDCOCALIB:** To force dco calibration in c73usb250_normal locking. Required if user wishes to change DCO frequency 1 - force DCO calibration. 0 - c73usb250_normal operation. No DCO frequency change. **Power Well:** SUS
0	0x0 RW	**FORCESFRON:** To forces SFR on when DCO is disabled for faster lock time. Sampled by refclk only while pllen=0. This is not used for USB2 PHY. 1 - force SFR ON. 0 - force SFR OFF. **Power Well:** SUS

7.14.8 USB2 PLL2 (USB2_PLL2)—Offset 7F03h

Access Method

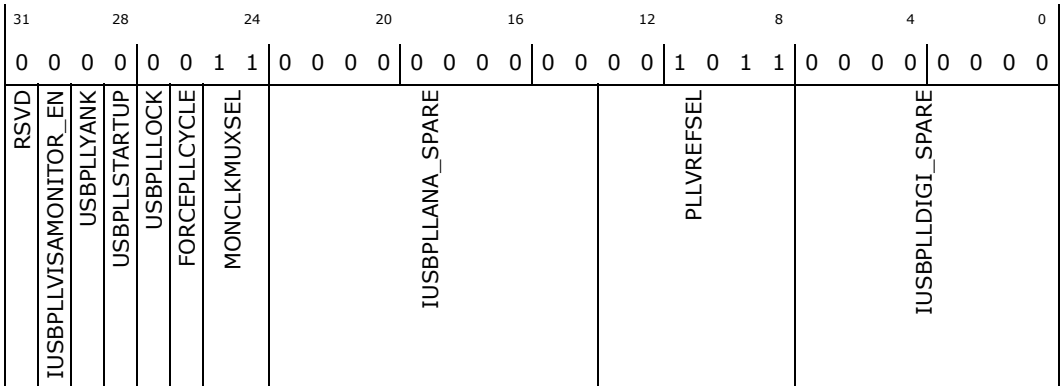
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 7F03h

Op Codes:

h - Read, h - Write

Default: 03000B00h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS
30	0x0 RW	**PLL VISA MONITOR (IUSBPLLVISAMONITOR_EN):** 0 - Gate visa monitor clocks to save power during functional mode (default). 1 - Ungate visa monitor clocks during debug. **Power Well:** SUS
29	0x0 RO	**USBPLLYANK:** Output to Core. Indicates the PLL feedback loop has been open for some time while the analog core is enabled. When asserted high, V1 is forced to a voltage that brings the VCO frequency well within the c73usb250_normal operating range of the feedback path logic 1 - YANK condition detected 0 - c73usb250_normal operation ** This signal goes HIGH if VCO output goes idle due to bad startup **Power Well:** SUS
28	0x0 RO	**USBPLLSTARTUP:** Output to Core. Startup Pulse - indicates the analog core has recently been enabled, LOCK acquisition begins on the falling edge of this output 1 - STARTUP condition detected 0 - PLL lock acquisition in progress, the PLL is locked or the analog core is disabled ** This signal goes HIGH during PLL startup phase **Power Well:** SUS
27	0x0 RO	**USBPLLLOCK:** Output to Core. Lock Indicator 1 - PLL is LOCKED (as indicated by the Lock Detect timer expiring) 0 - PLL is Not Locked NOTE: Time or Application Critical operations should not depend on the accuracy or validity of this output **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
26	0x0 RW/1S	**FORCEPLLCYCLE:** Force PLL Cycle: When set, the PLL SM will sequence a shutdown of PLL, followed by startup. Bit is cleared by HW once the PLL cycle has completed. A write of 0 has no impact. This flow is similar to the dynamic PLL shutdown flow, where the core reset is not asserted, but the PLL related clocks are gated/enabled cleanly. It is expected that SW will set this bit only when the EHCI RUN bit is cleared (HALTED set). This bit will take effect regardless of the Disable Dynamic PLL **Power Well:** SUS
25:24	0x3 RW	**MONCLKMUXSEL:** Bits for selecting clock to monitor through VISA: 00 - reference clock 01 - coreclk480 10 - adpll fbclkview 11 - vss (default) **Power Well:** SUS
23:14	0x0 RW	**ADPLL ANA SPARE (IUSBPLLANA_SPARE):** Spare input config pins. **Power Well:** SUS
13:8	0xb RW	**PLLVREFSEL:** This bus is ignored by default. In order to use it, set iusbpllconfig(1) to 1 or iusbpllopenlpen to 1 On functional mode these bits control PLL startup voltage reference. When iusbpllconfig(1)= 0 the PLL automatically chooses the best vrefsel for fastest lock time and ignores this bus In open loop mode (iusbpllopenlpen=1) these bits control the VCO frequency Default (dot0 LBW/HBW): 6 b001011 **Power Well:** SUS
7:0	0x0 RW	**ADPLL DIGI SPARE (IUSBPLLDIGI_SPARE):** Spare input config pins. **Power Well:** SUS

7.14.9 USB2 COMPBG (USB2_COMPBG)—Offset 7F04h

Access Method

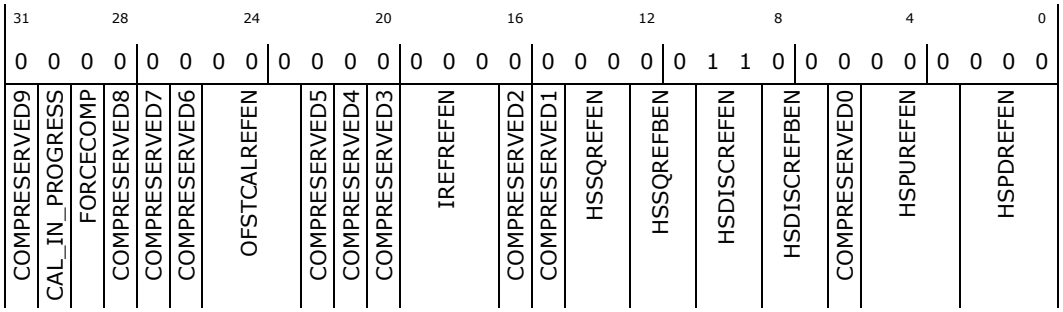
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 7F04h

Op Codes:

h - Read, h - Write

Default: 00000600h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**COMPRESERVED9:** Spare bits related to compensation. **Power Well:** SUS
30	0x0 RO	**CAL IN PROGRESS (CAL_IN_PROGRESS):** This bit is to indicate that Compensation State Machine is still in progress and rcomp/icomp value are not yet updated **Power Well:** SUS
29	0x0 WO	**FORCECOMP:** When set to 1b, this will force global comp Finite State Machine to start calibrating. BIOS has to wait for sufficient time for the calibration complete. This is a pulse trigger event. **Power Well:** SUS
28	0x0 RW	**COMPRESERVED8:** Spare bits related to compensation. **Power Well:** SUS
27	0x0 RW	**COMPRESERVED7:** Spare bits related to compensation. **Power Well:** SUS
26	0x0 RW	**COMPRESERVED6:** Spare bits related to compensation. **Power Well:** SUS
25:23	0x0 RW	**OFSTCALREFEN:** Comparator Offset CAL reference voltage (500mV) select signal to select reference voltage to AFE global COMP. ofstrefen2 ofstrefen1 ofstrefen0 0 0 0 500mV 0 0 1 300mV 0 1 0 350mV 0 1 1 400mV 1 0 0 450mV 1 0 1 550mV 1 1 0 600mV 1 1 1 650mV **Power Well:** SUS
22	0x0 RW	**COMPRESERVED5:** Spare bits related to compensation. **Power Well:** SUS
21	0x0 RW	**COMPRESERVED4:** Spare bits related to compensation. **Power Well:** SUS
20	0x0 RW	**COMPRESERVED3:** Spare bits related to compensation. **Power Well:** SUS
19:17	0x0 RW	**IREFREFEN:** IREF reference voltage (300mV) select signal to select reference voltage to AFE global icomp. irefrefen2 irefrefen1 irefrefen0 1 1 1 350mV 1 1 0 337.5mV 1 0 1 325mV 1 0 0 312.5mV 0 1 1 287.5mV 0 1 0 275mV 0 0 1 262.5mV 0 0 0 300mV **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW	**COMPRESERVED2:** Spare bits related to compensation. **Power Well:** SUS
15	0x0 RW	**COMPRESERVED1:** Spare bits related to compensation. **Power Well:** SUS
14:13	0x0 RW	**HSSQREFEN (HSSQREFEN):** **Feed directly to SHIP or AFE:AFE** **Functional or Test Mode: Functional** HS SQ reference voltage (312.5mV) select signal to select reference voltage to AFE hssqrefen1 hssqrefen0 Vref 1 1 select 350mV 1 0 select 325mV 0 1 select 300mV 0 0 select 312.5mV **Power Well:** SUS
12:11	0x0 RW	**HSSQREFBEN:** HS SQ reference voltage (100mV) enable signal to select reference voltage to AFE hssqrefben1 hssqrefben0 1 1 select 150mV 1 0 select 125mV 0 1 select 75mV 0 0 select 100mV **Power Well:** SUS
10:9	0x3 RW	**HSDISCREFEN:** HS DISC BG reference voltage (575mV) select signal to select reference voltage to AFE port. This register is combined together with HSSQREFBEN register to produce the following truth table. discrefen1 discrefen0 discrefben1 discrefben0 x 1 1 1 select 575mV (default) x 1 1 0 select 650mV x 1 0 1 select 550mV x 1 0 0 select 537.5mV x 0 1 1 select 625mV (default) x 0 1 0 select 700mV x 0 0 1 select 600mV x 0 0 0 select 675mV **Power Well:** SUS
8:7	0x0 RW	**HSDISCREFBEN:** HS DISC reference voltage enable signal to select reference voltage to AFE. It s combined with iusbhsdiscrefen(1:0) for reference voltage selection. **Power Well:** SUS
6	0x0 RW	**COMPRESERVED0:** Spare bits related to compensation. **Power Well:** SUS
5:3	0x0 RW	**HSPUREFEN:** HS Pull-up Rcal reference voltage (500mV) select signal to select reference voltage to AFE global comp. hspurefen2 hspurefen1 hspurefen0 1 1 1 537.5mV 1 1 0 525mV 1 0 1 512.5mV 1 0 0 487.5mV 0 1 1 475mV 0 1 0 450mV 0 0 1 425mV 0 0 0 500mV **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
2:0	0x0 RW	**HSPDREFEN:** HS Pull-Down RCAL reference voltage (500mV) select signal to select reference voltage to AFE global comp. hspdrefen2 hspdrefen1 hspdrefen0 1 1 1 537.5mV 1 1 0 525mV 1 0 1 512.5mV 1 0 0 487.5mV 0 1 1 475mV 0 1 0 450mV 0 0 1 425mV 0 0 0 500mV **Power Well:** SUS

7.14.10 UTMI RX REG1 PER PORT (UTMI_RX_REG1_PER_PORT_PP0)—Offset 4105h

Access Method

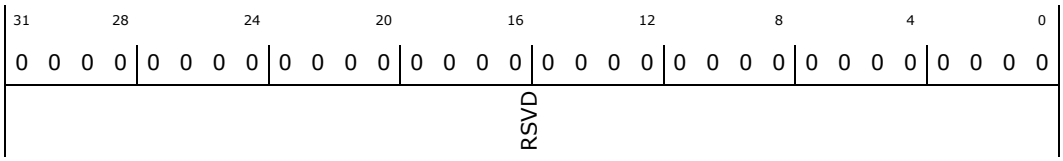
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4105h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS

7.14.11 UTMI RX REG2 PER PORT (UTMI_RX_REG2_PER_PORT_PP0)—Offset 4106h

Access Method

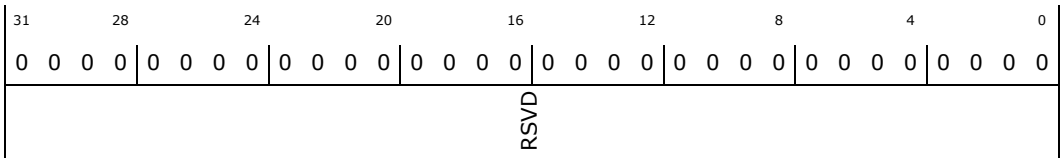
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4106h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD:** RSVD **Power Well:** SUS

7.14.12 UTMI TX REG PER PORT (UTMI_TX_REG_PER_PORT_PP0)—Offset 4107h

Access Method

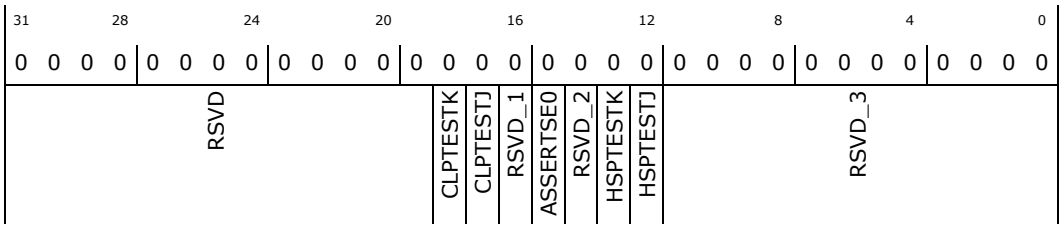
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4107h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS
18	0x0 WO	**CLPTESTK:** Classic force K **Power Well:** SUS
17	0x0 WO	**CLPTESTJ:** Classic force J **Power Well:** SUS
16	0x0 RO	**RSVD (RSVD_1):** Reserved. **Power Well:** SUS
15	0x0 WO	**ASSERTSE0:** Assert SE0 **Power Well:** SUS
14	0x0 RO	**RSVD (RSVD_2):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
13	0x0 WO	**HSPTESTK:** HS Test K mode **Power Well:** SUS
12	0x0 WO	**HSPTESTJ:** HS Test J mode **Power Well:** SUS
11:0	0x0 RO	**RSVD (RSVD_3):** Reserved. **Power Well:** SUS

7.14.13 UTMI MISC REG PER PORT (UTMI_MISC_REG_PER_PORT_PP0)—Offset 4108h

Access Method

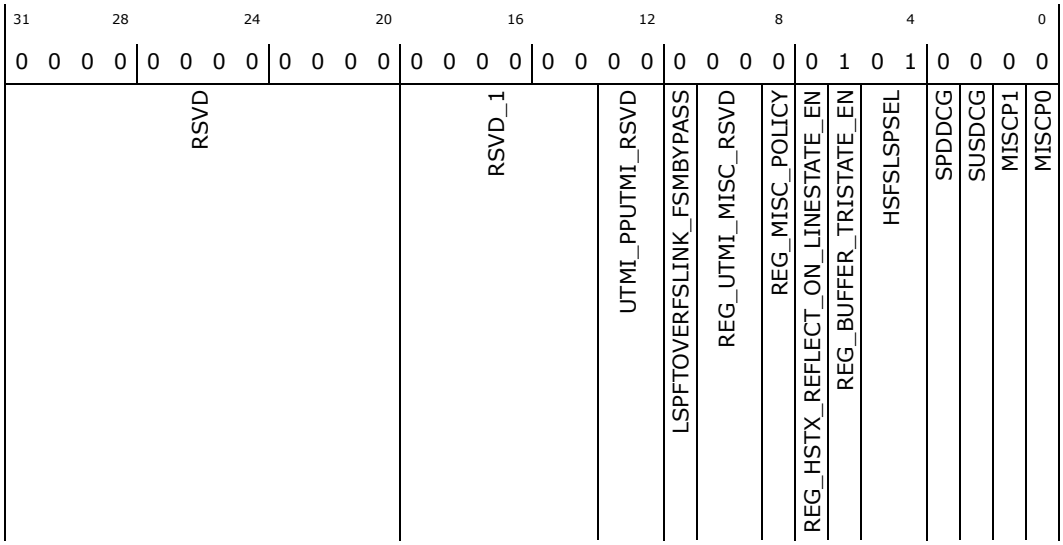
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4108h

Op Codes:

h - Read, h - Write

Default: 00000050h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RSVD:** RSVD **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
19:14	0x0 RW	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
13:12	0x0 RW	**UTMI PPUTMI BLOCK RESERVE (UTMI_PPUTMI_RSVD):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional Reserved pin going to uxfehpputmi fub Bit1: Opmode is delayed by 2 utmi clks while txvalid is direct from the utmi interface. Chicken to add 2 delays to txvalid. 1: Two additional delays txvalid in c73usb250_usbhsip_uxfehpputmi to resolve suspend resume treated as sync pattern. 0: keep as legacy. Bit0: Chicken bit for device remote wake (RTL as host), where glitch observe when host return K. 1: Enable OR-ing of linestate with pre-condition. Need to precon with K instead of J. 0: keep as legacy. **Power Well:** SUS
11	0x0 RW	**UTMI LSPKToverFSFSM Bypass (LSPFTOVERFSLINK_FSMBYPASS):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: Bypass c73usb250_usbhsip_uxfehpputmil3fsm to resolve HS suspend resume glitch on EOR. The FSM is adding delay to xcvrselect resulting delay of speed change during resume which cause HS EOR as FS EOR. **Power Well:** SUS
10:9	0x0 RW	**UTMI Misc reserve (REG_UTMI_MISC_RSVD):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional Reserved pin going to utmi_misc fub **Power Well:** SUS
8	0x0 RW	**UTMI Misc policy (REG_MISC_POLICY):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional LS Double K fix chicken bit policy. Set 1 to disable fix for double K seen on LS sync pattern. **Power Well:** SUS
7	0x0 RW	**High Speed Transmit Linestate reflect enable (REG_HSTX_REFLECT_ON_LINESTATE_EN):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To enable HS transmit reflect to linestate (Linestate to reflect J during transmit) 0: Disable HS transmit reflect. Linestate stay as SE0. **Power Well:** SUS
6	0x1 RW	**Tri Buffer enable (REG_BUFFER_TRISTATE_EN):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To enable tristating buffer with opmode=01. 0: Disable opmode=01 from buffer pull-up enable. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
5:4	0x1 RW	**HS/FS/LS Port Staggering Delay Select (HSFSLSPSEL):** This field selects the HS/FS/LS driveen staggering for this port: 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset **Power Well:** SUS
3	0x0 RW	**Speed Based Dynamic Clock Gating Enable (SPDDCG):** reg_utmi_spd_based_lcg_en (Disable bit for UTMI Local Clock Gating based on port speed: When clear, this allows the High Speed Link control's 480Mhz and its divided 48/60 MHz link clock trunk to be gated when idle conditions are met). 1: Enable Clock Gating 0: Disable Clock Gating **Power Well:** SUS
2	0x0 RW	**Suspend Based Dynamic Clock Gating (SUSDCG):** reg_utmi_susp_based_lcg_en (Disable bit for UTMI Local Clock Gating based on port suspend: When clear, this allows the High Speed Link control's 480Mhz and its divided 48/60 MHz link clock trunk to be gated when idle conditions are met.When set, UTMI local clock gating is bypassed). 1: Enable Clock Gating 0: Disable Clock Gating **Power Well:** SUS
1	0x0 RW	**Miscellaneous Policies 1 (MISCP1):** chicken bit to disable the PPT A1 Fix to deassert Rxactive early (this bit is introduced to disable the deassert rxactive early logic added in by PPT). 1: Disable fix 0: Enable fix **Power Well:** SUS
0	0x0 RW	**Miscellaneous Policies 0 (MISCP0):** chicken bit to disable the fix to reset the enclk counter upon txvalid (enclk counter is made to reset upon txvalid. This bit is to bypass this fix). 1: Disable fix 0: Enable fix **Power Well:** SUS

7.14.14 UTMI RX REG1 PER PORT (UTMI_RX_REG1_PER_PORT_PP1)—Offset 4205h

Access Method

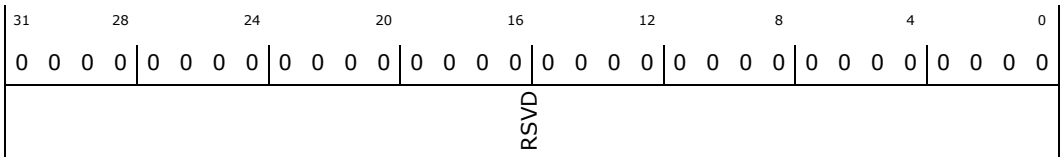
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4205h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS

7.14.15 UTMI RX REG2 PER PORT (UTMI_RX_REG2_PER_PORT_PP1)—Offset 4206h

Access Method

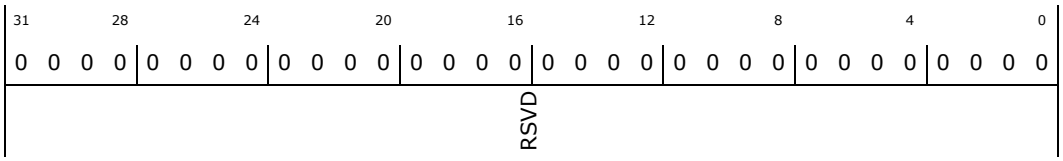
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4206h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD:** RSVD **Power Well:** SUS

7.14.16 UTMI TX REG PER PORT (UTMI_TX_REG_PER_PORT_PP1)—Offset 4207h

Access Method

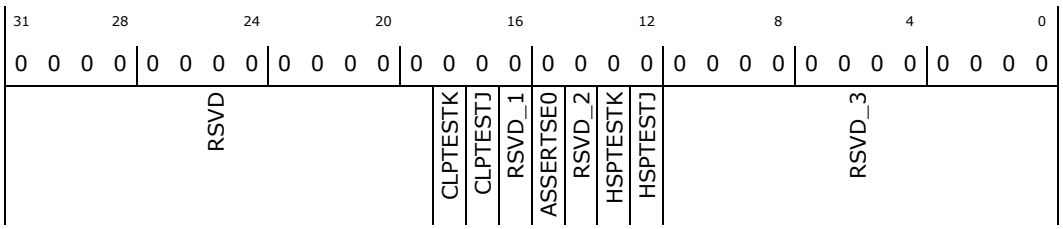
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4207h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS
18	0x0 WO	**CLPTESTK:** Classic force K **Power Well:** SUS
17	0x0 WO	**CLPTESTJ:** Classic force J **Power Well:** SUS
16	0x0 RO	**RSVD (RSVD_1):** Reserved. **Power Well:** SUS
15	0x0 WO	**ASSERTSE0:** Assert SE0 **Power Well:** SUS
14	0x0 RO	**RSVD (RSVD_2):** Reserved. **Power Well:** SUS
13	0x0 WO	**HSPTESTK:** HS Test K mode **Power Well:** SUS
12	0x0 WO	**HSPTESTJ:** HS Test J mode **Power Well:** SUS
11:0	0x0 RO	**RSVD (RSVD_3):** Reserved. **Power Well:** SUS

7.14.17 UTMI MISC REG PER PORT (UTMI_MISC_REG_PER_PORT_PP1)—Offset 4208h

Access Method

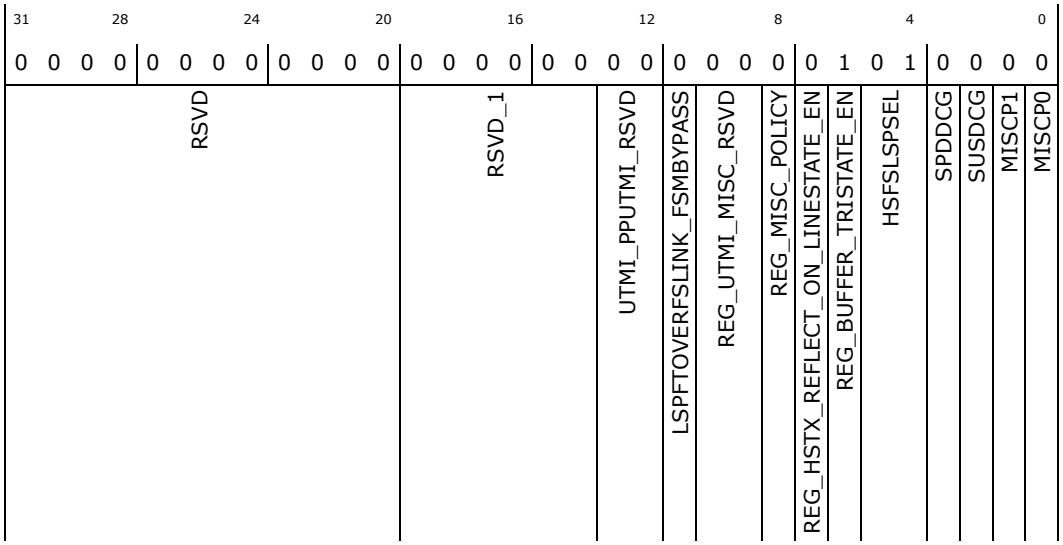
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4208h

Op Codes:

h - Read, h - Write

Default: 00000050h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RSVD:** RSVD **Power Well:** SUS
19:14	0x0 RW	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
13:12	0x0 RW	**UTMI PPUTMI BLOCK RESERVE (UTMI_PPUTMI_RSVD):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional Reserved pin going to uxfehpputmi fub Bit1: Opmode is delayed by 2 utmi clks while txvalid is direct from the utmi interface. Chicken to add 2 delays to txvalid. 1: Two additional delays txvalid in c73usb250_usbhsip_uxfehpputmi to resolve suspend resume treated as sync pattern. 0: keep as legacy. Bit0: Chicken bit for device remote wake (RTL as host), where glitch observe when host retrun K. 1: Enable OR-ing of linestate with pre-condition. Need to precon with K instead of J. 0: keep as legacy. **Power Well:** SUS
11	0x0 RW	**UTMI LSPKToverFSFSM Bypass (LSPFTOVERFSLINK_FSMBYPASS):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: Bypass c73usb250_usbhsip_uxfehpputmil3fsm to resolve HS suspend resume glitch on EOR. The FSM is adding delay to xcvrselect resulting delay of speed change during resume which cause HS EOR as FS EOR. **Power Well:** SUS
10:9	0x0 RW	**UTMI Misc reserve (REG_UTMI_MISC_RSVD):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional Reserved pin going to utmi_misc fub **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**UTMI Misc policy (REG_MISC_POLICY):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional LS Double K fix chicken bit policy. Set 1 to disable fix for double K seen on LS sync pattern. **Power Well:** SUS
7	0x0 RW	**High Speed Transmit Linestate reflect enable (REG_HSTX_REFLECT_ON_LINESTATE_EN):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To enable HS transmit reflect to linestate (Linestate to reflect J during transmit) 0: Disable HS transmit reflect. Linestate stay as SE0. **Power Well:** SUS
6	0x1 RW	**Tri Buffer enable (REG_BUFFER_TRISTATE_EN):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To enable tristating buffer with opmode=01. 0: Disable opmode=01 from buffer pull-up enable. **Power Well:** SUS
5:4	0x1 RW	**HS/FS/LS Port Staggering Delay Select (HSFSLSPSEL):** This field selects the HS/FS/LS driveen staggering for this port: 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset **Power Well:** SUS
3	0x0 RW	**Speed Based Dynamic Clock Gating Enable (SPDDCG):** reg_utmi_spd_based_lcg_en (Disable bit for UTMI Local Clock Gating based on port speed: When clear, this allows the High Speed Link control's 480Mhz and its divided 48/60 MHz link clock trunk to be gated when idle conditions are met). 1: Enable Clock Gating 0: Disable Clock Gating **Power Well:** SUS
2	0x0 RW	**Suspend Based Dynamic Clock Gating (SUSDCG):** reg_utmi_susp_based_lcg_en (Disable bit for UTMI Local Clock Gating based on port suspend: When clear, this allows the High Speed Link control's 480Mhz and its divided 48/60 MHz link clock trunk to be gated when idle conditions are met.When set, UTMI local clock gating is bypassed). 1: Enable Clock Gating 0: Disable Clock Gating **Power Well:** SUS
1	0x0 RW	**Miscellaneous Policies 1 (MISCP1):** chicken bit to disable the PPT A1 Fix to deassert Rxactive early (this bit is introduced to disable the deassert rxactive early logic added in by PPT). 1: Disable fix 0: Enable fix **Power Well:** SUS
0	0x0 RW	**Miscellaneous Policies 0 (MISCP0):** chicken bit to disable the fix to reset the enclk counter upon txvalid (enclk counter is made to reset upon txvalid. This bit is to bypass this fix). 1: Disable fix 0: Enable fix **Power Well:** SUS

7.14.18 UTMI RX REG1 PER PORT (UTMI_RX_REG1_PER_PORT_PP2)—Offset 4305h

Access Method

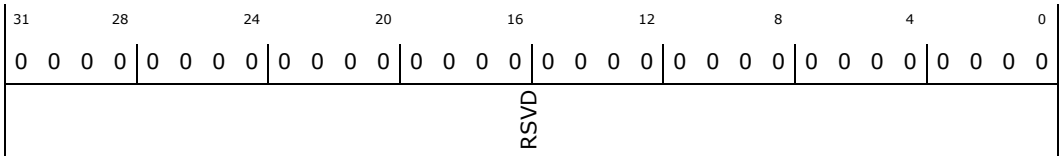
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4305h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS

7.14.19 UTMI RX REG2 PER PORT (UTMI_RX_REG2_PER_PORT_PP2)—Offset 4306h

Access Method

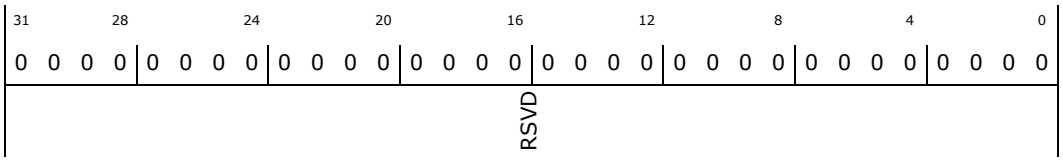
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4306h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD:** RSVD **Power Well:** SUS

7.14.20 UTMI TX REG PER PORT (UTMI_TX_REG_PER_PORT_PP2)—Offset 4307h

Access Method

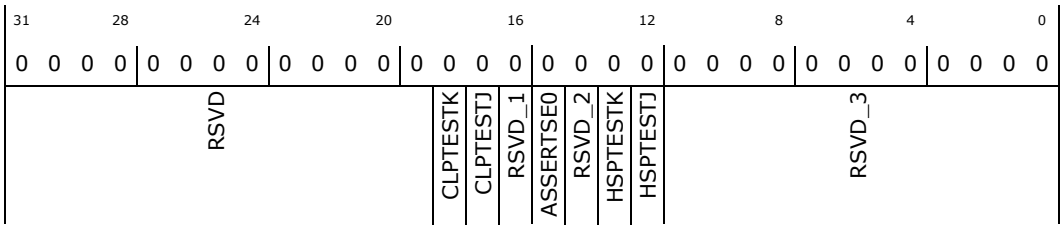
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4307h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS
18	0x0 WO	**CLPTESTK:** Classic force K **Power Well:** SUS
17	0x0 WO	**CLPTESTJ:** Classic force J **Power Well:** SUS
16	0x0 RO	**RSVD (RSVD_1):** Reserved. **Power Well:** SUS
15	0x0 WO	**ASSERTSE0:** Assert SE0 **Power Well:** SUS
14	0x0 RO	**RSVD (RSVD_2):** Reserved. **Power Well:** SUS
13	0x0 WO	**HSPTESTK:** HS Test K mode **Power Well:** SUS
12	0x0 WO	**HSPTESTJ:** HS Test J mode **Power Well:** SUS
11:0	0x0 RO	**RSVD (RSVD_3):** Reserved. **Power Well:** SUS

7.14.21 UTMI MISC REG PER PORT (UTMI_MISC_REG_PER_PORT_PP2)—Offset 4308h

Access Method

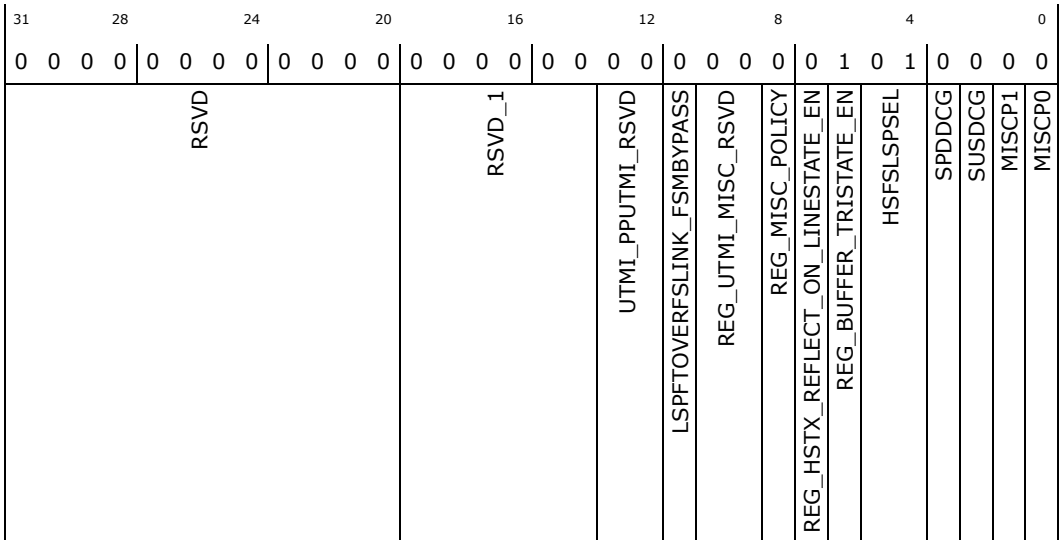
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4308h

Op Codes:

h - Read, h - Write

Default: 00000050h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RSVD:** RSVD **Power Well:** SUS
19:14	0x0 RW	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
13:12	0x0 RW	**UTMI PPUTMI BLOCK RESERVE (UTMI_PPUTMI_RSVD):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional Reserved pin going to uxfehpputmi fub Bit1: Opmode is delayed by 2 utmi clks while txvalid is direct from the utmi interface. Chicken to add 2 delays to txvalid. 1: Two additional delays txvalid in c73usb250_usbhsip_uxfehpputmi to resolve suspend resume treated as sync pattern. 0: keep as legacy. Bit0: Chicken bit for device remote wake (RTL as host), where glitch observe when host retrun K. 1: Enable OR-ing of linestate with pre-condition. Need to precon with K instead of J. 0: keep as legacy. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
11	0x0 RW	**UTMI LSPKToverFSFSM Bypass (LSPFTOVERFSLINK_FSMBYPASS):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: Bypass c73usb250_usbhsip_uxfehpputmil3fsm to resolve HS suspend resume glitch on EOR. The FSM is adding delay to xcvrselect resulting delay of speed change during resume which cause HS EOR as FS EOR. **Power Well:** SUS
10:9	0x0 RW	**UTMI Misc reserve (REG_UTMI_MISC_RSVD):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional Reserved pin going to utmi_misc fub **Power Well:** SUS
8	0x0 RW	**UTMI Misc policy (REG_MISC_POLICY):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional LS Double K fix chicken bit policy. Set 1 to disable fix for double K seen on LS sync pattern. **Power Well:** SUS
7	0x0 RW	**High Speed Transmit Linestate reflect enable (REG_HSTX_REFLECT_ON_LINESTATE_EN):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To enable HS transmit reflect to linestate (Linestate to reflect J during transmit) 0: Disable HS transmit reflect. Linestate stay as SE0. **Power Well:** SUS
6	0x1 RW	**Tri Buffer enable (REG_BUFFER_TRISTATE_EN):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To enable tristating buffer with opmode=01. 0: Disable opmode=01 from buffer pull-up enable. **Power Well:** SUS
5:4	0x1 RW	**HS/FS/LS Port Staggering Delay Select (HSFSLSPSEL):** This field selects the HS/FS/LS driveen staggering for this port: 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset **Power Well:** SUS
3	0x0 RW	**Speed Based Dynamic Clock Gating Enable (SPDDCG):** reg_utmi_spd_based_lcg_en (Disable bit for UTMI Local Clock Gating based on port speed: When clear, this allows the High Speed Link control's 480Mhz and its divided 48/60 MHz link clock trunk to be gated when idle conditions are met). 1: Enable Clock Gating 0: Disable Clock Gating **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**Suspend Based Dynamic Clock Gating (SUSDCG):** reg_utmi_susp_based_lcg_en (Disable bit for UTMI Local Clock Gating based on port suspend: When clear, this allows the High Speed Link control's 480Mhz and its divided 48/60 MHz link clock trunk to be gated when idle conditions are met.When set, UTMI local clock gating is bypassed). 1: Enable Clock Gating 0: Disable Clock Gating **Power Well:** SUS
1	0x0 RW	**Miscellaneous Policies 1 (MISCP1):** chicken bit to disable the PPT A1 Fix to deassert Rxactive early (this bit is introduced to disable the deassert rxactive early logic added in by PPT). 1: Disable fix 0: Enable fix **Power Well:** SUS
0	0x0 RW	**Miscellaneous Policies 0 (MISCP0):** chicken bit to disable the fix to reset the enclk counter upon txvalid (enclk counter is made to reset upon txvalid. This bit is to bypass this fix). 1: Disable fix 0: Enable fix **Power Well:** SUS

7.14.22 UTMI RX REG1 PER PORT (UTMI_RX_REG1_PER_PORT_PP3)—Offset 4405h

Access Method

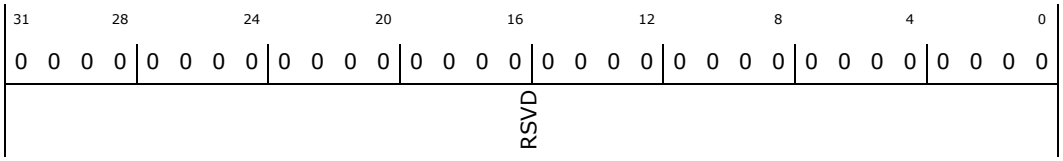
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4405h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS

7.14.23 UTMI RX REG2 PER PORT (UTMI_RX_REG2_PER_PORT_PP3)—Offset 4406h

Access Method

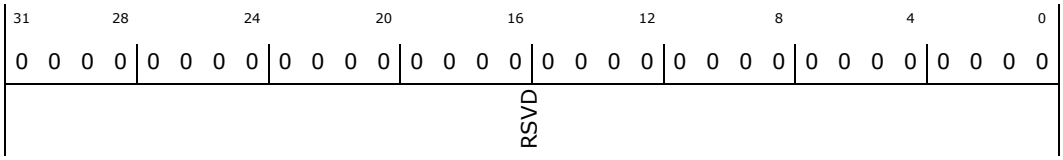
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4406h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD:** RSVD **Power Well:** SUS

7.14.24 UTMI TX REG PER PORT (UTMI_TX_REG_PER_PORT_PP3)—Offset 4407h

Access Method

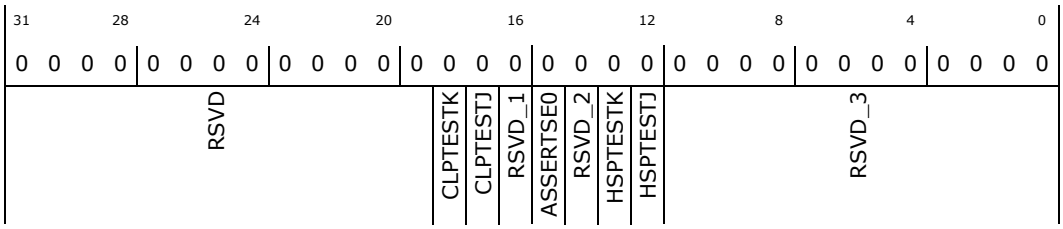
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4407h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS
18	0x0 WO	**CLPTESTK:** Classic force K **Power Well:** SUS
17	0x0 WO	**CLPTESTJ:** Classic force J **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RO	**RSVD (RSVD_1):** Reserved. **Power Well:** SUS
15	0x0 WO	**ASSERTSE0:** Assert SE0 **Power Well:** SUS
14	0x0 RO	**RSVD (RSVD_2):** Reserved. **Power Well:** SUS
13	0x0 WO	**HSPTESTK:** HS Test K mode **Power Well:** SUS
12	0x0 WO	**HSPTESTJ:** HS Test J mode **Power Well:** SUS
11:0	0x0 RO	**RSVD (RSVD_3):** Reserved. **Power Well:** SUS

7.14.25 UTMI MISC REG PER PORT (UTMI_MISC_REG_PER_PORT_PP3)—Offset 4408h

Access Method

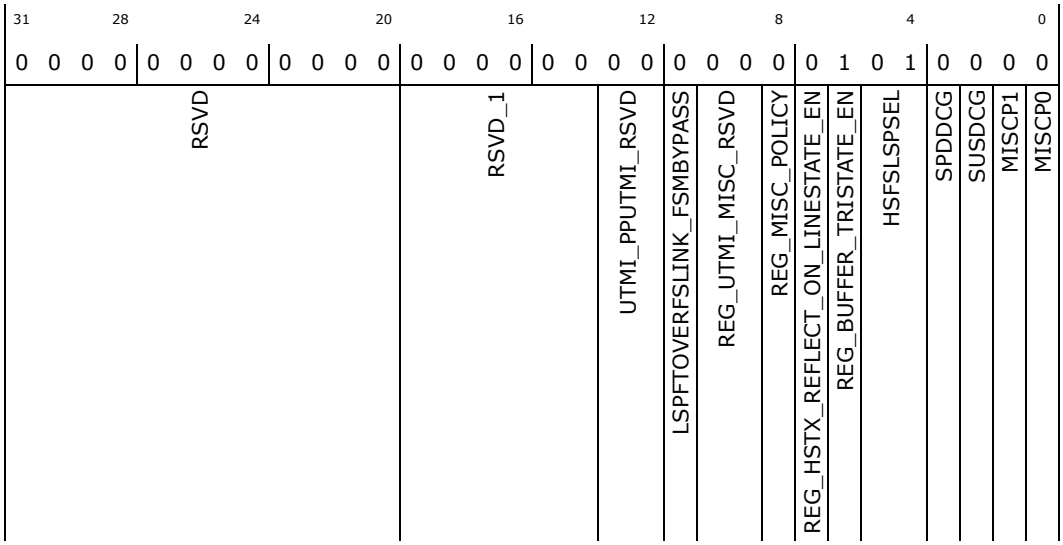
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4408h

Op Codes:

h - Read, h - Write

Default: 00000050h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RSVD:** RSVD **Power Well:** SUS
19:14	0x0 RW	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
13:12	0x0 RW	**UTMI PPUTMI BLOCK RESERVE (UTMI_PPUTMI_RSVD):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional Reserved pin going to uxfehpputmi fub Bit1: Opmode is delayed by 2 utmi clks while txvalid is direct from the utmi interface. Chicken to add 2 delays to txvalid. 1: Two additional delays txvalid in c73usb250_usbhsip_uxfehpputmi to resolve suspend resume treated as sync pattern. 0: keep as legacy. Bit0: Chicken bit for device remote wake (RTL as host), where glitch observe when host retrun K. 1: Enable OR-ing of linestate with pre-condition. Need to precon with K instead of J. 0: keep as legacy. **Power Well:** SUS
11	0x0 RW	**UTMI LSPKToverFSFSM Bypass (LSPFTOVERFSLINK_FSMBYPASS):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: Bypass c73usb250_usbhsip_uxfehpputmil3fsm to resolve HS suspend resume glitch on EOR. The FSM is adding delay to xcvrselect resulting delay of speed change during resume which cause HS EOR as FS EOR. **Power Well:** SUS
10:9	0x0 RW	**UTMI Misc reserve (REG_UTMI_MISC_RSVD):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional Reserved pin going to utmi_misc fub **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**UTMI Misc policy (REG_MISC_POLICY):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional LS Double K fix chicken bit policy. Set 1 to disable fix for double K seen on LS sync pattern. **Power Well:** SUS
7	0x0 RW	**High Speed Transmit Linestate reflect enable (REG_HSTX_REFLECT_ON_LINESTATE_EN):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To enable HS transmit reflect to linestate (Linestate to reflect J during transmit) 0: Disable HS transmit reflect. Linestate stay as SE0. **Power Well:** SUS
6	0x1 RW	**Tri Buffer enable (REG_BUFFER_TRISTATE_EN):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To enable tristating buffer with opmode=01. 0: Disable opmode=01 from buffer pull-up enable. **Power Well:** SUS
5:4	0x1 RW	**HS/FS/LS Port Staggering Delay Select (HSFSLSPSEL):** This field selects the HS/FS/LS driveen staggering for this port: 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset **Power Well:** SUS
3	0x0 RW	**Speed Based Dynamic Clock Gating Enable (SPDDCG):** reg_utmi_spd_based_lcg_en (Disable bit for UTMI Local Clock Gating based on port speed: When clear, this allows the High Speed Link control's 480Mhz and its divided 48/60 MHz link clock trunk to be gated when idle conditions are met). 1: Enable Clock Gating 0: Disable Clock Gating **Power Well:** SUS
2	0x0 RW	**Suspend Based Dynamic Clock Gating (SUSDCG):** reg_utmi_susp_based_lcg_en (Disable bit for UTMI Local Clock Gating based on port suspend: When clear, this allows the High Speed Link control's 480Mhz and its divided 48/60 MHz link clock trunk to be gated when idle conditions are met.When set, UTMI local clock gating is bypassed). 1: Enable Clock Gating 0: Disable Clock Gating **Power Well:** SUS
1	0x0 RW	**Miscellaneous Policies 1 (MISCP1):** chicken bit to disable the PPT A1 Fix to deassert Rxactive early (this bit is introduced to disable the deassert rxactive early logic added in by PPT). 1: Disable fix 0: Enable fix **Power Well:** SUS
0	0x0 RW	**Miscellaneous Policies 0 (MISCP0):** chicken bit to disable the fix to reset the enclk counter upon txvalid (enclk counter is made to reset upon txvalid. This bit is to bypass this fix). 1: Disable fix 0: Enable fix **Power Well:** SUS

7.14.26 UTMI RX REG1 PER PORT (UTMI_RX_REG1_PER_PORT_PP4)—Offset 4505h

Access Method

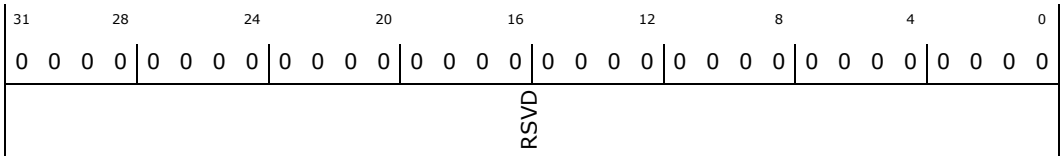
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4505h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS

7.14.27 UTMI RX REG2 PER PORT (UTMI_RX_REG2_PER_PORT_PP4)—Offset 4506h

Access Method

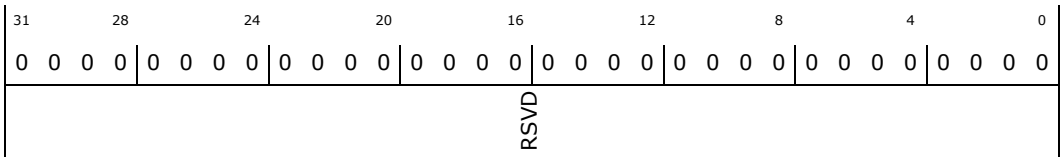
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4506h

Op Codes:

h - Read, h - Write

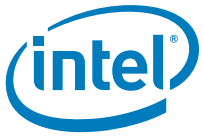
Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD:** RSVD **Power Well:** SUS

7.14.28 UTMI TX REG PER PORT (UTMI_TX_REG_PER_PORT_PP4)—Offset 4507h

Access Method



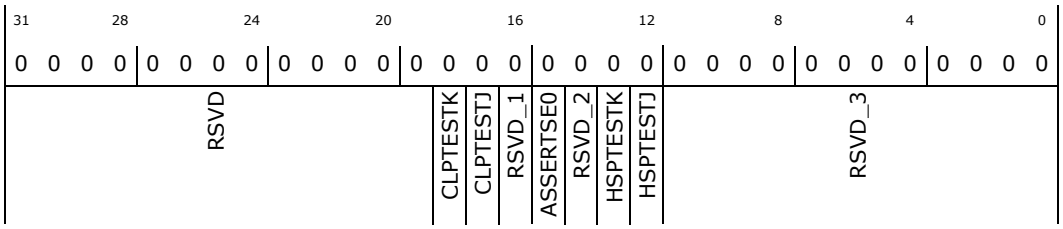
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4507h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS
18	0x0 WO	**CLPTESTK:** Classic force K **Power Well:** SUS
17	0x0 WO	**CLPTESTJ:** Classic force J **Power Well:** SUS
16	0x0 RO	**RSVD (RSVD_1):** Reserved. **Power Well:** SUS
15	0x0 WO	**ASSERTSE0:** Assert SE0 **Power Well:** SUS
14	0x0 RO	**RSVD (RSVD_2):** Reserved. **Power Well:** SUS
13	0x0 WO	**HSPTESTK:** HS Test K mode **Power Well:** SUS
12	0x0 WO	**HSPTESTJ:** HS Test J mode **Power Well:** SUS
11:0	0x0 RO	**RSVD (RSVD_3):** Reserved. **Power Well:** SUS

7.14.29 UTMI MISC REG PER PORT (UTMI_MISC_REG_PER_PORT_PP4)—Offset 4508h

Access Method

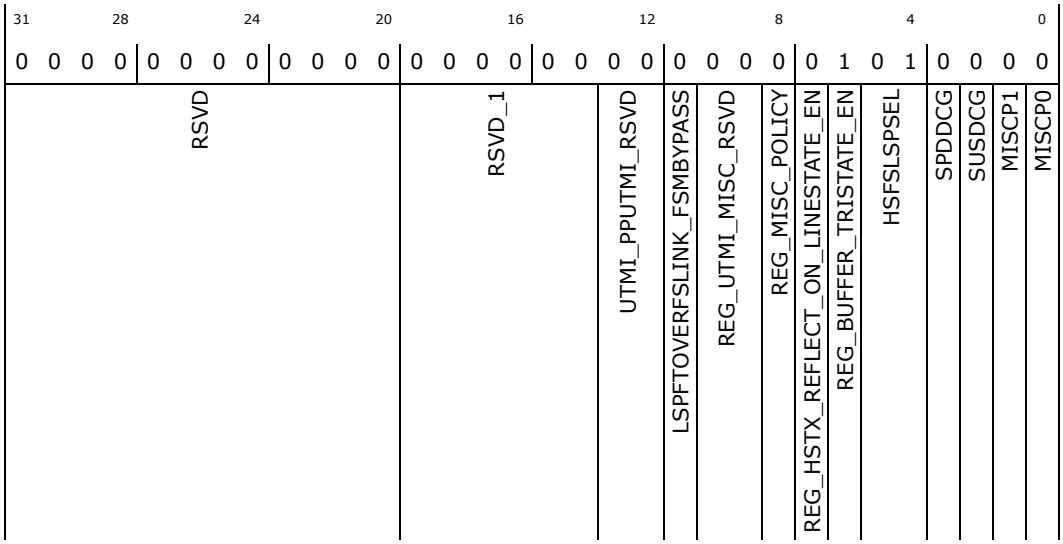
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4508h

Op Codes:

h - Read, h - Write

Default: 00000050h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RSVD:** RSVD **Power Well:** SUS
19:14	0x0 RW	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
13:12	0x0 RW	**UTMI PPUTMI BLOCK RESERVE (UTMI_PPUTMI_RSVD):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional Reserved pin going to uxfehpputmi fub Bit1: Opmode is delayed by 2 utmi clks while txvalid is direct from the utmi interface. Chicken to add 2 delays to txvalid. 1: Two additional delays txvalid in c73usb250_usbhsip_uxfehpputmi to resolve suspend resume treated as sync pattern. 0: keep as legacy. Bit0: Chicken bit for device remote wake (RTL as host), where glitch observe when host retrun K. 1: Enable OR-ing of linestate with pre-condition. Need to precon with K instead of J. 0: keep as legacy. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
11	0x0 RW	**UTMI LSPKToverFSFSM Bypass (LSPFTOVERFSLINK_FSMBYPASS):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: Bypass c73usb250_usbhsip_uxfehpputmil3fsm to resolve HS suspend resume glitch on EOR. The FSM is adding delay to xcvrselect resulting delay of speed change during resume which cause HS EOR as FS EOR. **Power Well:** SUS
10:9	0x0 RW	**UTMI Misc reserve (REG_UTMI_MISC_RSVD):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional Reserved pin going to utmi_misc fub **Power Well:** SUS
8	0x0 RW	**UTMI Misc policy (REG_MISC_POLICY):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional LS Double K fix chicken bit policy. Set 1 to disable fix for double K seen on LS sync pattern. **Power Well:** SUS
7	0x0 RW	**High Speed Transmit Linestate reflect enable (REG_HSTX_REFLECT_ON_LINESTATE_EN):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To enable HS transmit reflect to linestate (Linestate to reflect J during transmit) 0: Disable HS transmit reflect. Linestate stay as SE0. **Power Well:** SUS
6	0x1 RW	**Tri Buffer enable (REG_BUFFER_TRISTATE_EN):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To enable tristating buffer with opmode=01. 0: Disable opmode=01 from buffer pull-up enable. **Power Well:** SUS
5:4	0x1 RW	**HS/FS/LS Port Staggering Delay Select (HSFSLSPSEL):** This field selects the HS/FS/LS driveen staggering for this port: 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset **Power Well:** SUS
3	0x0 RW	**Speed Based Dynamic Clock Gating Enable (SPDDCG):** reg_utmi_spd_based_lcg_en (Disable bit for UTMI Local Clock Gating based on port speed: When clear, this allows the High Speed Link control's 480Mhz and its divided 48/60 MHz link clock trunk to be gated when idle conditions are met). 1: Enable Clock Gating 0: Disable Clock Gating **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**Suspend Based Dynamic Clock Gating (SUSDCG):** reg_utmi_susp_based_lcg_en (Disable bit for UTMI Local Clock Gating based on port suspend: When clear, this allows the High Speed Link control's 480Mhz and its divided 48/60 MHz link clock trunk to be gated when idle conditions are met.When set, UTMI local clock gating is bypassed). 1: Enable Clock Gating 0: Disable Clock Gating **Power Well:** SUS
1	0x0 RW	**Miscellaneous Policies 1 (MISCP1):** chicken bit to disable the PPT A1 Fix to deassert Rxactive early (this bit is introduced to disable the deassert rxactive early logic added in by PPT). 1: Disable fix 0: Enable fix **Power Well:** SUS
0	0x0 RW	**Miscellaneous Policies 0 (MISCP0):** chicken bit to disable the fix to reset the enclk counter upon txvalid (enclk counter is made to reset upon txvalid. This bit is to bypass this fix). 1: Disable fix 0: Enable fix **Power Well:** SUS

7.14.30 RCOMP REGISTER (RCOMP_REGISTER)—Offset 7F09h

Access Method

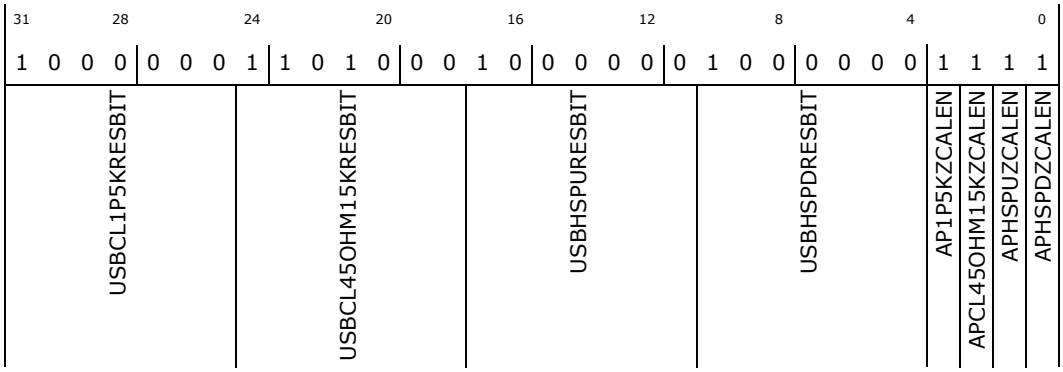
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 7F09h

Op Codes:

h - Read, h - Write

Default: 81A2040Fh



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x40 RO/V	**USBCL1P5KRESBIT:** Device mode CL 1.5K RCOMP bits coming from core logic to set the CL 1.5k pull-up impedance value. This register is hard coded, These bits are binary weighted and are for device mode classic 1.5k pull-up calibration. These bits will always change during RCAL to tune the termination resistance **Power Well:** SUS
24:18	0x68 RO/V	**USBCL45OHM15KRESBIT:** CL 45 ohm/15K RCOMP bits coming from core logic to set the CL 45 ohm/15k pull-down impedance value. This register is hard coded, These bits are binary weighted and are for classic 45 ohm/15k pull-down calibration. These bits will always change during RCAL to tune the termination resistance **Power Well:** SUS
17:11	0x40 RO/V	**USBHSPURESBIT:** HS PU RCOMP bits coming from core logic to set the HS pull-up impedance value. This register is hard coded, These bits are binary weighted and are for HS TX pull-up calibration. These bits will always change during RCAL to tune the termination resistance **Power Well:** SUS
10:4	0x40 RO/V	**USBHSPDRESBIT:** HS PD RCOMP bits coming from core logic to set the HS pull-down impedance value. This register is hard coded, These bits are binary weighted and are for HS TX pull-down calibration. These bits will always change during RCAL to tune the termination resistance **Power Well:** SUS
3	0x1 RW	**AP1P5KZCALEN:** Set it to 1b to enable Device Mode 1.5K Pull Up hardware based RCAL. **Power Well:** SUS
2	0x1 RW	**APCL45OHM15KZCALEN:** Set it to 1b to enable CL 45 Ohm/15K Pull Down hardware based RCAL. **Power Well:** SUS
1	0x1 RW	**APHSPUZCALEN:** Set it to 1b to enable HS Pull-up hardware based RCAL. **Power Well:** SUS
0	0x1 RW	**APHSPDZCALEN:** Set it to 1b to enable HS Pull-Down hardware based RCAL. **Power Well:** SUS

7.14.31 ICOMP REGISTER (ICOMP_REGISTER)—Offset 7F0Ah

Access Method

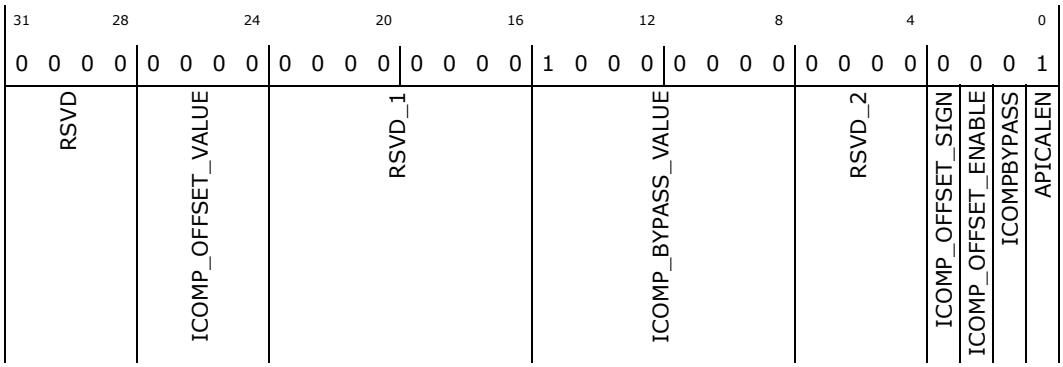
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 7F0Ah

Op Codes:

h - Read, h - Write

Default: 00008001h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RSVD:** Reserved **Power Well:** SUS
27:24	0x0 RW	**ICOMP OFFSET VALUE (ICOMP_OFFSET_VALUE):** icomp offset value The state machine has the ability to manipulate the evaluated values as desired with the programmable offset and override adjustments for the value that going to be updated in the AFE. Once steady state 1-0-1 or 0-1-0 is detected on curcountup and icomp offset enable bit is set, an offset will be added, with the amount of offset programmable via this configuration bits. **Power Well:** SUS
23:16	0x0 RO	**RSVD (RSVD_1):** Reserved **Power Well:** SUS
15:8	0x80 RW	**ICOMP BYPASS VALUE (ICOMP_BYPASS_VALUE):** Icomp bypass value The ability to bypass the ICOMP compensated binary value with this value that is going to be updated in the AFE when icompbypass bit is set. **Power Well:** SUS
7:4	0x0 RO	**RSVD (RSVD_2):** Reserved **Power Well:** SUS
3	0x0 RW	**ICOMP OFFSET SIGN (ICOMP_OFFSET_SIGN):** icomp offset sign bit 1 - incrementing offset value 0 - decrementing offset value **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**ICOMP OFFSET ENABLE (ICOMP_OFFSET_ENABLE):** icomp offset enable bit 1 - enable icomp offset override 0 - disable icomp offset override **Power Well:** SUS
1	0x0 RW	**ICOMPBYPASS:** Icomp bypass mode. config controlled. 1 - enable icomp bypass 0 - disable icomp bypass **Power Well:** SUS
0	0x1 RW	**APICALEN:** Set it to 1b to enable hardware based ICAL. **Power Well:** SUS

7.14.32 USB2 TEST GLOBAL REG1 (USB2_TEST_GLOBAL_REG1)—Offset 400Bh

Access Method

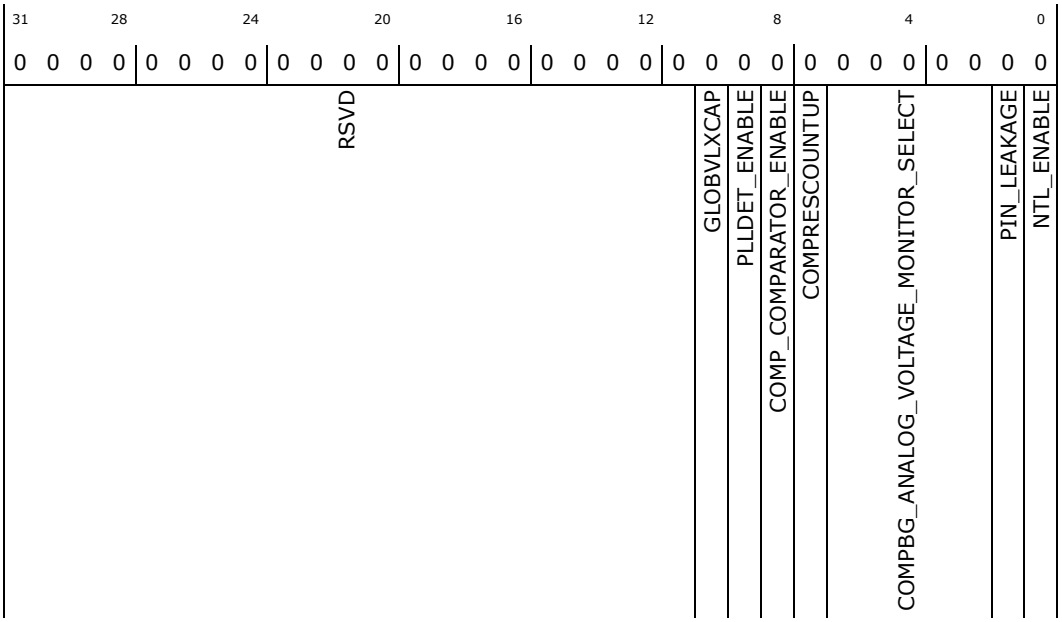
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 400Bh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:11	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS
10	0x0 RW	**Global VIx Capture (GLOBVLXCAP):** 1: Captures the live values from AFE. Test SW is required to allow enough settling time before setting this bit. 0: Allows the live values to propagate into register fields. **Power Well:** SUS
9	0x0 RW	**PLLDET ENABLE (PLLDET_ENABLE):** PLL determinism enable bit. (Bit is not applicable for 1271) **Power Well:** SUS
8	0x0 RW	**COMP COMPARATOR ENABLE (COMP_COMPARATOR_ENABLE):** If set, COMP comparator is enabled. iusbhspucalen_h will be forced to 1 . Iusbtxcuren_h will be forced to 0 . iusbhspuresbit(6:0) and iusbhspdresbit(6:0) will be forced to 0 . **Power Well:** SUS
7	0x0 RO	**COMPRESCOUNTUP:** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it **Power Well:** SUS
6:2	0x0 RW	**COMPBG ANALOG VOLTAGE MONITOR SELECT (COMPBG_ANALOG_VOLTAGE_MONITOR_SELECT):** Change from 4 bits to 5 bits. 00000 =) (default) 00001 =) Select vcccoreport_1p0_lv for powerdroop detect 00010 =) Select vccsusport_1p0_lv for powerdroop detect 00011 =) Current calibration N-channel biasing voltage 00100 =) Current calibration P-channel biasing voltage 00101 =) select vccdusbsus_1p0_lv for powerdroop detect 00110 =) reserve for future use 00111 =) HS pull-up calibration Vref 01000 =) Current Calibration Vref 01001 =) Classic 15K pull-up Calibration Vref 01010 =) Comparator Offset Calibration Vref 01011 =) HS Disconnect Vref 01100 =) HS Squelch Vref+ 01101 =) HS Squelch Vref- 01110 =) LDO monitoring signals 01111 onwards =) reserve for future use **Power Well:** SUS
1	0x0 RW	**PIN LEAKAGE/IDDQ ENABLE (PIN_LEAKAGE):** Pin Leakage test mode enable. If asserted, pin leakage test mode is enabled and AFE pin constraints will be enabled. **Power Well:** SUS
0	0x0 RW	**NTL ENABLE (NTL_ENABLE):** Enable control bit for NTL test mode. If asserted, NTL test mode is enabled and AFE pin constraints is set. **Power Well:** SUS

7.14.33 USB2 TEST GLOBAL REG2 (USB2_TEST_GLOBAL_REG2)—Offset 400Ch

Access Method

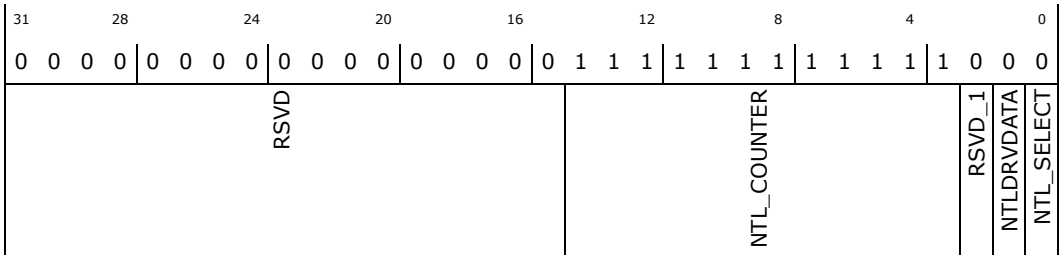
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 400Ch

Op Codes:

h - Read, h - Write

Default: 00007FF8h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS
14:3	0xfff RW	**NTL COUNTER (NTL_COUNTER):** 12-bit NTL countdown value **Power Well:** SUS
2	0x0 RO	**RSVD (RSVD_1):** Reserved. **Power Well:** SUS
1	0x0 RW	**NTLDRVDATA:** (usbdata==nrziout) if to detect voltage on D+, then set usbdata to a 1 if to detect voltage on D-, then set usbdata to a 0 **Power Well:** SUS
0	0x0 RW	**NTL SELECT (NTL_SELECT):** select classic j or classic k. if 0, select K and drive 1 on D- and 0 on D+. if 1, select J and drive 1 on D+ and 0 on D- (ntl pre-conditioning) **Power Well:** SUS

7.14.34 USB2 TEST GLOBAL REG3 (USB2_TEST_GLOBAL_REG3)—Offset 400Dh

Access Method

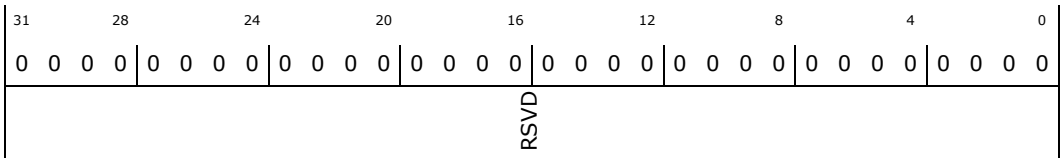
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 400Dh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS

7.14.35 USB2 TEST GLOBAL REG4 (USB2_TEST_GLOBAL_REG4)—Offset 400Eh

Access Method

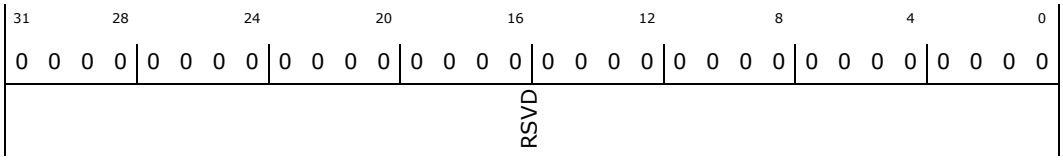
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 400Eh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS

7.14.36 ICOMP PERPORT REG (ICOMP_PERPORT_REG_PP0)—Offset 410Fh

Access Method

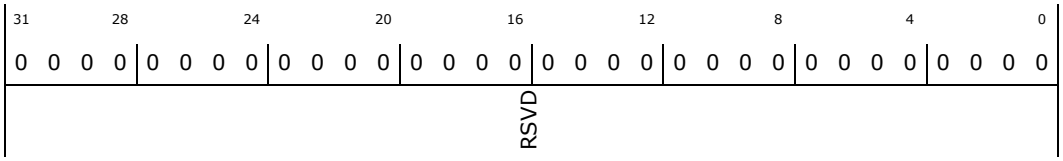
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 410Fh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD:** RSVD **Power Well:** SUS

7.14.37 ICOMP PERPORT REG (ICOMP_PERPORT_REG_PP1)—Offset 420Fh

Access Method

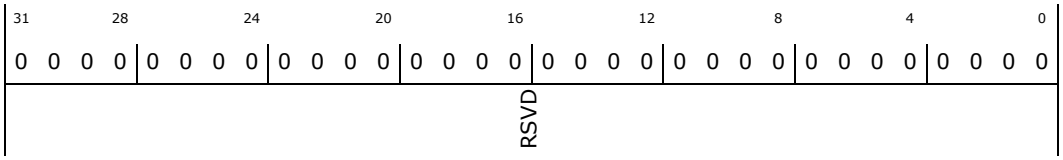
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 420Fh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD:** RSVD **Power Well:** SUS

7.14.38 ICOMP PERPORT REG (ICOMP_PERPORT_REG_PP2)—Offset 430Fh

Access Method

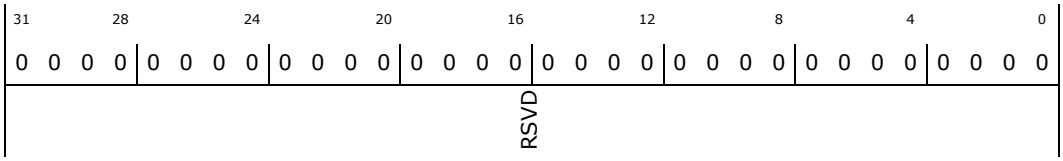
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 430Fh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD:** RSVD **Power Well:** SUS

7.14.39 ICOMP PERPORT REG (ICOMP_PERPORT_REG_PP3)—Offset 440Fh

Access Method

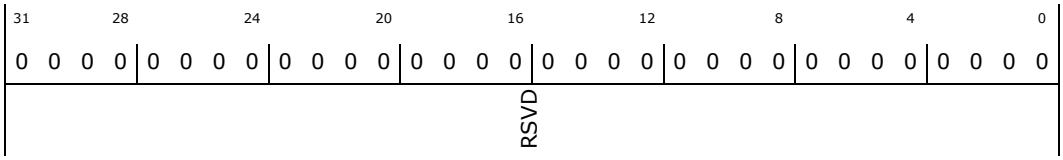
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 440Fh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD:** RSVD **Power Well:** SUS

7.14.40 ICOMP PERPORT REG (ICOMP_PERPORT_REG_PP4)—Offset 450Fh

Access Method

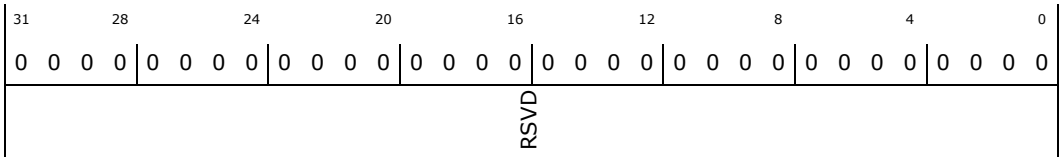
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 450Fh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD:** RSVD **Power Well:** SUS

7.14.41 USB2 TEST GLOBAL REG5 (USB2_TEST_GLOBAL_REG5)—Offset 4010h

Access Method

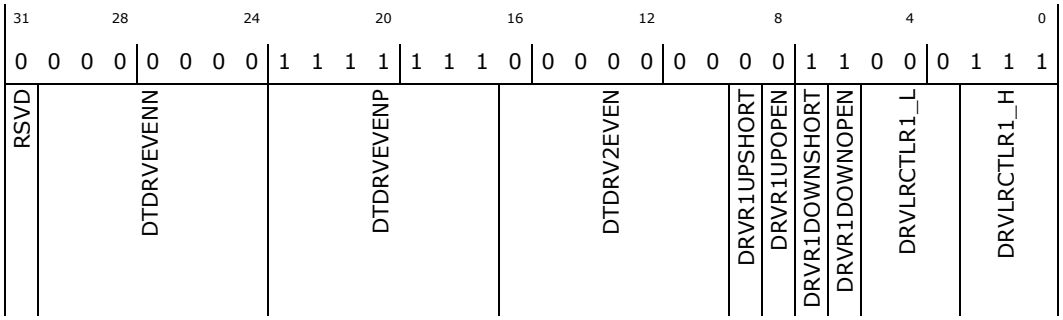
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4010h

Op Codes:

h - Read, h - Write

Default: 00FE00C7h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS
30:24	0x0 RW	**DTDRVEVENN:** Even controls of the N-switch of the R1 resistors from the positive pad s side and odd controls of the N-switch of the R1 resistor from the negative pad's side. Each bit stands for different binary segment of the R-DAC. 0000000 (default) Digital monitoring: 0000000b DC monitoring: 0000000b (use default setting) **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
23:17	0x7f RW	**DTDRVEVENP:** Even controls of the P-switch of the R1 resistors from the positive pad s side and odd controls of the P-switch of the R1 resistor from the negative pad's side. Each bit stands for different binary segment of the R-DAC. 1111111 (default) Digital monitoring: 0111111b DC monitoring: 1111111b (use default setting) **Power Well:** SUS
16:10	0x0 RW	**DTDRV2EVEN:** Even controls of the R2 resistors. Each bit stands for different binary segment of the R-DAC. 0000000 (default) **Power Well:** SUS
9	0x0 RW	**DRVR1UPSHORT:** Enable/disble control to short r1 p-switch 0 - disable (default) 1 - short r1 p-switch Digital/DC monitoring: 0b (disable) **Power Well:** SUS
8	0x0 RW	**DRVR1UPOPEN:** Enable/disable control the R1 p-switch driver 0 - disable (default) 1 - enable Digital monitoring: 1b (enable R1 p-switch driver) DC monitoring: 0b (disable R1 p-switch driver) **Power Well:** SUS
7	0x1 RW	**DRVR1DOWNSHORT:** Enable/disble control to short r1 n-switch 1 - disable (default) 0 - short r1 n-switch Digital/DC monitoring: 1b (disable) **Power Well:** SUS
6	0x1 RW	**DRVR1DOWNOPEN:** Enable/disable control the R1 n-switch driver 1 - disable (default) 0 - enable Digital monitoring: 0b (enable R1 n-switch driver) DC monitoring: 1b (disable R1 n-switch driver) **Power Well:** SUS
5:3	0x0 RW	**DRVLRCTLR1_L:** Control the R1 pre-driver NMOS 000 - disable (default) 111 - enable other values can be used for pre-driver strength Digital monitoring: 111b (enable R1 pre-driver NMOS) DC monitoring: 000b (disable R1 pre-driver NMOS) **Power Well:** SUS
2:0	0x7 RW	**DRVLRCTLR1_H:** Controls the R1 pre-driver PMOS 111 - disable (default) 000 - enable other values can be used for pre-driver strength Digital monitoring: 000b (enable R1 pre-driver PMOS) DC monitoring: 111b (disable R1 pre-driver PMOS) **Power Well:** SUS

7.14.42 USB2 TEST GLOBAL REG6 (USB2_TEST_GLOBAL_REG6)—Offset 4011h

Access Method

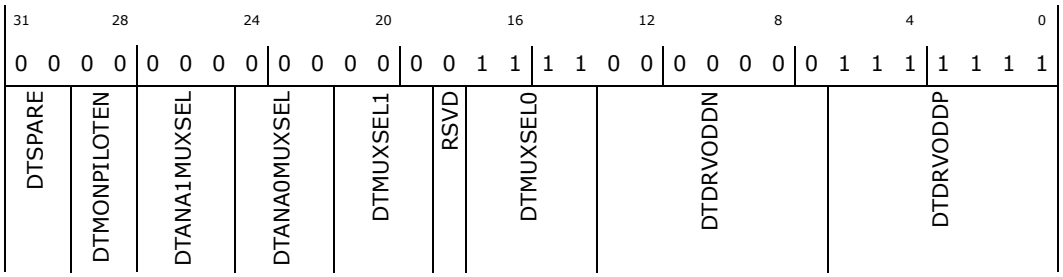
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4011h

Op Codes:

h - Read, h - Write

Default: 0003C07Fh



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DTSPARE:** Reserved bits **Power Well:** SUS
29:28	0x0 RW	**DTMONPILOTEN:** Used to enable/disable DC Monitor Port0 and Port1 00 - disable (default) 01 - enable port0 DC monitor 10 - enable port1 DC monitor 11 - enable port0 and port1 DC monitor Digital monitoring: 00b (disable DC Monitor) DC monitoring: 11b (enable DC Monitor) **Power Well:** SUS
27:25	0x0 RW	**DTANA1MUXSEL:** Used to select mux setting of Port1 of DC monitoring 000 - ana0_1 comprcalref (default) 001 - ana1_1 compvbgbuf 010 - ana2_1 vss 011 - ana3_1 vss 100 - ana4_1 vss 101 - ana5_1 vss 110 - ana6_1 vss 111 - ana7_1 vss **Power Well:** SUS
24:22	0x0 RW	**DTANA0MUXSEL:** Used to select mux setting of Port0 of DC monitoring 000 - ana0_0 vss (default) 001 - ana1_0 vss 010 - ana2_0 vss 011 - ana3_0 vss 100 - ana4_0 vss 101 - ana5_0 vss 110 - ana6_0 vss 111 - ana7_0 vss **Power Well:** SUS
21:19	0x0 RW	**DTMUXSEL1:** Used to select mux setting of Port1 of Digital monitoring 000 - obs0_1 opllfbclk (default) 001 - obs1_1 monpllfbclkmon 010 - obs2_1 monplllock 011 - obs3_1 vss 100 - obs4_1 vss 101 - obs5_1 vss 110 - obs6_1 vss 111 - obs7_1 vss **Power Well:** SUS
18	0x0 RO	**RSVD:** RSVD **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
17:14	0xf RW	**DTMUXSEL0:** Used to select mux setting of Port0 of Digital monitoring 0000 select opllsleep 0001 select omonpllbypt 0010 select omonplllock 0011 select omonpllstartup 0100 select omonpllyank 0101 select opllspare(0) 0110 select opllspare(1) 0111 select opllspare(2) 1000 - select opllspare(3) 1001 select opllrefclk 1010 select opllfbclk 1011 - omonpllfbclkmon Others - vss **Power Well:** SUS
13:7	0x0 RW	**DTDRVODDN:** Odd controls of the N-switch of the R1 resistors from the positive pad s side and even controls of the N-switch of the R1 resistor from the negative pad's side. Each bit stands for different binary segment of the R-DAC. 0000000 (default) Digital monitoring: 1000000b DC monitoring: 0000000b (use default setting) **Power Well:** SUS
6:0	0x7f RW	**DTDRVODDP:** Odd controls of the P-switch of the R1 resistors from the positive pad s side and even controls of the P-switch of the R1 resistor from the negative pad's side. Each bit stands for different binary segment of the R-DAC. 1111111 (default) Digital monitoring: 1111111b DC monitoring: 1111111b (use default setting) **Power Well:** SUS

7.14.43 USB2 TEST GLOBAL REG7 (USB2_TEST_GLOBAL_REG7)—Offset 4012h

Access Method

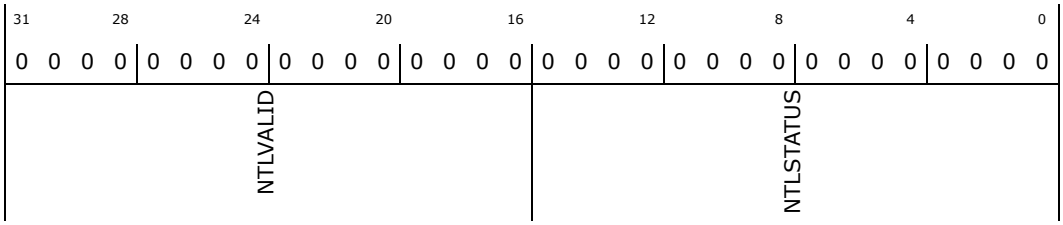
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4012h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**NTLVALID:** NTL status is valid when this is 1. H/W writes, S/W reads. H/W resets this bit to 0 when csr_ntlen=0. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RO	**NTL STATUS (NTLSTATUS):** indicates has leakage issue. H/W writes, S/W reads **Power Well:** SUS

7.14.44 USB2 TEST PERPORT REG1 (USB2_TEST_PERPORT_REG1_PP0)—Offset 4113h

Access Method

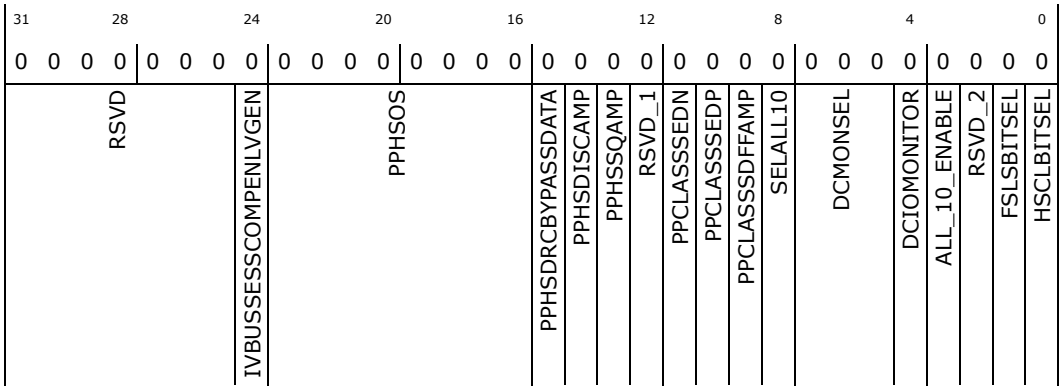
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4113h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS
24	0x0 RW	**ivbussesscompenlvgen (IVBUSSESSCOMPENLVGEN):** To enable vbus sense sampling comparator for DCIO. **Power Well:** SUS
23:16	0x0 RO	**Per-Port HS OS[7:0] (PPHSOS):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. 0: Phase 1 1: Phase 2 7: Phase 8 **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**Per-Port HS DRC Bypassed Data: (PPHSDRCBYPASSDATA):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
14	0x0 RO	**Per-Port HS Disconnect Amp (PPHSDISCAMP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
13	0x0 RO	**Per-Port HS Squelch Amp (PPHSSQAMP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
12	0x0 RO	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
11	0x0 RO	**Per-Port Classic SE Data N (PPCLASSSEDN):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
10	0x0 RO	**Per-Port Classic SE Data P (PPCLASSSEDP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it **Power Well:** SUS
9	0x0 RO	**Per-Port Classic Diff Amp (PPCLASSSDFFAMP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
8	0x0 RW	**SELALL10:** csr_sel10=0 nrziout is driven to 0 csr_sel10=1 nrziout is driven to 1 **Power Well:** SUS
7:5	0x0 RW	**DCMONSEL:** 000 =) dcmon = i_cldiffdata (olaneusblsfsdiffrx) (USB Classic Differential Amp Data Pair) 001 =) dcmon = i_hsdisconnect (olaneusbhsdisconnect) (USB2 Differential Amp Disconnect) 010 =) dcmon = i_hsunsquelch (olaneusbhsunsquelch) (USB2 Differential Amp Squelch) 011 =) dcmon = i_hssample (olaneusbossample) (USB2 High Speed Sample) 100 =) Reserved. 101 =) dcmon= i_clsedataplus (olaneusbsedataprx) (USB Classic Single Ended D+) 110 =) dcmon= i_clsedataminus (olaneusbsedatanrx) (USB Classic Single Ended D-) 111 =) dcmon= i_hsrawdata (olaneusbrdatabp) (USB2 Raw Data) **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**DCIO MONITOR (DCIOMONITOR):** Enable control bit for DCIO monitor signals. If asserted, drivers of the chosen pad will be enabled **Power Well:** SUS
3	0x0 RW	**ALL 10 ENABLE (ALL_10_ENABLE):** All10 test mode enable. If asserted, all10 test mode is enabled. **Power Well:** SUS
2	0x0 RO	**RSVD (RSVD_2):** Reserved. **Power Well:** SUS
1	0x0 RW	**FSLSBITSEL:** fslsbitsel=0 ls is selected fslsbitsel=1 fs is selected **Power Well:** SUS
0	0x0 RW	**HSCLBITSEL:** hsclbitsel=0 classic is selected hsclbitsel=1 hs is selected **Power Well:** SUS

7.14.45 USB2 TEST PERPORT REG1 (USB2_TEST_PERPORT_REG1_PP1)—Offset 4213h

Access Method

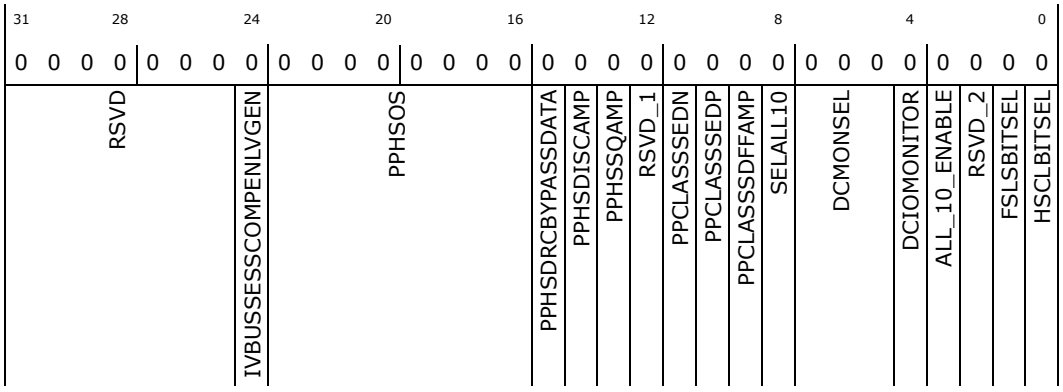
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4213h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS
24	0x0 RW	**ivbussesscompenlvgen (IVBUSSESSCOMPENLVGEN):** To enable vbus sense sampling comparator for DCIO. **Power Well:** SUS
23:16	0x0 RO	**Per-Port HS OS[7:0] (PPHSOS):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. 0: Phase 1 1: Phase 2 7: Phase 8 **Power Well:** SUS
15	0x0 RO	**Per-Port HS DRC Bypassed Data: (PPHSDRCBYPASSDATA):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
14	0x0 RO	**Per-Port HS Disconnect Amp (PPHSDISCAMP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
13	0x0 RO	**Per-Port HS Squelch Amp (PPHSSQAMP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
12	0x0 RO	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
11	0x0 RO	**Per-Port Classic SE Data N (PPCLASSSEDN):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
10	0x0 RO	**Per-Port Classic SE Data P (PPCLASSSEDP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it **Power Well:** SUS
9	0x0 RO	**Per-Port Classic Diff Amp (PPCLASSSDFFAMP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
8	0x0 RW	**SELALL10:** csr_sel10=0 nrziout is driven to 0 csr_sel10=1 nrziout is driven to 1 **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
7:5	0x0 RW	**DCMONSEL:** 000 =) dcmon = i_cldiffdata (olaneusblsfsdiffrx) (USB Classic Differential Amp Data Pair) 001 =) dcmon = i_hsdisconnect (olaneusbhsdisconnect) (USB2 Differential Amp Disconnect) 010 =) dcmon = i_hsunsquelch (olaneusbhsunsquelch) (USB2 Differential Amp Squelch) 011 =) dcmon = i_hssample (olaneusbossample) (USB2 High Speed Sample) 100 =) Reserved. 101 =) dcmon= i_clsedataplus (olaneusbsedataprx) (USB Classic Single Ended D+) 110 =) dcmon= i_clsedataminus (olaneusbsedatanrx) (USB Classic Single Ended D-) 111 =) dcmon= i_hsrawdata (olaneusbrdatabp) (USB2 Raw Data) **Power Well:** SUS
4	0x0 RW	**DCIO MONITOR (DCIOMONITOR):** Enable control bit for DCIO monitor signals. If asserted, drivers of the chosen pad will be enabled **Power Well:** SUS
3	0x0 RW	**ALL 10 ENABLE (ALL_10_ENABLE):** All10 test mode enable. If asserted, all10 test mode is enabled. **Power Well:** SUS
2	0x0 RO	**RSVD (RSVD_2):** Reserved. **Power Well:** SUS
1	0x0 RW	**FSLSBITSEL:** fslsbitsel=0 ls is selected fslsbitsel=1 fs is selected **Power Well:** SUS
0	0x0 RW	**HSCLBITSEL:** hsclbitsel=0 classic is selected hsclbitsel=1 hs is selected **Power Well:** SUS

7.14.46 USB2 TEST PERPORT REG1 (USB2_TEST_PERPORT_REG1_PP2)—Offset 4313h

Access Method

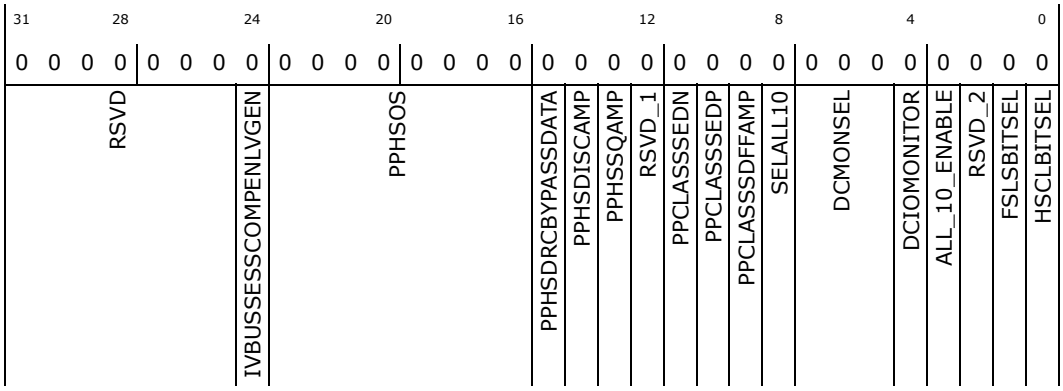
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4313h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS
24	0x0 RW	**ivbussesscompenlvgen (IVBUSSESSCOMPENLVGEN):** To enable vbus sense sampling comparator for DCIO. **Power Well:** SUS
23:16	0x0 RO	**Per-Port HS OS[7:0] (PPHSOS):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. 0: Phase 1 1: Phase 2 7: Phase 8 **Power Well:** SUS
15	0x0 RO	**Per-Port HS DRC Bypassed Data: (PPHSDRCBYPASSDATA):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
14	0x0 RO	**Per-Port HS Disconnect Amp (PPHSDISCAMP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
13	0x0 RO	**Per-Port HS Squelch Amp (PPHSSQAMP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
12	0x0 RO	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
11	0x0 RO	**Per-Port Classic SE Data N (PPCLASSSEDN):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RO	**Per-Port Classic SE Data P (PPCLASSSEDP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it **Power Well:** SUS
9	0x0 RO	**Per-Port Classic Diff Amp (PPCLASSSDFFAMP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
8	0x0 RW	**SELALL10:** csr_sel10=0 nrziout is driven to 0 csr_sel10=1 nrziout is driven to 1 **Power Well:** SUS
7:5	0x0 RW	**DCMONSEL:** 000 =) dcmon = i_cldiffdata (olaneusblsfsdiffrx) (USB Classic Differential Amp Data Pair) 001 =) dcmon = i_hsdisconnect (olaneusbhsdisconnect) (USB2 Differential Amp Disconnect) 010 =) dcmon = i_hsunsquelch (olaneusbhsunsquelch) (USB2 Differential Amp Squelch) 011 =) dcmon = i_hssample (olaneusbossample) (USB2 High Speed Sample) 100 =) Reserved. 101 =) dcmon= i_clsedataplus (olaneusbsedataprx) (USB Classic Single Ended D+) 110 =) dcmon= i_clsedataminus (olaneusbsedatanrx) (USB Classic Single Ended D-) 111 =) dcmon= i_hsrawdata (olaneusbrdatabp) (USB2 Raw Data) **Power Well:** SUS
4	0x0 RW	**DCIO MONITOR (DCIOMONITOR):** Enable control bit for DCIO monitor signals. If asserted, drivers of the chosen pad will be enabled **Power Well:** SUS
3	0x0 RW	**ALL 10 ENABLE (ALL_10_ENABLE):** All10 test mode enable. If asserted, all10 test mode is enabled. **Power Well:** SUS
2	0x0 RO	**RSVD (RSVD_2):** Reserved. **Power Well:** SUS
1	0x0 RW	**FSLSBITSEL:** fslsbitsel=0 ls is selected fslsbitsel=1 fs is selected **Power Well:** SUS
0	0x0 RW	**HSCLBITSEL:** hsclbitsel=0 classic is selected hsclbitsel=1 hs is selected **Power Well:** SUS

7.14.47 USB2 TEST PERPORT REG1 (USB2_TEST_PERPORT_REG1_PP3)—Offset 4413h

Access Method

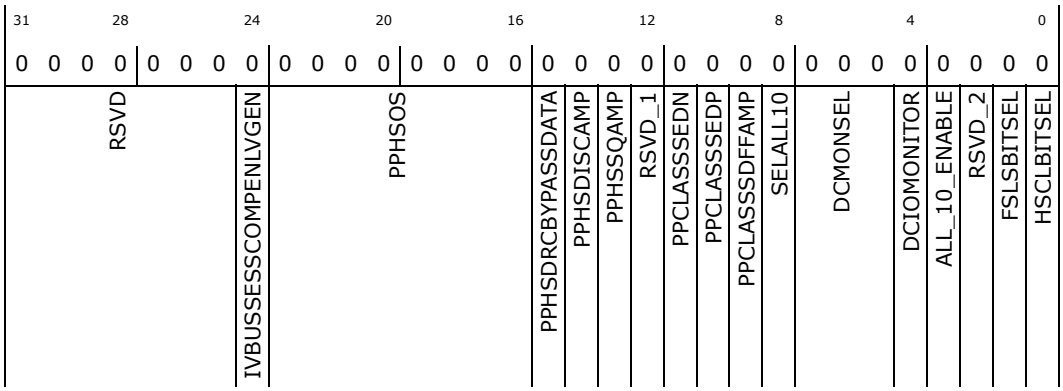
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4413h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS
24	0x0 RW	**ivbussesscompenlvgen (IVBUSSESSCOMPENLVGEN):** To enable vbus sense sampling comparator for DCIO. **Power Well:** SUS
23:16	0x0 RO	**Per-Port HS OS[7:0] (PPHSOS):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. 0: Phase 1 1: Phase 2 7: Phase 8 **Power Well:** SUS
15	0x0 RO	**Per-Port HS DRC Bypassed Data: (PPHSDRCBYPASSDATA):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
14	0x0 RO	**Per-Port HS Disconnect Amp (PPHSDISCAMP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
13	0x0 RO	**Per-Port HS Squelch Amp (PPHSSQAMP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
12	0x0 RO	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
11	0x0 RO	**Per-Port Classic SE Data N (PPCLASSSEDN):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
10	0x0 RO	**Per-Port Classic SE Data P (PPCLASSSEDP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it **Power Well:** SUS
9	0x0 RO	**Per-Port Classic Diff Amp (PPCLASSSDFFAMP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
8	0x0 RW	**SELALL10:** csr_sel10=0 nrziout is driven to 0 csr_sel10=1 nrziout is driven to 1 **Power Well:** SUS
7:5	0x0 RW	**DCMONSEL:** 000 =) dcmon = i_cldiffdata (olaneusblsfsdiffrx) (USB Classic Differential Amp Data Pair) 001 =) dcmon = i_hsdisconnect (olaneusbhsdisconnect) (USB2 Differential Amp Disconnect) 010 =) dcmon = i_hsunsquelch (olaneusbhsunsquelch) (USB2 Differential Amp Squelch) 011 =) dcmon = i_hssample (olaneusbossample) (USB2 High Speed Sample) 100 =) Reserved. 101 =) dcmon= i_clsedataplus (olaneusbsedataprx) (USB Classic Single Ended D+) 110 =) dcmon= i_clsedataminus (olaneusbsedatanrx) (USB Classic Single Ended D-) 111 =) dcmon= i_hsrawdata (olaneusbrdatabp) (USB2 Raw Data) **Power Well:** SUS
4	0x0 RW	**DCIO MONITOR (DCIOMONITOR):** Enable control bit for DCIO monitor signals. If asserted, drivers of the chosen pad will be enabled **Power Well:** SUS
3	0x0 RW	**ALL 10 ENABLE (ALL_10_ENABLE):** All10 test mode enable. If asserted, all10 test mode is enabled. **Power Well:** SUS
2	0x0 RO	**RSVD (RSVD_2):** Reserved. **Power Well:** SUS
1	0x0 RW	**FSLSBITSEL:** fslsbitsel=0 ls is selected fslsbitsel=1 fs is selected **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**HSCLBITSEL:** hsclbitsel=0 classic is selected hsclbitsel=1 hs is selected **Power Well:** SUS

7.14.48 USB2 TEST PERPORT REG1 (USB2_TEST_PERPORT_REG1_PP4)—Offset 4513h

Access Method

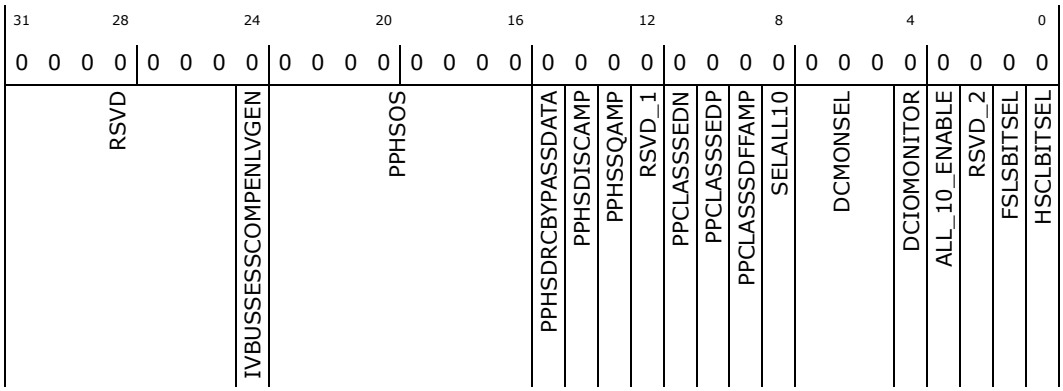
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4513h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS
24	0x0 RW	**ivbussesscompenlvgen (IVBUSSESSCOMPENLVGEN):** To enable vbus sense sampling comparator for DCIO. **Power Well:** SUS
23:16	0x0 RO	**Per-Port HS OS[7:0] (PPHSOS):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. 0: Phase 1 1: Phase 2 7: Phase 8 **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**Per-Port HS DRC Bypassed Data: (PPHSDRCBYPASSDATA):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
14	0x0 RO	**Per-Port HS Disconnect Amp (PPHSDISCAMP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
13	0x0 RO	**Per-Port HS Squelch Amp (PPHSSQAMP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
12	0x0 RO	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
11	0x0 RO	**Per-Port Classic SE Data N (PPCLASSSEDN):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
10	0x0 RO	**Per-Port Classic SE Data P (PPCLASSSEDP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it **Power Well:** SUS
9	0x0 RO	**Per-Port Classic Diff Amp (PPCLASSSDFFAMP):** bit is set, the last value from this amp is re-circulated to allow test SW to reliably read it. **Power Well:** SUS
8	0x0 RW	**SELALL10:** csr_sel10=0 nrziout is driven to 0 csr_sel10=1 nrziout is driven to 1 **Power Well:** SUS
7:5	0x0 RW	**DCMONSEL:** 000 =) dcmon = i_cldiffdata (olaneusblsfsdiffrx) (USB Classic Differential Amp Data Pair) 001 =) dcmon = i_hsdisconnect (olaneusbhsdisconnect) (USB2 Differential Amp Disconnect) 010 =) dcmon = i_hsunsquelch (olaneusbhsunsquelch) (USB2 Differential Amp Squelch) 011 =) dcmon = i_hssample (olaneusbossample) (USB2 High Speed Sample) 100 =) Reserved. 101 =) dcmon= i_clsedataplus (olaneusbsedataprx) (USB Classic Single Ended D+) 110 =) dcmon= i_clsedataminus (olaneusbsedatanrx) (USB Classic Single Ended D-) 111 =) dcmon= i_hsrawdata (olaneusbrdatabp) (USB2 Raw Data) **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**DCIO MONITOR (DCIOMONITOR):** Enable control bit for DCIO monitor signals. If asserted, drivers of the chosen pad will be enabled **Power Well:** SUS
3	0x0 RW	**ALL 10 ENABLE (ALL_10_ENABLE):** All10 test mode enable. If asserted, all10 test mode is enabled. **Power Well:** SUS
2	0x0 RO	**RSVD (RSVD_2):** Reserved. **Power Well:** SUS
1	0x0 RW	**FSLSBITSEL:** fslsbitsel=0 ls is selected fslsbitsel=1 fs is selected **Power Well:** SUS
0	0x0 RW	**HSCLBITSEL:** hsclbitsel=0 classic is selected hsclbitsel=1 hs is selected **Power Well:** SUS

7.14.49 USB2 COMPBG2 (USB2_COMPBG2)—Offset 7F14h

Access Method

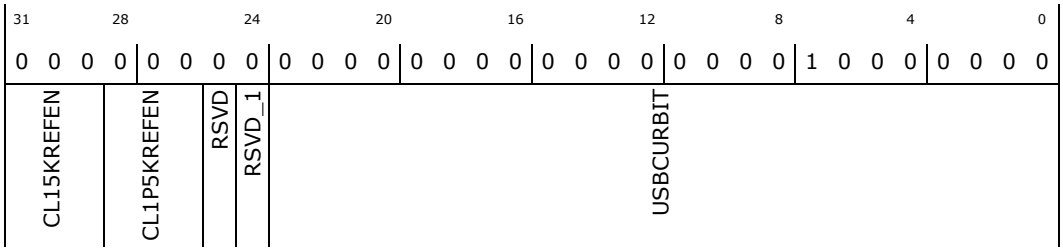
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 7F14h

Op Codes:

h - Read, h - Write

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CL15KREFEN:** CL15k Pull-Down Rcal reference voltage (525mV625mV) select signal to select reference voltage to AFE global icomp. Cl15krefen2 cl15klrefen1 cl15krefen0 1 1 1 575mV 1 1 0 562.5mV 1 0 1 550mV 1 0 0 537.5mV 0 1 1 512.5mV 0 1 0 500mV 0 0 1 475mV 0 0 0 525mV (default) For CL 45ohm Pull-Up reference voltage (825mV) programability signals. 3'b000 = 0.825 3'b001 = 0.7875 3'b010 = 0.8 3'b011 = 0.8125 3'b100 = 0.8375 3'b101 = 0.85 3'b110 = 0.8625 3'b111 = 0.875 **Power Well:** SUS
28:26	0x0 RW	**CL1P5KREFEN:** Device mode 1.5k Pull-Up Rcal reference voltage (500mV) select signal to select reference voltage to AFE global 1.5k rcomp. Cl1p5krefen2 cl1p5klrefen1 cl1p5krefen0 1 1 1 537.5mV 1 1 0 525mV 1 0 1 512.5mV 1 0 0 487.5mV 0 1 1 475mV 0 1 0 450mV 0 0 1 425mV 0 0 0 500mV (default) **Power Well:** SUS
25	0x0 RW	**RSVD:** RSVD The purpose of this implementation is to enable selection between low/high codes when the CL 15K rcomp code is dithering. The comp_sel table is as below: comp_sel RCOMP bit Description 0 Low high resistance(default) 1 High low resistance **Power Well:** SUS
24	0x0 RW	**RSVD (RSVD_1):** RSVD The purpose of this implementation is to enable selection between low/high codes when the CL 1.5K rcomp code is dithering. The comp_sel table is as below: comp_sel RCOMP bit Description 0 Low high resistance(default) 1 High low resistance **Power Well:** SUS
23:0	0x80 RO/V	**USBCURBIT:** Global ICOMP bits coming from the core logic to set the current source. This register is hard coded, These bits are thermometer coded **Power Well:** SUS

7.14.50 USB2 VISA PERPORT REG1 (USB2_VISA_PERPORT_REG1_PP0)—Offset 4115h

Access Method

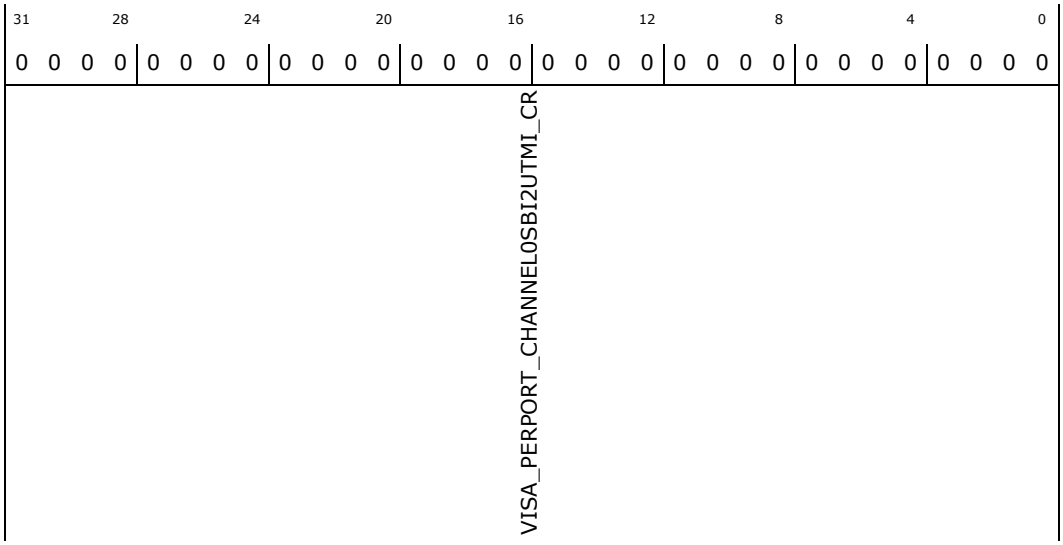
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4115h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VISA_PERPORT_CHANNEL0SBI2UTMI_CR:** Lane 0 Data Select 16 - byp 15:8 - clk select 7:0 - lane select **Power Well:** SUS

7.14.51 USB2 VISA PERPORT REG2 (USB2_VISA_PERPORT_REG2_PP0)—Offset 4116h

Access Method

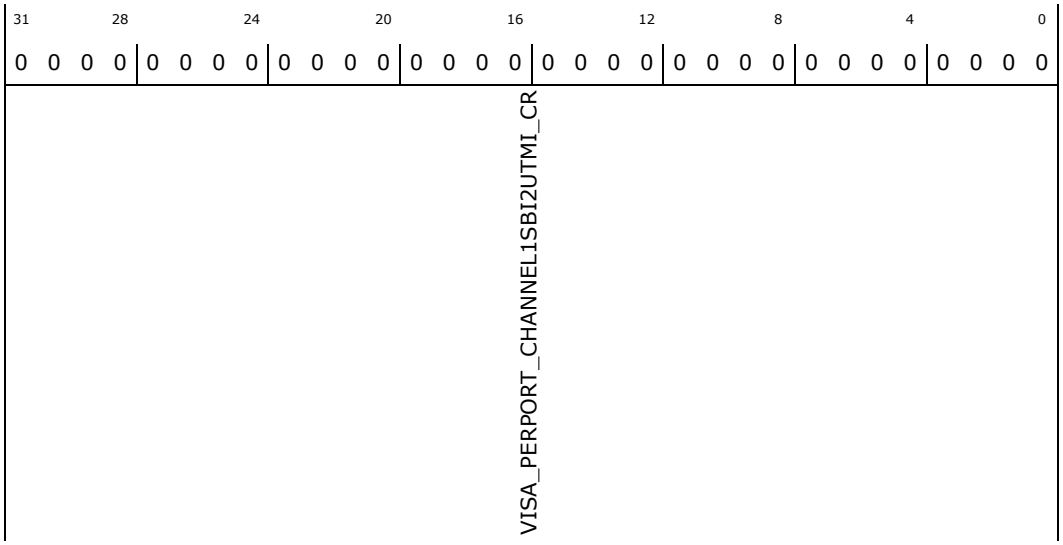
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4116h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VISA_PERPORT_CHANNEL1SBI2UTMI_CR:** Lane 1 Data Select 16 - byp 15:8 - clk select 7:0 - lane select **Power Well:** SUS

7.14.52 USB2 VISA PERPORT REG3 (USB2_VISA_PERPORT_REG3_PP0)—Offset 4117h

Access Method

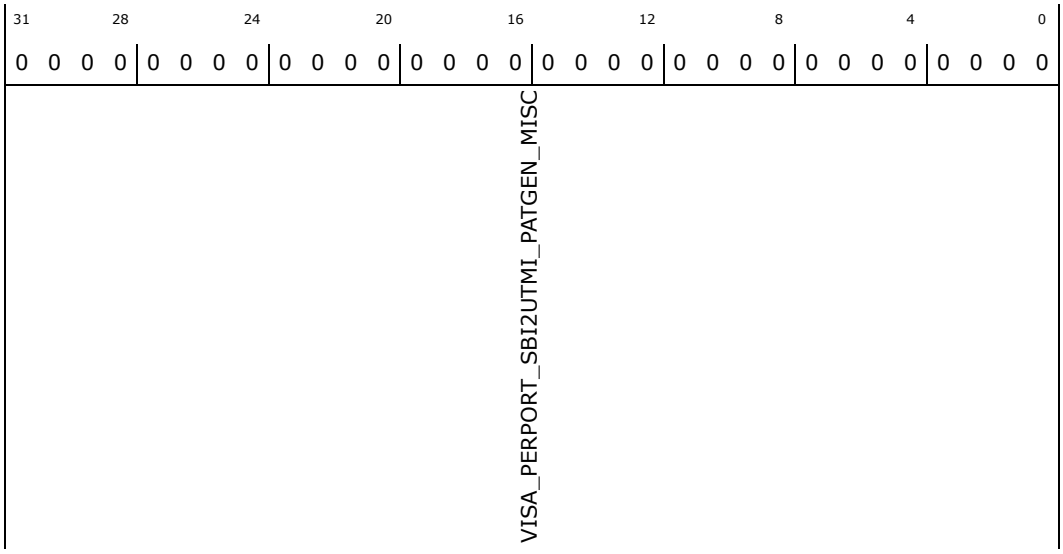
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4117h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VISA_PERPORT_SBI2UTMI_PATGEN_MISC:** Visa PatGen and Misc 15:8 - Pat0(Advanced only) 6:4 - PG mode 3 - t_o 0 - ven **Power Well:** SUS

7.14.53 USB2 VISA PERPORT REG1 (USB2_VISA_PERPORT_REG1_PP1)—Offset 4215h

Access Method

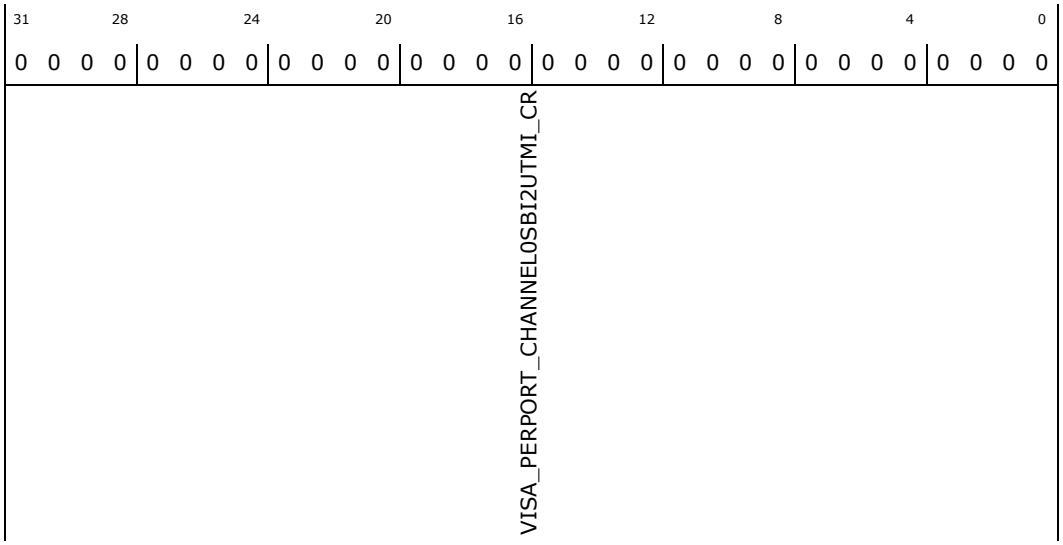
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4215h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VISA_PERPORT_CHANNEL0SBI2UTMI_CR:** Lane 0 Data Select 16 - byp 15:8 - clk select 7:0 - lane select **Power Well:** SUS

7.14.54 USB2 VISA PERPORT REG2 (USB2_VISA_PERPORT_REG2_PP1)—Offset 4216h

Access Method

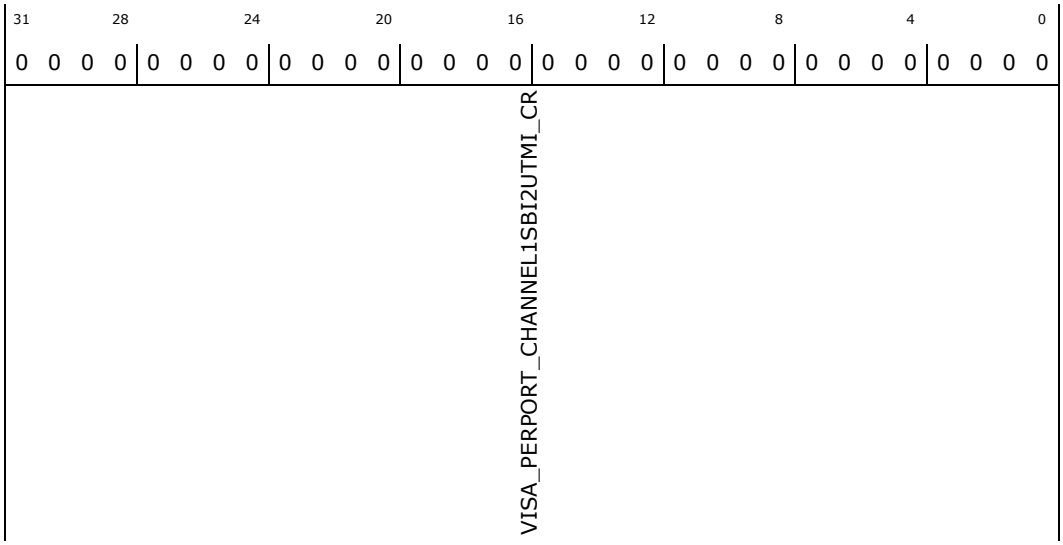
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4216h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VISA_PERPORT_CHANNEL1SBI2UTMI_CR:** Lane 1 Data Select 16 - byp 15:8 - clk select 7:0 - lane select **Power Well:** SUS

7.14.55 USB2 VISA PERPORT REG3 (USB2_VISA_PERPORT_REG3_PP1)—Offset 4217h

Access Method

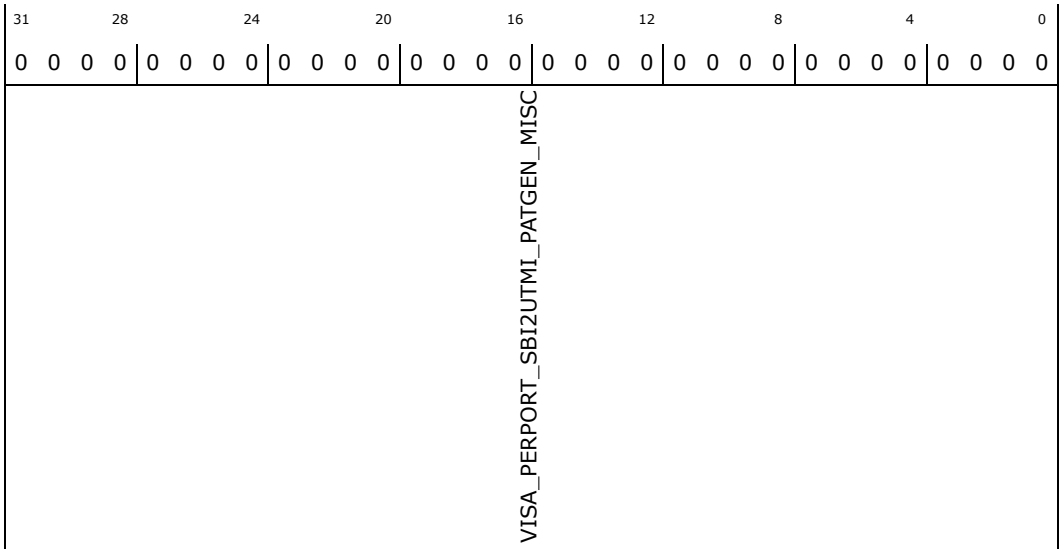
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4217h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VISA_PERPORT_SBI2UTMI_PATGEN_MISC:** Visa PatGen and Misc 15:8 - Pat0(Advanced only) 6:4 - PG mode 3 - t_o 0 - ven **Power Well:** SUS

7.14.56 USB2 VISA PERPORT REG1 (USB2_VISA_PERPORT_REG1_PP2)—Offset 4315h

Access Method

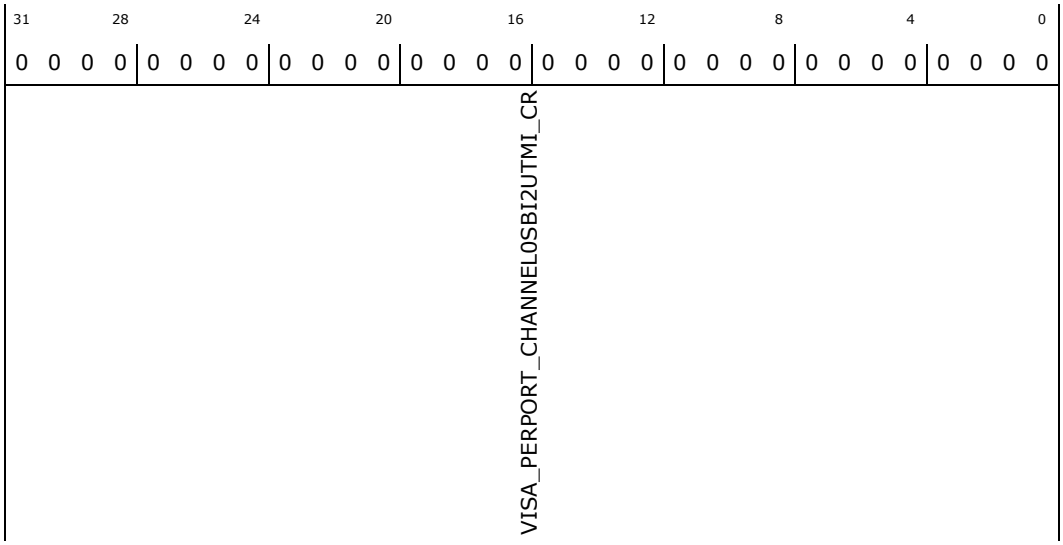
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4315h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VISA_PERPORT_CHANNEL0SBI2UTMI_CR:** Lane 0 Data Select 16 - byp 15:8 - clk select 7:0 - lane select **Power Well:** SUS

7.14.57 USB2 VISA PERPORT REG2 (USB2_VISA_PERPORT_REG2_PP2)—Offset 4316h

Access Method

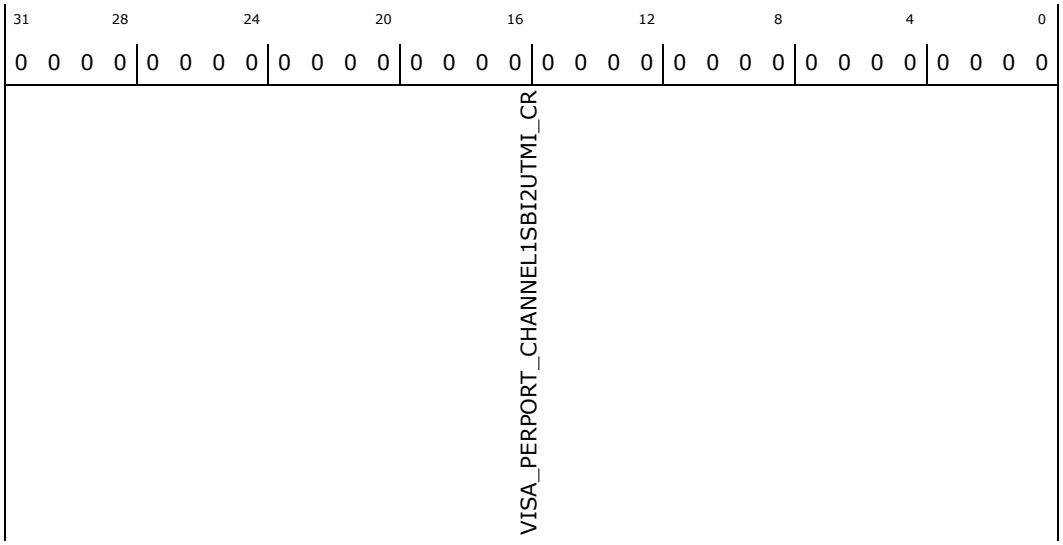
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4316h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VISA_PERPORT_CHANNEL1SBI2UTMI_CR:** Lane 1 Data Select 16 - byp 15:8 - clk select 7:0 - lane select **Power Well:** SUS

7.14.58 USB2 VISA PERPORT REG3 (USB2_VISA_PERPORT_REG3_PP2)—Offset 4317h

Access Method

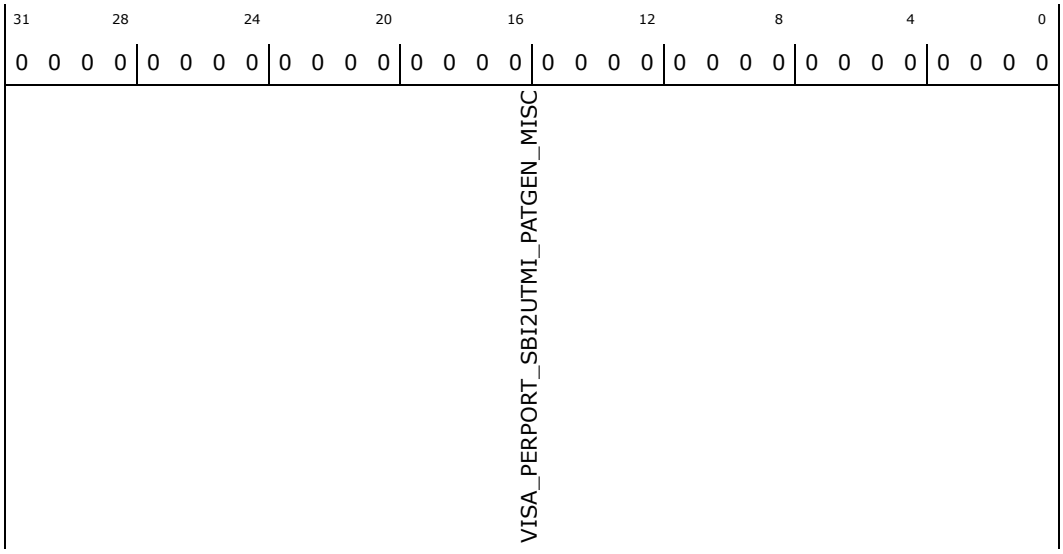
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4317h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VISA_PERPORT_SBI2UTMI_PATGEN_MISC:** Visa PatGen and Misc 15:8 - Pat0(Advanced only) 6:4 - PG mode 3 - t_o 0 - ven **Power Well:** SUS

7.14.59 USB2 VISA PERPORT REG1 (USB2_VISA_PERPORT_REG1_PP3)—Offset 4415h

Access Method

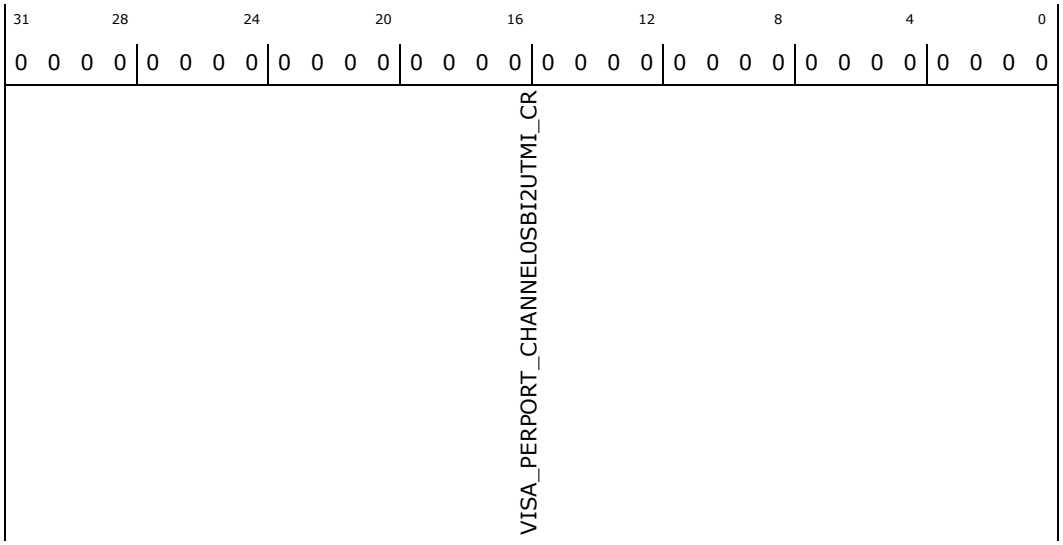
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4415h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VISA_PERPORT_CHANNEL0SBI2UTMI_CR:** Lane 0 Data Select 16 - byp 15:8 - clk select 7:0 - lane select **Power Well:** SUS

7.14.60 USB2 VISA PERPORT REG2 (USB2_VISA_PERPORT_REG2_PP3)—Offset 4416h

Access Method

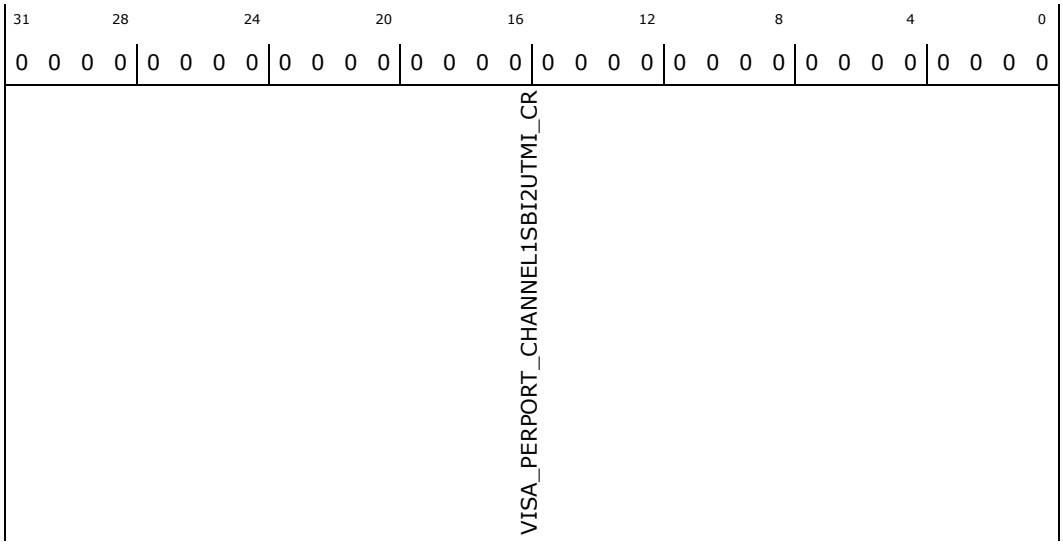
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4416h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VISA_PERPORT_CHANNEL1SBI2UTMI_CR:** Lane 1 Data Select 16 - byp 15:8 - clk select 7:0 - lane select **Power Well:** SUS

7.14.61 USB2 VISA PERPORT REG3 (USB2_VISA_PERPORT_REG3_PP3)—Offset 4417h

Access Method

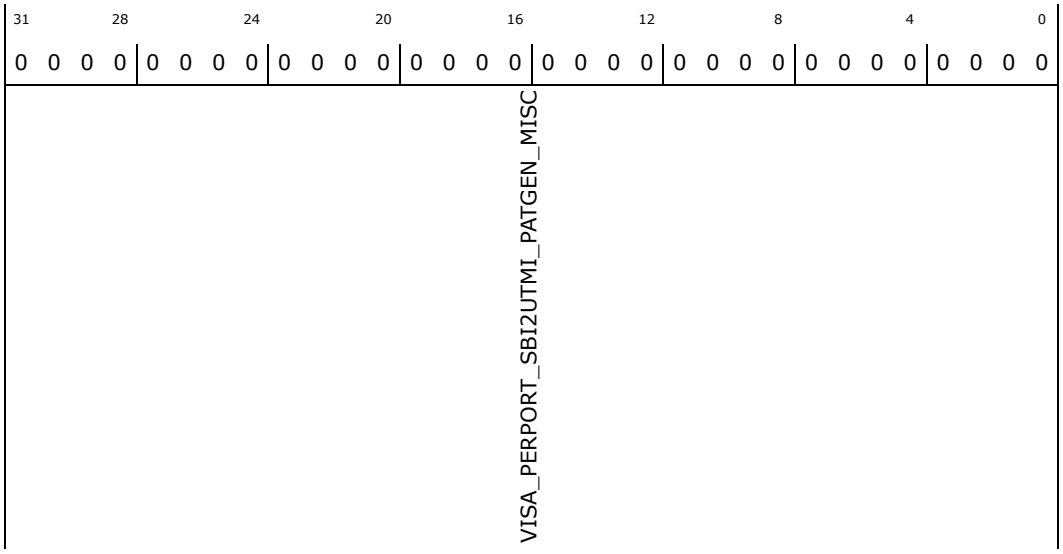
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4417h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VISA_PERPORT_SBI2UTMI_PATGEN_MISC:** Visa PatGen and Misc 15:8 - Pat0(Advanced only) 6:4 - PG mode 3 - t_o 0 - ven **Power Well:** SUS

7.14.62 USB2 VISA PERPORT REG1 (USB2_VISA_PERPORT_REG1_PP4)—Offset 4515h

Access Method

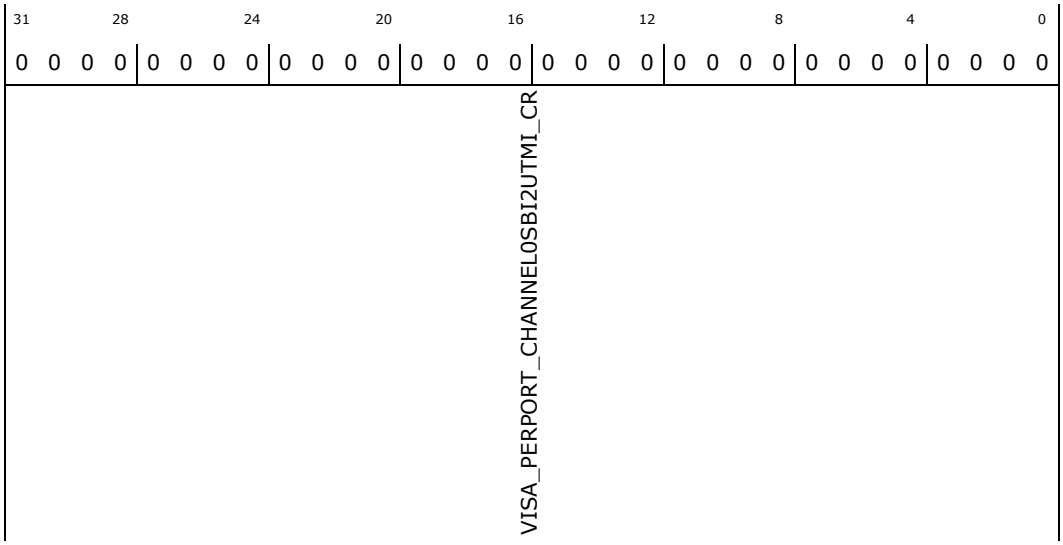
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4515h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VISA_PERPORT_CHANNEL0SBI2UTMI_CR:** Lane 0 Data Select 16 - byp 15:8 - clk select 7:0 - lane select **Power Well:** SUS

7.14.63 USB2 VISA PERPORT REG2 (USB2_VISA_PERPORT_REG2_PP4)—Offset 4516h

Access Method

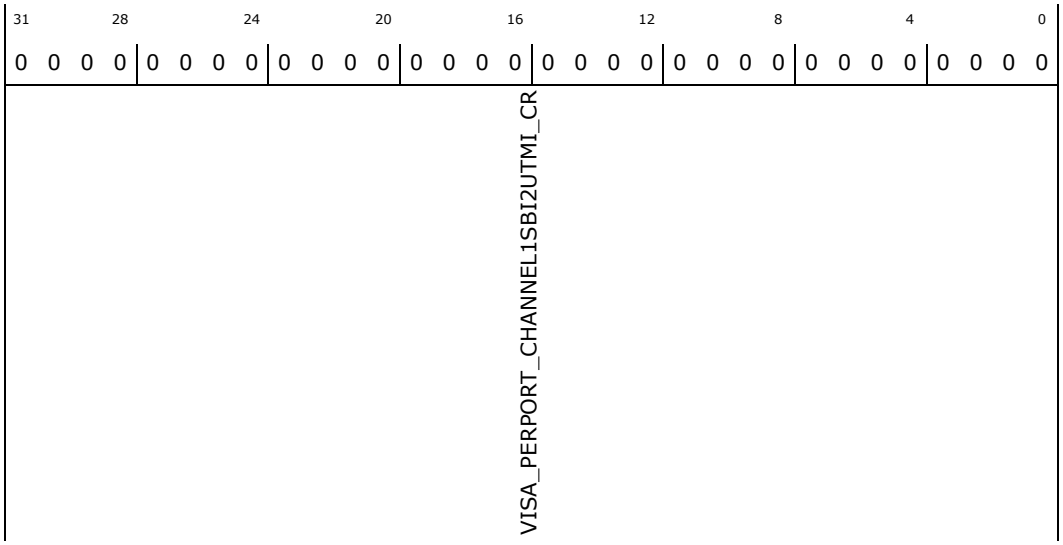
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4516h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VISA_PERPORT_CHANNEL1SBI2UTMI_CR:** Lane 1 Data Select 16 - byp 15:8 - clk select 7:0 - lane select **Power Well:** SUS

7.14.64 USB2 VISA PERPORT REG3 (USB2_VISA_PERPORT_REG3_PP4)—Offset 4517h

Access Method

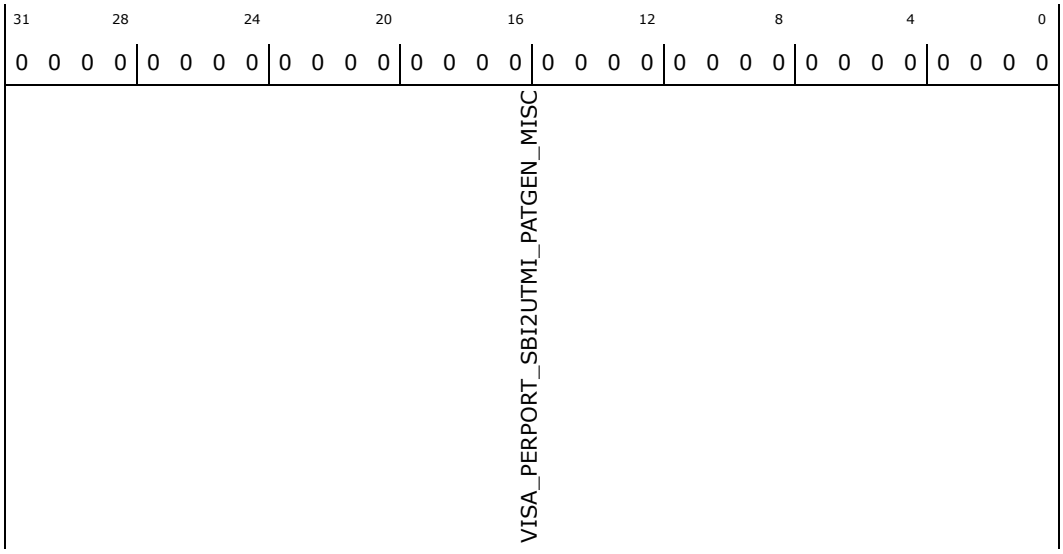
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4517h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VISA_PERPORT_SBI2UTMI_PATGEN_MISC:** Visa PatGen and Misc 15:8 - Pat0(Advanced only) 6:4 - PG mode 3 - t_o 0 - ven **Power Well:** SUS

7.14.65 USB2 VISA GLOBAL REG1 (USB2_VISA_GLOBAL_REG1)—Offset 4018h

Access Method

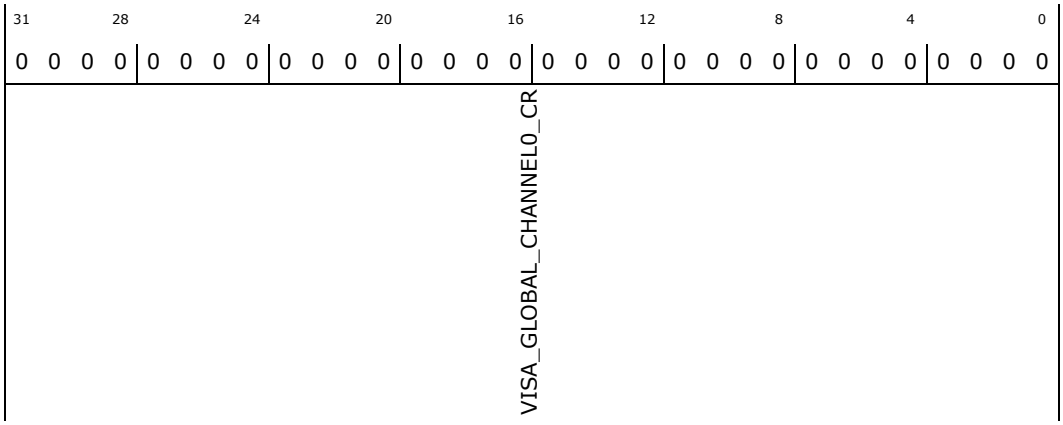
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4018h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VISA_GLOBAL_CHANNEL0_CR:** Lane 0 Data Select 16 - byp 15:8 - clk select 7:0 - lane select **Power Well:** SUS

7.14.66 USB2 VISA GLOBAL REG2 (USB2_VISA_GLOBAL_REG2)—Offset 4019h

Access Method

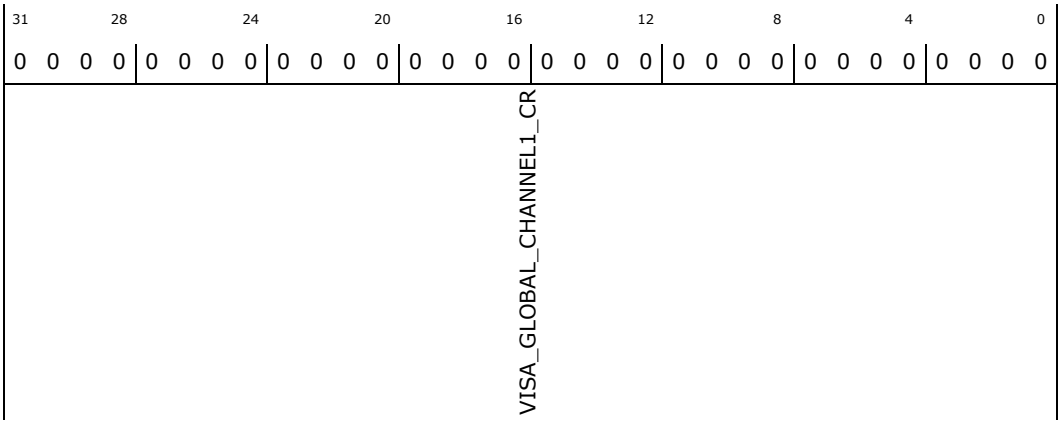
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4019h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VISA_GLOBAL_CHANNEL1_CR:** Lane 1 Data Select 16 - byp 15:8 - clk select 7:0 - lane select **Power Well:** SUS

7.14.67 USB2 VISA GLOBAL REG3 (USB2_VISA_GLOBAL_REG3)—Offset 401Ah

Access Method

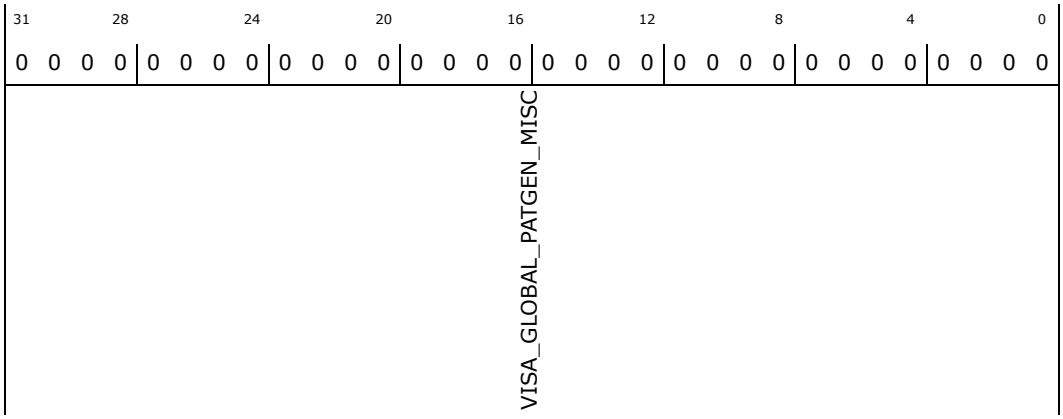
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 401Ah

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**VISA_GLOBAL_PATGEN_MISC:** Visa PatGen and Misc 15:8 - Pat0(Advanced only) 6:4 - PG mode 3 - t_o 0 - ven **Power Well:** SUS

7.14.68 USB2 SQ DPDM OFFSET PERPORT REG (USB2_SQ_DPDM_OFFSET_PERPORT_REG_PP0)—Offset 411Bh

Access Method

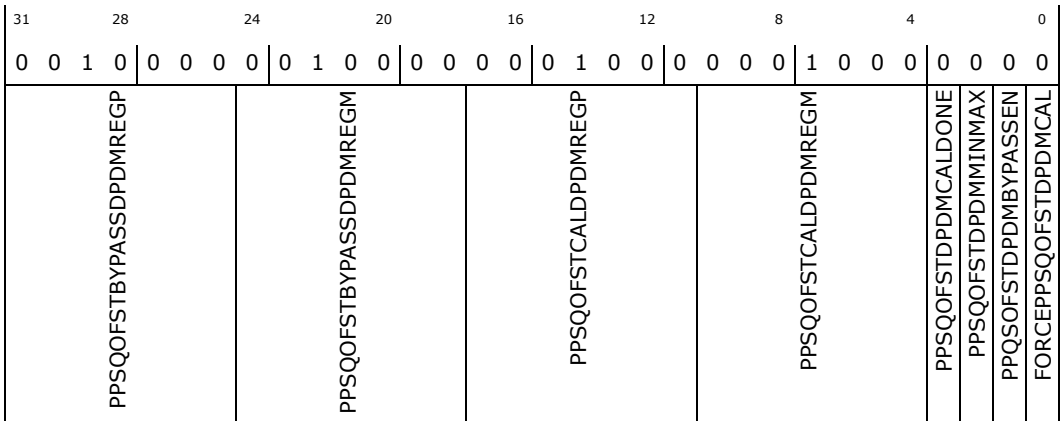
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 411Bh

Op Codes:

h - Read, h - Write

Default: 20404080h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x10 RW	**PPSQOFSTBYPASSDPDMREGP:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldpdmregp(6:0) will be overwritten by this register when ppsqofstDPDMBYPASSEN is asserted 1 . **Power Well:** SUS
24:18	0x10 RW	**PPSQOFSTBYPASSDPDMREGM:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldpdmregm(6:0)will be overwritten by this register when ppsqofstDPDMBYPASSEN is asserted 1 . **Power Well:** SUS
17:11	0x8 RO	**PPSQOFSTCALDPDMREGP:** 7-bit register that stores the DpDm squelch detector offset cancellation Dm-side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDPDMCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to ppsqofstcaldpdmregM. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTDPDMCAL asserted: regP count up regM countdown regP count up until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTDPDMCAL asserted: regP countdown regM count up regP countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1269.8. **Power Well:** SUS
10:4	0x8 RO	**PPSQOFSTCALDPDMREGM:** 7-bit register that stores the DpDm squelch detector offset cancellation Dp side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDPDMCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to ppsqofstcaldpdmregP. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTDPDMCAL asserted: regP count up regM countdown regP count up until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTDPDMCAL asserted: regP countdown regM count up regP countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1269.8. **Power Well:** SUS
3	0x0 RO	**PPSQOFSTDPDMCALDONE:** This bit is set to 1b by state machine to indicate the calibration completion. This bit need to be cleared when FORCEppsqofstDPDMcal (starting of next calibration cycle). **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW/1C	**PPSQOFSTDPDMMINMAX:** Flag bit when ppsqofstcaldpdmregP OR ppsqofstcaldpdmregM offset counter reach the max range. The max range high limit is set by USBSQOFSTDPDMMAXLIMIT and low limit is always 0000000b. For P1269.8 is when it reaches 0011111b or 0000000b. This is to prevent roll back when the variation is out of range. This bit is to be cleared by software. **Power Well:** SUS
1	0x0 RW	**PPQSOFSTDPDMBYPASSEN:** Software programmable. The values of ilane13:0usbppsqofstcaldpdmregp(6:0) and ilane13:0usbppsqofstcaldpdmregm(6:0) will be overwritten by ppsqofstbypassdpdmregp and ppsqofstbypassdpdmregm respectively when this bit assert 1b . **Power Well:** SUS
0	0x0 WO	**DpDm SQ Offset Calibration Enable Signal (FORCEPPSQOFSTDPDMCAL):** When set to 1b, this will force per-port squelch offset cancellation Finite State Machine to start calibrating. State Machine need to ensure only either DpDm or DmDp SQ detector is enabled for calibration at each time. BIOS have to wait for sufficient time for the calibration complete. This is a pulse trigger event. **Power Well:** SUS

7.14.69 USB2 SQ DMDP OFFSET PERPORT REG (USB2_SQ_DMDP_OFFSET_PERPORT_REG_PP0)—Offset 411Ch

Access Method

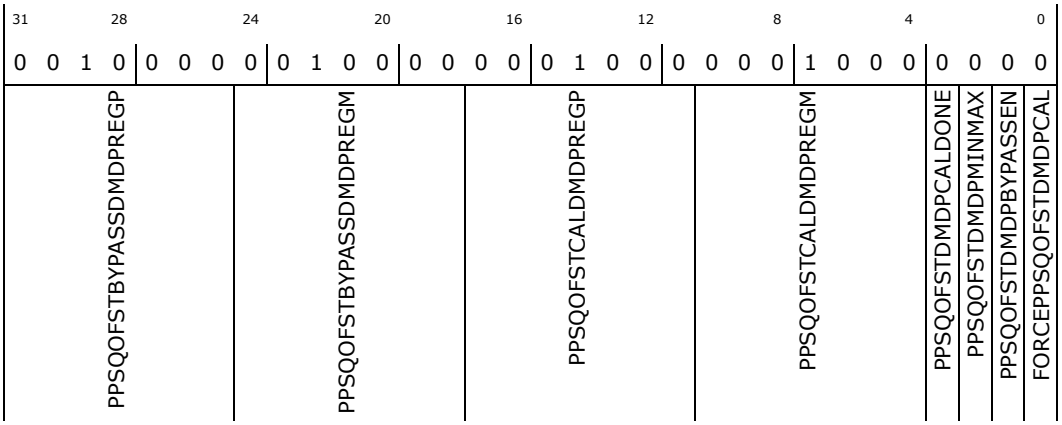
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 411Ch

Op Codes:

h - Read, h - Write

Default: 20404080h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x10 RW	**PPSQOFSTBYPASSDMDPREGP:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldmdpregp(6:0) will be overwritten by this register when ppsqofstDMDPBYPASSEN is asserted 1 . **Power Well:** SUS
24:18	0x10 RW	**PPSQOFSTBYPASSDMDPREGM:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldmdpregm(6:0)will be overwritten by this register when ppsqofstDMDPBYPASSEN is asserted 1 . **Power Well:** SUS
17:11	0x8 RO	**PPSQOFSTCALDMDPREGP:** 7-bit register that stores the DmDp squelch detector offset cancellation Dp side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDMDPCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to PPSQOFSTCALDMDPREGM. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTCALDPDMEN asserted: regP count down regM count up regP count down until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTCALDPDMEN asserted: regM countdown regP count up regM countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1271. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
10:4	0x8 RO	**PPSQOFSTCALDMDPREGM:** 7-bit register that stores the DpDm squelch detector offset cancellation Dp side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDPDMCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to PPSQOFSTCALDPDMREGP. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTDPDMCAL asserted: regP count down regM count up regP count down until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTDPDMCAL asserted: regM countdown regP count up regM countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1271. **Power Well:** SUS
3	0x0 RO	**PPSQOFSTDMDPCALDONE:** This bit is set to 1b by state machine to indicate the calibration completion. This bit need to be cleared when FORCEppsqofstDMDPcal (starting of next calibration cycle). **Power Well:** SUS
2	0x0 RW/1C	**PPSQOFSTDMDPMINMAX:** Flag bit when PPSQOFSTCALDPDMREGP OR PPSQOFSTCALDPDMREGM offset counter reach the max range. The max range high limit is set by USBSQOFSTDPDMMAXLIMIT and low limit is always 0000000b. For P1271 is when it reaches 0011111b or 0000000b. This is to prevent roll back when the variation is out of range. This bit is to be cleared by software. **Power Well:** SUS
1	0x0 RW	**PPSQOFSTDMDPBYPASSEN:** Software programmable. The values of ilane13:0usbppsqofstcaldmdpregm(6:0) and ilane13:0usbppsqofstcaldmdpregp(6:0) will be overwritten by ppsqofstbypassdmdpregm and ppsqofstbypassdmdpregp respectively when this bit assert 1b . **Power Well:** SUS
0	0x0 WO	**DmDp SQ Offset Calibration Enable Signal (FORCEPPSQOFSTDMDPCAL):** When set to 1b, this will force per-port squelch offset cancellation Finite State Machine to start calibrating. State Machine need to ensure only either DmDp or DmDp SQ detector is enabled for calibration at each time. BIOS have to wait for sufficient time for the calibration complete. This is a pulse trigger event. **Power Well:** SUS

7.14.70 USB2 DIS OFFSET PERPORT REG (USB2_DIS_OFFSET_PERPORT_REG_PP0)—Offset 411Dh

Access Method

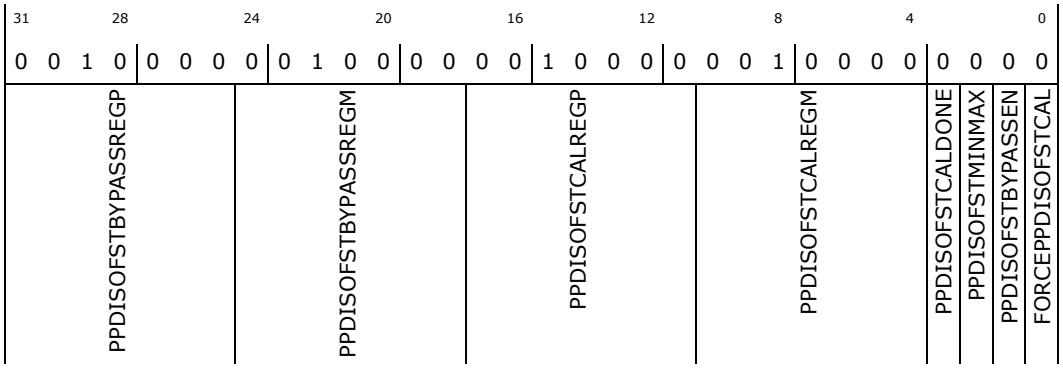
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 411Dh

Op Codes:

h - Read, h - Write

Default: 20408100h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x10 RW	**PPDISOFSTBYPASSREGP:** Software programmable. It is used during test mode. The values of ilane13:0usbppDISofstcalregp(6:0) will be overwritten by this register when ppDISofstbypassen is asserted 1 . **Power Well:** SUS
24:18	0x10 RW	**PPDISOFSTBYPASSREGM:** Software programmable. It is used during test mode. The values of ilane13:0usbppdisofstcalregm(6:0) will be overwritten by this register when ppDISofstbypassen is asserted 1 . **Power Well:** SUS
17:11	0x10 RO	**PPDISOFSTCALREGP:** 7-bit register that stores the disconnect detector offset cancellation left-side code. This 7-bit register must be initialized to default value prior to every calibration routine (before PPDISOFSTCALEN asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to right-register. This is to reduce the signal common mode variation to impact to circuit performance. If hsdisconnect output is low when FORCEPPDISOFSTCAL asserted: regP count down regM count up regP count down until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If hsdisconnect output is high when FORCEPPDISOFSTCAL asserted: regM countdown regP count up regM countdown until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 7:6 are unused for P1271. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
10:4	0x10 RO	**PPDISOFSTCALREGM:** 7-bit register that stores the disconnect detector offset cancellation right-side code. This 7-bit register must be initialized to default value prior to every calibration routine (before PPDISOFSTCALEN asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to left-register. This is to reduce the signal common mode variation to impact to circuit performance. If hsdisconnect output is low when FORCEPPDISOFSTCAL asserted: regP count down regM count up regP count down until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If hsdisconnect output is high when FORCEPPDISOFSTCAL asserted: regM countdown regP count up regM countdown until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1271. **Power Well:** SUS
3	0x0 RO	**PPDISOFSTCALDONE:** This bit is set to 1b by state machine to indicate the calibration completion. This bit need to be cleared when FORCEPPDISofstcal (starting of next calibration cycle). **Power Well:** SUS
2	0x0 RW/1C	**PPDISOFSTMINMAX:** Flag bit when ppDISofstcalregp OR ppDISofstcalregm offset counter reach the max limit set by the product. For P1269.8 is when it reaches 0001111b or 0000000b. This is to prevent roll back when the variation is out of range. **Power Well:** SUS
1	0x0 RW	**PPDISOFSTBYPASSEN:** Software programmable. The values of ilane13:0usbppDISofstcalregp(6:0) and ilane13:0usbppDISofstcalregm(6:0) will be overwritten by ppDISofstbypassregp and ppDISofstbypassregm respectively when ppDISofstbypassen is asserted 1 . **Power Well:** SUS
0	0x0 WO	**FORCEPPDISOFSTCAL:** When set to 1b, this will force per-port disconnect offset cancellation Finite State Machine to start calibrating. BIOS has to wait for sufficient time for the calibration complete. **Power Well:** SUS

7.14.71 USB2 SQ DPDM OFFSET PERPORT REG (USB2_SQ_DPDM_OFFSET_PERPORT_REG_PP1)—Offset 421Bh

Access Method

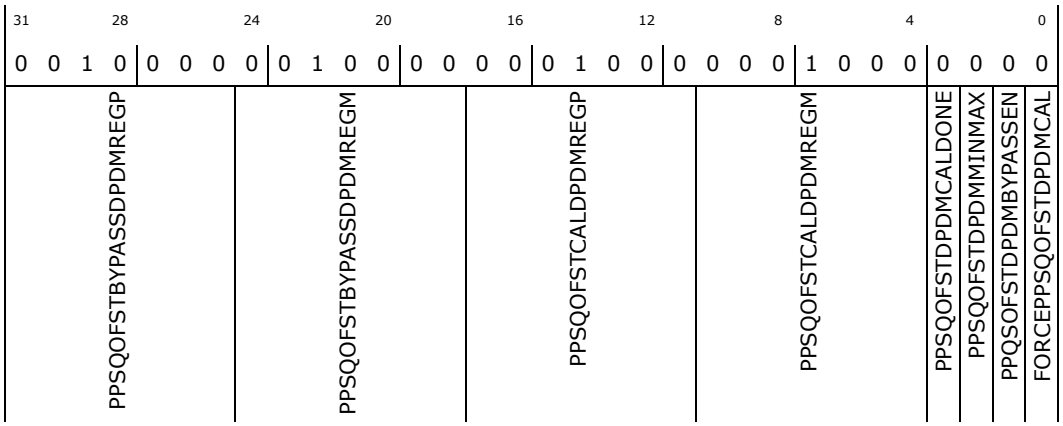
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 421Bh

Op Codes:

h - Read, h - Write

Default: 20404080h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x10 RW	**PPSQOFSTBYPASSDPDMREGP:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldpdmregp(6:0) will be overwritten by this register when ppsqofstDPDMBYPASSEN is asserted 1 . **Power Well:** SUS
24:18	0x10 RW	**PPSQOFSTBYPASSDPDMREGM:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldpdmregm(6:0)will be overwritten by this register when ppsqofstDPDMBYPASSEN is asserted 1 . **Power Well:** SUS
17:11	0x8 RO	**PPSQOFSTCALDPDMREGP:** 7-bit register that stores the DpDm squelch detector offset cancellation Dm-side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDPDMCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to ppsqofstcaldpdmregM. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTDPDMCAL asserted: regP count up regM countdown regP count up until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTDPDMCAL asserted: regP countdown regM count up regP countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1269.8. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
10:4	0x8 RO	**PPSQOFSTCALDPDMREGM:** 7-bit register that stores the DpDm squelch detector offset cancellation Dp side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDPDMCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to ppsqofstcaldpdmregP. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTDPDMCAL asserted: regP count up regM countdown regP count up until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTDPDMCAL asserted: regP countdown regM count up regP countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1269.8. **Power Well:** SUS
3	0x0 RO	**PPSQOFSTDPDMCALDONE:** This bit is set to 1b by state machine to indicate the calibration completion. This bit need to be cleared when FORCEppsqofstDPDMcal (starting of next calibration cycle). **Power Well:** SUS
2	0x0 RW/1C	**PPSQOFSTDPDMMINMAX:** Flag bit when ppsqofstcaldpdmregP OR ppsqofstcaldpdmregM offset counter reach the max range. The max range high limit is set by USBSQOFSTDPDMMAXLIMIT and low limit is always 0000000b. For P1269.8 is when it reaches 0011111b or 0000000b. This is to prevent roll back when the variation is out of range. This bit is to be cleared by software. **Power Well:** SUS
1	0x0 RW	**PPQSOFSTDPDMBYPASSEN:** Software programmable. The values of ilane13:0usbppsqofstcaldpdmregp(6:0) and ilane13:0usbppsqofstcaldpdmregm(6:0) will be overwritten by ppsqofstbypassdpdmregp and ppsqofstbypassdpdmregm respectively when this bit assert 1b . **Power Well:** SUS
0	0x0 WO	**DpDm SQ Offset Calibration Enable Signal (FORCEPPSQOFSTDPDMCAL):** When set to 1b, this will force per-port squelch offset cancellation Finite State Machine to start calibrating. State Machine need to ensure only either DpDm or DmDp SQ detector is enabled for calibration at each time. BIOS have to wait for sufficient time for the calibration complete. This is a pulse trigger event. **Power Well:** SUS

7.14.72 USB2 SQ DMDP OFFSET PERPORT REG (USB2_SQ_DMDP_OFFSET_PERPORT_REG_PP1)—Offset 421Ch

Access Method

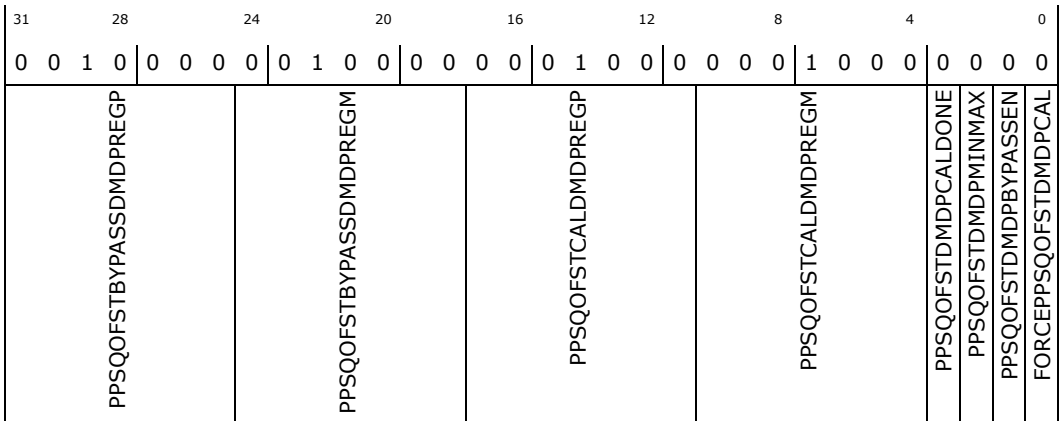
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 421Ch

Op Codes:

h - Read, h - Write

Default: 20404080h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x10 RW	**PPSQOFSTBYPASSDMDPREGP:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldmdpregp(6:0) will be overwritten by this register when ppsqofstDMDPBYPASSEN is asserted 1 . **Power Well:** SUS
24:18	0x10 RW	**PPSQOFSTBYPASSDMDPREGM:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldmdpregm(6:0)will be overwritten by this register when ppsqofstDMDPBYPASSEN is asserted 1 . **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
17:11	0x8 RO	**PPSQOFSTCALDMDPREGP:** 7-bit register that stores the DmDp squelch detector offset cancellation Dp side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDMDPCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to PPSQOFSTCALDMDPREGM. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTCALDPDMEN asserted: regP count down regM count up regP count down until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTCALDPDMEN asserted: regM countdown regP count up regM countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1271. **Power Well:** SUS
10:4	0x8 RO	**PPSQOFSTCALDMDPREGM:** 7-bit register that stores the DpDm squelch detector offset cancellation Dp side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDPDMCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to PPSQOFSTCALDPDMREGP. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTDPDMCAL asserted: regP count down regM count up regP count down until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTDPDMCAL asserted: regM countdown regP count up regM countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1271. **Power Well:** SUS
3	0x0 RO	**PPSQOFSTDMDPCALDONE:** This bit is set to 1b by state machine to indicate the calibration completion. This bit need to be cleared when FORCEppsqofstDMDPcal (starting of next calibration cycle). **Power Well:** SUS
2	0x0 RW/1C	**PPSQOFSTDMDPMINMAX:** Flag bit when PPSQOFSTCALDPDMREGP OR PPSQOFSTCALDPDMREGM offset counter reach the max range. The max range high limit is set by USBSQOFSTDPDMMAXLIMIT and low limit is always 0000000b. For P1271 is when it reaches 0011111b or 0000000b. This is to prevent roll back when the variation is out of range. This bit is to be cleared by software. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**PPSQOFSTDMDPBYPASSEN:** Software programmable. The values of ilane13:0usbppsqofstcaldmdpregm(6:0) and ilane13:0usbppsqofstcaldmdpregp(6:0) will be overwritten by ppsqofstbypassdmdpregm and ppsqofstbypassdmdpregp respectively when this bit assert 1b . **Power Well:** SUS
0	0x0 WO	**DmDp SQ Offset Calibration Enable Signal (FORCEPPSQOFSTDMDPCAL):** When set to 1b, this will force per-port squelch offset cancellation Finite State Machine to start calibrating. State Machine need to ensure only either DmDp or DmDp SQ detector is enabled for calibration at each time. BIOS have to wait for sufficient time for the calibration complete. This is a pulse trigger event. **Power Well:** SUS

7.14.73 USB2 DIS OFFSET PERPORT REG (USB2_DIS_OFFSET_PERPORT_REG_PP1)—Offset 421Dh

Access Method

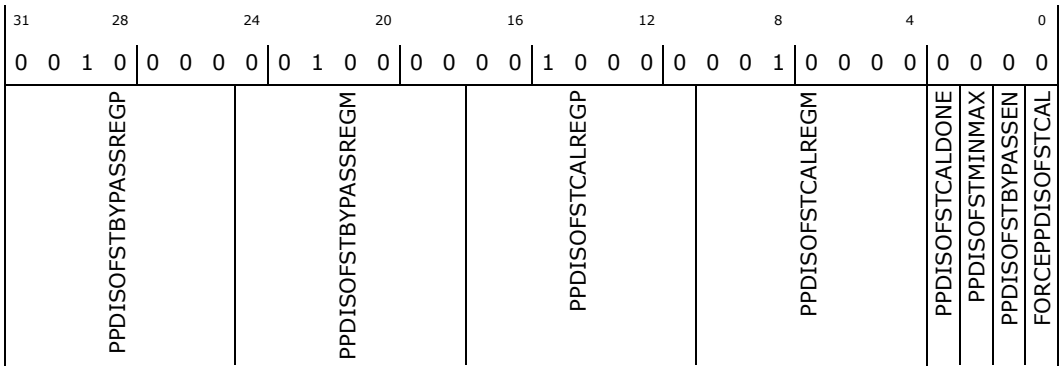
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 421Dh

Op Codes:

h - Read, h - Write

Default: 20408100h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x10 RW	**PPDISOFSTBYPASSREGP:** Software programmable. It is used during test mode. The values of ilane13:0usbppDISofstcalregp(6:0) will be overwritten by this register when ppDISofstbypassen is asserted 1 . **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
24:18	0x10 RW	**PPDISOFSTBYPASSREGM:** Software programmable. It is used during test mode. The values of ilane13:0usbppdisofstcalregm(6:0) will be overwritten by this register when ppDISofstbypassen is asserted 1 . **Power Well:** SUS
17:11	0x10 RO	**PPDISOFSTCALREGP:** 7-bit register that stores the disconnect detector offset cancellation left-side code. This 7-bit register must be initialized to default value prior to every calibration routine (before PPDISOFSTCALEN asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to right-register. This is to reduce the signal common mode variation to impact to circuit performance. If hsdisconnect output is low when FORCEPPDISOFSTCAL asserted: regP count down regM count up regP count down until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If hsdisconnect output is high when FORCEPPDISOFSTCAL asserted: regM countdown regP count up regM countdown until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 7:6 are unused for P1271. **Power Well:** SUS
10:4	0x10 RO	**PPDISOFSTCALREGM:** 7-bit register that stores the disconnect detector offset cancellation right-side code. This 7-bit register must be initialized to default value prior to every calibration routine (before PPDISOFSTCALEN asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to left-register. This is to reduce the signal common mode variation to impact to circuit performance. If hsdisconnect output is low when FORCEPPDISOFSTCAL asserted: regP count down regM count up regP count down until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If hsdisconnect output is high when FORCEPPDISOFSTCAL asserted: regM countdown regP count up regM countdown until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1271. **Power Well:** SUS
3	0x0 RO	**PPDISOFSTCALDONE:** This bit is set to 1b by state machine to indicate the calibration completion. This bit need to be cleared when FORCEPPDISofstcal (starting of next calibration cycle). **Power Well:** SUS
2	0x0 RW/1C	**PPDISOFSTMINMAX:** Flag bit when ppDISofstcalregp OR ppDISofstcalregm offset counter reach the max limit set by the product. For P1269.8 is when it reaches 0001111b or 0000000b. This is to prevent roll back when the variation is out of range. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**PPDISOFSTBYPASSEN:** Software programmable. The values of ilane13:0usbppDISofstcalregp(6:0) and ilane13:0usbppDISofstcalregm(6:0) will be overwritten by ppDISofstbypassregp and ppDISofstbypassregm respectively when ppDISofstbypassen is asserted 1 . **Power Well:** SUS
0	0x0 WO	**FORCEPPDISOFSTCAL:** When set to 1b, this will force per-port disconnect offset cancellation Finite State Machine to start calibrating. BIOS has to wait for sufficient time for the calibration complete. **Power Well:** SUS

7.14.74 USB2 SQ DPDM OFFSET PERPORT REG (USB2_SQ_DPDM_OFFSET_PERPORT_REG_PP2)—Offset 431Bh

Access Method

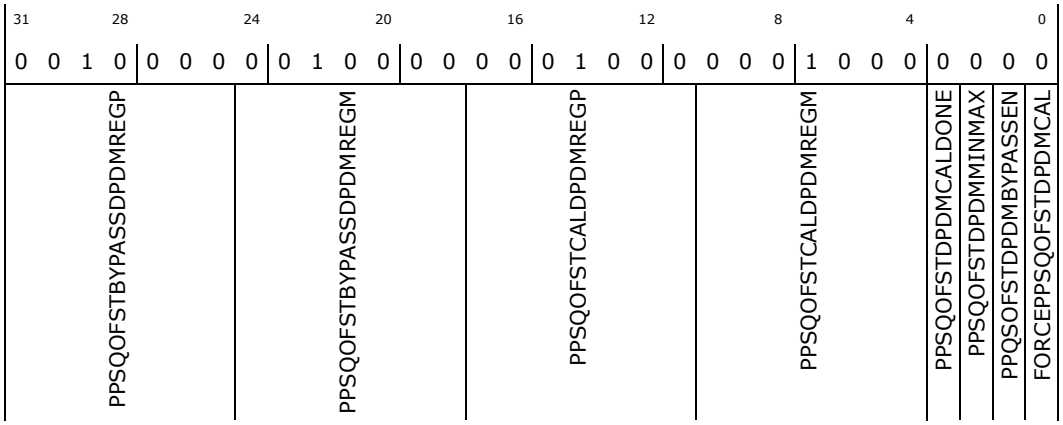
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 431Bh

Op Codes:

h - Read, h - Write

Default: 20404080h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x10 RW	**PPSQOFSTBYPASSDPDMREGP:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldpdmregp(6:0) will be overwritten by this register when ppsqofstDPDMBYPASSEN is asserted 1 . **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
24:18	0x10 RW	**PPSQOFSTBYPASSDPDMREGM:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldpdmregm(6:0)will be overwritten by this register when ppsqofstDPDMBYPASSEN is asserted 1 . **Power Well:** SUS
17:11	0x8 RO	**PPSQOFSTCALDPDMREGP:** 7-bit register that stores the DpDm squelch detector offset cancellation Dm-side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDPDMCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to ppsqofstcaldpdmregM. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTDPDMCAL asserted: regP count up regM countdown regP count up until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTDPDMCAL asserted: regP countdown regM count up regP countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1269.8. **Power Well:** SUS
10:4	0x8 RO	**PPSQOFSTCALDPDMREGM:** 7-bit register that stores the DpDm squelch detector offset cancellation Dp side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDPDMCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to ppsqofstcaldpdmregP. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTDPDMCAL asserted: regP count up regM countdown regP count up until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTDPDMCAL asserted: regP countdown regM count up regP countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1269.8. **Power Well:** SUS
3	0x0 RO	**PPSQOFSTDPDMCALDONE:** This bit is set to 1b by state machine to indicate the calibration completion. This bit need to be cleared when FORCEppsqofstDPDMcal (starting of next calibration cycle). **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW/1C	**PPSQOFSTDPDMMINMAX:** Flag bit when ppsqofstcaldpdmregP OR ppsqofstcaldpdmregM offset counter reach the max range. The max range high limit is set by USBSQOFSTDPDMMAXLIMIT and low limit is always 0000000b. For P1269.8 is when it reaches 0011111b or 0000000b. This is to prevent roll back when the variation is out of range. This bit is to be cleared by software. **Power Well:** SUS
1	0x0 RW	**PPQSOFSTDPDMBYPASSEN:** Software programmable. The values of ilane13:0usbppsqofstcaldpdmregp(6:0) and ilane13:0usbppsqofstcaldpdmregm(6:0) will be overwritten by ppsqofstbypassdpdmregp and ppsqofstbypassdpdmregm respectively when this bit assert 1b . **Power Well:** SUS
0	0x0 WO	**DpDm SQ Offset Calibration Enable Signal (FORCEPPSQOFSTDPDMCAL):** When set to 1b, this will force per-port squelch offset cancellation Finite State Machine to start calibrating. State Machine need to ensure only either DpDm or DmDp SQ detector is enabled for calibration at each time. BIOS have to wait for sufficient time for the calibration complete. This is a pulse trigger event. **Power Well:** SUS

7.14.75 USB2 SQ DMDP OFFSET PERPORT REG (USB2_SQ_DMDP_OFFSET_PERPORT_REG_PP2)—Offset 431Ch

Access Method

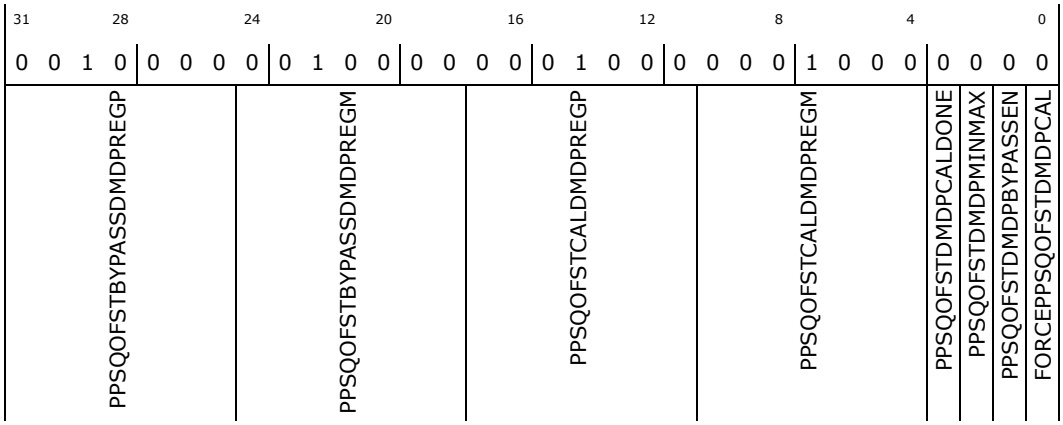
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 431Ch

Op Codes:

h - Read, h - Write

Default: 20404080h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x10 RW	**PPSQOFSTBYPASSDMDPREGP:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldmdpregp(6:0) will be overwritten by this register when ppsqofstDMDPBYPASSEN is asserted 1 . **Power Well:** SUS
24:18	0x10 RW	**PPSQOFSTBYPASSDMDPREGM:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldmdpregm(6:0)will be overwritten by this register when ppsqofstDMDPBYPASSEN is asserted 1 . **Power Well:** SUS
17:11	0x8 RO	**PPSQOFSTCALDMDPREGP:** 7-bit register that stores the DmDp squelch detector offset cancellation Dp side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDMDPCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to PPSQOFSTCALDMDPREGM. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTCALDPDMEN asserted: regP count down regM count up regP count down until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTCALDPDMEN asserted: regM countdown regP count up regM countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1271. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
10:4	0x8 RO	**PPSQOFSTCALDMDPREGM:** 7-bit register that stores the DpDm squelch detector offset cancellation Dp side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDPDMCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to PPSQOFSTCALDPDMREGP. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTDPDMCAL asserted: regP count down regM count up regP count down until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTDPDMCAL asserted: regM countdown regP count up regM countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1271. **Power Well:** SUS
3	0x0 RO	**PPSQOFSTDMDPCALDONE:** This bit is set to 1b by state machine to indicate the calibration completion. This bit need to be cleared when FORCEppsqofstDMDPcal (starting of next calibration cycle). **Power Well:** SUS
2	0x0 RW/1C	**PPSQOFSTDMDPMINMAX:** Flag bit when PPSQOFSTCALDPDMREGP OR PPSQOFSTCALDPDMREGM offset counter reach the max range. The max range high limit is set by USBSQOFSTDPDMMAXLIMIT and low limit is always 0000000b. For P1271 is when it reaches 0011111b or 0000000b. This is to prevent roll back when the variation is out of range. This bit is to be cleared by software. **Power Well:** SUS
1	0x0 RW	**PPSQOFSTDMDPBYPASSEN:** Software programmable. The values of ilane13:0usbppsqofstcaldmdpregm(6:0) and ilane13:0usbppsqofstcaldmdpregp(6:0) will be overwritten by ppsqofstbypassdmdpregm and ppsqofstbypassdmdpregp respectively when this bit assert 1b . **Power Well:** SUS
0	0x0 WO	**DmDp SQ Offset Calibration Enable Signal (FORCEPPSQOFSTDMDPCAL):** When set to 1b, this will force per-port squelch offset cancellation Finite State Machine to start calibrating. State Machine need to ensure only either DmDp or DmDp SQ detector is enabled for calibration at each time. BIOS have to wait for sufficient time for the calibration complete. This is a pulse trigger event. **Power Well:** SUS

7.14.76 USB2 DIS OFFSET PERPORT REG (USB2_DIS_OFFSET_PERPORT_REG_PP2)—Offset 431Dh

Access Method

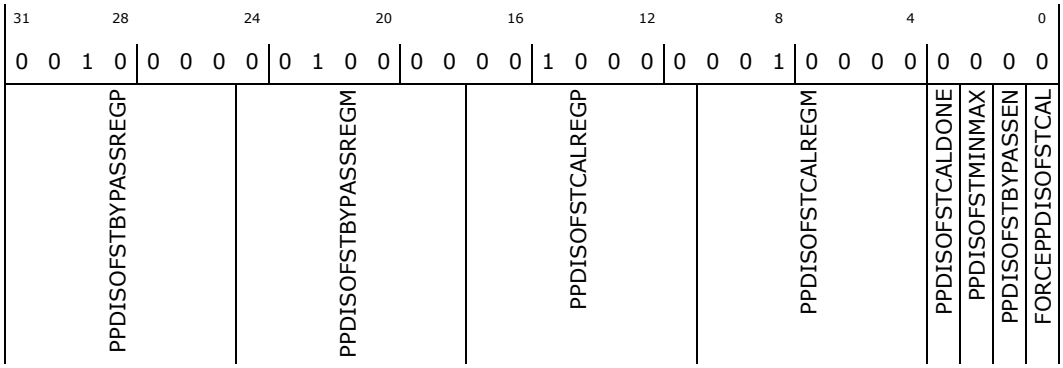
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 431Dh

Op Codes:

h - Read, h - Write

Default: 20408100h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x10 RW	**PPDISOFSTBYPASSREGP:** Software programmable. It is used during test mode. The values of ilane13:0usbppDISofstcalregp(6:0) will be overwritten by this register when ppDISofstbypassen is asserted 1 . **Power Well:** SUS
24:18	0x10 RW	**PPDISOFSTBYPASSREGM:** Software programmable. It is used during test mode. The values of ilane13:0usbppdisofstcalregm(6:0) will be overwritten by this register when ppDISofstbypassen is asserted 1 . **Power Well:** SUS
17:11	0x10 RO	**PPDISOFSTCALREGP:** 7-bit register that stores the disconnect detector offset cancellation left-side code. This 7-bit register must be initialized to default value prior to every calibration routine (before PPDISOFSTCALEN asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to right-register. This is to reduce the signal common mode variation to impact to circuit performance. If hsdisconnect output is low when FORCEPPDISOFSTCAL asserted: regP count down regM count up regP count down until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If hsdisconnect output is high when FORCEPPDISOFSTCAL asserted: regM countdown regP count up regM countdown until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 7:6 are unused for P1271. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
10:4	0x10 RO	**PPDISOFSTCALREGM:** 7-bit register that stores the disconnect detector offset cancellation right-side code. This 7-bit register must be initialized to default value prior to every calibration routine (before PPDISOFSTCALEN asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to left-register. This is to reduce the signal common mode variation to impact to circuit performance. If hsdisconnect output is low when FORCEPPDISOFSTCAL asserted: regP count down regM count up regP count down until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If hsdisconnect output is high when FORCEPPDISOFSTCAL asserted: regM countdown regP count up regM countdown until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1271. **Power Well:** SUS
3	0x0 RO	**PPDISOFSTCALDONE:** This bit is set to 1b by state machine to indicate the calibration completion. This bit need to be cleared when FORCEPPDISofstcal (starting of next calibration cycle). **Power Well:** SUS
2	0x0 RW/1C	**PPDISOFSTMINMAX:** Flag bit when ppDISofstcalregp OR ppDISofstcalregm offset counter reach the max limit set by the product. For P1269.8 is when it reaches 0001111b or 0000000b. This is to prevent roll back when the variation is out of range. **Power Well:** SUS
1	0x0 RW	**PPDISOFSTBYPASSEN:** Software programmable. The values of ilane13:0usbppDISofstcalregp(6:0) and ilane13:0usbppDISofstcalregm(6:0) will be overwritten by ppDISofstbypassregp and ppDISofstbypassregm respectively when ppDISofstbypassen is asserted 1 . **Power Well:** SUS
0	0x0 WO	**FORCEPPDISOFSTCAL:** When set to 1b, this will force per-port disconnect offset cancellation Finite State Machine to start calibrating. BIOS has to wait for sufficient time for the calibration complete. **Power Well:** SUS

7.14.77 USB2 SQ DPDM OFFSET PERPORT REG (USB2_SQ_DPDM_OFFSET_PERPORT_REG_PP3)—Offset 441Bh

Access Method

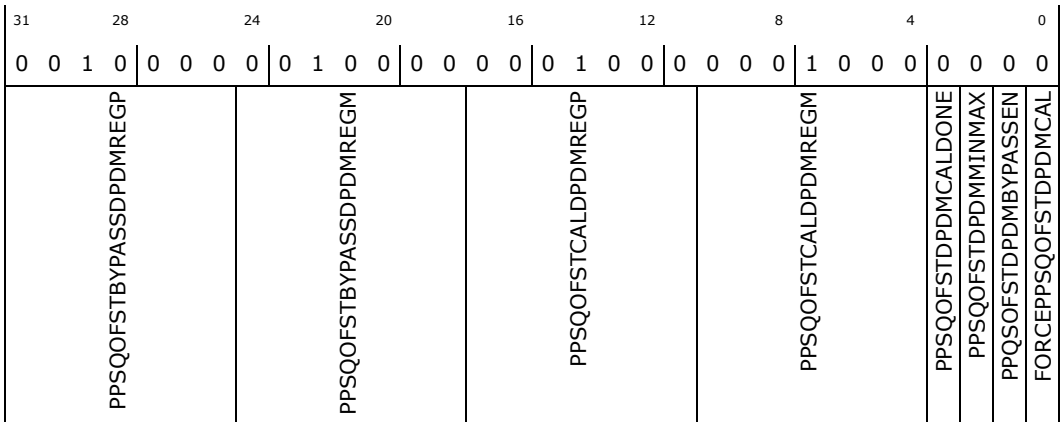
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 441Bh

Op Codes:

h - Read, h - Write

Default: 20404080h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x10 RW	**PPSQOFSTBYPASSDPDMREGP:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldpdmregp(6:0) will be overwritten by this register when ppsqofstDPDMBYPASSEN is asserted 1 . **Power Well:** SUS
24:18	0x10 RW	**PPSQOFSTBYPASSDPDMREGM:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldpdmregm(6:0)will be overwritten by this register when ppsqofstDPDMBYPASSEN is asserted 1 . **Power Well:** SUS
17:11	0x8 RO	**PPSQOFSTCALDPDMREGP:** 7-bit register that stores the DpDm squelch detector offset cancellation Dm-side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDPDMCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to ppsqofstcaldpdmregM. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTDPDMCAL asserted: regP count up regM countdown regP count up until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTDPDMCAL asserted: regP countdown regM count up regP countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1269.8. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
10:4	0x8 RO	**PPSQOFSTCALDPDMREGM:** 7-bit register that stores the DpDm squelch detector offset cancellation Dp side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDPDMCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to ppsqofstcaldpdmregP. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTDPDMCAL asserted: regP count up regM countdown regP count up until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTDPDMCAL asserted: regP countdown regM count up regP countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1269.8. **Power Well:** SUS
3	0x0 RO	**PPSQOFSTDPDMCALDONE:** This bit is set to 1b by state machine to indicate the calibration completion. This bit need to be cleared when FORCEppsqofstDPDMcal (starting of next calibration cycle). **Power Well:** SUS
2	0x0 RW/1C	**PPSQOFSTDPDMMINMAX:** Flag bit when ppsqofstcaldpdmregP OR ppsqofstcaldpdmregM offset counter reach the max range. The max range high limit is set by USBSQOFSTDPDMMAXLIMIT and low limit is always 0000000b. For P1269.8 is when it reaches 0011111b or 0000000b. This is to prevent roll back when the variation is out of range. This bit is to be cleared by software. **Power Well:** SUS
1	0x0 RW	**PPQSOFSTDPDMBYPASSEN:** Software programmable. The values of ilane13:0usbppsqofstcaldpdmregp(6:0) and ilane13:0usbppsqofstcaldpdmregm(6:0) will be overwritten by ppsqofstbypassdpdmregp and ppsqofstbypassdpdmregm respectively when this bit assert 1b . **Power Well:** SUS
0	0x0 WO	**DpDm SQ Offset Calibration Enable Signal (FORCEPPSQOFSTDPDMCAL):** When set to 1b, this will force per-port squelch offset cancellation Finite State Machine to start calibrating. State Machine need to ensure only either DpDm or DmDp SQ detector is enabled for calibration at each time. BIOS have to wait for sufficient time for the calibration complete. This is a pulse trigger event. **Power Well:** SUS

7.14.78 USB2 SQ DMDP OFFSET PERPORT REG (USB2_SQ_DMDP_OFFSET_PERPORT_REG_PP3)—Offset 441Ch

Access Method

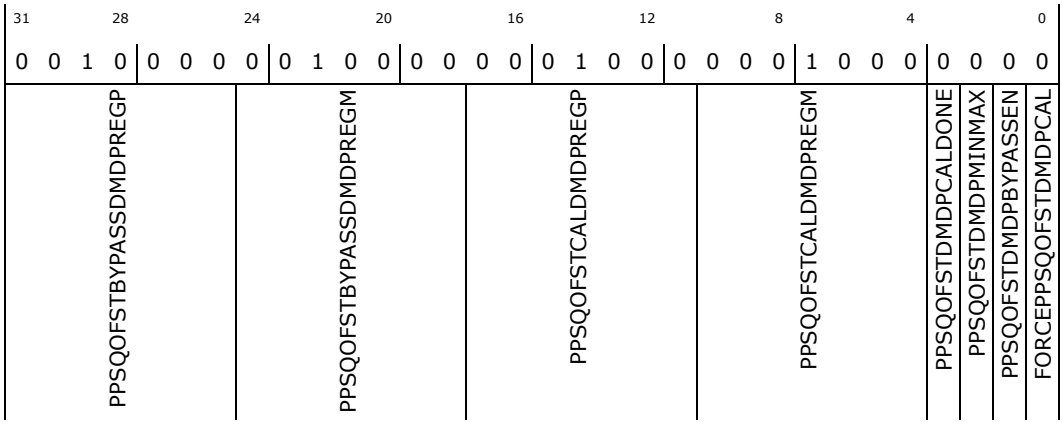
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 441Ch

Op Codes:

h - Read, h - Write

Default: 20404080h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x10 RW	**PPSQOFSTBYPASSDMDPREGP:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldmdpregp(6:0) will be overwritten by this register when ppsqofstDMDPBYPASSEN is asserted 1 . **Power Well:** SUS
24:18	0x10 RW	**PPSQOFSTBYPASSDMDPREGM:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldmdpregm(6:0)will be overwritten by this register when ppsqofstDMDPBYPASSEN is asserted 1 . **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
17:11	0x8 RO	**PPSQOFSTCALDMDPREGP:** 7-bit register that stores the DmDp squelch detector offset cancellation Dp side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDMDPCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to PPSQOFSTCALDMDPREGM. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTCALDPDMEN asserted: regP count down regM count up regP count down until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTCALDPDMEN asserted: regM countdown regP count up regM countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1271. **Power Well:** SUS
10:4	0x8 RO	**PPSQOFSTCALDMDPREGM:** 7-bit register that stores the DpDm squelch detector offset cancellation Dp side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDPDMCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to PPSQOFSTCALDPDMREGP. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTDPDMCAL asserted: regP count down regM count up regP count down until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTDPDMCAL asserted: regM countdown regP count up regM countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1271. **Power Well:** SUS
3	0x0 RO	**PPSQOFSTDMDPCALDONE:** This bit is set to 1b by state machine to indicate the calibration completion. This bit need to be cleared when FORCEppsqofstDMDPcal (starting of next calibration cycle). **Power Well:** SUS
2	0x0 RW/1C	**PPSQOFSTDMDPMINMAX:** Flag bit when PPSQOFSTCALDPDMREGP OR PPSQOFSTCALDPDMREGM offset counter reach the max range. The max range high limit is set by USBSQOFSTDPDMMAXLIMIT and low limit is always 0000000b. For P1271 is when it reaches 0011111b or 0000000b. This is to prevent roll back when the variation is out of range. This bit is to be cleared by software. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**PPSQOFSTDMDPBYPASSEN:** Software programmable. The values of ilane13:0usbppsqofstcaldmdpregm(6:0) and ilane13:0usbppsqofstcaldmdpregp(6:0) will be overwritten by ppsqofstbypassdmdpregm and ppsqofstbypassdmdpregp respectively when this bit assert 1b . **Power Well:** SUS
0	0x0 WO	**DmDp SQ Offset Calibration Enable Signal (FORCEPPSQOFSTDMDPCAL):** When set to 1b, this will force per-port squelch offset cancellation Finite State Machine to start calibrating. State Machine need to ensure only either DmDp or DmDp SQ detector is enabled for calibration at each time. BIOS have to wait for sufficient time for the calibration complete. This is a pulse trigger event. **Power Well:** SUS

7.14.79 USB2 DIS OFFSET PERPORT REG (USB2_DIS_OFFSET_PERPORT_REG_PP3)—Offset 441Dh

Access Method

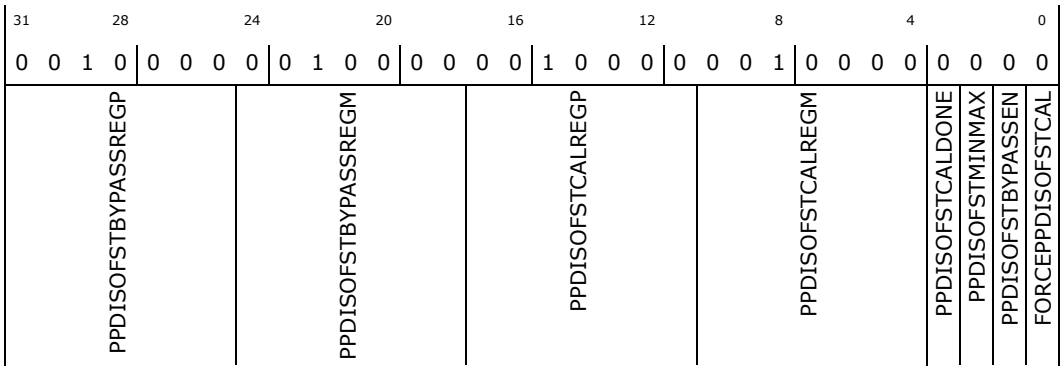
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 441Dh

Op Codes:

h - Read, h - Write

Default: 20408100h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x10 RW	**PPDISOFSTBYPASSREGP:** Software programmable. It is used during test mode. The values of ilane13:0usbppDISofstcalregp(6:0) will be overwritten by this register when ppDISofstbypassen is asserted 1 . **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
24:18	0x10 RW	**PPDISOFSTBYPASSREGM:** Software programmable. It is used during test mode. The values of ilane13:0usbppdisofstcalregm(6:0) will be overwritten by this register when ppDISofstbypassen is asserted 1 . **Power Well:** SUS
17:11	0x10 RO	**PPDISOFSTCALREGP:** 7-bit register that stores the disconnect detector offset cancellation left-side code. This 7-bit register must be initialized to default value prior to every calibration routine (before PPDISOFSTCALEN asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to right-register. This is to reduce the signal common mode variation to impact to circuit performance. If hsdisconnect output is low when FORCEPPDISOFSTCAL asserted: regP count down regM count up regP count down until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If hsdisconnect output is high when FORCEPPDISOFSTCAL asserted: regM countdown regP count up regM countdown until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 7:6 are unused for P1271. **Power Well:** SUS
10:4	0x10 RO	**PPDISOFSTCALREGM:** 7-bit register that stores the disconnect detector offset cancellation right-side code. This 7-bit register must be initialized to default value prior to every calibration routine (before PPDISOFSTCALEN asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to left-register. This is to reduce the signal common mode variation to impact to circuit performance. If hsdisconnect output is low when FORCEPPDISOFSTCAL asserted: regP count down regM count up regP count down until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If hsdisconnect output is high when FORCEPPDISOFSTCAL asserted: regM countdown regP count up regM countdown until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1271. **Power Well:** SUS
3	0x0 RO	**PPDISOFSTCALDONE:** This bit is set to 1b by state machine to indicate the calibration completion. This bit need to be cleared when FORCEPPDISofstcal (starting of next calibration cycle). **Power Well:** SUS
2	0x0 RW/1C	**PPDISOFSTMINMAX:** Flag bit when ppDISofstcalregp OR ppDISofstcalregm offset counter reach the max limit set by the product. For P1269.8 is when it reaches 0001111b or 0000000b. This is to prevent roll back when the variation is out of range. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**PPDISOFSTBYPASSEN:** Software programmable. The values of ilane13:0usbppDISofstcalregp(6:0) and ilane13:0usbppDISofstcalregm(6:0) will be overwritten by ppDISofstbypassregp and ppDISofstbypassregm respectively when ppDISofstbypassen is asserted 1 . **Power Well:** SUS
0	0x0 WO	**FORCEPPDISOFSTCAL:** When set to 1b, this will force per-port disconnect offset cancellation Finite State Machine to start calibrating. BIOS has to wait for sufficient time for the calibration complete. **Power Well:** SUS

7.14.80 USB2 SQ DPDM OFFSET PERPORT REG (USB2_SQ_DPDM_OFFSET_PERPORT_REG_PP4)—Offset 451Bh

Access Method

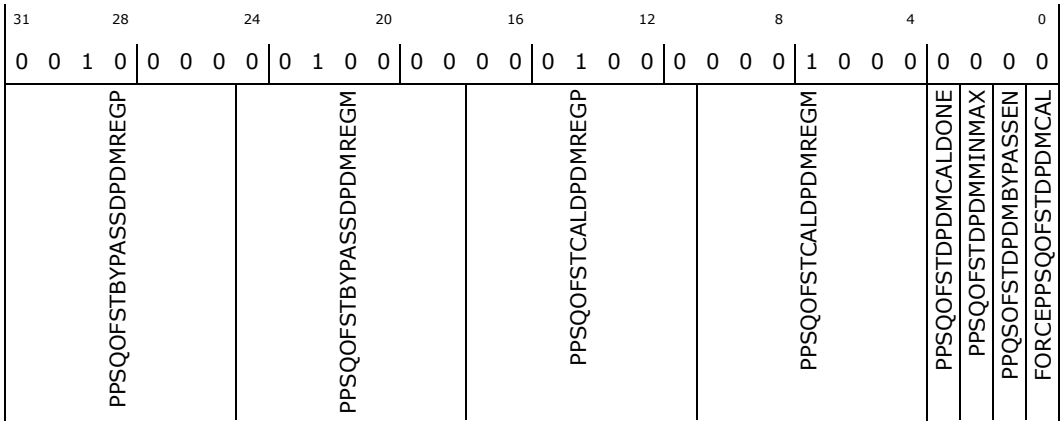
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 451Bh

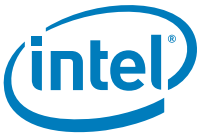
Op Codes:

h - Read, h - Write

Default: 20404080h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x10 RW	**PPSQOFSTBYPASSDPDMREGP:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldpdmregp(6:0) will be overwritten by this register when ppsqofstDPDMBYPASSEN is asserted 1 . **Power Well:** SUS



Bit Range	Default & Access	Field Name (ID): Description
24:18	0x10 RW	**PPSQOFSTBYPASSDPDMREGM:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldpdmregm(6:0)will be overwritten by this register when ppsqofstDPDMBYPASSEN is asserted 1 . **Power Well:** SUS
17:11	0x8 RO	**PPSQOFSTCALDPDMREGP:** 7-bit register that stores the DpDm squelch detector offset cancellation Dm-side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDPDMCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to ppsqofstcaldpdmregM. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTDPDMCAL asserted: regP count up regM countdown regP count up until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTDPDMCAL asserted: regP countdown regM count up regP countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1269.8. **Power Well:** SUS
10:4	0x8 RO	**PPSQOFSTCALDPDMREGM:** 7-bit register that stores the DpDm squelch detector offset cancellation Dp side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDPDMCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to ppsqofstcaldpdmregP. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTDPDMCAL asserted: regP count up regM countdown regP count up until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTDPDMCAL asserted: regP countdown regM count up regP countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1269.8. **Power Well:** SUS
3	0x0 RO	**PPSQOFSTDPDMCALDONE:** This bit is set to 1b by state machine to indicate the calibration completion. This bit need to be cleared when FORCEppsqofstDPDMcal (starting of next calibration cycle). **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW/1C	**PPSQOFSTDPDMMINMAX:** Flag bit when ppsqofstcaldpdmregP OR ppsqofstcaldpdmregM offset counter reach the max range. The max range high limit is set by USBSQOFSTDPDMMAXLIMIT and low limit is always 0000000b. For P1269.8 is when it reaches 0011111b or 0000000b. This is to prevent roll back when the variation is out of range. This bit is to be cleared by software. **Power Well:** SUS
1	0x0 RW	**PPQSOFSTDPDMBYPASSEN:** Software programmable. The values of ilane13:0usbppsqofstcaldpdmregp(6:0) and ilane13:0usbppsqofstcaldpdmregm(6:0) will be overwritten by ppsqofstbypassdpdmregp and ppsqofstbypassdpdmregm respectively when this bit assert 1b . **Power Well:** SUS
0	0x0 WO	**DpDm SQ Offset Calibration Enable Signal (FORCEPPSQOFSTDPDMCAL):** When set to 1b, this will force per-port squelch offset cancellation Finite State Machine to start calibrating. State Machine need to ensure only either DpDm or DmDp SQ detector is enabled for calibration at each time. BIOS have to wait for sufficient time for the calibration complete. This is a pulse trigger event. **Power Well:** SUS

7.14.81 USB2 SQ DMDP OFFSET PERPORT REG (USB2_SQ_DMDP_OFFSET_PERPORT_REG_PP4)—Offset 451Ch

Access Method

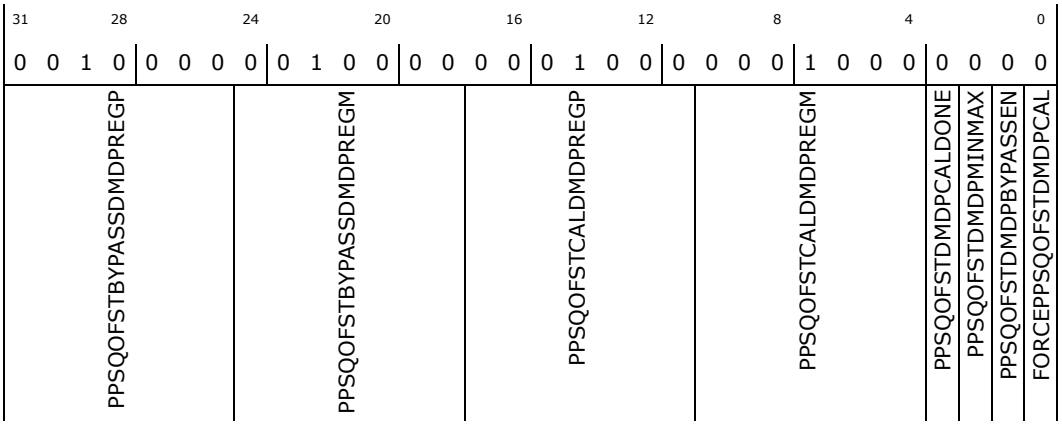
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 451Ch

Op Codes:

h - Read, h - Write

Default: 20404080h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x10 RW	**PPSQOFSTBYPASSDMDPREGP:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldmdpregp(6:0) will be overwritten by this register when ppsqofstDMDPBYPASSEN is asserted 1 . **Power Well:** SUS
24:18	0x10 RW	**PPSQOFSTBYPASSDMDPREGM:** Software programmable. It is used during test mode. The values of AFE pins ilane13:0usbppsqofstcaldmdpregm(6:0)will be overwritten by this register when ppsqofstDMDPBYPASSEN is asserted 1 . **Power Well:** SUS
17:11	0x8 RO	**PPSQOFSTCALDMDPREGP:** 7-bit register that stores the DmDp squelch detector offset cancellation Dp side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDMDPCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to PPSQOFSTCALDMDPREGM. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTCALDPDMEN asserted: regP count down regM count up regP count down until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTCALDPDMEN asserted: regM countdown regP count up regM countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1271. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
10:4	0x8 RO	**PPSQOFSTCALDMDPREGM:** 7-bit register that stores the DpDm squelch detector offset cancellation Dp side code. This 7-bit register must be initialized to default value prior to every calibration routine (before FORCEPPSQOFSTDPDMCAL asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to PPSQOFSTCALDPDMREGP. This is to reduce the signal common mode variation to impact to circuit performance. If unsquelch output is low when FORCEPPSQOFSTDPDMCAL asserted: regP count down regM count up regP count down until unsquelch output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If unsquelch output is high when FORCEPPSQOFSTDPDMCAL asserted: regM countdown regP count up regM countdown until squelch output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1271. **Power Well:** SUS
3	0x0 RO	**PPSQOFSTDMDPCALDONE:** This bit is set to 1b by state machine to indicate the calibration completion. This bit need to be cleared when FORCEppsqofstDMDPcal (starting of next calibration cycle). **Power Well:** SUS
2	0x0 RW/1C	**PPSQOFSTDMDPMINMAX:** Flag bit when PPSQOFSTCALDPDMREGP OR PPSQOFSTCALDPDMREGM offset counter reach the max range. The max range high limit is set by USBSQOFSTDPDMMAXLIMIT and low limit is always 0000000b. For P1271 is when it reaches 0011111b or 0000000b. This is to prevent roll back when the variation is out of range. This bit is to be cleared by software. **Power Well:** SUS
1	0x0 RW	**PPSQOFSTDMDPBYPASSEN:** Software programmable. The values of ilane13:0usbppsqofstcaldmdpregm(6:0) and ilane13:0usbppsqofstcaldmdpregp(6:0) will be overwritten by ppsqofstbypassdmdpregm and ppsqofstbypassdmdpregp respectively when this bit assert 1b . **Power Well:** SUS
0	0x0 WO	**DmDp SQ Offset Calibration Enable Signal (FORCEPPSQOFSTDMDPCAL):** When set to 1b, this will force per-port squelch offset cancellation Finite State Machine to start calibrating. State Machine need to ensure only either DmDp or DmDp SQ detector is enabled for calibration at each time. BIOS have to wait for sufficient time for the calibration complete. This is a pulse trigger event. **Power Well:** SUS

7.14.82 USB2 DIS OFFSET PERPORT REG (USB2_DIS_OFFSET_PERPORT_REG_PP4)—Offset 451Dh

Access Method

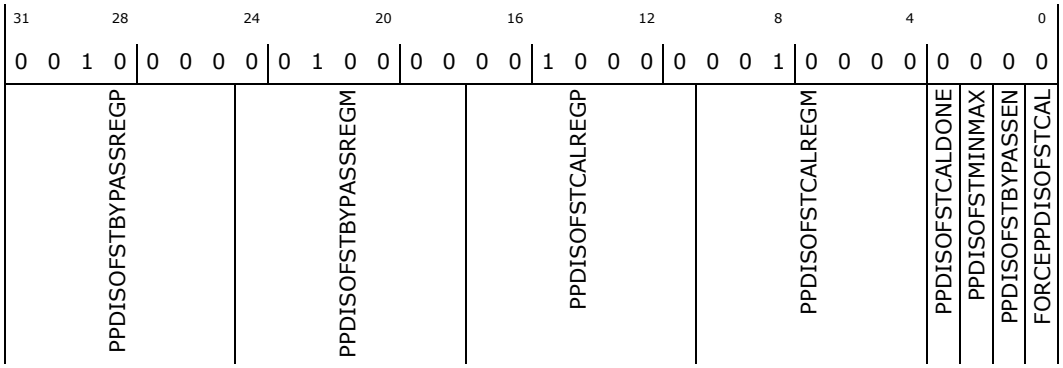
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 451Dh

Op Codes:

h - Read, h - Write

Default: 20408100h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x10 RW	**PPDISOFSTBYPASSREGP:** Software programmable. It is used during test mode. The values of ilane13:0usbppDISofstcalregp(6:0) will be overwritten by this register when ppDISofstbypassen is asserted 1 . **Power Well:** SUS
24:18	0x10 RW	**PPDISOFSTBYPASSREGM:** Software programmable. It is used during test mode. The values of ilane13:0usbppdisofstcalregm(6:0) will be overwritten by this register when ppDISofstbypassen is asserted 1 . **Power Well:** SUS
17:11	0x10 RO	**PPDISOFSTCALREGP:** 7-bit register that stores the disconnect detector offset cancellation left-side code. This 7-bit register must be initialized to default value prior to every calibration routine (before PPDISOFSTCALEN asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to right-register. This is to reduce the signal common mode variation to impact to circuit performance. If hsdisconnect output is low when FORCEPPDISOFSTCAL asserted: regP count down regM count up regP count down until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If hsdisconnect output is high when FORCEPPDISOFSTCAL asserted: regM countdown regP count up regM countdown until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 7:6 are unused for P1271. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
10:4	0x10 RO	**PPDISOFSTCALREGM:** 7-bit register that stores the disconnect detector offset cancellation right-side code. This 7-bit register must be initialized to default value prior to every calibration routine (before PPDISOFSTCALEN asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to left-register. This is to reduce the signal common mode variation to impact to circuit performance. If hsdisconnect output is low when FORCEPPDISOFSTCAL asserted: regP count down regM count up regP count down until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If hsdisconnect output is high when FORCEPPDISOFSTCAL asserted: regM countdown regP count up regM countdown until hsdisconnect output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. Note: bit 10:9 are unused for P1271. **Power Well:** SUS
3	0x0 RO	**PPDISOFSTCALDONE:** This bit is set to 1b by state machine to indicate the calibration completion. This bit need to be cleared when FORCEPPDISofstcal (starting of next calibration cycle). **Power Well:** SUS
2	0x0 RW/1C	**PPDISOFSTMINMAX:** Flag bit when ppDISofstcalregp OR ppDISofstcalregm offset counter reach the max limit set by the product. For P1269.8 is when it reaches 0001111b or 0000000b. This is to prevent roll back when the variation is out of range. **Power Well:** SUS
1	0x0 RW	**PPDISOFSTBYPASSEN:** Software programmable. The values of ilane13:0usbppDISofstcalregp(6:0) and ilane13:0usbppDISofstcalregm(6:0) will be overwritten by ppDISofstbypassregp and ppDISofstbypassregm respectively when ppDISofstbypassen is asserted 1 . **Power Well:** SUS
0	0x0 WO	**FORCEPPDISOFSTCAL:** When set to 1b, this will force per-port disconnect offset cancellation Finite State Machine to start calibrating. BIOS has to wait for sufficient time for the calibration complete. **Power Well:** SUS

7.14.83 USB2 SQDIS OFFSET GLOBAL REG (USB2_SQDIS_OFFSET_GLOBAL_REG)—Offset 7F1Eh

Access Method

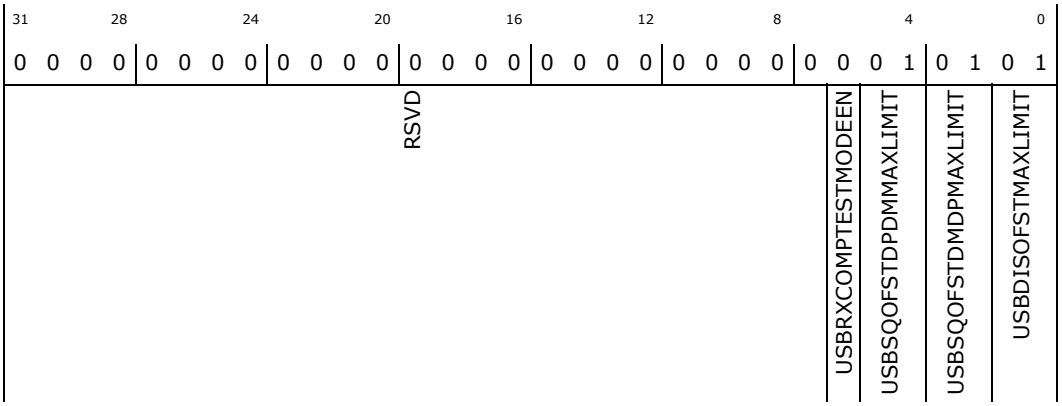
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 7F1Eh

Op Codes:

h - Read, h - Write

Default: 00000015h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS
6	0x0 RW	**USBRXCOMPTESTMODEEN:** This global bit connects directly to AFE ilane(0:13)usbrxcomptestmodeen. When this bit is asserted, SQ DpDm detector, SQ DmDp Detector and Disc detector Opamp differential inputs will be disconnected from Vref/Vrefb voltage and will have the direct connection to Pad voltage. This allow offset to be introduced through Dp/Dm for offset cancellation max range and monotonous characterization purposes. **Power Well:** SUS
5:4	0x1 RW	**USBSQOFSTDPDMMAXLIMIT:** This register defines the counter limit for the DpDm SQ offset cancellation SM. 11b = 7-bits 10b = 6-bits 01b = 5-bits 00b = 4-bits **Power Well:** SUS
3:2	0x1 RW	**USBSQOFSTDMDPMAXLIMIT:** This register defines the counter limit for the DmDp SQ offset cancellation SM. 11b = 7-bits 10b = 6-bits 01b = 5-bits 00b = 4-bits **Power Well:** SUS
1:0	0x1 RW	**USBDISOFSTMAXLIMIT:** This register defines the counter limit for the Disconnect detector offset cancellation SM. 11b = 7-bits 10b = 6-bits 01b = 5-bits 00b = 4-bits This limit applies to the GLB COMPARATOR calibration as well. **Power Well:** SUS

7.14.84 USB2 DEVICE MODE GLOBAL REG (USB2_DEVICE_MODE_GLOBAL_REG)—Offset 401Fh

Access Method

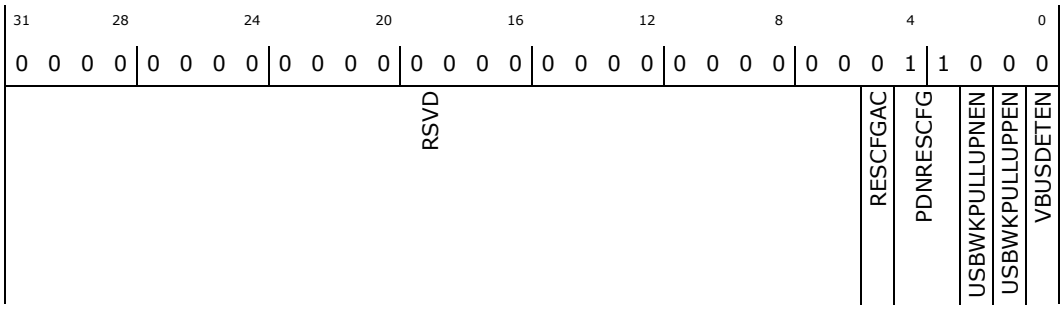
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 401Fh

Op Codes:

h - Read, h - Write

Default: 00000018h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**RSVD:** Reserved. **Power Well:** SUS
5	0x0 RW	**DEVICE STATIC VS DYNAMIC (RESCFGAC):** Enable register based control versus dynamic control for OTG host and device switching. 1: Enable register control (PDNRESCFG - 0x1F, 4:3). 0: Dynamic control based on utmi dp/dm pulldown. **Power Well:** SUS
4:3	0x3 RW	**PDNRESCFG:** Feed directly to SHIP or AFE : AFE Functional or Test Mode : Functional Config bit (global to all ports) Feed directly to SHIP or AFE : AFE Functional or Test Mode : Functional To select the pull-down resistive dividers (15k, 250k , mtg 30k) Host: 11b (default) Device: 10b (default) The pull-down resistive divider is used to step down the common mode level of the input differential signal to meet electrical spec of input receivers. **Power Well:** SUS
2	0x0 RW	**USBWKPULLUPNEN:** Set 1b to enable the 1.5kohm pull-up on MINUS pads of the respective port to support OTG. This bit is only used for test mode. This CSR bit OR with signal from pputmi, then output to AFE This reg is not applicable for P1269.8 **Power Well:** SUS
1	0x0 RW	**USBWKPULLUPPEN:** Set to 1b to enable the 1.5kohm pull-up on PLUS pads of the respective port to support OTG. This bit is only used for test mode. This CSR bit OR with signal from pputmi, then output to AFE. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**VBUSDETEN:** Set to 1b to enable the VBUS comparator which is used for debug or test purposes. During debug mode, andlt;VBUS_valid) pin could be observed through VISA. Additional VISA configuration is required to mux this signal out to observation port. This CSR bit OR with signal from pputmi, then output to AFE. **Power Well:** SUS

7.14.85 USB2 TEST GLOBAL SERIAL LOOPBACK (USB2_TEST_GLOBAL_SERIAL_LOOPBACK)—Offset 4020h

Access Method

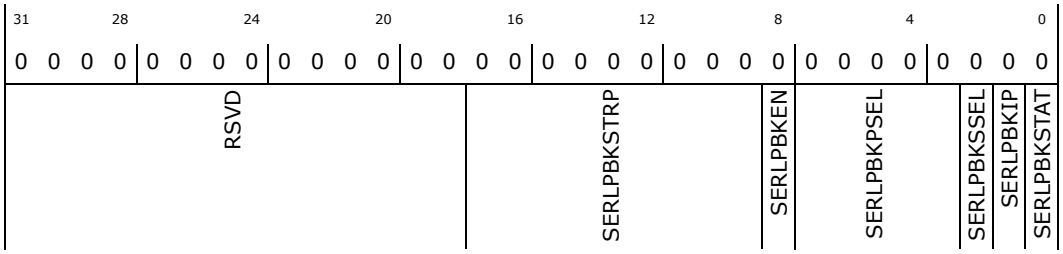
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4020h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0x0 RO	**RSVD:** RSVD **Power Well:** SUS
17:9	0x0 RW	**Serial Loopback Strobe Points (SERLPBKSTRP):** Speed Begin Mid End FS 12d (Ch) 22d (16h) 32d (20h) LS 167d (A7h) 169d (A9h) 172d (ACh) These points define the reliable strobing of the D-/+ on the AFE during loopback. Bits are allowed to change only when loopback mode has stopped. It is expected that the Strobe Point is done prior to starting the serial loopback mode. **Power Well:** SUS
8	0x0 RW	**Serial Loopback Enable (SERLPBKEN):** 1: Start serial loopback mode within SHIP. 0: Stop serial loopback mode within SHIP. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
7:3	0x0 RW	**Serial Loopback Port Select[M:0] (SERLPBKPSEL):** Selects the physical port number to run the loopback test: 0: Port 0 1: Port 1 ... N: Port N Bit is allowed to change only when loopback mode has stopped. It is expected that the port select is done prior to starting the serial loopback mode. **Power Well:** SUS
2	0x0 RW	**Serial Loopback Speed Select (SERLPBKSSEL):** 1: FS 0: LS Bit is allowed to change only when loopback mode has stopped. It is expected that the speed select is done prior to starting the serial loopback mode. **Power Well:** SUS
1	0x0 RO	**Serial Loopback In Progress (SERLPBKIP):** 1: Serial loopback mode is in progress. 0: Serial loopback mode has stopped. **Power Well:** SUS
0	0x0 RW/1C	**Serial Loopback Status (SERLPBKSTAT):** bit. Status is only valid once loopback mode has fully stopped. **Power Well:** SUS

7.14.86 USB2 GLOBAL COMP CMP OFFSET REG (USB2_GLOBAL_COMP_CMP_OFFSET_REG)—Offset 7F21h

Access Method

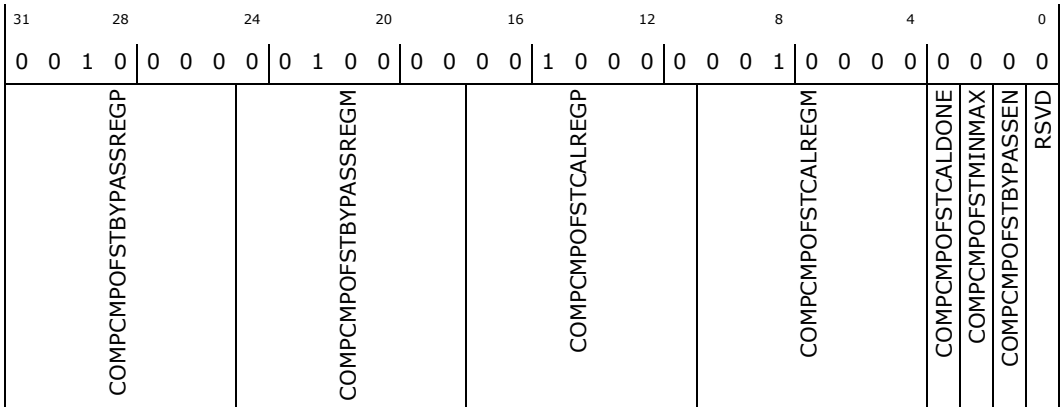
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 7F21h

Op Codes:

h - Read, h - Write

Default: 20408100h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x10 RW	**COMPCMPOFSTBYPASSREGP:** Software programmable. It is used during test mode. The values of iusbcompcmpofstcalregp(6:0) will be overwritten by this register when compcmpofstbypassen is asserted 1 . **Power Well:** SUS
24:18	0x10 RW	**COMPCMPOFSTBYPASSREGM:** Software programmable. It is used during test mode. The values of iusbcompcmpofstcalregm(6:0) will be overwritten by this register when compcmpofstbypassen is asserted 1 . **Power Well:** SUS
17:11	0x10 RO	**COMPCMPOFSTCALREGP:** 7-bit register that stores the comparator offset cancellation left-side code. This 7-bit register must be initialized to default value prior to every calibration routine (before COMPCMPOFSTCALEN asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to rightt-register. This is to reduce the signal common mode variation to impact to circuit performance. If comparator output (rescountup) is low when FORCEPPCOMPCMPOFSTCALDPDMEN asserted: regP count down regM count up regP count down until comparator output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If comparator output (rescountup) is high when FORCECOMPCMPOFSTCALDPDMEN asserted: regM countdown regP count up regM countdown until comparator output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. **Power Well:** SUS
10:4	0x10 RO	**COMPCMPOFSTCALREGM:** 7-bit register that stores the comparator offset cancellation right-side code. This 7-bit register must be initialized to default value prior to every calibration routine (before COMPCMPOFSTCALEN asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to left-register. This is to reduce the signal common mode variation to impact to circuit performance. If comparator output (rescountup)is low when FORCEPPCOMPCMPOFSTCALDPDMEN asserted: regP count down regM count up regP count down until comparator output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If comparator output (rescountup) is high when FORCEPPCOMPCMPOFSTCALDPDMEN asserted: regM countdown regP count up regM countdown until comparator output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. **Power Well:** SUS
3	0x0 RO	**COMPCMPOFSTCALDONE:** This bit is set to 1b by state machine to indicate the calibration completion. This bit need to be cleared when FORCECOMPCMPOFSTCAL (starting of next calibration cycle). **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW/1C	**COMPCMPOFSTMINMAX:** Flag bit when compcmpofstcalregp OR compcmpofstcalregm offset counter reach the max limit set by the product. This is to prevent roll back when the variation is out of range. **Power Well:** SUS
1	0x0 RW	**COMPCMPOFSTBYPASSEN:** Software programmable. The values of iusbcompcmpofstcalregp(6:0) and iusbcompcmpofstcalregm(6:0) will be overwritten by compcmpofstbypassregp and compcmpofstbypassregm respectively when compcmpofstbypassen is asserted 1 . **Power Well:** SUS
0	0x0 RO	**RSVD:** RSVD **Power Well:** SUS

7.14.87 PER PORT RCOMP HS PULLUP REGISTER (PER_PORT_RCOMP_HS_PULLUP_REGISTER_PP0)—Offset 4122h

Access Method

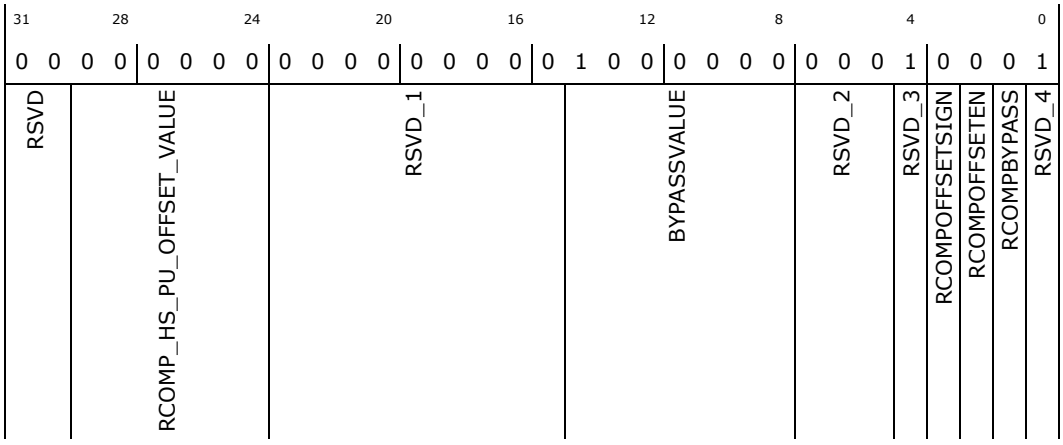
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4122h

Op Codes:

h - Read, h - Write

Default: 00004011h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RSVD:** RSVD **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
29:24	0x0 RW	**RCOMP HS PU OFFSET VALUE (RCOMP_HS_PU_OFFSET_VALUE):** rcomp offset value bit **Power Well:** SUS
23:15	0x0 RO	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
14:8	0x40 RW	**BYPASS VALUE (BYPASSVALUE):** bypass value **Power Well:** SUS
7:5	0x0 RO	**RSVD (RSVD_2):** RSVD **Power Well:** SUS
4	0x1 RW	**RSVD (RSVD_3):** RSVD (RSVD): Reserved HALFRESBITEN (HALFRESBITEN): Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional halfres bit enable. **Power Well:** SUS
3	0x0 RW	**RCOMPOFFSETSIGN:** rcomp offset sign bit 1 - incrementing offset value 0 - decrementing offset value **Power Well:** SUS
2	0x0 RW	**RCOMPOFFSETEN:** rcomp offset enable bit 1 - enable rcomp offset override 0 - disable rcomp offset override **Power Well:** SUS
1	0x0 RW	**RCOMPBYPASS:** rcompbyass mode, config controlled 1 - enable rcomp bypass 0 - disable rcomp bypass **Power Well:** SUS
0	0x1 RW	**RSVD (RSVD_4):** RSVD **Power Well:** SUS

7.14.88 PER PORT RCOMP HS PULLDOWN REGISTER (PER_PORT_RCOMP_HS_PULLDOWN_REGISTER_PP0)—Offset 4123h

Access Method

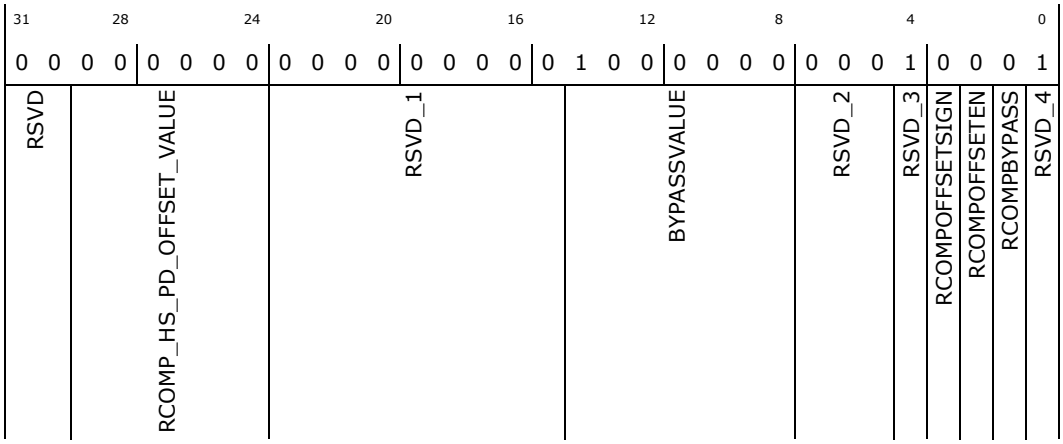
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4123h

Op Codes:

h - Read, h - Write

Default: 00004011h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RSVD:** Reserved for future use. **Power Well:** SUS
29:24	0x0 RW	**RCOMP HS PD OFFSET VALUE (RCOMP_HS_PD_OFFSET_VALUE):** rcomp offset value bit **Power Well:** SUS
23:15	0x0 RO	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
14:8	0x40 RW	**BYPASS VALUE (BYPASSVALUE):** bypass value **Power Well:** SUS
7:5	0x0 RO	**RSVD (RSVD_2):** RSVD **Power Well:** SUS
4	0x1 RW	**RSVD (RSVD_3):** RSVD (RSVD): HALFRESBITEN (HALFRESBITEN): Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional halfres bit enable. **Power Well:** SUS
3	0x0 RW	**RCOMPOFFSETSIGN:** rcomp offset sign bit 1 - incrementing offset value 0 - decrementing offset value **Power Well:** SUS
2	0x0 RW	**RCOMPOFFSETEN:** rcomp offset enable bit 1 - enable rcomp offset override 0 - disable rcomp offset override **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**RCOMPBYPASS:** rcompbyass mode, config controlled 1 - enable rcomp bypass 0 - disable rcomp bypass **Power Well:** SUS
0	0x1 RW	**RSVD (RSVD_4):** RSVD **Power Well:** SUS

7.14.89 PER PORT RCOMP HS PULLUP REGISTER (PER_PORT_RCOMP_HS_PULLUP_REGISTER_PP1)—Offset 4222h

Access Method

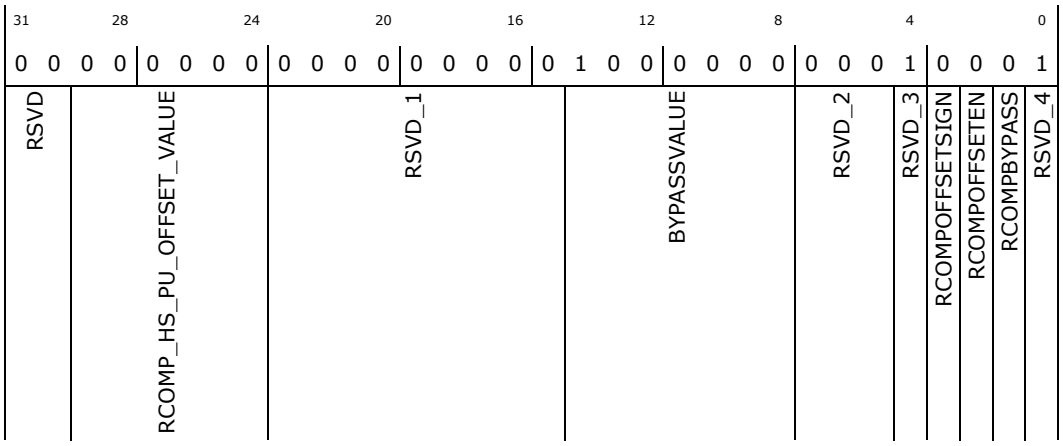
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4222h

Op Codes:

h - Read, h - Write

Default: 00004011h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RSVD:** RSVD **Power Well:** SUS
29:24	0x0 RW	**RCOMP HS PU OFFSET VALUE (RCOMP_HS_PU_OFFSET_VALUE):** rcomp offset value bit **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
23:15	0x0 RO	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
14:8	0x40 RW	**BYPASS VALUE (BYPASSVALUE):** bypass value **Power Well:** SUS
7:5	0x0 RO	**RSVD (RSVD_2):** RSVD **Power Well:** SUS
4	0x1 RW	**RSVD (RSVD_3):** RSVD (RSVD): Reserved HALFRESBITEN (HALFRESBITEN): Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional halfres bit enable. **Power Well:** SUS
3	0x0 RW	**RCOMPOFFSETSIGN:** rcomp offset sign bit 1 - incrementing offset value 0 - decrementing offset value **Power Well:** SUS
2	0x0 RW	**RCOMPOFFSETEN:** rcomp offset enable bit 1 - enable rcomp offset override 0 - disable rcomp offset override **Power Well:** SUS
1	0x0 RW	**RCOMPBYPASS:** rcompbyass mode, config controlled 1 - enable rcomp bypass 0 - disable rcomp bypass **Power Well:** SUS
0	0x1 RW	**RSVD (RSVD_4):** RSVD **Power Well:** SUS

7.14.90 PER PORT RCOMP HS PULLDOWN REGISTER (PER_PORT_RCOMP_HS_PULLDOWN_REGISTER_PP1)—Offset 4223h

Access Method

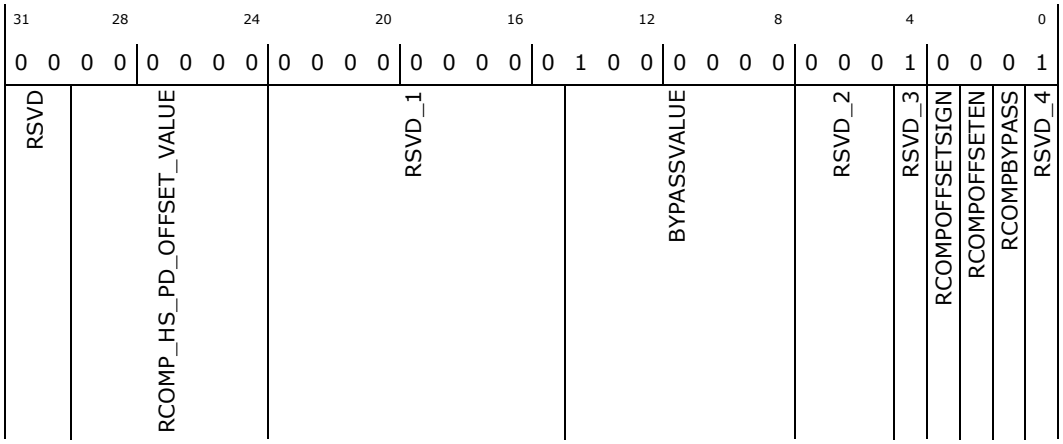
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4223h

Op Codes:

h - Read, h - Write

Default: 00004011h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RSVD:** Reserved for future use. **Power Well:** SUS
29:24	0x0 RW	**RCOMP HS PD OFFSET VALUE (RCOMP_HS_PD_OFFSET_VALUE):** rcomp offset value bit **Power Well:** SUS
23:15	0x0 RO	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
14:8	0x40 RW	**BYPASS VALUE (BYPASSVALUE):** bypass value **Power Well:** SUS
7:5	0x0 RO	**RSVD (RSVD_2):** RSVD **Power Well:** SUS
4	0x1 RW	**RSVD (RSVD_3):** RSVD (RSVD): HALFRESBITEN (HALFRESBITEN): Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional halfres bit enable. **Power Well:** SUS
3	0x0 RW	**RCOMPOFFSETSIGN:** rcomp offset sign bit 1 - incrementing offset value 0 - decrementing offset value **Power Well:** SUS
2	0x0 RW	**RCOMPOFFSETEN:** rcomp offset enable bit 1 - enable rcomp offset override 0 - disable rcomp offset override **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**RCOMPBYPASS:** rcompbyass mode, config controlled 1 - enable rcomp bypass 0 - disable rcomp bypass **Power Well:** SUS
0	0x1 RW	**RSVD (RSVD_4):** RSVD **Power Well:** SUS

7.14.91 PER PORT RCOMP HS PULLUP REGISTER (PER_PORT_RCOMP_HS_PULLUP_REGISTER_PP2)—Offset 4322h

Access Method

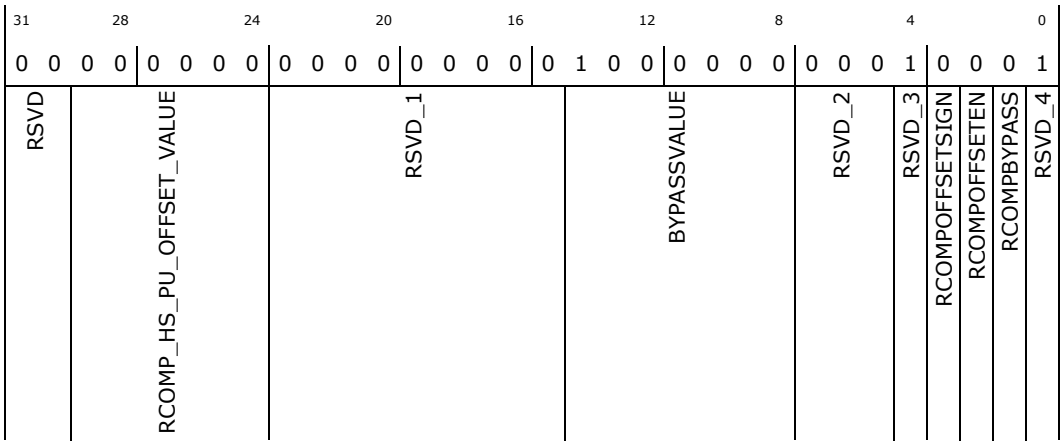
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4322h

Op Codes:

h - Read, h - Write

Default: 00004011h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RSVD:** RSVD **Power Well:** SUS
29:24	0x0 RW	**RCOMP HS PU OFFSET VALUE (RCOMP_HS_PU_OFFSET_VALUE):** rcomp offset value bit **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
23:15	0x0 RO	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
14:8	0x40 RW	**BYPASS VALUE (BYPASSVALUE):** bypass value **Power Well:** SUS
7:5	0x0 RO	**RSVD (RSVD_2):** RSVD **Power Well:** SUS
4	0x1 RW	**RSVD (RSVD_3):** RSVD (RSVD): Reserved HALFRESBITEN (HALFRESBITEN): Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional halfres bit enable. **Power Well:** SUS
3	0x0 RW	**RCOMPOFFSETSIGN:** rcomp offset sign bit 1 - incrementing offset value 0 - decrementing offset value **Power Well:** SUS
2	0x0 RW	**RCOMPOFFSETEN:** rcomp offset enable bit 1 - enable rcomp offset override 0 - disable rcomp offset override **Power Well:** SUS
1	0x0 RW	**RCOMPBYPASS:** rcompbyass mode, config controlled 1 - enable rcomp bypass 0 - disable rcomp bypass **Power Well:** SUS
0	0x1 RW	**RSVD (RSVD_4):** RSVD **Power Well:** SUS

7.14.92 PER PORT RCOMP HS PULLDOWN REGISTER (PER_PORT_RCOMP_HS_PULLDOWN_REGISTER_PP2)—Offset 4323h

Access Method

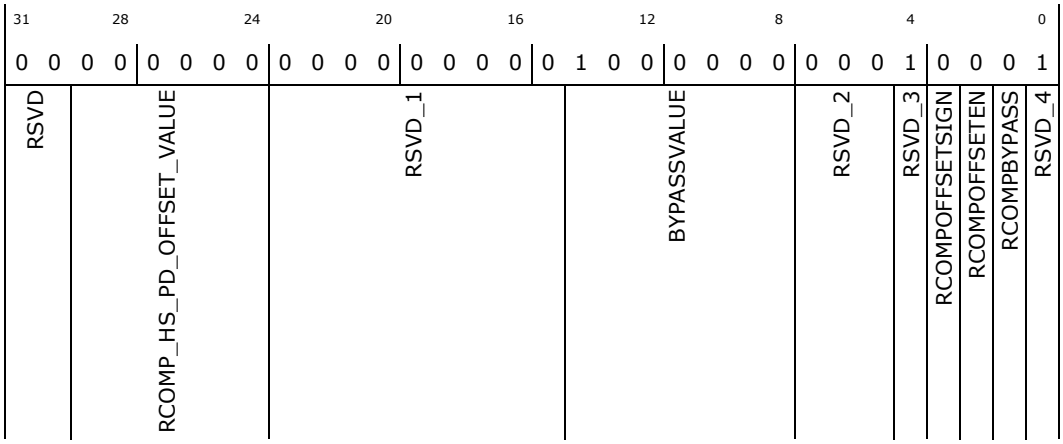
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4323h

Op Codes:

h - Read, h - Write

Default: 00004011h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RSVD:** Reserved for future use. **Power Well:** SUS
29:24	0x0 RW	**RCOMP HS PD OFFSET VALUE (RCOMP_HS_PD_OFFSET_VALUE):** rcomp offset value bit **Power Well:** SUS
23:15	0x0 RO	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
14:8	0x40 RW	**BYPASS VALUE (BYPASSVALUE):** bypass value **Power Well:** SUS
7:5	0x0 RO	**RSVD (RSVD_2):** RSVD **Power Well:** SUS
4	0x1 RW	**RSVD (RSVD_3):** RSVD (RSVD): HALFRESBITEN (HALFRESBITEN): Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional halfres bit enable. **Power Well:** SUS
3	0x0 RW	**RCOMPOFFSETSIGN:** rcomp offset sign bit 1 - incrementing offset value 0 - decrementing offset value **Power Well:** SUS
2	0x0 RW	**RCOMPOFFSETEN:** rcomp offset enable bit 1 - enable rcomp offset override 0 - disable rcomp offset override **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**RCOMPBYPASS:** rcompbyass mode, config controlled 1 - enable rcomp bypass 0 - disable rcomp bypass **Power Well:** SUS
0	0x1 RW	**RSVD (RSVD_4):** RSVD **Power Well:** SUS

7.14.93 PER PORT RCOMP HS PULLUP REGISTER (PER_PORT_RCOMP_HS_PULLUP_REGISTER_PP3)—Offset 4422h

Access Method

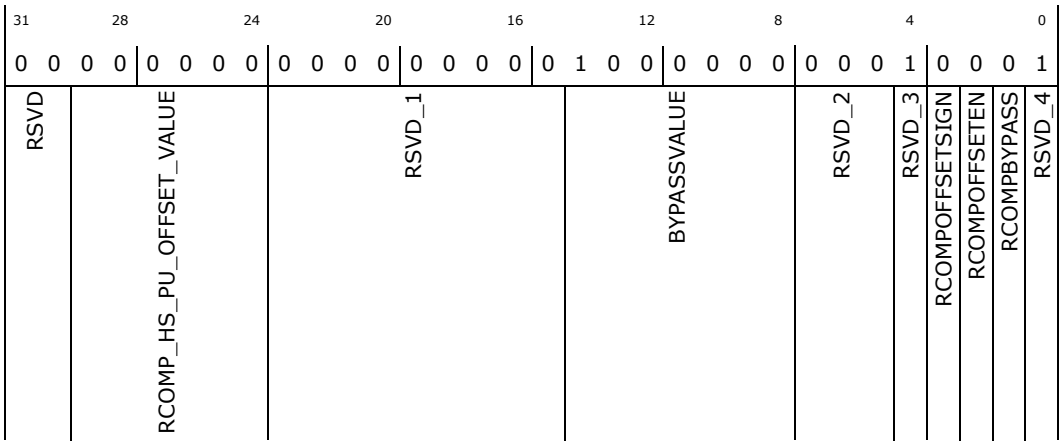
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4422h

Op Codes:

h - Read, h - Write

Default: 00004011h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RSVD:** RSVD **Power Well:** SUS
29:24	0x0 RW	**RCOMP HS PU OFFSET VALUE (RCOMP_HS_PU_OFFSET_VALUE):** rcomp offset value bit **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
23:15	0x0 RO	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
14:8	0x40 RW	**BYPASS VALUE (BYPASSVALUE):** bypass value **Power Well:** SUS
7:5	0x0 RO	**RSVD (RSVD_2):** RSVD **Power Well:** SUS
4	0x1 RW	**RSVD (RSVD_3):** RSVD (RSVD): Reserved HALFRESBITEN (HALFRESBITEN): Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional halfres bit enable. **Power Well:** SUS
3	0x0 RW	**RCOMPOFFSETSIGN:** rcomp offset sign bit 1 - incrementing offset value 0 - decrementing offset value **Power Well:** SUS
2	0x0 RW	**RCOMPOFFSETEN:** rcomp offset enable bit 1 - enable rcomp offset override 0 - disable rcomp offset override **Power Well:** SUS
1	0x0 RW	**RCOMPBYPASS:** rcompbyass mode, config controlled 1 - enable rcomp bypass 0 - disable rcomp bypass **Power Well:** SUS
0	0x1 RW	**RSVD (RSVD_4):** RSVD **Power Well:** SUS

7.14.94 PER PORT RCOMP HS PULLDOWN REGISTER (PER_PORT_RCOMP_HS_PULLDOWN_REGISTER_PP3)—Offset 4423h

Access Method

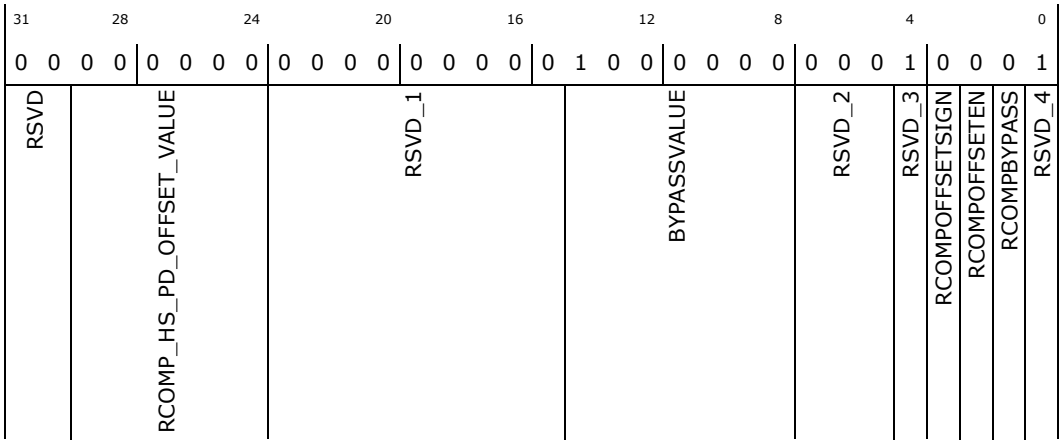
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4423h

Op Codes:

h - Read, h - Write

Default: 00004011h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RSVD:** Reserved for future use. **Power Well:** SUS
29:24	0x0 RW	**RCOMP HS PD OFFSET VALUE (RCOMP_HS_PD_OFFSET_VALUE):** rcomp offset value bit **Power Well:** SUS
23:15	0x0 RO	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
14:8	0x40 RW	**BYPASS VALUE (BYPASSVALUE):** bypass value **Power Well:** SUS
7:5	0x0 RO	**RSVD (RSVD_2):** RSVD **Power Well:** SUS
4	0x1 RW	**RSVD (RSVD_3):** RSVD (RSVD): HALFRESBITEN (HALFRESBITEN): Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional halfres bit enable. **Power Well:** SUS
3	0x0 RW	**RCOMPOFFSETSIGN:** rcomp offset sign bit 1 - incrementing offset value 0 - decrementing offset value **Power Well:** SUS
2	0x0 RW	**RCOMPOFFSETEN:** rcomp offset enable bit 1 - enable rcomp offset override 0 - disable rcomp offset override **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**RCOMPBYPASS:** rcompbyass mode, config controlled 1 - enable rcomp bypass 0 - disable rcomp bypass **Power Well:** SUS
0	0x1 RW	**RSVD (RSVD_4):** RSVD **Power Well:** SUS

7.14.95 PER PORT RCOMP HS PULLUP REGISTER (PER_PORT_RCOMP_HS_PULLUP_REGISTER_PP4)—Offset 4522h

Access Method

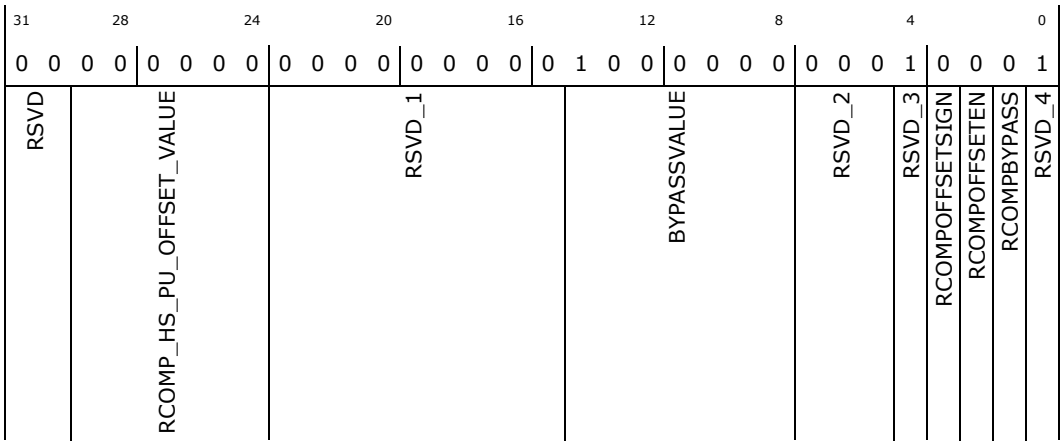
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4522h

Op Codes:

h - Read, h - Write

Default: 00004011h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RSVD:** RSVD **Power Well:** SUS
29:24	0x0 RW	**RCOMP HS PU OFFSET VALUE (RCOMP_HS_PU_OFFSET_VALUE):** rcomp offset value bit **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
23:15	0x0 RO	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
14:8	0x40 RW	**BYPASS VALUE (BYPASSVALUE):** bypass value **Power Well:** SUS
7:5	0x0 RO	**RSVD (RSVD_2):** RSVD **Power Well:** SUS
4	0x1 RW	**RSVD (RSVD_3):** RSVD (RSVD): Reserved HALFRESBITEN (HALFRESBITEN): Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional halfres bit enable. **Power Well:** SUS
3	0x0 RW	**RCOMPOFFSETSIGN:** rcomp offset sign bit 1 - incrementing offset value 0 - decrementing offset value **Power Well:** SUS
2	0x0 RW	**RCOMPOFFSETEN:** rcomp offset enable bit 1 - enable rcomp offset override 0 - disable rcomp offset override **Power Well:** SUS
1	0x0 RW	**RCOMPBYPASS:** rcompbyass mode, config controlled 1 - enable rcomp bypass 0 - disable rcomp bypass **Power Well:** SUS
0	0x1 RW	**RSVD (RSVD_4):** RSVD **Power Well:** SUS

7.14.96 PER PORT RCOMP HS PULLDOWN REGISTER (PER_PORT_RCOMP_HS_PULLDOWN_REGISTER_PP4)—Offset 4523h

Access Method

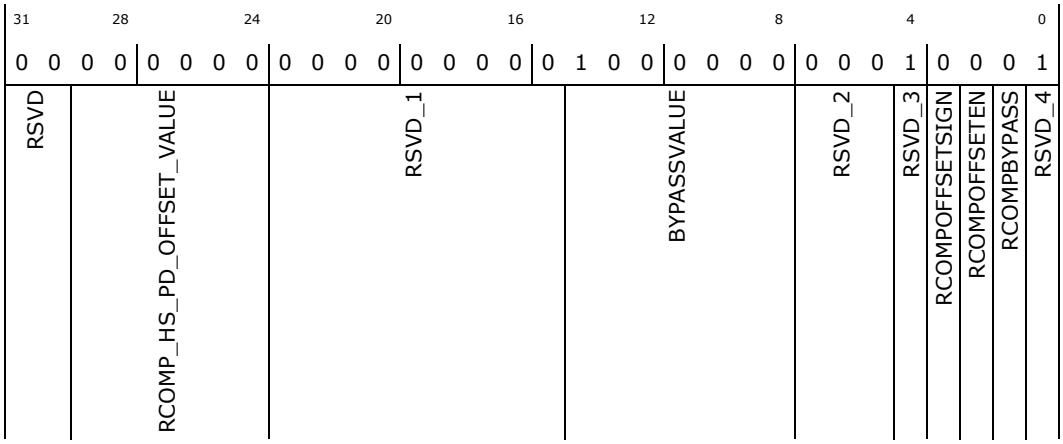
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4523h

Op Codes:

h - Read, h - Write

Default: 00004011h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RSVD:** Reserved for future use. **Power Well:** SUS
29:24	0x0 RW	**RCOMP HS PD OFFSET VALUE (RCOMP_HS_PD_OFFSET_VALUE):** rcomp offset value bit **Power Well:** SUS
23:15	0x0 RO	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
14:8	0x40 RW	**BYPASS VALUE (BYPASSVALUE):** bypass value **Power Well:** SUS
7:5	0x0 RO	**RSVD (RSVD_2):** RSVD **Power Well:** SUS
4	0x1 RW	**RSVD (RSVD_3):** RSVD (RSVD): HALFRESBITEN (HALFRESBITEN): Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional halfres bit enable. **Power Well:** SUS
3	0x0 RW	**RCOMPOFFSETSIGN:** rcomp offset sign bit 1 - incrementing offset value 0 - decrementing offset value **Power Well:** SUS
2	0x0 RW	**RCOMPOFFSETEN:** rcomp offset enable bit 1 - enable rcomp offset override 0 - disable rcomp offset override **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**RCOMPBYPASS:** rcompbyass mode, config controlled 1 - enable rcomp bypass 0 - disable rcomp bypass **Power Well:** SUS
0	0x1 RW	**RSVD (RSVD_4):** RSVD **Power Well:** SUS

7.14.97 GLOBAL RCOMP CL 45OHM 15K PULLDOWN REGISTER (GLOBAL_RCOMP_CL_45OHM_15K_PULLDOWN_REGISTER)—Offset 4024h

Access Method

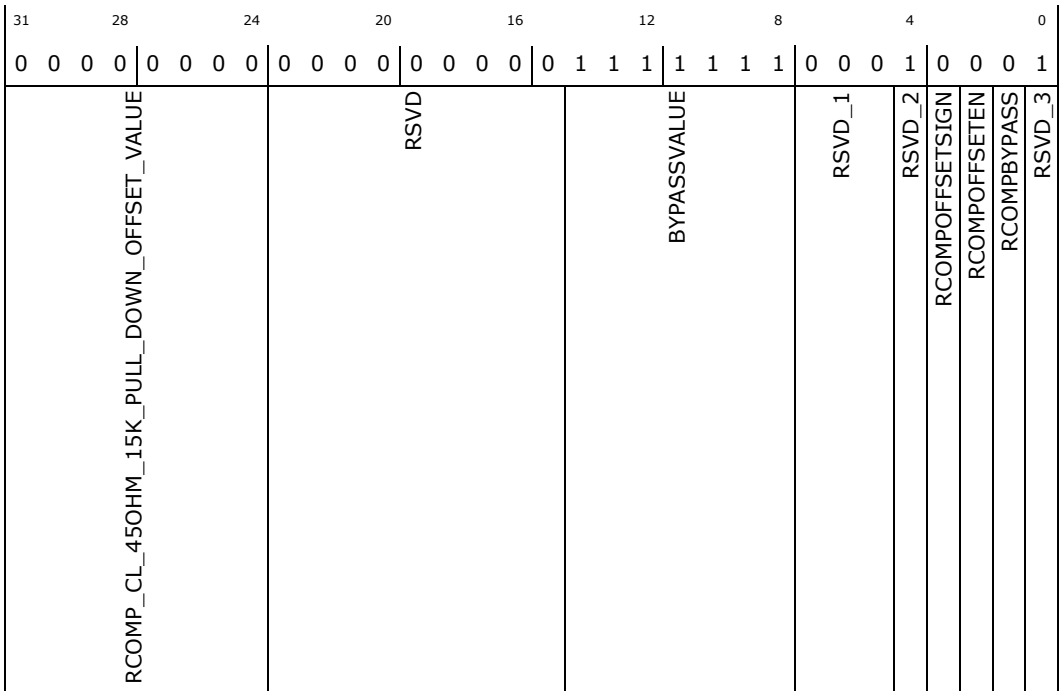
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4024h

Op Codes:

h - Read, h - Write

Default: 00007F11h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**RCOMP CL 45OHM_15K PULL DOWN OFFSET VALUE (RCOMP_CL_45OHM_15K_PULL_DOWN_OFFSET_VALUE):** rcomp offset value bit. Bits (31:30) are not used by HW, SW should not program these to non-zero values for 15K compensation. Bits (31:29) are not used by HW, SW should not program these to non-zero values for CL 45 ohm compensation. **Power Well:** SUS
23:15	0x0 RO	**RSVD:** RSVD **Power Well:** SUS
14:8	0x7f RW	**BYPASSVALUE:** bypass value **Power Well:** SUS
7:5	0x0 RO	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
4	0x1 RW	**RSVD (RSVD_2):** RSVD **Power Well:** SUS
3	0x0 RW	**RCOMPOFFSETSIGN:** rcomp offset sign bit 1 - incrementing offset value 0 - decrementing offset value **Power Well:** SUS
2	0x0 RW	**RCOMPOFFSETEN:** rcompbyass mode, config controlled 1 - enable rcomp bypass 0 - disable rcomp bypass **Power Well:** SUS
1	0x0 RW	**RCOMPBYPASS:** rcompbyass mode, config controlled 1 - enable rcomp bypass 0 - disable rcomp bypass **Power Well:** SUS
0	0x1 RW	**RSVD (RSVD_3):** Reserved. **Power Well:** SUS

7.14.98 GLOBAL RCOMP CL 1POINT5K PULL-UP REGISTER (GLOBAL_RCOMP_CL_1POINT5K_PULLUP_REGISTER)—Offset 4025h

Note: This entire register is a placeholder for future addition of the 1.5k R compensation. It has no associated functionality.

Access Method

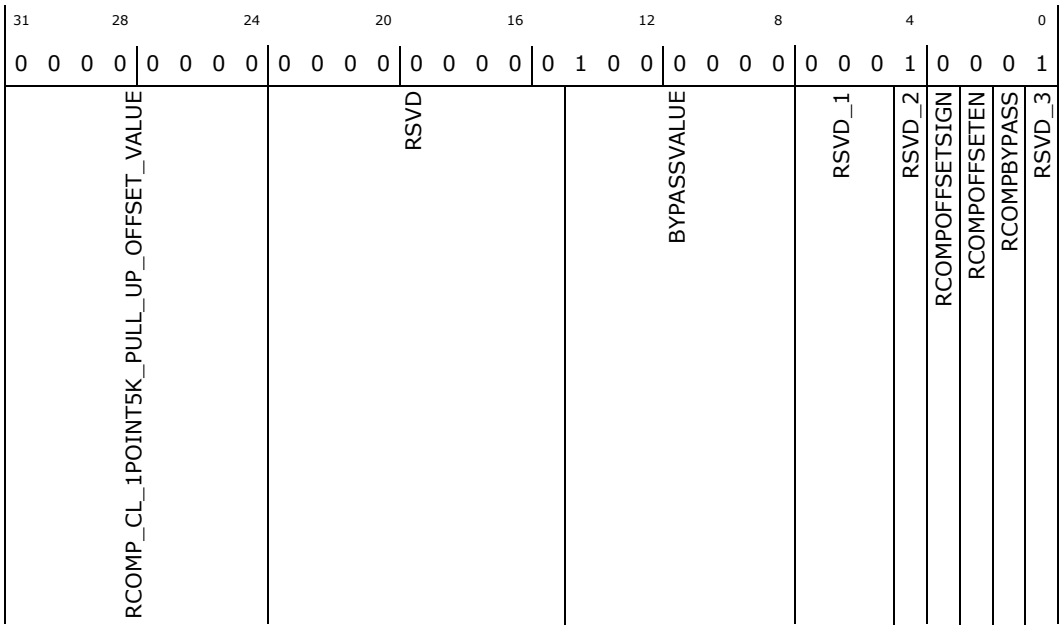
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4025h

Op Codes:

h - Read, h - Write

Default: 00004011h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**RCOMP CL 1.5K PULL UP OFFSET VALUE (RCOMP_CL_1POINT5K_PULL_UP_OFFSET_VALUE):** rcomp offset value bit Bits (31:30) are not used by HW, SW should not program these to non-zero values. **Power Well:** SUS
23:15	0x0 RO	**RSVD:** RSVD **Power Well:** SUS
14:8	0x40 RW	**BYPASS VALUE (BYPASSVALUE):** bypass value **Power Well:** SUS
7:5	0x0 RO	**RSVD (RSVD_1):** RSVD **Power Well:** SUS
4	0x1 RW	**RSVD (RSVD_2):** RSVD (RSVD): HALFRESBITEN (HALFRESBITEN): Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional halfres bit enable. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**RCOMPOFFSETSIGN:** rcomp offset sign bit 1 - incrementing offset value 0 - decrementing offset value **Power Well:** SUS
2	0x0 RW	**RCOMPOFFSETEN:** rcomp offset enable bit 1 - enable rcomp offset override 0 - disable rcomp offset override **Power Well:** SUS
1	0x0 RW	**RCOMPBYPASS:** rcompbyass mode, config controlled 1 - enable rcomp bypass 0 - disable rcomp bypass **Power Well:** SUS
0	0x1 RW	**RSVD (RSVD_3):** Set it to 1b to enable hardware based RCAL. **Power Well:** SUS

7.14.99 USB2 PER PORT 2 (USB2_PER_PORT_2_PP0)—Offset 4126h

Access Method

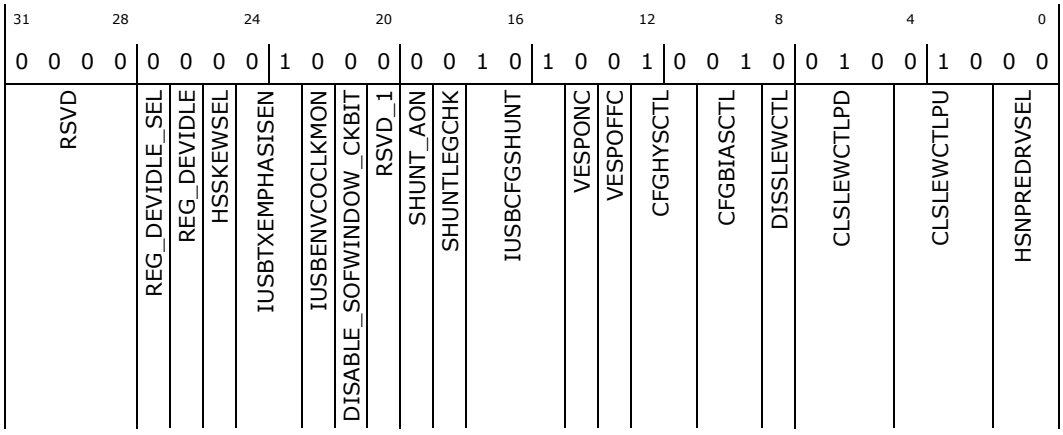
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4126h

Op Codes:

h - Read, h - Write

Default: 00829248h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RSVD:** RSVD **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
27	0x0 RW	**Manual Override of Device Idle Pullup Enable Select (REG_DEVIDLE_SEL):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To enable manual override on device Idle pullup enable. Enabling/Disabling come from reg_didle_force_onoff. 0: Disable Manual override on device idle pullup enable. Device idle pullup enable based on functional logic. **Power Well:** SUS
26	0x0 RW	**Device Idle Force On Off (REG_DEVIDLE):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To force turn on of device idle pullup enable. 0: To force turn off of device idle pullup enable. **Power Well:** SUS
25	0x0 RW	**HSSKEWSEL:** Select the skew direction for HS transition. Hsskewsel | Skew direction 0 | Delay HS Driver 0)1 Transition (default) 1 | Delay HS Driver 1)0 Transition **Power Well:** SUS
24:23	0x1 RW	**Per Port HS Transmitter Emphasis (IUSBTXEMPHASISEN):** Config bit (per port) Enables HS transmitter Emphasis for the respective ports Value Description 00 Emphasis OFF 01 De-emphasis ON (strength = TXISET+PETXISET) Default 10 Pre-emphasis ON (strength = TXISET+PETXISET) 11 Pre-emphasis and De-emphasis ON (strength = TXISET+PETXISET) **Power Well:** SUS
22	0x0 RW	**ADPLL clock monitoring through TX (IUSBENVCOCLKMON):** Signal to enable ADPLL clock monitoring through TX driver. **Power Well:** SUS
21	0x0 RW	**DISABLE SOF WINDOW FOR DISCONNECT (DISABLE_SOFWINDOW_CKBIT):** 1: Enable sampling only during SOF window for disconnect. 0:Sampling not limited to SOF window. **Power Well:** SUS
20	0x0 RW	**RSVD (RSVD_1):** Reserved. **Power Well:** SUS
19	0x0 RW	**EOS Shunt always on (SHUNT_AON):** To force shunt FSM to always on and not run shunt detect FSM. **Power Well:** SUS
18	0x0 RW	**EOS Shunt legcheck (SHUNTLEGCHK):** To Enable EOS Shunt protection legcheck. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
17:15	0x5 RW	**EOS Shunt configuration (IUSBCFGSHUNT):** Set Shunt strength control trim during VIHz 000 - Turn off shunt 100 - Lowest Shunt strength 101 - Low Shunt Strength 110 - Medium Shunt Strength 111 - High Shunt Strength **Power Well:** SUS
14	0x0 RW	**VIHz EOS Shunt Protection Off Control (VESPONC):** 1: Force the shunt to turn statically OFF. 0: Dynamic shunt ON/OFF mode based on port suspend. Bits (VESPOFFC, VESPONC) should never be set to 11b. **Power Well:** SUS
13	0x0 RW	**VIHz EOS Shunt Protection On Control (VESPOFFC):** 1: Force the shunt to turn statically ON. 0: Dynamic shunt ON/OFF mode based on port suspend. Bits (VESPOFFC, VESPONC) should never be set to 11b. **Power Well:** SUS
12:11	0x2 RW	**CFGHYSCTL:** Hysteresis control for Classic Single Ended Rx 00 - 0mV 01 - 25mV 10 - 75mV (default) 11 - 125mV **Power Well:** SUS
10:9	0x1 RW	**CFGBIASCTL:** Bias control for Classic Differential Rx 00 - 50uA 01 - 60uA (default) 1X - 70uA **Power Well:** SUS
8	0x0 RW	**DISSLEWCTL:** DISSLEWCTL (DISSLEWCTL): Feed directly to SHIP or AFE : AFE Functional or Test Mode : Functional 0 - enable slew rate control during Classic Tx (default) 1 - disable slew rate control during Classic Tx **Power Well:** SUS
7:5	0x2 RW	**CLSLEWCTLPD:** Pull-Down Slew rate control for Classic Low Speed Tx 000 - slowest slew rate 001 - slow slew rate 010 - c73usb250_Normal (default) 100 - fast slew rate **Power Well:** SUS
4:2	0x2 RW	**CLSLEWCTLPU:** Slew rate control for Classic Low Speed Tx 000 - slowest slew rate 001 - slow slew rate 010 - c73usb250_Normal (default) 100 - fast slew rate **Power Well:** SUS
1:0	0x0 RW	**HSNPREDRVSEL:** Delay/skews strength Control for HS driver. Use together with HSSKEWSEL. npredrvsel(1) | npredrvsel(0) | Skew Offset 0 | 0 | No Skew (default) 0 | 1 | 30mV 1 | 0 | 40mV 1 | 1 | 50mV **Power Well:** SUS

7.14.100 USB2 PER PORT 2 (USB2_PER_PORT_2_PP1)—Offset 4226h

Access Method

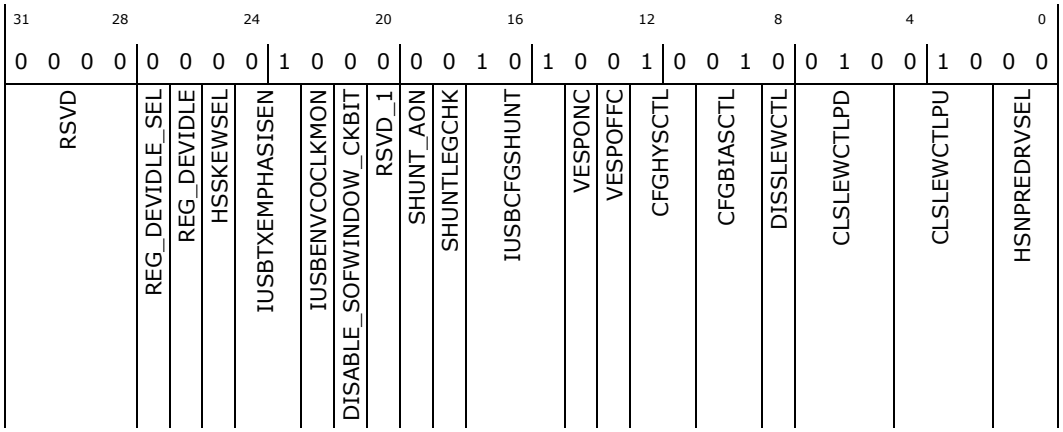
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4226h

Op Codes:

h - Read, h - Write

Default: 00829248h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RSVD:** RSVD **Power Well:** SUS
27	0x0 RW	**Manual Override of Device Idle Pullup Enable Select (REG_DEVIDLE_SEL):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To enable manual override on device Idle pullup enable. Enabling/Disabling come from reg_didle_force_onoff. 0: Disable Manual override on device idle pullup enable. Device idle pullup enable based on functional logic. **Power Well:** SUS
26	0x0 RW	**Device Idle Force On Off (REG_DEVIDLE):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To force turn on of device idle pullup enable. 0: To force turn off of device idle pullup enable. **Power Well:** SUS
25	0x0 RW	**HSSKEWSEL:** Select the skew direction for HS transition. Hsskewsel | Skew direction 0 | Delay HS Driver 0)1 Transition (default) 1 | Delay HS Driver 1)0 Transition **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
24:23	0x1 RW	**Per Port HS Transmitter Emphasis (IUSBTXEMPHASISEN):** Config bit (per port) Enables HS transmitter Emphasis for the respective ports Value Description 00 Emphasis OFF 01 De-emphasis ON (strength = TXISET+PETXISET) Default 10 Pre-emphasis ON (strength = TXISET+PETXISET) 11 Pre-emphasis and De-emphasis ON (strength = TXISET+PETXISET) **Power Well:** SUS
22	0x0 RW	**ADPLL clock monitoring through TX (IUSBENVCOCLKMON):** Signal to enable ADPLL clock monitoring through TX driver. **Power Well:** SUS
21	0x0 RW	**DISABLE SOF WINDOW FOR DISCONNECT (DISABLE_SOFWINDOW_CKBIT):** 1: Enable sampling only during SOF window for disconnect. 0:Sampling not limited to SOF window. **Power Well:** SUS
20	0x0 RW	**RSVD (RSVD_1):** Reserved. **Power Well:** SUS
19	0x0 RW	**EOS Shunt always on (SHUNT_AON):** To force shunt FSM to always on and not run shunt detect FSM. **Power Well:** SUS
18	0x0 RW	**EOS Shunt legcheck (SHUNTLEGCHK):** To Enable EOS Shunt protection legcheck. **Power Well:** SUS
17:15	0x5 RW	**EOS Shunt configuration (IUSBCFGSHUNT):** Set Shunt strength control trim during VIHz 000 - Turn off shunt 100 - Lowest Shunt strength 101 - Low Shunt Strength 110 - Medium Shunt Strength 111 - High Shunt Strength **Power Well:** SUS
14	0x0 RW	**VIHz EOS Shunt Protection Off Control (VESPONC):** 1: Force the shunt to turn statically OFF. 0: Dynamic shunt ON/OFF mode based on port suspend. Bits (VESPOFFC, VESPONC) should never be set to 11b. **Power Well:** SUS
13	0x0 RW	**VIHz EOS Shunt Protection On Control (VESPOFFC):** 1: Force the shunt to turn statically ON. 0: Dynamic shunt ON/OFF mode based on port suspend. Bits (VESPOFFC, VESPONC) should never be set to 11b. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
12:11	0x2 RW	**CFGHYSCTL:** Hysteresis control for Classic Single Ended Rx 00 - 0mV 01 - 25mV 10 - 75mV (default) 11 - 125mV **Power Well:** SUS
10:9	0x1 RW	**CFGBIASCTL:** Bias control for Classic Differential Rx 00 - 50uA 01 - 60uA (default) 1X - 70uA **Power Well:** SUS
8	0x0 RW	**DISSLEWCTL:** DISSLEWCTL (DISSLEWCTL): Feed directly to SHIP or AFE : AFE Functional or Test Mode : Functional 0 - enable slew rate control during Classic Tx (default) 1 - disable slew rate control during Classic Tx **Power Well:** SUS
7:5	0x2 RW	**CLSLEWCTLPD:** Pull-Down Slew rate control for Classic Low Speed Tx 000 - slowest slew rate 001 - slow slew rate 010 - c73usb250_Normal (default) 100 - fast slew rate **Power Well:** SUS
4:2	0x2 RW	**CLSLEWCTLPU:** Slew rate control for Classic Low Speed Tx 000 - slowest slew rate 001 - slow slew rate 010 - c73usb250_Normal (default) 100 - fast slew rate **Power Well:** SUS
1:0	0x0 RW	**HSNPREDRVSEL:** Delay/skews strength Control for HS driver. Use together with HSSKEWSEL. npredrvsel(1) | npredrvsel(0) | Skew Offset 0 | 0 | No Skew (default) 0 | 1 | 30mV 1 | 0 | 40mV 1 | 1 | 50mV **Power Well:** SUS

7.14.101 USB2 PER PORT 2 (USB2_PER_PORT_2_PP2)—Offset 4326h

Access Method

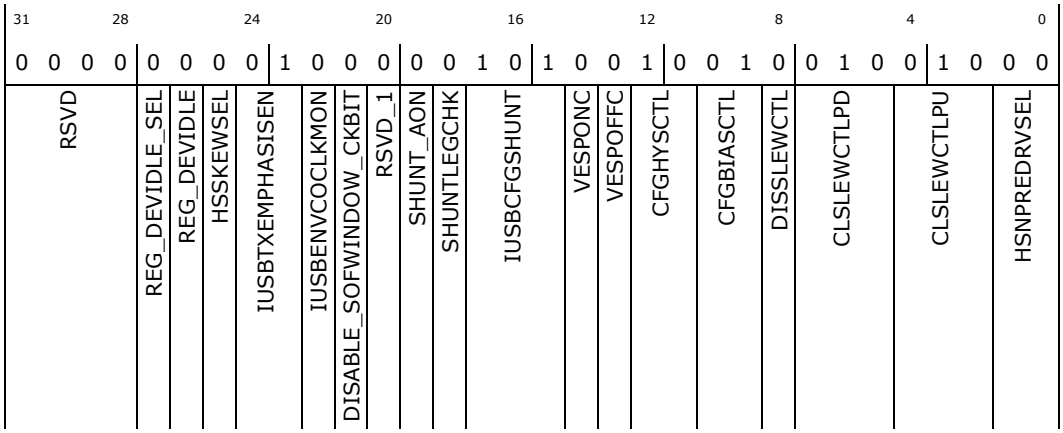
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4326h

Op Codes:

h - Read, h - Write

Default: 00829248h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RSVD:** RSVD **Power Well:** SUS
27	0x0 RW	**Manual Override of Device Idle Pullup Enable Select (REG_DEVIDLE_SEL):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To enable manual override on device Idle pullup enable. Enabling/Disabling come from reg_didle_force_onoff. 0: Disable Manual override on device idle pullup enable. Device idle pullup enable based on functional logic. **Power Well:** SUS
26	0x0 RW	**Device Idle Force On Off (REG_DEVIDLE):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To force turn on of device idle pullup enable. 0: To force turn off of device idle pullup enable. **Power Well:** SUS
25	0x0 RW	**HSSKEWSEL:** Select the skew direction for HS transition. Hsskewsel | Skew direction 0 | Delay HS Driver 0)1 Transition (default) 1 | Delay HS Driver 1)0 Transition **Power Well:** SUS
24:23	0x1 RW	**Per Port HS Transmitter Emphasis (IUSBTXEMPHASISEN):** Config bit (per port) Enables HS transmitter Emphasis for the respective ports Value Description 00 Emphasis OFF 01 De-emphasis ON (strength = TXISET+PETXISET) Default 10 Pre-emphasis ON (strength = TXISET+PETXISET) 11 Pre-emphasis and De-emphasis ON (strength = TXISET+PETXISET) **Power Well:** SUS
22	0x0 RW	**ADPLL clock monitoring through TX (IUSBENVCOCLKMON):** Signal to enable ADPLL clock monitoring through TX driver. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
21	0x0 RW	**DISABLE SOF WINDOW FOR DISCONNECT (DISABLE_SOFWINDOW_CKBIT):** 1: Enable sampling only during SOF window for disconnect. 0:Sampling not limited to SOF window. **Power Well:** SUS
20	0x0 RW	**RSVD (RSVD_1):** Reserved. **Power Well:** SUS
19	0x0 RW	**EOS Shunt always on (SHUNT_AON):** To force shunt FSM to always on and not run shunt detect FSM. **Power Well:** SUS
18	0x0 RW	**EOS Shunt legcheck (SHUNTLEGCHK):** To Enable EOS Shunt protection legcheck. **Power Well:** SUS
17:15	0x5 RW	**EOS Shunt configuration (IUSBCFGSHUNT):** Set Shunt strength control trim during VIHz 000 - Turn off shunt 100 - Lowest Shunt strength 101 - Low Shunt Strength 110 - Medium Shunt Strength 111 - High Shunt Strength **Power Well:** SUS
14	0x0 RW	**VIHz EOS Shunt Protection Off Control (VESPONC):** 1: Force the shunt to turn statically OFF. 0: Dynamic shunt ON/OFF mode based on port suspend. Bits (VESPOFFC, VESPONC) should never be set to 11b. **Power Well:** SUS
13	0x0 RW	**VIHz EOS Shunt Protection On Control (VESPOFFC):** 1: Force the shunt to turn statically ON. 0: Dynamic shunt ON/OFF mode based on port suspend. Bits (VESPOFFC, VESPONC) should never be set to 11b. **Power Well:** SUS
12:11	0x2 RW	**CFGHYSCTL:** Hysteresis control for Classic Single Ended Rx 00 - 0mV 01 - 25mV 10 - 75mV (default) 11 - 125mV **Power Well:** SUS
10:9	0x1 RW	**CFGBIASCTL:** Bias control for Classic Differential Rx 00 - 50uA 01 - 60uA (default) 1X - 70uA **Power Well:** SUS
8	0x0 RW	**DISSLEWCTL:** DISSLEWCTL (DISSLEWCTL): Feed directly to SHIP or AFE : AFE Functional or Test Mode : Functional 0 - enable slew rate control during Classic Tx (default) 1 - disable slew rate control during Classic Tx **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
7:5	0x2 RW	**CLSLEWCTLPD:** Pull-Down Slew rate control for Classic Low Speed Tx 000 - slowest slew rate 001 - slow slew rate 010 - c73usb250_Normal (default) 100 - fast slew rate **Power Well:** SUS
4:2	0x2 RW	**CLSLEWCTLPU:** Slew rate control for Classic Low Speed Tx 000 - slowest slew rate 001 - slow slew rate 010 - c73usb250_Normal (default) 100 - fast slew rate **Power Well:** SUS
1:0	0x0 RW	**HSNPREDRVSEL:** Delay/skews strength Control for HS driver. Use together with HSSKEWSEL. npredrvsel(1) | npredrvsel(0) | Skew Offset 0 | 0 | No Skew (default) 0 | 1 | 30mV 1 | 0 | 40mV 1 | 1 | 50mV **Power Well:** SUS

7.14.102 USB2 PER PORT 2 (USB2_PER_PORT_2_PP3)—Offset 4426h

Access Method

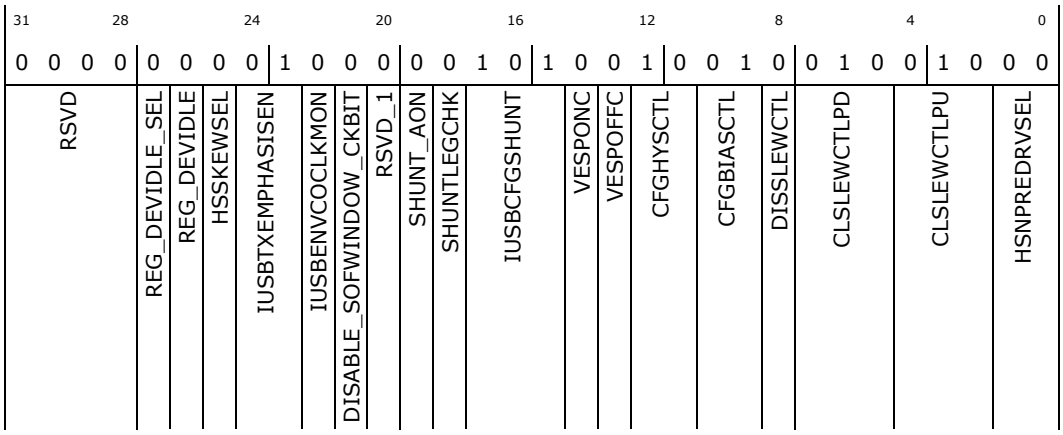
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4426h

Op Codes:

h - Read, h - Write

Default: 00829248h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RSVD:** RSVD **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
27	0x0 RW	**Manual Override of Device Idle Pullup Enable Select (REG_DEVIDLE_SEL):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To enable manual override on device Idle pullup enable. Enabling/Disabling come from reg_didle_force_onoff. 0: Disable Manual override on device idle pullup enable. Device idle pullup enable based on functional logic. **Power Well:** SUS
26	0x0 RW	**Device Idle Force On Off (REG_DEVIDLE):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To force turn on of device idle pullup enable. 0: To force turn off of device idle pullup enable. **Power Well:** SUS
25	0x0 RW	**HSSKEWSEL:** Select the skew direction for HS transition. Hsskewsel | Skew direction 0 | Delay HS Driver 0)1 Transition (default) 1 | Delay HS Driver 1)0 Transition **Power Well:** SUS
24:23	0x1 RW	**Per Port HS Transmitter Emphasis (IUSBTXEMPHASISEN):** Config bit (per port) Enables HS transmitter Emphasis for the respective ports Value Description 00 Emphasis OFF 01 De-emphasis ON (strength = TXISET+PETXISET) Default 10 Pre-emphasis ON (strength = TXISET+PETXISET) 11 Pre-emphasis and De-emphasis ON (strength = TXISET+PETXISET) **Power Well:** SUS
22	0x0 RW	**ADPLL clock monitoring through TX (IUSBENVCOCLKMON):** Signal to enable ADPLL clock monitoring through TX driver. **Power Well:** SUS
21	0x0 RW	**DISABLE SOF WINDOW FOR DISCONNECT (DISABLE_SOFWINDOW_CKBIT):** 1: Enable sampling only during SOF window for disconnect. 0:Sampling not limited to SOF window. **Power Well:** SUS
20	0x0 RW	**RSVD (RSVD_1):** Reserved. **Power Well:** SUS
19	0x0 RW	**EOS Shunt always on (SHUNT_AON):** To force shunt FSM to always on and not run shunt detect FSM. **Power Well:** SUS
18	0x0 RW	**EOS Shunt legcheck (SHUNTLEGCHK):** To Enable EOS Shunt protection legcheck. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
17:15	0x5 RW	**EOS Shunt configuration (IUSBCFGSHUNT):** Set Shunt strength control trim during VIHz 000 - Turn off shunt 100 - Lowest Shunt strength 101 - Low Shunt Strength 110 - Medium Shunt Strength 111 - High Shunt Strength **Power Well:** SUS
14	0x0 RW	**VIHz EOS Shunt Protection Off Control (VESPONC):** 1: Force the shunt to turn statically OFF. 0: Dynamic shunt ON/OFF mode based on port suspend. Bits (VESPOFFC, VESPONC) should never be set to 11b. **Power Well:** SUS
13	0x0 RW	**VIHz EOS Shunt Protection On Control (VESPOFFC):** 1: Force the shunt to turn statically ON. 0: Dynamic shunt ON/OFF mode based on port suspend. Bits (VESPOFFC, VESPONC) should never be set to 11b. **Power Well:** SUS
12:11	0x2 RW	**CFGHYSCTL:** Hysteresis control for Classic Single Ended Rx 00 - 0mV 01 - 25mV 10 - 75mV (default) 11 - 125mV **Power Well:** SUS
10:9	0x1 RW	**CFGBIASCTL:** Bias control for Classic Differential Rx 00 - 50uA 01 - 60uA (default) 1X - 70uA **Power Well:** SUS
8	0x0 RW	**DISSLEWCTL:** DISSLEWCTL (DISSLEWCTL): Feed directly to SHIP or AFE : AFE Functional or Test Mode : Functional 0 - enable slew rate control during Classic Tx (default) 1 - disable slew rate control during Classic Tx **Power Well:** SUS
7:5	0x2 RW	**CLSLEWCTLPD:** Pull-Down Slew rate control for Classic Low Speed Tx 000 - slowest slew rate 001 - slow slew rate 010 - c73usb250_Normal (default) 100 - fast slew rate **Power Well:** SUS
4:2	0x2 RW	**CLSLEWCTLPU:** Slew rate control for Classic Low Speed Tx 000 - slowest slew rate 001 - slow slew rate 010 - c73usb250_Normal (default) 100 - fast slew rate **Power Well:** SUS
1:0	0x0 RW	**HSNPREDRVSEL:** Delay/skews strength Control for HS driver. Use together with HSSKEWSEL. npredrvsel(1) | npredrvsel(0) | Skew Offset 0 | 0 | No Skew (default) 0 | 1 | 30mV 1 | 0 | 40mV 1 | 1 | 50mV **Power Well:** SUS

7.14.103 USB2 PER PORT 2 (USB2_PER_PORT_2_PP4)—Offset 4526h

Access Method

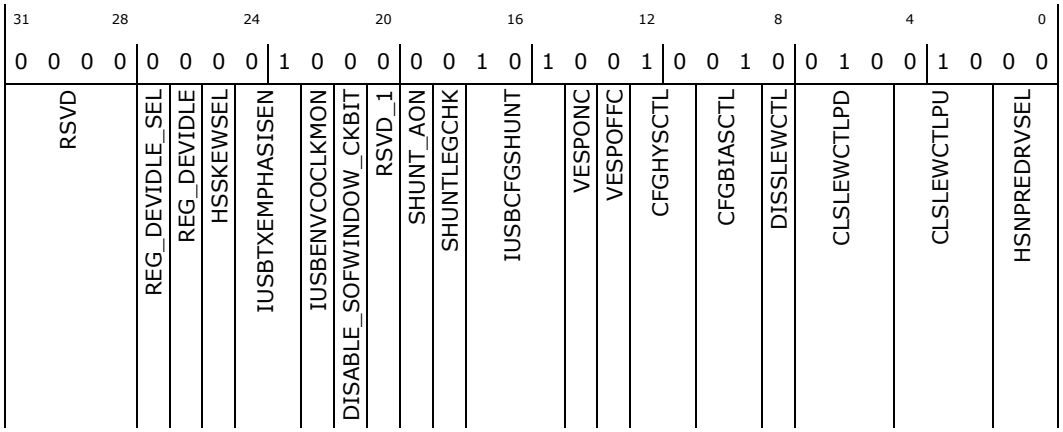
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4526h

Op Codes:

h - Read, h - Write

Default: 00829248h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RSVD:** RSVD **Power Well:** SUS
27	0x0 RW	**Manual Override of Device Idle Pullup Enable Select (REG_DEVIDLE_SEL):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To enable manual override on device Idle pullup enable. Enabling/Disabling come from reg_didle_force_onoff. 0: Disable Manual override on device idle pullup enable. Device idle pullup enable based on functional logic. **Power Well:** SUS
26	0x0 RW	**Device Idle Force On Off (REG_DEVIDLE):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Functional 1: To force turn on of device idle pullup enable. 0: To force turn off of device idle pullup enable. **Power Well:** SUS
25	0x0 RW	**HSSKEWSEL:** Select the skew direction for HS transition. Hsskewsel | Skew direction 0 | Delay HS Driver 0)1 Transition (default) 1 | Delay HS Driver 1)0 Transition **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
24:23	0x1 RW	**Per Port HS Transmitter Emphasis (IUSBTXEMPHASISEN):** Config bit (per port) Enables HS transmitter Emphasis for the respective ports Value Description 00 Emphasis OFF 01 De-emphasis ON (strength = TXISET+PETXISET) Default 10 Pre-emphasis ON (strength = TXISET+PETXISET) 11 Pre-emphasis and De-emphasis ON (strength = TXISET+PETXISET) **Power Well:** SUS
22	0x0 RW	**ADPLL clock monitoring through TX (IUSBENVCOCLKMON):** Signal to enable ADPLL clock monitoring through TX driver. **Power Well:** SUS
21	0x0 RW	**DISABLE SOF WINDOW FOR DISCONNECT (DISABLE_SOFWINDOW_CKBIT):** 1: Enable sampling only during SOF window for disconnect. 0:Sampling not limited to SOF window. **Power Well:** SUS
20	0x0 RW	**RSVD (RSVD_1):** Reserved. **Power Well:** SUS
19	0x0 RW	**EOS Shunt always on (SHUNT_AON):** To force shunt FSM to always on and not run shunt detect FSM. **Power Well:** SUS
18	0x0 RW	**EOS Shunt legcheck (SHUNTLEGCHK):** To Enable EOS Shunt protection legcheck. **Power Well:** SUS
17:15	0x5 RW	**EOS Shunt configuration (IUSBCFGSHUNT):** Set Shunt strength control trim during VIHz 000 - Turn off shunt 100 - Lowest Shunt strength 101 - Low Shunt Strength 110 - Medium Shunt Strength 111 - High Shunt Strength **Power Well:** SUS
14	0x0 RW	**VIHz EOS Shunt Protection Off Control (VESPONC):** 1: Force the shunt to turn statically OFF. 0: Dynamic shunt ON/OFF mode based on port suspend. Bits (VESPOFFC, VESPONC) should never be set to 11b. **Power Well:** SUS
13	0x0 RW	**VIHz EOS Shunt Protection On Control (VESPOFFC):** 1: Force the shunt to turn statically ON. 0: Dynamic shunt ON/OFF mode based on port suspend. Bits (VESPOFFC, VESPONC) should never be set to 11b. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
12:11	0x2 RW	**CFGHYSCTL:** Hysteresis control for Classic Single Ended Rx 00 - 0mV 01 - 25mV 10 - 75mV (default) 11 - 125mV **Power Well:** SUS
10:9	0x1 RW	**CFGBIASCTL:** Bias control for Classic Differential Rx 00 - 50uA 01 - 60uA (default) 1X - 70uA **Power Well:** SUS
8	0x0 RW	**DISSLEWCTL:** DISSLEWCTL (DISSLEWCTL): Feed directly to SHIP or AFE : AFE Functional or Test Mode : Functional 0 - enable slew rate control during Classic Tx (default) 1 - disable slew rate control during Classic Tx **Power Well:** SUS
7:5	0x2 RW	**CLSLEWCTLPD:** Pull-Down Slew rate control for Classic Low Speed Tx 000 - slowest slew rate 001 - slow slew rate 010 - c73usb250_Normal (default) 100 - fast slew rate **Power Well:** SUS
4:2	0x2 RW	**CLSLEWCTLPU:** Slew rate control for Classic Low Speed Tx 000 - slowest slew rate 001 - slow slew rate 010 - c73usb250_Normal (default) 100 - fast slew rate **Power Well:** SUS
1:0	0x0 RW	**HSNPREDRVSEL:** Delay/skews strength Control for HS driver. Use together with HSSKEWSEL. npredrvsel(1) | npredrvsel(0) | Skew Offset 0 | 0 | No Skew (default) 0 | 1 | 30mV 1 | 0 | 40mV 1 | 1 | 50mV **Power Well:** SUS

7.14.104 USB2 PLL3 (USB2_PLL3)—Offset 7F27h

Access Method

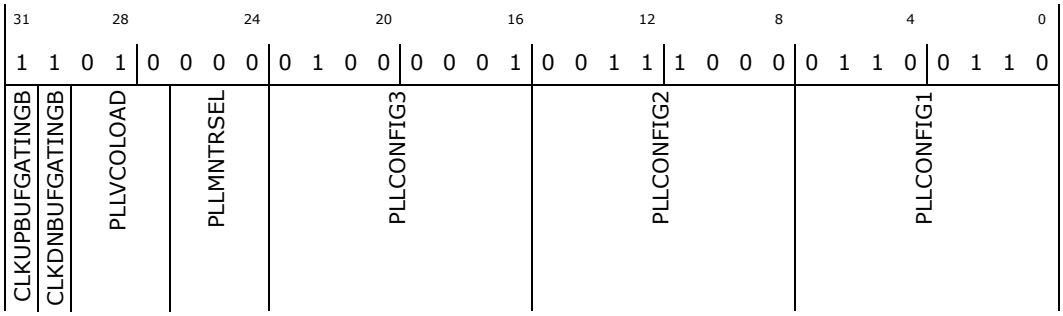
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 7F27h

Op Codes:

h - Read, h - Write

Default: D0413866h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**CLKUPBUFGATINGB:** Power saving on upper lane clocking. Set to 0b clock gates all clock buffers to upper lane AFE ports. Default is 1b. This bit does not gate coreclk480. **Power Well:** SUS
30	0x1 RW	**CLKDNBUFGATINGB:** Power saving on lower lane clocking. Set to 0b clock gates all clock buffers to lower lane AFE ports. Default is 1b. This bit does not gate coreclk480. **Power Well:** SUS
29:27	0x2 RW	**PLLVCOLOAD:** Controls the amount of capacitance that loads the VCO. These bits should be set by logic based on vco target frequency. These bits can also optimize power/jitter tradeoffs in case its needed For USBPLL the pins control power/jitter trade off (000 least power/most jitter). ipllvcoload(2:0) LBW VCO (GHz) HBW VCO (GHz) 000 3.3 - 3.6 3.5 - 4.267 001 2.75 - 3.3 3.0 - 3.5 010 2.25 - 2.75 2.5 - 3.0 011 1.8 - 2.25 2.133 - 2.5 Default: According to default VCO frequency. For USBPLL default is 010 the VCO. **Power Well:** SUS
26:24	0x0 RW	**PLLMNTRSEL:** PLL analog monitor mux select mntrsel opllmntr(1) opllmntr(0) 000 (default) VSS VSS 001 Vvcr Ivcr 010 Vctrl_pbias Ivco_tail 011 Vvcr_diode Ivcr_diode 100 Vnbias_ext Inbias 101 Vdrain_nbias Inbias 110 V1dac vccd 111 V1p vcca Default: 8b000 **Power Well:** SUS
23:16	0x41 RW	**PLLCONFIG3:** General PLL configuration signals #3 (7:6) - startup ramp (5) - sleep/yank counter (4:3) - fast lock mode (2) - new startup DAC (1) - use 50uA current reference (0) - enable vco phases 1 and 3 Default: 8 b01000001 **Power Well:** SUS
15:8	0x38 RW	**PLLCONFIG2:** General PLL configuration signals #2 (7:5) - lock threshold (4:3) - lock div select (2:0) - lock counter Default: 8 b00111000 **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x66 RW	**PLLCONFIG1:** General PLL configuration signals #1 (7:5) - residual pulse width (4:1) - chopper width control (0) - open loop mode enable Default: 8 b01100110 **Power Well:** SUS

7.14.105 PER PORT LOOPBACK CONTROL (PER_PORT_LOOPBACK_CONTROL_PP0)—Offset 4128h

Access Method

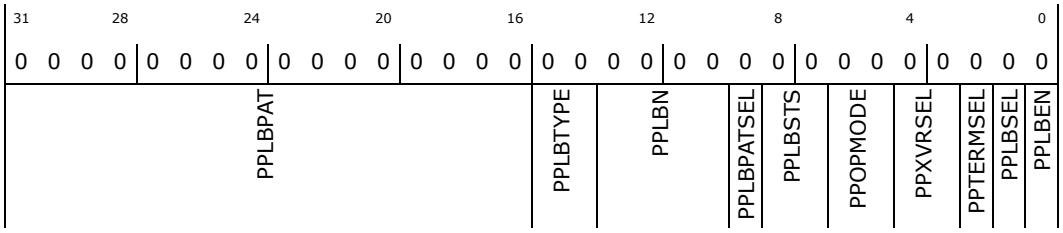
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4128h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Per port Loopback Pattern (PPLBPAT):** 2-byte pattern used during loopback. Note: This 2-byte pattern will be replicated to the upper 2-byte to form the DW pattern. This field is only applicable when PPLBPATSEL = 0b. **Power Well:** SUS
15:14	0x0 RW	**Per port Loopback Type (PPLBTYPE):** Loopback Type in test mode. This signal selects between DNELB and ANELB, and will only take effect if DTUTMILPBKEN is set. 00b: Digital Near-End Loopback (DNELB) 01b: Analog Near-End Loopback (ANELB) 10b: Analog Far-End Loopback (AFELB) 11b: Reserved **Power Well:** SUS
13:10	0x0 RW	**Per Port Loop Number (PPLBN):** Number of repeatable fixed pattern within a packet. Note: Connect register bit 3 to counter bit 7, register bit 2 to counter bit 5, register bit 1 to counter bit 3, register bit 0 to counter bit 1. Counter bits 6, 4, 2 and 0 will be tied off to 0. Hence, the programmable loop number shall be: 0000b: 0 loop 0001b: 2 loops 0010b: 8 loops 0011b: 10 loops 1100b: 160 loops 1101b: 162 loops 1110b: 168 loops 1111b: 170 loops (max) **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RW	**Per port Loopback Pattern Select (PPLBPATSEL):** Near end loopback pattern generation type: 0b: Fixed pattern 1b: USB2 test packet **Power Well:** SUS
8:7	0x0 RW/1C	**Per Port Loopback Status Reporting (PPLBSTS):** 00b: Loopback not started 01b: Loopback Pass 10b: Pattern mismatch 11b: Receive error SW writes a 11b to clear the status back to 00b. **Power Well:** SUS
6:5	0x0 RW	**Per Port Operational Mode (PPOPMODE):** Operational Mode in test mode. These signals select between various operational modes: 00b: c73usb250_Normal Operation 01b: Non-Driving 10b: Disable Bit Stuffing and NRZI encoding 11b: Reserved This field is only applicable when PPLBSEL = 1b. **Power Well:** SUS
4:3	0x0 RW	**Per Port Transceiver Select (PPXVRSEL):** This signal selects between the LS, FS and HS transceivers: 00b: HS transceiver enabled 01b: FS transceiver enabled 10b: LS transceiver enabled 11b: Reserved This field is only applicable when PPLBSEL = 1b. **Power Well:** SUS
2	0x0 RW	**Per Port Termination Select (PPTERMSEL):** Termination Select in test mode. This signal selects between the FS and HS terminations: 0b: HS termination enabled 1b: FS termination enabled This field is only applicable when PPLBSEL = 1b. **Power Well:** SUS
1	0x0 RW	**Per Port DFX Loopback Select (PPLBSEL):** Loopback select to choose loopback path. 1: select loopback path 0: select functional path **Power Well:** SUS
0	0x0 RW	**Per Port Loopback Enable (PPLBEN):** This bit will enable loopback test mode. 1: Enable loopback 0: Disable loopback **Power Well:** SUS

7.14.106 PER PORT LOOPBACK CONTROL (PER_PORT_LOOPBACK_CONTROL_PP1)—Offset 4228h

Access Method

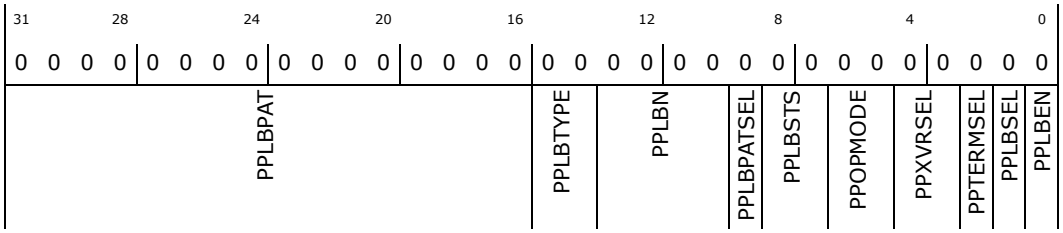
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4228h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Per port Loopback Pattern (PPLBPAT):** 2-byte pattern used during loopback. Note: This 2-byte pattern will be replicated to the upper 2-byte to form the DW pattern. This field is only applicable when PPLBPATSEL = 0b. **Power Well:** SUS
15:14	0x0 RW	**Per port Loopback Type (PPLBTYPE):** Loopback Type in test mode. This signal selects between DNELB and ANELB, and will only take effect if DTUTMILPBKEN is set. 00b: Digital Near-End Loopback (DNELB) 01b: Analog Near-End Loopback (ANELB) 10b: Analog Far-End Loopback (AFELB) 11b: Reserved **Power Well:** SUS
13:10	0x0 RW	**Per Port Loop Number (PPLBN):** Number of repeatable fixed pattern within a packet. Note: Connect register bit 3 to counter bit 7, register bit 2 to counter bit 5, register bit 1 to counter bit 3, register bit 0 to counter bit 1. Counter bits 6, 4, 2 and 0 will be tied off to 0. Hence, the programmable loop number shall be: 0000b: 0 loop 0001b: 2 loops 0010b: 8 loops 0011b: 10 loops 1100b: 160 loops 1101b: 162 loops 1110b: 168 loops 1111b: 170 loops (max) **Power Well:** SUS
9	0x0 RW	**Per port Loopback Pattern Select (PPLBPATSEL):** Near end loopback pattern generation type: 0b: Fixed pattern 1b: USB2 test packet **Power Well:** SUS
8:7	0x0 RW/1C	**Per Port Loopback Status Reporting (PPLBSTS):** 00b: Loopback not started 01b: Loopback Pass 10b: Pattern mismatch 11b: Receive error SW writes a 11b to clear the status back to 00b. **Power Well:** SUS
6:5	0x0 RW	**Per Port Operational Mode (PPOPMODE):** Operational Mode in test mode. These signals select between various operational modes: 00b: c73usb250_Normal Operation 01b: Non-Driving 10b: Disable Bit Stuffing and NRZI encoding 11b: Reserved This field is only applicable when PPLBSEL = 1b. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
4:3	0x0 RW	**Per Port Transceiver Select (PPXVRSEL):** This signal selects between the LS, FS and HS transceivers: 00b: HS transceiver enabled 01b: FS transceiver enabled 10b: LS transceiver enabled 11b: Reserved This field is only applicable when PPLBSEL = 1b. **Power Well:** SUS
2	0x0 RW	**Per Port Termination Select (PPTERMSEL):** Termination Select in test mode. This signal selects between the FS and HS terminations: 0b: HS termination enabled 1b: FS termination enabled This field is only applicable when PPLBSEL = 1b. **Power Well:** SUS
1	0x0 RW	**Per Port DFX Loopback Select (PPLBSEL):** Loopback select to choose loopback path. 1: select loopback path 0: select functional path **Power Well:** SUS
0	0x0 RW	**Per Port Loopback Enable (PPLBEN):** This bit will enable loopback test mode. 1: Enable loopback 0: Disable loopback **Power Well:** SUS

7.14.107 PER PORT LOOPBACK CONTROL (PER_PORT_LOOPBACK_CONTROL_PP2)—Offset 4328h

Access Method

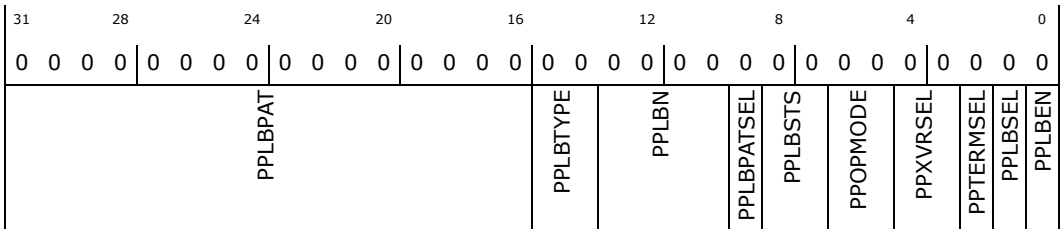
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4328h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Per port Loopback Pattern (PPLBPAT):** 2-byte pattern used during loopback. Note: This 2-byte pattern will be replicated to the upper 2-byte to form the DW pattern. This field is only applicable when PPLBPATSEL = 0b. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RW	**Per port Loopback Type (PPLBTYPE):** Loopback Type in test mode. This signal selects between DNELB and ANELB, and will only take effect if DTUTMILPBKEN is set. 00b: Digital Near-End Loopback (DNELB) 01b: Analog Near-End Loopback (ANELB) 10b: Analog Far-End Loopback (AFELB) 11b: Reserved **Power Well:** SUS
13:10	0x0 RW	**Per Port Loop Number (PPLBN):** Number of repeatable fixed pattern within a packet. Note: Connect register bit 3 to counter bit 7, register bit 2 to counter bit 5, register bit 1 to counter bit 3, register bit 0 to counter bit 1. Counter bits 6, 4, 2 and 0 will be tied off to 0. Hence, the programmable loop number shall be: 0000b: 0 loop 0001b: 2 loops 0010b: 8 loops 0011b: 10 loops 1100b: 160 loops 1101b: 162 loops 1110b: 168 loops 1111b: 170 loops (max) **Power Well:** SUS
9	0x0 RW	**Per port Loopback Pattern Select (PPLBPATSEL):** Near end loopback pattern generation type: 0b: Fixed pattern 1b: USB2 test packet **Power Well:** SUS
8:7	0x0 RW/1C	**Per Port Loopback Status Reporting (PPLBSTS):** 00b: Loopback not started 01b: Loopback Pass 10b: Pattern mismatch 11b: Receive error SW writes a 11b to clear the status back to 00b. **Power Well:** SUS
6:5	0x0 RW	**Per Port Operational Mode (PPOPMODE):** Operational Mode in test mode. These signals select between various operational modes: 00b: c73usb250_Normal Operation 01b: Non-Driving 10b: Disable Bit Stuffing and NRZI encoding 11b: Reserved This field is only applicable when PPLBSEL = 1b. **Power Well:** SUS
4:3	0x0 RW	**Per Port Transceiver Select (PPXVRSEL):** This signal selects between the LS, FS and HS transceivers: 00b: HS transceiver enabled 01b: FS transceiver enabled 10b: LS transceiver enabled 11b: Reserved This field is only applicable when PPLBSEL = 1b. **Power Well:** SUS
2	0x0 RW	**Per Port Termination Select (PPTERMSEL):** Termination Select in test mode. This signal selects between the FS and HS terminations: 0b: HS termination enabled 1b: FS termination enabled This field is only applicable when PPLBSEL = 1b. **Power Well:** SUS
1	0x0 RW	**Per Port DFX Loopback Select (PPLBSEL):** Loopback select to choose loopback path. 1: select loopback path 0: select functional path **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**Per Port Loopback Enable (PPLBEN):** This bit will enable loopback test mode. 1: Enable loopback 0: Disable loopback **Power Well:** SUS

7.14.108 PER PORT LOOPBACK CONTROL (PER_PORT_LOOPBACK_CONTROL_PP3)—Offset 4428h

Access Method

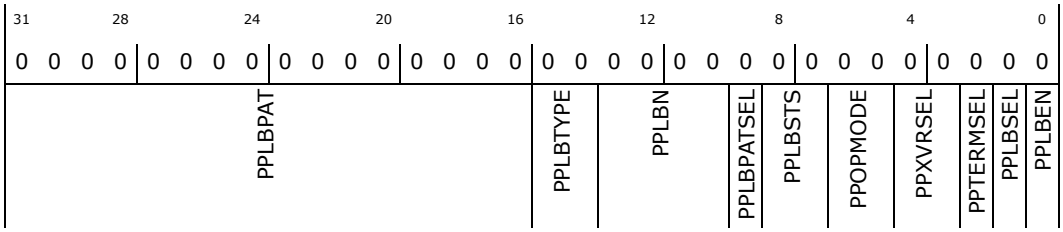
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4428h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Per port Loopback Pattern (PPLBPAT):** 2-byte pattern used during loopback. Note: This 2-byte pattern will be replicated to the upper 2-byte to form the DW pattern. This field is only applicable when PPLBPATSEL = 0b. **Power Well:** SUS
15:14	0x0 RW	**Per port Loopback Type (PPLBTYPE):** Loopback Type in test mode. This signal selects between DNELB and ANELB, and will only take effect if DTUTMILPBKEN is set. 00b: Digital Near-End Loopback (DNELB) 01b: Analog Near-End Loopback (ANELB) 10b: Analog Far-End Loopback (AFELB) 11b: Reserved **Power Well:** SUS
13:10	0x0 RW	**Per Port Loop Number (PPLBN):** Number of repeatable fixed pattern within a packet. Note: Connect register bit 3 to counter bit 7, register bit 2 to counter bit 5, register bit 1 to counter bit 3, register bit 0 to counter bit 1. Counter bits 6, 4, 2 and 0 will be tied off to 0. Hence, the programmable loop number shall be: 0000b: 0 loop 0001b: 2 loops 0010b: 8 loops 0011b: 10 loops 1100b: 160 loops 1101b: 162 loops 1110b: 168 loops 1111b: 170 loops (max) **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RW	**Per port Loopback Pattern Select (PPLBPATSEL):** Near end loopback pattern generation type: 0b: Fixed pattern 1b: USB2 test packet **Power Well:** SUS
8:7	0x0 RW/1C	**Per Port Loopback Status Reporting (PPLBSTS):** 00b: Loopback not started 01b: Loopback Pass 10b: Pattern mismatch 11b: Receive error SW writes a 11b to clear the status back to 00b. **Power Well:** SUS
6:5	0x0 RW	**Per Port Operational Mode (PPOPMODE):** Operational Mode in test mode. These signals select between various operational modes: 00b: c73usb250_Normal Operation 01b: Non-Driving 10b: Disable Bit Stuffing and NRZI encoding 11b: Reserved This field is only applicable when PPLBSEL = 1b. **Power Well:** SUS
4:3	0x0 RW	**Per Port Transceiver Select (PPXVRSEL):** This signal selects between the LS, FS and HS transceivers: 00b: HS transceiver enabled 01b: FS transceiver enabled 10b: LS transceiver enabled 11b: Reserved This field is only applicable when PPLBSEL = 1b. **Power Well:** SUS
2	0x0 RW	**Per Port Termination Select (PPTERMSEL):** Termination Select in test mode. This signal selects between the FS and HS terminations: 0b: HS termination enabled 1b: FS termination enabled This field is only applicable when PPLBSEL = 1b. **Power Well:** SUS
1	0x0 RW	**Per Port DFX Loopback Select (PPLBSEL):** Loopback select to choose loopback path. 1: select loopback path 0: select functional path **Power Well:** SUS
0	0x0 RW	**Per Port Loopback Enable (PPLBEN):** This bit will enable loopback test mode. 1: Enable loopback 0: Disable loopback **Power Well:** SUS

7.14.109 PER PORT LOOPBACK CONTROL (PER_PORT_LOOPBACK_CONTROL_PP4)—Offset 4528h

Access Method

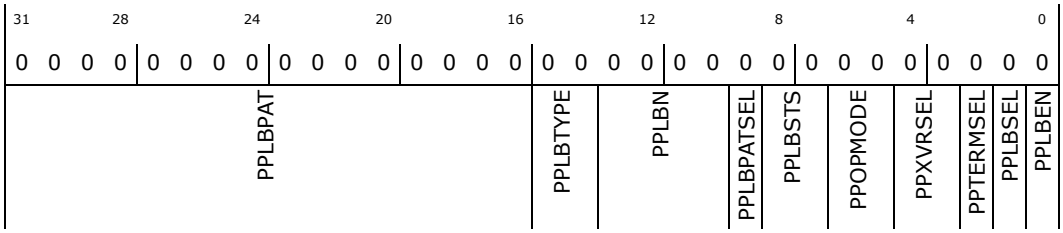
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4528h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Per port Loopback Pattern (PPLBPAT):** 2-byte pattern used during loopback. Note: This 2-byte pattern will be replicated to the upper 2-byte to form the DW pattern. This field is only applicable when PPLBPATSEL = 0b. **Power Well:** SUS
15:14	0x0 RW	**Per port Loopback Type (PPLBTYPE):** Loopback Type in test mode. This signal selects between DNELB and ANELB, and will only take effect if DTUTMILPBKEN is set. 00b: Digital Near-End Loopback (DNELB) 01b: Analog Near-End Loopback (ANELB) 10b: Analog Far-End Loopback (AFELB) 11b: Reserved **Power Well:** SUS
13:10	0x0 RW	**Per Port Loop Number (PPLBN):** Number of repeatable fixed pattern within a packet. Note: Connect register bit 3 to counter bit 7, register bit 2 to counter bit 5, register bit 1 to counter bit 3, register bit 0 to counter bit 1. Counter bits 6, 4, 2 and 0 will be tied off to 0. Hence, the programmable loop number shall be: 0000b: 0 loop 0001b: 2 loops 0010b: 8 loops 0011b: 10 loops 1100b: 160 loops 1101b: 162 loops 1110b: 168 loops 1111b: 170 loops (max) **Power Well:** SUS
9	0x0 RW	**Per port Loopback Pattern Select (PPLBPATSEL):** Near end loopback pattern generation type: 0b: Fixed pattern 1b: USB2 test packet **Power Well:** SUS
8:7	0x0 RW/1C	**Per Port Loopback Status Reporting (PPLBSTS):** 00b: Loopback not started 01b: Loopback Pass 10b: Pattern mismatch 11b: Receive error SW writes a 11b to clear the status back to 00b. **Power Well:** SUS
6:5	0x0 RW	**Per Port Operational Mode (PPOPMODE):** Operational Mode in test mode. These signals select between various operational modes: 00b: c73usb250_Normal Operation 01b: Non-Driving 10b: Disable Bit Stuffing and NRZI encoding 11b: Reserved This field is only applicable when PPLBSEL = 1b. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
4:3	0x0 RW	**Per Port Transceiver Select (PPXVRSEL):** This signal selects between the LS, FS and HS transceivers: 00b: HS transceiver enabled 01b: FS transceiver enabled 10b: LS transceiver enabled 11b: Reserved This field is only applicable when PPLBSEL = 1b. **Power Well:** SUS
2	0x0 RW	**Per Port Termination Select (PPTERMSEL):** Termination Select in test mode. This signal selects between the FS and HS terminations: 0b: HS termination enabled 1b: FS termination enabled This field is only applicable when PPLBSEL = 1b. **Power Well:** SUS
1	0x0 RW	**Per Port DFX Loopback Select (PPLBSEL):** Loopback select to choose loopback path. 1: select loopback path 0: select functional path **Power Well:** SUS
0	0x0 RW	**Per Port Loopback Enable (PPLBEN):** This bit will enable loopback test mode. 1: Enable loopback 0: Disable loopback **Power Well:** SUS

7.14.110 GLB ADP OFFSET REG (GLB_ADP_OFFSET_REG)—Offset 4029h

Access Method

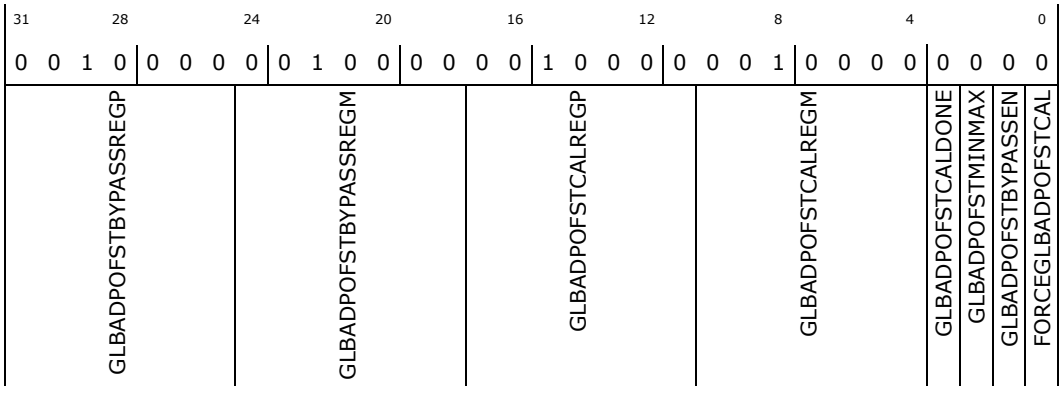
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4029h

Op Codes:

h - Read, h - Write

Default: 20408100h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x10 RW	**GLBADPOFSTBYPASSREGP:** Software programmable. It is used during test mode. The values of glbbADPofstcalreg(9:5) will be overwritten by this register when glbADPofstbypassen is asserted 1. **Power Well:** SUS
24:18	0x10 RW	**GLBADPOFSTBYPASSREGM:** Software programmable. It is used during test mode. The values of glbADPofstcalreg(4:0) will be overwritten by this register when glbADPofstbypassen is asserted 1. **Power Well:** SUS
17:11	0x10 RO	**GLBADPOFSTCALREGP:** 5-bit register that stores the ADP probe comparator offset cancellation left-side code. This 5-bit register must be initialized to default value prior to every calibration routine (before GLBADPOFSTCALEN asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to right-register. This is to reduce the signal common mode variation to impact to circuit performance. If oadpprbusblvgen output is low when FORCEGLBADPOFSTCAL asserted: regP count down -) regM count up -) regP count down -) until oadpprbusblvgen output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If oadpprbusblvgen output is high when FORCEGLBADPOFSTCAL asserted: regM countdown -) regP count up -) regM countdown -) until oadpprbusblvgen output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. **Power Well:** SUS
10:4	0x10 RO	**GLBADPOFSTCALREGM:** 5-bit register that stores the ADP probe comparator offset cancellation right-side code. This 5-bit register must be initialized to default value prior to every calibration routine (before GLBADPOFSTCALEN asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to left-register. This is to reduce the signal common mode variation to impact to circuit performance. If oadpprbusblvgen output is low when FORCEGLBADPOFSTCAL asserted: regP count down -) regM count up -) regP count down -) until oadpprbusblvgen output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If oadpprbusblvgen output is high when FORCEGLBADPOFSTCAL asserted: regM countdown -) regP count up -) regM countdown -) until oadpprbusblvgen output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. **Power Well:** SUS
3	0x0 RO	**GLBADPOFSTCALDONE:** This bit is set to 1b by state machine to indicate the calibration completion. This bit need to be cleared when FORCEGLBADPOFSTCAL (starting of next calibration cycle). **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW/1C	**GLBADPOFSTMINMAX:** Flag bit when glbADPofstcalregp OR glbADPofstcalregm offset counter reach the max limit set by the product. For P1271 is when it reaches 01111b or 00000b. This is to prevent roll back when the variation is out of range. **Power Well:** SUS
1	0x0 RW	**GLBADPOFSTBYPASSEN:** Software programmable. The values of glbADPofstcalreg(9:5) and glbADPofstcalreg(4:0) will be overwritten by ADPofstbypassregp and glbADPofstbypassregm respectively when glbADPofstbypassen is asserted 1. **Power Well:** SUS
0	0x0 WO	**FORCEGLBADPOFSTCAL:** When set to 1b, this will force ADP probe detect comparator offset cancellation Finite State Machine to start calibrating. BIOS has to wait for sufficient time for the calibration complete. **Power Well:** SUS

7.14.111 GLB VBUS OFFSET REG (GLB_VBUS_OFFSET_REG)—Offset 402Ah

Access Method

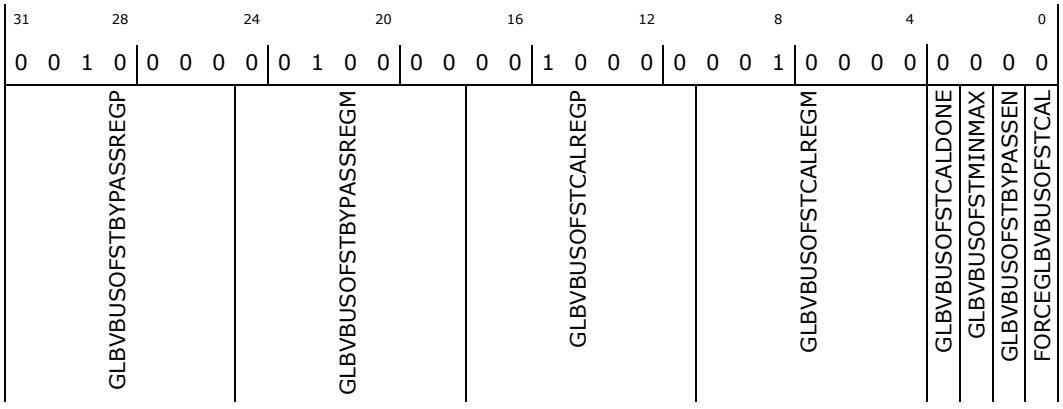
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 402Ah

Op Codes:

h - Read, h - Write

Default: 20408100h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x10 RW	**GLBVBUSOFSTBYPASSREGP:** Software programmable. It is used during test mode. The values of glbVBUSofstcalreg(9:5) will be overwritten by this register when glbVBUSofstbypassen is asserted 1. **Power Well:** SUS
24:18	0x10 RW	**GLBVBUSOFSTBYPASSREGM:** Software programmable. It is used during test mode. The values of glbVBUSofstcalreg(4:0) will be overwritten by this register when glbVBUSofstbypassen is asserted 1. **Power Well:** SUS
17:11	0x10 RO	**GLBVBUSOFSTCALREGP:** 5-bit register that stores the VBUS valid comparator offset cancellation left-side code. This 5-bit register must be initialized to default value prior to every calibration routine (before GLBVBUSOFSTCALEN asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to right-register. This is to reduce the signal common mode variation to impact to circuit performance. If ovbusvldusblvgen output is low when FORCEGLBVBUSOFSTCAL asserted: regP count down -) regM count up -) regP count down -) until ovbusvldusblvgen output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If ovbusvldusblvgen output is high when FORCEGLBVBUSOFSTCAL asserted: regM countdown -) regP count up -) regM countdown -) until ovbusvldusblvgen output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. **Power Well:** SUS
10:4	0x10 RO	**GLBVBUSOFSTCALREGM:** 5-bit register that stores the VBUS valid comparator offset cancellation right-side code. This 5-bit register must be initialized to default value prior to every calibration routine (before GLBVBUSOFSTCALEN asserted). The binary value is step through sequentially, in alternating cycle and in opposite polarity with respect to left-register. This is to reduce the signal common mode variation to impact to circuit performance. If ovbusvldusblvgen output is low when FORCEGLBVBUSOFSTCAL asserted: regP count down -) regM count up -) regP count down -) until ovbusvldusblvgen output produce a 0-1 transition. The register is manipulated by FSM to produce 101010 sequences to indicate calibration completion. If ovbusvldusblvgen output is high when FORCEGLBVBUSOFSTCAL asserted: regM countdown -) regP count up -) regM countdown -) until ovbusvldusblvgen output produce a 0-1 transition. The register is manipulated by FSM to produce 010101 sequences to indicate calibration completion. **Power Well:** SUS
3	0x0 RO	**GLBVBUSOFSTCALDONE:** This bit is set to 1b by state machine to indicate the calibration completion. This bit need to be cleared when FORCEGLBVBUSOFSTCAL (starting of next calibration cycle). **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW/1C	**GLBVBUSOFSTMINMAX:** Flag bit when glbVBUSofstcalregp OR glbVBUSofstcalregm offset counter reach the max limit set by the product. For P1271 is when it reaches 01111b or 00000b. This is to prevent roll back when the variation is out of range. **Power Well:** SUS
1	0x0 RW	**GLBVBUSOFSTBYPASSEN:** Software programmable. The values of glbVBUSofstcalreg(9:5) and glbVBUSofstcalreg(4:0) will be overwritten by glbVBUSofstbypassregp and glbVBUSofstbypassregm respectively when glbVBUSofstbypassen is asserted 1. **Power Well:** SUS
0	0x0 WO	**FORCEGLBVBUSOFSTCAL:** When set to 1b, this will force VBUS valid detect comparator offset cancellation Finite State Machine to start calibrating. BIOS has to wait for sufficient time for the calibration complete. **Power Well:** SUS

7.14.112 GLB ADP VBUS COMP REG (GLB_ADP_VBUS_COMP_REG)—Offset 402Bh

Access Method

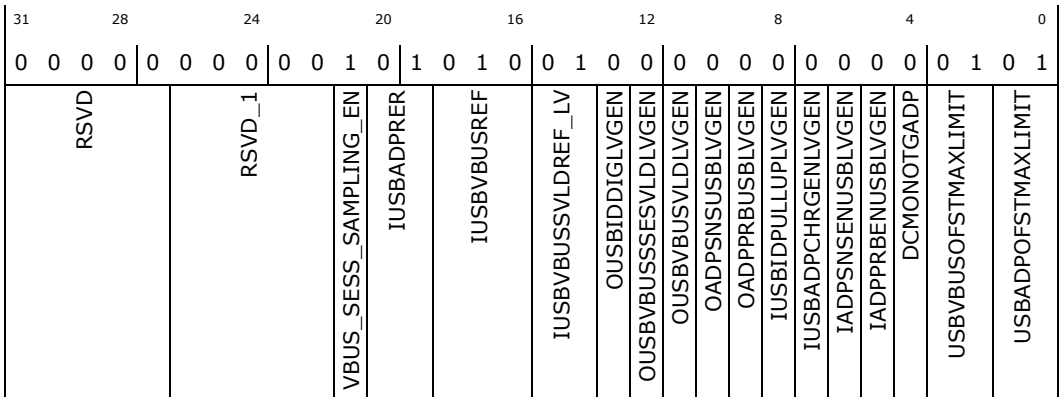
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 402Bh

Op Codes:

h - Read, h - Write

Default: 002A4005h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
26:22	0x0 RW	**RESERVED (RSVD_1):** Reserved. **Power Well:** SUS
21	0x1 RW	**VBUS SESSION SAMPLING ENABLE (VBUS_SESS_SAMPLING_EN):** Enable vbus session comparator for vbus and session sampling. **Power Well:** SUS
20:19	0x1 RW	**IUSBADPRER:** Adp vref select signal 2'b00 = 0.65 2'b01 = 0.675 2'b10 = 0.7 2'b11 = 0.725 **Power Well:** SUS
18:16	0x2 RW	**IUSBVBUSREF:** Vbus vref select signal 3'b000 = 0.7 3'b001 = 0.75 3'b010 = 0.8 3'b011 = 0.85 3'b100 = 0.9 3'b101 = 0.95 3'b110 = xxxx 3'b111 = xxxx **Power Well:** SUS
15:14	0x1 RW	**IUSBVBUSSVLDREF_LV:** Vbus sense valid vref select signal 2'b00 = 0.2 2'b01 = 0.25 2'b10 = 0.3 2'b11 = 0.4 **Power Well:** SUS
13	0x0 RO	**OUSBIDDIGLVGEN:** OTG ID dig status readout. **Power Well:** SUS
12	0x0 RO	**OUSBVBUSSSESVLDLVGEN:** VBUS sense status readout. **Power Well:** SUS
11	0x0 RO	**OUSBVBUSVLDLVGEN:** VBUS valid status readout. **Power Well:** SUS
10	0x0 RO	**OADPSNSUSBLVGEN:** ADP sense status readout. **Power Well:** SUS
9	0x0 RO	**OADPPRBUSBLVGEN:** ADP probe status readout. **Power Well:** SUS
8	0x0 RW	**IUSBIDPULLUPLVGEN:** OTG ID dig pullup enable for DCIO. **Power Well:** SUS
7	0x0 RW	**IUSBADPCHRGENLVGEN:** ADP charge enable for DCIO. **Power Well:** SUS
6	0x0 RW	**IADPSNSENUSBLVGEN:** ADP sense enable for DCIO. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**IADPPRBENUSBLVGEN:** ADP probe enable for DCIO. **Power Well:** SUS
4	0x0 RW	**DC OTG ADP MONITOR (DCMONOTGADP):** Enable DC monitor for OTG and ADP. **Power Well:** SUS
3:2	0x1 RW	**USBVBUSOFSTMAXLIMIT:** This register defines the counter limit for the VBUS valid detector offset cancellation SM. 11b = not supporting 10b = not supporting 01b = 5-bits 00b = 4-bits **Power Well:** SUS
1:0	0x1 RW	**USBADPOFSTMAXLIMIT:** This register defines the counter limit for the ADP probe detector offset cancellation SM. 11b = Not supporting 10b = Not supporting 01b = 5-bits 00b = 4-bits **Power Well:** SUS

7.14.113 USB2 GLOBAL PORT 2 (USB2_GLOBAL_PORT_2)—Offset 402Ch

Access Method

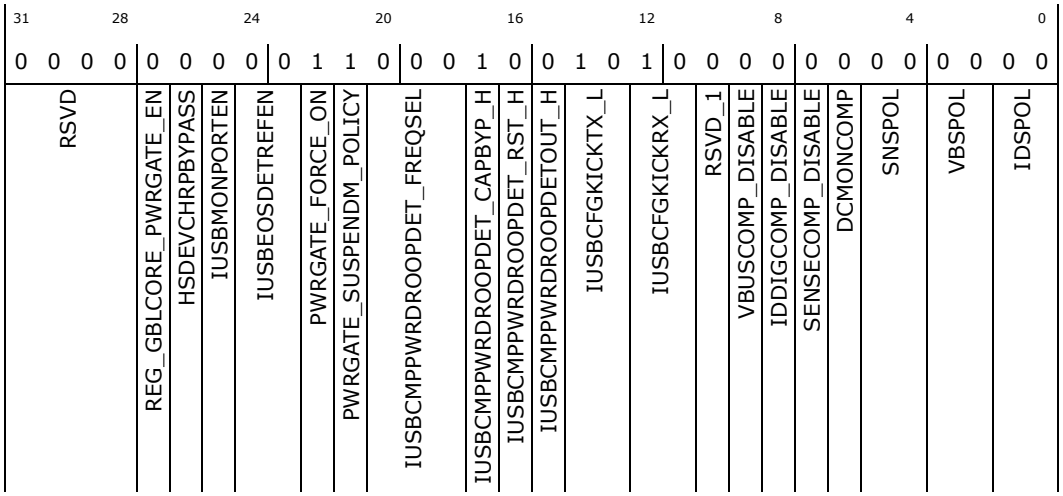
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 402Ch

Op Codes:

h - Read, h - Write

Default: 00625000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**RESERVED (RSVD):** Reserved. **Power Well:** SUS
27	0x0 RW	**Global lane core power gating enable (REG_GBLCORE_PWRGATE_EN):** Feed directly to SHIP or AFE: AFE Functional or Test Mode: Test Mode 1: Enable global lane core well shuf off once all ports are off. 0:Disable global lane shut off when all per-port are off. ie. Global lane will remain on and not autonomously shuf off once all ports are off. **Power Well:** SUS
26	0x0 RW	**HSDEVCHRPBYPASS:** Enable to bypass the pull-up on Dm pin during device chirp K mode. **Power Well:** SUS
25	0x0 RW	**Enable monitoring or power droop (IUSBMONPORTEN):** 1b1 when monitoring or power droop detector is enabled. 1b0 when using external clock. **Power Well:** SUS
24:23	0x0 RW	**EOS REFERENCE ENABLE SELECT (IUSBEOSDETREFEN):** Sel signal to select eosdet vref 2'b00 = 0.75V 2'b01 = 0.725V 2'b10 = 0.775V 2'b11 = 0.8V **Power Well:** SUS
22	0x1 RW	**Power gating DFX force on (PWRGATE_FORCE_ON):** 1: Disallow perport power gating. All LDO remains ON regardless of ihost_phy_pwr_req or suspend. 0:Allow dynamic control based on ihost_phy_pwr_req or suspend. **Power Well:** SUS
21	0x1 RW	**Per Port Power gating suspend policy (PWRGATE_SUSPENDM_POLICY):** 1: Per Port power gating based on utmi suspendm only. Once suspendm=0, phy will initiate perport power gating. 0: Per Port power gating based on utmi suspendm and ihost_ppXpwr_req. **Power Well:** SUS
20:18	0x0 RW	**High pass frequency select (IUSBCMPPWRDROOPDET_FREQSEL):** Power droop detect control signals to select for High Pass frequency. 000b - 1MHz 001b - 30MHz 010b - 60MHz 011b - Invalid 100b - Invalid 101b - Invalid 110b - Invalid 111b - Invalid **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
17	0x1 RW	**Bypass capacitor (IUSBCMPPWRDROOPDET_CAPBYP_H):** Signal to bypass the high pass filters capacitor. **Power Well:** SUS
16	0x0 RW	**Power droop detect reset (IUSBCMPPWRDROOPDET_RST_H):** Power droop detect reset signal for common lane. **Power Well:** SUS
15	0x0 RO	**Power droop detect observation (IUSBCMPPWRDROOPDETOUT_H):** Power droop detect output observation signal for common lane. **Power Well:** SUS
14:13	0x2 RW	**Transmit kicker (IUSBCFGKICKTX_L):** Kicker strength control during HS Tx 00 - Turn Off kicker 01 - Lowest kicker strength 10 - Default kicker strength 11 - Highest kicker strength **Power Well:** SUS
12:11	0x2 RW	**Receive kicker (IUSBCFGKICKRX_L):** Kicker strength control during HS Rx 00 - Turn Off kicker 01 - Lowest kicker strength 10 - Default kicker strength 11 - Highest kicker strength **Power Well:** SUS
10	0x0 RW	**RESERVED (RSVD_1):** Reserved. **Power Well:** SUS
9	0x0 RW	**DISABLING AFE VBUS COMPARATOR (VBUSCOMP_DISABLE):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Test mode 1: Disable AFE vbus comparator 0: Allow dynamic sampling enabling **Power Well:** SUS
8	0x0 RW	**DISABLING AFE IDDIG COMPARATOR (IDDIGCOMP_DISABLE):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Test mode 1: Disable AFE iddig comparator 0: Allow dynamic sampling enabling **Power Well:** SUS
7	0x0 RW	**DISABLNG AFE SENSE COMPARATOR (SENSECOMP_DISABLE):** Feed directly to SHIP or AFE : SHIP Functional or Test Mode : Test mode 1: Disable AFE sense comparator 0: Allow dynamic sampling enabling . **Power Well:** SUS
6	0x0 RW	**DC MONITOR FOR COMPARATOR (DCMONCOMP):** Enable DC monitor for comparator. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
5:4	0x0 RW	**Session valid Sample Policy (SNSPOL):** 00: Bypass 01: Force SNS valid output to 0b to the UTMI+ 10: Force SNS valid output to 1b to the UTMI+ 11: Sample mode (10 ms period) **Power Well:** SUS
3:2	0x0 RW	**VBUS valid Sample Policy (VBSPOL):** 00: Bypass 01: Force VBUS valid output to 0b to the UTMI+ 10: Force VBUS valid output to 1b to the UTMI+ 11: Sample mode (10 ms period) **Power Well:** SUS
1:0	0x0 RW	**IDDIG Sample Policy (IDSPOL):** 00: Bypass 01: Force IDDIG output to 0b to the UTMI+ 10: Force IDDIG output to 1b to the UTMI+ 11: Sample mode (2 ms period) **Power Well:** SUS

7.14.114 GLB CLOCK PORT 0/1 REPEATER (GLB_CLOCK_PORT_0_1_REPEATER)—Offset 402Dh

Access Method

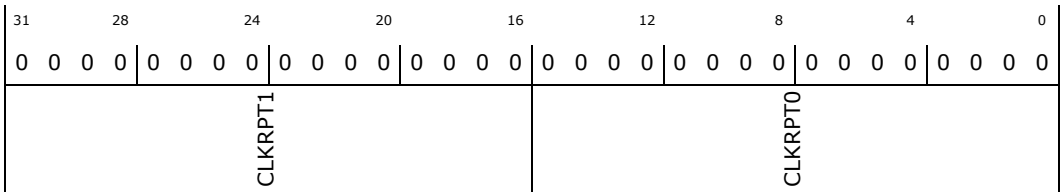
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 402Dh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Ports 15:0 for Clk Repeater 1 (CLKRPT1):** These per-port bits feed into Clock Repeater 1 functionality. **Power Well:** SUS
15:0	0x0 RW	**Ports 15:0 for Clk Repeater 0 (CLKRPT0):** These per-port bits feed into Clock Repeater 0 functionality. **Power Well:** SUS

7.14.115 GLB CLOCK PORT 2/3 REPEATER (GLB_CLOCK_PORT_2_3_REPEATER)—Offset 402Eh

Access Method

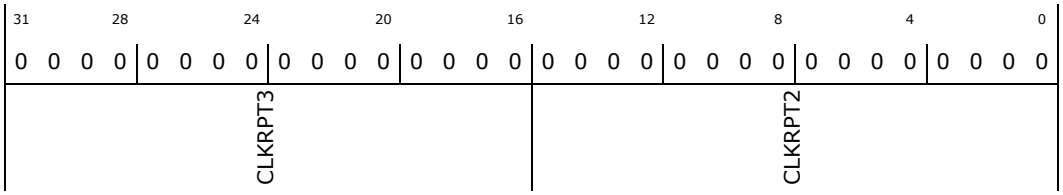
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 402Eh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**PORTS 15:0 FOR CLK REPEATER 3 (CLKRPT3):** These per-port bits feed into Clock Repeater 3 functionality. **Power Well:** SUS
15:0	0x0 RW	**PORTS 15:0 FOR CLK REPEATER 2 (CLKRPT2):** These per-port bits feed into Clock Repeater 2 functionality. **Power Well:** SUS

7.14.116 GLB CLOCK PORT 4/5 REPEATER (GLB_CLOCK_PORT_4_5_REPEATER)—Offset 402Fh

Access Method

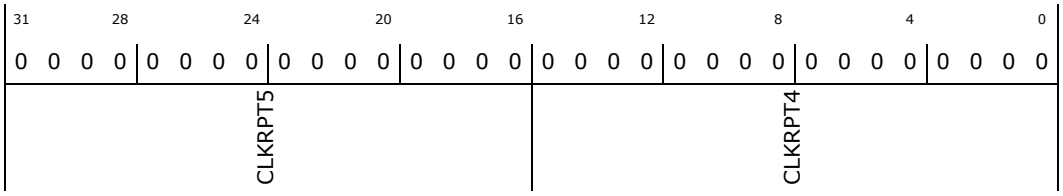
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 402Fh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**PORTS 15:0 FOR CLK REPEATER 5 (CLKRPT5):** These per-port bits feed into Clock Repeater 5 functionality. **Power Well:** SUS
15:0	0x0 RW	**PORTS 15:0 FOR CLK REPEATER 4 (CLKRPT4):** These per-port bits feed into Clock Repeater 4 functionality. **Power Well:** SUS

7.14.117 GLB CLOCK PORT 6/7 REPEATER (GLB_CLOCK_PORT_6_7_REPEATER)—Offset 4030h

Access Method

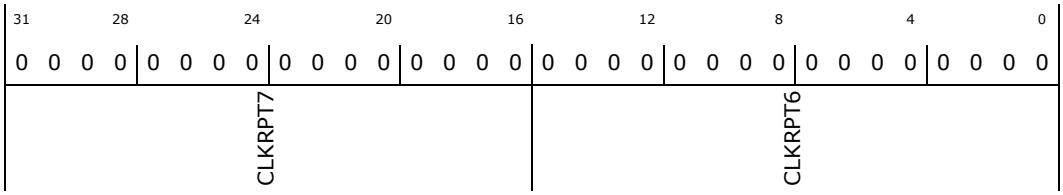
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4030h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**PORTS 15:0 FOR CLK REPEATER 7 (CLKRPT7):** These per-port bits feed into Clock Repeater 7 functionality. **Power Well:** SUS
15:0	0x0 RW	**PORTS 15:0 FOR CLK REPEATER 6 (CLKRPT6):** These per-port bits feed into Clock Repeater 6 functionality. **Power Well:** SUS

7.14.118 GLB CLOCK PORT 8/9 REPEATER (GLB_CLOCK_PORT_8_9_REPEATER)—Offset 4031h

Access Method

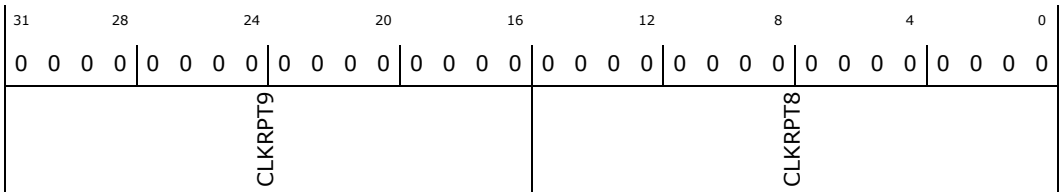
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4031h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**PORTS 15:0 FOR CLK REPEATER 9 (CLKRPT9):** These per-port bits feed into Clock Repeater 9 functionality. **Power Well:** SUS
15:0	0x0 RW	**PORTS 15:0 FOR CLK REPEATER 8 (CLKRPT8):** These per-port bits feed into Clock Repeater 8 functionality. **Power Well:** SUS

7.14.119 GLB CLOCK PORT 10/11 REPEATER (GLB_CLOCK_PORT_10_11_REPEATER)—Offset 4032h

Access Method

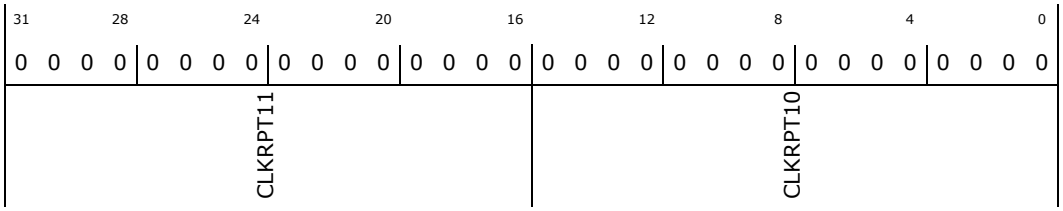
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4032h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**PORTS 15:0 FOR CLK REPEATER 11 (CLKRPT11):** These per-port bits feed into Clock Repeater 11 functionality. **Power Well:** SUS
15:0	0x0 RW	**PORTS 15:0 FOR CLK REPEATER 10 (CLKRPT10):** These per-port bits feed into Clock Repeater 10 functionality. **Power Well:** SUS

7.14.120 GLB CLOCK PORT 12/13 REPEATER (GLB_CLOCK_PORT_12_13_REPEATER)—Offset 4033h

Access Method

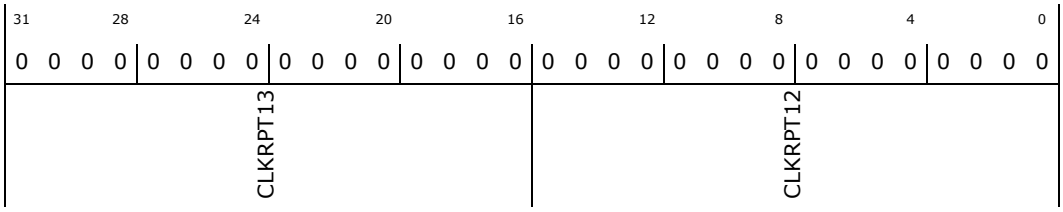
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4033h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**PORTS 15:0 FOR CLK REPEATER 13 (CLKRPT13):** These per-port bits feed into Clock Repeater 13 functionality. **Power Well:** SUS
15:0	0x0 RW	**PORTS 15:0 FOR CLK REPEATER 12 (CLKRPT12):** These per-port bits feed into Clock Repeater 12 functionality. **Power Well:** SUS

7.14.121 GLB CLOCK PORT 14/15 REPEATER (GLB_CLOCK_PORT_14_15_REPEATER)—Offset 4034h

Access Method

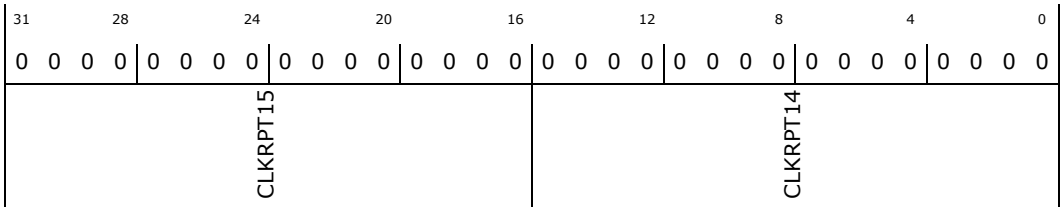
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4034h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**PORTS 15:0 FOR CLK REPEATER 15 (CLKRPT15):** These per-port bits feed into Clock Repeater 15 functionality. **Power Well:** SUS
15:0	0x0 RW	**PORTS 15:0 FOR CLK REPEATER 14 (CLKRPT14):** These per-port bits feed into Clock Repeater 14 functionality. **Power Well:** SUS

7.14.122 GLB LDO MSTR REG 1 (GLB_LDO_MSTR_REG_1)—Offset 4035h

Access Method

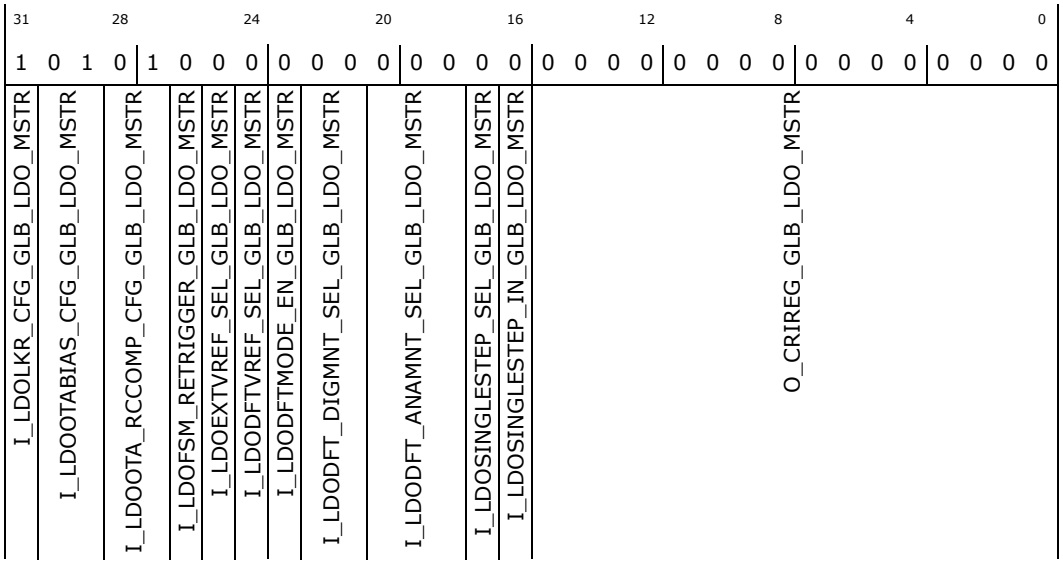
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4035h

Op Codes:

h - Read, h - Write

Default: A8000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**LDO leaker programmability (I_LDOLKR_CFG_GLB_LDO_MSTR):** LDO: leaker programmability signal **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
30:29	0x1 RW	**LDO OTA tail current bias programmability (I_LDOOTABIAS_CFG_GLB_LDO_MSTR):** LDO: OTA tail current bias programmability **Power Well:** SUS
28:27	0x1 RW	**LDO OTA RC compensation programmability (I_LDOOTA_RCCOMP_CFG_GLB_LDO_MSTR):** LDO: OTA RC compensation programmability **Power Well:** SUS
26	0x0 RW	**LDO re-CAL (I_LDOFSM_RETRIGGER_GLB_LDO_MSTR):** LDO: To re-calibrate the LDO FSM while LDO is running **Power Well:** SUS
25	0x0 RW	**LDO external reference voltage (I_LDOEXTVREF_SEL_GLB_LDO_MSTR):** LDO: to select external VREF voltage **Power Well:** SUS
24	0x0 RW	**LDO DFT ref voltage (I_LDODFTVREF_SEL_GLB_LDO_MSTR):** LDO: to select the LDO DFT reference voltage **Power Well:** SUS
23	0x0 RW	**LDO DFT test mode enable (I_LDODFTMODE_EN_GLB_LDO_MSTR):** LDO: LDO DFT test mode enable **Power Well:** SUS
22:21	0x0 RW	**LDO digital monitor (I_LDODFT_DIGMNT_SEL_GLB_LDO_MSTR):** LDO: Digital monitor select bits **Power Well:** SUS
20:18	0x0 RW	**LDO analog monitor (I_LDODFT_ANAMNT_SEL_GLB_LDO_MSTR):** LDO: Analog monitor select bits **Power Well:** SUS
17	0x0 RW	**LDO single step mode (I_LDOSINGLESTEP_SEL_GLB_LDO_MSTR):** LDO: used in DFT mode to select single step mode **Power Well:** SUS
16	0x0 RW	**LDO custom clock (I_LDOSINGLESTEP_IN_GLB_LDO_MSTR):** LDO: used in DFT mode to provide custom clock **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RO	**LDO status (O_CRIREG_GLB_LDO_MSTR):** 16-bit CRI output for LDO status signals. **Power Well:** SUS

7.14.123 GLB LDO MSTR REG 2 (GLB_LDO_MSTR_REG_2)—Offset 4036h

Access Method

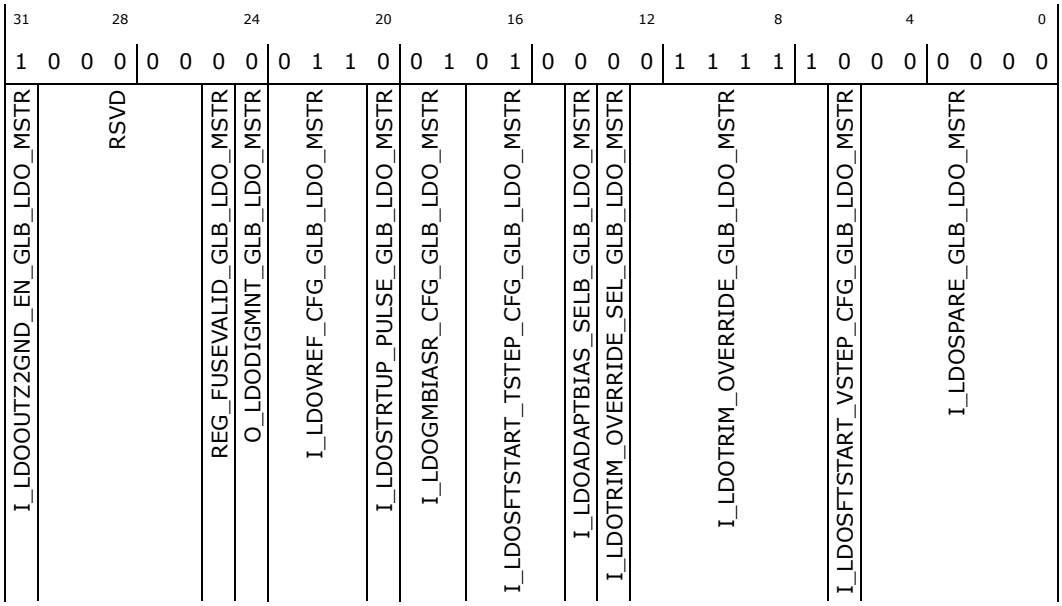
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4036h

Op Codes:

h - Read, h - Write

Default: 80650F80h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**LDO VCC output gnd or Z (I_LDOOUTZ2GND_EN_GLB_LDO_MSTR):** When (i_ldooutz2gnd_en AND i_pwrreq_xldo1p0)=1, the corresponding LDO output (vcc_primldo1p0_lv) vcc_xldo1p0_lv=0, otherwise, high-z. **Power Well:** SUS
30:26	0x0 RW	**RSVD:** Reserved for future use. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
25	0x0 RW	**FUSE Valid (REG_FUSEVALID_GLB_LDO_MSTR):** 1: To indicate fuse values in configuration registers are now valid. Power gating FSM will initiate LDO calibration. This bit is only valid/used when iosf fuse pulling is not used (soc_phy_iosf_fusepull_strap=0). **Power Well:** SUS
24	0x0 RO	**LDO digital monitor (O_LDODIGMNT_GLB_LDO_MSTR):** Feed directly to SHIP or AFE: AFE Functional or Test Mode: Functional digital monitor port. **Power Well:** SUS
23:21	0x3 RW	**LDO reference voltage (I_LDOVREF_CFG_GLB_LDO_MSTR):** LDO reference voltage programmability bits, from common fuse. **Power Well:** SUS
20	0x0 RW	**LDO backup gm bias (I_LDOSTRTUP_PULSE_GLB_LDO_MSTR):** Backup option for gm-bias startup, from common fuse **Power Well:** SUS
19:18	0x1 RW	**LDO iref resistor program (I_LDOGMBIASR_CFG_GLB_LDO_MSTR):** LDO Iref block - resistor programmability, from common fuse. **Power Well:** SUS
17:15	0x2 RW	**LDO soft start tstep (I_LDOSFTSTART_TSTEP_CFG_GLB_LDO_MSTR):** LDO soft start timer configuration used to select different clock period for soft-start, from common fuse. **Power Well:** SUS
14	0x0 RW	**LDO adaptive biasing (I_LDOADAPTBIAS_SELB_GLB_LDO_MSTR):** To enable/disable adaptive biasing scheme, by default adaptive biasing scheme is ON (active low). Common fuse. **Power Well:** SUS
13	0x0 RW	**LDO trim override select (I_LDOTRIM_OVERRIDE_SEL_GLB_LDO_MSTR):** Signal from unique fuse to select the LDO trim override option **Power Well:** SUS
12:7	0x1f RW	**LDO trim override (I_LDOTRIM_OVERRIDE_GLB_LDO_MSTR):** Inputs from unique fuse to override the FSM calibration values, In master-slave config, master and slaves LDOs need unique signals. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
6	0x0 RW	**LDO soft start vstep (I_LDOSFTSTART_VSTEP_CFG_GLB_LDO_MSTR):** LDO soft start timer configuration used to select different voltage step in soft-start, from unique fuse. **Power Well:** SUS
5:0	0x0 RW	**LDO spare (I_LDOSPARE_GLB_LDO_MSTR):** spare digital inputs, 16 CRI used, 7 unique fuse used, 1 left, 7 common fuse used, 9 left (common fuse (10:2), unique fuse (1),) **Power Well:** SUS

7.14.124 GLB LDO SLV REG 1 (GLB_LDO_SLV_REG_1)—Offset 4037h

Access Method

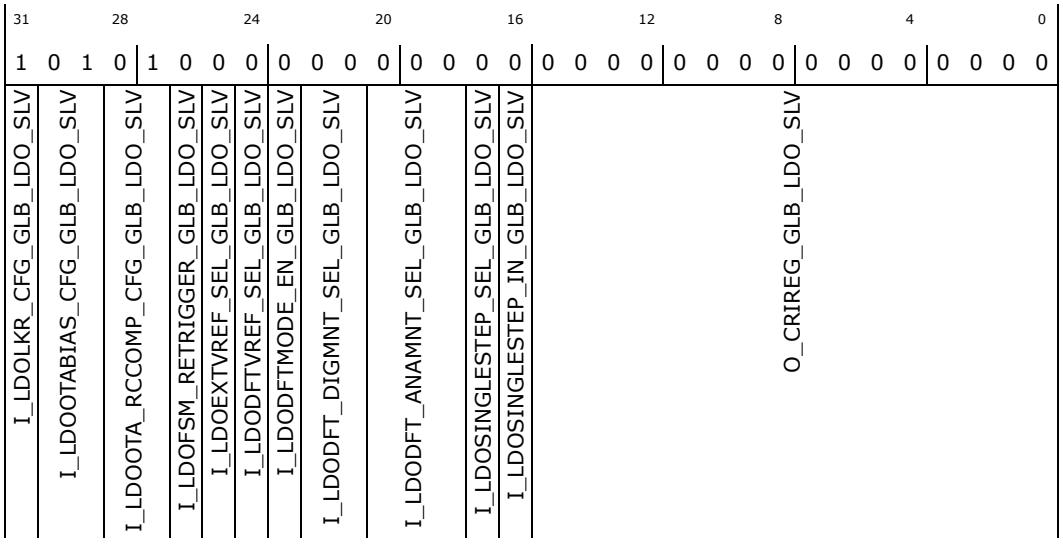
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4037h

Op Codes:

h - Read, h - Write

Default: A8000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**LDO leaker programmability (I_LDOLKR_CFG_GLB_LDO_SLV):** LDO: leaker programmability signal **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
30:29	0x1 RW	**LDO OTA tail current bias programmability (I_LDOOTABIAS_CFG_GLB_LDO_SLV):** LDO: OTA tail current bias programmability **Power Well:** SUS
28:27	0x1 RW	**LDO OTA RC compensation programmability (I_LDOOTA_RCCOMP_CFG_GLB_LDO_SLV):** LDO: OTA RC compensation programmability **Power Well:** SUS
26	0x0 RW	**LDO re-CAL (I_LDOFSM_RETRIGGER_GLB_LDO_SLV):** LDO: To re-calibrate the LDO FSM while LDO is running **Power Well:** SUS
25	0x0 RW	**LDO external reference voltage (I_LDOEXTVREF_SEL_GLB_LDO_SLV):** LDO: to select external VREF voltage **Power Well:** SUS
24	0x0 RW	**LDO DFT ref voltage (I_LDODFTVREF_SEL_GLB_LDO_SLV):** LDO: to select the LDO DFT reference voltage **Power Well:** SUS
23	0x0 RW	**LDO DFT test mode enable (I_LDODFTMODE_EN_GLB_LDO_SLV):** LDO: LDO DFT test mode enable **Power Well:** SUS
22:21	0x0 RW	**LDO digital monitor (I_LDODFT_DIGMNT_SEL_GLB_LDO_SLV):** LDO: Digital monitor select bits **Power Well:** SUS
20:18	0x0 RW	**LDO analog monitor (I_LDODFT_ANAMNT_SEL_GLB_LDO_SLV):** LDO: Analog monitor select bits **Power Well:** SUS
17	0x0 RW	**LDO single step mode (I_LDOSINGLESTEP_SEL_GLB_LDO_SLV):** LDO: used in DFT mode to select single step mode **Power Well:** SUS
16	0x0 RW	**LDO custom clock (I_LDOSINGLESTEP_IN_GLB_LDO_SLV):** LDO: used in DFT mode to provide custom clock **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RO	**LDO status (O_CRIREG_GLB_LDO_SLV):** 16-bit CRI output for LDO status signals. **Power Well:** SUS

7.14.125 GLB LDO SLV REG 2 (GLB_LDO_SLV_REG_2)—Offset 4038h

Access Method

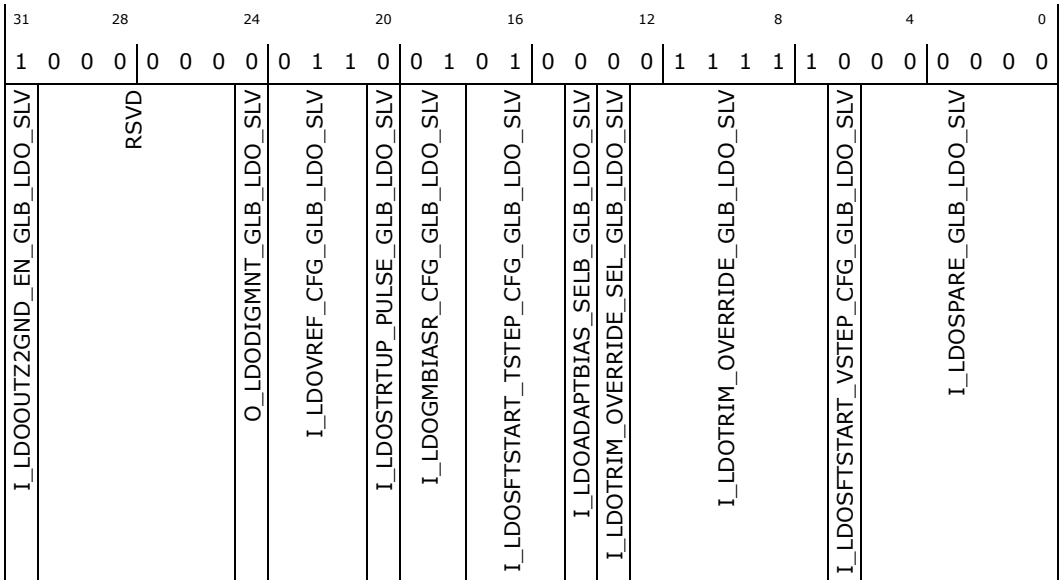
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4038h

Op Codes:

h - Read, h - Write

Default: 80650F80h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**LDO VCC output gnd or Z (I_LDOOUTZ2GND_EN_GLB_LDO_SLV):** When (i_ldooutz2gnd_en AND i_pwrreq_xldo1p0)=1, the corresponding LDO output (vcc_primldo1p0_lv) vcc_xldo1p0_lv=0, otherwise, high-z. **Power Well:** SUS
30:25	0x0 RW	**RSVD:** Reserved for future use. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
24	0x0 RO	**LDO digital monitor (O_LDODIGMNT_GLB_LDO_SLV):** Feed directly to SHIP or AFE: AFE Functional or Test Mode: Functional digital monitor port. **Power Well:** SUS
23:21	0x3 RW	**LDO reference voltage (I_LDOVREF_CFG_GLB_LDO_SLV):** LDO reference voltage programmability bits, from common fuse. **Power Well:** SUS
20	0x0 RW	**LDO backup gm bias (I_LDOSTRTUP_PULSE_GLB_LDO_SLV):** Backup option for gm-bias startup, from common fuse **Power Well:** SUS
19:18	0x1 RW	**LDO iref resistor program (I_LDOGMBIASR_CFG_GLB_LDO_SLV):** LDO Iref block - resistor programmability, from common fuse. **Power Well:** SUS
17:15	0x2 RW	**LDO soft start tstep (I_LDOSFTSTART_TSTEP_CFG_GLB_LDO_SLV):** LDO soft start timer configuration used to select different clock period for soft-start, from common fuse. **Power Well:** SUS
14	0x0 RW	**LDO adaptive biasing (I_LDOADAPTBIAS_SELB_GLB_LDO_SLV):** To enable/disable adaptive biasing scheme, by default adaptive biasing scheme is ON (active low). Common fuse. **Power Well:** SUS
13	0x0 RW	**LDO trim override select (I_LDOTRIM_OVERRIDE_SEL_GLB_LDO_SLV):** Signal from unique fuse to select the LDO trim override option **Power Well:** SUS
12:7	0x1f RW	**LDO trim override (I_LDOTRIM_OVERRIDE_GLB_LDO_SLV):** Inputs from unique fuse to override the FSM calibration values, In master-slave config, master and slaves LDOs need unique signals. **Power Well:** SUS
6	0x0 RW	**LDO soft start vstep (I_LDOSFTSTART_VSTEP_CFG_GLB_LDO_SLV):** LDO soft start timer configuration used to select different voltage step in soft-start, from unique fuse. **Power Well:** SUS
5:0	0x0 RW	**LDO spare (I_LDOSPARE_GLB_LDO_SLV):** spare digital inputs, 16 CRI used, 7 unique fuse used, 1 left, 7 common fuse used, 9 left (common fuse (10:2), unique fuse (1),) **Power Well:** SUS

7.14.126 PP LDO SLV REG 1 (PP_LDO_SLV_REG_1_PP0)—Offset 4139h

Access Method

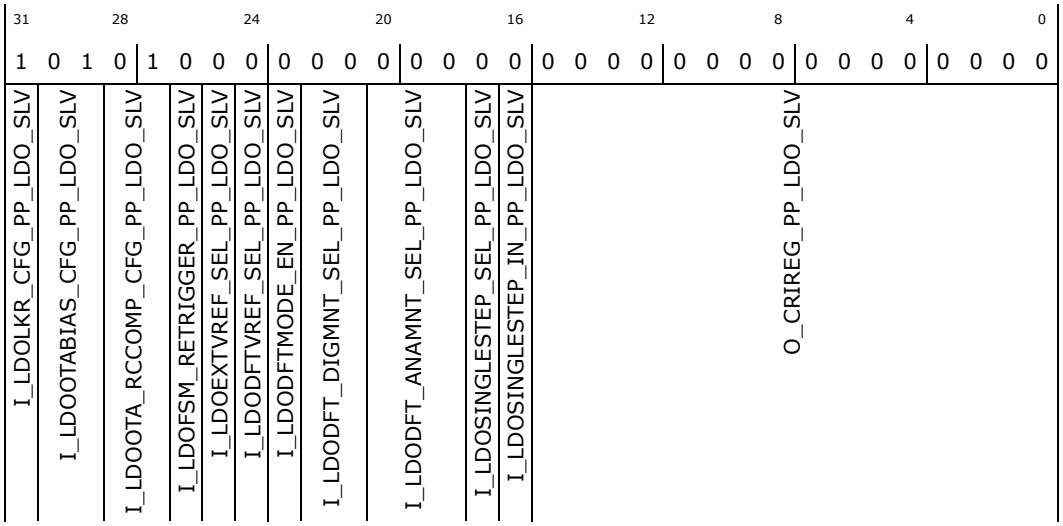
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4139h

Op Codes:

h - Read, h - Write

Default: A8000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**LDO leaker programmability (I_LDOLKR_CFG_PP_LDO_SLV):** LDO: leaker programmability signal **Power Well:** SUS
30:29	0x1 RW	**LDO OTA tail current bias programmability (I_LDOOTABIAS_CFG_PP_LDO_SLV):** LDO: OTA tail current bias programmability **Power Well:** SUS
28:27	0x1 RW	**LDO OTA RC compensation programmability (I_LDOOTA_RCCOMP_CFG_PP_LDO_SLV):** LDO: OTA RC compensation programmability **Power Well:** SUS
26	0x0 RW	**LDO re-CAL (I_LDOFSM_RETRIGGER_PP_LDO_SLV):** LDO: To re-calibrate the LDO FSM while LDO is running **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
25	0x0 RW	**LDO external reference voltage (I_LDOEXTVREF_SEL_PP_LDO_SLV):** LDO: to select external VREF voltage **Power Well:** SUS
24	0x0 RW	**LDO DFT ref voltage (I_LDODFTVREF_SEL_PP_LDO_SLV):** LDO: to select the LDO DFT reference voltage **Power Well:** SUS
23	0x0 RW	**LDO DFT test mode enable (I_LDODFTMODE_EN_PP_LDO_SLV):** LDO: LDO DFT test mode enable **Power Well:** SUS
22:21	0x0 RW	**LDO digital monitor (I_LDODFT_DIGMNT_SEL_PP_LDO_SLV):** LDO: Digital monitor select bits **Power Well:** SUS
20:18	0x0 RW	**LDO analog monitor (I_LDODFT_ANAMNT_SEL_PP_LDO_SLV):** LDO: Analog monitor select bits **Power Well:** SUS
17	0x0 RW	**LDO single step mode (I_LDOSINGLESTEP_SEL_PP_LDO_SLV):** LDO: used in DFT mode to select single step mode **Power Well:** SUS
16	0x0 RW	**LDO custom clock (I_LDOSINGLESTEP_IN_PP_LDO_SLV):** LDO: used in DFT mode to provide custom clock **Power Well:** SUS
15:0	0x0 RO	**LDO status (O_CRIREG_PP_LDO_SLV):** 16-bit CRI output for LDO status signals. **Power Well:** SUS

7.14.127 PP LDO SLV REG 2 (PP_LDO_SLV_REG_2_PP0)—Offset 413Ah

Access Method

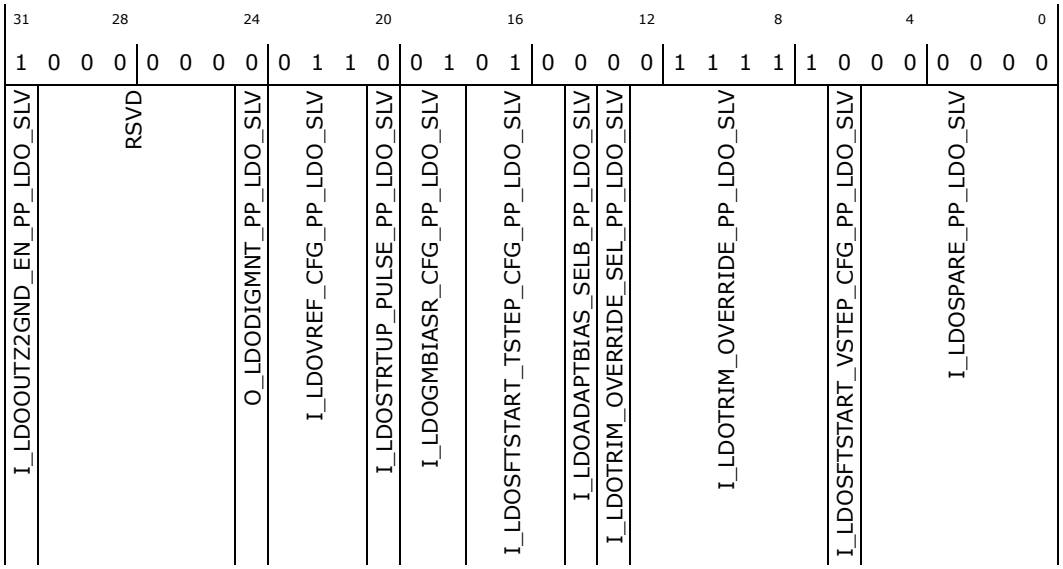
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 413Ah

Op Codes:

h - Read, h - Write

Default: 80650F80h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**LDO VCC output gnd or Z (I_LDOOUTZ2GND_EN_PP_LDO_SLV):** When (i_ldooutz2gnd_en AND i_pwrreq_xldo1p0)=1, the corresponding LDO output (vcc_primldo1p0_lv) vcc_xldo1p0_lv=0, otherwise, high-z. **Power Well:** SUS
30:25	0x0 RW	**RSVD:** Reserved for future use. **Power Well:** SUS
24	0x0 RO	**LDO digital monitor (O_LDODIGMNT_PP_LDO_SLV):** Feed directly to SHIP or AFE: AFE Functional or Test Mode: Functional digital monitor port. **Power Well:** SUS
23:21	0x3 RW	**LDO reference voltage (I_LDOVREF_CFG_PP_LDO_SLV):** LDO reference voltage programmability bits, from common fuse. **Power Well:** SUS
20	0x0 RW	**LDO backup gm bias (I_LDOSTRTUP_PULSE_PP_LDO_SLV):** Backup option for gm-bias startup, from common fuse **Power Well:** SUS
19:18	0x1 RW	**LDO iref resistor program (I_LDOGMBIASR_CFG_PP_LDO_SLV):** LDO Iref block - resistor programmability, from common fuse. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
17:15	0x2 RW	**LDO soft start tstep (I_LDOSFTSTART_TSTEP_CFG_PP_LDO_SLV):** LDO soft start timer configuration used to select different clock period for soft-start, from common fuse. **Power Well:** SUS
14	0x0 RW	**LDO adaptive biasing (I_LDOADAPTBIAS_SELB_PP_LDO_SLV):** To enable/disable adaptive biasing scheme, by default adaptive biasing scheme is ON (active low). Common fuse. **Power Well:** SUS
13	0x0 RW	**LDO trim override select (I_LDOTRIM_OVERRIDE_SEL_PP_LDO_SLV):** Signal from unique fuse to select the LDO trim override option **Power Well:** SUS
12:7	0x1f RW	**LDO trim override (I_LDOTRIM_OVERRIDE_PP_LDO_SLV):** Inputs from unique fuse to override the FSM calibration values, In master-slave config, master and slaves LDOs need unique signals. **Power Well:** SUS
6	0x0 RW	**LDO soft start vstep (I_LDOSFTSTART_VSTEP_CFG_PP_LDO_SLV):** LDO soft start timer configuration used to select different voltage step in soft-start, from unique fuse. **Power Well:** SUS
5:0	0x0 RW	**LDO spare (I_LDOSPARE_PP_LDO_SLV):** spare digital inputs, 16 CRI used, 7 unique fuse used, 1 left, 7 common fuse used, 9 left (common fuse (10:2), unique fuse (1),) **Power Well:** SUS

7.14.128 PP LDO SLV REG 1 (PP_LDO_SLV_REG_1_PP1)—Offset 4239h

Access Method

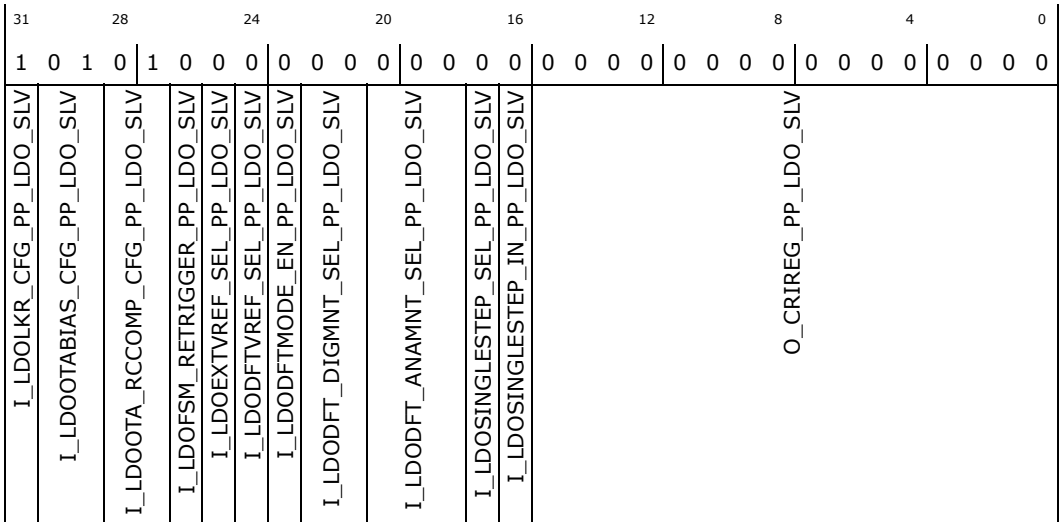
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4239h

Op Codes:

h - Read, h - Write

Default: A8000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**LDO leaker programmability (I_LDOLKR_CFG_PP_LDO_SLV):** LDO: leaker programmability signal **Power Well:** SUS
30:29	0x1 RW	**LDO OTA tail current bias programmability (I_LDOOTABIAS_CFG_PP_LDO_SLV):** LDO: OTA tail current bias programmability **Power Well:** SUS
28:27	0x1 RW	**LDO OTA RC compensation programmability (I_LDOOTA_RCCOMP_CFG_PP_LDO_SLV):** LDO: OTA RC compensation programmability **Power Well:** SUS
26	0x0 RW	**LDO re-CAL (I_LDOFSM_RETRIGGER_PP_LDO_SLV):** LDO: To re-calibrate the LDO FSM while LDO is running **Power Well:** SUS
25	0x0 RW	**LDO external reference voltage (I_LDOEXTVREF_SEL_PP_LDO_SLV):** LDO: to select external VREF voltage **Power Well:** SUS
24	0x0 RW	**LDO DFT ref voltage (I_LDODFTVREF_SEL_PP_LDO_SLV):** LDO: to select the LDO DFT reference voltage **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
23	0x0 RW	**LDO DFT test mode enable (I_LDODFTMODE_EN_PP_LDO_SLV):** LDO: LDO DFT test mode enable **Power Well:** SUS
22:21	0x0 RW	**LDO digital monitor (I_LDODFT_DIGMNT_SEL_PP_LDO_SLV):** LDO: Digital monitor select bits **Power Well:** SUS
20:18	0x0 RW	**LDO analog monitor (I_LDODFT_ANAMNT_SEL_PP_LDO_SLV):** LDO: Analog monitor select bits **Power Well:** SUS
17	0x0 RW	**LDO single step mode (I_LDOSINGLESTEP_SEL_PP_LDO_SLV):** LDO: used in DFT mode to select single step mode **Power Well:** SUS
16	0x0 RW	**LDO custom clock (I_LDOSINGLESTEP_IN_PP_LDO_SLV):** LDO: used in DFT mode to provide custom clock **Power Well:** SUS
15:0	0x0 RO	**LDO status (O_CRIREG_PP_LDO_SLV):** 16-bit CRI output for LDO status signals. **Power Well:** SUS

7.14.129 PP LDO SLV REG 2 (PP_LDO_SLV_REG_2_PP1)—Offset 423Ah

Access Method

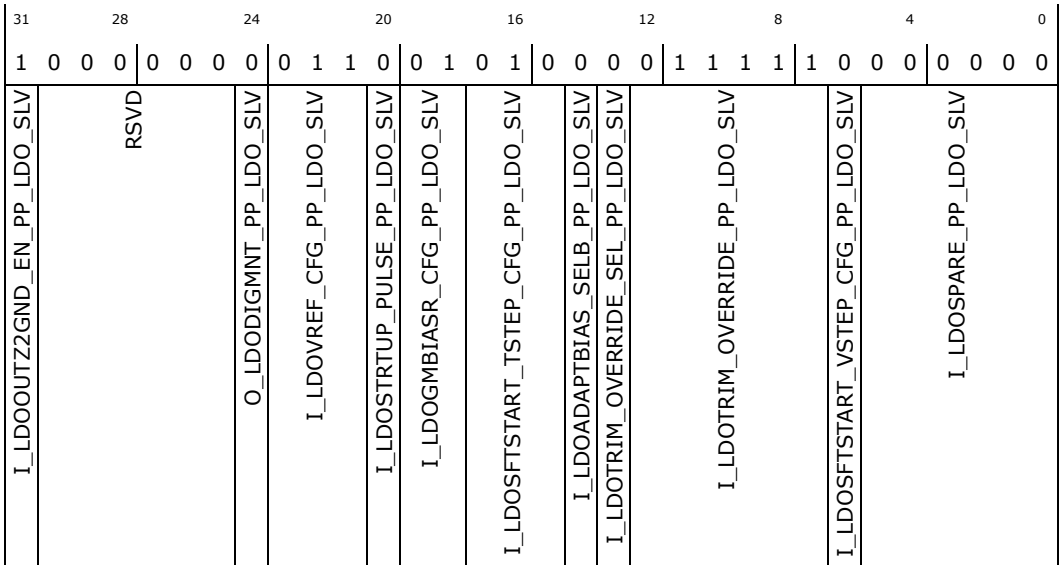
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 423Ah

Op Codes:

h - Read, h - Write

Default: 80650F80h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**LDO VCC output gnd or Z (I_LDOOUTZ2GND_EN_PP_LDO_SLV):** When (i_ldooutz2gnd_en AND i_pwrreq_xldo1p0)=1, the corresponding LDO output (vcc_primldo1p0_lv) vcc_xldo1p0_lv=0, otherwise, high-z. **Power Well:** SUS
30:25	0x0 RW	**RSVD:** Reserved for future use. **Power Well:** SUS
24	0x0 RO	**LDO digital monitor (O_LDODIGMNT_PP_LDO_SLV):** Feed directly to SHIP or AFE: AFE Functional or Test Mode: Functional digital monitor port. **Power Well:** SUS
23:21	0x3 RW	**LDO reference voltage (I_LDOVREF_CFG_PP_LDO_SLV):** LDO reference voltage programmability bits, from common fuse. **Power Well:** SUS
20	0x0 RW	**LDO backup gm bias (I_LDOSTRTUP_PULSE_PP_LDO_SLV):** Backup option for gm-bias startup, from common fuse **Power Well:** SUS
19:18	0x1 RW	**LDO iref resistor program (I_LDOGMBIASR_CFG_PP_LDO_SLV):** LDO Iref block - resistor programmability, from common fuse. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
17:15	0x2 RW	**LDO soft start tstep (I_LDOSFTSTART_TSTEP_CFG_PP_LDO_SLV):** LDO soft start timer configuration used to select different clock period for soft-start, from common fuse. **Power Well:** SUS
14	0x0 RW	**LDO adaptive biasing (I_LDOADAPTBIAS_SELB_PP_LDO_SLV):** To enable/disable adaptive biasing scheme, by default adaptive biasing scheme is ON (active low). Common fuse. **Power Well:** SUS
13	0x0 RW	**LDO trim override select (I_LDOTRIM_OVERRIDE_SEL_PP_LDO_SLV):** Signal from unique fuse to select the LDO trim override option **Power Well:** SUS
12:7	0x1f RW	**LDO trim override (I_LDOTRIM_OVERRIDE_PP_LDO_SLV):** Inputs from unique fuse to override the FSM calibration values, In master-slave config, master and slaves LDOs need unique signals. **Power Well:** SUS
6	0x0 RW	**LDO soft start vstep (I_LDOSFTSTART_VSTEP_CFG_PP_LDO_SLV):** LDO soft start timer configuration used to select different voltage step in soft-start, from unique fuse. **Power Well:** SUS
5:0	0x0 RW	**LDO spare (I_LDOSPARE_PP_LDO_SLV):** spare digital inputs, 16 CRI used, 7 unique fuse used, 1 left, 7 common fuse used, 9 left (common fuse (10:2), unique fuse (1),) **Power Well:** SUS

7.14.130 PP LDO SLV REG 1 (PP_LDO_SLV_REG_1_PP2)—Offset 4339h

Access Method

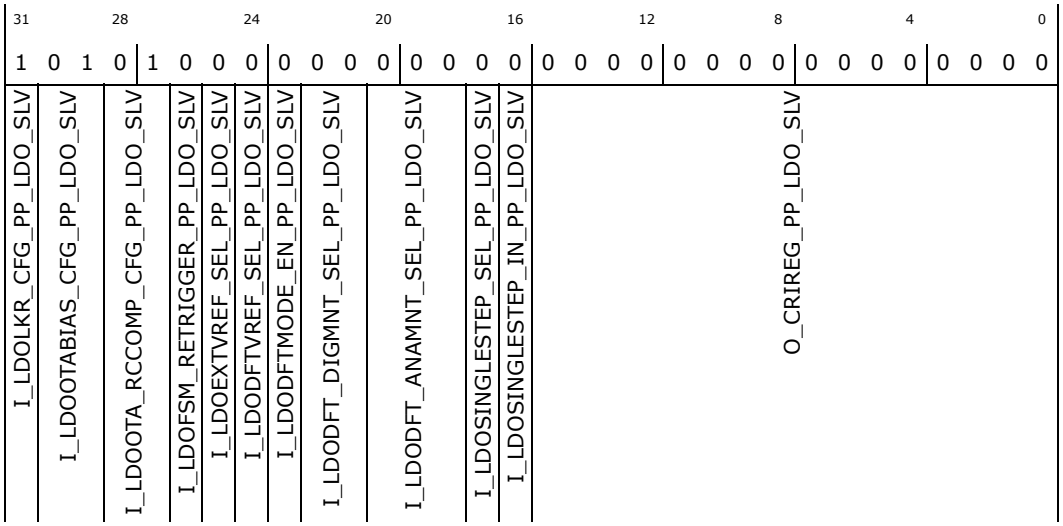
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4339h

Op Codes:

h - Read, h - Write

Default: A8000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**LDO leaker programmability (I_LDOLKR_CFG_PP_LDO_SLV):** LDO: leaker programmability signal **Power Well:** SUS
30:29	0x1 RW	**LDO OTA tail current bias programmability (I_LDOOTABIAS_CFG_PP_LDO_SLV):** LDO: OTA tail current bias programmability **Power Well:** SUS
28:27	0x1 RW	**LDO OTA RC compensation programmability (I_LDOOTA_RCCOMP_CFG_PP_LDO_SLV):** LDO: OTA RC compensation programmability **Power Well:** SUS
26	0x0 RW	**LDO re-CAL (I_LDOFSM_RETRIGGER_PP_LDO_SLV):** LDO: To re-calibrate the LDO FSM while LDO is running **Power Well:** SUS
25	0x0 RW	**LDO external reference voltage (I_LDOEXTVREF_SEL_PP_LDO_SLV):** LDO: to select external VREF voltage **Power Well:** SUS
24	0x0 RW	**LDO DFT ref voltage (I_LDODFTVREF_SEL_PP_LDO_SLV):** LDO: to select the LDO DFT reference voltage **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
23	0x0 RW	**LDO DFT test mode enable (I_LDODFTMODE_EN_PP_LDO_SLV):** LDO: LDO DFT test mode enable **Power Well:** SUS
22:21	0x0 RW	**LDO digital monitor (I_LDODFT_DIGMNT_SEL_PP_LDO_SLV):** LDO: Digital monitor select bits **Power Well:** SUS
20:18	0x0 RW	**LDO analog monitor (I_LDODFT_ANAMNT_SEL_PP_LDO_SLV):** LDO: Analog monitor select bits **Power Well:** SUS
17	0x0 RW	**LDO single step mode (I_LDOSINGLESTEP_SEL_PP_LDO_SLV):** LDO: used in DFT mode to select single step mode **Power Well:** SUS
16	0x0 RW	**LDO custom clock (I_LDOSINGLESTEP_IN_PP_LDO_SLV):** LDO: used in DFT mode to provide custom clock **Power Well:** SUS
15:0	0x0 RO	**LDO status (O_CRIREG_PP_LDO_SLV):** 16-bit CRI output for LDO status signals. **Power Well:** SUS

7.14.131 PP LDO SLV REG 2 (PP_LDO_SLV_REG_2_PP2)—Offset 433Ah

Access Method

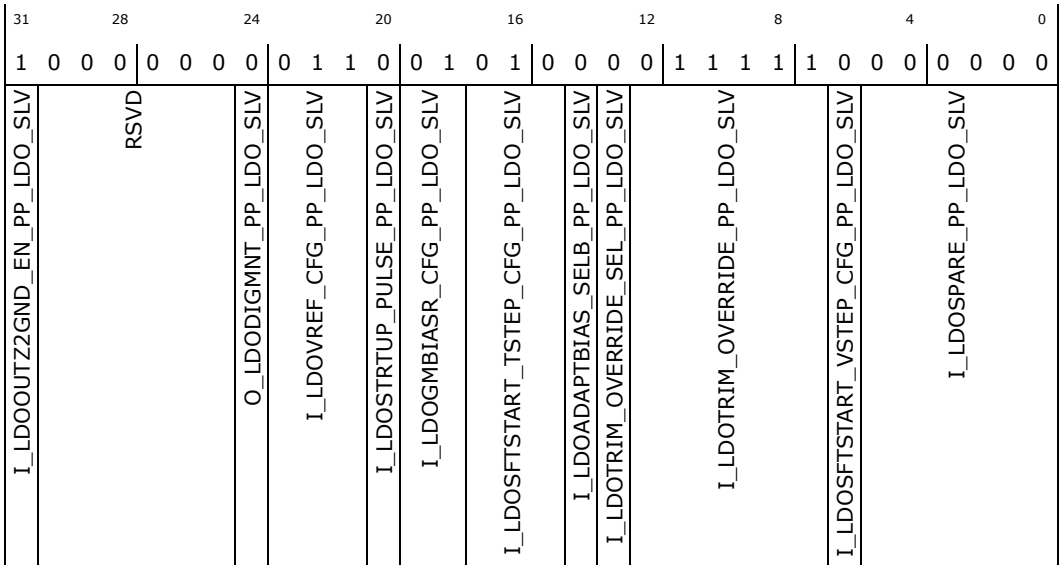
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 433Ah

Op Codes:

h - Read, h - Write

Default: 80650F80h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**LDO VCC output gnd or Z (I_LDOOUTZ2GND_EN_PP_LDO_SLV):** When (i_ldooutz2gnd_en AND i_pwrreq_xldo1p0)=1, the corresponding LDO output (vcc_primldo1p0_lv) vcc_xldo1p0_lv=0, otherwise, high-z. **Power Well:** SUS
30:25	0x0 RW	**RSVD:** Reserved for future use. **Power Well:** SUS
24	0x0 RO	**LDO digital monitor (O_LDODIGMNT_PP_LDO_SLV):** Feed directly to SHIP or AFE: AFE Functional or Test Mode: Functional digital monitor port. **Power Well:** SUS
23:21	0x3 RW	**LDO reference voltage (I_LDOVREF_CFG_PP_LDO_SLV):** LDO reference voltage programmability bits, from common fuse. **Power Well:** SUS
20	0x0 RW	**LDO backup gm bias (I_LDOSTRTUP_PULSE_PP_LDO_SLV):** Backup option for gm-bias startup, from common fuse **Power Well:** SUS
19:18	0x1 RW	**LDO iref resistor program (I_LDOGMBIASR_CFG_PP_LDO_SLV):** LDO Iref block - resistor programmability, from common fuse. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
17:15	0x2 RW	**LDO soft start tstep (I_LDOSFTSTART_TSTEP_CFG_PP_LDO_SLV):** LDO soft start timer configuration used to select different clock period for soft-start, from common fuse. **Power Well:** SUS
14	0x0 RW	**LDO adaptive biasing (I_LDOADAPTBIAS_SELB_PP_LDO_SLV):** To enable/disable adaptive biasing scheme, by default adaptive biasing scheme is ON (active low). Common fuse. **Power Well:** SUS
13	0x0 RW	**LDO trim override select (I_LDOTRIM_OVERRIDE_SEL_PP_LDO_SLV):** Signal from unique fuse to select the LDO trim override option **Power Well:** SUS
12:7	0x1f RW	**LDO trim override (I_LDOTRIM_OVERRIDE_PP_LDO_SLV):** Inputs from unique fuse to override the FSM calibration values, In master-slave config, master and slaves LDOs need unique signals. **Power Well:** SUS
6	0x0 RW	**LDO soft start vstep (I_LDOSFTSTART_VSTEP_CFG_PP_LDO_SLV):** LDO soft start timer configuration used to select different voltage step in soft-start, from unique fuse. **Power Well:** SUS
5:0	0x0 RW	**LDO spare (I_LDOSPARE_PP_LDO_SLV):** spare digital inputs, 16 CRI used, 7 unique fuse used, 1 left, 7 common fuse used, 9 left (common fuse (10:2), unique fuse (1),) **Power Well:** SUS

7.14.132 PP LDO SLV REG 1 (PP_LDO_SLV_REG_1_PP3)—Offset 4439h

Access Method

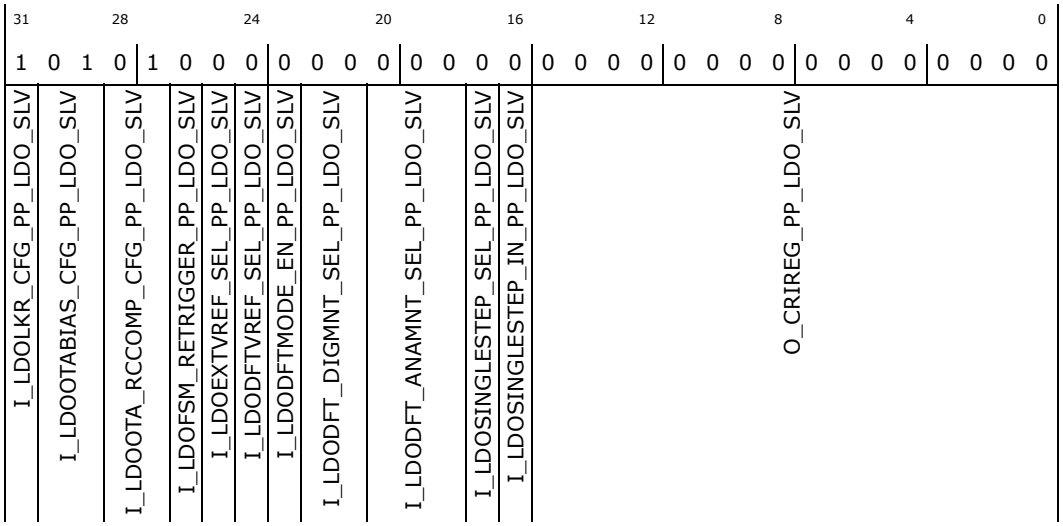
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4439h

Op Codes:

h - Read, h - Write

Default: A8000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**LDO leaker programmability (I_LDOLKR_CFG_PP_LDO_SLV):** LDO: leaker programmability signal **Power Well:** SUS
30:29	0x1 RW	**LDO OTA tail current bias programmability (I_LDOOTABIAS_CFG_PP_LDO_SLV):** LDO: OTA tail current bias programmability **Power Well:** SUS
28:27	0x1 RW	**LDO OTA RC compensation programmability (I_LDOOTA_RCCOMP_CFG_PP_LDO_SLV):** LDO: OTA RC compensation programmability **Power Well:** SUS
26	0x0 RW	**LDO re-CAL (I_LDOFSM_RETRIGGER_PP_LDO_SLV):** LDO: To re-calibrate the LDO FSM while LDO is running **Power Well:** SUS
25	0x0 RW	**LDO external reference voltage (I_LDOEXTVREF_SEL_PP_LDO_SLV):** LDO: to select external VREF voltage **Power Well:** SUS
24	0x0 RW	**LDO DFT ref voltage (I_LDODFTVREF_SEL_PP_LDO_SLV):** LDO: to select the LDO DFT reference voltage **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
23	0x0 RW	**LDO DFT test mode enable (I_LDODFTMODE_EN_PP_LDO_SLV):** LDO: LDO DFT test mode enable **Power Well:** SUS
22:21	0x0 RW	**LDO digital monitor (I_LDODFT_DIGMNT_SEL_PP_LDO_SLV):** LDO: Digital monitor select bits **Power Well:** SUS
20:18	0x0 RW	**LDO analog monitor (I_LDODFT_ANAMNT_SEL_PP_LDO_SLV):** LDO: Analog monitor select bits **Power Well:** SUS
17	0x0 RW	**LDO single step mode (I_LDOSINGLESTEP_SEL_PP_LDO_SLV):** LDO: used in DFT mode to select single step mode **Power Well:** SUS
16	0x0 RW	**LDO custom clock (I_LDOSINGLESTEP_IN_PP_LDO_SLV):** LDO: used in DFT mode to provide custom clock **Power Well:** SUS
15:0	0x0 RO	**LDO status (O_CRIREG_PP_LDO_SLV):** 16-bit CRI output for LDO status signals. **Power Well:** SUS

7.14.133 PP LDO SLV REG 2 (PP_LDO_SLV_REG_2_PP3)—Offset 443Ah

Access Method

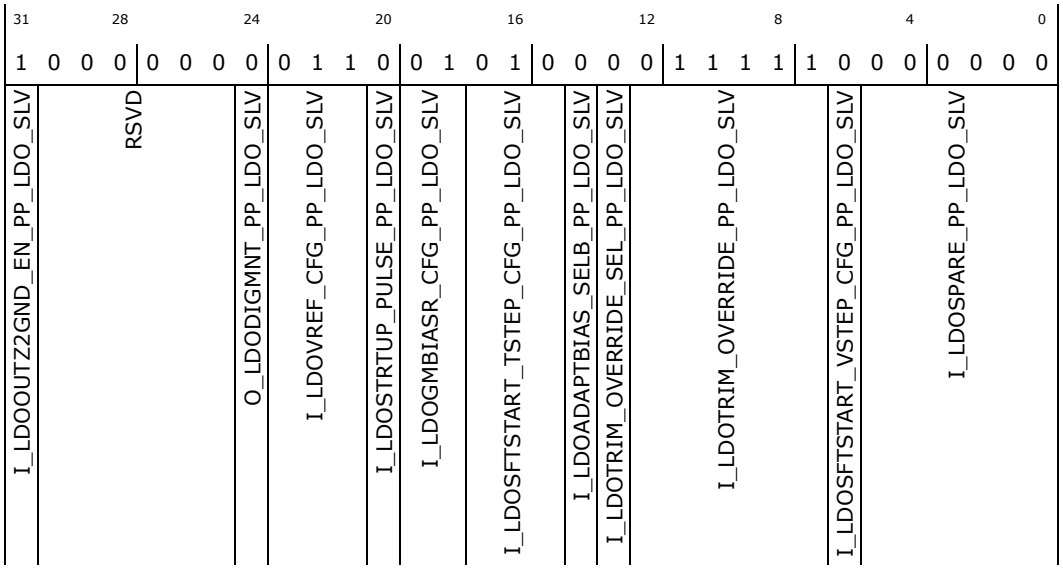
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 443Ah

Op Codes:

h - Read, h - Write

Default: 80650F80h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**LDO VCC output gnd or Z (I_LDOOUTZ2GND_EN_PP_LDO_SLV):** When (i_ldooutz2gnd_en AND i_pwrreq_xldo1p0)=1, the corresponding LDO output (vcc_primldo1p0_lv) vcc_xldo1p0_lv=0, otherwise, high-z. **Power Well:** SUS
30:25	0x0 RW	**RSVD:** Reserved for future use. **Power Well:** SUS
24	0x0 RO	**LDO digital monitor (O_LDODIGMNT_PP_LDO_SLV):** Feed directly to SHIP or AFE: AFE Functional or Test Mode: Functional digital monitor port. **Power Well:** SUS
23:21	0x3 RW	**LDO reference voltage (I_LDOVREF_CFG_PP_LDO_SLV):** LDO reference voltage programmability bits, from common fuse. **Power Well:** SUS
20	0x0 RW	**LDO backup gm bias (I_LDOSTRTUP_PULSE_PP_LDO_SLV):** Backup option for gm-bias startup, from common fuse **Power Well:** SUS
19:18	0x1 RW	**LDO iref resistor program (I_LDOGMBIASR_CFG_PP_LDO_SLV):** LDO Iref block - resistor programmability, from common fuse. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
17:15	0x2 RW	**LDO soft start tstep (I_LDOSFTSTART_TSTEP_CFG_PP_LDO_SLV):** LDO soft start timer configuration used to select different clock period for soft-start, from common fuse. **Power Well:** SUS
14	0x0 RW	**LDO adaptive biasing (I_LDOADAPTBIAS_SELB_PP_LDO_SLV):** To enable/disable adaptive biasing scheme, by default adaptive biasing scheme is ON (active low). Common fuse. **Power Well:** SUS
13	0x0 RW	**LDO trim override select (I_LDOTRIM_OVERRIDE_SEL_PP_LDO_SLV):** Signal from unique fuse to select the LDO trim override option **Power Well:** SUS
12:7	0x1f RW	**LDO trim override (I_LDOTRIM_OVERRIDE_PP_LDO_SLV):** Inputs from unique fuse to override the FSM calibration values, In master-slave config, master and slaves LDOs need unique signals. **Power Well:** SUS
6	0x0 RW	**LDO soft start vstep (I_LDOSFTSTART_VSTEP_CFG_PP_LDO_SLV):** LDO soft start timer configuration used to select different voltage step in soft-start, from unique fuse. **Power Well:** SUS
5:0	0x0 RW	**LDO spare (I_LDOSPARE_PP_LDO_SLV):** spare digital inputs, 16 CRI used, 7 unique fuse used, 1 left, 7 common fuse used, 9 left (common fuse (10:2), unique fuse (1),) **Power Well:** SUS

7.14.134 PP LDO SLV REG 1 (PP_LDO_SLV_REG_1_PP4)—Offset 4539h

Access Method

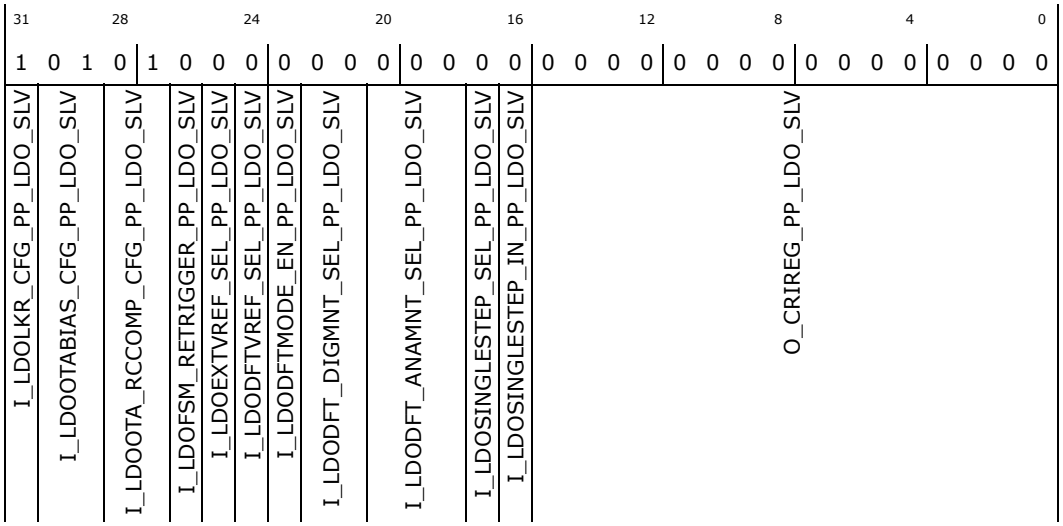
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 4539h

Op Codes:

h - Read, h - Write

Default: A8000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**LDO leaker programmability (I_LDOLKR_CFG_PP_LDO_SLV):** LDO: leaker programmability signal **Power Well:** SUS
30:29	0x1 RW	**LDO OTA tail current bias programmability (I_LDOOTABIAS_CFG_PP_LDO_SLV):** LDO: OTA tail current bias programmability **Power Well:** SUS
28:27	0x1 RW	**LDO OTA RC compensation programmability (I_LDOOTA_RCCOMP_CFG_PP_LDO_SLV):** LDO: OTA RC compensation programmability **Power Well:** SUS
26	0x0 RW	**LDO re-CAL (I_LDOFSM_RETRIGGER_PP_LDO_SLV):** LDO: To re-calibrate the LDO FSM while LDO is running **Power Well:** SUS
25	0x0 RW	**LDO external reference voltage (I_LDOEXTVREF_SEL_PP_LDO_SLV):** LDO: to select external VREF voltage **Power Well:** SUS
24	0x0 RW	**LDO DFT ref voltage (I_LDODFTVREF_SEL_PP_LDO_SLV):** LDO: to select the LDO DFT reference voltage **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
23	0x0 RW	**LDO DFT test mode enable (I_LDODFTMODE_EN_PP_LDO_SLV):** LDO: LDO DFT test mode enable **Power Well:** SUS
22:21	0x0 RW	**LDO digital monitor (I_LDODFT_DIGMNT_SEL_PP_LDO_SLV):** LDO: Digital monitor select bits **Power Well:** SUS
20:18	0x0 RW	**LDO analog monitor (I_LDODFT_ANAMNT_SEL_PP_LDO_SLV):** LDO: Analog monitor select bits **Power Well:** SUS
17	0x0 RW	**LDO single step mode (I_LDOSINGLESTEP_SEL_PP_LDO_SLV):** LDO: used in DFT mode to select single step mode **Power Well:** SUS
16	0x0 RW	**LDO custom clock (I_LDOSINGLESTEP_IN_PP_LDO_SLV):** LDO: used in DFT mode to provide custom clock **Power Well:** SUS
15:0	0x0 RO	**LDO status (O_CRIREG_PP_LDO_SLV):** 16-bit CRI output for LDO status signals. **Power Well:** SUS

7.14.135 PP LDO SLV REG 2 (PP_LDO_SLV_REG_2_PP4)—Offset 453Ah

Access Method

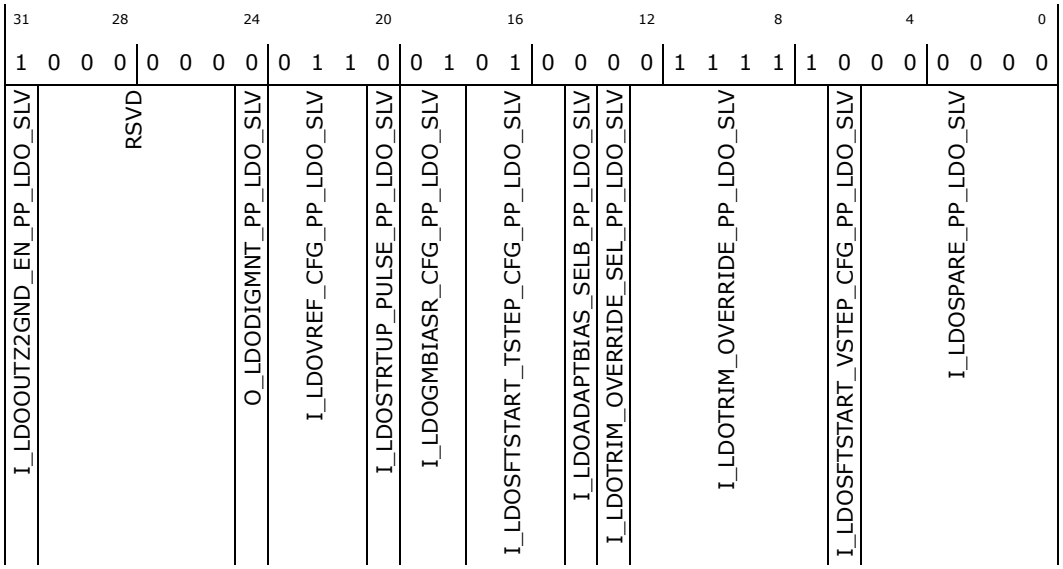
Type: Message Bus Register (Size: 32 bits)

Offset: [Port:] + 453Ah

Op Codes:

h - Read, h - Write

Default: 80650F80h



Bit Range	Default & Access	Field Name (ID): Description
31	0x1 RW	**LDO VCC output gnd or Z (I_LDOOUTZ2GND_EN_PP_LDO_SLV):** When (i_ldooutz2gnd_en AND i_pwrreq_xldo1p0)=1, the corresponding LDO output (vcc_primldo1p0_lv) vcc_xldo1p0_lv=0, otherwise, high-z. **Power Well:** SUS
30:25	0x0 RW	**RSVD:** Reserved for future use. **Power Well:** SUS
24	0x0 RO	**LDO digital monitor (O_LDODIGMNT_PP_LDO_SLV):** Feed directly to SHIP or AFE: AFE Functional or Test Mode: Functional digital monitor port. **Power Well:** SUS
23:21	0x3 RW	**LDO reference voltage (I_LDOVREF_CFG_PP_LDO_SLV):** LDO reference voltage programmability bits, from common fuse. **Power Well:** SUS
20	0x0 RW	**LDO backup gm bias (I_LDOSTRTUP_PULSE_PP_LDO_SLV):** Backup option for gm-bias startup, from common fuse **Power Well:** SUS
19:18	0x1 RW	**LDO iref resistor program (I_LDOGMBIASR_CFG_PP_LDO_SLV):** LDO Iref block - resistor programmability, from common fuse. **Power Well:** SUS

Bit Range	Default & Access	Field Name (ID): Description
17:15	0x2 RW	**LDO soft start tstep (I_LDOSFTSTART_TSTEP_CFG_PP_LDO_SLV):** LDO soft start timer configuration used to select different clock period for soft-start, from common fuse. **Power Well:** SUS
14	0x0 RW	**LDO adaptive biasing (I_LDOADAPTBIAS_SELB_PP_LDO_SLV):** To enable/disable adaptive biasing scheme, by default adaptive biasing scheme is ON (active low). Common fuse. **Power Well:** SUS
13	0x0 RW	**LDO trim override select (I_LDOTRIM_OVERRIDE_SEL_PP_LDO_SLV):** Signal from unique fuse to select the LDO trim override option **Power Well:** SUS
12:7	0x1f RW	**LDO trim override (I_LDOTRIM_OVERRIDE_PP_LDO_SLV):** Inputs from unique fuse to override the FSM calibration values, In master-slave config, master and slaves LDOs need unique signals. **Power Well:** SUS
6	0x0 RW	**LDO soft start vstep (I_LDOSFTSTART_VSTEP_CFG_PP_LDO_SLV):** LDO soft start timer configuration used to select different voltage step in soft-start, from unique fuse. **Power Well:** SUS
5:0	0x0 RW	**LDO spare (I_LDOSPARE_PP_LDO_SLV):** spare digital inputs, 16 CRI used, 7 unique fuse used, 1 left, 7 common fuse used, 9 left (common fuse (10:2), unique fuse (1),) **Power Well:** SUS

7.15 USB 3.0 I/O Configuration Registers

7.15.1 USB 3.0 TX_REGS_IO Address Map

This section contains the summary of I/O Registers for controlling the swing and de-emphasis for USB 3.0 interface.

Note: The Tx Register Bits listed below are the same for all 4 lanes [3:0] are same but the address are different. Here are the addresses for each lane:

Registers Bits	Port ID	Lane0	Lane1	Lane2	Lane3
omargin000	0x61	0x2088	0x2288	0x0088	0x0288
ow2tapgen2deemph3p5	0x61	0x2090	0x2290	0x0090	0x0290
ocalccont	0x61	0x2094	0x2294	0x0094	0x0294

Note: Please use IOSF-SB bus to access these register. The details are available in Section 25.1 in the *Braswell BIOS Writers Guide* (CDI/IBL document number 541233).

Table 7-51. Summary of USB 3.0 TX_Registers

Table 2.

ModPhy Register Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8–Bh	4	"TX_DWORD2 (tx_dword2)—Offset 8h" on page 3315	5580983Ah
10–13h	4	"TX_DWORD4 (tx_dword4)—Offset 10h" on page 3316	2B404D55h
14–17h	4	"TX_DWORD5 (tx_dword5)—Offset 14h" on page 3316	00008000h

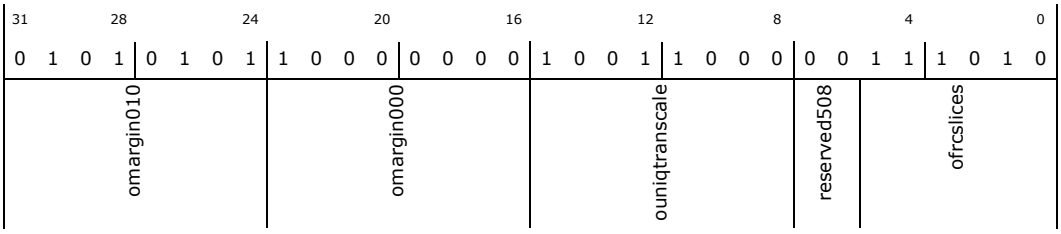
7.15.2 TX_DWORD2 (tx_dword2)—Offset 8h

Access Method

Type: I/O Register (Size: 32 bits)

Offset: 8h

Default: 5580983Ah



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x55 RW	Reserved
23:16	0x80 RW	**omargin000:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x98 RW	Reserved
7:6	0x0 RO	Reserved
5:0	0x3a RW	Reserved

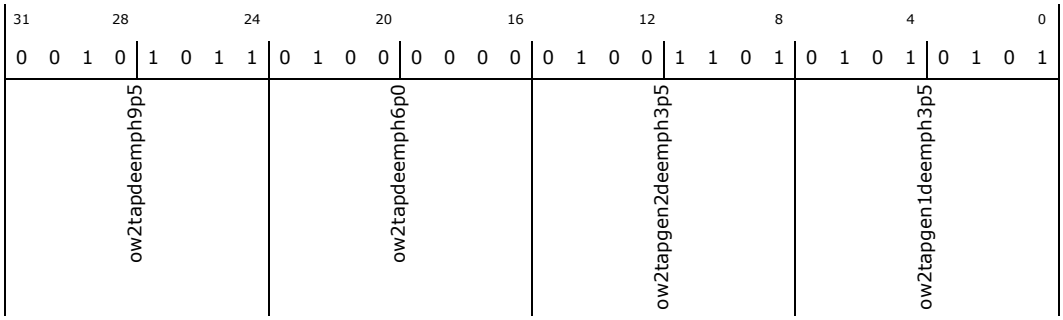
7.15.3 TX_DWORD4 (tx_dword4)—Offset 10h

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: 10h

Default: 2B404D55h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x2b RW	Reserved
23:16	0x40 RW	Reserved
15:8	0x4d RW	**ow2tapgen2deemph3p5:** Independent control for de-emphasis based on GEN1 rate protocols as factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally should be set at 3.5 dB de-emphasis.
7:0	0x55 RW	Reserved

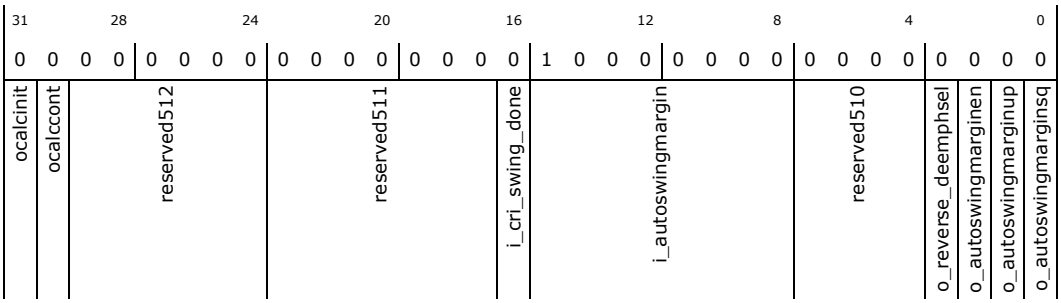
7.15.4 TX_DWORD5 (tx_dword5)—Offset 14h

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: 14h

Default: 00008000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	Reserved
30	0x0 RW	**ocalccont:** initiate calculation of swing-control circuit. While this signal is '1' the calculation is being done consecutively
29:24	0x0 RO	Reserved
23:17	0x0 RO	Reserved
16	X RO/V	Reserved
15:8	0x80 RO/V	Reserved
7:4	0x0 RO	Reserved
3	0x0 RW	Reserved
2	0x0 RW	Reserved
1	0x0 RW	Reserved
0	0x0 RW	Reserved

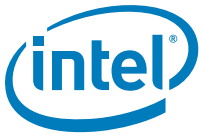
§ §

8 Low Power Engine (LPE) for Audio (I2S) Registers

8.1 LPE DMA 0 Memory Mapped I/O Registers

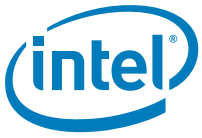
Table 52. Summary of DMA 0 Memory Mapped I/O Registers—lpe_bridge.BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"reg_SAR_type (SAR0)—Offset 0h" on page 3323	00000000h
8–Bh	4	"reg_DAR_type (DAR0)—Offset 8h" on page 3324	00000000h
10–13h	4	"reg_LLP_type (LLP0)—Offset 10h" on page 3325	00000000h
18–1Bh	4	"reg_CTL_LO_type (CTL_LO0)—Offset 18h" on page 3325	00000000h
1C–1Fh	4	"reg_CTL_HI_type (CTL_HI0)—Offset 1Ch" on page 3327	00000000h
20–23h	4	"reg_SSTAT_type (SSTAT0)—Offset 20h" on page 3329	00000000h
28–2Bh	4	"reg_DSTAT_type (DSTAT0)—Offset 28h" on page 3329	00000000h
30–33h	4	"reg_SSTATAR_type (SSTATAR0)—Offset 30h" on page 3330	00000000h
38–3Bh	4	"reg_DSTATAR_type (DSTATAR0)—Offset 38h" on page 3330	00000000h
40–43h	4	"reg_CFG_LO_type (CFG_LO0)—Offset 40h" on page 3331	00000203h
44–47h	4	"reg_CFG_HI_type (CFG_HI0)—Offset 44h" on page 3333	00000000h
48–4Bh	4	"reg_SGR_type (SGR0)—Offset 48h" on page 3334	00000000h
50–53h	4	"reg_DSR_type (DSR0)—Offset 50h" on page 3335	00000000h
58–5Bh	4	"reg_SAR_type (SAR1)—Offset 58h" on page 3335	00000000h
60–63h	4	"reg_DAR_type (DAR1)—Offset 60h" on page 3336	00000000h
68–6Bh	4	"reg_LLP_type (LLP1)—Offset 68h" on page 3337	00000000h
70–73h	4	"reg_CTL_LO_type (CTL_LO1)—Offset 70h" on page 3338	00000000h
74–77h	4	"reg_CTL_HI_type (CTL_HI1)—Offset 74h" on page 3340	00000000h
78–7Bh	4	"reg_SSTAT_type (SSTAT1)—Offset 78h" on page 3341	00000000h
80–83h	4	"reg_DSTAT_type (DSTAT1)—Offset 80h" on page 3342	00000000h
88–8Bh	4	"reg_SSTATAR_type (SSTATAR1)—Offset 88h" on page 3343	00000000h
90–93h	4	"reg_DSTATAR_type (DSTATAR1)—Offset 90h" on page 3343	00000000h
98–9Bh	4	"reg_CFG_LO_type (CFG_LO1)—Offset 98h" on page 3344	00000203h
9C–9Fh	4	"reg_CFG_HI_type (CFG_HI1)—Offset 9Ch" on page 3346	00000000h
A0–A3h	4	"reg_SGR_type (SGR1)—Offset A0h" on page 3347	00000000h
A8–ABh	4	"reg_DSR_type (DSR1)—Offset A8h" on page 3348	00000000h
B0–B3h	4	"reg_SAR_type (SAR2)—Offset B0h" on page 3348	00000000h
B8–BBh	4	"reg_DAR_type (DAR2)—Offset B8h" on page 3349	00000000h
C0–C3h	4	"reg_LLP_type (LLP2)—Offset C0h" on page 3350	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
C8–CBh	4	"reg_CTL_LO_type (CTL_LO2)—Offset C8h" on page 3351	00000000h
CC–CFh	4	"reg_CTL_HI_type (CTL_HI2)—Offset CCh" on page 3353	00000000h
D0–D3h	4	"reg_SSTAT_type (SSTAT2)—Offset D0h" on page 3354	00000000h
D8–DBh	4	"reg_DSTAT_type (DSTAT2)—Offset D8h" on page 3355	00000000h
E0–E3h	4	"reg_SSTATAR_type (SSTATAR2)—Offset E0h" on page 3356	00000000h
E8–EBh	4	"reg_DSTATAR_type (DSTATAR2)—Offset E8h" on page 3356	00000000h
F0–F3h	4	"reg_CFG_LO_type (CFG_LO2)—Offset F0h" on page 3357	00000203h
F4–F7h	4	"reg_CFG_HI_type (CFG_HI2)—Offset F4h" on page 3359	00000000h
F8–FBh	4	"reg_SGR_type (SGR2)—Offset F8h" on page 3360	00000000h
100–103h	4	"reg_DSR_type (DSR2)—Offset 100h" on page 3361	00000000h
108–10Bh	4	"reg_SAR_type (SAR3)—Offset 108h" on page 3361	00000000h
110–113h	4	"reg_DAR_type (DAR3)—Offset 110h" on page 3362	00000000h
118–11Bh	4	"reg_LLP_type (LLP3)—Offset 118h" on page 3363	00000000h
120–123h	4	"reg_CTL_LO_type (CTL_LO3)—Offset 120h" on page 3364	00000000h
124–127h	4	"reg_CTL_HI_type (CTL_HI3)—Offset 124h" on page 3366	00000000h
128–12Bh	4	"reg_SSTAT_type (SSTAT3)—Offset 128h" on page 3367	00000000h
130–133h	4	"reg_DSTAT_type (DSTAT3)—Offset 130h" on page 3368	00000000h
138–13Bh	4	"reg_SSTATAR_type (SSTATAR3)—Offset 138h" on page 3369	00000000h
140–143h	4	"reg_DSTATAR_type (DSTATAR3)—Offset 140h" on page 3369	00000000h
148–14Bh	4	"reg_CFG_LO_type (CFG_LO3)—Offset 148h" on page 3370	00000203h
14C–14Fh	4	"reg_CFG_HI_type (CFG_HI3)—Offset 14Ch" on page 3372	00000000h
150–153h	4	"reg_SGR_type (SGR3)—Offset 150h" on page 3373	00000000h
158–15Bh	4	"reg_DSR_type (DSR3)—Offset 158h" on page 3374	00000000h
160–163h	4	"reg_SAR_type (SAR4)—Offset 160h" on page 3374	00000000h
168–16Bh	4	"reg_DAR_type (DAR4)—Offset 168h" on page 3375	00000000h
170–173h	4	"reg_LLP_type (LLP4)—Offset 170h" on page 3376	00000000h
178–17Bh	4	"reg_CTL_LO_type (CTL_LO4)—Offset 178h" on page 3377	00000000h
17C–17Fh	4	"reg_CTL_HI_type (CTL_HI4)—Offset 17Ch" on page 3379	00000000h
180–183h	4	"reg_SSTAT_type (SSTAT4)—Offset 180h" on page 3380	00000000h
188–18Bh	4	"reg_DSTAT_type (DSTAT4)—Offset 188h" on page 3381	00000000h
190–193h	4	"reg_SSTATAR_type (SSTATAR4)—Offset 190h" on page 3382	00000000h
198–19Bh	4	"reg_DSTATAR_type (DSTATAR4)—Offset 198h" on page 3382	00000000h
1A0–1A3h	4	"reg_CFG_LO_type (CFG_LO4)—Offset 1A0h" on page 3383	00000203h
1A4–1A7h	4	"reg_CFG_HI_type (CFG_HI4)—Offset 1A4h" on page 3385	00000000h
1A8–1ABh	4	"reg_SGR_type (SGR4)—Offset 1A8h" on page 3386	00000000h
1B0–1B3h	4	"reg_DSR_type (DSR4)—Offset 1B0h" on page 3387	00000000h
1B8–1BBh	4	"reg_SAR_type (SAR5)—Offset 1B8h" on page 3387	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1C0–1C3h	4	"reg_DAR_type (DAR5)—Offset 1C0h" on page 3388	00000000h
1C8–1CBh	4	"reg_LLP_type (LLP5)—Offset 1C8h" on page 3389	00000000h
1D0–1D3h	4	"reg_CTL_LO_type (CTL_LO5)—Offset 1D0h" on page 3390	00000000h
1D4–1D7h	4	"reg_CTL_HI_type (CTL_HI5)—Offset 1D4h" on page 3392	00000000h
1D8–1DBh	4	"reg_SSTAT_type (SSTAT5)—Offset 1D8h" on page 3393	00000000h
1E0–1E3h	4	"reg_DSTAT_type (DSTAT5)—Offset 1E0h" on page 3394	00000000h
1E8–1EBh	4	"reg_SSTATAR_type (SSTATAR5)—Offset 1E8h" on page 3395	00000000h
1F0–1F3h	4	"reg_DSTATAR_type (DSTATAR5)—Offset 1F0h" on page 3395	00000000h
1F8–1FBh	4	"reg_CFG_LO_type (CFG_LO5)—Offset 1F8h" on page 3396	00000203h
1FC–1FFh	4	"reg_CFG_HI_type (CFG_HI5)—Offset 1FCh" on page 3398	00000000h
200–203h	4	"reg_SGR_type (SGR5)—Offset 200h" on page 3399	00000000h
208–20Bh	4	"reg_DSR_type (DSR5)—Offset 208h" on page 3400	00000000h
210–213h	4	"reg_SAR_type (SAR6)—Offset 210h" on page 3400	00000000h
218–21Bh	4	"reg_DAR_type (DAR6)—Offset 218h" on page 3401	00000000h
220–223h	4	"reg_LLP_type (LLP6)—Offset 220h" on page 3402	00000000h
228–22Bh	4	"reg_CTL_LO_type (CTL_LO6)—Offset 228h" on page 3403	00000000h
22C–22Fh	4	"reg_CTL_HI_type (CTL_HI6)—Offset 22Ch" on page 3405	00000000h
230–233h	4	"reg_SSTAT_type (SSTAT6)—Offset 230h" on page 3406	00000000h
238–23Bh	4	"reg_DSTAT_type (DSTAT6)—Offset 238h" on page 3407	00000000h
240–243h	4	"reg_SSTATAR_type (SSTATAR6)—Offset 240h" on page 3408	00000000h
248–24Bh	4	"reg_DSTATAR_type (DSTATAR6)—Offset 248h" on page 3408	00000000h
250–253h	4	"reg_CFG_LO_type (CFG_LO6)—Offset 250h" on page 3409	00000203h
254–257h	4	"reg_CFG_HI_type (CFG_HI6)—Offset 254h" on page 3411	00000000h
258–25Bh	4	"reg_SGR_type (SGR6)—Offset 258h" on page 3412	00000000h
260–263h	4	"reg_DSR_type (DSR6)—Offset 260h" on page 3413	00000000h
268–26Bh	4	"reg_SAR_type (SAR7)—Offset 268h" on page 3413	00000000h
270–273h	4	"reg_DAR_type (DAR7)—Offset 270h" on page 3414	00000000h
278–27Bh	4	"reg_LLP_type (LLP7)—Offset 278h" on page 3415	00000000h
280–283h	4	"reg_CTL_LO_type (CTL_LO7)—Offset 280h" on page 3416	00000000h
284–287h	4	"reg_CTL_HI_type (CTL_HI7)—Offset 284h" on page 3418	00000000h
288–28Bh	4	"reg_SSTAT_type (SSTAT7)—Offset 288h" on page 3419	00000000h
290–293h	4	"reg_DSTAT_type (DSTAT7)—Offset 290h" on page 3420	00000000h
298–29Bh	4	"reg_SSTATAR_type (SSTATAR7)—Offset 298h" on page 3421	00000000h
2A0–2A3h	4	"reg_DSTATAR_type (DSTATAR7)—Offset 2A0h" on page 3421	00000000h
2A8–2ABh	4	"reg_CFG_LO_type (CFG_LO7)—Offset 2A8h" on page 3422	00000203h
2AC–2AFh	4	"reg_CFG_HI_type (CFG_HI7)—Offset 2ACh" on page 3424	00000000h
2B0–2B3h	4	"reg_SGR_type (SGR7)—Offset 2B0h" on page 3425	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2B8–2BBh	4	"reg_DSR_type (DSR7)—Offset 2B8h" on page 3426	00000000h
2C0–2C3h	4	"reg_Raw_type (RawTfr)—Offset 2C0h" on page 3426	00000000h
2C8–2CBh	4	"reg_Raw_type (RawBlock)—Offset 2C8h" on page 3427	00000000h
2D0–2D3h	4	"reg_Raw_type (RawSrcTran)—Offset 2D0h" on page 3427	00000000h
2D8–2DBh	4	"reg_Raw_type (RawDstTran)—Offset 2D8h" on page 3428	00000000h
2E0–2E3h	4	"reg_Raw_type (RawErr)—Offset 2E0h" on page 3429	00000000h
2E8–2EBh	4	"reg_Status_type (StatusTfr)—Offset 2E8h" on page 3429	00000000h
2F0–2F3h	4	"reg_Status_type (StatusBlock)—Offset 2F0h" on page 3430	00000000h
2F8–2FBh	4	"reg_Status_type (StatusSrcTran)—Offset 2F8h" on page 3431	00000000h
300–303h	4	"reg_Status_type (StatusDstTran)—Offset 300h" on page 3431	00000000h
308–30Bh	4	"reg_Status_type (StatusErr)—Offset 308h" on page 3432	00000000h
310–313h	4	"reg_Mask_type (MaskTfr)—Offset 310h" on page 3432	00000000h
318–31Bh	4	"reg_Mask_type (MaskBlock)—Offset 318h" on page 3433	00000000h
320–323h	4	"reg_Mask_type (MaskSrcTran)—Offset 320h" on page 3434	00000000h
328–32Bh	4	"reg_Mask_type (MaskDstTran)—Offset 328h" on page 3435	00000000h
330–333h	4	"reg_Mask_type (MaskErr)—Offset 330h" on page 3436	00000000h
338–33Bh	4	"reg_Clear_type (ClearTfr)—Offset 338h" on page 3437	00000000h
340–343h	4	"reg_Clear_type (ClearBlock)—Offset 340h" on page 3438	00000000h
348–34Bh	4	"reg_Clear_type (ClearSrcTran)—Offset 348h" on page 3438	00000000h
350–353h	4	"reg_Clear_type (ClearDstTran)—Offset 350h" on page 3439	00000000h
358–35Bh	4	"reg_Clear_type (ClearErr)—Offset 358h" on page 3439	00000000h
360–363h	4	"reg_StatusInt_type (StatusInt)—Offset 360h" on page 3440	00000000h
398–39Bh	4	"reg_DmaCfgReg_type (DmaCfgReg)—Offset 398h" on page 3441	00000000h
3A0–3A3h	4	"reg_ChEnReg_type (ChEnReg)—Offset 3A0h" on page 3441	00000000h
3B8–3BBh	4	"reg_CLASS_PRIORITY0_LO_type (ClassPriority0_LO)—Offset 3B8h" on page 3442	00000000h
3BC–3BFh	4	"reg_CLASS_PRIORITY0_HI_type (ClassPriority0_HI)—Offset 3BCh" on page 3443	00000000h
3C0–3C3h	4	"reg_CLASS_PRIORITY1_LO_type (ClassPriority1_LO)—Offset 3C0h" on page 3443	00000000h
3C4–3C7h	4	"reg_CLASS_PRIORITY1_HI_type (ClassPriority1_HI)—Offset 3C4h" on page 3444	00000000h
400–403h	4	"reg_FIFO_PARTITION0_LO_type (FifoPartition0_LO)—Offset 400h" on page 3444	00000000h
404–407h	4	"reg_FIFO_PARTITION0_HI_type (FifoPartition0_HI)—Offset 404h" on page 3445	00000000h
408–40Bh	4	"reg_FIFO_PARTITION1_LO_type (FifoPartition1_LO)—Offset 408h" on page 3446	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40C–40Fh	4	"reg_FIFO_PARTITION1_HI_type (FifoPartition1_HI)—Offset 40Ch" on page 3446	00000000h
410–413h	4	"reg_SAI_Error_type (SAI_ERR)—Offset 410h" on page 3447	00000000h
418–41Bh	4	"reg_GLOBAL_CFG_type (GLOBAL_CFG)—Offset 418h" on page 3447	00000000h

8.1.1 reg_SAR_type (SAR0)—Offset 0h

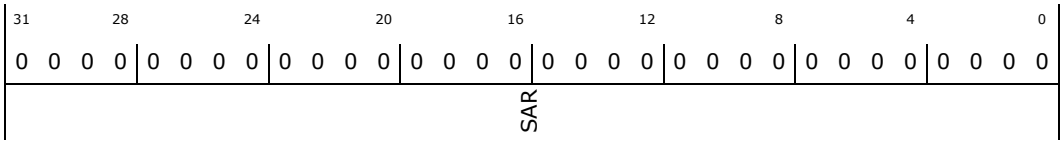
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.1.2 reg_DAR_type (DAR0)—Offset 8h

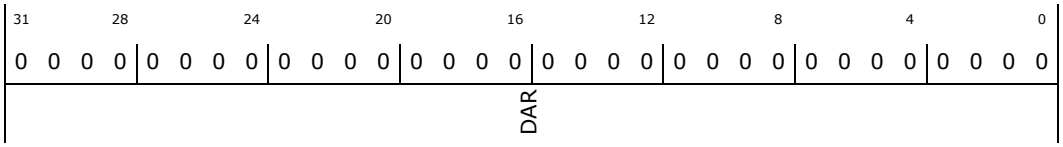
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

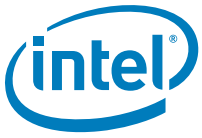
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported



8.1.3 reg_LLP_type (LLP0)—Offset 10h

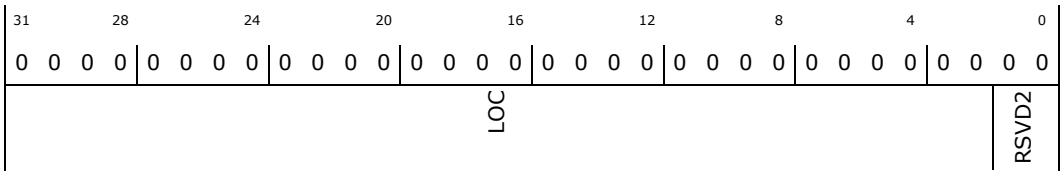
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.1.4 reg_CTL_LO_type (CTL_LO0)—Offset 18h

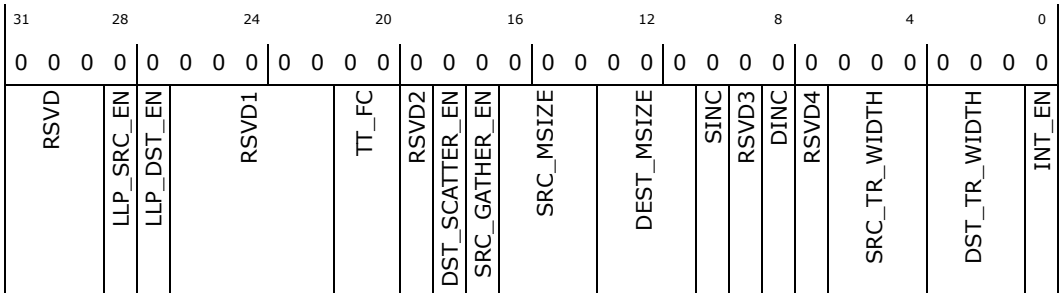
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

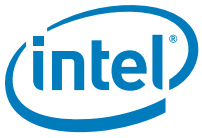
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 18h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.



Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.1.5 reg_CTL_HI_type (CTL_HI0)—Offset 1Ch

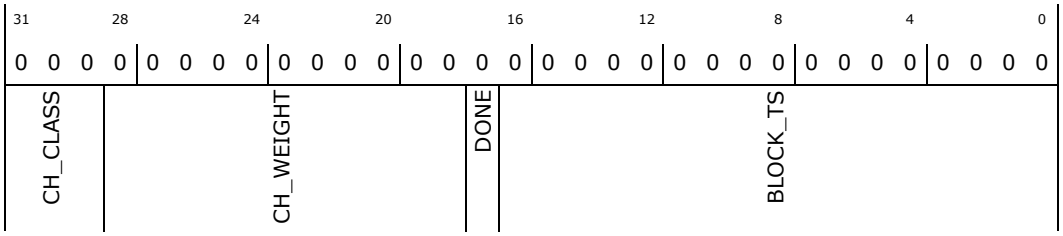
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 1Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesn't mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.1.6 reg_SSTAT_type (SSTAT0)—Offset 20h

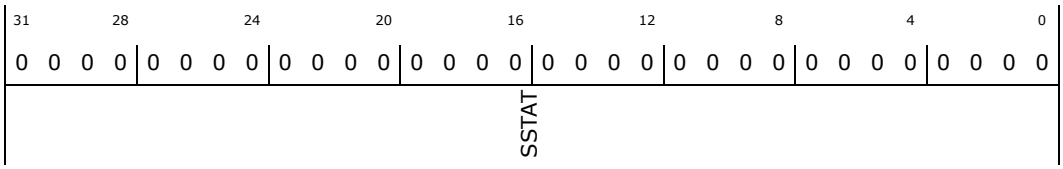
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 20h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.1.7 reg_DSTAT_type (DSTAT0)—Offset 28h

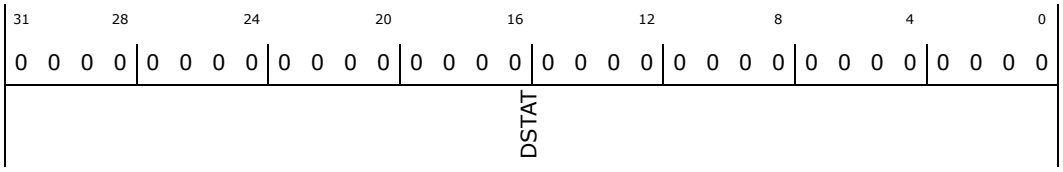
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 28h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.1.8 reg_SSTATAR_type (SSTATAR0)—Offset 30h

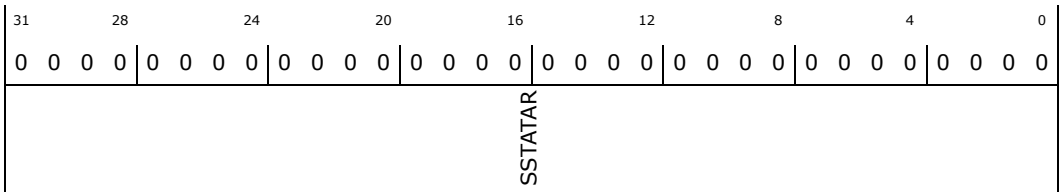
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.1.9 reg_DSTATAR_type (DSTATAR0)—Offset 38h

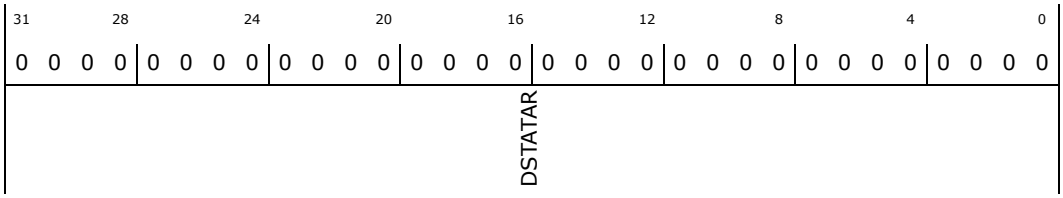
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 38h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.1.10 reg_CFG_LO_type (CFG_LO0)—Offset 40h

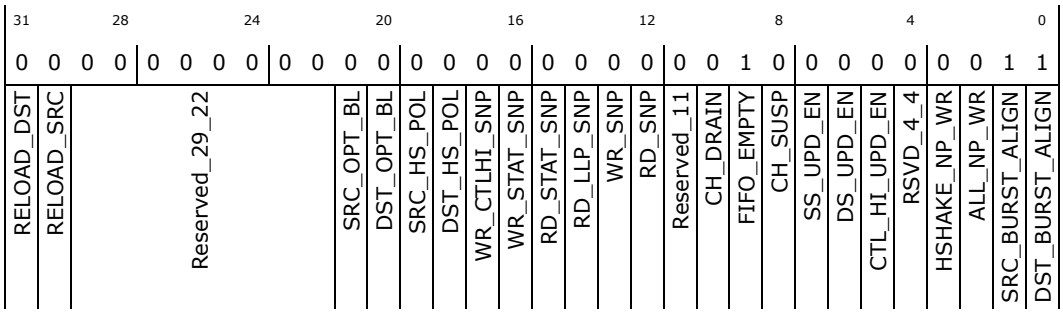
This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 40h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled

Bit Range	Default & Access	Field Name (ID): Description
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.1.11 reg_CFG_HI_type (CFG_HI0)—Offset 44h

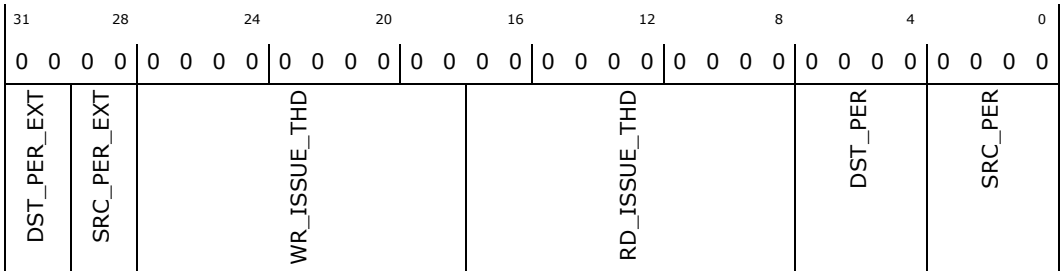
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 44h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.

Bit Range	Default & Access	Field Name (ID): Description
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

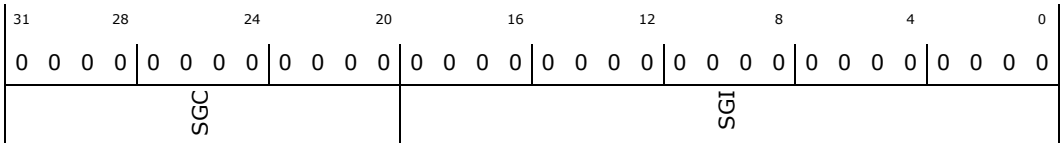
8.1.12 reg_SGR_type (SGR0)—Offset 48h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** [lpe_bridge.BAR + 98000h] + 48h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.1.13 reg_DSR_type (DSR0)—Offset 50h

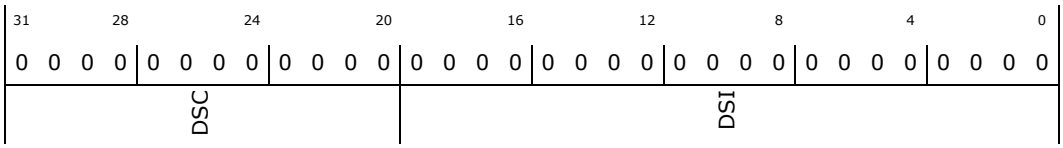
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 50h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.1.14 reg_SAR_type (SAR1)—Offset 58h

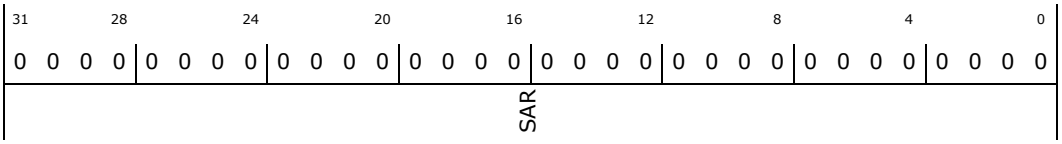
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 58h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.1.15 reg_DAR_type (DAR1)—Offset 60h

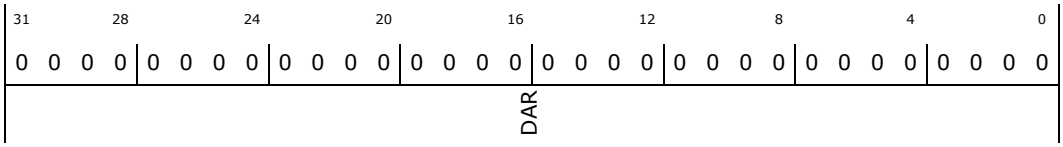
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 60h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.1.16 reg_LLP_type (LLP1)—Offset 68h

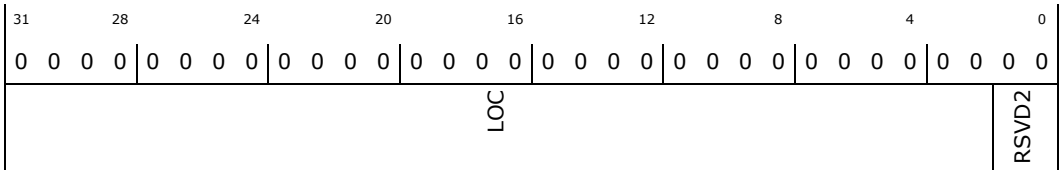
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 68h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.1.17 reg_CTL_LO_type (CTL_LO1)—Offset 70h

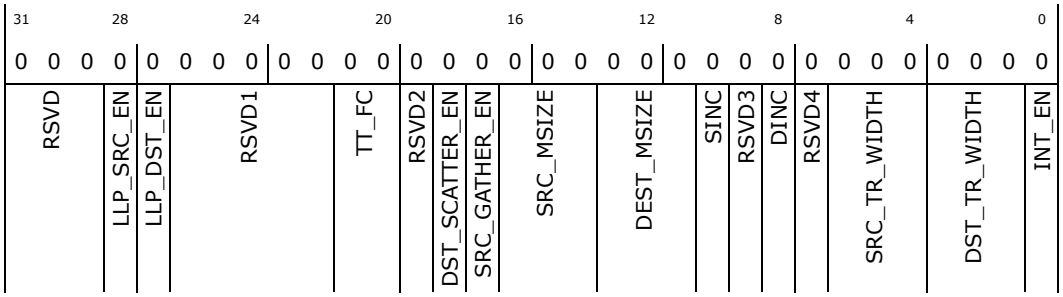
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 70h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)

Bit Range	Default & Access	Field Name (ID): Description
26:22	0x0 RO	**RSVD1:** RSVD
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.1.18 reg_CTL_HI_type (CTL_HI1)—Offset 74h

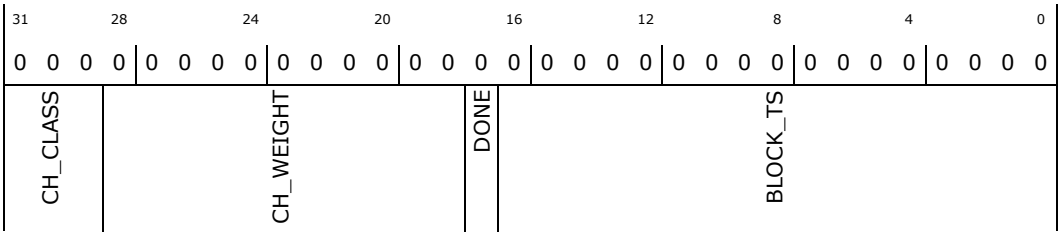
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

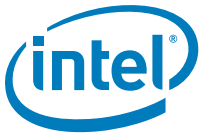
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 74h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below



Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesn't mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.1.19 reg_SSTAT_type (SSTAT1)—Offset 78h

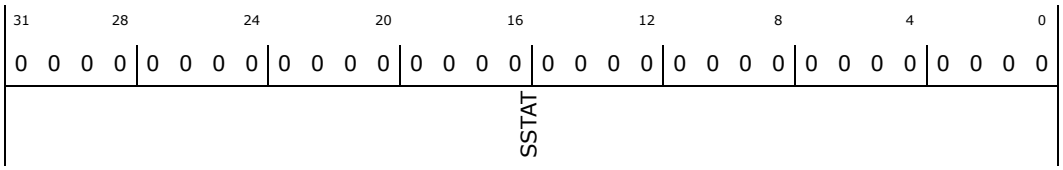
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 78h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.1.20 reg_DSTAT_type (DSTAT1)—Offset 80h

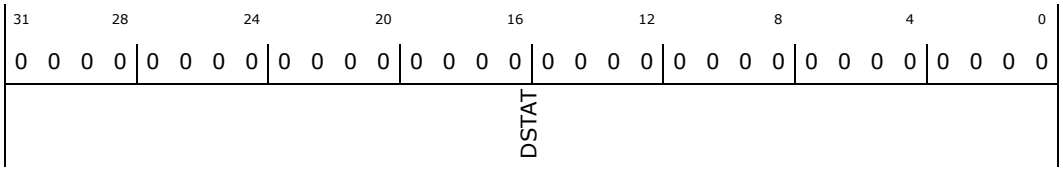
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 98000h] + 80h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.1.21 reg_SSTATAR_type (SSTATAR1)—Offset 88h

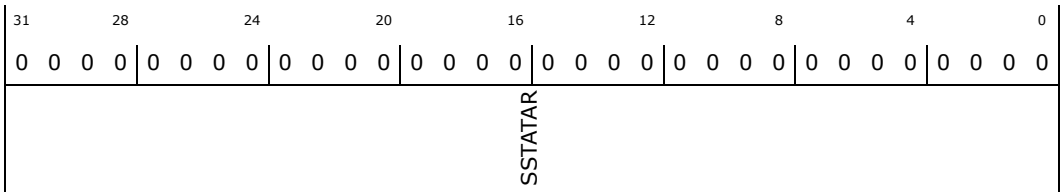
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 88h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.1.22 reg_DSTATAR_type (DSTATAR1)—Offset 90h

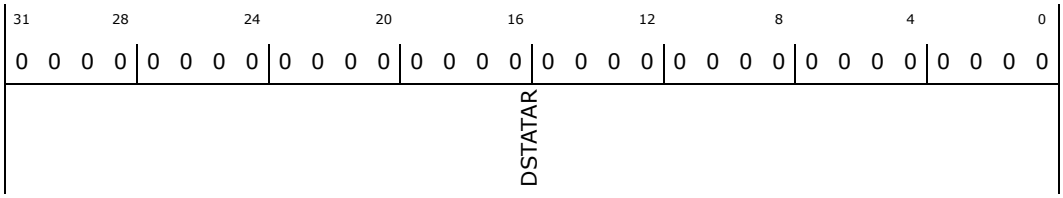
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 90h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.1.23 reg_CFG_LO_type (CFG_LO1)—Offset 98h

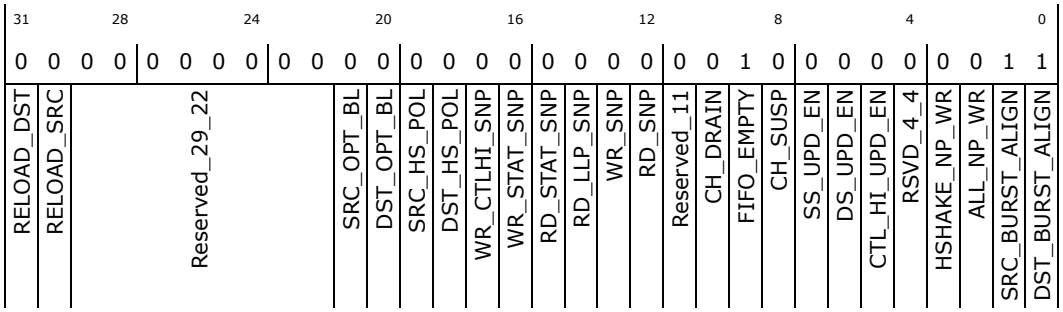
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 98h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.1.24 reg_CFG_HI_type (CFG_HI1)—Offset 9Ch

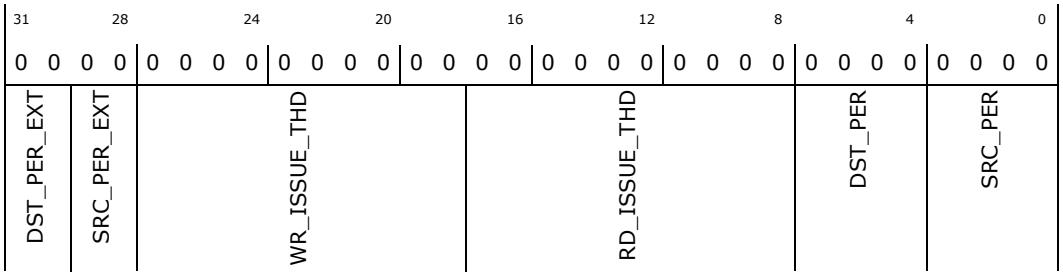
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

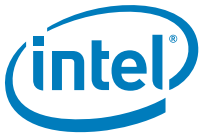
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 9Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.



Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.1.25 reg_SGR_type (SGR1)—Offset A0h

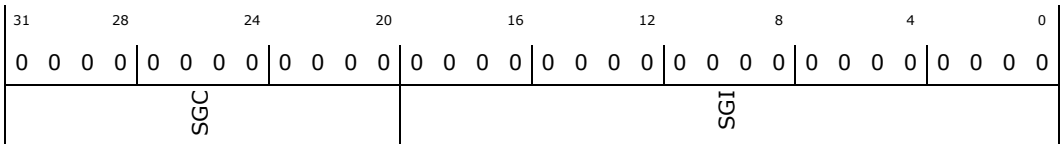
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.1.26 reg_DSR_type (DSR1)—Offset A8h

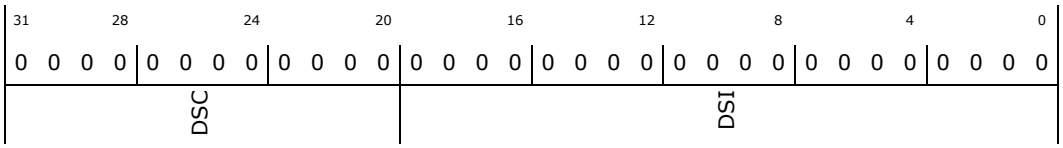
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.1.27 reg_SAR_type (SAR2)—Offset B0h

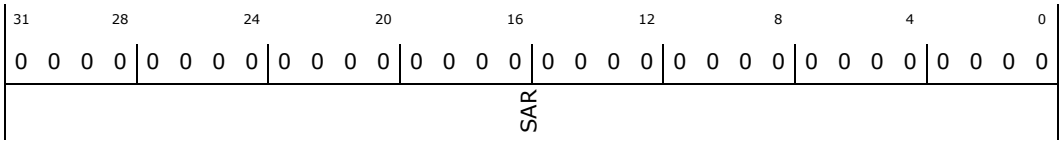
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.1.28 reg_DAR_type (DAR2)—Offset B8h

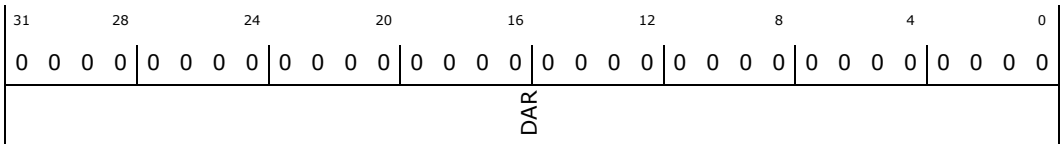
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.1.29 reg_LLP_type (LLP2)—Offset C0h

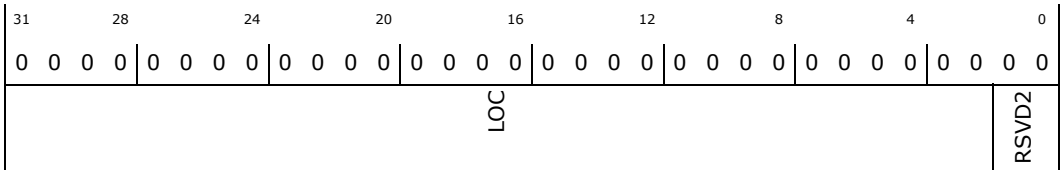
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.1.30 reg_CTL_LO_type (CTL_LO2)—Offset C8h

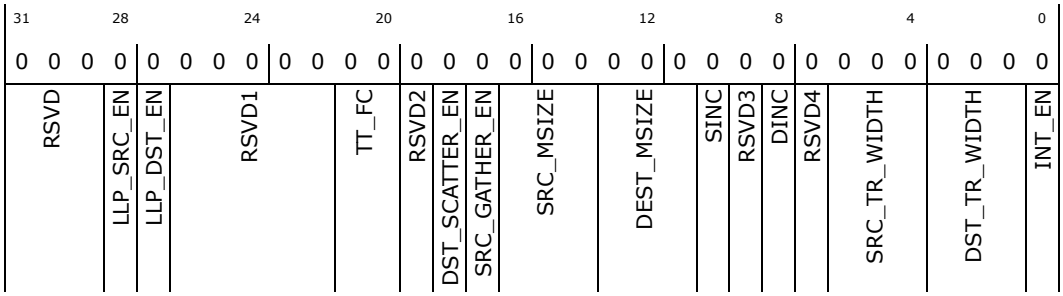
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + C8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.1.31 reg_CTL_HI_type (CTL_HI2)—Offset CCh

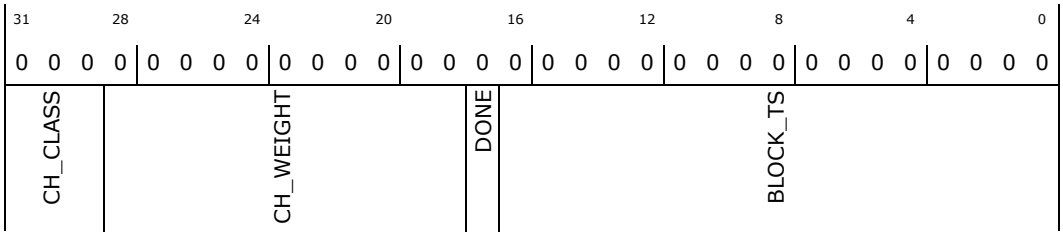
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + CCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesn't mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.1.32 reg_SSTAT_type (SSTAT2)—Offset D0h

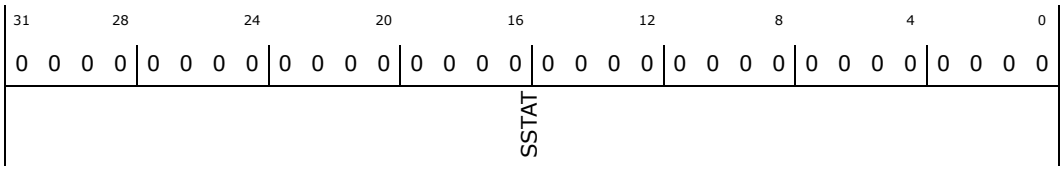
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.1.33 reg_DSTAT_type (DSTAT2)—Offset D8h

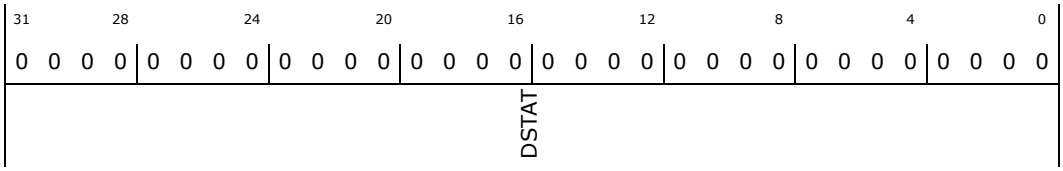
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + D8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.1.34 reg_SSTATAR_type (SSTATAR2)—Offset E0h

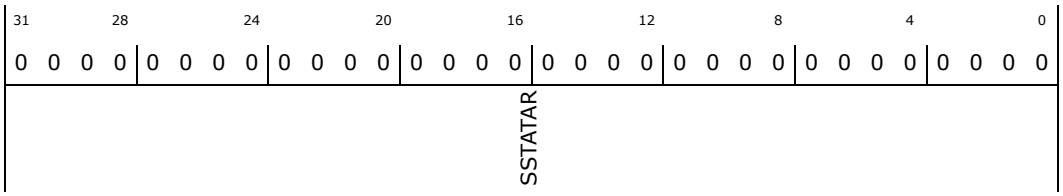
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + E0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.1.35 reg_DSTATAR_type (DSTATAR2)—Offset E8h

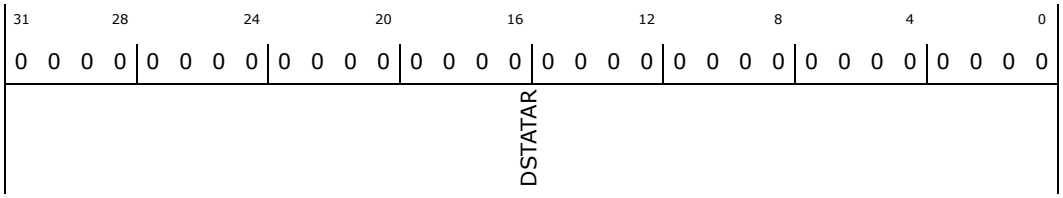
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + E8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.1.36 reg_CFG_LO_type (CFG_LO2)—Offset F0h

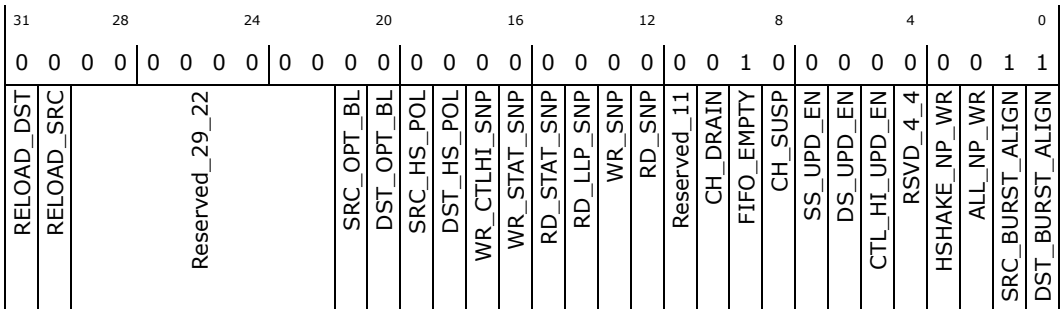
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + F0h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.1.37 reg_CFG_HI_type (CFG_HI2)—Offset F4h

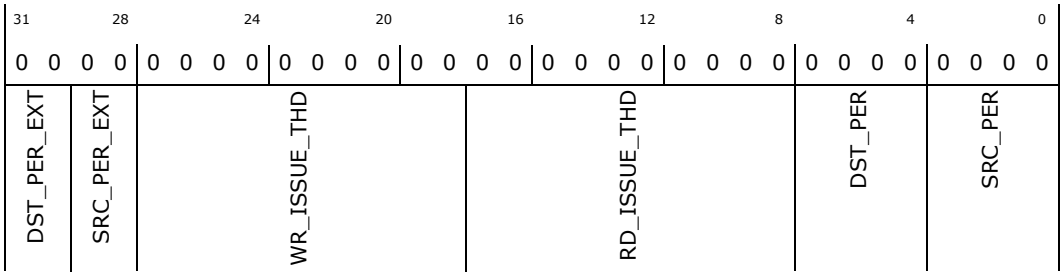
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + F4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.1.38 reg_SGR_type (SGR2)—Offset F8h

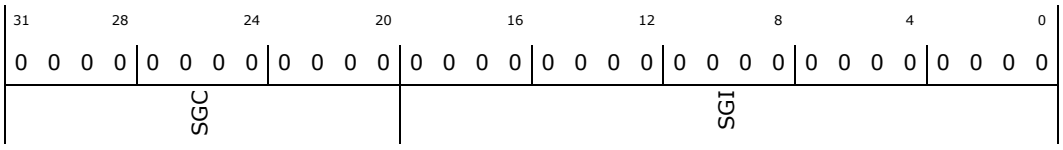
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.1.39 reg_DSR_type (DSR2)—Offset 100h

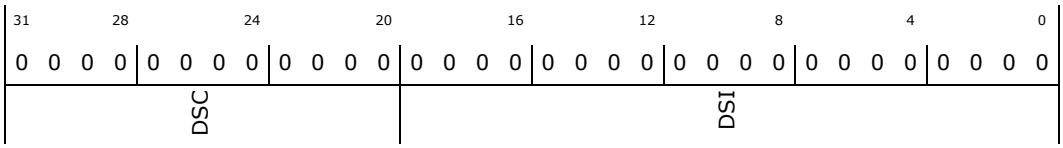
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 100h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.1.40 reg_SAR_type (SAR3)—Offset 108h

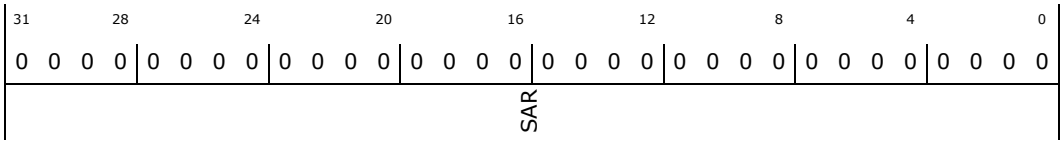
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 108h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.1.41 reg_DAR_type (DAR3)—Offset 110h

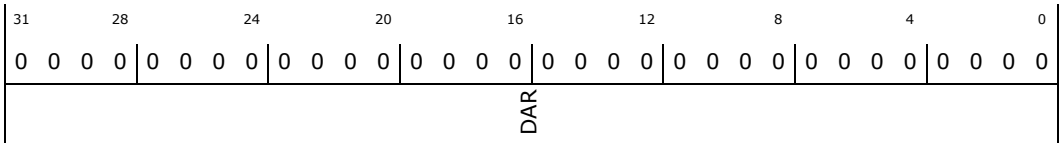
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

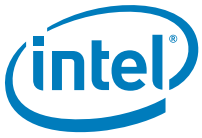
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 110h

Default: 00000000h





Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.1.42 reg_LLP_type (LLP3)—Offset 118h

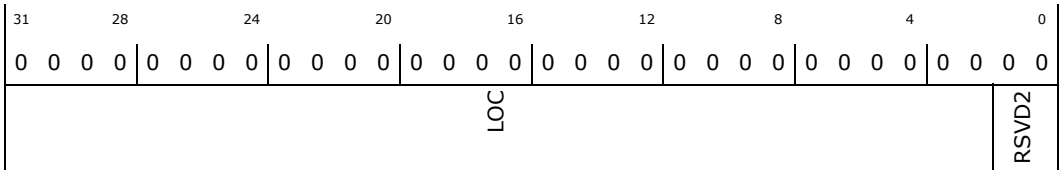
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 118h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.1.43 reg_CTL_LO_type (CTL_LO3)—Offset 120h

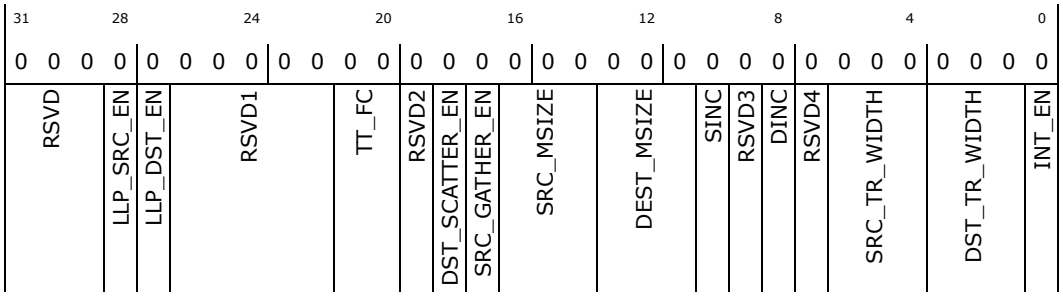
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 120h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.1.44 reg_CTL_HI_type (CTL_HI3)—Offset 124h

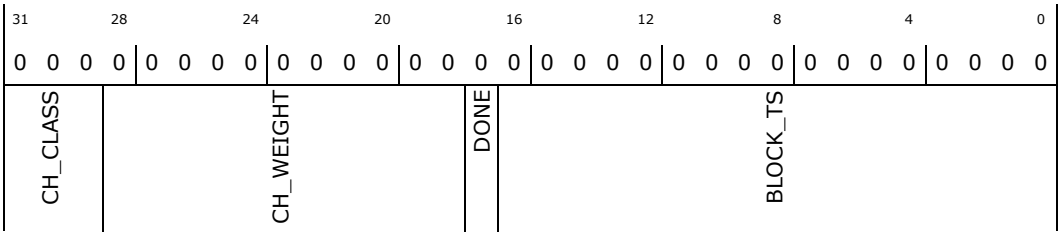
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

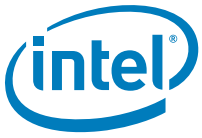
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 124h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below



Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesn't mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.1.45 reg_SSTAT_type (SSTAT3)—Offset 128h

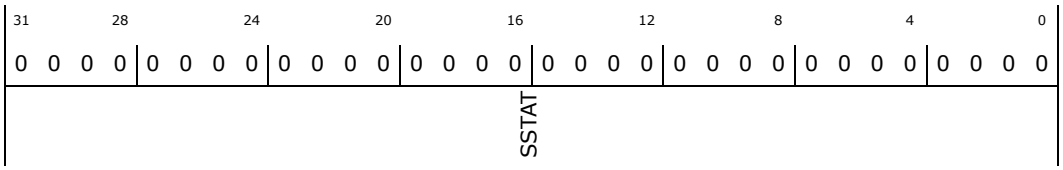
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 128h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.1.46 reg_DSTAT_type (DSTAT3)—Offset 130h

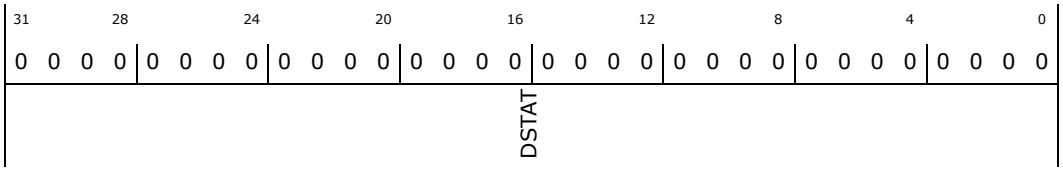
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 130h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.1.47 reg_SSTATAR_type (SSTATAR3)—Offset 138h

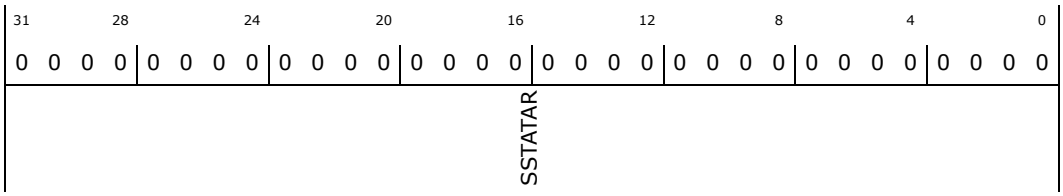
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 138h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.1.48 reg_DSTATAR_type (DSTATAR3)—Offset 140h

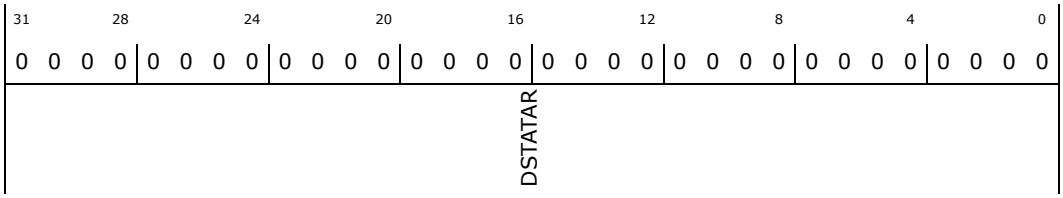
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 140h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.1.49 reg_CFG_LO_type (CFG_LO3)—Offset 148h

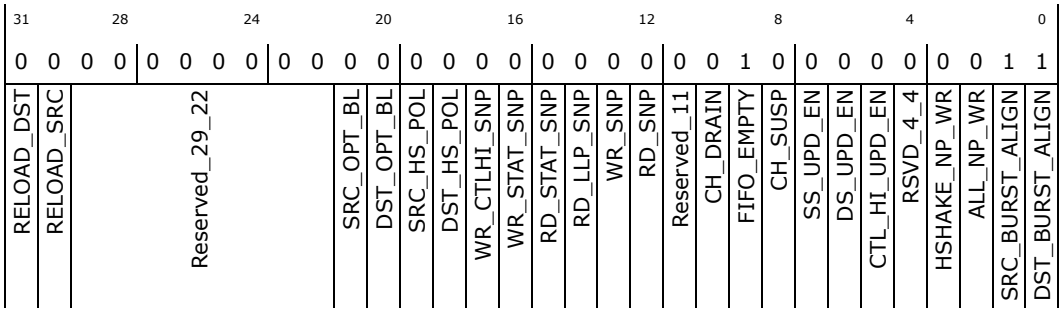
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 148h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.1.50 reg_CFG_HI_type (CFG_HI3)—Offset 14Ch

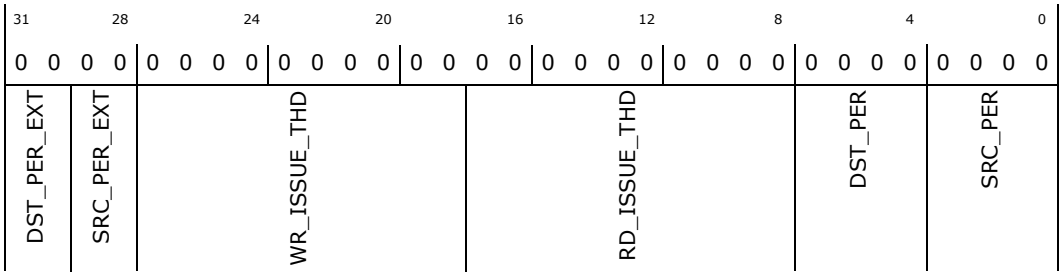
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 14Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.1.51 reg_SGR_type (SGR3)—Offset 150h

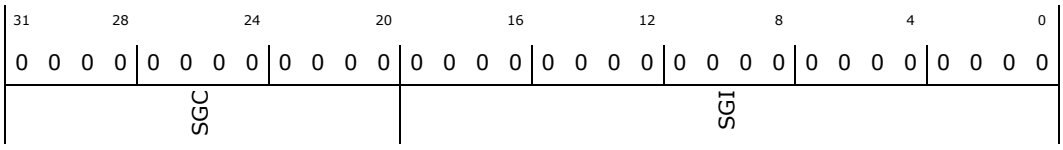
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 150h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.1.52 reg_DSR_type (DSR3)—Offset 158h

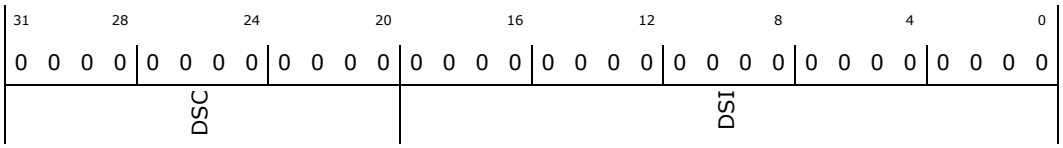
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 158h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.1.53 reg_SAR_type (SAR4)—Offset 160h

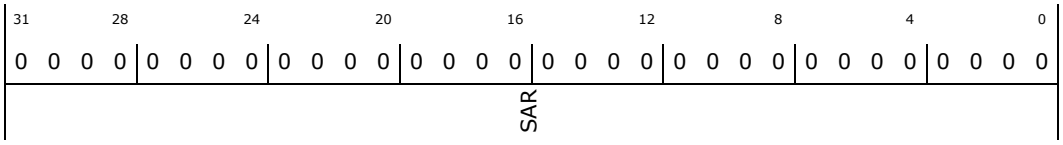
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 160h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.1.54 reg_DAR_type (DAR4)—Offset 168h

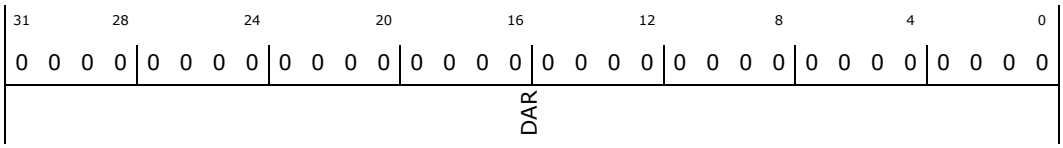
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 168h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.1.55 reg_LLP_type (LLP4)—Offset 170h

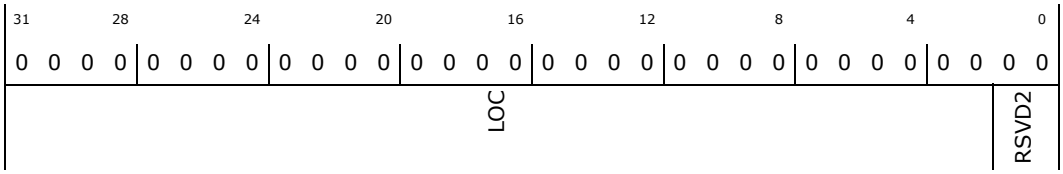
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 170h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.1.56 reg_CTL_LO_type (CTL_LO4)—Offset 178h

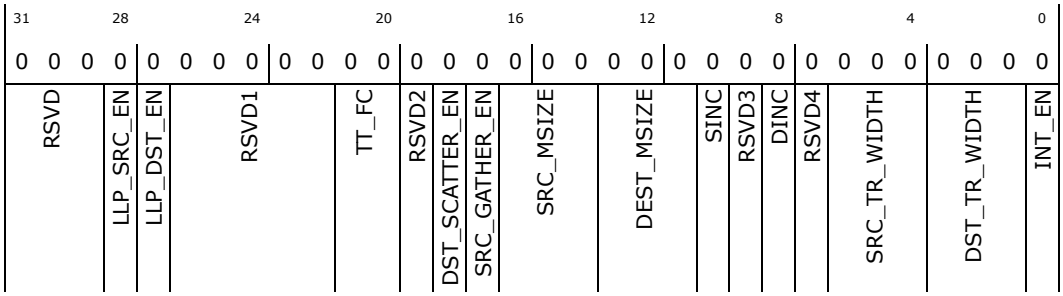
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 178h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.1.57 reg_CTL_HI_type (CTL_HI4)—Offset 17Ch

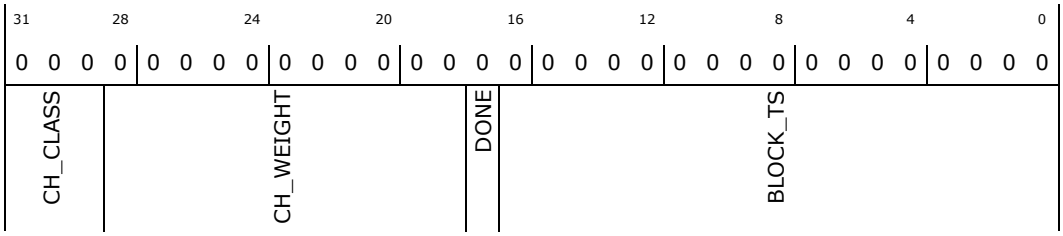
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 17Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesn't mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.1.58 reg_SSTAT_type (SSTAT4)—Offset 180h

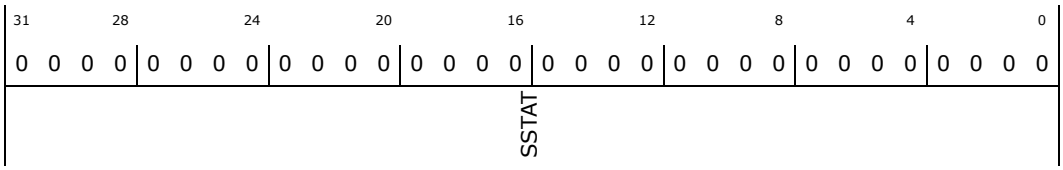
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 180h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.1.59 reg_DSTAT_type (DSTAT4)—Offset 188h

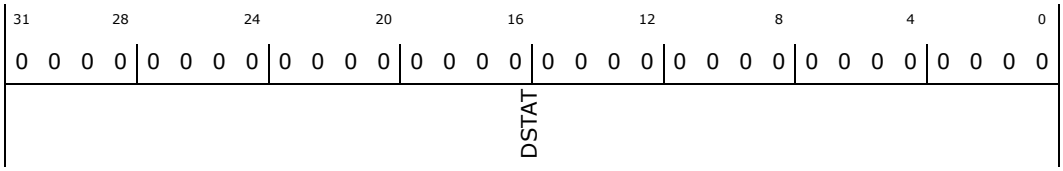
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 188h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.1.60 reg_SSTATAR_type (SSTATAR4)—Offset 190h

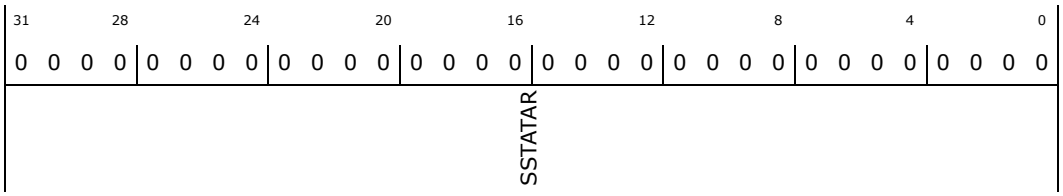
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 190h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.1.61 reg_DSTATAR_type (DSTATAR4)—Offset 198h

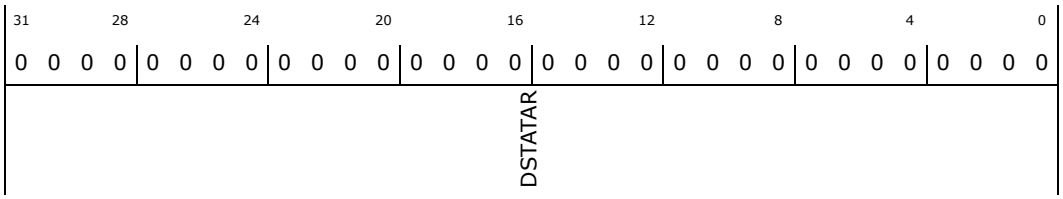
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 198h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.1.62 reg_CFG_LO_type (CFG_LO4)—Offset 1A0h

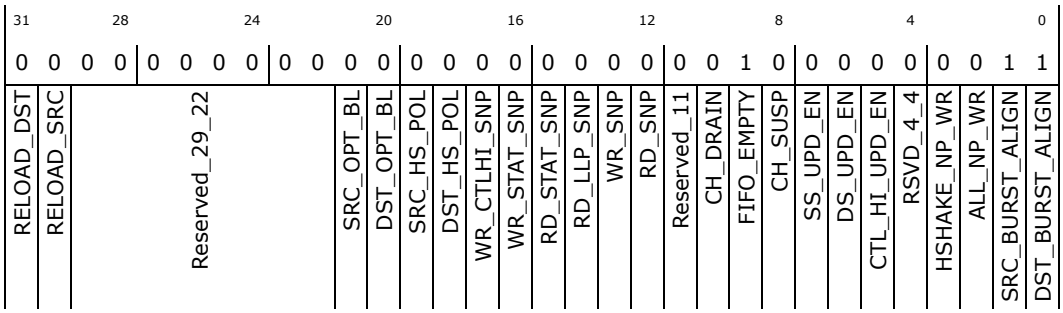
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 1A0h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.1.63 reg_CFG_HI_type (CFG_HI4)—Offset 1A4h

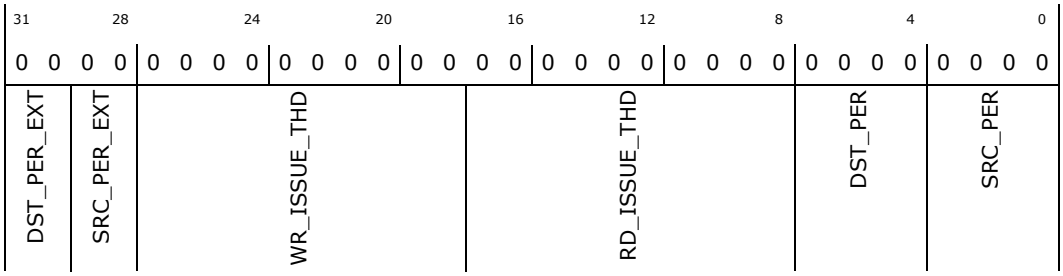
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 1A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.1.64 reg_SGR_type (SGR4)—Offset 1A8h

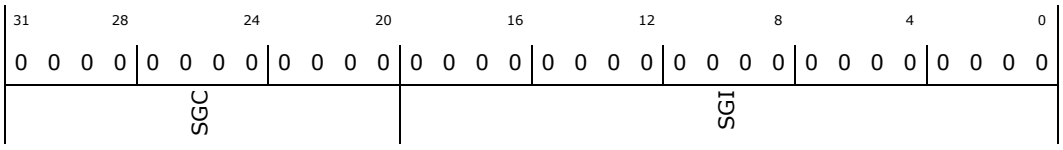
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 1A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.1.65 reg_DSR_type (DSR4)—Offset 1B0h

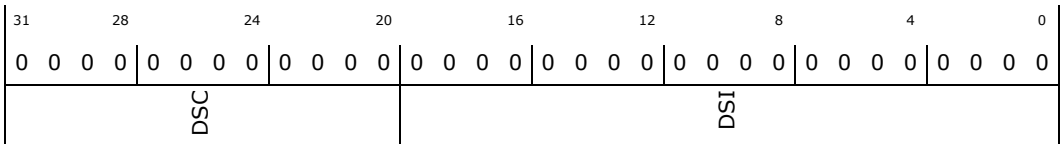
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 1B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.1.66 reg_SAR_type (SAR5)—Offset 1B8h

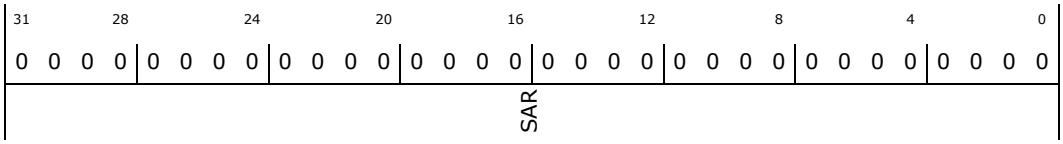
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 1B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.1.67 reg_DAR_type (DAR5)—Offset 1C0h

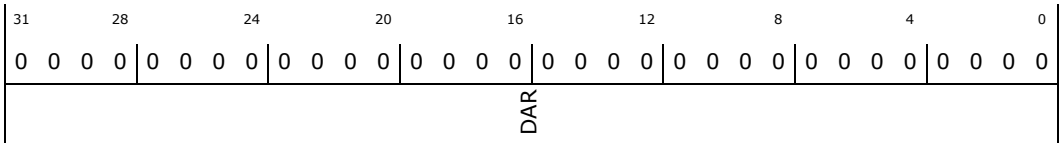
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

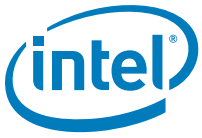
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 1C0h

Default: 00000000h





Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.1.68 reg_LLP_type (LLP5)—Offset 1C8h

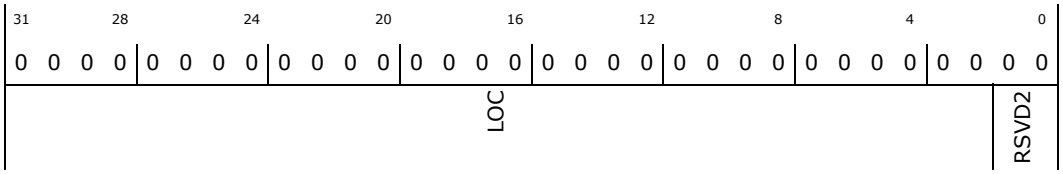
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 1C8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.1.69 reg_CTL_LO_type (CTL_LO5)—Offset 1D0h

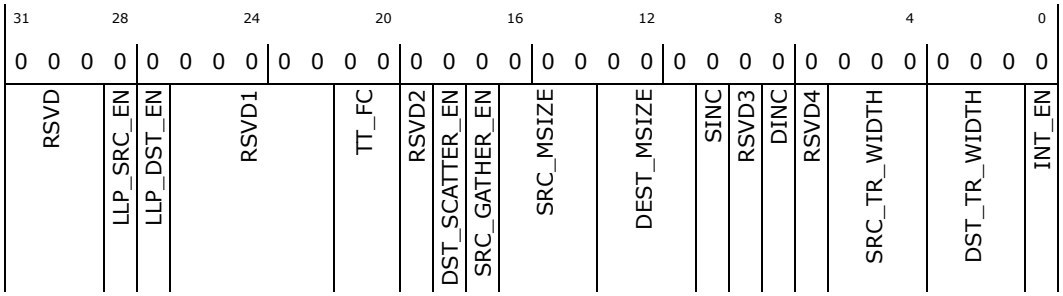
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 1D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.1.70 reg_CTL_HI_type (CTL_HI5)—Offset 1D4h

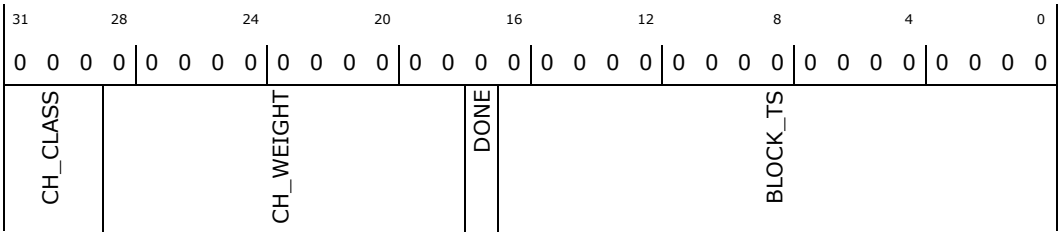
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

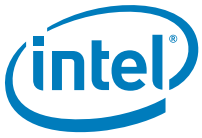
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 1D4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below



Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesn't mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.1.71 reg_SSTAT_type (SSTAT5)—Offset 1D8h

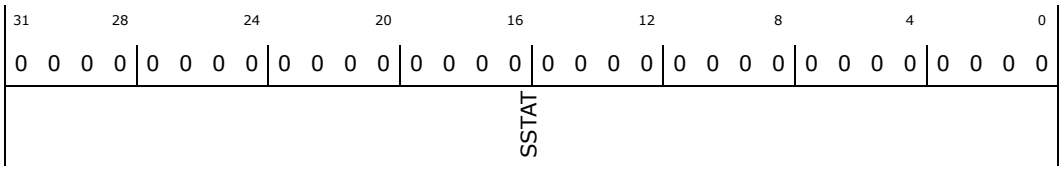
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 1D8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.1.72 reg_DSTAT_type (DSTAT5)—Offset 1E0h

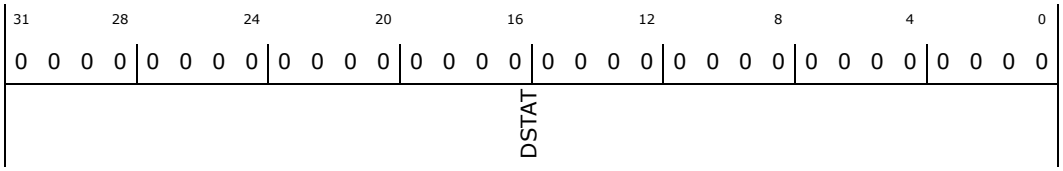
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 1E0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.1.73 reg_SSTATAR_type (SSTATAR5)—Offset 1E8h

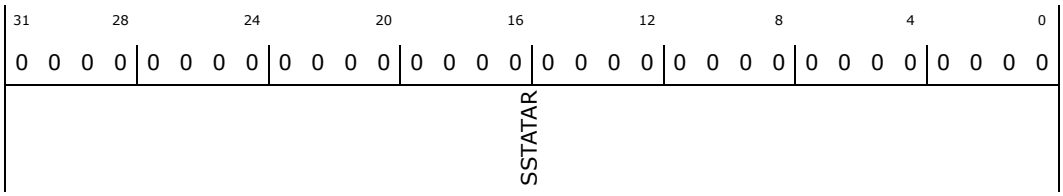
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 1E8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.1.74 reg_DSTATAR_type (DSTATAR5)—Offset 1F0h

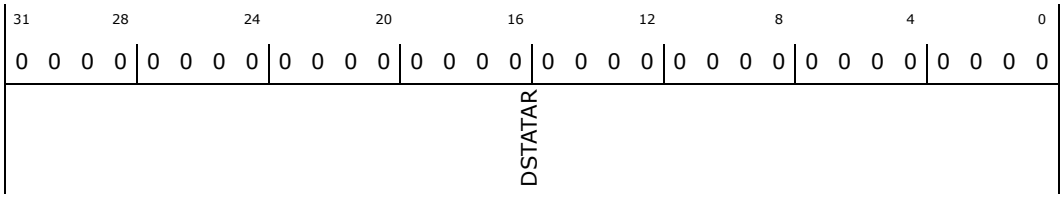
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 1F0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.1.75 reg_CFG_LO_type (CFG_LO5)—Offset 1F8h

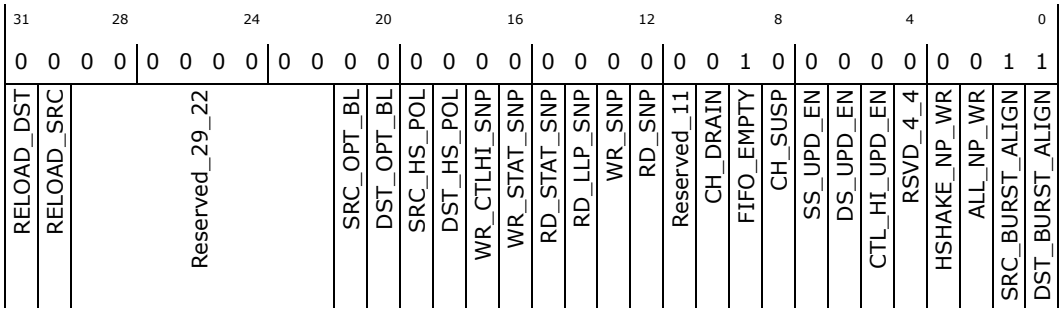
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

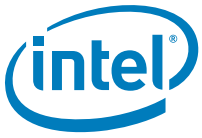
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 1F8h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values



Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.1.76 reg_CFG_HI_type (CFG_HI5)—Offset 1FCh

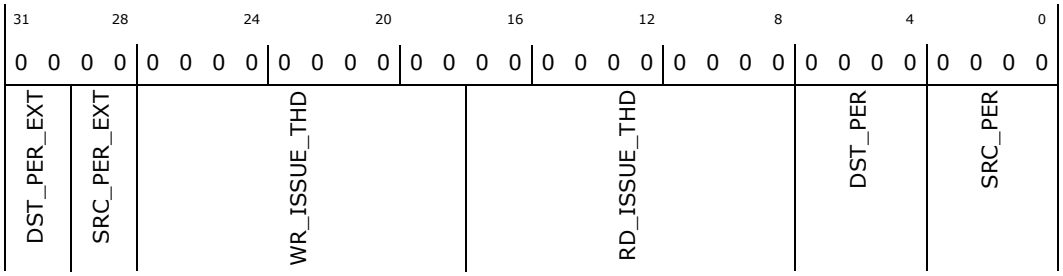
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 1FCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.1.77 reg_SGR_type (SGR5)—Offset 200h

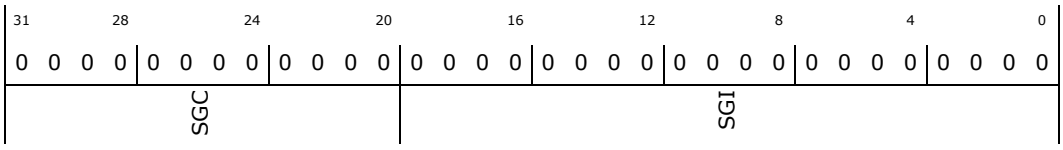
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 200h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.1.78 reg_DSR_type (DSR5)—Offset 208h

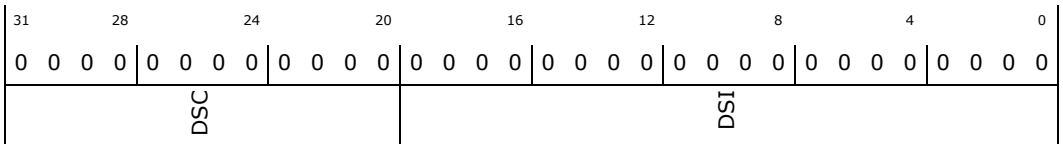
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 208h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.1.79 reg_SAR_type (SAR6)—Offset 210h

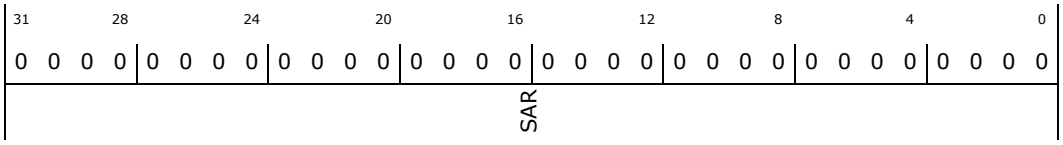
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 210h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.1.80 reg_DAR_type (DAR6)—Offset 218h

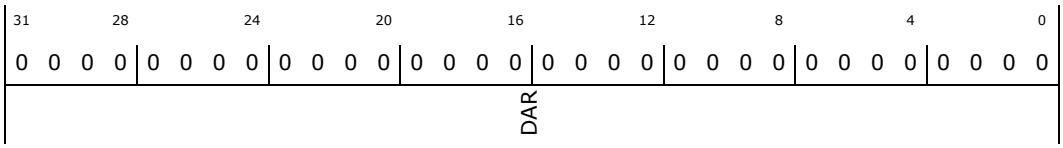
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 218h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.1.81 reg_LLP_type (LLP6)—Offset 220h

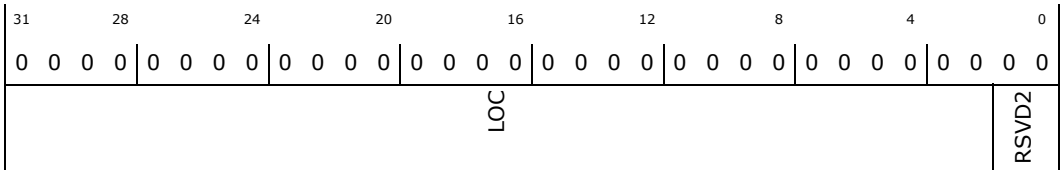
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 220h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.1.82 reg_CTL_LO_type (CTL_LO6)—Offset 228h

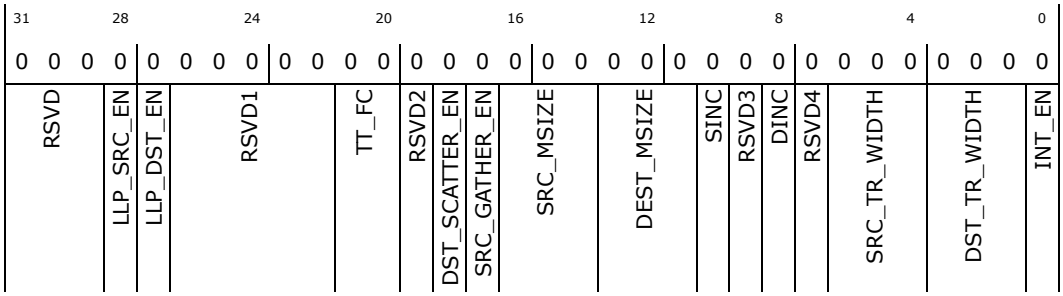
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 228h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.1.83 reg_CTL_HI_type (CTL_HI6)—Offset 22Ch

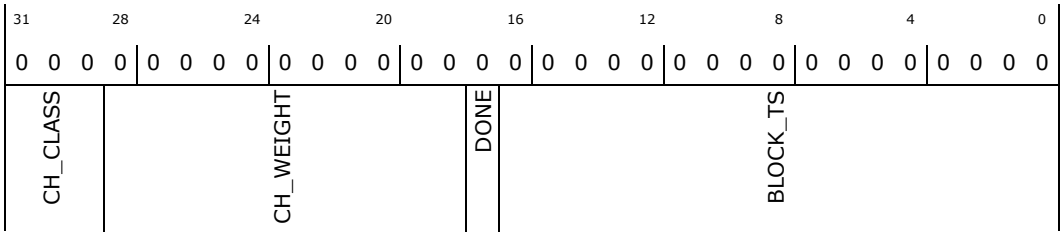
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 22Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesn't mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.1.84 reg_SSTAT_type (SSTAT6)—Offset 230h

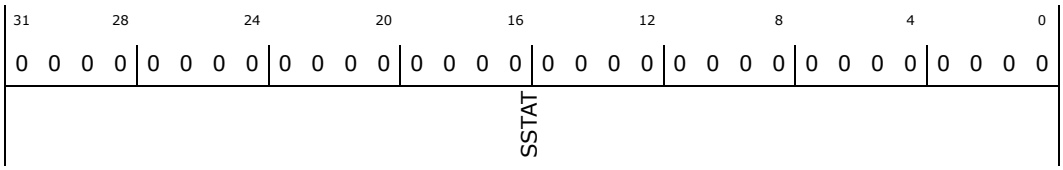
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 230h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.1.85 reg_DSTAT_type (DSTAT6)—Offset 238h

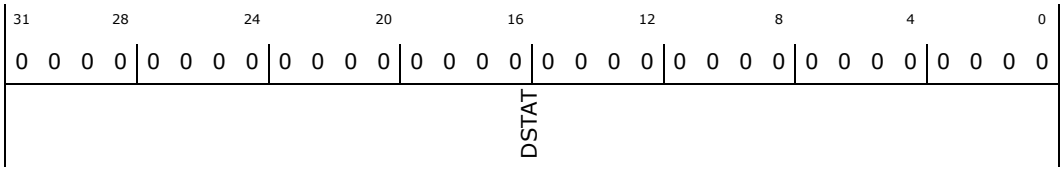
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 238h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.1.86 reg_SSTATAR_type (SSTATAR6)—Offset 240h

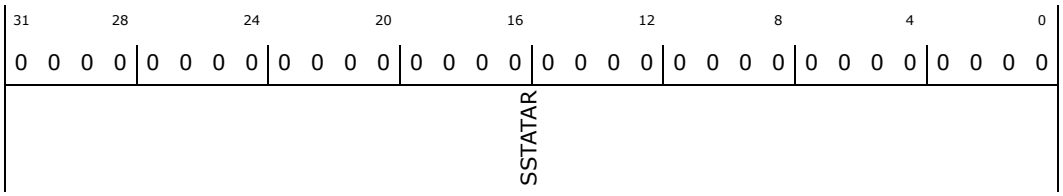
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 240h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.1.87 reg_DSTATAR_type (DSTATAR6)—Offset 248h

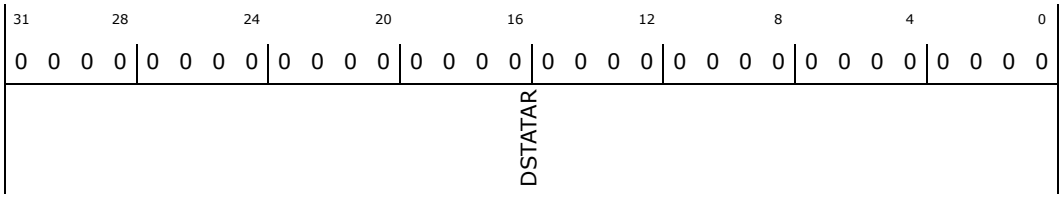
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 248h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.1.88 reg_CFG_LO_type (CFG_LO6)—Offset 250h

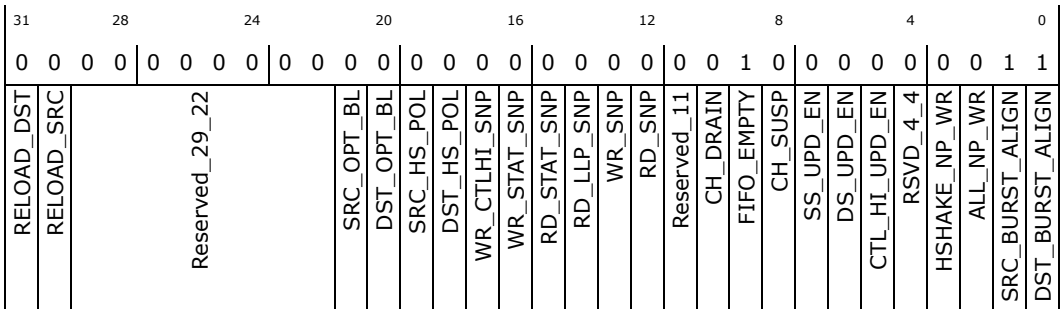
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 250h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.1.89 reg_CFG_HI_type (CFG_HI6)—Offset 254h

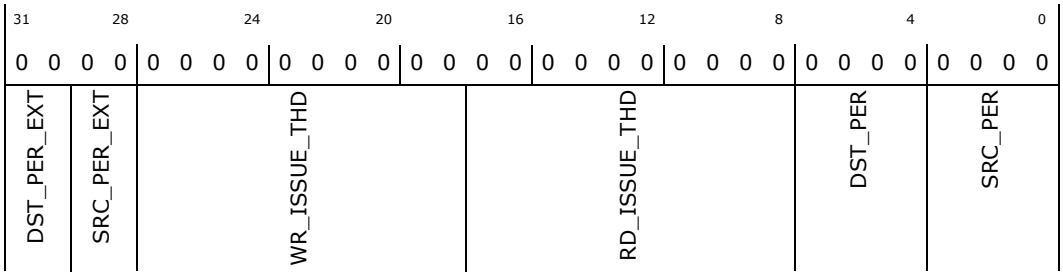
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 254h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.1.90 reg_SGR_type (SGR6)—Offset 258h

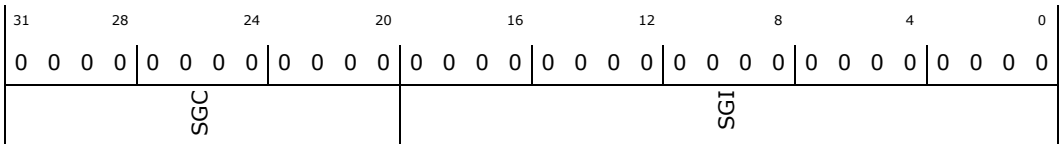
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 258h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.1.91 reg_DSR_type (DSR6)—Offset 260h

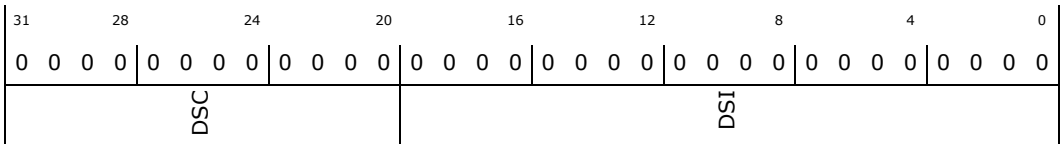
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 260h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.1.92 reg_SAR_type (SAR7)—Offset 268h

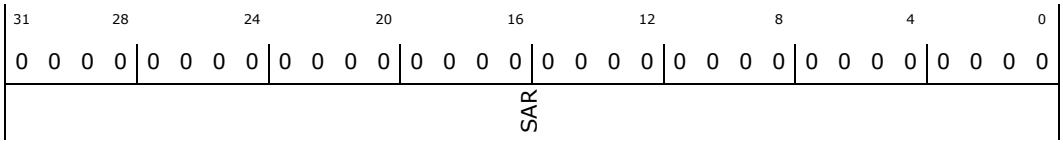
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 268h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.1.93 reg_DAR_type (DAR7)—Offset 270h

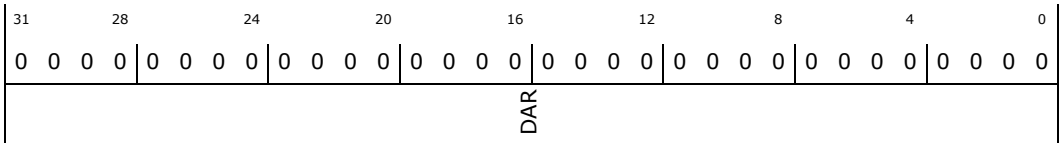
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

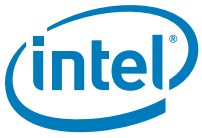
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 270h

Default: 00000000h





Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.1.94 reg_LLP_type (LLP7)—Offset 278h

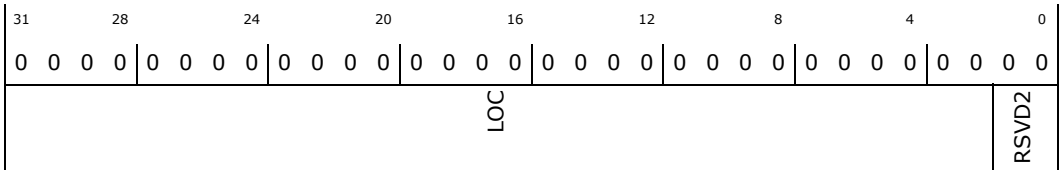
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 278h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.1.95 reg_CTL_LO_type (CTL_LO7)—Offset 280h

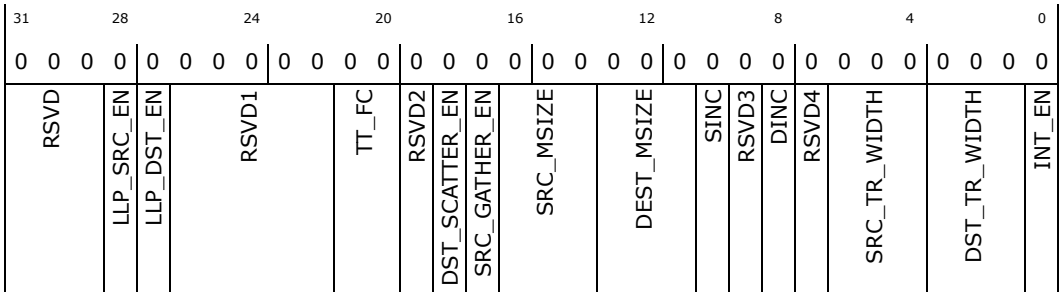
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 280h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.1.96 reg_CTL_HI_type (CTL_HI7)—Offset 284h

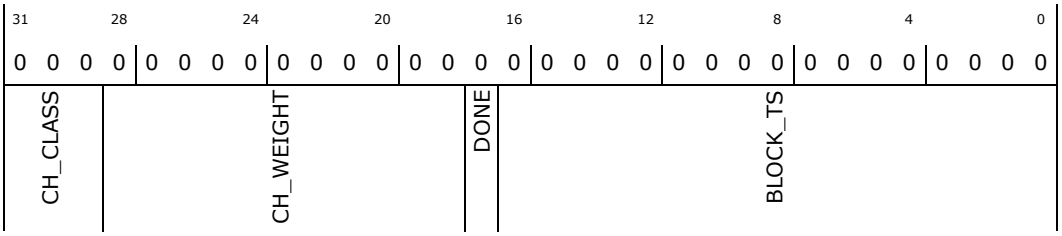
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

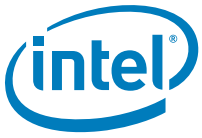
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 284h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below



Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesn't mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.1.97 reg_SSTAT_type (SSTAT7)—Offset 288h

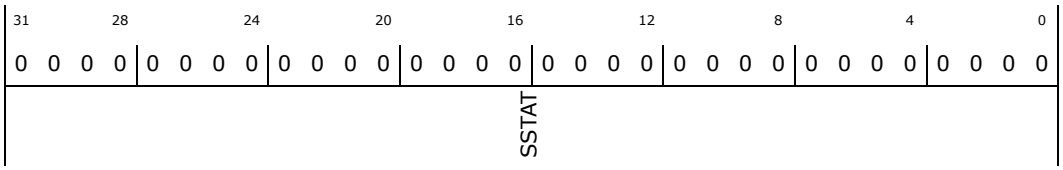
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 288h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.1.98 reg_DSTAT_type (DSTAT7)—Offset 290h

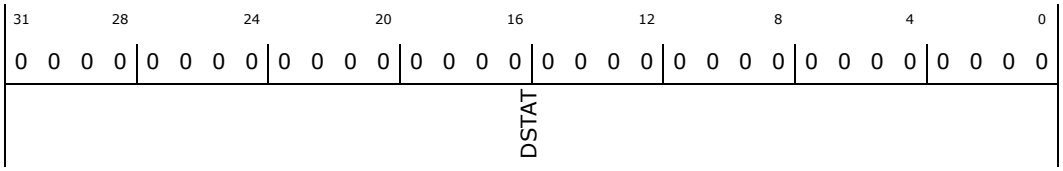
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 290h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.1.99 reg_SSTATAR_type (SSTATAR7)—Offset 298h

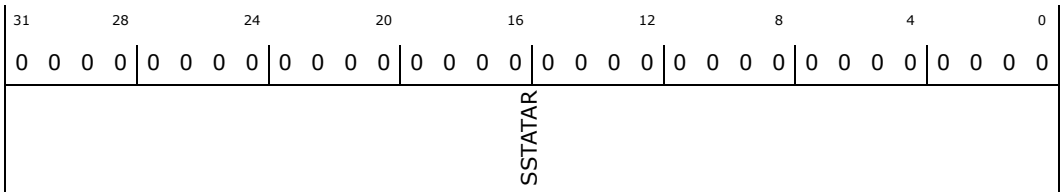
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 298h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.1.100 reg_DSTATAR_type (DSTATAR7)—Offset 2A0h

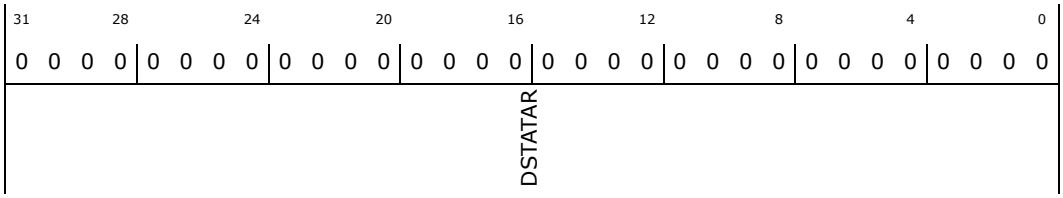
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 2A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.1.101 reg_CFG_LO_type (CFG_LO7)—Offset 2A8h

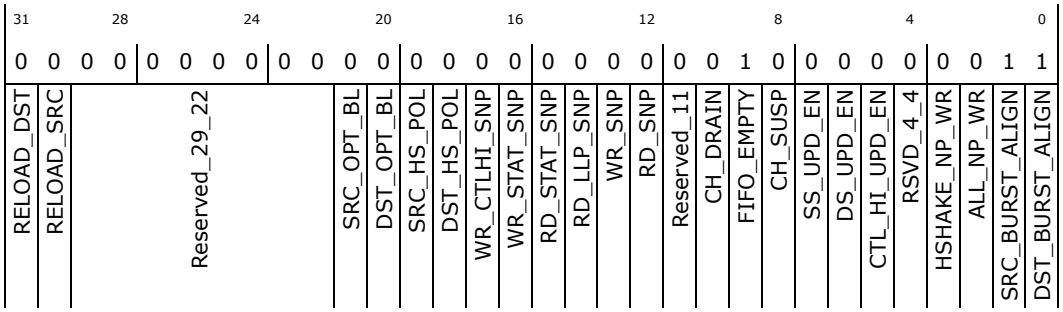
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 2A8h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.1.102 reg_CFG_HI_type (CFG_HI7)—Offset 2ACh

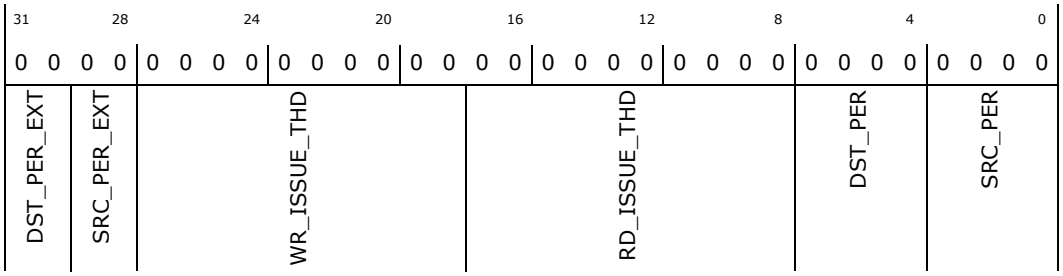
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

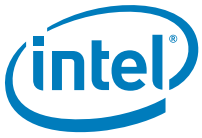
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 2ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.



Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.1.103 reg_SGR_type (SGR7)—Offset 2B0h

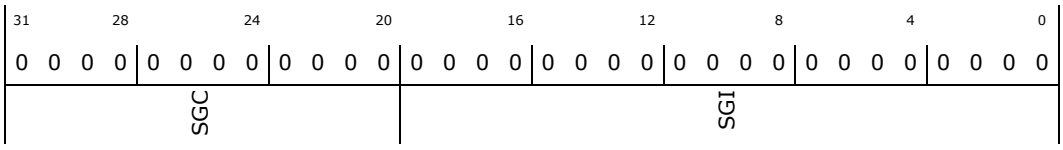
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 2B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.1.104 reg_DSR_type (DSR7)—Offset 2B8h

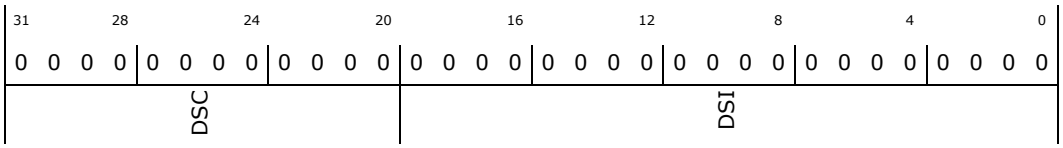
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 2B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.1.105 reg_Raw_type (RawTfr)—Offset 2C0h

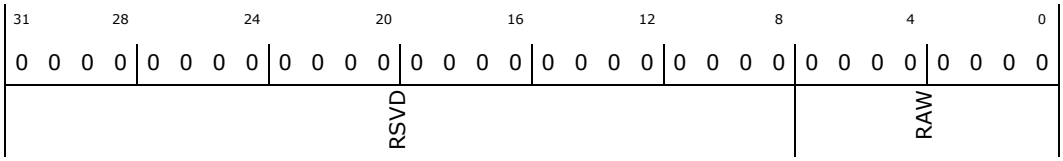
Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 2C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**RAW:** Raw interrupt status

8.1.106 reg_Raw_type (RawBlock)—Offset 2C8h

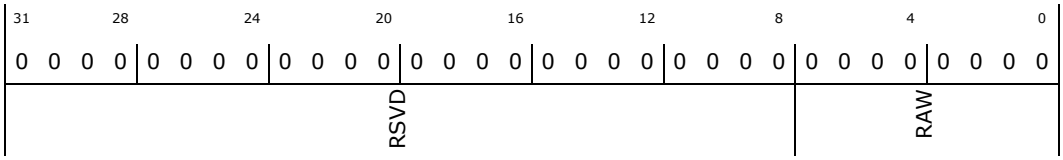
Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 2C8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**RAW:** Raw interrupt status

8.1.107 reg_Raw_type (RawSrcTran)—Offset 2D0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw

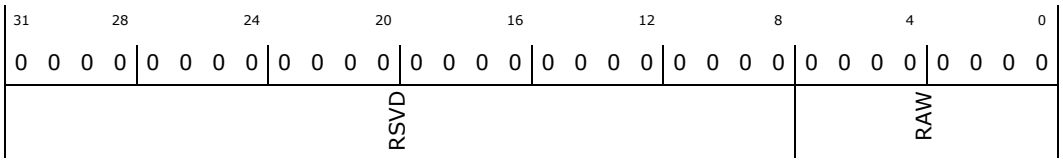
transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 2D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**RAW:** Raw interrupt status

8.1.108 reg_Raw_type (RawDstTran)—Offset 2D8h

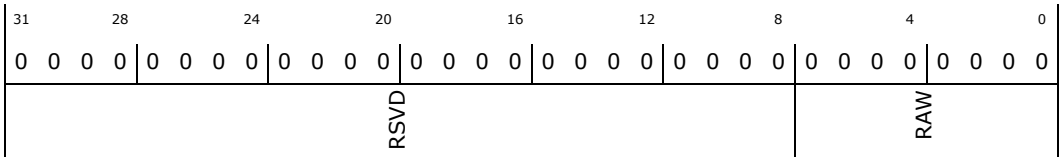
Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 2D8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**RAW:** Raw interrupt status

8.1.109 reg_Raw_type (RawErr)—Offset 2E0h

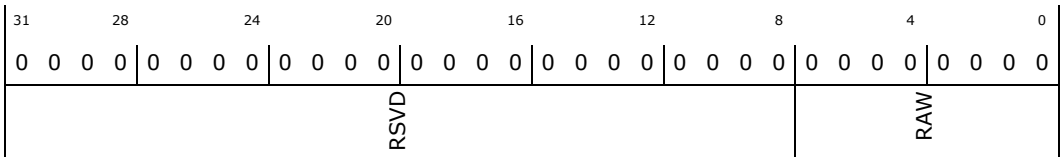
Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 2E0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**RAW:** Raw interrupt status

8.1.110 reg_Status_type (StatusTfr)—Offset 2E8h

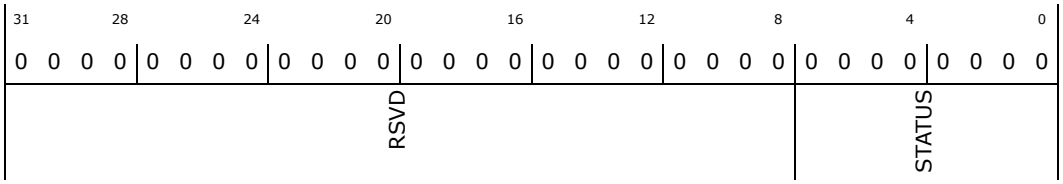
All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 2E8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**STATUS:** Interrupt status

8.1.111 reg_Status_type (StatusBlock)—Offset 2F0h

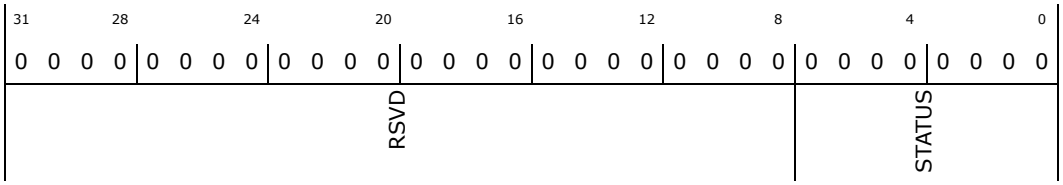
All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 2F0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**STATUS:** Interrupt status

8.1.112 reg_Status_type (StatusSrcTran)—Offset 2F8h

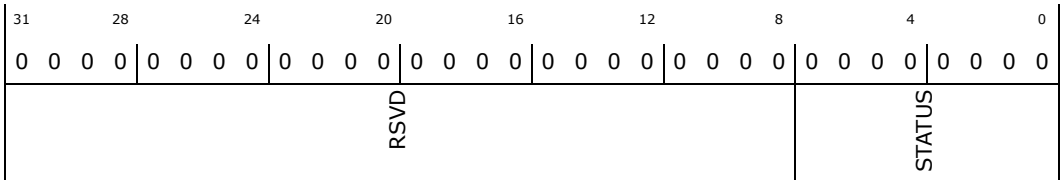
All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 98000h] + 2F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**STATUS:** Interrupt status

8.1.113 reg_Status_type (StatusDstTran)—Offset 300h

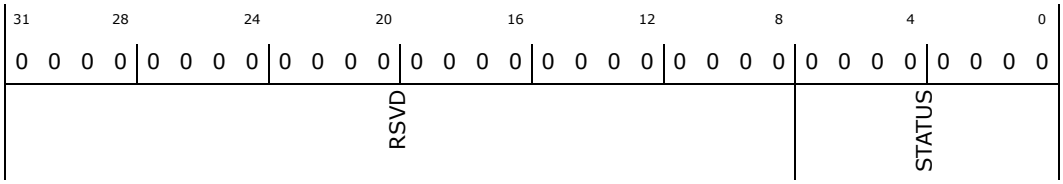
All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 98000h] + 300h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**STATUS:** Interrupt status

8.1.114 reg_Status_type (StatusErr)—Offset 308h

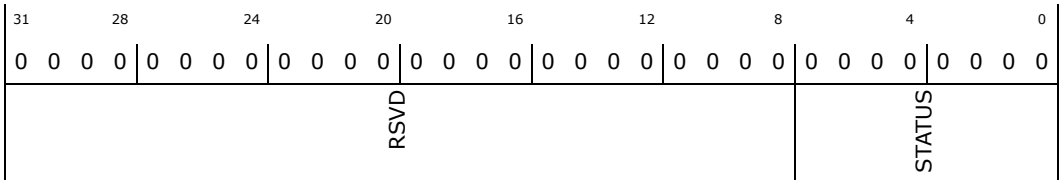
All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 308h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**STATUS:** Interrupt status

8.1.115 reg_Mask_type (MaskTfr)—Offset 310h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation.

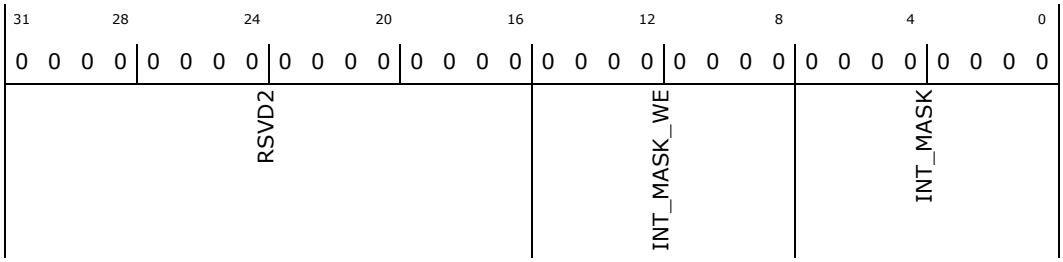
For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 310h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD2:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

8.1.116 reg_Mask_type (MaskBlock)—Offset 318h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged.

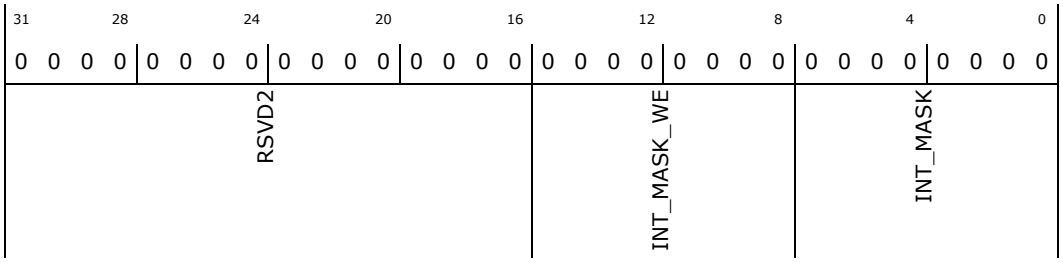
Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 318h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD2:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

8.1.117 reg_Mask_type (MaskSrcTran)—Offset 320h

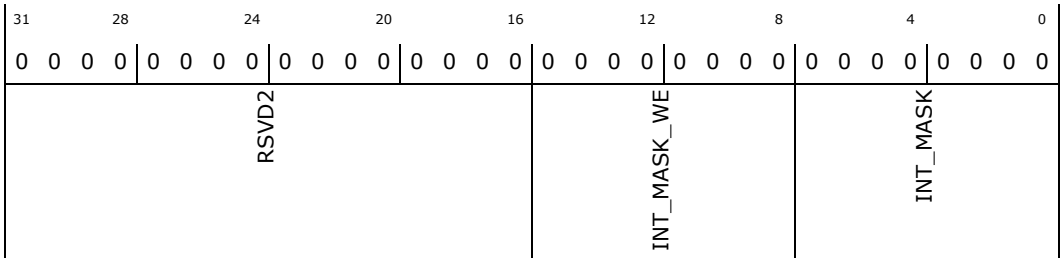
The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 320h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD2:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

8.1.118 reg_Mask_type (MaskDstTran)—Offset 328h

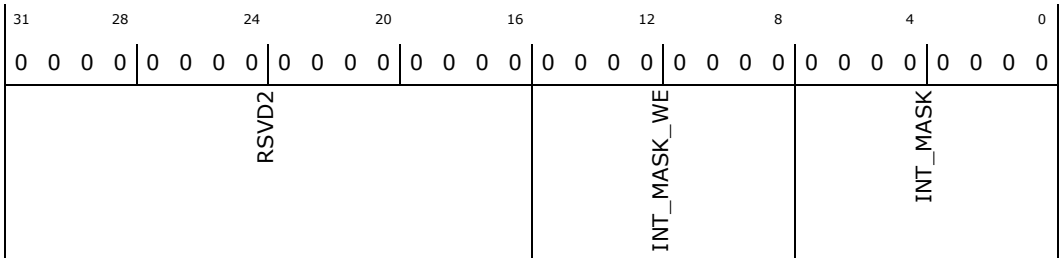
The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 328h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD2:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

8.1.119 reg_Mask_type (MaskErr)—Offset 330h

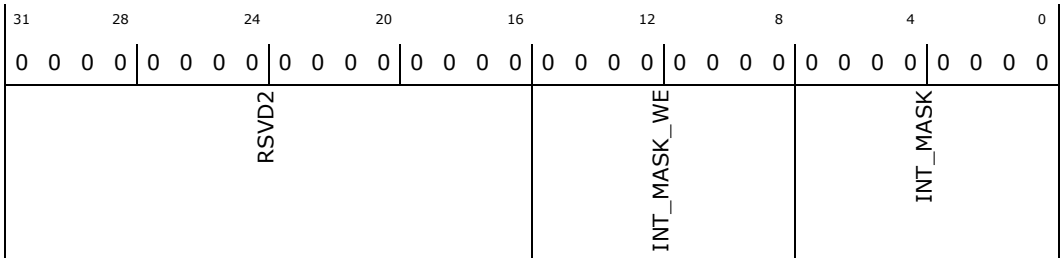
The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 330h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD2:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

8.1.120 reg_Clear_type (ClearTfr)—Offset 338h

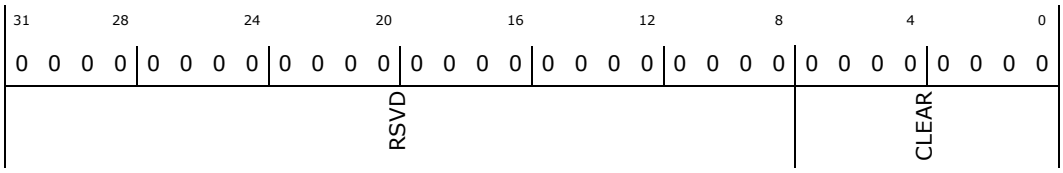
Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 338h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

8.1.121 reg_Clear_type (ClearBlock)—Offset 340h

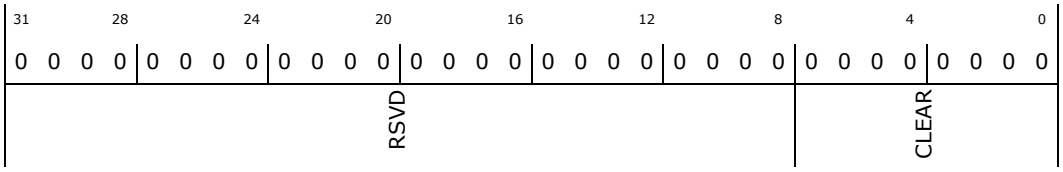
Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 340h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

8.1.122 reg_Clear_type (ClearSrcTran)—Offset 348h

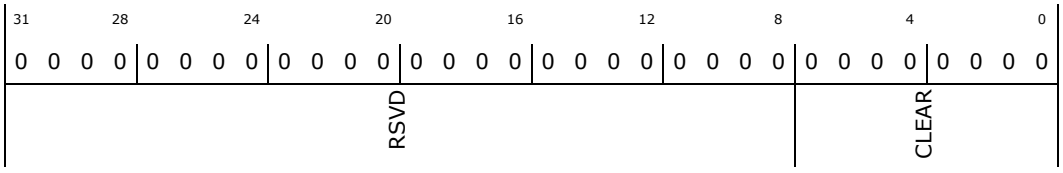
Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 348h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

8.1.123 reg_Clear_type (ClearDstTran)—Offset 350h

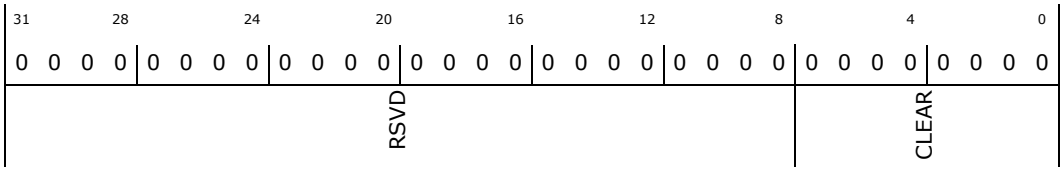
Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 98000h] + 350h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

8.1.124 reg_Clear_type (ClearErr)—Offset 358h

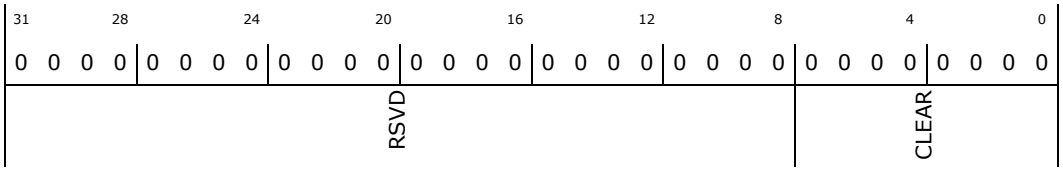
Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 98000h] + 358h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

8.1.125 reg_StatusInt_type (StatusInt)—Offset 360h

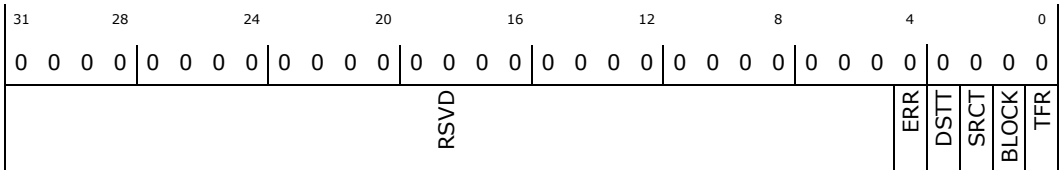
The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran,StatusErr is ORed to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 360h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RO	**RSVD:** Reserved
4	0x0 RO	**ERR:** OR of the contents of StatusErr register.
3	0x0 RO	**DSTT:** OR of the contents of StatusDst register.
2	0x0 RO	**SRCT:** OR of the contents of StatusSrcTran register
1	0x0 RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0x0 RO	**TFR:** OR of the contents of StatusTfr register.

8.1.126 reg_DmaCfgReg_type (DmaCfgReg)—Offset 398h

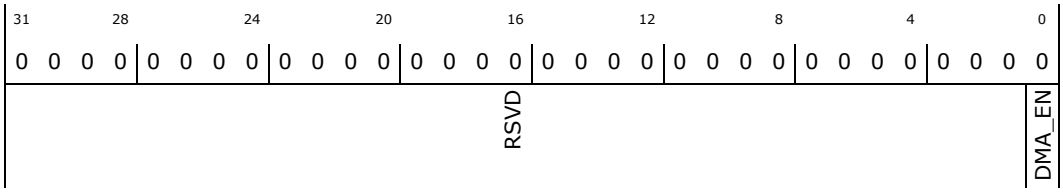
This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 398h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD:** Reserved
0	0x0 RW	**DMA_EN:** DMA Enable bit. 0 = DMA Disabled 1 = DMA Enabled

8.1.127 reg_ChEnReg_type (ChEnReg)—Offset 3A0h

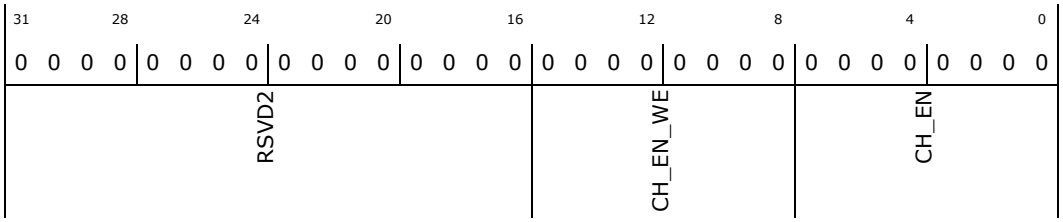
This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority. All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer. For example, writing hex 01x1 writes a 1 into ChEnReg(0), while ChEnReg(7:1) remains unchanged. Writing hex 00xx leaves ChEnReg(7:0) unchanged. Note that a read-modified write is not required.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 3A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD2:** Reserved
15:8	0x0 WO	**CH_EN_WE:** Channel enable write enable.
7:0	0x0 RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

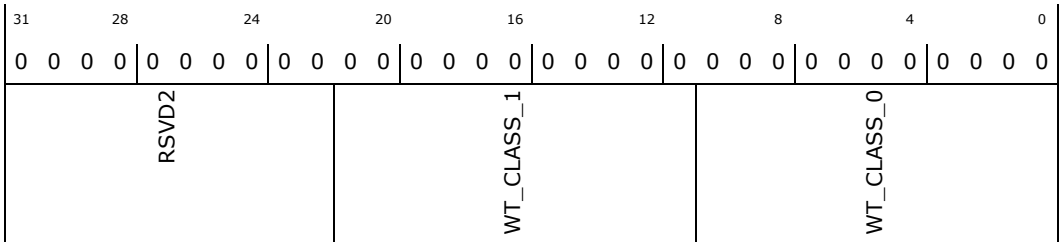
8.1.128 reg_CLASS_PRIORITY0_LO_type (ClassPriority0_LO)—Offset 3B8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 3B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**RSVD2:** Reserved
21:11	0x0 RW	**WT_CLASS_1:** Class Weight 1: Value of K assigns a weight of (K+1) to Class 1. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0x0 RW	**WT_CLASS_0:** Class Weight 0: Value of K assigns a weight of (K+1) to Class 0. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

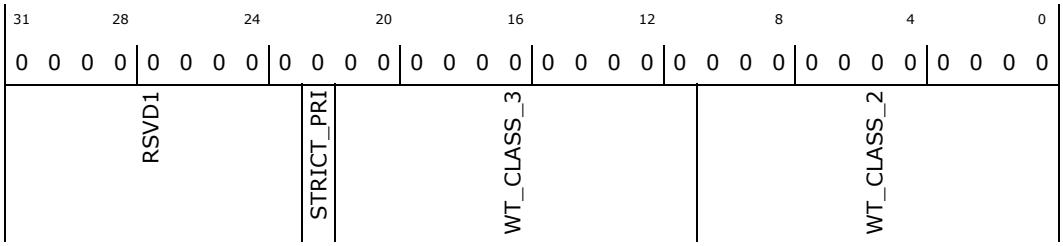
8.1.129 reg_CLASS_PRIORITY0_HI_type (ClassPriority0_HI)—Offset 3BCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 3BCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RSVD1:** Reserved
22	0x0 RW	**STRICT_PRI:** If set, Higher class values will always have higher priorities than lower class values. If not set, round-robin arbitration will be used between different classes using WT_CLASS_n values.
21:11	0x0 RW	**WT_CLASS_3:** Class Weight 3: Value of K assigns a weight of (K+1) to Class 3. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0x0 RW	**WT_CLASS_2:** Class Weight 2: Value of K assigns a weight of (K+1) to Class 2. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

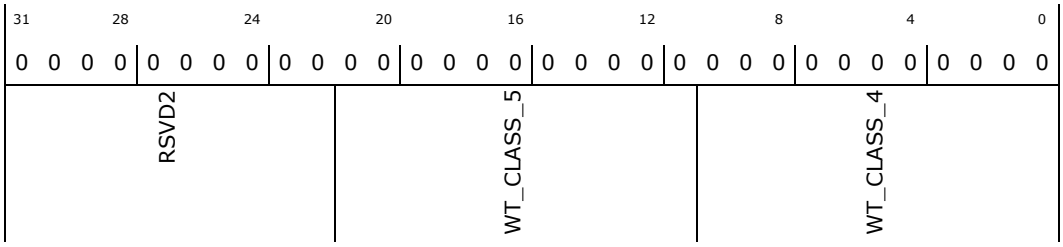
8.1.130 reg_CLASS_PRIORITY1_LO_type (ClassPriority1_LO)—Offset 3C0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 3C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**RSVD2:** Reserved
21:11	0x0 RW	**WT_CLASS_5:** Class Weight 5: Value of K assigns a weight of (K+1) to Class 5. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0x0 RW	**WT_CLASS_4:** Class Weight 4: Value of K assigns a weight of (K+1) to Class 4. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

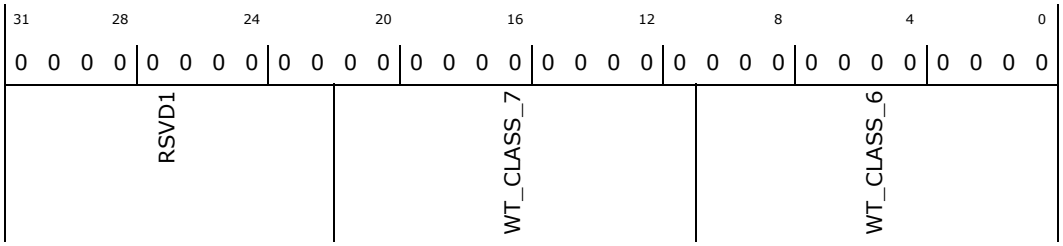
8.1.131 reg_CLASS_PRIORITY1_HI_type (ClassPriority1_HI)—Offset 3C4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 3C4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**RSVD1:** Reserved
21:11	0x0 RW	**WT_CLASS_7:** Class Weight 7: Value of K assigns a weight of (K+1) to Class 7. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0x0 RW	**WT_CLASS_6:** Class Weight 6: Value of K assigns a weight of (K+1) to Class 6. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

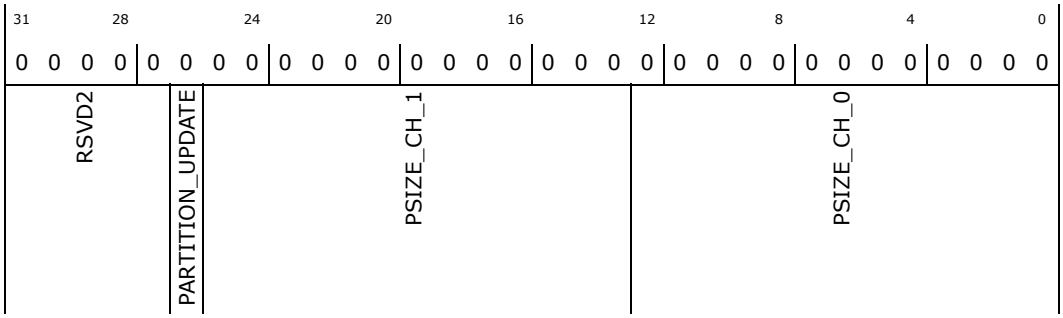
8.1.132 reg_FIFO_PARTITION0_LO_type (FifoPartition0_LO)—Offset 400h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 400h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RSVD2:** Reserved
26	0x0 RW	**PARTITION_UPDATE:** SW needs to write to this bit for the partitioning assignments to take effect.
25:13	0x0 RW	**PSIZE_CH_1:** Partition Byte Size assigned to Channel 1. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0x0 RW	**PSIZE_CH_0:** Partition Byte Size assigned to Channel 0. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

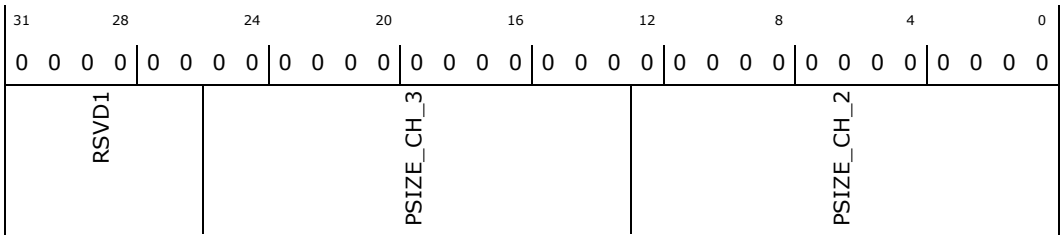
8.1.133 reg_FIFO_PARTITION0_HI_type (FifoPartition0_HI)—Offset 404h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 404h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD1:** Reserved
25:13	0x0 RW	**PSIZE_CH_3:** Partition Byte Size assigned to Channel 3. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

Bit Range	Default & Access	Field Name (ID): Description
12:0	0x0 RW	**PSIZE_CH_2:** Partition Byte Size assigned to Channel 2. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

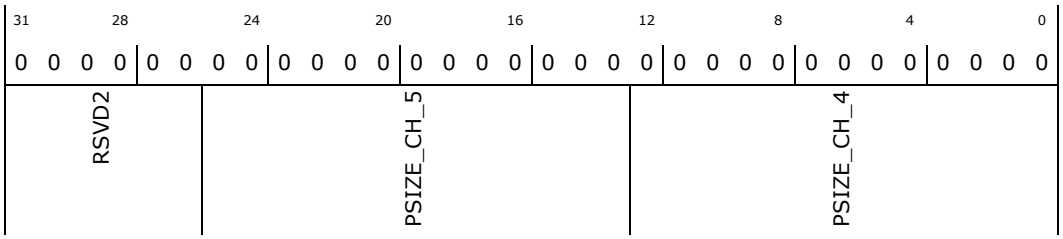
8.1.134 reg_FIFO_PARTITION1_LO_type (FifoPartition1_LO)—Offset 408h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 408h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD2:** Reserved
25:13	0x0 RW	**PSIZE_CH_5:** Partition Byte Size assigned to Channel 5. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0x0 RW	**PSIZE_CH_4:** Partition Byte Size assigned to Channel 4. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

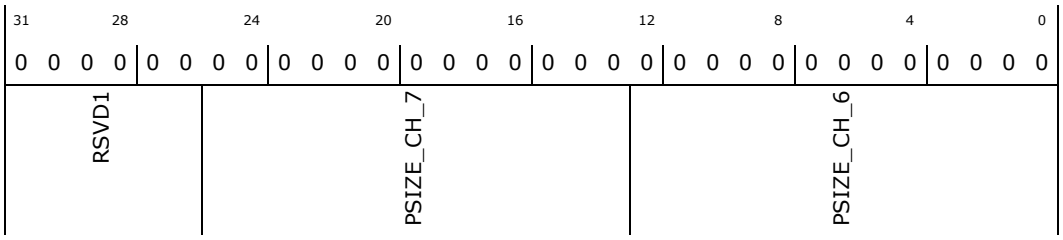
8.1.135 reg_FIFO_PARTITION1_HI_type (FifoPartition1_HI)—Offset 40Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 40Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD1:** Reserved
25:13	0x0 RW	**PSIZE_CH_7:** Partition Byte Size assigned to Channel 7. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0x0 RW	**PSIZE_CH_6:** Partition Byte Size assigned to Channel 6. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

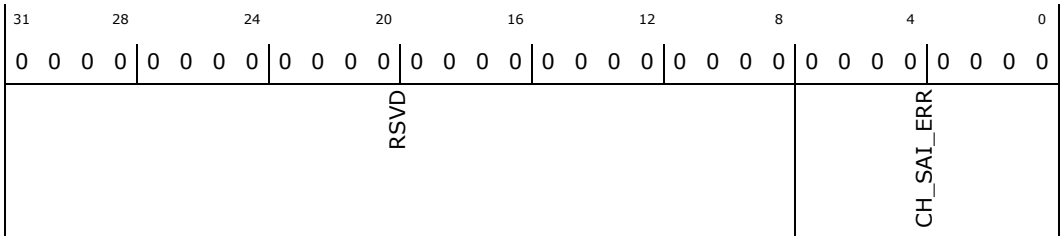
8.1.136 reg_SAI_Error_type (SAI_ERR)—Offset 410h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 410h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**CH_SAI_ERR:** 1: SAI Error occurred on Ch [n] 0: No SAI Error occurred on Ch [n] SAI_ERROR[n] is set by HW on SAI violation for channel [n]. All bits get cleared by SW when reading this register

8.1.137 reg_GLOBAL_CFG_type (GLOBAL_CFG)—Offset 418h

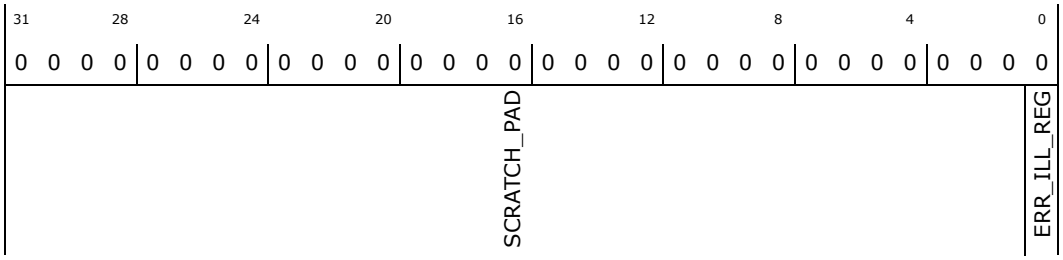
GLOBAL_CFG: GLOBAL DMA Configuration Register

Access Method

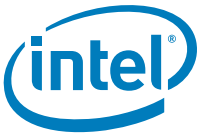
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 98000h] + 418h

Default: 00000000h



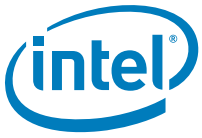
Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**SCRATCH_PAD:** This field will have all bits with R/W attribute to be used for future configuration and de-feature bits.
0	0x0 RW	**ERR_ILL_REG:** 0x1 : Issue ERR response on reading illegal (non-existing) registers 0x0 : Issue DVA response on reading illegal (non-existing) registers



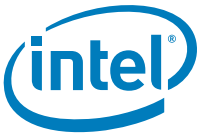
8.2 LPE DMA 1 Memory Mapped I/O Registers

Table 53. Summary of DMA 1 Memory Mapped I/O Registers—lpe_bridge.BAR

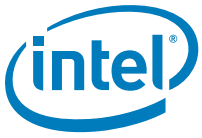
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"reg_SAR_type (SAR0)—Offset 0h" on page 3454	00000000h
8–Bh	4	"reg_DAR_type (DAR0)—Offset 8h" on page 3455	00000000h
10–13h	4	"reg_LLP_type (LLP0)—Offset 10h" on page 3456	00000000h
18–1Bh	4	"reg_CTL_LO_type (CTL_LO0)—Offset 18h" on page 3456	00000000h
1C–1Fh	4	"reg_CTL_HI_type (CTL_HI0)—Offset 1Ch" on page 3458	00000000h
20–23h	4	"reg_SSTAT_type (SSTAT0)—Offset 20h" on page 3460	00000000h
28–2Bh	4	"reg_DSTAT_type (DSTAT0)—Offset 28h" on page 3460	00000000h
30–33h	4	"reg_SSTATAR_type (SSTATAR0)—Offset 30h" on page 3461	00000000h
38–3Bh	4	"reg_DSTATAR_type (DSTATAR0)—Offset 38h" on page 3461	00000000h
40–43h	4	"reg_CFG_LO_type (CFG_LO0)—Offset 40h" on page 3462	00000203h
44–47h	4	"reg_CFG_HI_type (CFG_HI0)—Offset 44h" on page 3464	00000000h
48–4Bh	4	"reg_SGR_type (SGR0)—Offset 48h" on page 3465	00000000h
50–53h	4	"reg_DSR_type (DSR0)—Offset 50h" on page 3466	00000000h
58–5Bh	4	"reg_SAR_type (SAR1)—Offset 58h" on page 3466	00000000h
60–63h	4	"reg_DAR_type (DAR1)—Offset 60h" on page 3467	00000000h
68–6Bh	4	"reg_LLP_type (LLP1)—Offset 68h" on page 3468	00000000h
70–73h	4	"reg_CTL_LO_type (CTL_LO1)—Offset 70h" on page 3469	00000000h
74–77h	4	"reg_CTL_HI_type (CTL_HI1)—Offset 74h" on page 3471	00000000h
78–7Bh	4	"reg_SSTAT_type (SSTAT1)—Offset 78h" on page 3472	00000000h
80–83h	4	"reg_DSTAT_type (DSTAT1)—Offset 80h" on page 3473	00000000h
88–8Bh	4	"reg_SSTATAR_type (SSTATAR1)—Offset 88h" on page 3474	00000000h
90–93h	4	"reg_DSTATAR_type (DSTATAR1)—Offset 90h" on page 3474	00000000h
98–9Bh	4	"reg_CFG_LO_type (CFG_LO1)—Offset 98h" on page 3475	00000203h
9C–9Fh	4	"reg_CFG_HI_type (CFG_HI1)—Offset 9Ch" on page 3477	00000000h
A0–A3h	4	"reg_SGR_type (SGR1)—Offset A0h" on page 3478	00000000h
A8–ABh	4	"reg_DSR_type (DSR1)—Offset A8h" on page 3479	00000000h
B0–B3h	4	"reg_SAR_type (SAR2)—Offset B0h" on page 3479	00000000h
B8–BBh	4	"reg_DAR_type (DAR2)—Offset B8h" on page 3480	00000000h
C0–C3h	4	"reg_LLP_type (LLP2)—Offset C0h" on page 3481	00000000h
C8–CBh	4	"reg_CTL_LO_type (CTL_LO2)—Offset C8h" on page 3482	00000000h
CC–CFh	4	"reg_CTL_HI_type (CTL_HI2)—Offset CCh" on page 3484	00000000h
D0–D3h	4	"reg_SSTAT_type (SSTAT2)—Offset D0h" on page 3485	00000000h
D8–DBh	4	"reg_DSTAT_type (DSTAT2)—Offset D8h" on page 3486	00000000h
E0–E3h	4	"reg_SSTATAR_type (SSTATAR2)—Offset E0h" on page 3487	00000000h



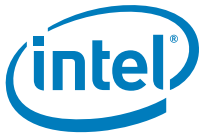
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
E8–EBh	4	"reg_DSTATAR_type (DSTATAR2)—Offset E8h" on page 3487	00000000h
F0–F3h	4	"reg_CFG_LO_type (CFG_LO2)—Offset F0h" on page 3488	00000203h
F4–F7h	4	"reg_CFG_HI_type (CFG_HI2)—Offset F4h" on page 3490	00000000h
F8–FBh	4	"reg_SGR_type (SGR2)—Offset F8h" on page 3491	00000000h
100–103h	4	"reg_DSR_type (DSR2)—Offset 100h" on page 3492	00000000h
108–10Bh	4	"reg_SAR_type (SAR3)—Offset 108h" on page 3492	00000000h
110–113h	4	"reg_DAR_type (DAR3)—Offset 110h" on page 3493	00000000h
118–11Bh	4	"reg_LLP_type (LLP3)—Offset 118h" on page 3494	00000000h
120–123h	4	"reg_CTL_LO_type (CTL_LO3)—Offset 120h" on page 3495	00000000h
124–127h	4	"reg_CTL_HI_type (CTL_HI3)—Offset 124h" on page 3497	00000000h
128–12Bh	4	"reg_SSTAT_type (SSTAT3)—Offset 128h" on page 3498	00000000h
130–133h	4	"reg_DSTAT_type (DSTAT3)—Offset 130h" on page 3499	00000000h
138–13Bh	4	"reg_SSTATAR_type (SSTATAR3)—Offset 138h" on page 3500	00000000h
140–143h	4	"reg_DSTATAR_type (DSTATAR3)—Offset 140h" on page 3500	00000000h
148–14Bh	4	"reg_CFG_LO_type (CFG_LO3)—Offset 148h" on page 3501	00000203h
14C–14Fh	4	"reg_CFG_HI_type (CFG_HI3)—Offset 14Ch" on page 3503	00000000h
150–153h	4	"reg_SGR_type (SGR3)—Offset 150h" on page 3504	00000000h
158–15Bh	4	"reg_DSR_type (DSR3)—Offset 158h" on page 3505	00000000h
160–163h	4	"reg_SAR_type (SAR4)—Offset 160h" on page 3505	00000000h
168–16Bh	4	"reg_DAR_type (DAR4)—Offset 168h" on page 3506	00000000h
170–173h	4	"reg_LLP_type (LLP4)—Offset 170h" on page 3507	00000000h
178–17Bh	4	"reg_CTL_LO_type (CTL_LO4)—Offset 178h" on page 3508	00000000h
17C–17Fh	4	"reg_CTL_HI_type (CTL_HI4)—Offset 17Ch" on page 3510	00000000h
180–183h	4	"reg_SSTAT_type (SSTAT4)—Offset 180h" on page 3511	00000000h
188–18Bh	4	"reg_DSTAT_type (DSTAT4)—Offset 188h" on page 3512	00000000h
190–193h	4	"reg_SSTATAR_type (SSTATAR4)—Offset 190h" on page 3513	00000000h
198–19Bh	4	"reg_DSTATAR_type (DSTATAR4)—Offset 198h" on page 3513	00000000h
1A0–1A3h	4	"reg_CFG_LO_type (CFG_LO4)—Offset 1A0h" on page 3514	00000203h
1A4–1A7h	4	"reg_CFG_HI_type (CFG_HI4)—Offset 1A4h" on page 3516	00000000h
1A8–1ABh	4	"reg_SGR_type (SGR4)—Offset 1A8h" on page 3517	00000000h
1B0–1B3h	4	"reg_DSR_type (DSR4)—Offset 1B0h" on page 3518	00000000h
1B8–1BBh	4	"reg_SAR_type (SAR5)—Offset 1B8h" on page 3518	00000000h
1C0–1C3h	4	"reg_DAR_type (DAR5)—Offset 1C0h" on page 3519	00000000h
1C8–1CBh	4	"reg_LLP_type (LLP5)—Offset 1C8h" on page 3520	00000000h
1D0–1D3h	4	"reg_CTL_LO_type (CTL_LO5)—Offset 1D0h" on page 3521	00000000h
1D4–1D7h	4	"reg_CTL_HI_type (CTL_HI5)—Offset 1D4h" on page 3523	00000000h
1D8–1DBh	4	"reg_SSTAT_type (SSTAT5)—Offset 1D8h" on page 3524	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1E0–1E3h	4	"reg_DSTAT_type (DSTAT5)—Offset 1E0h" on page 3525	00000000h
1E8–1EBh	4	"reg_SSTATAR_type (SSTATAR5)—Offset 1E8h" on page 3526	00000000h
1F0–1F3h	4	"reg_DSTATAR_type (DSTATAR5)—Offset 1F0h" on page 3526	00000000h
1F8–1FBh	4	"reg_CFG_LO_type (CFG_LO5)—Offset 1F8h" on page 3527	00000203h
1FC–1FFh	4	"reg_CFG_HI_type (CFG_HI5)—Offset 1FCh" on page 3529	00000000h
200–203h	4	"reg_SGR_type (SGR5)—Offset 200h" on page 3530	00000000h
208–20Bh	4	"reg_DSR_type (DSR5)—Offset 208h" on page 3531	00000000h
210–213h	4	"reg_SAR_type (SAR6)—Offset 210h" on page 3531	00000000h
218–21Bh	4	"reg_DAR_type (DAR6)—Offset 218h" on page 3532	00000000h
220–223h	4	"reg_LLP_type (LLP6)—Offset 220h" on page 3533	00000000h
228–22Bh	4	"reg_CTL_LO_type (CTL_LO6)—Offset 228h" on page 3534	00000000h
22C–22Fh	4	"reg_CTL_HI_type (CTL_HI6)—Offset 22Ch" on page 3536	00000000h
230–233h	4	"reg_SSTAT_type (SSTAT6)—Offset 230h" on page 3537	00000000h
238–23Bh	4	"reg_DSTAT_type (DSTAT6)—Offset 238h" on page 3538	00000000h
240–243h	4	"reg_SSTATAR_type (SSTATAR6)—Offset 240h" on page 3539	00000000h
248–24Bh	4	"reg_DSTATAR_type (DSTATAR6)—Offset 248h" on page 3539	00000000h
250–253h	4	"reg_CFG_LO_type (CFG_LO6)—Offset 250h" on page 3540	00000203h
254–257h	4	"reg_CFG_HI_type (CFG_HI6)—Offset 254h" on page 3542	00000000h
258–25Bh	4	"reg_SGR_type (SGR6)—Offset 258h" on page 3543	00000000h
260–263h	4	"reg_DSR_type (DSR6)—Offset 260h" on page 3544	00000000h
268–26Bh	4	"reg_SAR_type (SAR7)—Offset 268h" on page 3544	00000000h
270–273h	4	"reg_DAR_type (DAR7)—Offset 270h" on page 3545	00000000h
278–27Bh	4	"reg_LLP_type (LLP7)—Offset 278h" on page 3546	00000000h
280–283h	4	"reg_CTL_LO_type (CTL_LO7)—Offset 280h" on page 3547	00000000h
284–287h	4	"reg_CTL_HI_type (CTL_HI7)—Offset 284h" on page 3549	00000000h
288–28Bh	4	"reg_SSTAT_type (SSTAT7)—Offset 288h" on page 3550	00000000h
290–293h	4	"reg_DSTAT_type (DSTAT7)—Offset 290h" on page 3551	00000000h
298–29Bh	4	"reg_SSTATAR_type (SSTATAR7)—Offset 298h" on page 3552	00000000h
2A0–2A3h	4	"reg_DSTATAR_type (DSTATAR7)—Offset 2A0h" on page 3552	00000000h
2A8–2ABh	4	"reg_CFG_LO_type (CFG_LO7)—Offset 2A8h" on page 3553	00000203h
2AC–2AFh	4	"reg_CFG_HI_type (CFG_HI7)—Offset 2ACh" on page 3555	00000000h
2B0–2B3h	4	"reg_SGR_type (SGR7)—Offset 2B0h" on page 3556	00000000h
2B8–2BBh	4	"reg_DSR_type (DSR7)—Offset 2B8h" on page 3557	00000000h
2C0–2C3h	4	"reg_Raw_type (RawTfr)—Offset 2C0h" on page 3557	00000000h
2C8–2CBh	4	"reg_Raw_type (RawBlock)—Offset 2C8h" on page 3558	00000000h
2D0–2D3h	4	"reg_Raw_type (RawSrcTran)—Offset 2D0h" on page 3558	00000000h
2D8–2DBh	4	"reg_Raw_type (RawDstTran)—Offset 2D8h" on page 3559	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2E0–2E3h	4	"reg_Raw_type (RawErr)—Offset 2E0h" on page 3560	00000000h
2E8–2EBh	4	"reg_Status_type (StatusTfr)—Offset 2E8h" on page 3560	00000000h
2F0–2F3h	4	"reg_Status_type (StatusBlock)—Offset 2F0h" on page 3561	00000000h
2F8–2FBh	4	"reg_Status_type (StatusSrcTran)—Offset 2F8h" on page 3562	00000000h
300–303h	4	"reg_Status_type (StatusDstTran)—Offset 300h" on page 3562	00000000h
308–30Bh	4	"reg_Status_type (StatusErr)—Offset 308h" on page 3563	00000000h
310–313h	4	"reg_Mask_type (MaskTfr)—Offset 310h" on page 3563	00000000h
318–31Bh	4	"reg_Mask_type (MaskBlock)—Offset 318h" on page 3564	00000000h
320–323h	4	"reg_Mask_type (MaskSrcTran)—Offset 320h" on page 3565	00000000h
328–32Bh	4	"reg_Mask_type (MaskDstTran)—Offset 328h" on page 3566	00000000h
330–333h	4	"reg_Mask_type (MaskErr)—Offset 330h" on page 3567	00000000h
338–33Bh	4	"reg_Clear_type (ClearTfr)—Offset 338h" on page 3568	00000000h
340–343h	4	"reg_Clear_type (ClearBlock)—Offset 340h" on page 3569	00000000h
348–34Bh	4	"reg_Clear_type (ClearSrcTran)—Offset 348h" on page 3569	00000000h
350–353h	4	"reg_Clear_type (ClearDstTran)—Offset 350h" on page 3570	00000000h
358–35Bh	4	"reg_Clear_type (ClearErr)—Offset 358h" on page 3570	00000000h
360–363h	4	"reg_StatusInt_type (StatusInt)—Offset 360h" on page 3571	00000000h
398–39Bh	4	"reg_DmaCfgReg_type (DmaCfgReg)—Offset 398h" on page 3572	00000000h
3A0–3A3h	4	"reg_ChEnReg_type (ChEnReg)—Offset 3A0h" on page 3572	00000000h
3B8–3BBh	4	"reg_CLASS_PRIORITY0_LO_type (ClassPriority0_LO)—Offset 3B8h" on page 3573	00000000h
3BC–3BFh	4	"reg_CLASS_PRIORITY0_HI_type (ClassPriority0_HI)—Offset 3BCh" on page 3574	00000000h
3C0–3C3h	4	"reg_CLASS_PRIORITY1_LO_type (ClassPriority1_LO)—Offset 3C0h" on page 3574	00000000h
3C4–3C7h	4	"reg_CLASS_PRIORITY1_HI_type (ClassPriority1_HI)—Offset 3C4h" on page 3575	00000000h
400–403h	4	"reg_FIFO_PARTITION0_LO_type (FifoPartition0_LO)—Offset 400h" on page 3575	00000000h
404–407h	4	"reg_FIFO_PARTITION0_HI_type (FifoPartition0_HI)—Offset 404h" on page 3576	00000000h
408–40Bh	4	"reg_FIFO_PARTITION1_LO_type (FifoPartition1_LO)—Offset 408h" on page 3577	00000000h
40C–40Fh	4	"reg_FIFO_PARTITION1_HI_type (FifoPartition1_HI)—Offset 40Ch" on page 3577	00000000h
410–413h	4	"reg_SAI_Error_type (SAI_ERR)—Offset 410h" on page 3578	00000000h
418–41Bh	4	"reg_GLOBAL_CFG_type (GLOBAL_CFG)—Offset 418h" on page 3578	00000000h



8.2.1 reg_SAR_type (SAR0)—Offset 0h

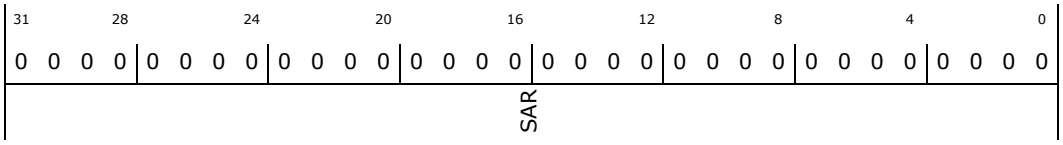
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.2 reg_DAR_type (DAR0)—Offset 8h

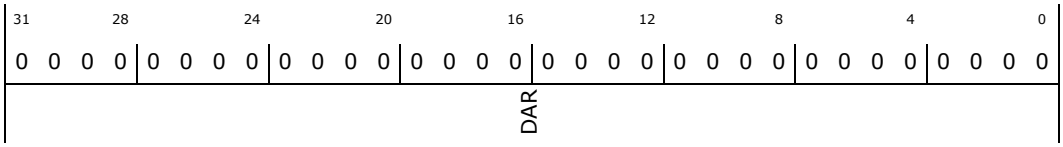
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.3 reg_LLP_type (LLP0)—Offset 10h

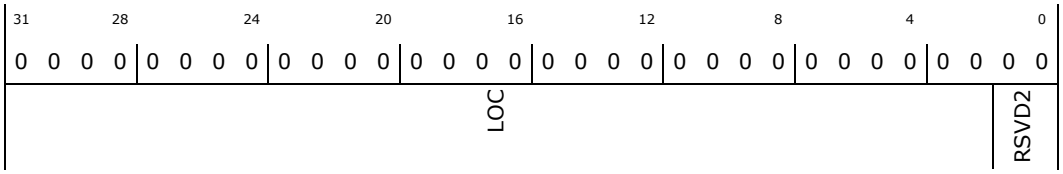
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.2.4 reg_CTL_LO_type (CTL_LO0)—Offset 18h

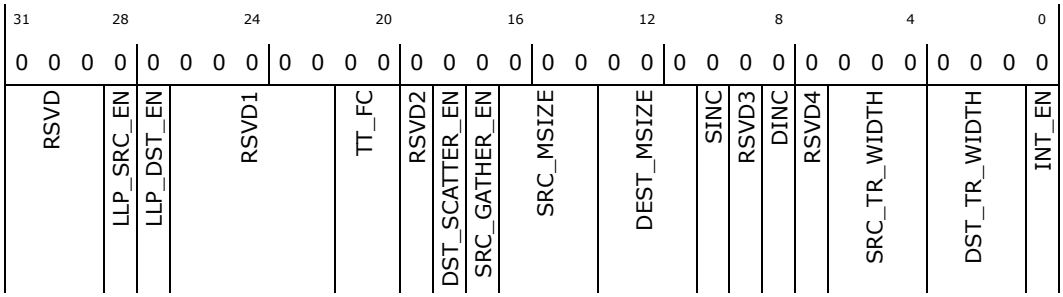
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 18h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.2.5 reg_CTL_HI_type (CTL_HI0)—Offset 1Ch

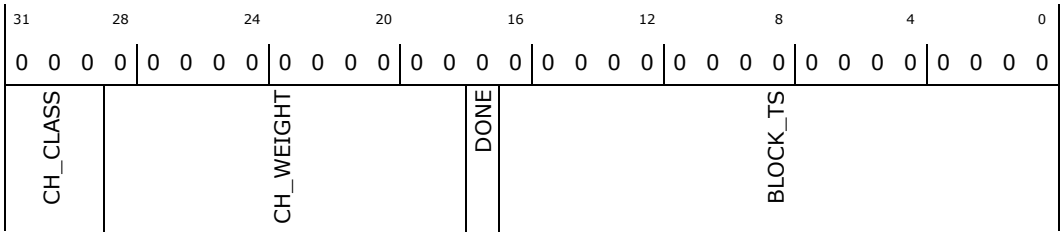
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 1Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.2.6 reg_SSTAT_type (SSTAT0)—Offset 20h

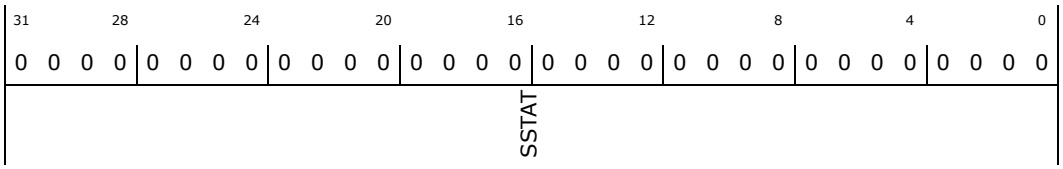
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 20h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.2.7 reg_DSTAT_type (DSTAT0)—Offset 28h

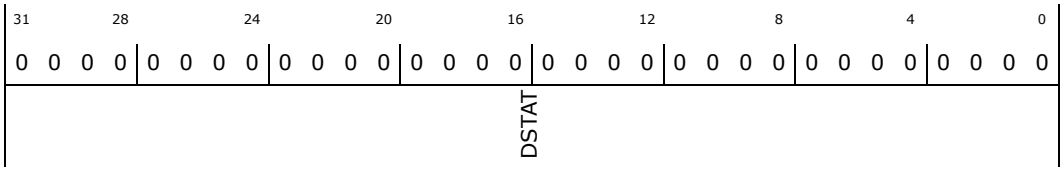
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 28h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.2.8 reg_SSTATAR_type (SSTATAR0)—Offset 30h

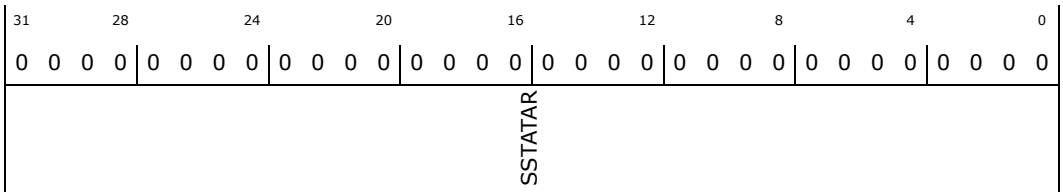
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.2.9 reg_DSTATAR_type (DSTATAR0)—Offset 38h

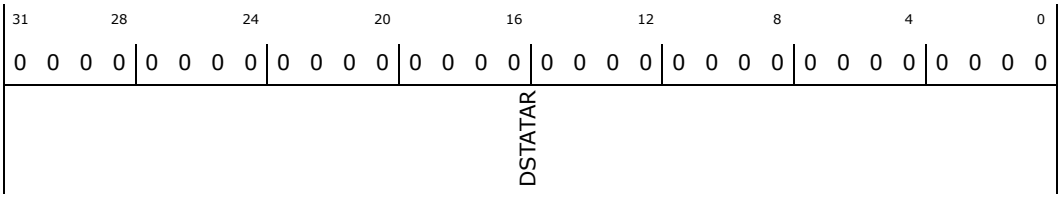
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 38h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.2.10 reg_CFG_LO_type (CFG_LO0)—Offset 40h

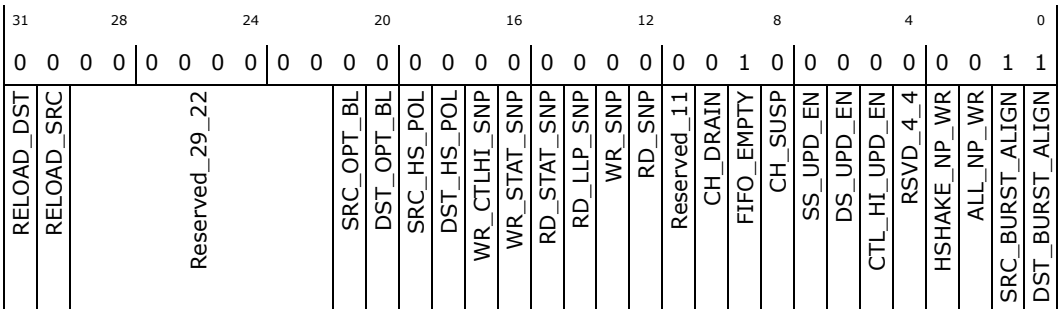
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 40h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled

Bit Range	Default & Access	Field Name (ID): Description
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.2.11 reg_CFG_HI_type (CFG_HI0)—Offset 44h

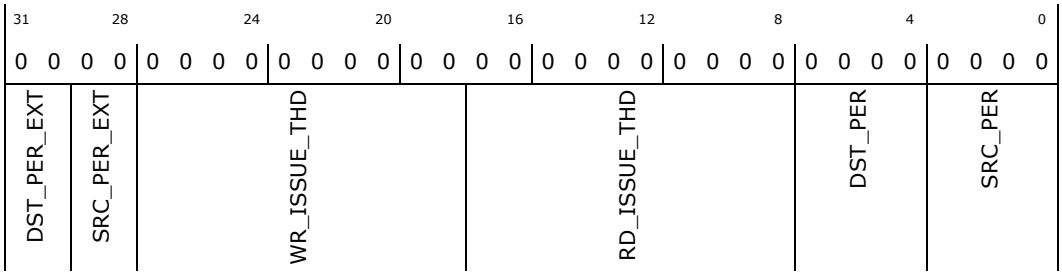
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 44h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.

Bit Range	Default & Access	Field Name (ID): Description
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.2.12 reg_SGR_type (SGR0)—Offset 48h

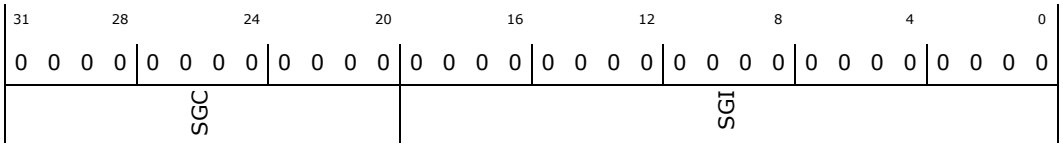
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 48h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.2.13 reg_DSR_type (DSR0)—Offset 50h

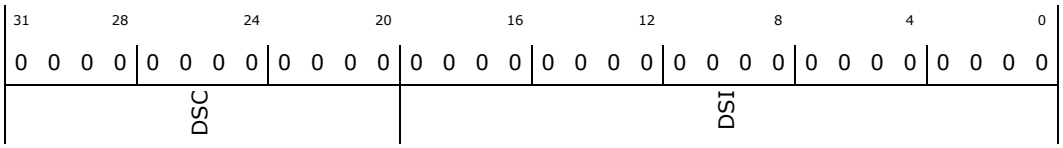
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 50h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.2.14 reg_SAR_type (SAR1)—Offset 58h

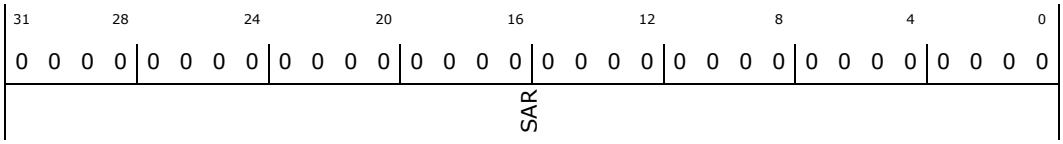
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 58h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.15 reg_DAR_type (DAR1)—Offset 60h

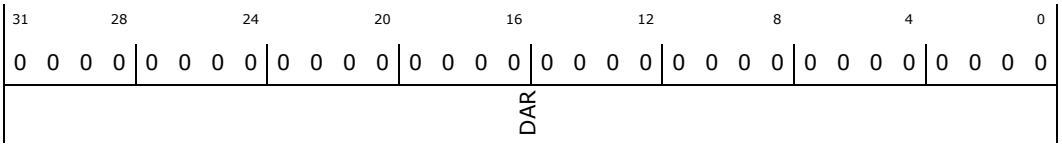
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 60h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.16 reg_LLP_type (LLP1)—Offset 68h

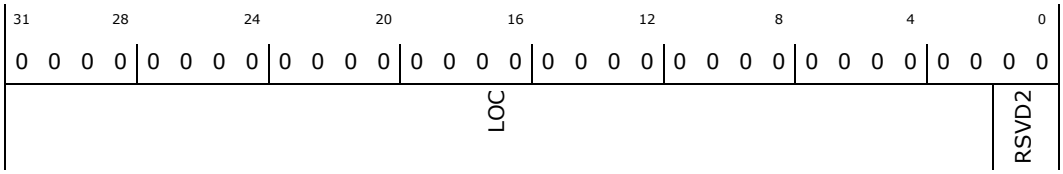
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 68h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.2.17 reg_CTL_LO_type (CTL_LO1)—Offset 70h

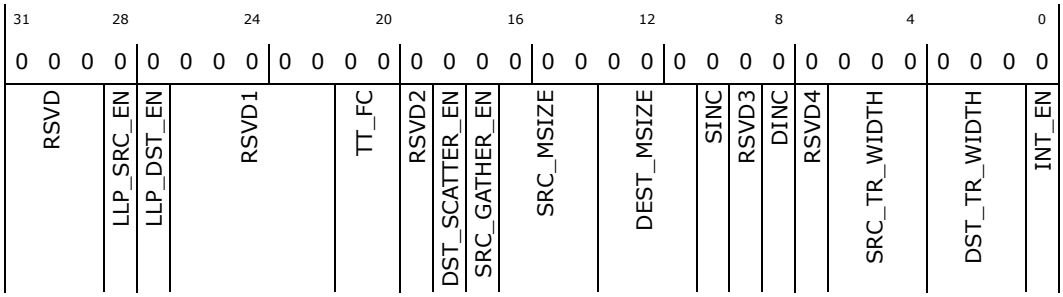
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 70h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)

Bit Range	Default & Access	Field Name (ID): Description
26:22	0x0 RO	**RSVD1:** RSVD
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.2.18 reg_CTL_HI_type (CTL_HI1)—Offset 74h

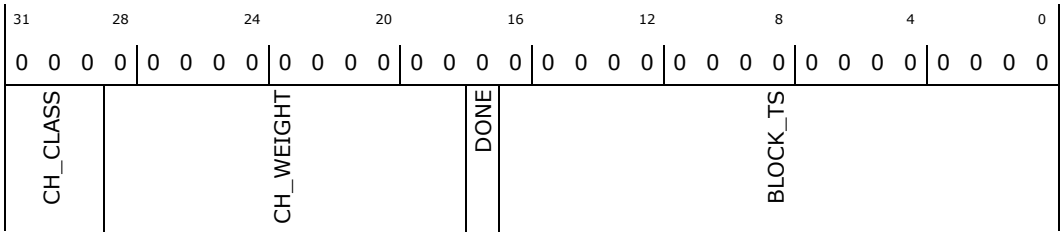
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 74h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.2.19 reg_SSTAT_type (SSTAT1)—Offset 78h

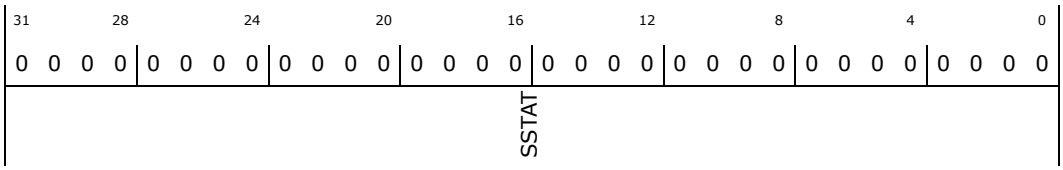
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 78h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.2.20 reg_DSTAT_type (DSTAT1)—Offset 80h

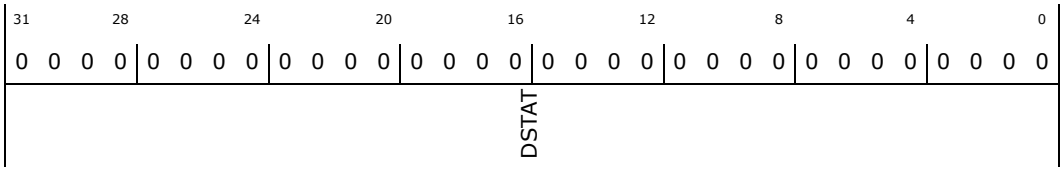
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 80h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.2.21 reg_SSTATAR_type (SSTATAR1)—Offset 88h

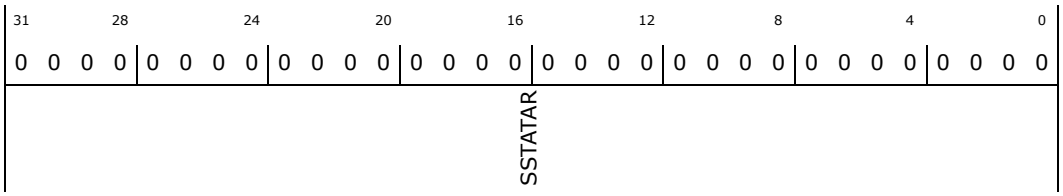
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 88h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.2.22 reg_DSTATAR_type (DSTATAR1)—Offset 90h

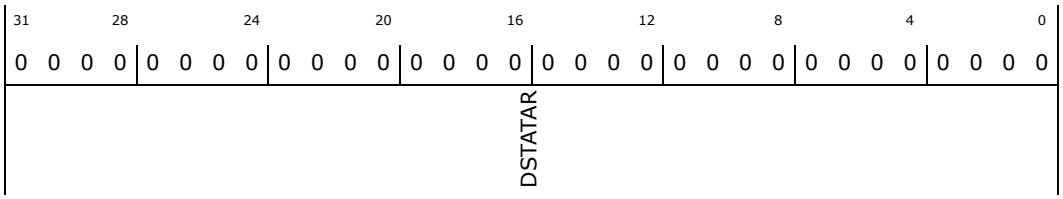
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 90h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.2.23 reg_CFG_LO_type (CFG_LO1)—Offset 98h

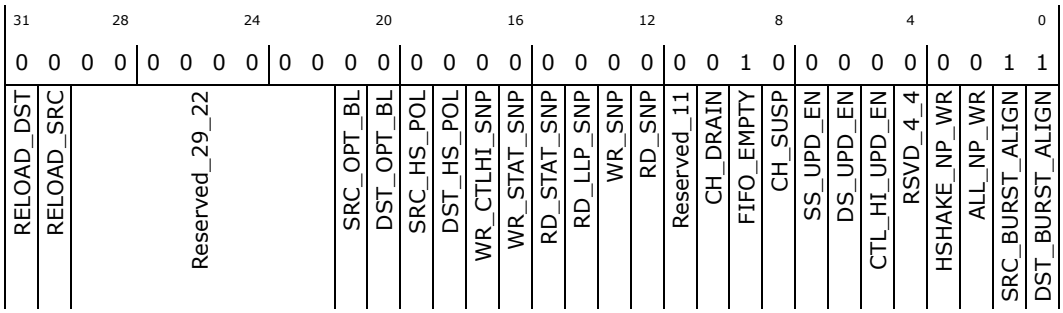
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 98h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.2.24 reg_CFG_HI_type (CFG_HI1)—Offset 9Ch

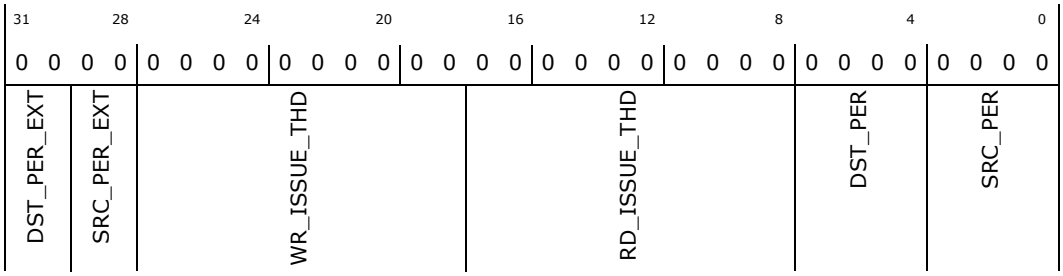
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 9Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.2.25 reg_SGR_type (SGR1)—Offset A0h

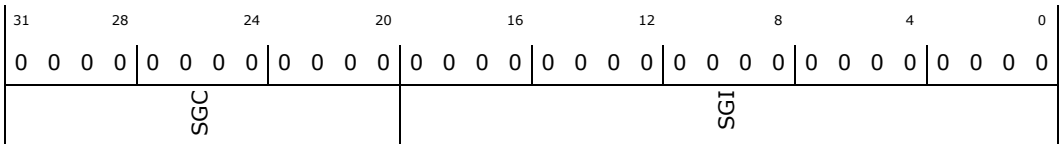
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.2.26 reg_DSR_type (DSR1)—Offset A8h

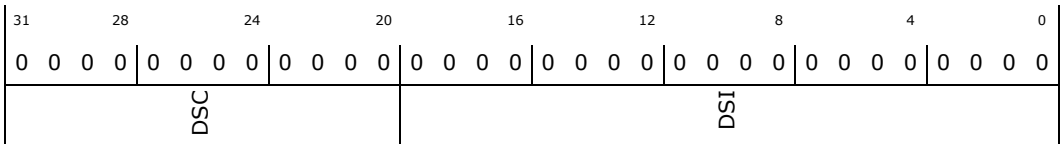
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.2.27 reg_SAR_type (SAR2)—Offset B0h

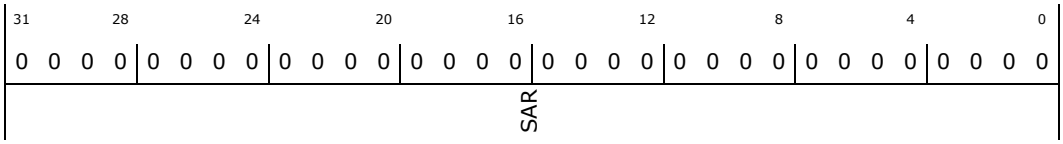
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.28 reg_DAR_type (DAR2)—Offset B8h

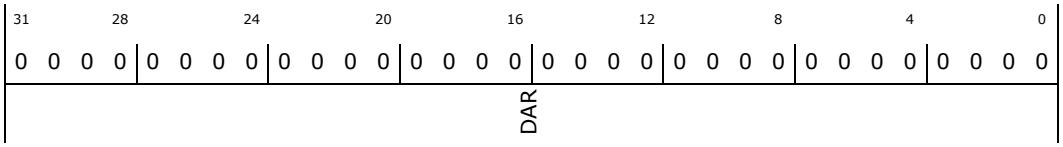
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.29 reg_LLP_type (LLP2)—Offset C0h

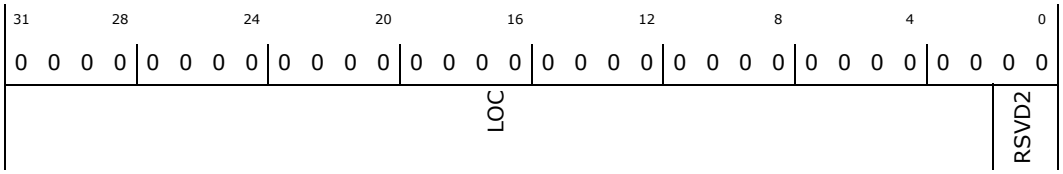
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.2.30 reg_CTL_LO_type (CTL_LO2)—Offset C8h

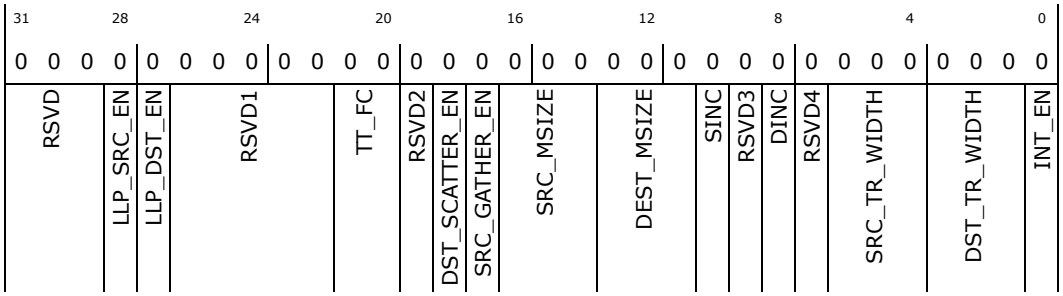
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + C8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.2.31 reg_CTL_HI_type (CTL_HI2)—Offset CCh

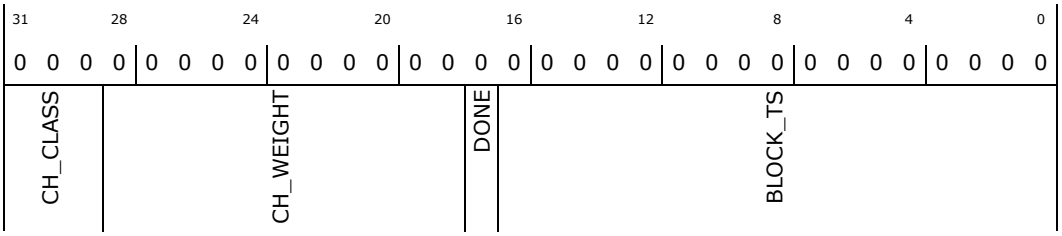
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + CCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.2.32 reg_SSTAT_type (SSTAT2)—Offset D0h

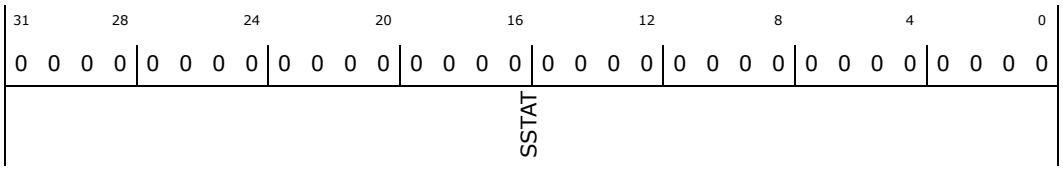
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.2.33 reg_DSTAT_type (DSTAT2)—Offset D8h

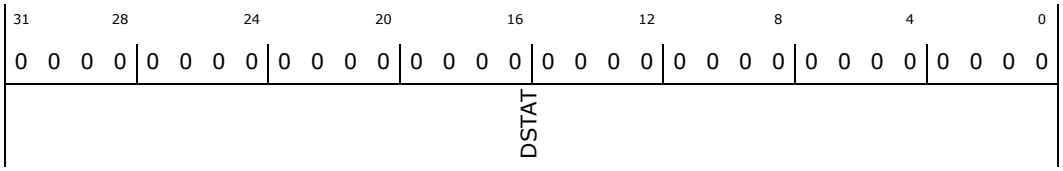
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + D8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.2.34 reg_SSTATAR_type (SSTATAR2)—Offset E0h

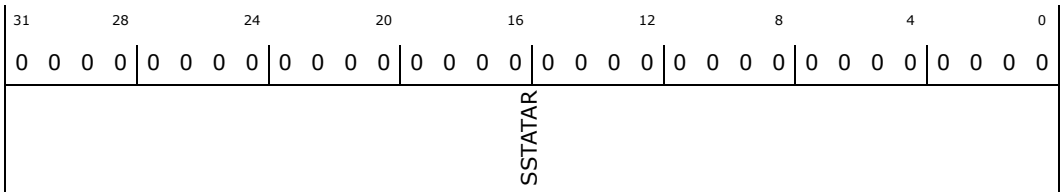
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + E0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.2.35 reg_DSTATAR_type (DSTATAR2)—Offset E8h

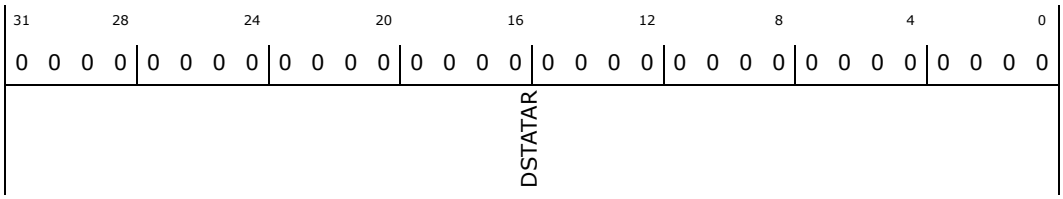
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + E8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.2.36 reg_CFG_LO_type (CFG_LO2)—Offset F0h

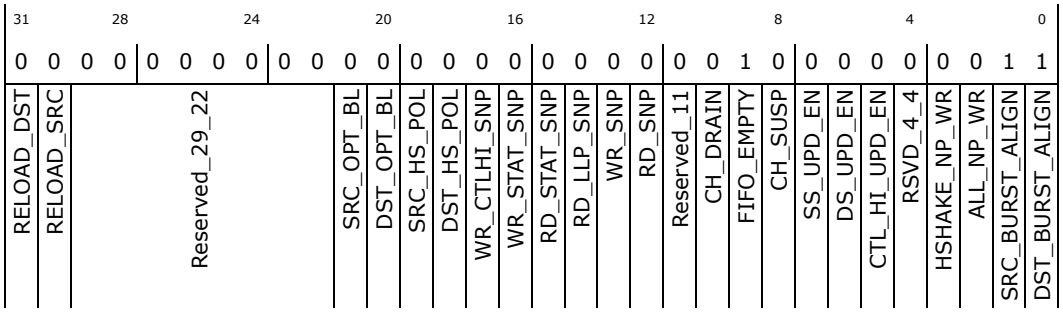
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + F0h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.2.37 reg_CFG_HI_type (CFG_HI2)—Offset F4h

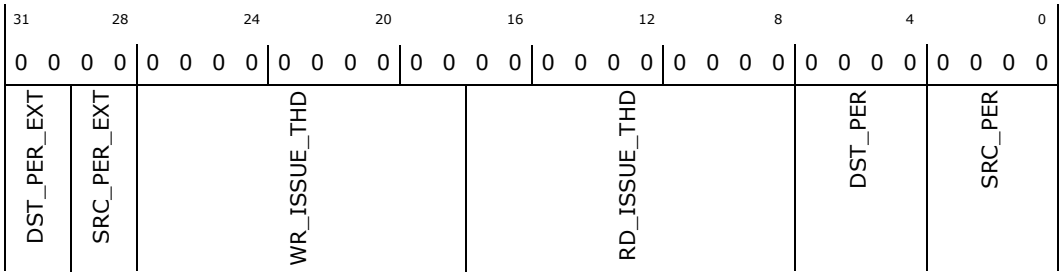
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + F4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.2.38 reg_SGR_type (SGR2)—Offset F8h

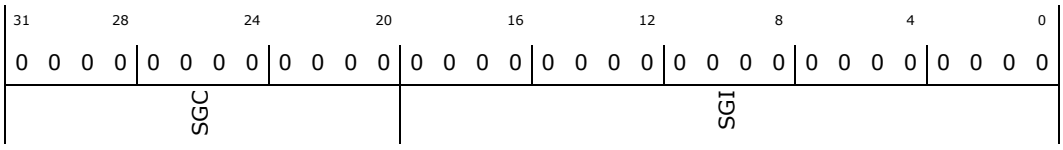
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.2.39 reg_DSR_type (DSR2)—Offset 100h

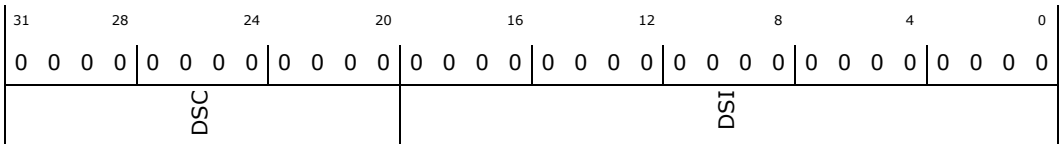
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 100h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.2.40 reg_SAR_type (SAR3)—Offset 108h

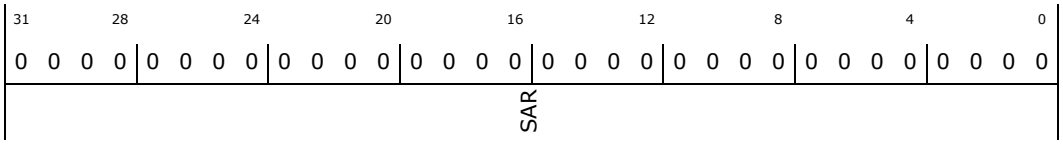
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 108h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.41 reg_DAR_type (DAR3)—Offset 110h

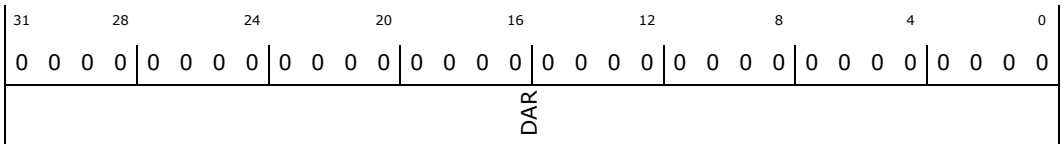
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 110h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.42 reg_LLP_type (LLP3)—Offset 118h

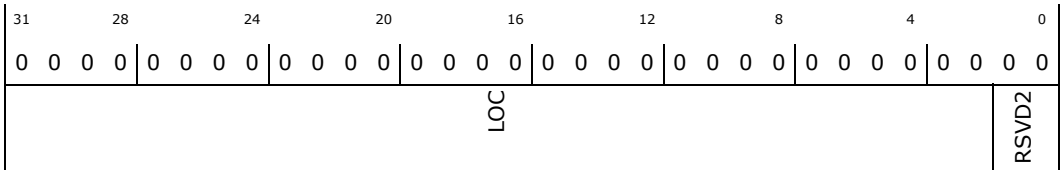
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 118h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.2.43 reg_CTL_LO_type (CTL_LO3)—Offset 120h

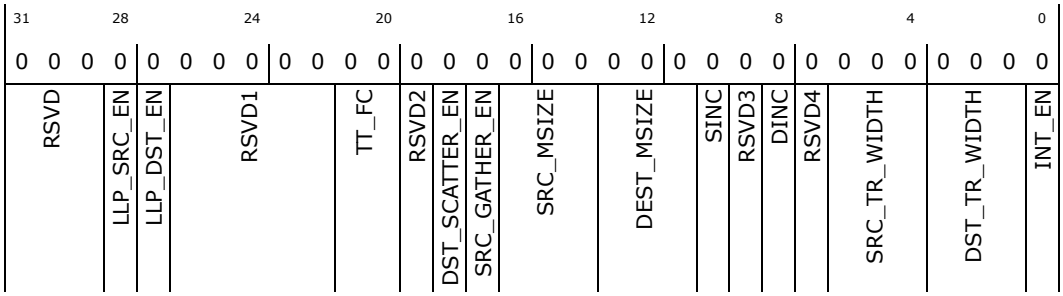
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

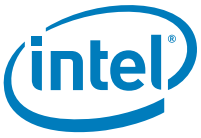
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 120h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD



Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.2.44 reg_CTL_HI_type (CTL_HI3)—Offset 124h

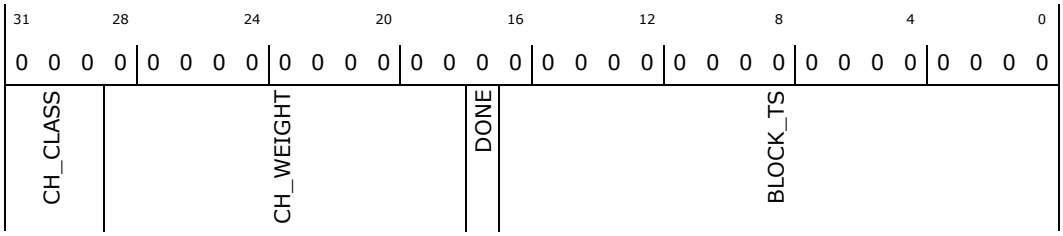
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 124h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.2.45 reg_SSTAT_type (SSTAT3)—Offset 128h

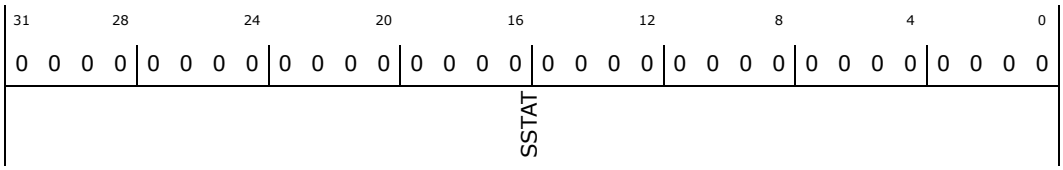
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 128h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.2.46 reg_DSTAT_type (DSTAT3)—Offset 130h

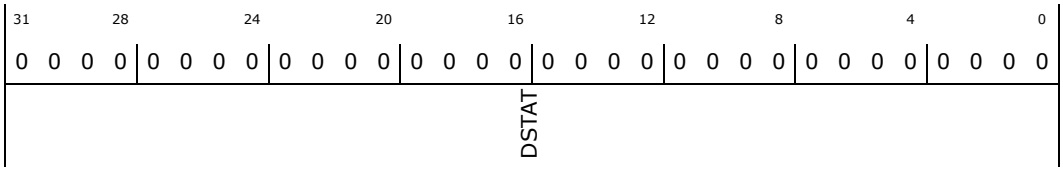
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 130h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.2.47 reg_SSTATAR_type (SSTATAR3)—Offset 138h

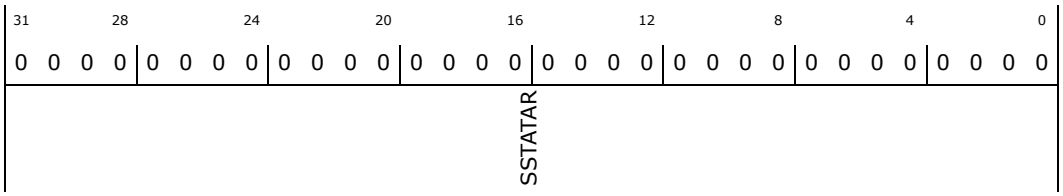
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 138h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.2.48 reg_DSTATAR_type (DSTATAR3)—Offset 140h

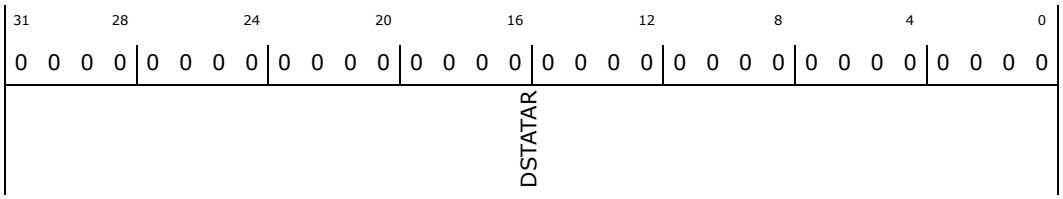
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 140h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.2.49 reg_CFG_LO_type (CFG_LO3)—Offset 148h

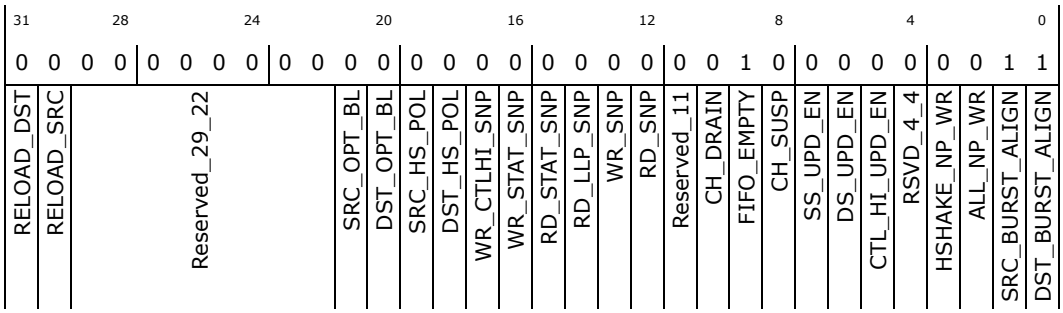
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 148h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.2.50 reg_CFG_HI_type (CFG_HI3)—Offset 14Ch

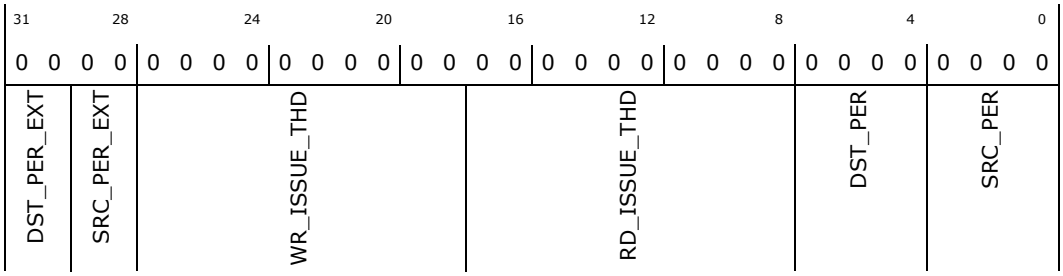
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 14Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.2.51 reg_SGR_type (SGR3)—Offset 150h

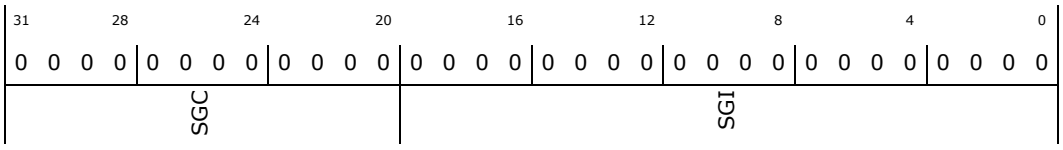
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 150h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.2.52 reg_DSR_type (DSR3)—Offset 158h

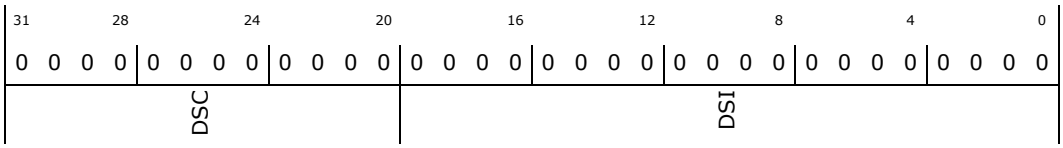
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 158h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.2.53 reg_SAR_type (SAR4)—Offset 160h

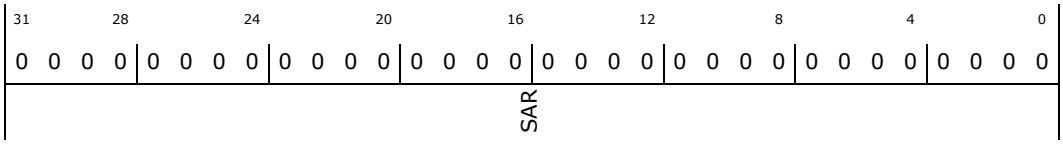
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 160h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.54 reg_DAR_type (DAR4)—Offset 168h

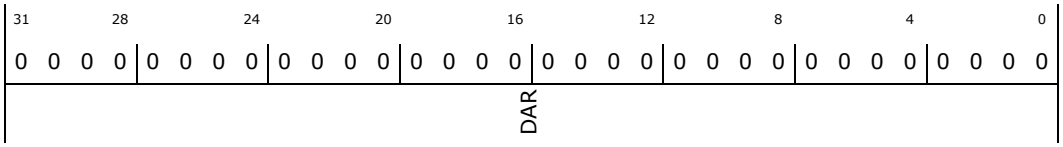
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 168h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.55 reg_LLP_type (LLP4)—Offset 170h

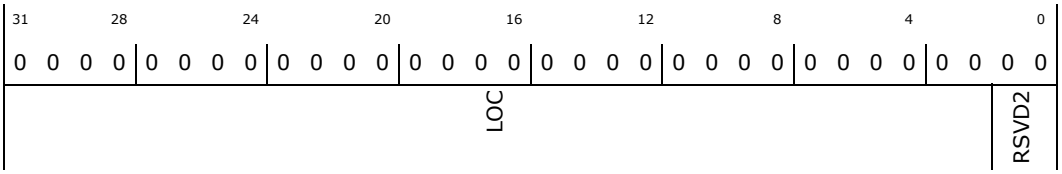
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 170h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.2.56 reg_CTL_LO_type (CTL_LO4)—Offset 178h

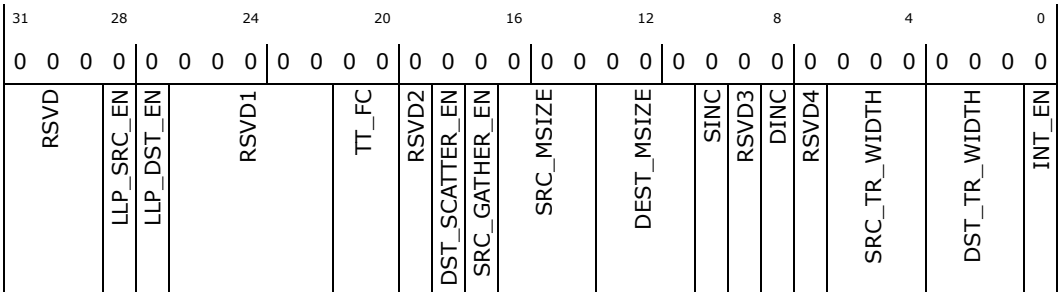
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 178h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.2.57 reg_CTL_HI_type (CTL_HI4)—Offset 17Ch

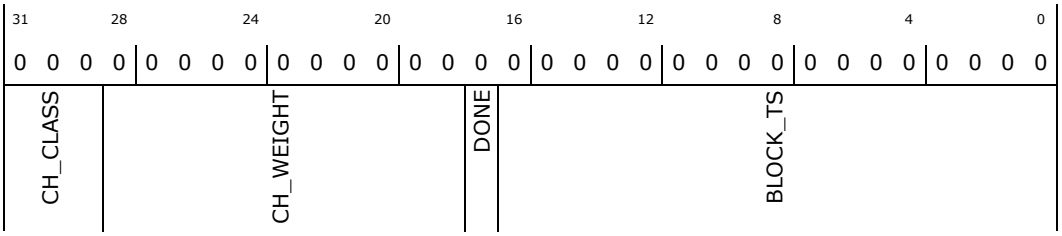
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 17Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.2.58 reg_SSTAT_type (SSTAT4)—Offset 180h

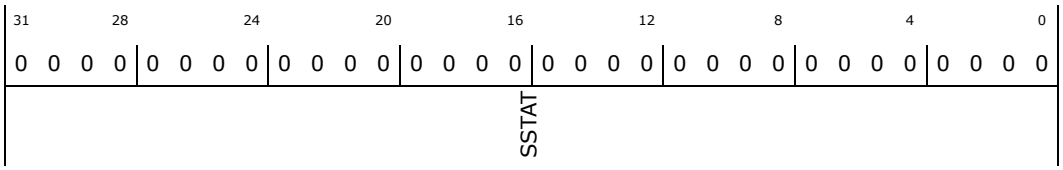
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 180h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.2.59 reg_DSTAT_type (DSTAT4)—Offset 188h

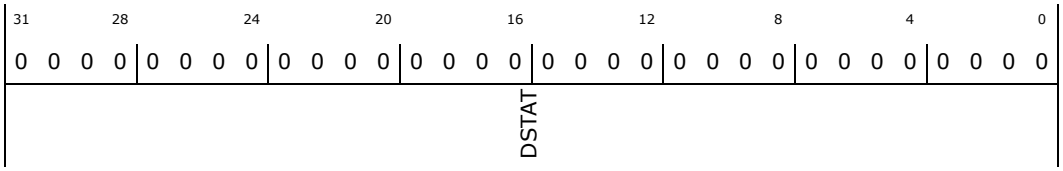
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 188h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.2.60 reg_SSTATAR_type (SSTATAR4)—Offset 190h

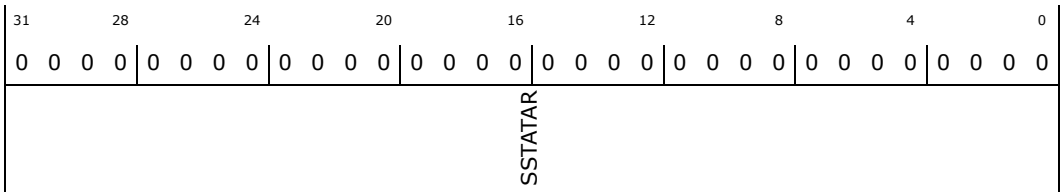
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 190h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.2.61 reg_DSTATAR_type (DSTATAR4)—Offset 198h

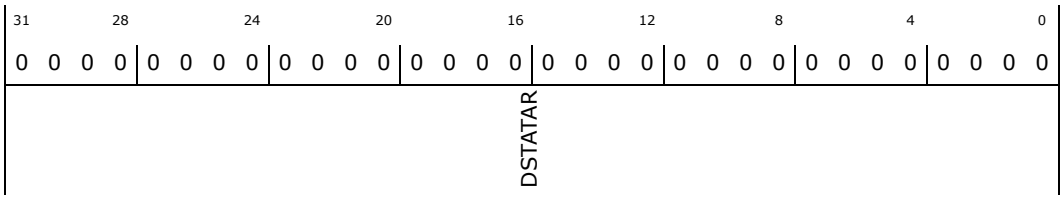
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 198h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.2.62 reg_CFG_LO_type (CFG_LO4)—Offset 1A0h

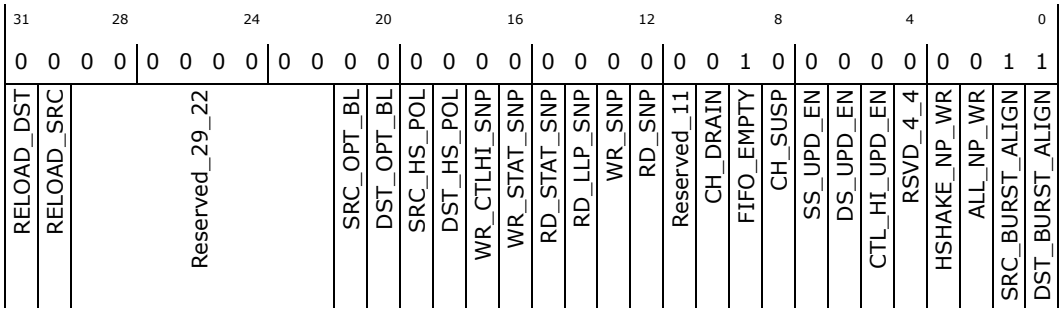
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 1A0h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.2.63 reg_CFG_HI_type (CFG_HI4)—Offset 1A4h

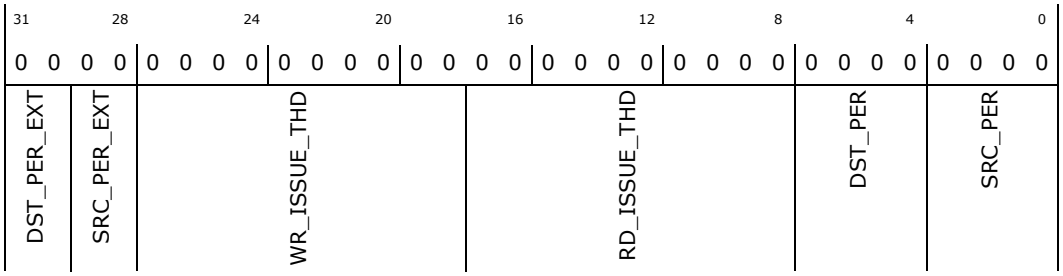
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 1A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.2.64 reg_SGR_type (SGR4)—Offset 1A8h

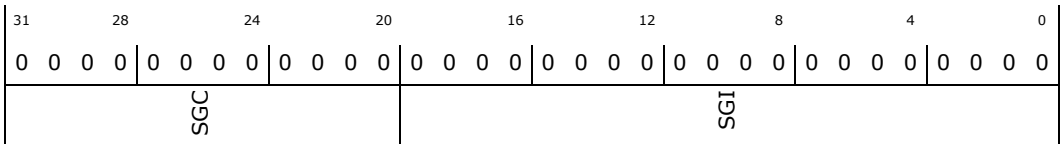
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 1A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.2.65 reg_DSR_type (DSR4)—Offset 1B0h

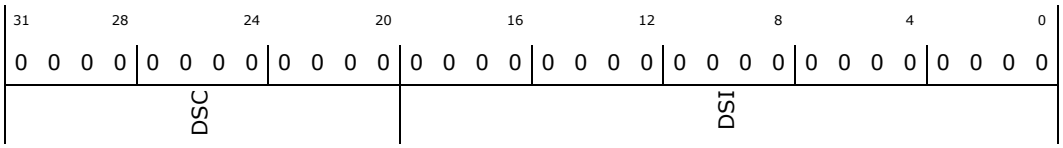
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 1B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.2.66 reg_SAR_type (SAR5)—Offset 1B8h

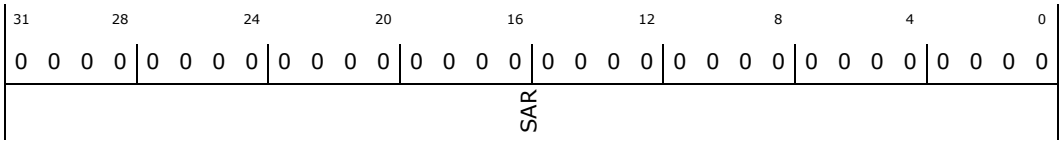
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 1B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.67 reg_DAR_type (DAR5)—Offset 1C0h

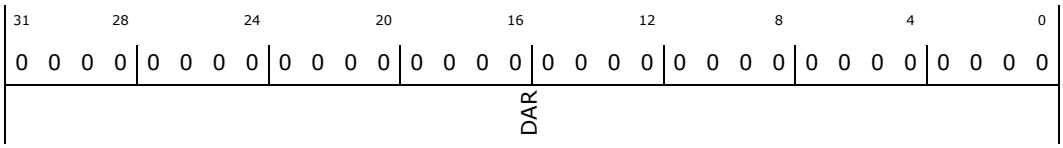
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

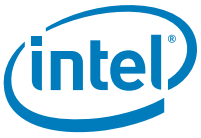
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 1C0h

Default: 00000000h





Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.68 reg_LLP_type (LLP5)—Offset 1C8h

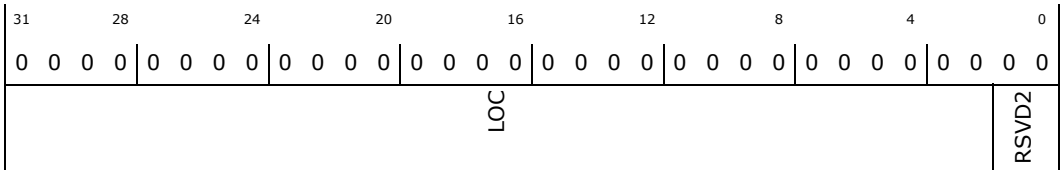
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 1C8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.2.69 reg_CTL_LO_type (CTL_LO5)—Offset 1D0h

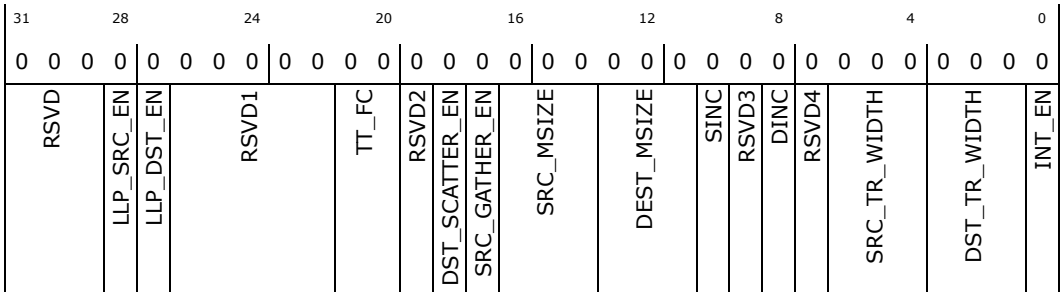
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 1D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.2.70 reg_CTL_HI_type (CTL_HI5)—Offset 1D4h

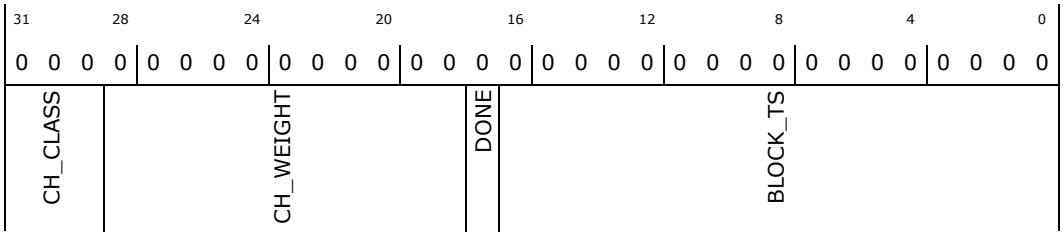
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 1D4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.2.71 reg_SSTAT_type (SSTAT5)—Offset 1D8h

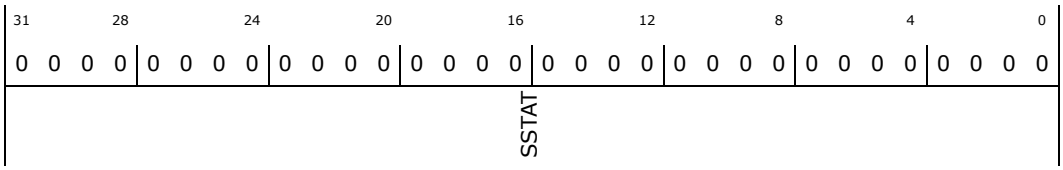
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 1D8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.2.72 reg_DSTAT_type (DSTAT5)—Offset 1E0h

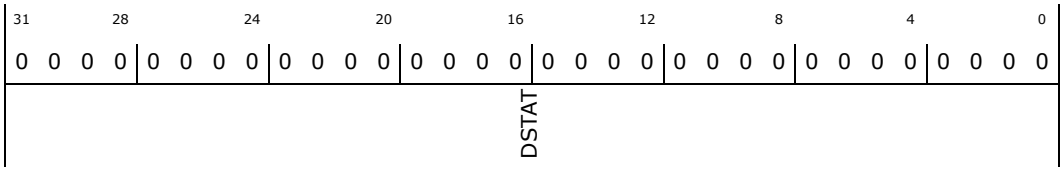
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 1E0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.2.73 reg_SSTATAR_type (SSTATAR5)—Offset 1E8h

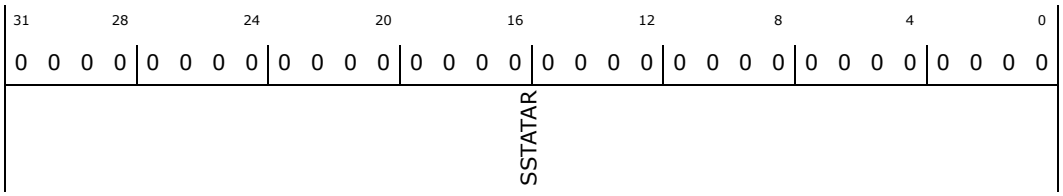
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 1E8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.2.74 reg_DSTATAR_type (DSTATAR5)—Offset 1F0h

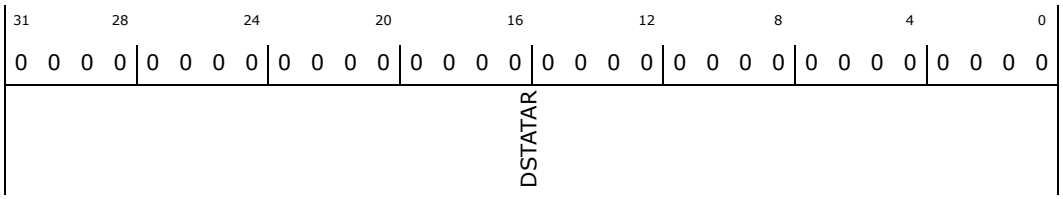
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 1F0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.2.75 reg_CFG_LO_type (CFG_LO5)—Offset 1F8h

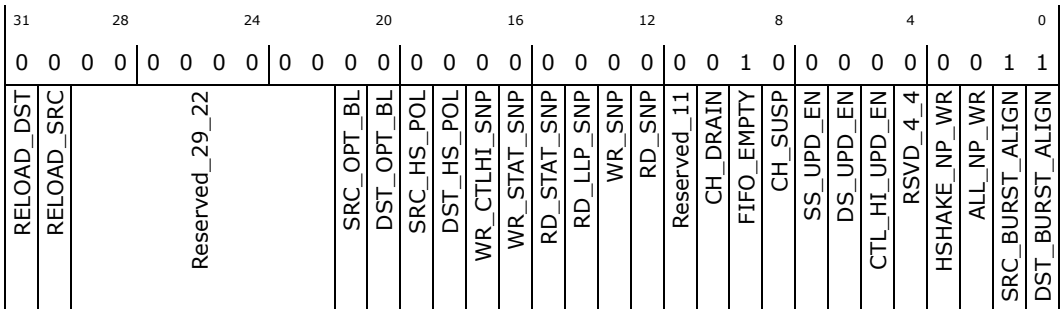
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 1F8h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.2.76 reg_CFG_HI_type (CFG_HI5)—Offset 1FCh

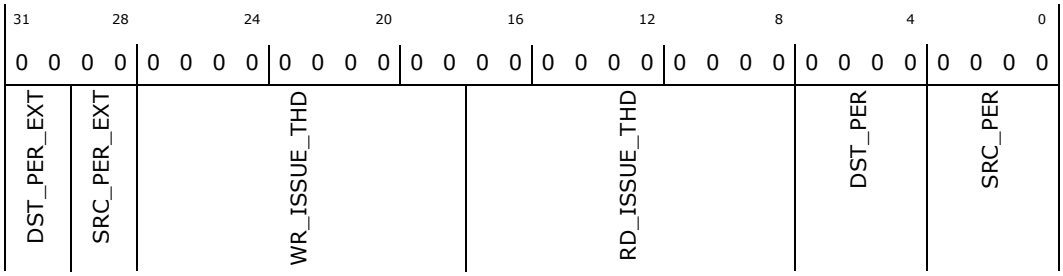
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 1FCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.2.77 reg_SGR_type (SGR5)—Offset 200h

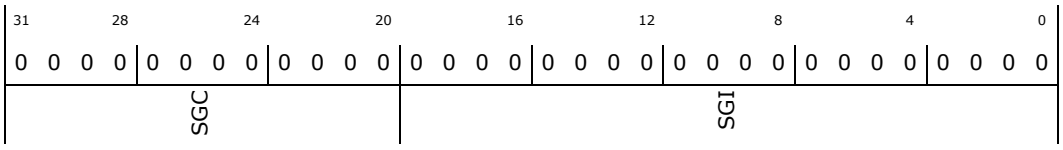
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 200h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.2.78 reg_DSR_type (DSR5)—Offset 208h

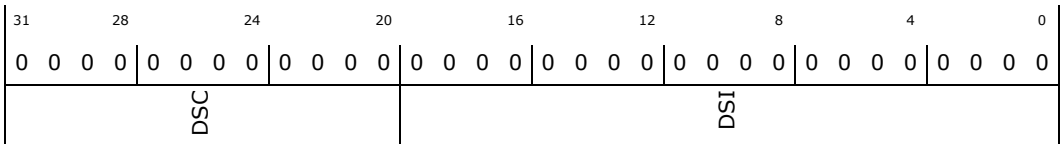
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 208h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.2.79 reg_SAR_type (SAR6)—Offset 210h

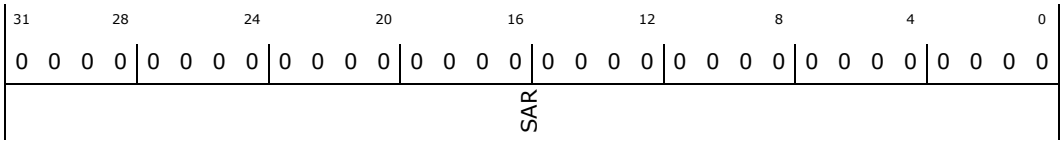
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 210h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.80 reg_DAR_type (DAR6)—Offset 218h

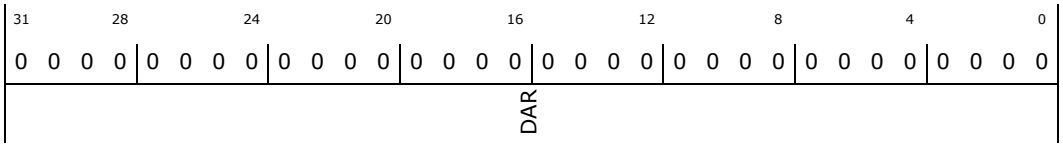
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 218h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.81 reg_LLP_type (LLP6)—Offset 220h

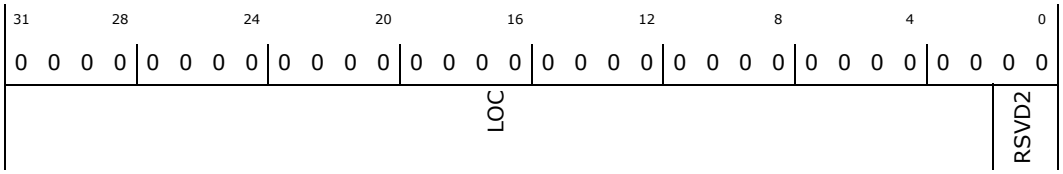
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 220h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.2.82 reg_CTL_LO_type (CTL_LO6)—Offset 228h

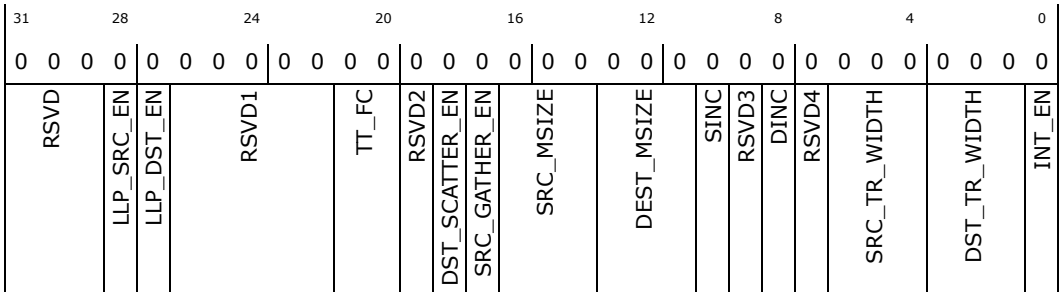
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 228h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.2.83 reg_CTL_HI_type (CTL_HI6)—Offset 22Ch

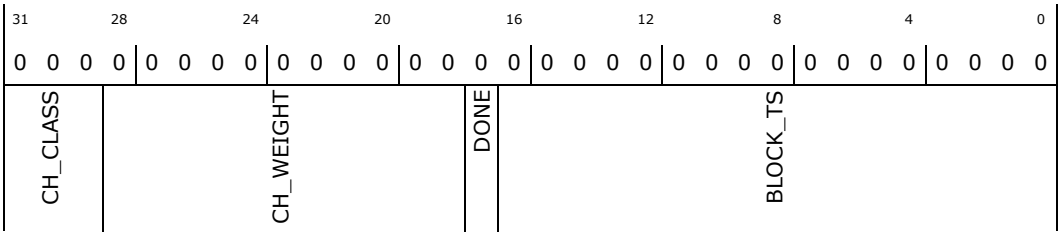
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 22Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.2.84 reg_SSTAT_type (SSTAT6)—Offset 230h

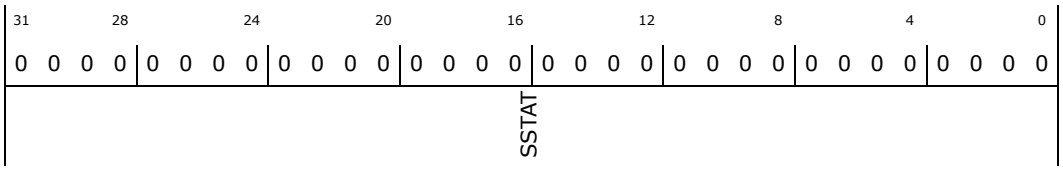
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 230h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.2.85 reg_DSTAT_type (DSTAT6)—Offset 238h

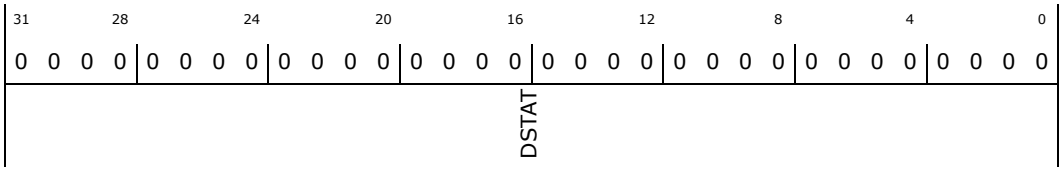
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 238h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.2.86 reg_SSTATAR_type (SSTATAR6)—Offset 240h

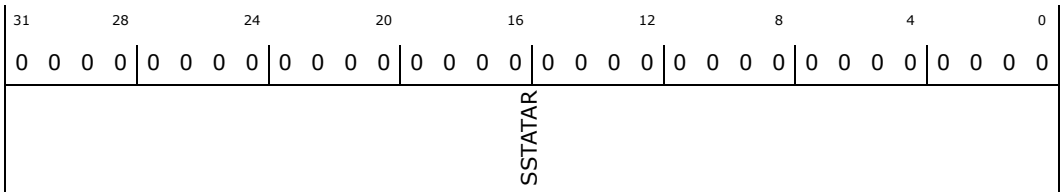
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 240h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.2.87 reg_DSTATAR_type (DSTATAR6)—Offset 248h

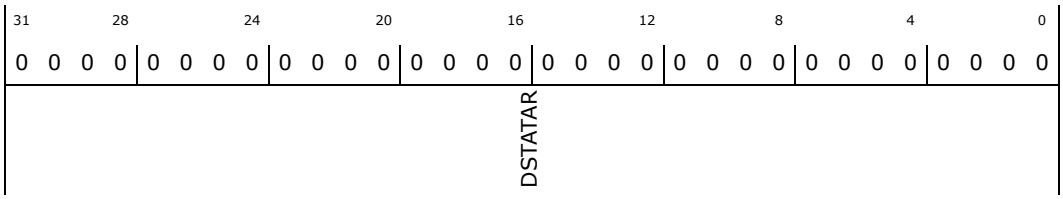
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 248h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.2.88 reg_CFG_LO_type (CFG_LO6)—Offset 250h

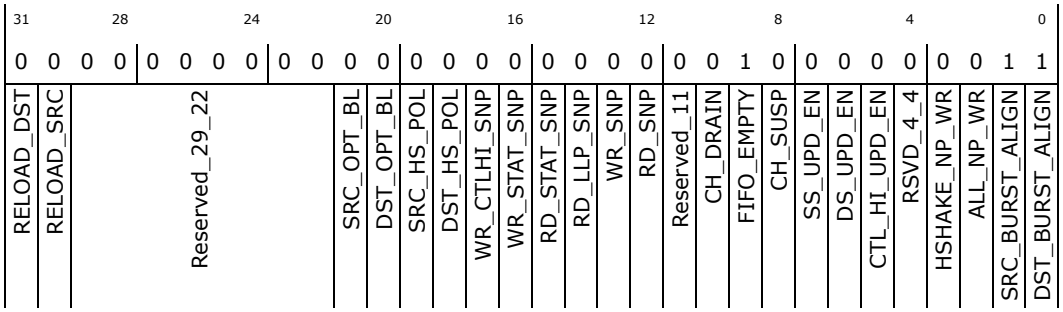
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 250h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.2.89 reg_CFG_HI_type (CFG_HI6)—Offset 254h

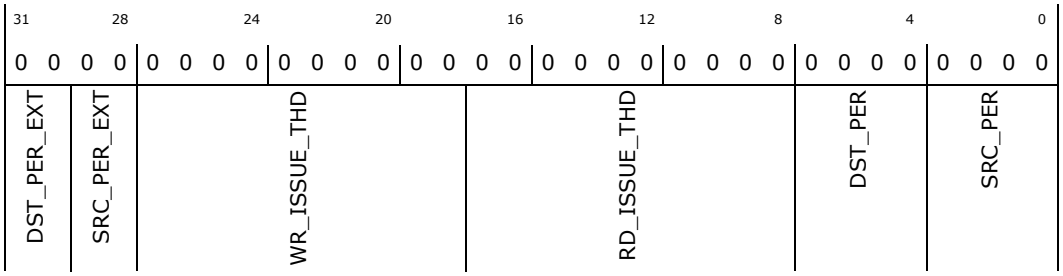
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 254h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.2.90 reg_SGR_type (SGR6)—Offset 258h

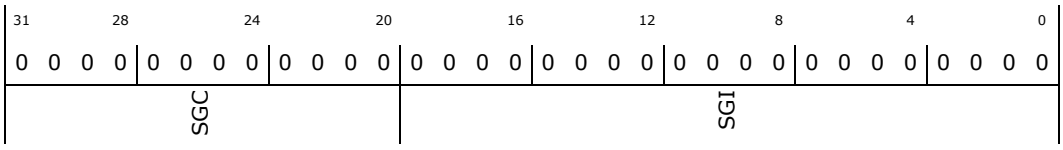
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 258h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.2.91 reg_DSR_type (DSR6)—Offset 260h

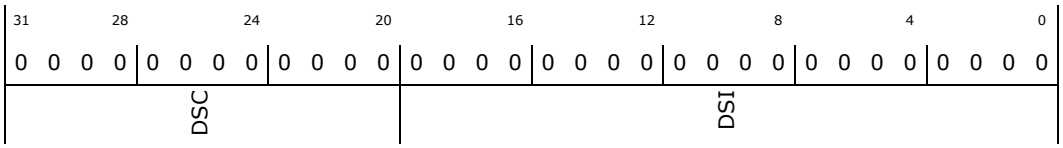
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 260h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.2.92 reg_SAR_type (SAR7)—Offset 268h

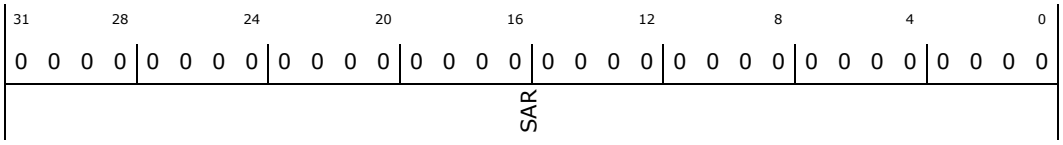
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 268h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.93 reg_DAR_type (DAR7)—Offset 270h

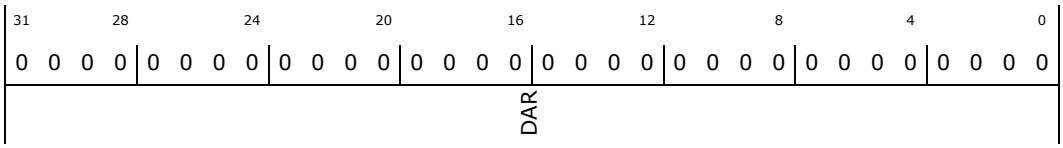
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 270h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.2.94 reg_LLP_type (LLP7)—Offset 278h

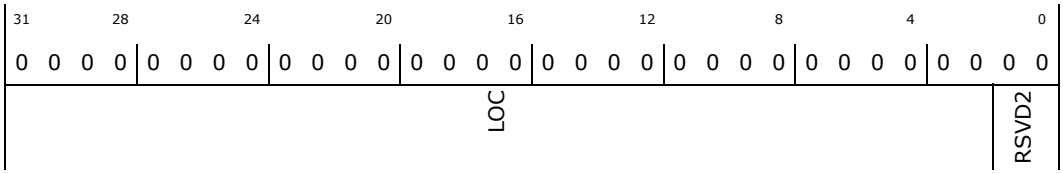
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 278h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.2.95 reg_CTL_LO_type (CTL_LO7)—Offset 280h

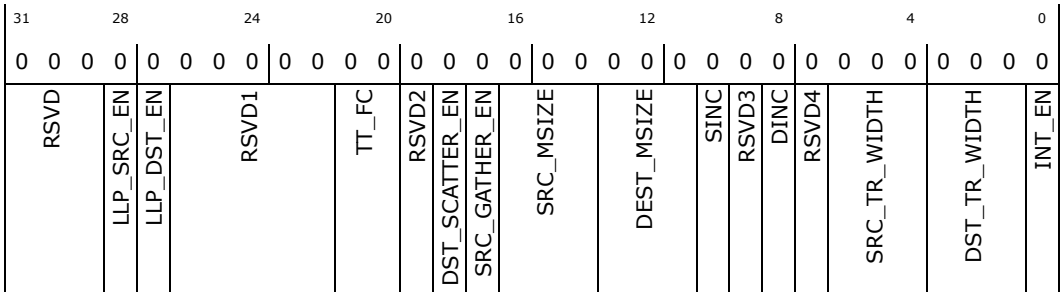
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 280h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.2.96 reg_CTL_HI_type (CTL_HI7)—Offset 284h

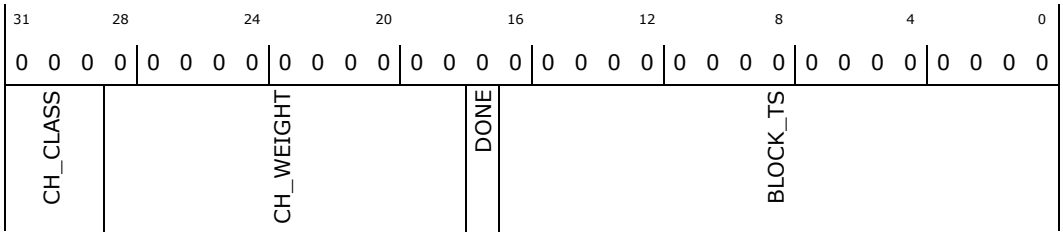
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 284h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.2.97 reg_SSTAT_type (SSTAT7)—Offset 288h

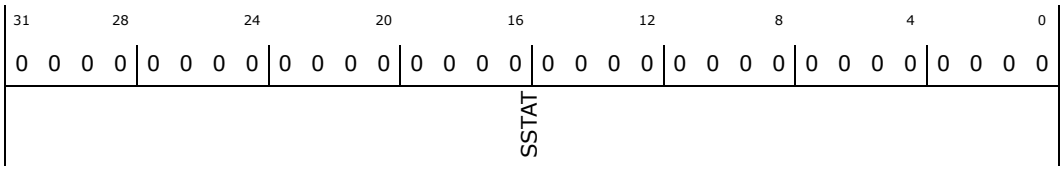
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 288h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.2.98 reg_DSTAT_type (DSTAT7)—Offset 290h

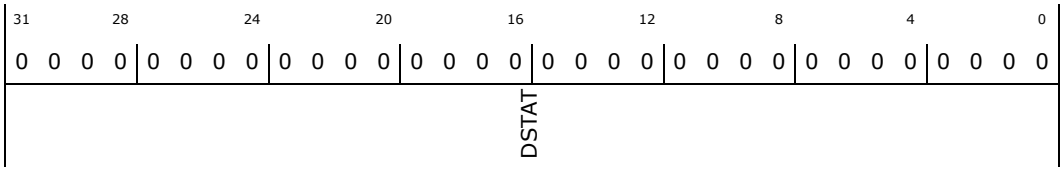
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 290h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.2.99 reg_SSTATAR_type (SSTATAR7)—Offset 298h

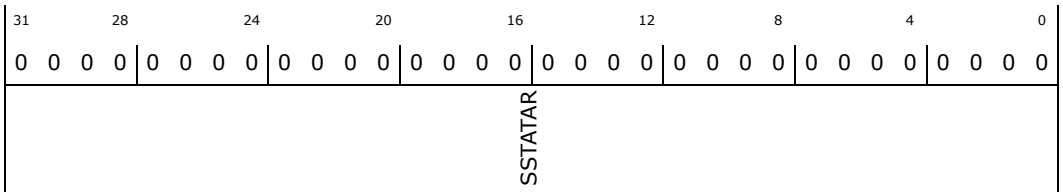
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 298h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.2.100 reg_DSTATAR_type (DSTATAR7)—Offset 2A0h

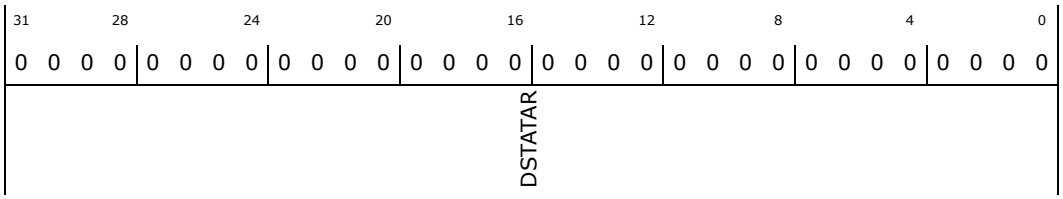
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 2A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.2.101 reg_CFG_LO_type (CFG_LO7)—Offset 2A8h

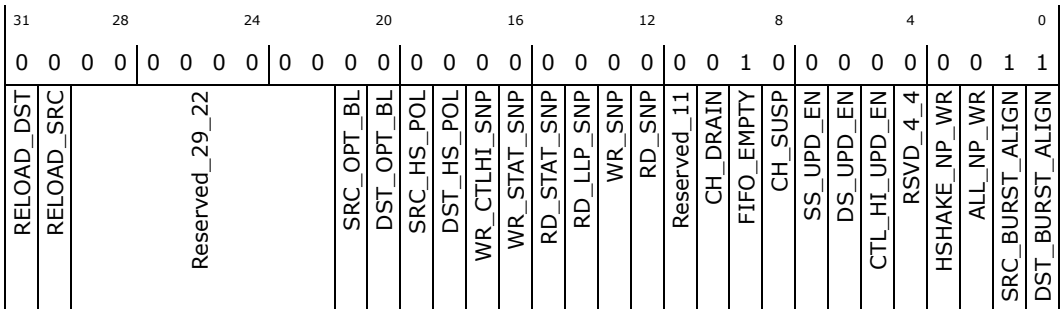
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 2A8h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.2.102 reg_CFG_HI_type (CFG_HI7)—Offset 2ACh

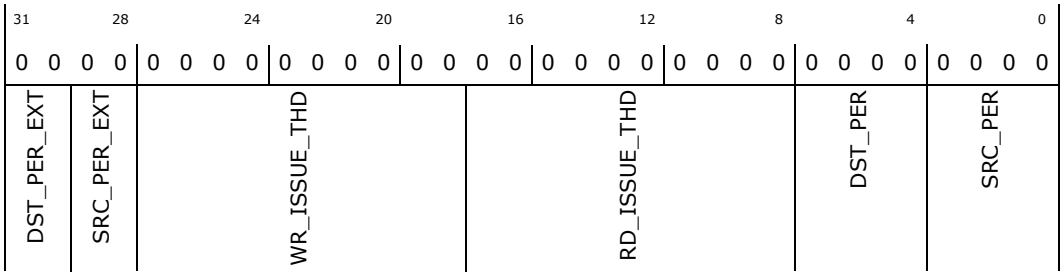
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 2ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.2.103 reg_SGR_type (SGR7)—Offset 2B0h

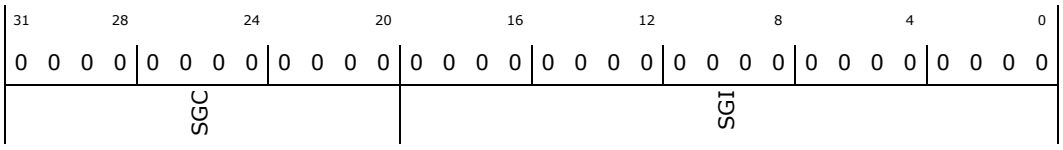
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 2B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.2.104 reg_DSR_type (DSR7)—Offset 2B8h

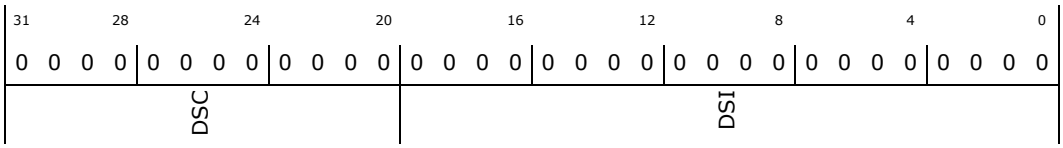
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 2B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.2.105 reg_Raw_type (RawTfr)—Offset 2C0h

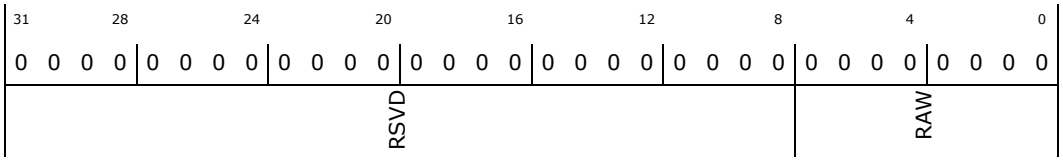
Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 2C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**RAW:** Raw interrupt status

8.2.106 reg_Raw_type (RawBlock)—Offset 2C8h

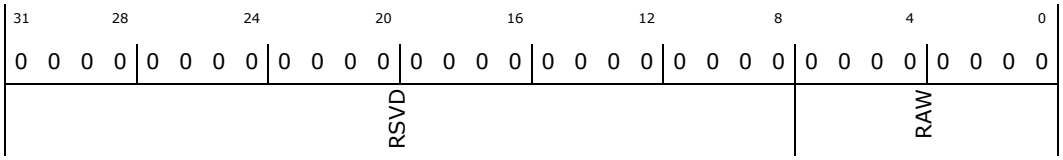
Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 2C8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**RAW:** Raw interrupt status

8.2.107 reg_Raw_type (RawSrcTran)—Offset 2D0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw

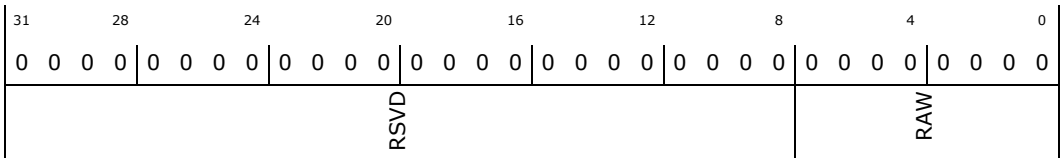
transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 2D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**RAW:** Raw interrupt status

8.2.108 reg_Raw_type (RawDstTran)—Offset 2D8h

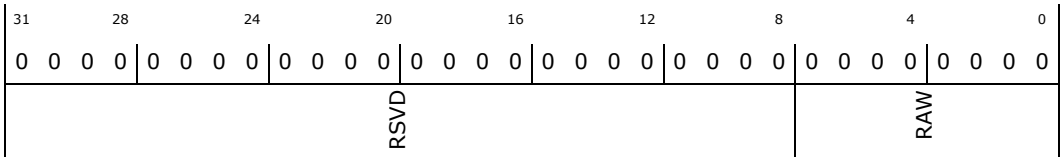
Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 2D8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**RAW:** Raw interrupt status

8.2.109 reg_Raw_type (RawErr)—Offset 2E0h

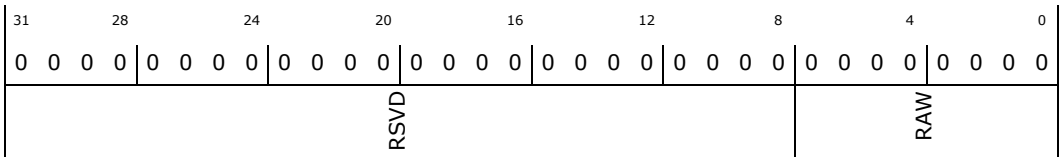
Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 2E0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**RAW:** Raw interrupt status

8.2.110 reg_Status_type (StatusTfr)—Offset 2E8h

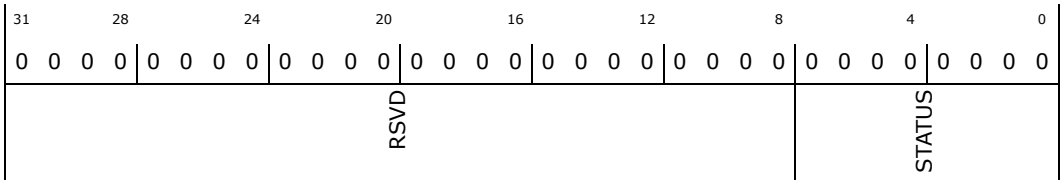
All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 2E8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**STATUS:** Interrupt status

8.2.111 reg_Status_type (StatusBlock)—Offset 2F0h

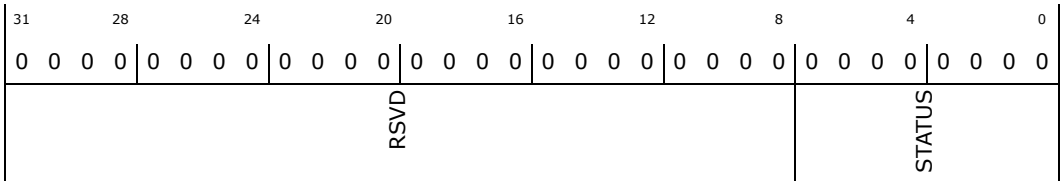
All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 2F0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**STATUS:** Interrupt status

8.2.112 reg_Status_type (StatusSrcTran)—Offset 2F8h

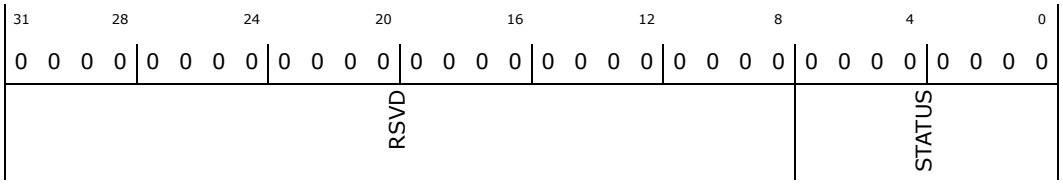
All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 2F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**STATUS:** Interrupt status

8.2.113 reg_Status_type (StatusDstTran)—Offset 300h

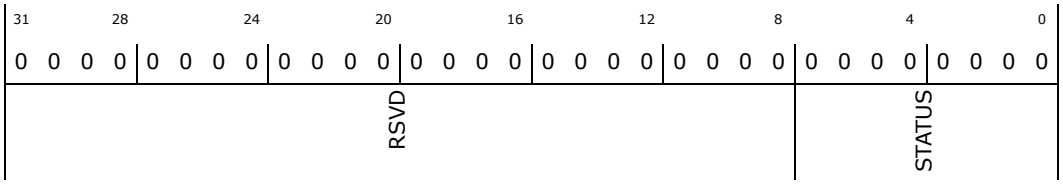
All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 300h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**STATUS:** Interrupt status

8.2.114 reg_Status_type (StatusErr)—Offset 308h

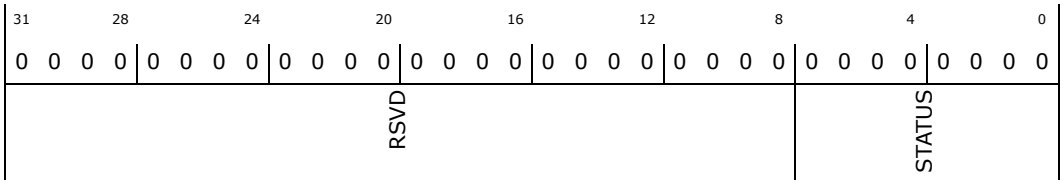
All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 308h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**STATUS:** Interrupt status

8.2.115 reg_Mask_type (MaskTfr)—Offset 310h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation.

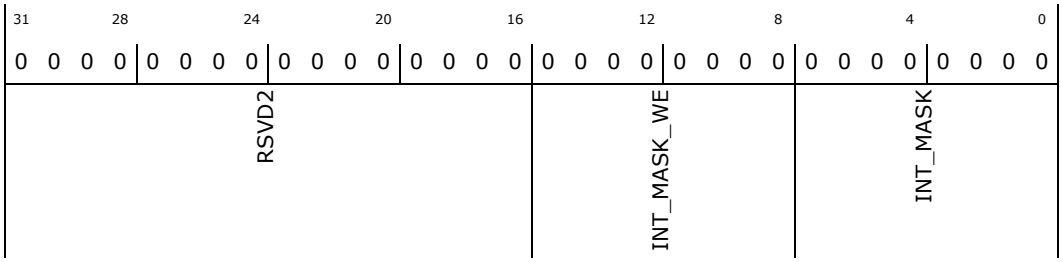
For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 310h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD2:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

8.2.116 reg_Mask_type (MaskBlock)—Offset 318h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged.

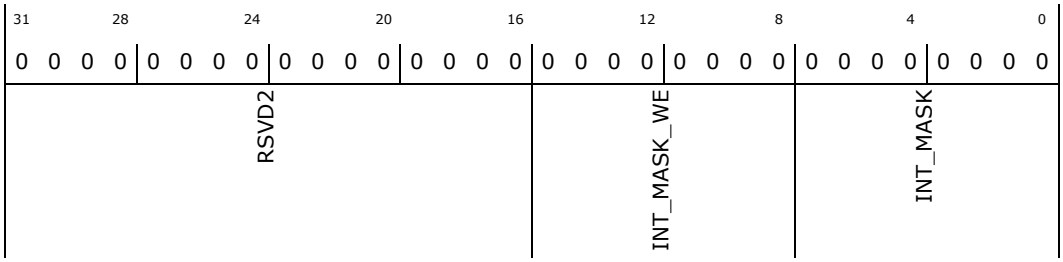
Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 318h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD2:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

8.2.117 reg_Mask_type (MaskSrcTran)—Offset 320h

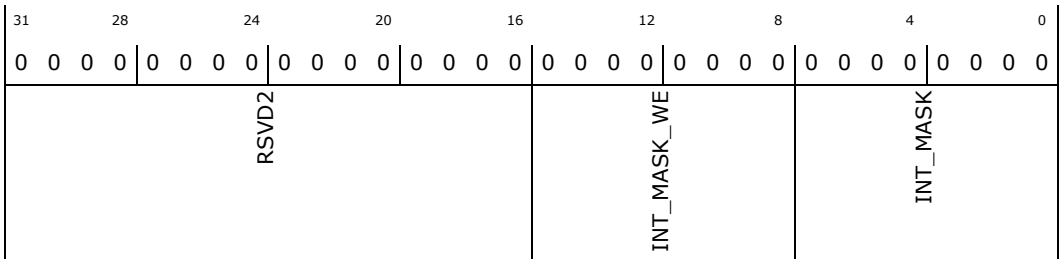
The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 320h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD2:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

8.2.118 reg_Mask_type (MaskDstTran)—Offset 328h

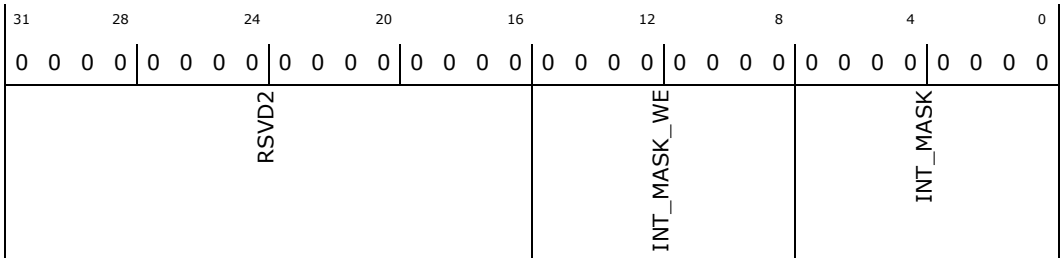
The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 328h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD2:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

8.2.119 reg_Mask_type (MaskErr)—Offset 330h

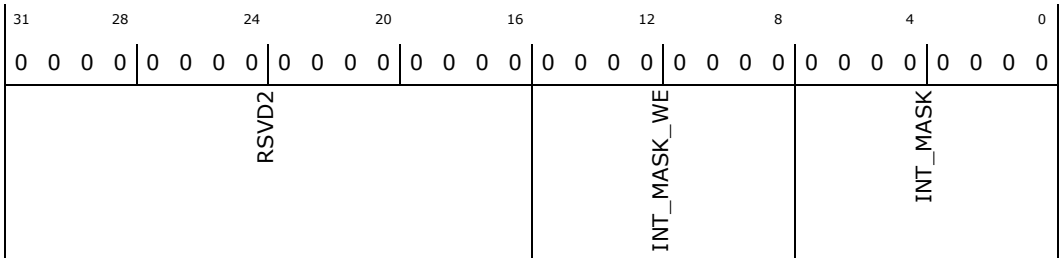
The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 330h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD2:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

8.2.120 reg_Clear_type (ClearTfr)—Offset 338h

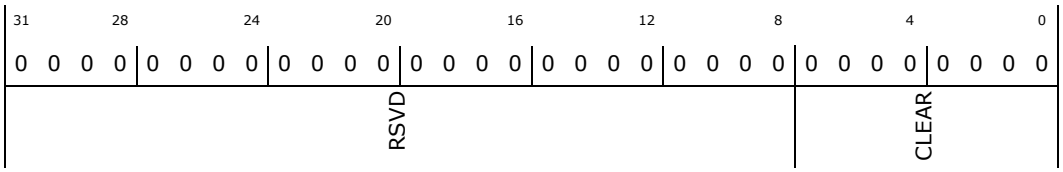
Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 338h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

8.2.121 reg_Clear_type (ClearBlock)—Offset 340h

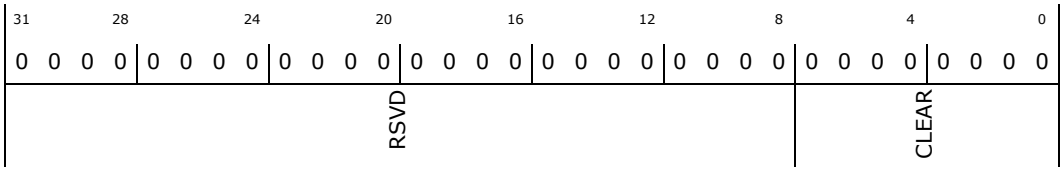
Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 340h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

8.2.122 reg_Clear_type (ClearSrcTran)—Offset 348h

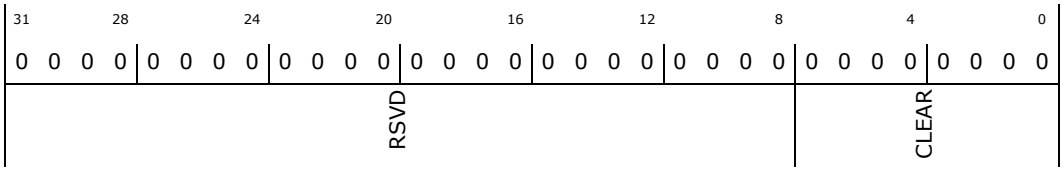
Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 348h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

8.2.123 reg_Clear_type (ClearDstTran)—Offset 350h

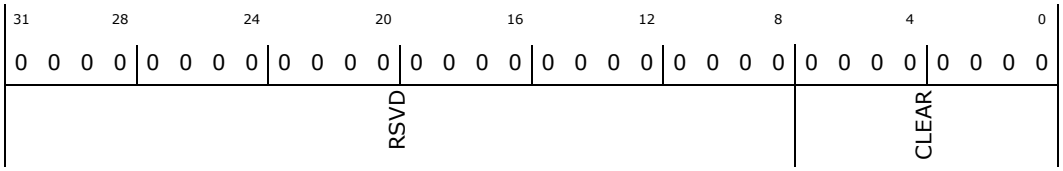
Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 350h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

8.2.124 reg_Clear_type (ClearErr)—Offset 358h

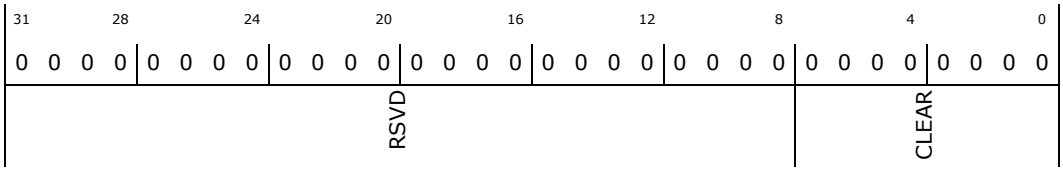
Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 358h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

8.2.125 reg_StatusInt_type (StatusInt)—Offset 360h

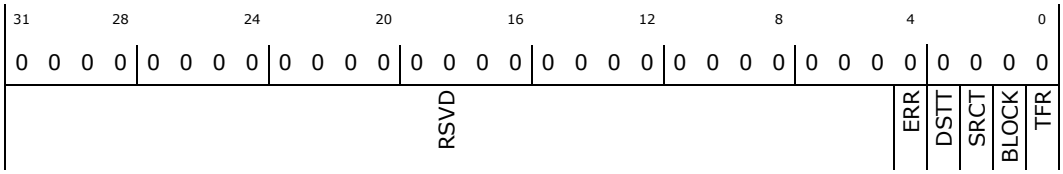
The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran,StatusErr is ORed to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 360h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RO	**RSVD:** Reserved
4	0x0 RO	**ERR:** OR of the contents of StatusErr register.
3	0x0 RO	**DSTT:** OR of the contents of StatusDst register.
2	0x0 RO	**SRCT:** OR of the contents of StatusSrcTran register
1	0x0 RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0x0 RO	**TFR:** OR of the contents of StatusTfr register.

8.2.126 reg_DmaCfgReg_type (DmaCfgReg)—Offset 398h

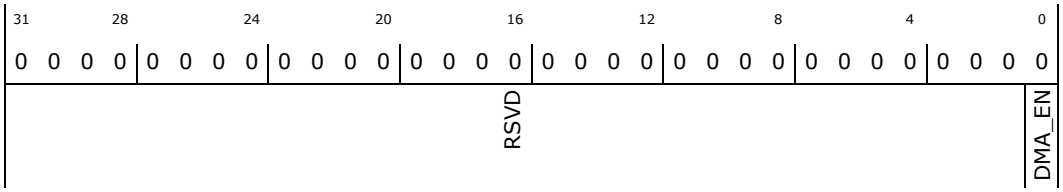
This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 398h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD:** Reserved
0	0x0 RW	**DMA_EN:** DMA Enable bit. 0 = DMA Disabled 1 = DMA Enabled

8.2.127 reg_ChEnReg_type (ChEnReg)—Offset 3A0h

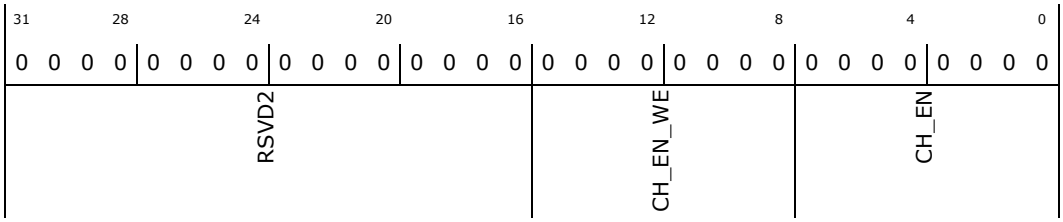
This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority. All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer. For example, writing hex 01x1 writes a 1 into ChEnReg(0), while ChEnReg(7:1) remains unchanged. Writing hex 00xx leaves ChEnReg(7:0) unchanged. Note that a read-modified write is not required.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 3A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD2:** Reserved
15:8	0x0 WO	**CH_EN_WE:** Channel enable write enable.
7:0	0x0 RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

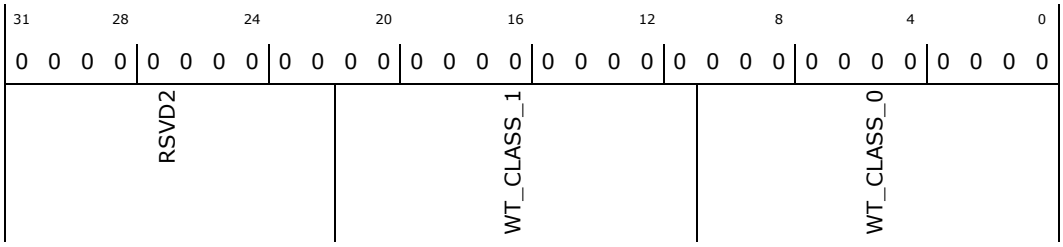
8.2.128 reg_CLASS_PRIORITY0_LO_type (ClassPriority0_LO)—Offset 3B8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 3B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**RSVD2:** Reserved
21:11	0x0 RW	**WT_CLASS_1:** Class Weight 1: Value of K assigns a weight of (K+1) to Class 1. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0x0 RW	**WT_CLASS_0:** Class Weight 0: Value of K assigns a weight of (K+1) to Class 0. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

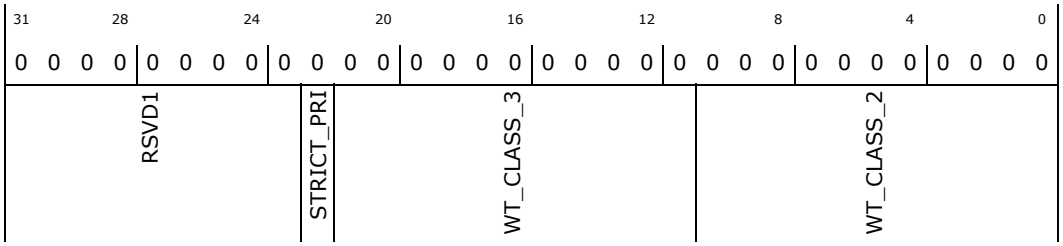
8.2.129 reg_CLASS_PRIORITY0_HI_type (ClassPriority0_HI)—Offset 3BCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 3BCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RSVD1:** Reserved
22	0x0 RW	**STRICT_PRI:** If set, Higher class values will always have higher priorities than lower class values. If not set, round-robin arbitration will be used between different classes using WT_CLASS_n values.
21:11	0x0 RW	**WT_CLASS_3:** Class Weight 3: Value of K assigns a weight of (K+1) to Class 3. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0x0 RW	**WT_CLASS_2:** Class Weight 2: Value of K assigns a weight of (K+1) to Class 2. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

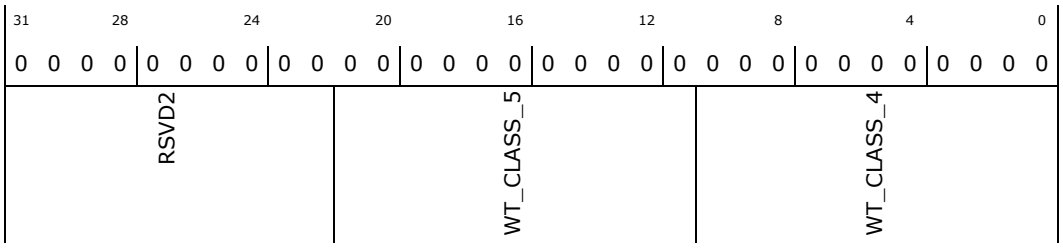
8.2.130 reg_CLASS_PRIORITY1_LO_type (ClassPriority1_LO)—Offset 3C0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 3C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**RSVD2:** Reserved
21:11	0x0 RW	**WT_CLASS_5:** Class Weight 5: Value of K assigns a weight of (K+1) to Class 5. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0x0 RW	**WT_CLASS_4:** Class Weight 4: Value of K assigns a weight of (K+1) to Class 4. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

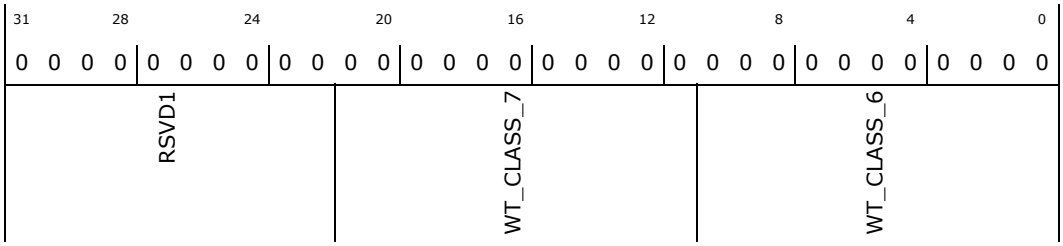
8.2.131 reg_CLASS_PRIORITY1_HI_type (ClassPriority1_HI)—Offset 3C4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 3C4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**RSVD1:** Reserved
21:11	0x0 RW	**WT_CLASS_7:** Class Weight 7: Value of K assigns a weight of (K+1) to Class 7. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0x0 RW	**WT_CLASS_6:** Class Weight 6: Value of K assigns a weight of (K+1) to Class 6. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

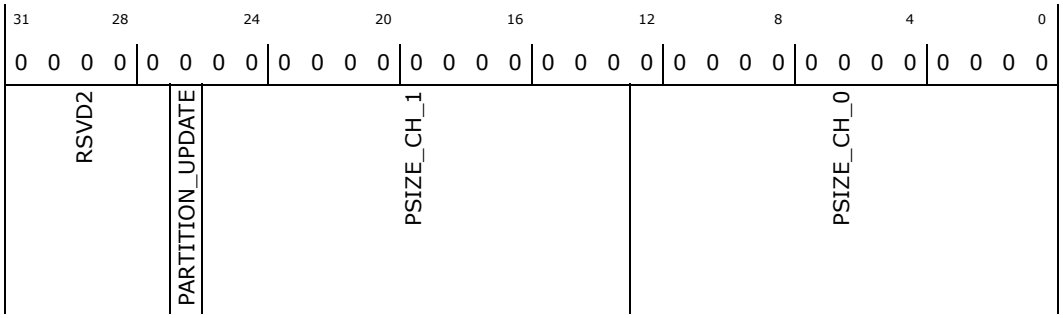
8.2.132 reg_FIFO_PARTITION0_LO_type (FifoPartition0_LO)—Offset 400h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 400h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RSVD2:** Reserved
26	0x0 RW	**PARTITION_UPDATE:** SW needs to write to this bit for the partitioning assignments to take effect.
25:13	0x0 RW	**PSIZE_CH_1:** Partition Byte Size assigned to Channel 1. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0x0 RW	**PSIZE_CH_0:** Partition Byte Size assigned to Channel 0. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

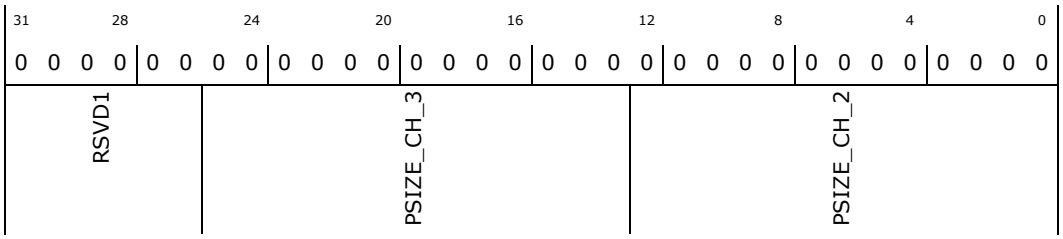
8.2.133 reg_FIFO_PARTITION0_HI_type (FifoPartition0_HI)—Offset 404h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 9C000h] + 404h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD1:** Reserved
25:13	0x0 RW	**PSIZE_CH_3:** Partition Byte Size assigned to Channel 3. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

Bit Range	Default & Access	Field Name (ID): Description
12:0	0x0 RW	**PSIZE_CH_2:** Partition Byte Size assigned to Channel 2. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

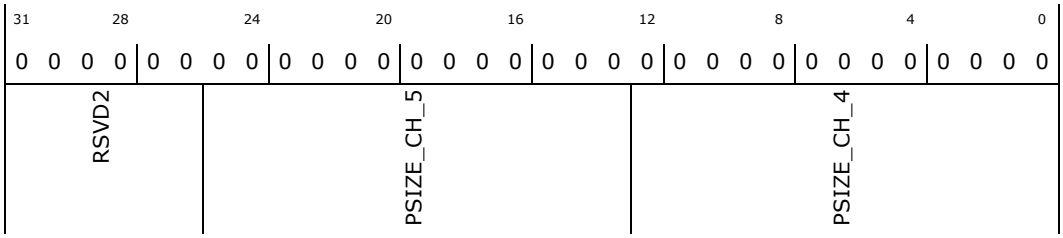
8.2.134 reg_FIFO_PARTITION1_LO_type (FifoPartition1_LO)—Offset 408h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 408h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD2:** Reserved
25:13	0x0 RW	**PSIZE_CH_5:** Partition Byte Size assigned to Channel 5. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0x0 RW	**PSIZE_CH_4:** Partition Byte Size assigned to Channel 4. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

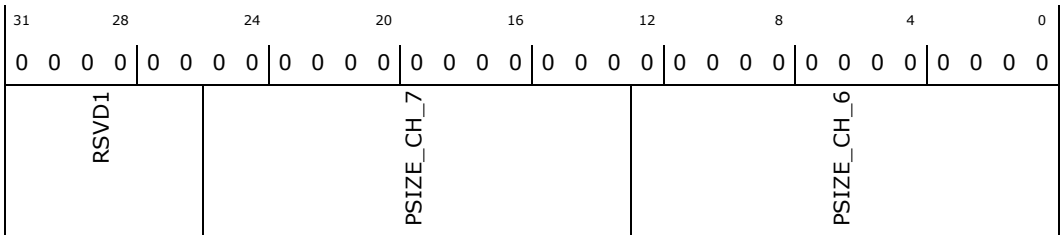
8.2.135 reg_FIFO_PARTITION1_HI_type (FifoPartition1_HI)—Offset 40Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 40Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD1:** Reserved
25:13	0x0 RW	**PSIZE_CH_7:** Partition Byte Size assigned to Channel 7. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0x0 RW	**PSIZE_CH_6:** Partition Byte Size assigned to Channel 6. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

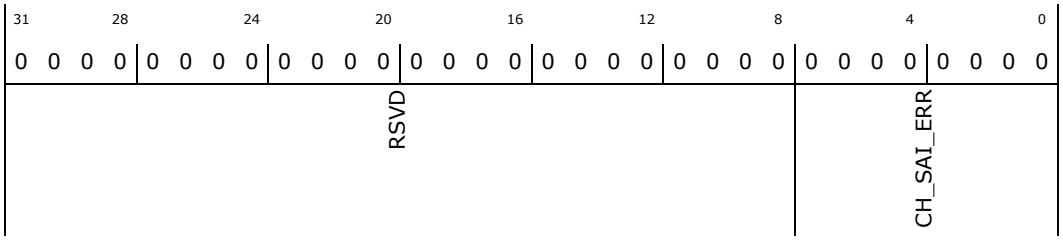
8.2.136 reg_SAI_Error_type (SAI_ERR)—Offset 410h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 410h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**CH_SAI_ERR:** 1: SAI Error occurred on Ch [n] 0: No SAI Error occurred on Ch [n] SAI_ERROR[n] is set by HW on SAI violation for channel [n]. All bits get cleared by SW when reading this register

8.2.137 reg_GLOBAL_CFG_type (GLOBAL_CFG)—Offset 418h

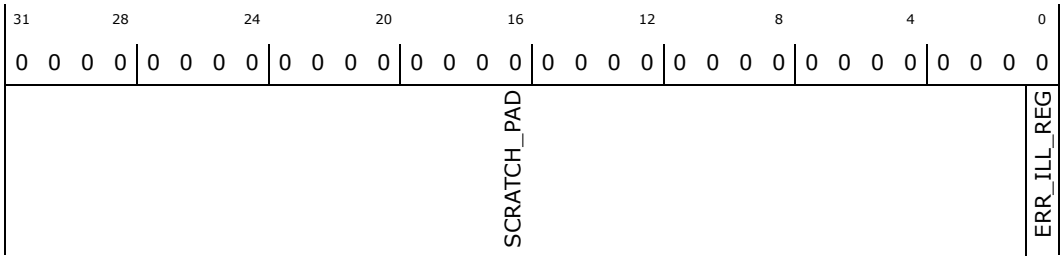
GLOBAL_CFG: GLOBAL DMA Configuration Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 9C000h] + 418h

Default: 00000000h

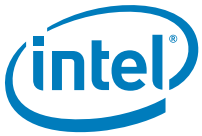


Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**SCRATCH_PAD:** This field will have all bits with R/W attribute to be used for future configuration and de-feature bits.
0	0x0 RW	**ERR_ILL_REG:** 0x1 : Issue ERR response on reading illegal (non-existing) registers 0x0 : Issue DVA response on reading illegal (non-existing) registers

8.3 LPE DMA 2 Memory Mapped I/O Registers

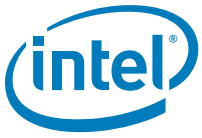
Table 54. Summary of DMA 2 Memory Mapped I/O Registers—lpe_bridge.BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"reg_SAR_type (SAR0)—Offset 0h" on page 3584	00000000h
8–Bh	4	"reg_DAR_type (DAR0)—Offset 8h" on page 3585	00000000h
10–13h	4	"reg_LLP_type (LLP0)—Offset 10h" on page 3586	00000000h
18–1Bh	4	"reg_CTL_LO_type (CTL_LO0)—Offset 18h" on page 3586	00000000h
1C–1Fh	4	"reg_CTL_HI_type (CTL_HI0)—Offset 1Ch" on page 3588	00000000h
20–23h	4	"reg_SSTAT_type (SSTAT0)—Offset 20h" on page 3590	00000000h
28–2Bh	4	"reg_DSTAT_type (DSTAT0)—Offset 28h" on page 3590	00000000h
30–33h	4	"reg_SSTATAR_type (SSTATAR0)—Offset 30h" on page 3591	00000000h
38–3Bh	4	"reg_DSTATAR_type (DSTATAR0)—Offset 38h" on page 3591	00000000h
40–43h	4	"reg_CFG_LO_type (CFG_LO0)—Offset 40h" on page 3592	00000203h
44–47h	4	"reg_CFG_HI_type (CFG_HI0)—Offset 44h" on page 3594	00000000h
48–4Bh	4	"reg_SGR_type (SGR0)—Offset 48h" on page 3595	00000000h
50–53h	4	"reg_DSR_type (DSR0)—Offset 50h" on page 3596	00000000h
58–5Bh	4	"reg_SAR_type (SAR1)—Offset 58h" on page 3596	00000000h
60–63h	4	"reg_DAR_type (DAR1)—Offset 60h" on page 3597	00000000h
68–6Bh	4	"reg_LLP_type (LLP1)—Offset 68h" on page 3598	00000000h
70–73h	4	"reg_CTL_LO_type (CTL_LO1)—Offset 70h" on page 3599	00000000h
74–77h	4	"reg_CTL_HI_type (CTL_HI1)—Offset 74h" on page 3601	00000000h
78–7Bh	4	"reg_SSTAT_type (SSTAT1)—Offset 78h" on page 3602	00000000h
80–83h	4	"reg_DSTAT_type (DSTAT1)—Offset 80h" on page 3603	00000000h
88–8Bh	4	"reg_SSTATAR_type (SSTATAR1)—Offset 88h" on page 3604	00000000h
90–93h	4	"reg_DSTATAR_type (DSTATAR1)—Offset 90h" on page 3604	00000000h
98–9Bh	4	"reg_CFG_LO_type (CFG_LO1)—Offset 98h" on page 3605	00000203h
9C–9Fh	4	"reg_CFG_HI_type (CFG_HI1)—Offset 9Ch" on page 3607	00000000h
A0–A3h	4	"reg_SGR_type (SGR1)—Offset A0h" on page 3608	00000000h
A8–ABh	4	"reg_DSR_type (DSR1)—Offset A8h" on page 3609	00000000h
B0–B3h	4	"reg_SAR_type (SAR2)—Offset B0h" on page 3609	00000000h
B8–BBh	4	"reg_DAR_type (DAR2)—Offset B8h" on page 3610	00000000h
C0–C3h	4	"reg_LLP_type (LLP2)—Offset C0h" on page 3611	00000000h
C8–CBh	4	"reg_CTL_LO_type (CTL_LO2)—Offset C8h" on page 3612	00000000h
CC–CFh	4	"reg_CTL_HI_type (CTL_HI2)—Offset CCh" on page 3614	00000000h
D0–D3h	4	"reg_SSTAT_type (SSTAT2)—Offset D0h" on page 3615	00000000h
D8–DBh	4	"reg_DSTAT_type (DSTAT2)—Offset D8h" on page 3616	00000000h
E0–E3h	4	"reg_SSTATAR_type (SSTATAR2)—Offset E0h" on page 3617	00000000h

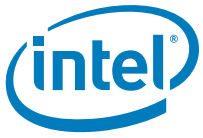


Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
E8–EBh	4	"reg_DSTATAR_type (DSTATAR2)—Offset E8h" on page 3617	00000000h
F0–F3h	4	"reg_CFG_LO_type (CFG_LO2)—Offset F0h" on page 3618	00000203h
F4–F7h	4	"reg_CFG_HI_type (CFG_HI2)—Offset F4h" on page 3620	00000000h
F8–FBh	4	"reg_SGR_type (SGR2)—Offset F8h" on page 3621	00000000h
100–103h	4	"reg_DSR_type (DSR2)—Offset 100h" on page 3622	00000000h
108–10Bh	4	"reg_SAR_type (SAR3)—Offset 108h" on page 3622	00000000h
110–113h	4	"reg_DAR_type (DAR3)—Offset 110h" on page 3623	00000000h
118–11Bh	4	"reg_LLP_type (LLP3)—Offset 118h" on page 3624	00000000h
120–123h	4	"reg_CTL_LO_type (CTL_LO3)—Offset 120h" on page 3625	00000000h
124–127h	4	"reg_CTL_HI_type (CTL_HI3)—Offset 124h" on page 3627	00000000h
128–12Bh	4	"reg_SSTAT_type (SSTAT3)—Offset 128h" on page 3628	00000000h
130–133h	4	"reg_DSTAT_type (DSTAT3)—Offset 130h" on page 3629	00000000h
138–13Bh	4	"reg_SSTATAR_type (SSTATAR3)—Offset 138h" on page 3630	00000000h
140–143h	4	"reg_DSTATAR_type (DSTATAR3)—Offset 140h" on page 3630	00000000h
148–14Bh	4	"reg_CFG_LO_type (CFG_LO3)—Offset 148h" on page 3631	00000203h
14C–14Fh	4	"reg_CFG_HI_type (CFG_HI3)—Offset 14Ch" on page 3633	00000000h
150–153h	4	"reg_SGR_type (SGR3)—Offset 150h" on page 3634	00000000h
158–15Bh	4	"reg_DSR_type (DSR3)—Offset 158h" on page 3635	00000000h
160–163h	4	"reg_SAR_type (SAR4)—Offset 160h" on page 3635	00000000h
168–16Bh	4	"reg_DAR_type (DAR4)—Offset 168h" on page 3636	00000000h
170–173h	4	"reg_LLP_type (LLP4)—Offset 170h" on page 3637	00000000h
178–17Bh	4	"reg_CTL_LO_type (CTL_LO4)—Offset 178h" on page 3638	00000000h
17C–17Fh	4	"reg_CTL_HI_type (CTL_HI4)—Offset 17Ch" on page 3640	00000000h
180–183h	4	"reg_SSTAT_type (SSTAT4)—Offset 180h" on page 3641	00000000h
188–18Bh	4	"reg_DSTAT_type (DSTAT4)—Offset 188h" on page 3642	00000000h
190–193h	4	"reg_SSTATAR_type (SSTATAR4)—Offset 190h" on page 3643	00000000h
198–19Bh	4	"reg_DSTATAR_type (DSTATAR4)—Offset 198h" on page 3643	00000000h
1A0–1A3h	4	"reg_CFG_LO_type (CFG_LO4)—Offset 1A0h" on page 3644	00000203h
1A4–1A7h	4	"reg_CFG_HI_type (CFG_HI4)—Offset 1A4h" on page 3646	00000000h
1A8–1ABh	4	"reg_SGR_type (SGR4)—Offset 1A8h" on page 3647	00000000h
1B0–1B3h	4	"reg_DSR_type (DSR4)—Offset 1B0h" on page 3648	00000000h
1B8–1BBh	4	"reg_SAR_type (SAR5)—Offset 1B8h" on page 3648	00000000h
1C0–1C3h	4	"reg_DAR_type (DAR5)—Offset 1C0h" on page 3649	00000000h
1C8–1CBh	4	"reg_LLP_type (LLP5)—Offset 1C8h" on page 3650	00000000h
1D0–1D3h	4	"reg_CTL_LO_type (CTL_LO5)—Offset 1D0h" on page 3651	00000000h
1D4–1D7h	4	"reg_CTL_HI_type (CTL_HI5)—Offset 1D4h" on page 3653	00000000h
1D8–1DBh	4	"reg_SSTAT_type (SSTAT5)—Offset 1D8h" on page 3654	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1E0–1E3h	4	"reg_DSTAT_type (DSTAT5)—Offset 1E0h" on page 3655	00000000h
1E8–1EBh	4	"reg_SSTATAR_type (SSTATAR5)—Offset 1E8h" on page 3656	00000000h
1F0–1F3h	4	"reg_DSTATAR_type (DSTATAR5)—Offset 1F0h" on page 3656	00000000h
1F8–1FBh	4	"reg_CFG_LO_type (CFG_LO5)—Offset 1F8h" on page 3657	00000203h
1FC–1FFh	4	"reg_CFG_HI_type (CFG_HI5)—Offset 1FCh" on page 3659	00000000h
200–203h	4	"reg_SGR_type (SGR5)—Offset 200h" on page 3660	00000000h
208–20Bh	4	"reg_DSR_type (DSR5)—Offset 208h" on page 3661	00000000h
210–213h	4	"reg_SAR_type (SAR6)—Offset 210h" on page 3661	00000000h
218–21Bh	4	"reg_DAR_type (DAR6)—Offset 218h" on page 3662	00000000h
220–223h	4	"reg_LLP_type (LLP6)—Offset 220h" on page 3663	00000000h
228–22Bh	4	"reg_CTL_LO_type (CTL_LO6)—Offset 228h" on page 3664	00000000h
22C–22Fh	4	"reg_CTL_HI_type (CTL_HI6)—Offset 22Ch" on page 3666	00000000h
230–233h	4	"reg_SSTAT_type (SSTAT6)—Offset 230h" on page 3667	00000000h
238–23Bh	4	"reg_DSTAT_type (DSTAT6)—Offset 238h" on page 3668	00000000h
240–243h	4	"reg_SSTATAR_type (SSTATAR6)—Offset 240h" on page 3669	00000000h
248–24Bh	4	"reg_DSTATAR_type (DSTATAR6)—Offset 248h" on page 3669	00000000h
250–253h	4	"reg_CFG_LO_type (CFG_LO6)—Offset 250h" on page 3670	00000203h
254–257h	4	"reg_CFG_HI_type (CFG_HI6)—Offset 254h" on page 3672	00000000h
258–25Bh	4	"reg_SGR_type (SGR6)—Offset 258h" on page 3673	00000000h
260–263h	4	"reg_DSR_type (DSR6)—Offset 260h" on page 3674	00000000h
268–26Bh	4	"reg_SAR_type (SAR7)—Offset 268h" on page 3674	00000000h
270–273h	4	"reg_DAR_type (DAR7)—Offset 270h" on page 3675	00000000h
278–27Bh	4	"reg_LLP_type (LLP7)—Offset 278h" on page 3676	00000000h
280–283h	4	"reg_CTL_LO_type (CTL_LO7)—Offset 280h" on page 3677	00000000h
284–287h	4	"reg_CTL_HI_type (CTL_HI7)—Offset 284h" on page 3679	00000000h
288–28Bh	4	"reg_SSTAT_type (SSTAT7)—Offset 288h" on page 3680	00000000h
290–293h	4	"reg_DSTAT_type (DSTAT7)—Offset 290h" on page 3681	00000000h
298–29Bh	4	"reg_SSTATAR_type (SSTATAR7)—Offset 298h" on page 3682	00000000h
2A0–2A3h	4	"reg_DSTATAR_type (DSTATAR7)—Offset 2A0h" on page 3682	00000000h
2A8–2ABh	4	"reg_CFG_LO_type (CFG_LO7)—Offset 2A8h" on page 3683	00000203h
2AC–2AFh	4	"reg_CFG_HI_type (CFG_HI7)—Offset 2ACh" on page 3685	00000000h
2B0–2B3h	4	"reg_SGR_type (SGR7)—Offset 2B0h" on page 3686	00000000h
2B8–2BBh	4	"reg_DSR_type (DSR7)—Offset 2B8h" on page 3687	00000000h
2C0–2C3h	4	"reg_Raw_type (RawTfr)—Offset 2C0h" on page 3687	00000000h
2C8–2CBh	4	"reg_Raw_type (RawBlock)—Offset 2C8h" on page 3688	00000000h
2D0–2D3h	4	"reg_Raw_type (RawSrcTran)—Offset 2D0h" on page 3688	00000000h
2D8–2DBh	4	"reg_Raw_type (RawDstTran)—Offset 2D8h" on page 3689	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2E0–2E3h	4	"reg_Raw_type (RawErr)—Offset 2E0h" on page 3690	00000000h
2E8–2EBh	4	"reg_Status_type (StatusTfr)—Offset 2E8h" on page 3690	00000000h
2F0–2F3h	4	"reg_Status_type (StatusBlock)—Offset 2F0h" on page 3691	00000000h
2F8–2FBh	4	"reg_Status_type (StatusSrcTran)—Offset 2F8h" on page 3692	00000000h
300–303h	4	"reg_Status_type (StatusDstTran)—Offset 300h" on page 3692	00000000h
308–30Bh	4	"reg_Status_type (StatusErr)—Offset 308h" on page 3693	00000000h
310–313h	4	"reg_Mask_type (MaskTfr)—Offset 310h" on page 3693	00000000h
318–31Bh	4	"reg_Mask_type (MaskBlock)—Offset 318h" on page 3694	00000000h
320–323h	4	"reg_Mask_type (MaskSrcTran)—Offset 320h" on page 3695	00000000h
328–32Bh	4	"reg_Mask_type (MaskDstTran)—Offset 328h" on page 3696	00000000h
330–333h	4	"reg_Mask_type (MaskErr)—Offset 330h" on page 3697	00000000h
338–33Bh	4	"reg_Clear_type (ClearTfr)—Offset 338h" on page 3698	00000000h
340–343h	4	"reg_Clear_type (ClearBlock)—Offset 340h" on page 3699	00000000h
348–34Bh	4	"reg_Clear_type (ClearSrcTran)—Offset 348h" on page 3699	00000000h
350–353h	4	"reg_Clear_type (ClearDstTran)—Offset 350h" on page 3700	00000000h
358–35Bh	4	"reg_Clear_type (ClearErr)—Offset 358h" on page 3700	00000000h
360–363h	4	"reg_StatusInt_type (StatusInt)—Offset 360h" on page 3701	00000000h
398–39Bh	4	"reg_DmaCfgReg_type (DmaCfgReg)—Offset 398h" on page 3702	00000000h
3A0–3A3h	4	"reg_ChEnReg_type (ChEnReg)—Offset 3A0h" on page 3702	00000000h
3B8–3BBh	4	"reg_CLASS_PRIORITY0_LO_type (ClassPriority0_LO)—Offset 3B8h" on page 3703	00000000h
3BC–3BFh	4	"reg_CLASS_PRIORITY0_HI_type (ClassPriority0_HI)—Offset 3BCh" on page 3704	00000000h
3C0–3C3h	4	"reg_CLASS_PRIORITY1_LO_type (ClassPriority1_LO)—Offset 3C0h" on page 3704	00000000h
3C4–3C7h	4	"reg_CLASS_PRIORITY1_HI_type (ClassPriority1_HI)—Offset 3C4h" on page 3705	00000000h
400–403h	4	"reg_FIFO_PARTITION0_LO_type (FifoPartition0_LO)—Offset 400h" on page 3705	00000000h
404–407h	4	"reg_FIFO_PARTITION0_HI_type (FifoPartition0_HI)—Offset 404h" on page 3706	00000000h
408–40Bh	4	"reg_FIFO_PARTITION1_LO_type (FifoPartition1_LO)—Offset 408h" on page 3707	00000000h
40C–40Fh	4	"reg_FIFO_PARTITION1_HI_type (FifoPartition1_HI)—Offset 40Ch" on page 3707	00000000h
410–413h	4	"reg_SAI_Error_type (SAI_ERR)—Offset 410h" on page 3708	00000000h
418–41Bh	4	"reg_GLOBAL_CFG_type (GLOBAL_CFG)—Offset 418h" on page 3708	00000000h



8.3.1 reg_SAR_type (SAR0)—Offset 0h

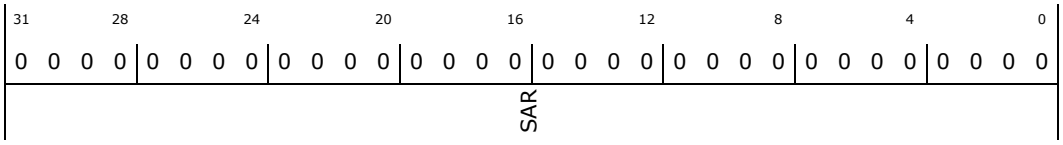
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.3.2 reg_DAR_type (DAR0)—Offset 8h

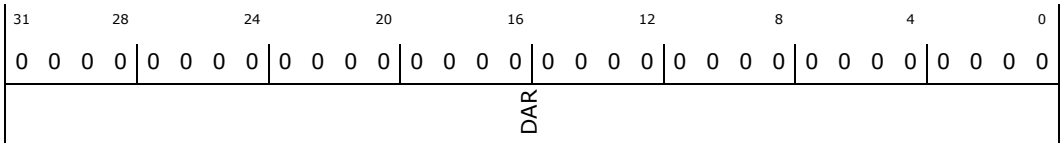
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

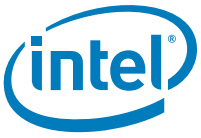
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported



8.3.3 reg_LLP_type (LLP0)—Offset 10h

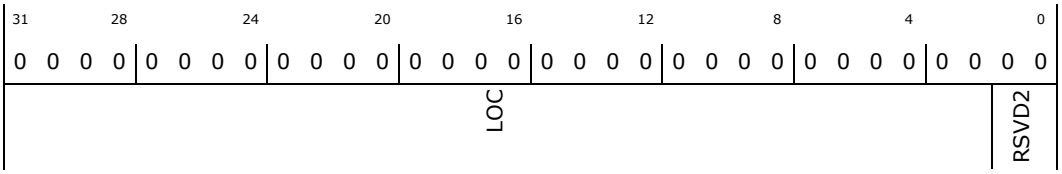
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.3.4 reg_CTL_LO_type (CTL_LO0)—Offset 18h

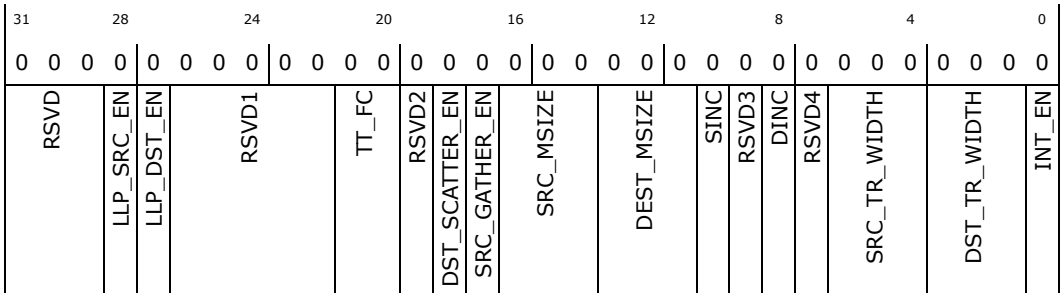
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 18h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.3.5 reg_CTL_HI_type (CTL_HI0)—Offset 1Ch

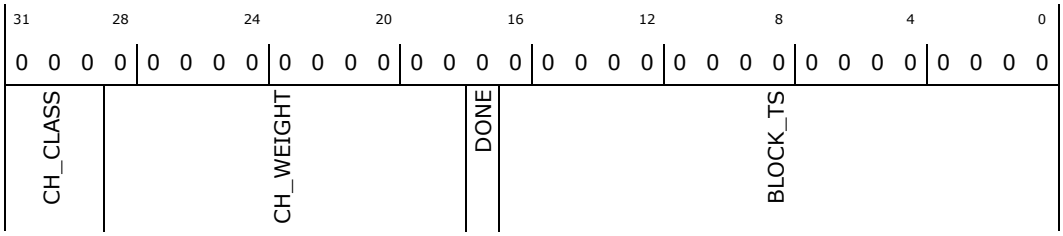
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 1Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.3.6 reg_SSTAT_type (SSTAT0)—Offset 20h

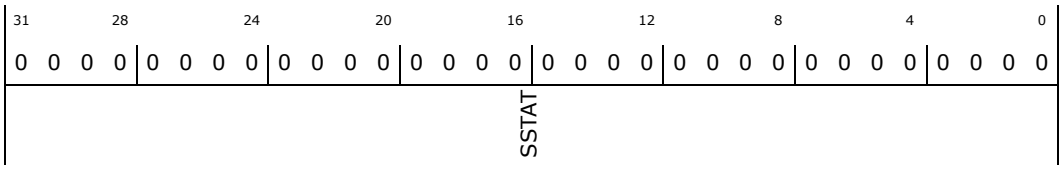
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 20h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.3.7 reg_DSTAT_type (DSTAT0)—Offset 28h

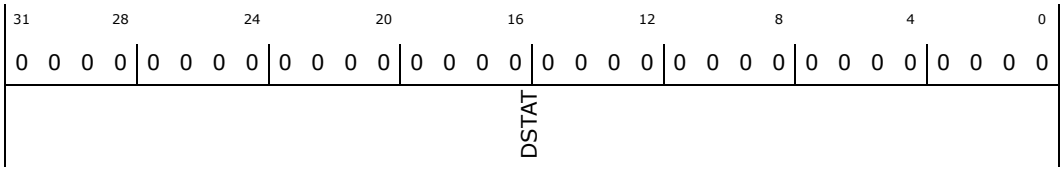
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 28h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.3.8 reg_SSTATAR_type (SSTATAR0)—Offset 30h

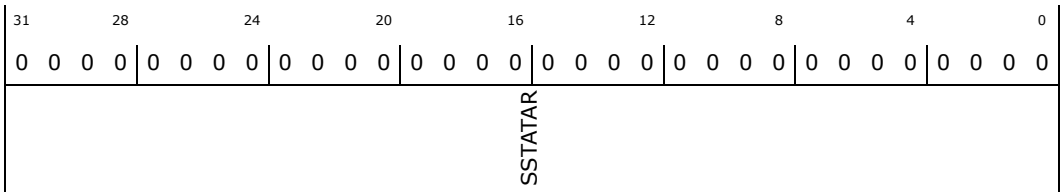
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.3.9 reg_DSTATAR_type (DSTATAR0)—Offset 38h

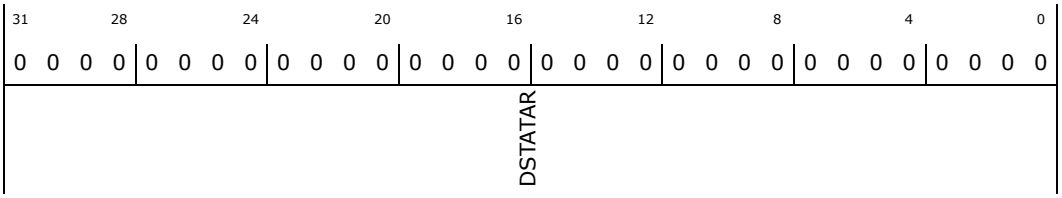
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 38h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.3.10 reg_CFG_LO_type (CFG_LO0)—Offset 40h

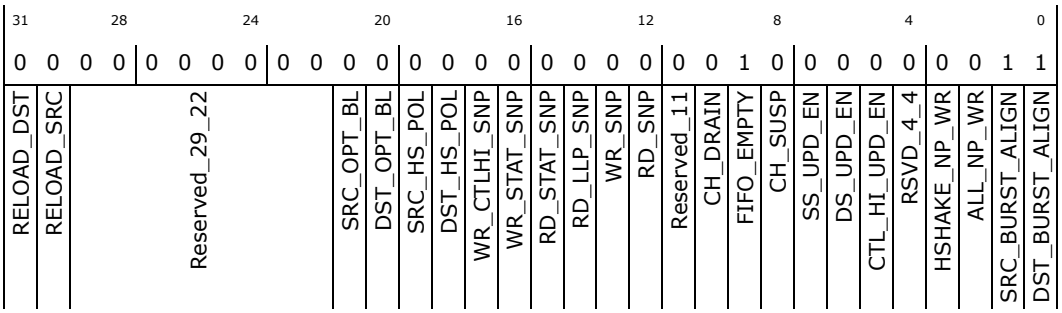
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 40h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled

Bit Range	Default & Access	Field Name (ID): Description
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.3.11 reg_CFG_HI_type (CFG_HI0)—Offset 44h

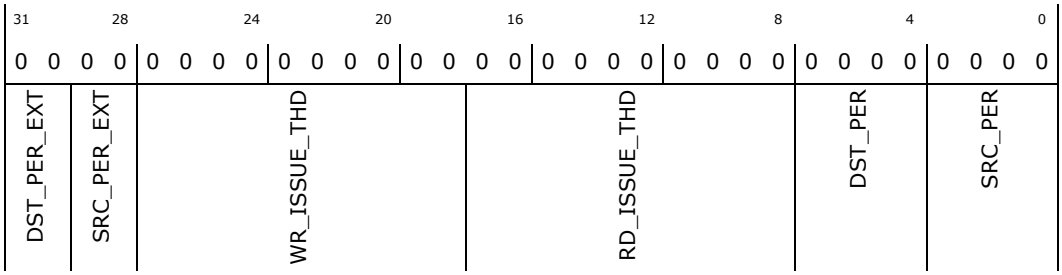
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 44h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.

Bit Range	Default & Access	Field Name (ID): Description
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.3.12 reg_SGR_type (SGR0)—Offset 48h

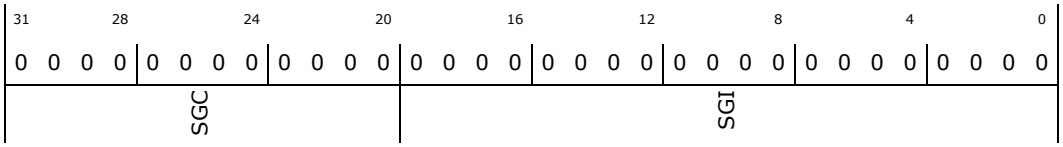
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 48h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.3.13 reg_DSR_type (DSR0)—Offset 50h

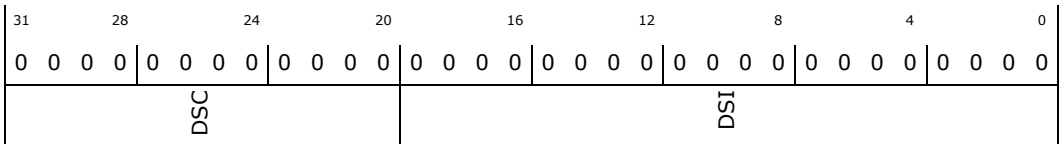
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 50h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.3.14 reg_SAR_type (SAR1)—Offset 58h

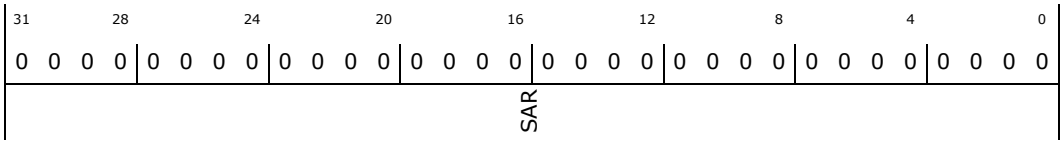
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 58h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.3.15 reg_DAR_type (DAR1)—Offset 60h

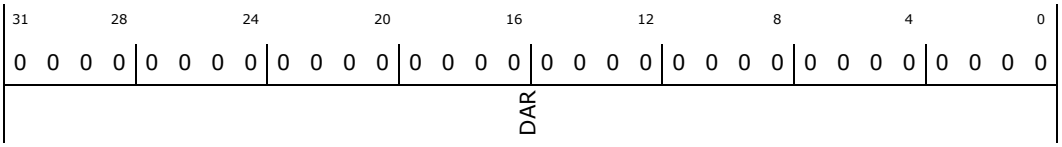
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 60h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.3.16 reg_LLP_type (LLP1)—Offset 68h

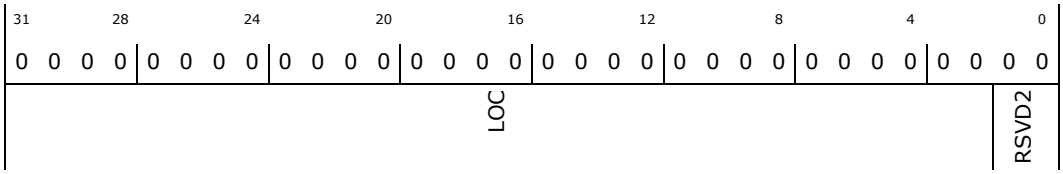
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 68h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.3.17 reg_CTL_LO_type (CTL_LO1)—Offset 70h

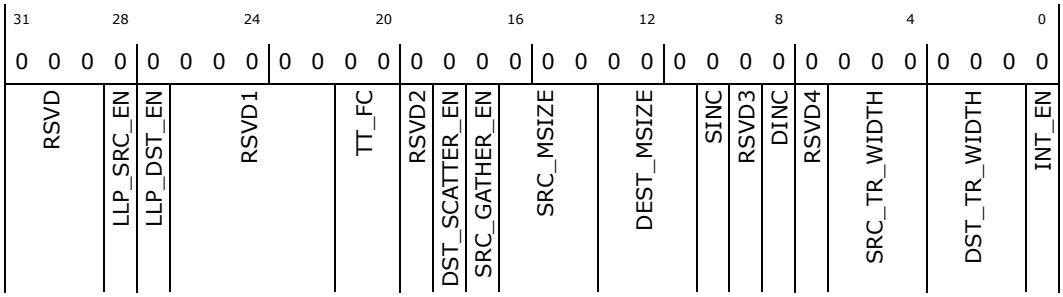
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

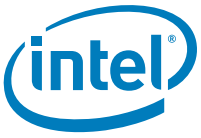
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 70h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)



Bit Range	Default & Access	Field Name (ID): Description
26:22	0x0 RO	**RSVD1:** RSVD
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.3.18 reg_CTL_HI_type (CTL_HI1)—Offset 74h

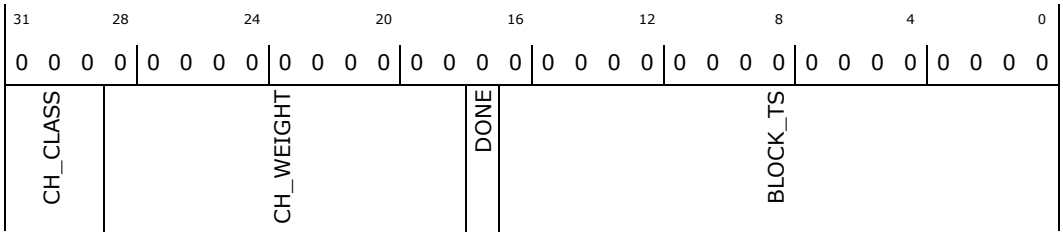
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 74h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.3.19 reg_SSTAT_type (SSTAT1)—Offset 78h

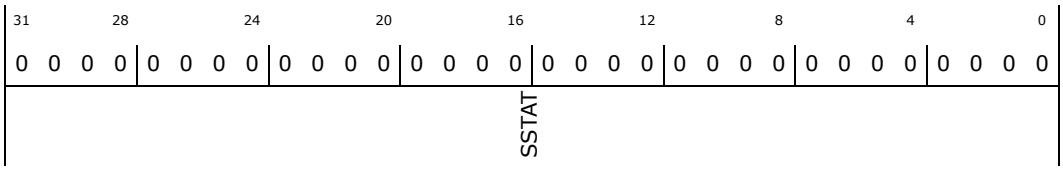
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 78h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.3.20 reg_DSTAT_type (DSTAT1)—Offset 80h

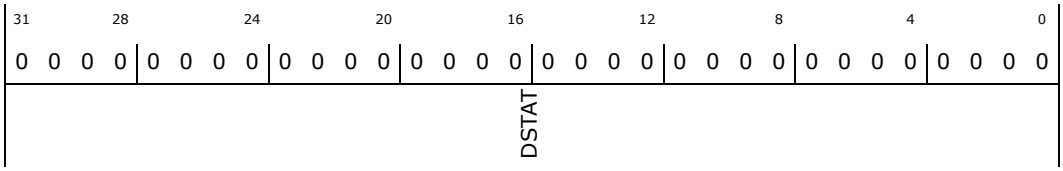
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 80h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.3.21 reg_SSTATAR_type (SSTATAR1)—Offset 88h

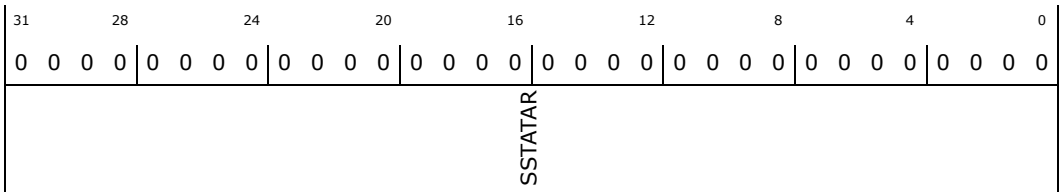
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 88h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.3.22 reg_DSTATAR_type (DSTATAR1)—Offset 90h

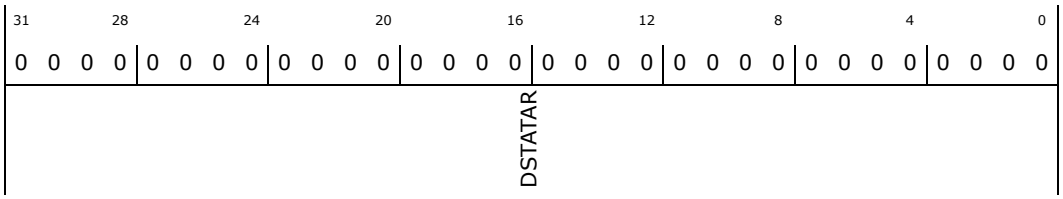
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 90h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.3.23 reg_CFG_LO_type (CFG_LO1)—Offset 98h

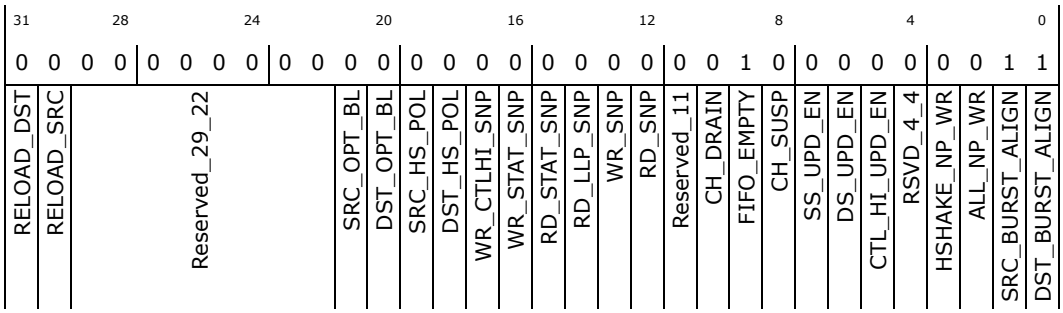
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 98h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.3.24 reg_CFG_HI_type (CFG_HI1)—Offset 9Ch

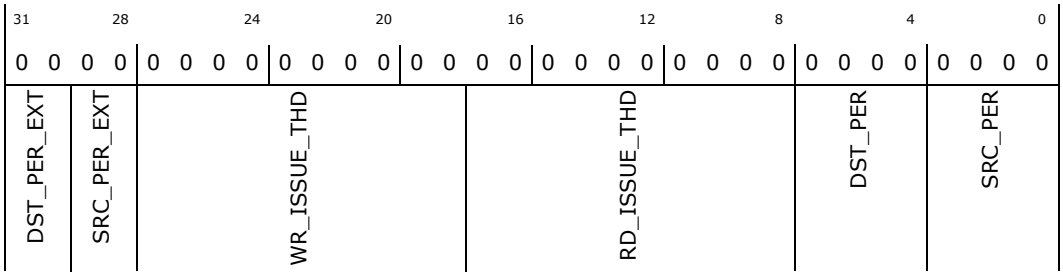
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 9Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.3.25 reg_SGR_type (SGR1)—Offset A0h

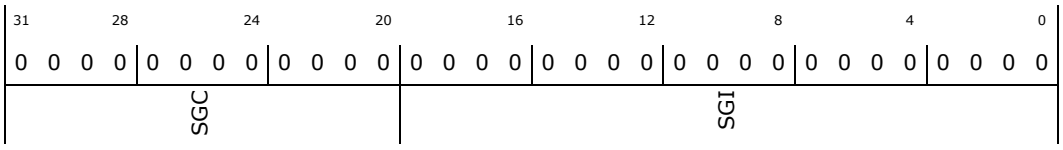
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.3.26 reg_DSR_type (DSR1)—Offset A8h

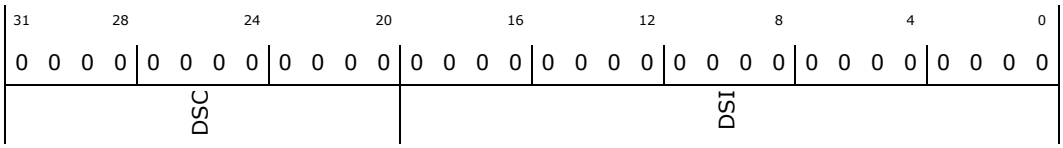
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.3.27 reg_SAR_type (SAR2)—Offset B0h

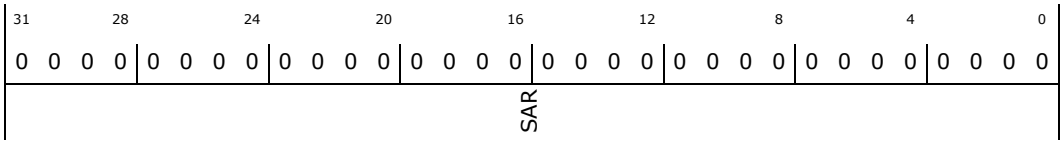
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.3.28 reg_DAR_type (DAR2)—Offset B8h

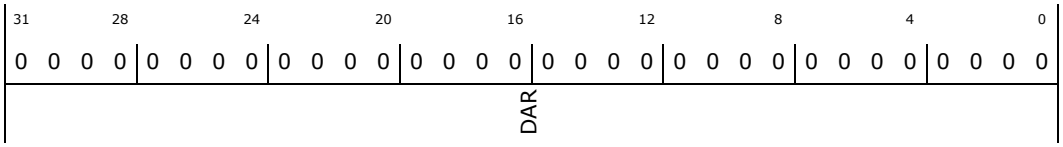
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.3.29 reg_LLP_type (LLP2)—Offset C0h

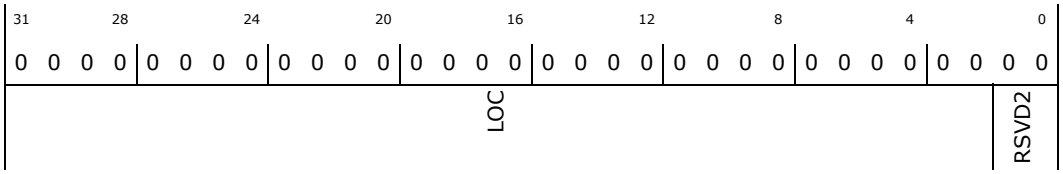
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.3.30 reg_CTL_LO_type (CTL_LO2)—Offset C8h

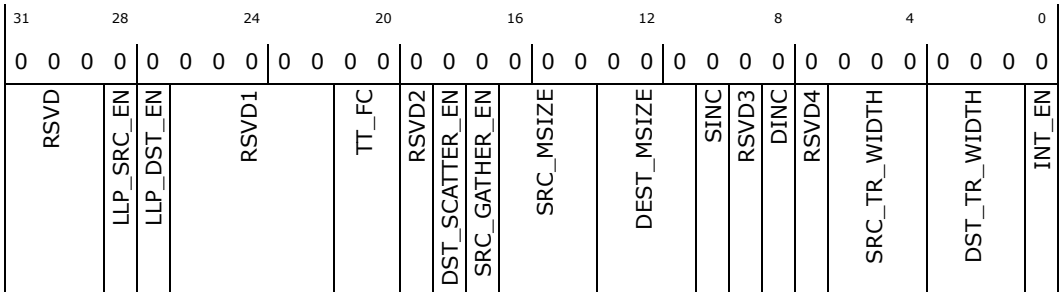
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + C8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.3.31 reg_CTL_HI_type (CTL_HI2)—Offset CCh

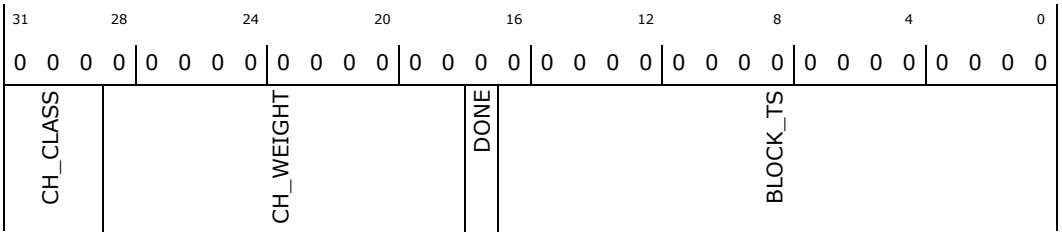
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + CCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.3.32 reg_SSTAT_type (SSTAT2)—Offset D0h

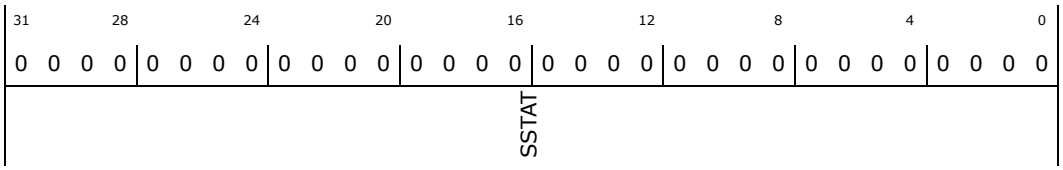
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.3.33 reg_DSTAT_type (DSTAT2)—Offset D8h

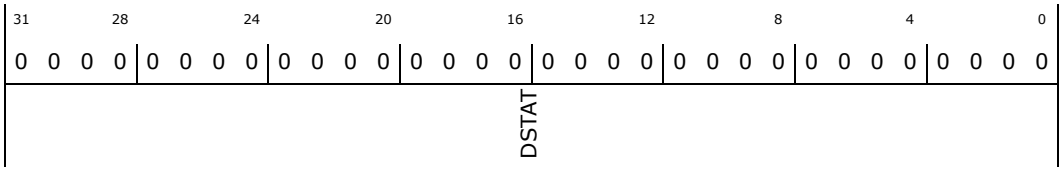
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + D8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.3.34 reg_SSTATAR_type (SSTATAR2)—Offset E0h

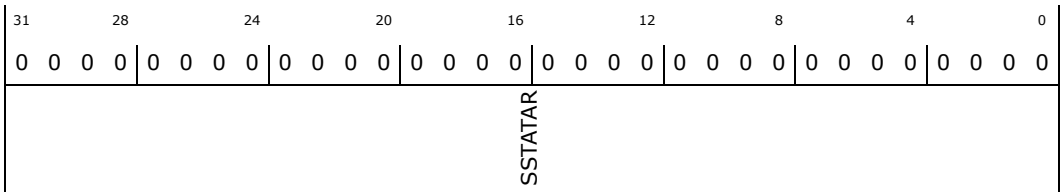
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + E0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.3.35 reg_DSTATAR_type (DSTATAR2)—Offset E8h

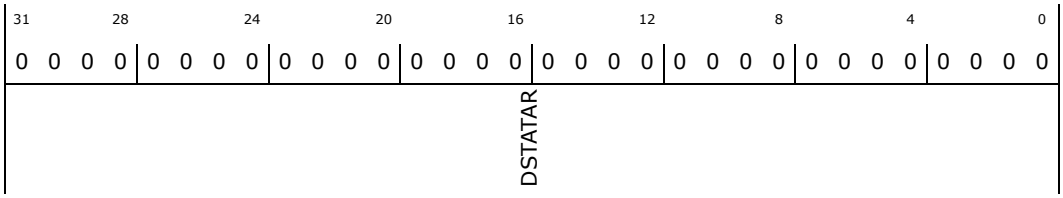
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + E8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.3.36 reg_CFG_LO_type (CFG_LO2)—Offset F0h

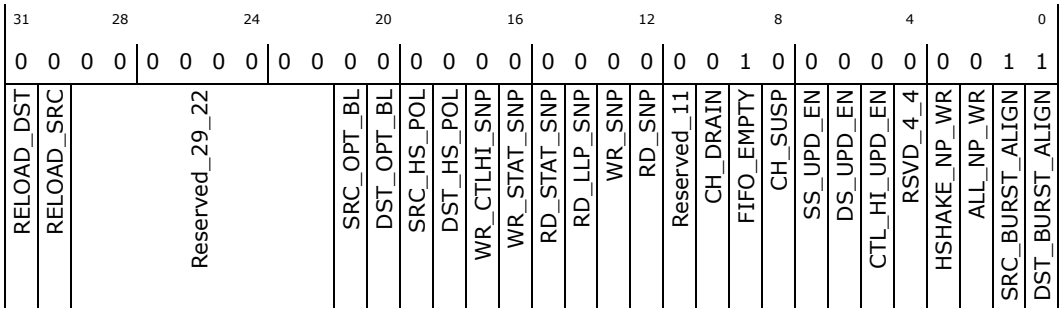
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + F0h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.3.37 reg_CFG_HI_type (CFG_HI2)—Offset F4h

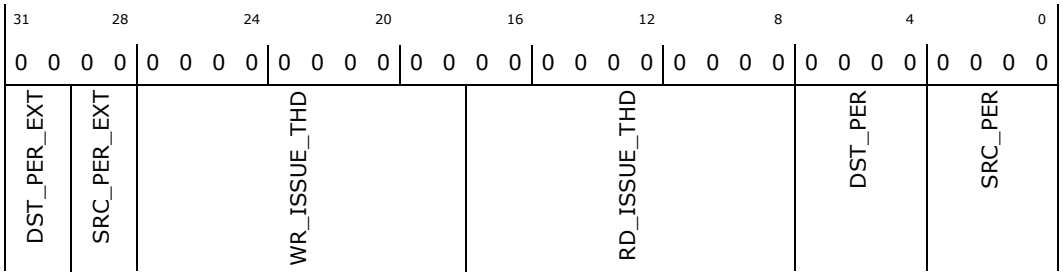
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + F4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.3.38 reg_SGR_type (SGR2)—Offset F8h

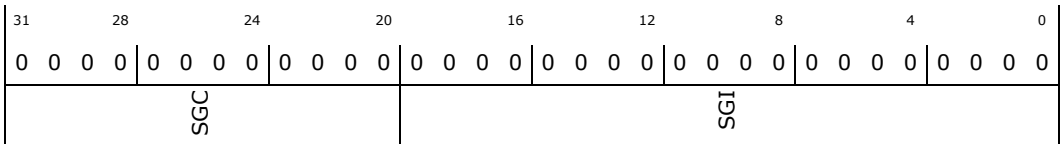
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.3.39 reg_DSR_type (DSR2)—Offset 100h

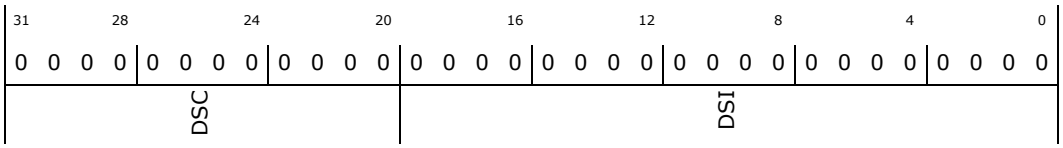
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 100h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.3.40 reg_SAR_type (SAR3)—Offset 108h

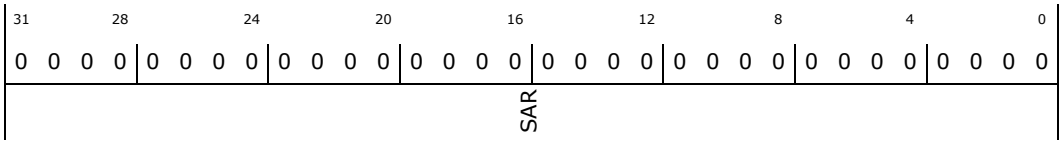
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 108h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.3.41 reg_DAR_type (DAR3)—Offset 110h

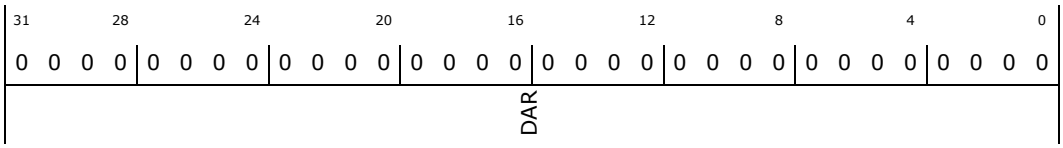
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 110h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.3.42 reg_LLP_type (LLP3)—Offset 118h

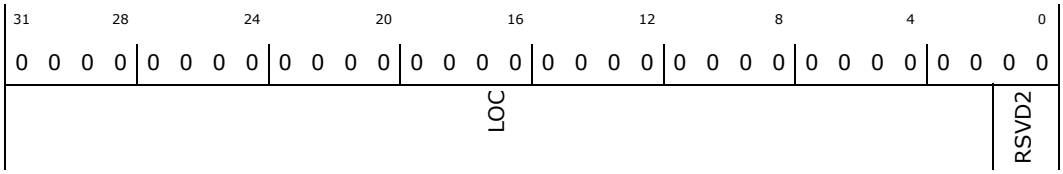
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 118h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.3.43 reg_CTL_LO_type (CTL_LO3)—Offset 120h

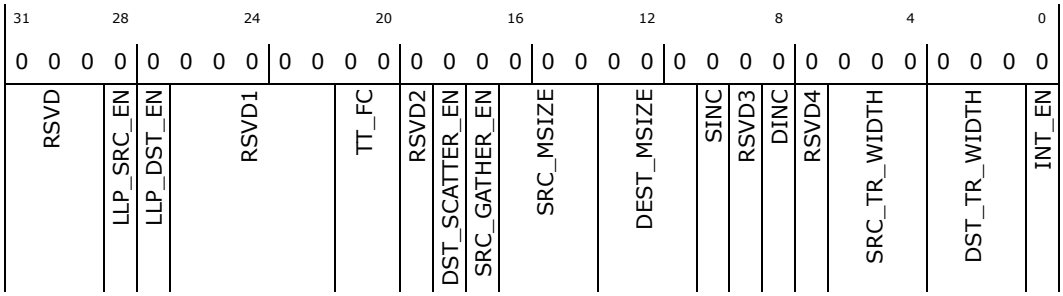
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 120h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.3.44 reg_CTL_HI_type (CTL_HI3)—Offset 124h

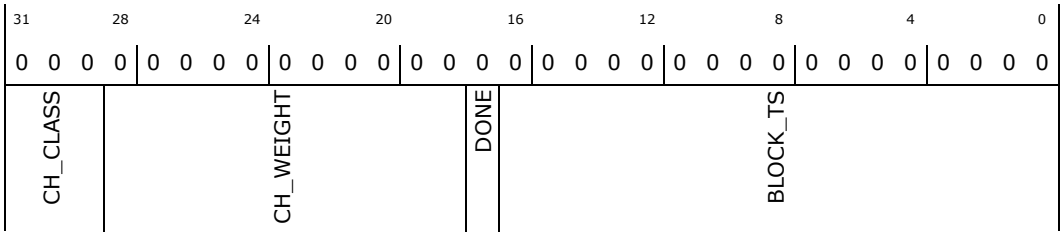
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

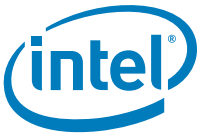
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 124h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below



Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.3.45 reg_SSTAT_type (SSTAT3)—Offset 128h

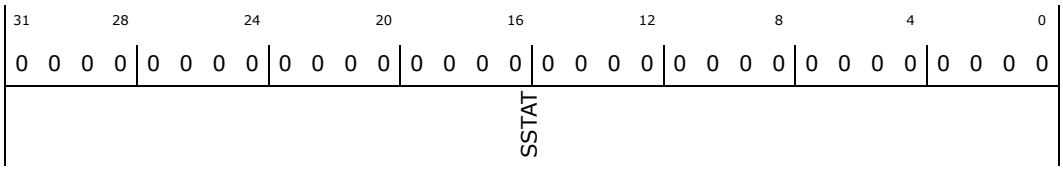
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 128h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.3.46 reg_DSTAT_type (DSTAT3)—Offset 130h

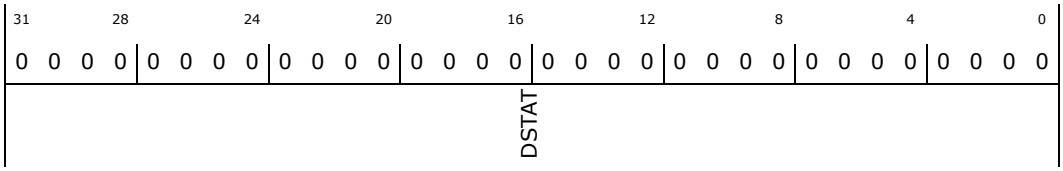
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 130h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.3.47 reg_SSTATAR_type (SSTATAR3)—Offset 138h

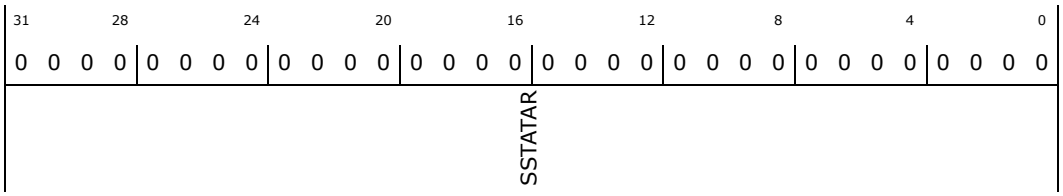
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 138h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.3.48 reg_DSTATAR_type (DSTATAR3)—Offset 140h

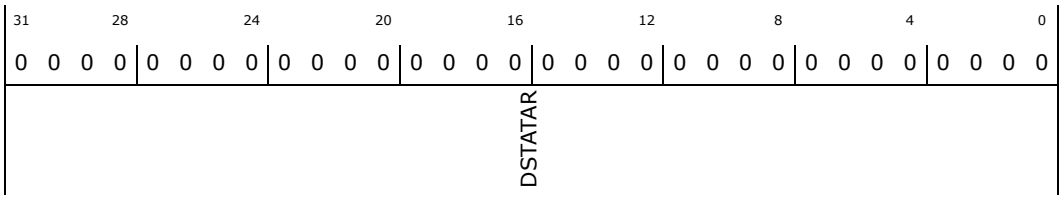
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 140h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.3.49 reg_CFG_LO_type (CFG_LO3)—Offset 148h

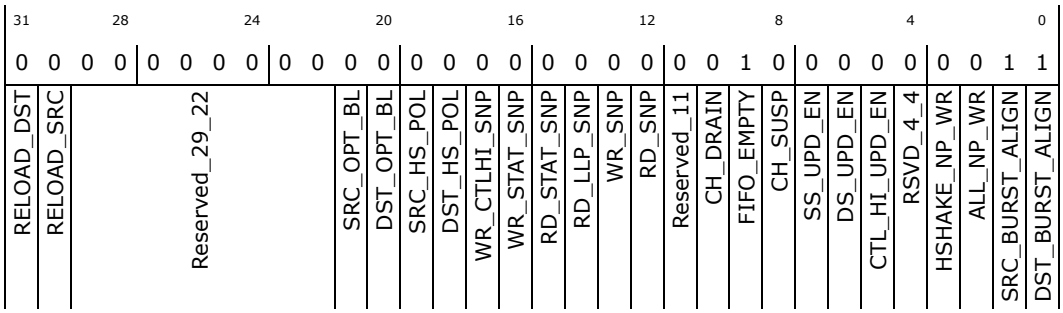
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 148h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.3.50 reg_CFG_HI_type (CFG_HI3)—Offset 14Ch

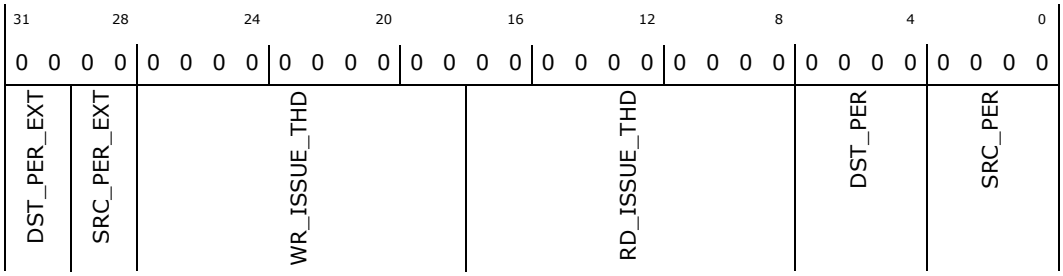
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 14Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.3.51 reg_SGR_type (SGR3)—Offset 150h

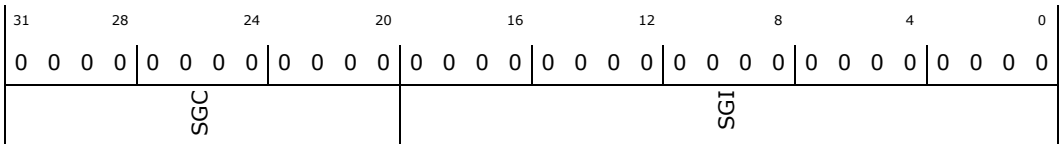
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 150h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.3.52 reg_DSR_type (DSR3)—Offset 158h

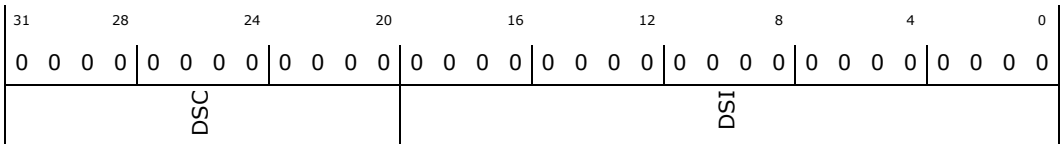
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 158h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.3.53 reg_SAR_type (SAR4)—Offset 160h

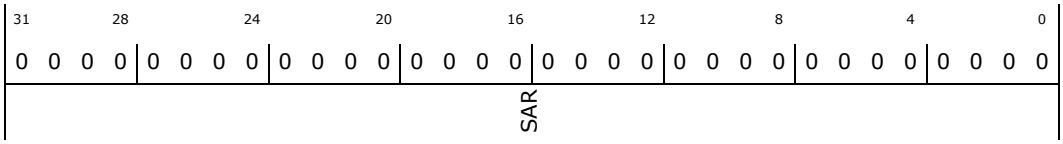
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 160h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.3.54 reg_DAR_type (DAR4)—Offset 168h

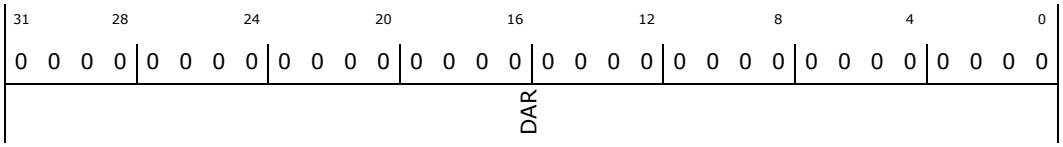
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 168h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.3.55 reg_LLP_type (LLP4)—Offset 170h

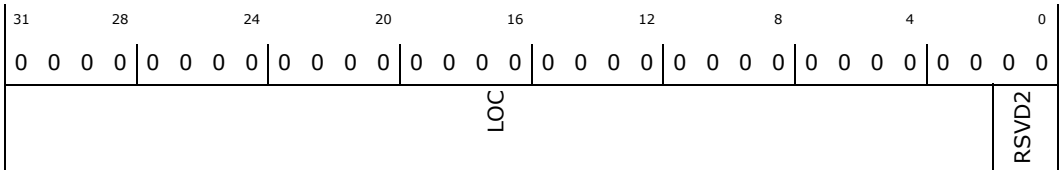
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 170h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.3.56 reg_CTL_LO_type (CTL_LO4)—Offset 178h

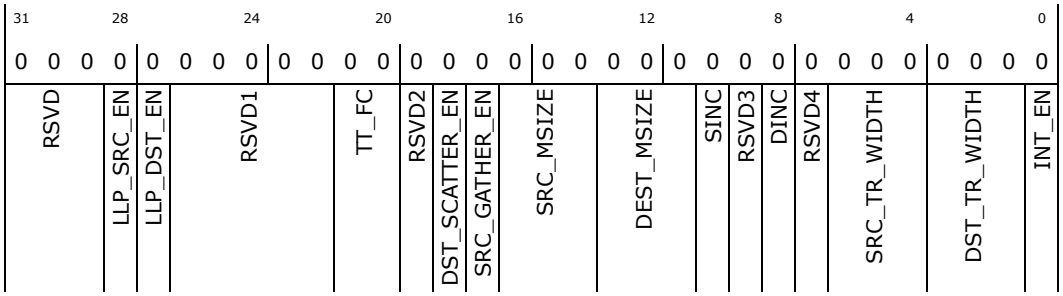
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 178h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.3.57 reg_CTL_HI_type (CTL_HI4)—Offset 17Ch

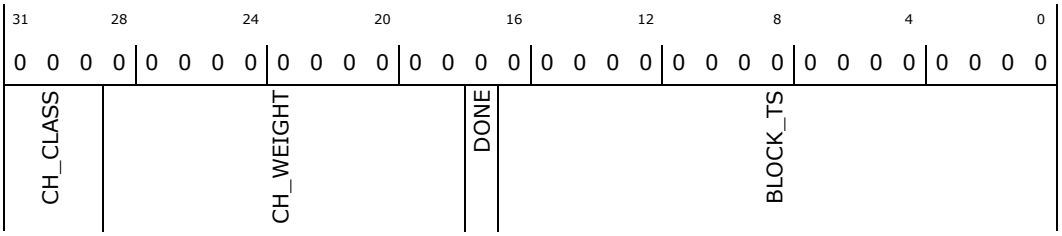
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 17Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.3.58 reg_SSTAT_type (SSTAT4)—Offset 180h

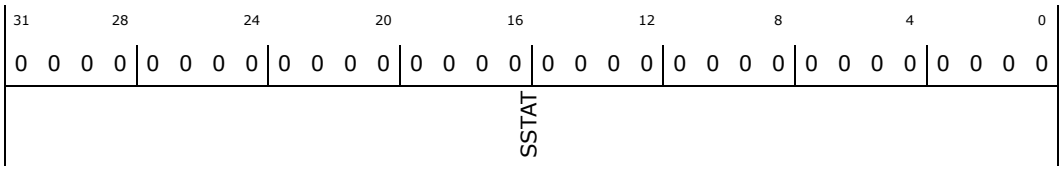
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 180h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.3.59 reg_DSTAT_type (DSTAT4)—Offset 188h

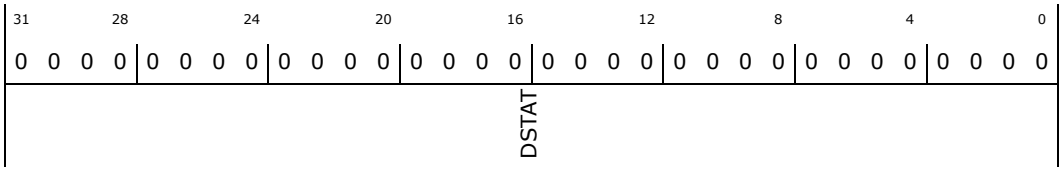
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 188h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.3.60 reg_SSTATAR_type (SSTATAR4)—Offset 190h

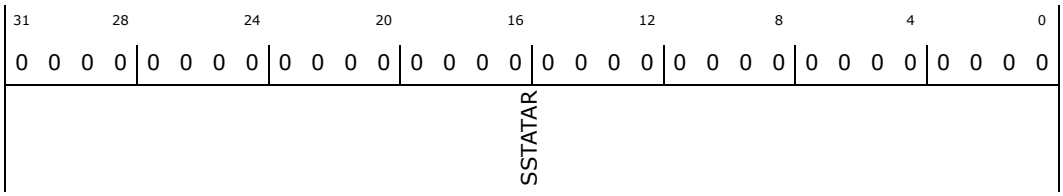
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 190h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.3.61 reg_DSTATAR_type (DSTATAR4)—Offset 198h

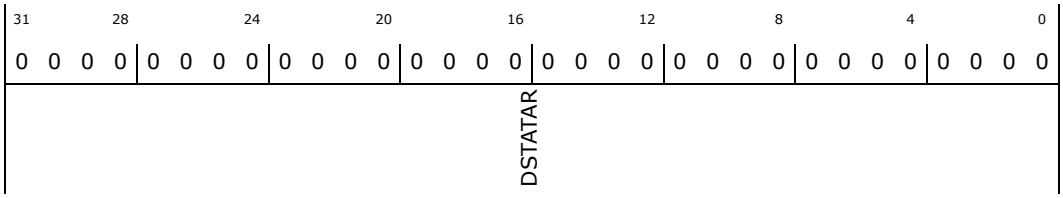
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 198h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.3.62 reg_CFG_LO_type (CFG_LO4)—Offset 1A0h

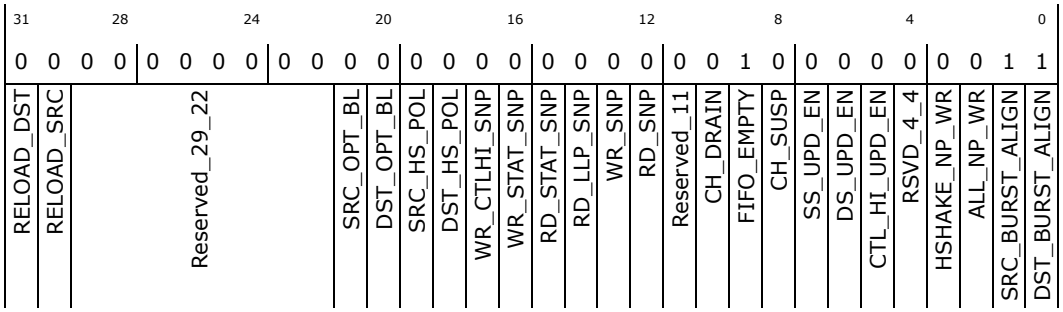
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 1A0h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.3.63 reg_CFG_HI_type (CFG_HI4)—Offset 1A4h

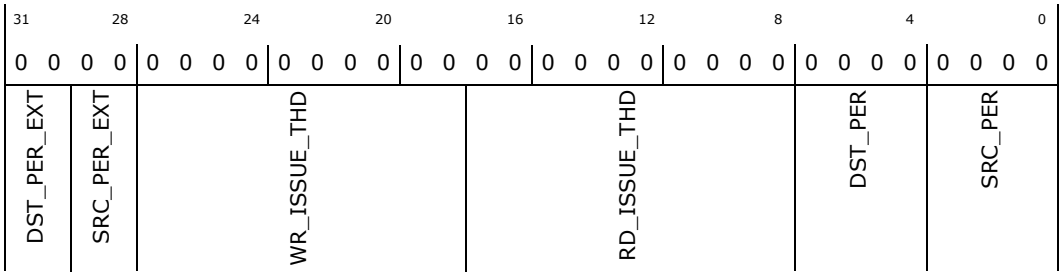
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 1A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.3.64 reg_SGR_type (SGR4)—Offset 1A8h

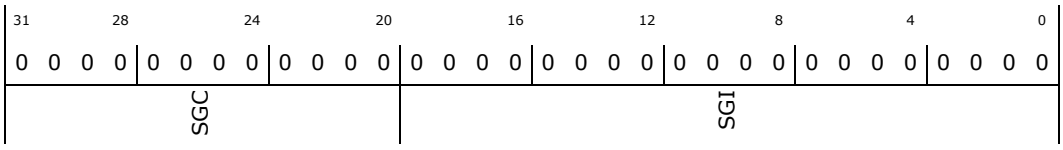
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 1A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.3.65 reg_DSR_type (DSR4)—Offset 1B0h

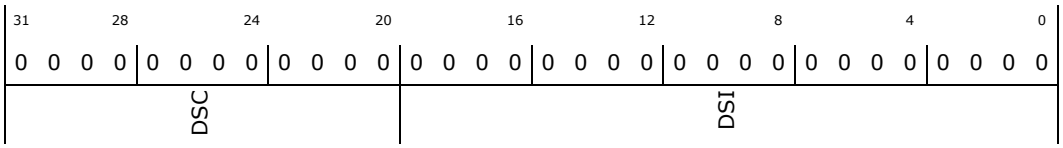
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 1B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.3.66 reg_SAR_type (SAR5)—Offset 1B8h

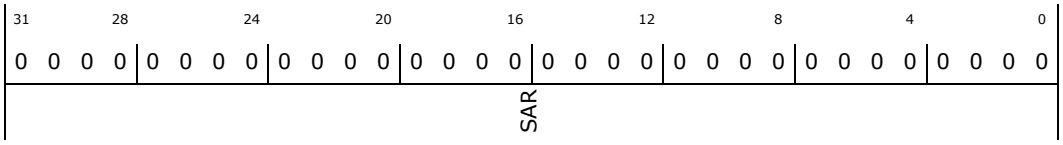
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 1B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.3.67 reg_DAR_type (DAR5)—Offset 1C0h

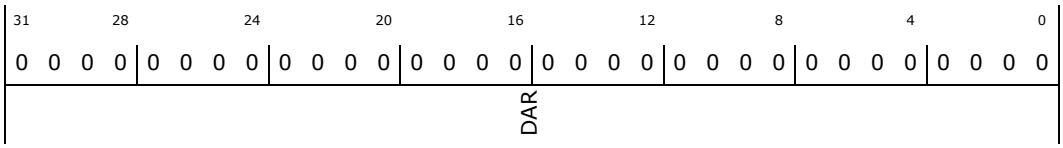
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 1C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.3.68 reg_LLP_type (LLP5)—Offset 1C8h

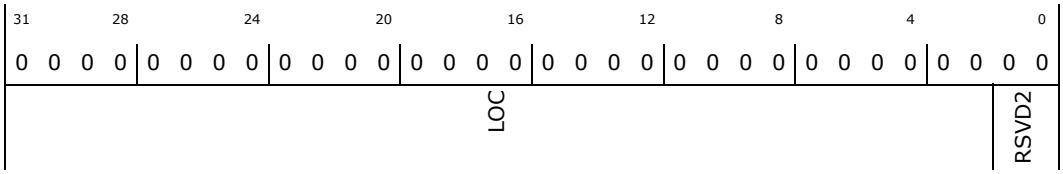
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 1C8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.3.69 reg_CTL_LO_type (CTL_LO5)—Offset 1D0h

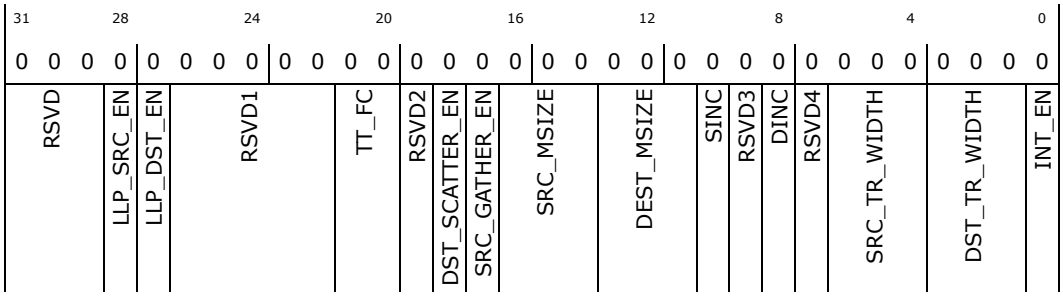
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 1D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.3.70 reg_CTL_HI_type (CTL_HI5)—Offset 1D4h

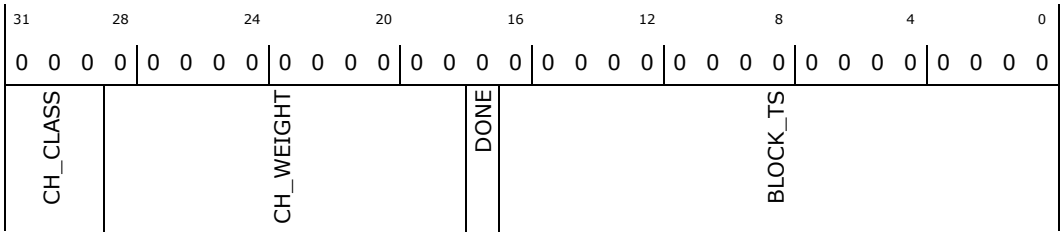
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 1D4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.3.71 reg_SSTAT_type (SSTAT5)—Offset 1D8h

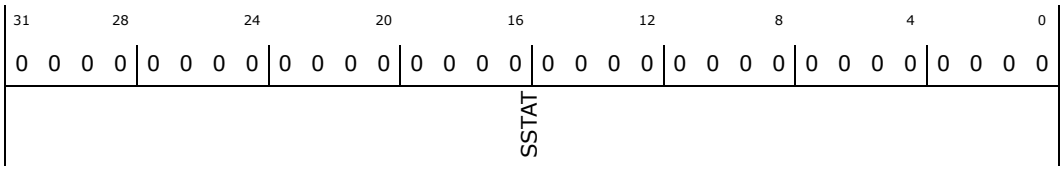
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 1D8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.3.72 reg_DSTAT_type (DSTAT5)—Offset 1E0h

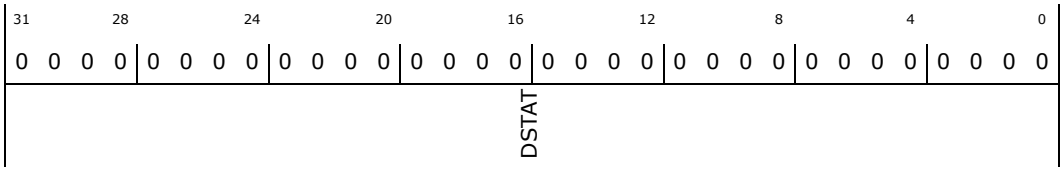
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 1E0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.3.73 reg_SSTATAR_type (SSTATAR5)—Offset 1E8h

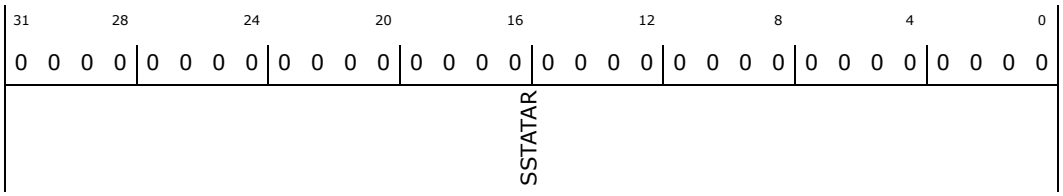
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 1E8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.3.74 reg_DSTATAR_type (DSTATAR5)—Offset 1F0h

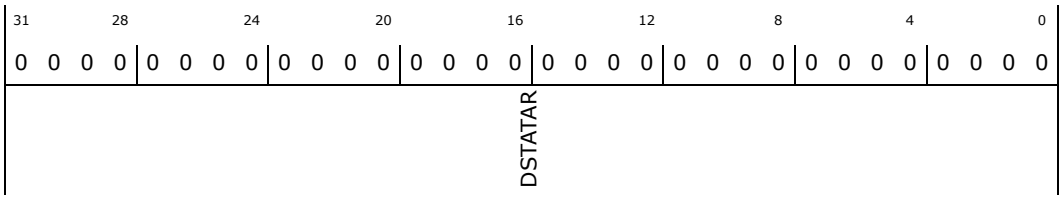
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 1F0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.3.75 reg_CFG_LO_type (CFG_LO5)—Offset 1F8h

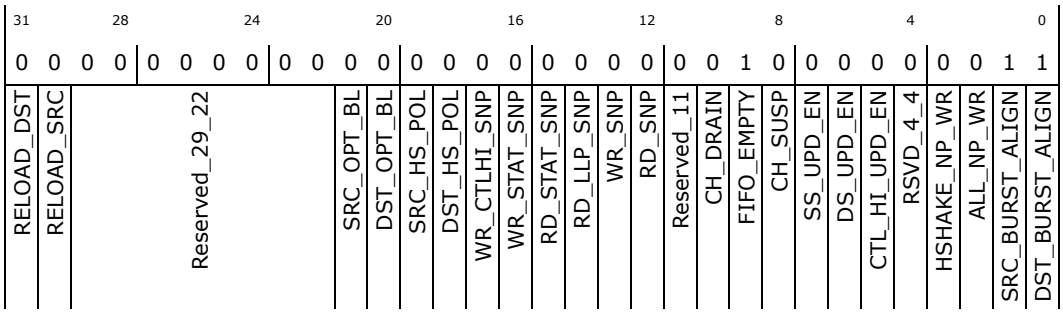
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 1F8h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.3.76 reg_CFG_HI_type (CFG_HI5)—Offset 1FCh

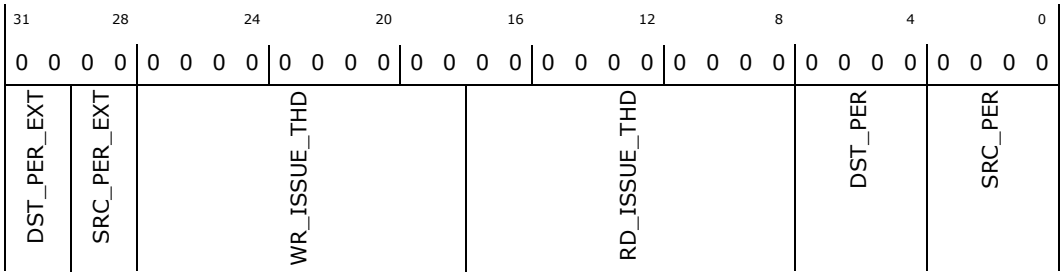
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 1FCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.3.77 reg_SGR_type (SGR5)—Offset 200h

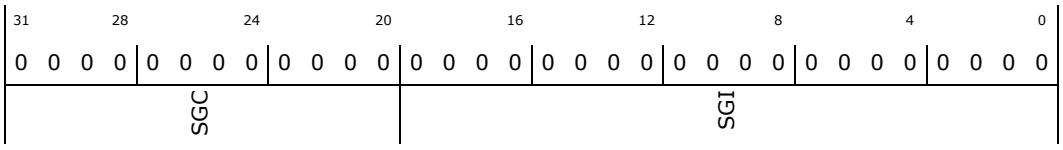
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 200h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.3.78 reg_DSR_type (DSR5)—Offset 208h

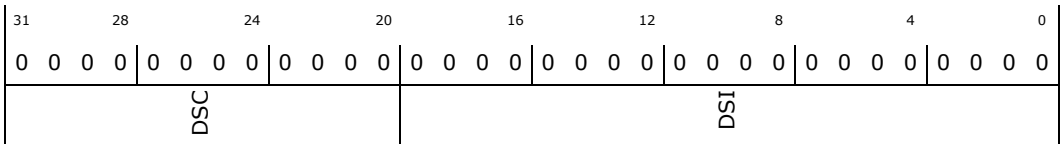
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 208h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.3.79 reg_SAR_type (SAR6)—Offset 210h

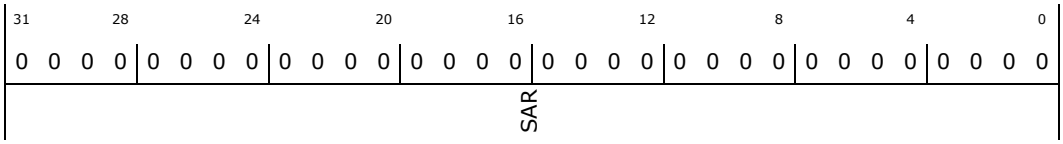
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 210h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.3.80 reg_DAR_type (DAR6)—Offset 218h

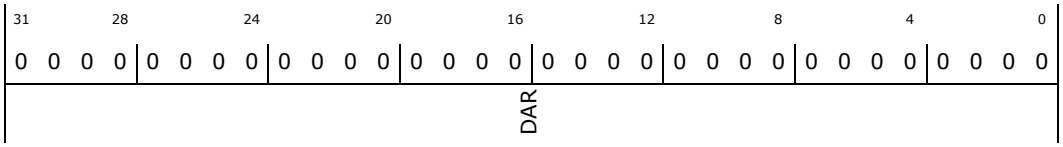
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 218h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.3.81 reg_LLP_type (LLP6)—Offset 220h

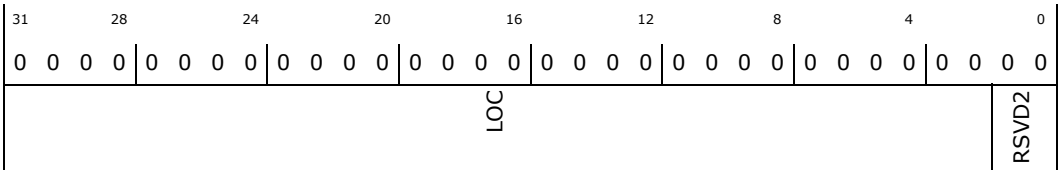
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 220h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.3.82 reg_CTL_LO_type (CTL_LO6)—Offset 228h

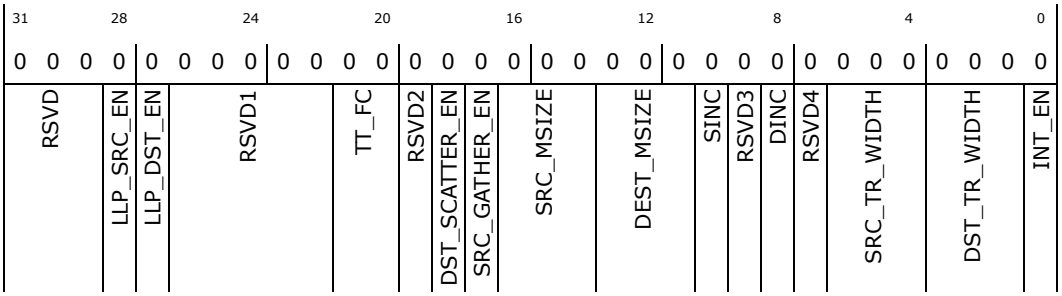
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 228h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.3.83 reg_CTL_HI_type (CTL_HI6)—Offset 22Ch

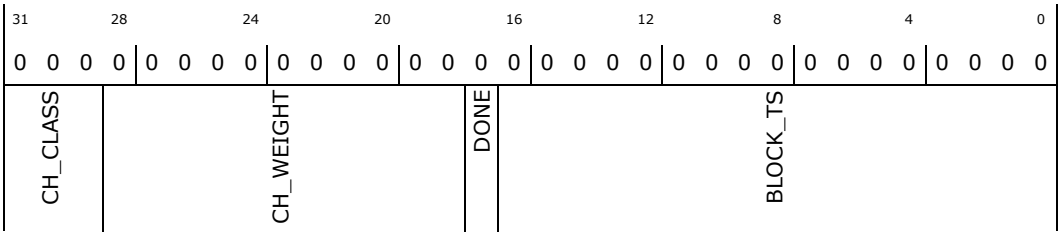
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 22Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below

Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.3.84 reg_SSTAT_type (SSTAT6)—Offset 230h

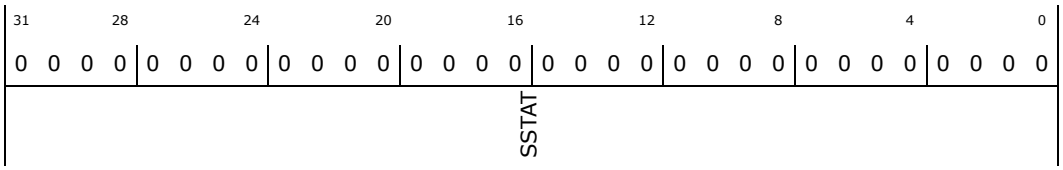
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 230h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.3.85 reg_DSTAT_type (DSTAT6)—Offset 238h

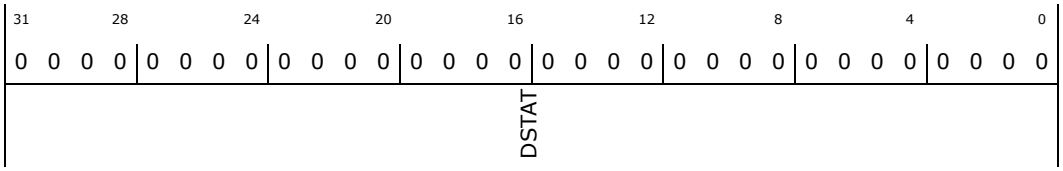
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 238h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.3.86 reg_SSTATAR_type (SSTATAR6)—Offset 240h

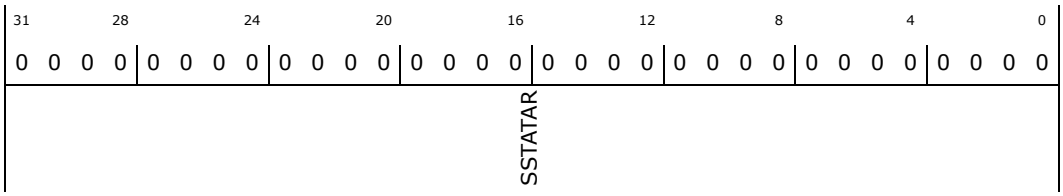
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 240h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.3.87 reg_DSTATAR_type (DSTATAR6)—Offset 248h

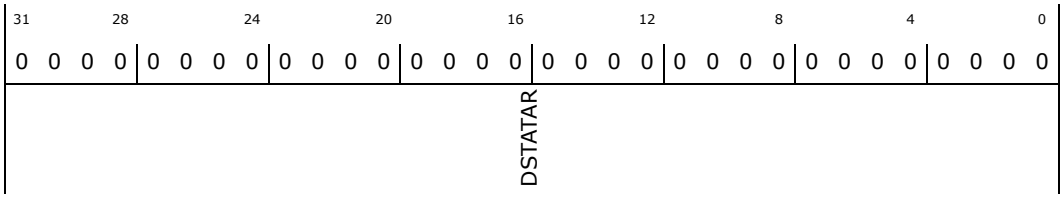
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 248h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.3.88 reg_CFG_LO_type (CFG_LO6)—Offset 250h

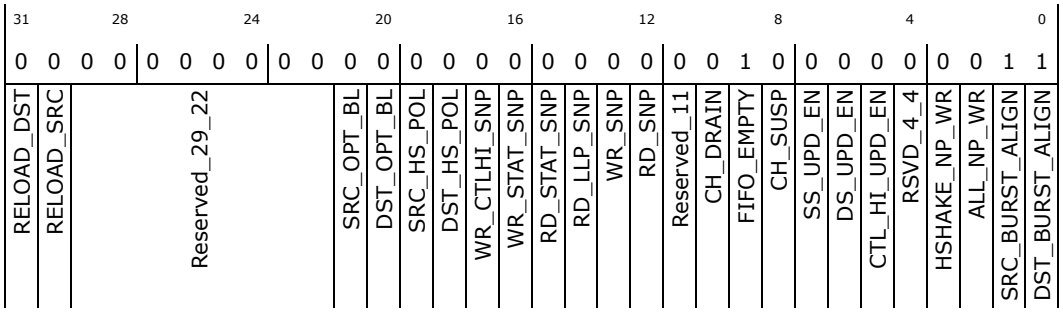
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 250h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.3.89 reg_CFG_HI_type (CFG_HI6)—Offset 254h

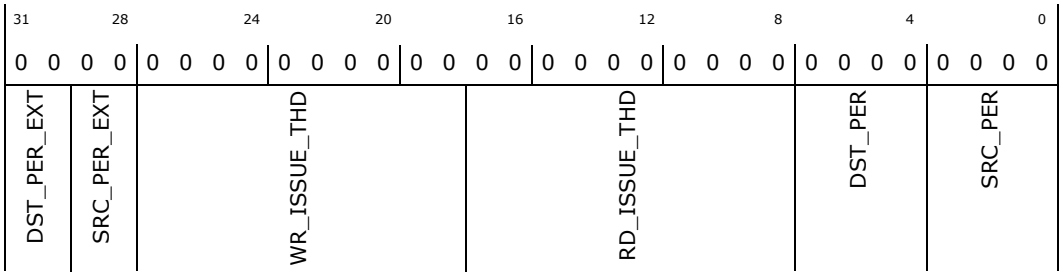
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 254h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.3.90 reg_SGR_type (SGR6)—Offset 258h

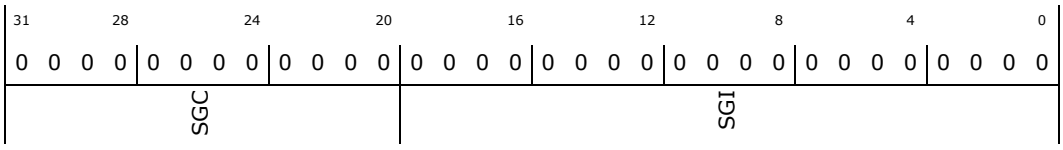
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 258h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.3.91 reg_DSR_type (DSR6)—Offset 260h

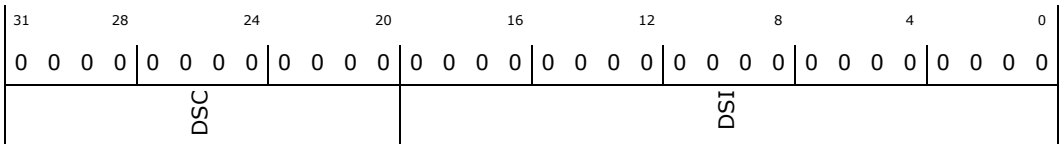
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 260h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.3.92 reg_SAR_type (SAR7)—Offset 268h

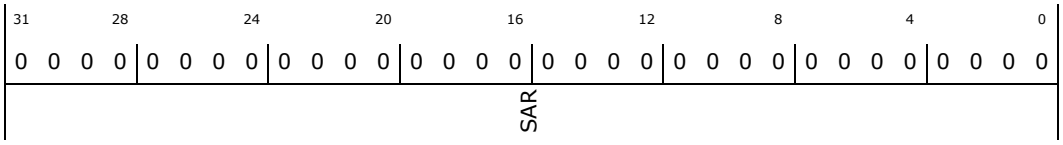
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 268h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.3.93 reg_DAR_type (DAR7)—Offset 270h

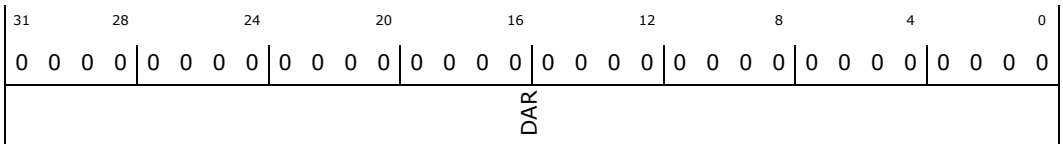
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 270h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

8.3.94 reg_LLP_type (LLP7)—Offset 278h

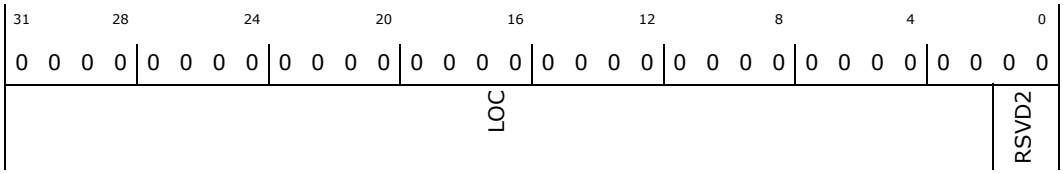
Note: You need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled The LLP register has two functions: The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer-single or multi-block. Table shows how the method of updating the channel registers is a function of LLP.LOC != 0. If LLP.LOC is set to 0x0, then transfers using linked lists are not enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type. LLP.LOC != 0 contains the pointer to the next LLI for block chaining using linked lists, The LLPx register can also point to the address where write-back of the control and source/destination status information occur after block completion.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 278h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0x0 RO	**RSVD2:** Reserved

8.3.95 reg_CTL_LO_type (CTL_LO7)—Offset 280h

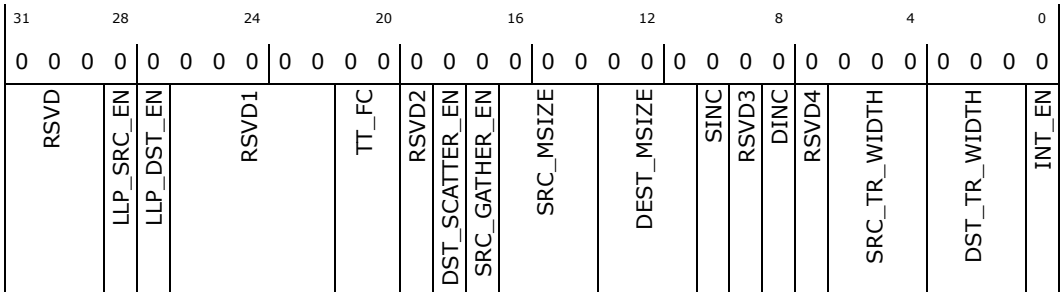
This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 280h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**RSVD:** Reserved
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0x0 RO	**RSVD1:** RSVD

Bit Range	Default & Access	Field Name (ID): Description
21:20	0x0 RW	**TT_FC:** Transfer Type and Flow Control. The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0x0 RO	**RSVD2:** Reserved
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0x0 RW	**SRC_MSIZE:** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. TABLE 5-1 talks about the encoding for this field.
13:11	0x0 RW	**DEST_MSIZE:** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination. TABLE 5-1 talks about the encoding for this field.
10	0x0 RW	**SINC:** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0x0 RO	**RSVD3:** Reserved
8	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0x0 RO	**RSVD4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width (4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations) Table 5-2 lists the decoding for this field. For a non-memory peripheral, this is typically the peripheral (source) FIFO width.
0	0x0 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

8.3.96 reg_CTL_HI_type (CTL_HI7)—Offset 284h

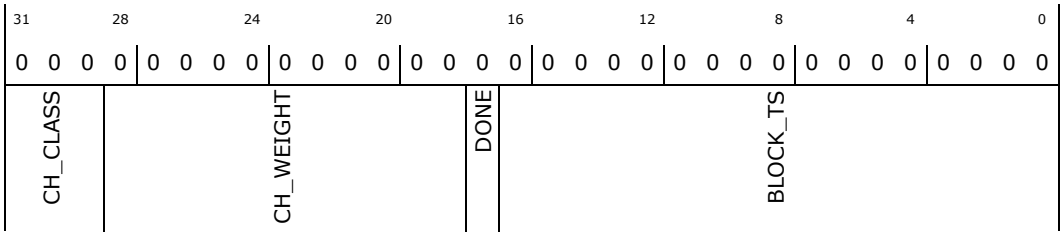
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

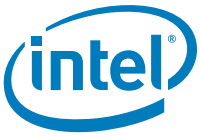
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 284h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**CH_CLASS:** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior. ** See restriction in CH_WEIGHT below



Bit Range	Default & Access	Field Name (ID): Description
28:18	0x0 RW	**CH_WEIGHT:** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0x0 RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0x0 RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

8.3.97 reg_SSTAT_type (SSTAT7)—Offset 288h

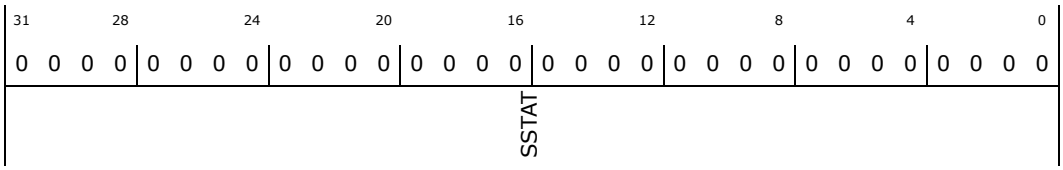
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block. Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 288h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

8.3.98 reg_DSTAT_type (DSTAT7)—Offset 290h

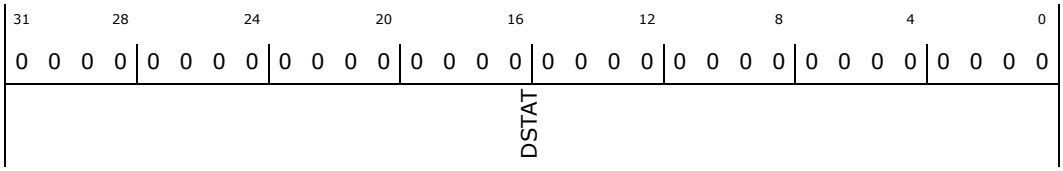
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 290h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

8.3.99 reg_SSTATAR_type (SSTATAR7)—Offset 298h

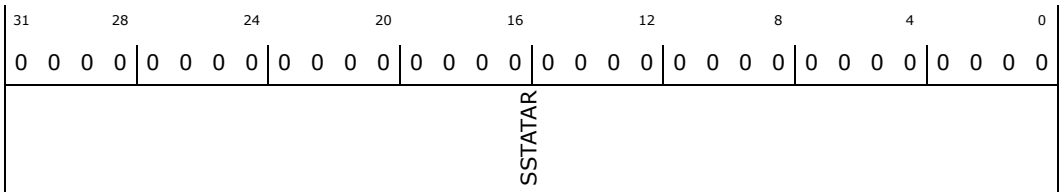
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 298h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SSTATAR:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

8.3.100 reg_DSTATAR_type (DSTATAR7)—Offset 2A0h

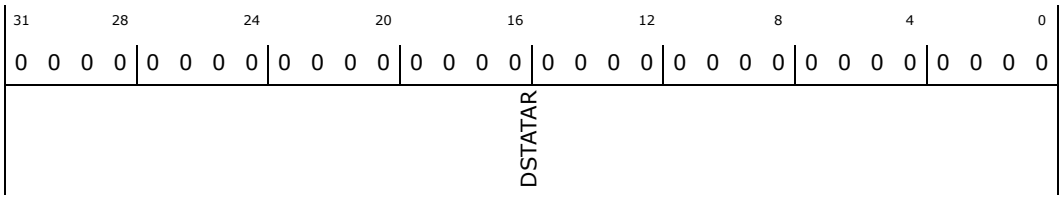
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 2A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DSTATAR:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

8.3.101 reg_CFG_LO_type (CFG_LO7)—Offset 2A8h

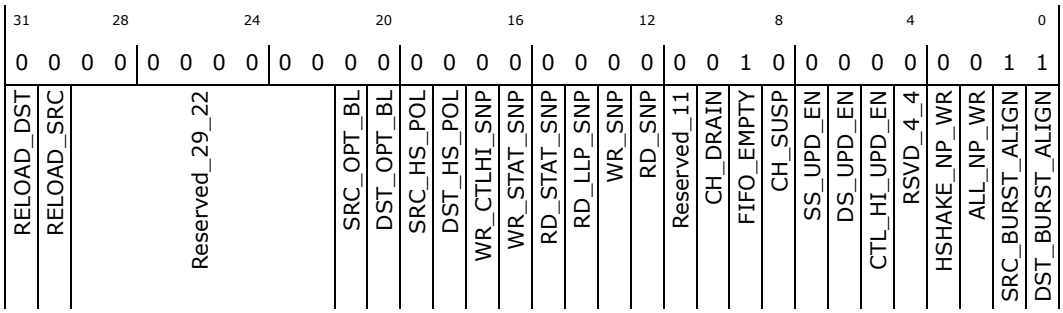
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer.This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 2A8h

Default: 00000203h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0x0 RO	**Reserved_29_22:** Reserved
21	0x0 RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0x0 RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**WR_CTLHI_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the CTL_HI register values
16	0x0 RW	**WR_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port for writing back the SSTAT/DSTAT register values

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**RD_STAT_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading SSTAT/DSTAT register values
14	0x0 RW	**RD_LLP_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port for reading LLP Descriptors
13	0x0 RW	**WR_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Write Port
12	0x0 RW	**RD_SNP:** This Snoop-Attribute bit is driven on the MSB of MReqInfo of DMA Read Port
11	0x0 RO	**Reserved_11:** Reserved
10	0x0 RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0x0 RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0x0 RO	**RSVD_4_4:** Reserved
3	0x0 RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0x0 RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	0x1 RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

8.3.102 reg_CFG_HI_type (CFG_HI7)—Offset 2ACh

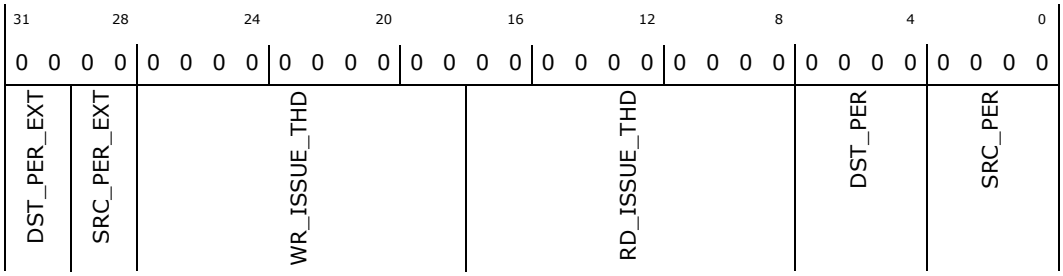
This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 2ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**DST_PER_EXT:** Destination Peripheral Extension : This 2-bit field is used to extend the DST_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall destination peripheral ID becomes DST_PER_EXT[1:0], DST_PER[3:0] which covers the (0-63) range.
29:28	0x0 RW	**SRC_PER_EXT:** Source Peripheral Extension : This 2-bit field is used to extend the SRC_PER field below beyond the Synopsys limit of (0-15) to accommodate additional hardware handshaking interfaces (16-63). In other words, the overall source peripheral ID becomes SRC_PER_EXT[1:0], SRC_PER[3:0] which covers the (0-63) range.
27:18	0x0 RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0x0 RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads (Refer to Section 4.1.1.4). Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS
3:0	0x0 RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface. For more details on mapping please refer to 3.5.3 HARDWARE HANDSHAKE INTERFACE MAPPING TO DMA CHANNELS

8.3.103 reg_SGR_type (SGR7)—Offset 2B0h

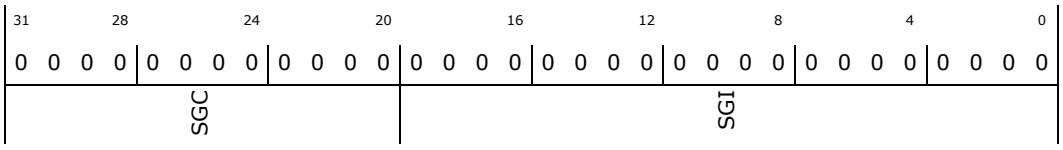
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 2B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval.

8.3.104 reg_DSR_type (DSR7)—Offset 2B8h

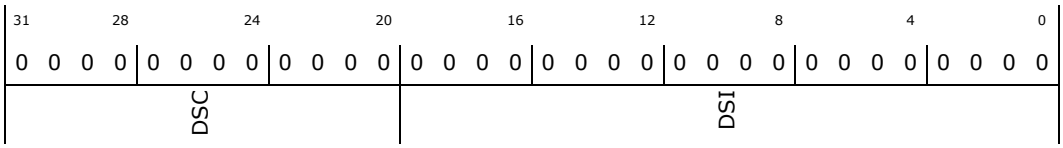
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 2B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC:** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI:** Destination scatter interval.

8.3.105 reg_Raw_type (RawTfr)—Offset 2C0h

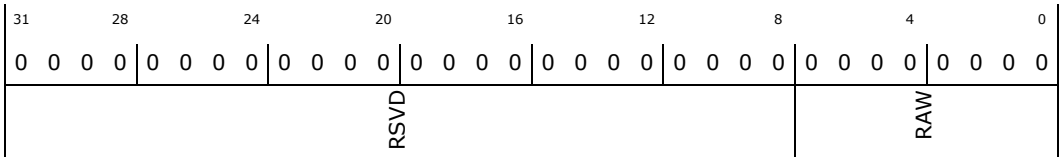
Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 2C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**RAW:** Raw interrupt status

8.3.106 reg_Raw_type (RawBlock)—Offset 2C8h

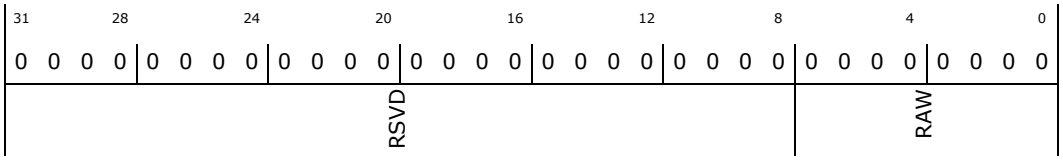
Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 2C8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**RAW:** Raw interrupt status

8.3.107 reg_Raw_type (RawSrcTran)—Offset 2D0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw

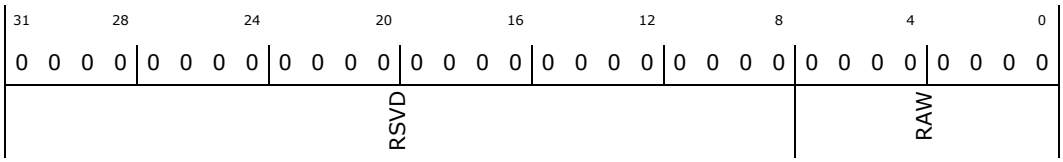
transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 2D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**RAW:** Raw interrupt status

8.3.108 reg_Raw_type (RawDstTran)—Offset 2D8h

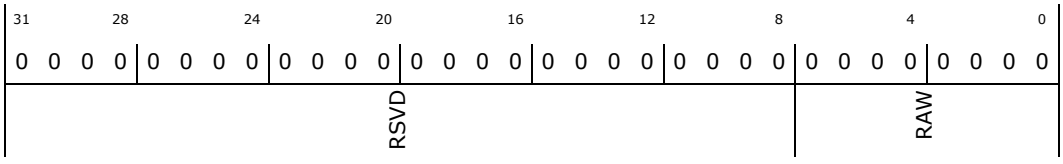
Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 2D8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**RAW:** Raw interrupt status

8.3.109 reg_Raw_type (RawErr)—Offset 2E0h

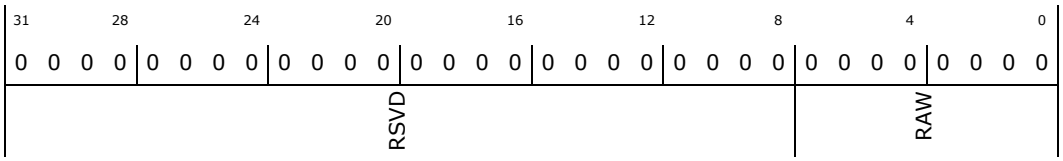
Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers The following RAW registers are available in the DMA RawTfr - Raw Status for Transfer Interrupts RawBlock - Raw Status for Block Interrupts Register RawSrcTran - Raw Status for Source Transaction Interrupts Register RawDstTran - Raw Status for Destination Transaction Interrupts Register RawErr - Raw Status for Error Interrupts Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 2E0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**RAW:** Raw interrupt status

8.3.110 reg_Status_type (StatusTfr)—Offset 2E8h

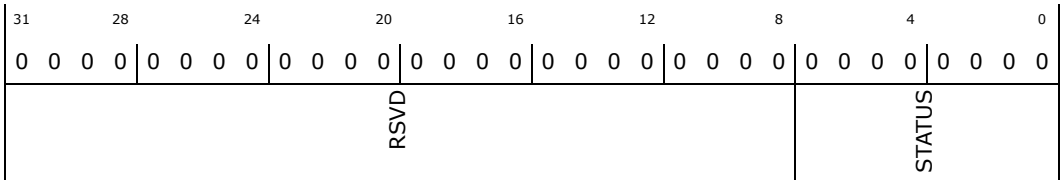
All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 2E8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**STATUS:** Interrupt status

8.3.111 reg_Status_type (StatusBlock)—Offset 2F0h

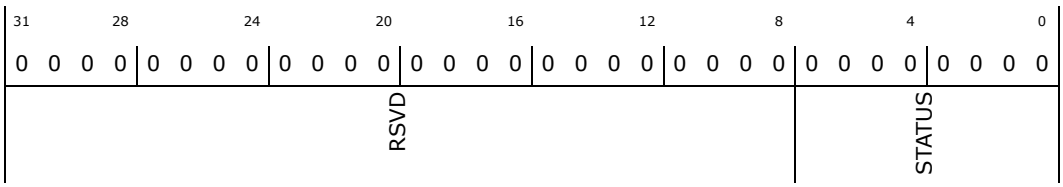
All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 2F0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**STATUS:** Interrupt status

8.3.112 reg_Status_type (StatusSrcTran)—Offset 2F8h

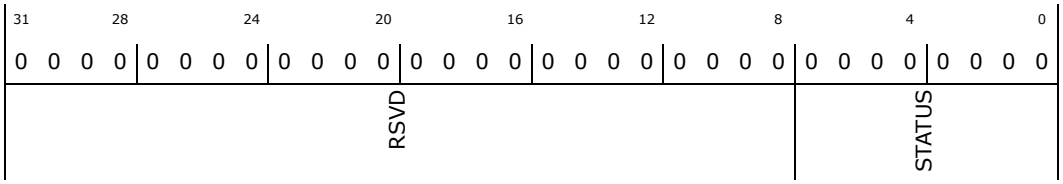
All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 2F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**STATUS:** Interrupt status

8.3.113 reg_Status_type (StatusDstTran)—Offset 300h

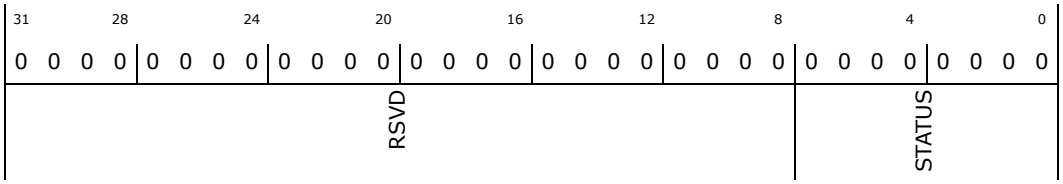
All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 300h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**STATUS:** Interrupt status

8.3.114 reg_Status_type (StatusErr)—Offset 308h

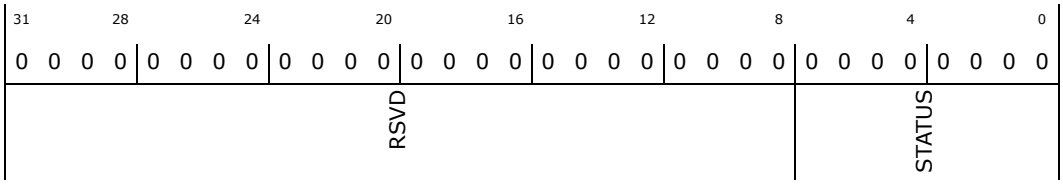
All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 308h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**STATUS:** Interrupt status

8.3.115 reg_Mask_type (MaskTfr)—Offset 310h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation.

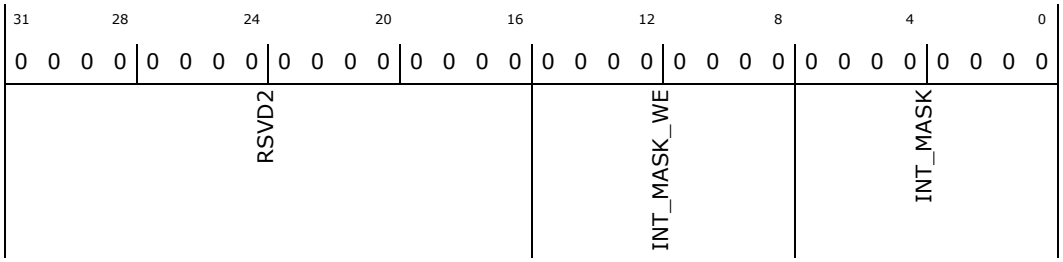
For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 310h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD2:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

8.3.116 reg_Mask_type (MaskBlock)—Offset 318h

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged.

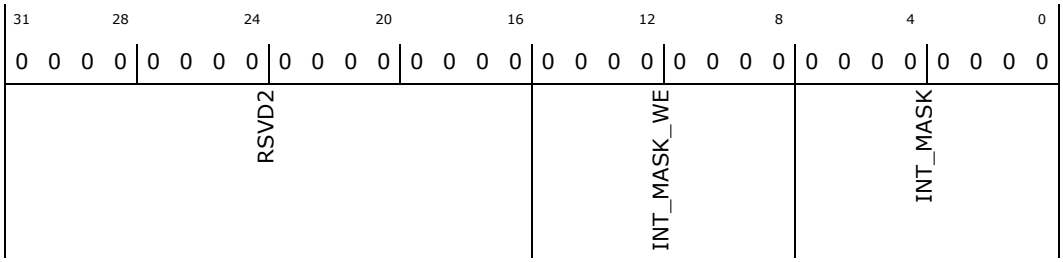
Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 318h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD2:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

8.3.117 reg_Mask_type (MaskSrcTran)—Offset 320h

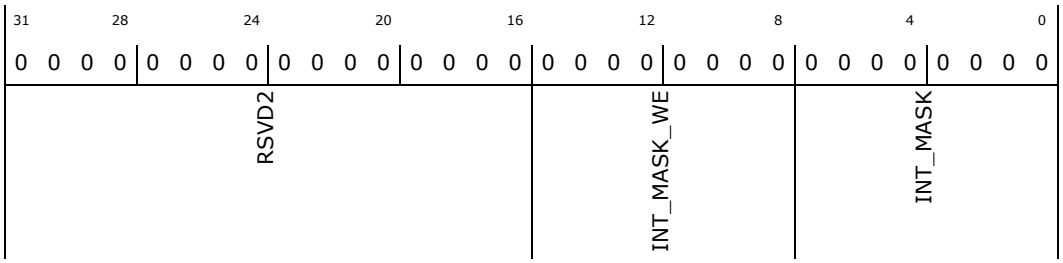
The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 320h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD2:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

8.3.118 reg_Mask_type (MaskDstTran)—Offset 328h

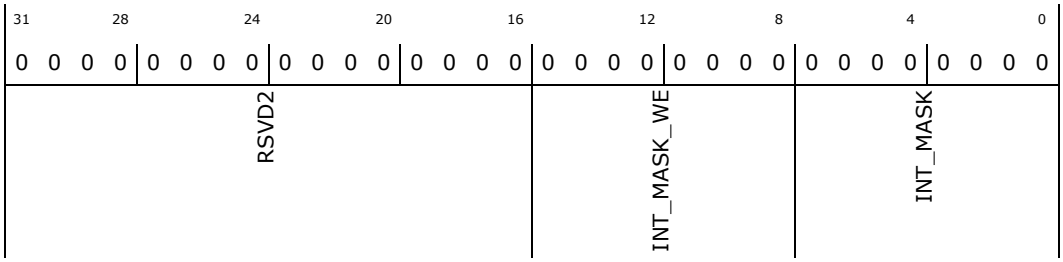
The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 328h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD2:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

8.3.119 reg_Mask_type (MaskErr)—Offset 330h

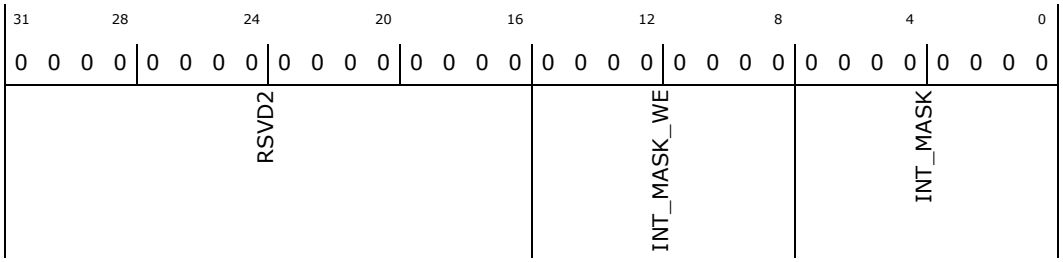
The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 330h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD2:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt mask 0-mask 1-unmask

8.3.120 reg_Clear_type (ClearTfr)—Offset 338h

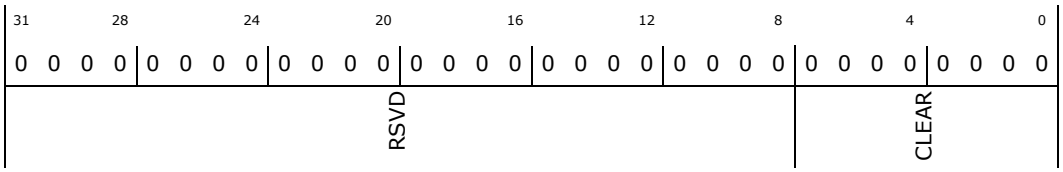
Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 338h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

8.3.121 reg_Clear_type (ClearBlock)—Offset 340h

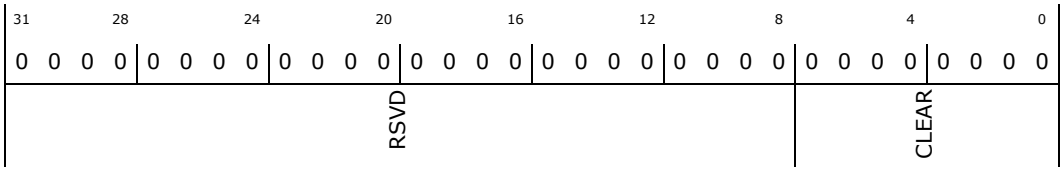
Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 340h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

8.3.122 reg_Clear_type (ClearSrcTran)—Offset 348h

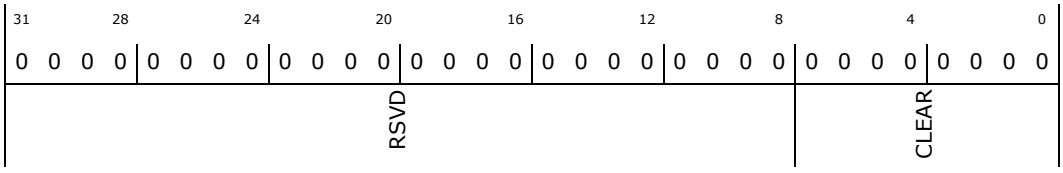
Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 348h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

8.3.123 reg_Clear_type (ClearDstTran)—Offset 350h

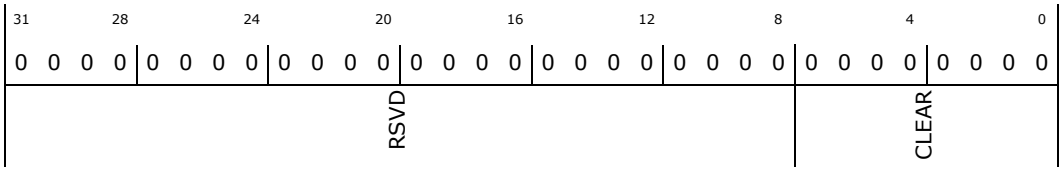
Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 350h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

8.3.124 reg_Clear_type (ClearErr)—Offset 358h

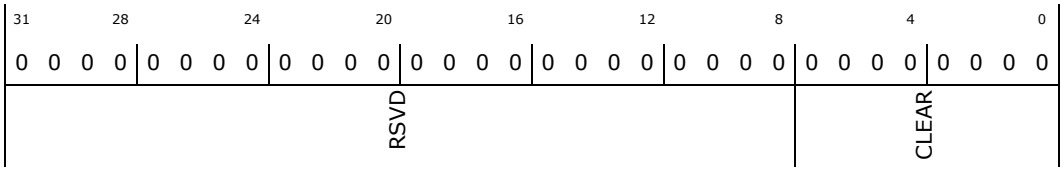
Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 358h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 WO	**CLEAR:** Interrupt clear. 0 = no effect 1 = clear interrupt

8.3.125 reg_StatusInt_type (StatusInt)—Offset 360h

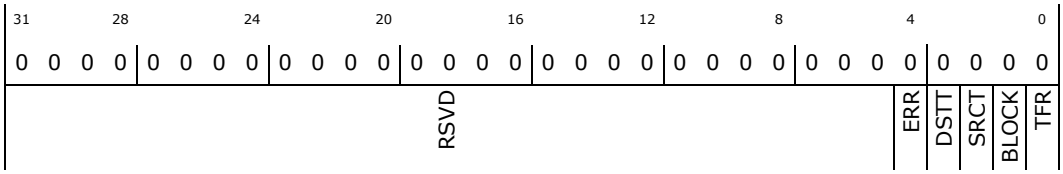
The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran,StatusErr is ORed to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 360h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RO	**RSVD:** Reserved
4	0x0 RO	**ERR:** OR of the contents of StatusErr register.
3	0x0 RO	**DSTT:** OR of the contents of StatusDst register.
2	0x0 RO	**SRCT:** OR of the contents of StatusSrcTran register
1	0x0 RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0x0 RO	**TFR:** OR of the contents of StatusTfr register.

8.3.126 reg_DmaCfgReg_type (DmaCfgReg)—Offset 398h

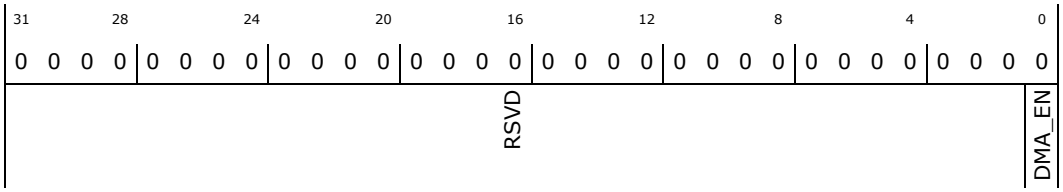
This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 398h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD:** Reserved
0	0x0 RW	**DMA_EN:** DMA Enable bit. 0 = DMA Disabled 1 = DMA Enabled

8.3.127 reg_ChEnReg_type (ChEnReg)—Offset 3A0h

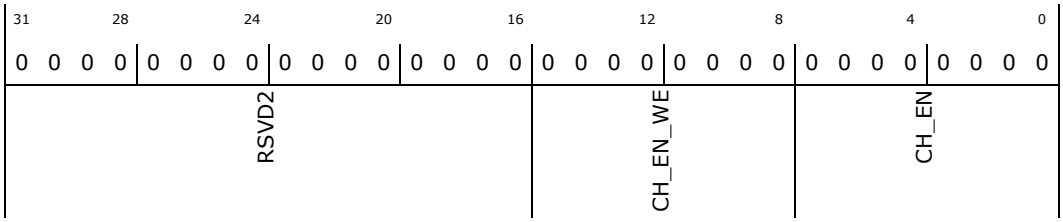
This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority. All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer. For example, writing hex 01x1 writes a 1 into ChEnReg(0), while ChEnReg(7:1) remains unchanged. Writing hex 00xx leaves ChEnReg(7:0) unchanged. Note that a read-modified write is not required.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 3A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD2:** Reserved
15:8	0x0 WO	**CH_EN_WE:** Channel enable write enable.
7:0	0x0 RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

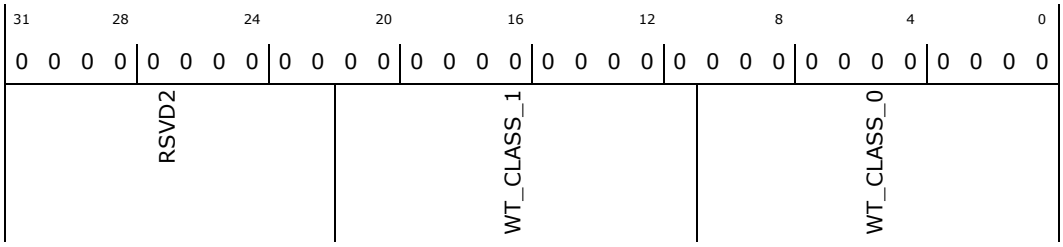
8.3.128 reg_CLASS_PRIORITY0_LO_type (ClassPriority0_LO)—Offset 3B8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 3B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**RSVD2:** Reserved
21:11	0x0 RW	**WT_CLASS_1:** Class Weight 1: Value of K assigns a weight of (K+1) to Class 1. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0x0 RW	**WT_CLASS_0:** Class Weight 0: Value of K assigns a weight of (K+1) to Class 0. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

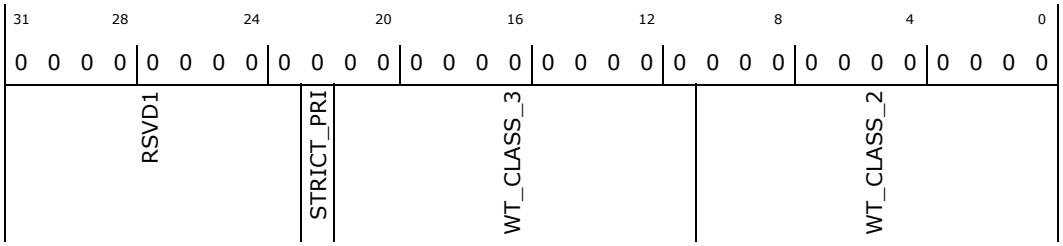
8.3.129 reg_CLASS_PRIORITY0_HI_type (ClassPriority0_HI)—Offset 3BCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 3BCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0x0 RO	**RSVD1:** Reserved
22	0x0 RW	**STRICT_PRI:** If set, Higher class values will always have higher priorities than lower class values. If not set, round-robin arbitration will be used between different classes using WT_CLASS_n values.
21:11	0x0 RW	**WT_CLASS_3:** Class Weight 3: Value of K assigns a weight of (K+1) to Class 3. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0x0 RW	**WT_CLASS_2:** Class Weight 2: Value of K assigns a weight of (K+1) to Class 2. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

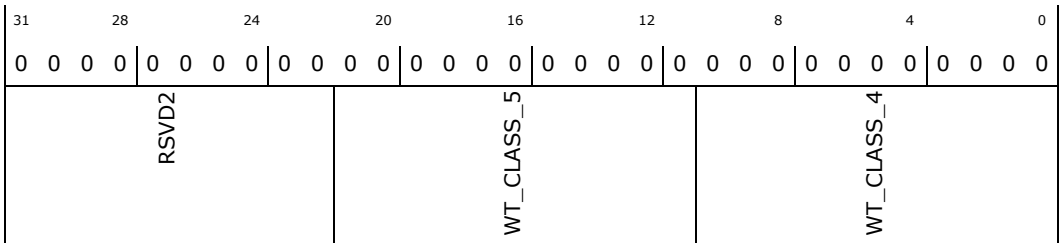
8.3.130 reg_CLASS_PRIORITY1_LO_type (ClassPriority1_LO)—Offset 3C0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 3C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**RSVD2:** Reserved
21:11	0x0 RW	**WT_CLASS_5:** Class Weight 5: Value of K assigns a weight of (K+1) to Class 5. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0x0 RW	**WT_CLASS_4:** Class Weight 4: Value of K assigns a weight of (K+1) to Class 4. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

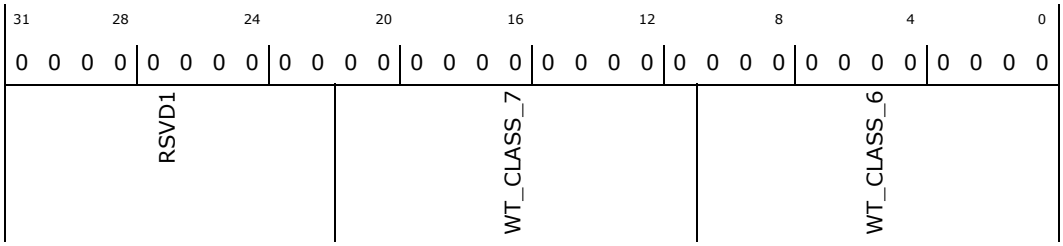
8.3.131 reg_CLASS_PRIORITY1_HI_type (ClassPriority1_HI)—Offset 3C4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 3C4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**RSVD1:** Reserved
21:11	0x0 RW	**WT_CLASS_7:** Class Weight 7: Value of K assigns a weight of (K+1) to Class 7. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.
10:0	0x0 RW	**WT_CLASS_6:** Class Weight 6: Value of K assigns a weight of (K+1) to Class 6. Since K is from 0 to (2^11-1)=2047, Arbitration Class Weight ranges from 1 to 2048 bytes.

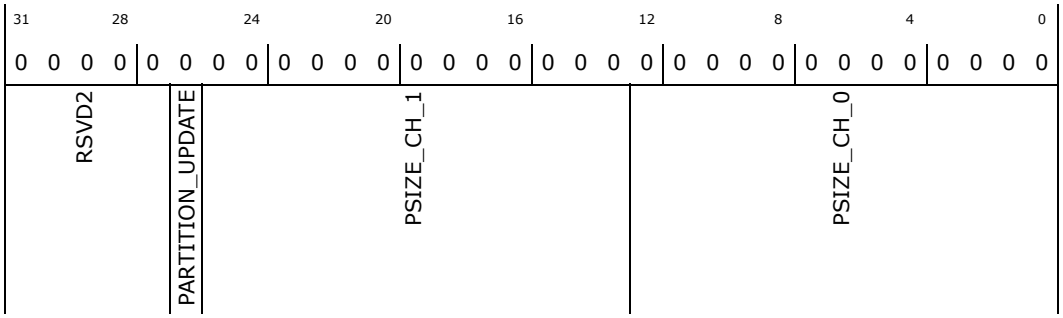
8.3.132 reg_FIFO_PARTITION0_LO_type (FifoPartition0_LO)—Offset 400h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 400h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RSVD2:** Reserved
26	0x0 RW	**PARTITION_UPDATE:** SW needs to write to this bit for the partitioning assignments to take effect.
25:13	0x0 RW	**PSIZE_CH_1:** Partition Byte Size assigned to Channel 1. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0x0 RW	**PSIZE_CH_0:** Partition Byte Size assigned to Channel 0. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

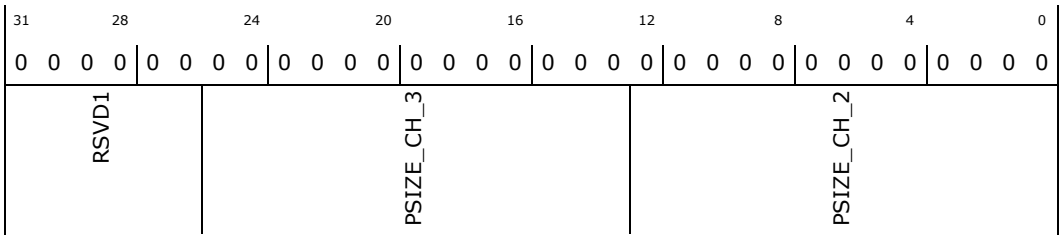
8.3.133 reg_FIFO_PARTITION0_HI_type (FifoPartition0_HI)—Offset 404h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + 94000h] + 404h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD1:** Reserved
25:13	0x0 RW	**PSIZE_CH_3:** Partition Byte Size assigned to Channel 3. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

Bit Range	Default & Access	Field Name (ID): Description
12:0	0x0 RW	**PSIZE_CH_2:** Partition Byte Size assigned to Channel 2. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

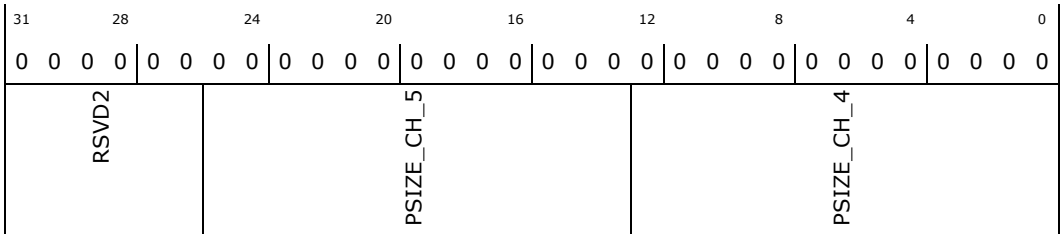
8.3.134 reg_FIFO_PARTITION1_LO_type (FifoPartition1_LO)—Offset 408h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 408h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD2:** Reserved
25:13	0x0 RW	**PSIZE_CH_5:** Partition Byte Size assigned to Channel 5. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0x0 RW	**PSIZE_CH_4:** Partition Byte Size assigned to Channel 4. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

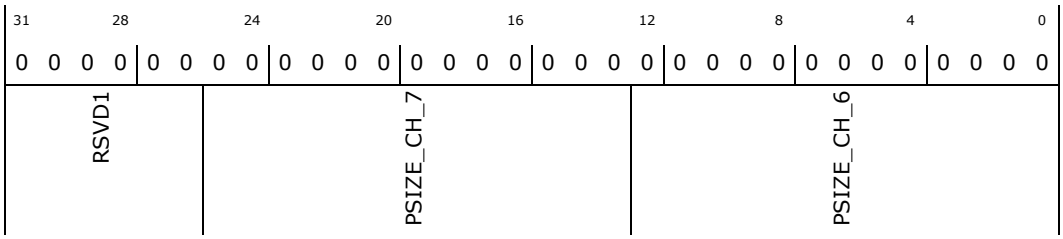
8.3.135 reg_FIFO_PARTITION1_HI_type (FifoPartition1_HI)—Offset 40Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 40Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD1:** Reserved
25:13	0x0 RW	**PSIZE_CH_7:** Partition Byte Size assigned to Channel 7. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.
12:0	0x0 RW	**PSIZE_CH_6:** Partition Byte Size assigned to Channel 6. Ranges from 0 Bytes to (2^13 - 1)=8191 Bytes. However, size needs to be DW Aligned, i.e. a multiple of 4.

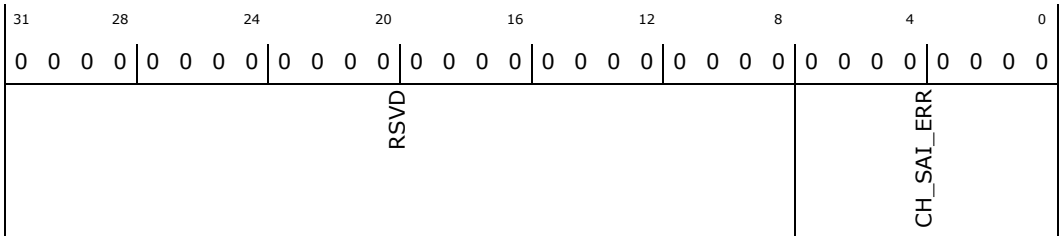
8.3.136 reg_SAI_Error_type (SAI_ERR)—Offset 410h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 410h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RO	**CH_SAI_ERR:** 1: SAI Error occurred on Ch [n] 0: No SAI Error occurred on Ch [n] SAI_ERROR[n] is set by HW on SAI violation for channel [n]. All bits get cleared by SW when reading this register

8.3.137 reg_GLOBAL_CFG_type (GLOBAL_CFG)—Offset 418h

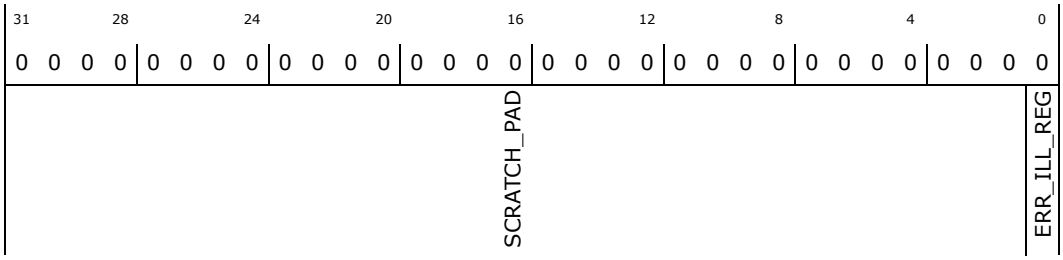
GLOBAL_CFG: GLOBAL DMA Configuration Register

Access Method

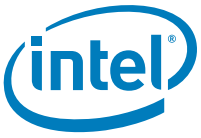
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + 94000h] + 418h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**SCRATCH_PAD:** This field will have all bits with R/W attribute to be used for future configuration and de-feature bits.
0	0x0 RW	**ERR_ILL_REG:** 0x1 : Issue ERR response on reading illegal (non-existing) registers 0x0 : Issue DVA response on reading illegal (non-existing) registers



8.4 LPE PCI Configuration Registers

Table 55. Summary of LPE PCI Configuration Registers—0/21/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"reg_DEVVENDID_type (DEVVENDID)—Offset 0h" on page 3711	0F288086h
4–7h	4	"reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h" on page 3711	00100000h
8–Bh	4	"reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h" on page 3712	04010000h
C–Fh	4	"reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch" on page 3713	00000000h
10–13h	4	"reg_BAR_type (BAR)—Offset 10h" on page 3713	00000000h
18–1Bh	4	"reg_BAR1_type (BAR1)—Offset 18h" on page 3714	00000000h
2C–2Fh	4	"reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch" on page 3715	00000000h
30–33h	4	"reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 3715	00000000h
34–37h	4	"reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h" on page 3716	00000080h
3C–3Fh	4	"reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch" on page 3716	00000100h
80–83h	4	"reg_POWERCAPID_type (POWERCAPID)—Offset 80h" on page 3717	00030001h
84–87h	4	"reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h" on page 3718	00000008h
F8–FBh	4	"reg_MANID_type (MANID)—Offset F8h" on page 3718	04000F1Ch

8.4.1 reg_DEVVENDID_type (DEVVENDID)—Offset 0h

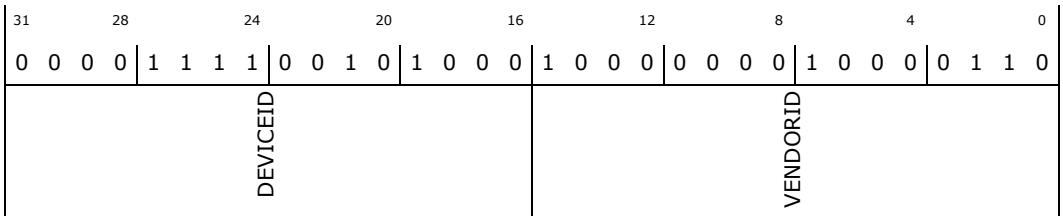
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:21, F:0] + 0h

Default: 0F288086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xf28 RO	**DEVICEID:** Reserved.
15:0	0x8086 RO	**VENDORID:** Reserved.

8.4.2 reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h

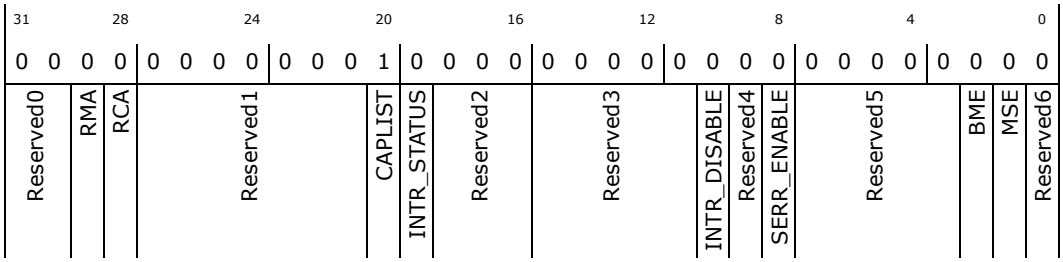
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:21, F:0] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved0:** Reserved.
29	0x0 RW/1C	**RMA:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
28	0x0 RW/1C	**RCA:** Reserved.
27:21	0x0 RO	**Reserved1:** Reserved.
20	0x1 RO	**CAPLIST:** Reserved.
19	0x0 RO	**INTR_STATUS:** Reserved.
18:16	0x0 RO	**Reserved2:** Reserved.
15:11	0x0 RO	**Reserved3:** Reserved.
10	0x0 RW	**INTR_DISABLE:** Reserved.
9	0x0 RO	**Reserved4:** Reserved.
8	0x0 RW	**SERR_ENABLE:** Reserved.
7:3	0x0 RO	**Reserved5:** Reserved.
2	0x0 RW	**BME:** Reserved.
1	0x0 RW	**MSE:** Reserved.
0	0x0 RO	**Reserved6:** Reserved.

8.4.3 reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h

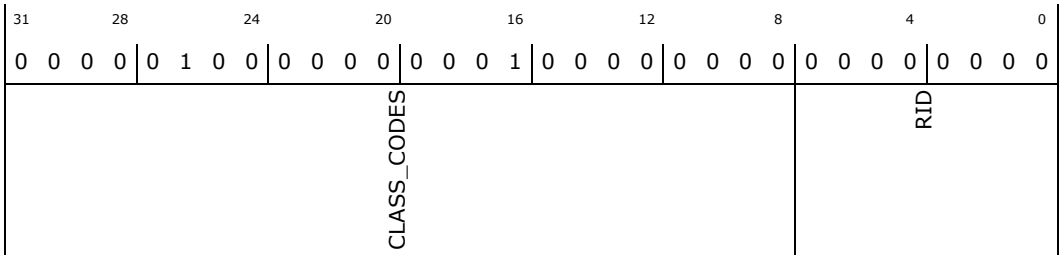
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:21, F:0] + 8h

Default: 04010000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x40100 RO	**CLASS_CODES:** Reserved.
7:0	0x0 RO	**RID:** Reserved.

8.4.4 reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch

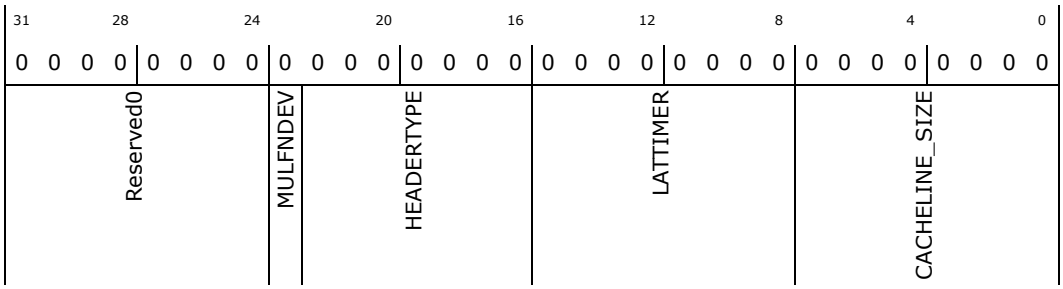
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:21, F:0] + Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved.
23	0x0 RO	**MULFNDEV:** Reserved.
22:16	0x0 RO	**HEADERTYPE:** Reserved.
15:8	0x0 RO	**LATTIMER:** Reserved.
7:0	0x0 RW	**CACHELINE_SIZE:** Reserved.

8.4.5 reg_BAR_type (BAR)—Offset 10h

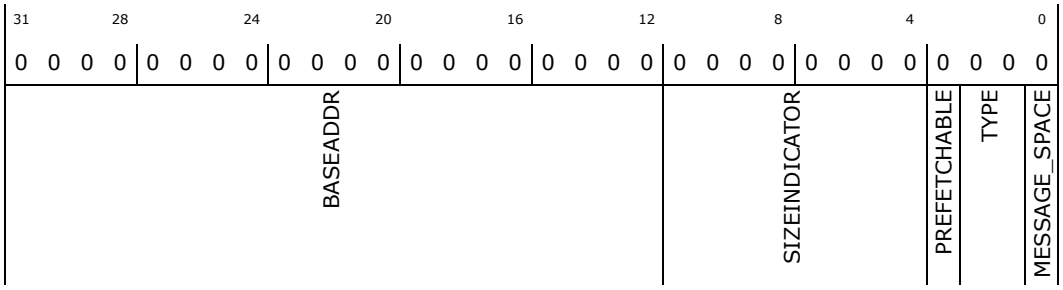
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:21, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Reserved.
11:4	0x0 RO	**SIZEINDICATOR:** Reserved.
3	0x0 RO	**PREFETCHABLE:** Reserved.
2:1	0x0 RO	**TYPE:** Reserved.
0	0x0 RO	**MESSAGE_SPACE:** Reserved.

8.4.6 reg_BAR1_type (BAR1)—Offset 18h

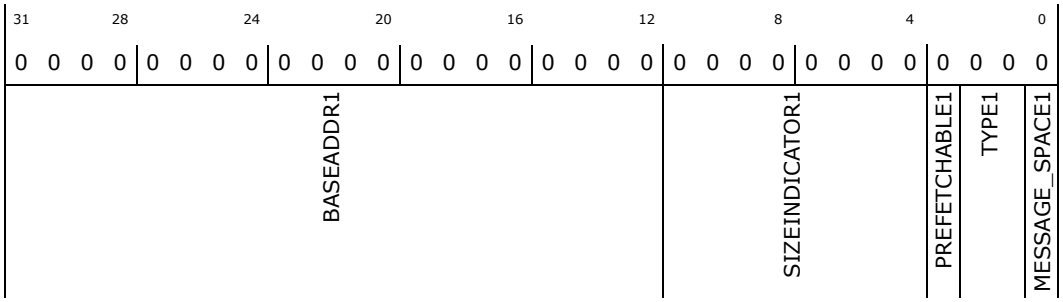
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:21, F:0] + 18h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Reserved.
11:4	0x0 RO	**SIZEINDICATOR1:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RO	**PREFETCHABLE1:** Reserved.
2:1	0x0 RO	**TYPE1:** Reserved.
0	0x0 RO	**MESSAGE_SPACE1:** Reserved.

8.4.7 reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch

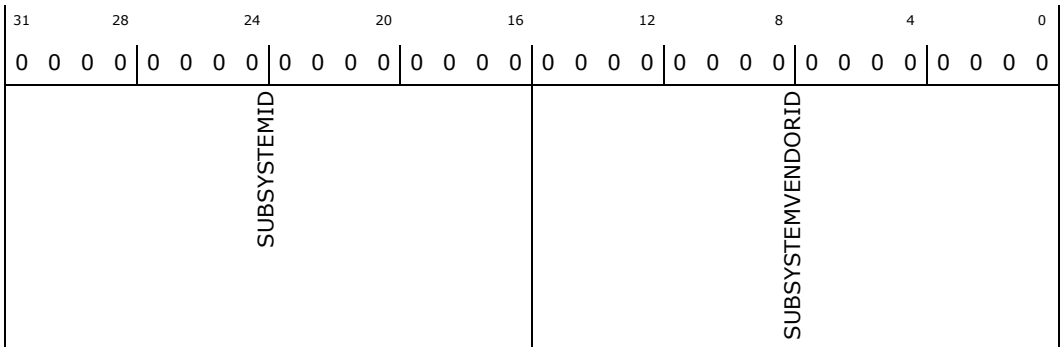
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:21, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Reserved.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Reserved.

8.4.8 reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h

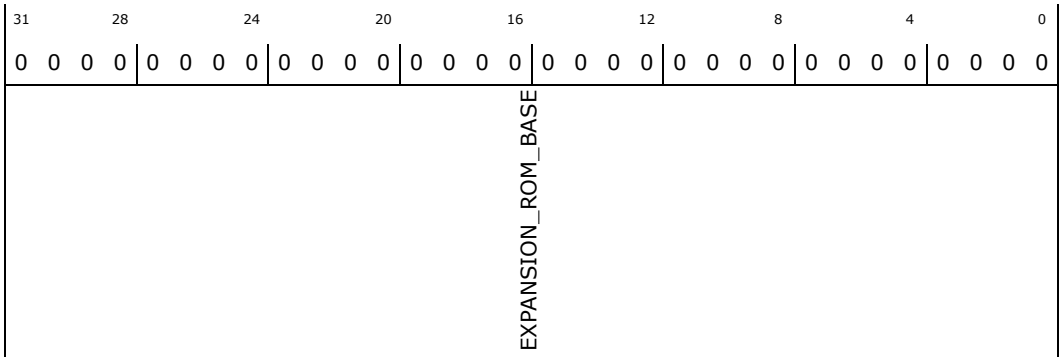
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:21, F:0] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** Reserved.

8.4.9 reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h

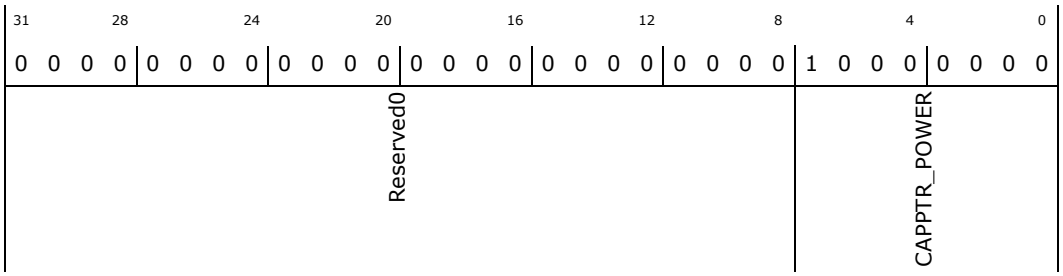
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:21, F:0] + 34h

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved.
7:0	0x80 RO	**CAPPTR_POWER:** Reserved.

8.4.10 reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch

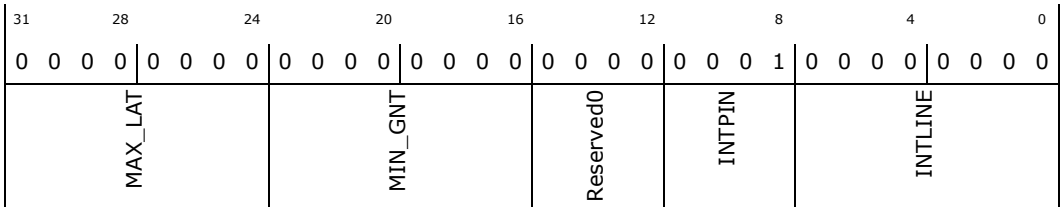
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:21, F:0] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Reserved.
23:16	0x0 RO	**MIN_GNT:** Reserved.
15:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x1 RO	**INTPIN:** Reserved.
7:0	0x0 RW	**INTLINE:** Reserved.

8.4.11 reg_POWERCAPID_type (POWERCAPID)—Offset 80h

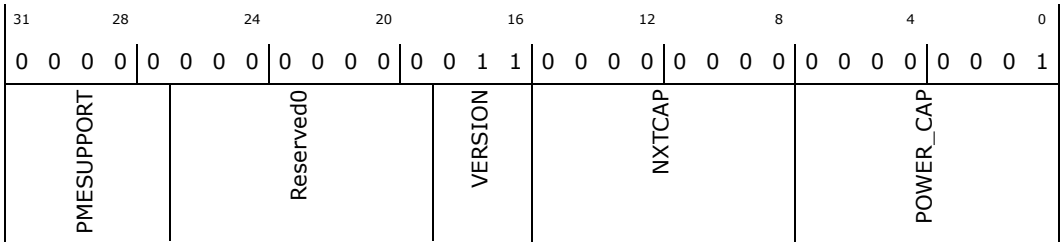
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:21, F:0] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** Reserved.
26:19	0x0 RO	**Reserved0:** Reserved.
18:16	0x3 RO	**VERSION:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**NXTCAP:** Reserved.
7:0	0x1 RO	**POWER_CAP:** Reserved.

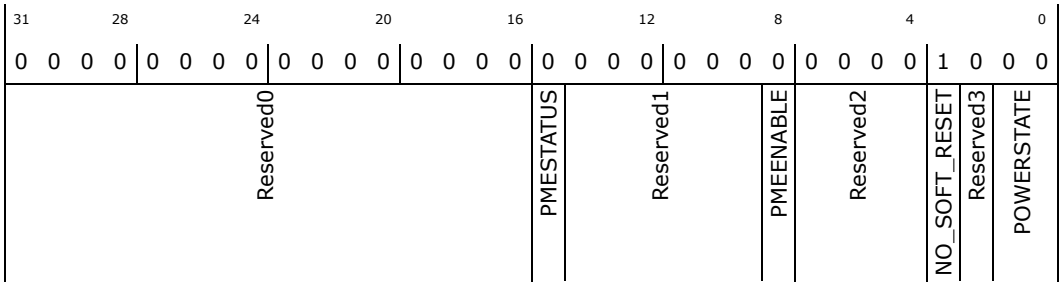
8.4.12 reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:21, F:0] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved.
15	0x0 RW/1C	**PMESTATUS:** Reserved.
14:9	0x0 RO	**Reserved1:** Reserved.
8	0x0 RW	**PMEENABLE:** Reserved.
7:4	0x0 RO	**Reserved2:** Reserved.
3	0x1 RO	**NO_SOFT_RESET:** Reserved.
2	0x0 RO	**Reserved3:** Reserved.
1:0	0x0 RW	**POWERSTATE:** Reserved.

8.4.13 reg_MANID_type (MANID)—Offset F8h

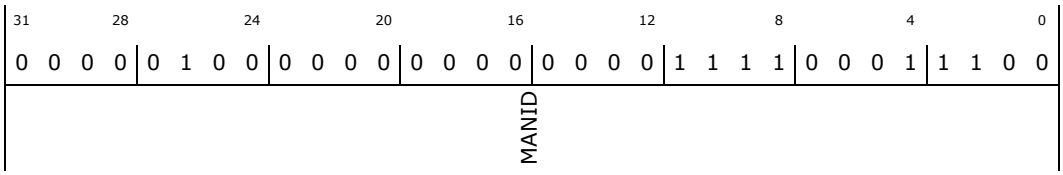
Manufacturers ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:21, F:0] + F8h

Default: 04000F1Ch



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x4000f1c RO	**MANID:** Reserved.

8.5 LPE Memory Mapped I/O Registers

Table 56. Summary of LPE Memory Mapped I/O Registers—lpe_bridge.BAR1

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"reg_DEVVENDID_type (DEVVENDID)—Offset 0h" on page 3721	0F288086h
4–7h	4	"reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h" on page 3721	00100000h
8–Bh	4	"reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h" on page 3722	04010000h
C–Fh	4	"reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch" on page 3723	00000000h
10–13h	4	"reg_BAR_type (BAR)—Offset 10h" on page 3723	00000000h
18–1Bh	4	"reg_BAR1_type (BAR1)—Offset 18h" on page 3724	00000000h
2C–2Fh	4	"reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch" on page 3725	00000000h
30–33h	4	"reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 3725	00000000h
34–37h	4	"reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h" on page 3726	00000080h
3C–3Fh	4	"reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch" on page 3726	00000100h
80–83h	4	"reg_POWERCAPID_type (POWERCAPID)—Offset 80h" on page 3727	00030001h
84–87h	4	"reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h" on page 3728	00000008h
F8–FBh	4	"reg_MANID_type (MANID)—Offset F8h" on page 3728	04000F1Ch

8.5.1 reg_DEVVENDID_type (DEVVENDID)—Offset 0h

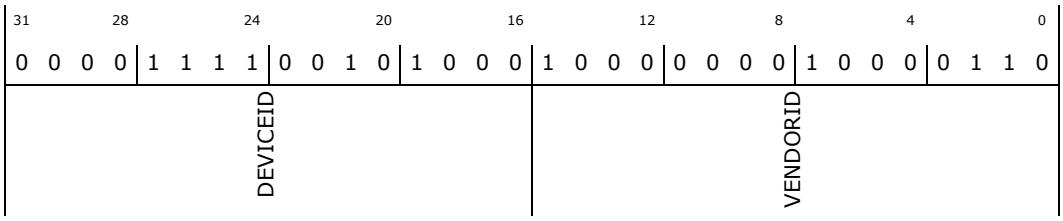
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR1] + 0h

Default: 0F288086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xf28 RO	**DEVICEID:** Reserved.
15:0	0x8086 RO	**VENDORID:** Reserved.

8.5.2 reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h

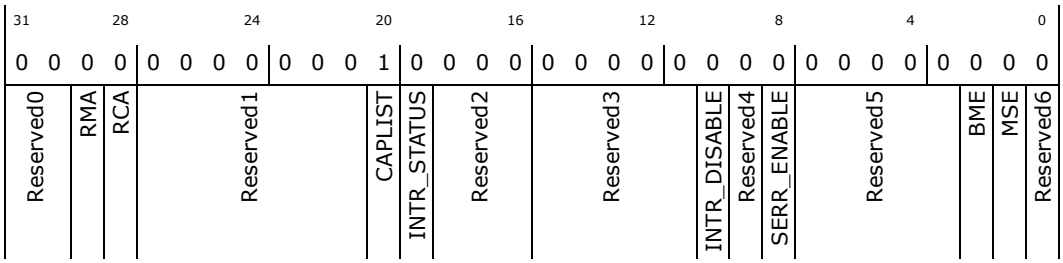
STATUSCOMMAND- Status and Command

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR1] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved0:** Reserved.
29	0x0 RW/1C	**RMA:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
28	0x0 RW/1C	**RCA:** Reserved.
27:21	0x0 RO	**Reserved1:** Reserved.
20	0x1 RO	**CAPLIST:** Reserved.
19	0x0 RO	**INTR_STATUS:** Reserved.
18:16	0x0 RO	**Reserved2:** Reserved.
15:11	0x0 RO	**Reserved3:** Reserved.
10	0x0 RW	**INTR_DISABLE:** Reserved.
9	0x0 RO	**Reserved4:** Reserved.
8	0x0 RW	**SERR_ENABLE:** Reserved.
7:3	0x0 RO	**Reserved5:** Reserved.
2	0x0 RW	**BME:** Reserved.
1	0x0 RW	**MSE:** Reserved.
0	0x0 RO	**Reserved6:** Reserved.

8.5.3 reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h

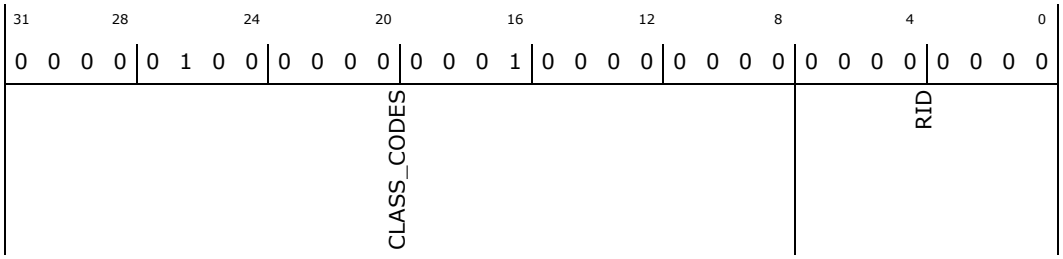
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR1] + 8h

Default: 04010000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x40100 RO	**CLASS_CODES:** Reserved.
7:0	0x0 RO	**RID:** Reserved.

8.5.4 reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch

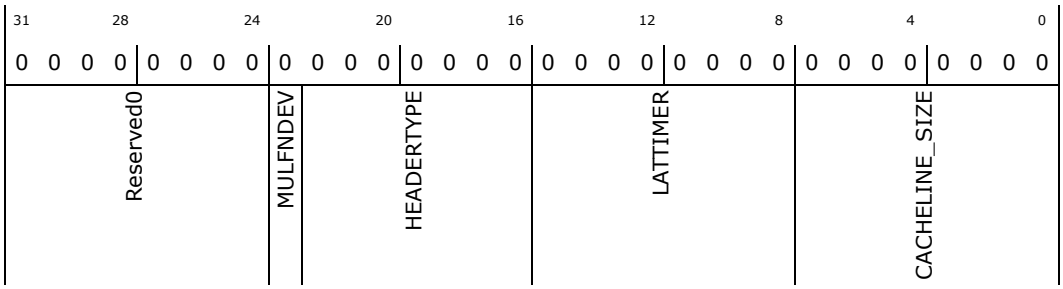
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR1] + Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved.
23	0x0 RO	**MULFNDEV:** Reserved.
22:16	0x0 RO	**HEADERTYPE:** Reserved.
15:8	0x0 RO	**LATTIMER:** Reserved.
7:0	0x0 RW	**CACHELINE_SIZE:** Reserved.

8.5.5 reg_BAR_type (BAR)—Offset 10h

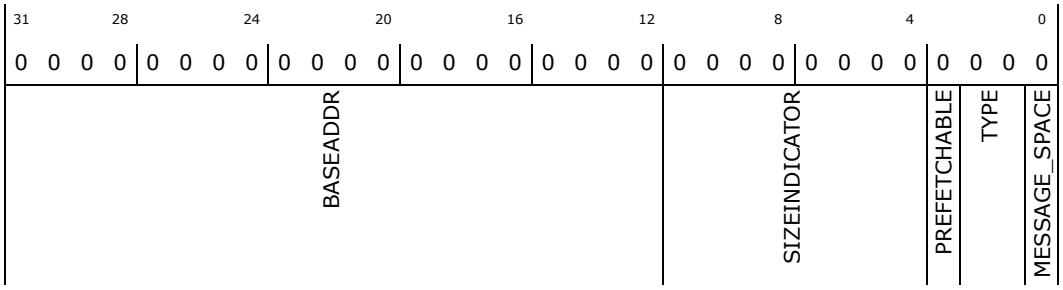
BAR -Base Address Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Reserved.
11:4	0x0 RO	**SIZEINDICATOR:** Reserved.
3	0x0 RO	**PREFETCHABLE:** Reserved.
2:1	0x0 RO	**TYPE:** Reserved.
0	0x0 RO	**MESSAGE_SPACE:** Reserved.

8.5.6 reg_BAR1_type (BAR1)—Offset 18h

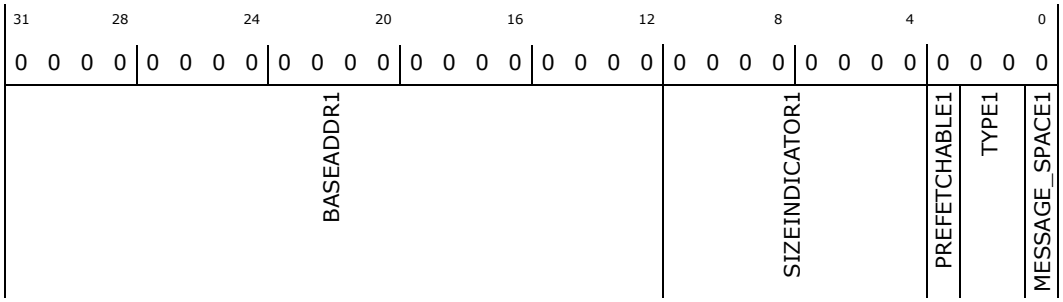
BAR1 -Base Address Register1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR1] + 18h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Reserved.
11:4	0x0 RO	**SIZEINDICATOR1:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RO	**PREFETCHABLE1:** Reserved.
2:1	0x0 RO	**TYPE1:** Reserved.
0	0x0 RO	**MESSAGE_SPACE1:** Reserved.

8.5.7 reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch

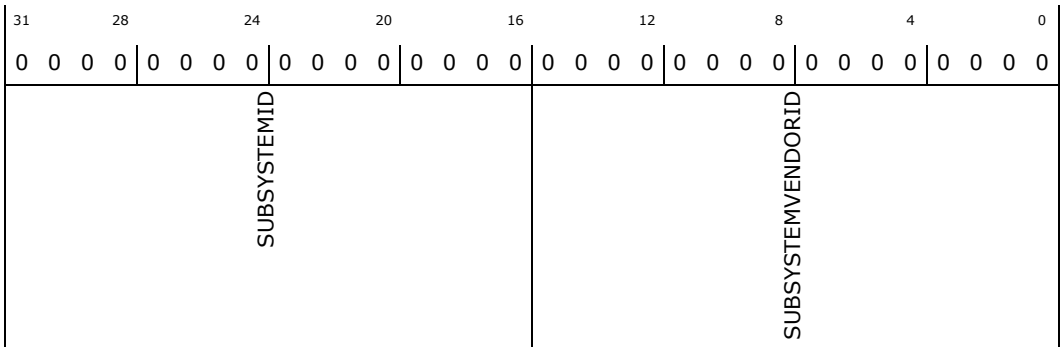
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR1] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Reserved.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Reserved.

8.5.8 reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h

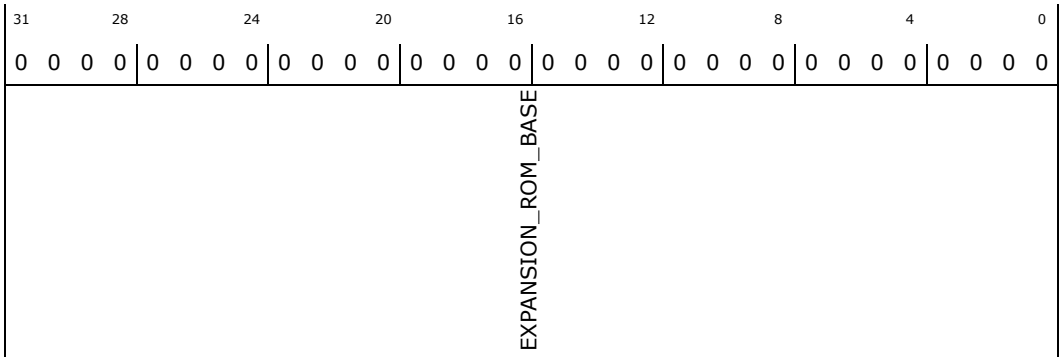
EXPANSION ROM base address

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR1] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** Reserved.

8.5.9 reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h

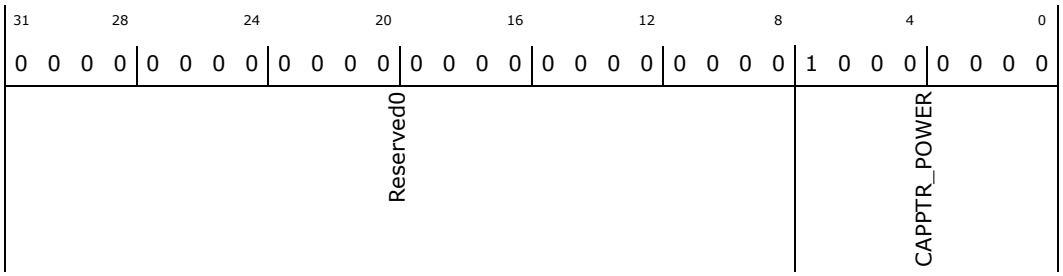
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR1] + 34h

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved.
7:0	0x80 RO	**CAPPTR_POWER:** Reserved.

8.5.10 reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch

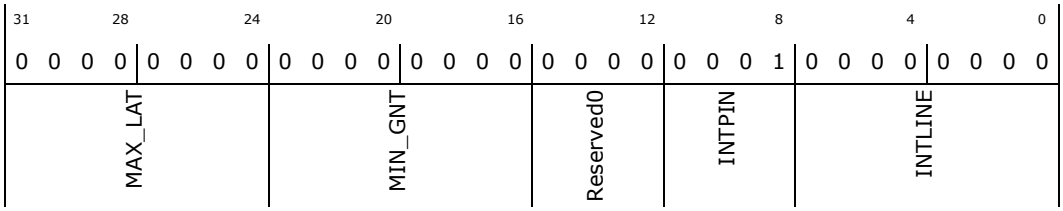
INTERRUPTREG - Interrupt Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR1] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Reserved.
23:16	0x0 RO	**MIN_GNT:** Reserved.
15:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x1 RO	**INTPIN:** Reserved.
7:0	0x0 RW	**INTLINE:** Reserved.

8.5.11 reg_POWERCAPID_type (POWERCAPID)—Offset 80h

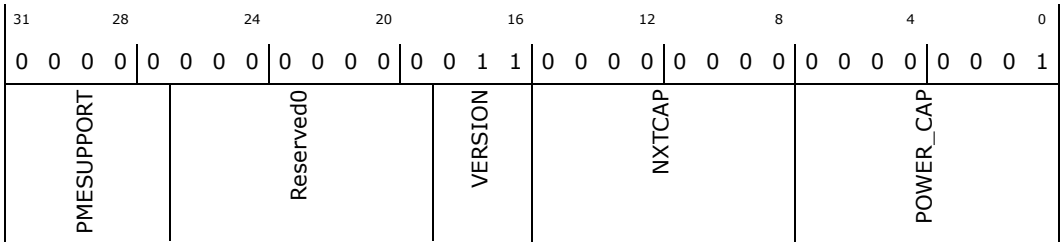
POWERCAPID - PowerManagement Capability ID

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR1] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** Reserved.
26:19	0x0 RO	**Reserved0:** Reserved.
18:16	0x3 RO	**VERSION:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**NXTCAP:** Reserved.
7:0	0x1 RO	**POWER_CAP:** Reserved.

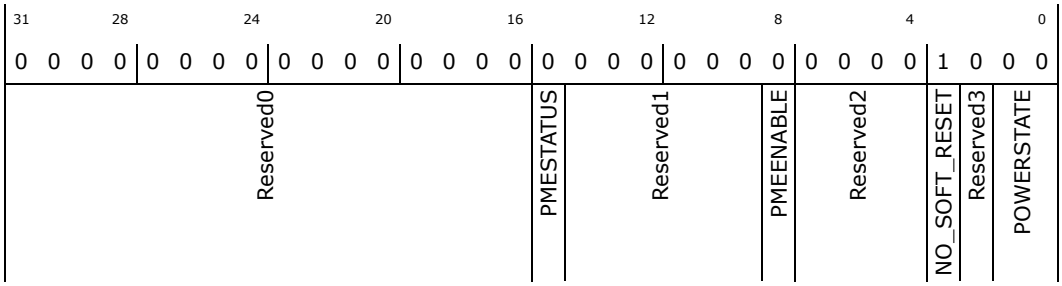
8.5.12 reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR1] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved.
15	0x0 RW/1C	**PMESTATUS:** Reserved.
14:9	0x0 RO	**Reserved1:** Reserved.
8	0x0 RW	**PMEENABLE:** Reserved.
7:4	0x0 RO	**Reserved2:** Reserved.
3	0x1 RO	**NO_SOFT_RESET:** Reserved.
2	0x0 RO	**Reserved3:** Reserved.
1:0	0x0 RW	**POWERSTATE:** Reserved.

8.5.13 reg_MANID_type (MANID)—Offset F8h

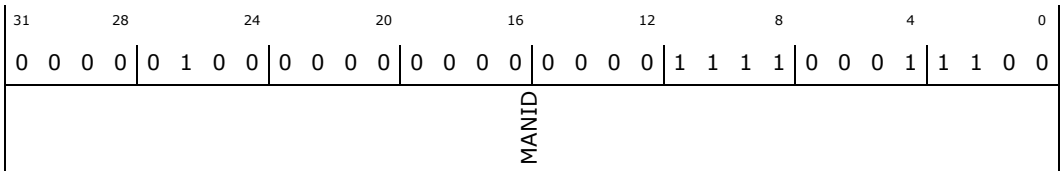
Manufacturers ID

Access Method

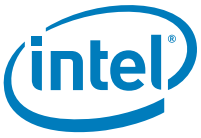
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR1] + F8h

Default: 04000F1Ch



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x4000f1c RO	**MANID:** Reserved.



8.6 SIO SPI 0 Memory Mapped I/O Registers

Table 57. Summary of SIO SPI 0 Memory Mapped I/O Registers—lpe_bridge.BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"SSP Control 0 Register (SSCR0)—Offset 0h" on page 3731	00000000h
4–7h	4	"SSP Control 1 Register (SSCR1)—Offset 4h" on page 3732	43000000h
8–Bh	4	"SSP Status Register (SSSR)—Offset 8h" on page 3734	0000F004h
C–Fh	4	"SSP Interupt Test Register (SSITR)—Offset Ch" on page 3736	00000000h
10–13h	4	"SSP Data Register (SSDR)—Offset 10h" on page 3737	00000000h
28–2Bh	4	"SSP Time-Out Regsiter (SSTO)—Offset 28h" on page 3738	00000000h
2C–2Fh	4	"SSP Programmable Protocol Register (SSPSP)—Offset 2Ch" on page 3738	00000000h
30–33h	4	"SSM TX Time Slot Active Register (SSTSA)—Offset 30h" on page 3739	00000000h
34–37h	4	"SSP RX Time Slot Active Register (SSRSA)—Offset 34h" on page 3740	00000000h
38–3Bh	4	"SSP Time Slot Status Register (SSTSS)—Offset 38h" on page 3740	00000000h
3C–3Fh	4	"SSP Audio Clock Divider (SSACD)—Offset 3Ch" on page 3741	00000000h
40–43h	4	"SSP Control 2 Register (SSCR2)—Offset 40h" on page 3742	00000800h
44–47h	4	"SSP Frame Select Register (SSFS)—Offset 44h" on page 3743	00000001h
48h + [0-7]*4h	4	"SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h" on page 3744	00000000h
68–6Bh	4	"SSP FIFO Level Register (SFIFOL)—Offset 68h" on page 3745	FFFF0000h
6C–6Fh	4	"SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch" on page 3745	00000000h
70–73h	4	"SSP Control 3 Register (SSCR3)—Offset 70h" on page 3746	0000C604h
74–77h	4	"SSP Control 4 Register (SSCR4)—Offset 74h" on page 3748	00000000h
78–7Bh	4	"SSP Control 5 Register (SSCR5)—Offset 78h" on page 3749	00000000h

8.6.1 SSP Control 0 Register (SSCR0)—Offset 0h

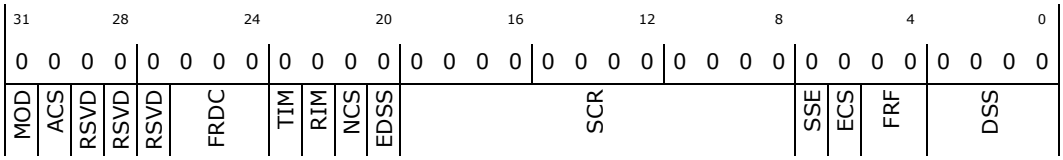
The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A0000h] + 0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Mode Select (MOD):** 0 = Normal SSP Mode 1 = Network Mode
30	0x0 RW	**Audio Clock Select (ACS):** 0 = Clock selection is determined by the NCS and ECS bits 1 = Audio Clock (and Audio Clock Divider) are used to clock the SSP's serial clock (SSPSCLK)
29	0x0 RO	**Reserved (RSVD):** Reserved.
28	0x0 RO	**Reserved (RSVD):** Reserved.
27	0x0 RO	**Reserved (RSVD):** Reserved.
26:24	0x0 RW	**Frame Rate Divider Control (FRDC):** Value 0-7 indicates the number of time slots per frame when in network mode (the actual number of time slots is FRDC+1, so 1 to 8 time slots).
23	0x0 RW	**Transmit FIFO Under Run Interrupt Mask (TIM):** 0 = TUR events will generate an SSP interrupt 1 = TUR events will not generate an SSP interrupt
22	0x0 RW	**Receive FIFO Over Run Interrupt Mask (RIM):** 0 = ROR events will generate an SSP interrupt 1 = ROR events will not generate an SSP interrupt
21	0x0 RW	**Network Clock Select (NCS):** 0 = Clock selection is determined by ECS bit 1 = Network clock is used to create the SSP's serial clock (SSPSCLK)
20	0x0 RW	**Extended Data Size Select (EDSS):** 0 = A zero is preappended to the DSS value which sets the DSS range from 4-16 bits 1 = A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits

Bit Range	Default & Access	Field Name (ID): Description
19:8	0x0 RW	**Serial Clock Rate (SCR):** Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0x0 RW	**Synchronous Serial Port Enable (SSE):** 0 = SSP operation disabled and FIFOs are cleared 1 = SSP operation enabled
6	0x0 RW	**External Clock Select (ECS):** 0 = On-chip clock used to produce the SSP's serial clock (SSPSCLK) 1 = SSPEXTCLK/GPIO pin is used to create the SSP's SSPCLK
5:4	0x0 RW	**Frame Format (FRF):** 00 = Motorola Serial Peripheral Interface (SPI) 01 = Texas Instruments Synchronous Serial Protocol (SSP) 10 = National Semiconductor Microwire 11 = Programmable Serial Protocol (PSP)
3:0	0x0 RW	**Data Size Select (DSS):** With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

8.6.2 SSP Control 1 Register (SSCR1)—Offset 4h

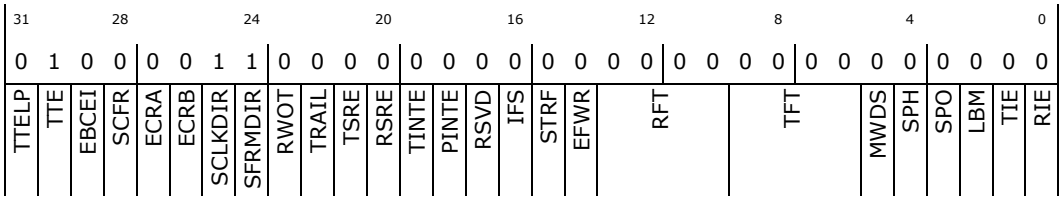
The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A0000h] + 4h

Default: 43000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**TXD Tristate Enable on Last Phase (TTELP):** 0 = TXD line will be tristated on same clock edge as TXD is to be flopped 1 = TXD line will be tristated 1/2 clock edge after TXD is to be flopped
30	0x1 RW	**TXD Tristate Enable (TTE):** 0 = TXD line will not be tristated 1 = TXD line will be tristated when no transmitting data
29	0x0 RW	**Enable Bit Count Error Interrupt (EBCEI):** 0 = Interrupt due to a bit count error is disabled 1 = Interrupt due to a bit count error is enabled

Bit Range	Default & Access	Field Name (ID): Description
28	0x0 RW	**Slave Clock Free Running (SCFR):** 0 = clock input to SSPSCLK is continuously running 1 = clock input to SSPSCLK is only active durring transfers
27	0x0 RW	**Enable Clock Request A (ECRA):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
26	0x0 RW	**Enable Clock Request B (ECRB):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
25	0x1 RW	**SSP Serial Bit Rate Clock (SSPSCLK) Direction (SCLKDIR):** 0 = Master mode, SSP drives SSPSCLK 1 = Slave mode, SSP recieves SSPSCLK
24	0x1 RW	**SSP Frame (SSPSFRM) Direction (SFRMDIR):** 0 = Master mode, SSP drives SSPSFRM 1 = Slave mode, SSP receives SSPSFRM
23	0x0 RW	**Receive With Out Transmit (RWOT):** 0 = Transmit/Receive mode 1 = Receive without transmit mode
22	0x0 RW	**Trailing Byte (TRAIL):** 0 = Processor based, trailing bytes are handled by processor 1 = DMA based, trailing bytes are handled by DMA
21	0x0 RW	**Transmit Service Request Enable (TSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
20	0x0 RW	**Receive Service Request Enable (RSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
19	0x0 RW	**Receiver Time-out Interrupt Enable (TINTE):** 0 = Receiver Time-out interrupts are disabled 1 = Receiver Time-out interrupts are enabled
18	0x0 RW	**Peripheral Trailing Byte Interrupts Enable (PINTE):** 0 = Peripheral Trailing Byte Interrupts are disabled 1 = Peripheral Trailing Byte Interrupts are enabled
17	0x0 RW	**RSVD:** Reserved
16	0x0 RW	**Invert Frame Signal (IFS):** 0 = Frame polarity is determined by SSP format and PSP polarity bits 1 = Frame signal will be inverted from the normal SSP frame signal (as defined by the SSP format nad PSP polarity bits)
15	0x0 RW	**Select FIFO for EFWR (test mode bit) (when EFWR=1) (STRF):** 0 = Transmit FIFO is selected for both writes and reads through the SSP Data Register (SSDR) 1 = Receive FIFO is selected for both writes and reads through the SSP Data Register (SSDR)
14	0x0 RW	**Enable FIFO Write/Read (test mode bit) (EFWR):** 0 = FIFO write/read special function is disabled (normal SSP operational mode) 1 = FIFO write/read special function is enabled

Bit Range	Default & Access	Field Name (ID): Description
13:10	0x0 RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
9:6	0x0 RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
5	0x0 RW	**Microwire Transmit Data Size (MWDS):** 0 = 8-bit command words are transmitted 1 = 16-bit command words are transmitted
4	0x0 RW	**Motorola SPI SSPSCLK Phase Setting (SPH):** 0 = SSPSCLK is inactive one sycle at the start of a fram and 1/2 cycle at the end of a frame 1 = SSPSCLK is inactive 1/2 cycle at the start of a frame and one cycle at the end of a frame
3	0x0 RW	**Motorola SPI SSPSCLK polarity setting (SPO):** 0 = The inactive or idle state of SSPSCLK is low 1 = The inactive or idle state of SSPSCLK is high
2	0x0 RW	**Loop-Back Mode (test mode bit) (LBM):** 0 = Normal serial port operation enabled 1 = Output of transmit serial shifter connected to input of receive serial shifter, internally
1	0x0 RW	**Transmit FIFO Interrupt Enable (TIE):** 0 = Transmit FIFO level interrupt is disabled 1 = Transmit FIFO level interrupt is enabled
0	0x0 RW	**Receive FIFO Interrupt Enable (RIE):** 0 = Receive FIFO level interrupt is disabled 1 = Receive FIFO level interrupt is enabled

8.6.3 SSP Status Register (SSSR)—Offset 8h

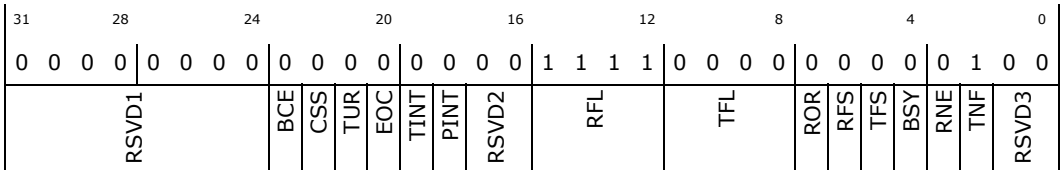
The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A0000h] + 8h

Default: 0000F004h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD1:** Reserved
23	0x0 RW/1C	**Bit Count Error (BCE):** 0 = SSP has not experienced a bit count error 1 = SSPSFRM signal has been asserted when the bit counter was not 0
22	0x0 RO	**Clock Synchronization Status (CSS):** 0 = SSP is ready for slave clock operations 1 = SSP is currently busy synchronizing slave mode signals
21	0x0 RW/1C	**Transmit FIFO Under Run (TUR):** 0 = Transmit FIFO has not experienced an under run 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0x0 RW/1C	**End of Chain (EOC):** 0 = DMA has not signaled an end of chain condition 1 = DMA has signaled an end of chain condition
19	0x0 RW/1C	**Receiver Time-out Interrupt (TINT):** 0 = No receiver time-out pending 1 = Receiver time-out pending
18	0x0 RW/1C	**Peripheral Trailing Byte Interrupt (PINT):** 0 = No peripheral trailing byte interrupt pending 1 = Peripheral trailing byte interrupt pending
17:16	0x0 RO	**RSVD2:** Reserved
15:12	0xf RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value 0xF is read, the FIFO is either empty or full and the programmer should refer to the RNE bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
11:8	0x0 RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the TNF bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
7	0x0 RW/1C	**Receive FIFO Overrun (ROR):** 0 = Receive FIFO has not experienced an overrun 1 = Attempted data write to full receive FIFO, request interrupt
6	0x0 RO	**Receive FIFO Service Request (RFS):** 0 = Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0x0 RO	**Transmit FIFO Service Request (TFS):** 0 = Transmit FIFO level exceeds the TFT threshold (TFT+1), or SSP disabled 1 = Transmit FIFO level is at or below TFT threshold (TFT+1), request interrupt

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RO	**SSP Busy (BSY):** 0 = SSP is idle or disabled 1 = SSP currently transmitting or receiving a frame
3	0x0 RO	**Receive FIOF Not Empty (RNE):** 0 = Receive FIFO is empty 1 = Receive FIFO is not empty
2	0x1 RO	**Transmit FIFO Not Full (TNF):** 0 = Transmit FIFO is full 1 = Transmit FIFO is not full
1:0	0x0 RO	**RSVD3:** Reserved

8.6.4 SSP Interupt Test Register (SSITR)—Offset Ch

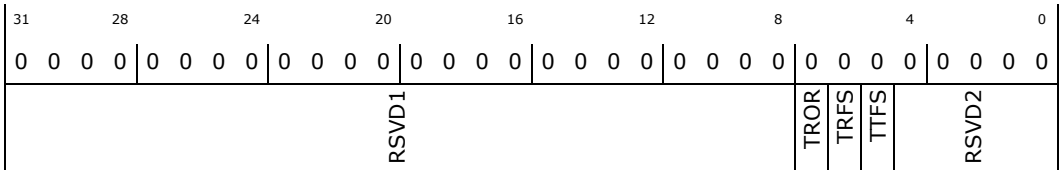
The read-write SSP Interrupt Test registers should be used only for testing purposes. Writing a 1 to the test transmit FIFO request SSITR.TTFS, bit 5, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Transmit FIFO. Writing a 1 to the test receive FIFO request SSITR.TRFS, bit 6, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Receive FIFO. Writing a 1 to the test receive FIFO overrun bit SSITR.TROR, bit 7, will generate a non-maskable Interrupt strobe signal to the Interrupt controller only, no DMA request will be made. Setting any of these bits will also cause the corresponding status bit(s) to be set in the Enhanced SSP Status register (SSSR). The Interrupt and/or service request, caused by the setting of one of these test bits, will remain active until the test bit is cleared by writing a 0 it. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A0000h] + Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD1:** Reserved
7	0x0 RW	**Test Receive FIFO overrun (TROR):** 0 = No receive FIFO overrun service request 1 = Generates non-maskable interrupt to CPU. No DMA request is generated
6	0x0 RW	**Test Receive FIFO service request (TRFS):** 0 = No receive FIFO service request 1 = Generates non-maskable interrupt to CPU and a DMA request for receive FIFO

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**Test Transmit FIFO service request (TTFS):** 0 = No transmit FIFO service request pending 1 = Generates non-maskable interrupt to CPU and a DMA request for transmit FIFO
4:0	0x0 RO	**RSVD2:** Reserved

8.6.5 SSP Data Register (SSDR)—Offset 10h

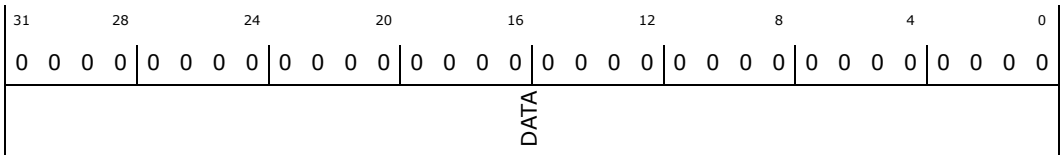
The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO, the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.TFL, SSSR.RFL, SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32-bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32-bits is automatically right-justified in the Receive FIFO. When the Enhanced SSP is programmed for National Semiconductor Microwire* frame format and if the size for Transmit data is 8-bits as selected by SSCR1.MWDS=0, then the most significant 24-bits are ignored. Similarly, if the size for the Transmit data is 16-bit as selected by SSCR1.MWDS=1, then most significant 16-bits are ignored. The SSCR0.DSS field controls the Receive data size.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A0000h] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Data (DATA):** Data word to be written to/read from transmit/receive FIFO. When reading from this register when the SSP is disabled (SSE=0) then this will return indeterminate data.

8.6.6 SSP Time-Out Regsiter (SSTO)—Offset 28h

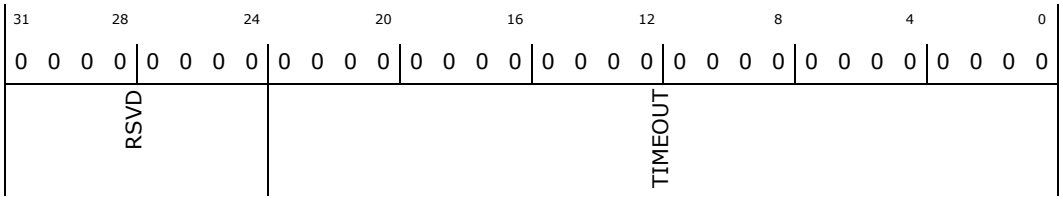
The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A0000h] + 28h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD:** Reserved
23:0	0x0 RW	**Timeout Value (TIMEOUT):** Is the value that defines the timeout interval, given by TIMEOUT/Peripheral Clock Frequency

8.6.7 SSP Programmable Protocol Register (SSPSP)—Offset 2Ch

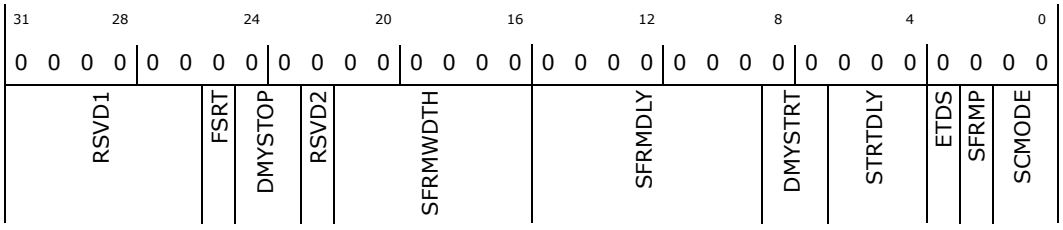
The Enhanced SSP Programmable Protocol registers are read-write registers that contain eight fields that are used to program the various programmable serial-protocol parameters. When using PSP format in Network mode, the parameters SFRMDLY, STRTDLY, DMYSTP, DMYSTRT must be set to 0. Other parameters (such as FRMPOL, SCMODE, FSRT, SFRMDWDTH) are programmable. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A0000h] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD1:** Reserved
25	0x0 RW	**Frame Sync Relative Timing Bit (FSRT):** 0 = Next frame is asserted after the end of the T4 timing 1 = Next frame is asserted with the LSB of the previous frame
24:23	0x0 RW	**Dummy Stop (DMYSTOP):** Programmed value sets the number of SSPSCLK cycles that follow the transmitted data
22	0x0 RW	**RSVD2:** Reserved
21:16	0x0 RW	**Serial Frame Width (SFRMWDTH):** Programmed value sets frame width (1-38)
15:9	0x0 RW	**Serial Frame Delay (SFRMDLY):** Programmed value sets the number of half SSPSCLK cycles from TXD/RXD being driven to SSPSFRM being asserted (0-74)
8:7	0x0 RW	**Dummy Start (DMYSTRT):** Programmed value sets the number of SSPSCLKs after STRTDLY is complete that precede the transmit/receive data
6:4	0x0 RW	**Start Delay (STRTDLY):** Programmed value sets start delay that is used to set the idle time of SSPSCLK between transfers (0-7 SSPSCLK periods)
3	0x0 RW	**End of Transfer Data State (ETDS):** 0 = Low 1 = Last value (bit 0)
2	0x0 RW	**Serial Frame Polarity (SFRMP):** 0 = SSPSFRM is active low 1 = SSPSFRM is active high
1:0	0x0 RW	**Serial bit-rate Clock Mode (SCMODE):** 00 = Data driven (falling), Data sampled (rising), Idle state (low) 01 = Data driven (rising), Data sampled (falling), Idle state (low) 10 = Data driven (rising), Data sampled (falling), Idle state (high) 11 = Data driven (falling), Data sampled (rising), Idle state (high)

8.6.8 SSM TX Time Slot Active Register (SSTSA)—Offset 30h

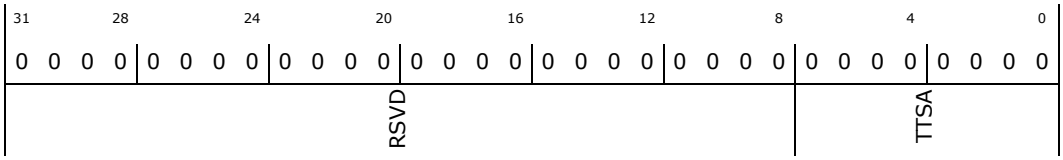
The Enhanced SSP TX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will transmit data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A0000h] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RW	**TX Time Slot Active (TTSA):** 0 = SSP will not transmit data in this time slot 1 = SSP will transmit data in this time slot

8.6.9 SSP RX Time Slot Active Register (SSRSA)—Offset 34h

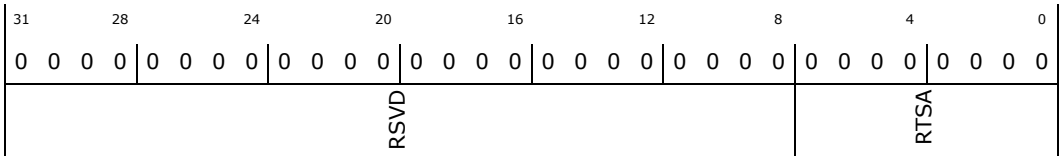
The Enhanced SSP RX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will receive data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A0000h] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RW	**RX Time Slot Active (RTSA):** 0 = SSP will not receive data in this time slot 1 = SSP will receive data in this time slot

8.6.10 SSP Time Slot Status Register (SSTSS)—Offset 38h

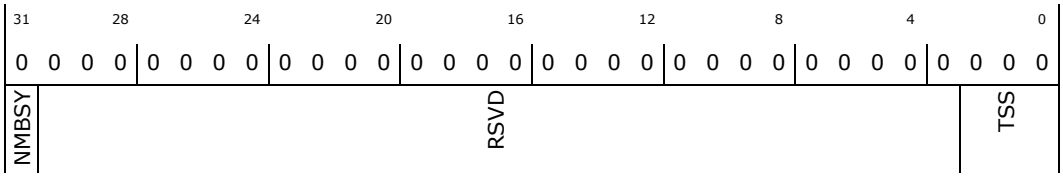
The Enhanced SSP Time Slot Status registers are read only registers that indicate which Time Slot the Enhanced SSP is currently in when the Enhanced SSP is in Network Mode (SSCR0.MOD = 1). This register is not valid when the Enhanced SSP is not in Network Mode. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A0000h] + 38h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Network Mode Busy (NMBSY):** 0 = No frame is currently active (in network mode only) 1 = SSP is in network mode and a frame is currently active
30:3	0x0 RO	**RSVD:** Reserved
2:0	0x0 RO	**Time Slot Status (TSS):** Value indicates which time slot is currently active

8.6.11 SSP Audio Clock Divider (SSACD)—Offset 3Ch

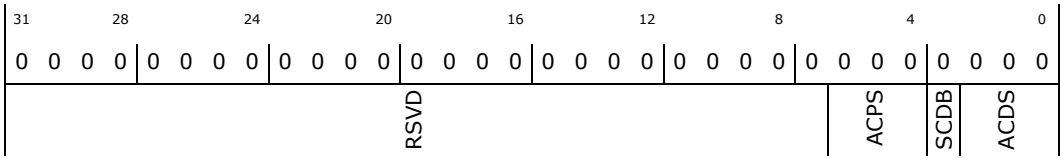
The Enhanced SSP Audio Clock Divider registers are read-write registers that indicate which clock frequency is sent to the Enhanced SSP and to the SYSCLK pin. If SSCR0.SCR is not 0, then there is no guaranteed phase relationship between SYSCLK and SSPSCLK. The SSPSFRM Frame Synch Sampling Frequency is calculated by dividing the chosen PLL output clock frequency (SSACD.ACPS) by the chosen divider (SSACD.ACDS) which gives the SYSCLK frequency. The SYSCLK is then divided by 4 (or by 1) to get the SSPSCLK. The SSPSCLK is divided by the data size (EDSS, DSS values) and by the number of time slots being used (SSCR0.FRDC value), if any, to give the SSPSFRM frequency. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined. It's important to note that this feature is only available if implemented by the project instantiation. A clock source and mux must be instantiated outside of the SSP controller for this feature to work. Only this register is designed into the SSP Controller.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A0000h] + 3Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**RSVD:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**Audio Clock PLL Select (ACPS):** Value indicates which PLL output clock is sent to the clock divider in the clock unit 000: 5.622MHz, 001: 11.345MHz, 010: 12.235MHz, 011: 14.857MHz, 100: 32.842MHz, 101: 48.000MHz, 110, 111: Reserved
3	0x0 RW	**SYSCLK Divider Bypass (SCDB):** 0 = SYSCLK is divided by 4 before being sent to SSP 1 = SYSCLK is not divided before being sent to SSP
2:0	0x0 RW	**Audio Clock Divider Select (ACDS):** Value indicates which divider will be used by the clock unit to create the SYSCLK output pin. Clock divider value will be 2^ACDS, max ACDS = 5.

8.6.12 SSP Control 2 Register (SSCR2)—Offset 40h

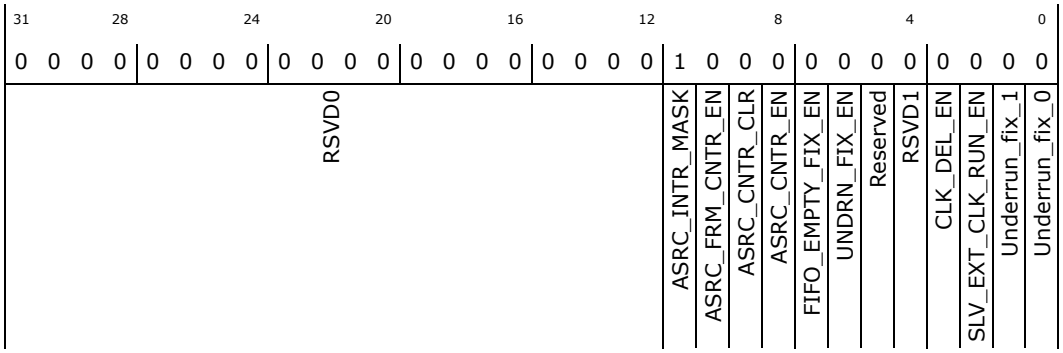
The command status register 2 is extension of command status register and contains various feature enable and disables.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A0000h] + 40h

Default: 00000800h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RSVD0:** Reserved
11	0x1 RW	**ASRC Interrupt Mask (ASRC_INTR_MASK):** Setting this bit to 1 masks the ASRC interrupt that is generated every time the frame count matches the frame threshold.
10	0x0 RW	**ASRC frame count enable (ASRC_FRM_CNTR_EN):** Setting this bit enables the frame counter to start running. Clearing this bit will make the frame counter go back to zero immediately.

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RW/AC	**ASRC Counter Clear (ASRC_CNTR_CLR):** Setting this to 1 will clear the ASRC Free running counter. This bit will self clear after the counter is cleared.
8	0x0 RW	**ASRC Counter enable (ASRC_CNTR_EN):** Setting this bit makes the Free running ASRC counter to start running. Clearing this bit will make it pause and hold it's current value.
7	0x0 RW	**Fifo empty fix enable (FIFO_EMPTY_FIX_EN):** Corner cases between the FIFO empty and APB writes happening to the TX FIFO around the time the new data needs to be sent out on the TXD are fixed with this bit.
6	0x0 RW	**Underrun fix enable (UNDRN_FIX_EN):** OSC to PLL switch along with underrun was causing unexpected behavior. This bit enables the fix for that bug.
5	0x0 RW	**Reserved:** This is a RW bit with no effect on IP behavior
4	0x0 RO	**RSVD1:** Reserved
3	0x0 RW	**Clock Delay Enable (CLK_DEL_EN):** When CLK_DEL_EN = 0, delay logic for capturing data from device is disabled. When CLK_DEL_EN = 1, delay logic for capturing data from device is delayed by half a period of the IO clock
2	0x0 RW	**Slave Mode External Clock Run Enable (SLV_EXT_CLK_RUN_EN):** When in Slave mode the receive state machine requires several clock edges (around 6) to properly sample incoming data. This bit enables a free running clock to the receive state machine before any data is received to properly sample the incoming data. 0 = Disable 1 = Enable
1	0x0 RW	**Mode 1 Underrun Fix (Underrun_fix_1):** Mode 1 of transmit underrun fix. In this mode, new data will start on the underrun slot. This function is only appled to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1 If both underrun modes are enable, mode 1 has higher priority.
0	0x0 RW	**Mode 0 Underrun Fix (Underrun_fix_0):** Mode 0 of transmit underrun fix. In this mode, new data will always start at slot 0. This function is only applied to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1

8.6.13 SSP Frame Select Register (SSFS)—Offset 44h

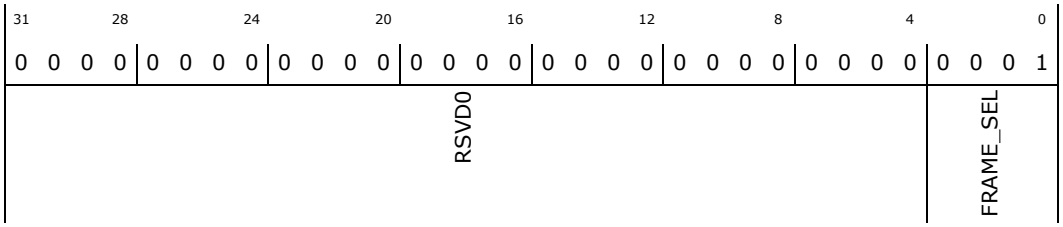
The SSP Frame select register is used to choose which frame signal to assert when accessing a slave device. SW drivers should set this register to assert the correct frame select to the targetted device.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A0000h] + 44h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RSVD0:** Reserved
3:0	0x1 RW	**Frame Select Enable (FRAME_SEL):** Each bit in this field corresponds to a frame signal of the SSP Controller. Not all SSP controllers have all frame selects pinned out so consult the pin list for indication of which SSP controllers support how many frame signals. [Bit 0] Frame Select 0 Master and Slave Supported [Bit 1] Frame Select 1 Master Only [Bit 2] Frame Select 2 Master Only [Bit 3] Frame Select 3 Master Only 0 = Frame Select Disabled 1 = Frame Select Enabled

8.6.14 SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h

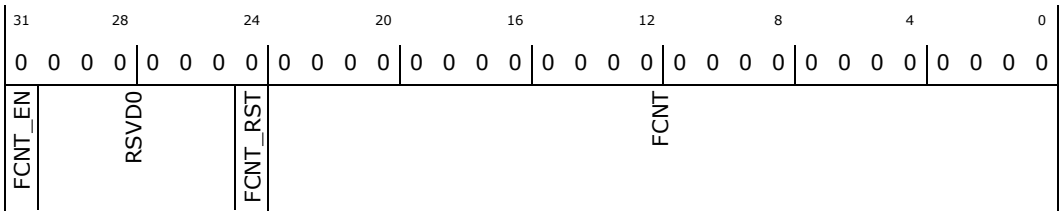
The slot frame counter is typically used in Audio modes and increments the counter every two SSPSCLKs. This allows the OS to check the progress of a transfer. Since the SSP can support upto 8 slots in network mode there are 8 slot frame counters.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset[0-7]: [Ipe_bridge.BAR + A0000h] + 48h + [0-7]*4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Slot Frame Count Enable (FCNT_EN):** 0 = Disable frame counter. 1 = Enable frame counter.
30:25	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
24	0x0 WO	**Slot Frame Count Reset (FCNT_RST):** SSP frame counter reset. Writing a 1 to this bit clears the frame counter.
23:0	0x0 RO	**Slot Frame Count (FCNT):** SSP frame count.

8.6.15 SSP FIFO Level Register (SFIFOL)—Offset 68h

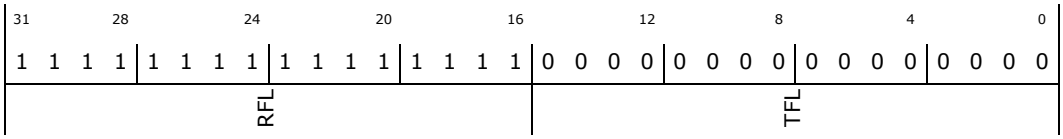
The SFIFOL register describes the current state of the RX and TX FIFOs. Not all bits of the TFL and RFL fields are used and depends on the actual hardware FIFO depth used in the instantiation of the SSP controller. This FIFO level register is meant to replace the SSSR.TFL and SSR.RFL fields.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A0000h] + 68h

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value of all 0xF's are read, the FIFO is either empty or full and the programmer should refer to the SSSR.RNE bit.
15:0	0x0 RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the SSSR.TNF bit.

8.6.16 SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch

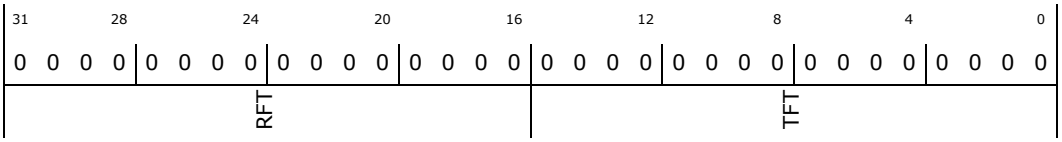
The SFIFOTT is a register that determines when the the FIFOs will assert an interrupt for FIFO full indication. This is meant to replace the SSCR1.RFT and SSCR1.TFT legacy registers. The max size of these registers is based on the actualy FIFO depth in hardware and not the actual size of the bit field.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A0000h] + 6Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. Notes on setting the RFT value. This applies to cases where SSP is receiving data from a device and is interfaced with a DMA channel via the hardware handshake mechanism. Please follow the following recommendations: 1. Number of bits denoted by the (DSS, EDSS) parameters in the SSP should match the SRC_TR_WIDTH programmed in the DMA channel. 2. (RFT+1) should be equal to (SRC_MSIZE). 3. Another option to 2 is to keep the BLOCK_TS in the DMA to be a multiple of (RFT+1)
15:0	0x0 RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.

8.6.17 SSP Control 3 Register (SSCR3)—Offset 70h

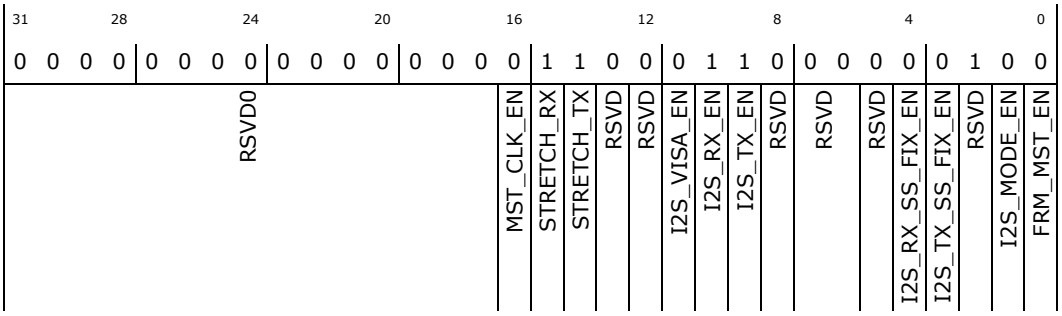
Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A0000h] + 70h

Default: 0000C604h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW	**Master Mode Clock Enable (MST_CLK_EN):** When in single slot master mode (which is the mode used for emulating I2S or LJ master mode), the SSP core can stop the clock on a Tx underflow condition, preventing the Rx side from receiving data. This bit, when set, forces the clock to run when a Tx underflow happens, thereby allowing Rx side to continue functioning while Tx side is in underflow. SW should set this bit when I2S or LJ master mode is enabled i.e. bits 0 and 1 in this register are both set or when using 1-slot PCM (SFS or LFS) master mode operation. Otherwise, SW should leave this at 0.
15	0x1 RW	**Stretch RX Pulse (STRETCH_RX):** HW uses this as a chicken bit to stretch the RX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
14	0x1 RW	**Stretch TX Pulse (STRETCH_TX):** HW uses this as a chicken bit to stretch the TX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
13	0x0 RO	**Reserved (RSVD):** Reserved.
12	0x0 RO	**Reserved (RSVD):** Reserved.
11	0x0 RW	**I2S VISA Enable (I2S_VISA_EN):** Enables newly added I2S and PCM wrapper logic debug signals sent out on the VISA bus instead of the core SSP debug signals. 0 = Core SSP Debug Signals 1 = New I2S and PCM Debug Signals
10	0x1 RW	**I2S Receive Enable (I2S_RX_EN):** When set, this bit enables data to be received on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
9	0x1 RW	**I2S Transmit Enable (I2S_TX_EN):** When set, this bit enables data to be transmitted on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
8	0x0 RO	**Reserved (RSVD):** Reserved.
7:6	0x0 RO	**Reserved (RSVD):** Reserved.
5	0x0 RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**I2S RX Slot Swap Fix Enable (I2S_RX_SS_FIX_EN):** This bit enables the Rx overrun fix in I2S or LJ modes and prevents channel swapping when Rx overrun happens. Note that this bit does not apply to any PCM modes. PCM modes still have the Rx overflow channel aliasing issue. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
3	0x0 RW	**I2S TX Slot Swap Fix Enable (I2S_TX_SS_FIX_EN):** This bit enables the TX underflow fix in I2S or LJ modes and prevents channel swapping when TX underflow happens. Note that this bit does not apply to any PCM modes. PCM modes still have the TX underflow channel aliasing issue. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
2	0x1 RO	**Reserved (RSVD):** Reserved.
1	0x0 RW	**I2S Mode Enable (I2S_MODE_EN):** This bit enables I2S Mode. In I2S mode, slave or master mode operation is selected by appropriately clearing/setting bit 0 in this register. SW should select I2S mode operation before enabling the SSP controller. 0 = Disabled 1 = Enabled
0	0x0 RW	**Frame Master Enable (FRM_MST_EN):** When set, this bit enables the internal frame generator logic that allows accurate frame rate generation. This bit should be set for I2S and PCM master mode operations and cleared for all other modes. SW should select the proper value in this bit before enabling SSP controller. 0 = Disabled 1 = Enabled

8.6.18 SSP Control 4 Register (SSCR4)—Offset 74h

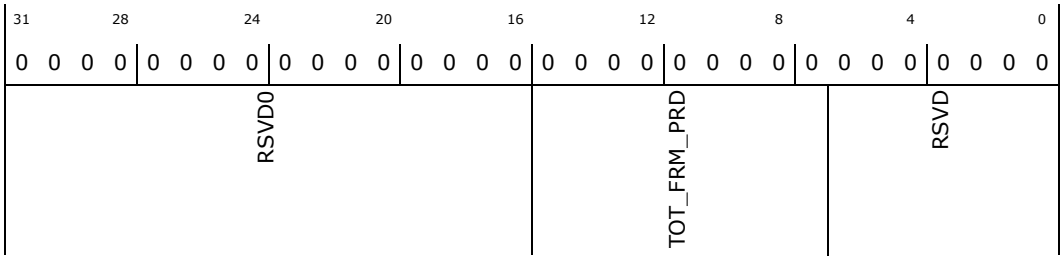
Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A0000h] + 74h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD0:** Reserved
15:7	0x0 RW	**Total Frame Period (TOT_FRM_PRD):** The total frame period (both asserted and de-asserted time of frame), measured in bit clocks, that is driven in I2S, LJ and PCM master modes. This can be controlled to get the desired accuracy on frame rate. A value of 0 and a value smaller than the value programmed in SSCR5.FrameAssertedWidth are illegal
6:0	0x0 RO	**Reserved (RSVD):** Reserved.

8.6.19 SSP Control 5 Register (SSCR5)—Offset 78h

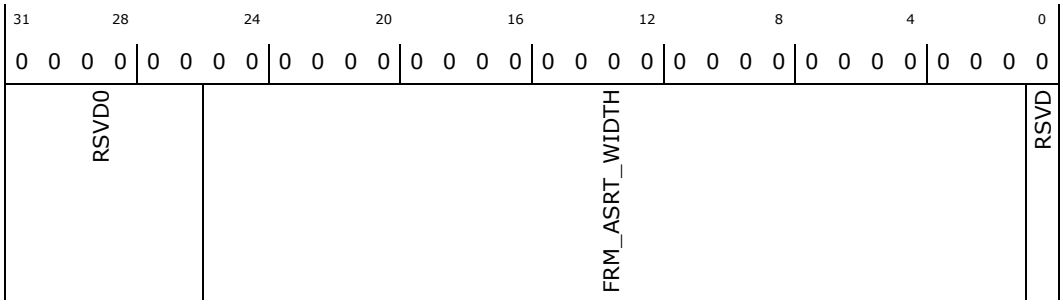
Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

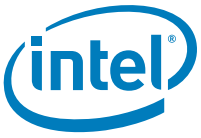
Offset: [Ipe_bridge.BAR + A0000h] + 78h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
25:1	0x0 RW	**Frame Assert Width (FRM_ASRT_WIDTH):** This field controls the width of the asserted period of frame in I2S, LJ and PCM master modes. A value of 1 indicates a width of 2 bit clock period, 2 indicates a width of 3 bit clock periods, etc. The frame width is Frame Assert Width + 1.
0	0x0 RO	**Reserved (RSVD):** Reserved.



8.7 SIO SPI 1 Memory Mapped I/O Registers

Table 58. Summary of SIO SPI 1 Memory Mapped I/O Registers—lpe_bridge.BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"SSP Control 0 Register (SSCR0)—Offset 0h" on page 3753	00000000h
4–7h	4	"SSP Control 1 Register (SSCR1)—Offset 4h" on page 3754	43000000h
8–Bh	4	"SSP Status Register (SSSR)—Offset 8h" on page 3756	0000F004h
C–Fh	4	"SSP Interupt Test Register (SSITR)—Offset Ch" on page 3758	00000000h
10–13h	4	"SSP Data Register (SSDR)—Offset 10h" on page 3759	00000000h
28–2Bh	4	"SSP Time-Out Regsiter (SSTO)—Offset 28h" on page 3760	00000000h
2C–2Fh	4	"SSP Programmable Protocol Register (SSPSP)—Offset 2Ch" on page 3760	00000000h
30–33h	4	"SSM TX Time Slot Active Register (SSTSA)—Offset 30h" on page 3761	00000000h
34–37h	4	"SSP RX Time Slot Active Register (SSRSA)—Offset 34h" on page 3762	00000000h
38–3Bh	4	"SSP Time Slot Status Register (SSTSS)—Offset 38h" on page 3762	00000000h
3C–3Fh	4	"SSP Audio Clock Divider (SSACD)—Offset 3Ch" on page 3763	00000000h
40–43h	4	"SSP Control 2 Register (SSCR2)—Offset 40h" on page 3764	00000800h
44–47h	4	"SSP Frame Select Register (SSFS)—Offset 44h" on page 3765	00000001h
48h + [0-7]*4h	4	"SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h" on page 3766	00000000h
68–6Bh	4	"SSP FIFO Level Register (SFIFOL)—Offset 68h" on page 3767	FFFF0000h
6C–6Fh	4	"SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch" on page 3767	00000000h
70–73h	4	"SSP Control 3 Register (SSCR3)—Offset 70h" on page 3768	0000C604h
74–77h	4	"SSP Control 4 Register (SSCR4)—Offset 74h" on page 3770	00000000h
78–7Bh	4	"SSP Control 5 Register (SSCR5)—Offset 78h" on page 3771	00000000h

8.7.1 SSP Control 0 Register (SSCR0)—Offset 0h

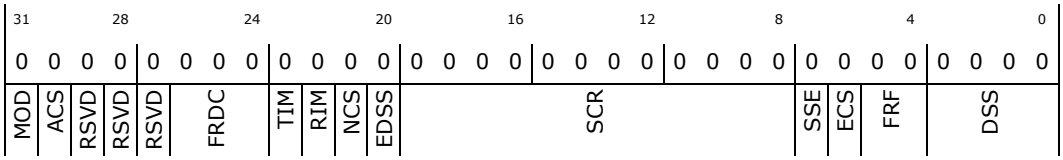
The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A1000h] + 0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Mode Select (MOD):** 0 = Normal SSP Mode 1 = Network Mode
30	0x0 RW	**Audio Clock Select (ACS):** 0 = Clock selection is determined by the NCS and ECS bits 1 = Audio Clock (and Audio Clock Divider) are used to clock the SSP's serial clock (SSPSCLK)
29	0x0 RO	**Reserved (RSVD):** Reserved.
28	0x0 RO	**Reserved (RSVD):** Reserved.
27	0x0 RO	**Reserved (RSVD):** Reserved.
26:24	0x0 RW	**Frame Rate Divider Control (FRDC):** Value 0-7 indicates the number of time slots per frame when in network mode (the actual number of time slots is FRDC+1, so 1 to 8 time slots).
23	0x0 RW	**Transmit FIFO Under Run Interrupt Mask (TIM):** 0 = TUR events will generate an SSP interrupt 1 = TUR events will not generate an SSP interrupt
22	0x0 RW	**Receive FIFO Over Run Interrupt Mask (RIM):** 0 = ROR events will generate an SSP interrupt 1 = ROR events will not generate an SSP interrupt
21	0x0 RW	**Network Clock Select (NCS):** 0 = Clock selection is determined by ECS bit 1 = Network clock is used to create the SSP's serial clock (SSPSCLK)
20	0x0 RW	**Extended Data Size Select (EDSS):** 0 = A zero is preappended to the DSS value which sets the DSS range from 4-16 bits 1 = A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits

Bit Range	Default & Access	Field Name (ID): Description
19:8	0x0 RW	**Serial Clock Rate (SCR):** Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0x0 RW	**Synchronous Serial Port Enable (SSE):** 0 = SSP operation disabled and FIFOs are cleared 1 = SSP operation enabled
6	0x0 RW	**External Clock Select (ECS):** 0 = On-chip clock used to produce the SSP's serial clock (SSPSCLK) 1 = SSPEXTCLK/GPIO pin is used to create the SSP's SSPCLK
5:4	0x0 RW	**Frame Format (FRF):** 00 = Motorola Serial Peripheral Interface (SPI) 01 = Texas Instruments Synchronous Serial Protocol (SSP) 10 = National Semiconductor Microwire 11 = Programmable Serial Protocol (PSP)
3:0	0x0 RW	**Data Size Select (DSS):** With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

8.7.2 SSP Control 1 Register (SSCR1)—Offset 4h

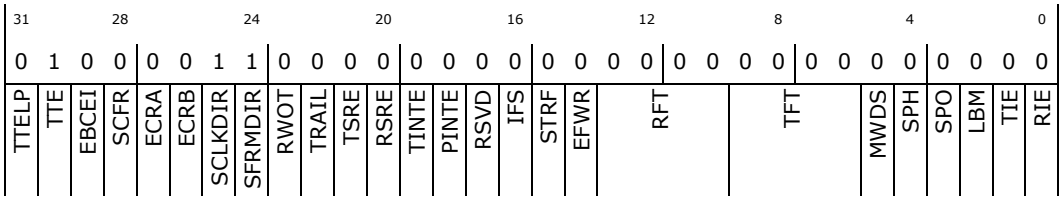
The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A1000h] + 4h

Default: 43000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**TXD Tristate Enable on Last Phase (TTELP):** 0 = TXD line will be tristated on same clock edge as TXD is to be flopped 1 = TXD line will be tristated 1/2 clock edge after TXD is to be flopped
30	0x1 RW	**TXD Tristate Enable (TTE):** 0 = TXD line will not be tristated 1 = TXD line will be tristated when no transmitting data
29	0x0 RW	**Enable Bit Count Error Interrupt (EBCEI):** 0 = Interrupt due to a bit count error is disabled 1 = Interrupt due to a bit count error is enabled

Bit Range	Default & Access	Field Name (ID): Description
28	0x0 RW	**Slave Clock Free Running (SCFR):** 0 = clock input to SSPSCLK is continuously running 1 = clock input to SSPSCLK is only active durring transfers
27	0x0 RW	**Enable Clock Request A (ECRA):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
26	0x0 RW	**Enable Clock Request B (ECRB):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
25	0x1 RW	**SSP Serial Bit Rate Clock (SSPSCLK) Direction (SCLKDIR):** 0 = Master mode, SSP drives SSPSCLK 1 = Slave mode, SSP recieves SSPSCLK
24	0x1 RW	**SSP Frame (SSPSFRM) Direction (SFRMDIR):** 0 = Master mode, SSP drives SSPSFRM 1 = Slave mode, SSP receives SSPSFRM
23	0x0 RW	**Receive With Out Transmit (RWOT):** 0 = Transmit/Receive mode 1 = Receive without transmit mode
22	0x0 RW	**Trailing Byte (TRAIL):** 0 = Processor based, trailing bytes are handled by processor 1 = DMA based, trailing bytes are handled by DMA
21	0x0 RW	**Transmit Service Request Enable (TSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
20	0x0 RW	**Receive Service Request Enable (RSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
19	0x0 RW	**Receiver Time-out Interrupt Enable (TINTE):** 0 = Receiver Time-out interrupts are disabled 1 = Receiver Time-out interrupts are enabled
18	0x0 RW	**Peripheral Trailing Byte Interrupts Enable (PINTE):** 0 = Peripheral Trailing Byte Interrupts are disabled 1 = Peripheral Trailing Byte Interrupts are enabled
17	0x0 RW	**RSVD:** Reserved
16	0x0 RW	**Invert Frame Signal (IFS):** 0 = Frame polarity is determined by SSP format and PSP polarity bits 1 = Frame signal will be inverted from the normal SSP frame signal (as defined by the SSP format nad PSP polarity bits)
15	0x0 RW	**Select FIFO for EFWR (test mode bit) (when EFWR=1) (STRF):** 0 = Transmit FIFO is selected for both writes and reads through the SSP Data Register (SSDR) 1 = Receive FIFO is selected for both writes and reads through the SSP Data Register (SSDR)
14	0x0 RW	**Enable FIFO Write/Read (test mode bit) (EFWR):** 0 = FIFO write/read special function is disabled (normal SSP operational mode) 1 = FIFO write/read special function is enabled

Bit Range	Default & Access	Field Name (ID): Description
13:10	0x0 RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
9:6	0x0 RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
5	0x0 RW	**Microwire Transmit Data Size (MWDS):** 0 = 8-bit command words are transmitted 1 = 16-bit command words are transmitted
4	0x0 RW	**Motorola SPI SSPSCLK Phase Setting (SPH):** 0 = SSPSCLK is inactive one sycle at the start of a fram and 1/2 cycle at the end of a frame 1 = SSPSCLK is inactive 1/2 cycle at the start of a frame and one cycle at the end of a frame
3	0x0 RW	**Motorola SPI SSPSCLK polarity setting (SPO):** 0 = The inactive or idle state of SSPSCLK is low 1 = The inactive or idle state of SSPSCLK is high
2	0x0 RW	**Loop-Back Mode (test mode bit) (LBM):** 0 = Normal serial port operation enabled 1 = Output of transmit serial shifter connected to input of receive serial shifter, internally
1	0x0 RW	**Transmit FIFO Interrupt Enable (TIE):** 0 = Transmit FIFO level interrupt is disabled 1 = Transmit FIFO level interrupt is enabled
0	0x0 RW	**Receive FIFO Interrupt Enable (RIE):** 0 = Receive FIFO level interrupt is disabled 1 = Receive FIFO level interrupt is enabled

8.7.3 SSP Status Register (SSSR)—Offset 8h

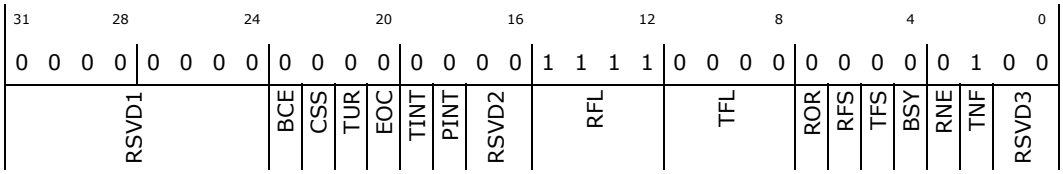
The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A1000h] + 8h

Default: 0000F004h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD1:** Reserved
23	0x0 RW/1C	**Bit Count Error (BCE):** 0 = SSP has not experienced a bit count error 1 = SSPSFRM signal has been asserted when the bit counter was not 0
22	0x0 RO	**Clock Synchronization Status (CSS):** 0 = SSP is ready for slave clock operations 1 = SSP is currently busy synchronizing slave mode signals
21	0x0 RW/1C	**Transmit FIFO Under Run (TUR):** 0 = Transmit FIFO has not experienced an under run 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0x0 RW/1C	**End of Chain (EOC):** 0 = DMA has not signaled an end of chain condition 1 = DMA has signaled an end of chain condition
19	0x0 RW/1C	**Receiver Time-out Interrupt (TINT):** 0 = No receiver time-out pending 1 = Receiver time-out pending
18	0x0 RW/1C	**Peripheral Trailing Byte Interrupt (PINT):** 0 = No peripheral trailing byte interrupt pending 1 = Peripheral trailing byte interrupt pending
17:16	0x0 RO	**RSVD2:** Reserved
15:12	0xf RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value 0xF is read, the FIFO is either empty or full and the programmer should refer to the RNE bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
11:8	0x0 RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the TNF bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
7	0x0 RW/1C	**Receive FIFO Overrun (ROR):** 0 = Receive FIFO has not experienced an overrun 1 = Attempted data write to full receive FIFO, request interrupt
6	0x0 RO	**Receive FIFO Service Request (RFS):** 0 = Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0x0 RO	**Transmit FIFO Service Request (TFS):** 0 = Transmit FIFO level exceeds the TFT threshold (TFT+1), or SSP disabled 1 = Transmit FIFO level is at or below TFT threshold (TFT+1), request interrupt

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RO	**SSP Busy (BSY):** 0 = SSP is idle or disabled 1 = SSP currently transmitting or receiving a frame
3	0x0 RO	**Receive FIOF Not Empty (RNE):** 0 = Receive FIFO is empty 1 = Receive FIFO is not empty
2	0x1 RO	**Transmit FIFO Not Full (TNF):** 0 = Transmit FIFO is full 1 = Transmit FIFO is not full
1:0	0x0 RO	**RSVD3:** Reserved

8.7.4 SSP Interupt Test Register (SSITR)—Offset Ch

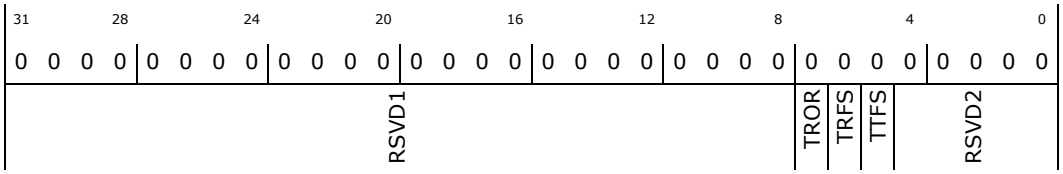
The read-write SSP Interrupt Test registers should be used only for testing purposes. Writing a 1 to the test transmit FIFO request SSITR.TTFS, bit 5, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Transmit FIFO. Writing a 1 to the test receive FIFO request SSITR.TRFS, bit 6, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Receive FIFO. Writing a 1 to the test receive FIFO overrun bit SSITR.TROR, bit 7, will generate a non-maskable Interrupt strobe signal to the Interrupt controller only, no DMA request will be made. Setting any of these bits will also cause the corresponding status bit(s) to be set in the Enhanced SSP Status register (SSSR). The Interrupt and/or service request, caused by the setting of one of these test bits, will remain active until the test bit is cleared by writing a 0 it. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A1000h] + Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD1:** Reserved
7	0x0 RW	**Test Receive FIFO overrun (TROR):** 0 = No receive FIFO overrun service request 1 = Generates non-maskable interrupt to CPU. No DMA request is generated
6	0x0 RW	**Test Receive FIFO service request (TRFS):** 0 = No receive FIFO service request 1 = Generates non-maskable interrupt to CPU and a DMA request for receive FIFO

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**Test Transmit FIFO service request (TTFS):** 0 = No transmit FIFO service request pending 1 = Generates non-maskable interrupt to CPU and a DMA request for transmit FIFO
4:0	0x0 RO	**RSVD2:** Reserved

8.7.5 SSP Data Register (SSDR)—Offset 10h

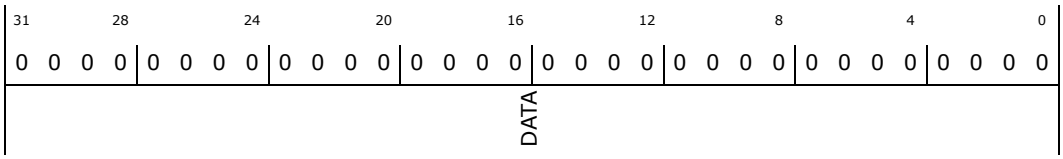
The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO, the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.TFL, SSSR.RFL, SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32-bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32-bits is automatically right-justified in the Receive FIFO. When the Enhanced SSP is programmed for National Semiconductor Microwire* frame format and if the size for Transmit data is 8-bits as selected by SSCR1.MWDS=0, then the most significant 24-bits are ignored. Similarly, if the size for the Transmit data is 16-bit as selected by SSCR1.MWDS=1, then most significant 16-bits are ignored. The SSCR0.DSS field controls the Receive data size.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A1000h] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Data (DATA):** Data word to be written to/read from transmit/receive FIFO. When reading from this register when the SSP is disabled (SSE=0) then this will return indeterminate data.

8.7.6 SSP Time-Out Regsiter (SSTO)—Offset 28h

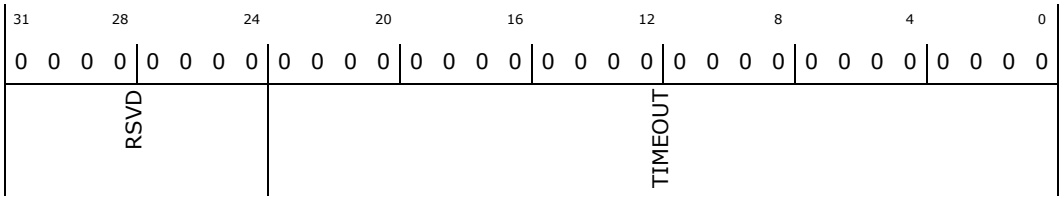
The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A1000h] + 28h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD:** Reserved
23:0	0x0 RW	**Timeout Value (TIMEOUT):** Is the value that defines the timeout interval, given by TIMEOUT/Peripheral Clock Frequency

8.7.7 SSP Programmable Protocol Register (SSPSP)—Offset 2Ch

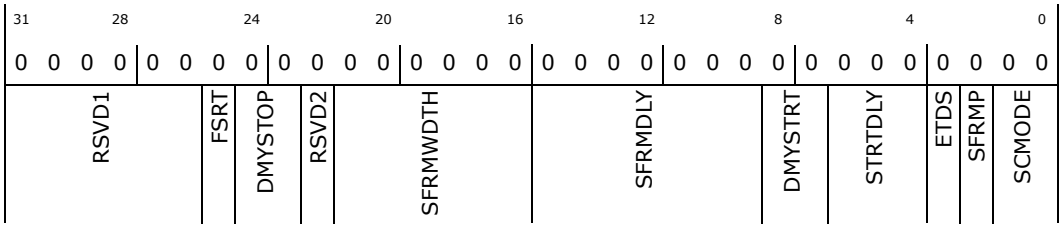
The Enhanced SSP Programmable Protocol registers are read-write registers that contain eight fields that are used to program the various programmable serial-protocol parameters. When using PSP format in Network mode, the parameters SFRMDLY, STRTDLY, DMYSTP, DMYSTRT must be set to 0. Other parameters (such as FRMPOL, SCMODE, FSRT, SFRMDWDTH) are programmable. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A1000h] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD1:** Reserved
25	0x0 RW	**Frame Sync Relative Timing Bit (FSRT):** 0 = Next frame is asserted after the end of the T4 timing 1 = Next frame is asserted with the LSB of the previous frame
24:23	0x0 RW	**Dummy Stop (DMYSTOP):** Programmed value sets the number of SSPSCLK cycles that follow the transmitted data
22	0x0 RW	**RSVD2:** Reserved
21:16	0x0 RW	**Serial Frame Width (SFRMWDTH):** Programmed value sets frame width (1-38)
15:9	0x0 RW	**Serial Frame Delay (SFRMDLY):** Programmed value sets the number of half SSPSCLK cycles from TXD/RXD being driven to SSPSFRM being asserted (0-74)
8:7	0x0 RW	**Dummy Start (DMYSTRT):** Programmed value sets the number of SSPSCLKs after STRTDLY is complete that precede the transmit/receive data
6:4	0x0 RW	**Start Delay (STRTDLY):** Programmed value sets start delay that is used to set the idle time of SSPSCLK between transfers (0-7 SSPSCLK periods)
3	0x0 RW	**End of Transfer Data State (ETDS):** 0 = Low 1 = Last value (bit 0)
2	0x0 RW	**Serial Frame Polarity (SFRMP):** 0 = SSPSFRM is active low 1 = SSPSFRM is active high
1:0	0x0 RW	**Serial bit-rate Clock Mode (SCMODE):** 00 = Data driven (falling), Data sampled (rising), Idle state (low) 01 = Data driven (rising), Data sampled (falling), Idle state (low) 10 = Data driven (rising), Data sampled (falling), Idle state (high) 11 = Data driven (falling), Data sampled (rising), Idle state (high)

8.7.8 SSM TX Time Slot Active Register (SSTSA)—Offset 30h

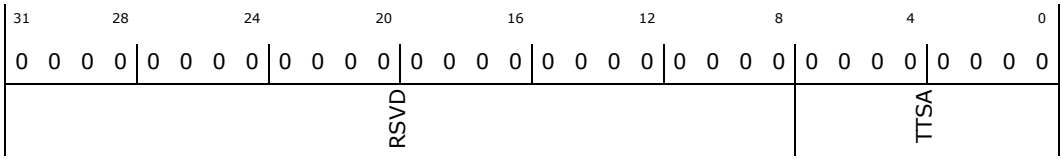
The Enhanced SSP TX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will transmit data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A1000h] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RW	**TX Time Slot Active (TTSA):** 0 = SSP will not transmit data in this time slot 1 = SSP will transmit data in this time slot

8.7.9 SSP RX Time Slot Active Register (SSRSA)—Offset 34h

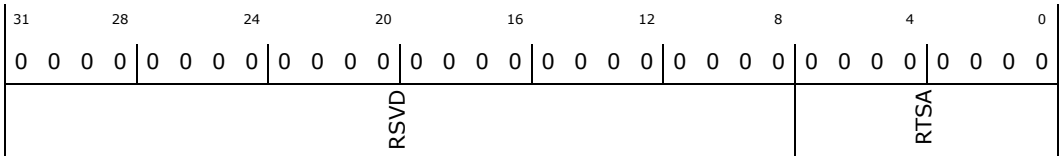
The Enhanced SSP RX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will receive data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A1000h] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RW	**RX Time Slot Active (RTSA):** 0 = SSP will not receive data in this time slot 1 = SSP will receive data in this time slot

8.7.10 SSP Time Slot Status Register (SSTSS)—Offset 38h

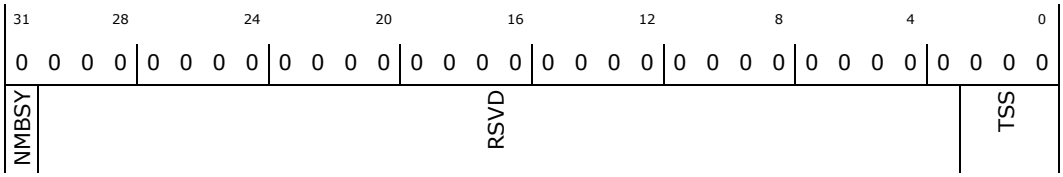
The Enhanced SSP Time Slot Status registers are read only registers that indicate which Time Slot the Enhanced SSP is currently in when the Enhanced SSP is in Network Mode (SSCR0.MOD = 1). This register is not valid when the Enhanced SSP is not in Network Mode. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A1000h] + 38h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Network Mode Busy (NMBSY):** 0 = No frame is currently active (in network mode only) 1 = SSP is in network mode and a frame is currently active
30:3	0x0 RO	**RSVD:** Reserved
2:0	0x0 RO	**Time Slot Status (TSS):** Value indicates which time slot is currently active

8.7.11 SSP Audio Clock Divider (SSACD)—Offset 3Ch

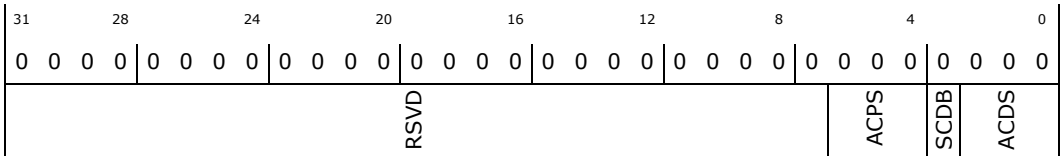
The Enhanced SSP Audio Clock Divider registers are read-write registers that indicate which clock frequency is sent to the Enhanced SSP and to the SYSCLK pin. If SSCR0.SCR is not 0, then there is no guaranteed phase relationship between SYSCLK and SSPSCLK. The SSPSFRM Frame Synch Sampling Frequency is calculated by dividing the chosen PLL output clock frequency (SSACD.ACPS) by the chosen divider (SSACD.ACDS) which gives the SYSCLK frequency. The SYSCLK is then divided by 4 (or by 1) to get the SSPSCLK. The SSPSCLK is divided by the data size (EDSS, DSS values) and by the number of time slots being used (SSCR0.FRDC value), if any, to give the SSPSFRM frequency. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined. It's important to note that this feature is only available if implemented by the project instantiation. A clock source and mux must be instantiated outside of the SSP controller for this feature to work. Only this register is designed into the SSP Controller.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A1000h] + 3Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**RSVD:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**Audio Clock PLL Select (ACPS):** Value indicates which PLL output clock is sent to the clock divider in the clock unit 000: 5.622MHz, 001: 11.345MHz, 010: 12.235MHz, 011: 14.857MHz, 100: 32.842MHz, 101: 48.000MHz, 110, 111: Reserved
3	0x0 RW	**SYSCLK Divider Bypass (SCDB):** 0 = SYSCLK is divided by 4 before being sent to SSP 1 = SYSCLK is not divided before being sent to SSP
2:0	0x0 RW	**Audio Clock Divider Select (ACDS):** Value indicates which divider will be used by the clock unit to create the SYSCLK output pin. Clock divider value will be 2^ACDS, max ACDS = 5.

8.7.12 SSP Control 2 Register (SSCR2)—Offset 40h

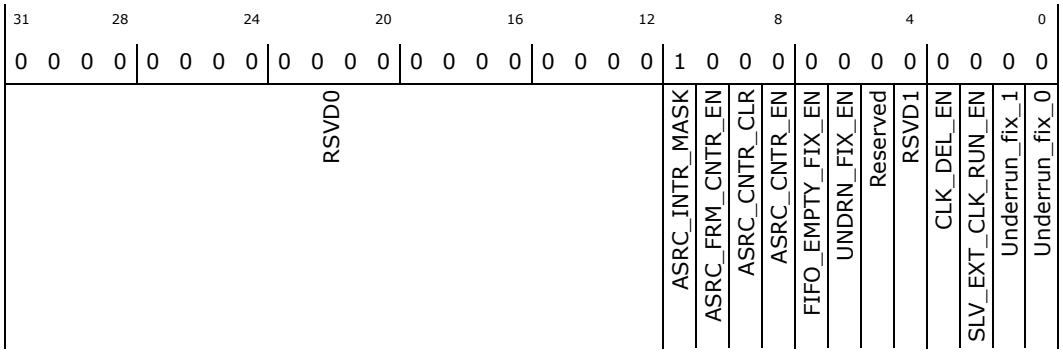
The command status register 2 is extension of command status register and contains various feature enable and disables.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A1000h] + 40h

Default: 00000800h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RSVD0:** Reserved
11	0x1 RW	**ASRC Interrupt Mask (ASRC_INTR_MASK):** Setting this bit to 1 masks the ASRC interrupt that is generated every time the frame count matches the frame threshold.
10	0x0 RW	**ASRC frame count enable (ASRC_FRM_CNTR_EN):** Setting this bit enables the frame counter to start running. Clearing this bit will make the frame counter go back to zero immediately.

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RW/AC	**ASRC Counter Clear (ASRC_CNTR_CLR):** Setting this to 1 will clear the ASRC Free running counter. This bit will self clear after the counter is cleared.
8	0x0 RW	**ASRC Counter enable (ASRC_CNTR_EN):** Setting this bit makes the Free running ASRC counter to start running. Clearing this bit will make it pause and hold it's current value.
7	0x0 RW	**Fifo empty fix enable (FIFO_EMPTY_FIX_EN):** Corner cases between the FIFO empty and APB writes happening to the TX FIFO around the time the new data needs to be sent out on the TXD are fixed with this bit.
6	0x0 RW	**Underrun fix enable (UNDRN_FIX_EN):** OSC to PLL switch along with underrun was causing unexpected behavior. This bit enables the fix for that bug.
5	0x0 RW	**Reserved:** This is a RW bit with no effect on IP behavior
4	0x0 RO	**RSVD1:** Reserved
3	0x0 RW	**Clock Delay Enable (CLK_DEL_EN):** When CLK_DEL_EN = 0, delay logic for capturing data from device is disabled. When CLK_DEL_EN = 1, delay logic for capturing data from device is delayed by half a period of the IO clock
2	0x0 RW	**Slave Mode External Clock Run Enable (SLV_EXT_CLK_RUN_EN):** When in Slave mode the receive state machine requires several clock edges (around 6) to properly sample incoming data. This bit enables a free running clock to the receive state machine before any data is received to properly sample the incoming data. 0 = Disable 1 = Enable
1	0x0 RW	**Mode 1 Underrun Fix (Underrun_fix_1):** Mode 1 of transmit underrun fix. In this mode, new data will start on the underrun slot. This function is only appled to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1 If both underrun modes are enable, mode 1 has higher priority.
0	0x0 RW	**Mode 0 Underrun Fix (Underrun_fix_0):** Mode 0 of transmit underrun fix. In this mode, new data will always start at slot 0. This function is only applied to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1

8.7.13 SSP Frame Select Register (SSFS)—Offset 44h

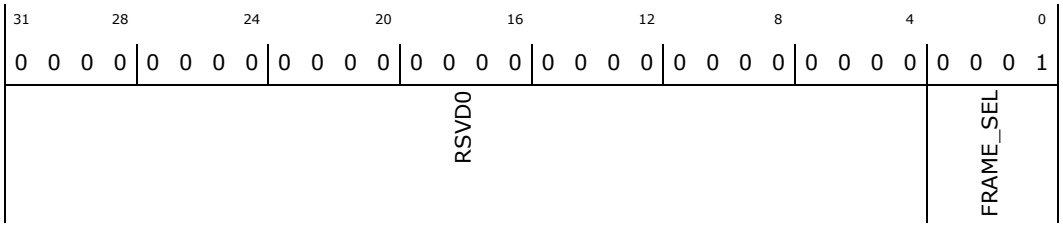
The SSP Frame select register is used to choose which frame signal to assert when accessing a slave device. SW drivers should set this register to assert the correct frame select to the targetted device.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A1000h] + 44h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RSVD0:** Reserved
3:0	0x1 RW	**Frame Select Enable (FRAME_SEL):** Each bit in this field corresponds to a frame signal of the SSP Controller. Not all SSP controllers have all frame selects pinned out so consult the pin list for indication of which SSP controllers support how many frame signals. [Bit 0] Frame Select 0 Master and Slave Supported [Bit 1] Frame Select 1 Master Only [Bit 2] Frame Select 2 Master Only [Bit 3] Frame Select 3 Master Only 0 = Frame Select Disabled 1 = Frame Select Enabled

8.7.14 SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h

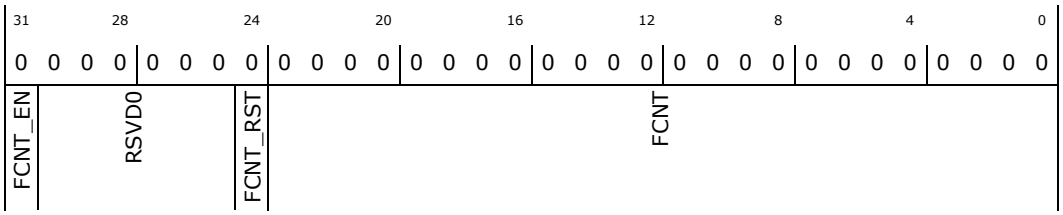
The slot frame counter is typically used in Audio modes and increments the counter every two SSPSCLKs. This allows the OS to check the progress of a transfer. Since the SSP can support upto 8 slots in network mode there are 8 slot frame counters.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset[0-7]: [Ipe_bridge.BAR + A1000h] + 48h + [0-7]*4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Slot Frame Count Enable (FCNT_EN):** 0 = Disable frame counter. 1 = Enable frame counter.
30:25	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
24	0x0 WO	**Slot Frame Count Reset (FCNT_RST):** SSP frame counter reset. Writing a 1 to this bit clears the frame counter.
23:0	0x0 RO	**Slot Frame Count (FCNT):** SSP frame count.

8.7.15 SSP FIFO Level Register (SFIFOL)—Offset 68h

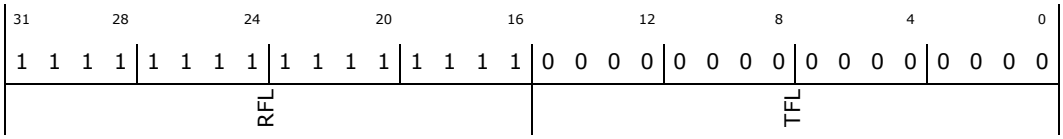
The SFIFOL register describes the current state of the RX and TX FIFOs. Not all bits of the TFL and RFL fields are used and depends on the actual hardware FIFO depth used in the instantiation of the SSP controller. This FIFO level register is meant to replace the SSSR.TFL and SSR.RFL fields.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A1000h] + 68h

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value of all 0xF's are read, the FIFO is either empty or full and the programmer should refer to the SSSR.RNE bit.
15:0	0x0 RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the SSSR.TNF bit.

8.7.16 SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch

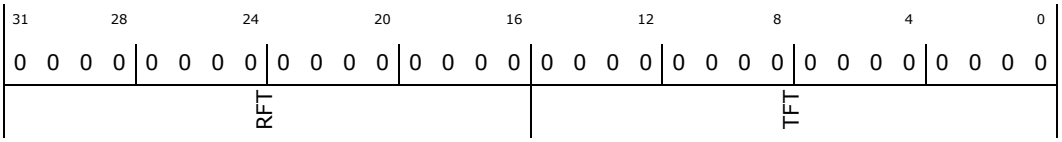
The SFIFOTT is a register that determines when the the FIFOs will assert an interrupt for FIFO full indication. This is meant to replace the SSCR1.RFT and SSCR1.TFT legacy registers. The max size of these registers is based on the actualy FIFO depth in hardware and not the actual size of the bit field.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A1000h] + 6Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. Notes on setting the RFT value. This applies to cases where SSP is receiving data from a device and is interfaced with a DMA channel via the hardware handshake mechanism. Please follow the following recommendations: 1. Number of bits denoted by the (DSS, EDSS) parameters in the SSP should match the SRC_TR_WIDTH programmed in the DMA channel. 2. (RFT+1) should be equal to (SRC_MSIZE). 3. Another option to 2 is to keep the BLOCK_TS in the DMA to be a multiple of (RFT+1)
15:0	0x0 RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.

8.7.17 SSP Control 3 Register (SSCR3)—Offset 70h

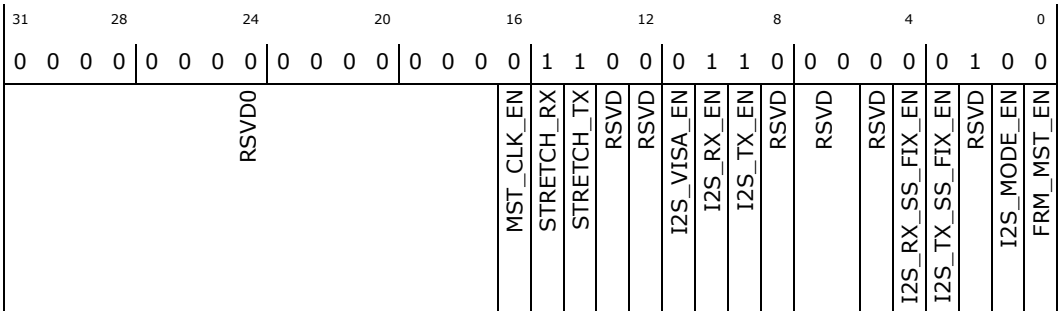
Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A1000h] + 70h

Default: 0000C604h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW	**Master Mode Clock Enable (MST_CLK_EN):** When in single slot master mode (which is the mode used for emulating I2S or LJ master mode), the SSP core can stop the clock on a Tx underflow condition, preventing the Rx side from receiving data. This bit, when set, forces the clock to run when a Tx underflow happens, thereby allowing Rx side to continue functioning while Tx side is in underflow. SW should set this bit when I2S or LJ master mode is enabled i.e. bits 0 and 1 in this register are both set or when using 1-slot PCM (SFS or LFS) master mode operation. Otherwise, SW should leave this at 0.
15	0x1 RW	**Stretch RX Pulse (STRETCH_RX):** HW uses this as a chicken bit to stretch the RX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
14	0x1 RW	**Stretch TX Pulse (STRETCH_TX):** HW uses this as a chicken bit to stretch the TX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
13	0x0 RO	**Reserved (RSVD):** Reserved.
12	0x0 RO	**Reserved (RSVD):** Reserved.
11	0x0 RW	**I2S VISA Enable (I2S_VISA_EN):** Enables newly added I2S and PCM wrapper logic debug signals sent out on the VISA bus instead of the core SSP debug signals. 0 = Core SSP Debug Signals 1 = New I2S and PCM Debug Signals
10	0x1 RW	**I2S Receive Enable (I2S_RX_EN):** When set, this bit enables data to be received on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
9	0x1 RW	**I2S Transmit Enable (I2S_TX_EN):** When set, this bit enables data to be transmitted on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
8	0x0 RO	**Reserved (RSVD):** Reserved.
7:6	0x0 RO	**Reserved (RSVD):** Reserved.
5	0x0 RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**I2S RX Slot Swap Fix Enable (I2S_RX_SS_FIX_EN):** This bit enables the Rx overrun fix in I2S or LJ modes and prevents channel swapping when Rx overrun happens. Note that this bit does not apply to any PCM modes. PCM modes still have the Rx overflow channel aliasing issue. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
3	0x0 RW	**I2S TX Slot Swap Fix Enable (I2S_TX_SS_FIX_EN):** This bit enables the TX underflow fix in I2S or LJ modes and prevents channel swapping when TX underflow happens. Note that this bit does not apply to any PCM modes. PCM modes still have the TX underflow channel aliasing issue. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
2	0x1 RO	**Reserved (RSVD):** Reserved.
1	0x0 RW	**I2S Mode Enable (I2S_MODE_EN):** This bit enables I2S Mode. In I2S mode, slave or master mode operation is selected by appropriately clearing/setting bit 0 in this register. SW should select I2S mode operation before enabling the SSP controller. 0 = Disabled 1 = Enabled
0	0x0 RW	**Frame Master Enable (FRM_MST_EN):** When set, this bit enables the internal frame generator logic that allows accurate frame rate generation. This bit should be set for I2S and PCM master mode operations and cleared for all other modes. SW should select the proper value in this bit before enabling SSP controller. 0 = Disabled 1 = Enabled

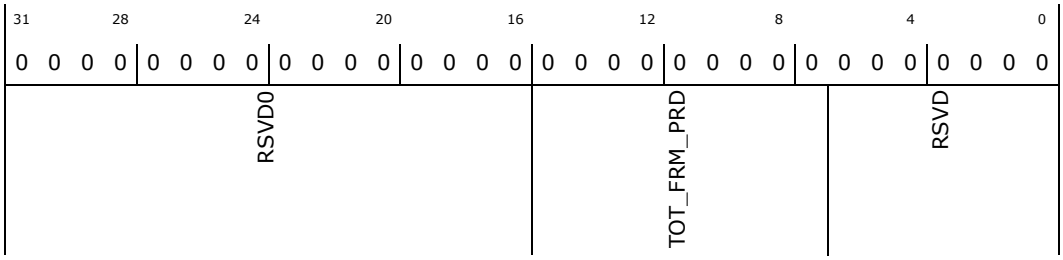
8.7.18 SSP Control 4 Register (SSCR4)—Offset 74h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** [Ipe_bridge.BAR + A1000h] + 74h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD0:** Reserved
15:7	0x0 RW	**Total Frame Period (TOT_FRM_PRD):** The total frame period (both asserted and de-asserted time of frame), measured in bit clocks, that is driven in I2S, LJ and PCM master modes. This can be controlled to get the desired accuracy on frame rate. A value of 0 and a value smaller than the value programmed in SSCR5.FrameAssertedWidth are illegal
6:0	0x0 RO	**Reserved (RSVD):** Reserved.

8.7.19 SSP Control 5 Register (SSCR5)—Offset 78h

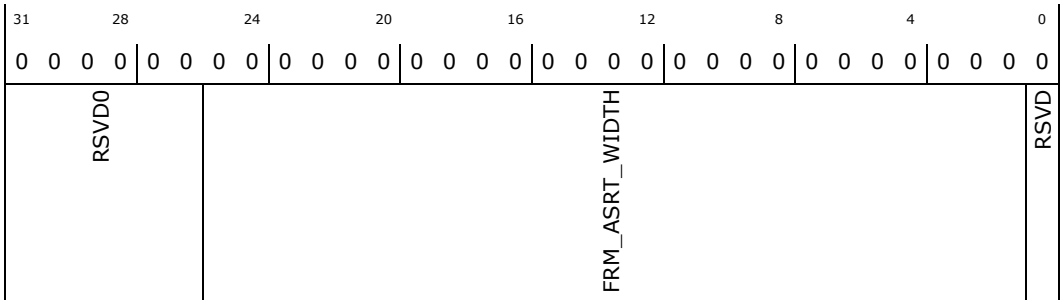
Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

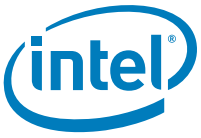
Offset: [Ipe_bridge.BAR + A1000h] + 78h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
25:1	0x0 RW	**Frame Assert Width (FRM_ASRT_WIDTH):** This field controls the width of the asserted period of frame in I2S, LJ and PCM master modes. A value of 1 indicates a width of 2 bit clock period, 2 indicates a width of 3 bit clock periods, etc. The frame width is Frame Assert Width + 1.
0	0x0 RO	**Reserved (RSVD):** Reserved.



8.8 SIO SPI 2 Memory Mapped I/O Registers

Table 59. Summary of SIO SPI 2 Memory Mapped I/O Registers—lpe_bridge.BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"SSP Control 0 Register (SSCR0)—Offset 0h" on page 3775	00000000h
4–7h	4	"SSP Control 1 Register (SSCR1)—Offset 4h" on page 3776	43000000h
8–Bh	4	"SSP Status Register (SSSR)—Offset 8h" on page 3778	0000F004h
C–Fh	4	"SSP Interupt Test Register (SSITR)—Offset Ch" on page 3780	00000000h
10–13h	4	"SSP Data Register (SSDR)—Offset 10h" on page 3781	00000000h
28–2Bh	4	"SSP Time-Out Regsiter (SSTO)—Offset 28h" on page 3782	00000000h
2C–2Fh	4	"SSP Programmable Protocol Register (SSPSP)—Offset 2Ch" on page 3782	00000000h
30–33h	4	"SSM TX Time Slot Active Register (SSTSA)—Offset 30h" on page 3783	00000000h
34–37h	4	"SSP RX Time Slot Active Register (SSRSA)—Offset 34h" on page 3784	00000000h
38–3Bh	4	"SSP Time Slot Status Register (SSTSS)—Offset 38h" on page 3784	00000000h
3C–3Fh	4	"SSP Audio Clock Divider (SSACD)—Offset 3Ch" on page 3785	00000000h
40–43h	4	"SSP Control 2 Register (SSCR2)—Offset 40h" on page 3786	00000800h
44–47h	4	"SSP Frame Select Register (SSFS)—Offset 44h" on page 3787	00000001h
48h + [0-7]*4h	4	"SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h" on page 3788	00000000h
68–6Bh	4	"SSP FIFO Level Register (SFIFOL)—Offset 68h" on page 3789	FFFF0000h
6C–6Fh	4	"SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch" on page 3789	00000000h
70–73h	4	"SSP Control 3 Register (SSCR3)—Offset 70h" on page 3790	0000C604h
74–77h	4	"SSP Control 4 Register (SSCR4)—Offset 74h" on page 3792	00000000h
78–7Bh	4	"SSP Control 5 Register (SSCR5)—Offset 78h" on page 3793	00000000h

8.8.1 SSP Control 0 Register (SSCR0)—Offset 0h

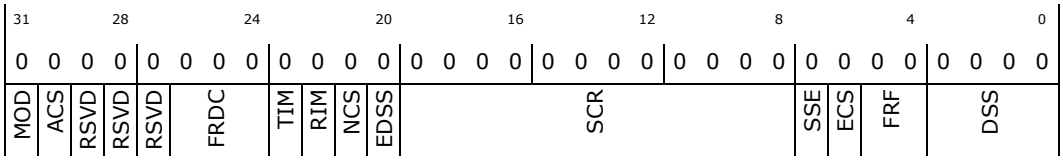
The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A2000h] + 0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Mode Select (MOD):** 0 = Normal SSP Mode 1 = Network Mode
30	0x0 RW	**Audio Clock Select (ACS):** 0 = Clock selection is determined by the NCS and ECS bits 1 = Audio Clock (and Audio Clock Divider) are used to clock the SSP's serial clock (SSPSCLK)
29	0x0 RO	**Reserved (RSVD):** Reserved.
28	0x0 RO	**Reserved (RSVD):** Reserved.
27	0x0 RO	**Reserved (RSVD):** Reserved.
26:24	0x0 RW	**Frame Rate Divider Control (FRDC):** Value 0-7 indicates the number of time slots per frame when in network mode (the actual number of time slots is FRDC+1, so 1 to 8 time slots).
23	0x0 RW	**Transmit FIFO Under Run Interrupt Mask (TIM):** 0 = TUR events will generate an SSP interrupt 1 = TUR events will not generate an SSP interrupt
22	0x0 RW	**Receive FIFO Over Run Interrupt Mask (RIM):** 0 = ROR events will generate an SSP interrupt 1 = ROR events will not generate an SSP interrupt
21	0x0 RW	**Network Clock Select (NCS):** 0 = Clock selection is determined by ECS bit 1 = Network clock is used to create the SSP's serial clock (SSPSCLK)
20	0x0 RW	**Extended Data Size Select (EDSS):** 0 = A zero is preappended to the DSS value which sets the DSS range from 4-16 bits 1 = A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits

Bit Range	Default & Access	Field Name (ID): Description
19:8	0x0 RW	**Serial Clock Rate (SCR):** Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0x0 RW	**Synchronous Serial Port Enable (SSE):** 0 = SSP operation disabled and FIFOs are cleared 1 = SSP operation enabled
6	0x0 RW	**External Clock Select (ECS):** 0 = On-chip clock used to produce the SSP's serial clock (SSPSCLK) 1 = SSPEXTCLK/GPIO pin is used to create the SSP's SSPCLK
5:4	0x0 RW	**Frame Format (FRF):** 00 = Motorola Serial Peripheral Interface (SPI) 01 = Texas Instruments Synchronous Serial Protocol (SSP) 10 = National Semiconductor Microwire 11 = Programmable Serial Protocol (PSP)
3:0	0x0 RW	**Data Size Select (DSS):** With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

8.8.2 SSP Control 1 Register (SSCR1)—Offset 4h

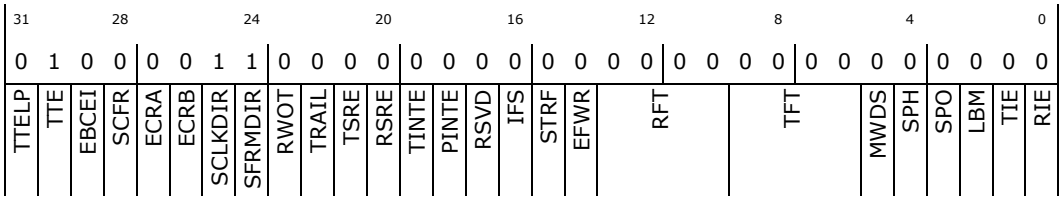
The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A2000h] + 4h

Default: 43000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**TXD Tristate Enable on Last Phase (TTELP):** 0 = TXD line will be tristated on same clock edge as TXD is to be flopped 1 = TXD line will be tristated 1/2 clock edge after TXD is to be flopped
30	0x1 RW	**TXD Tristate Enable (TTE):** 0 = TXD line will not be tristated 1 = TXD line will be tristated when no transmitting data
29	0x0 RW	**Enable Bit Count Error Interrupt (EBCEI):** 0 = Interrupt due to a bit count error is disabled 1 = Interrupt due to a bit count error is enabled

Bit Range	Default & Access	Field Name (ID): Description
28	0x0 RW	**Slave Clock Free Running (SCFR):** 0 = clock input to SSPSCLK is continuously running 1 = clock input to SSPSCLK is only active durring transfers
27	0x0 RW	**Enable Clock Request A (ECRA):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
26	0x0 RW	**Enable Clock Request B (ECRB):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
25	0x1 RW	**SSP Serial Bit Rate Clock (SSPSCLK) Direction (SCLKDIR):** 0 = Master mode, SSP drives SSPSCLK 1 = Slave mode, SSP recieves SSPSCLK
24	0x1 RW	**SSP Frame (SSPSFRM) Direction (SFRMDIR):** 0 = Master mode, SSP drives SSPSFRM 1 = Slave mode, SSP receives SSPSFRM
23	0x0 RW	**Receive With Out Transmit (RWOT):** 0 = Transmit/Receive mode 1 = Receive without transmit mode
22	0x0 RW	**Trailing Byte (TRAIL):** 0 = Processor based, trailing bytes are handled by processor 1 = DMA based, trailing bytes are handled by DMA
21	0x0 RW	**Transmit Service Request Enable (TSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
20	0x0 RW	**Receive Service Request Enable (RSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
19	0x0 RW	**Receiver Time-out Interrupt Enable (TINTE):** 0 = Receiver Time-out interrupts are disabled 1 = Receiver Time-out interrupts are enabled
18	0x0 RW	**Peripheral Trailing Byte Interrupts Enable (PINTE):** 0 = Peripheral Trailing Byte Interrupts are disabled 1 = Peripheral Trailing Byte Interrupts are enabled
17	0x0 RW	**RSVD:** Reserved
16	0x0 RW	**Invert Frame Signal (IFS):** 0 = Frame polarity is determined by SSP format and PSP polarity bits 1 = Frame signal will be inverted from the normal SSP frame signal (as defined by the SSP format nad PSP polarity bits)
15	0x0 RW	**Select FIFO for EFWR (test mode bit) (when EFWR=1) (STRF):** 0 = Transmit FIFO is selected for both writes and reads through the SSP Data Register (SSDR) 1 = Receive FIFO is selected for both writes and reads through the SSP Data Register (SSDR)
14	0x0 RW	**Enable FIFO Write/Read (test mode bit) (EFWR):** 0 = FIFO write/read special function is disabled (normal SSP operational mode) 1 = FIFO write/read special function is enabled

Bit Range	Default & Access	Field Name (ID): Description
13:10	0x0 RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
9:6	0x0 RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
5	0x0 RW	**Microwire Transmit Data Size (MWDS):** 0 = 8-bit command words are transmitted 1 = 16-bit command words are transmitted
4	0x0 RW	**Motorola SPI SSPSCLK Phase Setting (SPH):** 0 = SSPSCLK is inactive one sycle at the start of a fram and 1/2 cycle at the end of a frame 1 = SSPSCLK is inactive 1/2 cycle at the start of a frame and one cycle at the end of a frame
3	0x0 RW	**Motorola SPI SSPSCLK polarity setting (SPO):** 0 = The inactive or idle state of SSPSCLK is low 1 = The inactive or idle state of SSPSCLK is high
2	0x0 RW	**Loop-Back Mode (test mode bit) (LBM):** 0 = Normal serial port operation enabled 1 = Output of transmit serial shifter connected to input of receive serial shifter, internally
1	0x0 RW	**Transmit FIFO Interrupt Enable (TIE):** 0 = Transmit FIFO level interrupt is disabled 1 = Transmit FIFO level interrupt is enabled
0	0x0 RW	**Receive FIFO Interrupt Enable (RIE):** 0 = Receive FIFO level interrupt is disabled 1 = Receive FIFO level interrupt is enabled

8.8.3 SSP Status Register (SSSR)—Offset 8h

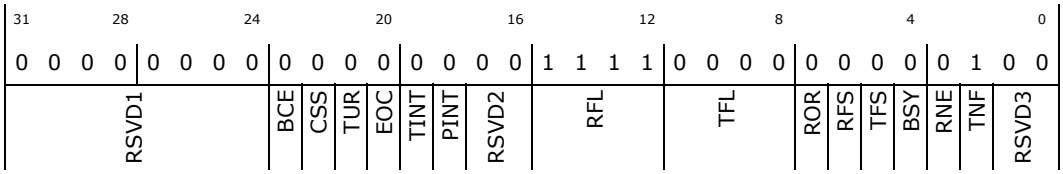
The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A2000h] + 8h

Default: 0000F004h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD1:** Reserved
23	0x0 RW/1C	**Bit Count Error (BCE):** 0 = SSP has not experienced a bit count error 1 = SSPSFRM signal has been asserted when the bit counter was not 0
22	0x0 RO	**Clock Synchronization Status (CSS):** 0 = SSP is ready for slave clock operations 1 = SSP is currently busy synchronizing slave mode signals
21	0x0 RW/1C	**Transmit FIFO Under Run (TUR):** 0 = Transmit FIFO has not experienced an under run 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0x0 RW/1C	**End of Chain (EOC):** 0 = DMA has not signaled an end of chain condition 1 = DMA has signaled an end of chain condition
19	0x0 RW/1C	**Receiver Time-out Interrupt (TINT):** 0 = No receiver time-out pending 1 = Receiver time-out pending
18	0x0 RW/1C	**Peripheral Trailing Byte Interrupt (PINT):** 0 = No peripheral trailing byte interrupt pending 1 = Peripheral trailing byte interrupt pending
17:16	0x0 RO	**RSVD2:** Reserved
15:12	0xf RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value 0xF is read, the FIFO is either empty or full and the programmer should refer to the RNE bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
11:8	0x0 RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the TNF bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
7	0x0 RW/1C	**Receive FIFO Overrun (ROR):** 0 = Receive FIFO has not experienced an overrun 1 = Attempted data write to full receive FIFO, request interrupt
6	0x0 RO	**Receive FIFO Service Request (RFS):** 0 = Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0x0 RO	**Transmit FIFO Service Request (TFS):** 0 = Transmit FIFO level exceeds the TFT threshold (TFT+1), or SSP disabled 1 = Transmit FIFO level is at or below TFT threshold (TFT+1), request interrupt

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RO	**SSP Busy (BSY):** 0 = SSP is idle or disabled 1 = SSP currently transmitting or receiving a frame
3	0x0 RO	**Receive FIOF Not Empty (RNE):** 0 = Receive FIFO is empty 1 = Receive FIFO is not empty
2	0x1 RO	**Transmit FIFO Not Full (TNF):** 0 = Transmit FIFO is full 1 = Transmit FIFO is not full
1:0	0x0 RO	**RSVD3:** Reserved

8.8.4 SSP Interupt Test Register (SSITR)—Offset Ch

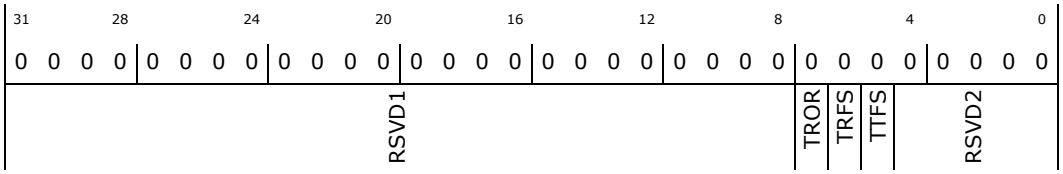
The read-write SSP Interrupt Test registers should be used only for testing purposes. Writing a 1 to the test transmit FIFO request SSITR.TTFS, bit 5, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Transmit FIFO. Writing a 1 to the test receive FIFO request SSITR.TRFS, bit 6, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Receive FIFO. Writing a 1 to the test receive FIFO overrun bit SSITR.TROR, bit 7, will generate a non-maskable Interrupt strobe signal to the Interrupt controller only, no DMA request will be made. Setting any of these bits will also cause the corresponding status bit(s) to be set in the Enhanced SSP Status register (SSSR). The Interrupt and/or service request, caused by the setting of one of these test bits, will remain active until the test bit is cleared by writing a 0 it. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A2000h] + Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD1:** Reserved
7	0x0 RW	**Test Receive FIFO overrun (TROR):** 0 = No receive FIFO overrun service request 1 = Generates non-maskable interrupt to CPU. No DMA request is generated
6	0x0 RW	**Test Receive FIFO service request (TRFS):** 0 = No receive FIFO service request 1 = Generates non-maskable interrupt to CPU and a DMA request for receive FIFO

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**Test Transmit FIFO service request (TTFS):** 0 = No transmit FIFO service request pending 1 = Generates non-maskable interrupt to CPU and a DMA request for transmit FIFO
4:0	0x0 RO	**RSVD2:** Reserved

8.8.5 SSP Data Register (SSDR)—Offset 10h

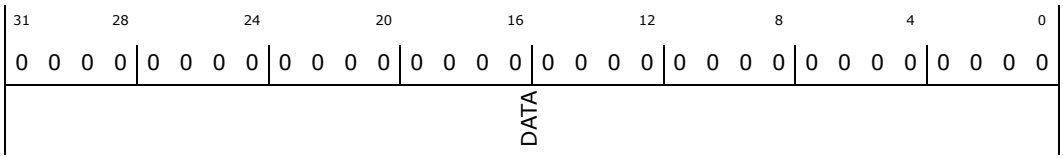
The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO, the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.TFL, SSSR.RFL, SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32-bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32-bits is automatically right-justified in the Receive FIFO. When the Enhanced SSP is programmed for National Semiconductor Microwire* frame format and if the size for Transmit data is 8-bits as selected by SSCR1.MWDS=0, then the most significant 24-bits are ignored. Similarly, if the size for the Transmit data is 16-bit as selected by SSCR1.MWDS=1, then most significant 16-bits are ignored. The SSCR0.DSS field controls the Receive data size.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A2000h] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Data (DATA):** Data word to be written to/read from transmit/receive FIFO. When reading from this register when the SSP is disabled (SSE=0) then this will return indeterminate data.

8.8.6 SSP Time-Out Regsiter (SSTO)—Offset 28h

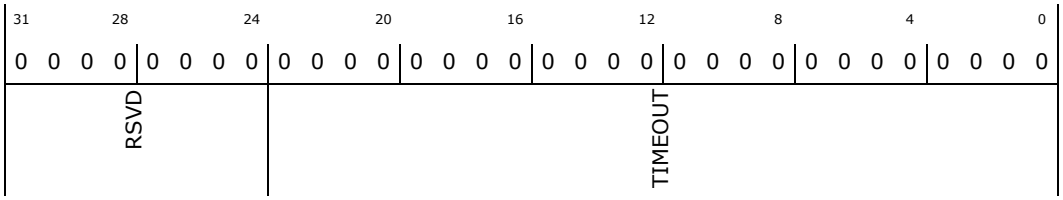
The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A2000h] + 28h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD:** Reserved
23:0	0x0 RW	**Timeout Value (TIMEOUT):** Is the value that defines the timeout interval, given by TIMEOUT/Peripheral Clock Frequency

8.8.7 SSP Programmable Protocol Register (SSPSP)—Offset 2Ch

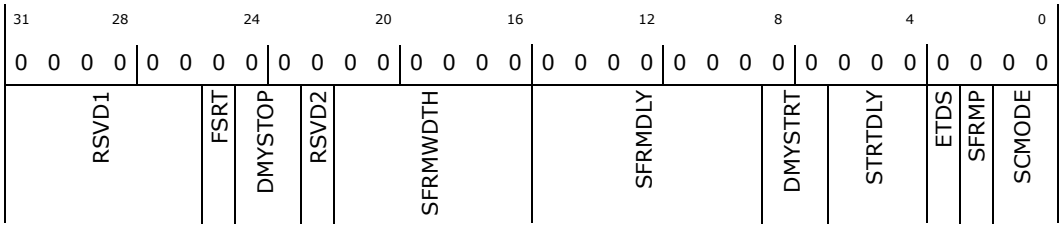
The Enhanced SSP Programmable Protocol registers are read-write registers that contain eight fields that are used to program the various programmable serial-protocol parameters. When using PSP format in Network mode, the parameters SFRMDLY, STRTDLY, DMYSTP, DMYSTRT must be set to 0. Other parameters (such as FRMPOL, SCMODE, FSRT, SFRMDWDTH) are programmable. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A2000h] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD1:** Reserved
25	0x0 RW	**Frame Sync Relative Timing Bit (FSRT):** 0 = Next frame is asserted after the end of the T4 timing 1 = Next frame is asserted with the LSB of the previous frame
24:23	0x0 RW	**Dummy Stop (DMYSTOP):** Programmed value sets the number of SSPSCLK cycles that follow the transmitted data
22	0x0 RW	**RSVD2:** Reserved
21:16	0x0 RW	**Serial Frame Width (SFRMWDTH):** Programmed value sets frame width (1-38)
15:9	0x0 RW	**Serial Frame Delay (SFRMDLY):** Programmed value sets the number of half SSPSCLK cycles from TXD/RXD being driven to SSPSFRM being asserted (0-74)
8:7	0x0 RW	**Dummy Start (DMYSTRT):** Programmed value sets the number of SSPSCLKs after STRTDLY is complete that precede the transmit/receive data
6:4	0x0 RW	**Start Delay (STRTDLY):** Programmed value sets start delay that is used to set the idle time of SSPSCLK between transfers (0-7 SSPSCLK periods)
3	0x0 RW	**End of Transfer Data State (ETDS):** 0 = Low 1 = Last value (bit 0)
2	0x0 RW	**Serial Frame Polarity (SFRMP):** 0 = SSPSFRM is active low 1 = SSPSFRM is active high
1:0	0x0 RW	**Serial bit-rate Clock Mode (SCMODE):** 00 = Data driven (falling), Data sampled (rising), Idle state (low) 01 = Data driven (rising), Data sampled (falling), Idle state (low) 10 = Data driven (rising), Data sampled (falling), Idle state (high) 11 = Data driven (falling), Data sampled (rising), Idle state (high)

8.8.8 SSM TX Time Slot Active Register (SSTSA)—Offset 30h

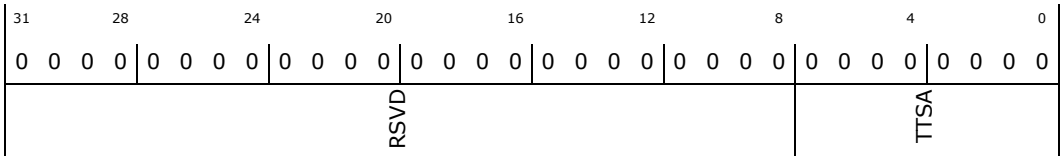
The Enhanced SSP TX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will transmit data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A2000h] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RW	**TX Time Slot Active (TTSA):** 0 = SSP will not transmit data in this time slot 1 = SSP will transmit data in this time slot

8.8.9 SSP RX Time Slot Active Register (SSRSA)—Offset 34h

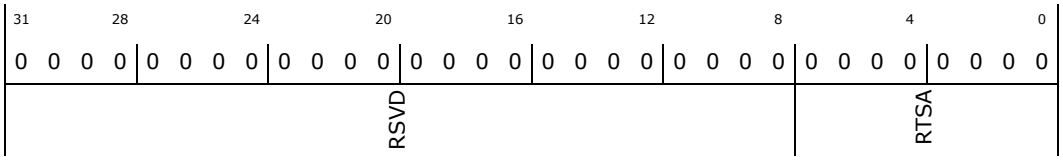
The Enhanced SSP RX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will receive data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A2000h] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RW	**RX Time Slot Active (RTSA):** 0 = SSP will not receive data in this time slot 1 = SSP will receive data in this time slot

8.8.10 SSP Time Slot Status Register (SSTSS)—Offset 38h

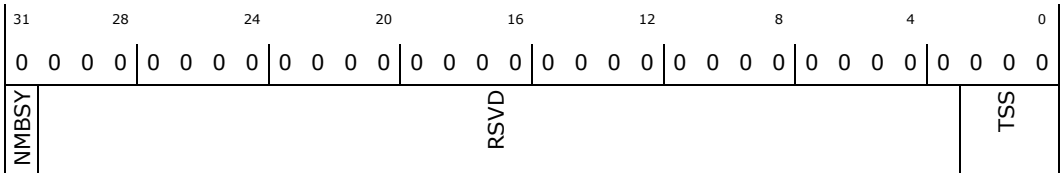
The Enhanced SSP Time Slot Status registers are read only registers that indicate which Time Slot the Enhanced SSP is currently in when the Enhanced SSP is in Network Mode (SSCR0.MOD = 1). This register is not valid when the Enhanced SSP is not in Network Mode. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A2000h] + 38h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Network Mode Busy (NMBSY):** 0 = No frame is currently active (in network mode only) 1 = SSP is in network mode and a frame is currently active
30:3	0x0 RO	**RSVD:** Reserved
2:0	0x0 RO	**Time Slot Status (TSS):** Value indicates which time slot is currently active

8.8.11 SSP Audio Clock Divider (SSACD)—Offset 3Ch

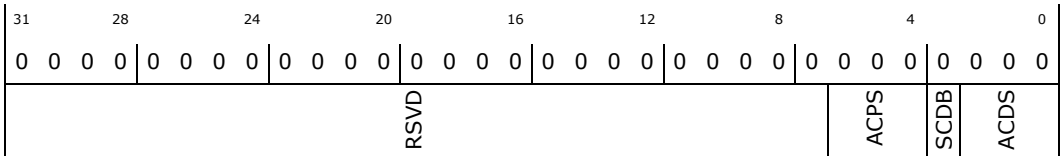
The Enhanced SSP Audio Clock Divider registers are read-write registers that indicate which clock frequency is sent to the Enhanced SSP and to the SYSCLK pin. If SSCR0.SCR is not 0, then there is no guaranteed phase relationship between SYSCLK and SSPSCLK. The SSPSFRM Frame Synch Sampling Frequency is calculated by dividing the chosen PLL output clock frequency (SSACD.ACPS) by the chosen divider (SSACD.ACDS) which gives the SYSCLK frequency. The SYSCLK is then divided by 4 (or by 1) to get the SSPSCLK. The SSPSCLK is divided by the data size (EDSS, DSS values) and by the number of time slots being used (SSCR0.FRDC value), if any, to give the SSPSFRM frequency. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined. It's important to note that this feature is only available if implemented by the project instantiation. A clock source and mux must be instantiated outside of the SSP controller for this feature to work. Only this register is designed into the SSP Controller.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A2000h] + 3Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**RSVD:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**Audio Clock PLL Select (ACPS):** Value indicates which PLL output clock is sent to the clock divider in the clock unit 000: 5.622MHz, 001: 11.345MHz, 010: 12.235MHz, 011: 14.857MHz, 100: 32.842MHz, 101: 48.000MHz, 110, 111: Reserved
3	0x0 RW	**SYSCLK Divider Bypass (SCDB):** 0 = SYSCLK is divided by 4 before being sent to SSP 1 = SYSCLK is not divided before being sent to SSP
2:0	0x0 RW	**Audio Clock Divider Select (ACDS):** Value indicates which divider will be used by the clock unit to create the SYSCLK output pin. Clock divider value will be 2^ACDS, max ACDS = 5.

8.8.12 SSP Control 2 Register (SSCR2)—Offset 40h

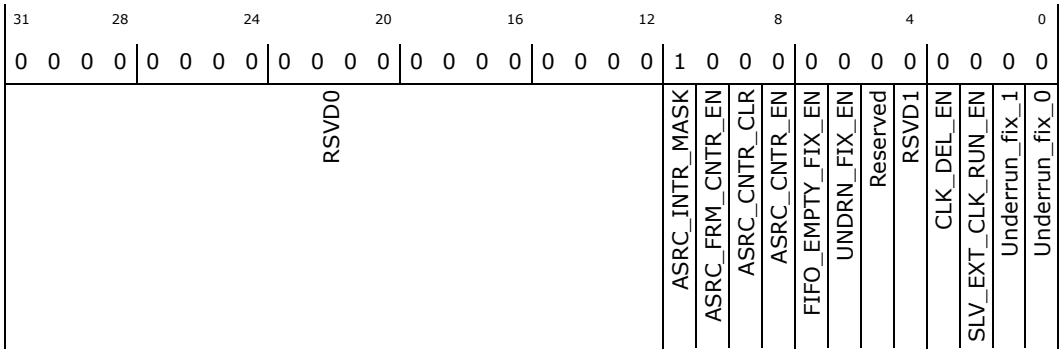
The command status register 2 is extension of command status register and contains various feature enable and disables.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A2000h] + 40h

Default: 00000800h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RSVD0:** Reserved
11	0x1 RW	**ASRC Interrupt Mask (ASRC_INTR_MASK):** Setting this bit to 1 masks the ASRC interrupt that is generated every time the frame count matches the frame threshold.
10	0x0 RW	**ASRC frame count enable (ASRC_FRM_CNTR_EN):** Setting this bit enables the frame counter to start running. Clearing this bit will make the frame counter go back to zero immediately.

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RW/AC	**ASRC Counter Clear (ASRC_CNTR_CLR):** Setting this to 1 will clear the ASRC Free running counter. This bit will self clear after the counter is cleared.
8	0x0 RW	**ASRC Counter enable (ASRC_CNTR_EN):** Setting this bit makes the Free running ASRC counter to start running. Clearing this bit will make it pause and hold it's current value.
7	0x0 RW	**Fifo empty fix enable (FIFO_EMPTY_FIX_EN):** Corner cases between the FIFO empty and APB writes happening to the TX FIFO around the time the new data needs to be sent out on the TXD are fixed with this bit.
6	0x0 RW	**Underrun fix enable (UNDRN_FIX_EN):** OSC to PLL switch along with underrun was causing unexpected behavior. This bit enables the fix for that bug.
5	0x0 RW	**Reserved:** This is a RW bit with no effect on IP behavior
4	0x0 RO	**RSVD1:** Reserved
3	0x0 RW	**Clock Delay Enable (CLK_DEL_EN):** When CLK_DEL_EN = 0, delay logic for capturing data from device is disabled. When CLK_DEL_EN = 1, delay logic for capturing data from device is delayed by half a period of the IO clock
2	0x0 RW	**Slave Mode External Clock Run Enable (SLV_EXT_CLK_RUN_EN):** When in Slave mode the receive state machine requires several clock edges (around 6) to properly sample incoming data. This bit enables a free running clock to the receive state machine before any data is received to properly sample the incoming data. 0 = Disable 1 = Enable
1	0x0 RW	**Mode 1 Underrun Fix (Underrun_fix_1):** Mode 1 of transmit underrun fix. In this mode, new data will start on the underrun slot. This function is only appled to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1 If both underrun modes are enable, mode 1 has higher priority.
0	0x0 RW	**Mode 0 Underrun Fix (Underrun_fix_0):** Mode 0 of transmit underrun fix. In this mode, new data will always start at slot 0. This function is only applied to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1

8.8.13 SSP Frame Select Register (SSFS)—Offset 44h

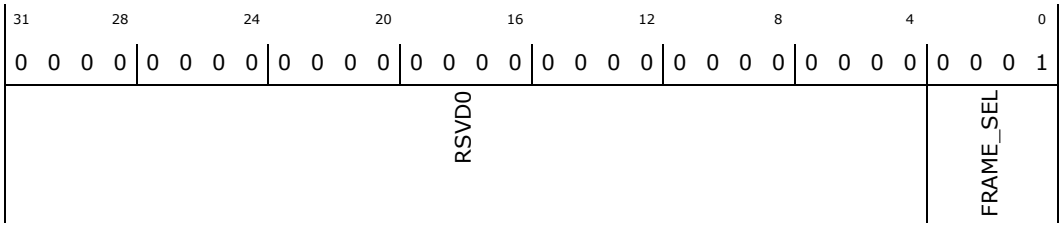
The SSP Frame select register is used to choose which frame signal to assert when accessing a slave device. SW drivers should set this register to assert the correct frame select to the targetted device.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A2000h] + 44h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RSVD0:** Reserved
3:0	0x1 RW	**Frame Select Enable (FRAME_SEL):** Each bit in this field corresponds to a frame signal of the SSP Controller. Not all SSP controllers have all frame selects pinned out so consult the pin list for indication of which SSP controllers support how many frame signals. [Bit 0] Frame Select 0 Master and Slave Supported [Bit 1] Frame Select 1 Master Only [Bit 2] Frame Select 2 Master Only [Bit 3] Frame Select 3 Master Only 0 = Frame Select Disabled 1 = Frame Select Enabled

8.8.14 SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h

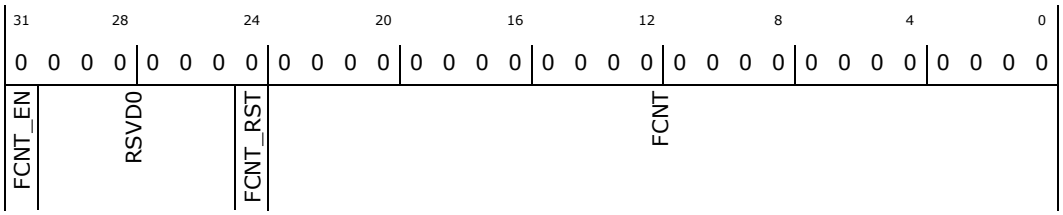
The slot frame counter is typically used in Audio modes and increments the counter every two SSPSCLKs. This allows the OS to check the progress of a transfer. Since the SSP can support upto 8 slots in network mode there are 8 slot frame counters.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset[0-7]: [Ipe_bridge.BAR + A2000h] + 48h + [0-7]*4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Slot Frame Count Enable (FCNT_EN):** 0 = Disable frame counter. 1 = Enable frame counter.
30:25	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
24	0x0 WO	**Slot Frame Count Reset (FCNT_RST):** SSP frame counter reset. Writing a 1 to this bit clears the frame counter.
23:0	0x0 RO	**Slot Frame Count (FCNT):** SSP frame count.

8.8.15 SSP FIFO Level Register (SFIFOL)—Offset 68h

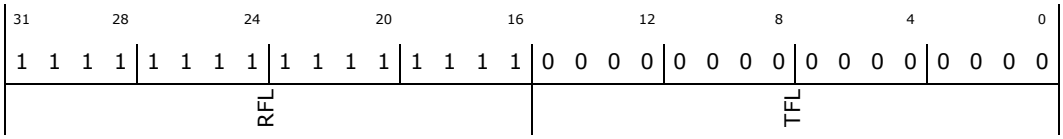
The SFIFOL register describes the current state of the RX and TX FIFOs. Not all bits of the TFL and RFL fields are used and depends on the actual hardware FIFO depth used in the instantiation of the SSP controller. This FIFO level register is meant to replace the SSSR.TFL and SSR.RFL fields.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A2000h] + 68h

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value of all 0xF's are read, the FIFO is either empty or full and the programmer should refer to the SSSR.RNE bit.
15:0	0x0 RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the SSSR.TNF bit.

8.8.16 SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch

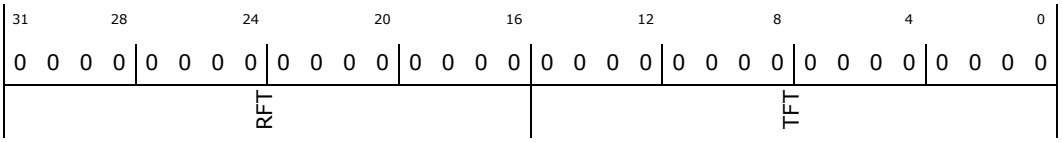
The SFIFOTT is a register that determines when the the FIFOs will assert an interrupt for FIFO full indication. This is meant to replace the SSCR1.RFT and SSCR1.TFT legacy registers. The max size of these registers is based on the actualy FIFO depth in hardware and not the actual size of the bit field.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A2000h] + 6Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. Notes on setting the RFT value. This applies to cases where SSP is receiving data from a device and is interfaced with a DMA channel via the hardware handshake mechanism. Please follow the following recommendations: 1. Number of bits denoted by the (DSS, EDSS) parameters in the SSP should match the SRC_TR_WIDTH programmed in the DMA channel. 2. (RFT+1) should be equal to (SRC_MSIZE). 3. Another option to 2 is to keep the BLOCK_TS in the DMA to be a multiple of (RFT+1)
15:0	0x0 RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.

8.8.17 SSP Control 3 Register (SSCR3)—Offset 70h

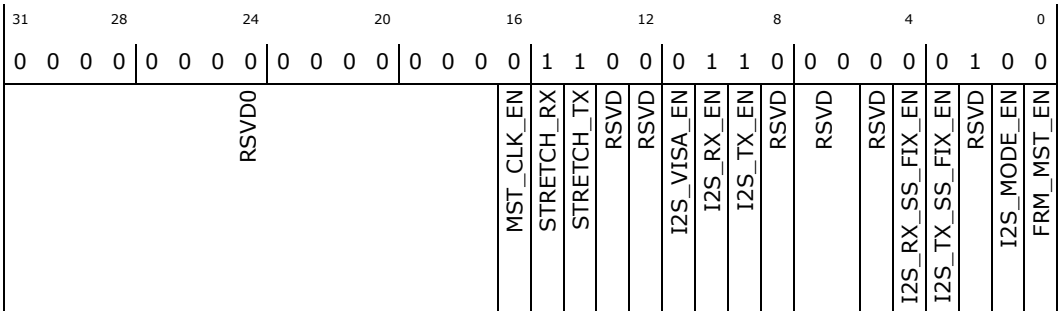
Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A2000h] + 70h

Default: 0000C604h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW	**Master Mode Clock Enable (MST_CLK_EN):** When in single slot master mode (which is the mode used for emulating I2S or LJ master mode), the SSP core can stop the clock on a Tx underflow condition, preventing the Rx side from receiving data. This bit, when set, forces the clock to run when a Tx underflow happens, thereby allowing Rx side to continue functioning while Tx side is in underflow. SW should set this bit when I2S or LJ master mode is enabled i.e. bits 0 and 1 in this register are both set or when using 1-slot PCM (SFS or LFS) master mode operation. Otherwise, SW should leave this at 0.
15	0x1 RW	**Stretch RX Pulse (STRETCH_RX):** HW uses this as a chicken bit to stretch the RX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
14	0x1 RW	**Stretch TX Pulse (STRETCH_TX):** HW uses this as a chicken bit to stretch the TX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
13	0x0 RO	**Reserved (RSVD):** Reserved.
12	0x0 RO	**Reserved (RSVD):** Reserved.
11	0x0 RW	**I2S VISA Enable (I2S_VISA_EN):** Enables newly added I2S and PCM wrapper logic debug signals sent out on the VISA bus instead of the core SSP debug signals. 0 = Core SSP Debug Signals 1 = New I2S and PCM Debug Signals
10	0x1 RW	**I2S Receive Enable (I2S_RX_EN):** When set, this bit enables data to be received on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
9	0x1 RW	**I2S Transmit Enable (I2S_TX_EN):** When set, this bit enables data to be transmitted on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
8	0x0 RO	**Reserved (RSVD):** Reserved.
7:6	0x0 RO	**Reserved (RSVD):** Reserved.
5	0x0 RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**I2S RX Slot Swap Fix Enable (I2S_RX_SS_FIX_EN):** This bit enables the Rx overrun fix in I2S or LJ modes and prevents channel swapping when Rx overrun happens. Note that this bit does not apply to any PCM modes. PCM modes still have the Rx overflow channel aliasing issue. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
3	0x0 RW	**I2S TX Slot Swap Fix Enable (I2S_TX_SS_FIX_EN):** This bit enables the TX underflow fix in I2S or LJ modes and prevents channel swapping when TX underflow happens. Note that this bit does not apply to any PCM modes. PCM modes still have the TX underflow channel aliasing issue. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
2	0x1 RO	**Reserved (RSVD):** Reserved.
1	0x0 RW	**I2S Mode Enable (I2S_MODE_EN):** This bit enables I2S Mode. In I2S mode, slave or master mode operation is selected by appropriately clearing/setting bit 0 in this register. SW should select I2S mode operation before enabling the SSP controller. 0 = Disabled 1 = Enabled
0	0x0 RW	**Frame Master Enable (FRM_MST_EN):** When set, this bit enables the internal frame generator logic that allows accurate frame rate generation. This bit should be set for I2S and PCM master mode operations and cleared for all other modes. SW should select the proper value in this bit before enabling SSP controller. 0 = Disabled 1 = Enabled

8.8.18 SSP Control 4 Register (SSCR4)—Offset 74h

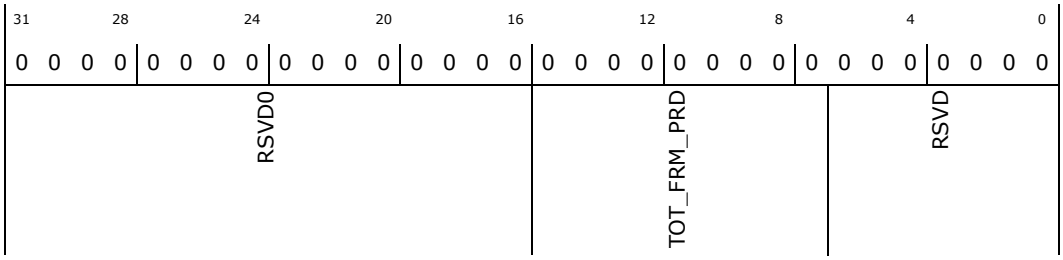
Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A2000h] + 74h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD0:** Reserved
15:7	0x0 RW	**Total Frame Period (TOT_FRM_PRD):** The total frame period (both asserted and de-asserted time of frame), measured in bit clocks, that is driven in I2S, LJ and PCM master modes. This can be controlled to get the desired accuracy on frame rate. A value of 0 and a value smaller than the value programmed in SSCR5.FrameAssertedWidth are illegal
6:0	0x0 RO	**Reserved (RSVD):** Reserved.

8.8.19 SSP Control 5 Register (SSCR5)—Offset 78h

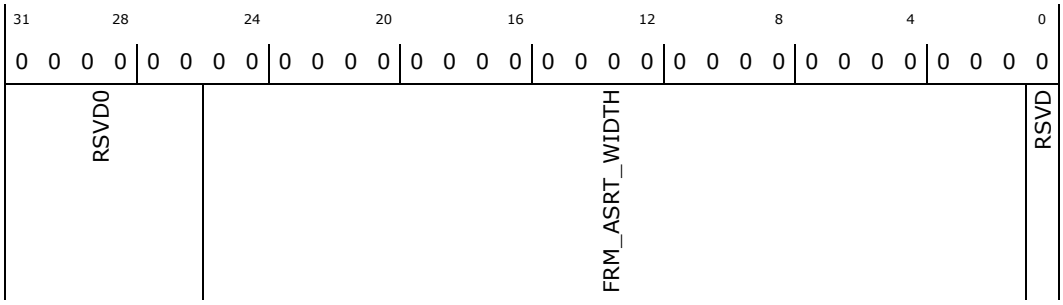
Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

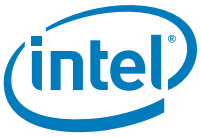
Offset: [Ipe_bridge.BAR + A2000h] + 78h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
25:1	0x0 RW	**Frame Assert Width (FRM_ASRT_WIDTH):** This field controls the width of the asserted period of frame in I2S, LJ and PCM master modes. A value of 1 indicates a width of 2 bit clock period, 2 indicates a width of 3 bit clock periods, etc. The frame width is Frame Assert Width + 1.
0	0x0 RO	**Reserved (RSVD):** Reserved.



8.9 SIO SPI 3 Memory Mapped I/O Registers

Table 60. Summary of SIO SPI 3 Memory Mapped I/O Registers—lpe_bridge.BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"SSP Control 0 Register (SSCR0)—Offset 0h" on page 3797	00000000h
4–7h	4	"SSP Control 1 Register (SSCR1)—Offset 4h" on page 3798	43000000h
8–Bh	4	"SSP Status Register (SSSR)—Offset 8h" on page 3800	0000F004h
C–Fh	4	"SSP Interupt Test Register (SSITR)—Offset Ch" on page 3802	00000000h
10–13h	4	"SSP Data Register (SSDR)—Offset 10h" on page 3803	00000000h
28–2Bh	4	"SSP Time-Out Regsiter (SSTO)—Offset 28h" on page 3804	00000000h
2C–2Fh	4	"SSP Programmable Protocol Register (SSPSP)—Offset 2Ch" on page 3804	00000000h
30–33h	4	"SSM TX Time Slot Active Register (SSTSA)—Offset 30h" on page 3805	00000000h
34–37h	4	"SSP RX Time Slot Active Register (SSRSA)—Offset 34h" on page 3806	00000000h
38–3Bh	4	"SSP Time Slot Status Register (SSTSS)—Offset 38h" on page 3806	00000000h
3C–3Fh	4	"SSP Audio Clock Divider (SSACD)—Offset 3Ch" on page 3807	00000000h
40–43h	4	"SSP Control 2 Register (SSCR2)—Offset 40h" on page 3808	00000800h
44–47h	4	"SSP Frame Select Register (SSFS)—Offset 44h" on page 3809	00000001h
48h + [0-7]*4h	4	"SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h" on page 3810	00000000h
68–6Bh	4	"SSP FIFO Level Register (SFIFOL)—Offset 68h" on page 3811	FFFF0000h
6C–6Fh	4	"SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch" on page 3811	00000000h
70–73h	4	"SSP Control 3 Register (SSCR3)—Offset 70h" on page 3812	0000C604h
74–77h	4	"SSP Control 4 Register (SSCR4)—Offset 74h" on page 3814	00000000h
78–7Bh	4	"SSP Control 5 Register (SSCR5)—Offset 78h" on page 3815	00000000h

8.9.1 SSP Control 0 Register (SSCR0)—Offset 0h

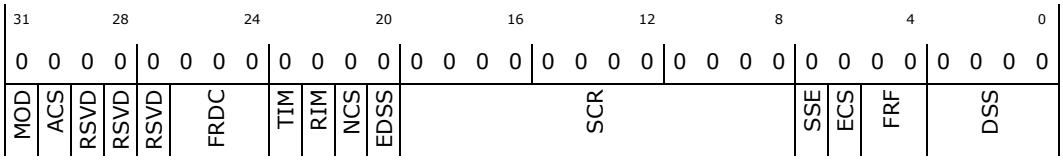
The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A4000h] + 0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Mode Select (MOD):** 0 = Normal SSP Mode 1 = Network Mode
30	0x0 RW	**Audio Clock Select (ACS):** 0 = Clock selection is determined by the NCS and ECS bits 1 = Audio Clock (and Audio Clock Divider) are used to clock the SSP's serial clock (SSPSCLK)
29	0x0 RO	**Reserved (RSVD):** Reserved.
28	0x0 RO	**Reserved (RSVD):** Reserved.
27	0x0 RO	**Reserved (RSVD):** Reserved.
26:24	0x0 RW	**Frame Rate Divider Control (FRDC):** Value 0-7 indicates the number of time slots per frame when in network mode (the actual number of time slots is FRDC+1, so 1 to 8 time slots).
23	0x0 RW	**Transmit FIFO Under Run Interrupt Mask (TIM):** 0 = TUR events will generate an SSP interrupt 1 = TUR events will not generate an SSP interrupt
22	0x0 RW	**Receive FIFO Over Run Interrupt Mask (RIM):** 0 = ROR events will generate an SSP interrupt 1 = ROR events will not generate an SSP interrupt
21	0x0 RW	**Network Clock Select (NCS):** 0 = Clock selection is determined by ECS bit 1 = Network clock is used to create the SSP's serial clock (SSPSCLK)
20	0x0 RW	**Extended Data Size Select (EDSS):** 0 = A zero is preappended to the DSS value which sets the DSS range from 4-16 bits 1 = A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits

Bit Range	Default & Access	Field Name (ID): Description
19:8	0x0 RW	**Serial Clock Rate (SCR):** Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0x0 RW	**Synchronous Serial Port Enable (SSE):** 0 = SSP operation disabled and FIFOs are cleared 1 = SSP operation enabled
6	0x0 RW	**External Clock Select (ECS):** 0 = On-chip clock used to produce the SSP's serial clock (SSPSCLK) 1 = SSPEXTCLK/GPIO pin is used to create the SSP's SSPCLK
5:4	0x0 RW	**Frame Format (FRF):** 00 = Motorola Serial Peripheral Interface (SPI) 01 = Texas Instruments Synchronous Serial Protocol (SSP) 10 = National Semiconductor Microwire 11 = Programmable Serial Protocol (PSP)
3:0	0x0 RW	**Data Size Select (DSS):** With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

8.9.2 SSP Control 1 Register (SSCR1)—Offset 4h

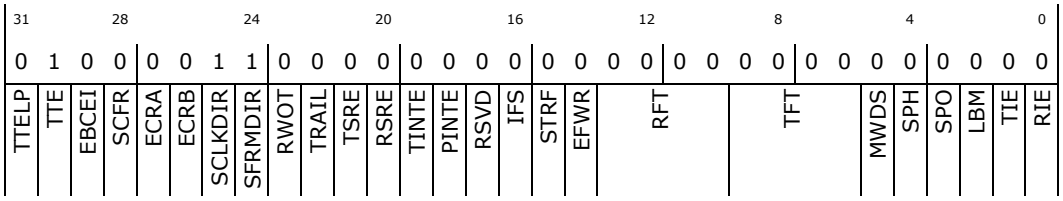
The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A4000h] + 4h

Default: 43000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**TXD Tristate Enable on Last Phase (TTELP):** 0 = TXD line will be tristated on same clock edge as TXD is to be flopped 1 = TXD line will be tristated 1/2 clock edge after TXD is to be flopped
30	0x1 RW	**TXD Tristate Enable (TTE):** 0 = TXD line will not be tristated 1 = TXD line will be tristated when no transmitting data
29	0x0 RW	**Enable Bit Count Error Interrupt (EBCEI):** 0 = Interrupt due to a bit count error is disabled 1 = Interrupt due to a bit count error is enabled

Bit Range	Default & Access	Field Name (ID): Description
28	0x0 RW	**Slave Clock Free Running (SCFR):** 0 = clock input to SSPSCLK is continuously running 1 = clock input to SSPSCLK is only active durring transfers
27	0x0 RW	**Enable Clock Request A (ECRA):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
26	0x0 RW	**Enable Clock Request B (ECRB):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
25	0x1 RW	**SSP Serial Bit Rate Clock (SSPSCLK) Direction (SCLKDIR):** 0 = Master mode, SSP drives SSPSCLK 1 = Slave mode, SSP recieves SSPSCLK
24	0x1 RW	**SSP Frame (SSPSFRM) Direction (SFRMDIR):** 0 = Master mode, SSP drives SSPSFRM 1 = Slave mode, SSP receives SSPSFRM
23	0x0 RW	**Receive With Out Transmit (RWOT):** 0 = Transmit/Receive mode 1 = Receive without transmit mode
22	0x0 RW	**Trailing Byte (TRAIL):** 0 = Processor based, trailing bytes are handled by processor 1 = DMA based, trailing bytes are handled by DMA
21	0x0 RW	**Transmit Service Request Enable (TSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
20	0x0 RW	**Receive Service Request Enable (RSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
19	0x0 RW	**Receiver Time-out Interrupt Enable (TINTE):** 0 = Receiver Time-out interrupts are disabled 1 = Receiver Time-out interrupts are enabled
18	0x0 RW	**Peripheral Trailing Byte Interrupts Enable (PINTE):** 0 = Peripheral Trailing Byte Interrupts are disabled 1 = Peripheral Trailing Byte Interrupts are enabled
17	0x0 RW	**RSVD:** Reserved
16	0x0 RW	**Invert Frame Signal (IFS):** 0 = Frame polarity is determined by SSP format and PSP polarity bits 1 = Frame signal will be inverted from the normal SSP frame signal (as defined by the SSP format nad PSP polarity bits)
15	0x0 RW	**Select FIFO for EFWR (test mode bit) (when EFWR=1) (STRF):** 0 = Transmit FIFO is selected for both writes and reads through the SSP Data Register (SSDR) 1 = Receive FIFO is selected for both writes and reads through the SSP Data Register (SSDR)
14	0x0 RW	**Enable FIFO Write/Read (test mode bit) (EFWR):** 0 = FIFO write/read special function is disabled (normal SSP operational mode) 1 = FIFO write/read special function is enabled

Bit Range	Default & Access	Field Name (ID): Description
13:10	0x0 RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
9:6	0x0 RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
5	0x0 RW	**Microwire Transmit Data Size (MWDS):** 0 = 8-bit command words are transmitted 1 = 16-bit command words are transmitted
4	0x0 RW	**Motorola SPI SSPSCLK Phase Setting (SPH):** 0 = SSPSCLK is inactive one sycle at the start of a fram and 1/2 cycle at the end of a frame 1 = SSPSCLK is inactive 1/2 cycle at the start of a frame and one cycle at the end of a frame
3	0x0 RW	**Motorola SPI SSPSCLK polarity setting (SPO):** 0 = The inactive or idle state of SSPSCLK is low 1 = The inactive or idle state of SSPSCLK is high
2	0x0 RW	**Loop-Back Mode (test mode bit) (LBM):** 0 = Normal serial port operation enabled 1 = Output of transmit serial shifter connected to input of receive serial shifter, internally
1	0x0 RW	**Transmit FIFO Interrupt Enable (TIE):** 0 = Transmit FIFO level interrupt is disabled 1 = Transmit FIFO level interrupt is enabled
0	0x0 RW	**Receive FIFO Interrupt Enable (RIE):** 0 = Receive FIFO level interrupt is disabled 1 = Receive FIFO level interrupt is enabled

8.9.3 SSP Status Register (SSSR)—Offset 8h

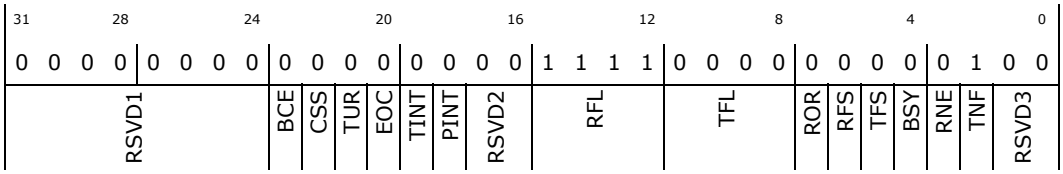
The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A4000h] + 8h

Default: 0000F004h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD1:** Reserved
23	0x0 RW/1C	**Bit Count Error (BCE):** 0 = SSP has not experienced a bit count error 1 = SSPSFRM signal has been asserted when the bit counter was not 0
22	0x0 RO	**Clock Synchronization Status (CSS):** 0 = SSP is ready for slave clock operations 1 = SSP is currently busy synchronizing slave mode signals
21	0x0 RW/1C	**Transmit FIFO Under Run (TUR):** 0 = Transmit FIFO has not experienced an under run 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0x0 RW/1C	**End of Chain (EOC):** 0 = DMA has not signaled an end of chain condition 1 = DMA has signaled an end of chain condition
19	0x0 RW/1C	**Receiver Time-out Interrupt (TINT):** 0 = No receiver time-out pending 1 = Receiver time-out pending
18	0x0 RW/1C	**Peripheral Trailing Byte Interrupt (PINT):** 0 = No peripheral trailing byte interrupt pending 1 = Peripheral trailing byte interrupt pending
17:16	0x0 RO	**RSVD2:** Reserved
15:12	0xf RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value 0xF is read, the FIFO is either empty or full and the programmer should refer to the RNE bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
11:8	0x0 RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the TNF bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
7	0x0 RW/1C	**Receive FIFO Overrun (ROR):** 0 = Receive FIFO has not experienced an overrun 1 = Attempted data write to full receive FIFO, request interrupt
6	0x0 RO	**Receive FIFO Service Request (RFS):** 0 = Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0x0 RO	**Transmit FIFO Service Request (TFS):** 0 = Transmit FIFO level exceeds the TFT threshold (TFT+1), or SSP disabled 1 = Transmit FIFO level is at or below TFT threshold (TFT+1), request interrupt

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RO	**SSP Busy (BSY):** 0 = SSP is idle or disabled 1 = SSP currently transmitting or receiving a frame
3	0x0 RO	**Receive FIOF Not Empty (RNE):** 0 = Receive FIFO is empty 1 = Receive FIFO is not empty
2	0x1 RO	**Transmit FIFO Not Full (TNF):** 0 = Transmit FIFO is full 1 = Transmit FIFO is not full
1:0	0x0 RO	**RSVD3:** Reserved

8.9.4 SSP Interupt Test Register (SSITR)—Offset Ch

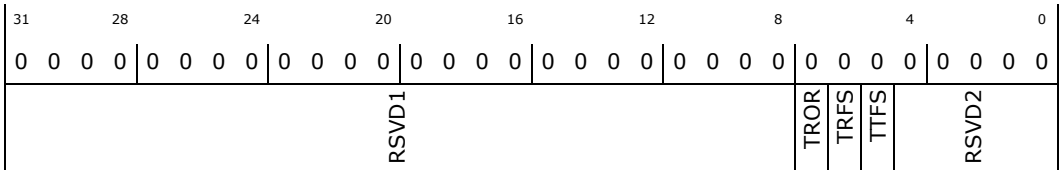
The read-write SSP Interrupt Test registers should be used only for testing purposes. Writing a 1 to the test transmit FIFO request SSITR.TTFS, bit 5, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Transmit FIFO. Writing a 1 to the test receive FIFO request SSITR.TRFS, bit 6, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Receive FIFO. Writing a 1 to the test receive FIFO overrun bit SSITR.TROR, bit 7, will generate a non-maskable Interrupt strobe signal to the Interrupt controller only, no DMA request will be made. Setting any of these bits will also cause the corresponding status bit(s) to be set in the Enhanced SSP Status register (SSSR). The Interrupt and/or service request, caused by the setting of one of these test bits, will remain active until the test bit is cleared by writing a 0 it. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A4000h] + Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD1:** Reserved
7	0x0 RW	**Test Receive FIFO overrun (TROR):** 0 = No receive FIFO overrun service request 1 = Generates non-maskable interrupt to CPU. No DMA request is generated
6	0x0 RW	**Test Receive FIFO service request (TRFS):** 0 = No receive FIFO service request 1 = Generates non-maskable interrupt to CPU and a DMA request for receive FIFO

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**Test Transmit FIFO service request (TTFS):** 0 = No transmit FIFO service request pending 1 = Generates non-maskable interrupt to CPU and a DMA request for transmit FIFO
4:0	0x0 RO	**RSVD2:** Reserved

8.9.5 SSP Data Register (SSDR)—Offset 10h

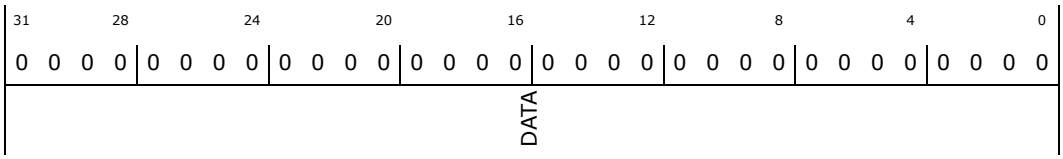
The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO, the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.TFL, SSSR.RFL, SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32-bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32-bits is automatically right-justified in the Receive FIFO. When the Enhanced SSP is programmed for National Semiconductor Microwire* frame format and if the size for Transmit data is 8-bits as selected by SSCR1.MWDS=0, then the most significant 24-bits are ignored. Similarly, if the size for the Transmit data is 16-bit as selected by SSCR1.MWDS=1, then most significant 16-bits are ignored. The SSCR0.DSS field controls the Receive data size.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A4000h] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Data (DATA):** Data word to be written to/read from transmit/receive FIFO. When reading from this register when the SSP is disabled (SSE=0) then this will return indeterminate data.

8.9.6 SSP Time-Out Regsiter (SSTO)—Offset 28h

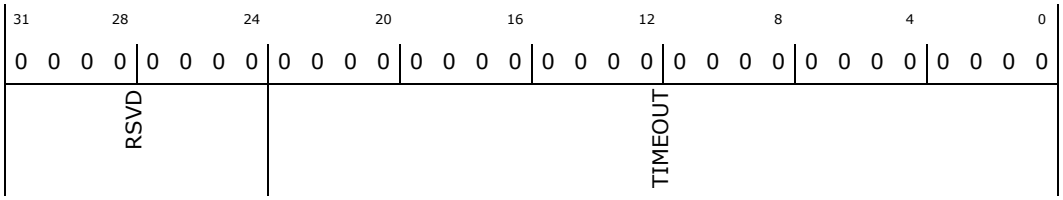
The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A4000h] + 28h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD:** Reserved
23:0	0x0 RW	**Timeout Value (TIMEOUT):** Is the value that defines the timeout interval, given by TIMEOUT/Peripheral Clock Frequency

8.9.7 SSP Programmable Protocol Register (SSPSP)—Offset 2Ch

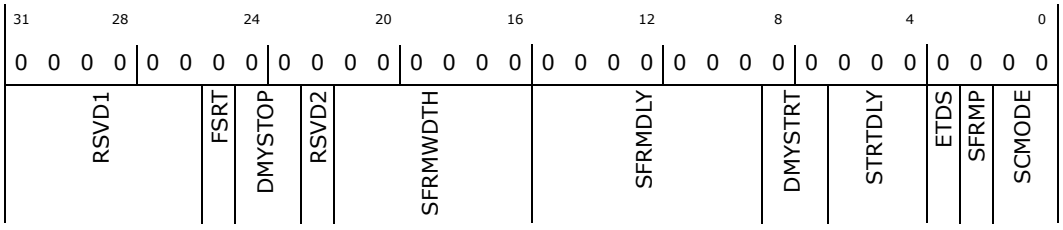
The Enhanced SSP Programmable Protocol registers are read-write registers that contain eight fields that are used to program the various programmable serial-protocol parameters. When using PSP format in Network mode, the parameters SFRMDLY, STRTDLY, DMYSTP, DMYSTRT must be set to 0. Other parameters (such as FRMPOL, SCMODE, FSRT, SFRMDWDTH) are programmable. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A4000h] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD1:** Reserved
25	0x0 RW	**Frame Sync Relative Timing Bit (FSRT):** 0 = Next frame is asserted after the end of the T4 timing 1 = Next frame is asserted with the LSB of the previous frame
24:23	0x0 RW	**Dummy Stop (DMYSTOP):** Programmed value sets the number of SSPSCLK cycles that follow the transmitted data
22	0x0 RW	**RSVD2:** Reserved
21:16	0x0 RW	**Serial Frame Width (SFRMWDTH):** Programmed value sets frame width (1-38)
15:9	0x0 RW	**Serial Frame Delay (SFRMDLY):** Programmed value sets the number of half SSPSCLK cycles from TXD/RXD being driven to SSPSFRM being asserted (0-74)
8:7	0x0 RW	**Dummy Start (DMYSTRT):** Programmed value sets the number of SSPSCLKs after STRTDLY is complete that precede the transmit/receive data
6:4	0x0 RW	**Start Delay (STRTDLY):** Programmed value sets start delay that is used to set the idle time of SSPSCLK between transfers (0-7 SSPSCLK periods)
3	0x0 RW	**End of Transfer Data State (ETDS):** 0 = Low 1 = Last value (bit 0)
2	0x0 RW	**Serial Frame Polarity (SFRMP):** 0 = SSPSFRM is active low 1 = SSPSFRM is active high
1:0	0x0 RW	**Serial bit-rate Clock Mode (SCMODE):** 00 = Data driven (falling), Data sampled (rising), Idle state (low) 01 = Data driven (rising), Data sampled (falling), Idle state (low) 10 = Data driven (rising), Data sampled (falling), Idle state (high) 11 = Data driven (falling), Data sampled (rising), Idle state (high)

8.9.8 SSM TX Time Slot Active Register (SSTSA)—Offset 30h

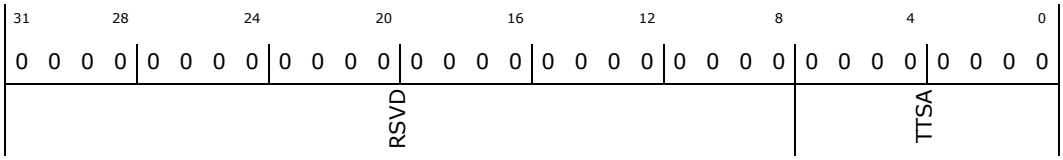
The Enhanced SSP TX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will transmit data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A4000h] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RW	**TX Time Slot Active (TTSA):** 0 = SSP will not transmit data in this time slot 1 = SSP will transmit data in this time slot

8.9.9 SSP RX Time Slot Active Register (SSRSA)—Offset 34h

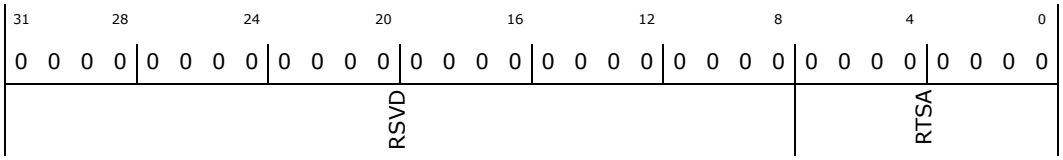
The Enhanced SSP RX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will receive data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A4000h] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RW	**RX Time Slot Active (RTSA):** 0 = SSP will not receive data in this time slot 1 = SSP will receive data in this time slot

8.9.10 SSP Time Slot Status Register (SSTSS)—Offset 38h

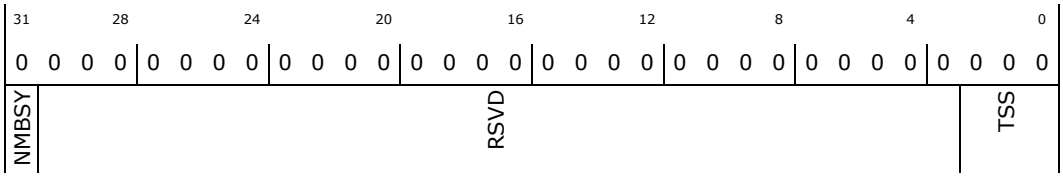
The Enhanced SSP Time Slot Status registers are read only registers that indicate which Time Slot the Enhanced SSP is currently in when the Enhanced SSP is in Network Mode (SSCR0.MOD = 1). This register is not valid when the Enhanced SSP is not in Network Mode. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A4000h] + 38h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Network Mode Busy (NMBSY):** 0 = No frame is currently active (in network mode only) 1 = SSP is in network mode and a frame is currently active
30:3	0x0 RO	**RSVD:** Reserved
2:0	0x0 RO	**Time Slot Status (TSS):** Value indicates which time slot is currently active

8.9.11 SSP Audio Clock Divider (SSACD)—Offset 3Ch

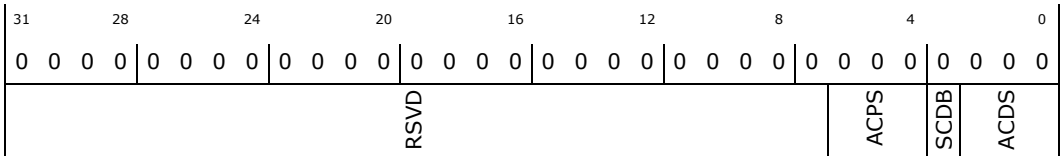
The Enhanced SSP Audio Clock Divider registers are read-write registers that indicate which clock frequency is sent to the Enhanced SSP and to the SYSCLK pin. If SSCR0.SCR is not 0, then there is no guaranteed phase relationship between SYSCLK and SSPSCLK. The SSPSFRM Frame Synch Sampling Frequency is calculated by dividing the chosen PLL output clock frequency (SSACD.ACPS) by the chosen divider (SSACD.ACDS) which gives the SYSCLK frequency. The SYSCLK is then divided by 4 (or by 1) to get the SSPSCLK. The SSPSCLK is divided by the data size (EDSS, DSS values) and by the number of time slots being used (SSCR0.FRDC value), if any, to give the SSPSFRM frequency. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined. It's important to note that this feature is only available if implemented by the project instantiation. A clock source and mux must be instantiated outside of the SSP controller for this feature to work. Only this register is designed into the SSP Controller.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A4000h] + 3Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**RSVD:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**Audio Clock PLL Select (ACPS):** Value indicates which PLL output clock is sent to the clock divider in the clock unit 000: 5.622MHz, 001: 11.345MHz, 010: 12.235MHz, 011: 14.857MHz, 100: 32.842MHz, 101: 48.000MHz, 110, 111: Reserved
3	0x0 RW	**SYSCLK Divider Bypass (SCDB):** 0 = SYSCLK is divided by 4 before being sent to SSP 1 = SYSCLK is not divided before being sent to SSP
2:0	0x0 RW	**Audio Clock Divider Select (ACDS):** Value indicates which divider will be used by the clock unit to create the SYSCLK output pin. Clock divider value will be 2^ACDS, max ACDS = 5.

8.9.12 SSP Control 2 Register (SSCR2)—Offset 40h

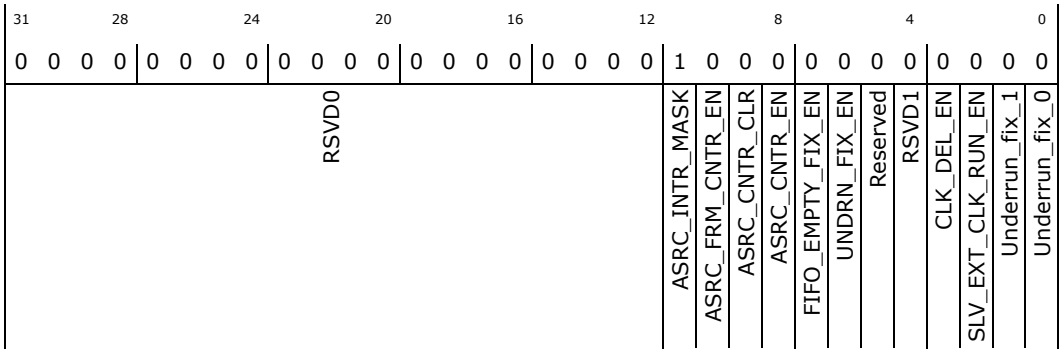
The command status register 2 is extension of command status register and contains various feature enable and disables.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A4000h] + 40h

Default: 00000800h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RSVD0:** Reserved
11	0x1 RW	**ASRC Interrupt Mask (ASRC_INTR_MASK):** Setting this bit to 1 masks the ASRC interrupt that is generated every time the frame count matches the frame threshold.
10	0x0 RW	**ASRC frame count enable (ASRC_FRM_CNTR_EN):** Setting this bit enables the frame counter to start running. Clearing this bit will make the frame counter go back to zero immediately.

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RW/AC	**ASRC Counter Clear (ASRC_CNTR_CLR):** Setting this to 1 will clear the ASRC Free running counter. This bit will self clear after the counter is cleared.
8	0x0 RW	**ASRC Counter enable (ASRC_CNTR_EN):** Setting this bit makes the Free running ASRC counter to start running. Clearing this bit will make it pause and hold it's current value.
7	0x0 RW	**Fifo empty fix enable (FIFO_EMPTY_FIX_EN):** Corner cases between the FIFO empty and APB writes happening to the TX FIFO around the time the new data needs to be sent out on the TXD are fixed with this bit.
6	0x0 RW	**Underrun fix enable (UNDRN_FIX_EN):** OSC to PLL switch along with underrun was causing unexpected behavior. This bit enables the fix for that bug.
5	0x0 RW	**Reserved:** This is a RW bit with no effect on IP behavior
4	0x0 RO	**RSVD1:** Reserved
3	0x0 RW	**Clock Delay Enable (CLK_DEL_EN):** When CLK_DEL_EN = 0, delay logic for capturing data from device is disabled. When CLK_DEL_EN = 1, delay logic for capturing data from device is delayed by half a period of the IO clock
2	0x0 RW	**Slave Mode External Clock Run Enable (SLV_EXT_CLK_RUN_EN):** When in Slave mode the receive state machine requires several clock edges (around 6) to properly sample incoming data. This bit enables a free running clock to the receive state machine before any data is received to properly sample the incoming data. 0 = Disable 1 = Enable
1	0x0 RW	**Mode 1 Underrun Fix (Underrun_fix_1):** Mode 1 of transmit underrun fix. In this mode, new data will start on the underrun slot. This function is only appled to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1 If both underrun modes are enable, mode 1 has higher priority.
0	0x0 RW	**Mode 0 Underrun Fix (Underrun_fix_0):** Mode 0 of transmit underrun fix. In this mode, new data will always start at slot 0. This function is only applied to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1

8.9.13 SSP Frame Select Register (SSFS)—Offset 44h

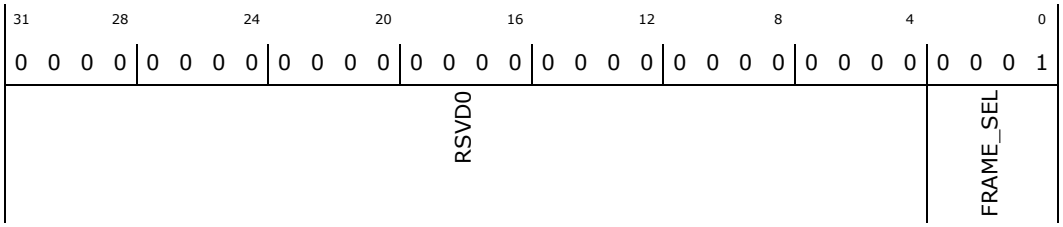
The SSP Frame select register is used to choose which frame signal to assert when accessing a slave device. SW drivers should set this register to assert the correct frame select to the targetted device.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A4000h] + 44h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RSVD0:** Reserved
3:0	0x1 RW	**Frame Select Enable (FRAME_SEL):** Each bit in this field corresponds to a frame signal of the SSP Controller. Not all SSP controllers have all frame selects pinned out so consult the pin list for indication of which SSP controllers support how many frame signals. [Bit 0] Frame Select 0 Master and Slave Supported [Bit 1] Frame Select 1 Master Only [Bit 2] Frame Select 2 Master Only [Bit 3] Frame Select 3 Master Only 0 = Frame Select Disabled 1 = Frame Select Enabled

8.9.14 SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h

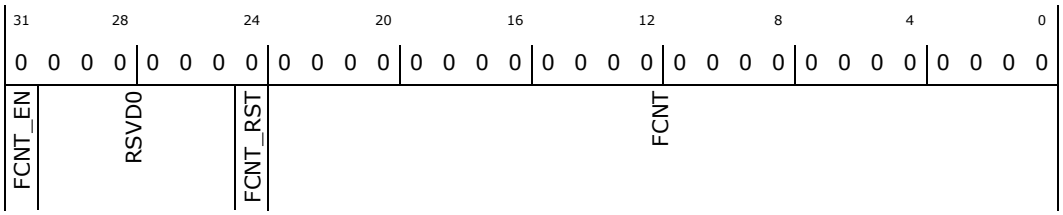
The slot frame counter is typically used in Audio modes and increments the counter every two SSPSCLKs. This allows the OS to check the progress of a transfer. Since the SSP can support upto 8 slots in network mode there are 8 slot frame counters.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset[0-7]: [Ipe_bridge.BAR + A4000h] + 48h + [0-7]*4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Slot Frame Count Enable (FCNT_EN):** 0 = Disable frame counter. 1 = Enable frame counter.
30:25	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
24	0x0 WO	**Slot Frame Count Reset (FCNT_RST):** SSP frame counter reset. Writing a 1 to this bit clears the frame counter.
23:0	0x0 RO	**Slot Frame Count (FCNT):** SSP frame count.

8.9.15 SSP FIFO Level Register (SFIFOL)—Offset 68h

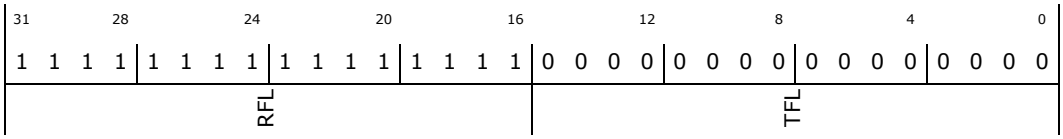
The SFIFOL register describes the current state of the RX and TX FIFOs. Not all bits of the TFL and RFL fields are used and depends on the actual hardware FIFO depth used in the instantiation of the SSP controller. This FIFO level register is meant to replace the SSSR.TFL and SSR.RFL fields.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A4000h] + 68h

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value of all 0xF's are read, the FIFO is either empty or full and the programmer should refer to the SSSR.RNE bit.
15:0	0x0 RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the SSSR.TNF bit.

8.9.16 SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch

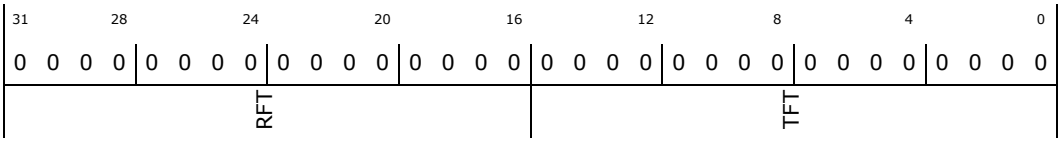
The SFIFOTT is a register that determines when the the FIFOs will assert an interrupt for FIFO full indication. This is meant to replace the SSCR1.RFT and SSCR1.TFT legacy registers. The max size of these registers is based on the actualy FIFO depth in hardware and not the actual size of the bit field.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A4000h] + 6Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. Notes on setting the RFT value. This applies to cases where SSP is receiving data from a device and is interfaced with a DMA channel via the hardware handshake mechanism. Please follow the following recommendations: 1. Number of bits denoted by the (DSS, EDSS) parameters in the SSP should match the SRC_TR_WIDTH programmed in the DMA channel. 2. (RFT+1) should be equal to (SRC_MSIZE). 3. Another option to 2 is to keep the BLOCK_TS in the DMA to be a multiple of (RFT+1)
15:0	0x0 RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.

8.9.17 SSP Control 3 Register (SSCR3)—Offset 70h

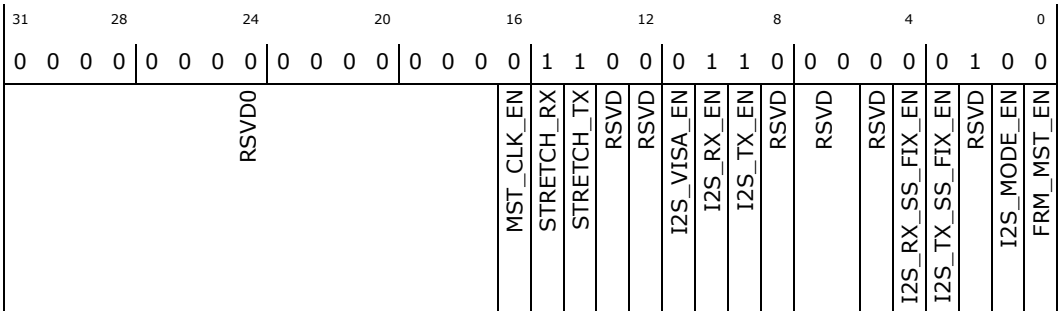
Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A4000h] + 70h

Default: 0000C604h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW	**Master Mode Clock Enable (MST_CLK_EN):** When in single slot master mode (which is the mode used for emulating I2S or LJ master mode), the SSP core can stop the clock on a Tx underflow condition, preventing the Rx side from receiving data. This bit, when set, forces the clock to run when a Tx underflow happens, thereby allowing Rx side to continue functioning while Tx side is in underflow. SW should set this bit when I2S or LJ master mode is enabled i.e. bits 0 and 1 in this register are both set or when using 1-slot PCM (SFS or LFS) master mode operation. Otherwise, SW should leave this at 0.
15	0x1 RW	**Stretch RX Pulse (STRETCH_RX):** HW uses this as a chicken bit to stretch the RX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
14	0x1 RW	**Stretch TX Pulse (STRETCH_TX):** HW uses this as a chicken bit to stretch the TX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
13	0x0 RO	**Reserved (RSVD):** Reserved.
12	0x0 RO	**Reserved (RSVD):** Reserved.
11	0x0 RW	**I2S VISA Enable (I2S_VISA_EN):** Enables newly added I2S and PCM wrapper logic debug signals sent out on the VISA bus instead of the core SSP debug signals. 0 = Core SSP Debug Signals 1 = New I2S and PCM Debug Signals
10	0x1 RW	**I2S Receive Enable (I2S_RX_EN):** When set, this bit enables data to be received on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
9	0x1 RW	**I2S Transmit Enable (I2S_TX_EN):** When set, this bit enables data to be transmitted on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
8	0x0 RO	**Reserved (RSVD):** Reserved.
7:6	0x0 RO	**Reserved (RSVD):** Reserved.
5	0x0 RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**I2S RX Slot Swap Fix Enable (I2S_RX_SS_FIX_EN):** This bit enables the Rx overrun fix in I2S or LJ modes and prevents channel swapping when Rx overrun happens. Note that this bit does not apply to any PCM modes. PCM modes still have the Rx overflow channel aliasing issue. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
3	0x0 RW	**I2S TX Slot Swap Fix Enable (I2S_TX_SS_FIX_EN):** This bit enables the TX underflow fix in I2S or LJ modes and prevents channel swapping when TX underflow happens. Note that this bit does not apply to any PCM modes. PCM modes still have the TX underflow channel aliasing issue. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
2	0x1 RO	**Reserved (RSVD):** Reserved.
1	0x0 RW	**I2S Mode Enable (I2S_MODE_EN):** This bit enables I2S Mode. In I2S mode, slave or master mode operation is selected by appropriately clearing/setting bit 0 in this register. SW should select I2S mode operation before enabling the SSP controller. 0 = Disabled 1 = Enabled
0	0x0 RW	**Frame Master Enable (FRM_MST_EN):** When set, this bit enables the internal frame generator logic that allows accurate frame rate generation. This bit should be set for I2S and PCM master mode operations and cleared for all other modes. SW should select the proper value in this bit before enabling SSP controller. 0 = Disabled 1 = Enabled

8.9.18 SSP Control 4 Register (SSCR4)—Offset 74h

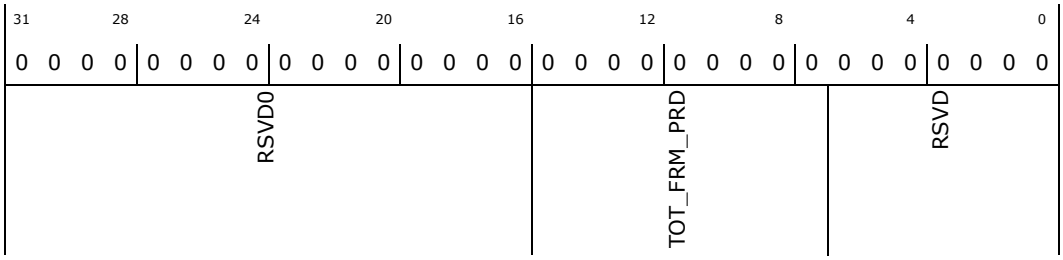
Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A4000h] + 74h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD0:** Reserved
15:7	0x0 RW	**Total Frame Period (TOT_FRM_PRD):** The total frame period (both asserted and de-asserted time of frame), measured in bit clocks, that is driven in I2S, LJ and PCM master modes. This can be controlled to get the desired accuracy on frame rate. A value of 0 and a value smaller than the value programmed in SSCR5.FrameAssertedWidth are illegal
6:0	0x0 RO	**Reserved (RSVD):** Reserved.

8.9.19 SSP Control 5 Register (SSCR5)—Offset 78h

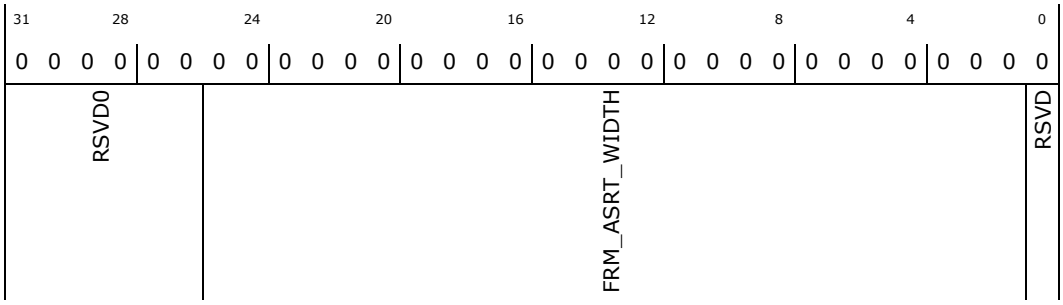
Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

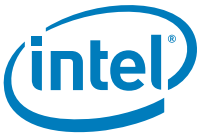
Offset: [Ipe_bridge.BAR + A4000h] + 78h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
25:1	0x0 RW	**Frame Assert Width (FRM_ASRT_WIDTH):** This field controls the width of the asserted period of frame in I2S, LJ and PCM master modes. A value of 1 indicates a width of 2 bit clock period, 2 indicates a width of 3 bit clock periods, etc. The frame width is Frame Assert Width + 1.
0	0x0 RO	**Reserved (RSVD):** Reserved.



8.10 SIO SPI 4 Memory Mapped I/O Registers

Table 61. Summary of SIO SPI 4 Memory Mapped I/O Registers—lpe_bridge.BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"SSP Control 0 Register (SSCR0)—Offset 0h" on page 3819	00000000h
4–7h	4	"SSP Control 1 Register (SSCR1)—Offset 4h" on page 3820	43000000h
8–Bh	4	"SSP Status Register (SSSR)—Offset 8h" on page 3822	0000F004h
C–Fh	4	"SSP Interupt Test Register (SSITR)—Offset Ch" on page 3824	00000000h
10–13h	4	"SSP Data Register (SSDR)—Offset 10h" on page 3825	00000000h
28–2Bh	4	"SSP Time-Out Regsiter (SSTO)—Offset 28h" on page 3826	00000000h
2C–2Fh	4	"SSP Programmable Protocol Register (SSPSP)—Offset 2Ch" on page 3826	00000000h
30–33h	4	"SSM TX Time Slot Active Register (SSTSA)—Offset 30h" on page 3827	00000000h
34–37h	4	"SSP RX Time Slot Active Register (SSRSA)—Offset 34h" on page 3828	00000000h
38–3Bh	4	"SSP Time Slot Status Register (SSTSS)—Offset 38h" on page 3828	00000000h
3C–3Fh	4	"SSP Audio Clock Divider (SSACD)—Offset 3Ch" on page 3829	00000000h
40–43h	4	"SSP Control 2 Register (SSCR2)—Offset 40h" on page 3830	00000800h
44–47h	4	"SSP Frame Select Register (SSFS)—Offset 44h" on page 3831	00000001h
48h + [0-7]*4h	4	"SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h" on page 3832	00000000h
68–6Bh	4	"SSP FIFO Level Register (SFIFOL)—Offset 68h" on page 3833	FFFF0000h
6C–6Fh	4	"SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch" on page 3833	00000000h
70–73h	4	"SSP Control 3 Register (SSCR3)—Offset 70h" on page 3834	0000C604h
74–77h	4	"SSP Control 4 Register (SSCR4)—Offset 74h" on page 3836	00000000h
78–7Bh	4	"SSP Control 5 Register (SSCR5)—Offset 78h" on page 3837	00000000h

8.10.1 SSP Control 0 Register (SSCR0)—Offset 0h

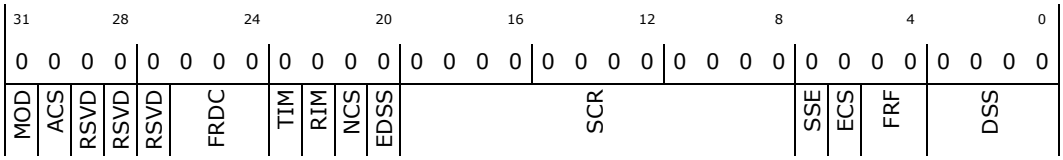
The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A5000h] + 0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Mode Select (MOD):** 0 = Normal SSP Mode 1 = Network Mode
30	0x0 RW	**Audio Clock Select (ACS):** 0 = Clock selection is determined by the NCS and ECS bits 1 = Audio Clock (and Audio Clock Divider) are used to clock the SSP's serial clock (SSPSCLK)
29	0x0 RO	**Reserved (RSVD):** Reserved.
28	0x0 RO	**Reserved (RSVD):** Reserved.
27	0x0 RO	**Reserved (RSVD):** Reserved.
26:24	0x0 RW	**Frame Rate Divider Control (FRDC):** Value 0-7 indicates the number of time slots per frame when in network mode (the actual number of time slots is FRDC+1, so 1 to 8 time slots).
23	0x0 RW	**Transmit FIFO Under Run Interrupt Mask (TIM):** 0 = TUR events will generate an SSP interrupt 1 = TUR events will not generate an SSP interrupt
22	0x0 RW	**Receive FIFO Over Run Interrupt Mask (RIM):** 0 = ROR events will generate an SSP interrupt 1 = ROR events will not generate an SSP interrupt
21	0x0 RW	**Network Clock Select (NCS):** 0 = Clock selection is determined by ECS bit 1 = Network clock is used to create the SSP's serial clock (SSPSCLK)
20	0x0 RW	**Extended Data Size Select (EDSS):** 0 = A zero is preappended to the DSS value which sets the DSS range from 4-16 bits 1 = A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits

Bit Range	Default & Access	Field Name (ID): Description
19:8	0x0 RW	**Serial Clock Rate (SCR):** Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0x0 RW	**Synchronous Serial Port Enable (SSE):** 0 = SSP operation disabled and FIFOs are cleared 1 = SSP operation enabled
6	0x0 RW	**External Clock Select (ECS):** 0 = On-chip clock used to produce the SSP's serial clock (SSPSCLK) 1 = SSPEXTCLK/GPIO pin is used to create the SSP's SSPCLK
5:4	0x0 RW	**Frame Format (FRF):** 00 = Motorola Serial Peripheral Interface (SPI) 01 = Texas Instruments Synchronous Serial Protocol (SSP) 10 = National Semiconductor Microwire 11 = Programmable Serial Protocol (PSP)
3:0	0x0 RW	**Data Size Select (DSS):** With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

8.10.2 SSP Control 1 Register (SSCR1)—Offset 4h

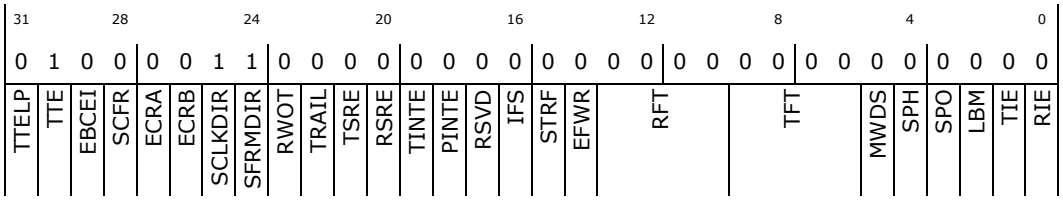
The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A5000h] + 4h

Default: 43000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**TXD Tristate Enable on Last Phase (TTELP):** 0 = TXD line will be tristated on same clock edge as TXD is to be flopped 1 = TXD line will be tristated 1/2 clock edge after TXD is to be flopped
30	0x1 RW	**TXD Tristate Enable (TTE):** 0 = TXD line will not be tristated 1 = TXD line will be tristated when no transmitting data
29	0x0 RW	**Enable Bit Count Error Interrupt (EBCEI):** 0 = Interrupt due to a bit count error is disabled 1 = Interrupt due to a bit count error is enabled

Bit Range	Default & Access	Field Name (ID): Description
28	0x0 RW	**Slave Clock Free Running (SCFR):** 0 = clock input to SSPSCLK is continuously running 1 = clock input to SSPSCLK is only active durring transfers
27	0x0 RW	**Enable Clock Request A (ECRA):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
26	0x0 RW	**Enable Clock Request B (ECRB):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
25	0x1 RW	**SSP Serial Bit Rate Clock (SSPSCLK) Direction (SCLKDIR):** 0 = Master mode, SSP drives SSPSCLK 1 = Slave mode, SSP recieves SSPSCLK
24	0x1 RW	**SSP Frame (SSPSFRM) Direction (SFRMDIR):** 0 = Master mode, SSP drives SSPSFRM 1 = Slave mode, SSP receives SSPSFRM
23	0x0 RW	**Receive With Out Transmit (RWOT):** 0 = Transmit/Receive mode 1 = Receive without transmit mode
22	0x0 RW	**Trailing Byte (TRAIL):** 0 = Processor based, trailing bytes are handled by processor 1 = DMA based, trailing bytes are handled by DMA
21	0x0 RW	**Transmit Service Request Enable (TSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
20	0x0 RW	**Receive Service Request Enable (RSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
19	0x0 RW	**Receiver Time-out Interrupt Enable (TINTE):** 0 = Receiver Time-out interrupts are disabled 1 = Receiver Time-out interrupts are enabled
18	0x0 RW	**Peripheral Trailing Byte Interrupts Enable (PINTE):** 0 = Peripheral Trailing Byte Interrupts are disabled 1 = Peripheral Trailing Byte Interrupts are enabled
17	0x0 RW	**RSVD:** Reserved
16	0x0 RW	**Invert Frame Signal (IFS):** 0 = Frame polarity is determined by SSP format and PSP polarity bits 1 = Frame signal will be inverted from the normal SSP frame signal (as defined by the SSP format nad PSP polarity bits)
15	0x0 RW	**Select FIFO for EFWR (test mode bit) (when EFWR=1) (STRF):** 0 = Transmit FIFO is selected for both writes and reads through the SSP Data Register (SSDR) 1 = Receive FIFO is selected for both writes and reads through the SSP Data Register (SSDR)
14	0x0 RW	**Enable FIFO Write/Read (test mode bit) (EFWR):** 0 = FIFO write/read special function is disabled (normal SSP operational mode) 1 = FIFO write/read special function is enabled

Bit Range	Default & Access	Field Name (ID): Description
13:10	0x0 RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
9:6	0x0 RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
5	0x0 RW	**Microwire Transmit Data Size (MWDS):** 0 = 8-bit command words are transmitted 1 = 16-bit command words are transmitted
4	0x0 RW	**Motorola SPI SSPSCLK Phase Setting (SPH):** 0 = SSPSCLK is inactive one sycle at the start of a fram and 1/2 cycle at the end of a frame 1 = SSPSCLK is inactive 1/2 cycle at the start of a frame and one cycle at the end of a frame
3	0x0 RW	**Motorola SPI SSPSCLK polarity setting (SPO):** 0 = The inactive or idle state of SSPSCLK is low 1 = The inactive or idle state of SSPSCLK is high
2	0x0 RW	**Loop-Back Mode (test mode bit) (LBM):** 0 = Normal serial port operation enabled 1 = Output of transmit serial shifter connected to input of receive serial shifter, internally
1	0x0 RW	**Transmit FIFO Interrupt Enable (TIE):** 0 = Transmit FIFO level interrupt is disabled 1 = Transmit FIFO level interrupt is enabled
0	0x0 RW	**Receive FIFO Interrupt Enable (RIE):** 0 = Receive FIFO level interrupt is disabled 1 = Receive FIFO level interrupt is enabled

8.10.3 SSP Status Register (SSSR)—Offset 8h

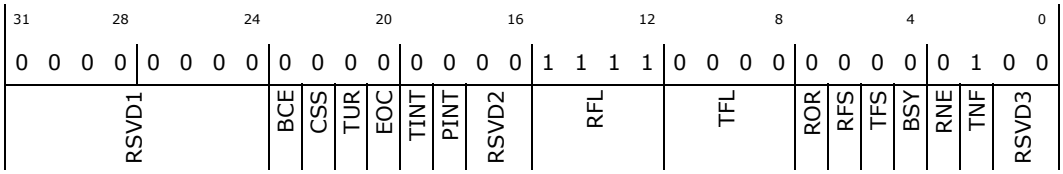
The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A5000h] + 8h

Default: 0000F004h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD1:** Reserved
23	0x0 RW/1C	**Bit Count Error (BCE):** 0 = SSP has not experienced a bit count error 1 = SSPSFRM signal has been asserted when the bit counter was not 0
22	0x0 RO	**Clock Synchronization Status (CSS):** 0 = SSP is ready for slave clock operations 1 = SSP is currently busy synchronizing slave mode signals
21	0x0 RW/1C	**Transmit FIFO Under Run (TUR):** 0 = Transmit FIFO has not experienced an under run 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0x0 RW/1C	**End of Chain (EOC):** 0 = DMA has not signaled an end of chain condition 1 = DMA has signaled an end of chain condition
19	0x0 RW/1C	**Receiver Time-out Interrupt (TINT):** 0 = No receiver time-out pending 1 = Receiver time-out pending
18	0x0 RW/1C	**Peripheral Trailing Byte Interrupt (PINT):** 0 = No peripheral trailing byte interrupt pending 1 = Peripheral trailing byte interrupt pending
17:16	0x0 RO	**RSVD2:** Reserved
15:12	0xf RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value 0xF is read, the FIFO is either empty or full and the programmer should refer to the RNE bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
11:8	0x0 RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the TNF bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
7	0x0 RW/1C	**Receive FIFO Overrun (ROR):** 0 = Receive FIFO has not experienced an overrun 1 = Attempted data write to full receive FIFO, request interrupt
6	0x0 RO	**Receive FIFO Service Request (RFS):** 0 = Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0x0 RO	**Transmit FIFO Service Request (TFS):** 0 = Transmit FIFO level exceeds the TFT threshold (TFT+1), or SSP disabled 1 = Transmit FIFO level is at or below TFT threshold (TFT+1), request interrupt

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RO	**SSP Busy (BSY):** 0 = SSP is idle or disabled 1 = SSP currently transmitting or receiving a frame
3	0x0 RO	**Receive FIOF Not Empty (RNE):** 0 = Receive FIFO is empty 1 = Receive FIFO is not empty
2	0x1 RO	**Transmit FIFO Not Full (TNF):** 0 = Transmit FIFO is full 1 = Transmit FIFO is not full
1:0	0x0 RO	**RSVD3:** Reserved

8.10.4 SSP Interupt Test Register (SSITR)—Offset Ch

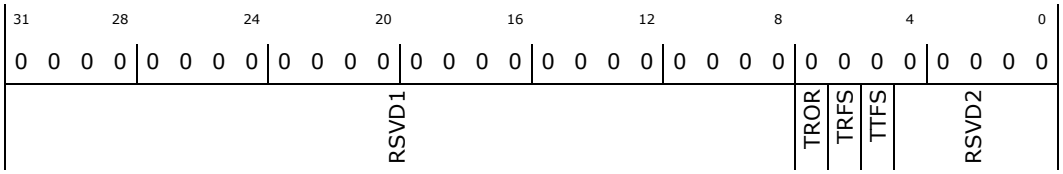
The read-write SSP Interrupt Test registers should be used only for testing purposes. Writing a 1 to the test transmit FIFO request SSITR.TTFS, bit 5, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Transmit FIFO. Writing a 1 to the test receive FIFO request SSITR.TRFS, bit 6, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Receive FIFO. Writing a 1 to the test receive FIFO overrun bit SSITR.TROR, bit 7, will generate a non-maskable Interrupt strobe signal to the Interrupt controller only, no DMA request will be made. Setting any of these bits will also cause the corresponding status bit(s) to be set in the Enhanced SSP Status register (SSSR). The Interrupt and/or service request, caused by the setting of one of these test bits, will remain active until the test bit is cleared by writing a 0 it. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A5000h] + Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD1:** Reserved
7	0x0 RW	**Test Receive FIFO overrun (TROR):** 0 = No receive FIFO overrun service request 1 = Generates non-maskable interrupt to CPU. No DMA request is generated
6	0x0 RW	**Test Receive FIFO service request (TRFS):** 0 = No receive FIFO service request 1 = Generates non-maskable interrupt to CPU and a DMA request for receive FIFO

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**Test Transmit FIFO service request (TTFS):** 0 = No transmit FIFO service request pending 1 = Generates non-maskable interrupt to CPU and a DMA request for transmit FIFO
4:0	0x0 RO	**RSVD2:** Reserved

8.10.5 SSP Data Register (SSDR)—Offset 10h

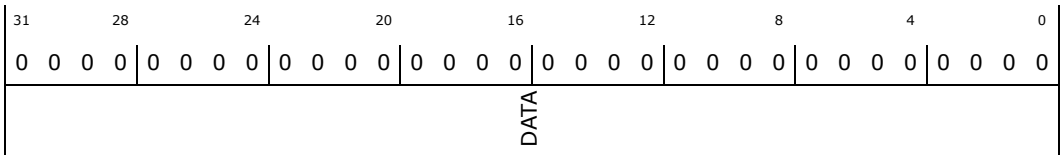
The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO, the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.TFL, SSSR.RFL, SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32-bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32-bits is automatically right-justified in the Receive FIFO. When the Enhanced SSP is programmed for National Semiconductor Microwire* frame format and if the size for Transmit data is 8-bits as selected by SSCR1.MWDS=0, then the most significant 24-bits are ignored. Similarly, if the size for the Transmit data is 16-bit as selected by SSCR1.MWDS=1, then most significant 16-bits are ignored. The SSCR0.DSS field controls the Receive data size.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A5000h] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Data (DATA):** Data word to be written to/read from transmit/receive FIFO. When reading from this register when the SSP is disabled (SSE=0) then this will return indeterminate data.

8.10.6 SSP Time-Out Regsiter (SSTO)—Offset 28h

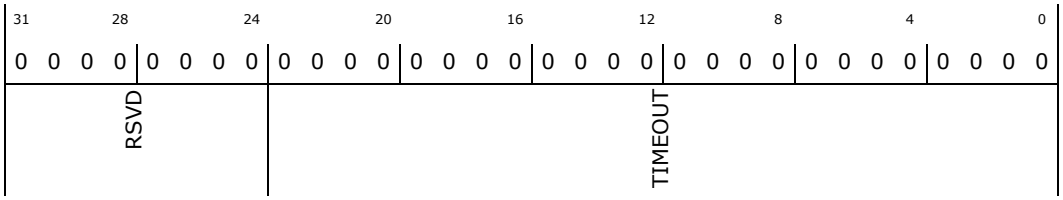
The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A5000h] + 28h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD:** Reserved
23:0	0x0 RW	**Timeout Value (TIMEOUT):** Is the value that defines the timeout interval, given by TIMEOUT/Peripheral Clock Frequency

8.10.7 SSP Programmable Protocol Register (SSPSP)—Offset 2Ch

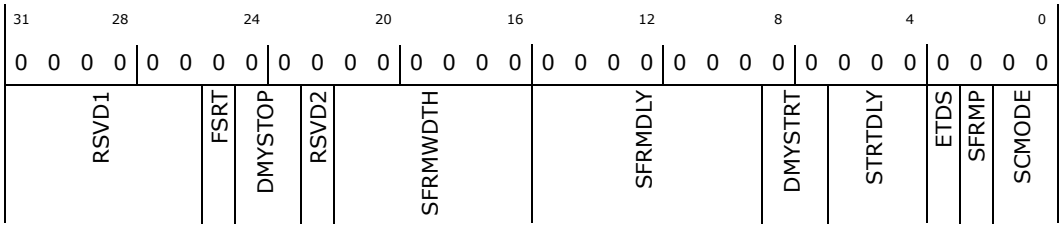
The Enhanced SSP Programmable Protocol registers are read-write registers that contain eight fields that are used to program the various programmable serial-protocol parameters. When using PSP format in Network mode, the parameters SFRMDLY, STRTDLY, DMYSTP, DMYSTRT must be set to 0. Other parameters (such as FRMPOL, SCMODE, FSRT, SFRMDWDTH) are programmable. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A5000h] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD1:** Reserved
25	0x0 RW	**Frame Sync Relative Timing Bit (FSRT):** 0 = Next frame is asserted after the end of the T4 timing 1 = Next frame is asserted with the LSB of the previous frame
24:23	0x0 RW	**Dummy Stop (DMYSTOP):** Programmed value sets the number of SSPSCLK cycles that follow the transmitted data
22	0x0 RW	**RSVD2:** Reserved
21:16	0x0 RW	**Serial Frame Width (SFRMWDTH):** Programmed value sets frame width (1-38)
15:9	0x0 RW	**Serial Frame Delay (SFRMDLY):** Programmed value sets the number of half SSPSCLK cycles from TXD/RXD being driven to SSPSFRM being asserted (0-74)
8:7	0x0 RW	**Dummy Start (DMYSTRT):** Programmed value sets the number of SSPSCLKs after STRTDLY is complete that precede the transmit/receive data
6:4	0x0 RW	**Start Delay (STRTDLY):** Programmed value sets start delay that is used to set the idle time of SSPSCLK between transfers (0-7 SSPSCLK periods)
3	0x0 RW	**End of Transfer Data State (ETDS):** 0 = Low 1 = Last value (bit 0)
2	0x0 RW	**Serial Frame Polarity (SFRMP):** 0 = SSPSFRM is active low 1 = SSPSFRM is active high
1:0	0x0 RW	**Serial bit-rate Clock Mode (SCMODE):** 00 = Data driven (falling), Data sampled (rising), Idle state (low) 01 = Data driven (rising), Data sampled (falling), Idle state (low) 10 = Data driven (rising), Data sampled (falling), Idle state (high) 11 = Data driven (falling), Data sampled (rising), Idle state (high)

8.10.8 SSM TX Time Slot Active Register (SSTSA)—Offset 30h

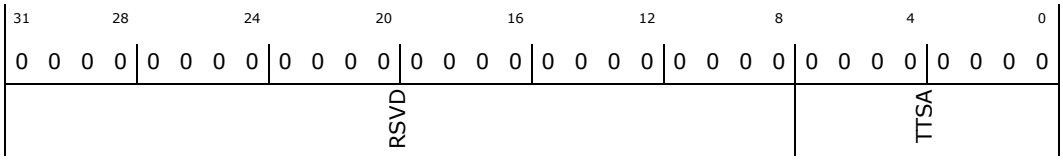
The Enhanced SSP TX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will transmit data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A5000h] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RW	**TX Time Slot Active (TTSA):** 0 = SSP will not transmit data in this time slot 1 = SSP will transmit data in this time slot

8.10.9 SSP RX Time Slot Active Register (SSRSA)—Offset 34h

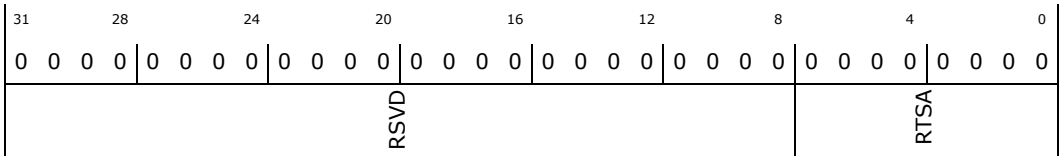
The Enhanced SSP RX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will receive data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A5000h] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RW	**RX Time Slot Active (RTSA):** 0 = SSP will not receive data in this time slot 1 = SSP will receive data in this time slot

8.10.10 SSP Time Slot Status Register (SSTSS)—Offset 38h

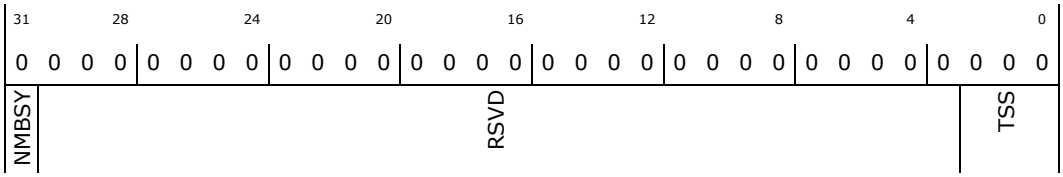
The Enhanced SSP Time Slot Status registers are read only registers that indicate which Time Slot the Enhanced SSP is currently in when the Enhanced SSP is in Network Mode (SSCR0.MOD = 1). This register is not valid when the Enhanced SSP is not in Network Mode. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A5000h] + 38h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Network Mode Busy (NMBSY):** 0 = No frame is currently active (in network mode only) 1 = SSP is in network mode and a frame is currently active
30:3	0x0 RO	**RSVD:** Reserved
2:0	0x0 RO	**Time Slot Status (TSS):** Value indicates which time slot is currently active

8.10.11 SSP Audio Clock Divider (SSACD)—Offset 3Ch

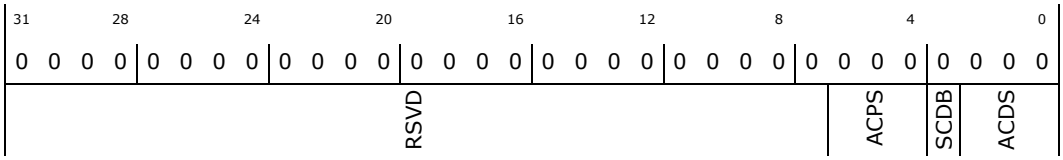
The Enhanced SSP Audio Clock Divider registers are read-write registers that indicate which clock frequency is sent to the Enhanced SSP and to the SYSCLK pin. If SSCR0.SCR is not 0, then there is no guaranteed phase relationship between SYSCLK and SSPSCLK. The SSPSFRM Frame Synch Sampling Frequency is calculated by dividing the chosen PLL output clock frequency (SSACD.ACPS) by the chosen divider (SSACD.ACDS) which gives the SYSCLK frequency. The SYSCLK is then divided by 4 (or by 1) to get the SSPSCLK. The SSPSCLK is divided by the data size (EDSS, DSS values) and by the number of time slots being used (SSCR0.FRDC value), if any, to give the SSPSFRM frequency. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined. It's important to note that this feature is only available if implemented by the project instantiation. A clock source and mux must be instantiated outside of the SSP controller for this feature to work. Only this register is designed into the SSP Controller.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A5000h] + 3Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**RSVD:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**Audio Clock PLL Select (ACPS):** Value indicates which PLL output clock is sent to the clock divider in the clock unit 000: 5.622MHz, 001: 11.345MHz, 010: 12.235MHz, 011: 14.857MHz, 100: 32.842MHz, 101: 48.000MHz, 110, 111: Reserved
3	0x0 RW	**SYSCLK Divider Bypass (SCDB):** 0 = SYSCLK is divided by 4 before being sent to SSP 1 = SYSCLK is not divided before being sent to SSP
2:0	0x0 RW	**Audio Clock Divider Select (ACDS):** Value indicates which divider will be used by the clock unit to create the SYSCLK output pin. Clock divider value will be 2^ACDS, max ACDS = 5.

8.10.12 SSP Control 2 Register (SSCR2)—Offset 40h

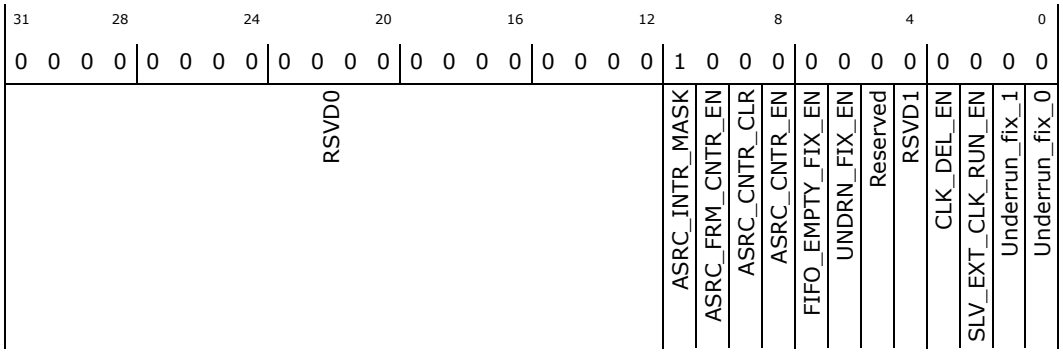
The command status register 2 is extension of command status register and contains various feature enable and disables.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A5000h] + 40h

Default: 00000800h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RSVD0:** Reserved
11	0x1 RW	**ASRC Interrupt Mask (ASRC_INTR_MASK):** Setting this bit to 1 masks the ASRC interrupt that is generated every time the frame count matches the frame threshold.
10	0x0 RW	**ASRC frame count enable (ASRC_FRM_CNTR_EN):** Setting this bit enables the frame counter to start running. Clearing this bit will make the frame counter go back to zero immediately.

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RW/AC	**ASRC Counter Clear (ASRC_CNTR_CLR):** Setting this to 1 will clear the ASRC Free running counter. This bit will self clear after the counter is cleared.
8	0x0 RW	**ASRC Counter enable (ASRC_CNTR_EN):** Setting this bit makes the Free running ASRC counter to start running. Clearing this bit will make it pause and hold it's current value.
7	0x0 RW	**Fifo empty fix enable (FIFO_EMPTY_FIX_EN):** Corner cases between the FIFO empty and APB writes happening to the TX FIFO around the time the new data needs to be sent out on the TXD are fixed with this bit.
6	0x0 RW	**Underrun fix enable (UNDRN_FIX_EN):** OSC to PLL switch along with underrun was causing unexpected behavior. This bit enables the fix for that bug.
5	0x0 RW	**Reserved:** This is a RW bit with no effect on IP behavior
4	0x0 RO	**RSVD1:** Reserved
3	0x0 RW	**Clock Delay Enable (CLK_DEL_EN):** When CLK_DEL_EN = 0, delay logic for capturing data from device is disabled. When CLK_DEL_EN = 1, delay logic for capturing data from device is delayed by half a period of the IO clock
2	0x0 RW	**Slave Mode External Clock Run Enable (SLV_EXT_CLK_RUN_EN):** When in Slave mode the receive state machine requires several clock edges (around 6) to properly sample incoming data. This bit enables a free running clock to the receive state machine before any data is received to properly sample the incoming data. 0 = Disable 1 = Enable
1	0x0 RW	**Mode 1 Underrun Fix (Underrun_fix_1):** Mode 1 of transmit underrun fix. In this mode, new data will start on the underrun slot. This function is only appled to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1 If both underrun modes are enable, mode 1 has higher priority.
0	0x0 RW	**Mode 0 Underrun Fix (Underrun_fix_0):** Mode 0 of transmit underrun fix. In this mode, new data will always start at slot 0. This function is only applied to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1

8.10.13 SSP Frame Select Register (SSFS)—Offset 44h

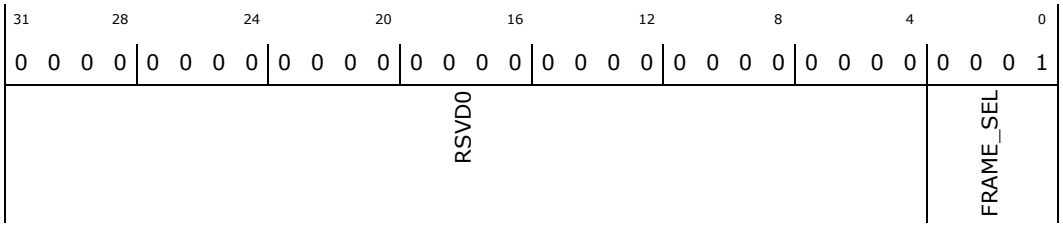
The SSP Frame select register is used to choose which frame signal to assert when accessing a slave device. SW drivers should set this register to assert the correct frame select to the targetted device.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A5000h] + 44h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RSVD0:** Reserved
3:0	0x1 RW	**Frame Select Enable (FRAME_SEL):** Each bit in this field corresponds to a frame signal of the SSP Controller. Not all SSP controllers have all frame selects pinned out so consult the pin list for indication of which SSP controllers support how many frame signals. [Bit 0] Frame Select 0 Master and Slave Supported [Bit 1] Frame Select 1 Master Only [Bit 2] Frame Select 2 Master Only [Bit 3] Frame Select 3 Master Only 0 = Frame Select Disabled 1 = Frame Select Enabled

8.10.14 SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h

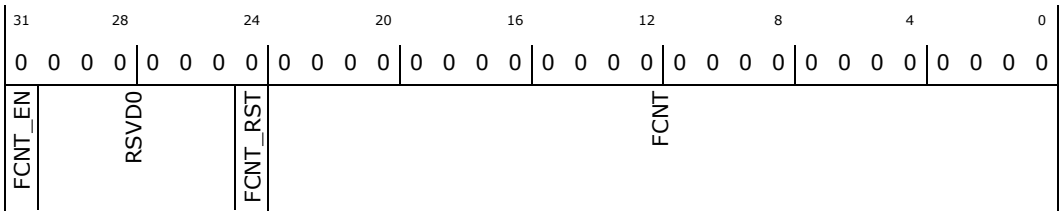
The slot frame counter is typically used in Audio modes and increments the counter every two SSPSCLKs. This allows the OS to check the progress of a transfer. Since the SSP can support upto 8 slots in network mode there are 8 slot frame counters.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset[0-7]: [Ipe_bridge.BAR + A5000h] + 48h + [0-7]*4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Slot Frame Count Enable (FCNT_EN):** 0 = Disable frame counter. 1 = Enable frame counter.
30:25	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
24	0x0 WO	**Slot Frame Count Reset (FCNT_RST):** SSP frame counter reset. Writing a 1 to this bit clears the frame counter.
23:0	0x0 RO	**Slot Frame Count (FCNT):** SSP frame count.

8.10.15 SSP FIFO Level Register (SFIFOL)—Offset 68h

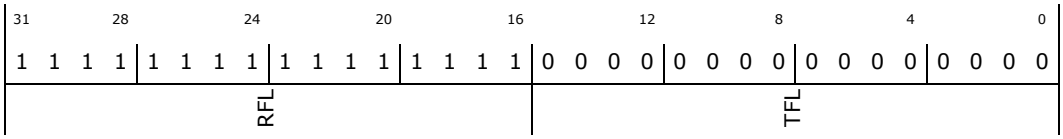
The SFIFOL register describes the current state of the RX and TX FIFOs. Not all bits of the TFL and RFL fields are used and depends on the actual hardware FIFO depth used in the instantiation of the SSP controller. This FIFO level register is meant to replace the SSSR.TFL and SSR.RFL fields.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A5000h] + 68h

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value of all 0xF's are read, the FIFO is either empty or full and the programmer should refer to the SSSR.RNE bit.
15:0	0x0 RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the SSSR.TNF bit.

8.10.16 SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch

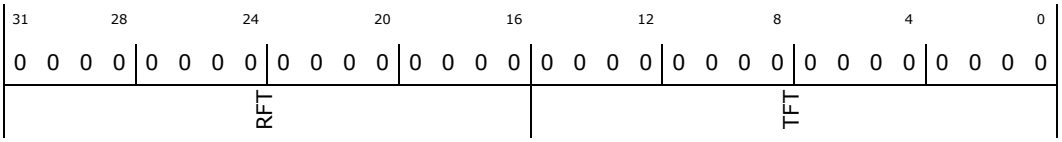
The SFIFOTT is a register that determines when the the FIFOs will assert an interrupt for FIFO full indication. This is meant to replace the SSCR1.RFT and SSCR1.TFT legacy registers. The max size of these registers is based on the actualy FIFO depth in hardware and not the actual size of the bit field.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A5000h] + 6Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. Notes on setting the RFT value. This applies to cases where SSP is receiving data from a device and is interfaced with a DMA channel via the hardware handshake mechanism. Please follow the following recommendations: 1. Number of bits denoted by the (DSS, EDSS) parameters in the SSP should match the SRC_TR_WIDTH programmed in the DMA channel. 2. (RFT+1) should be equal to (SRC_MSIZE). 3. Another option to 2 is to keep the BLOCK_TS in the DMA to be a multiple of (RFT+1)
15:0	0x0 RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.

8.10.17 SSP Control 3 Register (SSCR3)—Offset 70h

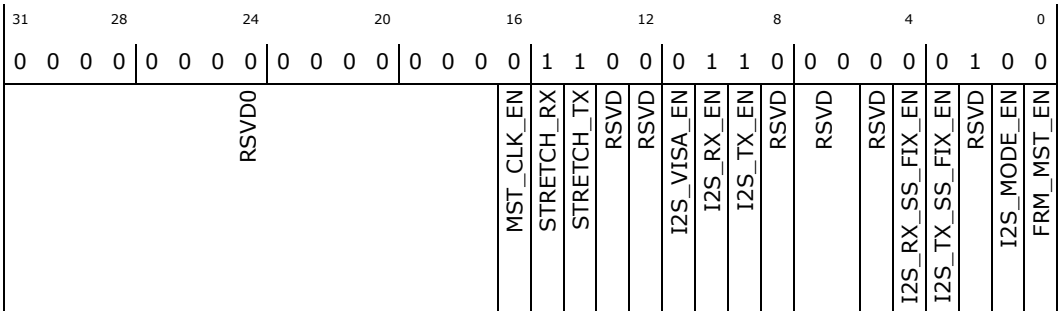
Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

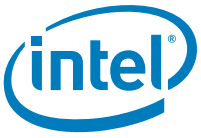
Offset: [Ipe_bridge.BAR + A5000h] + 70h

Default: 0000C604h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW	**Master Mode Clock Enable (MST_CLK_EN):** When in single slot master mode (which is the mode used for emulating I2S or LJ master mode), the SSP core can stop the clock on a Tx underflow condition, preventing the Rx side from receiving data. This bit, when set, forces the clock to run when a Tx underflow happens, thereby allowing Rx side to continue functioning while Tx side is in underflow. SW should set this bit when I2S or LJ master mode is enabled i.e. bits 0 and 1 in this register are both set or when using 1-slot PCM (SFS or LFS) master mode operation. Otherwise, SW should leave this at 0.
15	0x1 RW	**Stretch RX Pulse (STRETCH_RX):** HW uses this as a chicken bit to stretch the RX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
14	0x1 RW	**Stretch TX Pulse (STRETCH_TX):** HW uses this as a chicken bit to stretch the TX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
13	0x0 RO	**Reserved (RSVD):** Reserved.
12	0x0 RO	**Reserved (RSVD):** Reserved.
11	0x0 RW	**I2S VISA Enable (I2S_VISA_EN):** Enables newly added I2S and PCM wrapper logic debug signals sent out on the VISA bus instead of the core SSP debug signals. 0 = Core SSP Debug Signals 1 = New I2S and PCM Debug Signals
10	0x1 RW	**I2S Receive Enable (I2S_RX_EN):** When set, this bit enables data to be received on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
9	0x1 RW	**I2S Transmit Enable (I2S_TX_EN):** When set, this bit enables data to be transmitted on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
8	0x0 RO	**Reserved (RSVD):** Reserved.
7:6	0x0 RO	**Reserved (RSVD):** Reserved.
5	0x0 RO	**Reserved (RSVD):** Reserved.



Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**I2S RX Slot Swap Fix Enable (I2S_RX_SS_FIX_EN):** This bit enables the Rx overrun fix in I2S or LJ modes and prevents channel swapping when Rx overrun happens. Note that this bit does not apply to any PCM modes. PCM modes still have the Rx overflow channel aliasing issue. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
3	0x0 RW	**I2S TX Slot Swap Fix Enable (I2S_TX_SS_FIX_EN):** This bit enables the TX underflow fix in I2S or LJ modes and prevents channel swapping when TX underflow happens. Note that this bit does not apply to any PCM modes. PCM modes still have the TX underflow channel aliasing issue. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
2	0x1 RO	**Reserved (RSVD):** Reserved.
1	0x0 RW	**I2S Mode Enable (I2S_MODE_EN):** This bit enables I2S Mode. In I2S mode, slave or master mode operation is selected by appropriately clearing/setting bit 0 in this register. SW should select I2S mode operation before enabling the SSP controller. 0 = Disabled 1 = Enabled
0	0x0 RW	**Frame Master Enable (FRM_MST_EN):** When set, this bit enables the internal frame generator logic that allows accurate frame rate generation. This bit should be set for I2S and PCM master mode operations and cleared for all other modes. SW should select the proper value in this bit before enabling SSP controller. 0 = Disabled 1 = Enabled

8.10.18 SSP Control 4 Register (SSCR4)—Offset 74h

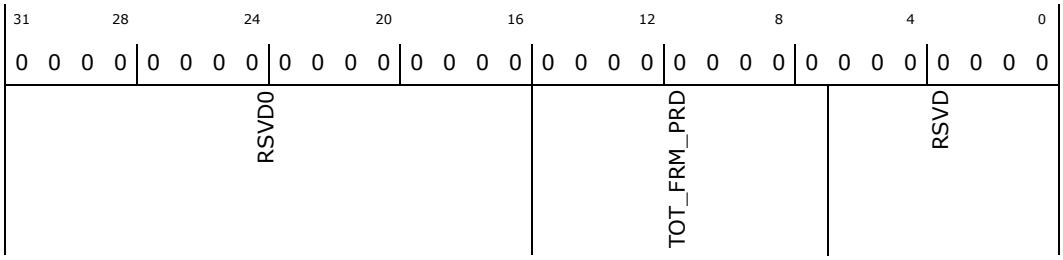
Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A5000h] + 74h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD0:** Reserved
15:7	0x0 RW	**Total Frame Period (TOT_FRM_PRD):** The total frame period (both asserted and de-asserted time of frame), measured in bit clocks, that is driven in I2S, LJ and PCM master modes. This can be controlled to get the desired accuracy on frame rate. A value of 0 and a value smaller than the value programmed in SSCR5.FrameAssertedWidth are illegal
6:0	0x0 RO	**Reserved (RSVD):** Reserved.

8.10.19 SSP Control 5 Register (SSCR5)—Offset 78h

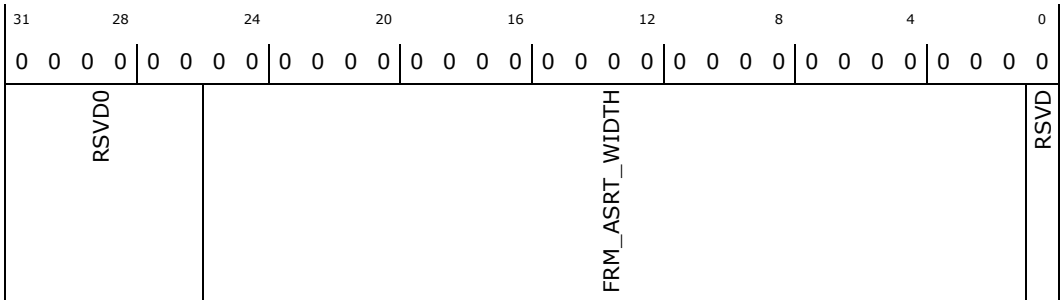
Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

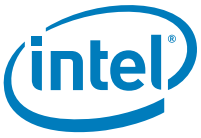
Offset: [Ipe_bridge.BAR + A5000h] + 78h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
25:1	0x0 RW	**Frame Assert Width (FRM_ASRT_WIDTH):** This field controls the width of the asserted period of frame in I2S, LJ and PCM master modes. A value of 1 indicates a width of 2 bit clock period, 2 indicates a width of 3 bit clock periods, etc. The frame width is Frame Assert Width + 1.
0	0x0 RO	**Reserved (RSVD):** Reserved.



8.11 SIO SPI 5 Memory Mapped I/O Registers

Table 62. Summary of SIO SPI 5 Memory Mapped I/O Registers—lpe_bridge.BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"SSP Control 0 Register (SSCR0)—Offset 0h" on page 3841	00000000h
4–7h	4	"SSP Control 1 Register (SSCR1)—Offset 4h" on page 3842	43000000h
8–Bh	4	"SSP Status Register (SSSR)—Offset 8h" on page 3844	0000F004h
C–Fh	4	"SSP Interupt Test Register (SSITR)—Offset Ch" on page 3846	00000000h
10–13h	4	"SSP Data Register (SSDR)—Offset 10h" on page 3847	00000000h
28–2Bh	4	"SSP Time-Out Regsiter (SSTO)—Offset 28h" on page 3848	00000000h
2C–2Fh	4	"SSP Programmable Protocol Register (SSPSP)—Offset 2Ch" on page 3848	00000000h
30–33h	4	"SSM TX Time Slot Active Register (SSTSA)—Offset 30h" on page 3849	00000000h
34–37h	4	"SSP RX Time Slot Active Register (SSRSA)—Offset 34h" on page 3850	00000000h
38–3Bh	4	"SSP Time Slot Status Register (SSTSS)—Offset 38h" on page 3850	00000000h
3C–3Fh	4	"SSP Audio Clock Divider (SSACD)—Offset 3Ch" on page 3851	00000000h
40–43h	4	"SSP Control 2 Register (SSCR2)—Offset 40h" on page 3852	00000800h
44–47h	4	"SSP Frame Select Register (SSFS)—Offset 44h" on page 3853	00000001h
48h + [0-7]*4h	4	"SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h" on page 3854	00000000h
68–6Bh	4	"SSP FIFO Level Register (SFIFOL)—Offset 68h" on page 3855	FFFF0000h
6C–6Fh	4	"SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch" on page 3855	00000000h
70–73h	4	"SSP Control 3 Register (SSCR3)—Offset 70h" on page 3856	0000C604h
74–77h	4	"SSP Control 4 Register (SSCR4)—Offset 74h" on page 3858	00000000h
78–7Bh	4	"SSP Control 5 Register (SSCR5)—Offset 78h" on page 3859	00000000h

8.11.1 SSP Control 0 Register (SSCR0)—Offset 0h

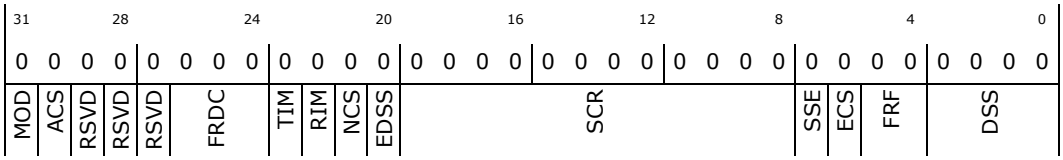
The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A6000h] + 0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Mode Select (MOD):** 0 = Normal SSP Mode 1 = Network Mode
30	0x0 RW	**Audio Clock Select (ACS):** 0 = Clock selection is determined by the NCS and ECS bits 1 = Audio Clock (and Audio Clock Divider) are used to clock the SSP's serial clock (SSPSCLK)
29	0x0 RO	**Reserved (RSVD):** Reserved.
28	0x0 RO	**Reserved (RSVD):** Reserved.
27	0x0 RO	**Reserved (RSVD):** Reserved.
26:24	0x0 RW	**Frame Rate Divider Control (FRDC):** Value 0-7 indicates the number of time slots per frame when in network mode (the actual number of time slots is FRDC+1, so 1 to 8 time slots).
23	0x0 RW	**Transmit FIFO Under Run Interrupt Mask (TIM):** 0 = TUR events will generate an SSP interrupt 1 = TUR events will not generate an SSP interrupt
22	0x0 RW	**Receive FIFO Over Run Interrupt Mask (RIM):** 0 = ROR events will generate an SSP interrupt 1 = ROR events will not generate an SSP interrupt
21	0x0 RW	**Network Clock Select (NCS):** 0 = Clock selection is determined by ECS bit 1 = Network clock is used to create the SSP's serial clock (SSPSCLK)
20	0x0 RW	**Extended Data Size Select (EDSS):** 0 = A zero is preappended to the DSS value which sets the DSS range from 4-16 bits 1 = A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits

Bit Range	Default & Access	Field Name (ID): Description
19:8	0x0 RW	**Serial Clock Rate (SCR):** Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0x0 RW	**Synchronous Serial Port Enable (SSE):** 0 = SSP operation disabled and FIFOs are cleared 1 = SSP operation enabled
6	0x0 RW	**External Clock Select (ECS):** 0 = On-chip clock used to produce the SSP's serial clock (SSPSCLK) 1 = SSPEXTCLK/GPIO pin is used to create the SSP's SSPCLK
5:4	0x0 RW	**Frame Format (FRF):** 00 = Motorola Serial Peripheral Interface (SPI) 01 = Texas Instruments Synchronous Serial Protocol (SSP) 10 = National Semiconductor Microwire 11 = Programmable Serial Protocol (PSP)
3:0	0x0 RW	**Data Size Select (DSS):** With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

8.11.2 SSP Control 1 Register (SSCR1)—Offset 4h

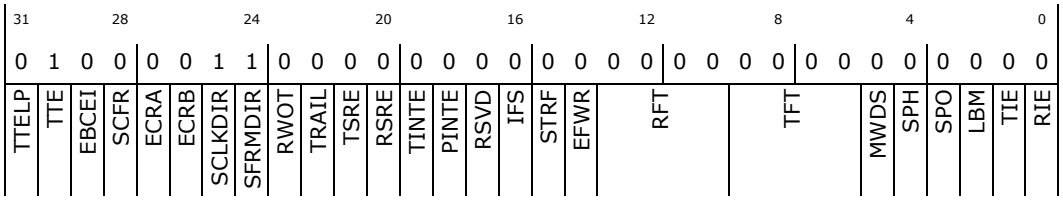
The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A6000h] + 4h

Default: 43000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**TXD Tristate Enable on Last Phase (TTELP):** 0 = TXD line will be tristated on same clock edge as TXD is to be flopped 1 = TXD line will be tristated 1/2 clock edge after TXD is to be flopped
30	0x1 RW	**TXD Tristate Enable (TTE):** 0 = TXD line will not be tristated 1 = TXD line will be tristated when no transmitting data
29	0x0 RW	**Enable Bit Count Error Interrupt (EBCEI):** 0 = Interrupt due to a bit count error is disabled 1 = Interrupt due to a bit count error is enabled

Bit Range	Default & Access	Field Name (ID): Description
28	0x0 RW	**Slave Clock Free Running (SCFR):** 0 = clock input to SSPSCLK is continuously running 1 = clock input to SSPSCLK is only active durring transfers
27	0x0 RW	**Enable Clock Request A (ECRA):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
26	0x0 RW	**Enable Clock Request B (ECRB):** 0 = clock request from other SSP is disabled 1 = clock request from other SSP is enabled
25	0x1 RW	**SSP Serial Bit Rate Clock (SSPSCLK) Direction (SCLKDIR):** 0 = Master mode, SSP drives SSPSCLK 1 = Slave mode, SSP recieves SSPSCLK
24	0x1 RW	**SSP Frame (SSPSFRM) Direction (SFRMDIR):** 0 = Master mode, SSP drives SSPSFRM 1 = Slave mode, SSP receives SSPSFRM
23	0x0 RW	**Receive With Out Transmit (RWOT):** 0 = Transmit/Receive mode 1 = Receive without transmit mode
22	0x0 RW	**Trailing Byte (TRAIL):** 0 = Processor based, trailing bytes are handled by processor 1 = DMA based, trailing bytes are handled by DMA
21	0x0 RW	**Transmit Service Request Enable (TSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
20	0x0 RW	**Receive Service Request Enable (RSRE):** 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
19	0x0 RW	**Receiver Time-out Interrupt Enable (TINTE):** 0 = Receiver Time-out interrupts are disabled 1 = Receiver Time-out interrupts are enabled
18	0x0 RW	**Peripheral Trailing Byte Interrupts Enable (PINTE):** 0 = Peripheral Trailing Byte Interrupts are disabled 1 = Peripheral Trailing Byte Interrupts are enabled
17	0x0 RW	**RSVD:** Reserved
16	0x0 RW	**Invert Frame Signal (IFS):** 0 = Frame polarity is determined by SSP format and PSP polarity bits 1 = Frame signal will be inverted from the normal SSP frame signal (as defined by the SSP format nad PSP polarity bits)
15	0x0 RW	**Select FIFO for EFWR (test mode bit) (when EFWR=1) (STRF):** 0 = Transmit FIFO is selected for both writes and reads through the SSP Data Register (SSDR) 1 = Receive FIFO is selected for both writes and reads through the SSP Data Register (SSDR)
14	0x0 RW	**Enable FIFO Write/Read (test mode bit) (EFWR):** 0 = FIFO write/read special function is disabled (normal SSP operational mode) 1 = FIFO write/read special function is enabled

Bit Range	Default & Access	Field Name (ID): Description
13:10	0x0 RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
9:6	0x0 RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. This is a legacy field and only represents the lower 4b of the FIFO Trigger Threshold. Please see SFIFOTT register for complete threshold setting.
5	0x0 RW	**Microwire Transmit Data Size (MWDS):** 0 = 8-bit command words are transmitted 1 = 16-bit command words are transmitted
4	0x0 RW	**Motorola SPI SSPSCLK Phase Setting (SPH):** 0 = SSPSCLK is inactive one sycle at the start of a fram and 1/2 cycle at the end of a frame 1 = SSPSCLK is inactive 1/2 cycle at the start of a frame and one cycle at the end of a frame
3	0x0 RW	**Motorola SPI SSPSCLK polarity setting (SPO):** 0 = The inactive or idle state of SSPSCLK is low 1 = The inactive or idle state of SSPSCLK is high
2	0x0 RW	**Loop-Back Mode (test mode bit) (LBM):** 0 = Normal serial port operation enabled 1 = Output of transmit serial shifter connected to input of receive serial shifter, internally
1	0x0 RW	**Transmit FIFO Interrupt Enable (TIE):** 0 = Transmit FIFO level interrupt is disabled 1 = Transmit FIFO level interrupt is enabled
0	0x0 RW	**Receive FIFO Interrupt Enable (RIE):** 0 = Receive FIFO level interrupt is disabled 1 = Receive FIFO level interrupt is enabled

8.11.3 SSP Status Register (SSSR)—Offset 8h

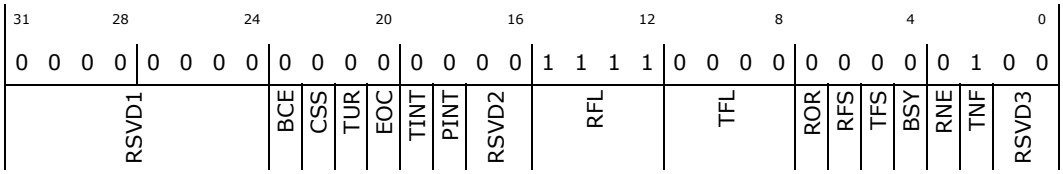
The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A6000h] + 8h

Default: 0000F004h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD1:** Reserved
23	0x0 RW/1C	**Bit Count Error (BCE):** 0 = SSP has not experienced a bit count error 1 = SSPSFRM signal has been asserted when the bit counter was not 0
22	0x0 RO	**Clock Synchronization Status (CSS):** 0 = SSP is ready for slave clock operations 1 = SSP is currently busy synchronizing slave mode signals
21	0x0 RW/1C	**Transmit FIFO Under Run (TUR):** 0 = Transmit FIFO has not experienced an under run 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0x0 RW/1C	**End of Chain (EOC):** 0 = DMA has not signaled an end of chain condition 1 = DMA has signaled an end of chain condition
19	0x0 RW/1C	**Receiver Time-out Interrupt (TINT):** 0 = No receiver time-out pending 1 = Receiver time-out pending
18	0x0 RW/1C	**Peripheral Trailing Byte Interrupt (PINT):** 0 = No peripheral trailing byte interrupt pending 1 = Peripheral trailing byte interrupt pending
17:16	0x0 RO	**RSVD2:** Reserved
15:12	0xf RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value 0xF is read, the FIFO is either empty or full and the programmer should refer to the RNE bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
11:8	0x0 RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the TNF bit. This is a legacy register and only represents the lower 4b of the FIFO Level. The SFIFOL register contains the full FIFO level status.
7	0x0 RW/1C	**Receive FIFO Overrun (ROR):** 0 = Receive FIFO has not experienced an overrun 1 = Attempted data write to full receive FIFO, request interrupt
6	0x0 RO	**Receive FIFO Service Request (RFS):** 0 = Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0x0 RO	**Transmit FIFO Service Request (TFS):** 0 = Transmit FIFO level exceeds the TFT threshold (TFT+1), or SSP disabled 1 = Transmit FIFO level is at or below TFT threshold (TFT+1), request interrupt

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RO	**SSP Busy (BSY):** 0 = SSP is idle or disabled 1 = SSP currently transmitting or receiving a frame
3	0x0 RO	**Receive FIOF Not Empty (RNE):** 0 = Receive FIFO is empty 1 = Receive FIFO is not empty
2	0x1 RO	**Transmit FIFO Not Full (TNF):** 0 = Transmit FIFO is full 1 = Transmit FIFO is not full
1:0	0x0 RO	**RSVD3:** Reserved

8.11.4 SSP Interupt Test Register (SSITR)—Offset Ch

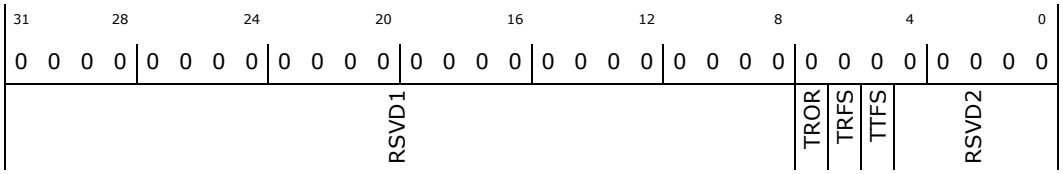
The read-write SSP Interrupt Test registers should be used only for testing purposes. Writing a 1 to the test transmit FIFO request SSITR.TTFS, bit 5, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Transmit FIFO. Writing a 1 to the test receive FIFO request SSITR.TRFS, bit 6, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Receive FIFO. Writing a 1 to the test receive FIFO overrun bit SSITR.TROR, bit 7, will generate a non-maskable Interrupt strobe signal to the Interrupt controller only, no DMA request will be made. Setting any of these bits will also cause the corresponding status bit(s) to be set in the Enhanced SSP Status register (SSSR). The Interrupt and/or service request, caused by the setting of one of these test bits, will remain active until the test bit is cleared by writing a 0 it. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A6000h] + Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD1:** Reserved
7	0x0 RW	**Test Receive FIFO overrun (TROR):** 0 = No receive FIFO overrun service request 1 = Generates non-maskable interrupt to CPU. No DMA request is generated
6	0x0 RW	**Test Receive FIFO service request (TRFS):** 0 = No receive FIFO service request 1 = Generates non-maskable interrupt to CPU and a DMA request for receive FIFO

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW	**Test Transmit FIFO service request (TTFS):** 0 = No transmit FIFO service request pending 1 = Generates non-maskable interrupt to CPU and a DMA request for transmit FIFO
4:0	0x0 RO	**RSVD2:** Reserved

8.11.5 SSP Data Register (SSDR)—Offset 10h

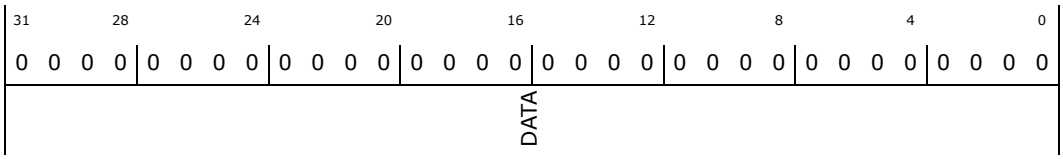
The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO, the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.TFL, SSSR.RFL, SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32-bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32-bits is automatically right-justified in the Receive FIFO. When the Enhanced SSP is programmed for National Semiconductor Microwire* frame format and if the size for Transmit data is 8-bits as selected by SSCR1.MWDS=0, then the most significant 24-bits are ignored. Similarly, if the size for the Transmit data is 16-bit as selected by SSCR1.MWDS=1, then most significant 16-bits are ignored. The SSCR0.DSS field controls the Receive data size.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A6000h] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Data (DATA):** Data word to be written to/read from transmit/receive FIFO. When reading from this register when the SSP is disabled (SSE=0) then this will return indeterminate data.

8.11.6 SSP Time-Out Regsiter (SSTO)—Offset 28h

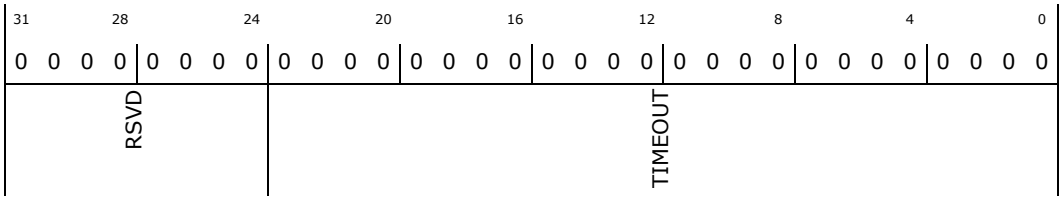
The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A6000h] + 28h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD:** Reserved
23:0	0x0 RW	**Timeout Value (TIMEOUT):** Is the value that defines the timeout interval, given by TIMEOUT/Peripheral Clock Frequency

8.11.7 SSP Programmable Protocol Register (SSPSP)—Offset 2Ch

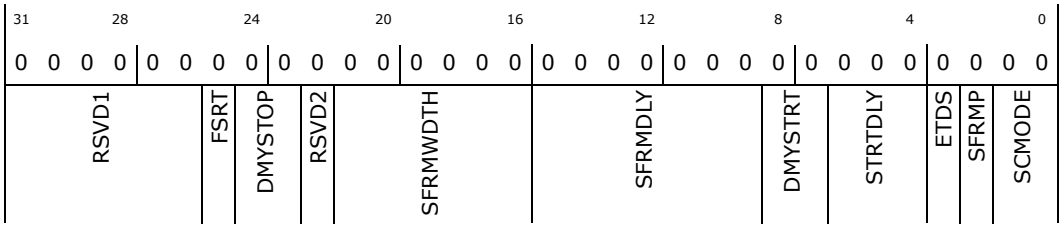
The Enhanced SSP Programmable Protocol registers are read-write registers that contain eight fields that are used to program the various programmable serial-protocol parameters. When using PSP format in Network mode, the parameters SFRMDLY, STRTDLY, DMYSTP, DMYSTRT must be set to 0. Other parameters (such as FRMPOL, SCMODE, FSRT, SFRMDWDTH) are programmable. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A6000h] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD1:** Reserved
25	0x0 RW	**Frame Sync Relative Timing Bit (FSRT):** 0 = Next frame is asserted after the end of the T4 timing 1 = Next frame is asserted with the LSB of the previous frame
24:23	0x0 RW	**Dummy Stop (DMYSTOP):** Programmed value sets the number of SSPSCLK cycles that follow the transmitted data
22	0x0 RW	**RSVD2:** Reserved
21:16	0x0 RW	**Serial Frame Width (SFRMWDTH):** Programmed value sets frame width (1-38)
15:9	0x0 RW	**Serial Frame Delay (SFRMDLY):** Programmed value sets the number of half SSPSCLK cycles from TXD/RXD being driven to SSPSFRM being asserted (0-74)
8:7	0x0 RW	**Dummy Start (DMYSTRT):** Programmed value sets the number of SSPSCLKs after STRTDLY is complete that precede the transmit/receive data
6:4	0x0 RW	**Start Delay (STRTDLY):** Programmed value sets start delay that is used to set the idle time of SSPSCLK between transfers (0-7 SSPSCLK periods)
3	0x0 RW	**End of Transfer Data State (ETDS):** 0 = Low 1 = Last value (bit 0)
2	0x0 RW	**Serial Frame Polarity (SFRMP):** 0 = SSPSFRM is active low 1 = SSPSFRM is active high
1:0	0x0 RW	**Serial bit-rate Clock Mode (SCMODE):** 00 = Data driven (falling), Data sampled (rising), Idle state (low) 01 = Data driven (rising), Data sampled (falling), Idle state (low) 10 = Data driven (rising), Data sampled (falling), Idle state (high) 11 = Data driven (falling), Data sampled (rising), Idle state (high)

8.11.8 SSM TX Time Slot Active Register (SSTSA)—Offset 30h

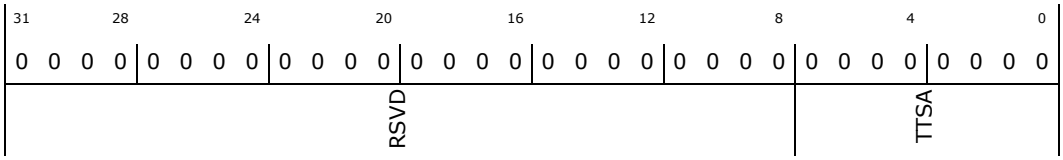
The Enhanced SSP TX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will transmit data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A6000h] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RW	**TX Time Slot Active (TTSA):** 0 = SSP will not transmit data in this time slot 1 = SSP will transmit data in this time slot

8.11.9 SSP RX Time Slot Active Register (SSRSA)—Offset 34h

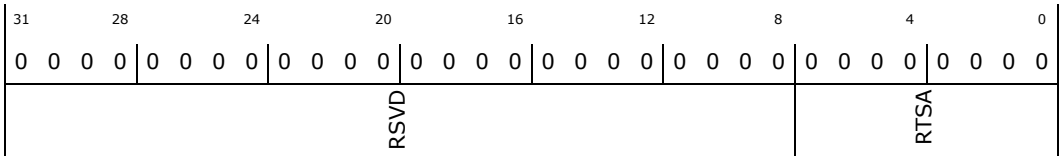
The Enhanced SSP RX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will receive data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A6000h] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RW	**RX Time Slot Active (RTSA):** 0 = SSP will not receive data in this time slot 1 = SSP will receive data in this time slot

8.11.10 SSP Time Slot Status Register (SSTSS)—Offset 38h

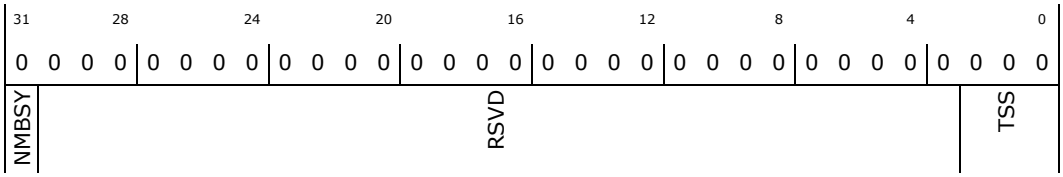
The Enhanced SSP Time Slot Status registers are read only registers that indicate which Time Slot the Enhanced SSP is currently in when the Enhanced SSP is in Network Mode (SSCR0.MOD = 1). This register is not valid when the Enhanced SSP is not in Network Mode. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A6000h] + 38h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Network Mode Busy (NMBSY):** 0 = No frame is currently active (in network mode only) 1 = SSP is in network mode and a frame is currently active
30:3	0x0 RO	**RSVD:** Reserved
2:0	0x0 RO	**Time Slot Status (TSS):** Value indicates which time slot is currently active

8.11.11 SSP Audio Clock Divider (SSACD)—Offset 3Ch

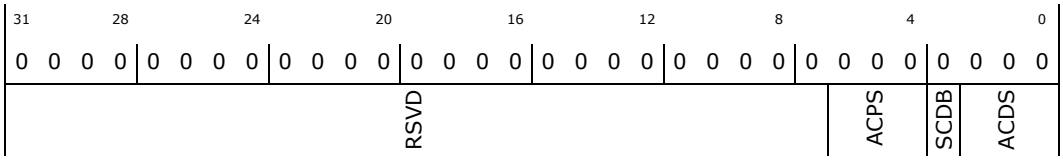
The Enhanced SSP Audio Clock Divider registers are read-write registers that indicate which clock frequency is sent to the Enhanced SSP and to the SYSCLK pin. If SSCR0.SCR is not 0, then there is no guaranteed phase relationship between SYSCLK and SSPSCLK. The SSPSFRM Frame Synch Sampling Frequency is calculated by dividing the chosen PLL output clock frequency (SSACD.ACPS) by the chosen divider (SSACD.ACDS) which gives the SYSCLK frequency. The SYSCLK is then divided by 4 (or by 1) to get the SSPSCLK. The SSPSCLK is divided by the data size (EDSS, DSS values) and by the number of time slots being used (SSCR0.FRDC value), if any, to give the SSPSFRM frequency. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined. It's important to note that this feature is only available if implemented by the project instantiation. A clock source and mux must be instantiated outside of the SSP controller for this feature to work. Only this register is designed into the SSP Controller.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A6000h] + 3Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**RSVD:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
6:4	0x0 RW	**Audio Clock PLL Select (ACPS):** Value indicates which PLL output clock is sent to the clock divider in the clock unit 000: 5.622MHz, 001: 11.345MHz, 010: 12.235MHz, 011: 14.857MHz, 100: 32.842MHz, 101: 48.000MHz, 110, 111: Reserved
3	0x0 RW	**SYSCLK Divider Bypass (SCDB):** 0 = SYSCLK is divided by 4 before being sent to SSP 1 = SYSCLK is not divided before being sent to SSP
2:0	0x0 RW	**Audio Clock Divider Select (ACDS):** Value indicates which divider will be used by the clock unit to create the SYSCLK output pin. Clock divider value will be 2^ACDS, max ACDS = 5.

8.11.12 SSP Control 2 Register (SSCR2)—Offset 40h

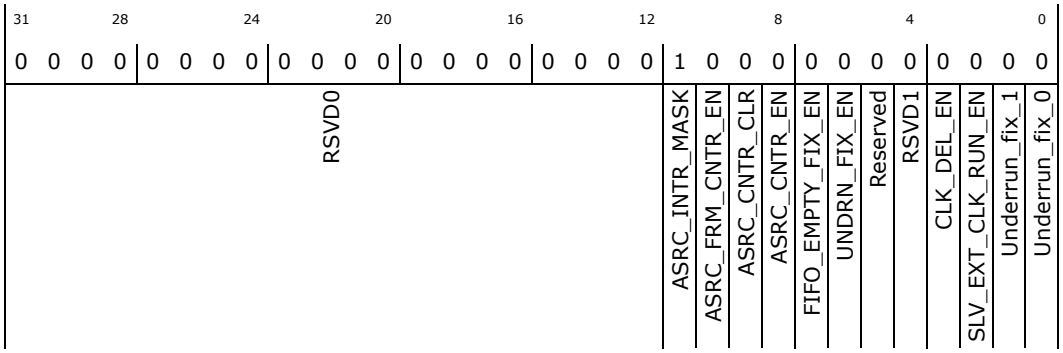
The command status register 2 is extension of command status register and contains various feature enable and disables.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A6000h] + 40h

Default: 00000800h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RSVD0:** Reserved
11	0x1 RW	**ASRC Interrupt Mask (ASRC_INTR_MASK):** Setting this bit to 1 masks the ASRC interrupt that is generated every time the frame count matches the frame threshold.
10	0x0 RW	**ASRC frame count enable (ASRC_FRM_CNTR_EN):** Setting this bit enables the frame counter to start running. Clearing this bit will make the frame counter go back to zero immediately.

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RW/AC	**ASRC Counter Clear (ASRC_CNTR_CLR):** Setting this to 1 will clear the ASRC Free running counter. This bit will self clear after the counter is cleared.
8	0x0 RW	**ASRC Counter enable (ASRC_CNTR_EN):** Setting this bit makes the Free running ASRC counter to start running. Clearing this bit will make it pause and hold it's current value.
7	0x0 RW	**Fifo empty fix enable (FIFO_EMPTY_FIX_EN):** Corner cases between the FIFO empty and APB writes happening to the TX FIFO around the time the new data needs to be sent out on the TXD are fixed with this bit.
6	0x0 RW	**Underrun fix enable (UNDRN_FIX_EN):** OSC to PLL switch along with underrun was causing unexpected behavior. This bit enables the fix for that bug.
5	0x0 RW	**Reserved:** This is a RW bit with no effect on IP behavior
4	0x0 RO	**RSVD1:** Reserved
3	0x0 RW	**Clock Delay Enable (CLK_DEL_EN):** When CLK_DEL_EN = 0, delay logic for capturing data from device is disabled. When CLK_DEL_EN = 1, delay logic for capturing data from device is delayed by half a period of the IO clock
2	0x0 RW	**Slave Mode External Clock Run Enable (SLV_EXT_CLK_RUN_EN):** When in Slave mode the receive state machine requires several clock edges (around 6) to properly sample incoming data. This bit enables a free running clock to the receive state machine before any data is received to properly sample the incoming data. 0 = Disable 1 = Enable
1	0x0 RW	**Mode 1 Underrun Fix (Underrun_fix_1):** Mode 1 of transmit underrun fix. In this mode, new data will start on the underrun slot. This function is only appled to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1 If both underrun modes are enable, mode 1 has higher priority.
0	0x0 RW	**Mode 0 Underrun Fix (Underrun_fix_0):** Mode 0 of transmit underrun fix. In this mode, new data will always start at slot 0. This function is only applied to TI and PSP modes. 0 = disable mode 1 1 = enable mode 1

8.11.13 SSP Frame Select Register (SSFS)—Offset 44h

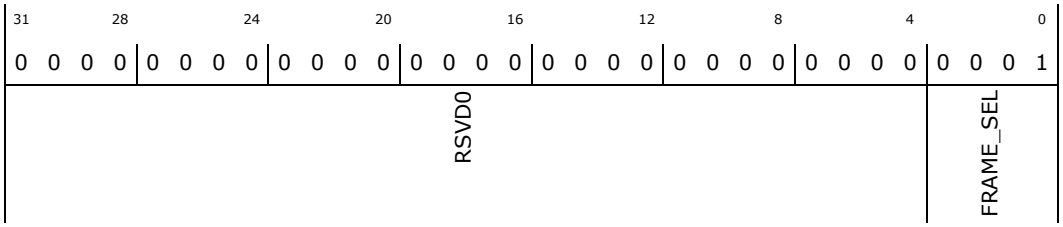
The SSP Frame select register is used to choose which frame signal to assert when accessing a slave device. SW drivers should set this register to assert the correct frame select to the targetted device.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A6000h] + 44h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RSVD0:** Reserved
3:0	0x1 RW	**Frame Select Enable (FRAME_SEL):** Each bit in this field corresponds to a frame signal of the SSP Controller. Not all SSP controllers have all frame selects pinned out so consult the pin list for indication of which SSP controllers support how many frame signals. [Bit 0] Frame Select 0 Master and Slave Supported [Bit 1] Frame Select 1 Master Only [Bit 2] Frame Select 2 Master Only [Bit 3] Frame Select 3 Master Only 0 = Frame Select Disabled 1 = Frame Select Enabled

8.11.14 SSP Slot Frame Counter Register[0-7] (FRAME_CNT[0-7])—Offset 48h, Count 8, Stride 4h

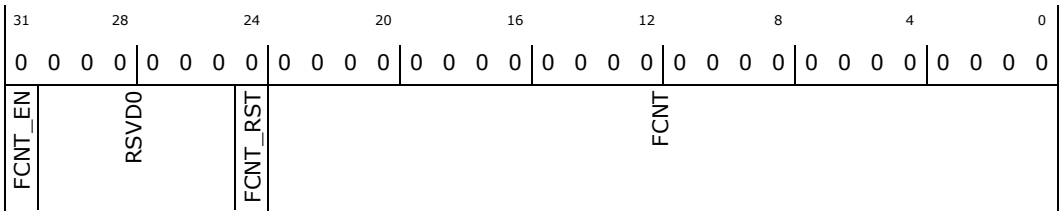
The slot frame counter is typically used in Audio modes and increments the counter every two SSPSCLKs. This allows the OS to check the progress of a transfer. Since the SSP can support upto 8 slots in network mode there are 8 slot frame counters.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset[0-7]: [Ipe_bridge.BAR + A6000h] + 48h + [0-7]*4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Slot Frame Count Enable (FCNT_EN):** 0 = Disable frame counter. 1 = Enable frame counter.
30:25	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
24	0x0 WO	**Slot Frame Count Reset (FCNT_RST):** SSP frame counter reset. Writing a 1 to this bit clears the frame counter.
23:0	0x0 RO	**Slot Frame Count (FCNT):** SSP frame count.

8.11.15 SSP FIFO Level Register (SFIFOL)—Offset 68h

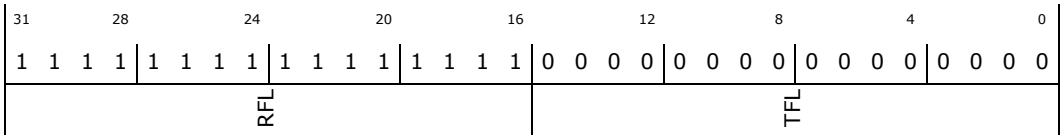
The SFIFOL register describes the current state of the RX and TX FIFOs. Not all bits of the TFL and RFL fields are used and depends on the actual hardware FIFO depth used in the instantiation of the SSP controller. This FIFO level register is meant to replace the SSSR.TFL and SSR.RFL fields.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A6000h] + 68h

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RO	**Receive FIFO Level (RFL):** Number of entries minus one in Receive FIFO. Note: When the value of all 0xF's are read, the FIFO is either empty or full and the programmer should refer to the SSSR.RNE bit.
15:0	0x0 RO	**Transmit FIFO Level (TFL):** Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the SSSR.TNF bit.

8.11.16 SSP FIFO Trigger Threshold Register (SFIFOTT)—Offset 6Ch

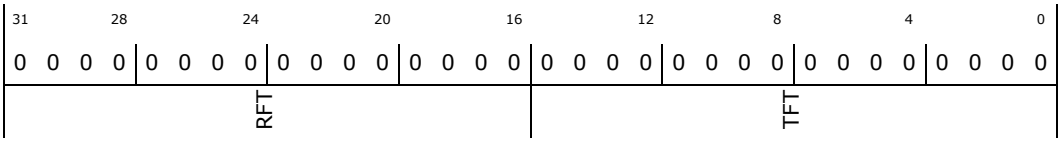
The SFIFOTT is a register that determines when the the FIFOs will assert an interrupt for FIFO full indication. This is meant to replace the SSCR1.RFT and SSCR1.TFT legacy registers. The max size of these registers is based on the actualy FIFO depth in hardware and not the actual size of the bit field.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [lpe_bridge.BAR + A6000h] + 6Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Receive FIFO Trigger Threshold (RFT):** Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1. Notes on setting the RFT value. This applies to cases where SSP is receiving data from a device and is interfaced with a DMA channel via the hardware handshake mechanism. Please follow the following recommendations: 1. Number of bits denoted by the (DSS, EDSS) parameters in the SSP should match the SRC_TR_WIDTH programmed in the DMA channel. 2. (RFT+1) should be equal to (SRC_MSIZE). 3. Another option to 2 is to keep the BLOCK_TS in the DMA to be a multiple of (RFT+1)
15:0	0x0 RW	**Transmit FIFO Trigger Threshold (TFT):** Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.

8.11.17 SSP Control 3 Register (SSCR3)—Offset 70h

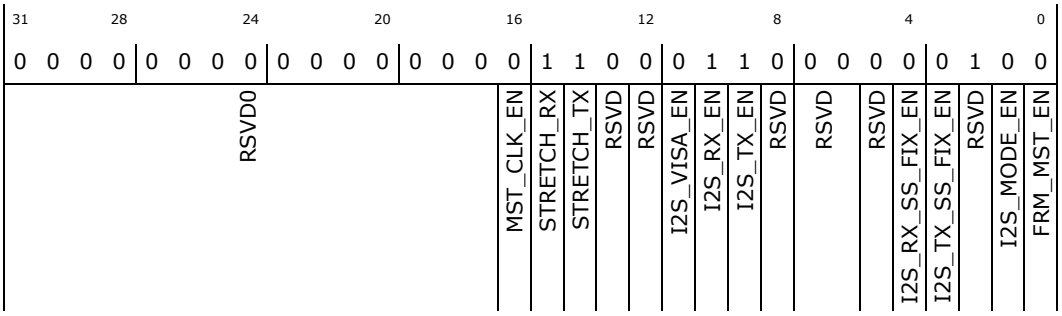
Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [Ipe_bridge.BAR + A6000h] + 70h

Default: 0000C604h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW	**Master Mode Clock Enable (MST_CLK_EN):** When in single slot master mode (which is the mode used for emulating I2S or LJ master mode), the SSP core can stop the clock on a Tx underflow condition, preventing the Rx side from receiving data. This bit, when set, forces the clock to run when a Tx underflow happens, thereby allowing Rx side to continue functioning while Tx side is in underflow. SW should set this bit when I2S or LJ master mode is enabled i.e. bits 0 and 1 in this register are both set or when using 1-slot PCM (SFS or LFS) master mode operation. Otherwise, SW should leave this at 0.
15	0x1 RW	**Stretch RX Pulse (STRETCH_RX):** HW uses this as a chicken bit to stretch the RX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
14	0x1 RW	**Stretch TX Pulse (STRETCH_TX):** HW uses this as a chicken bit to stretch the TX pulse for proper clock crossing between SSP and APB domains. Note this bit is not tied to any specific SSP/PCM/I2S modes. SW should preserve this bit as the default value.
13	0x0 RO	**Reserved (RSVD):** Reserved.
12	0x0 RO	**Reserved (RSVD):** Reserved.
11	0x0 RW	**I2S VISA Enable (I2S_VISA_EN):** Enables newly added I2S and PCM wrapper logic debug signals sent out on the VISA bus instead of the core SSP debug signals. 0 = Core SSP Debug Signals 1 = New I2S and PCM Debug Signals
10	0x1 RW	**I2S Receive Enable (I2S_RX_EN):** When set, this bit enables data to be received on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
9	0x1 RW	**I2S Transmit Enable (I2S_TX_EN):** When set, this bit enables data to be transmitted on both the left and right slots of I2S. Otherwise, data on the slots are ignored. HW does not signal FIFO full condition when this bit is cleared. SW can set/clear this bit dynamically when I2S mode is operational.
8	0x0 RO	**Reserved (RSVD):** Reserved.
7:6	0x0 RO	**Reserved (RSVD):** Reserved.
5	0x0 RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**I2S RX Slot Swap Fix Enable (I2S_RX_SS_FIX_EN):** This bit enables the Rx overrun fix in I2S or LJ modes and prevents channel swapping when Rx overrun happens. Note that this bit does not apply to any PCM modes. PCM modes still have the Rx overflow channel aliasing issue. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
3	0x0 RW	**I2S TX Slot Swap Fix Enable (I2S_TX_SS_FIX_EN):** This bit enables the TX underflow fix in I2S or LJ modes and prevents channel swapping when TX underflow happens. Note that this bit does not apply to any PCM modes. PCM modes still have the TX underflow channel aliasing issue. SW should set this bit only when I2S or LJ mode (slave or master) is enabled. 0 = Disable 1 = Enable
2	0x1 RO	**Reserved (RSVD):** Reserved.
1	0x0 RW	**I2S Mode Enable (I2S_MODE_EN):** This bit enables I2S Mode. In I2S mode, slave or master mode operation is selected by appropriately clearing/setting bit 0 in this register. SW should select I2S mode operation before enabling the SSP controller. 0 = Disabled 1 = Enabled
0	0x0 RW	**Frame Master Enable (FRM_MST_EN):** When set, this bit enables the internal frame generator logic that allows accurate frame rate generation. This bit should be set for I2S and PCM master mode operations and cleared for all other modes. SW should select the proper value in this bit before enabling SSP controller. 0 = Disabled 1 = Enabled

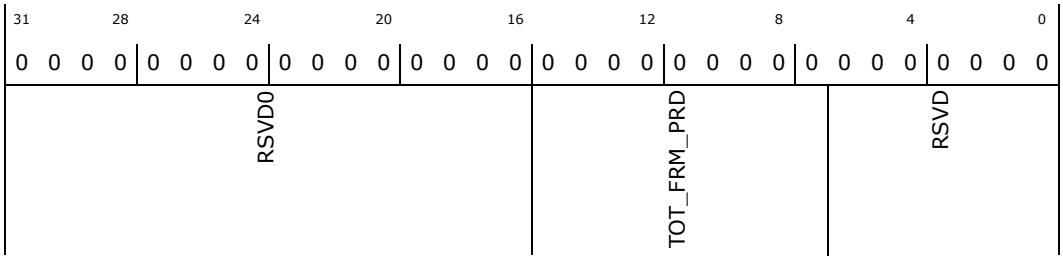
8.11.18 SSP Control 4 Register (SSCR4)—Offset 74h

Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** [Ipe_bridge.BAR + A6000h] + 74h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD0:** Reserved
15:7	0x0 RW	**Total Frame Period (TOT_FRM_PRD):** The total frame period (both asserted and de-asserted time of frame), measured in bit clocks, that is driven in I2S, LJ and PCM master modes. This can be controlled to get the desired accuracy on frame rate. A value of 0 and a value smaller than the value programmed in SSCR5.FrameAssertedWidth are illegal
6:0	0x0 RO	**Reserved (RSVD):** Reserved.

8.11.19 SSP Control 5 Register (SSCR5)—Offset 78h

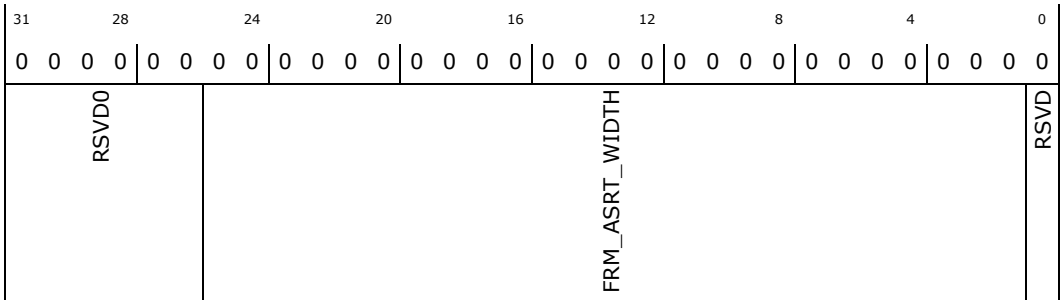
Software should only program this register if configuring the SSP in I2S/LJ mode or PCM master mode. If neither is being enabled, SW can leave this register at the default power on value.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

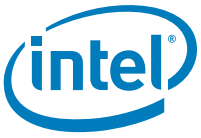
Offset: [Ipe_bridge.BAR + A6000h] + 78h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
25:1	0x0 RW	**Frame Assert Width (FRM_ASRT_WIDTH):** This field controls the width of the asserted period of frame in I2S, LJ and PCM master modes. A value of 1 indicates a width of 2 bit clock period, 2 indicates a width of 3 bit clock periods, etc. The frame width is Frame Assert Width + 1.
0	0x0 RO	**Reserved (RSVD):** Reserved.



8.12 LPE Audio Memory Mapped I/O Registers

Table 63. Summary of LPE Audio Memory Mapped I/O Registers—lpe_bridge.BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–7h	8	"reg_CSR_type (CSR)—Offset 0h" on page 3864	0000790001E40001h
8–Fh	8	"reg_XT_PISR_type (PISR)—Offset 8h" on page 3866	0000000000000000h
10–17h	8	"reg_XT_PIMR_type (PIMR)—Offset 10h" on page 3867	0000000000000000h
18–1Fh	8	"reg_IA_PISR_type (ISRX)—Offset 18h" on page 3869	0000000000000000h
20–27h	8	"reg_ISRD_type (ISRD)—Offset 20h" on page 3870	0000000000000000h
28–2Fh	8	"reg_IA_PIMR_type (IMRX)—Offset 28h" on page 3870	0000000000000000h
30–37h	8	"reg_IMRD_type (IMRD)—Offset 30h" on page 3872	0000000000000000h
38–3Fh	8	"reg_IPCX_type (IPCX)—Offset 38h" on page 3872	0000000000000000h
40–47h	8	"reg_IPCD_type (IPCD)—Offset 40h" on page 3873	0000000000000000h
48–4Fh	8	"reg_ISRSC_type (ISRSC)—Offset 48h" on page 3874	0000000000000000h
50–57h	8	"reg_ISRLPESC_type (ISRLPESC)—Offset 50h" on page 3874	0000000000000000h
58–5Fh	8	"reg_IMRSC_type (IMRSC)—Offset 58h" on page 3875	0000000000000000h
60–67h	8	"reg_IMRLPESC_type (IMRLPESC)—Offset 60h" on page 3876	0000000000000000h
68–6Fh	8	"reg_IPCSC_type (IPCSC)—Offset 68h" on page 3877	0000000000000000h
70–77h	8	"reg_IPCLPESC_type (IPCLPESC)—Offset 70h" on page 3877	0000000000000000h
78–7Fh	8	"reg_CLKCTL_type (CLKCTL)—Offset 78h" on page 3878	00000000003F0013h
80–87h	8	"reg_FR_LAT_REQ_type (FR_LAT_REQ)—Offset 80h" on page 3879	0000000000000000h
88–8Fh	8	"reg_CHICKEN_BITS_type (CHICKEN_BITS)—Offset 88h" on page 3880	0000000000000000h
90–97h	8	"reg_ISRPSH_type (ISRPSH)—Offset 90h" on page 3881	0000000000000000h
98–9Fh	8	"reg_ISRLPEPSH_type (ISRLPEPSH)—Offset 98h" on page 3881	0000000000000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
A0–A7h	8	"reg_IMRPSH_type (IMRPSH)—Offset A0h" on page 3882	0000000000000000h
A8–AFh	8	"reg_IMRLPEPSH_type (IMRLPEPSH)—Offset A8h" on page 3883	0000000000000000h
B0–B7h	8	"reg_IPCPSH_type (IPCPSH)—Offset B0h" on page 3883	0000000000000000h
B8–BFh	8	"reg_IPCLPEPSH_type (IPCLPEPSH)—Offset B8h" on page 3884	0000000000000000h
C0–C7h	8	"reg_EXT_TIMER_CNTL_type (EXT_TIMER_CNTL)—Offset C0h" on page 3885	0000000000000000h
C8–CFh	8	"reg_EXT_TIMER_STAT_type (EXT_TIMER_STAT)—Offset C8h" on page 3886	0000000000000000h
D0–D7h	8	"reg_S0ix_TIMER_CNTL_type (S0ix_TIMER_CNTL)—Offset D0h" on page 3886	0000000000000000h
D8–DFh	8	"reg_S0ix_TIMER_STAT_type (S0ix_TIMER_STAT)—Offset D8h" on page 3887	0000000000000000h
E0–E7h	8	"reg_RAW_PISR_type (XT_RAW_PISR)—Offset E0h" on page 3887	0000000000000000h
E8–EFh	8	"reg_SSP0_DIV_CTRL_type (SSP0_DIV_CTRL)—Offset E8h" on page 3888	8000000100000001h
F0–F7h	8	"reg_SSP1_DIV_CTRL_type (SSP1_DIV_CTRL)—Offset F0h" on page 3889	8000000100000001h
F8–FFh	8	"reg_SSP2_DIV_CTRL_type (SSP2_DIV_CTRL)—Offset F8h" on page 3890	8000000100000001h
100–107h	8	"reg_SSP3_DIV_CTRL_type (SSP3_DIV_CTRL)—Offset 100h" on page 3891	8000000100000001h
108–10Fh	8	"reg_SSP4_DIV_CTRL_type (SSP4_DIV_CTRL)—Offset 108h" on page 3891	8000000100000001h
110–117h	8	"reg_SSP5_DIV_CTRL_type (SSP5_DIV_CTRL)—Offset 110h" on page 3892	8000000100000001h

8.12.1 reg_CSR_type (CSR)—Offset 0h

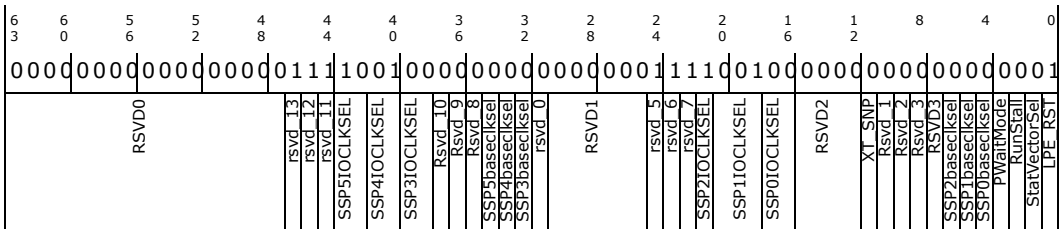
This register controls clock and reset of the block, various configurations of the block and reflects general status of the block.

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 0h

Default: 0000790001E40001h



Bit Range	Default & Access	Field Name (ID): Description
63:47	0x0 RO	**RSVD0:** Reserved
46	0x1 RW	**rsvd_13:** Reserved
45	0x1 RW	**rsvd_12:** Reserved
44	0x1 RW	**rsvd_11:** Reserved
43:42	0x2 RW	**SSP5IOCLKSEL:** SSP 5 IO clock select 0: select SSP 3 IO clock for SSP 2 IO clock input 1: select SSP 4 IO clock for SSP 2 IO clock input 2: select SSP 5 IO clock for SSP 2 IO clock input
41:40	0x1 RW	**SSP4IOCLKSEL:** SSP 4 IO clock select 0: select SSP 3 IO clock for SSP 1 IO clock input 1: select SSP 4 IO clock for SSP 1 IO clock input 2: select SSP 5 IO clock for SSP 1 IO clock input
39:38	0x0 RW	**SSP3IOCLKSEL:** SSP 3 IO clock select 0: select SSP 3 IO clock for SSP 0 IO clock input 1: select SSP 4 IO clock for SSP 0 IO clock input 2: select SSP 5 IO clock for SSP 0 IO clock input
37	0x0 RW	**Rsvd_10:** Reserved
36	0x0 RW	**Rsvd_9:** Reserved
35	0x0 RW	**Rsvd_8:** Reserved
34	0x0 RW	**SSP5baseclksel:** 1 =) Select 25 Mhz clock for the SSP5 base clock; 0 =) Select 19.2 Mhz clock for the SSP base clock
33	0x0 RW	**SSP4baseclksel:** 1 =) Select 25 Mhz clock for the SSP4 base clock; 0 =) Select 19.2 Mhz clock for the SSP base clock
32	0x0 RW	**SSP3baseclksel:** 1 =) Select 25 Mhz clock for the SSP3 base clock; 0 =) Select 19.2 Mhz clock for the SSP base clock

Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**rsvd_0:** Reserved.
30:25	0x0 RO	**RSVD1:** Reserved
24	0x1 RW	**rsvd_5:** Reserved
23	0x1 RW	**rsvd_6:** Reserved
22	0x1 RW	**rsvd_7:** Reserved
21:20	0x2 RW	**SSP2IOCLKSEL:** SSP 2 IO clock select 0: select SSP 0 IO clock for SSP 2 IO clock input 1: select SSP 1 IO clock for SSP 2 IO clock input 2: select SSP 2 IO clock for SSP 2 IO clock input
19:18	0x1 RW	**SSP1IOCLKSEL:** SSP 1 IO clock select 0: select SSP 0 IO clock for SSP 1 IO clock input 1: select SSP 1 IO clock for SSP 1 IO clock input 2: select SSP 2 IO clock for SSP 1 IO clock input
17:16	0x0 RW	**SSP0IOCLKSEL:** SSP 0 IO clock select 0: select SSP 0 IO clock for SSP 0 IO clock input 1: select SSP 1 IO clock for SSP 0 IO clock input 2: select SSP 2 IO clock for SSP 0 IO clock input
15:12	0x0 RO	**RSVD2:** Reserved
11	0x0 RW	**XT_SNP:** This bit controls whether the Tensilica initiated traffic is Snooped or Non-snooped. 0 =) Non-Snooped 1 =) Snooped
10	0x0 RW	**Rsvd_1:** Reserved
9	0x0 RW	**Rsvd_2:** Reserved
8	0x0 RW	**Rsvd_3:** Reserved
7	0x0 RO	**RSVD3:** Reserved
6	0x0 RW	**SSP2baseclksel:** 1 =) Select 25 Mhz clock for the SSP2 base clock; 0 =) Select 19.2 Mhz clock for the SSP base clock
5	0x0 RW	**SSP1baseclksel:** 1 =) Select 25 Mhz clock for the SSP1 base clock; 0 =) Select 19.2 Mhz clock for the SSP base clock
4	0x0 RW	**SSP0baseclksel:** 1 =) Select 25 Mhz clock for the SSP0 base clock; 0 =) Select 19.2 Mhz clock for the SSP base clock
3	0x0 RO	**PWaitMode:** Satus bit when set to '1 indicates that LPE core is stalled.
2	0x0 RW	**RunStall:** When set to '1, LPE core is stalled.
1	0x0 RW	**StatVectorSel:** When set to '1, LPE core boots from the Alternate reset vector. This is set to ff2c_0000 - first address of Audio IRAM. Default reset vector is set to 0x100000.

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**LPE_RST:** LPE Reset. LPE held in reset state until this bit is set to 0. Minimum number of cycles is defined LPE manual. The bit should be cleared by writing a '0' into this bit, to bring the LPE out of reset.

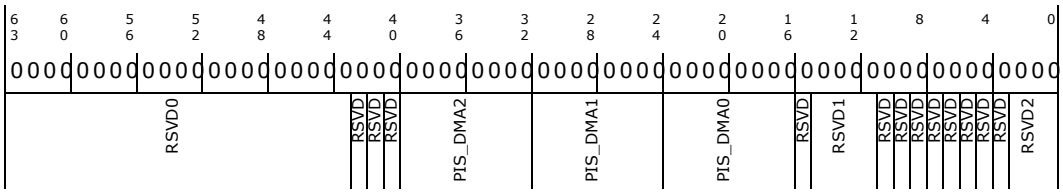
8.12.2 reg_XT_PISR_type (PISR)—Offset 8h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 8h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:43	0x0 RO	**RSVD0:** Reserved
42	0x0 RO	**Reserved (RSVD):** Reserved.
41	0x0 RO	**Reserved (RSVD):** Reserved.
40	0x0 RO	**Reserved (RSVD):** Reserved.
39:32	0x0 RW/1C	**PIS_DMA2:** DMA 2 interrupts
31:24	0x0 RW/1C	**PIS_DMA1:** DMA 1 interrupts
23:16	0x0 RW/1C	**PIS_DMA0:** DMA 0 interrupts
15	0x0 RO	**Reserved (RSVD):** Reserved.
14:11	0x0 RO	**RSVD1:** Reserved
10	0x0 RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RO	**Reserved (RSVD):** Reserved.
8	0x0 RO	**Reserved (RSVD):** Reserved.
7	0x0 RO	**Reserved (RSVD):** Reserved.
6	0x0 RO	**Reserved (RSVD):** Reserved.
5	0x0 RO	**Reserved (RSVD):** Reserved.
4	0x0 RO	**Reserved (RSVD):** Reserved.
3	0x0 RO	**Reserved (RSVD):** Reserved.
2:0	0x0 RO	**RSVD2:** Reserved

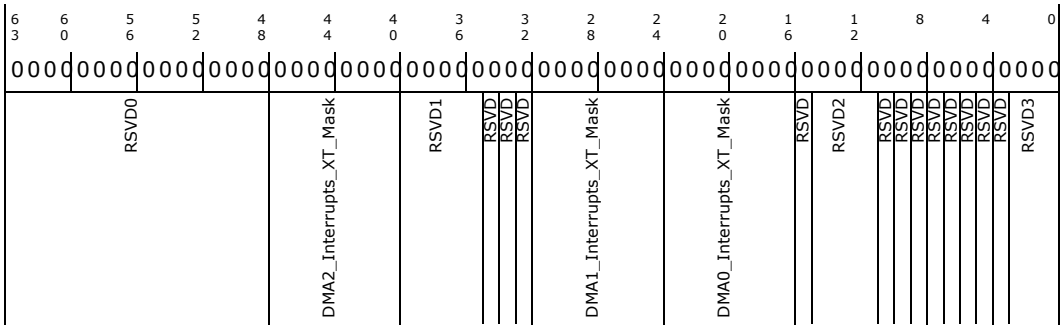
8.12.3 reg_XT_PIMR_type (PIMR)—Offset 10h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [Ipe_bridge.BAR + 140000h] + 10h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:48	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
47:40	0x0 RW	**DMA2_Interrupts_XT_Mask:** DMA 2 interrupts
39:35	0x0 RO	**RSVD1:** Reserved
34	0x0 RO	**Reserved (RSVD):** Reserved.
33	0x0 RO	**Reserved (RSVD):** Reserved.
32	0x0 RO	**Reserved (RSVD):** Reserved.
31:24	0x0 RW	**DMA1_Interrupts_XT_Mask:** DMA 1 interrupts
23:16	0x0 RW	**DMA0_Interrupts_XT_Mask:** DMA 0 interrupts
15	0x0 RO	**Reserved (RSVD):** Reserved.
14:11	0x0 RO	**RSVD2:** Reserved
10	0x0 RO	**Reserved (RSVD):** Reserved.
9	0x0 RO	**Reserved (RSVD):** Reserved.
8	0x0 RO	**Reserved (RSVD):** Reserved.
7	0x0 RO	**Reserved (RSVD):** Reserved.
6	0x0 RO	**Reserved (RSVD):** Reserved.
5	0x0 RO	**Reserved (RSVD):** Reserved.
4	0x0 RO	**Reserved (RSVD):** Reserved.
3	0x0 RO	**Reserved (RSVD):** Reserved.
2:0	0x0 RO	**RSVD3:** Reserved

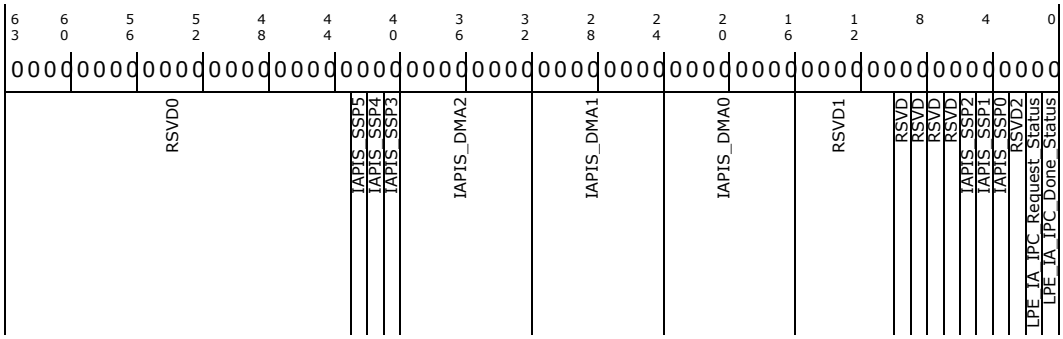
8.12.4 reg_IA_PISR_type (ISRX)—Offset 18h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 18h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:43	0x0 RO	**RSVD0:** Reserved
42	0x0 RW/1C	**IAPIS_SSP5:** SSP5 Interrupt Request for SC 1: interrupt when SSP5 interrupt is asserted. 0: Deasserted
41	0x0 RW/1C	**IAPIS_SSP4:** SSP4 Interrupt Request for SC 1: interrupt when SSP4 interrupt is asserted. 0: Deasserted
40	0x0 RW/1C	**IAPIS_SSP3:** SSP3 Interrupt Request for SC 1: interrupt when SSP3 interrupt is asserted. 0: Deasserted
39:32	0x0 RW/1C	**IAPIS_DMA2:** DMA 2 interrupts
31:24	0x0 RW/1C	**IAPIS_DMA1:** DMA 1 interrupts
23:16	0x0 RW/1C	**IAPIS_DMA0:** DMA 0 interrupts
15:10	0x0 RO	**RSVD1:** Reserved
9	0x0 RO	**Reserved (RSVD):** Reserved.
8	0x0 RO	**Reserved (RSVD):** Reserved.
7	0x0 RO	**Reserved (RSVD):** Reserved.
6	0x0 RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW/1C	**IAPIS_SSP2:** SSP2 Interrupt Request for SC 1: interrupt when SSP2 interrupt is asserted. 0: Deasserted
4	0x0 RW/1C	**IAPIS_SSP1:** SSP1 Interrupt Request for SC 1: interrupt when SSP1 interrupt is asserted. 0: Deasserted
3	0x0 RW/1C	**IAPIS_SSP0:** SSP0 Interrupt Request for SC 1: interrupt when SSP0 interrupt is asserted. 0: Deasserted
2	0x0 RO	**RSVD2:** Reserved
1	0x0 RO	**LPE_IA_IPC_Request_Status:** IPCD Interrupt Request 1: interrupt when LPE writes a message into IPCD register with bit 63 set 0: Deasserted
0	0x0 RO	**LPE_IA_IPC_Done_Status:** IPCX Interrupt Request 1: interrupt when LPE writes a message into IPCX register with bit 62 set is asserted 0: Deasserted.

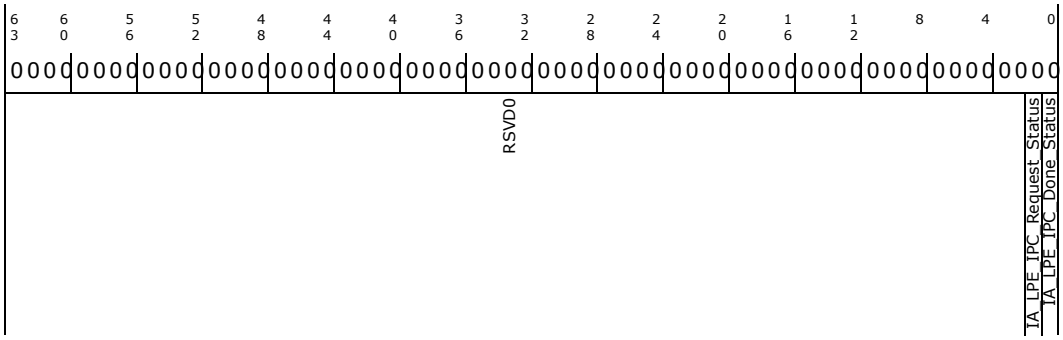
8.12.5 reg_ISRD_type (ISRD)—Offset 20h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 20h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:2	0x0 RO	**RSVD0:** Reserved
1	0x0 RO	**IA_LPE_IPC_Request_Status:** IPCIA Interrupt Request to LPE 1: interrupt when IA-32 CPU writes a message into IPCIA register with bit 63 set. 0: Deasserted
0	0x0 RO	**IA_LPE_IPC_Done_Status:** IPCLPEIA Interrupt Request to LPE 1: interrupt when IA-32 CPU writes a message into IPCLPEIA register with bit 62 set is asserted 0: Deasserted.

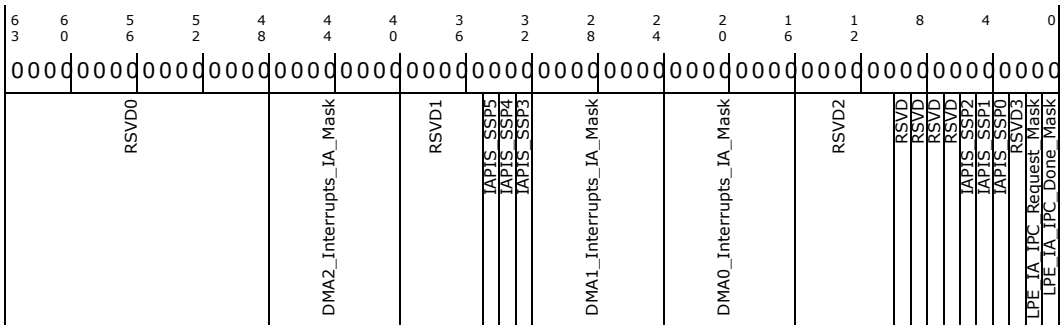
8.12.6 reg_IA_PIMR_type (IMRX)—Offset 28h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 28h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:48	0x0 RO	**RSVD0:** Reserved
47:40	0x0 RW	**DMA2_Interrupts_IA_Mask:** DMA 2 interrupts mask
39:35	0x0 RO	**RSVD1:** Reserved
34	0x0 RW	**IAPIS_SSP5:** SSP5 Interrupt Mask for IA 1: Interrupt is masked 0: Interrupt is unmasked
33	0x0 RW	**IAPIS_SSP4:** SSP4 Interrupt Mask for IA 1: Interrupt is masked 0: Interrupt is unmasked
32	0x0 RW	**IAPIS_SSP3:** SSP3 Interrupt Mask for IA 1: Interrupt is masked 0: Interrupt is unmasked
31:24	0x0 RW	**DMA1_Interrupts_IA_Mask:** DMA 1 interrupts mask
23:16	0x0 RW	**DMA0_Interrupts_IA_Mask:** DMA 0 interrupts mask
15:10	0x0 RO	**RSVD2:** Reserved
9	0x0 RO	**Reserved (RSVD):** Reserved.
8	0x0 RO	**Reserved (RSVD):** Reserved.
7	0x0 RO	**Reserved (RSVD):** Reserved.
6	0x0 RO	**Reserved (RSVD):** Reserved.
5	0x0 RW	**IAPIS_SSP2:** SSP2 Interrupt Mask for IA 1: Interrupt is masked 0: Interrupt is unmasked

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**IAPIS_SSP1:** SSP1 Interrupt Mask for IA 1: Interrupt is masked 0: Interrupt is unmasked
3	0x0 RW	**IAPIS_SSP0:** SSP0 Interrupt Mask for IA 1: Interrupt is masked 0: Interrupt is unmasked
2	0x0 RO	**RSVD3:** Reserved
1	0x0 RW	**LPE_IA_IPC_Request_Mask:** LPE to IA IPC Request Mask 1: Interrupt is masked 0: Interrupt is unmasked
0	0x0 RW	**LPE_IA_IPC_Done_Mask:** LPE to IA IPC Done Mask 1: Interrupt is masked 0: Interrupt is unmasked

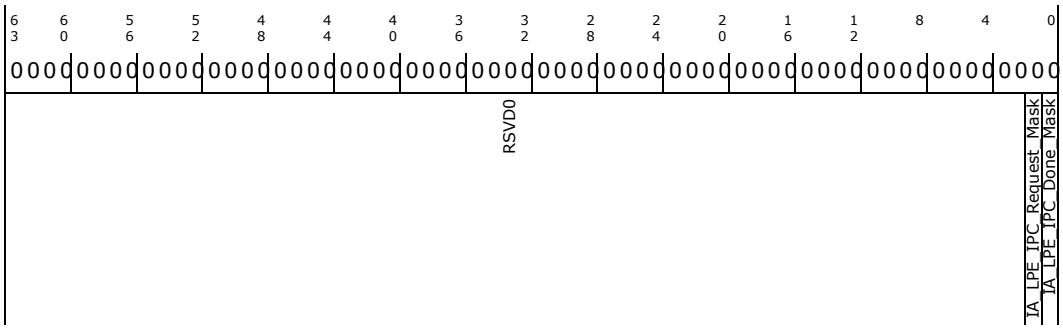
8.12.7 reg_IMRD_type (IMRD)—Offset 30h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 30h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:2	0x0 RO	**RSVD0:** Reserved
1	0x0 RW	**IA_LPE_IPC_Request_Mask:** IPCIA interrupt Enable to LPE
0	0x0 RW	**IA_LPE_IPC_Done_Mask:** IPCLPEIA interrupt Enable to LPE

8.12.8 reg_IPCX_type (IPCX)—Offset 38h

The Inter-process Status and Message register for IA-32 contains a message sent from the IA-32 CPU to LPE. The format of the CPU message bits (61:0) is not defined in the HW specs. It is defined in the LPE Firmware specifications. The message may contain optional data fields stored in the shared memory region (mailbox). When the message is written in this register, the software must set bit 63 to indicate that the IPCIA is not

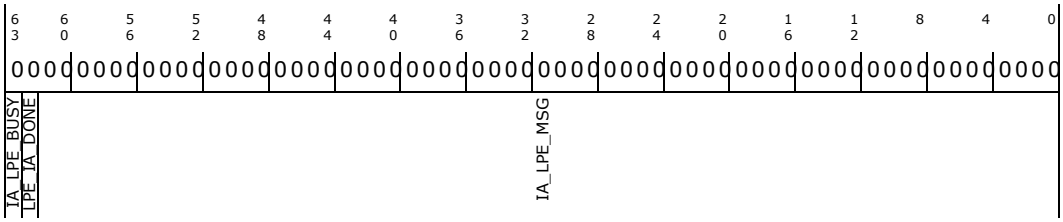
empty. Setting Busy also asserts interrupt request to LPE if the interrupt is enabled in the IMRLPEIA. After LPE reads the message code from the register, it must perform a write with bit 63 cleared. The IA-32 CPU must not attempt to write into IPCIA if bit 63 is set.

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 38h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63	0x0 RW	**IA_LPE_BUSY:** Busy. When this bit is cleared, the LPE Ready to accept a message
62	0x0 RW	**LPE_IA_DONE:** Done. When the bit is set, the LPE completed the operation and requests attention
61:0	0x0 RW	**IA_LPE_MSG:** IA-32 to LPE Message

8.12.9 reg_IPCD_type (IPCD)—Offset 40h

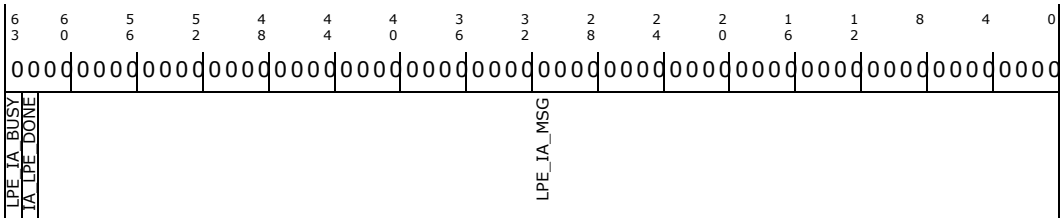
Inter-process Status and Message register for LPE contains a message sent from LPE to IA-32 CPU. The format of the CPU message bits 29:0 is defined in the LPE Firmware specifications. The message may contain optional data fields stored in the shared memory region (mailbox). When software writes the message is in this register, it should set bit 63 to indicate that the new data is written. When IA-32 CPU reads the message code from the register, and writes back with the bit 63 cleared. When the IA-32 CPU processes the message sent by LPE, it may set bit 63 in IPCD to assert interrupt request to LPE. The LPE must not attempt to write into IPCLPEIA if bit 63 is set.

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 40h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63	0x0 RW	**LPE_IA_BUSY:** Busy. When this bit is cleared, the IA CPU is Ready to accept a new message
62	0x0 RW	**IA_LPE_DONE:** Done. When the bit is set, the IA CPU completed operation and requests attention from LPE
61:0	0x0 RW	**LPE_IA_MSG:** LPE to IA CPU Message

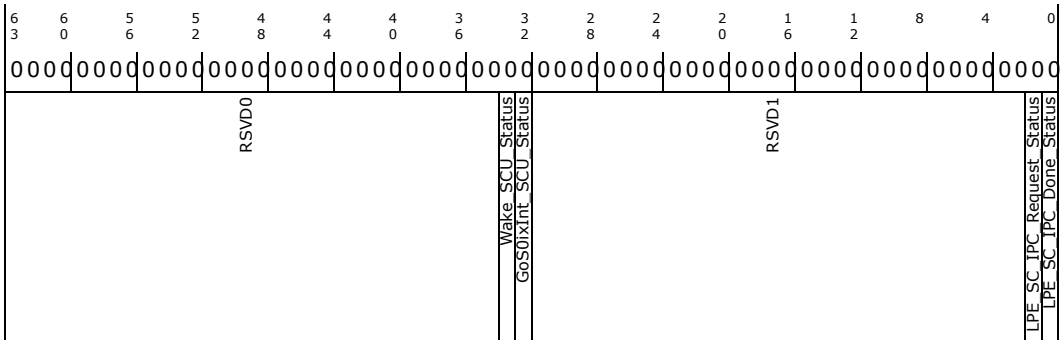
8.12.10 reg_ISRSC_type (ISRSC)—Offset 48h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 48h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:34	0x0 RO	**RSVD0:** Reserved
33	0x0 RW/1C	**Wake_SCU_Status:** This bit is set by hardware when a blocked transaction is detected. It generates a wake to the SCU
32	0x0 RW/1C	**GoS0ixInt_SCU_Status:** This bit is set by expiry of the Re-entry timer. The bit gets set only if GoS0ixInt_En bit is set and this interrupt is unmasked.
31:2	0x0 RO	**RSVD1:** Reserved
1	0x0 RO	**LPE_SC_IPC_Request_Status:** IPCLPESC Interrupt Request 1: interrupt when LPE writes a message into IPCLPESC register with bit 63 set 0: Deasserted
0	0x0 RW/1C	**LPE_SC_IPC_Done_Status:** IPCSC Interrupt Request 1: interrupt when LPE writes a message into IPCSC register with bit 62 set is asserted 0: Deasserted.

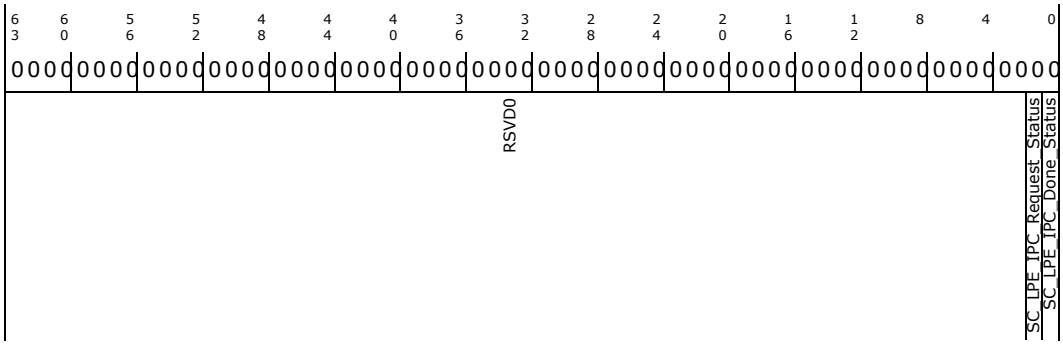
8.12.11 reg_ISRLPESC_type (ISRLPESC)—Offset 50h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 50h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:2	0x0 RO	**RSVD0:** Reserved
1	0x0 RO	**SC_LPE_IPC_Request_Status:** IPCSC Interrupt Request to LPE 1: interrupt when SC writes a message into IPCSC register with bit 63 set. 0: Deasserted
0	0x0 RO	**SC_LPE_IPC_Done_Status:** IPCLPESC Interrupt Request to LPE 1: interrupt when SC CPU writes a message into IPCLPEIA register with bit 62 set is asserted 0: Deasserted.

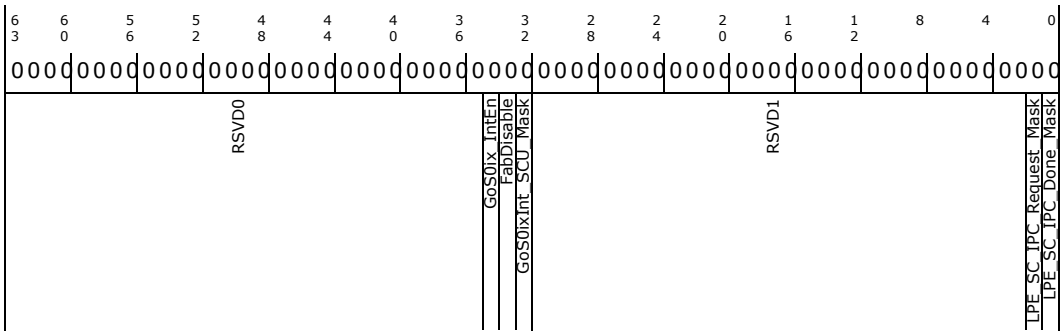
8.12.12 reg_IMRSC_type (IMRSC)—Offset 58h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 58h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:35	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
34	0x0 RW/1C	**GoS0ix_IntEn:** This bit indicates that Reentry to S0iX interrupts to SCU are enabled. The bit is set by hardware when a transaction is blocked at the Audio to Secondary interface due to the secondary fabric being gated and the fabdisable bit being set. Software is expected to clear this bit along with the Secondary Fabric Reject bit. This disables the interrupts.
33	0x0 RW	**FabDisable:** This bit is used to generate the wake interrupt to SCU. When set the interrupt generation is enabled. When cleared the interrupt generation is disabled
32	0x0 RW	**GoS0ixInt_SCU_Mask:** Mask bit for S0ix Reentry interrupt to SCU
31:2	0x0 RO	**RSVD1:** Reserved
1	0x0 RW	**LPE_SC_IPC_Request_Mask:** IPCLPESC Interrupt Enable to SC CPU
0	0x0 RW	**LPE_SC_IPC_Done_Mask:** IPCSC Interrupt Enable to SC CPU

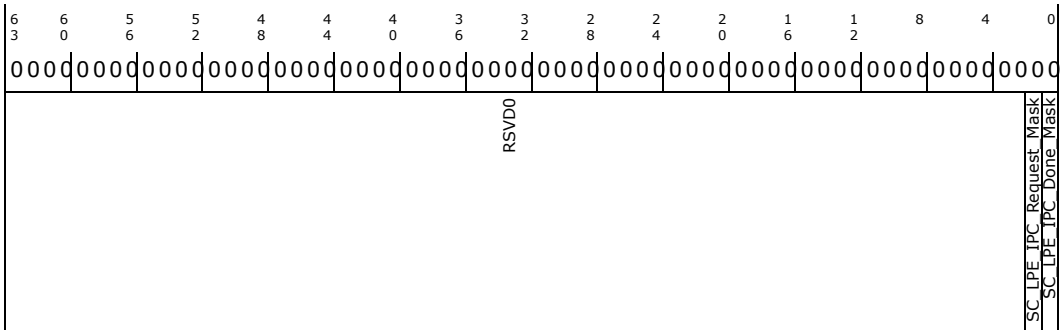
8.12.13 reg_IMRLPESC_type (IMRLPESC)—Offset 60h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 60h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:2	0x0 RO	**RSVD0:** Reserved
1	0x0 RW	**SC_LPE_IPC_Request_Mask:** IPCSC interrupt Enable to LPE
0	0x0 RW	**SC_LPE_IPC_Done_Mask:** IPCLPESC interrupt Enable to LPE

8.12.14 reg_IPCSC_type (IPCSC)—Offset 68h

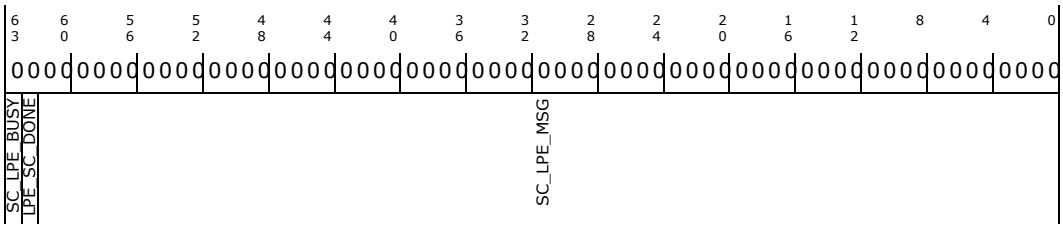
The Inter-process Status and Message register for SC contains a message sent from the SC CPU to LPE. The format of the CPU message bits (29:0) is not defined in the HW specs. It is defined in the LPE Firmware specifications. The message may contain optional data fields stored in the shared memory region (mailbox). When the message is written in this register, the software must set bit 63 to indicate that the IPCSC is not empty. Setting Busy also asserts interrupt request to LPE if the interrupt is enabled in the IMRLPESC. After LPE reads the message code from the register, it must perform a write with bit 63 cleared. The SC CPU must not attempt to write into IPCIA if bit 63 is set.

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 68h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63	0x0 RW	**SC_LPE_BUSY:** Busy. When this bit is cleared, the LPE Ready to accept a message
62	0x0 RW	**LPE_SC_DONE:** Done. When the bit is set, the LPE completed the operation and requests attention
61:0	0x0 RW	**SC_LPE_MSG:** SC to LPE Message

8.12.15 reg_IPCLPESC_type (IPCLPESC)—Offset 70h

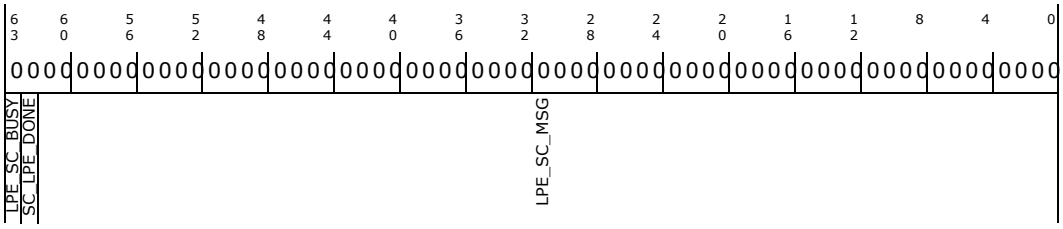
Inter-process Status and Message register for LPE contains a message sent from LPE to SC. The format of the CPU message bits 29:0 is defined in the LPE Firmware specifications. The message may contain optional data fields stored in the shared memory region (mailbox). When software writes the message is in this register, it should set bit 63 to indicate that the new data is written. When SC reads the message code from the register, and writes back with the bit 63 cleared. When the SC CPU processes the message sent by LPE, it may set bit 62 in IPCLPESC to assert interrupt request to LPE. The LPE must not attempt to write into IPCD if bit 63 is set.

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 70h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63	0x0 RW	**LPE_SC_BUSY:** Busy. When this bit is cleared, the SC CPU is Ready to accept a new message
62	0x0 RW	**SC_LPE_DONE:** Done. When the bit is set, the SC CPU completed operation and requests attention from LPE
61:0	0x0 RW	**LPE_SC_MSG:** LPE to SC CPU Message

8.12.16 reg_CLKCTL_type (CLKCTL)—Offset 78h

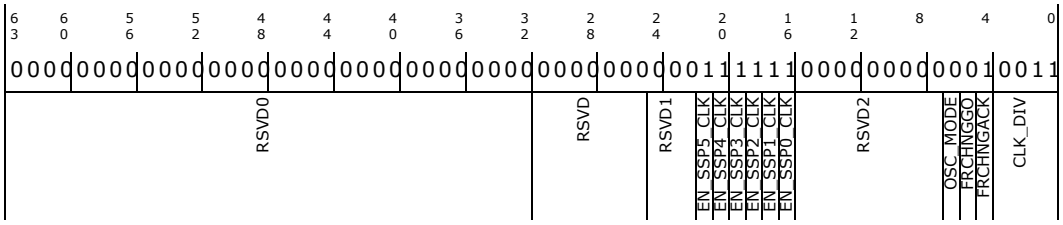
LPE Clock Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 78h

Default: 00000000003F0013h



Bit Range	Default & Access	Field Name (ID): Description
63:32	0x0 RO	**RSVD0:** Reserved
31:25	0x0 RO	**RSVD:** Reserved.
24:22	0x0 RO	**RSVD1:** Reserved
21	0x1 RW	**EN_SSP5_CLK:** clock output enable
20	0x1 RW	**EN_SSP4_CLK:** clock output enable
19	0x1 RW	**EN_SSP3_CLK:** clock output enable

Bit Range	Default & Access	Field Name (ID): Description
18	0x1 RW	**EN_SSP2_CLK:** clock output enable
17	0x1 RW	**EN_SSP1_CLK:** clock output enable
16	0x1 RW	**EN_SSP0_CLK:** clock output enable
15:7	0x0 RO	**RSVD2:** Reserved
6	0x0 RO	**OSC_MODE:** 1 indicates that PLL is turned off
5	0x0 RW/1S	**FRCHNGGO:** Go bit indicating that the value in 2:0 can be applied to core. This bit will get cleared on the rising edge of the ack from Clock Control Unit.
4	0x1 RO	**FRCHNGACK:** Sets on the falling edge of ack. A 1'b1 indicates that the frequency change is done. The bit auto clears on the rising edge of frequency change request.
3:0	0x3 RW	**CLK_DIV:** 0000: 19.2 MHz 0001: 19.2 Mhz 0010: 38.4 Mhz 0011: 50 Mhz 0100: 100 Mhz 0101: 200 Mhz 0110: 250 Mhz 0111: 333 Mhz 1000: 50 Mhz (SUS-RO) 1001: 100 Mhz (SUS-RO) 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved

8.12.17 reg_FR_LAT_REQ_type (FR_LAT_REQ)—Offset 80h

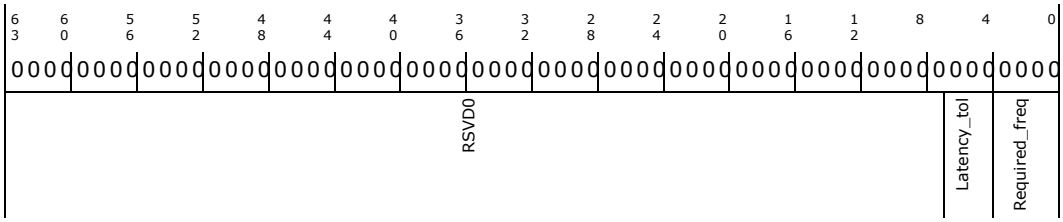
LPE

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 80h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:7	0x0 RO	**RSVD0:** Reserved
6:4	0x0 RW	**Latency_tol:** Latency tolerance for Cache Misses is listed here. SCU firmware is required to read this register and make a decision on whether it can enter a lower power state and still meet the latency tolerance.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x0 RW	**Required_freq:** The following encoding specifies the frequency that the Audio Cluster requires for current operations. 0000: 19.2 MHz 0001: 19.2 Mhz 0010: 38.4 Mhz 0011: 50 Mhz 0100: 100 Mhz 0101: 200 Mhz 0110: 250 Mhz 0111: 333 Mhz 1000: 50 Mhz (SUS-RO) 1001: 100 Mhz (SUS-RO) 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved Please note, that this does not guarantee that this frequency will be generated from the CCU. The SCU firmware is required to read this register before making a decision on entering lower power states.

8.12.18 reg_CHICKEN_BITS_type (CHICKEN_BITS)—Offset 88h

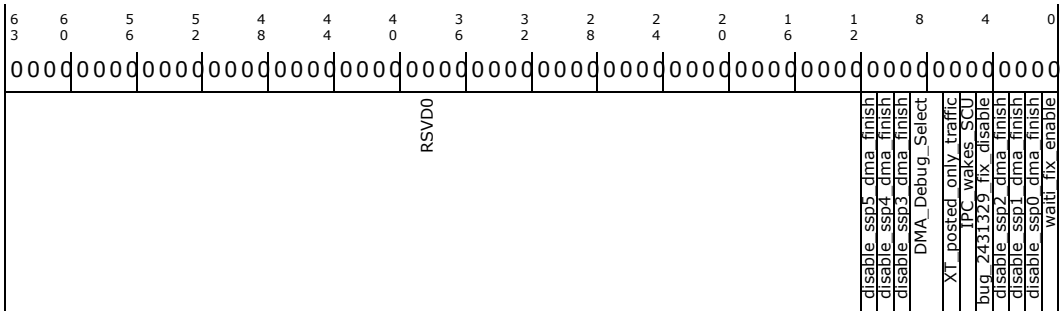
LPE

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 88h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:12	0x0 RO	**RSVD0:** Reserved
11	0x0 RW	**disable_ssp5_dma_finish:** Setting this to 1 will cause the SSP Unit to ignore the dma_finish signal. Set this to 1 for MultiBlock transfers.
10	0x0 RW	**disable_ssp4_dma_finish:** Setting this to 1 will cause the SSP Unit to ignore the dma_finish signal. Set this to 1 for MultiBlock transfers.
9	0x0 RW	**disable_ssp3_dma_finish:** Setting this to 1 will cause the SSP Unit to ignore the dma_finish signal. Set this to 1 for MultiBlock transfers.
8:7	0x0 RW	**DMA_Debug_Select:** Setting this bit will select DMA 1 debug signals to be routed to the VISA Mux.
6	0x0 RW	**XT_posted_only_traffic:** Setting this bit will select make all the traffic from Tensilica to be posted.
5	0x0 RW	**IPC_wakes_SCU:** Setting this to 1 will cause the IPC to be fed into the wake cone for SCU.

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**bug_2431329_fix_disable:** Setting this to 1 will disable the synopsys compatible hardware handshake mechanism. Keep this set to 0 for regular hardware handshake operation.
3	0x0 RW	**disable_ssp2_dma_finish:** Setting this to 1 will cause the SSP Unit to ignore the dma_finish signal. Set this to 1 for MultiBlock transfers.
2	0x0 RW	**disable_ssp1_dma_finish:** Setting this to 1 will cause the SSP Unit to ignore the dma_finish signal. Set this to 1 for MultiBlock transfers.
1	0x0 RW	**disable_ssp0_dma_finish:** Setting this to 1 will cause the SSP Unit to ignore the dma_finish signal. Set this to 1 for MultiBlock transfers.
0	0x0 RW	**waiti_fix_enable:** Setting this bit to 1 makes the frequency change request to be valid only if the core is in WAITI.

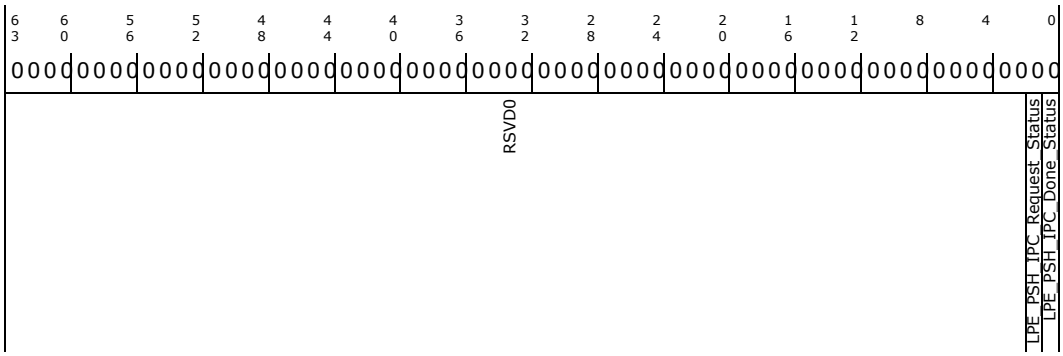
8.12.19 reg_ISRPSH_type (ISRPSH)—Offset 90h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 90h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:2	0x0 RO	**RSVD0:** Reserved
1	0x0 RO	**LPE_PSH_IPC_Request_Status:** IPCLPEPSH Interrupt Request 1: interrupt when LPE writes a message into IPCLPEPSH register with bit 63 set 0: Deasserted
0	0x0 RW/1C	**LPE_PSH_IPC_Done_Status:** IPCPSH Interrupt Request 1: interrupt when LPE writes a message into IPCPSH register with bit 62 set is asserted 0: Deasserted.

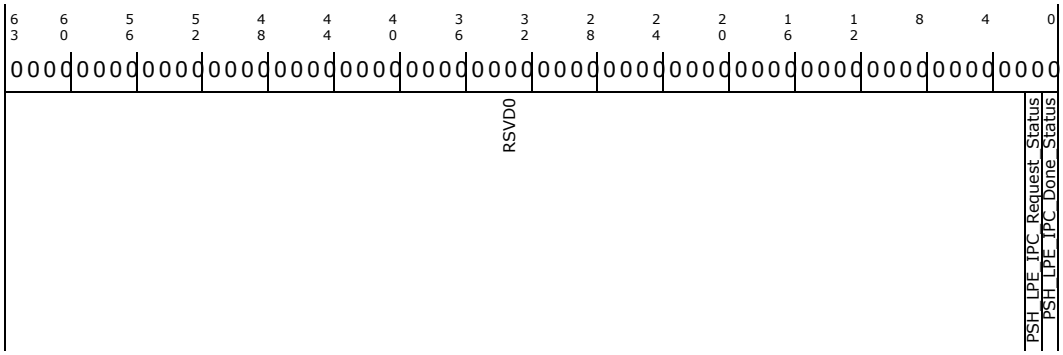
8.12.20 reg_ISRLPEPSH_type (ISRLPEPSH)—Offset 98h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 98h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:2	0x0 RO	**RSVD0:** Reserved
1	0x0 RO	**PSH_LPE_IPC_Request_Status:** IPCPSH Interrupt Request to LPE 1: interrupt when PSH writes a message into IPCPSH register with bit 63 set. 0: Deasserted
0	0x0 RO	**PSH_LPE_IPC_Done_Status:** IPCLPEPSH Interrupt Request to LPE 1: interrupt when PSH CPU writes a message into IPCLPEIA register with bit 62 set is asserted 0: Deasserted.

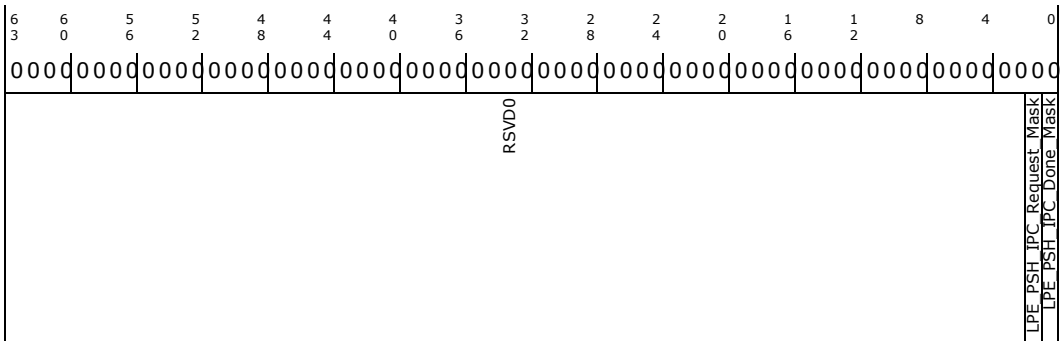
8.12.21 reg_IMRPSH_type (IMRPSH)—Offset A0h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + A0h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:2	0x0 RO	**RSVD0:** Reserved
1	0x0 RW	**LPE_PSH_IPC_Request_Mask:** IPCLPEPSH Interrupt Enable to PSH CPU
0	0x0 RW	**LPE_PSH_IPC_Done_Mask:** IPCPSH Interrupt Enable to PSH CPU

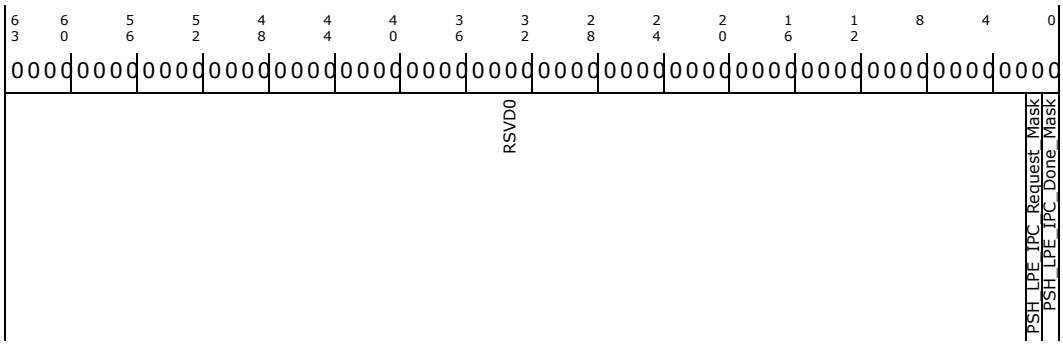
8.12.22 reg_IMRLPEPSH_type (IMRLPEPSH)—Offset A8h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + A8h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:2	0x0 RO	**RSVD0:** Reserved
1	0x0 RW	**PSH_LPE_IPC_Request_Mask:** IPCPSH interrupt Enable to LPE
0	0x0 RW	**PSH_LPE_IPC_Done_Mask:** IPCLPEPSH interrupt Enable to LPE

8.12.23 reg_IPCPSH_type (IPCPSH)—Offset B0h

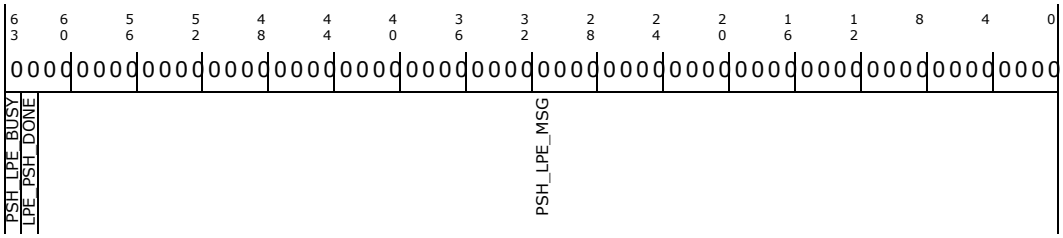
The Inter-process Status and Message register for PSH contains a message sent from the PSH CPU to LPE. The format of the CPU message bits (29:0) is not defined in the HW specs. It is defined in the LPE Firmware specifications. The message may contain optional data fields stored in the shared memory region (mailbox). When the message is written in this register, the software must set bit 63 to indicate that the IPCPSH is not empty. Setting Busy also asserts interrupt request to LPE if the interrupt is enabled in the IMRLPEPSH. After LPE reads the message code from the register, it must perform a write with bit 63 cleared. The PSH CPU must not attempt to write into IPCIA if bit 63 is set.

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + B0h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63	0x0 RW	**PSH_LPE_BUSY:** Busy. When this bit is cleared, the LPE Ready to accept a message
62	0x0 RW	**LPE_PSH_DONE:** Done. When the bit is set, the LPE completed the operation and requests attention
61:0	0x0 RW	**PSH_LPE_MSG:** PSH to LPE Message

8.12.24 reg_IPCLPEPSH_type (IPCLPEPSH)—Offset B8h

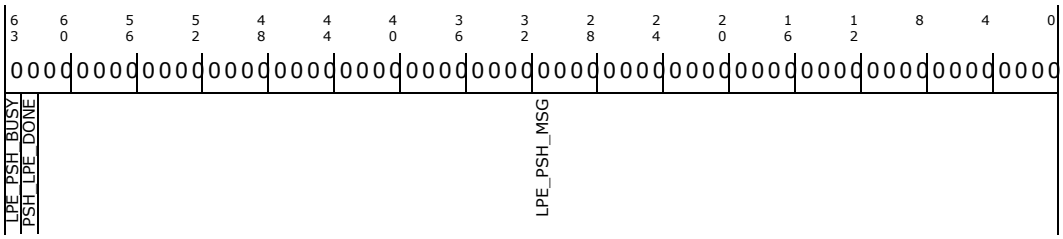
Inter-process Status and Message register for LPE contains a message sent from LPE to PSH. The format of the CPU message bits 29:0 is defined in the LPE Firmware specifications. The message may contain optional data fields stored in the shared memory region (mailbox). When software writes the message is in this register, it should set bit 63 to indicate that the new data is written. When PSH reads the message code from the register, and writes back with the bit 63 cleared. When the PSH CPU processes the message sent by LPE, it may set bit 62 in IPCLPEPSH to assert interrupt request to LPE. The LPE must not attempt to write into IPCD if bit 63 is set.

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + B8h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63	0x0 RW	**LPE_PSH_BUSY:** Busy. When this bit is cleared, the PSH CPU is Ready to accept a new message
62	0x0 RW	**PSH_LPE_DONE:** Done. When the bit is set, the PSH CPU completed operation and requests attention from LPE
61:0	0x0 RW	**LPE_PSH_MSG:** LPE to PSH CPU Message

8.12.25 reg_EXT_TIMER_CNTL_type (EXT_TIMER_CNTL)—Offset C0h

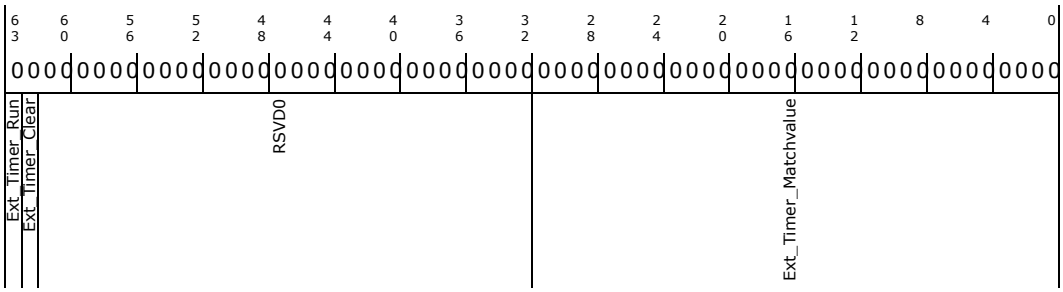
External Timer Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + C0h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63	0x0 RW	**Ext_Timer_Run:** Timer Run bit. The timer runs only when this bit is set. It resumes running from the current value in the readvalue bits. Clearing the bit pauses the timer.
62	0x0 RW/S	**Ext_Timer_Clear:** Timer Clear bit. Clears the timer and sets the value back to zero. This should also be reflected in the readvalue bits
61:32	0x0 RO	**RSVD0:** Reserved
31:0	0x0 RW	**Ext_Timer_Matchvalue:** The timer will generate a pulse when the Readvalue reaches Matchvalue. The pulse causes a level interrupt to get set in the PISR register. The PISR interrupt needs to be cleared before the next pulse is generated. The timer keeps counting beyond the Readvalue. Setting the Matchvalue to zero makes this a free running timer and no interrupt will be generated in this case. For correct operation, the ISR should either set a new Matchvalue or set it to zero. If nothing is done, the timer will roll over and trigger an interrupt again when it reaches the Matchvalue.

8.12.26 reg_EXT_TIMER_STAT_type (EXT_TIMER_STAT)—Offset C8h

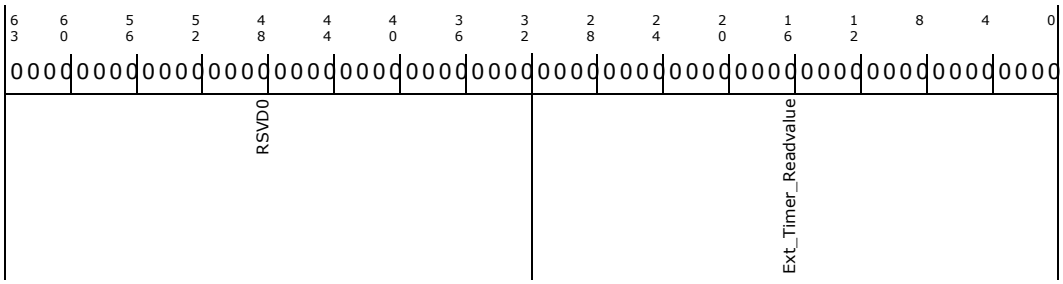
External Timer Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + C8h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:32	0x0 RO	**RSVD0:** Reserved
31:0	0x0 RO	**Ext_Timer_Readvalue:** Shows the current count value of the timer

8.12.27 reg_S0ix_TIMER_CNTL_type (S0ix_TIMER_CNTL)—Offset D0h

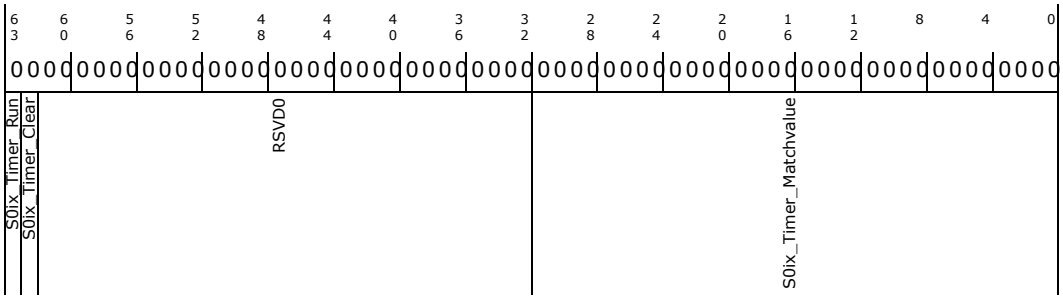
External Timer Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + D0h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63	0x0 RW	**S0ix_Timer_Run:** Timer Run bit. The timer runs only when this bit is set. It resumes running from the current value in the readvalue bits. Clearing the bit pauses the timer.
62	0x0 RW/S	**S0ix_Timer_Clear:** Timer Clear bit. Clears the timer and sets the value back to zero. This should also be reflected in the readvalue bits
61:32	0x0 RO	**RSVD0:** Reserved
31:0	0x0 RW	**S0ix_Timer_Matchvalue:** The timer will generate a pulse when the Readvalue reaches Matchvalue. The pulse causes a level interrupt to get set in the PISR register. The PISR interrupt needs to be cleared before the next pulse is generated. The timer keeps counting beyond the Readvalue. Setting the Matchvalue to zero makes this a free running timer and no interrupt will be generated in this case. For correct operation, the ISR should either set a new Matchvalue or set it to zero. If nothing is done, the timer will roll over and trigger an interrupt again when it reaches the Matchvalue.

8.12.28 reg_S0ix_TIMER_STAT_type (S0ix_TIMER_STAT)—Offset D8h

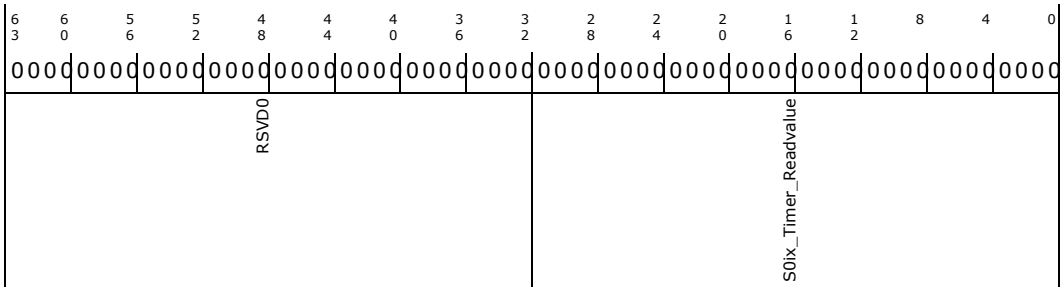
External Timer Control Register

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + D8h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:32	0x0 RO	**RSVD0:** Reserved
31:0	0x0 RO	**S0ix_Timer_Readvalue:** Shows the current count value of the timer

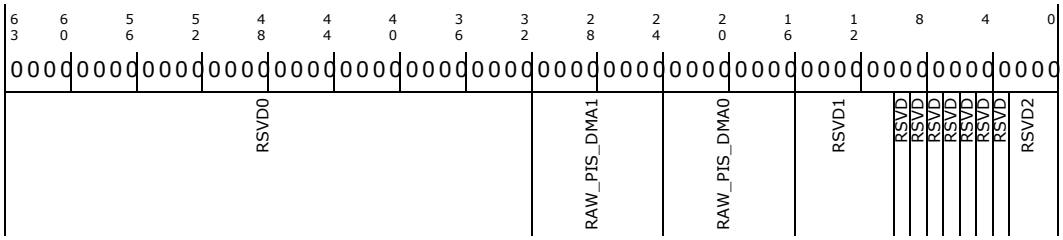
8.12.29 reg_RAW_PISR_type (XT_RAW_PISR)—Offset E0h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + E0h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:32	0x0 RO	**RSVD0:** Reserved
31:24	0x0 RO	**RAW_PIS_DMA1:** DMA 1 interrupts
23:16	0x0 RO	**RAW_PIS_DMA0:** DMA 0 interrupts
15:10	0x0 RO	**RSVD1:** Reserved
9	0x0 RO	**Reserved (RSVD):** Reserved.
8	0x0 RO	**Reserved (RSVD):** Reserved.
7	0x0 RO	**Reserved (RSVD):** Reserved.
6	0x0 RO	**Reserved (RSVD):** Reserved.
5	0x0 RO	**Reserved (RSVD):** Reserved.
4	0x0 RO	**Reserved (RSVD):** Reserved.
3	0x0 RO	**Reserved (RSVD):** Reserved.
2:0	0x0 RO	**RSVD2:** Reserved

8.12.30 reg_SSP0_DIV_CTRL_type (SSP0_DIV_CTRL)—Offset E8h

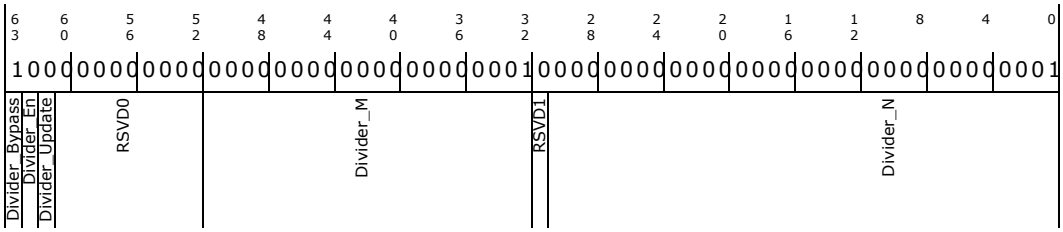
SSP0 M/N Clock Divider control

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + E8h

Default: 8000000100000001h



Bit Range	Default & Access	Field Name (ID): Description
63	0x1 RW	**Divider_Bypass:** SSP0 Bypass divider
62	0x0 RW	**Divider_En:** SSP0 Enable divider
61	0x0 RW	**Divider_Update:** SSP0 Update divider
60:52	0x0 RO	**RSVD0:** Reserved
51:32	0x1 RW	**Divider_M:** SSP0 Nominator value
31:20	0x0 RO	**RSVD1:** Reserved
19:0	0x1 RW	**Divider_N:** SSP0 Denominator value

8.12.31 reg_SSP1_DIV_CTRL_type (SSP1_DIV_CTRL)—Offset F0h

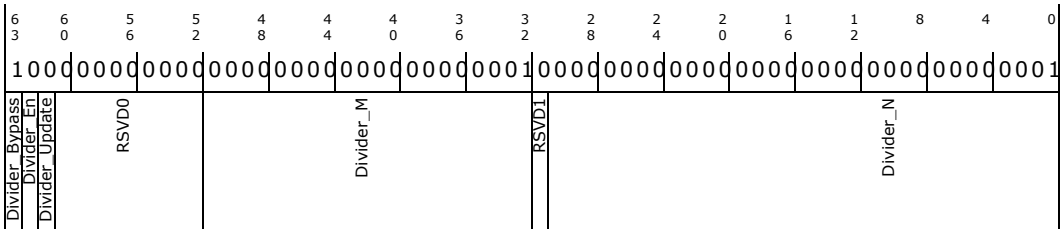
SSP1 M/N Clock Divider control

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + F0h

Default: 8000000100000001h



Bit Range	Default & Access	Field Name (ID): Description
63	0x1 RW	**Divider_Bypass:** SSP1 Bypass divider
62	0x0 RW	**Divider_En:** SSP1 Enable divider
61	0x0 RW	**Divider_Update:** SSP1 Update divider
60:52	0x0 RO	**RSVD0:** Reserved
51:32	0x1 RW	**Divider_M:** SSP1 Nominator value
31:20	0x0 RO	**RSVD1:** Reserved
19:0	0x1 RW	**Divider_N:** SSP1 Denominator value

8.12.32 reg_SSP2_DIV_CTRL_type (SSP2_DIV_CTRL)—Offset F8h

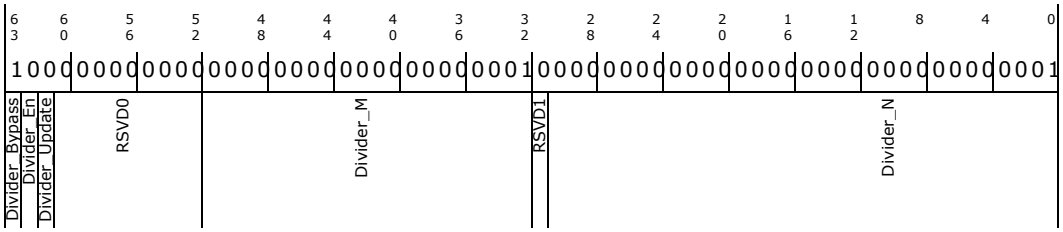
SSP2 M/N Clock Divider control

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + F8h

Default: 8000000100000001h



Bit Range	Default & Access	Field Name (ID): Description
63	0x1 RW	**Divider_Bypass:** SSP2 Bypass divider
62	0x0 RW	**Divider_En:** SSP2 Enable divider
61	0x0 RW	**Divider_Update:** SSP2 Update divider
60:52	0x0 RO	**RSVD0:** Reserved
51:32	0x1 RW	**Divider_M:** SSP2 Nominator value

Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RSVD1:** Reserved
19:0	0x1 RW	**Divider_N:** SSP2 Denominator value

8.12.33 reg_SSP3_DIV_CTRL_type (SSP3_DIV_CTRL)—Offset 100h

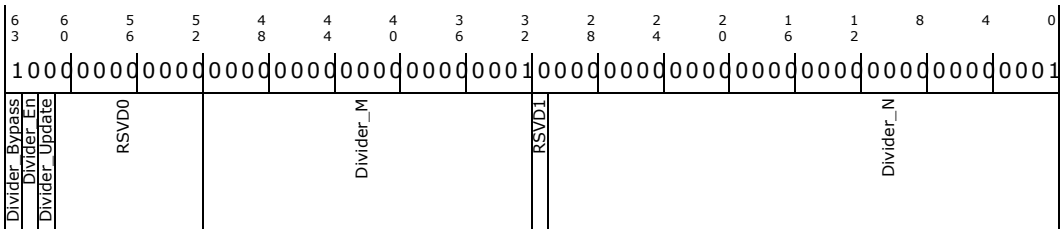
SSP3 M/N Clock Divider control

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [Ipe_bridge.BAR + 140000h] + 100h

Default: 8000000100000001h



Bit Range	Default & Access	Field Name (ID): Description
63	0x1 RW	**Divider_Bypass:** SSP3 Bypass divider
62	0x0 RW	**Divider_En:** SSP3 Enable divider
61	0x0 RW	**Divider_Update:** SSP3 Update divider
60:52	0x0 RO	**RSVD0:** Reserved
51:32	0x1 RW	**Divider_M:** SSP3 Nominator value
31:20	0x0 RO	**RSVD1:** Reserved
19:0	0x1 RW	**Divider_N:** SSP3 Denominator value

8.12.34 reg_SSP4_DIV_CTRL_type (SSP4_DIV_CTRL)—Offset 108h

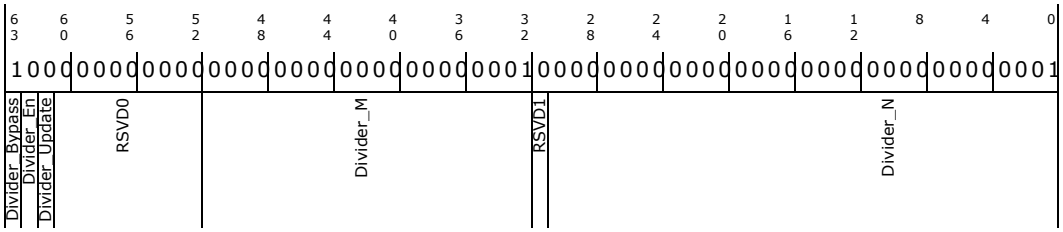
SSP4 M/N Clock Divider control

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 108h

Default: 8000000100000001h



Bit Range	Default & Access	Field Name (ID): Description
63	0x1 RW	**Divider_Bypass:** SSP4 Bypass divider
62	0x0 RW	**Divider_En:** SSP4 Enable divider
61	0x0 RW	**Divider_Update:** SSP4 Update divider
60:52	0x0 RO	**RSVD0:** Reserved
51:32	0x1 RW	**Divider_M:** SSP4 Nominator value
31:20	0x0 RO	**RSVD1:** Reserved
19:0	0x1 RW	**Divider_N:** SSP4 Denominator value

8.12.35 reg_SSP5_DIV_CTRL_type (SSP5_DIV_CTRL)—Offset 110h

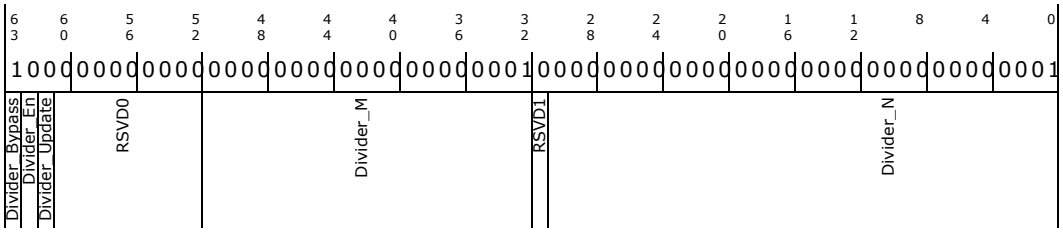
SSP5 M/N Clock Divider control

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: [lpe_bridge.BAR + 140000h] + 110h

Default: 8000000100000001h



Bit Range	Default & Access	Field Name (ID): Description
63	0x1 RW	**Divider_Bypass:** SSP5 Bypass divider
62	0x0 RW	**Divider_En:** SSP5 Enable divider
61	0x0 RW	**Divider_Update:** SSP5 Update divider
60:52	0x0 RO	**RSVD0:** Reserved
51:32	0x1 RW	**Divider_M:** SSP5 Nominator value
31:20	0x0 RO	**RSVD1:** Reserved
19:0	0x1 RW	**Divider_N:** SSP5 Denominator value

9 Serial IO (SIO)

9.1 SIO DMA 1 PCI Configuration Registers for I2C

Table 64. Summary of SIO DMA 1 PCI Configuration Registers—0/30/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 3895	00008086h
4–7h	4	"STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h" on page 3895	00100000h
8–Bh	4	"REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 3897	00000000h
C–Fh	4	"CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 3898	00800000h
10–13h	4	"BAR -Base Address Register (BAR)—Offset 10h" on page 3898	00000000h
14–17h	4	"BAR1 -Base Address Register1 (BAR1)—Offset 14h" on page 3899	00000000h
2C–2Fh	4	"SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 3900	00000000h
30–33h	4	"EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 3901	00000000h
34–37h	4	"CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 3901	00000000h
3C–3Fh	4	"INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 3902	00000100h
80–83h	4	"POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 3902	00030001h
84–87h	4	"PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 3903	00000008h
F8–FBh	4	"Manufacturers ID (MANID)—Offset F8h" on page 3904	00000000h

9.1.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

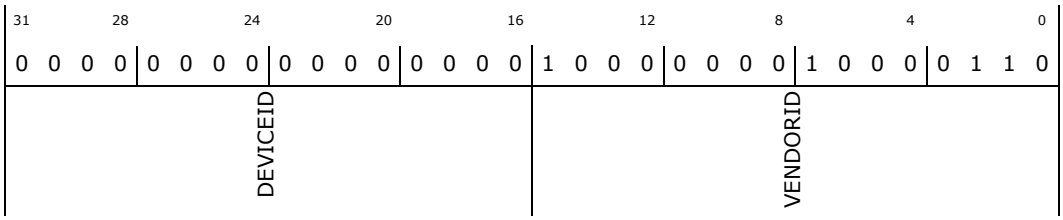
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**DEVICEID:** Device ID identifies the particular AHB/APB device. This is tied to a strap at the top level. Because of tool issues, the HTML files show this field as 0, but the following are the POR values for SoC: LPIO1 DMA: 0x2286 LPIO1 PWM1: 0x2288 LPIO1 PWM2: 0x2289 LPIO1 HSUART1: 0x228A LPIO1 HSUART2: 0x228C LPIO1 SPI1: 0x228E LPIO1 SPI2: 0x2290 LPIO1 SPI3: 0x22AC LPIO2 DMA: 0x22C0 LPIO2 I2C1: 0x22C1 LPIO2 I2C2: 0x22C2 LPIO2 I2C3: 0x22C3 LPIO2 I2C4: 0x22C4 LPIO2 I2C5: 0x22C5 LPIO2 I2C6: 0x22C6 LPIO2 I2C7: 0x22C7 For the final word on this, please see Ray Ng's SoC RevID and DevID HAS on Infofactory: https://ifcollaborate.intel.com/IFC/getdoc.aspx?docbase=InfoFactoryKBandchronid=09005ffd80e84b43andver=CURRENTandqepop=false
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap the top level.

9.1.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

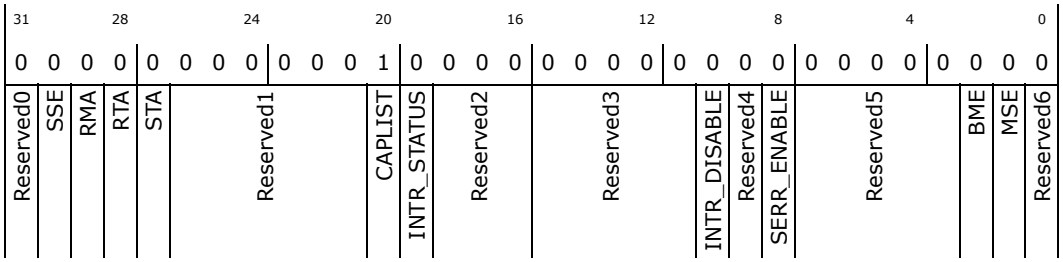
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved0:** Reserved
30	0x0 RW/1C	**SSE:** This bit is set when a device sends an DO_SERR message, and the SERR# Enable bit in the Command register is 1
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric PortReceived Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27	0x0 RW/1C	**STA:** The Bridge sets this bit whenever it responds to a transaction with CA abort. If the SERR# Enable bit is set, the Bridge sets the Signaled System Error bit and sends an DO_SERR message on the IOSF Sideband.
26:21	0x0 RO	**Reserved1:** Reserved
20	0x1 RO	**CAPLIST:** Capabilities List: Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt .i.e Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.. Reset value of this bit is 0.
9	0x0 RO	**Reserved4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: If both SERR# Enable and the Unsupported Request Reporting Enable (URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0x0 RO	**Reserved6:** Reserved

9.1.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

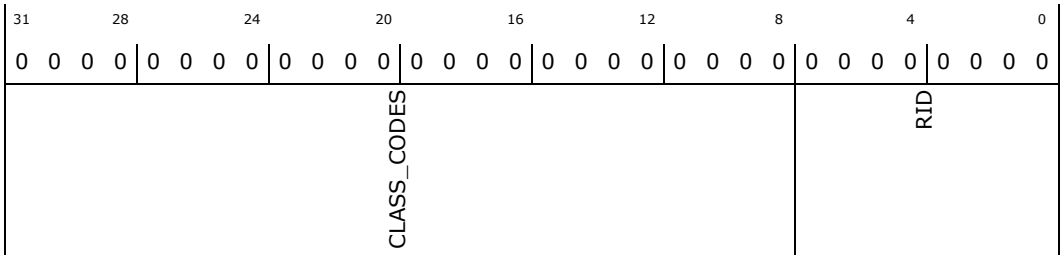
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

9.1.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

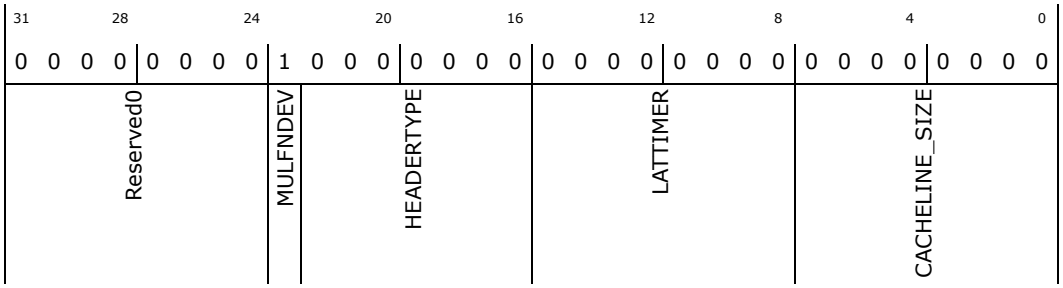
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + Ch

Default: 00800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x1 RO	**MULFNDEV:** Multi Function Device: This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. Value of 1 indicates multifunction device value of 0 indicates single function device
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	0x0 RO	**LATTIMER:** Latency Timer: Doesn.t apply to PCI Express. Hardwired to 00h.
7:0	0x0 RW	**CACHELINE_SIZE:** Cache Line Size: Doesn.t apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

9.1.5 BAR -Base Address Register (BAR)—Offset 10h

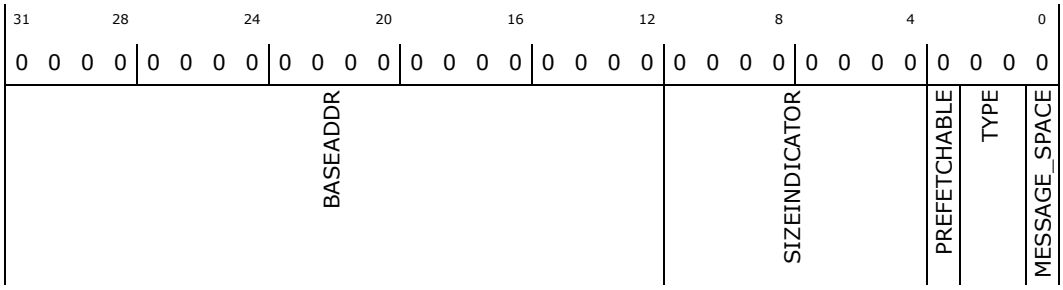
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the AHB device memory space. Taken from Strap values as 1's. Please note that for DMA this field goes from [31:14], or 16kbyte, and the SIZEINDICATOR field goes from [13:4].
11:4	0x0 RO	**SIZEINDICATOR:** Size Indicator Read Only: Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0x0 RO	**TYPE:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.1.6 BAR1 -Base Address Register1 (BAR1)—Offset 14h

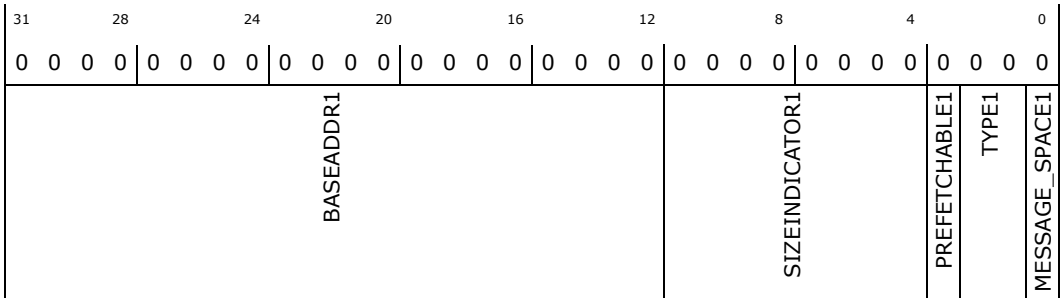
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	0x0 RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not
2:1	0x0 RO	**TYPE1:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.1.7 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

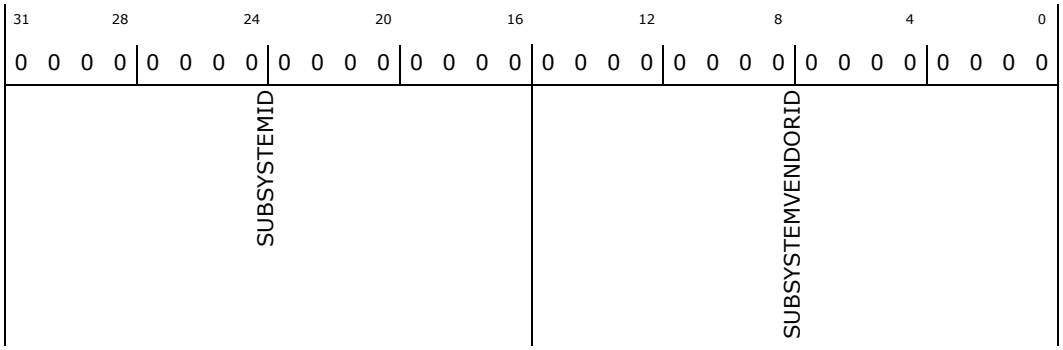
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

9.1.8 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

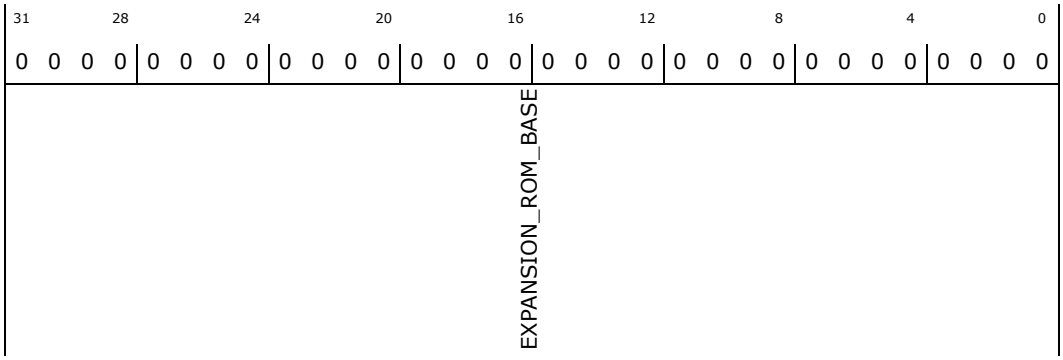
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** A value of all zeros indicates no support for expansion ROM.

9.1.9 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

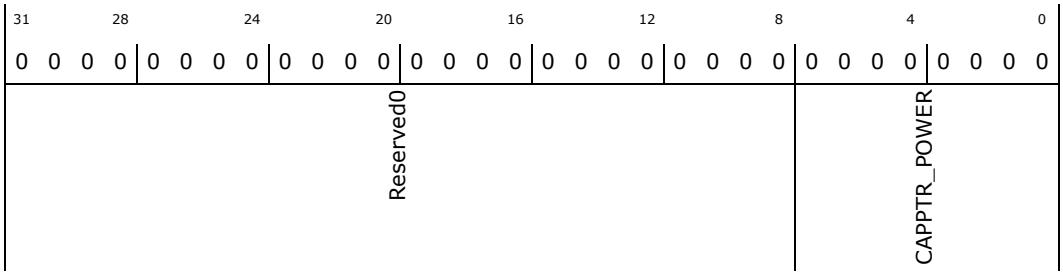
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x0 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

9.1.10 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

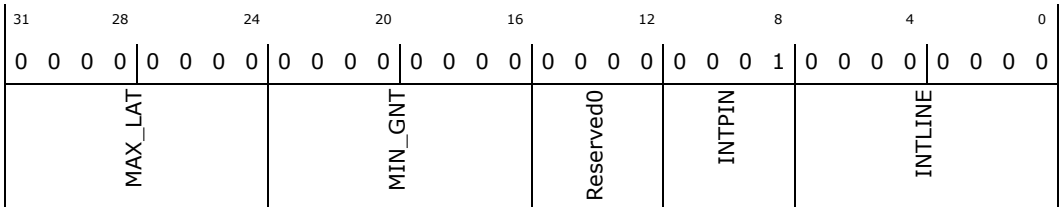
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

9.1.11 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

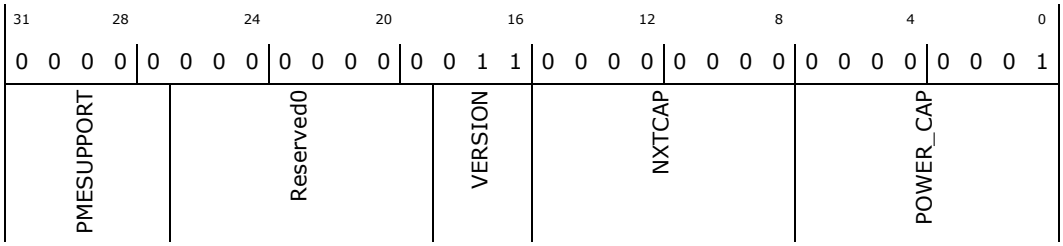
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** PME_Support - This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

9.1.12 PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

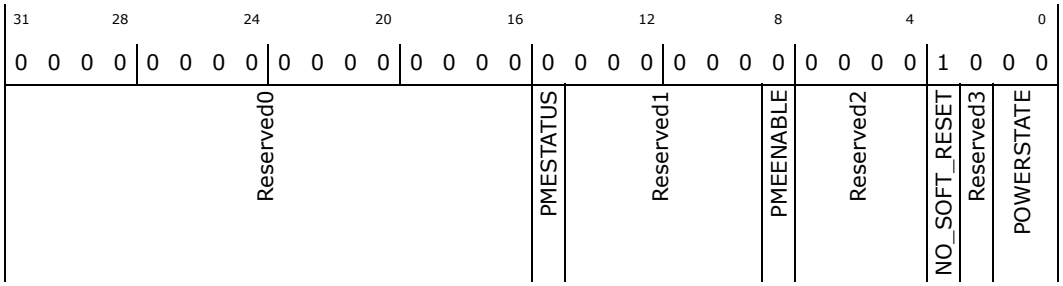
PMECTRLSTATUS - PME Control and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

9.1.13 Manufacturers ID (MANID)—Offset F8h

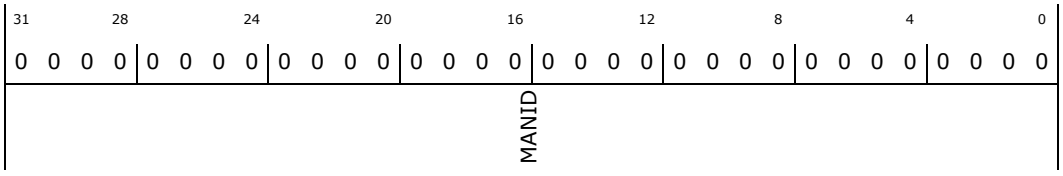
Manufacturers ID

Access Method

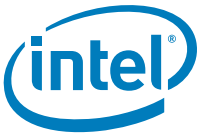
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:0] + F8h

Default: 00000000h



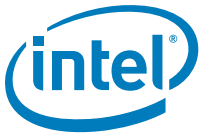
Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: This register is brought out as straps to the top level.



9.2 SIO DMA 1 Memory Mapped I/O Registers for I2C

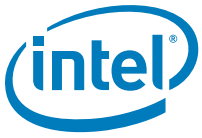
Table 65. Summary of SIO DMA 1 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Source Address Register for Channel 0 - LOW (SAR0_LO)—Offset 0h" on page 3915	00000000h
4–7h	4	"Source Address Register for Channel 0 - HIGH (SAR0_HI)—Offset 4h" on page 3915	00000000h
8–Bh	4	"Destination Address Register for Channel 0 - LOW (DAR0_LO)—Offset 8h" on page 3916	00000000h
C–Fh	4	"Destination Address Register for Channel 0 - HIGH (DAR0_HI)—Offset Ch" on page 3916	00000000h
10–13h	4	"Linked List Pointer Register for Channel 0 - LOW (LLP0_LO)—Offset 10h" on page 3917	00000000h
14–17h	4	"Linked List Pointer Register for Channel 0 - HIGH (LLP0_HI)—Offset 14h" on page 3917	00000000h
18–1Bh	4	"Control Register for Channel 0 - LOW (CTL0_LO)—Offset 18h" on page 3918	00304801h
1C–1Fh	4	"Control Register for Channel 0 - HIGH (CTL0_HI)—Offset 1Ch" on page 3919	00000002h
40–43h	4	"Configuration register for Channel 0 - LOW (CFG0_LO)—Offset 40h" on page 3919	00000E00h
44–47h	4	"Configuration register for Channel 0 - HIGH (CFG0_HI)—Offset 44h" on page 3921	00000004h
48–4Bh	4	"Source Gather Register for Channel 0 - LOW (SGR0_LO)—Offset 48h" on page 3922	00000000h
4C–4Fh	4	"Source Gather Register for Channel 0 - HIGH (SGR0_HI)—Offset 4Ch" on page 3922	00000000h
50–53h	4	"Destination Scatter Register for Channel 0 - LOW (DSR0_LO)—Offset 50h" on page 3923	00000000h
54–57h	4	"Dest scatter Register for Channel 0 - HIGH (DSR0_HI)—Offset 54h" on page 3923	00000000h
58–5Bh	4	"Source Address Register for Channel 1 - LOW (SAR1_LO)—Offset 58h" on page 3924	00000000h
5C–5Fh	4	"Source Address Register for Channel 1 - HIGH (SAR1_HI)—Offset 5Ch" on page 3924	00000000h
60–63h	4	"Destination Address Register for Channel 1 - LOW (DAR1_LO)—Offset 60h" on page 3925	00000000h
64–67h	4	"Destination Address Register for Channel 1 - HIGH (DAR1_HI)—Offset 64h" on page 3925	00000000h
68–6Bh	4	"Linked List Pointer Register for Channel 1 - LOW (LLP1_LO)—Offset 68h" on page 3926	00000000h
6C–6Fh	4	"Linked List Pointer Register for Channel 1 - HIGH (LLP1_HI)—Offset 6Ch" on page 3926	00000000h

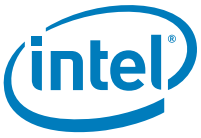


Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
70–73h	4	"Control Register for Channel 1 - LOW (CTL1_LO)—Offset 70h" on page 3927	00304801h
74–77h	4	"Control Register for Channel 1 - HIGH (CTL1_HI)—Offset 74h" on page 3928	00000002h
98–9Bh	4	"Configuration register for Channel 1 - LOW (CFG1_LO)—Offset 98h" on page 3929	00000E20h
9C–9Fh	4	"Configuration register for Channel 1 - HIGH (CFG1_HI)—Offset 9Ch" on page 3930	00000004h
A0–A3h	4	"Source Gather Register for Channel 1 - LOW (SGR1_LO)—Offset A0h" on page 3931	00000000h
A4–A7h	4	"Source Gather Register for Channel 1 - HIGH (SGR1_HI)—Offset A4h" on page 3932	00000000h
A8–ABh	4	"Destination Scatter Register for Channel 1 - LOW (DSR1_LO)—Offset A8h" on page 3932	00000000h
AC–AFh	4	"Dest scatter Register for Channel 1 - HIGH (DSR1_HI)—Offset ACh" on page 3933	00000000h
B0–B3h	4	"Source Address Register for Channel 2 - LOW (SAR2_LO)—Offset B0h" on page 3933	00000000h
B4–B7h	4	"Source Address Register for Channel 2 - HIGH (SAR2_HI)—Offset B4h" on page 3934	00000000h
B8–BBh	4	"Destination Address Register for Channel 2 - LOW (DAR2_LO)—Offset B8h" on page 3934	00000000h
BC–BFh	4	"Destination Address Register for Channel 2 - HIGH (DAR2_HI)—Offset BCh" on page 3935	00000000h
C0–C3h	4	"Linked List Pointer Register for Channel 2 - LOW (LLP2_LO)—Offset C0h" on page 3935	00000000h
C4–C7h	4	"Linked List Pointer Register for Channel 2 - HIGH (LLP2_HI)—Offset C4h" on page 3936	00000000h
C8–CBh	4	"Control Register for Channel 2 - LOW (CTL2_LO)—Offset C8h" on page 3936	00304801h
CC–CFh	4	"Control Register for Channel 2 - HIGH (CTL2_HI)—Offset CCh" on page 3938	00000002h
F0–F3h	4	"Configuration register for Channel 2 - LOW (CFG2_LO)—Offset F0h" on page 3938	00000E40h
F4–F7h	4	"Configuration register for Channel 2 - HIGH (CFG2_HI)—Offset F4h" on page 3939	00000004h
F8–FBh	4	"Source Gather Register for Channel 2 - LOW (SGR2_LO)—Offset F8h" on page 3940	00000000h
FC–FFh	4	"Source Gather Register for Channel 2 - HIGH (SGR2_HI)—Offset FCh" on page 3941	00000000h
100–103h	4	"Destination Scatter Register for Channel 2 - LOW (DSR2_LO)—Offset 100h" on page 3941	00000000h
104–107h	4	"Dest scatter Register for Channel 2 - HIGH (DSR2_HI)—Offset 104h" on page 3942	00000000h

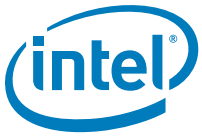
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
108–10Bh	4	"Source Address Register for Channel 3 - LOW (SAR3_LO)—Offset 108h" on page 3942	00000000h
10C–10Fh	4	"Source Address Register for Channel 3 - HIGH (SAR3_HI)—Offset 10Ch" on page 3943	00000000h
110–113h	4	"Destination Address Register for Channel 3 - LOW (DAR3_LO)—Offset 110h" on page 3943	00000000h
114–117h	4	"Destination Address Register for Channel 3 - HIGH (DAR3_HI)—Offset 114h" on page 3944	00000000h
118–11Bh	4	"Linked List Pointer Register for Channel 3 - LOW (LLP3_LO)—Offset 118h" on page 3944	00000000h
11C–11Fh	4	"Linked List Pointer Register for Channel 3 - HIGH (LLP3_HI)—Offset 11Ch" on page 3945	00000000h
120–123h	4	"Control Register for Channel 3 - LOW (CTL3_LO)—Offset 120h" on page 3945	00304801h
124–127h	4	"Control Register for Channel 3 - HIGH (CTL3_HI)—Offset 124h" on page 3947	00000002h
148–14Bh	4	"Configuration register for Channel 3 - LOW (CFG3_LO)—Offset 148h" on page 3947	00000E60h
14C–14Fh	4	"Configuration register for Channel 3 - HIGH (CFG3_HI)—Offset 14Ch" on page 3949	00000004h
150–153h	4	"Source Gather Register for Channel 3 - LOW (SGR3_LO)—Offset 150h" on page 3950	00000000h
154–157h	4	"Source Gather Register for Channel 3 - HIGH (SGR3_HI)—Offset 154h" on page 3950	00000000h
158–15Bh	4	"Destination Scatter Register for Channel 3 - LOW (DSR3_LO)—Offset 158h" on page 3951	00000000h
15C–15Fh	4	"Dest scatter Register for Channel 3 - HIGH (DSR3_HI)—Offset 15Ch" on page 3951	00000000h
160–163h	4	"Source Address Register for Channel 4 - LOW (SAR4_LO)—Offset 160h" on page 3952	00000000h
164–167h	4	"Source Address Register for Channel 4 - HIGH (SAR4_HI)—Offset 164h" on page 3952	00000000h
168–16Bh	4	"Destination Address Register for Channel 4 - LOW (DAR4_LO)—Offset 168h" on page 3953	00000000h
16C–16Fh	4	"Destination Address Register for Channel 4 - HIGH (DAR4_HI)—Offset 16Ch" on page 3953	00000000h
170–173h	4	"Linked List Pointer Register for Channel 4 - LOW (LLP4_LO)—Offset 170h" on page 3954	00000000h
174–177h	4	"Linked List Pointer Register for Channel 4 - HIGH (LLP4_HI)—Offset 174h" on page 3954	00000000h
178–17Bh	4	"Control Register for Channel 4 - LOW (CTL4_LO)—Offset 178h" on page 3955	00304801h
17C–17Fh	4	"Control Register for Channel 4 - HIGH (CTL4_HI)—Offset 17Ch" on page 3956	00000002h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1A0–1A3h	4	"Configuration register for Channel 4 - LOW (CFG4_LO)—Offset 1A0h" on page 3957	00000E80h
1A4–1A7h	4	"Configuration register for Channel 4 - HIGH (CFG4_HI)—Offset 1A4h" on page 3958	00000004h
1A8–1ABh	4	"Source Gather Register for Channel 4 - LOW (SGR4_LO)—Offset 1A8h" on page 3959	00000000h
1AC–1AFh	4	"Source Gather Register for Channel 4 - HIGH (SGR4_HI)—Offset 1ACh" on page 3960	00000000h
1B0–1B3h	4	"Destination Scatter Register for Channel 4 - LOW (DSR4_LO)—Offset 1B0h" on page 3960	00000000h
1B4–1B7h	4	"Dest scatter Register for Channel 4 - HIGH (DSR4_HI)—Offset 1B4h" on page 3961	00000000h
1B8–1BBh	4	"Source Address Register for Channel 5 - LOW (SAR5_LO)—Offset 1B8h" on page 3961	00000000h
1BC–1BFh	4	"Source Address Register for Channel 5 - HIGH (SAR5_HI)—Offset 1BCh" on page 3962	00000000h
1C0–1C3h	4	"Destination Address Register for Channel 5 - LOW (DAR5_LO)—Offset 1C0h" on page 3962	00000000h
1C4–1C7h	4	"Destination Address Register for Channel 5 - HIGH (DAR5_HI)—Offset 1C4h" on page 3963	00000000h
1C8–1CBh	4	"Linked List Pointer Register for Channel 5 - LOW (LLP5_LO)—Offset 1C8h" on page 3963	00000000h
1CC–1CFh	4	"Linked List Pointer Register for Channel 5 - HIGH (LLP5_HI)—Offset 1CCh" on page 3964	00000000h
1D0–1D3h	4	"Control Register for Channel 5 - LOW (CTL5_LO)—Offset 1D0h" on page 3964	00304801h
1D4–1D7h	4	"Control Register for Channel 5 - HIGH (CTL5_HI)—Offset 1D4h" on page 3966	00000002h
1F8–1FBh	4	"Configuration register for Channel 5 - LOW (CFG5_LO)—Offset 1F8h" on page 3966	00000EA0h
1FC–1FFh	4	"Configuration register for Channel 5 - HIGH (CFG5_HI)—Offset 1FCh" on page 3967	00000004h
200–203h	4	"Source Gather Register for Channel 5 - LOW (SGR5_LO)—Offset 200h" on page 3968	00000000h
204–207h	4	"Source Gather Register for Channel 5 - HIGH (SGR5_HI)—Offset 204h" on page 3969	00000000h
208–20Bh	4	"Destination Scatter Register for Channel 5 - LOW (DSR5_LO)—Offset 208h" on page 3969	00000000h
20C–20Fh	4	"Dest scatter Register for Channel 5 - HIGH (DSR5_HI)—Offset 20Ch" on page 3970	00000000h
210–213h	4	"Source Address Register for Channel 6 - LOW (SAR6_LO)—Offset 210h" on page 3970	00000000h
214–217h	4	"Source Address Register for Channel 6 - HIGH (SAR6_HI)—Offset 214h" on page 3971	00000000h

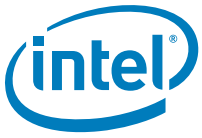


Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
218–21Bh	4	"Destination Address Register for Channel 6 - LOW (DAR6_LO)—Offset 218h" on page 3971	00000000h
21C–21Fh	4	"Destination Address Register for Channel 6 - HIGH (DAR6_HI)—Offset 21Ch" on page 3972	00000000h
220–223h	4	"Linked List Pointer Register for Channel 6 - LOW (LLP6_LO)—Offset 220h" on page 3972	00000000h
224–227h	4	"Linked List Pointer Register for Channel 6 - HIGH (LLP6_HI)—Offset 224h" on page 3973	00000000h
228–22Bh	4	"Control Register for Channel 6 - LOW (CTL6_LO)—Offset 228h" on page 3973	00304801h
22C–22Fh	4	"Control Register for Channel 6 - HIGH (CTL6_HI)—Offset 22Ch" on page 3975	00000002h
250–253h	4	"Configuration register for Channel 6 - LOW (CFG6_LO)—Offset 250h" on page 3975	00000EC0h
254–257h	4	"Configuration register for Channel 6 - HIGH (CFG6_HI)—Offset 254h" on page 3977	00000004h
258–25Bh	4	"Source Gather Register for Channel 6 - LOW (SGR6_LO)—Offset 258h" on page 3978	00000000h
25C–25Fh	4	"Source Gather Register for Channel 6 - HIGH (SGR6_HI)—Offset 25Ch" on page 3978	00000000h
260–263h	4	"Destination Scatter Register for Channel 6 - LOW (DSR6_LO)—Offset 260h" on page 3979	00000000h
264–267h	4	"Dest scatter Register for Channel 6 - HIGH (DSR6_HI)—Offset 264h" on page 3979	00000000h
268–26Bh	4	"Source Address Register for Channel 7 - LOW (SAR7_LO)—Offset 268h" on page 3980	00000000h
26C–26Fh	4	"Source Address Register for Channel 7 - HIGH (SAR7_HI)—Offset 26Ch" on page 3980	00000000h
270–273h	4	"Destination Address Register for Channel 7 - LOW (DAR7_LO)—Offset 270h" on page 3981	00000000h
274–277h	4	"Destination Address Register for Channel 7 - HIGH (DAR7_HI)—Offset 274h" on page 3981	00000000h
278–27Bh	4	"Linked List Pointer Register for Channel 7 - LOW (LLP7_LO)—Offset 278h" on page 3982	00000000h
27C–27Fh	4	"Linked List Pointer Register for Channel 7 - HIGH (LLP7_HI)—Offset 27Ch" on page 3982	00000000h
280–283h	4	"Control Register for Channel 7 - LOW (CTL7_LO)—Offset 280h" on page 3983	00304801h
284–287h	4	"Control Register for Channel 7 - HIGH (CTL7_HI)—Offset 284h" on page 3984	00000002h
2A8–2ABh	4	"Configuration register for Channel 7 - LOW (CFG7_LO)—Offset 2A8h" on page 3985	00000EE0h
2AC–2AFh	4	"Configuration register for Channel 7 - HIGH (CFG7_HI)—Offset 2ACh" on page 3986	00000004h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2B0–2B3h	4	"Source Gather Register for Channel 7 - LOW (SGR7_LO)—Offset 2B0h" on page 3987	00000000h
2B4–2B7h	4	"Source Gather Register for Channel 7 - HIGH (SGR7_HI)—Offset 2B4h" on page 3988	00000000h
2B8–2BBh	4	"Destination Scatter Register for Channel 7 - LOW (DSR7_LO)—Offset 2B8h" on page 3988	00000000h
2BC–2BFh	4	"Dest scatter Register for Channel 7 - HIGH (DSR7_HI)—Offset 2BCh" on page 3989	00000000h
2C0–2C3h	4	"RawTfr Interrupt Raw Status Registers - LOW (RawTfr_LO)—Offset 2C0h" on page 3989	00000000h
2C4–2C7h	4	"RawTfr Interrupt Raw Status Registers - HIGH (RawTfr_HI)—Offset 2C4h" on page 3990	00000000h
2C8–2CBh	4	"RawBlock Interrupt Raw Status Registers - LOW (RawBlock_LO)—Offset 2C8h" on page 3990	00000000h
2CC–2CFh	4	"RawBlock Interrupt Raw Status Registers - HIGH (RawBlock_HI)—Offset 2CCh" on page 3991	00000000h
2D0–2D3h	4	"RawSrcTran Interrupt Raw Status Registers - LOW (RawSrcTran_LO)—Offset 2D0h" on page 3991	00000000h
2D4–2D7h	4	"RawSrcTran Interrupt Raw Status Registers - HIGH (RawSrcTran_HI)—Offset 2D4h" on page 3992	00000000h
2D8–2DBh	4	"RawDstTran Interrupt Raw Status Registers - LOW (RawDstTran_LO)—Offset 2D8h" on page 3992	00000000h
2DC–2DFh	4	"RawDstTran Interrupt Raw Status Registers - HIGH (RawDstTran_HI)—Offset 2DCh" on page 3993	00000000h
2E0–2E3h	4	"RawErr Interrupt Raw Status Registers - LOW (RawErr_LO)—Offset 2E0h" on page 3993	00000000h
2E4–2E7h	4	"RawErr Interrupt Raw Status Registers - HIGH (RawErr_HI)—Offset 2E4h" on page 3994	00000000h
2E8–2EBh	4	"StatusTfr Interrupt Status Registers - LOW (StatusTfr_LO)—Offset 2E8h" on page 3994	00000000h
2EC–2EFh	4	"StatusTfr Interrupt Status Registers - HIGH (StatusTfr_HI)—Offset 2ECh" on page 3995	00000000h
2F0–2F3h	4	"StatusBlock Interrupt Status Registers - LOW (StatusBlock_LO)—Offset 2F0h" on page 3995	00000000h
2F4–2F7h	4	"StatusBlock Interrupt Status Registers - HIGH (StatusBlock_HI)—Offset 2F4h" on page 3996	00000000h
2F8–2FBh	4	"StatusSrcTran Interrupt Status Registers - LOW (StatusSrcTran_LO)—Offset 2F8h" on page 3996	00000000h
2FC–2FFh	4	"StatusSrcTran Interrupt Status Registers - HIGH (StatusSrcTran_HI)—Offset 2FCh" on page 3997	00000000h
300–303h	4	"StatusDstTran Interrupt Status Registers - LOW (StatusDstTran_LO)—Offset 300h" on page 3997	00000000h
304–307h	4	"StatusDstTran Interrupt Status Registers - HIGH (StatusDstTran_HI)—Offset 304h" on page 3998	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
308–30Bh	4	"StatusErr Interrupt Status Registers - LOW (StatusErr_LO)—Offset 308h" on page 3998	00000000h
30C–30Fh	4	"StatusErr Interrupt Status Registers - HIGH (StatusErr_HI)—Offset 30Ch" on page 3999	00000000h
310–313h	4	"MaskTfr Interrupt Mask Registers - LOW (MaskTfr_LO)—Offset 310h" on page 3999	00000000h
314–317h	4	"MaskTfr Interrupt Mask Registers - HIGH (MaskTfr_HI)—Offset 314h" on page 4000	00000000h
318–31Bh	4	"MaskBlock Interrupt Mask Registers - LOW (MaskBlock_LO)—Offset 318h" on page 4001	00000000h
31C–31Fh	4	"MaskBlock Interrupt Mask Registers - HIGH (MaskBlock_HI)—Offset 31Ch" on page 4001	00000000h
320–323h	4	"MaskSrcTran Interrupt Mask Registers - LOW (MaskSrcTran_LO)—Offset 320h" on page 4002	00000000h
324–327h	4	"MaskSrcTran Interrupt Mask Registers - HIGH (MaskSrcTran_HI)—Offset 324h" on page 4002	00000000h
328–32Bh	4	"MaskDstTran Interrupt Mask Registers - LOW (MaskDstTran_LO)—Offset 328h" on page 4003	00000000h
32C–32Fh	4	"MaskDstTran Interrupt Mask Registers - HIGH (MaskDstTran_HI)—Offset 32Ch" on page 4003	00000000h
330–333h	4	"MaskErr Interrupt Mask Registers - LOW (MaskErr_LO)—Offset 330h" on page 4004	00000000h
334–337h	4	"MaskErr Interrupt Mask Registers - HIGH (MaskErr_HI)—Offset 334h" on page 4005	00000000h
338–33Bh	4	"ClearTfr Interrupt Clear Registers - LOW (ClearTfr_LO)—Offset 338h" on page 4005	00000000h
33C–33Fh	4	"ClearTfr Interrupt Clear Registers - HIGH (ClearTfr_HI)—Offset 33Ch" on page 4006	00000000h
340–343h	4	"ClearBlock Interrupt Clear Registers - LOW (ClearBlock_LO)—Offset 340h" on page 4006	00000000h
344–347h	4	"ClearBlock Interrupt Clear Registers - HIGH (ClearBlock_HI)—Offset 344h" on page 4007	00000000h
348–34Bh	4	"ClearSrcTran Interrupt Clear Registers - LOW (ClearSrcTran_LO)—Offset 348h" on page 4007	00000000h
34C–34Fh	4	"ClearSrcTran Interrupt Clear Registers - HIGH (ClearSrcTran_HI)—Offset 34Ch" on page 4008	00000000h
350–353h	4	"ClearDstTran Interrupt Clear Registers - LOW (ClearDstTran_LO)—Offset 350h" on page 4008	00000000h
354–357h	4	"ClearDstTran Interrupt Clear Registers - HIGH (ClearDstTran_HI)—Offset 354h" on page 4009	00000000h
358–35Bh	4	"ClearErr Interrupt Clear Registers - LOW (ClearErr_LO)—Offset 358h" on page 4009	00000000h
35C–35Fh	4	"ClearErr Interrupt Clear Registers - HIGH (ClearErr_HI)—Offset 35Ch" on page 4010	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
360–363h	4	"Combined Interrupt Status Register - LOW (StatusInt_LO)—Offset 360h" on page 4010	00000000h
364–367h	4	"Combined Interrupt Status Register - HIGH (StatusInt_HI)—Offset 364h" on page 4011	00000000h
368–36Bh	4	"Source Software Transaction Request Register - LOW (ReqSrcReg_LO)—Offset 368h" on page 4011	00000000h
36C–36Fh	4	"Source Software Transaction Request Register - HIGH (ReqSrcReg_HI)—Offset 36Ch" on page 4012	00000000h
370–373h	4	"Destination Software Transaction Request Register - LOW (ReqDstReg_LO)—Offset 370h" on page 4012	00000000h
374–377h	4	"Destination Software Transaction Request Register - HIGH (ReqDstReg_HI)—Offset 374h" on page 4013	00000000h
378–37Bh	4	"Single Source Transaction Request Register - LOW (SglRqSrcReg_LO)—Offset 378h" on page 4014	00000000h
37C–37Fh	4	"Single Source Transaction Request Register - HIGH (SglRqSrcReg_HI)—Offset 37Ch" on page 4014	00000000h
380–383h	4	"Single Destination Transaction Request Register - LOW (SglRqDstReg_LO)—Offset 380h" on page 4015	00000000h
384–387h	4	"Single Destination Transaction Request Register - HIGH (SglRqDstReg_HI)—Offset 384h" on page 4015	00000000h
388–38Bh	4	"Last Source Transaction Request Register - LOW (LstSrcReg_LO)—Offset 388h" on page 4016	00000000h
38C–38Fh	4	"Last Source Transaction Request Register - HIGH (LstSrcReg_HI)—Offset 38Ch" on page 4016	00000000h
390–393h	4	"Last Destination Transaction Request Register - LOW (LstDstReg_LO)—Offset 390h" on page 4017	00000000h
394–397h	4	"Last Destination Transaction Request Register - HIGH (LstDstReg_HI)—Offset 394h" on page 4018	00000000h
398–39Bh	4	"DW_ahb_dmac Configuration Register - LOW (DmaCfgReg_LO)—Offset 398h" on page 4018	00000000h
39C–39Fh	4	"DW_ahb_dmac Configuration Register - HIGH (DmaCfgReg_HI)—Offset 39Ch" on page 4019	00000000h
3A0–3A3h	4	"DW_ahb_dmac Channel Enable Register - LOW (ChEnReg_LO)—Offset 3A0h" on page 4019	00000000h
3A4–3A7h	4	"DW_ahb_dmac Channel Enable Register - HIGH (ChEnReg_HI)—Offset 3A4h" on page 4020	00000000h
3A8–3ABh	4	"DW_ahb_dmac ID Register - LOW (DmaIdReg_LO)—Offset 3A8h" on page 4020	C0CAC01Ah
3AC–3AFh	4	"DW_ahb_dmac ID Register - HIGH (DmaIdReg_HI)—Offset 3ACh" on page 4021	00000000h
3B0–3B3h	4	"DW_ahb_dmac Test Register - LOW (DmaTestReg_LO)—Offset 3B0h" on page 4021	00000000h
3B4–3B7h	4	"DW_ahb_dmac Test Register - HIGH (DmaTestReg_HI)—Offset 3B4h" on page 4022	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3C8–3CBh	4	"DW_ahb_dmac Component Parameters Register 6 - LOW (DMA_COMP_PARAMS_6_LO)—Offset 3C8h" on page 4022	00000000h
3CC–3CFh	4	"DW_ahb_dmac Component Parameters Register 6 - HIGH (DMA_COMP_PARAMS_6_HI)—Offset 3CCh" on page 4023	38220300h
3D0–3D3h	4	"DW_ahb_dmac Component Parameters Register 5 - LOW (DMA_COMP_PARAMS_5_LO)—Offset 3D0h" on page 4025	38220300h
3D4–3D7h	4	"DW_ahb_dmac Component Parameters Register 5 - HIGH (DMA_COMP_PARAMS_5_HI)—Offset 3D4h" on page 4026	38220300h
3D8–3DBh	4	"DW_ahb_dmac Component Parameters Register 4 - LOW (DMA_COMP_PARAMS_4_LO)—Offset 3D8h" on page 4028	38220300h
3DC–3DFh	4	"DW_ahb_dmac Component Parameters Register 4 - HIGH (DMA_COMP_PARAMS_4_HI)—Offset 3DCh" on page 4030	38220300h
3E0–3E3h	4	"DW_ahb_dmac Component Parameters Register 3 - LOW (DMA_COMP_PARAMS_3_LO)—Offset 3E0h" on page 4032	38220300h
3E4–3E7h	4	"DW_ahb_dmac Component Parameters Register 3 - HIGH (DMA_COMP_PARAMS_3_HI)—Offset 3E4h" on page 4033	38220300h
3E8–3EBh	4	"DW_ahb_dmac Component Parameters Register 2 - LOW (DMA_COMP_PARAMS_2_LO)—Offset 3E8h" on page 4035	38220300h
3EC–3EFh	4	"DW_ahb_dmac Component Parameters Register 2 - HIGH (DMA_COMP_PARAMS_2_HI)—Offset 3ECh" on page 4037	00000000h
3F0–3F3h	4	"DW_ahb_dmac Component Parameters Register 1 - LOW (DMA_COMP_PARAMS_1_LO)—Offset 3F0h" on page 4038	AAAAAAAAh
3F4–3F7h	4	"DW_ahb_dmac Component Parameters Register 1 - HIGH (DMA_COMP_PARAMS_1_HI)—Offset 3F4h" on page 4040	37000F04h
3F8–3FBh	4	"DMA Component ID Register - LOW (DmaCompsID_LO)—Offset 3F8h" on page 4041	44571110h
3FC–3FFh	4	"DMA Component ID Register - HIGH (DmaCompsID_HI)—Offset 3FCh" on page 4042	3231362Ah

9.2.1 Source Address Register for Channel 0 - LOW (SAR0_LO)—Offset 0h

Source Address Register for Channel 0

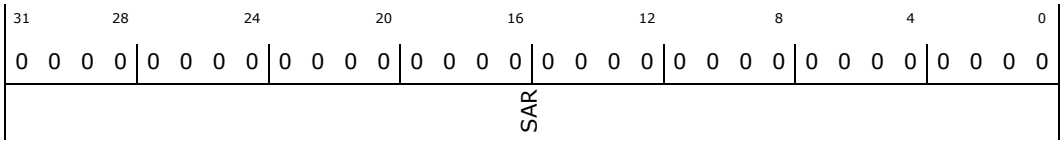
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

9.2.2 Source Address Register for Channel 0 - HIGH (SAR0_HI)—Offset 4h

Source Address Register for Channel 0

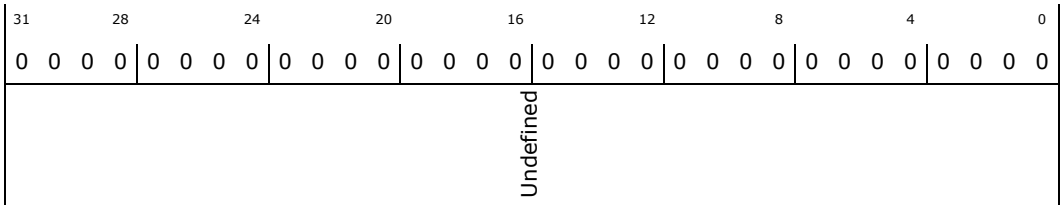
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.2.3 Destination Address Register for Channel 0 - LOW (DAR0_LO)—Offset 8h

Destination Address Register for Channel 0

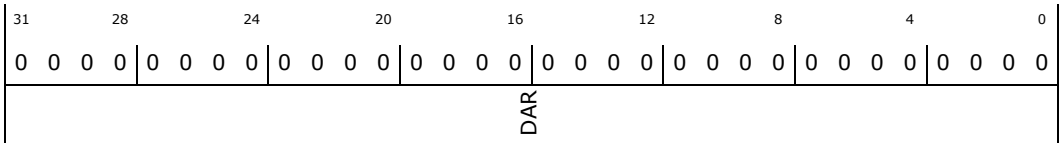
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

9.2.4 Destination Address Register for Channel 0 - HIGH (DAR0_HI)—Offset Ch

Destination Address Register for Channel 0

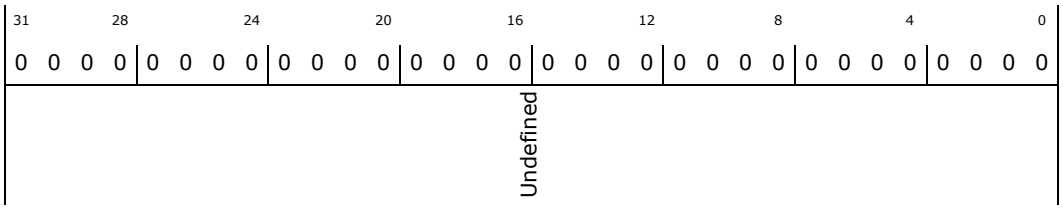
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.5 Linked List Pointer Register for Channel 0 - LOW (LLP0_LO)—Offset 10h

Linked List Pointer Register for Channel 0

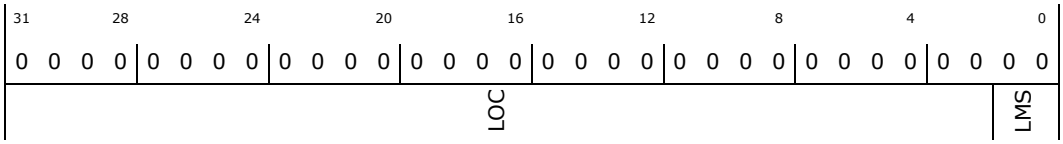
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0x0 RW	**LMS:** List Master Select. Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

9.2.6 Linked List Pointer Register for Channel 0 - HIGH (LLP0_HI)—Offset 14h

Linked List Pointer Register for Channel 0

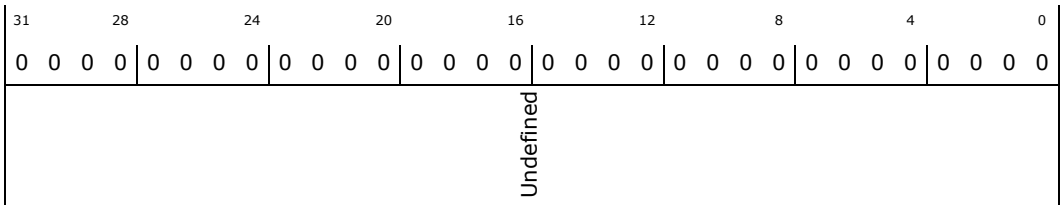
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.2.7 Control Register for Channel 0 - LOW (CTL0_LO)—Offset 18h

Control Register for Channel 0

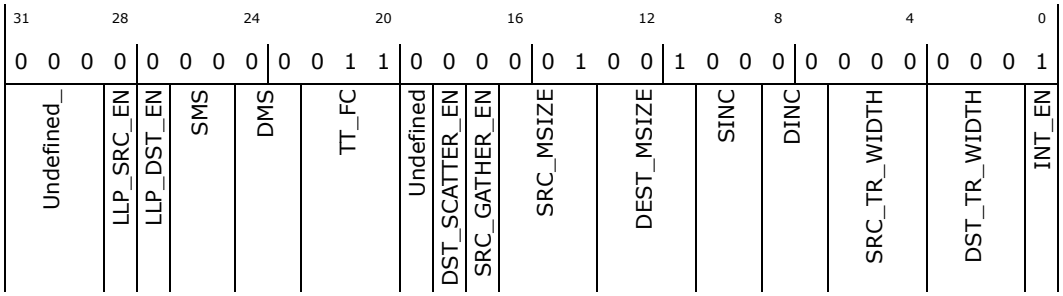
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**Undefined_:** RESERVED
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0x0 RW	**SMS:** Source Master Select. Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0x0 RW	**DMS:** Destination Master Select. Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	0x3 RW	**TT_FC:** Transfer Type and Flow Control.
19	0x0 RW	**Undefined:** RESERVED
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit. 0 = disabled 1 = enabled
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit. 0 = disabled 1 = enabled
16:14	0x1 RW	**SRC_MSIZE:** Source Burst Transaction Length.
13:11	0x1 RW	**DEST_MSIZE:** Destination Burst Transaction Length.
10:9	0x0 RW	**SINC:** Source Address Increment. 00 = Increment 01 = Decrement 1x = No change

Bit Range	Default & Access	Field Name (ID): Description
8:7	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. 00 = Increment 01 = Decrement 1x = No change
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	0x1 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

9.2.8 Control Register for Channel 0 - HIGH (CTL0_HI)—Offset 1Ch

Control Register for Channel 0

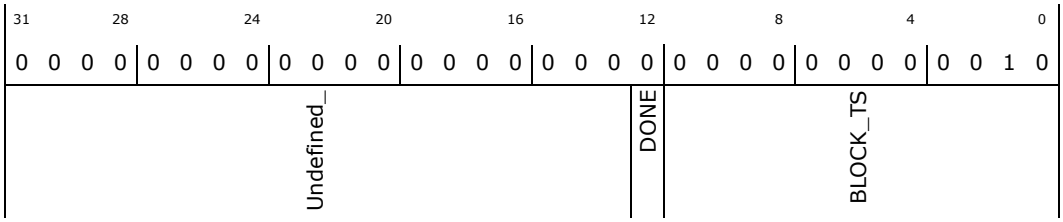
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Undefined_:** RESERVED
12	0x0 RW	**DONE:** Done bit
11:0	0x2 RW	**BLOCK_TS:** Block Transfer Size. When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

9.2.9 Configuration register for Channel 0 - LOW (CFG0_LO)—Offset 40h

Configuration register for Channel 0

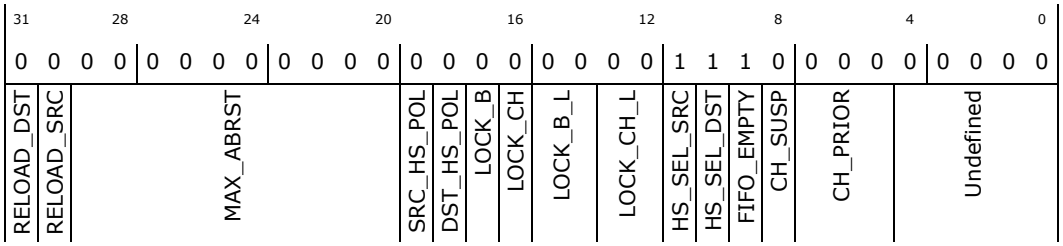
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000E00h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0x0 RW	**MAX_ABRST:** Maximum AMBA Burst Length. Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**LOCK_B:** Bus Lock Bit. When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0x0 RW	**LOCK_CH:** Channel Lock Bit. When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0x0 RW	**LOCK_B_L:** Bus Lock Level. Indicates the duration over which CFGx.LOCK_B bit applies. 00 = Over complete DMA transfer 01 = Over complete DMA block transfer 1x = Over complete DMA transaction
13:12	0x0 RW	**LOCK_CH_L:** Channel Lock Level. Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	0x1 RW	**HS_SEL_SRC:** Source Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
10	0x1 RW	**HS_SEL_DST:** Destination Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking

Bit Range	Default & Access	Field Name (ID): Description
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA transfers from source until this bit is cleared.
7:5	0x0 RW	**CH_PRIOR:** Channel priority. Priority of 7 is the highest priority.
4:0	0x0 RW	**Undefined:** RESERVED

9.2.10 Configuration register for Channel 0 - HIGH (CFG0_HI)—Offset 44h

Configuration register for Channel 0 _ HIGH

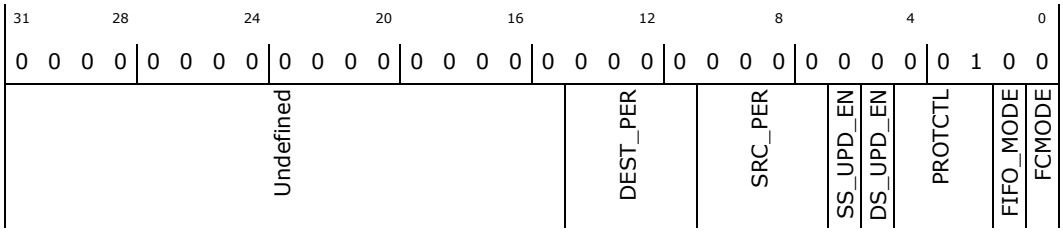
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RW	**Undefined:** Reserved
14:11	0x0 RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0x0 RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.

Bit Range	Default & Access	Field Name (ID): Description
4:2	0x1 RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0x0 RW	**FIFO_MODE:** FIFO Mode Select. Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0 = Space/data available for single AHB transfer of the specified transfer width. 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0x0 RW	**FCMODE:** Flow Control Mode. Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. 1 = Source transaction requests are not serviced until a destination transaction request occurs.

9.2.11 Source Gather Register for Channel 0 - LOW (SGR0_LO)—Offset 48h

Source Gather Register for Channel 0

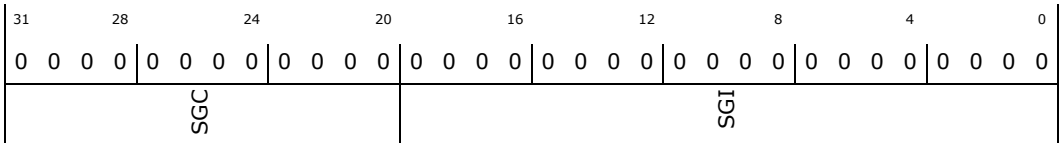
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval

9.2.12 Source Gather Register for Channel 0 - HIGH (SGR0_HI)—Offset 4Ch

Source Gather Register for Channel 0

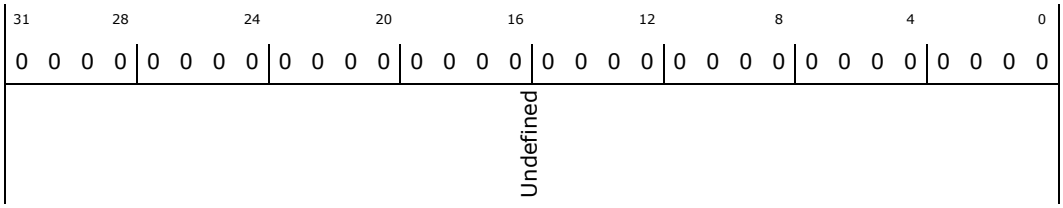
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.13 Destination Scatter Register for Channel 0 - LOW (DSR0_LO)—Offset 50h

Destination Scatter Register for Channel 0

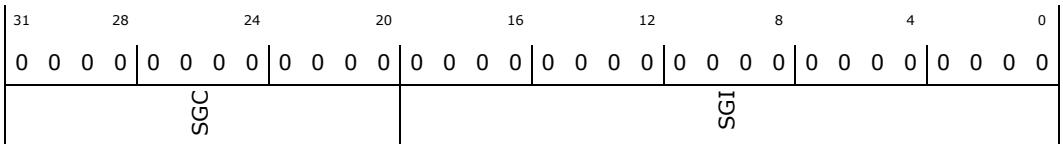
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC (SGC):** Dest scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI (SGI):** Dest scatter interval

9.2.14 Dest scatter Register for Channel 0 - HIGH (DSR0_HI)—Offset 54h

Dest scatter Register for Channel 0

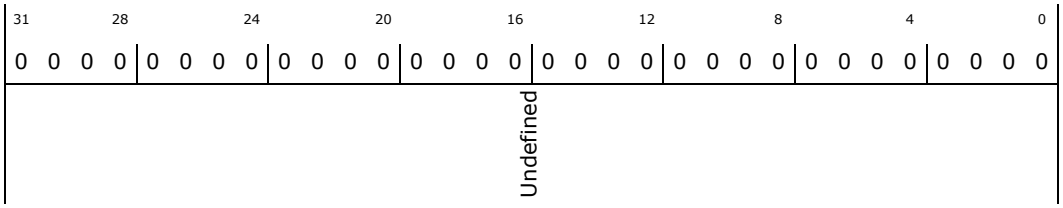
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.15 Source Address Register for Channel 1 - LOW (SAR1_LO)—Offset 58h

Source Address Register for Channel 1

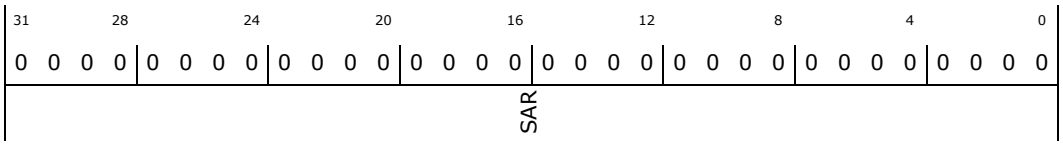
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

9.2.16 Source Address Register for Channel 1 - HIGH (SAR1_HI)—Offset 5Ch

Source Address Register for Channel 1

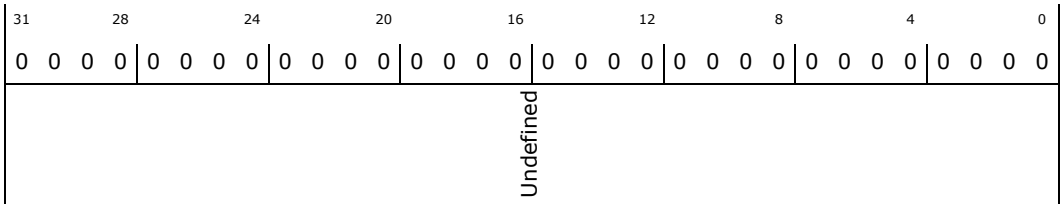
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.2.17 Destination Address Register for Channel 1 - LOW (DAR1_LO)—Offset 60h

Destination Address Register for Channel 1

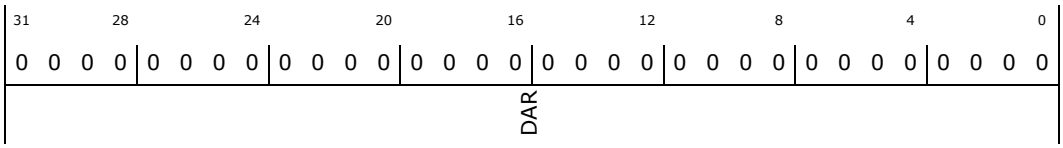
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

9.2.18 Destination Address Register for Channel 1 - HIGH (DAR1_HI)—Offset 64h

Destination Address Register for Channel 1

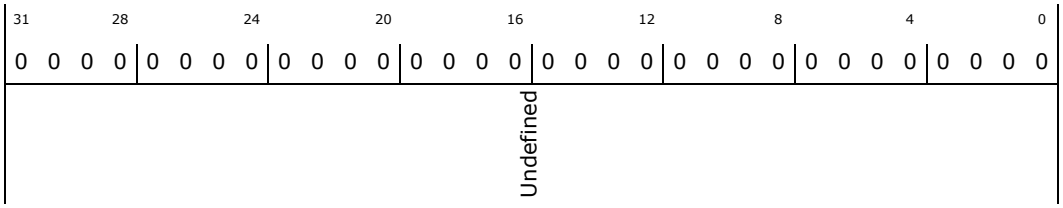
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.19 Linked List Pointer Register for Channel 1 - LOW (LLP1_LO)—Offset 68h

Linked List Pointer Register for Channel 1

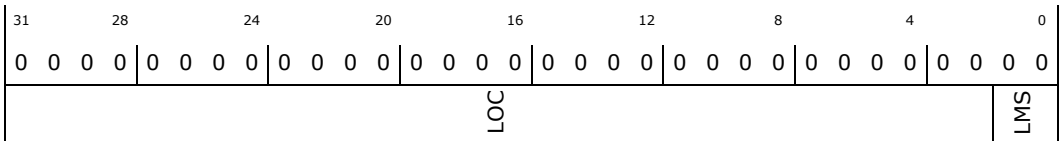
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0x0 RW	**LMS:** List Master Select. Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

9.2.20 Linked List Pointer Register for Channel 1 - HIGH (LLP1_HI)—Offset 6Ch

Linked List Pointer Register for Channel 1

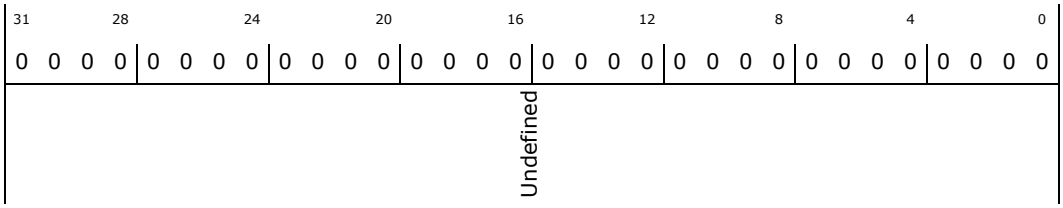
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.2.21 Control Register for Channel 1 - LOW (CTL1_LO)—Offset 70h

Control Register for Channel 1

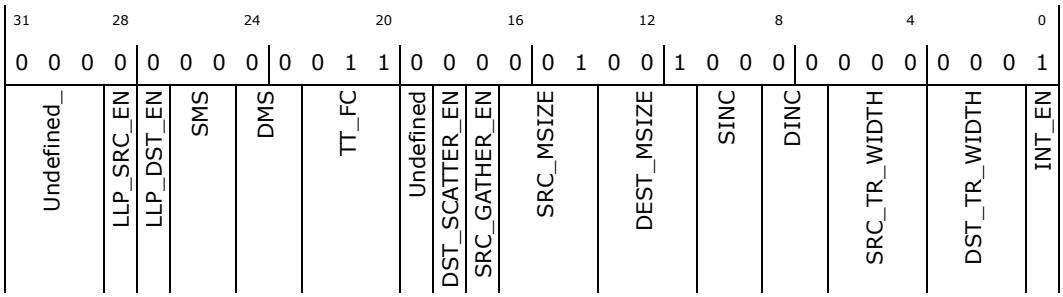
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**Undefined_:** RESERVED
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.

Bit Range	Default & Access	Field Name (ID): Description
26:25	0x0 RW	**SMS:** Source Master Select. Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0x0 RW	**DMS:** Destination Master Select. Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	0x3 RW	**TT_FC:** Transfer Type and Flow Control.
19	0x0 RW	**Undefined:** RESERVED
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit. 0 = disabled 1 = enabled
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit. 0 = disabled 1 = enabled
16:14	0x1 RW	**SRC_MSIZE:** Source Burst Transaction Length.
13:11	0x1 RW	**DEST_MSIZE:** Destination Burst Transaction Length.
10:9	0x0 RW	**SINC:** Source Address Increment. 00 = Increment 01 = Decrement 1x = No change
8:7	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. 00 = Increment 01 = Decrement 1x = No change
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	0x1 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

9.2.22 Control Register for Channel 1 - HIGH (CTL1_HI)—Offset 74h

Control Register for Channel 1

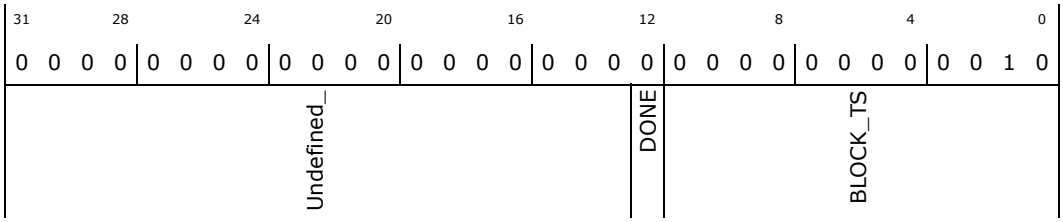
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Undefined_:** RESERVED
12	0x0 RW	**DONE:** Done bit
11:0	0x2 RW	**BLOCK_TS:** Block Transfer Size. When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

9.2.23 Configuration register for Channel 1 - LOW (CFG1_LO)—Offset 98h

Configuration register for Channel 1

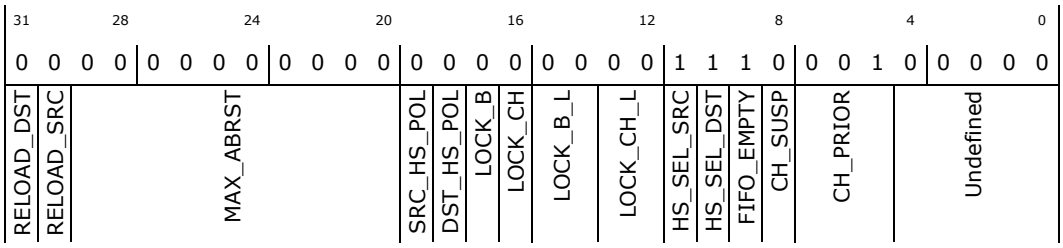
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

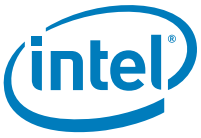
Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000E20h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.



Bit Range	Default & Access	Field Name (ID): Description
29:20	0x0 RW	**MAX_ABRST:** Maximum AMBA Burst Length. Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**LOCK_B:** Bus Lock Bit. When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0x0 RW	**LOCK_CH:** Channel Lock Bit. When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0x0 RW	**LOCK_B_L:** Bus Lock Level. Indicates the duration over which CFGx.LOCK_B bit applies. 00 = Over complete DMA transfer 01 = Over complete DMA block transfer 1x = Over complete DMA transaction
13:12	0x0 RW	**LOCK_CH_L:** Channel Lock Level. Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	0x1 RW	**HS_SEL_SRC:** Source Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
10	0x1 RW	**HS_SEL_DST:** Destination Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA transfers from source until this bit is cleared.
7:5	0x1 RW	**CH_PRIOR:** Channel priority. Priority of 7 is the highest priority.
4:0	0x0 RW	**Undefined:** RESERVED

9.2.24 Configuration register for Channel 1 - HIGH (CFG1_HI)—Offset 9Ch

Configuration register for Channel 1 _ HIGH

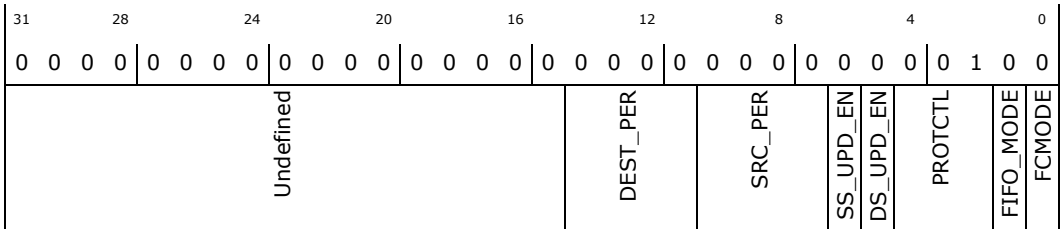
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RW	**Undefined:** Reserved
14:11	0x0 RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0x0 RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	0x1 RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0x0 RW	**FIFO_MODE:** FIFO Mode Select. Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0 = Space/data available for single AHB transfer of the specified transfer width. 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0x0 RW	**FCMODE:** Flow Control Mode. Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. 1 = Source transaction requests are not serviced until a destination transaction request occurs.

9.2.25 Source Gather Register for Channel 1 - LOW (SGR1_LO)—Offset A0h

Source Gather Register for Channel 1

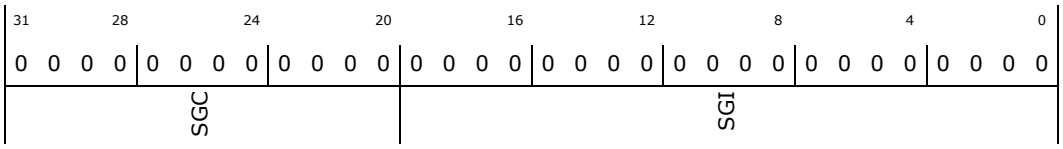
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval

9.2.26 Source Gather Register for Channel 1 - HIGH (SGR1_HI)—Offset A4h

Source Gather Register for Channel 1

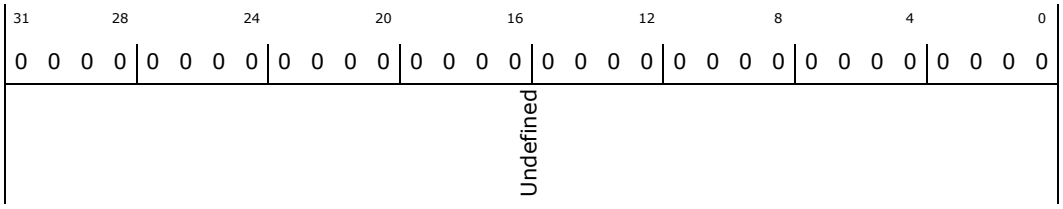
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.27 Destination Scatter Register for Channel 1 - LOW (DSR1_LO)—Offset A8h

Destination Scatter Register for Channel 1

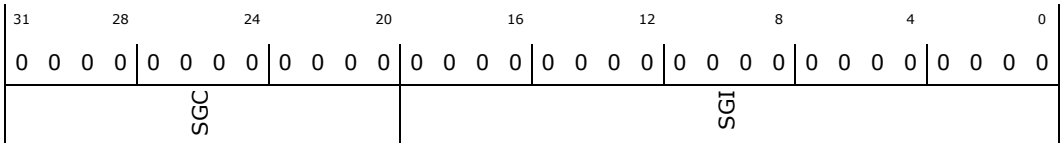
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC (SGC):** Dest scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI (SGI):** Dest scatter interval

9.2.28 Dest scatter Register for Channel 1 - HIGH (DSR1_HI)—Offset ACh

Dest scatter Register for Channel 1

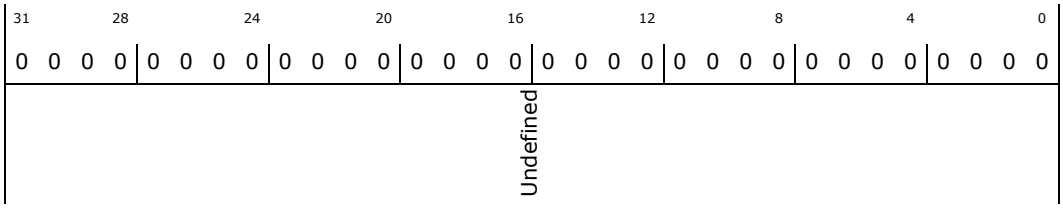
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.29 Source Address Register for Channel 2 - LOW (SAR2_LO)—Offset B0h

Source Address Register for Channel 2

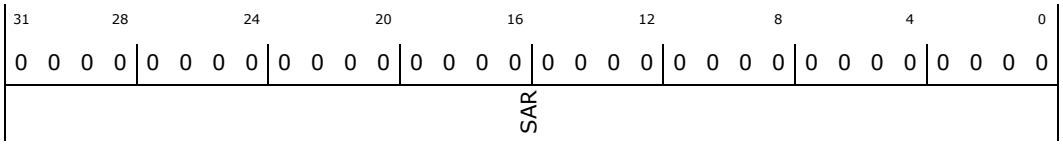
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

9.2.30 Source Address Register for Channel 2 - HIGH (SAR2_HI)—Offset B4h

Source Address Register for Channel 2

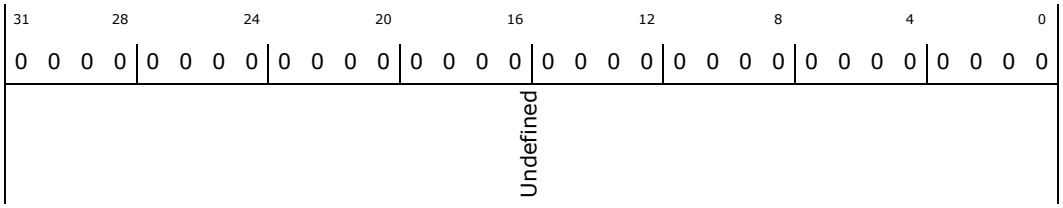
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.2.31 Destination Address Register for Channel 2 - LOW (DAR2_LO)—Offset B8h

Destination Address Register for Channel 2

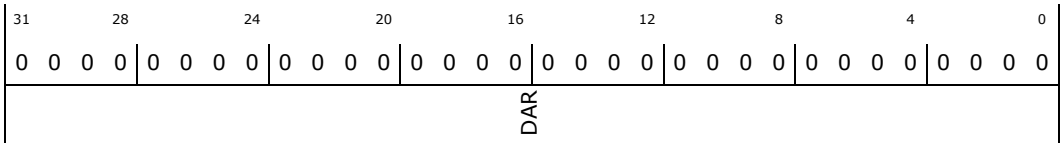
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

9.2.32 Destination Address Register for Channel 2 - HIGH (DAR2_HI)—Offset BCh

Destination Address Register for Channel 2

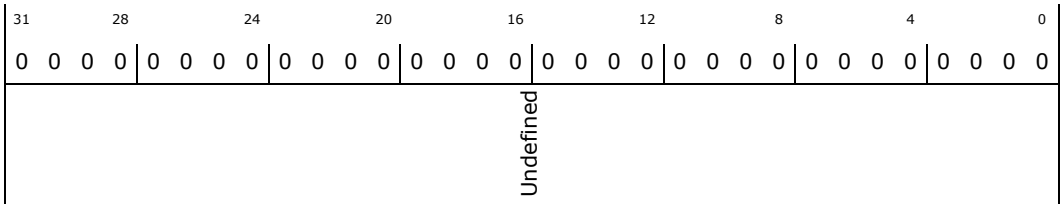
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.33 Linked List Pointer Register for Channel 2 - LOW (LLP2_LO)—Offset C0h

Linked List Pointer Register for Channel 2

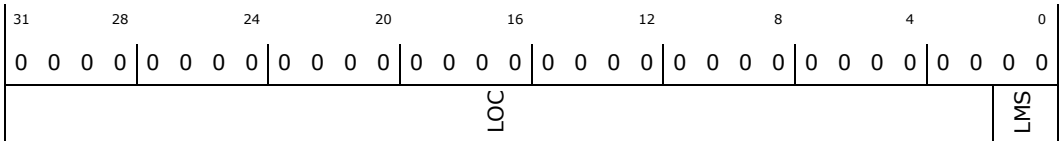
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0x0 RW	**LMS:** List Master Select. Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

9.2.34 Linked List Pointer Register for Channel 2 - HIGH (LLP2_HI)—Offset C4h

Linked List Pointer Register for Channel 2

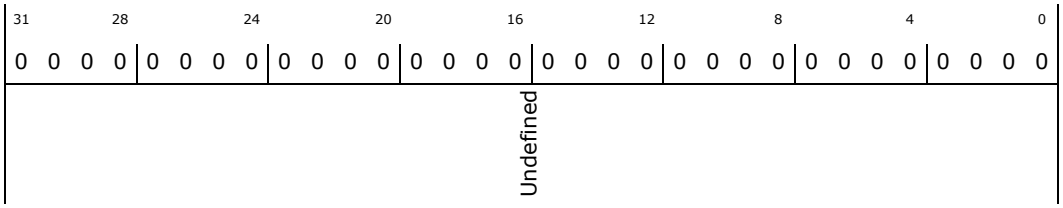
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.2.35 Control Register for Channel 2 - LOW (CTL2_LO)—Offset C8h

Control Register for Channel 2

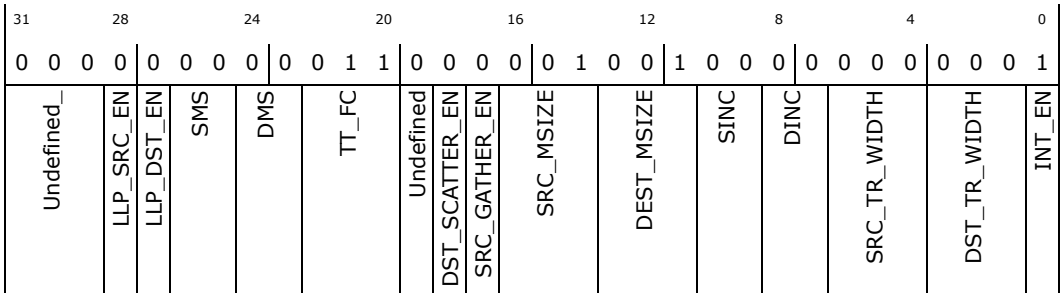
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**Undefined_:** RESERVED
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0x0 RW	**SMS:** Source Master Select. Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0x0 RW	**DMS:** Destination Master Select. Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	0x3 RW	**TT_FC:** Transfer Type and Flow Control.
19	0x0 RW	**Undefined:** RESERVED
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit. 0 = disabled 1 = enabled
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit. 0 = disabled 1 = enabled
16:14	0x1 RW	**SRC_MSIZE:** Source Burst Transaction Length.
13:11	0x1 RW	**DEST_MSIZE:** Destination Burst Transaction Length.
10:9	0x0 RW	**SINC:** Source Address Increment. 00 = Increment 01 = Decrement 1x = No change
8:7	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. 00 = Increment 01 = Decrement 1x = No change
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	0x1 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

9.2.36 Control Register for Channel 2 - HIGH (CTL2_HI)—Offset CCh

Control Register for Channel 2

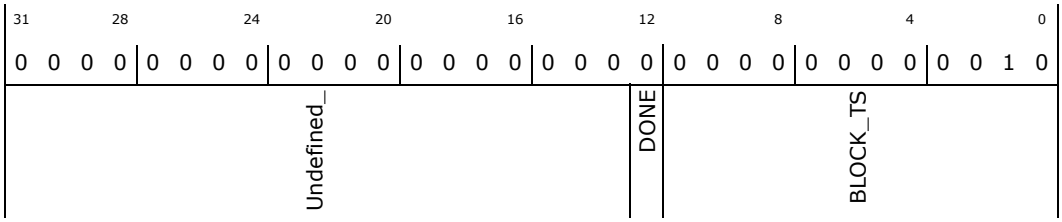
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Undefined_:** RESERVED
12	0x0 RW	**DONE:** Done bit
11:0	0x2 RW	**BLOCK_TS:** Block Transfer Size. When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

9.2.37 Configuration register for Channel 2 - LOW (CFG2_LO)—Offset F0h

Configuration register for Channel 2

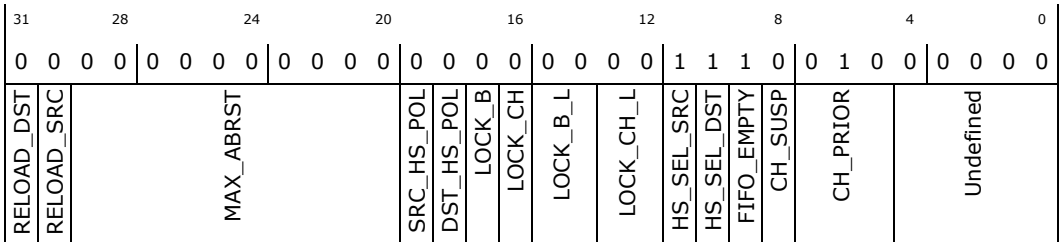
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000E40h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0x0 RW	**MAX_ABRST:** Maximum AMBA Burst Length. Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**LOCK_B:** Bus Lock Bit. When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0x0 RW	**LOCK_CH:** Channel Lock Bit. When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0x0 RW	**LOCK_B_L:** Bus Lock Level. Indicates the duration over which CFGx.LOCK_B bit applies. 00 = Over complete DMA transfer 01 = Over complete DMA block transfer 1x = Over complete DMA transaction
13:12	0x0 RW	**LOCK_CH_L:** Channel Lock Level. Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	0x1 RW	**HS_SEL_SRC:** Source Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
10	0x1 RW	**HS_SEL_DST:** Destination Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA transfers from source until this bit is cleared.
7:5	0x2 RW	**CH_PRIOR:** Channel priority. Priority of 7 is the highest priority.
4:0	0x0 RW	**Undefined:** RESERVED

9.2.38 Configuration register for Channel 2 - HIGH (CFG2_HI)—Offset F4h

Configuration register for Channel 2 _ HIGH

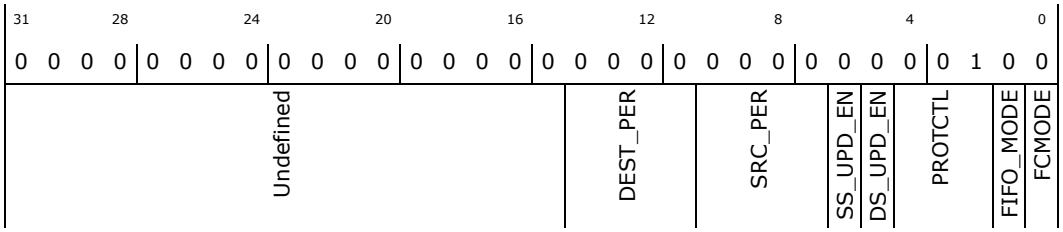
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RW	**Undefined:** Reserved
14:11	0x0 RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0x0 RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	0x1 RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0x0 RW	**FIFO_MODE:** FIFO Mode Select. Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0 = Space/data available for single AHB transfer of the specified transfer width. 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0x0 RW	**FCMODE:** Flow Control Mode. Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. 1 = Source transaction requests are not serviced until a destination transaction request occurs.

9.2.39 Source Gather Register for Channel 2 - LOW (SGR2_LO)—Offset F8h

Source Gather Register for Channel 2

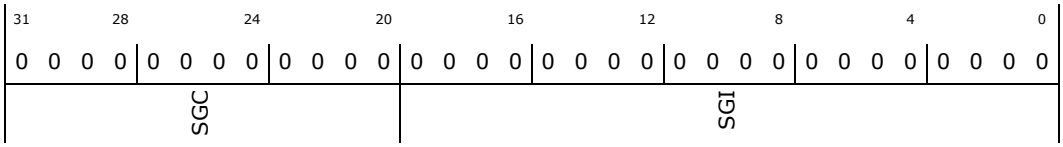
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval

9.2.40 Source Gather Register for Channel 2 - HIGH (SGR2_HI)—Offset FCh

Source Gather Register for Channel 2

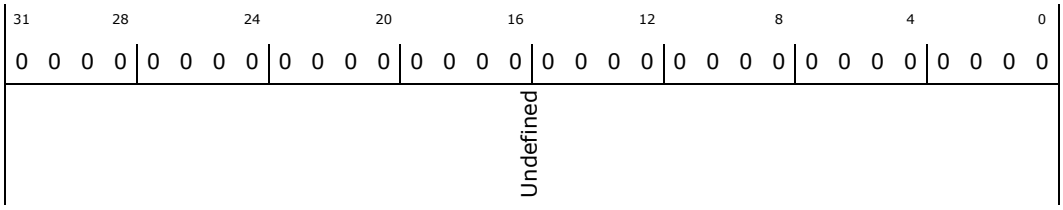
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.41 Destination Scatter Register for Channel 2 - LOW (DSR2_LO)—Offset 100h

Destination Scatter Register for Channel 2

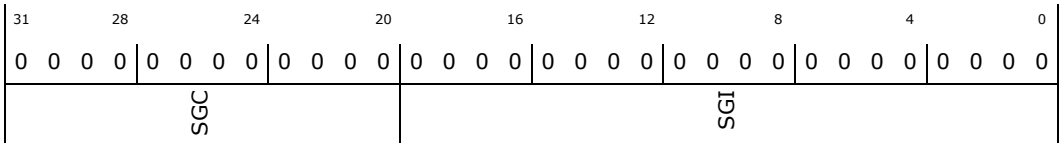
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 100h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC (SGC):** Dest scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI (SGI):** Dest scatter interval

9.2.42 Dest scatter Register for Channel 2 - HIGH (DSR2_HI)—Offset 104h

Dest scatter Register for Channel 2

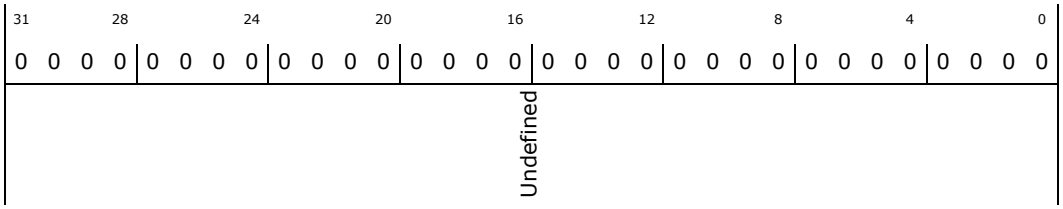
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 104h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.43 Source Address Register for Channel 3 - LOW (SAR3_LO)—Offset 108h

Source Address Register for Channel 3

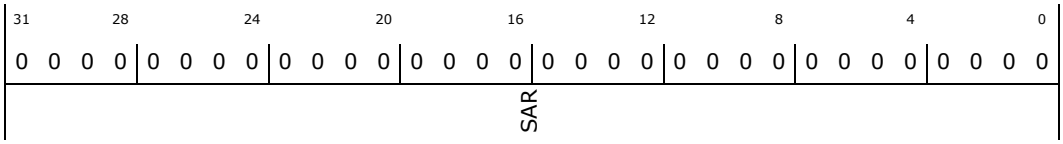
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 108h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

9.2.44 Source Address Register for Channel 3 - HIGH (SAR3_HI)—Offset 10Ch

Source Address Register for Channel 3

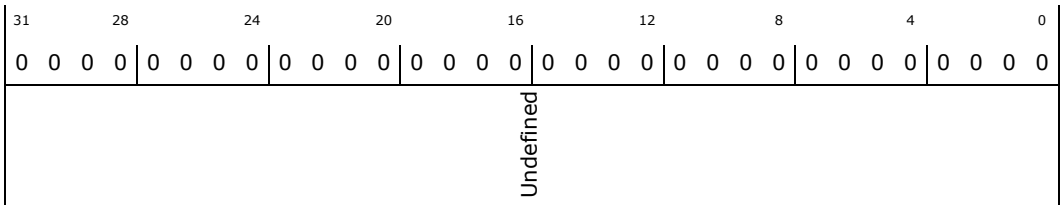
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.2.45 Destination Address Register for Channel 3 - LOW (DAR3_LO)—Offset 110h

Destination Address Register for Channel 3

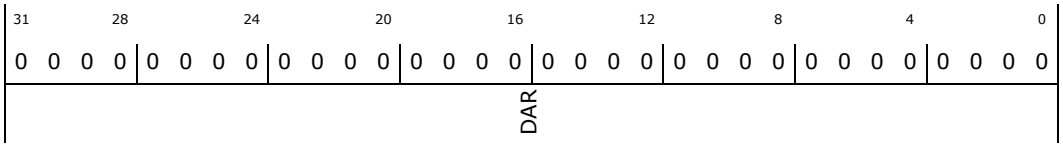
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 110h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

9.2.46 Destination Address Register for Channel 3 - HIGH (DAR3_HI)—Offset 114h

Destination Address Register for Channel 3

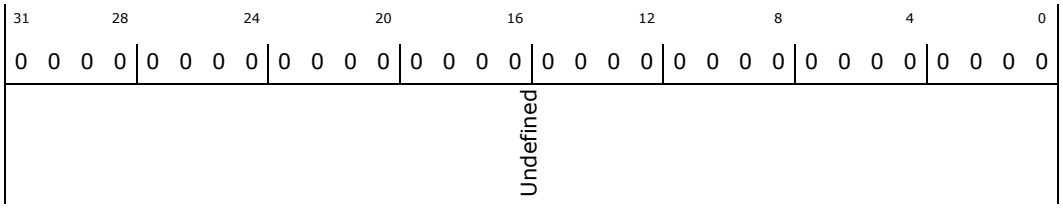
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 114h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.47 Linked List Pointer Register for Channel 3 - LOW (LLP3_LO)—Offset 118h

Linked List Pointer Register for Channel 3

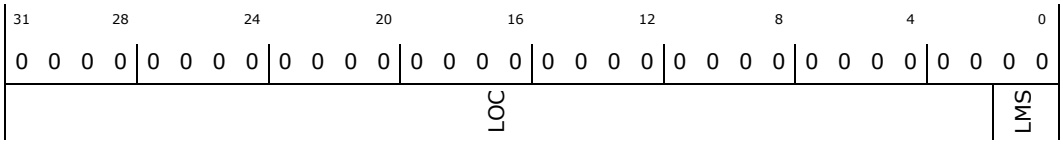
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 118h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0x0 RW	**LMS:** List Master Select. Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

9.2.48 Linked List Pointer Register for Channel 3 - HIGH (LLP3_HI)—Offset 11Ch

Linked List Pointer Register for Channel 3

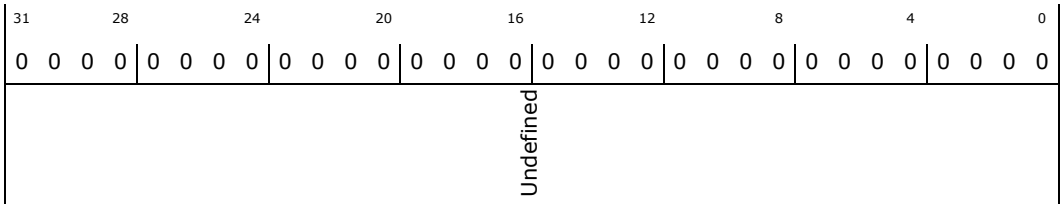
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 11Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.2.49 Control Register for Channel 3 - LOW (CTL3_LO)—Offset 120h

Control Register for Channel 3

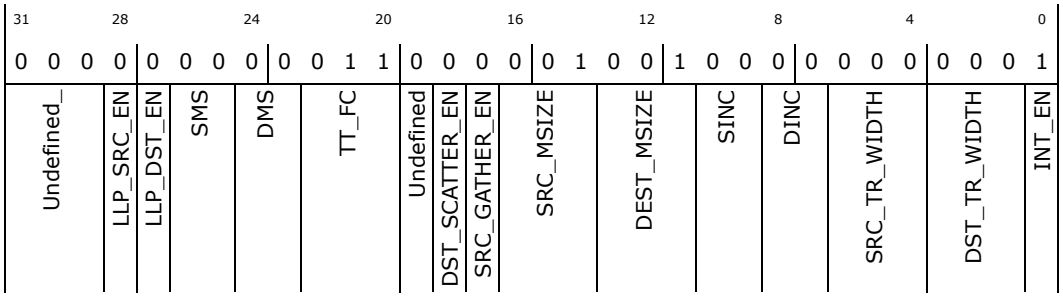
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 120h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**Undefined_:** RESERVED
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0x0 RW	**SMS:** Source Master Select. Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0x0 RW	**DMS:** Destination Master Select. Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	0x3 RW	**TT_FC:** Transfer Type and Flow Control.
19	0x0 RW	**Undefined:** RESERVED
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit. 0 = disabled 1 = enabled
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit. 0 = disabled 1 = enabled
16:14	0x1 RW	**SRC_MSIZE:** Source Burst Transaction Length.
13:11	0x1 RW	**DEST_MSIZE:** Destination Burst Transaction Length.
10:9	0x0 RW	**SINC:** Source Address Increment. 00 = Increment 01 = Decrement 1x = No change
8:7	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. 00 = Increment 01 = Decrement 1x = No change
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.

Bit Range	Default & Access	Field Name (ID): Description
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	0x1 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

9.2.50 Control Register for Channel 3 - HIGH (CTL3_HI)—Offset 124h

Control Register for Channel 3

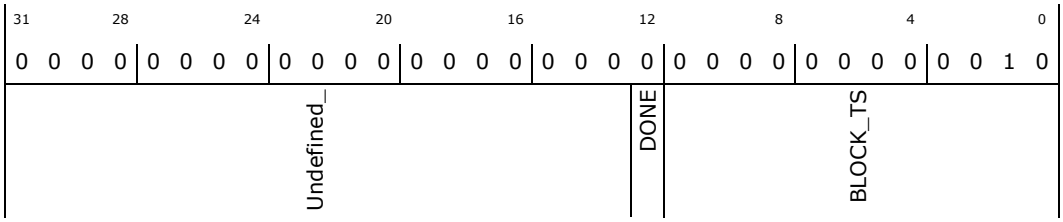
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 124h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Undefined_:** RESERVED
12	0x0 RW	**DONE:** Done bit
11:0	0x2 RW	**BLOCK_TS:** Block Transfer Size. When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

9.2.51 Configuration register for Channel 3 - LOW (CFG3_LO)—Offset 148h

Configuration register for Channel 3

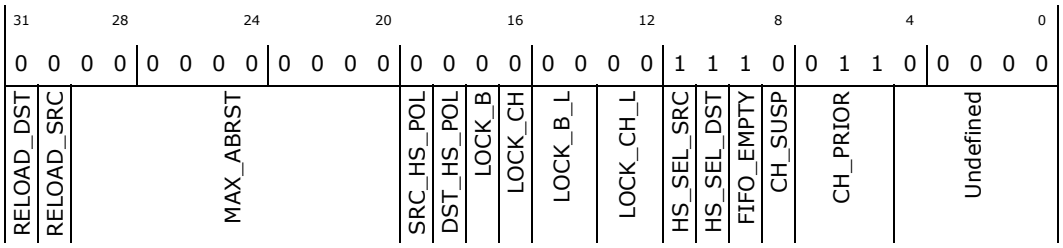
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 148h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000E60h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0x0 RW	**MAX_ABRST:** Maximum AMBA Burst Length. Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**LOCK_B:** Bus Lock Bit. When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0x0 RW	**LOCK_CH:** Channel Lock Bit. When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0x0 RW	**LOCK_B_L:** Bus Lock Level. Indicates the duration over which CFGx.LOCK_B bit applies. 00 = Over complete DMA transfer 01 = Over complete DMA block transfer 1x = Over complete DMA transaction
13:12	0x0 RW	**LOCK_CH_L:** Channel Lock Level. Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	0x1 RW	**HS_SEL_SRC:** Source Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
10	0x1 RW	**HS_SEL_DST:** Destination Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA transfers from source until this bit is cleared.
7:5	0x3 RW	**CH_PRIOR:** Channel priority. Priority of 7 is the highest priority.

Bit Range	Default & Access	Field Name (ID): Description
4:0	0x0 RW	**Undefined:** RESERVED

9.2.52 Configuration register for Channel 3 - HIGH (CFG3_HI)—Offset 14Ch

Configuration register for Channel 3 _ HIGH

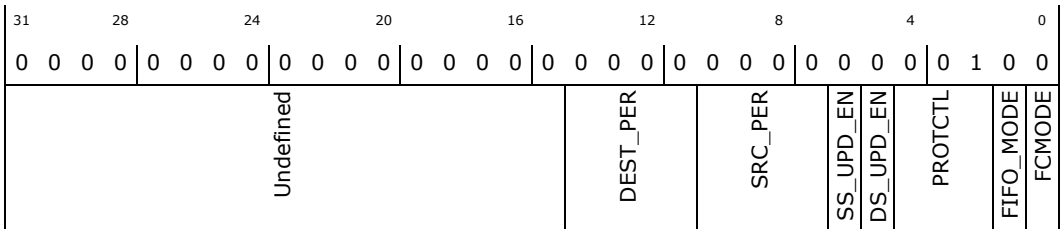
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RW	**Undefined:** Reserved
14:11	0x0 RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0x0 RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	0x1 RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**FIFO_MODE:** FIFO Mode Select. Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0 = Space/data available for single AHB transfer of the specified transfer width. 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0x0 RW	**FCMODE:** Flow Control Mode. Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. 1 = Source transaction requests are not serviced until a destination transaction request occurs.

9.2.53 Source Gather Register for Channel 3 - LOW (SGR3_LO)—Offset 150h

Source Gather Register for Channel 3

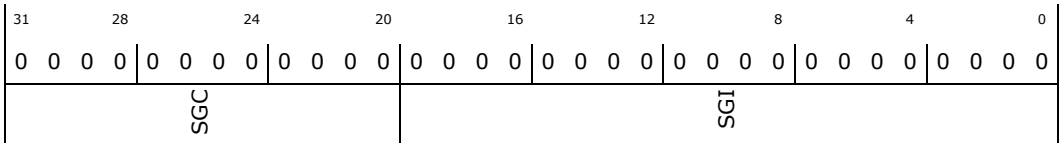
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 150h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval

9.2.54 Source Gather Register for Channel 3 - HIGH (SGR3_HI)—Offset 154h

Source Gather Register for Channel 3

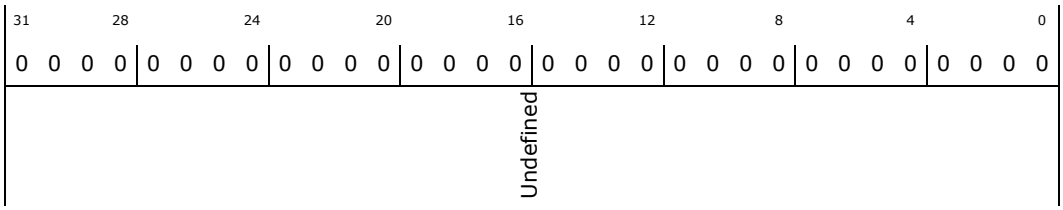
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 154h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.55 Destination Scatter Register for Channel 3 - LOW (DSR3_LO)—Offset 158h

Destination Scatter Register for Channel 3

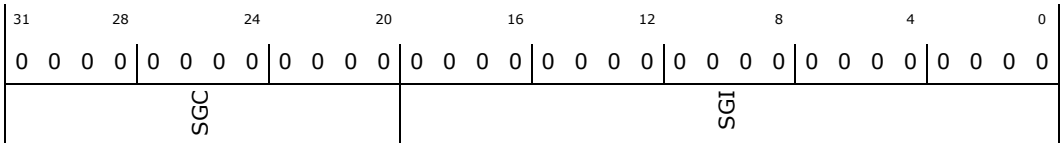
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 158h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC (SGC):** Dest scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI (SGI):** Dest scatter interval

9.2.56 Dest scatter Register for Channel 3 - HIGH (DSR3_HI)—Offset 15Ch

Dest scatter Register for Channel 3

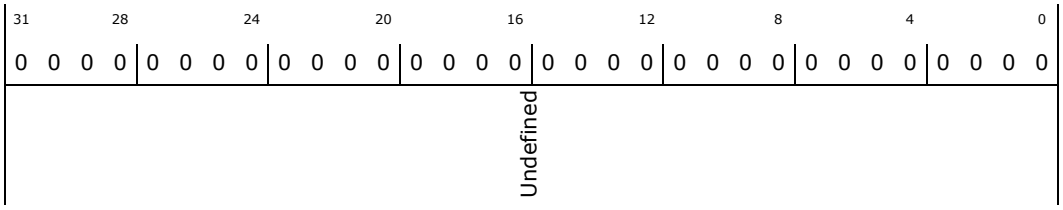
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 15Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.57 Source Address Register for Channel 4 - LOW (SAR4_LO)—Offset 160h

Source Address Register for Channel 4

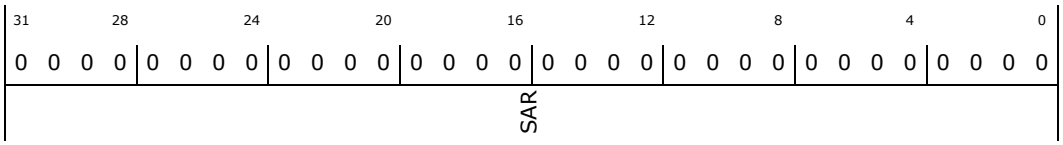
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 160h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

9.2.58 Source Address Register for Channel 4 - HIGH (SAR4_HI)—Offset 164h

Source Address Register for Channel 4

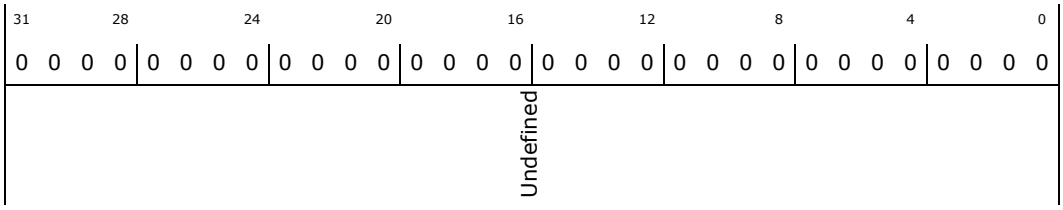
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 164h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.2.59 Destination Address Register for Channel 4 - LOW (DAR4_LO)—Offset 168h

Destination Address Register for Channel 4

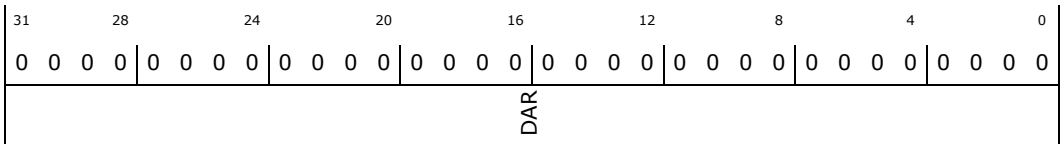
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 168h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

9.2.60 Destination Address Register for Channel 4 - HIGH (DAR4_HI)—Offset 16Ch

Destination Address Register for Channel 4

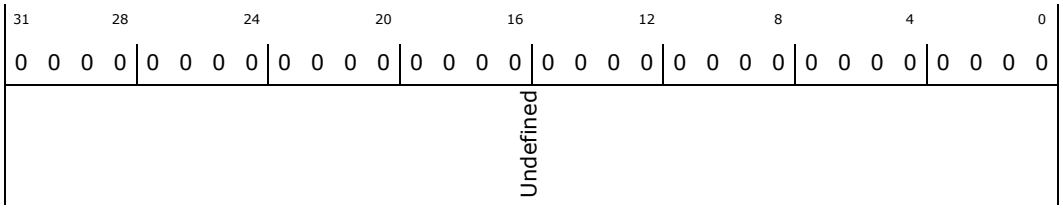
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 16Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.61 Linked List Pointer Register for Channel 4 - LOW (LLP4_LO)—Offset 170h

Linked List Pointer Register for Channel 4

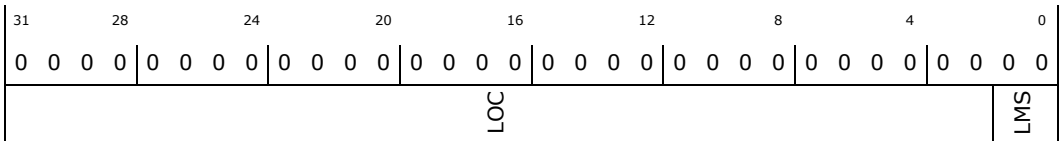
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 170h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0x0 RW	**LMS:** List Master Select. Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

9.2.62 Linked List Pointer Register for Channel 4 - HIGH (LLP4_HI)—Offset 174h

Linked List Pointer Register for Channel 4

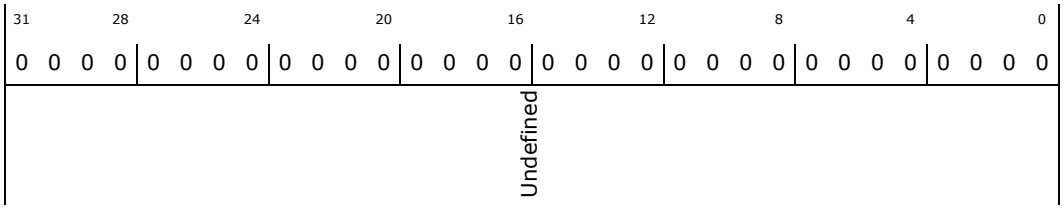
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 174h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.2.63 Control Register for Channel 4 - LOW (CTL4_LO)—Offset 178h

Control Register for Channel 4

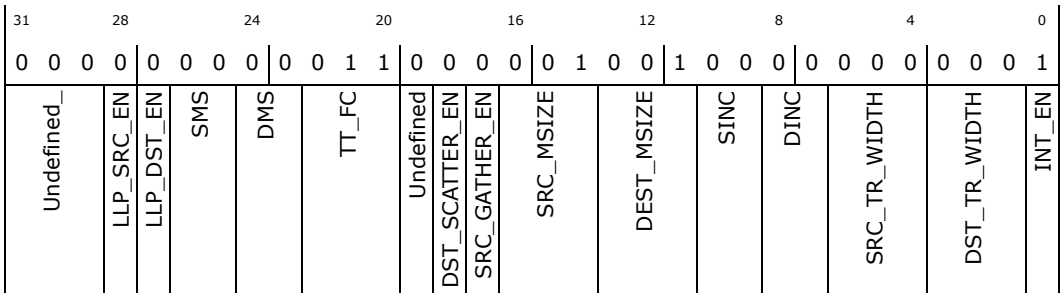
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 178h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**Undefined_:** RESERVED
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0x0 RW	**SMS:** Source Master Select. Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0x0 RW	**DMS:** Destination Master Select. Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	0x3 RW	**TT_FC:** Transfer Type and Flow Control.

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RW	**Undefined:** RESERVED
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit. 0 = disabled 1 = enabled
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit. 0 = disabled 1 = enabled
16:14	0x1 RW	**SRC_MSIZE:** Source Burst Transaction Length.
13:11	0x1 RW	**DEST_MSIZE:** Destination Burst Transaction Length.
10:9	0x0 RW	**SINC:** Source Address Increment. 00 = Increment 01 = Decrement 1x = No change
8:7	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. 00 = Increment 01 = Decrement 1x = No change
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	0x1 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

9.2.64 Control Register for Channel 4 - HIGH (CTL4_HI)—Offset 17Ch

Control Register for Channel 4

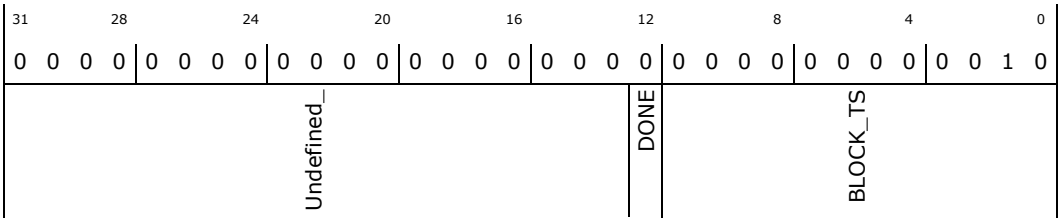
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 17Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Undefined_:** RESERVED
12	0x0 RW	**DONE:** Done bit
11:0	0x2 RW	**BLOCK_TS:** Block Transfer Size. When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

9.2.65 Configuration register for Channel 4 - LOW (CFG4_LO)—Offset 1A0h

Configuration register for Channel 4

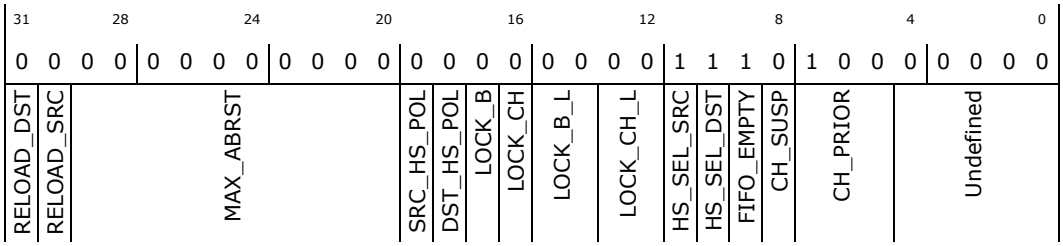
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000E80h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0x0 RW	**MAX_ABRST:** Maximum AMBA Burst Length. Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**LOCK_B:** Bus Lock Bit. When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW	**LOCK_CH:** Channel Lock Bit. When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0x0 RW	**LOCK_B_L:** Bus Lock Level. Indicates the duration over which CFGx.LOCK_B bit applies. 00 = Over complete DMA transfer 01 = Over complete DMA block transfer 1x = Over complete DMA transaction
13:12	0x0 RW	**LOCK_CH_L:** Channel Lock Level. Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	0x1 RW	**HS_SEL_SRC:** Source Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
10	0x1 RW	**HS_SEL_DST:** Destination Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA transfers from source until this bit is cleared.
7:5	0x4 RW	**CH_PRIOR:** Channel priority. Priority of 7 is the highest priority.
4:0	0x0 RW	**Undefined:** RESERVED

9.2.66 Configuration register for Channel 4 - HIGH (CFG4_HI)—Offset 1A4h

Configuration register for Channel 4 _ HIGH

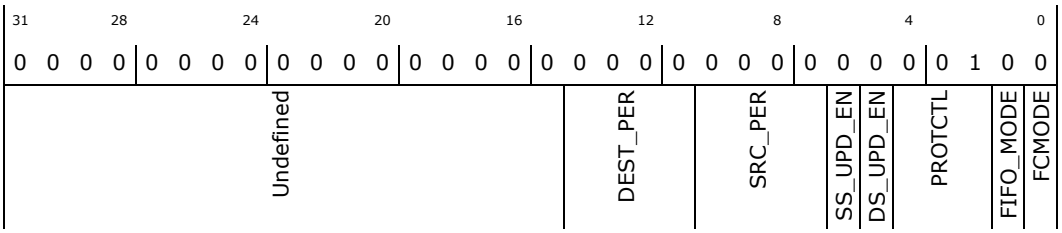
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RW	**Undefined:** Reserved
14:11	0x0 RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0x0 RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	0x1 RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0x0 RW	**FIFO_MODE:** FIFO Mode Select. Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0 = Space/data available for single AHB transfer of the specified transfer width. 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0x0 RW	**FCMODE:** Flow Control Mode. Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. 1 = Source transaction requests are not serviced until a destination transaction request occurs.

9.2.67 Source Gather Register for Channel 4 - LOW (SGR4_LO)—Offset 1A8h

Source Gather Register for Channel 4

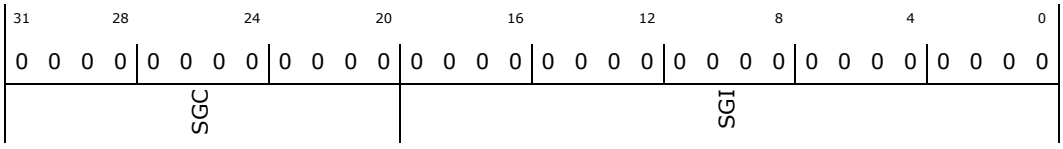
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval

9.2.68 Source Gather Register for Channel 4 - HIGH (SGR4_HI)—Offset 1ACh

Source Gather Register for Channel 4

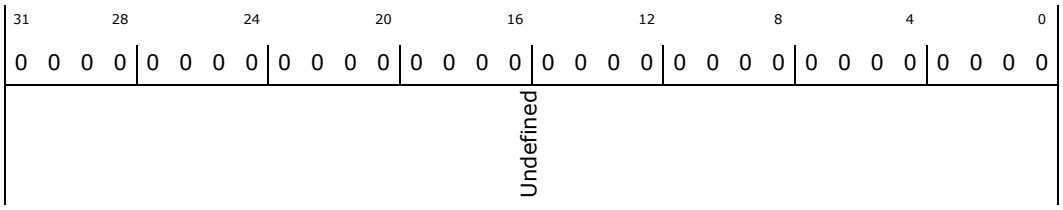
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.69 Destination Scatter Register for Channel 4 - LOW (DSR4_LO)—Offset 1B0h

Destination Scatter Register for Channel 4

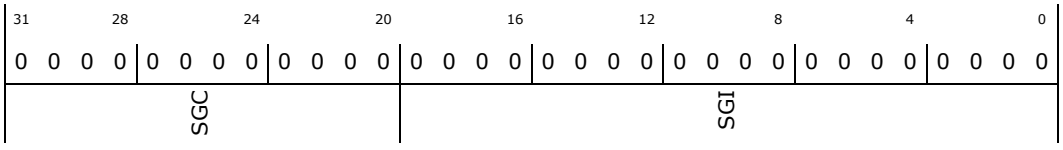
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC (SGC):** Dest scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI (SGI):** Dest scatter interval

9.2.70 Dest scatter Register for Channel 4 - HIGH (DSR4_HI)—Offset 1B4h

Dest scatter Register for Channel 4

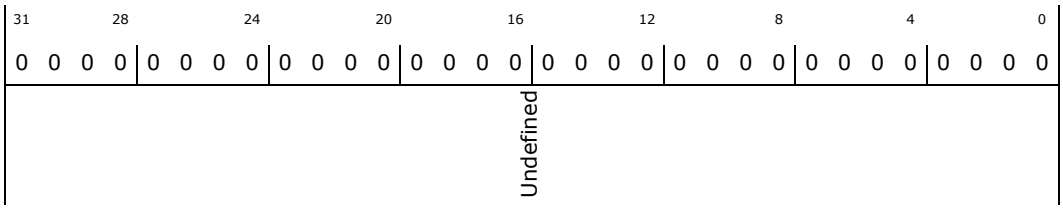
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.71 Source Address Register for Channel 5 - LOW (SAR5_LO)—Offset 1B8h

Source Address Register for Channel 5

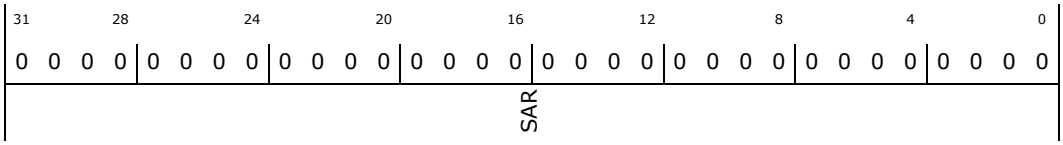
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

9.2.72 Source Address Register for Channel 5 - HIGH (SAR5_HI)—Offset 1BCh

Source Address Register for Channel 5

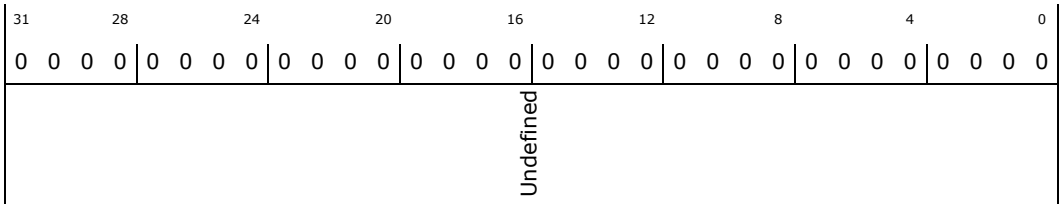
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.2.73 Destination Address Register for Channel 5 - LOW (DAR5_LO)—Offset 1C0h

Destination Address Register for Channel 5

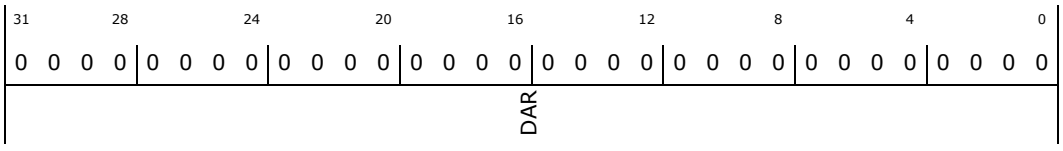
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

9.2.74 Destination Address Register for Channel 5 - HIGH (DAR5_HI)—Offset 1C4h

Destination Address Register for Channel 5

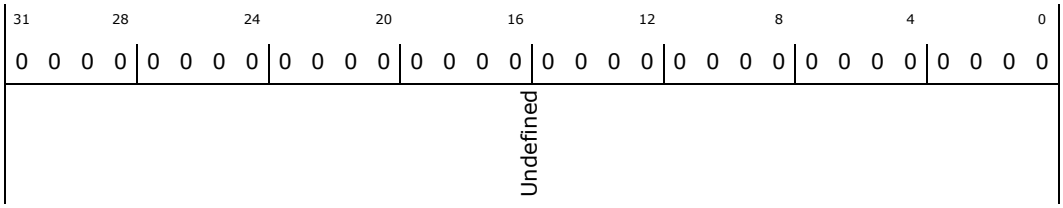
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.75 Linked List Pointer Register for Channel 5 - LOW (LLP5_LO)—Offset 1C8h

Linked List Pointer Register for Channel 5

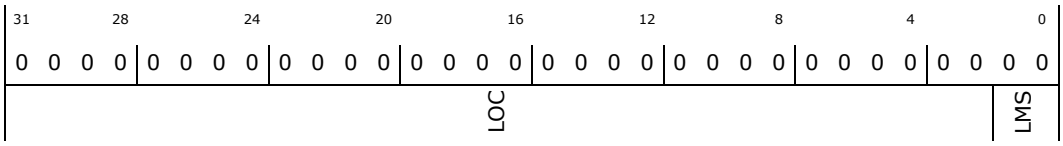
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0x0 RW	**LMS:** List Master Select. Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

9.2.76 Linked List Pointer Register for Channel 5 - HIGH (LLP5_HI)—Offset 1CCh

Linked List Pointer Register for Channel 5

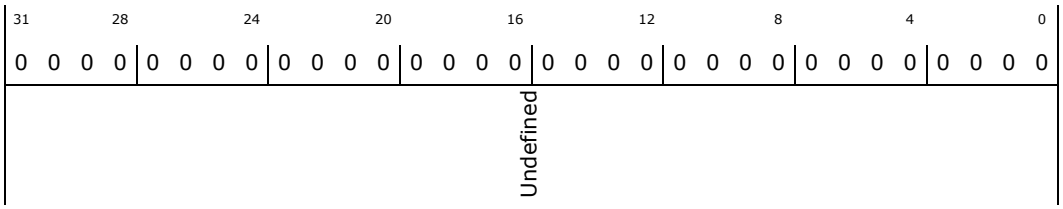
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.2.77 Control Register for Channel 5 - LOW (CTL5_LO)—Offset 1D0h

Control Register for Channel 5

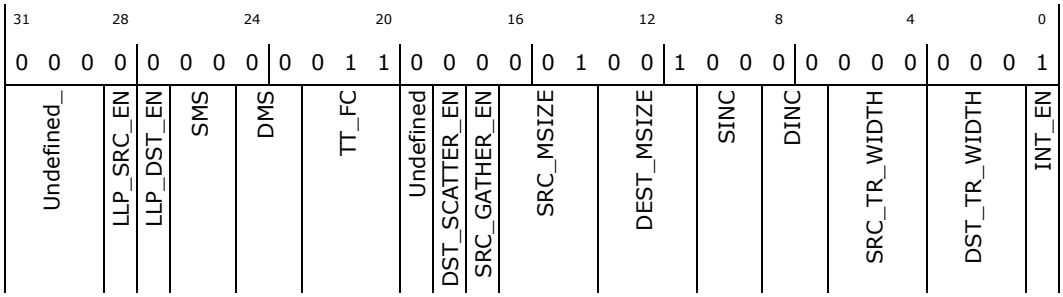
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**Undefined_:** RESERVED
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0x0 RW	**SMS:** Source Master Select. Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0x0 RW	**DMS:** Destination Master Select. Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	0x3 RW	**TT_FC:** Transfer Type and Flow Control.
19	0x0 RW	**Undefined:** RESERVED
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit. 0 = disabled 1 = enabled
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit. 0 = disabled 1 = enabled
16:14	0x1 RW	**SRC_MSIZE:** Source Burst Transaction Length.
13:11	0x1 RW	**DEST_MSIZE:** Destination Burst Transaction Length.
10:9	0x0 RW	**SINC:** Source Address Increment. 00 = Increment 01 = Decrement 1x = No change
8:7	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. 00 = Increment 01 = Decrement 1x = No change
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	0x1 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

9.2.78 Control Register for Channel 5 - HIGH (CTL5_HI)—Offset 1D4h

Control Register for Channel 5

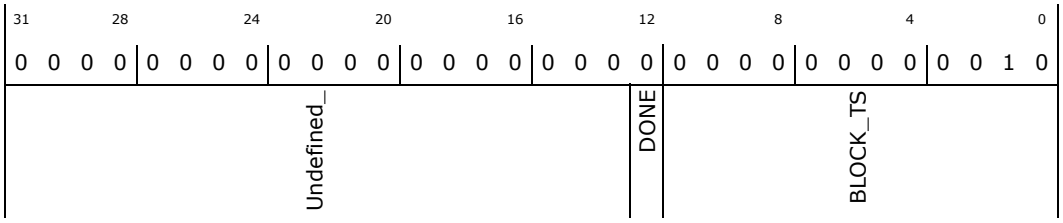
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Undefined_:** RESERVED
12	0x0 RW	**DONE:** Done bit
11:0	0x2 RW	**BLOCK_TS:** Block Transfer Size. When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

9.2.79 Configuration register for Channel 5 - LOW (CFG5_LO)—Offset 1F8h

Configuration register for Channel 5

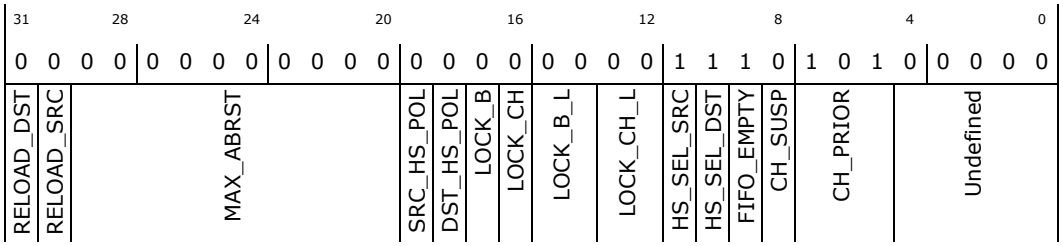
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000EA0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0x0 RW	**MAX_ABRST:** Maximum AMBA Burst Length. Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**LOCK_B:** Bus Lock Bit. When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0x0 RW	**LOCK_CH:** Channel Lock Bit. When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0x0 RW	**LOCK_B_L:** Bus Lock Level. Indicates the duration over which CFGx.LOCK_B bit applies. 00 = Over complete DMA transfer 01 = Over complete DMA block transfer 1x = Over complete DMA transaction
13:12	0x0 RW	**LOCK_CH_L:** Channel Lock Level. Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	0x1 RW	**HS_SEL_SRC:** Source Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
10	0x1 RW	**HS_SEL_DST:** Destination Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA transfers from source until this bit is cleared.
7:5	0x5 RW	**CH_PRIOR:** Channel priority. Priority of 7 is the highest priority.
4:0	0x0 RW	**Undefined:** RESERVED

9.2.80 Configuration register for Channel 5 - HIGH (CFG5_HI)—Offset 1FCh

Configuration register for Channel 5 _ HIGH

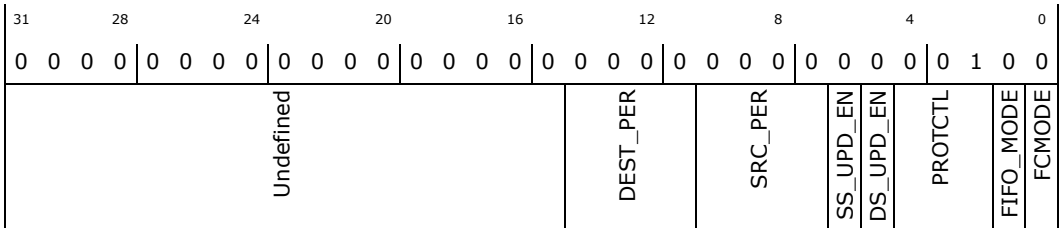
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RW	**Undefined:** Reserved
14:11	0x0 RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0x0 RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	0x1 RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0x0 RW	**FIFO_MODE:** FIFO Mode Select. Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0 = Space/data available for single AHB transfer of the specified transfer width. 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0x0 RW	**FCMODE:** Flow Control Mode. Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. 1 = Source transaction requests are not serviced until a destination transaction request occurs.

9.2.81 Source Gather Register for Channel 5 - LOW (SGR5_LO)—Offset 200h

Source Gather Register for Channel 5

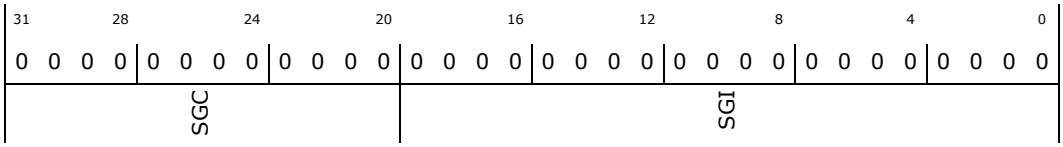
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 200h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval

9.2.82 Source Gather Register for Channel 5 - HIGH (SGR5_HI)—Offset 204h

Source Gather Register for Channel 5

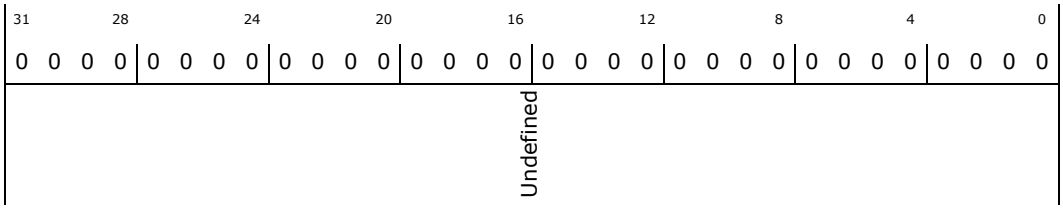
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 204h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.83 Destination Scatter Register for Channel 5 - LOW (DSR5_LO)—Offset 208h

Destination Scatter Register for Channel 5

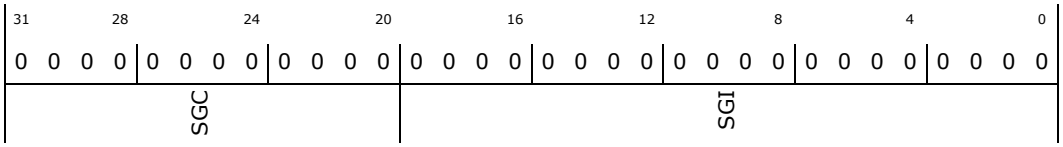
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 208h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC (SGC):** Dest scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI (SGI):** Dest scatter interval

9.2.84 Dest scatter Register for Channel 5 - HIGH (DSR5_HI)—Offset 20Ch

Dest scatter Register for Channel 5

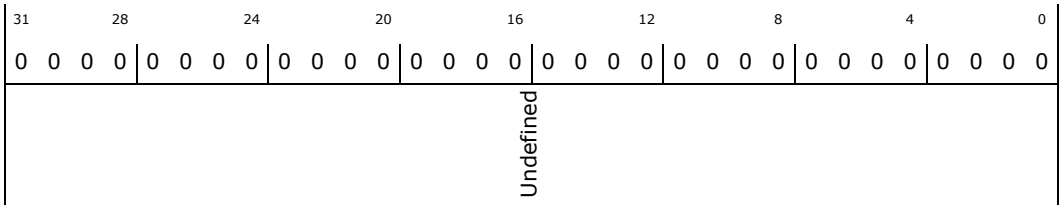
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 20Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.85 Source Address Register for Channel 6 - LOW (SAR6_LO)—Offset 210h

Source Address Register for Channel 6

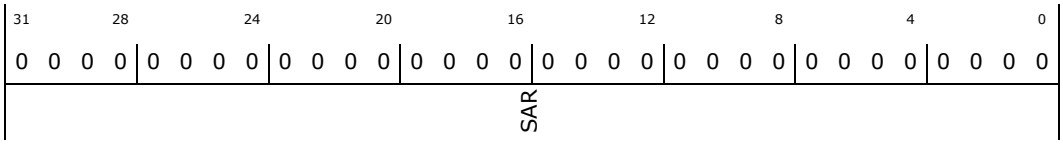
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 210h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

9.2.86 Source Address Register for Channel 6 - HIGH (SAR6_HI)—Offset 214h

Source Address Register for Channel 6

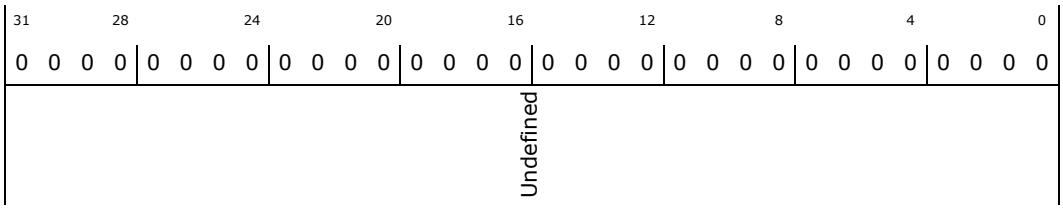
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 214h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.2.87 Destination Address Register for Channel 6 - LOW (DAR6_LO)—Offset 218h

Destination Address Register for Channel 6

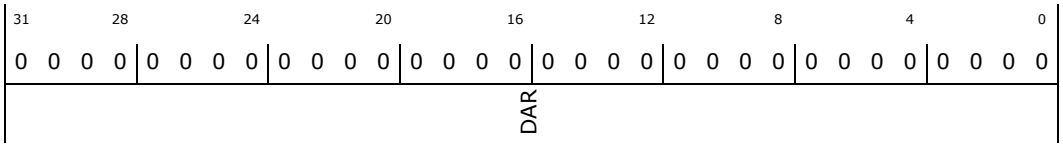
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 218h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

9.2.88 Destination Address Register for Channel 6 - HIGH (DAR6_HI)—Offset 21Ch

Destination Address Register for Channel 6

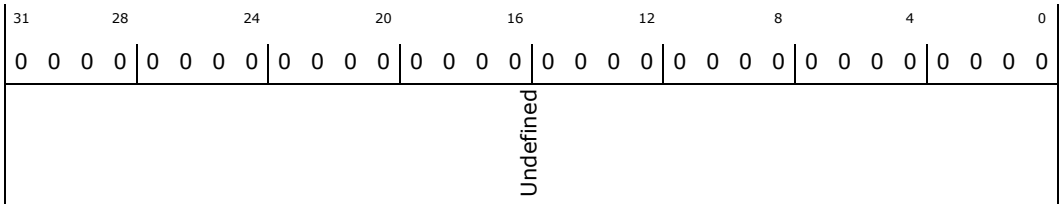
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 21Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.89 Linked List Pointer Register for Channel 6 - LOW (LLP6_LO)—Offset 220h

Linked List Pointer Register for Channel 6

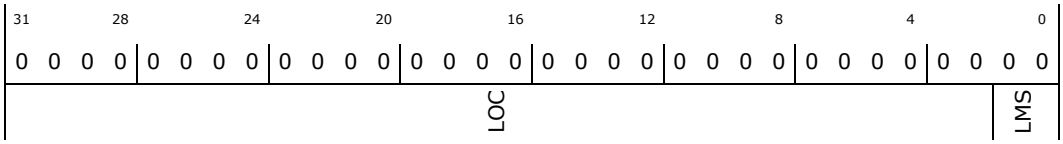
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 220h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0x0 RW	**LMS:** List Master Select. Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

9.2.90 Linked List Pointer Register for Channel 6 - HIGH (LLP6_HI)—Offset 224h

Linked List Pointer Register for Channel 6

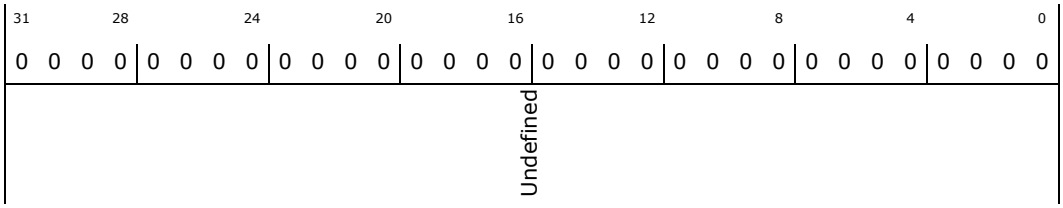
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 224h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.2.91 Control Register for Channel 6 - LOW (CTL6_LO)—Offset 228h

Control Register for Channel 6

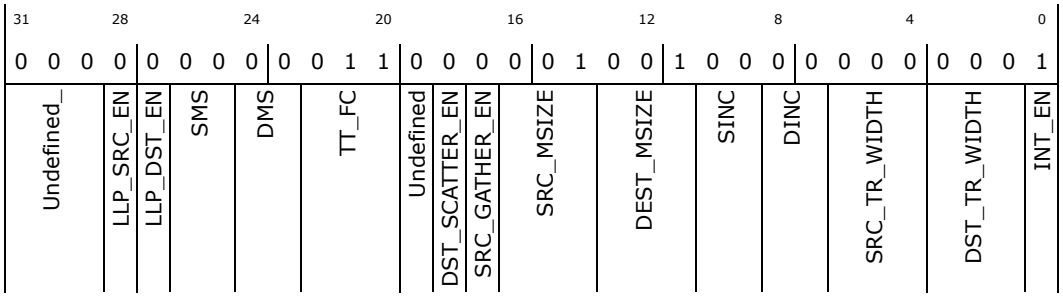
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 228h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**Undefined_:** RESERVED
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0x0 RW	**SMS:** Source Master Select. Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0x0 RW	**DMS:** Destination Master Select. Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	0x3 RW	**TT_FC:** Transfer Type and Flow Control.
19	0x0 RW	**Undefined:** RESERVED
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit. 0 = disabled 1 = enabled
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit. 0 = disabled 1 = enabled
16:14	0x1 RW	**SRC_MSIZE:** Source Burst Transaction Length.
13:11	0x1 RW	**DEST_MSIZE:** Destination Burst Transaction Length.
10:9	0x0 RW	**SINC:** Source Address Increment. 00 = Increment 01 = Decrement 1x = No change
8:7	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. 00 = Increment 01 = Decrement 1x = No change
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.

Bit Range	Default & Access	Field Name (ID): Description
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	0x1 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

9.2.92 Control Register for Channel 6 - HIGH (CTL6_HI)—Offset 22Ch

Control Register for Channel 6

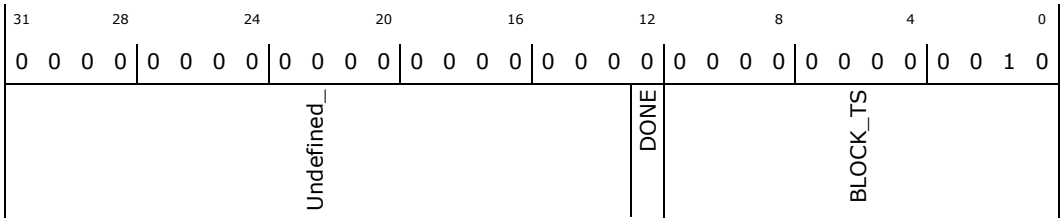
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 22Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Undefined_:** RESERVED
12	0x0 RW	**DONE:** Done bit
11:0	0x2 RW	**BLOCK_TS:** Block Transfer Size. When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

9.2.93 Configuration register for Channel 6 - LOW (CFG6_LO)—Offset 250h

Configuration register for Channel 6

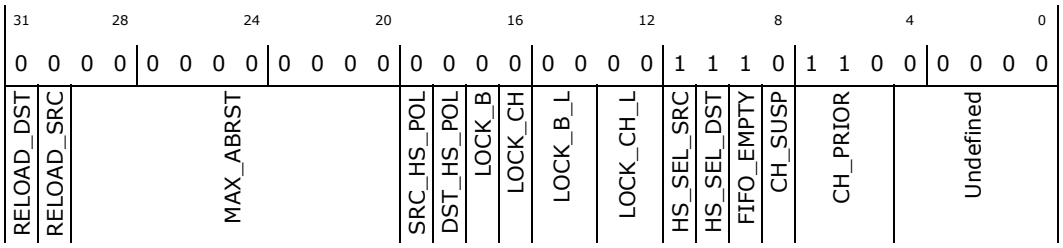
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 250h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000EC0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0x0 RW	**MAX_ABRST:** Maximum AMBA Burst Length. Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**LOCK_B:** Bus Lock Bit. When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0x0 RW	**LOCK_CH:** Channel Lock Bit. When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0x0 RW	**LOCK_B_L:** Bus Lock Level. Indicates the duration over which CFGx.LOCK_B bit applies. 00 = Over complete DMA transfer 01 = Over complete DMA block transfer 1x = Over complete DMA transaction
13:12	0x0 RW	**LOCK_CH_L:** Channel Lock Level. Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	0x1 RW	**HS_SEL_SRC:** Source Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
10	0x1 RW	**HS_SEL_DST:** Destination Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA transfers from source until this bit is cleared.
7:5	0x6 RW	**CH_PRIOR:** Channel priority. Priority of 7 is the highest priority.

Bit Range	Default & Access	Field Name (ID): Description
4:0	0x0 RW	**Undefined:** RESERVED

9.2.94 Configuration register for Channel 6 - HIGH (CFG6_HI)—Offset 254h

Configuration register for Channel 6 _ HIGH

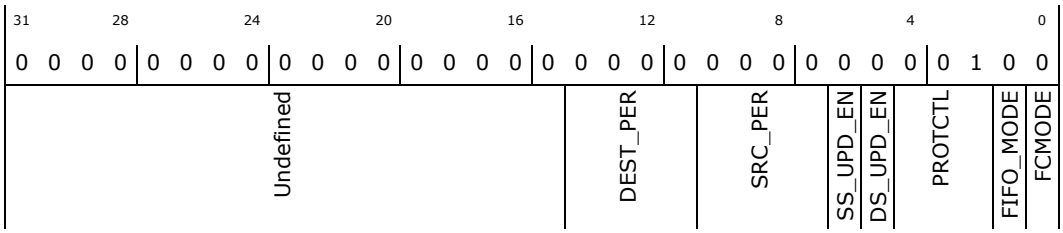
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 254h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RW	**Undefined:** Reserved
14:11	0x0 RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0x0 RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	0x1 RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**FIFO_MODE:** FIFO Mode Select. Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0 = Space/data available for single AHB transfer of the specified transfer width. 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0x0 RW	**FCMODE:** Flow Control Mode. Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. 1 = Source transaction requests are not serviced until a destination transaction request occurs.

9.2.95 Source Gather Register for Channel 6 - LOW (SGR6_LO)—Offset 258h

Source Gather Register for Channel 6

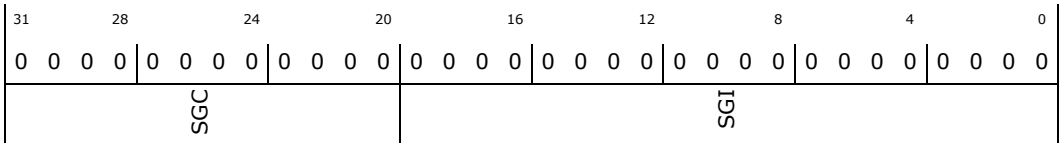
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 258h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval

9.2.96 Source Gather Register for Channel 6 - HIGH (SGR6_HI)—Offset 25Ch

Source Gather Register for Channel 6

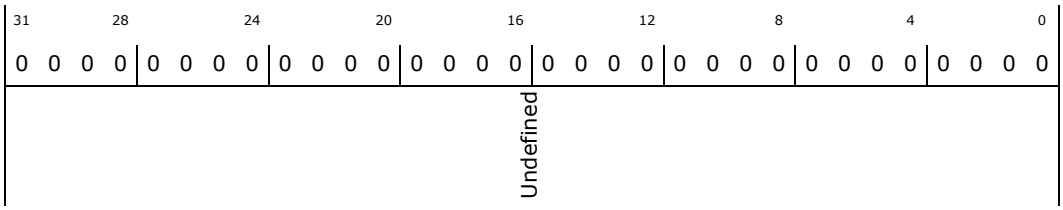
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 25Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.97 Destination Scatter Register for Channel 6 - LOW (DSR6_LO)—Offset 260h

Destination Scatter Register for Channel 6

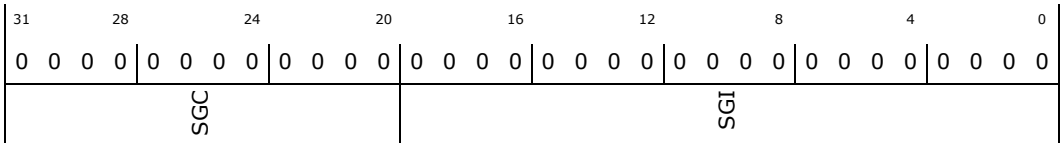
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 260h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC (SGC):** Dest scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI (SGI):** Dest scatter interval

9.2.98 Dest scatter Register for Channel 6 - HIGH (DSR6_HI)—Offset 264h

Dest scatter Register for Channel 6

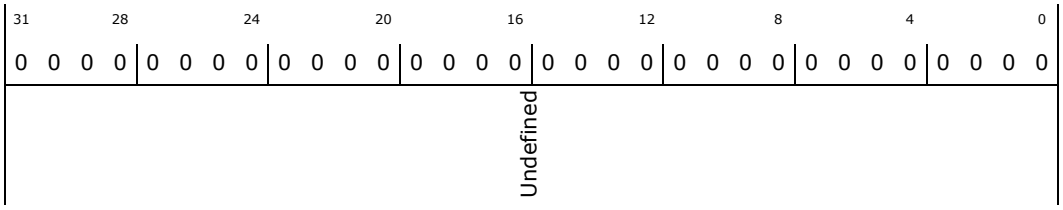
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 264h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.99 Source Address Register for Channel 7 - LOW (SAR7_LO)—Offset 268h

Source Address Register for Channel 7

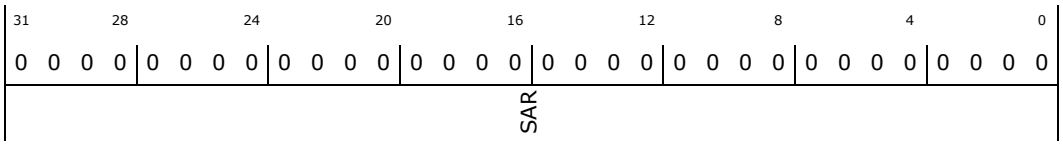
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 268h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

9.2.100 Source Address Register for Channel 7 - HIGH (SAR7_HI)—Offset 26Ch

Source Address Register for Channel 7

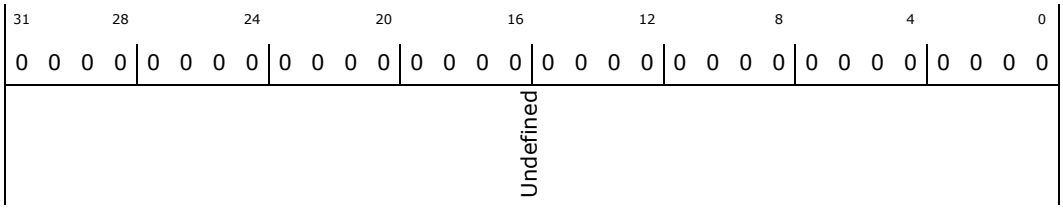
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 26Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.2.101 Destination Address Register for Channel 7 - LOW (DAR7_LO)—Offset 270h

Destination Address Register for Channel 7

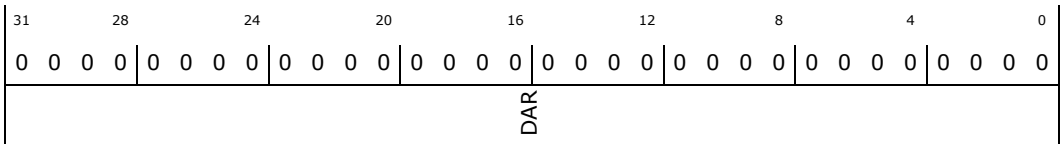
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 270h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

9.2.102 Destination Address Register for Channel 7 - HIGH (DAR7_HI)—Offset 274h

Destination Address Register for Channel 7

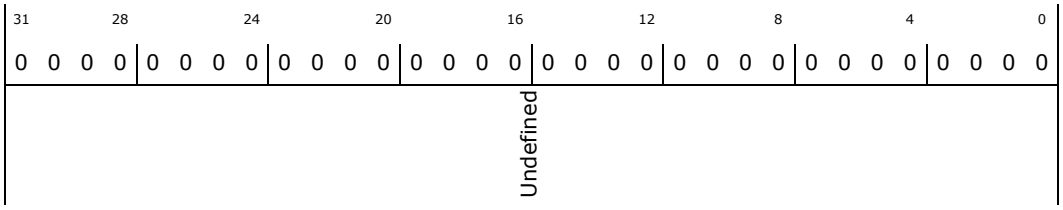
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 274h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.103 Linked List Pointer Register for Channel 7 - LOW (LLP7_LO)—Offset 278h

Linked List Pointer Register for Channel 7

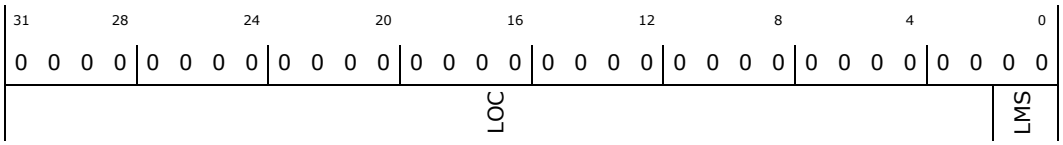
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 278h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0x0 RW	**LMS:** List Master Select. Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

9.2.104 Linked List Pointer Register for Channel 7 - HIGH (LLP7_HI)—Offset 27Ch

Linked List Pointer Register for Channel 7

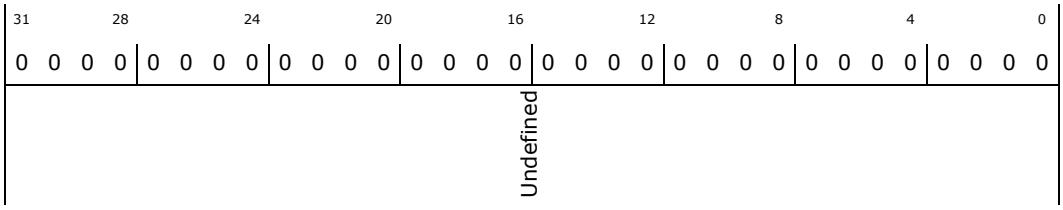
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 27Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.2.105 Control Register for Channel 7 - LOW (CTL7_LO)—Offset 280h

Control Register for Channel 7

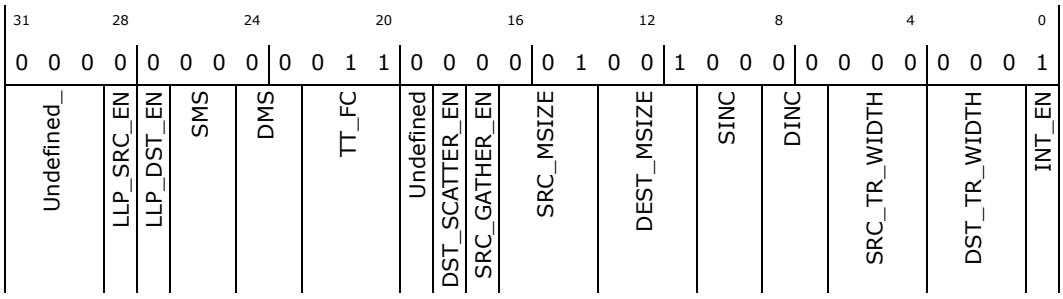
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 280h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**Undefined_:** RESERVED
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0x0 RW	**SMS:** Source Master Select. Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0x0 RW	**DMS:** Destination Master Select. Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	0x3 RW	**TT_FC:** Transfer Type and Flow Control.

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RW	**Undefined:** RESERVED
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit. 0 = disabled 1 = enabled
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit. 0 = disabled 1 = enabled
16:14	0x1 RW	**SRC_MSIZE:** Source Burst Transaction Length.
13:11	0x1 RW	**DEST_MSIZE:** Destination Burst Transaction Length.
10:9	0x0 RW	**SINC:** Source Address Increment. 00 = Increment 01 = Decrement 1x = No change
8:7	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. 00 = Increment 01 = Decrement 1x = No change
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	0x1 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

9.2.106 Control Register for Channel 7 - HIGH (CTL7_HI)—Offset 284h

Control Register for Channel 7

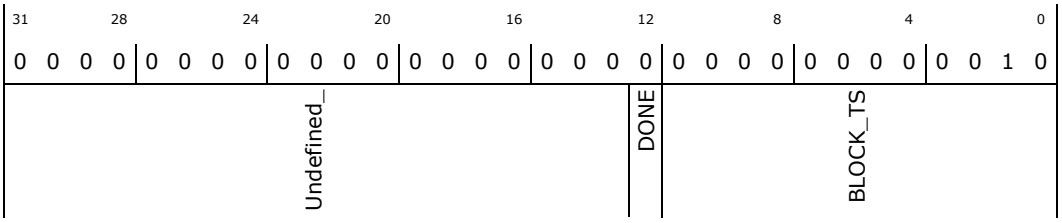
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 284h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Undefined_:** RESERVED
12	0x0 RW	**DONE:** Done bit
11:0	0x2 RW	**BLOCK_TS:** Block Transfer Size. When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

9.2.107 Configuration register for Channel 7 - LOW (CFG7_LO)—Offset 2A8h

Configuration register for Channel 7

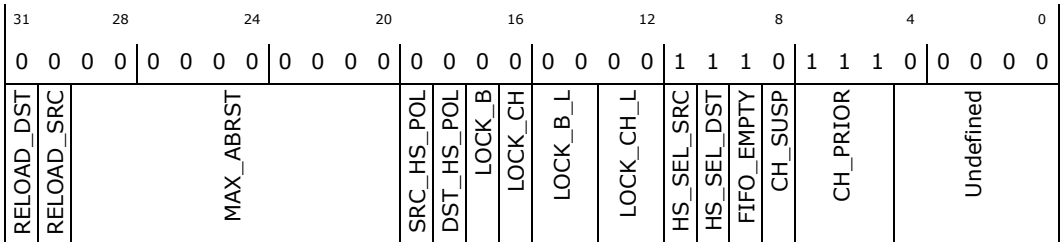
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000EE0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0x0 RW	**MAX_ABRST:** Maximum AMBA Burst Length. Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**LOCK_B:** Bus Lock Bit. When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW	**LOCK_CH:** Channel Lock Bit. When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0x0 RW	**LOCK_B_L:** Bus Lock Level. Indicates the duration over which CFGx.LOCK_B bit applies. 00 = Over complete DMA transfer 01 = Over complete DMA block transfer 1x = Over complete DMA transaction
13:12	0x0 RW	**LOCK_CH_L:** Channel Lock Level. Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	0x1 RW	**HS_SEL_SRC:** Source Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
10	0x1 RW	**HS_SEL_DST:** Destination Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA transfers from source until this bit is cleared.
7:5	0x7 RW	**CH_PRIOR:** Channel priority. Priority of 7 is the highest priority.
4:0	0x0 RW	**Undefined:** RESERVED

9.2.108 Configuration register for Channel 7 - HIGH (CFG7_HI)—Offset 2ACh

Configuration register for Channel 7 _ HIGH

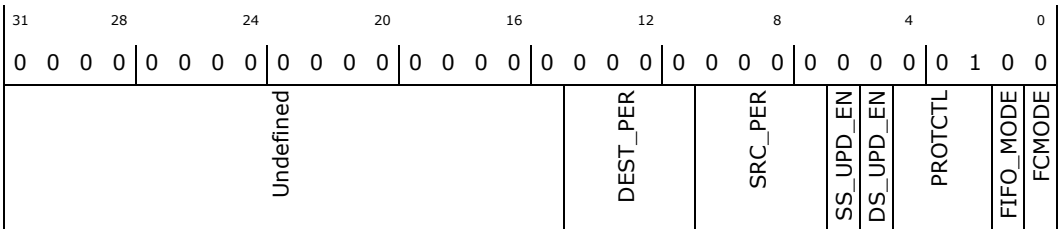
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RW	**Undefined:** Reserved
14:11	0x0 RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0x0 RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	0x1 RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0x0 RW	**FIFO_MODE:** FIFO Mode Select. Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0 = Space/data available for single AHB transfer of the specified transfer width. 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0x0 RW	**FCMODE:** Flow Control Mode. Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. 1 = Source transaction requests are not serviced until a destination transaction request occurs.

9.2.109 Source Gather Register for Channel 7 - LOW (SGR7_LO)—Offset 2B0h

Source Gather Register for Channel 7

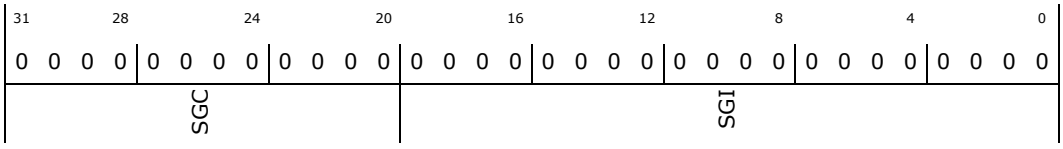
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval

9.2.110 Source Gather Register for Channel 7 - HIGH (SGR7_HI)—Offset 2B4h

Source Gather Register for Channel 7

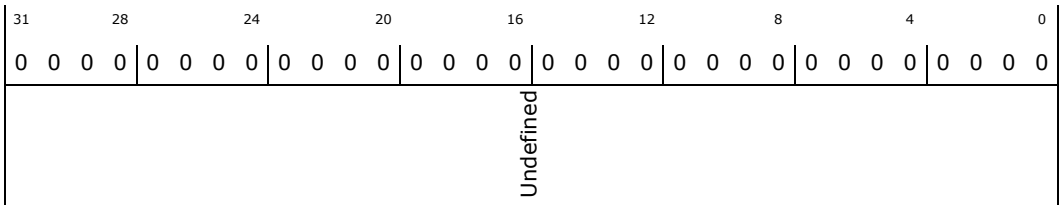
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.111 Destination Scatter Register for Channel 7 - LOW (DSR7_LO)—Offset 2B8h

Destination Scatter Register for Channel 7

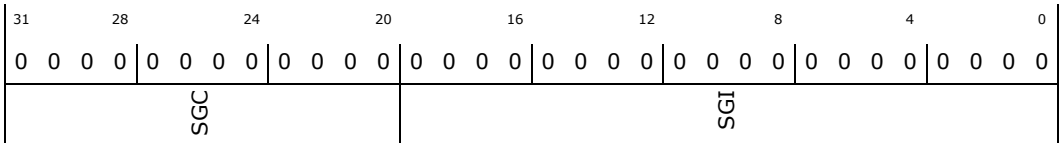
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC (SGC):** Dest scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI (SGI):** Dest scatter interval

9.2.112 Dest scatter Register for Channel 7 - HIGH (DSR7_HI)—Offset 2BCh

Dest scatter Register for Channel 7

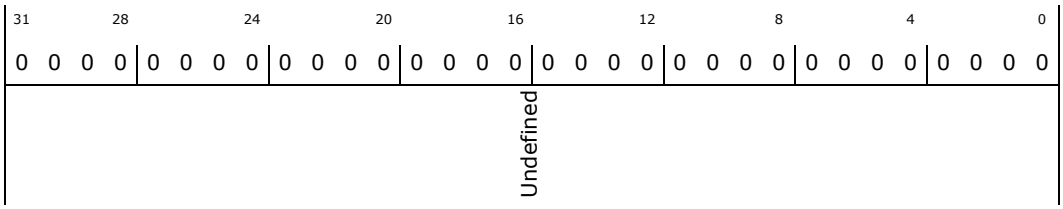
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.113 RawTfr Interrupt Raw Status Registers - LOW (RawTfr_LO)—Offset 2C0h

RawTfr Interrupt Raw Status Registers

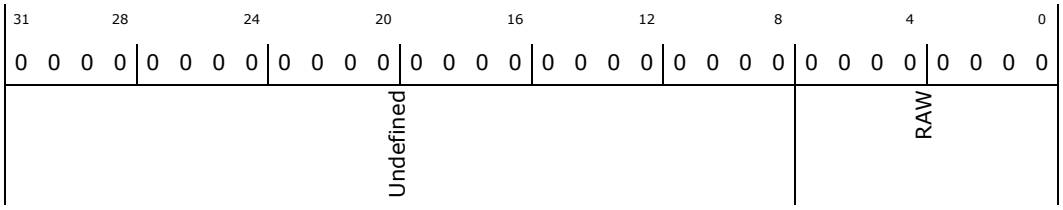
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RW	**RAW:** Raw interrupt status

9.2.114 RawTfr Interrupt Raw Status Registers - HIGH (RawTfr_HI)—Offset 2C4h

RawTfr Interrupt Raw Status Registers

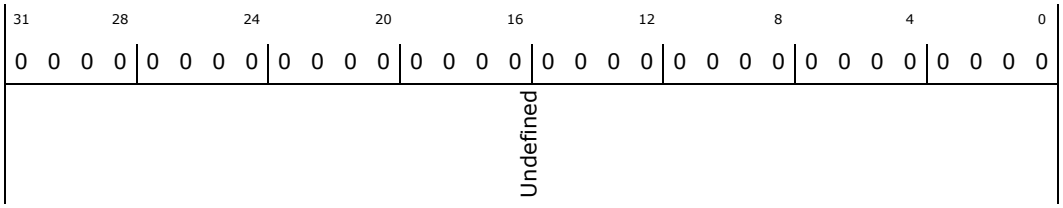
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.115 RawBlock Interrupt Raw Status Registers - LOW (RawBlock_LO)—Offset 2C8h

RawBlock Interrupt Raw Status Registers

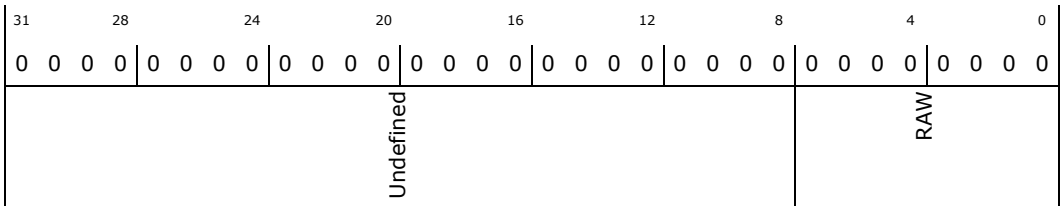
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RW	**RAW:** Raw interrupt status

9.2.116 RawBlock Interrupt Raw Status Registers - HIGH (RawBlock_HI)—Offset 2CCh

RawBlock Interrupt Raw Status Registers

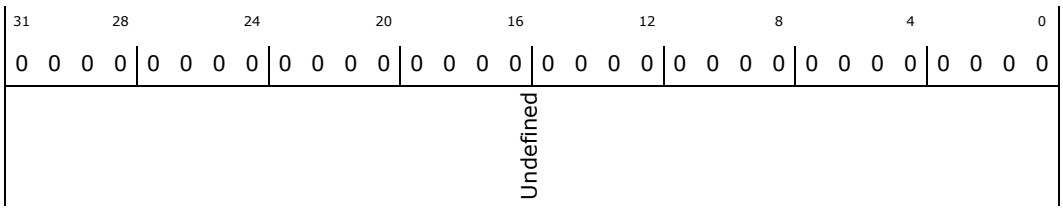
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.117 RawSrcTran Interrupt Raw Status Registers - LOW (RawSrcTran_LO)—Offset 2D0h

RawSrcTran Interrupt Raw Status Registers

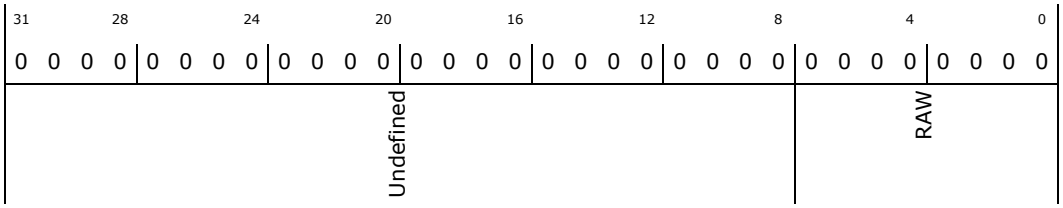
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RW	**RAW:** Raw interrupt status

9.2.118 RawSrcTran Interrupt Raw Status Registers - HIGH (RawSrcTran_HI)—Offset 2D4h

RawSrcTran Interrupt Raw Status Registers

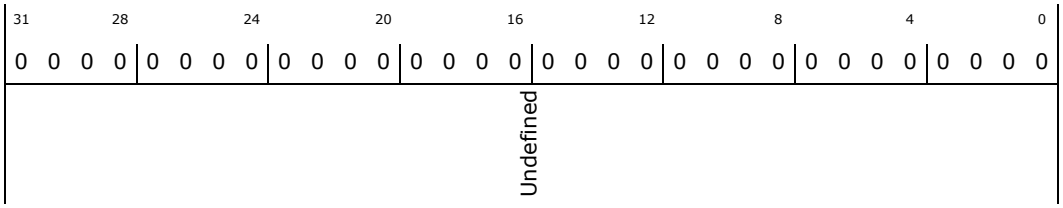
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.119 RawDstTran Interrupt Raw Status Registers - LOW (RawDstTran_LO)—Offset 2D8h

RawDstTran Interrupt Raw Status Registers

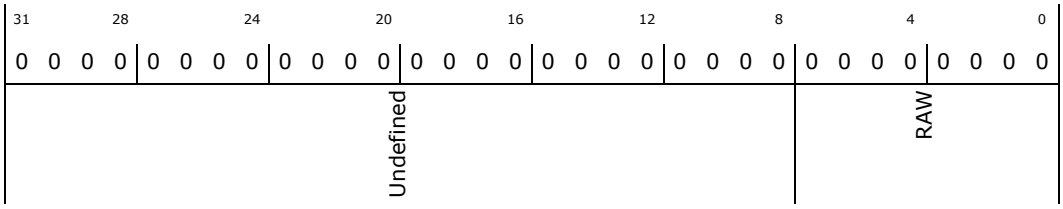
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RW	**RAW:** Raw interrupt status

9.2.120 RawDstTran Interrupt Raw Status Registers - HIGH (RawDstTran_HI)—Offset 2DCh

RawDstTran Interrupt Raw Status Registers

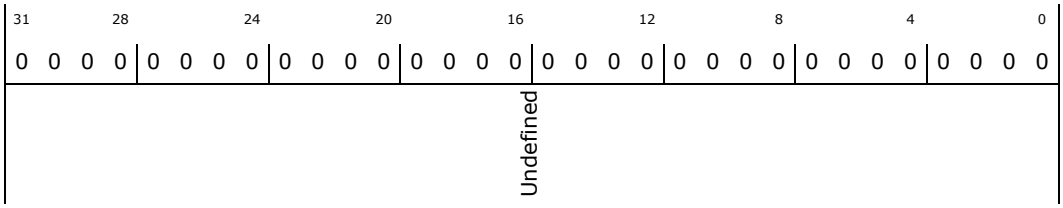
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.121 RawErr Interrupt Raw Status Registers - LOW (RawErr_LO)—Offset 2E0h

RawErr Interrupt Raw Status Registers

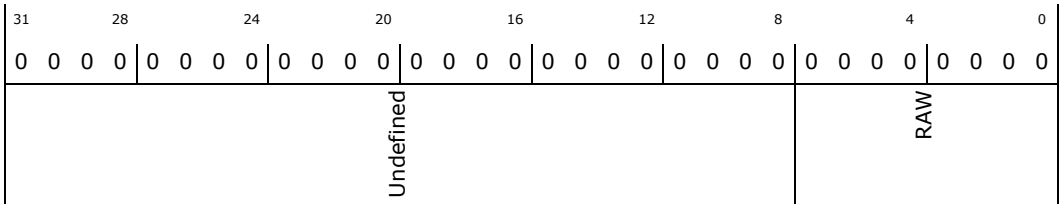
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RW	**RAW:** Raw interrupt status

9.2.122 RawErr Interrupt Raw Status Registers - HIGH (RawErr_HI)—Offset 2E4h

RawErr Interrupt Raw Status Registers

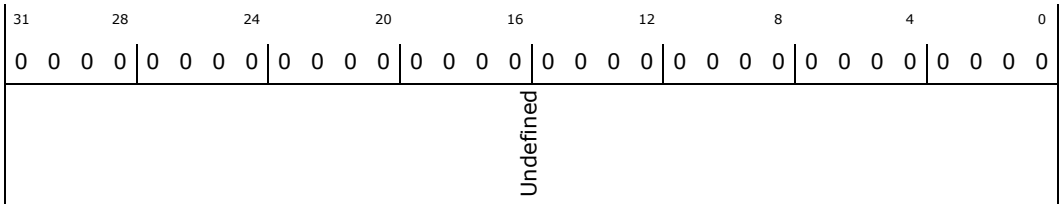
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.123 StatusTfr Interrupt Status Registers - LOW (StatusTfr_LO)—Offset 2E8h

StatusTfr Interrupt Status Registers

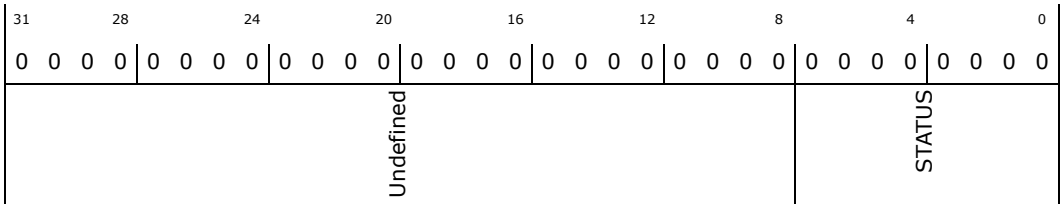
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RO	**STATUS:** Status interrupt status

9.2.124 StatusTfr Interrupt Status Registers - HIGH (StatusTfr_HI)—Offset 2ECh

StatusTfr Interrupt Status Registers

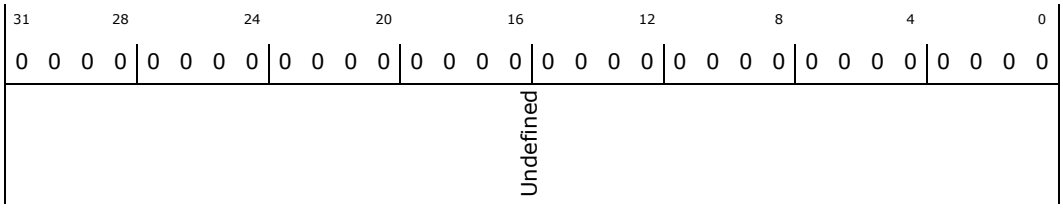
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.125 StatusBlock Interrupt Status Registers - LOW (StatusBlock_LO)—Offset 2F0h

StatusBlock Interrupt Status Registers

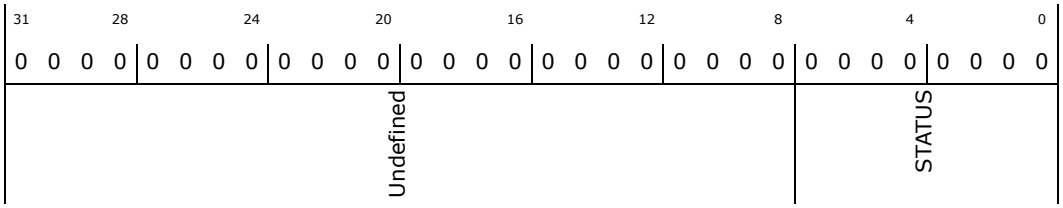
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RO	**STATUS:** Status interrupt status

9.2.126 StatusBlock Interrupt Status Registers - HIGH (StatusBlock_HI)—Offset 2F4h

StatusBlock Interrupt Status Registers

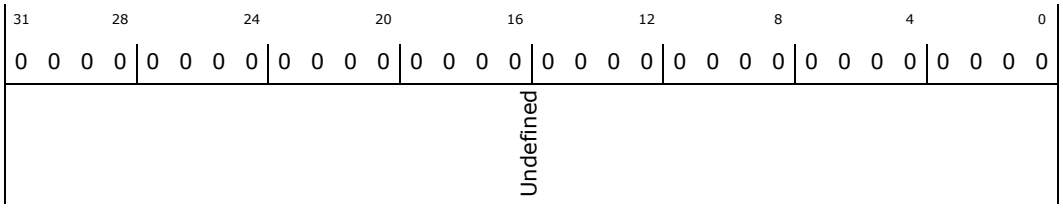
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.127 StatusSrcTran Interrupt Status Registers - LOW (StatusSrcTran_LO)—Offset 2F8h

StatusSrcTran Interrupt Status Registers

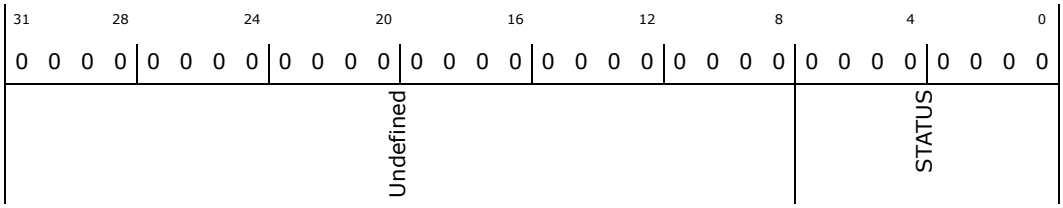
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RO	**STATUS:** Status interrupt status

9.2.128 StatusSrcTran Interrupt Status Registers - HIGH (StatusSrcTran_HI)—Offset 2FCh

StatusSrcTran Interrupt Status Registers

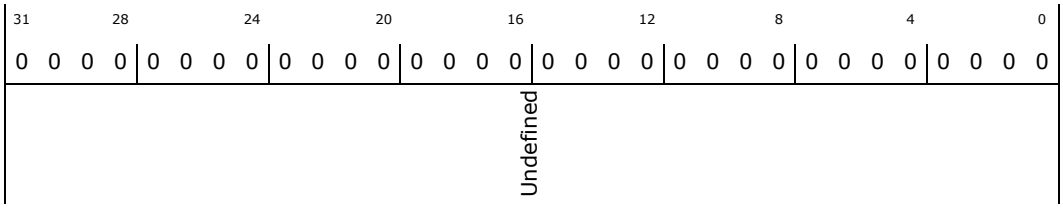
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.129 StatusDstTran Interrupt Status Registers - LOW (StatusDstTran_LO)—Offset 300h

StatusDstTran Interrupt Status Registers

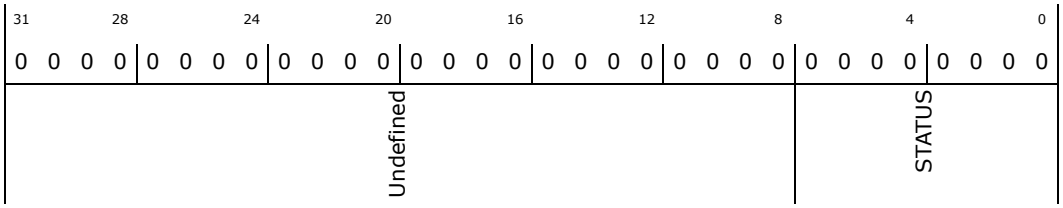
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 300h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RO	**STATUS:** Status interrupt status

9.2.130 StatusDstTran Interrupt Status Registers - HIGH (StatusDstTran_HI)—Offset 304h

StatusDstTran Interrupt Status Registers

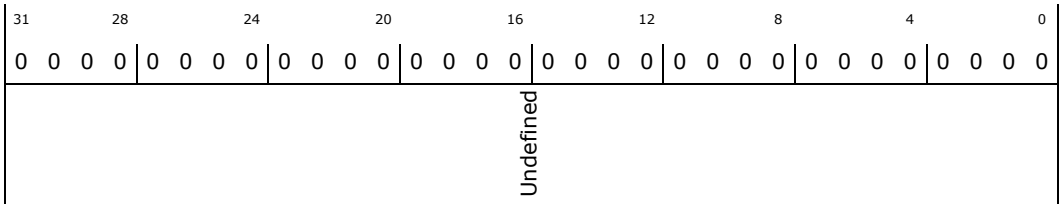
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 304h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.131 StatusErr Interrupt Status Registers - LOW (StatusErr_LO)—Offset 308h

StatusErr Interrupt Status Registers

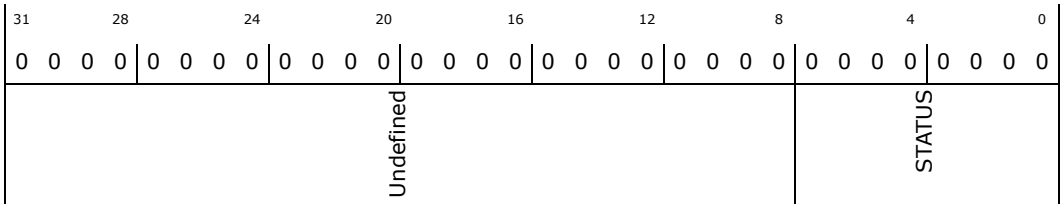
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 308h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RO	**STATUS:** Status interrupt status

9.2.132 StatusErr Interrupt Status Registers - HIGH (StatusErr_HI)—Offset 30Ch

StatusErr Interrupt Status Registers

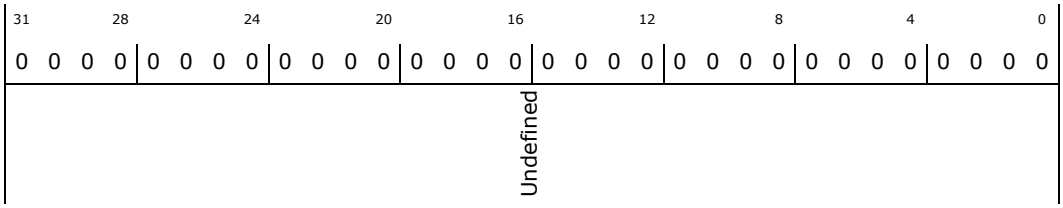
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.133 MaskTfr Interrupt Mask Registers - LOW (MaskTfr_LO)—Offset 310h

MaskTfr Interrupt Mask Registers

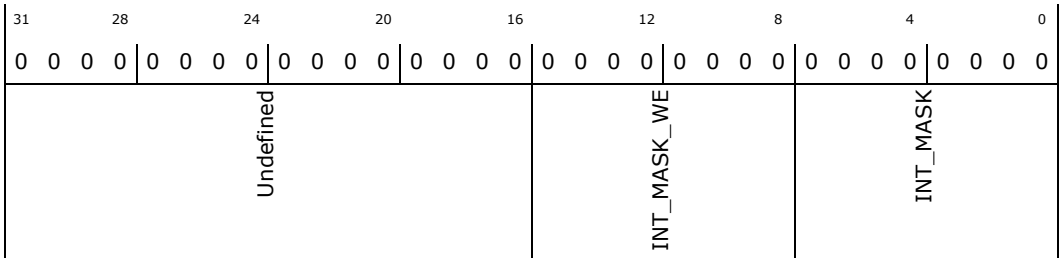
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 310h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 RW	**INT_MASK_WE:** Interrupt Mask Write Enable 0=write disabled 1=write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt Mask 0=masked 1=unmasked

9.2.134 MaskTfr Interrupt Mask Registers - HIGH (MaskTfr_HI)—Offset 314h

MaskTfr Interrupt Mask Registers

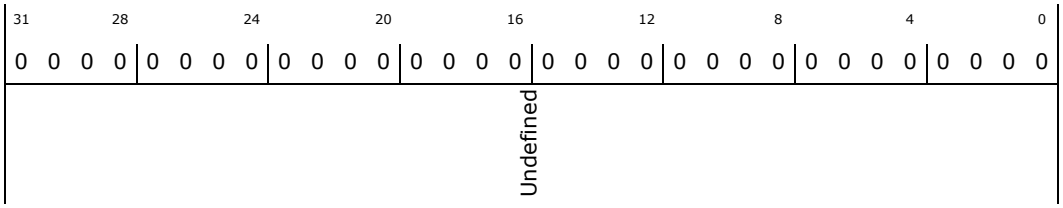
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 314h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.135 MaskBlock Interrupt Mask Registers - LOW (MaskBlock_LO)—Offset 318h

MaskBlock Interrupt Mask Registers

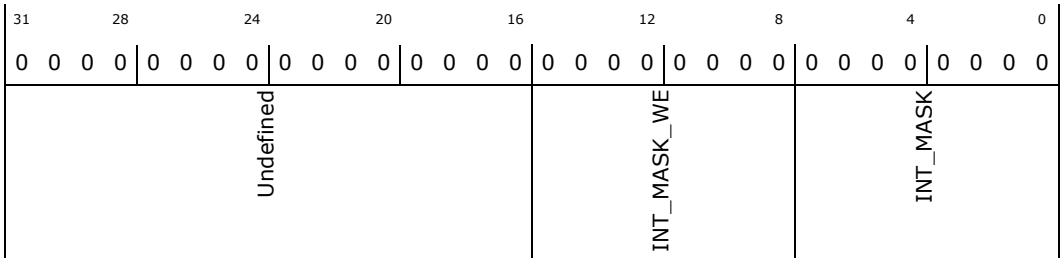
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 318h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0=write disabled 1=write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt Mask 0=masked 1=unmasked

9.2.136 MaskBlock Interrupt Mask Registers - HIGH (MaskBlock_HI)—Offset 31Ch

MaskBlock Interrupt Mask Registers

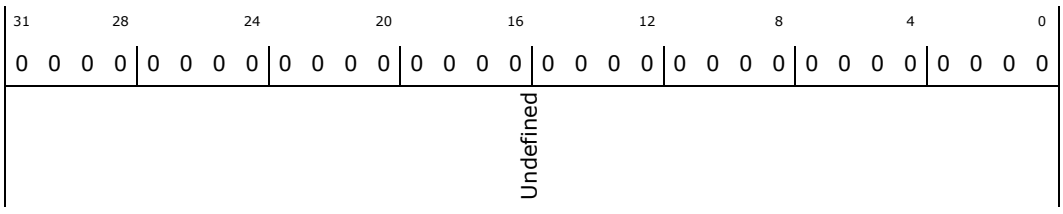
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 31Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.137 MaskSrcTran Interrupt Mask Registers - LOW (MaskSrcTran_LO)—Offset 320h

MaskSrcTran Interrupt Mask Registers

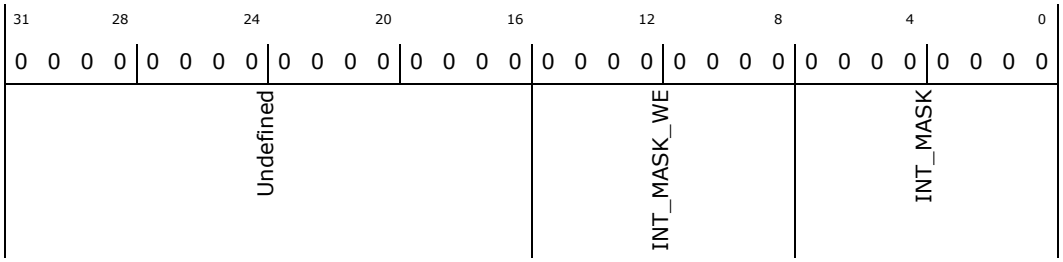
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 320h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0=write disabled 1=write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt Mask 0=masked 1=unmasked

9.2.138 MaskSrcTran Interrupt Mask Registers - HIGH (MaskSrcTran_HI)—Offset 324h

MaskSrcTran Interrupt Mask Registers

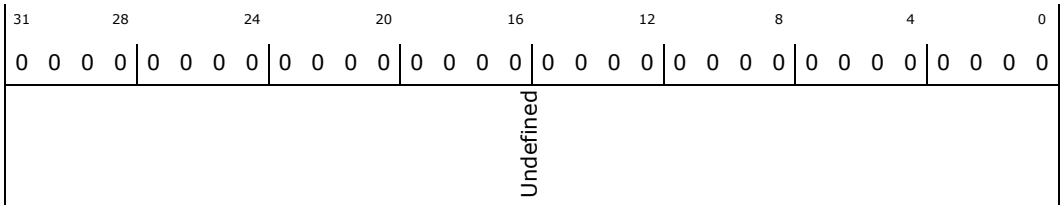
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 324h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.139 MaskDstTran Interrupt Mask Registers - LOW (MaskDstTran_LO)—Offset 328h

MaskDstTran Interrupt Mask Registers

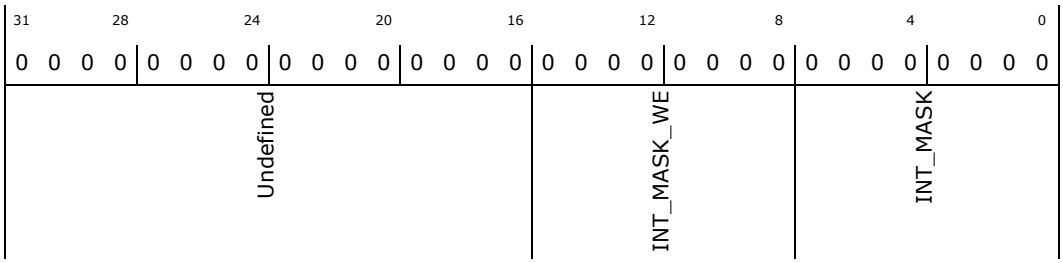
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 328h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0=write disabled 1=write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt Mask 0=masked 1=unmasked

9.2.140 MaskDstTran Interrupt Mask Registers - HIGH (MaskDstTran_HI)—Offset 32Ch

MaskDstTran Interrupt Mask Registers

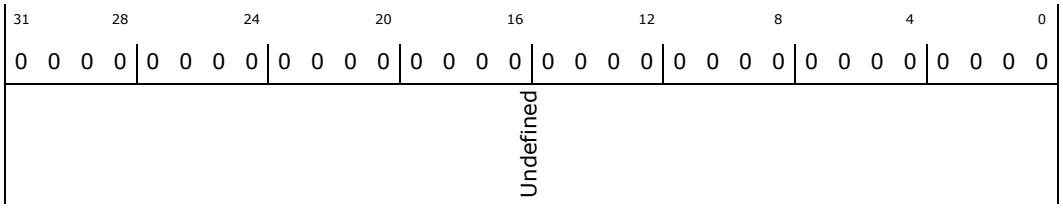
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 32Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.141 MaskErr Interrupt Mask Registers - LOW (MaskErr_LO)—Offset 330h

MaskErr Interrupt Mask Registers

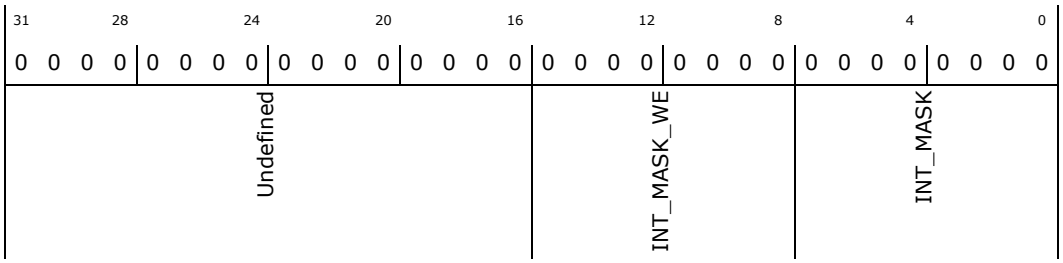
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 330h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0=write disabled 1=write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt Mask 0=masked 1=unmasked

9.2.142 MaskErr Interrupt Mask Registers - HIGH (MaskErr_HI)—Offset 334h

MaskErr Interrupt Mask Registers

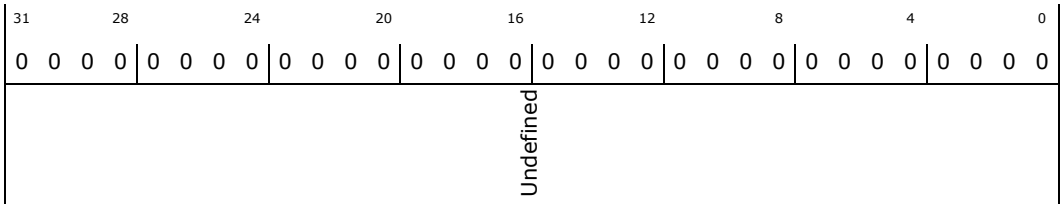
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 334h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.143 ClearTfr Interrupt Clear Registers - LOW (ClearTfr_LO)—Offset 338h

ClearTfr Interrupt Clear Registers

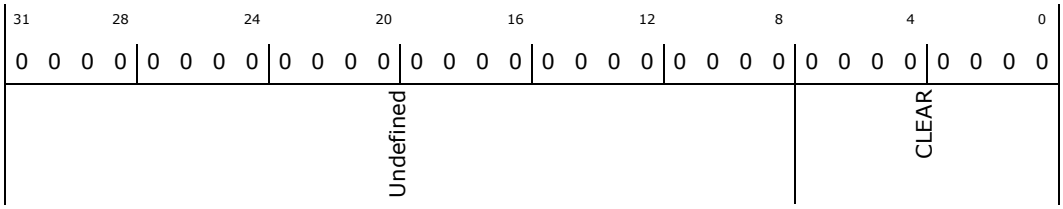
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 338h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 WO	**CLEAR:** Clear interrupt status

9.2.144 ClearTfr Interrupt Clear Registers - HIGH (ClearTfr_HI)—Offset 33Ch

ClearTfr Interrupt Clear Registers

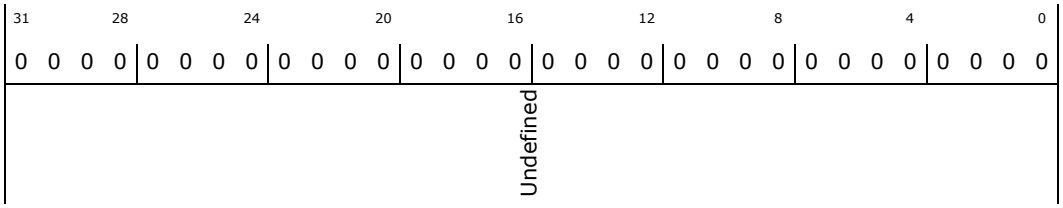
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 33Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.145 ClearBlock Interrupt Clear Registers - LOW (ClearBlock_LO)—Offset 340h

ClearBlock Interrupt Clear Registers

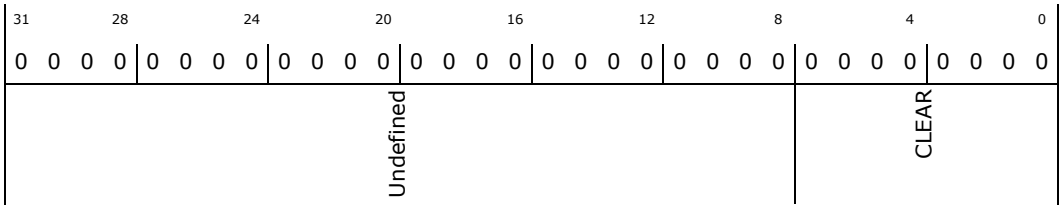
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 340h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 WO	**CLEAR:** Clear interrupt status

9.2.146 ClearBlock Interrupt Clear Registers - HIGH (ClearBlock_HI)—Offset 344h

ClearBlock Interrupt Clear Registers

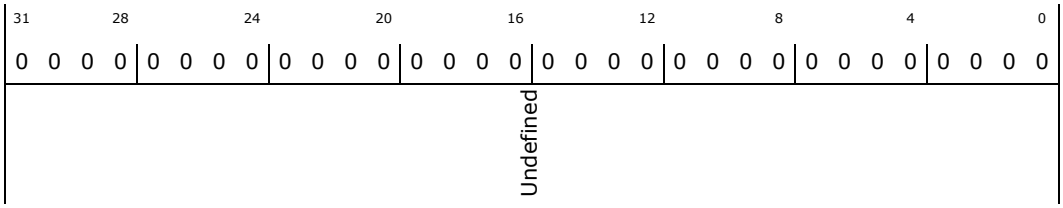
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 344h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.147 ClearSrcTran Interrupt Clear Registers - LOW (ClearSrcTran_LO)—Offset 348h

ClearSrcTran Interrupt Clear Registers

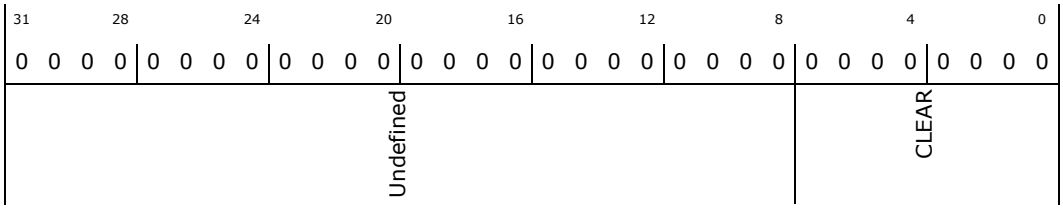
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 348h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 WO	**CLEAR:** Clear interrupt status

9.2.148 ClearSrcTran Interrupt Clear Registers - HIGH (ClearSrcTran_HI)—Offset 34Ch

ClearSrcTran Interrupt Clear Registers

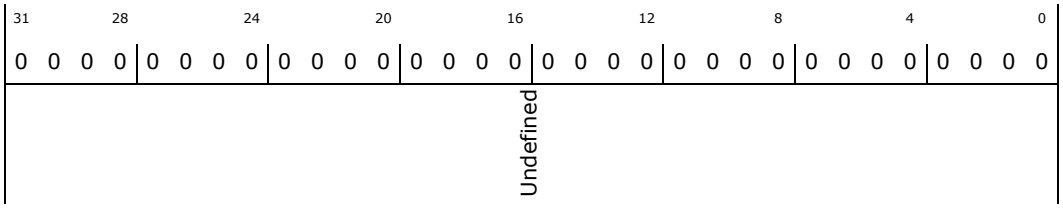
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.149 ClearDstTran Interrupt Clear Registers - LOW (ClearDstTran_LO)—Offset 350h

ClearDstTran Interrupt Clear Registers

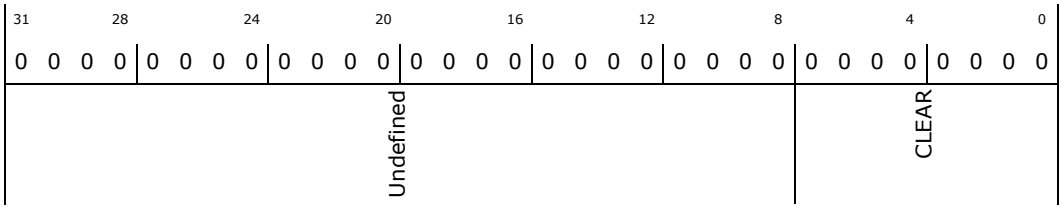
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 350h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 WO	**CLEAR:** Clear interrupt status

9.2.150 ClearDstTran Interrupt Clear Registers - HIGH (ClearDstTran_HI)—Offset 354h

ClearDstTran Interrupt Clear Registers

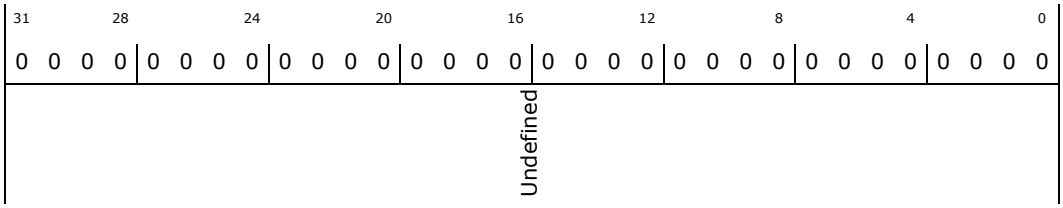
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 354h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.151 ClearErr Interrupt Clear Registers - LOW (ClearErr_LO)—Offset 358h

ClearErr Interrupt Clear Registers

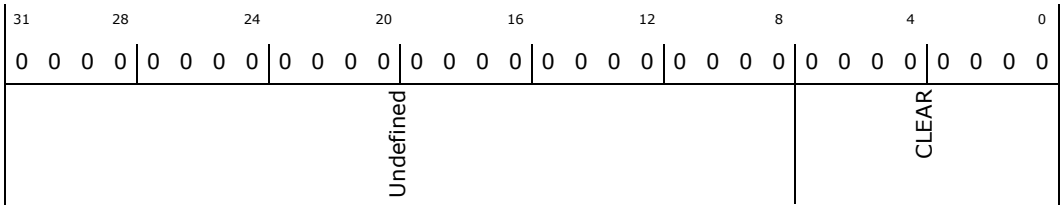
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 358h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 WO	**CLEAR:** Clear interrupt status

9.2.152 ClearErr Interrupt Clear Registers - HIGH (ClearErr_HI)—Offset 35Ch

ClearErr Interrupt Clear Registers

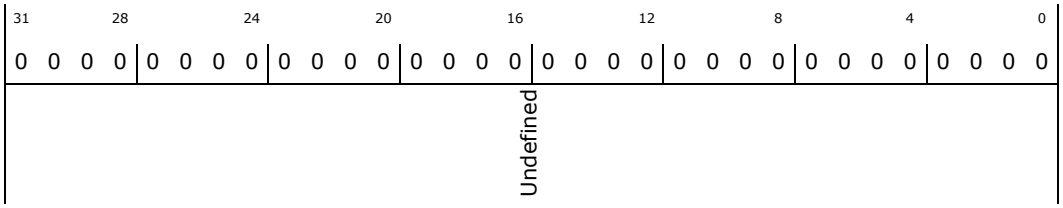
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 35Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.153 Combined Interrupt Status Register - LOW (StatusInt_LO)—Offset 360h

Combined Interrupt Status Register

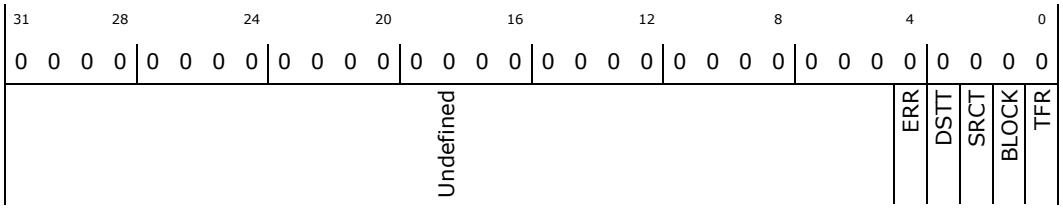
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 360h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RW	**Undefined:** Reserved
4	0x0 RO	**ERR:** OR of the contents of StatusErr register.

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RO	**DSTT:** OR of the contents of StatusDst register.
2	0x0 RO	**SRCT:** OR of the contents of StatusSrcTran register.
1	0x0 RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0x0 RO	**TFR:** OR of the contents of StatusTfr register.

9.2.154 Combined Interrupt Status Register - HIGH (StatusInt_HI)—Offset 364h

Combined Interrupt Status Register

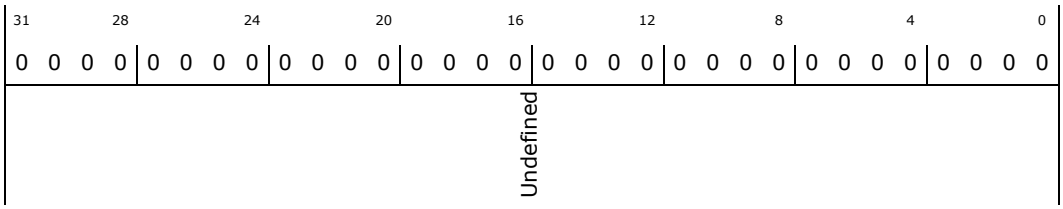
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 364h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.155 Source Software Transaction Request Register - LOW (ReqSrcReg_LO)—Offset 368h

Source Software Transaction Request Register

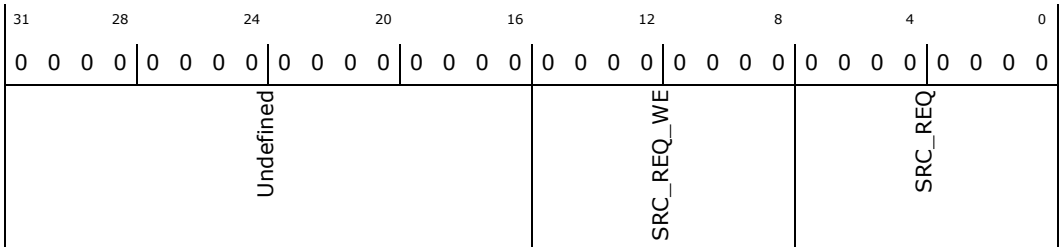
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 368h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**SRC_REQ_WE:** Source req write enable 0=write disabled 1=write enabled
7:0	0x0 RW	**SRC_REQ:** Source request

9.2.156 Source Software Transaction Request Register - HIGH (ReqSrcReg_HI)—Offset 36Ch

Source Software Transaction Request Register

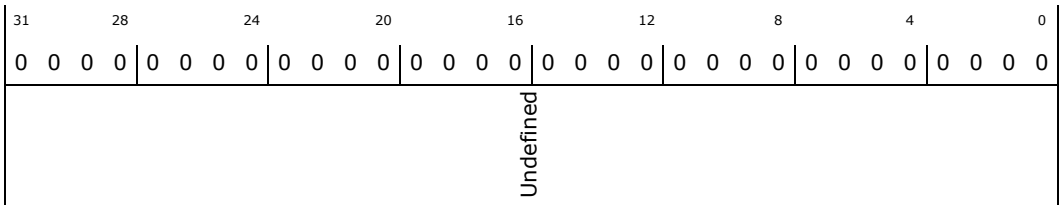
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 36Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.157 Destination Software Transaction Request Register - LOW (ReqDstReg_LO)—Offset 370h

Destination Software Transaction Request Register

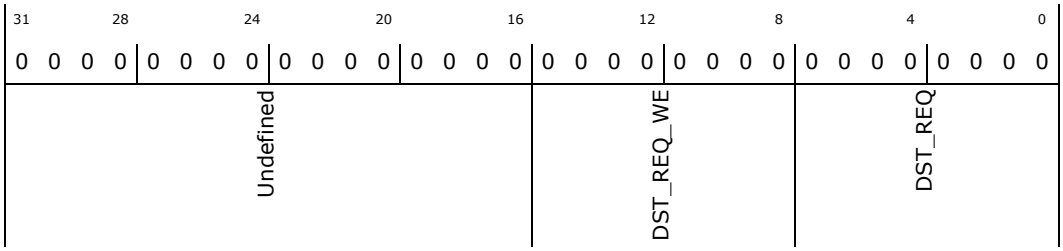
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 370h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**DST_REQ_WE:** Destination request write enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**DST_REQ:** Destination Software Transaction Request Register

9.2.158 Destination Software Transaction Request Register - HIGH (ReqDstReg_HI)—Offset 374h

Destination Software Transaction Request Register

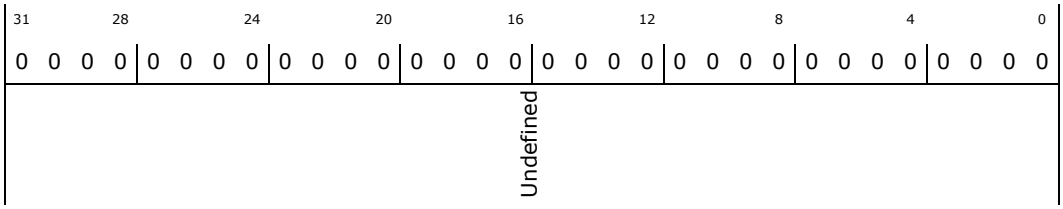
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 374h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.159 Single Source Transaction Request Register - LOW (SglRqSrcReg_LO)—Offset 378h

Single Source Transaction Request Register

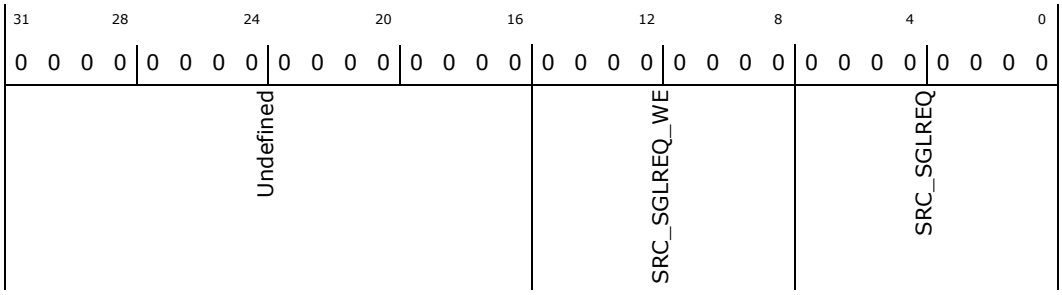
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 378h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**SRC_SGLREQ_WE:** Source req write enable 0=write disabled 1=write enabled
7:0	0x0 RW	**SRC_SGLREQ:** Source request

9.2.160 Single Source Transaction Request Register - HIGH (SglRqSrcReg_HI)—Offset 37Ch

Single Source Transaction Request Register

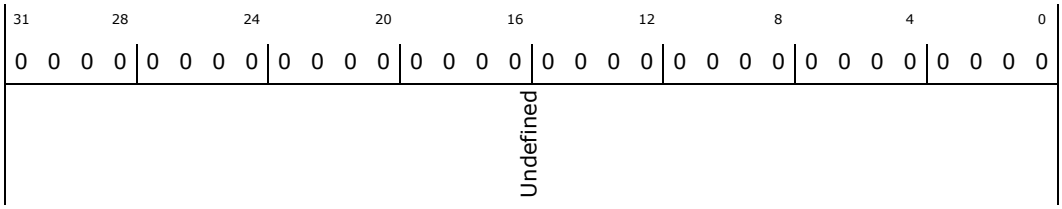
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 37Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.161 Single Destination Transaction Request Register - LOW (SglRqDstReg_LO)—Offset 380h

Single Destination Transaction Request Register

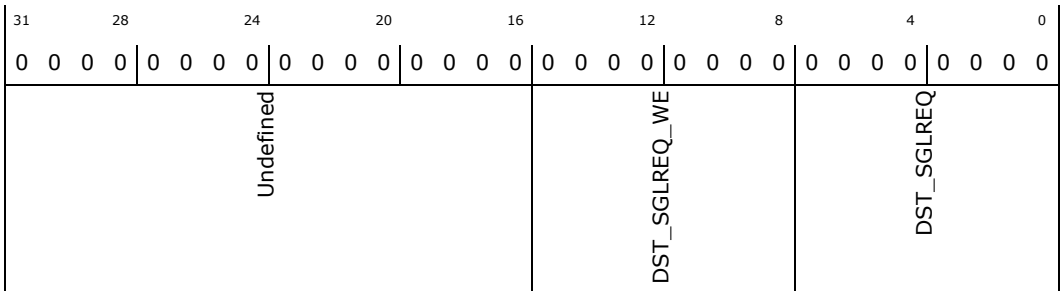
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 380h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**DST_SGLREQ_WE:** Destination request write enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**DST_SGLREQ:** Destination Software Transaction Request Register

9.2.162 Single Destination Transaction Request Register - HIGH (SglRqDstReg_HI)—Offset 384h

Single Destination Transaction Request Register

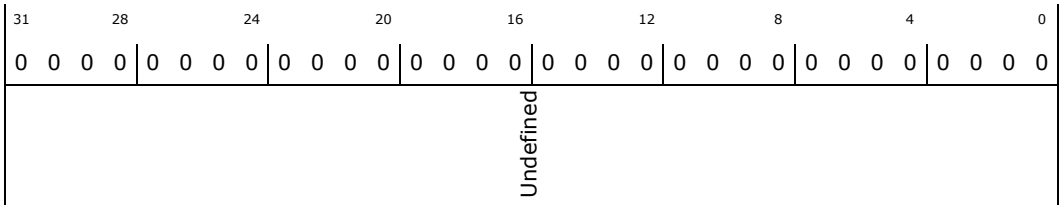
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 384h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.163 Last Source Transaction Request Register - LOW (LstSrcReg_LO)—Offset 388h

Last Source Transaction Request Register

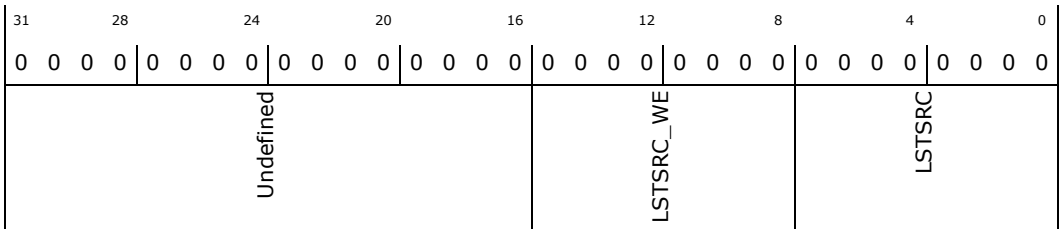
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 388h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**LSTSRC_WE:** Last Source transaction req write enable 0=write disabled 1=write enabled
7:0	0x0 RW	**LSTSRC:** Last Source transaction request 0 = Not last transaction in current block 1 = Last transaction in current block

9.2.164 Last Source Transaction Request Register - HIGH (LstSrcReg_HI)—Offset 38Ch

Last Source Transaction Request Register

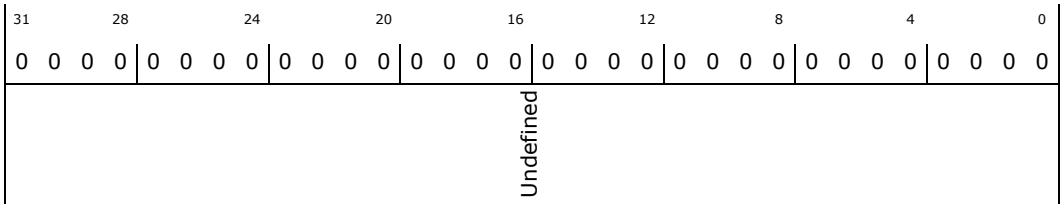
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 38Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.165 Last Destination Transaction Request Register - LOW (LstDstReg_LO)—Offset 390h

Last Destination Transaction Request Register

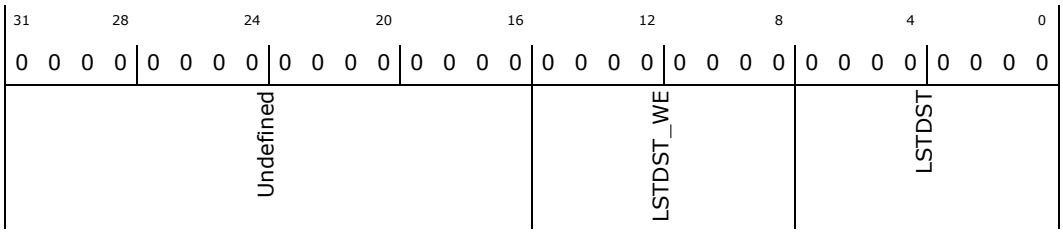
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 390h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**LSTDST_WE:** Last Destination transaction request write enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**LSTDST:** Last Destination Transaction Request Register 0 = Not last transaction in current block 1 = Last transaction in current block

9.2.166 Last Destination Transaction Request Register - HIGH (LstDstReg_HI)—Offset 394h

Last Destination Transaction Request Register

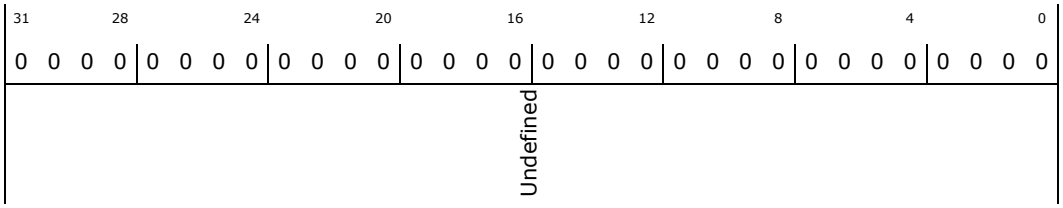
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 394h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.167 DW_ahb_dmac Configuration Register - LOW (DmaCfgReg_LO)—Offset 398h

DW_ahb_dmac Configuration Register

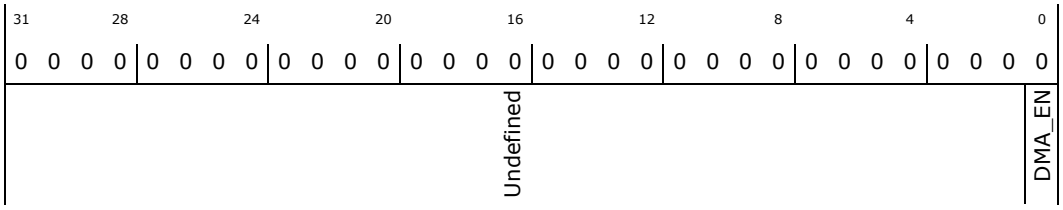
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 398h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Undefined:** Reserved
0	0x0 RW	**DMA_EN:** DW_ahb_dmac Enable bit. 0 = DW_ahb_dmac Disabled 1 = DW_ahb_dmac Enabled

9.2.168 DW_ahb_dmac Configuration Register - HIGH (DmaCfgReg_HI)—Offset 39Ch

DW_ahb_dmac Configuration Register

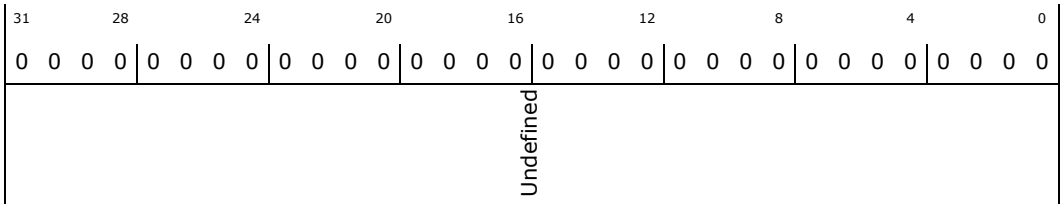
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 39Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.169 DW_ahb_dmac Channel Enable Register - LOW (ChEnReg_LO)—Offset 3A0h

DW_ahb_dmac Channel Enable Register

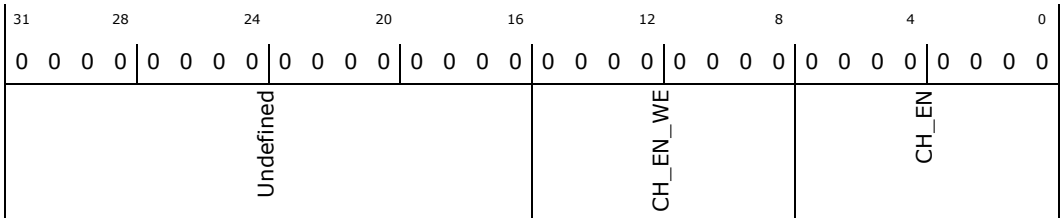
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**CH_EN_WE:** Channel enable write enable.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel; clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel

9.2.170 DW_ahb_dmac Channel Enable Register - HIGH (ChEnReg_HI)—Offset 3A4h

DW_ahb_dmac Channel Enable Register

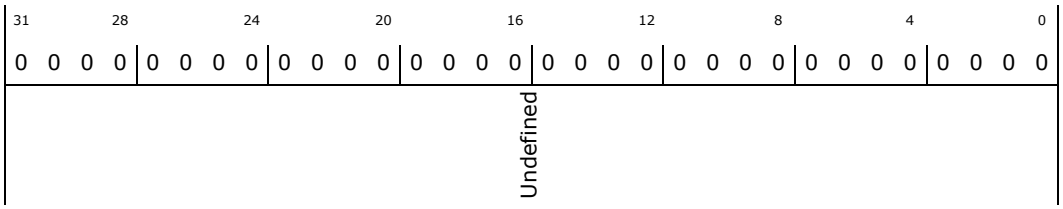
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.171 DW_ahb_dmac ID Register - LOW (DmaIdReg_LO)—Offset 3A8h

DW_ahb_dmac ID Register

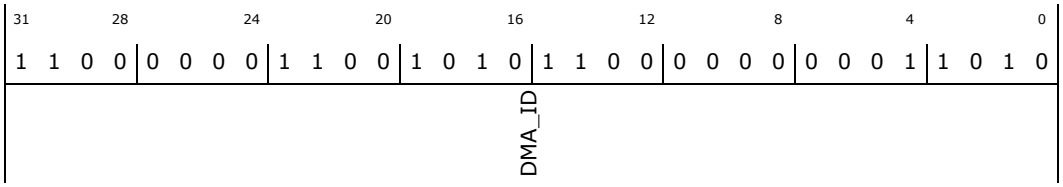
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: C0CAC01Ah



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xc0cac01a RO	**DMA_ID:** Hardcoded DW_ahb_dmac Peripheral ID

9.2.172 DW_ahb_dmac ID Register - HIGH (DmaIdReg_HI)—Offset 3ACh

DW_ahb_dmac ID Register

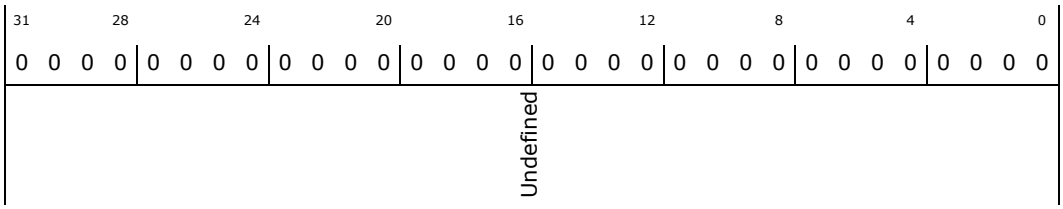
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.173 DW_ahb_dmac Test Register - LOW (DmaTestReg_LO)—Offset 3B0h

DW_ahb_dmac Test Register

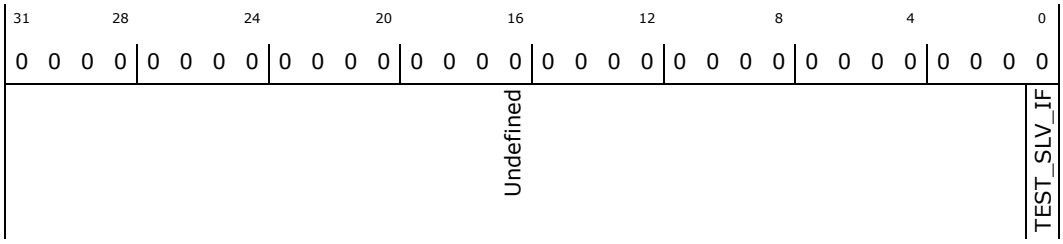
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Undefined:** Reserved
0	0x0 RW	**TEST_SLV_IF:** Puts the AHB slave interface into test mode. In this mode, the readback value of the writable registers always matches the value written. This bit does not allow writing to read-only registers. 0 = Normal mode 1 = Test mode

9.2.174 DW_ahb_dmac Test Register - HIGH (DmaTestReg_HI)—Offset 3B4h

DW_ahb_dmac Test Register

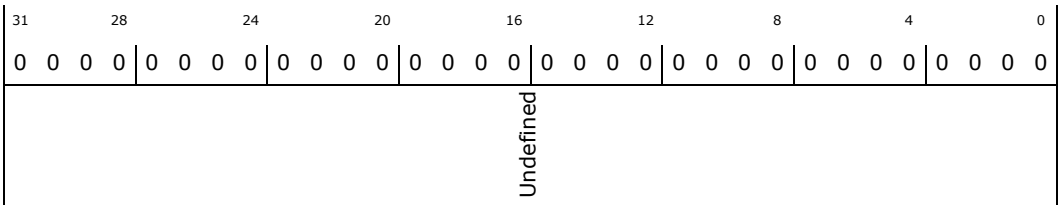
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.2.175 DW_ahb_dmac Component Parameters Register 6 - LOW (DMA_COMP_PARAMS_6_LO)—Offset 3C8h

DW_ahb_dmac Component Parameters Register 6

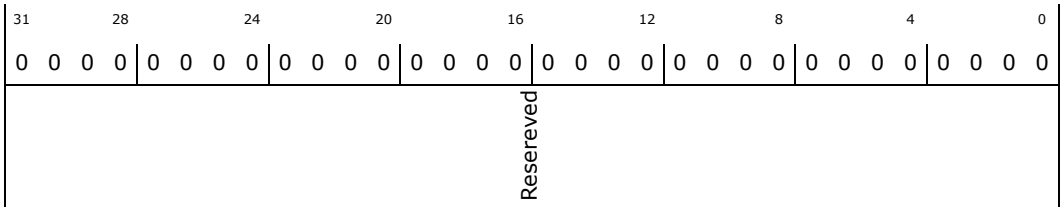
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Resereved:** Resereved

9.2.176 DW_ahb_dmac Component Parameters Register 6 - HIGH (DMA_COMP_PARAMS_6_HI)—Offset 3CCh

DW_ahb_dmac Component Parameters Register 6

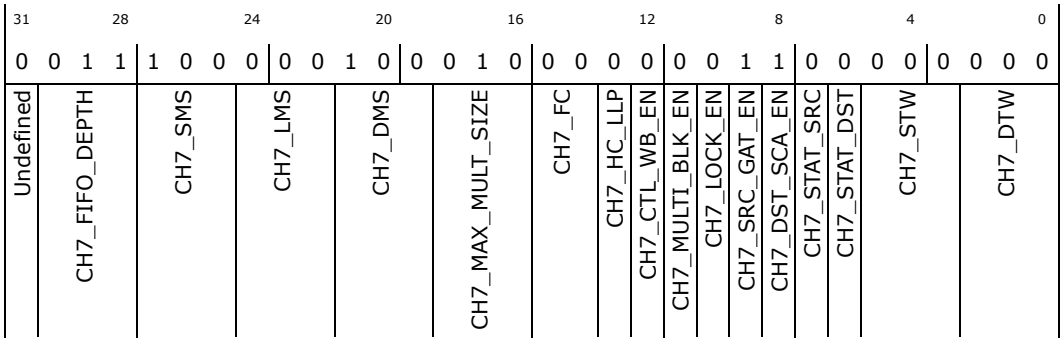
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Undefined:** Reserved
30:28	0x3 RO	**CH7_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH7_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 8 0x1 = 16 0x2 = 32 0x3 = 64 0x4 = 128
27:25	0x4 RO	**CH7_SMS:** The value of this register is derived from the DMAH_CH7_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE

Bit Range	Default & Access	Field Name (ID): Description
24:22	0x0 RO	**CH7_LMS:** The value of this register is derived from the DMAH_CH7_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
21:19	0x4 RO	**CH7_DMS:** The value of this register is derived from the DMAH_CH7_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
18:16	0x2 RO	**CH7_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH7_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 4 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
15:14	0x0 RO	**CH7_FC:** The value of this register is derived from the DMAH_CH7_FC coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = DMA 0x1 = SRC 0x2 = DST 0x3 = ANY
13	0x0 RO	**CH7_HC_LLP:** The value of this register is derived from the DMAH_CH7_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. 0x0 = FALSE 0x1 = TRUE
12	0x0 RO	**CH7_CTL_WB_EN:** The value of this register is derived from the DMAH_CH7_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
11	0x0 RO	**CH7_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH7_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. 0x0 = FALSE 0x1 = TRUE
10	0x0 RO	**CH7_LOCK_EN:** The value of this register is derived from the DMAH_CH7_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = FALSE 0x1 = TRUE
9	0x1 RO	**CH7_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH7_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
8	0x1 RO	**CH7_DST_SCA_EN:** The value of this register is derived from the DMAH_CH7_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
7	0x0 RO	**CH7_STAT_SRC:** The value of this register is derived from the DMAH_CH7_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
6	0x0 RO	**CH7_STAT_DST:** The value of this register is derived from the DMAH_CH7_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
5:3	0x0 RO	**CH7_STW:** The value of this register is derived from the DMAH_CH7_STW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
2:0	0x0 RO	**CH7_DTW:** The value of this register is derived from the DMAH_CH7_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved

9.2.177 DW_ahb_dmac Component Parameters Register 5 - LOW (DMA_COMP_PARAMS_5_LO)—Offset 3D0h

DW_ahb_dmac Component Parameters Register 5

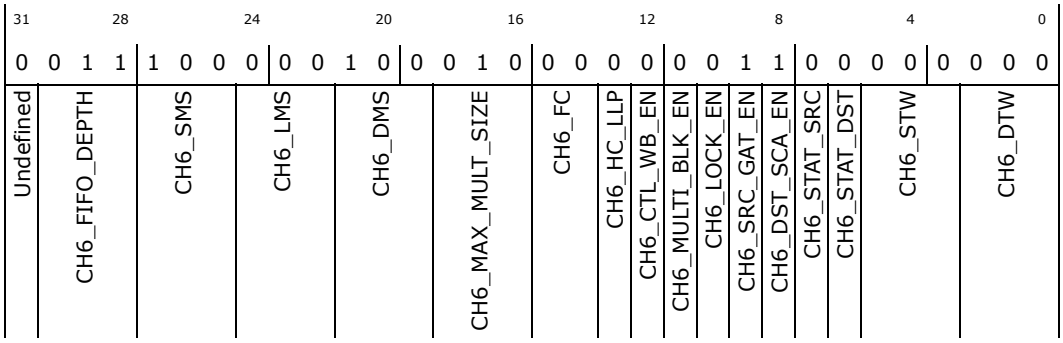
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Undefined:** Reserved
30:28	0x3 RO	**CH6_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH6_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 8 0x1 = 16 0x2 = 3 20x3 = 64 0x4 = 128
27:25	0x4 RO	**CH6_SMS:** The value of this register is derived from the DMAH_CH6_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
24:22	0x0 RO	**CH6_LMS:** The value of this register is derived from the DMAH_CH6_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
21:19	0x4 RO	**CH6_DMS:** The value of this register is derived from the DMAH_CH6_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
18:16	0x2 RO	**CH6_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH6_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 4 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
15:14	0x0 RO	**CH6_FC:** The value of this register is derived from the DMAH_CH6_FC coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = DMA 0x1 = SRC 0x2 = DST 0x3 = ANY

Bit Range	Default & Access	Field Name (ID): Description
13	0x0 RO	**CH6_HC_LLP:** The value of this register is derived from the DMAH_CH6_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. 0x0 = FALSE 0x1 = TRUE
12	0x0 RO	**CH6_CTL_WB_EN:** The value of this register is derived from the DMAH_CH6_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
11	0x0 RO	**CH6_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH6_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. 0x0 = FALSE 0x1 = TRUE
10	0x0 RO	**CH6_LOCK_EN:** The value of this register is derived from the DMAH_CH6_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = FALSE 0x1 = TRUE
9	0x1 RO	**CH6_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH6_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
8	0x1 RO	**CH6_DST_SCA_EN:** The value of this register is derived from the DMAH_CH6_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
7	0x0 RO	**CH6_STAT_SRC:** The value of this register is derived from the DMAH_CH6_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
6	0x0 RO	**CH6_STAT_DST:** The value of this register is derived from the DMAH_CH6_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
5:3	0x0 RO	**CH6_STW:** The value of this register is derived from the DMAH_CH6_STW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
2:0	0x0 RO	**CH6_DTW:** The value of this register is derived from the DMAH_CH6_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved

9.2.178 DW_ahb_dmac Component Parameters Register 5 - HIGH (DMA_COMP_PARAMS_5_HI)—Offset 3D4h

DW_ahb_dmac Component Parameters Register 5

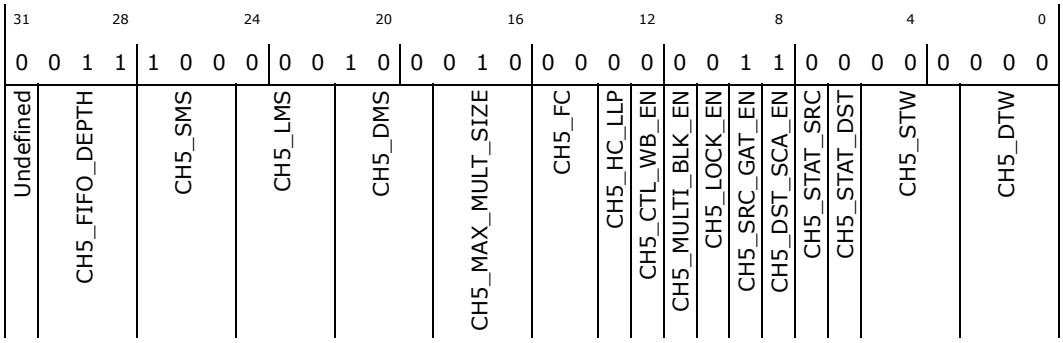
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Undefined:** Reserved
30:28	0x3 RO	**CH5_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH5_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 8 0x1 = 16 0x2 = 3 20x3 = 64 0x4 = 128
27:25	0x4 RO	**CH5_SMS:** The value of this register is derived from the DMAH_CH5_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
24:22	0x0 RO	**CH5_LMS:** The value of this register is derived from the DMAH_CH5_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
21:19	0x4 RO	**CH5_DMS:** The value of this register is derived from the DMAH_CH5_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
18:16	0x2 RO	**CH5_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH5_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 4 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
15:14	0x0 RO	**CH5_FC:** The value of this register is derived from the DMAH_CH5_FC coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = DMA 0x1 = SRC 0x2 = DST 0x3 = ANY
13	0x0 RO	**CH5_HC_LLP:** The value of this register is derived from the DMAH_CH5_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. 0x0 = FALSE 0x1 = TRUE
12	0x0 RO	**CH5_CTL_WB_EN:** The value of this register is derived from the DMAH_CH5_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
11	0x0 RO	**CH5_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH5_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. 0x0 = FALSE 0x1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RO	**CH5_LOCK_EN:** The value of this register is derived from the DMAH_CH5_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = FALSE 0x1 = TRUE
9	0x1 RO	**CH5_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH5_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
8	0x1 RO	**CH5_DST_SCA_EN:** The value of this register is derived from the DMAH_CH5_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
7	0x0 RO	**CH5_STAT_SRC:** The value of this register is derived from the DMAH_CH5_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
6	0x0 RO	**CH5_STAT_DST:** The value of this register is derived from the DMAH_CH5_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
5:3	0x0 RO	**CH5_STW:** The value of this register is derived from the DMAH_CH5_STW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
2:0	0x0 RO	**CH5_DTW:** The value of this register is derived from the DMAH_CH5_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved

9.2.179 DW_ahb_dmac Component Parameters Register 4 - LOW (DMA_COMP_PARAMS_4_LO)—Offset 3D8h

DW_ahb_dmac Component Parameters Register 4

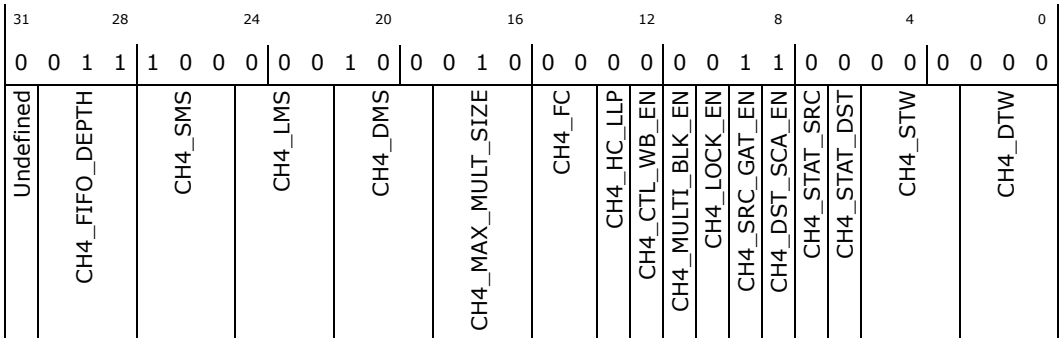
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Undefined:** Reserved
30:28	0x3 RO	**CH4_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH4_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 8 0x1 = 16 0x2 = 3 20x3 = 64 0x4 = 128
27:25	0x4 RO	**CH4_SMS:** The value of this register is derived from the DMAH_CH4_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
24:22	0x0 RO	**CH4_LMS:** The value of this register is derived from the DMAH_CH4_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
21:19	0x4 RO	**CH4_DMS:** The value of this register is derived from the DMAH_CH4_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
18:16	0x2 RO	**CH4_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH4_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 4 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
15:14	0x0 RO	**CH4_FC:** The value of this register is derived from the DMAH_CH4_FC coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = DMA 0x1 = SRC 0x2 = DST 0x3 = ANY
13	0x0 RO	**CH4_HC_LLP:** The value of this register is derived from the DMAH_CH4_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. 0x0 = FALSE 0x1 = TRUE
12	0x0 RO	**CH4_CTL_WB_EN:** The value of this register is derived from the DMAH_CH4_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
11	0x0 RO	**CH4_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH4_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. 0x0 = FALSE 0x1 = TRUE
10	0x0 RO	**CH4_LOCK_EN:** The value of this register is derived from the DMAH_CH4_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = FALSE 0x1 = TRUE
9	0x1 RO	**CH4_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH4_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
8	0x1 RO	**CH4_DST_SCA_EN:** The value of this register is derived from the DMAH_CH4_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
7	0x0 RO	**CH4_STAT_SRC:** The value of this register is derived from the DMAH_CH4_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
6	0x0 RO	**CH4_STAT_DST:** The value of this register is derived from the DMAH_CH4_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
5:3	0x0 RO	**CH4_STW:** The value of this register is derived from the DMAH_CH4_STW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
2:0	0x0 RO	**CH4_DTW:** The value of this register is derived from the DMAH_CH4_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved

9.2.180 DW_ahb_dmac Component Parameters Register 4 - HIGH (DMA_COMP_PARAMS_4_HI)—Offset 3DCh

DW_ahb_dmac Component Parameters Register 4

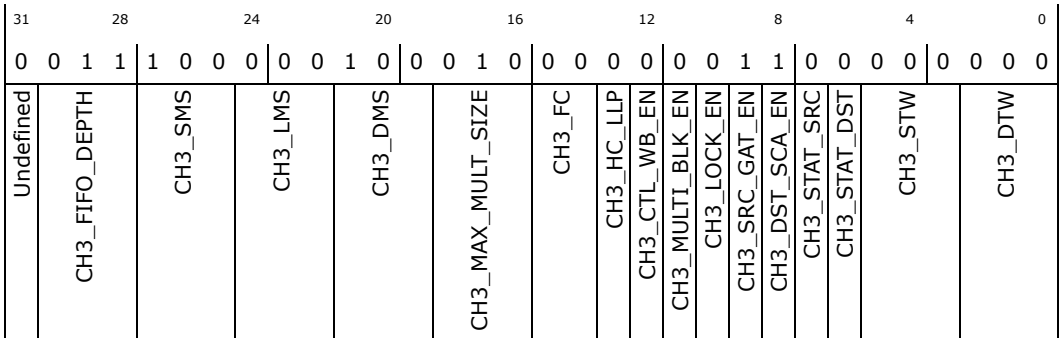
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Undefined:** Reserved
30:28	0x3 RO	**CH3_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH3_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 8 0x1 = 16 0x2 = 3 20x3 = 64 0x4 = 128
27:25	0x4 RO	**CH3_SMS:** The value of this register is derived from the DMAH_CH3_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE

Bit Range	Default & Access	Field Name (ID): Description
24:22	0x0 RO	**CH3_LMS:** The value of this register is derived from the DMAH_CH3_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
21:19	0x4 RO	**CH3_DMS:** The value of this register is derived from the DMAH_CH3_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
18:16	0x2 RO	**CH3_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH3_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 4 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
15:14	0x0 RO	**CH3_FC:** The value of this register is derived from the DMAH_CH3_FC coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = DMA 0x1 = SRC 0x2 = DST 0x3 = ANY
13	0x0 RO	**CH3_HC_LLP:** The value of this register is derived from the DMAH_CH3_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. 0x0 = FALSE 0x1 = TRUE
12	0x0 RO	**CH3_CTL_WB_EN:** The value of this register is derived from the DMAH_CH3_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
11	0x0 RO	**CH3_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH3_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. 0x0 = FALSE 0x1 = TRUE
10	0x0 RO	**CH3_LOCK_EN:** The value of this register is derived from the DMAH_CH3_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = FALSE 0x1 = TRUE
9	0x1 RO	**CH3_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH3_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
8	0x1 RO	**CH3_DST_SCA_EN:** The value of this register is derived from the DMAH_CH3_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
7	0x0 RO	**CH3_STAT_SRC:** he value of this register is derived from the DMAH_CH3_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
6	0x0 RO	**CH3_STAT_DST:** The value of this register is derived from the DMAH_CH3_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
5:3	0x0 RO	**CH3_STW:** The value of this register is derived from the DMAH_CH3_STW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
2:0	0x0 RO	**CH3_DTW:** The value of this register is derived from the DMAH_CH3_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved

9.2.181 DW_ahb_dmac Component Parameters Register 3 - LOW (DMA_COMP_PARAMS_3_LO)—Offset 3E0h

DW_ahb_dmac Component Parameters Register 3

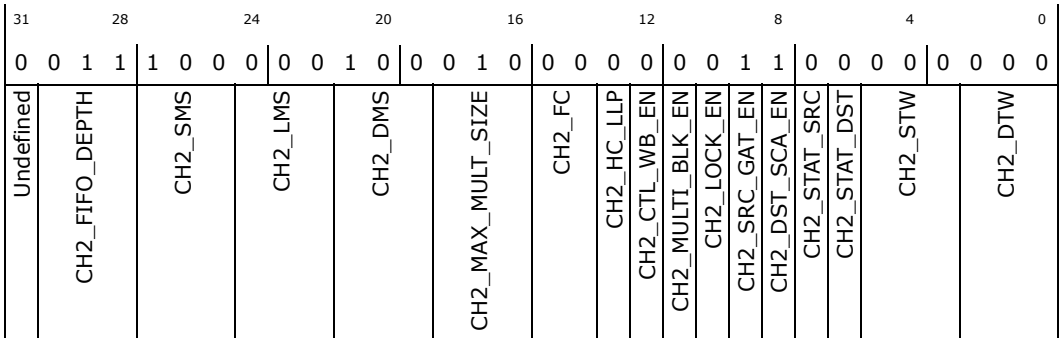
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Undefined:** Reserved
30:28	0x3 RO	**CH2_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH2_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 8 0x1 = 16 0x2 = 3 20x3 = 64 0x4 = 128
27:25	0x4 RO	**CH2_SMS:** The value of this register is derived from the DMAH_CH2_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
24:22	0x0 RO	**CH2_LMS:** The value of this register is derived from the DMAH_CH2_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
21:19	0x4 RO	**CH2_DMS:** The value of this register is derived from the DMAH_CH2_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
18:16	0x2 RO	**CH2_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH2_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 4 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
15:14	0x0 RO	**CH2_FC:** The value of this register is derived from the DMAH_CH2_FC coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = DMA 0x1 = SRC 0x2 = DST 0x3 = ANY

Bit Range	Default & Access	Field Name (ID): Description
13	0x0 RO	**CH2_HC_LLP:** The value of this register is derived from the DMAH_CH2_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. 0x0 = FALSE 0x1 = TRUE
12	0x0 RO	**CH2_CTL_WB_EN:** The value of this register is derived from the DMAH_CH2_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
11	0x0 RO	**CH2_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH2_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to . 0x0 = FALSE 0x1 = TRUE
10	0x0 RO	**CH2_LOCK_EN:** The value of this register is derived from the DMAH_CH2_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = FALSE 0x1 = TRUE
9	0x1 RO	**CH2_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH2_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
8	0x1 RO	**CH2_DST_SCA_EN:** The value of this register is derived from the DMAH_CH2_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
7	0x0 RO	**CH2_STAT_SRC:** The value of this register is derived from the DMAH_CH2_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
6	0x0 RO	**CH2_STAT_DST:** The value of this register is derived from the DMAH_CH2_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
5:3	0x0 RO	**CH2_STW:** The value of this register is derived from the DMAH_CH2_STW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
2:0	0x0 RO	**CH2_DTW:** The value of this register is derived from the DMAH_CH2_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved

9.2.182 DW_ahb_dmac Component Parameters Register 3 - HIGH (DMA_COMP_PARAMS_3_HI)—Offset 3E4h

DW_ahb_dmac Component Parameters Register 3

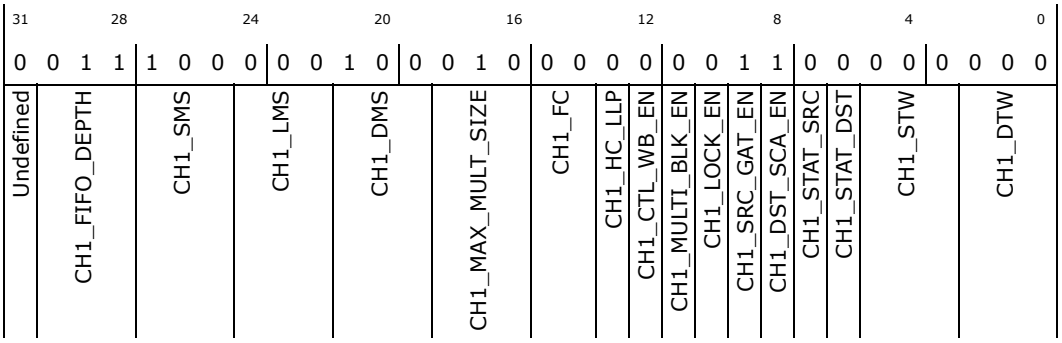
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Undefined:** Reserved
30:28	0x3 RO	**CH1_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH1_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 8 0x1 = 16 0x2 = 3 20x3 = 64 0x4 = 128
27:25	0x4 RO	**CH1_SMS:** The value of this register is derived from the DMAH_CH1_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
24:22	0x0 RO	**CH1_LMS:** The value of this register is derived from the DMAH_CH1_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
21:19	0x4 RO	**CH1_DMS:** The value of this register is derived from the DMAH_CH1_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
18:16	0x2 RO	**CH1_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH1_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 4 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
15:14	0x0 RO	**CH1_FC:** The value of this register is derived from the DMAH_CH1_FC coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = DMA 0x1 = SRC 0x2 = DST 0x3 = ANY
13	0x0 RO	**CH1_HC_LLP:** The value of this register is derived from the DMAH_CH1_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. 0x0 = FALSE 0x1 = TRUE
12	0x0 RO	**CH1_CTL_WB_EN:** The value of this register is derived from the DMAH_CH1_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
11	0x0 RO	**CH1_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH1_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. 0x0 = FALSE 0x1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RO	**CH1_LOCK_EN:** The value of this register is derived from the DMAH_CH1_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = FALSE 0x1 = TRUE
9	0x1 RO	**CH1_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH1_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
8	0x1 RO	**CH1_DST_SCA_EN:** The value of this register is derived from the DMAH_CH1_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
7	0x0 RO	**CH1_STAT_SRC:** The value of this register is derived from the DMAH_CH1_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
6	0x0 RO	**CH1_STAT_DST:** The value of this register is derived from the DMAH_CH1_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
5:3	0x0 RO	**CH1_STW:** The value of this register is derived from the DMAH_CH1_STW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
2:0	0x0 RO	**CH1_DTW:** The value of this register is derived from the DMAH_CH1_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved

9.2.183 DW_ahb_dmac Component Parameters Register 2 - LOW (DMA_COMP_PARAMS_2_LO)—Offset 3E8h

DW_ahb_dmac Component Parameters Register 2

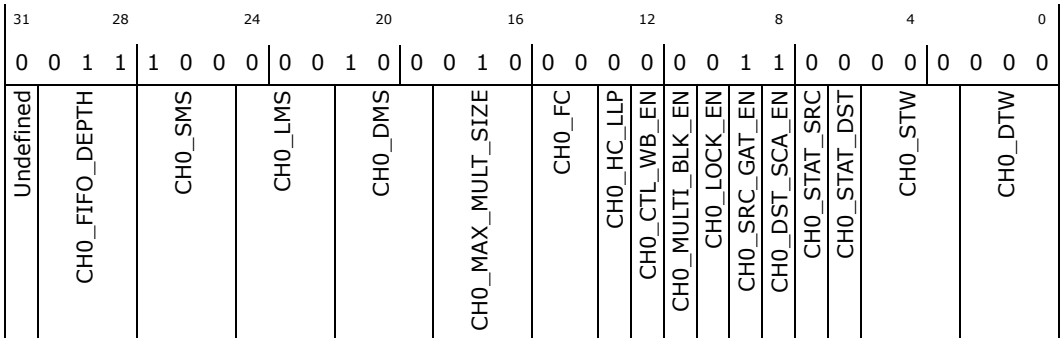
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Undefined:** Reserved
30:28	0x3 RO	**CH0_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH0_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 8 0x1 = 16 0x2 = 3 20x3 = 64 0x4 = 128
27:25	0x4 RO	**CH0_SMS:** The value of this register is derived from the DMAH_CH0_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
24:22	0x0 RO	**CH0_LMS:** The value of this register is derived from the DMAH_CH0_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
21:19	0x4 RO	**CH0_DMS:** The value of this register is derived from the DMAH_CH0_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
18:16	0x2 RO	**CH0_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH0_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 4 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
15:14	0x0 RO	**CH0_FC:** The value of this register is derived from the DMAH_CH0_FC coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = DMA 0x1 = SRC 0x2 = DST 0x3 = ANY
13	0x0 RO	**CH0_HC_LLP:** The value of this register is derived from the DMAH_CH0_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. 0x0 = FALSE 0x1 = TRUE
12	0x0 RO	**CH0_CTL_WB_EN:** The value of this register is derived from the DMAH_CH0_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
11	0x0 RO	**CH0_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH0_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. 0x0 = FALSE 0x1 = TRUE
10	0x0 RO	**CH0_LOCK_EN:** The value of this register is derived from the DMAH_CH0_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = FALSE 0x1 = TRUE
9	0x1 RO	**CH0_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH0_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
8	0x1 RO	**CH0_DST_SCA_EN:** The value of this register is derived from the DMAH_CH0_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
7	0x0 RO	**CH0_STAT_SRC:** The value of this register is derived from the DMAH_CH0_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
6	0x0 RO	**CH0_STAT_DST:** The value of this register is derived from the DMAH_CH0_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
5:3	0x0 RO	**CH0_STW:** The value of this register is derived from the DMAH_CH0_STW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
2:0	0x0 RO	**CH0_DTW:** The value of this register is derived from the DMAH_CH0_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved

9.2.184 DW_ahb_dmac Component Parameters Register 2 - HIGH (DMA_COMP_PARAMS_2_HI)—Offset 3ECh

DW_ahb_dmac Component Parameters Register 2

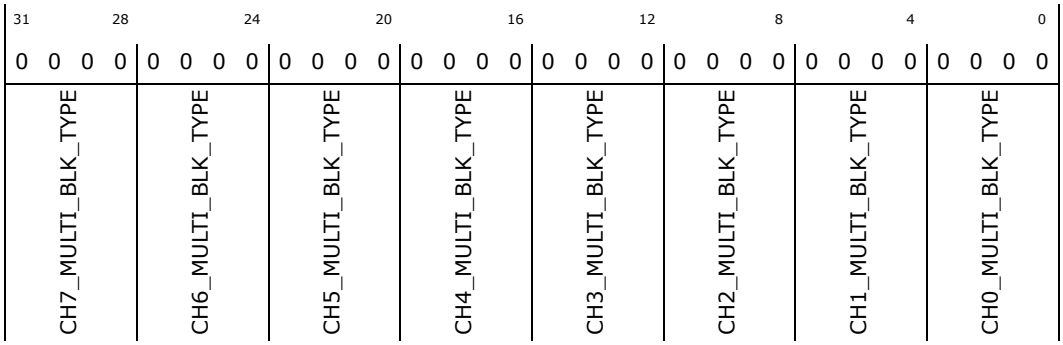
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**CH7_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. 0x0 = NO_HARDCODE 0x1 = CONT_RELOAD 0x2 = RELOAD_CONT 0x3 = RELOAD_RELOAD 0x4 = CONT_LLP 0x5 = RELOAD_LLP 0x6 = LLP_CONT 0x7 = LLP_RELOAD 0x8 = LLP_LLP

Bit Range	Default & Access	Field Name (ID): Description
27:24	0x0 RO	**CH6_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. 0x0 = NO_HARDCODE 0x1 = CONT_RELOAD 0x2 = RELOAD_CONT 0x3 = RELOAD_RELOAD 0x4 = CONT_LLP 0x5 = RELOAD_LLP 0x6 = LLP_CONT 0x7 = LLP_RELOAD 0x8 = LLP_LLP
23:20	0x0 RO	**CH5_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. 0x0 = NO_HARDCODE 0x1 = CONT_RELOAD 0x2 = RELOAD_CONT 0x3 = RELOAD_RELOAD 0x4 = CONT_LLP 0x5 = RELOAD_LLP 0x6 = LLP_CONT 0x7 = LLP_RELOAD 0x8 = LLP_LLP
19:16	0x0 RO	**CH4_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. 0x0 = NO_HARDCODE 0x1 = CONT_RELOAD 0x2 = RELOAD_CONT 0x3 = RELOAD_RELOAD 0x4 = CONT_LLP 0x5 = RELOAD_LLP 0x6 = LLP_CONT 0x7 = LLP_RELOAD 0x8 = LLP_LLP
15:12	0x0 RO	**CH3_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. 0x0 = NO_HARDCODE 0x1 = CONT_RELOAD 0x2 = RELOAD_CONT 0x3 = RELOAD_RELOAD 0x4 = CONT_LLP 0x5 = RELOAD_LLP 0x6 = LLP_CONT 0x7 = LLP_RELOAD 0x8 = LLP_LLP
11:8	0x0 RO	**CH2_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. 0x0 = NO_HARDCODE 0x1 = CONT_RELOAD 0x2 = RELOAD_CONT 0x3 = RELOAD_RELOAD 0x4 = CONT_LLP 0x5 = RELOAD_LLP 0x6 = LLP_CONT 0x7 = LLP_RELOAD 0x8 = LLP_LLP
7:4	0x0 RO	**CH1_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. 0x0 = NO_HARDCODE 0x1 = CONT_RELOAD 0x2 = RELOAD_CONT 0x3 = RELOAD_RELOAD 0x4 = CONT_LLP 0x5 = RELOAD_LLP 0x6 = LLP_CONT 0x7 = LLP_RELOAD 0x8 = LLP_LLP
3:0	0x0 RO	**CH0_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. 0x0 = NO_HARDCODE 0x1 = CONT_RELOAD 0x2 = RELOAD_CONT 0x3 = RELOAD_RELOAD 0x4 = CONT_LLP 0x5 = RELOAD_LLP 0x6 = LLP_CONT 0x7 = LLP_RELOAD 0x8 = LLP_LLP

9.2.185 DW_ahb_dmac Component Parameters Register 1 - LOW (DMA_COMP_PARAMS_1_LO)—Offset 3F0h

DW_ahb_dmac Component Parameters Register 1

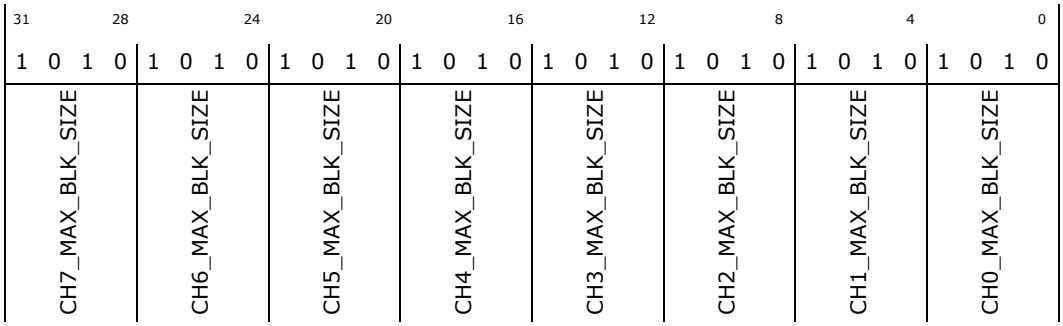
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: AAAAAAAAh



Bit Range	Default & Access	Field Name (ID): Description
31:28	0xa RO	**CH7_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. 0x0 = 3 0x1 = 7 0x2 =15 0x3 = 31 0x4 = 63 0x5 = 127 0x6 = 255 0x7 = 511 0x8 = 1023 0x9 = 2047 0xa = 4095
27:24	0xa RO	**CH6_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. 0x0 = 3 0x1 = 7 0x2 =15 0x3 = 31 0x4 = 63 0x5 = 127 0x6 = 255 0x7 = 511 0x8 = 1023 0x9 = 2047 0xa = 4095
23:20	0xa RO	**CH5_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. 0x0 = 3 0x1 = 7 0x2 =15 0x3 = 31 0x4 = 63 0x5 = 127 0x6 = 255 0x7 = 511 0x8 = 1023 0x9 = 2047 0xa = 4095
19:16	0xa RO	**CH4_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. 0x0 = 3 0x1 = 7 0x2 =15 0x3 = 31 0x4 = 63 0x5 = 127 0x6 = 255 0x7 = 511 0x8 = 1023 0x9 = 2047 0xa = 4095
15:12	0xa RO	**CH3_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. 0x0 = 3 0x1 = 7 0x2 =15 0x3 = 31 0x4 = 63 0x5 = 127 0x6 = 255 0x7 = 511 0x8 = 1023 0x9 = 2047 0xa = 4095
11:8	0xa RO	**CH2_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. 0x0 = 3 0x1 = 7 0x2 =15 0x3 = 31 0x4 = 63 0x5 = 127 0x6 = 255 0x7 = 511 0x8 = 1023 0x9 = 2047 0xa = 4095
7:4	0xa RO	**CH1_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. 0x0 = 3 0x1 = 7 0x2 =15 0x3 = 31 0x4 = 63 0x5 = 127 0x6 = 255 0x7 = 511 0x8 = 1023 0x9 = 2047 0xa = 4095
3:0	0xa RO	**CH0_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. 0x0 = 3 0x1 = 7 0x2 =15 0x3 = 31 0x4 = 63 0x5 = 127 0x6 = 255 0x7 = 511 0x8 = 1023 0x9 = 2047 0xa = 4095

9.2.186 DW_ahb_dmac Component Parameters Register 1 - HIGH (DMA_COMP_PARAMS_1_HI)—Offset 3F4h

DW_ahb_dmac Component Parameters Register 1

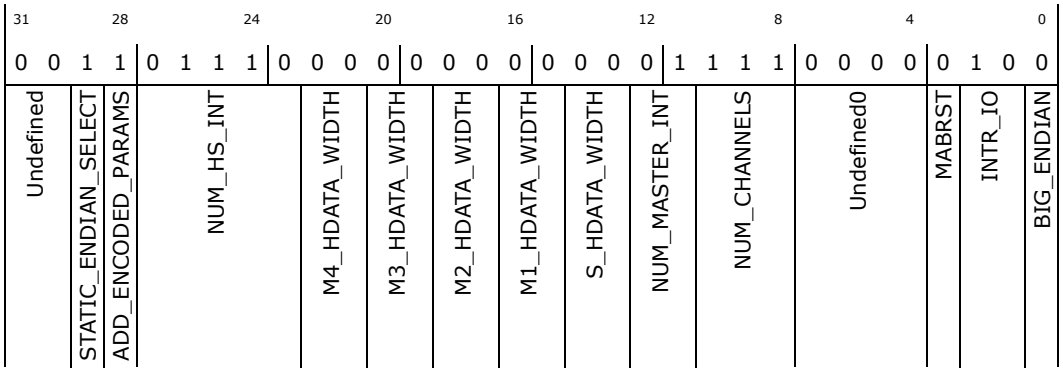
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 37000F04h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**Undefined:** Reserved
29	0x1 RO	**STATIC_ENDIAN_SELECT:** The value of this register is derived from the DMAH_STATIC_ENDIAN_SELECT coreConsultant parameter. For a description of this parameter, refer to page 104. 0 = FALSE 1 = TRUE
28	0x1 RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the DMAH_ADD_ENCODED_PARAMS coreConsultant parameter. For a description of this parameter, refer to page 104. 0 = FALSE 1 = TRUE
27:23	0xe RO	**NUM_HS_INT:** The value of this register is derived from the DMAH_NUM_HS_INT coreConsultant parameter. For a description of this parameter, refer to page 102. 0x00 = 0 to 0x10 = 16
22:21	0x0 RO	**M4_HDATA_WIDTH:** The value of this register is derived from the DMAH_M4_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. 0x0 = 32 bits 0x1 = 64 bits 0x2 = 128 bits 0x3 = 256 bits
20:19	0x0 RO	**M3_HDATA_WIDTH:** The value of this register is derived from the DMAH_M3_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. 0x0 = 32 bits 0x1 = 64 bits 0x2 = 128 bits 0x3 = 256 bits
18:17	0x0 RO	**M2_HDATA_WIDTH:** The value of this register is derived from the DMAH_M2_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. 0x0 = 32 bits 0x1 = 64 bits 0x2 = 128 bits 0x3 = 256 bits

Bit Range	Default & Access	Field Name (ID): Description
16:15	0x0 RO	**M1_HDATA_WIDTH:** The value of this register is derived from the DMAH_M1_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. 0x0 = 32 bits 0x1 = 64 bits 0x2 = 128 bits 0x3 = 256 bits
14:13	0x0 RO	**S_HDATA_WIDTH:** The value of this register is derived from the DMAH_S_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. 0x0 = 32 bits 0x1 = 64 bits 0x2 = 128 bits 0x3 = 256 bits
12:11	0x1 RO	**NUM_MASTER_INT:** The value of this register is derived from the DMAH_NUM_MASTER_INT coreConsultant parameter. For a description of this parameter, refer to page 102. 0x0 = 1 to 0x3 = 4
10:8	0x7 RO	**NUM_CHANNELS:** The value of this register is derived from the DMAH_NUM_CHANNELS coreConsultant parameter. For a description of this parameter, refer to page 102. 0x0 = 1 to 0x7 = 8
7:4	0x0 RW	**Undefined0:** Reserved
3	0x0 RO	**MABRST:** The value of this register is derived from the DMAH_MABRST coreConsultant parameter. For a description of this parameter, refer to page 103. 0 = FALSE 1 = TRUE
2:1	0x2 RO	**INTR_IO:** The value of this register is derived from the DMAH_INTR_IO coreConsultant parameter. For a description of this parameter, refer to page 103. 0x0 = ALL 0x1 = TYPE 0x2 = COMBINED 0x3 = reserved
0	0x0 RO	**BIG_ENDIAN:** The value of this register is derived from the DMAH_BIG_ENDIAN coreConsultant parameter. For a description of this parameter, refer to page 104. 0 = FALSE 1 = TRUE

9.2.187 DMA Component ID Register - LOW (DmaCompsID_LO)—Offset 3F8h

DMA Component ID Register

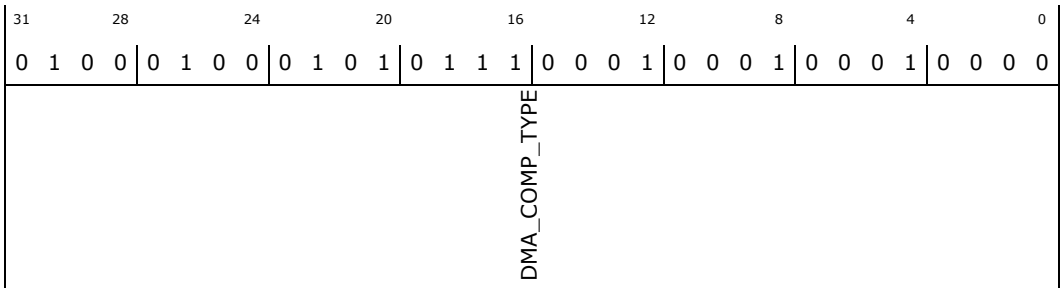
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 44571110h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x44571110 RO	**DMA_COMP_TYPE:** Designware Component Type number = 0x44_57_11_10. This assigned unique hex value is constant and is derived from the two ASCII letters -DW- followed by a 32-bit unsigned number.

9.2.188 DMA Component ID Register - HIGH (DmaCompsID_HI)—Offset 3FCh

DMA Component ID Register

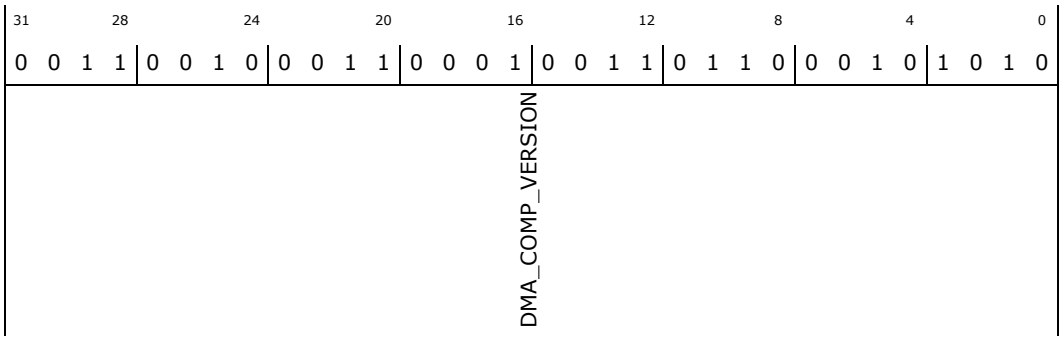
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

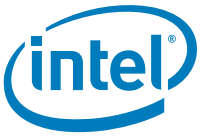
Offset: [BAR] + 3FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:0] + 10h

Default: 3231362Ah



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x3231362a RO	**DMA_COMP_VERSION:** Version of the component



9.3 SIO DMA 2 PCI Configuration Registers for I2C

Table 66. Summary of SIO DMA 2 PCI Configuration Registers—0/24/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4045	00008086h
4–7h	4	"STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h" on page 4045	00100000h
8–Bh	4	"REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4047	00000000h
C–Fh	4	"CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4048	00800000h
10–13h	4	"BAR -Base Address Register (BAR)—Offset 10h" on page 4048	00000000h
14–17h	4	"BAR1 -Base Address Register1 (BAR1)—Offset 14h" on page 4049	00000000h
2C–2Fh	4	"SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4050	00000000h
30–33h	4	"EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4051	00000000h
34–37h	4	"CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4051	00000000h
3C–3Fh	4	"INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4052	00000100h
80–83h	4	"POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4052	00030001h
84–87h	4	"PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4053	00000008h
F8–FBh	4	"Manufacturers ID (MANID)—Offset F8h" on page 4054	00000000h

9.3.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

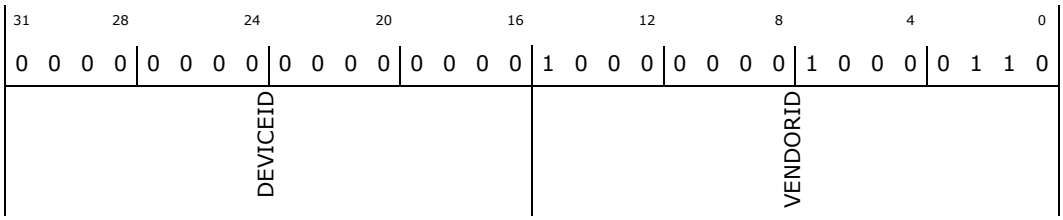
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**DEVICEID:** Device ID identifies the particular AHB/APB device. This is tied to a strap at the top level. Because of tool issues, the HTML files show this field as 0, but the following are the POR values for SoC: LPIO1 DMA: 0x2286 LPIO1 PWM1: 0x2288 LPIO1 PWM2: 0x2289 LPIO1 HSUART1: 0x228A LPIO1 HSUART2: 0x228C LPIO1 SPI1: 0x228E LPIO1 SPI2: 0x2290 LPIO1 SPI3: 0x22AC LPIO2 DMA: 0x22C0 LPIO2 I2C1: 0x22C1 LPIO2 I2C2: 0x22C2 LPIO2 I2C3: 0x22C3 LPIO2 I2C4: 0x22C4 LPIO2 I2C5: 0x22C5 LPIO2 I2C6: 0x22C6 LPIO2 I2C7: 0x22C7 For the final word on this, please see Ray Ng's SoC RevID and DevID HAS on Infofactory: https://ifcollaborate.intel.com/IFC/getdoc.aspx?docbase=InfoFactoryKBandchronid=09005ffd80e84b43andver=CURRENTandqepop=false
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap the top level.

9.3.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

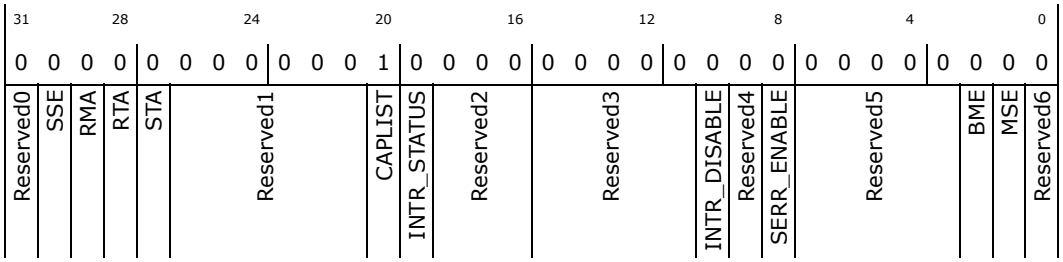
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved0:** Reserved
30	0x0 RW/1C	**SSE:** This bit is set when a device sends an DO_SERR message, and the SERR# Enable bit in the Command register is 1
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric PortReceived Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27	0x0 RW/1C	**STA:** The Bridge sets this bit whenever it responds to a transaction with CA abort. If the SERR# Enable bit is set, the Bridge sets the Signaled System Error bit and sends an DO_SERR message on the IOSF Sideband.
26:21	0x0 RO	**Reserved1:** Reserved
20	0x1 RO	**CAPLIST:** Capabilities List: Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt .i.e Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.. Reset value of this bit is 0.
9	0x0 RO	**Reserved4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: If both SERR# Enable and the Unsupported Request Reporting Enable (URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0x0 RO	**Reserved6:** Reserved

9.3.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

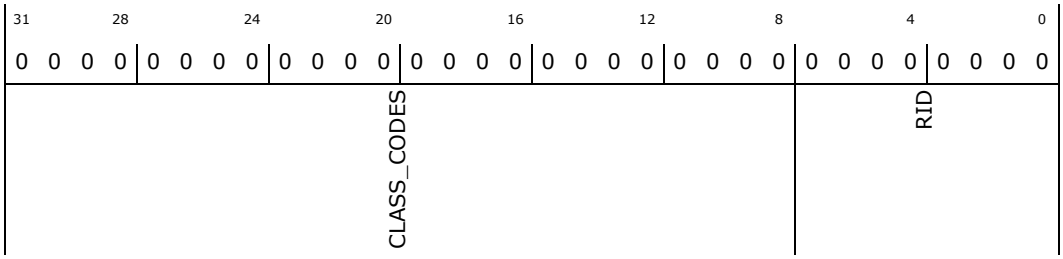
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

9.3.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

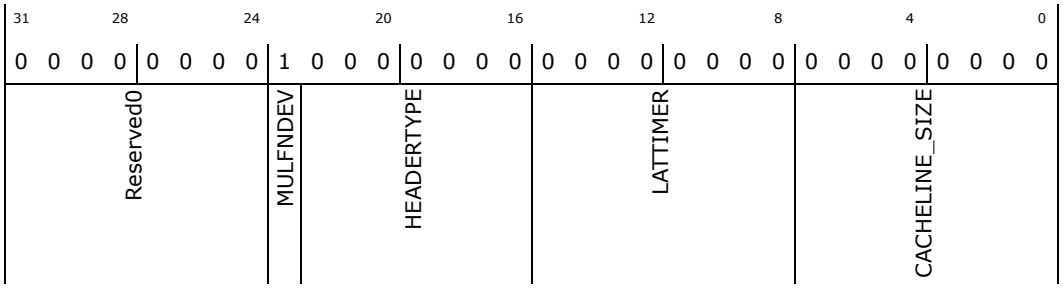
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + Ch

Default: 00800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x1 RO	**MULFNDEV:** Multi Function Device: This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. Value of 1 indicates multifunction device value of 0 indicates single function device
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	0x0 RO	**LATTIMER:** Latency Timer: Doesn.t apply to PCI Express. Hardwired to 00h.
7:0	0x0 RW	**CACHELINE_SIZE:** Cache Line Size: Doesn.t apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

9.3.5 BAR -Base Address Register (BAR)—Offset 10h

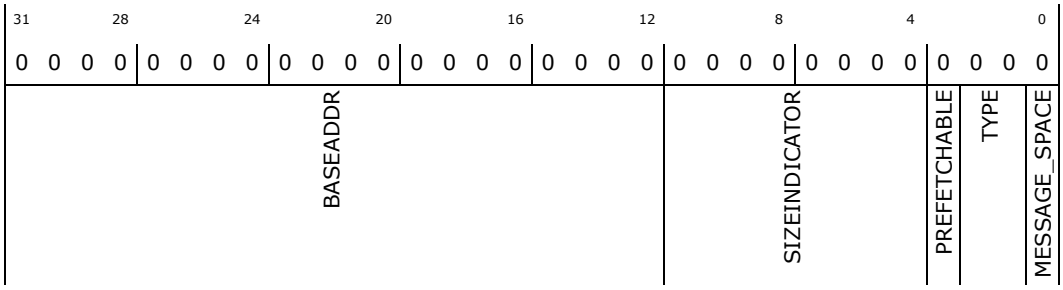
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the AHB device memory space. Taken from Strap values as 1's. Please note that for DMA this field goes from [31:14], or 16kbyte, and the SIZEINDICATOR field goes from [13:4].
11:4	0x0 RO	**SIZEINDICATOR:** Size Indicator Read Only: Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0x0 RO	**TYPE:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.3.6 BAR1 -Base Address Register1 (BAR1)—Offset 14h

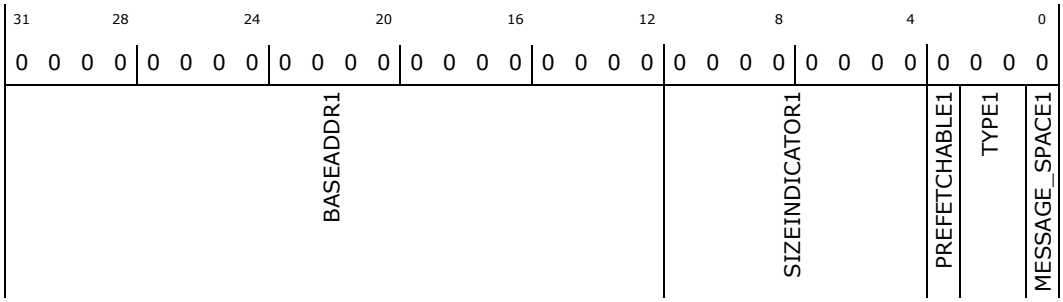
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	0x0 RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not
2:1	0x0 RO	**TYPE1:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.3.7 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

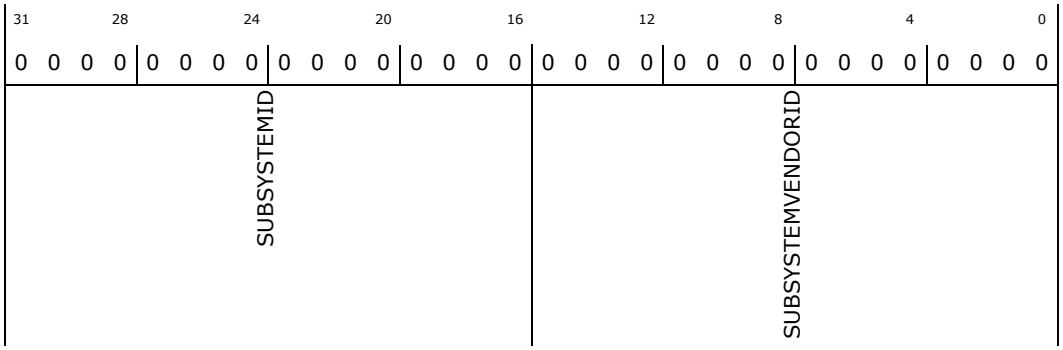
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

9.3.8 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

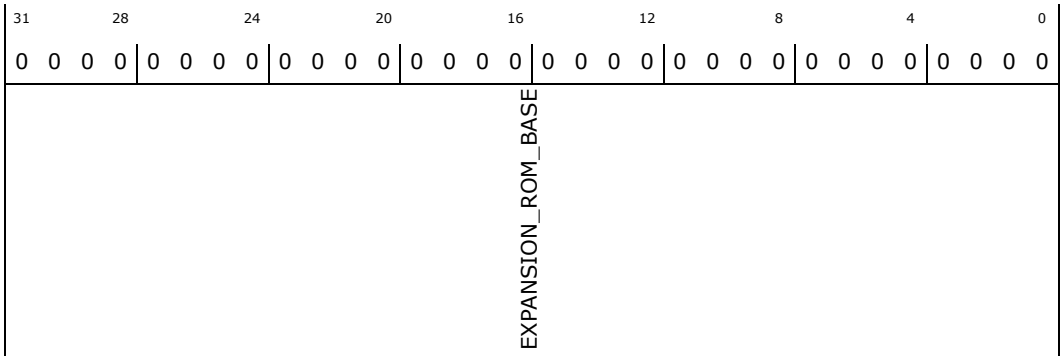
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** A value of all zeros indicates no support for expansion ROM.

9.3.9 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

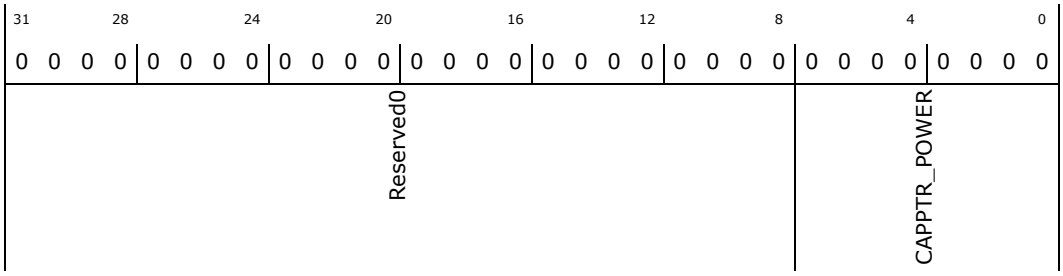
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x0 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

9.3.10 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

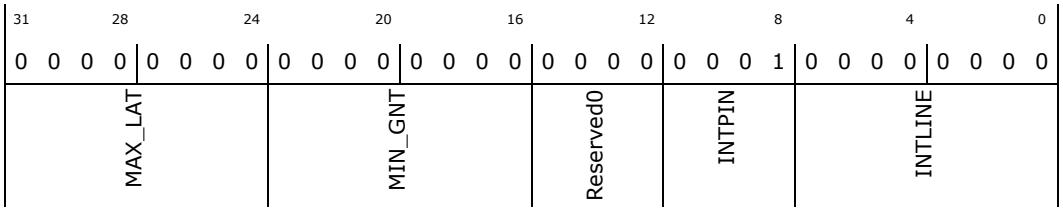
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

9.3.11 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

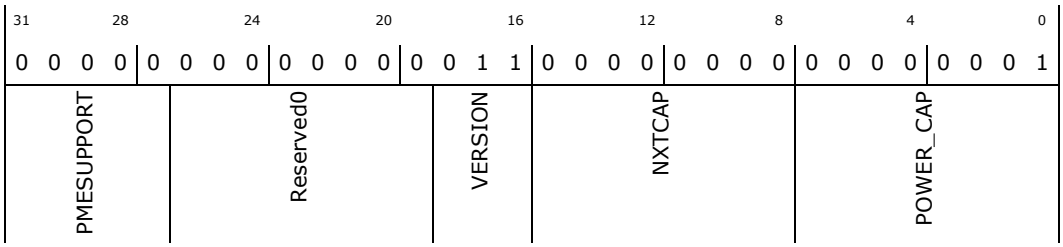
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** PME_Support - This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

9.3.12 PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

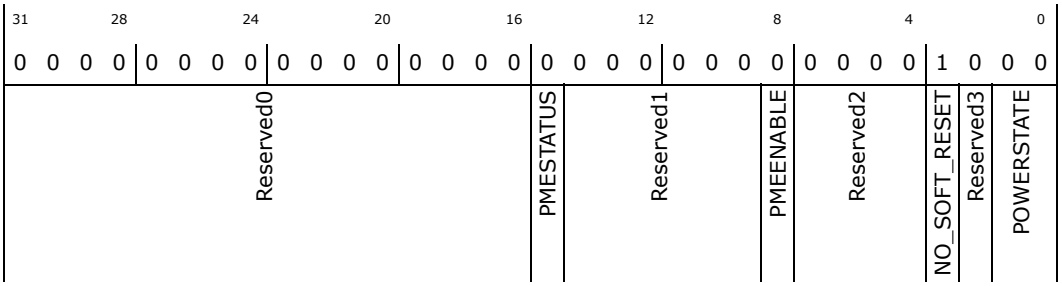
PMECTRLSTATUS - PME Control and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

9.3.13 Manufacturers ID (MANID)—Offset F8h

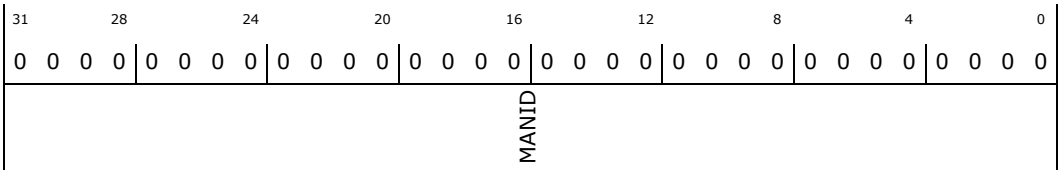
Manufacturers ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:0] + F8h

Default: 00000000h

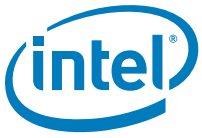


Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: This register is brought out as straps to the top level.

9.4 SIO DMA 2 Memory Mapped I/O Registers for I2C

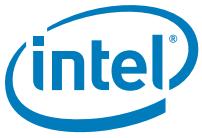
Table 67. Summary of SIO DMA 2 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Source Address Register for Channel 0 - LOW (SAR0_LO)—Offset 0h" on page 4065	00000000h
4–7h	4	"Source Address Register for Channel 0 - HIGH (SAR0_HI)—Offset 4h" on page 4065	00000000h
8–Bh	4	"Destination Address Register for Channel 0 - LOW (DAR0_LO)—Offset 8h" on page 4066	00000000h
C–Fh	4	"Destination Address Register for Channel 0 - HIGH (DAR0_HI)—Offset Ch" on page 4066	00000000h
10–13h	4	"Linked List Pointer Register for Channel 0 - LOW (LLP0_LO)—Offset 10h" on page 4067	00000000h
14–17h	4	"Linked List Pointer Register for Channel 0 - HIGH (LLP0_HI)—Offset 14h" on page 4067	00000000h
18–1Bh	4	"Control Register for Channel 0 - LOW (CTL0_LO)—Offset 18h" on page 4068	00304801h
1C–1Fh	4	"Control Register for Channel 0 - HIGH (CTL0_HI)—Offset 1Ch" on page 4069	00000002h
40–43h	4	"Configuration register for Channel 0 - LOW (CFG0_LO)—Offset 40h" on page 4069	00000E00h
44–47h	4	"Configuration register for Channel 0 - HIGH (CFG0_HI)—Offset 44h" on page 4071	00000004h
48–4Bh	4	"Source Gather Register for Channel 0 - LOW (SGR0_LO)—Offset 48h" on page 4072	00000000h
4C–4Fh	4	"Source Gather Register for Channel 0 - HIGH (SGR0_HI)—Offset 4Ch" on page 4072	00000000h
50–53h	4	"Destination Scatter Register for Channel 0 - LOW (DSR0_LO)—Offset 50h" on page 4073	00000000h
54–57h	4	"Dest scatter Register for Channel 0 - HIGH (DSR0_HI)—Offset 54h" on page 4073	00000000h
58–5Bh	4	"Source Address Register for Channel 1 - LOW (SAR1_LO)—Offset 58h" on page 4074	00000000h
5C–5Fh	4	"Source Address Register for Channel 1 - HIGH (SAR1_HI)—Offset 5Ch" on page 4074	00000000h
60–63h	4	"Destination Address Register for Channel 1 - LOW (DAR1_LO)—Offset 60h" on page 4075	00000000h
64–67h	4	"Destination Address Register for Channel 1 - HIGH (DAR1_HI)—Offset 64h" on page 4075	00000000h
68–6Bh	4	"Linked List Pointer Register for Channel 1 - LOW (LLP1_LO)—Offset 68h" on page 4076	00000000h
6C–6Fh	4	"Linked List Pointer Register for Channel 1 - HIGH (LLP1_HI)—Offset 6Ch" on page 4076	00000000h

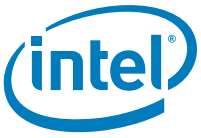


Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
70–73h	4	"Control Register for Channel 1 - LOW (CTL1_LO)—Offset 70h" on page 4077	00304801h
74–77h	4	"Control Register for Channel 1 - HIGH (CTL1_HI)—Offset 74h" on page 4078	00000002h
98–9Bh	4	"Configuration register for Channel 1 - LOW (CFG1_LO)—Offset 98h" on page 4079	00000E20h
9C–9Fh	4	"Configuration register for Channel 1 - HIGH (CFG1_HI)—Offset 9Ch" on page 4080	00000004h
A0–A3h	4	"Source Gather Register for Channel 1 - LOW (SGR1_LO)—Offset A0h" on page 4081	00000000h
A4–A7h	4	"Source Gather Register for Channel 1 - HIGH (SGR1_HI)—Offset A4h" on page 4082	00000000h
A8–ABh	4	"Destination Scatter Register for Channel 1 - LOW (DSR1_LO)—Offset A8h" on page 4082	00000000h
AC–AFh	4	"Dest scatter Register for Channel 1 - HIGH (DSR1_HI)—Offset ACh" on page 4083	00000000h
B0–B3h	4	"Source Address Register for Channel 2 - LOW (SAR2_LO)—Offset B0h" on page 4083	00000000h
B4–B7h	4	"Source Address Register for Channel 2 - HIGH (SAR2_HI)—Offset B4h" on page 4084	00000000h
B8–BBh	4	"Destination Address Register for Channel 2 - LOW (DAR2_LO)—Offset B8h" on page 4084	00000000h
BC–BFh	4	"Destination Address Register for Channel 2 - HIGH (DAR2_HI)—Offset BCh" on page 4085	00000000h
C0–C3h	4	"Linked List Pointer Register for Channel 2 - LOW (LLP2_LO)—Offset C0h" on page 4085	00000000h
C4–C7h	4	"Linked List Pointer Register for Channel 2 - HIGH (LLP2_HI)—Offset C4h" on page 4086	00000000h
C8–CBh	4	"Control Register for Channel 2 - LOW (CTL2_LO)—Offset C8h" on page 4086	00304801h
CC–CFh	4	"Control Register for Channel 2 - HIGH (CTL2_HI)—Offset CCh" on page 4088	00000002h
F0–F3h	4	"Configuration register for Channel 2 - LOW (CFG2_LO)—Offset F0h" on page 4088	00000E40h
F4–F7h	4	"Configuration register for Channel 2 - HIGH (CFG2_HI)—Offset F4h" on page 4089	00000004h
F8–FBh	4	"Source Gather Register for Channel 2 - LOW (SGR2_LO)—Offset F8h" on page 4090	00000000h
FC–FFh	4	"Source Gather Register for Channel 2 - HIGH (SGR2_HI)—Offset FCh" on page 4091	00000000h
100–103h	4	"Destination Scatter Register for Channel 2 - LOW (DSR2_LO)—Offset 100h" on page 4091	00000000h
104–107h	4	"Dest scatter Register for Channel 2 - HIGH (DSR2_HI)—Offset 104h" on page 4092	00000000h

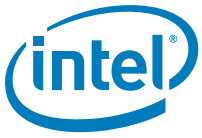
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
108–10Bh	4	"Source Address Register for Channel 3 - LOW (SAR3_LO)—Offset 108h" on page 4092	00000000h
10C–10Fh	4	"Source Address Register for Channel 3 - HIGH (SAR3_HI)—Offset 10Ch" on page 4093	00000000h
110–113h	4	"Destination Address Register for Channel 3 - LOW (DAR3_LO)—Offset 110h" on page 4093	00000000h
114–117h	4	"Destination Address Register for Channel 3 - HIGH (DAR3_HI)—Offset 114h" on page 4094	00000000h
118–11Bh	4	"Linked List Pointer Register for Channel 3 - LOW (LLP3_LO)—Offset 118h" on page 4094	00000000h
11C–11Fh	4	"Linked List Pointer Register for Channel 3 - HIGH (LLP3_HI)—Offset 11Ch" on page 4095	00000000h
120–123h	4	"Control Register for Channel 3 - LOW (CTL3_LO)—Offset 120h" on page 4095	00304801h
124–127h	4	"Control Register for Channel 3 - HIGH (CTL3_HI)—Offset 124h" on page 4097	00000002h
148–14Bh	4	"Configuration register for Channel 3 - LOW (CFG3_LO)—Offset 148h" on page 4097	00000E60h
14C–14Fh	4	"Configuration register for Channel 3 - HIGH (CFG3_HI)—Offset 14Ch" on page 4099	00000004h
150–153h	4	"Source Gather Register for Channel 3 - LOW (SGR3_LO)—Offset 150h" on page 4100	00000000h
154–157h	4	"Source Gather Register for Channel 3 - HIGH (SGR3_HI)—Offset 154h" on page 4100	00000000h
158–15Bh	4	"Destination Scatter Register for Channel 3 - LOW (DSR3_LO)—Offset 158h" on page 4101	00000000h
15C–15Fh	4	"Dest scatter Register for Channel 3 - HIGH (DSR3_HI)—Offset 15Ch" on page 4101	00000000h
160–163h	4	"Source Address Register for Channel 4 - LOW (SAR4_LO)—Offset 160h" on page 4102	00000000h
164–167h	4	"Source Address Register for Channel 4 - HIGH (SAR4_HI)—Offset 164h" on page 4102	00000000h
168–16Bh	4	"Destination Address Register for Channel 4 - LOW (DAR4_LO)—Offset 168h" on page 4103	00000000h
16C–16Fh	4	"Destination Address Register for Channel 4 - HIGH (DAR4_HI)—Offset 16Ch" on page 4103	00000000h
170–173h	4	"Linked List Pointer Register for Channel 4 - LOW (LLP4_LO)—Offset 170h" on page 4104	00000000h
174–177h	4	"Linked List Pointer Register for Channel 4 - HIGH (LLP4_HI)—Offset 174h" on page 4104	00000000h
178–17Bh	4	"Control Register for Channel 4 - LOW (CTL4_LO)—Offset 178h" on page 4105	00304801h
17C–17Fh	4	"Control Register for Channel 4 - HIGH (CTL4_HI)—Offset 17Ch" on page 4106	00000002h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1A0–1A3h	4	"Configuration register for Channel 4 - LOW (CFG4_LO)—Offset 1A0h" on page 4107	00000E80h
1A4–1A7h	4	"Configuration register for Channel 4 - HIGH (CFG4_HI)—Offset 1A4h" on page 4108	00000004h
1A8–1ABh	4	"Source Gather Register for Channel 4 - LOW (SGR4_LO)—Offset 1A8h" on page 4109	00000000h
1AC–1AFh	4	"Source Gather Register for Channel 4 - HIGH (SGR4_HI)—Offset 1ACh" on page 4110	00000000h
1B0–1B3h	4	"Destination Scatter Register for Channel 4 - LOW (DSR4_LO)—Offset 1B0h" on page 4110	00000000h
1B4–1B7h	4	"Dest scatter Register for Channel 4 - HIGH (DSR4_HI)—Offset 1B4h" on page 4111	00000000h
1B8–1BBh	4	"Source Address Register for Channel 5 - LOW (SAR5_LO)—Offset 1B8h" on page 4111	00000000h
1BC–1BFh	4	"Source Address Register for Channel 5 - HIGH (SAR5_HI)—Offset 1BCh" on page 4112	00000000h
1C0–1C3h	4	"Destination Address Register for Channel 5 - LOW (DAR5_LO)—Offset 1C0h" on page 4112	00000000h
1C4–1C7h	4	"Destination Address Register for Channel 5 - HIGH (DAR5_HI)—Offset 1C4h" on page 4113	00000000h
1C8–1CBh	4	"Linked List Pointer Register for Channel 5 - LOW (LLP5_LO)—Offset 1C8h" on page 4113	00000000h
1CC–1CFh	4	"Linked List Pointer Register for Channel 5 - HIGH (LLP5_HI)—Offset 1CCh" on page 4114	00000000h
1D0–1D3h	4	"Control Register for Channel 5 - LOW (CTL5_LO)—Offset 1D0h" on page 4114	00304801h
1D4–1D7h	4	"Control Register for Channel 5 - HIGH (CTL5_HI)—Offset 1D4h" on page 4116	00000002h
1F8–1FBh	4	"Configuration register for Channel 5 - LOW (CFG5_LO)—Offset 1F8h" on page 4116	00000EA0h
1FC–1FFh	4	"Configuration register for Channel 5 - HIGH (CFG5_HI)—Offset 1FCh" on page 4117	00000004h
200–203h	4	"Source Gather Register for Channel 5 - LOW (SGR5_LO)—Offset 200h" on page 4118	00000000h
204–207h	4	"Source Gather Register for Channel 5 - HIGH (SGR5_HI)—Offset 204h" on page 4119	00000000h
208–20Bh	4	"Destination Scatter Register for Channel 5 - LOW (DSR5_LO)—Offset 208h" on page 4119	00000000h
20C–20Fh	4	"Dest scatter Register for Channel 5 - HIGH (DSR5_HI)—Offset 20Ch" on page 4120	00000000h
210–213h	4	"Source Address Register for Channel 6 - LOW (SAR6_LO)—Offset 210h" on page 4120	00000000h
214–217h	4	"Source Address Register for Channel 6 - HIGH (SAR6_HI)—Offset 214h" on page 4121	00000000h

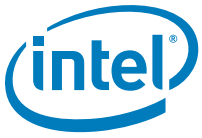


Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
218–21Bh	4	"Destination Address Register for Channel 6 - LOW (DAR6_LO)—Offset 218h" on page 4121	00000000h
21C–21Fh	4	"Destination Address Register for Channel 6 - HIGH (DAR6_HI)—Offset 21Ch" on page 4122	00000000h
220–223h	4	"Linked List Pointer Register for Channel 6 - LOW (LLP6_LO)—Offset 220h" on page 4122	00000000h
224–227h	4	"Linked List Pointer Register for Channel 6 - HIGH (LLP6_HI)—Offset 224h" on page 4123	00000000h
228–22Bh	4	"Control Register for Channel 6 - LOW (CTL6_LO)—Offset 228h" on page 4123	00304801h
22C–22Fh	4	"Control Register for Channel 6 - HIGH (CTL6_HI)—Offset 22Ch" on page 4125	00000002h
250–253h	4	"Configuration register for Channel 6 - LOW (CFG6_LO)—Offset 250h" on page 4125	00000EC0h
254–257h	4	"Configuration register for Channel 6 - HIGH (CFG6_HI)—Offset 254h" on page 4127	00000004h
258–25Bh	4	"Source Gather Register for Channel 6 - LOW (SGR6_LO)—Offset 258h" on page 4128	00000000h
25C–25Fh	4	"Source Gather Register for Channel 6 - HIGH (SGR6_HI)—Offset 25Ch" on page 4128	00000000h
260–263h	4	"Destination Scatter Register for Channel 6 - LOW (DSR6_LO)—Offset 260h" on page 4129	00000000h
264–267h	4	"Dest scatter Register for Channel 6 - HIGH (DSR6_HI)—Offset 264h" on page 4129	00000000h
268–26Bh	4	"Source Address Register for Channel 7 - LOW (SAR7_LO)—Offset 268h" on page 4130	00000000h
26C–26Fh	4	"Source Address Register for Channel 7 - HIGH (SAR7_HI)—Offset 26Ch" on page 4130	00000000h
270–273h	4	"Destination Address Register for Channel 7 - LOW (DAR7_LO)—Offset 270h" on page 4131	00000000h
274–277h	4	"Destination Address Register for Channel 7 - HIGH (DAR7_HI)—Offset 274h" on page 4131	00000000h
278–27Bh	4	"Linked List Pointer Register for Channel 7 - LOW (LLP7_LO)—Offset 278h" on page 4132	00000000h
27C–27Fh	4	"Linked List Pointer Register for Channel 7 - HIGH (LLP7_HI)—Offset 27Ch" on page 4132	00000000h
280–283h	4	"Control Register for Channel 7 - LOW (CTL7_LO)—Offset 280h" on page 4133	00304801h
284–287h	4	"Control Register for Channel 7 - HIGH (CTL7_HI)—Offset 284h" on page 4134	00000002h
2A8–2ABh	4	"Configuration register for Channel 7 - LOW (CFG7_LO)—Offset 2A8h" on page 4135	00000EE0h
2AC–2AFh	4	"Configuration register for Channel 7 - HIGH (CFG7_HI)—Offset 2ACh" on page 4136	00000004h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2B0–2B3h	4	"Source Gather Register for Channel 7 - LOW (SGR7_LO)—Offset 2B0h" on page 4137	00000000h
2B4–2B7h	4	"Source Gather Register for Channel 7 - HIGH (SGR7_HI)—Offset 2B4h" on page 4138	00000000h
2B8–2BBh	4	"Destination Scatter Register for Channel 7 - LOW (DSR7_LO)—Offset 2B8h" on page 4138	00000000h
2BC–2BFh	4	"Dest scatter Register for Channel 7 - HIGH (DSR7_HI)—Offset 2BCh" on page 4139	00000000h
2C0–2C3h	4	"RawTfr Interrupt Raw Status Registers - LOW (RawTfr_LO)—Offset 2C0h" on page 4139	00000000h
2C4–2C7h	4	"RawTfr Interrupt Raw Status Registers - HIGH (RawTfr_HI)—Offset 2C4h" on page 4140	00000000h
2C8–2CBh	4	"RawBlock Interrupt Raw Status Registers - LOW (RawBlock_LO)—Offset 2C8h" on page 4140	00000000h
2CC–2CFh	4	"RawBlock Interrupt Raw Status Registers - HIGH (RawBlock_HI)—Offset 2CCh" on page 4141	00000000h
2D0–2D3h	4	"RawSrcTran Interrupt Raw Status Registers - LOW (RawSrcTran_LO)—Offset 2D0h" on page 4141	00000000h
2D4–2D7h	4	"RawSrcTran Interrupt Raw Status Registers - HIGH (RawSrcTran_HI)—Offset 2D4h" on page 4142	00000000h
2D8–2DBh	4	"RawDstTran Interrupt Raw Status Registers - LOW (RawDstTran_LO)—Offset 2D8h" on page 4142	00000000h
2DC–2DFh	4	"RawDstTran Interrupt Raw Status Registers - HIGH (RawDstTran_HI)—Offset 2DCh" on page 4143	00000000h
2E0–2E3h	4	"RawErr Interrupt Raw Status Registers - LOW (RawErr_LO)—Offset 2E0h" on page 4143	00000000h
2E4–2E7h	4	"RawErr Interrupt Raw Status Registers - HIGH (RawErr_HI)—Offset 2E4h" on page 4144	00000000h
2E8–2EBh	4	"StatusTfr Interrupt Status Registers - LOW (StatusTfr_LO)—Offset 2E8h" on page 4144	00000000h
2EC–2EFh	4	"StatusTfr Interrupt Status Registers - HIGH (StatusTfr_HI)—Offset 2ECh" on page 4145	00000000h
2F0–2F3h	4	"StatusBlock Interrupt Status Registers - LOW (StatusBlock_LO)—Offset 2F0h" on page 4145	00000000h
2F4–2F7h	4	"StatusBlock Interrupt Status Registers - HIGH (StatusBlock_HI)—Offset 2F4h" on page 4146	00000000h
2F8–2FBh	4	"StatusSrcTran Interrupt Status Registers - LOW (StatusSrcTran_LO)—Offset 2F8h" on page 4146	00000000h
2FC–2FFh	4	"StatusSrcTran Interrupt Status Registers - HIGH (StatusSrcTran_HI)—Offset 2FCh" on page 4147	00000000h
300–303h	4	"StatusDstTran Interrupt Status Registers - LOW (StatusDstTran_LO)—Offset 300h" on page 4147	00000000h
304–307h	4	"StatusDstTran Interrupt Status Registers - HIGH (StatusDstTran_HI)—Offset 304h" on page 4148	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
308–30Bh	4	"StatusErr Interrupt Status Registers - LOW (StatusErr_LO)—Offset 308h" on page 4148	00000000h
30C–30Fh	4	"StatusErr Interrupt Status Registers - HIGH (StatusErr_HI)—Offset 30Ch" on page 4149	00000000h
310–313h	4	"MaskTfr Interrupt Mask Registers - LOW (MaskTfr_LO)—Offset 310h" on page 4149	00000000h
314–317h	4	"MaskTfr Interrupt Mask Registers - HIGH (MaskTfr_HI)—Offset 314h" on page 4150	00000000h
318–31Bh	4	"MaskBlock Interrupt Mask Registers - LOW (MaskBlock_LO)—Offset 318h" on page 4151	00000000h
31C–31Fh	4	"MaskBlock Interrupt Mask Registers - HIGH (MaskBlock_HI)—Offset 31Ch" on page 4151	00000000h
320–323h	4	"MaskSrcTran Interrupt Mask Registers - LOW (MaskSrcTran_LO)—Offset 320h" on page 4152	00000000h
324–327h	4	"MaskSrcTran Interrupt Mask Registers - HIGH (MaskSrcTran_HI)—Offset 324h" on page 4152	00000000h
328–32Bh	4	"MaskDstTran Interrupt Mask Registers - LOW (MaskDstTran_LO)—Offset 328h" on page 4153	00000000h
32C–32Fh	4	"MaskDstTran Interrupt Mask Registers - HIGH (MaskDstTran_HI)—Offset 32Ch" on page 4153	00000000h
330–333h	4	"MaskErr Interrupt Mask Registers - LOW (MaskErr_LO)—Offset 330h" on page 4154	00000000h
334–337h	4	"MaskErr Interrupt Mask Registers - HIGH (MaskErr_HI)—Offset 334h" on page 4155	00000000h
338–33Bh	4	"ClearTfr Interrupt Clear Registers - LOW (ClearTfr_LO)—Offset 338h" on page 4155	00000000h
33C–33Fh	4	"ClearTfr Interrupt Clear Registers - HIGH (ClearTfr_HI)—Offset 33Ch" on page 4156	00000000h
340–343h	4	"ClearBlock Interrupt Clear Registers - LOW (ClearBlock_LO)—Offset 340h" on page 4156	00000000h
344–347h	4	"ClearBlock Interrupt Clear Registers - HIGH (ClearBlock_HI)—Offset 344h" on page 4157	00000000h
348–34Bh	4	"ClearSrcTran Interrupt Clear Registers - LOW (ClearSrcTran_LO)—Offset 348h" on page 4157	00000000h
34C–34Fh	4	"ClearSrcTran Interrupt Clear Registers - HIGH (ClearSrcTran_HI)—Offset 34Ch" on page 4158	00000000h
350–353h	4	"ClearDstTran Interrupt Clear Registers - LOW (ClearDstTran_LO)—Offset 350h" on page 4158	00000000h
354–357h	4	"ClearDstTran Interrupt Clear Registers - HIGH (ClearDstTran_HI)—Offset 354h" on page 4159	00000000h
358–35Bh	4	"ClearErr Interrupt Clear Registers - LOW (ClearErr_LO)—Offset 358h" on page 4159	00000000h
35C–35Fh	4	"ClearErr Interrupt Clear Registers - HIGH (ClearErr_HI)—Offset 35Ch" on page 4160	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
360–363h	4	"Combined Interrupt Status Register - LOW (StatusInt_LO)—Offset 360h" on page 4160	00000000h
364–367h	4	"Combined Interrupt Status Register - HIGH (StatusInt_HI)—Offset 364h" on page 4161	00000000h
368–36Bh	4	"Source Software Transaction Request Register - LOW (ReqSrcReg_LO)—Offset 368h" on page 4161	00000000h
36C–36Fh	4	"Source Software Transaction Request Register - HIGH (ReqSrcReg_HI)—Offset 36Ch" on page 4162	00000000h
370–373h	4	"Destination Software Transaction Request Register - LOW (ReqDstReg_LO)—Offset 370h" on page 4162	00000000h
374–377h	4	"Destination Software Transaction Request Register - HIGH (ReqDstReg_HI)—Offset 374h" on page 4163	00000000h
378–37Bh	4	"Single Source Transaction Request Register - LOW (SglRqSrcReg_LO)—Offset 378h" on page 4164	00000000h
37C–37Fh	4	"Single Source Transaction Request Register - HIGH (SglRqSrcReg_HI)—Offset 37Ch" on page 4164	00000000h
380–383h	4	"Single Destination Transaction Request Register - LOW (SglRqDstReg_LO)—Offset 380h" on page 4165	00000000h
384–387h	4	"Single Destination Transaction Request Register - HIGH (SglRqDstReg_HI)—Offset 384h" on page 4165	00000000h
388–38Bh	4	"Last Source Transaction Request Register - LOW (LstSrcReg_LO)—Offset 388h" on page 4166	00000000h
38C–38Fh	4	"Last Source Transaction Request Register - HIGH (LstSrcReg_HI)—Offset 38Ch" on page 4166	00000000h
390–393h	4	"Last Destination Transaction Request Register - LOW (LstDstReg_LO)—Offset 390h" on page 4167	00000000h
394–397h	4	"Last Destination Transaction Request Register - HIGH (LstDstReg_HI)—Offset 394h" on page 4168	00000000h
398–39Bh	4	"DW_ahb_dmac Configuration Register - LOW (DmaCfgReg_LO)—Offset 398h" on page 4168	00000000h
39C–39Fh	4	"DW_ahb_dmac Configuration Register - HIGH (DmaCfgReg_HI)—Offset 39Ch" on page 4169	00000000h
3A0–3A3h	4	"DW_ahb_dmac Channel Enable Register - LOW (ChEnReg_LO)—Offset 3A0h" on page 4169	00000000h
3A4–3A7h	4	"DW_ahb_dmac Channel Enable Register - HIGH (ChEnReg_HI)—Offset 3A4h" on page 4170	00000000h
3A8–3ABh	4	"DW_ahb_dmac ID Register - LOW (DmaIdReg_LO)—Offset 3A8h" on page 4170	C0CAC01Ah
3AC–3AFh	4	"DW_ahb_dmac ID Register - HIGH (DmaIdReg_HI)—Offset 3ACh" on page 4171	00000000h
3B0–3B3h	4	"DW_ahb_dmac Test Register - LOW (DmaTestReg_LO)—Offset 3B0h" on page 4171	00000000h
3B4–3B7h	4	"DW_ahb_dmac Test Register - HIGH (DmaTestReg_HI)—Offset 3B4h" on page 4172	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3C8–3CBh	4	"DW_ahb_dmac Component Parameters Register 6 - LOW (DMA_COMP_PARAMS_6_LO)—Offset 3C8h" on page 4172	00000000h
3CC–3CFh	4	"DW_ahb_dmac Component Parameters Register 6 - HIGH (DMA_COMP_PARAMS_6_HI)—Offset 3CCh" on page 4173	38220300h
3D0–3D3h	4	"DW_ahb_dmac Component Parameters Register 5 - LOW (DMA_COMP_PARAMS_5_LO)—Offset 3D0h" on page 4175	38220300h
3D4–3D7h	4	"DW_ahb_dmac Component Parameters Register 5 - HIGH (DMA_COMP_PARAMS_5_HI)—Offset 3D4h" on page 4176	38220300h
3D8–3DBh	4	"DW_ahb_dmac Component Parameters Register 4 - LOW (DMA_COMP_PARAMS_4_LO)—Offset 3D8h" on page 4178	38220300h
3DC–3DFh	4	"DW_ahb_dmac Component Parameters Register 4 - HIGH (DMA_COMP_PARAMS_4_HI)—Offset 3DCh" on page 4180	38220300h
3E0–3E3h	4	"DW_ahb_dmac Component Parameters Register 3 - LOW (DMA_COMP_PARAMS_3_LO)—Offset 3E0h" on page 4182	38220300h
3E4–3E7h	4	"DW_ahb_dmac Component Parameters Register 3 - HIGH (DMA_COMP_PARAMS_3_HI)—Offset 3E4h" on page 4183	38220300h
3E8–3EBh	4	"DW_ahb_dmac Component Parameters Register 2 - LOW (DMA_COMP_PARAMS_2_LO)—Offset 3E8h" on page 4185	38220300h
3EC–3EFh	4	"DW_ahb_dmac Component Parameters Register 2 - HIGH (DMA_COMP_PARAMS_2_HI)—Offset 3ECh" on page 4187	00000000h
3F0–3F3h	4	"DW_ahb_dmac Component Parameters Register 1 - LOW (DMA_COMP_PARAMS_1_LO)—Offset 3F0h" on page 4188	AAAAAAAAh
3F4–3F7h	4	"DW_ahb_dmac Component Parameters Register 1 - HIGH (DMA_COMP_PARAMS_1_HI)—Offset 3F4h" on page 4190	37000F04h
3F8–3FBh	4	"DMA Component ID Register - LOW (DmaCompsID_LO)—Offset 3F8h" on page 4191	44571110h
3FC–3FFh	4	"DMA Component ID Register - HIGH (DmaCompsID_HI)—Offset 3FCh" on page 4192	3231362Ah

9.4.1 Source Address Register for Channel 0 - LOW (SAR0_LO)—Offset 0h

Source Address Register for Channel 0

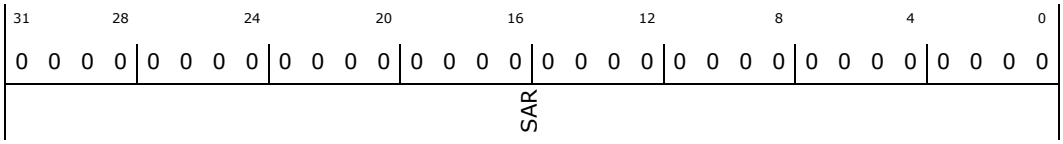
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

9.4.2 Source Address Register for Channel 0 - HIGH (SAR0_HI)—Offset 4h

Source Address Register for Channel 0

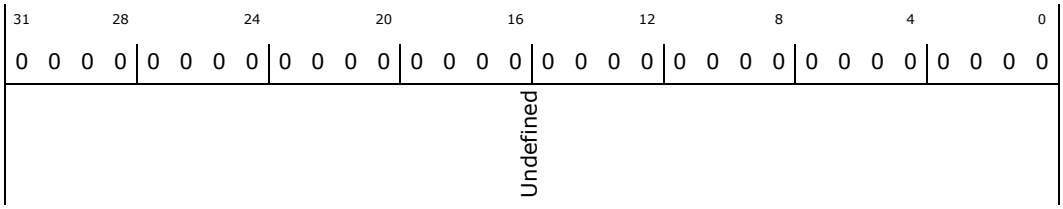
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.4.3 Destination Address Register for Channel 0 - LOW (DAR0_LO)—Offset 8h

Destination Address Register for Channel 0

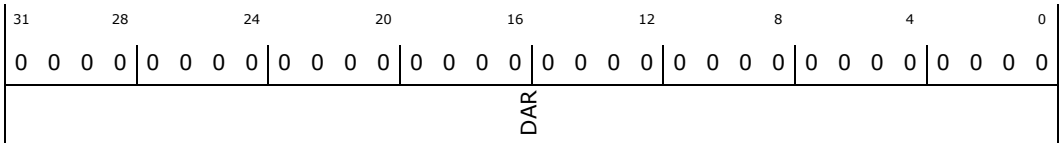
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

9.4.4 Destination Address Register for Channel 0 - HIGH (DAR0_HI)—Offset Ch

Destination Address Register for Channel 0

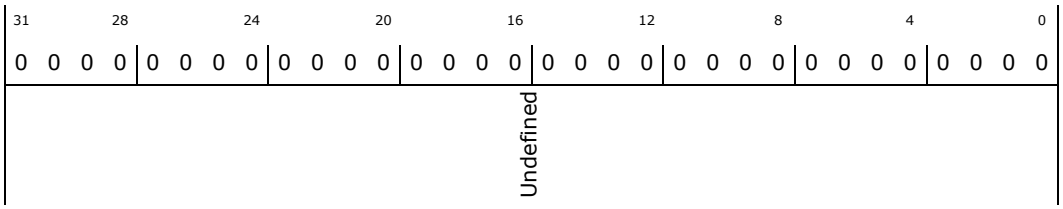
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.5 Linked List Pointer Register for Channel 0 - LOW (LLP0_LO)—Offset 10h

Linked List Pointer Register for Channel 0

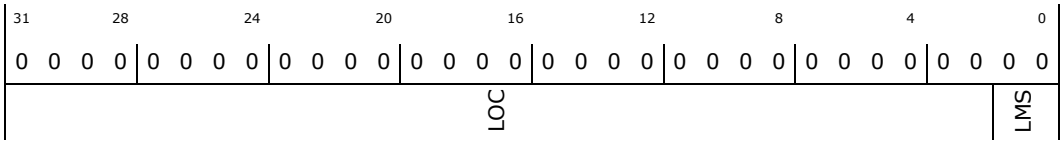
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0x0 RW	**LMS:** List Master Select. Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

9.4.6 Linked List Pointer Register for Channel 0 - HIGH (LLP0_HI)—Offset 14h

Linked List Pointer Register for Channel 0

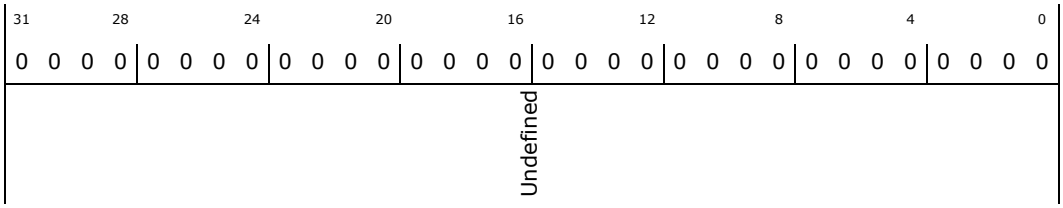
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.4.7 Control Register for Channel 0 - LOW (CTL0_LO)—Offset 18h

Control Register for Channel 0

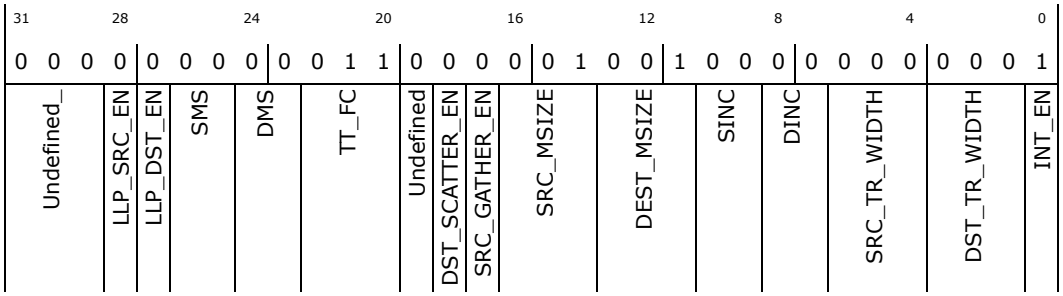
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**Undefined_:** RESERVED
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0x0 RW	**SMS:** Source Master Select. Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0x0 RW	**DMS:** Destination Master Select. Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	0x3 RW	**TT_FC:** Transfer Type and Flow Control.
19	0x0 RW	**Undefined:** RESERVED
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit. 0 = disabled 1 = enabled
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit. 0 = disabled 1 = enabled
16:14	0x1 RW	**SRC_MSIZE:** Source Burst Transaction Length.
13:11	0x1 RW	**DEST_MSIZE:** Destination Burst Transaction Length.
10:9	0x0 RW	**SINC:** Source Address Increment. 00 = Increment 01 = Decrement 1x = No change

Bit Range	Default & Access	Field Name (ID): Description
8:7	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. 00 = Increment 01 = Decrement 1x = No change
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	0x1 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

9.4.8 Control Register for Channel 0 - HIGH (CTL0_HI)—Offset 1Ch

Control Register for Channel 0

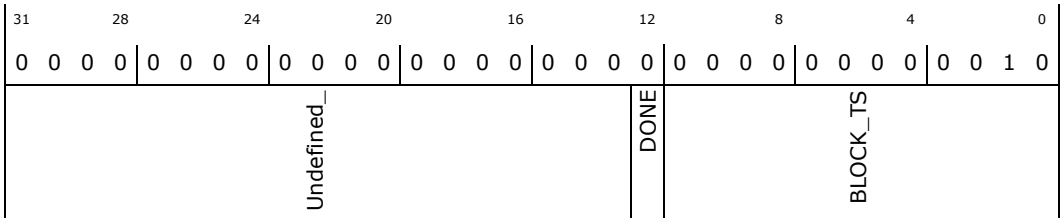
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Undefined_:** RESERVED
12	0x0 RW	**DONE:** Done bit
11:0	0x2 RW	**BLOCK_TS:** Block Transfer Size. When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

9.4.9 Configuration register for Channel 0 - LOW (CFG0_LO)—Offset 40h

Configuration register for Channel 0

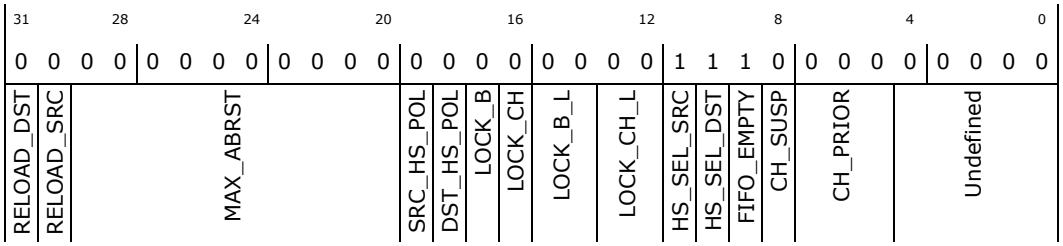
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000E00h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0x0 RW	**MAX_ABRST:** Maximum AMBA Burst Length. Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**LOCK_B:** Bus Lock Bit. When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0x0 RW	**LOCK_CH:** Channel Lock Bit. When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0x0 RW	**LOCK_B_L:** Bus Lock Level. Indicates the duration over which CFGx.LOCK_B bit applies. 00 = Over complete DMA transfer 01 = Over complete DMA block transfer 1x = Over complete DMA transaction
13:12	0x0 RW	**LOCK_CH_L:** Channel Lock Level. Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	0x1 RW	**HS_SEL_SRC:** Source Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
10	0x1 RW	**HS_SEL_DST:** Destination Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking

Bit Range	Default & Access	Field Name (ID): Description
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA transfers from source until this bit is cleared.
7:5	0x0 RW	**CH_PRIOR:** Channel priority. Priority of 7 is the highest priority.
4:0	0x0 RW	**Undefined:** RESERVED

9.4.10 Configuration register for Channel 0 - HIGH (CFG0_HI)—Offset 44h

Configuration register for Channel 0 _ HIGH

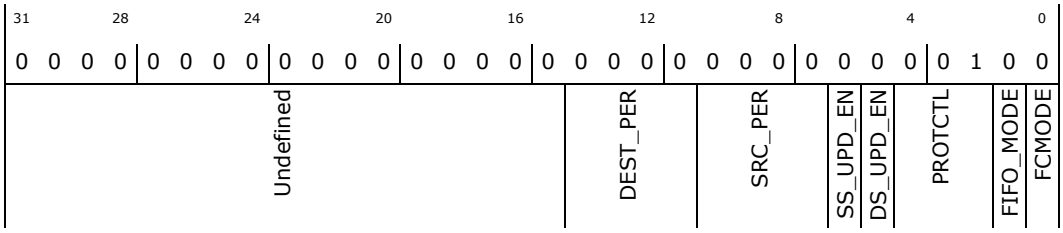
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RW	**Undefined:** Reserved
14:11	0x0 RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0x0 RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.

Bit Range	Default & Access	Field Name (ID): Description
4:2	0x1 RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0x0 RW	**FIFO_MODE:** FIFO Mode Select. Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0 = Space/data available for single AHB transfer of the specified transfer width. 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0x0 RW	**FCMODE:** Flow Control Mode. Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. 1 = Source transaction requests are not serviced until a destination transaction request occurs.

9.4.11 Source Gather Register for Channel 0 - LOW (SGR0_LO)—Offset 48h

Source Gather Register for Channel 0

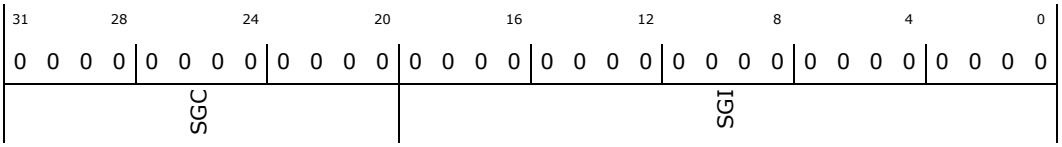
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval

9.4.12 Source Gather Register for Channel 0 - HIGH (SGR0_HI)—Offset 4Ch

Source Gather Register for Channel 0

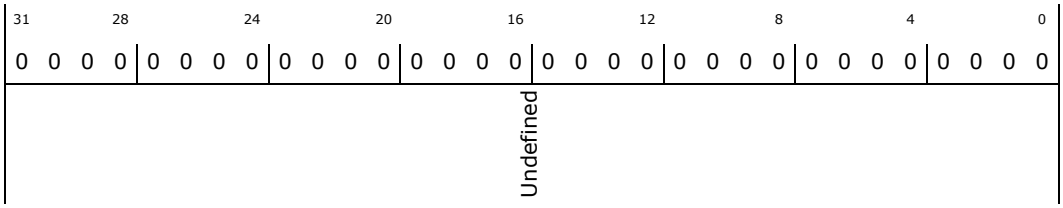
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.13 Destination Scatter Register for Channel 0 - LOW (DSR0_LO)—Offset 50h

Destination Scatter Register for Channel 0

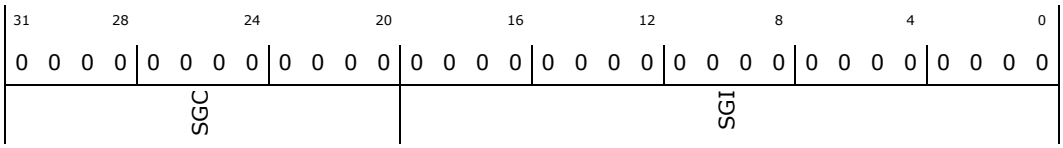
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC (SGC):** Dest scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI (SGI):** Dest scatter interval

9.4.14 Dest scatter Register for Channel 0 - HIGH (DSR0_HI)—Offset 54h

Dest scatter Register for Channel 0

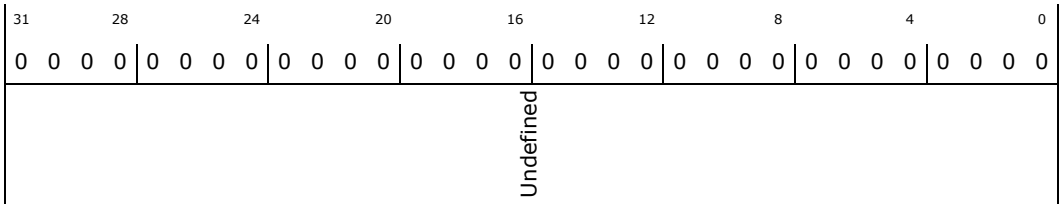
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.15 Source Address Register for Channel 1 - LOW (SAR1_LO)—Offset 58h

Source Address Register for Channel 1

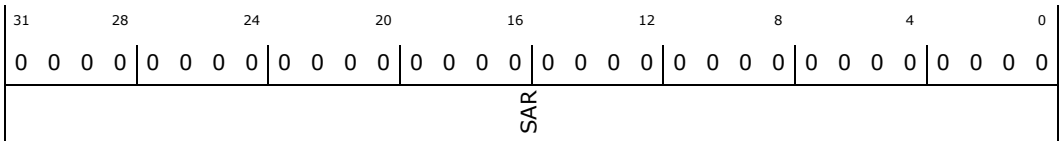
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

9.4.16 Source Address Register for Channel 1 - HIGH (SAR1_HI)—Offset 5Ch

Source Address Register for Channel 1

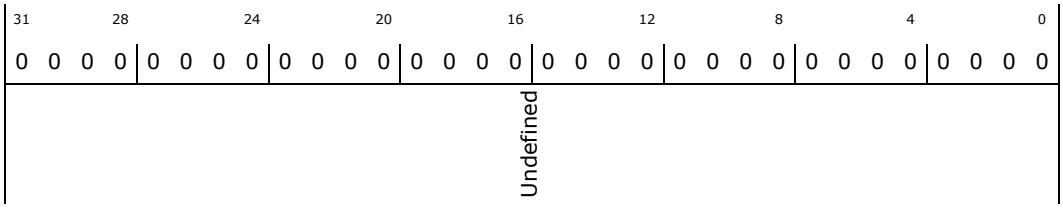
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.4.17 Destination Address Register for Channel 1 - LOW (DAR1_LO)—Offset 60h

Destination Address Register for Channel 1

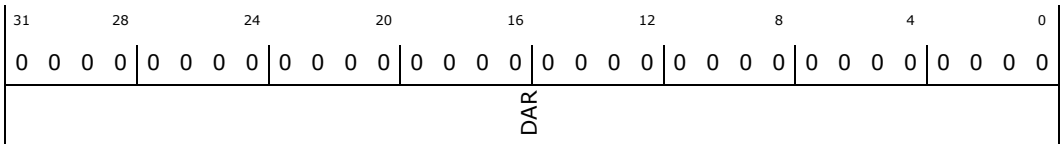
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

9.4.18 Destination Address Register for Channel 1 - HIGH (DAR1_HI)—Offset 64h

Destination Address Register for Channel 1

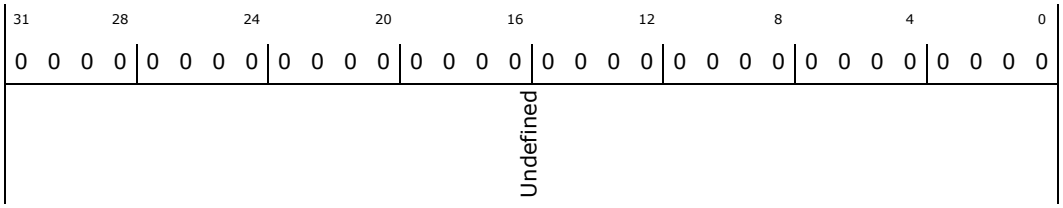
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.19 Linked List Pointer Register for Channel 1 - LOW (LLP1_LO)—Offset 68h

Linked List Pointer Register for Channel 1

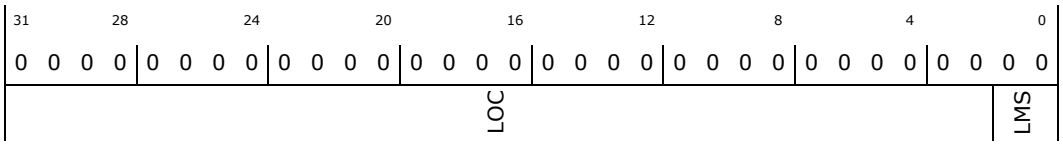
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0x0 RW	**LMS:** List Master Select. Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

9.4.20 Linked List Pointer Register for Channel 1 - HIGH (LLP1_HI)—Offset 6Ch

Linked List Pointer Register for Channel 1

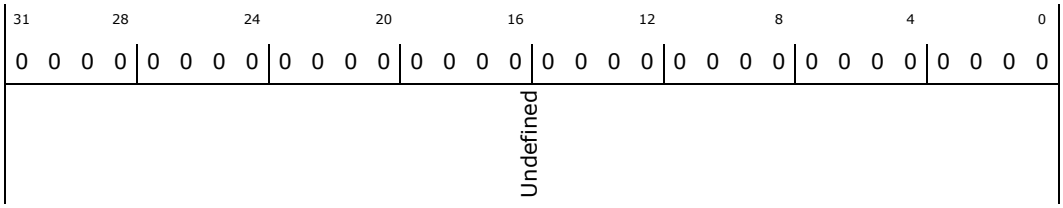
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.4.21 Control Register for Channel 1 - LOW (CTL1_LO)—Offset 70h

Control Register for Channel 1

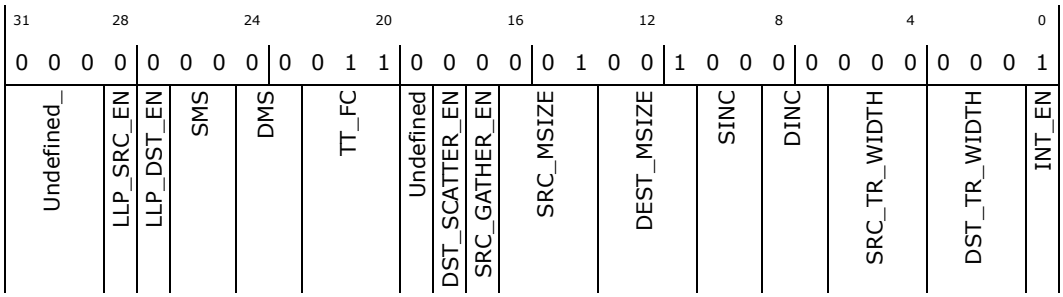
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

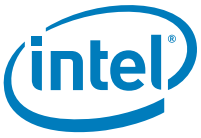
Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**Undefined_:** RESERVED
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.



Bit Range	Default & Access	Field Name (ID): Description
26:25	0x0 RW	**SMS:** Source Master Select. Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0x0 RW	**DMS:** Destination Master Select. Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	0x3 RW	**TT_FC:** Transfer Type and Flow Control.
19	0x0 RW	**Undefined:** RESERVED
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit. 0 = disabled 1 = enabled
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit. 0 = disabled 1 = enabled
16:14	0x1 RW	**SRC_MSIZE:** Source Burst Transaction Length.
13:11	0x1 RW	**DEST_MSIZE:** Destination Burst Transaction Length.
10:9	0x0 RW	**SINC:** Source Address Increment. 00 = Increment 01 = Decrement 1x = No change
8:7	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. 00 = Increment 01 = Decrement 1x = No change
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	0x1 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

9.4.22 Control Register for Channel 1 - HIGH (CTL1_HI)—Offset 74h

Control Register for Channel 1

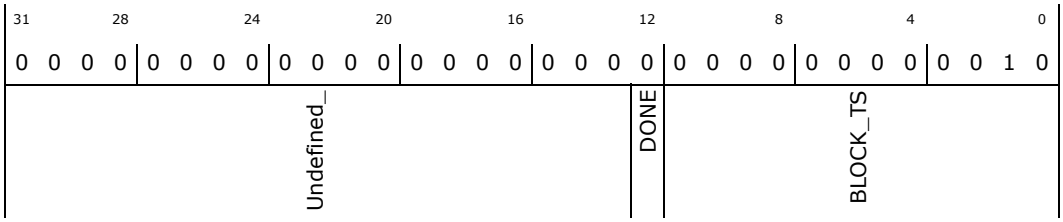
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Undefined_:** RESERVED
12	0x0 RW	**DONE:** Done bit
11:0	0x2 RW	**BLOCK_TS:** Block Transfer Size. When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

9.4.23 Configuration register for Channel 1 - LOW (CFG1_LO)—Offset 98h

Configuration register for Channel 1

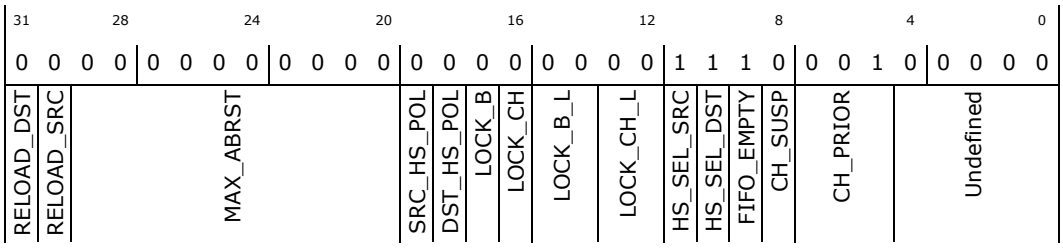
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000E20h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.

Bit Range	Default & Access	Field Name (ID): Description
29:20	0x0 RW	**MAX_ABRST:** Maximum AMBA Burst Length. Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**LOCK_B:** Bus Lock Bit. When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0x0 RW	**LOCK_CH:** Channel Lock Bit. When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0x0 RW	**LOCK_B_L:** Bus Lock Level. Indicates the duration over which CFGx.LOCK_B bit applies. 00 = Over complete DMA transfer 01 = Over complete DMA block transfer 1x = Over complete DMA transaction
13:12	0x0 RW	**LOCK_CH_L:** Channel Lock Level. Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	0x1 RW	**HS_SEL_SRC:** Source Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
10	0x1 RW	**HS_SEL_DST:** Destination Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA transfers from source until this bit is cleared.
7:5	0x1 RW	**CH_PRIOR:** Channel priority. Priority of 7 is the highest priority.
4:0	0x0 RW	**Undefined:** RESERVED

9.4.24 Configuration register for Channel 1 - HIGH (CFG1_HI)—Offset 9Ch

Configuration register for Channel 1 _ HIGH

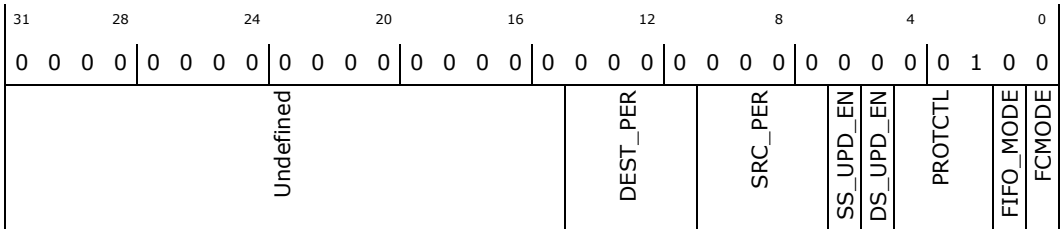
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RW	**Undefined:** Reserved
14:11	0x0 RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0x0 RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	0x1 RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0x0 RW	**FIFO_MODE:** FIFO Mode Select. Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0 = Space/data available for single AHB transfer of the specified transfer width. 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0x0 RW	**FCMODE:** Flow Control Mode. Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. 1 = Source transaction requests are not serviced until a destination transaction request occurs.

9.4.25 Source Gather Register for Channel 1 - LOW (SGR1_LO)—Offset A0h

Source Gather Register for Channel 1

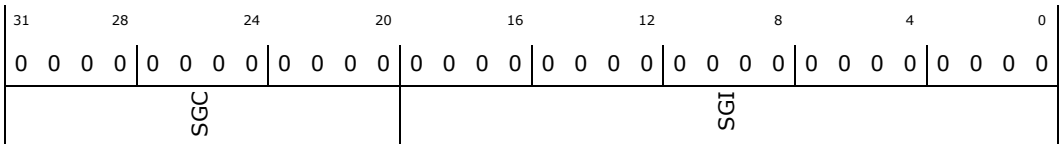
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval

9.4.26 Source Gather Register for Channel 1 - HIGH (SGR1_HI)—Offset A4h

Source Gather Register for Channel 1

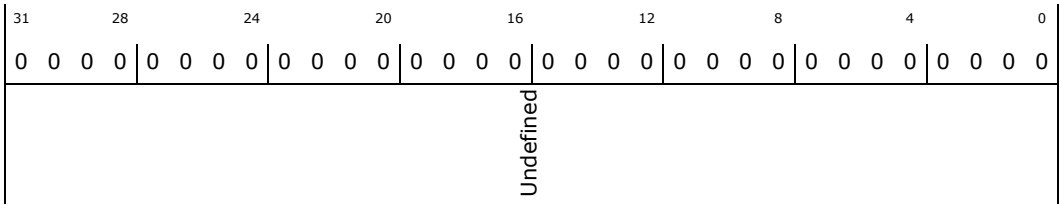
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.27 Destination Scatter Register for Channel 1 - LOW (DSR1_LO)—Offset A8h

Destination Scatter Register for Channel 1

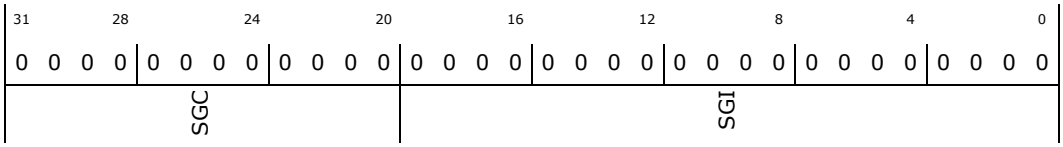
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC (SGC):** Dest scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI (SGI):** Dest scatter interval

9.4.28 Dest scatter Register for Channel 1 - HIGH (DSR1_HI)—Offset ACh

Dest scatter Register for Channel 1

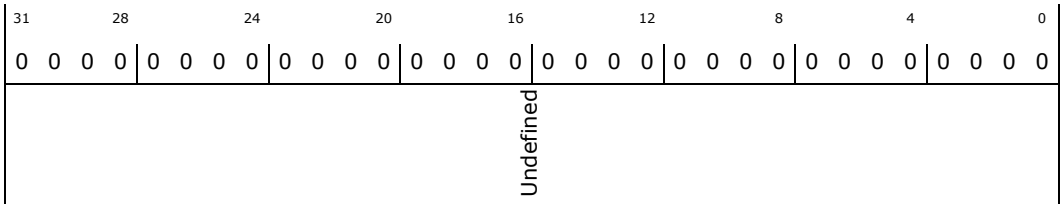
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.29 Source Address Register for Channel 2 - LOW (SAR2_LO)—Offset B0h

Source Address Register for Channel 2

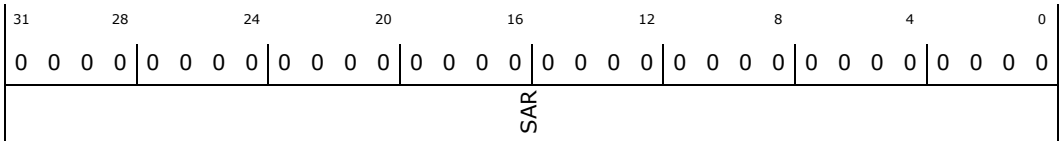
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

9.4.30 Source Address Register for Channel 2 - HIGH (SAR2_HI)—Offset B4h

Source Address Register for Channel 2

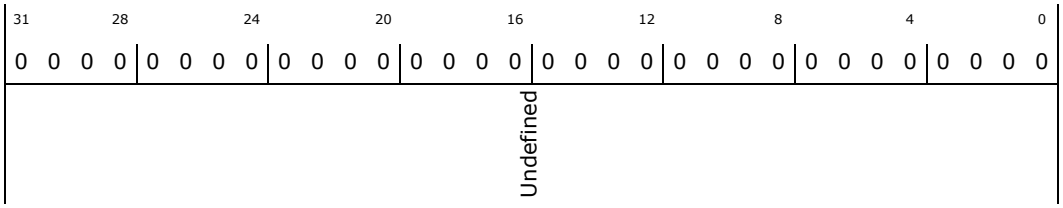
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.4.31 Destination Address Register for Channel 2 - LOW (DAR2_LO)—Offset B8h

Destination Address Register for Channel 2

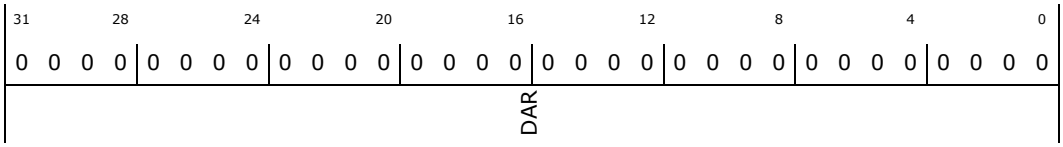
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

9.4.32 Destination Address Register for Channel 2 - HIGH (DAR2_HI)—Offset BCh

Destination Address Register for Channel 2

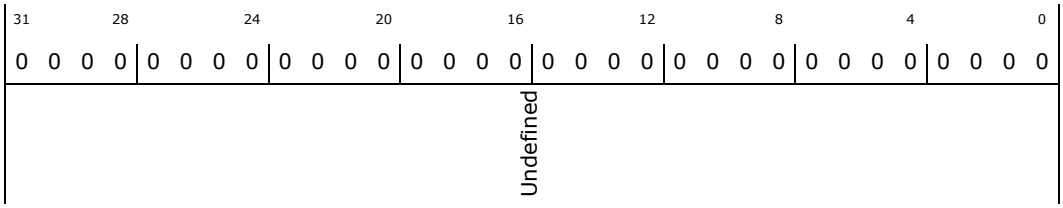
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.33 Linked List Pointer Register for Channel 2 - LOW (LLP2_LO)—Offset C0h

Linked List Pointer Register for Channel 2

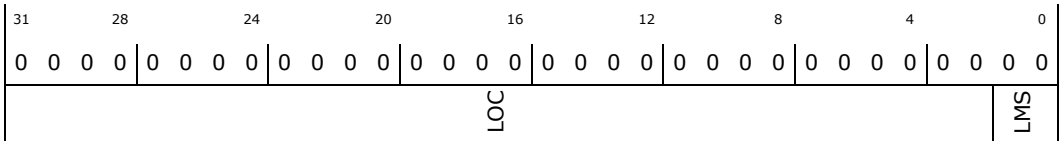
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0x0 RW	**LMS:** List Master Select. Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

9.4.34 Linked List Pointer Register for Channel 2 - HIGH (LLP2_HI)—Offset C4h

Linked List Pointer Register for Channel 2

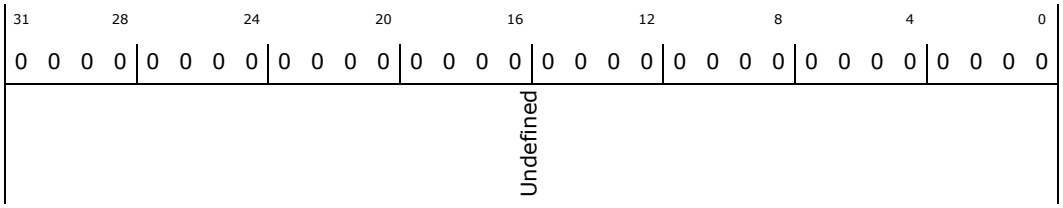
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.4.35 Control Register for Channel 2 - LOW (CTL2_LO)—Offset C8h

Control Register for Channel 2

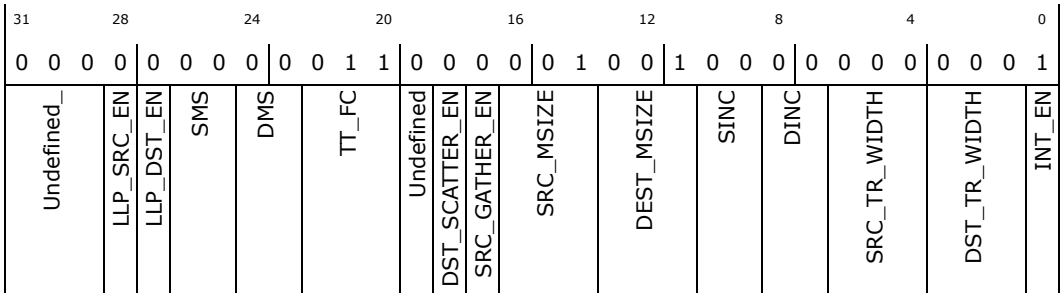
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**Undefined_:** RESERVED
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0x0 RW	**SMS:** Source Master Select. Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0x0 RW	**DMS:** Destination Master Select. Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	0x3 RW	**TT_FC:** Transfer Type and Flow Control.
19	0x0 RW	**Undefined:** RESERVED
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit. 0 = disabled 1 = enabled
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit. 0 = disabled 1 = enabled
16:14	0x1 RW	**SRC_MSIZE:** Source Burst Transaction Length.
13:11	0x1 RW	**DEST_MSIZE:** Destination Burst Transaction Length.
10:9	0x0 RW	**SINC:** Source Address Increment. 00 = Increment 01 = Decrement 1x = No change
8:7	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. 00 = Increment 01 = Decrement 1x = No change
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	0x1 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

9.4.36 Control Register for Channel 2 - HIGH (CTL2_HI)—Offset CCh

Control Register for Channel 2

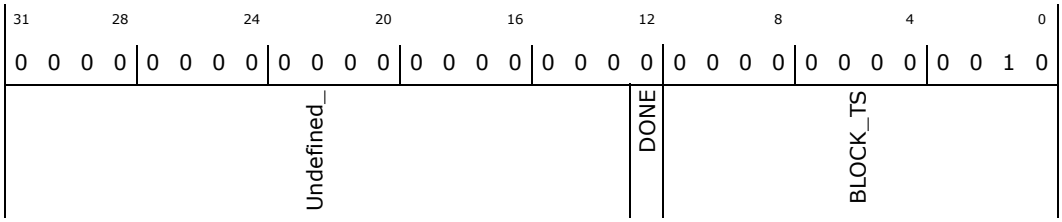
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Undefined_:** RESERVED
12	0x0 RW	**DONE:** Done bit
11:0	0x2 RW	**BLOCK_TS:** Block Transfer Size. When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

9.4.37 Configuration register for Channel 2 - LOW (CFG2_LO)—Offset F0h

Configuration register for Channel 2

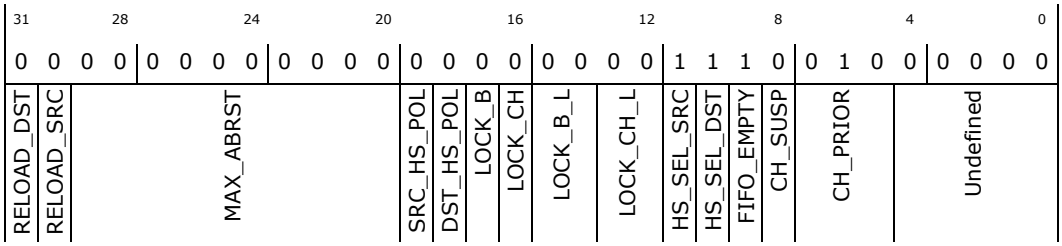
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000E40h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0x0 RW	**MAX_ABRST:** Maximum AMBA Burst Length. Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**LOCK_B:** Bus Lock Bit. When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0x0 RW	**LOCK_CH:** Channel Lock Bit. When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0x0 RW	**LOCK_B_L:** Bus Lock Level. Indicates the duration over which CFGx.LOCK_B bit applies. 00 = Over complete DMA transfer 01 = Over complete DMA block transfer 1x = Over complete DMA transaction
13:12	0x0 RW	**LOCK_CH_L:** Channel Lock Level. Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	0x1 RW	**HS_SEL_SRC:** Source Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
10	0x1 RW	**HS_SEL_DST:** Destination Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA transfers from source until this bit is cleared.
7:5	0x2 RW	**CH_PRIOR:** Channel priority. Priority of 7 is the highest priority.
4:0	0x0 RW	**Undefined:** RESERVED

9.4.38 Configuration register for Channel 2 - HIGH (CFG2_HI)—Offset F4h

Configuration register for Channel 2 _ HIGH

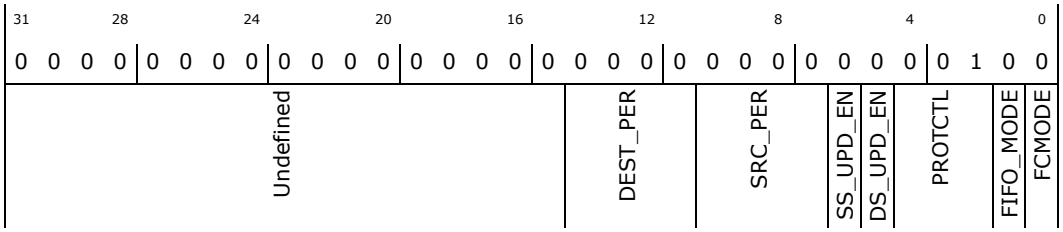
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RW	**Undefined:** Reserved
14:11	0x0 RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0x0 RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	0x1 RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0x0 RW	**FIFO_MODE:** FIFO Mode Select. Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0 = Space/data available for single AHB transfer of the specified transfer width. 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0x0 RW	**FCMODE:** Flow Control Mode. Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. 1 = Source transaction requests are not serviced until a destination transaction request occurs.

9.4.39 Source Gather Register for Channel 2 - LOW (SGR2_LO)—Offset F8h

Source Gather Register for Channel 2

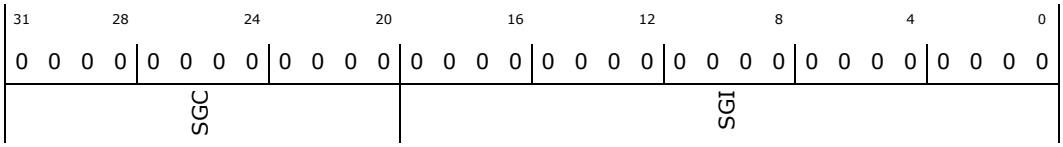
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval

9.4.40 Source Gather Register for Channel 2 - HIGH (SGR2_HI)—Offset FCh

Source Gather Register for Channel 2

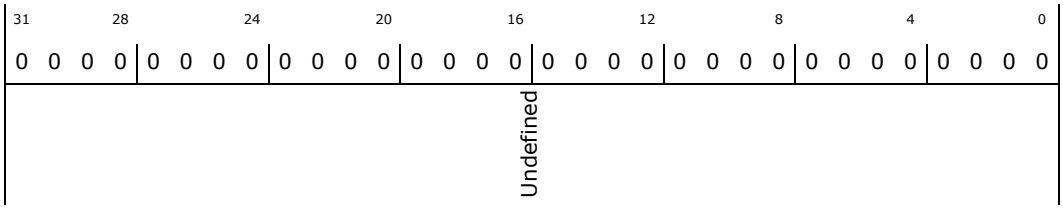
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.41 Destination Scatter Register for Channel 2 - LOW (DSR2_LO)—Offset 100h

Destination Scatter Register for Channel 2

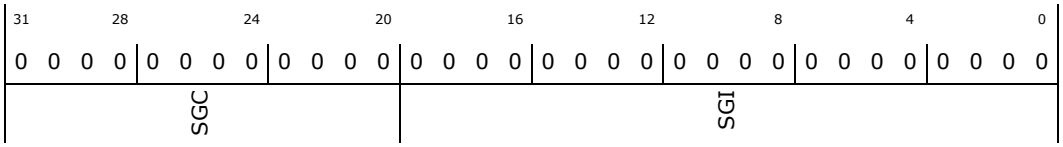
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 100h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC (SGC):** Dest scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI (SGI):** Dest scatter interval

9.4.42 Dest scatter Register for Channel 2 - HIGH (DSR2_HI)—Offset 104h

Dest scatter Register for Channel 2

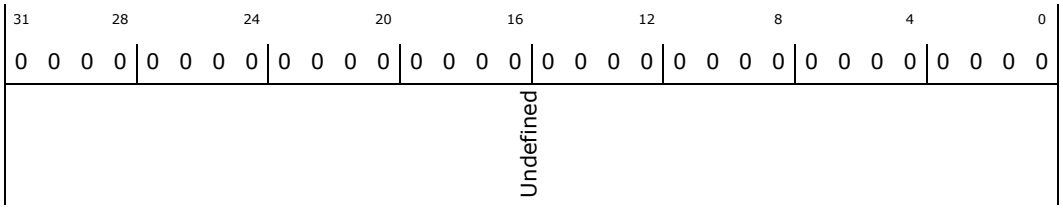
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 104h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.43 Source Address Register for Channel 3 - LOW (SAR3_LO)—Offset 108h

Source Address Register for Channel 3

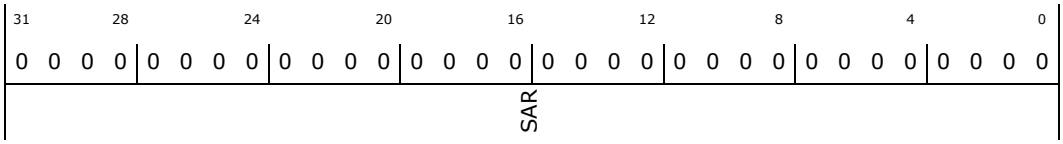
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 108h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

9.4.44 Source Address Register for Channel 3 - HIGH (SAR3_HI)—Offset 10Ch

Source Address Register for Channel 3

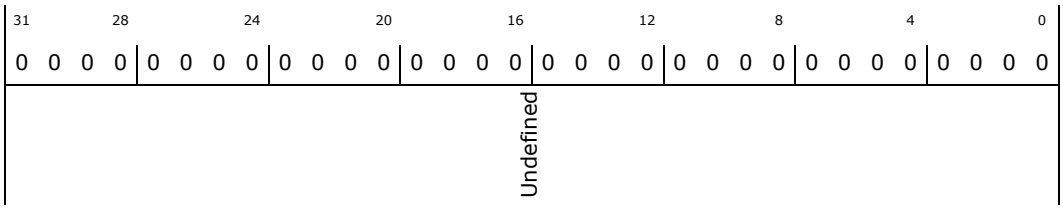
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.4.45 Destination Address Register for Channel 3 - LOW (DAR3_LO)—Offset 110h

Destination Address Register for Channel 3

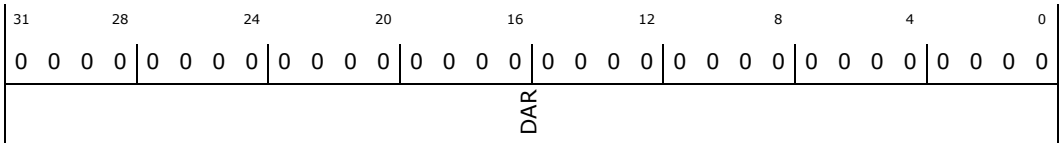
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 110h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

9.4.46 Destination Address Register for Channel 3 - HIGH (DAR3_HI)—Offset 114h

Destination Address Register for Channel 3

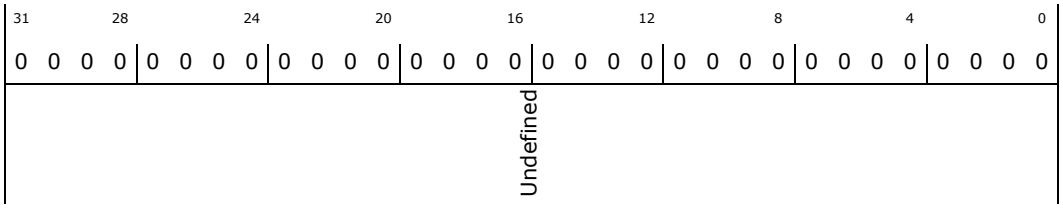
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 114h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.47 Linked List Pointer Register for Channel 3 - LOW (LLP3_LO)—Offset 118h

Linked List Pointer Register for Channel 3

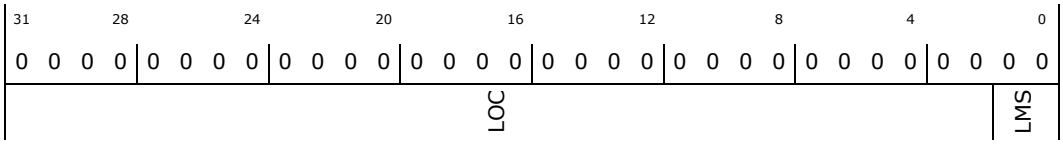
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 118h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0x0 RW	**LMS:** List Master Select. Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

9.4.48 Linked List Pointer Register for Channel 3 - HIGH (LLP3_HI)—Offset 11Ch

Linked List Pointer Register for Channel 3

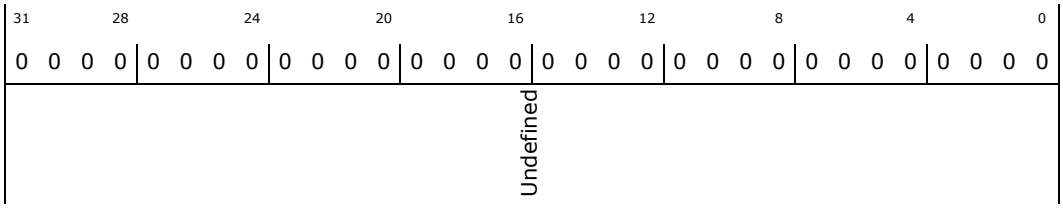
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 11Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.4.49 Control Register for Channel 3 - LOW (CTL3_LO)—Offset 120h

Control Register for Channel 3

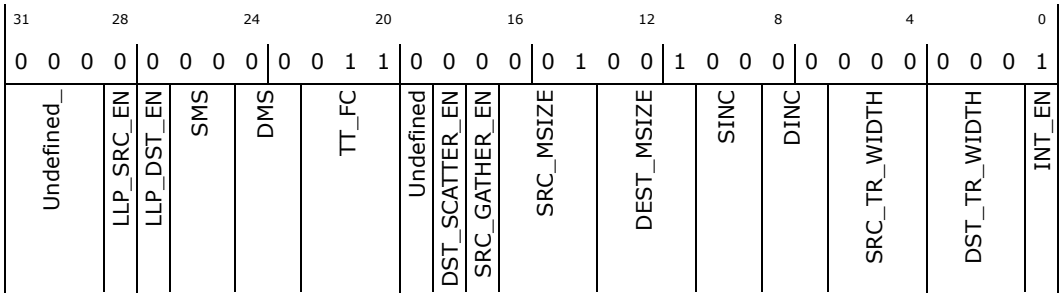
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 120h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**Undefined_:** RESERVED
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0x0 RW	**SMS:** Source Master Select. Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0x0 RW	**DMS:** Destination Master Select. Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	0x3 RW	**TT_FC:** Transfer Type and Flow Control.
19	0x0 RW	**Undefined:** RESERVED
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit. 0 = disabled 1 = enabled
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit. 0 = disabled 1 = enabled
16:14	0x1 RW	**SRC_MSIZE:** Source Burst Transaction Length.
13:11	0x1 RW	**DEST_MSIZE:** Destination Burst Transaction Length.
10:9	0x0 RW	**SINC:** Source Address Increment. 00 = Increment 01 = Decrement 1x = No change
8:7	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. 00 = Increment 01 = Decrement 1x = No change
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.

Bit Range	Default & Access	Field Name (ID): Description
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	0x1 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

9.4.50 Control Register for Channel 3 - HIGH (CTL3_HI)—Offset 124h

Control Register for Channel 3

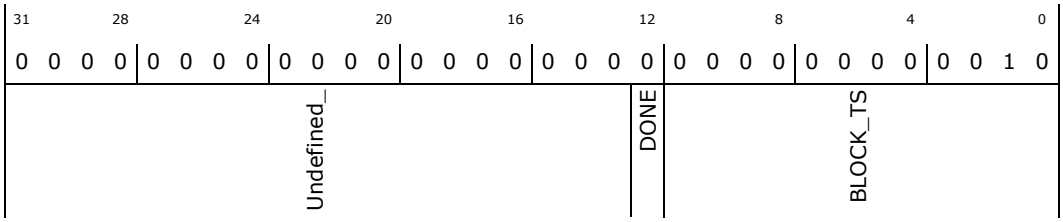
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 124h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Undefined_:** RESERVED
12	0x0 RW	**DONE:** Done bit
11:0	0x2 RW	**BLOCK_TS:** Block Transfer Size. When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

9.4.51 Configuration register for Channel 3 - LOW (CFG3_LO)—Offset 148h

Configuration register for Channel 3

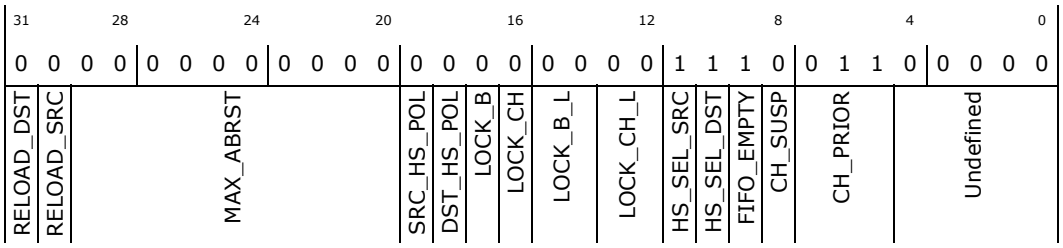
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 148h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000E60h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0x0 RW	**MAX_ABRST:** Maximum AMBA Burst Length. Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**LOCK_B:** Bus Lock Bit. When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0x0 RW	**LOCK_CH:** Channel Lock Bit. When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0x0 RW	**LOCK_B_L:** Bus Lock Level. Indicates the duration over which CFGx.LOCK_B bit applies. 00 = Over complete DMA transfer 01 = Over complete DMA block transfer 1x = Over complete DMA transaction
13:12	0x0 RW	**LOCK_CH_L:** Channel Lock Level. Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	0x1 RW	**HS_SEL_SRC:** Source Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
10	0x1 RW	**HS_SEL_DST:** Destination Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA transfers from source until this bit is cleared.
7:5	0x3 RW	**CH_PRIOR:** Channel priority. Priority of 7 is the highest priority.

Bit Range	Default & Access	Field Name (ID): Description
4:0	0x0 RW	**Undefined:** RESERVED

9.4.52 Configuration register for Channel 3 - HIGH (CFG3_HI)—Offset 14Ch

Configuration register for Channel 3 _ HIGH

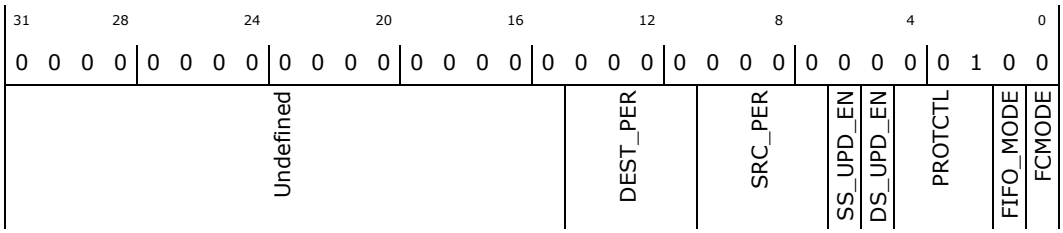
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RW	**Undefined:** Reserved
14:11	0x0 RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0x0 RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	0x1 RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**FIFO_MODE:** FIFO Mode Select. Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0 = Space/data available for single AHB transfer of the specified transfer width. 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0x0 RW	**FCMODE:** Flow Control Mode. Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. 1 = Source transaction requests are not serviced until a destination transaction request occurs.

9.4.53 Source Gather Register for Channel 3 - LOW (SGR3_LO)—Offset 150h

Source Gather Register for Channel 3

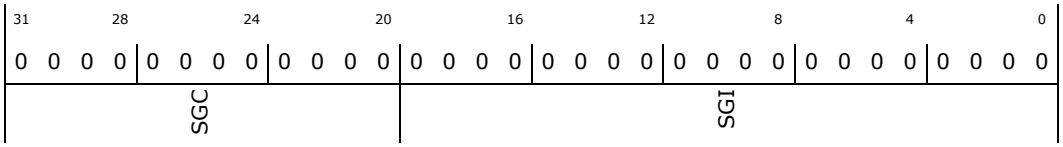
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 150h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval

9.4.54 Source Gather Register for Channel 3 - HIGH (SGR3_HI)—Offset 154h

Source Gather Register for Channel 3

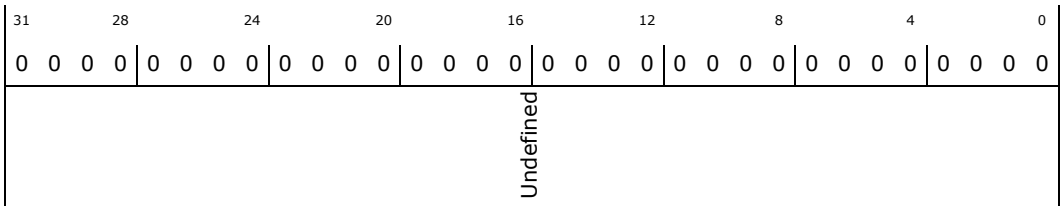
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 154h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.55 Destination Scatter Register for Channel 3 - LOW (DSR3_LO)—Offset 158h

Destination Scatter Register for Channel 3

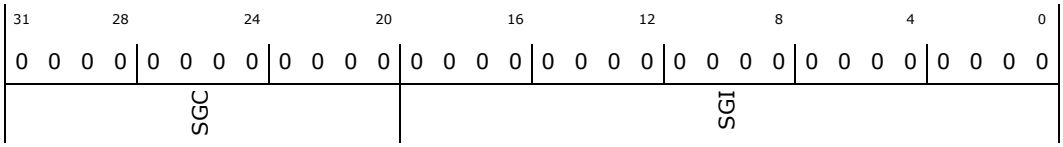
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 158h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC (SGC):** Dest scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI (SGI):** Dest scatter interval

9.4.56 Dest scatter Register for Channel 3 - HIGH (DSR3_HI)—Offset 15Ch

Dest scatter Register for Channel 3

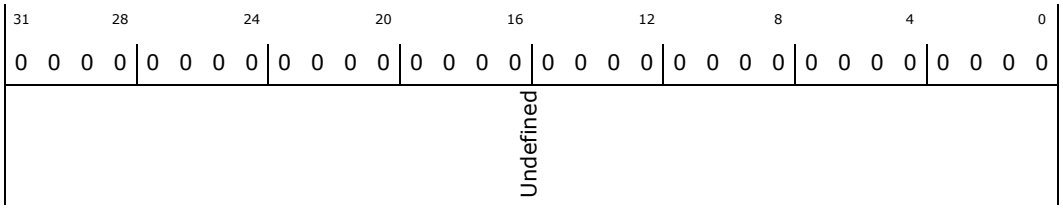
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 15Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.57 Source Address Register for Channel 4 - LOW (SAR4_LO)—Offset 160h

Source Address Register for Channel 4

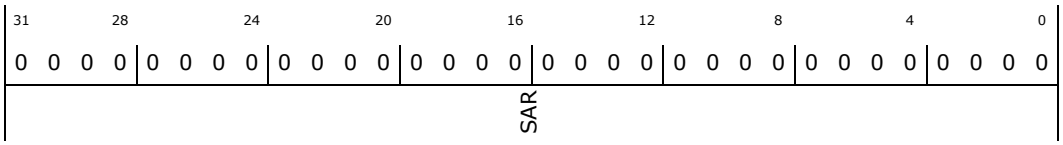
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 160h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

9.4.58 Source Address Register for Channel 4 - HIGH (SAR4_HI)—Offset 164h

Source Address Register for Channel 4

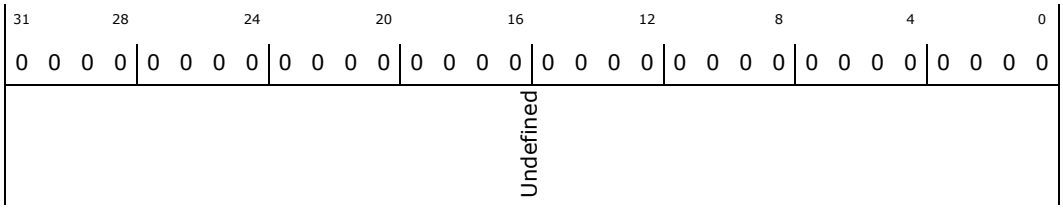
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 164h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.4.59 Destination Address Register for Channel 4 - LOW (DAR4_LO)—Offset 168h

Destination Address Register for Channel 4

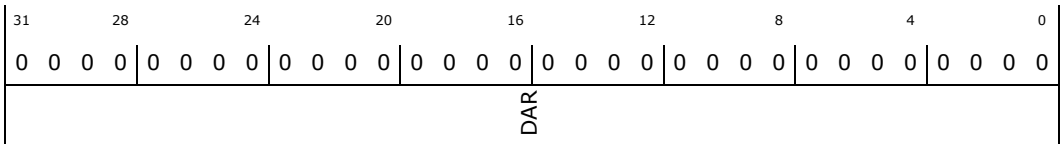
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 168h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

9.4.60 Destination Address Register for Channel 4 - HIGH (DAR4_HI)—Offset 16Ch

Destination Address Register for Channel 4

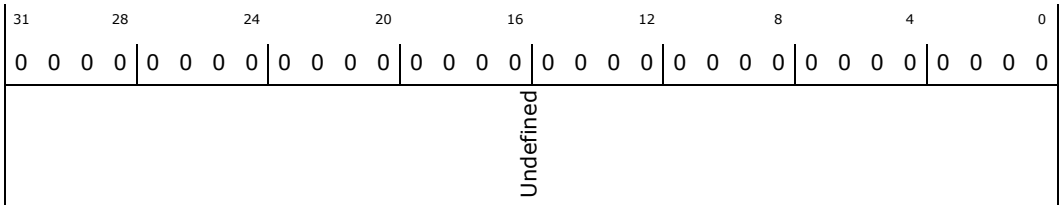
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 16Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.61 Linked List Pointer Register for Channel 4 - LOW (LLP4_LO)—Offset 170h

Linked List Pointer Register for Channel 4

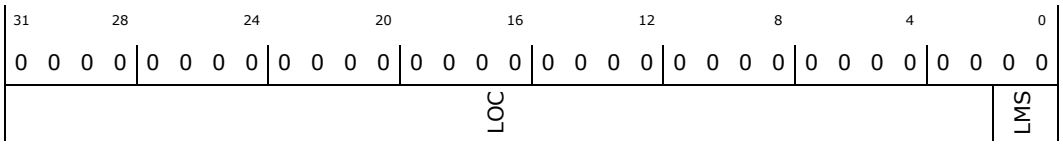
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 170h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0x0 RW	**LMS:** List Master Select. Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

9.4.62 Linked List Pointer Register for Channel 4 - HIGH (LLP4_HI)—Offset 174h

Linked List Pointer Register for Channel 4

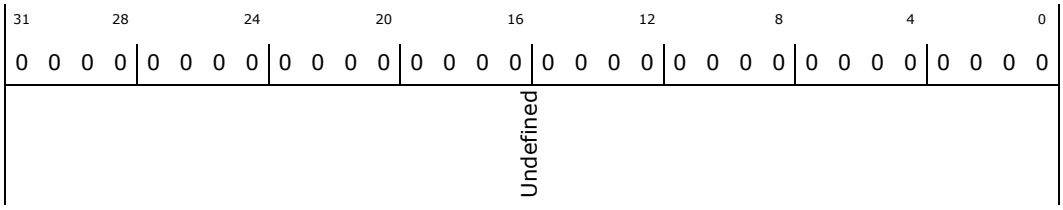
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 174h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.4.63 Control Register for Channel 4 - LOW (CTL4_LO)—Offset 178h

Control Register for Channel 4

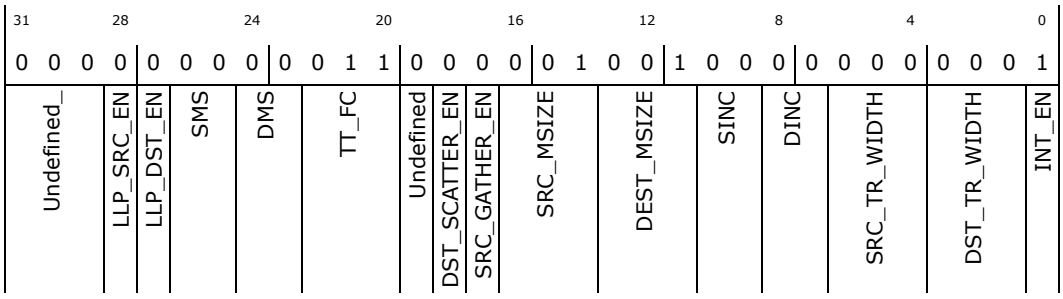
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 178h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**Undefined_:** RESERVED
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0x0 RW	**SMS:** Source Master Select. Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0x0 RW	**DMS:** Destination Master Select. Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	0x3 RW	**TT_FC:** Transfer Type and Flow Control.

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RW	**Undefined:** RESERVED
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit. 0 = disabled 1 = enabled
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit. 0 = disabled 1 = enabled
16:14	0x1 RW	**SRC_MSIZE:** Source Burst Transaction Length.
13:11	0x1 RW	**DEST_MSIZE:** Destination Burst Transaction Length.
10:9	0x0 RW	**SINC:** Source Address Increment. 00 = Increment 01 = Decrement 1x = No change
8:7	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. 00 = Increment 01 = Decrement 1x = No change
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	0x1 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

9.4.64 Control Register for Channel 4 - HIGH (CTL4_HI)—Offset 17Ch

Control Register for Channel 4

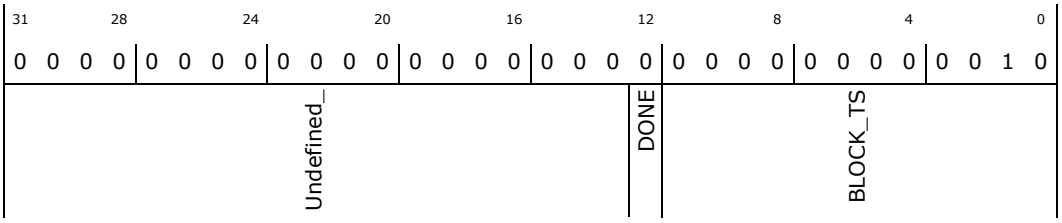
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 17Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Undefined_:** RESERVED
12	0x0 RW	**DONE:** Done bit
11:0	0x2 RW	**BLOCK_TS:** Block Transfer Size. When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

9.4.65 Configuration register for Channel 4 - LOW (CFG4_LO)—Offset 1A0h

Configuration register for Channel 4

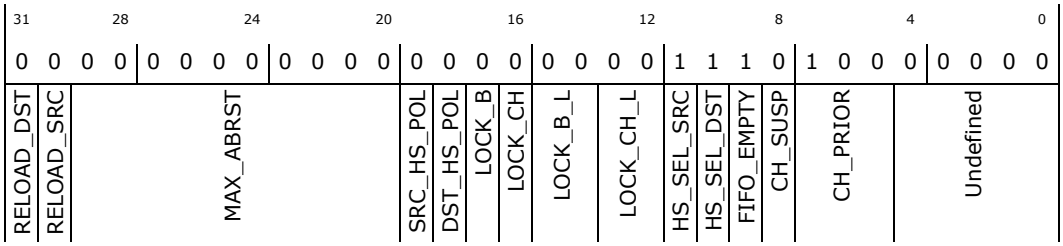
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000E80h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0x0 RW	**MAX_ABRST:** Maximum AMBA Burst Length. Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**LOCK_B:** Bus Lock Bit. When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW	**LOCK_CH:** Channel Lock Bit. When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0x0 RW	**LOCK_B_L:** Bus Lock Level. Indicates the duration over which CFGx.LOCK_B bit applies. 00 = Over complete DMA transfer 01 = Over complete DMA block transfer 1x = Over complete DMA transaction
13:12	0x0 RW	**LOCK_CH_L:** Channel Lock Level. Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	0x1 RW	**HS_SEL_SRC:** Source Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
10	0x1 RW	**HS_SEL_DST:** Destination Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA transfers from source until this bit is cleared.
7:5	0x4 RW	**CH_PRIOR:** Channel priority. Priority of 7 is the highest priority.
4:0	0x0 RW	**Undefined:** RESERVED

9.4.66 Configuration register for Channel 4 - HIGH (CFG4_HI)—Offset 1A4h

Configuration register for Channel 4 _ HIGH

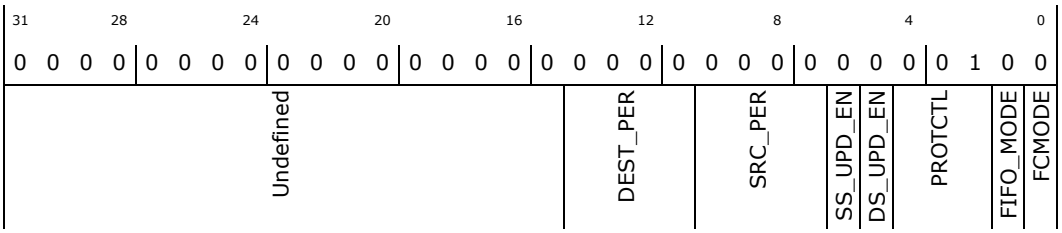
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RW	**Undefined:** Reserved
14:11	0x0 RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0x0 RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	0x1 RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0x0 RW	**FIFO_MODE:** FIFO Mode Select. Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0 = Space/data available for single AHB transfer of the specified transfer width. 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0x0 RW	**FCMODE:** Flow Control Mode. Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. 1 = Source transaction requests are not serviced until a destination transaction request occurs.

9.4.67 Source Gather Register for Channel 4 - LOW (SGR4_LO)—Offset 1A8h

Source Gather Register for Channel 4

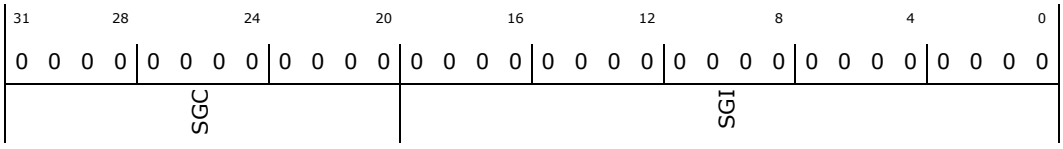
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval

9.4.68 Source Gather Register for Channel 4 - HIGH (SGR4_HI)—Offset 1ACh

Source Gather Register for Channel 4

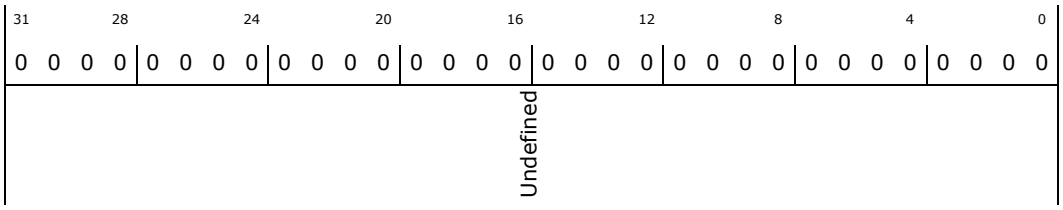
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.69 Destination Scatter Register for Channel 4 - LOW (DSR4_LO)—Offset 1B0h

Destination Scatter Register for Channel 4

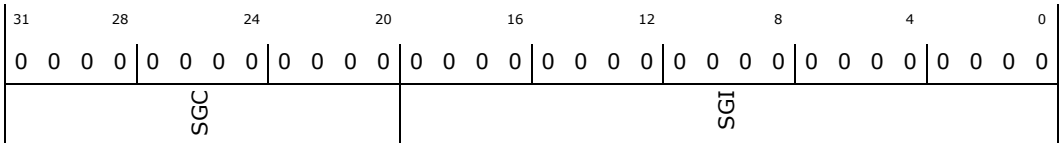
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC (SGC):** Dest scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI (SGI):** Dest scatter interval

9.4.70 Dest scatter Register for Channel 4 - HIGH (DSR4_HI)—Offset 1B4h

Dest scatter Register for Channel 4

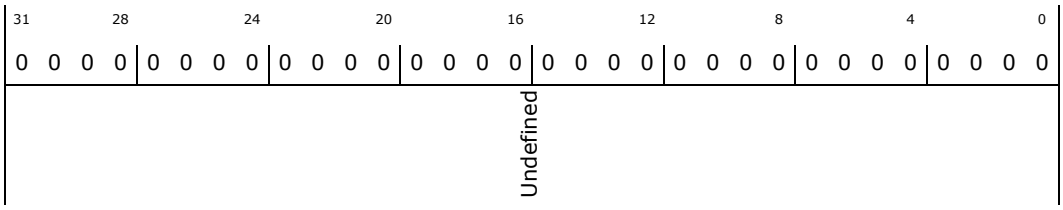
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.71 Source Address Register for Channel 5 - LOW (SAR5_LO)—Offset 1B8h

Source Address Register for Channel 5

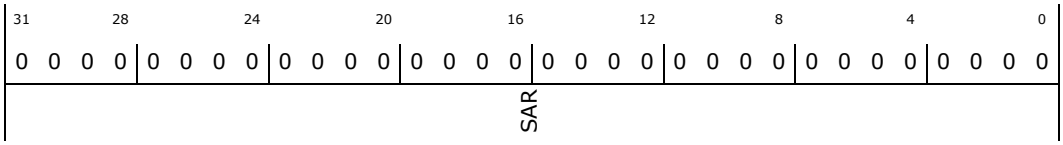
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

9.4.72 Source Address Register for Channel 5 - HIGH (SAR5_HI)—Offset 1BCh

Source Address Register for Channel 5

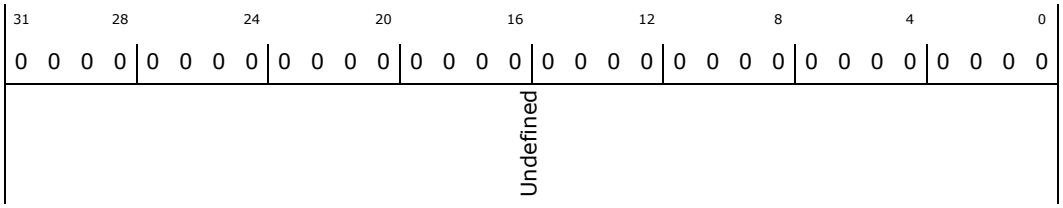
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.4.73 Destination Address Register for Channel 5 - LOW (DAR5_LO)—Offset 1C0h

Destination Address Register for Channel 5

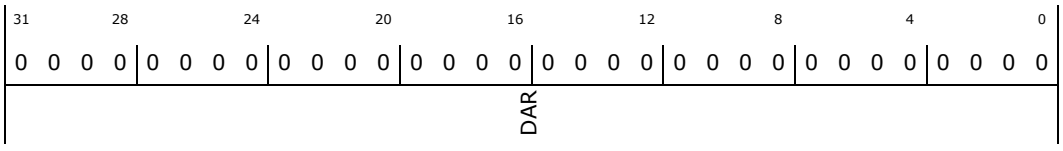
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

9.4.74 Destination Address Register for Channel 5 - HIGH (DAR5_HI)—Offset 1C4h

Destination Address Register for Channel 5

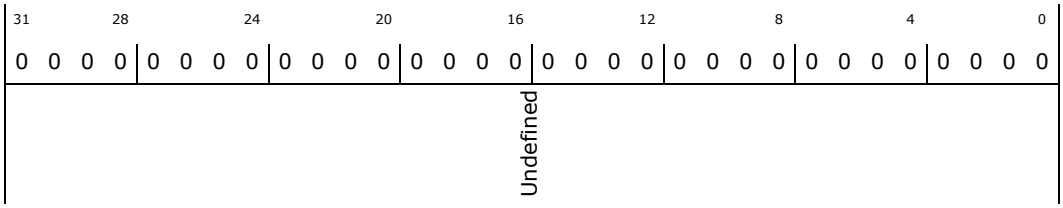
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.75 Linked List Pointer Register for Channel 5 - LOW (LLP5_LO)—Offset 1C8h

Linked List Pointer Register for Channel 5

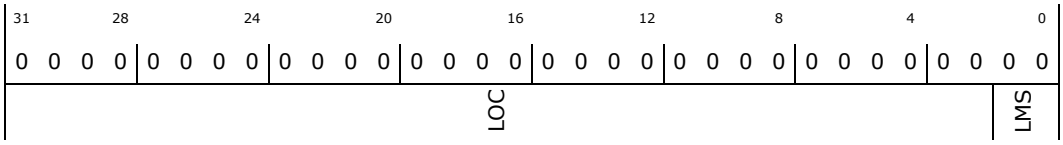
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0x0 RW	**LMS:** List Master Select. Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

9.4.76 Linked List Pointer Register for Channel 5 - HIGH (LLP5_HI)—Offset 1CCh

Linked List Pointer Register for Channel 5

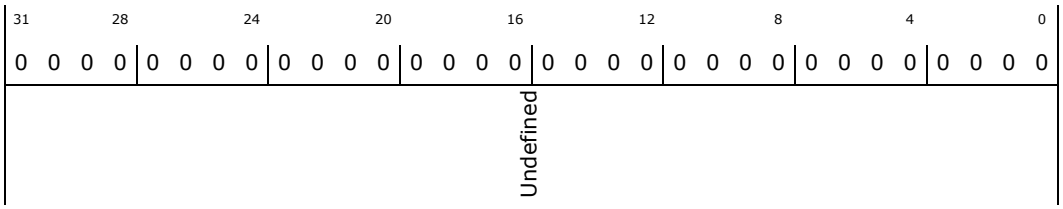
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.4.77 Control Register for Channel 5 - LOW (CTL5_LO)—Offset 1D0h

Control Register for Channel 5

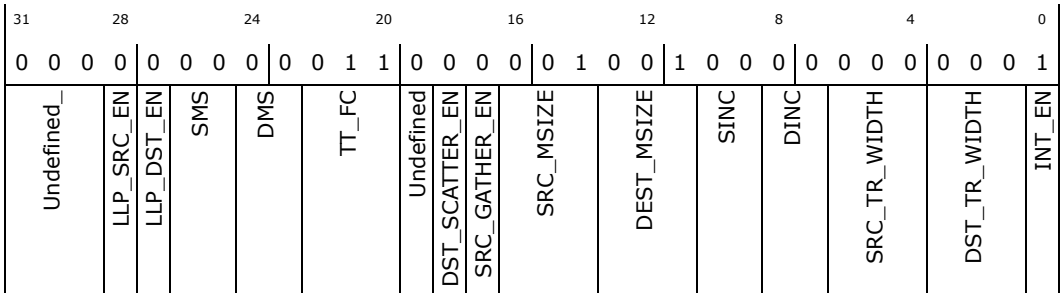
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**Undefined_:** RESERVED
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0x0 RW	**SMS:** Source Master Select. Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0x0 RW	**DMS:** Destination Master Select. Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	0x3 RW	**TT_FC:** Transfer Type and Flow Control.
19	0x0 RW	**Undefined:** RESERVED
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit. 0 = disabled 1 = enabled
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit. 0 = disabled 1 = enabled
16:14	0x1 RW	**SRC_MSIZE:** Source Burst Transaction Length.
13:11	0x1 RW	**DEST_MSIZE:** Destination Burst Transaction Length.
10:9	0x0 RW	**SINC:** Source Address Increment. 00 = Increment 01 = Decrement 1x = No change
8:7	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. 00 = Increment 01 = Decrement 1x = No change
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	0x1 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

9.4.78 Control Register for Channel 5 - HIGH (CTL5_HI)—Offset 1D4h

Control Register for Channel 5

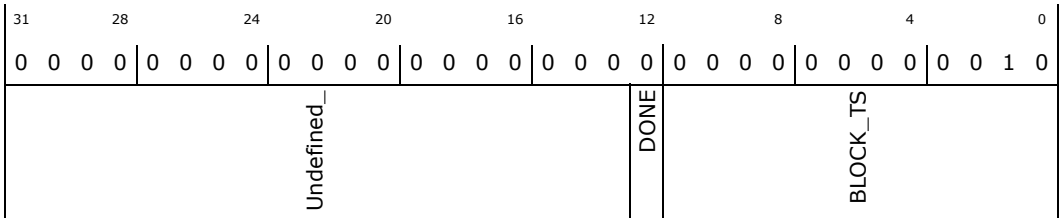
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Undefined_:** RESERVED
12	0x0 RW	**DONE:** Done bit
11:0	0x2 RW	**BLOCK_TS:** Block Transfer Size. When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

9.4.79 Configuration register for Channel 5 - LOW (CFG5_LO)—Offset 1F8h

Configuration register for Channel 5

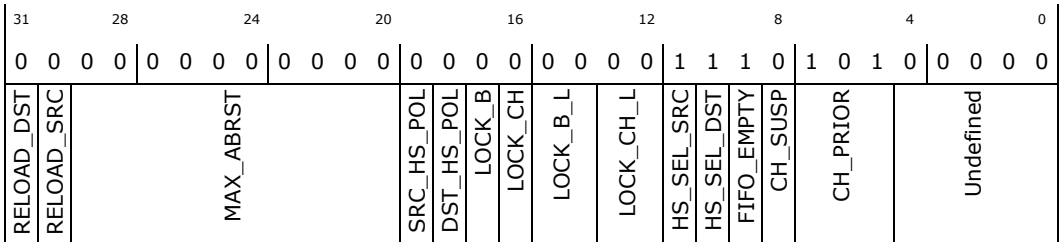
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000EA0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0x0 RW	**MAX_ABRST:** Maximum AMBA Burst Length. Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**LOCK_B:** Bus Lock Bit. When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0x0 RW	**LOCK_CH:** Channel Lock Bit. When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0x0 RW	**LOCK_B_L:** Bus Lock Level. Indicates the duration over which CFGx.LOCK_B bit applies. 00 = Over complete DMA transfer 01 = Over complete DMA block transfer 1x = Over complete DMA transaction
13:12	0x0 RW	**LOCK_CH_L:** Channel Lock Level. Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	0x1 RW	**HS_SEL_SRC:** Source Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
10	0x1 RW	**HS_SEL_DST:** Destination Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA transfers from source until this bit is cleared.
7:5	0x5 RW	**CH_PRIOR:** Channel priority. Priority of 7 is the highest priority.
4:0	0x0 RW	**Undefined:** RESERVED

9.4.80 Configuration register for Channel 5 - HIGH (CFG5_HI)—Offset 1FCh

Configuration register for Channel 5 _ HIGH

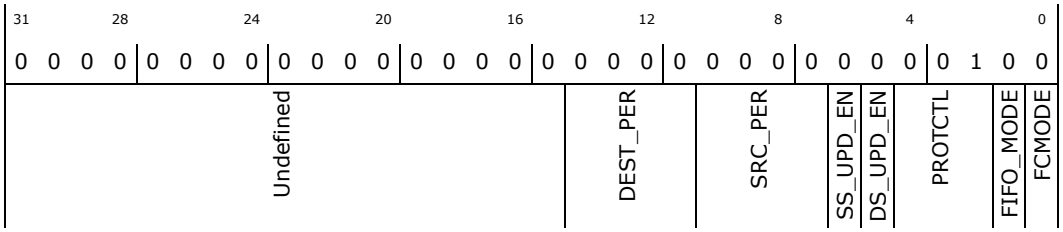
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RW	**Undefined:** Reserved
14:11	0x0 RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0x0 RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	0x1 RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0x0 RW	**FIFO_MODE:** FIFO Mode Select. Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0 = Space/data available for single AHB transfer of the specified transfer width. 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0x0 RW	**FCMODE:** Flow Control Mode. Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. 1 = Source transaction requests are not serviced until a destination transaction request occurs.

9.4.81 Source Gather Register for Channel 5 - LOW (SGR5_LO)—Offset 200h

Source Gather Register for Channel 5

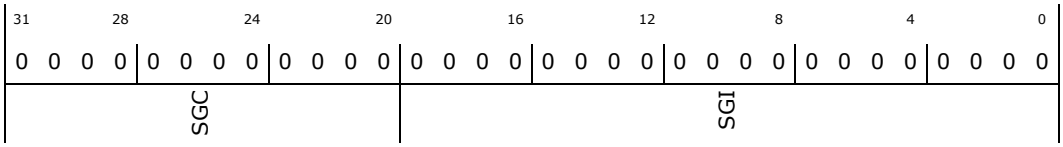
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 200h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval

9.4.82 Source Gather Register for Channel 5 - HIGH (SGR5_HI)—Offset 204h

Source Gather Register for Channel 5

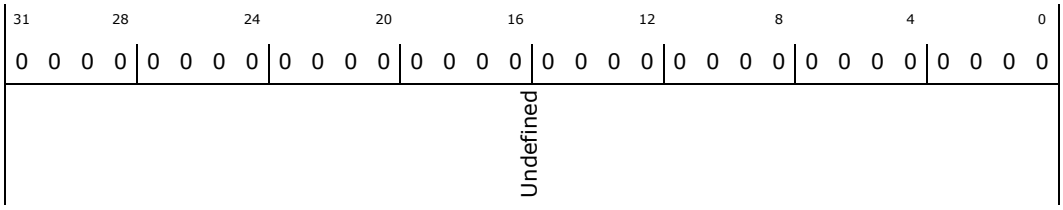
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 204h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.83 Destination Scatter Register for Channel 5 - LOW (DSR5_LO)—Offset 208h

Destination Scatter Register for Channel 5

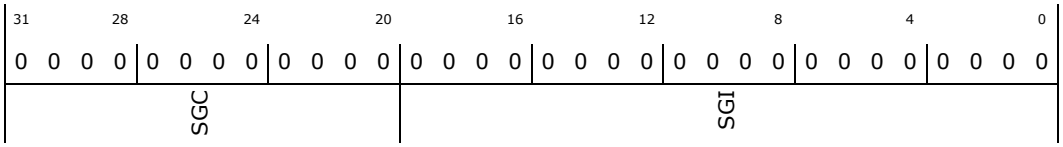
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 208h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC (SGC):** Dest scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI (SGI):** Dest scatter interval

9.4.84 Dest scatter Register for Channel 5 - HIGH (DSR5_HI)—Offset 20Ch

Dest scatter Register for Channel 5

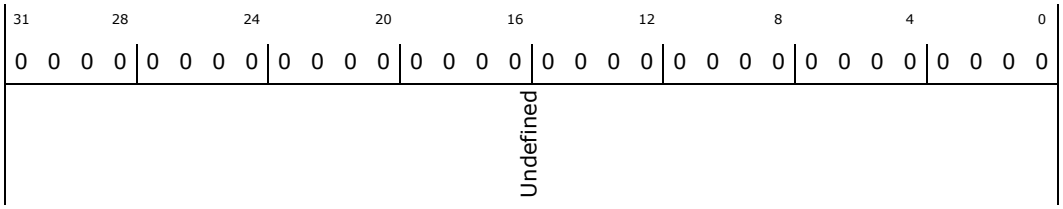
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 20Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.85 Source Address Register for Channel 6 - LOW (SAR6_LO)—Offset 210h

Source Address Register for Channel 6

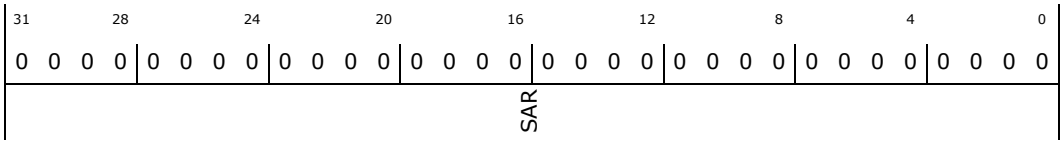
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 210h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

9.4.86 Source Address Register for Channel 6 - HIGH (SAR6_HI)—Offset 214h

Source Address Register for Channel 6

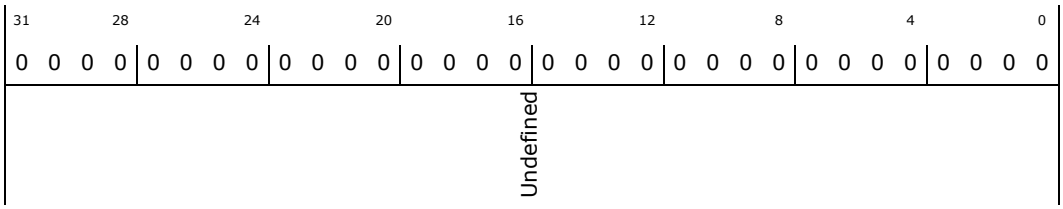
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 214h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.4.87 Destination Address Register for Channel 6 - LOW (DAR6_LO)—Offset 218h

Destination Address Register for Channel 6

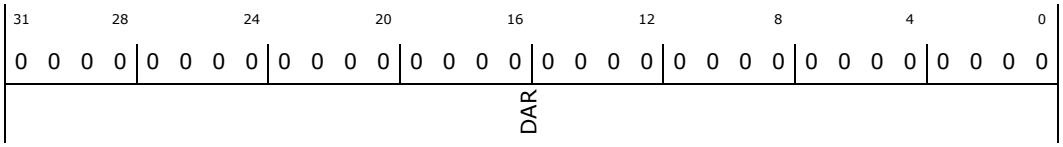
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 218h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

9.4.88 Destination Address Register for Channel 6 - HIGH (DAR6_HI)—Offset 21Ch

Destination Address Register for Channel 6

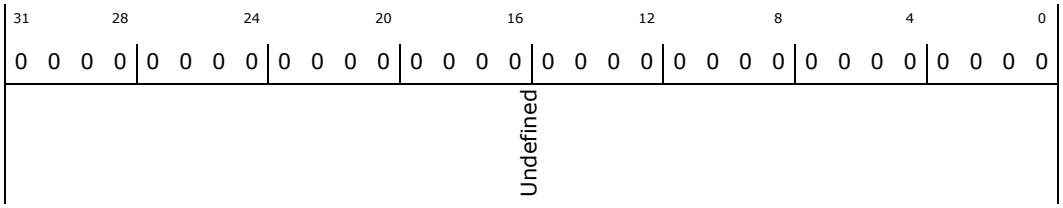
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 21Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.89 Linked List Pointer Register for Channel 6 - LOW (LLP6_LO)—Offset 220h

Linked List Pointer Register for Channel 6

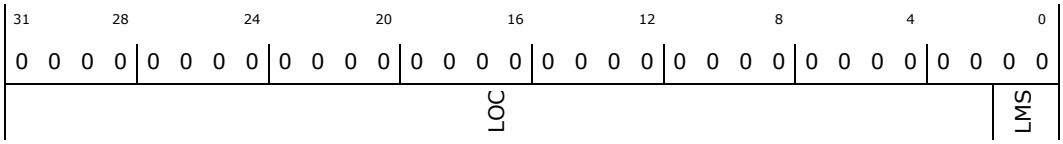
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 220h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0x0 RW	**LMS:** List Master Select. Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

9.4.90 Linked List Pointer Register for Channel 6 - HIGH (LLP6_HI)—Offset 224h

Linked List Pointer Register for Channel 6

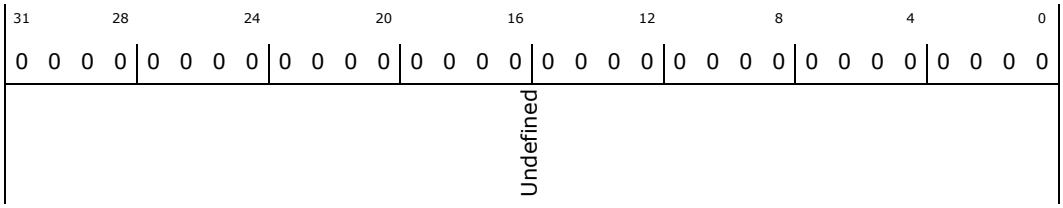
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 224h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.4.91 Control Register for Channel 6 - LOW (CTL6_LO)—Offset 228h

Control Register for Channel 6

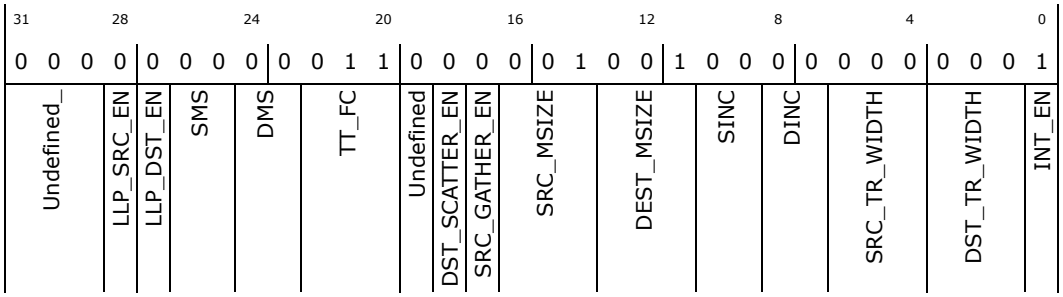
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 228h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**Undefined_:** RESERVED
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0x0 RW	**SMS:** Source Master Select. Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0x0 RW	**DMS:** Destination Master Select. Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	0x3 RW	**TT_FC:** Transfer Type and Flow Control.
19	0x0 RW	**Undefined:** RESERVED
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit. 0 = disabled 1 = enabled
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit. 0 = disabled 1 = enabled
16:14	0x1 RW	**SRC_MSIZE:** Source Burst Transaction Length.
13:11	0x1 RW	**DEST_MSIZE:** Destination Burst Transaction Length.
10:9	0x0 RW	**SINC:** Source Address Increment. 00 = Increment 01 = Decrement 1x = No change
8:7	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. 00 = Increment 01 = Decrement 1x = No change
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.

Bit Range	Default & Access	Field Name (ID): Description
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	0x1 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

9.4.92 Control Register for Channel 6 - HIGH (CTL6_HI)—Offset 22Ch

Control Register for Channel 6

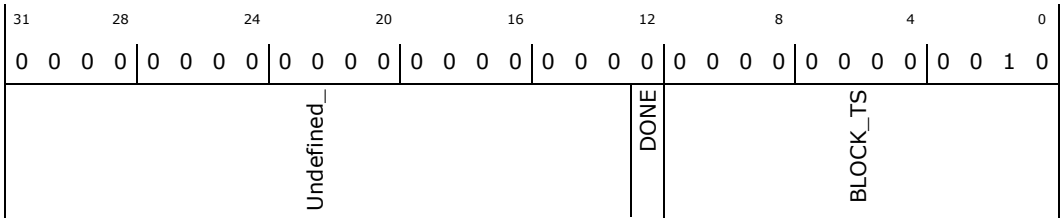
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 22Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Undefined_:** RESERVED
12	0x0 RW	**DONE:** Done bit
11:0	0x2 RW	**BLOCK_TS:** Block Transfer Size. When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

9.4.93 Configuration register for Channel 6 - LOW (CFG6_LO)—Offset 250h

Configuration register for Channel 6

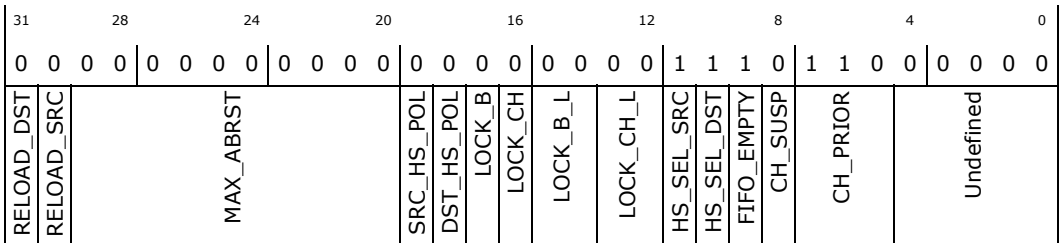
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 250h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000EC0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0x0 RW	**MAX_ABRST:** Maximum AMBA Burst Length. Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**LOCK_B:** Bus Lock Bit. When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.
16	0x0 RW	**LOCK_CH:** Channel Lock Bit. When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0x0 RW	**LOCK_B_L:** Bus Lock Level. Indicates the duration over which CFGx.LOCK_B bit applies. 00 = Over complete DMA transfer 01 = Over complete DMA block transfer 1x = Over complete DMA transaction
13:12	0x0 RW	**LOCK_CH_L:** Channel Lock Level. Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	0x1 RW	**HS_SEL_SRC:** Source Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
10	0x1 RW	**HS_SEL_DST:** Destination Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA transfers from source until this bit is cleared.
7:5	0x6 RW	**CH_PRIOR:** Channel priority. Priority of 7 is the highest priority.

Bit Range	Default & Access	Field Name (ID): Description
4:0	0x0 RW	**Undefined:** RESERVED

9.4.94 Configuration register for Channel 6 - HIGH (CFG6_HI)—Offset 254h

Configuration register for Channel 6 _ HIGH

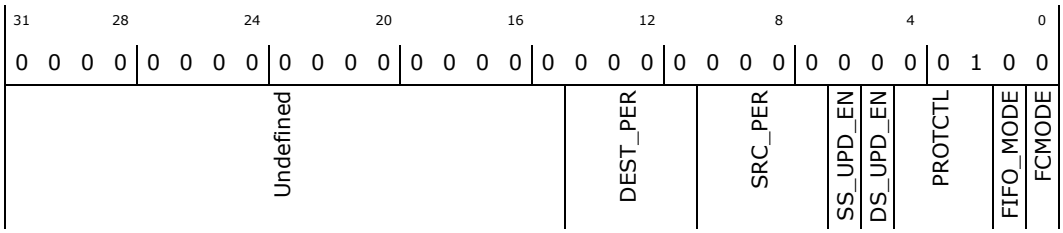
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 254h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RW	**Undefined:** Reserved
14:11	0x0 RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0x0 RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	0x1 RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**FIFO_MODE:** FIFO Mode Select. Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0 = Space/data available for single AHB transfer of the specified transfer width. 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0x0 RW	**FCMODE:** Flow Control Mode. Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. 1 = Source transaction requests are not serviced until a destination transaction request occurs.

9.4.95 Source Gather Register for Channel 6 - LOW (SGR6_LO)—Offset 258h

Source Gather Register for Channel 6

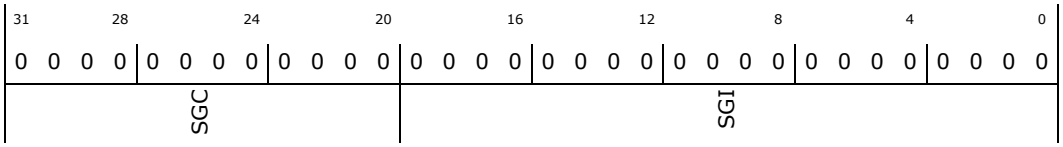
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 258h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval

9.4.96 Source Gather Register for Channel 6 - HIGH (SGR6_HI)—Offset 25Ch

Source Gather Register for Channel 6

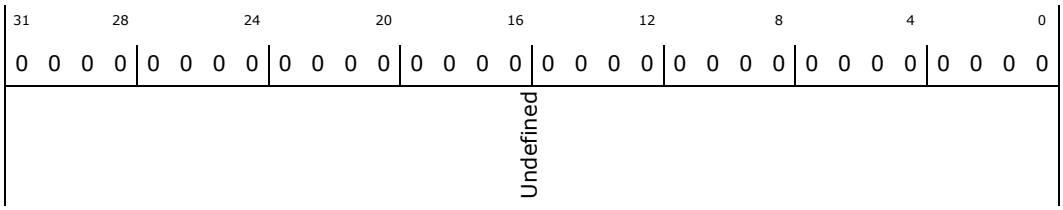
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 25Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.97 Destination Scatter Register for Channel 6 - LOW (DSR6_LO)—Offset 260h

Destination Scatter Register for Channel 6

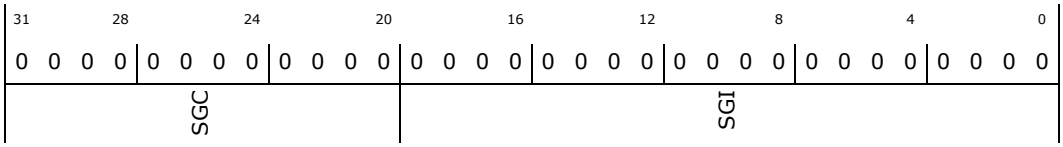
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 260h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC (SGC):** Dest scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI (SGI):** Dest scatter interval

9.4.98 Dest scatter Register for Channel 6 - HIGH (DSR6_HI)—Offset 264h

Dest scatter Register for Channel 6

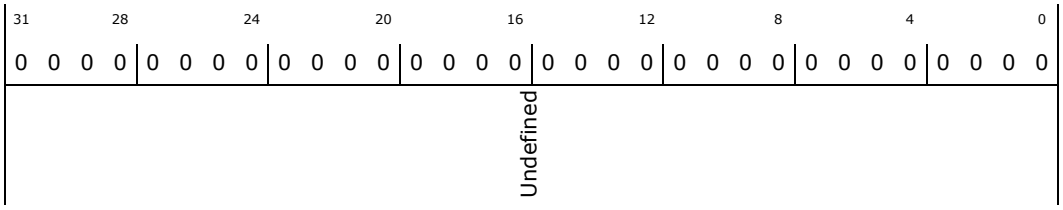
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 264h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.99 Source Address Register for Channel 7 - LOW (SAR7_LO)—Offset 268h

Source Address Register for Channel 7

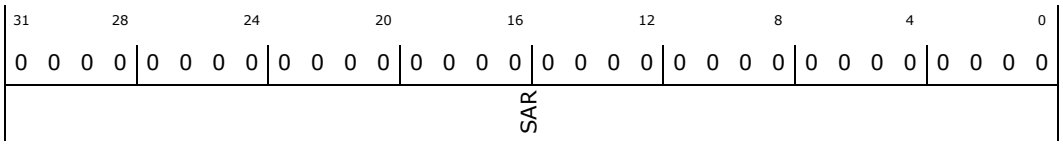
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 268h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SAR:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source transfer throughout the block transfer.

9.4.100 Source Address Register for Channel 7 - HIGH (SAR7_HI)—Offset 26Ch

Source Address Register for Channel 7

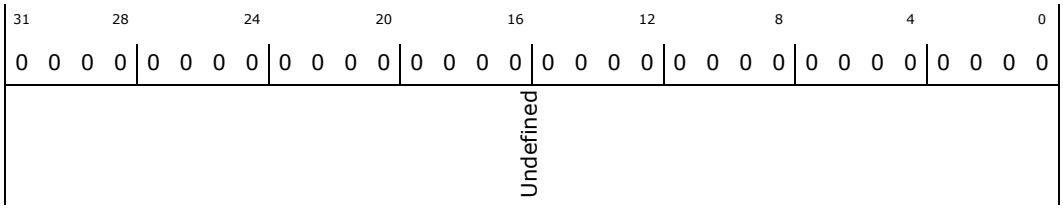
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 26Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.4.101 Destination Address Register for Channel 7 - LOW (DAR7_LO)—Offset 270h

Destination Address Register for Channel 7

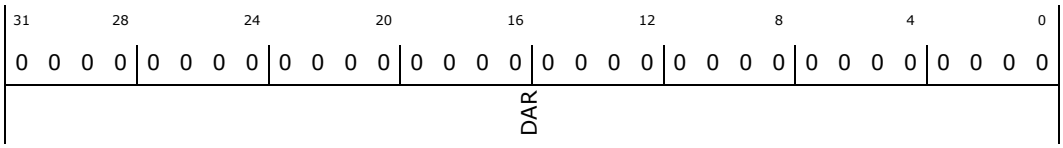
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 270h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**DAR:** Current Destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.

9.4.102 Destination Address Register for Channel 7 - HIGH (DAR7_HI)—Offset 274h

Destination Address Register for Channel 7

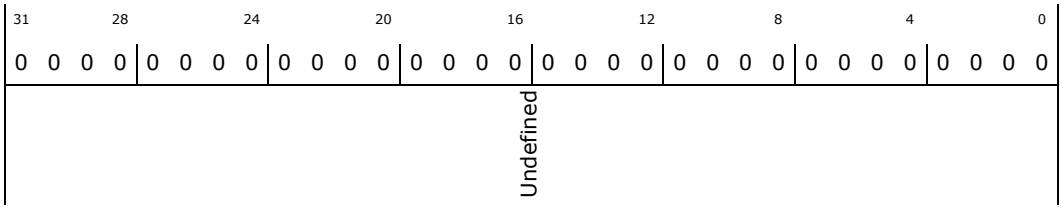
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 274h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.103 Linked List Pointer Register for Channel 7 - LOW (LLP7_LO)—Offset 278h

Linked List Pointer Register for Channel 7

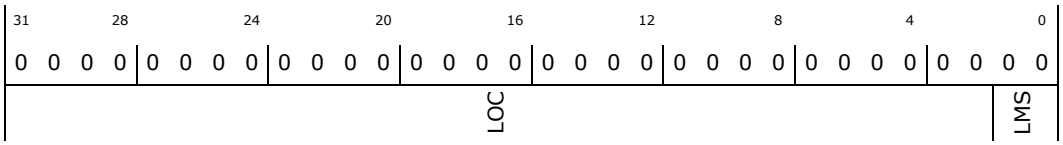
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 278h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled.
1:0	0x0 RW	**LMS:** List Master Select. Identifies the AHB layer/interface where the memory device that stores the next linked list item resides.

9.4.104 Linked List Pointer Register for Channel 7 - HIGH (LLP7_HI)—Offset 27Ch

Linked List Pointer Register for Channel 7

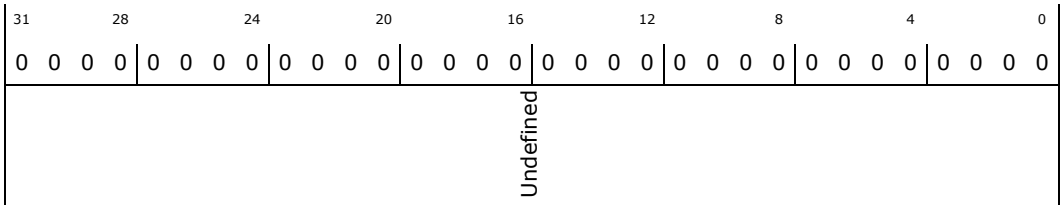
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 27Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** RESERVED

9.4.105 Control Register for Channel 7 - LOW (CTL7_LO)—Offset 280h

Control Register for Channel 7

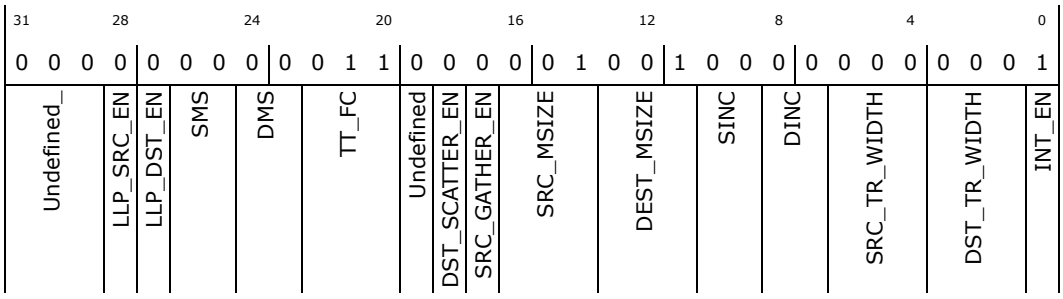
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 280h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00304801h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**Undefined_:** RESERVED
28	0x0 RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPx.LOC is non-zero
27	0x0 RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPx.LOC is non-zero.
26:25	0x0 RW	**SMS:** Source Master Select. Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed.
24:23	0x0 RW	**DMS:** Destination Master Select. Identifies the Master Interface layer where the destination device (peripheral or memory) resides.
22:20	0x3 RW	**TT_FC:** Transfer Type and Flow Control.

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RW	**Undefined:** RESERVED
18	0x0 RW	**DST_SCATTER_EN:** Destination scatter enable bit. 0 = disabled 1 = enabled
17	0x0 RW	**SRC_GATHER_EN:** Source gather enable bit. 0 = disabled 1 = enabled
16:14	0x1 RW	**SRC_MSIZE:** Source Burst Transaction Length.
13:11	0x1 RW	**DEST_MSIZE:** Destination Burst Transaction Length.
10:9	0x0 RW	**SINC:** Source Address Increment. 00 = Increment 01 = Decrement 1x = No change
8:7	0x0 RW	**DINC:** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. 00 = Increment 01 = Decrement 1x = No change
6:4	0x0 RW	**SRC_TR_WIDTH:** Source Transfer Width. This value must be less than or equal to DMAH_Mx_HDATA_WIDTH, where x is the AHB layer 1 to 4 where the source resides.
3:1	0x0 RW	**DST_TR_WIDTH:** Destination Transfer Width. This value must be less than or equal to DMAH_Mk_HDATA_WIDTH, where k is the AHB layer 1 to 4 where the destination resides.
0	0x1 RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

9.4.106 Control Register for Channel 7 - HIGH (CTL7_HI)—Offset 284h

Control Register for Channel 7

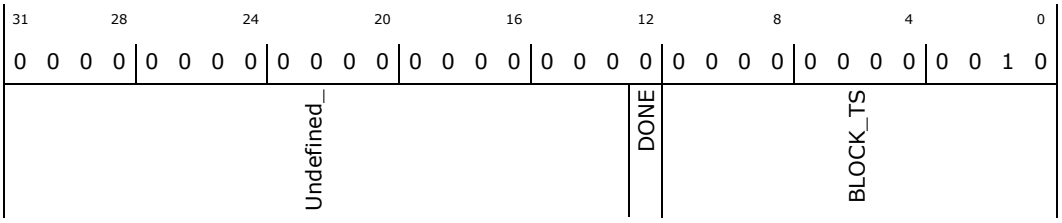
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 284h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Undefined_:** RESERVED
12	0x0 RW	**DONE:** Done bit
11:0	0x2 RW	**BLOCK_TS:** Block Transfer Size. When the DW_ahb_dmac is the flow controller, the user writes this field before the channel is enabled in order to indicate the block size.

9.4.107 Configuration register for Channel 7 - LOW (CFG7_LO)—Offset 2A8h

Configuration register for Channel 7

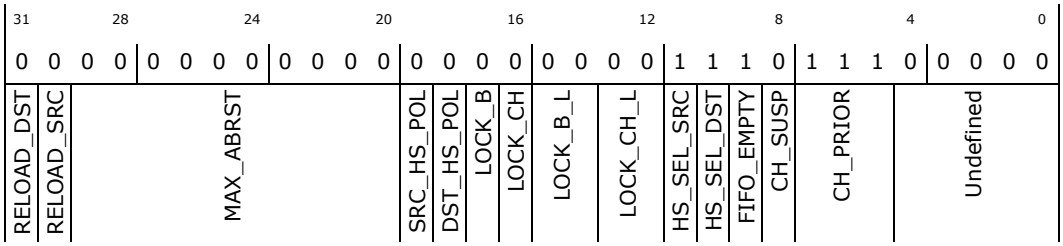
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000EE0h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RELOAD_DST:** Automatic Destination Reload. The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
30	0x0 RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers.
29:20	0x0 RW	**MAX_ABRST:** Maximum AMBA Burst Length. Maximum AMBA burst length that is used for DMA transfers on this channel. A value of 0 indicates that software is not limiting the maximum AMBA burst length for DMA transfers on this channel.
19	0x0 RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0x0 RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17	0x0 RW	**LOCK_B:** Bus Lock Bit. When active, the AHB bus master signal hlock is asserted for the duration specified in CFGx.LOCK_B_L.

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW	**LOCK_CH:** Channel Lock Bit. When the channel is granted control of the master bus interface and if the CFGx.LOCK_CH bit is asserted, then no other channels are granted control of the master bus interface for the duration specified in CFGx.LOCK_CH_L. Indicates to the master bus interface arbiter that this channel wants exclusive access to the master bus interface for the duration specified in CFGx.LOCK_CH_L.
15:14	0x0 RW	**LOCK_B_L:** Bus Lock Level. Indicates the duration over which CFGx.LOCK_B bit applies. 00 = Over complete DMA transfer 01 = Over complete DMA block transfer 1x = Over complete DMA transaction
13:12	0x0 RW	**LOCK_CH_L:** Channel Lock Level. Indicates the duration over which CFGx.LOCK_CH bit applies. 00 = DMA transfer 01 = DMA block transfer 1x = DMA transaction
11	0x1 RW	**HS_SEL_SRC:** Source Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
10	0x1 RW	**HS_SEL_DST:** Destination Software or Hardware Handshaking Select. 0 = HW handshaking 1 = SW handshaking
9	0x1 RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO.
8	0x0 RW	**CH_SUSP:** Channel Suspend. Suspends all DMA transfers from source until this bit is cleared.
7:5	0x7 RW	**CH_PRIOR:** Channel priority. Priority of 7 is the highest priority.
4:0	0x0 RW	**Undefined:** RESERVED

9.4.108 Configuration register for Channel 7 - HIGH (CFG7_HI)—Offset 2ACh

Configuration register for Channel 7 _ HIGH

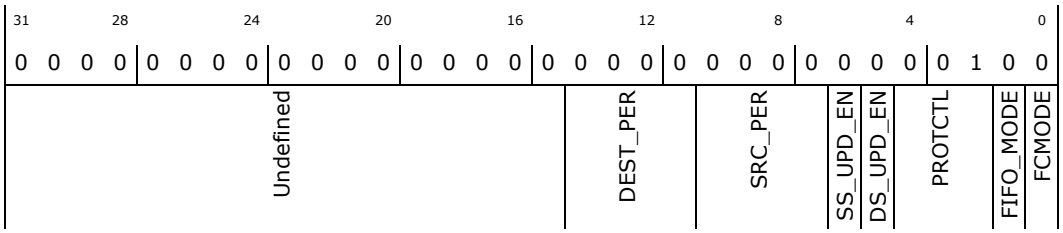
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RW	**Undefined:** Reserved
14:11	0x0 RW	**DEST_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored.
10:7	0x0 RW	**SRC_PER:** Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored.
6	0x0 RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARx register, stored in the SSTATx register and written out to the SSTATx location of the LLI (refer to Figure 52 on page 243) if SS_UPD_EN is high.
5	0x0 RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARx register, stored in the DSTATx register and written out to the DSTATx location of the LLI if DS_UPD_EN is high.
4:2	0x1 RW	**PROTCTL:** Protection Control bits used to drive the AHB HPROT[3:1] bus.
1	0x0 RW	**FIFO_MODE:** FIFO Mode Select. Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0 = Space/data available for single AHB transfer of the specified transfer width. 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the fifo depth for source transfers.
0	0x0 RW	**FCMODE:** Flow Control Mode. Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller. 0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled. 1 = Source transaction requests are not serviced until a destination transaction request occurs.

9.4.109 Source Gather Register for Channel 7 - LOW (SGR7_LO)—Offset 2B0h

Source Gather Register for Channel 7

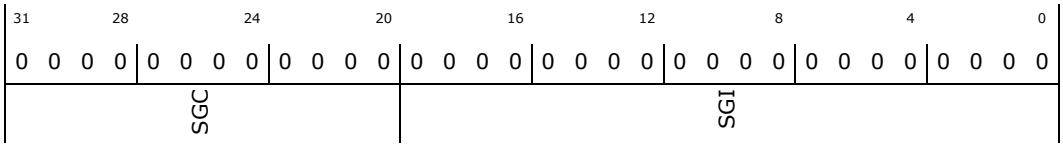
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**SGC:** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0x0 RW	**SGI:** Source gather interval

9.4.110 Source Gather Register for Channel 7 - HIGH (SGR7_HI)—Offset 2B4h

Source Gather Register for Channel 7

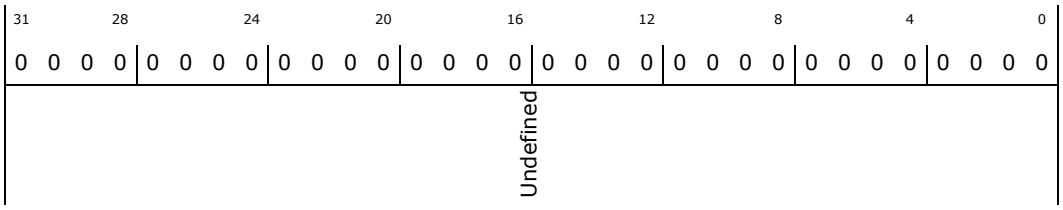
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.111 Destination Scatter Register for Channel 7 - LOW (DSR7_LO)—Offset 2B8h

Destination Scatter Register for Channel 7

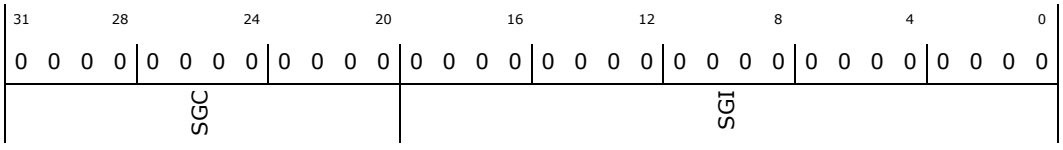
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2B8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**DSC (SGC):** Dest scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0x0 RW	**DSI (SGI):** Dest scatter interval

9.4.112 Dest scatter Register for Channel 7 - HIGH (DSR7_HI)—Offset 2BCh

Dest scatter Register for Channel 7

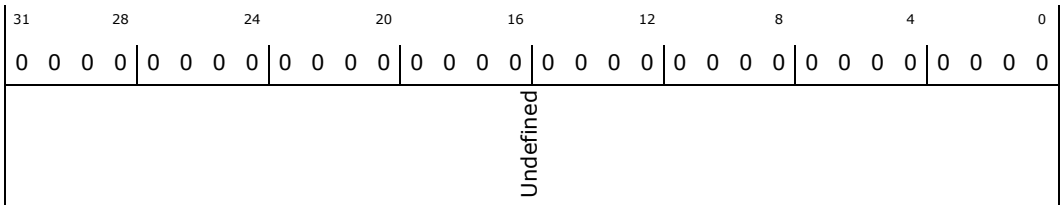
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2BCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.113 RawTfr Interrupt Raw Status Registers - LOW (RawTfr_LO)—Offset 2C0h

RawTfr Interrupt Raw Status Registers

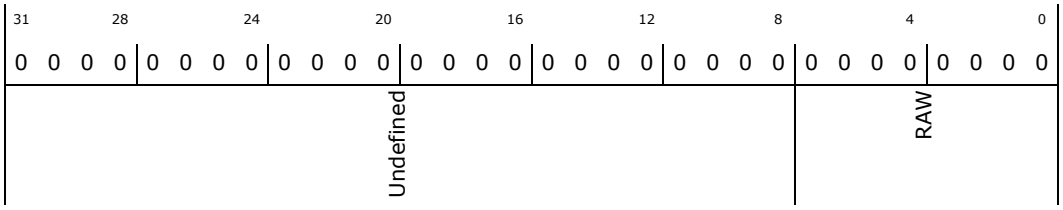
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2C0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RW	**RAW:** Raw interrupt status

9.4.114 RawTfr Interrupt Raw Status Registers - HIGH (RawTfr_HI)—Offset 2C4h

RawTfr Interrupt Raw Status Registers

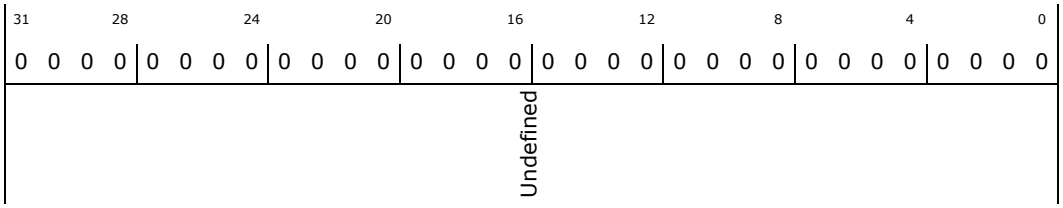
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2C4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.115 RawBlock Interrupt Raw Status Registers - LOW (RawBlock_LO)—Offset 2C8h

RawBlock Interrupt Raw Status Registers

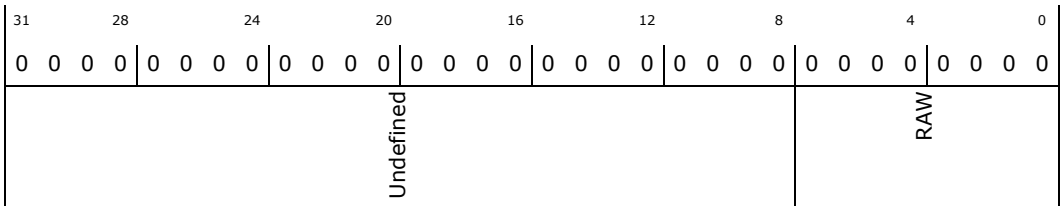
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RW	**RAW:** Raw interrupt status

9.4.116 RawBlock Interrupt Raw Status Registers - HIGH (RawBlock_HI)—Offset 2CCh

RawBlock Interrupt Raw Status Registers

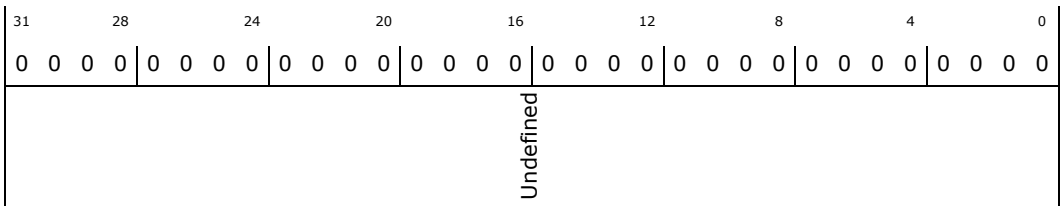
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.117 RawSrcTran Interrupt Raw Status Registers - LOW (RawSrcTran_LO)—Offset 2D0h

RawSrcTran Interrupt Raw Status Registers

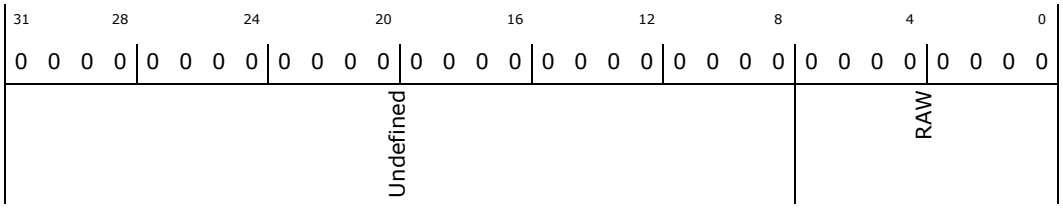
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RW	**RAW:** Raw interrupt status

9.4.118 RawSrcTran Interrupt Raw Status Registers - HIGH (RawSrcTran_HI)—Offset 2D4h

RawSrcTran Interrupt Raw Status Registers

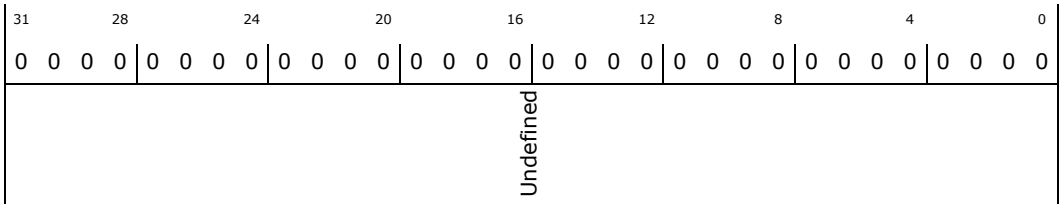
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.119 RawDstTran Interrupt Raw Status Registers - LOW (RawDstTran_LO)—Offset 2D8h

RawDstTran Interrupt Raw Status Registers

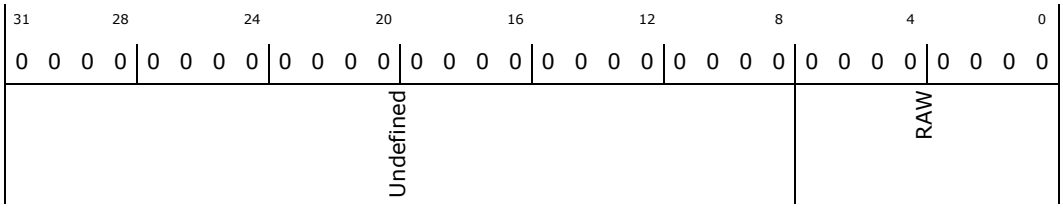
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RW	**RAW:** Raw interrupt status

9.4.120 RawDstTran Interrupt Raw Status Registers - HIGH (RawDstTran_HI)—Offset 2DCh

RawDstTran Interrupt Raw Status Registers

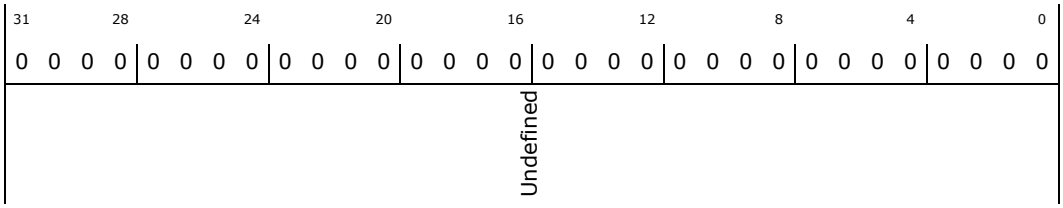
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.121 RawErr Interrupt Raw Status Registers - LOW (RawErr_LO)—Offset 2E0h

RawErr Interrupt Raw Status Registers

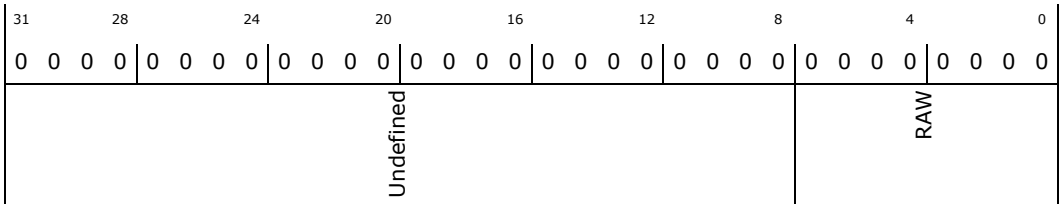
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RW	**RAW:** Raw interrupt status

9.4.122 RawErr Interrupt Raw Status Registers - HIGH (RawErr_HI)—Offset 2E4h

RawErr Interrupt Raw Status Registers

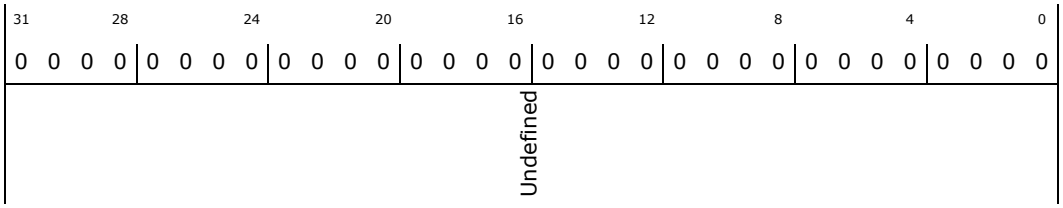
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.123 StatusTfr Interrupt Status Registers - LOW (StatusTfr_LO)—Offset 2E8h

StatusTfr Interrupt Status Registers

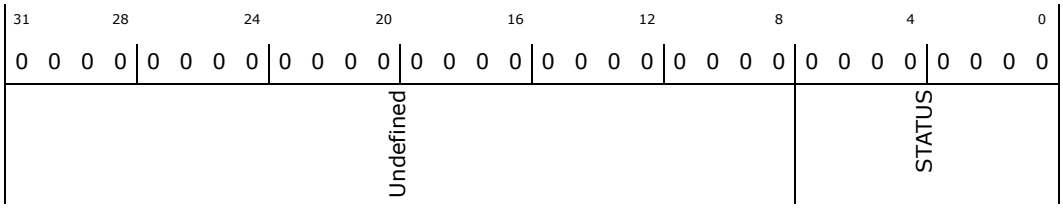
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RO	**STATUS:** Status interrupt status

9.4.124 StatusTfr Interrupt Status Registers - HIGH (StatusTfr_HI)—Offset 2ECh

StatusTfr Interrupt Status Registers

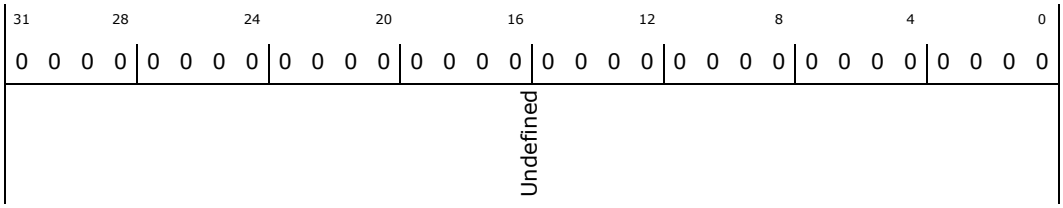
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

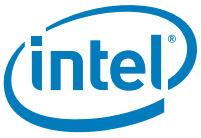
Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.125 StatusBlock Interrupt Status Registers - LOW (StatusBlock_LO)—Offset 2F0h

StatusBlock Interrupt Status Registers



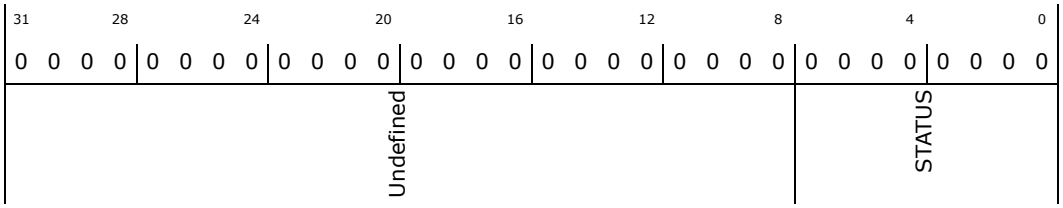
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RO	**STATUS:** Status interrupt status

9.4.126 StatusBlock Interrupt Status Registers - HIGH (StatusBlock_HI)—Offset 2F4h

StatusBlock Interrupt Status Registers

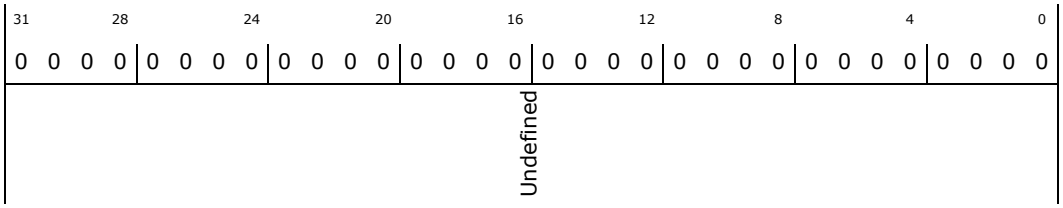
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.127 StatusSrcTran Interrupt Status Registers - LOW (StatusSrcTran_LO)—Offset 2F8h

StatusSrcTran Interrupt Status Registers

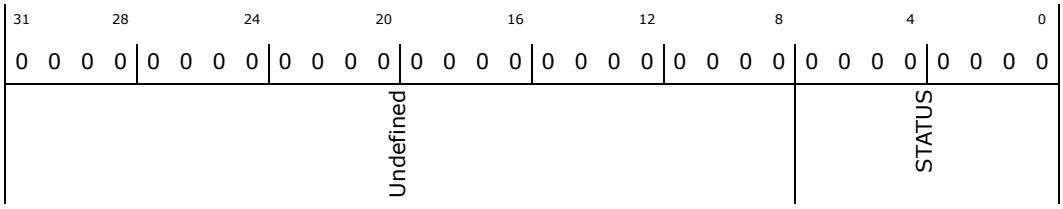
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RO	**STATUS:** Status interrupt status

9.4.128 StatusSrcTran Interrupt Status Registers - HIGH (StatusSrcTran_HI)—Offset 2FCh

StatusSrcTran Interrupt Status Registers

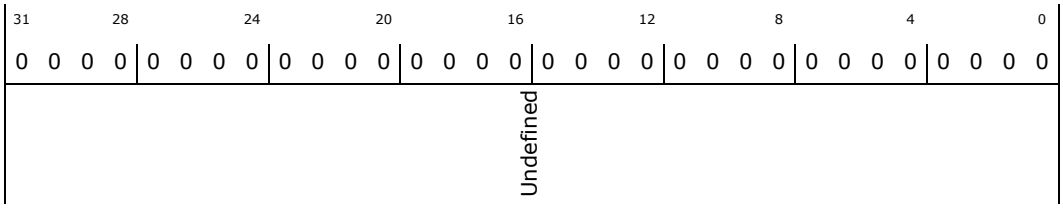
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

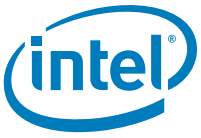
Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.129 StatusDstTran Interrupt Status Registers - LOW (StatusDstTran_LO)—Offset 300h

StatusDstTran Interrupt Status Registers



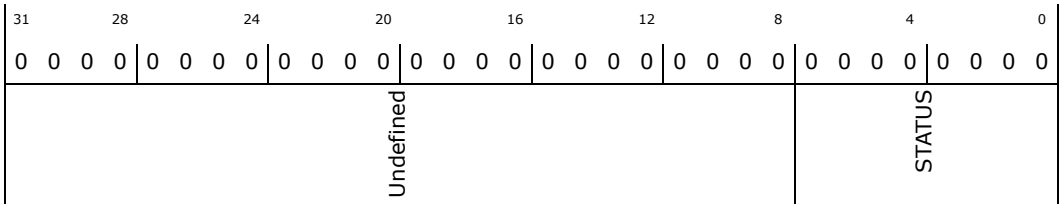
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 300h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RO	**STATUS:** Status interrupt status

9.4.130 StatusDstTran Interrupt Status Registers - HIGH (StatusDstTran_HI)—Offset 304h

StatusDstTran Interrupt Status Registers

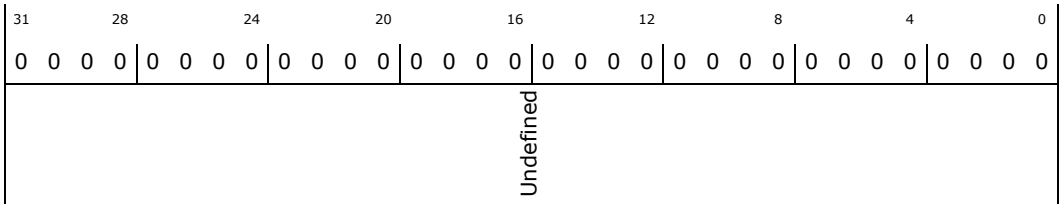
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 304h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.131 StatusErr Interrupt Status Registers - LOW (StatusErr_LO)—Offset 308h

StatusErr Interrupt Status Registers

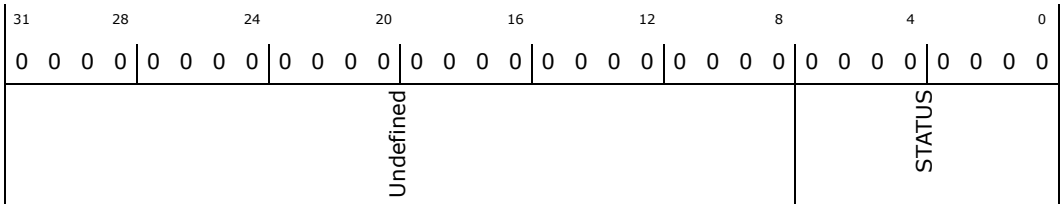
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 308h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 RO	**STATUS:** Status interrupt status

9.4.132 StatusErr Interrupt Status Registers - HIGH (StatusErr_HI)—Offset 30Ch

StatusErr Interrupt Status Registers

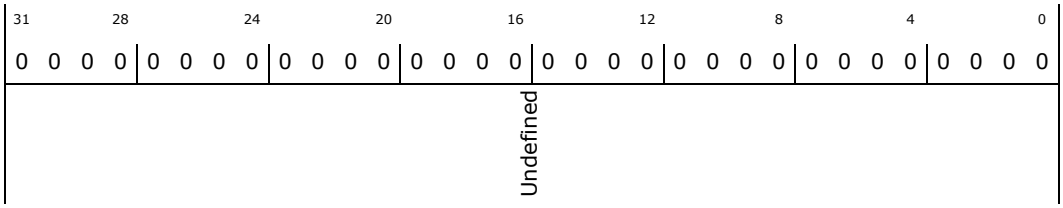
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.133 MaskTfr Interrupt Mask Registers - LOW (MaskTfr_LO)—Offset 310h

MaskTfr Interrupt Mask Registers

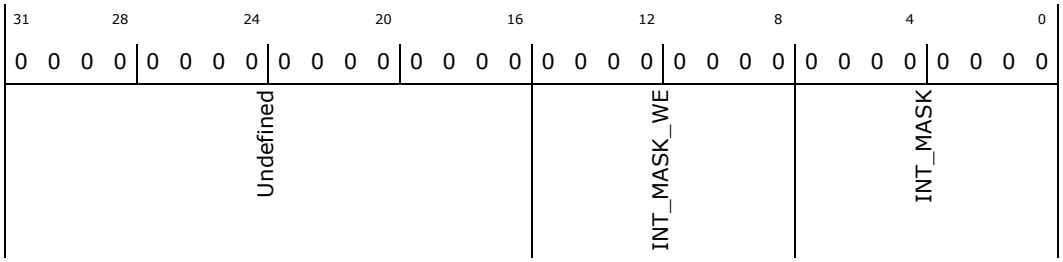
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 310h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 RW	**INT_MASK_WE:** Interrupt Mask Write Enable 0=write disabled 1=write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt Mask 0=masked 1=unmasked

9.4.134 MaskTfr Interrupt Mask Registers - HIGH (MaskTfr_HI)—Offset 314h

MaskTfr Interrupt Mask Registers

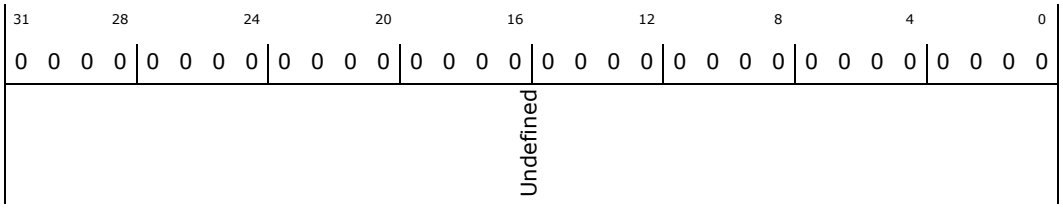
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 314h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.135 MaskBlock Interrupt Mask Registers - LOW (MaskBlock_LO)—Offset 318h

MaskBlock Interrupt Mask Registers

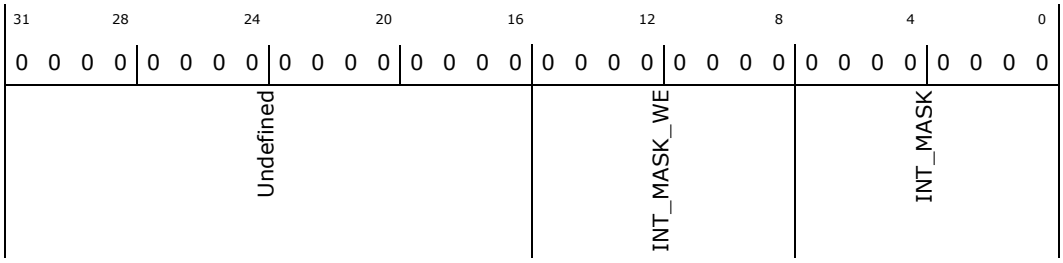
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 318h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0=write disabled 1=write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt Mask 0=masked 1=unmasked

9.4.136 MaskBlock Interrupt Mask Registers - HIGH (MaskBlock_HI)—Offset 31Ch

MaskBlock Interrupt Mask Registers

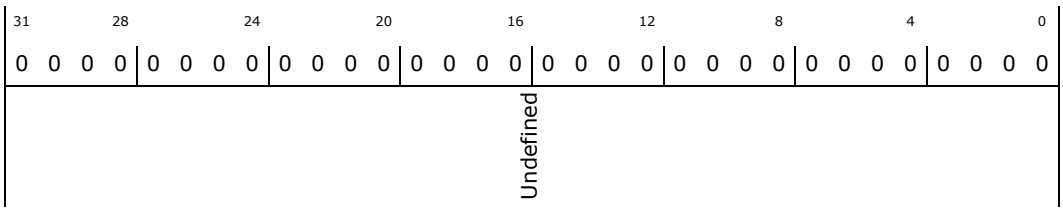
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 31Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.137 MaskSrcTran Interrupt Mask Registers - LOW (MaskSrcTran_LO)—Offset 320h

MaskSrcTran Interrupt Mask Registers

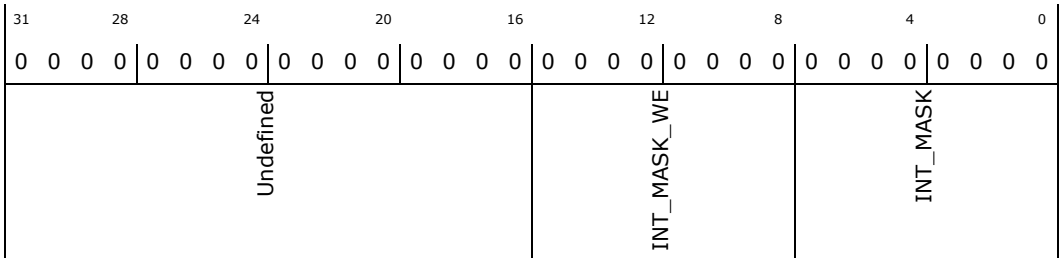
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 320h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0=write disabled 1=write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt Mask 0=masked 1=unmasked

9.4.138 MaskSrcTran Interrupt Mask Registers - HIGH (MaskSrcTran_HI)—Offset 324h

MaskSrcTran Interrupt Mask Registers

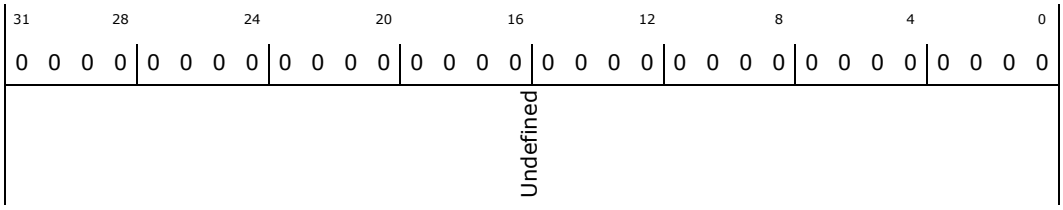
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 324h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.139 MaskDstTran Interrupt Mask Registers - LOW (MaskDstTran_LO)—Offset 328h

MaskDstTran Interrupt Mask Registers

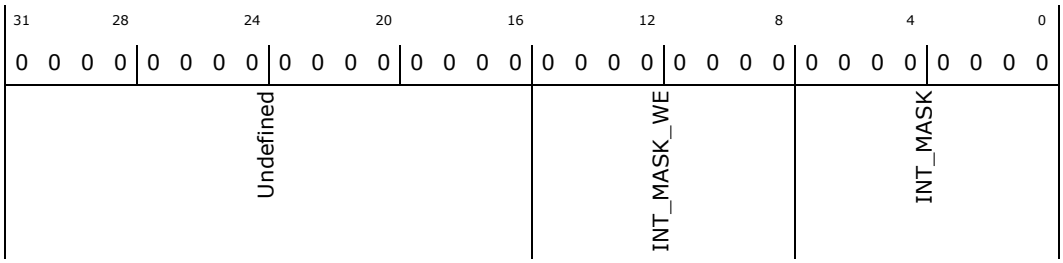
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 328h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0=write disabled 1=write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt Mask 0=masked 1=unmasked

9.4.140 MaskDstTran Interrupt Mask Registers - HIGH (MaskDstTran_HI)—Offset 32Ch

MaskDstTran Interrupt Mask Registers

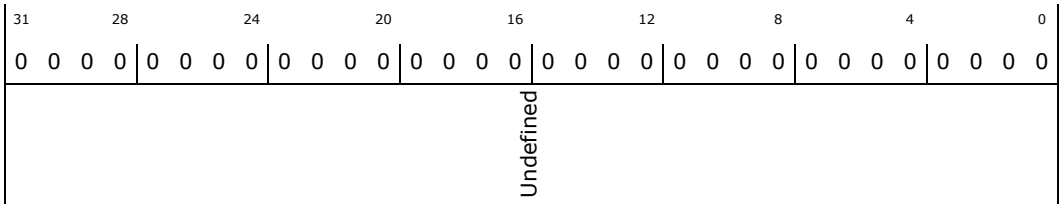
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 32Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.141 MaskErr Interrupt Mask Registers - LOW (MaskErr_LO)—Offset 330h

MaskErr Interrupt Mask Registers

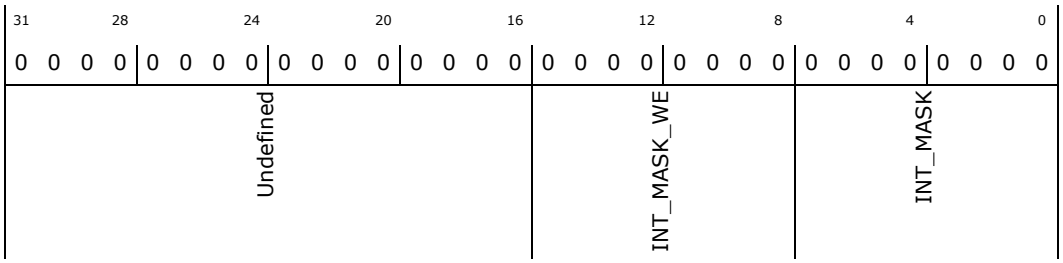
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 330h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**INT_MASK_WE:** Interrupt Mask Write Enable 0=write disabled 1=write enabled
7:0	0x0 RW	**INT_MASK:** Interrupt Mask 0=masked 1=unmasked

9.4.142 MaskErr Interrupt Mask Registers - HIGH (MaskErr_HI)—Offset 334h

MaskErr Interrupt Mask Registers

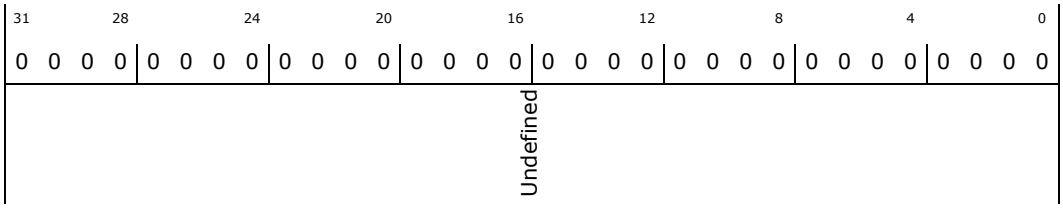
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 334h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.143 ClearTfr Interrupt Clear Registers - LOW (ClearTfr_LO)—Offset 338h

ClearTfr Interrupt Clear Registers

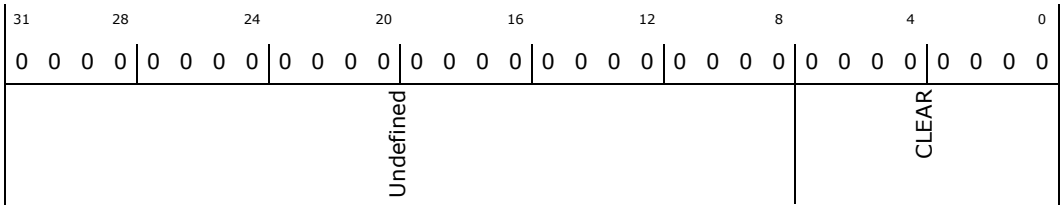
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 338h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 WO	**CLEAR:** Clear interrupt status

9.4.144 ClearTfr Interrupt Clear Registers - HIGH (ClearTfr_HI)—Offset 33Ch

ClearTfr Interrupt Clear Registers

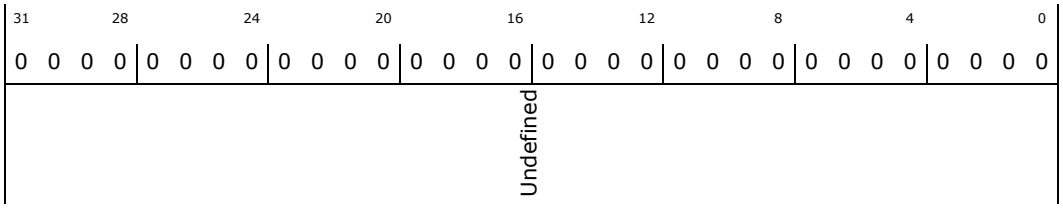
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 33Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.145 ClearBlock Interrupt Clear Registers - LOW (ClearBlock_LO)—Offset 340h

ClearBlock Interrupt Clear Registers

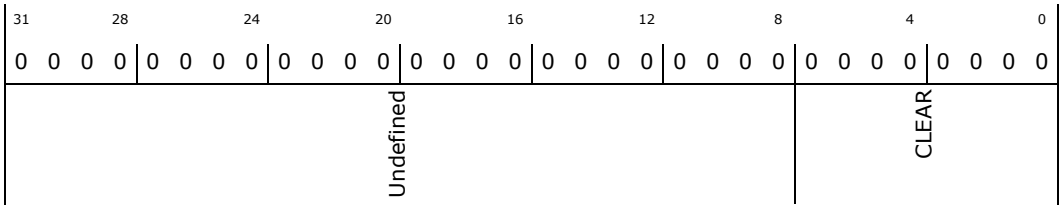
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 340h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 WO	**CLEAR:** Clear interrupt status

9.4.146 ClearBlock Interrupt Clear Registers - HIGH (ClearBlock_HI)—Offset 344h

ClearBlock Interrupt Clear Registers

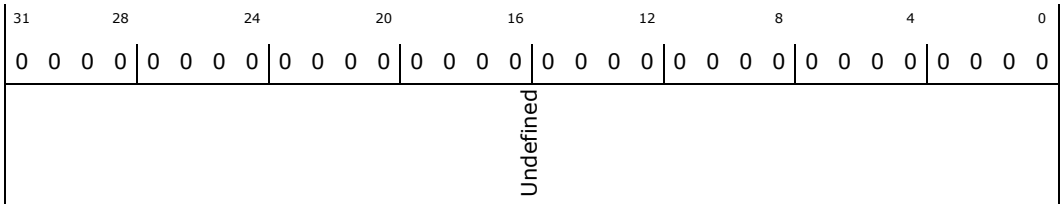
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 344h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.147 ClearSrcTran Interrupt Clear Registers - LOW (ClearSrcTran_LO)—Offset 348h

ClearSrcTran Interrupt Clear Registers

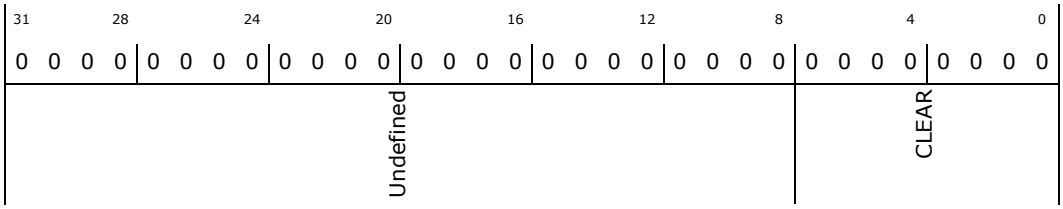
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 348h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 WO	**CLEAR:** Clear interrupt status

9.4.148 ClearSrcTran Interrupt Clear Registers - HIGH (ClearSrcTran_HI)—Offset 34Ch

ClearSrcTran Interrupt Clear Registers

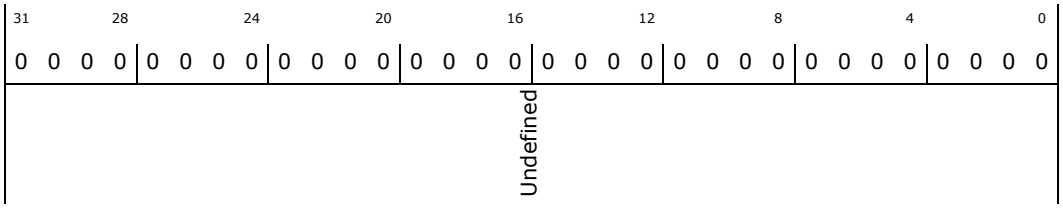
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.149 ClearDstTran Interrupt Clear Registers - LOW (ClearDstTran_LO)—Offset 350h

ClearDstTran Interrupt Clear Registers

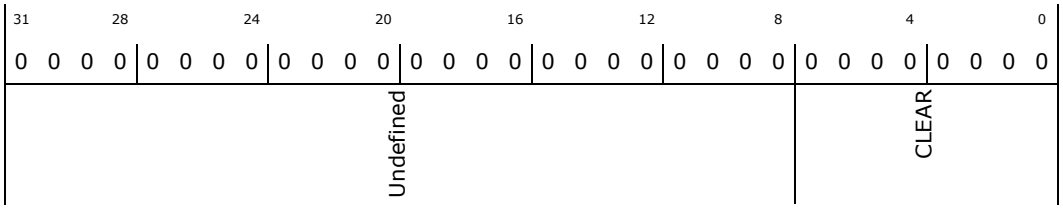
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 350h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 WO	**CLEAR:** Clear interrupt status

9.4.150 ClearDstTran Interrupt Clear Registers - HIGH (ClearDstTran_HI)—Offset 354h

ClearDstTran Interrupt Clear Registers

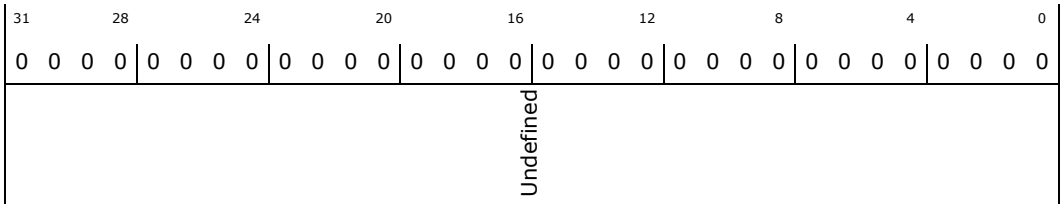
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 354h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.151 ClearErr Interrupt Clear Registers - LOW (ClearErr_LO)—Offset 358h

ClearErr Interrupt Clear Registers

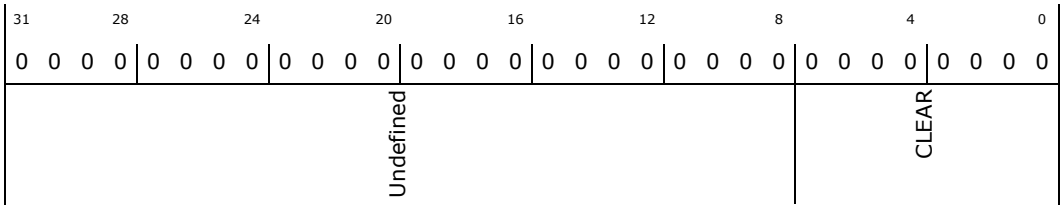
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 358h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Undefined:** Reserved
7:0	0x0 WO	**CLEAR:** Clear interrupt status

9.4.152 ClearErr Interrupt Clear Registers - HIGH (ClearErr_HI)—Offset 35Ch

ClearErr Interrupt Clear Registers

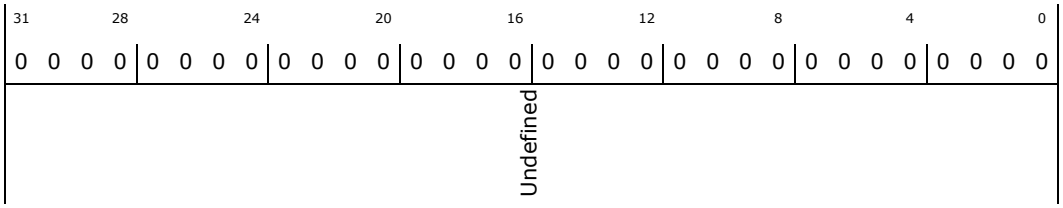
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 35Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.153 Combined Interrupt Status Register - LOW (StatusInt_LO)—Offset 360h

Combined Interrupt Status Register

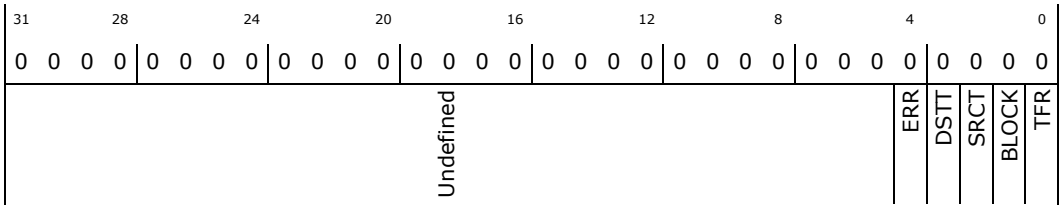
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 360h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RW	**Undefined:** Reserved
4	0x0 RO	**ERR:** OR of the contents of StatusErr register.

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RO	**DSTT:** OR of the contents of StatusDst register.
2	0x0 RO	**SRCT:** OR of the contents of StatusSrcTran register.
1	0x0 RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0x0 RO	**TFR:** OR of the contents of StatusTfr register.

9.4.154 Combined Interrupt Status Register - HIGH (StatusInt_HI)—Offset 364h

Combined Interrupt Status Register

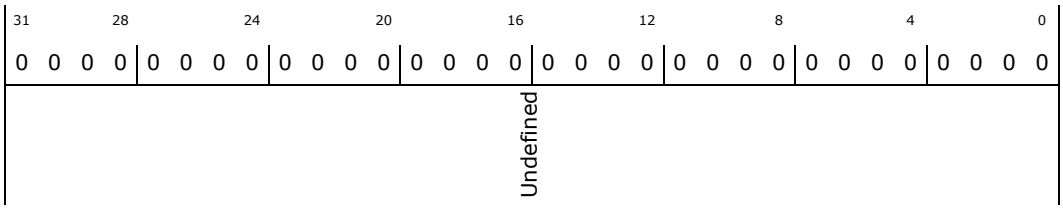
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 364h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.155 Source Software Transaction Request Register - LOW (ReqSrcReg_LO)—Offset 368h

Source Software Transaction Request Register

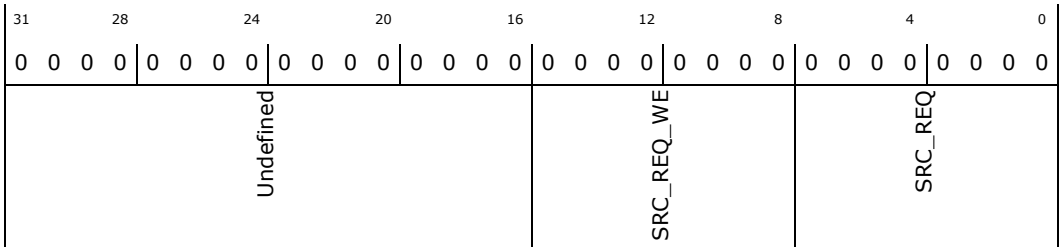
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 368h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**SRC_REQ_WE:** Source req write enable 0=write disabled 1=write enabled
7:0	0x0 RW	**SRC_REQ:** Source request

9.4.156 Source Software Transaction Request Register - HIGH (ReqSrcReg_HI)—Offset 36Ch

Source Software Transaction Request Register

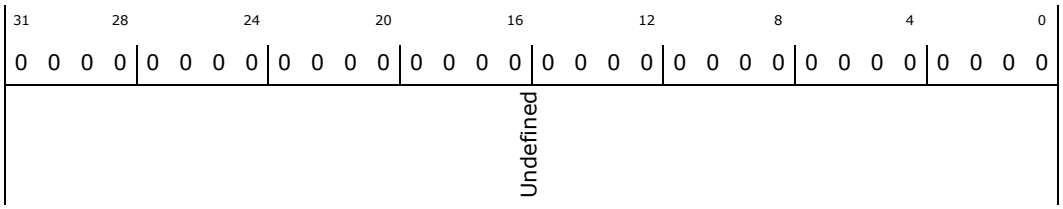
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 36Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.157 Destination Software Transaction Request Register - LOW (ReqDstReg_LO)—Offset 370h

Destination Software Transaction Request Register

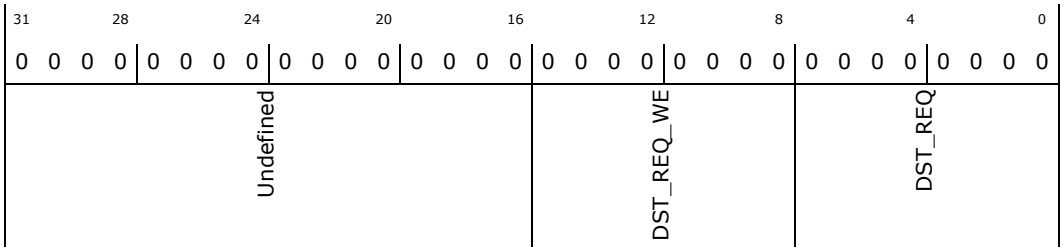
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 370h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**DST_REQ_WE:** Destination request write enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**DST_REQ:** Destination Software Transaction Request Register

9.4.158 Destination Software Transaction Request Register - HIGH (ReqDstReg_HI)—Offset 374h

Destination Software Transaction Request Register

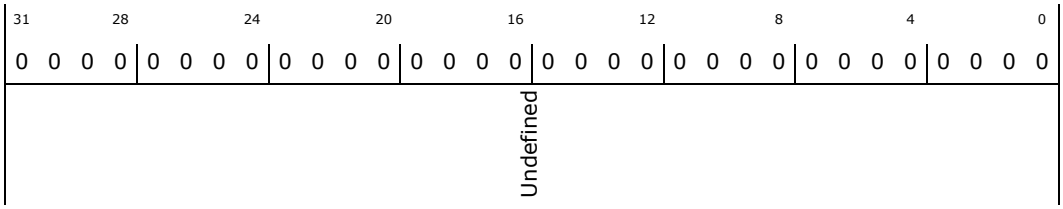
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 374h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.159 Single Source Transaction Request Register - LOW (SglRqSrcReg_LO)—Offset 378h

Single Source Transaction Request Register

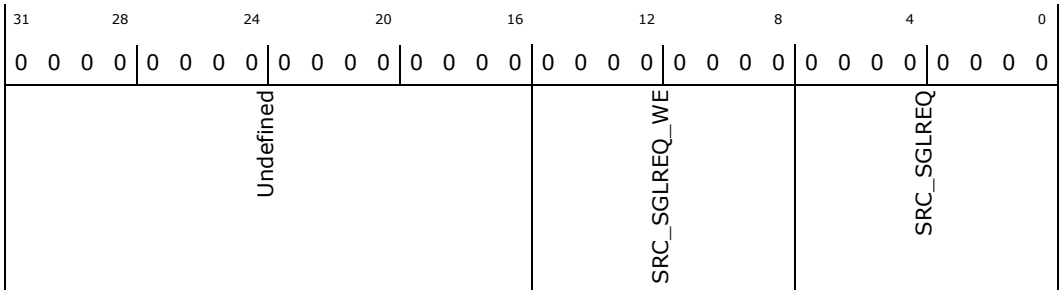
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 378h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**SRC_SGLREQ_WE:** Source req write enable 0=write disabled 1=write enabled
7:0	0x0 RW	**SRC_SGLREQ:** Source request

9.4.160 Single Source Transaction Request Register - HIGH (SglRqSrcReg_HI)—Offset 37Ch

Single Source Transaction Request Register

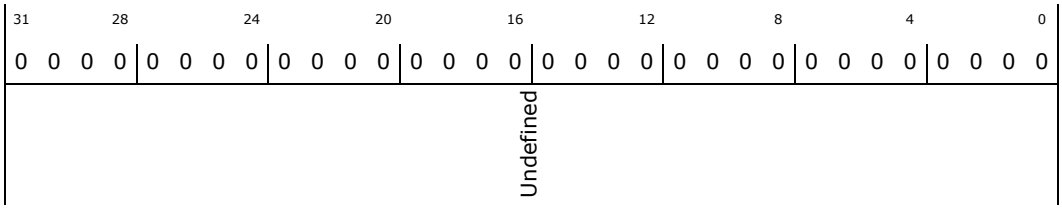
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 37Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.161 Single Destination Transaction Request Register - LOW (SglRqDstReg_LO)—Offset 380h

Single Destination Transaction Request Register

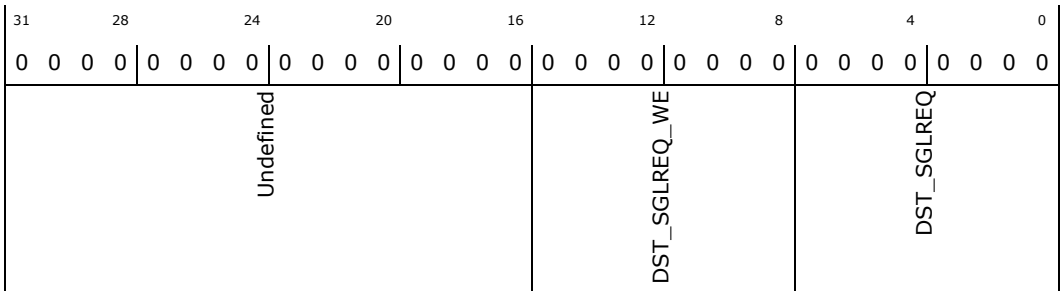
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 380h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**DST_SGLREQ_WE:** Destination request write enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**DST_SGLREQ:** Destination Software Transaction Request Register

9.4.162 Single Destination Transaction Request Register - HIGH (SglRqDstReg_HI)—Offset 384h

Single Destination Transaction Request Register

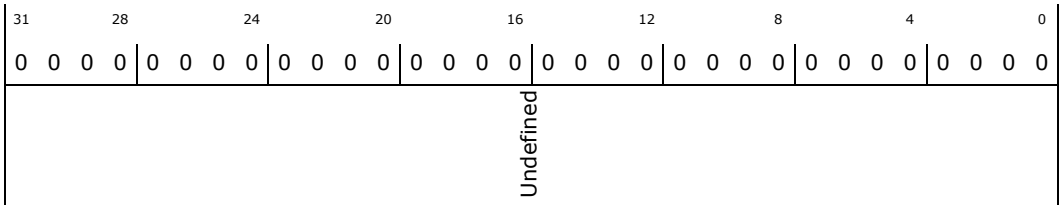
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 384h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.163 Last Source Transaction Request Register - LOW (LstSrcReg_LO)—Offset 388h

Last Source Transaction Request Register

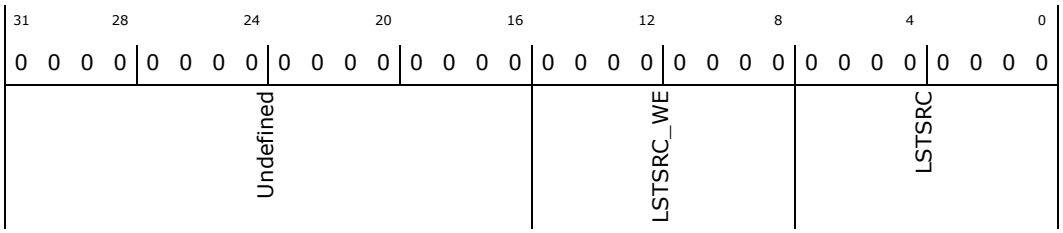
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 388h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**LSTSRC_WE:** Last Source transaction req write enable 0=write disabled 1=write enabled
7:0	0x0 RW	**LSTSRC:** Last Source transaction request 0 = Not last transaction in current block 1 = Last transaction in current block

9.4.164 Last Source Transaction Request Register - HIGH (LstSrcReg_HI)—Offset 38Ch

Last Source Transaction Request Register

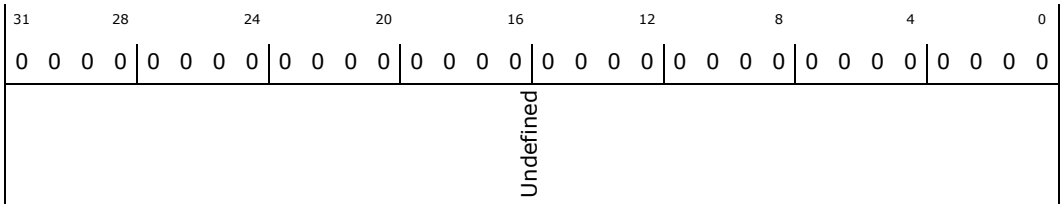
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 38Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.165 Last Destination Transaction Request Register - LOW (LstDstReg_LO)—Offset 390h

Last Destination Transaction Request Register

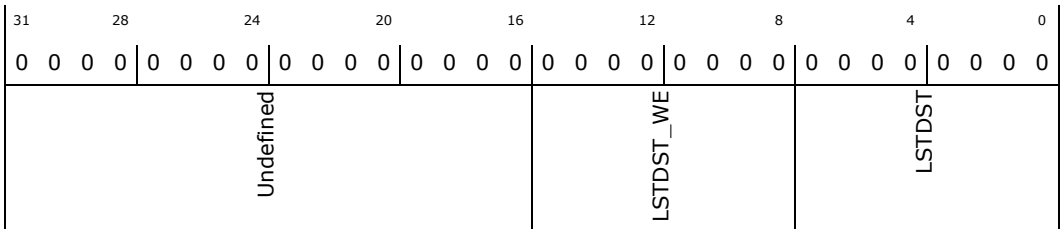
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 390h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**LSTDST_WE:** Last Destination transaction request write enable 0 = write disabled 1 = write enabled
7:0	0x0 RW	**LSTDST:** Last Destination Transaction Request Register 0 = Not last transaction in current block 1 = Last transaction in current block

9.4.166 Last Destination Transaction Request Register - HIGH (LstDstReg_HI)—Offset 394h

Last Destination Transaction Request Register

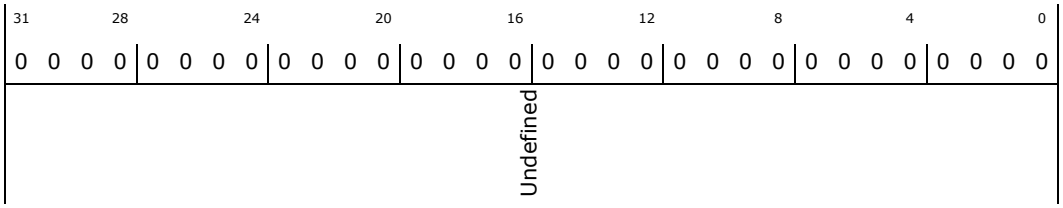
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 394h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.167 DW_ahb_dmac Configuration Register - LOW (DmaCfgReg_LO)—Offset 398h

DW_ahb_dmac Configuration Register

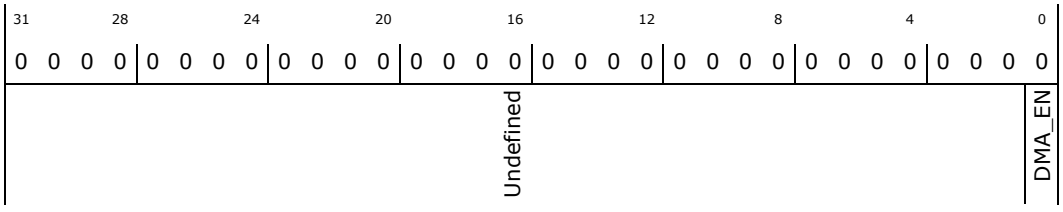
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 398h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Undefined:** Reserved
0	0x0 RW	**DMA_EN:** DW_ahb_dmac Enable bit. 0 = DW_ahb_dmac Disabled 1 = DW_ahb_dmac Enabled

9.4.168 DW_ahb_dmac Configuration Register - HIGH (DmaCfgReg_HI)—Offset 39Ch

DW_ahb_dmac Configuration Register

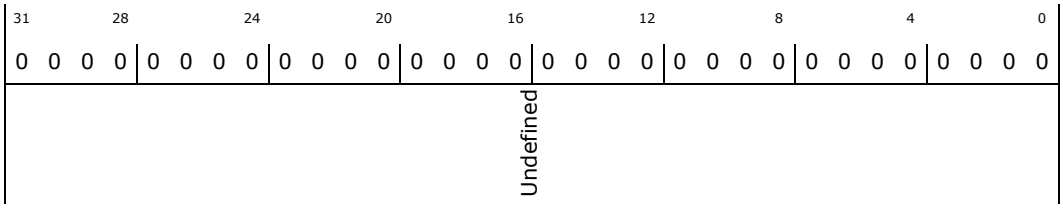
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 39Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.169 DW_ahb_dmac Channel Enable Register - LOW (ChEnReg_LO)—Offset 3A0h

DW_ahb_dmac Channel Enable Register

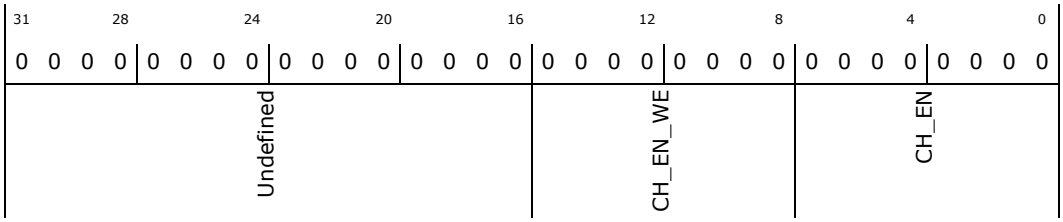
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Undefined:** Reserved
15:8	0x0 WO	**CH_EN_WE:** Channel enable write enable.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel; clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel

9.4.170 DW_ahb_dmac Channel Enable Register - HIGH (ChEnReg_HI)—Offset 3A4h

DW_ahb_dmac Channel Enable Register

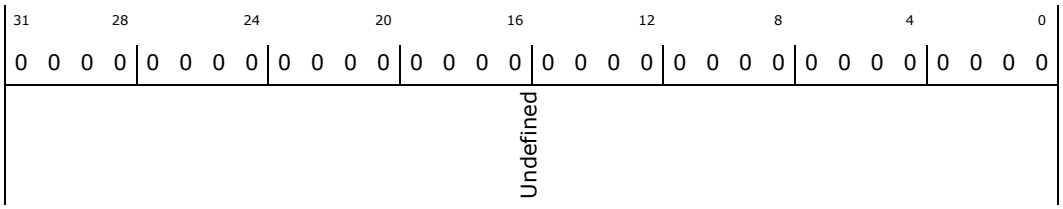
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.171 DW_ahb_dmac ID Register - LOW (DmaIdReg_LO)—Offset 3A8h

DW_ahb_dmac ID Register

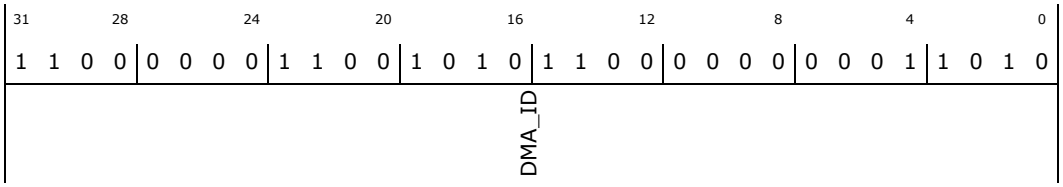
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: C0CAC01Ah



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xc0cac01a RO	**DMA_ID:** Hardcoded DW_ahb_dmac Peripheral ID

9.4.172 DW_ahb_dmac ID Register - HIGH (DmaIdReg_HI)—Offset 3ACh

DW_ahb_dmac ID Register

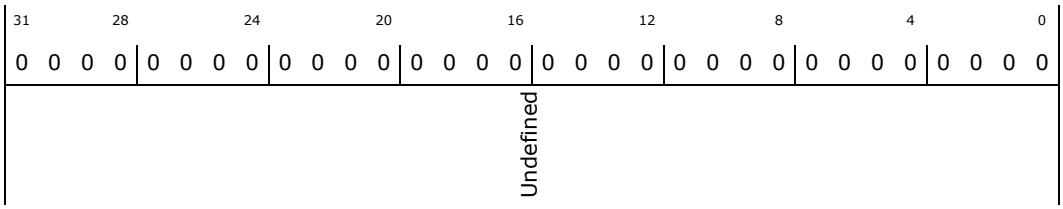
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3ACh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.173 DW_ahb_dmac Test Register - LOW (DmaTestReg_LO)—Offset 3B0h

DW_ahb_dmac Test Register

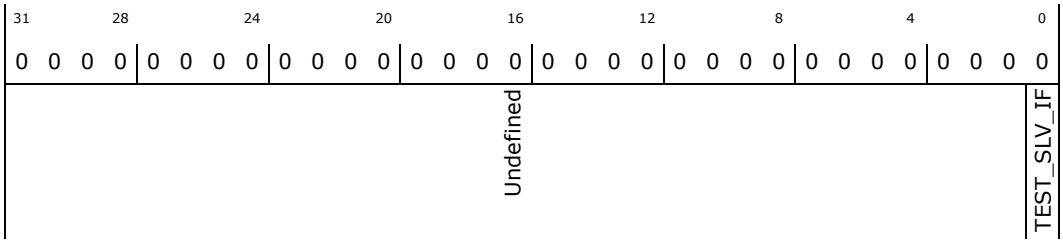
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3B0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Undefined:** Reserved
0	0x0 RW	**TEST_SLV_IF:** Puts the AHB slave interface into test mode. In this mode, the readback value of the writable registers always matches the value written. This bit does not allow writing to read-only registers. 0 = Normal mode 1 = Test mode

9.4.174 DW_ahb_dmac Test Register - HIGH (DmaTestReg_HI)—Offset 3B4h

DW_ahb_dmac Test Register

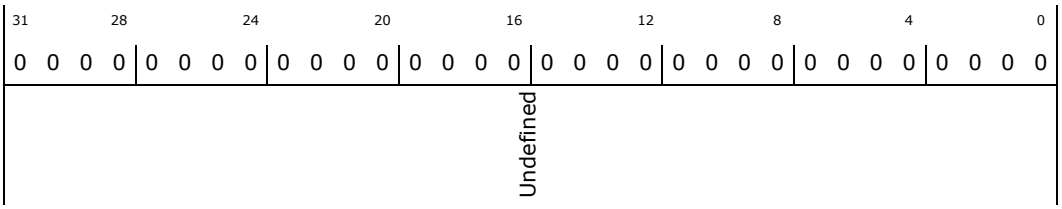
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3B4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Undefined:** Reserved

9.4.175 DW_ahb_dmac Component Parameters Register 6 - LOW (DMA_COMP_PARAMS_6_LO)—Offset 3C8h

DW_ahb_dmac Component Parameters Register 6

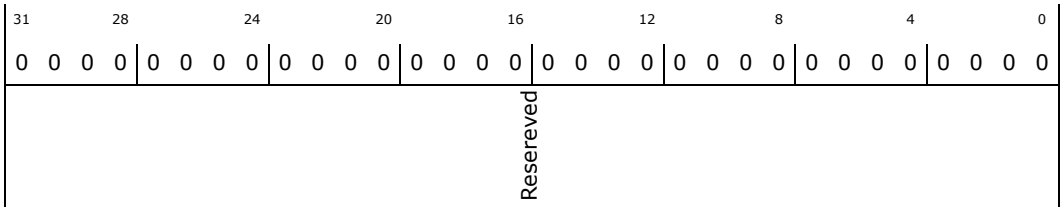
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3C8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Resereved:** Resereved

9.4.176 DW_ahb_dmac Component Parameters Register 6 - HIGH (DMA_COMP_PARAMS_6_HI)—Offset 3CCh

DW_ahb_dmac Component Parameters Register 6

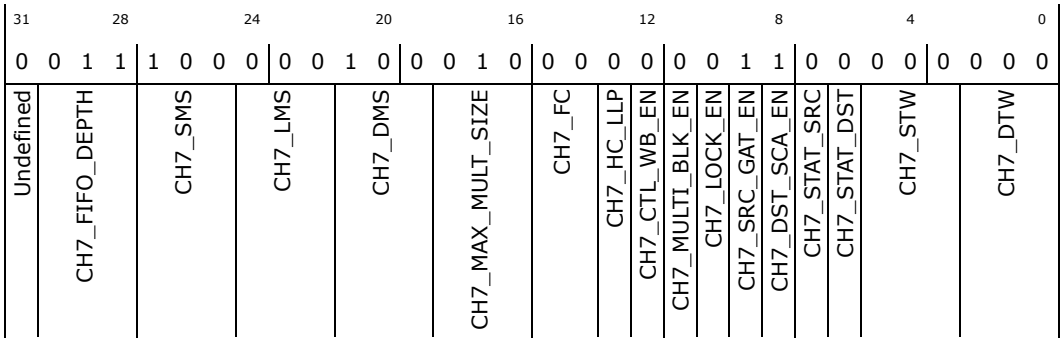
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3CCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Undefined:** Reserved
30:28	0x3 RO	**CH7_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH7_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 8 0x1 = 16 0x2 = 32 0x3 = 64 0x4 = 128
27:25	0x4 RO	**CH7_SMS:** The value of this register is derived from the DMAH_CH7_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE

Bit Range	Default & Access	Field Name (ID): Description
24:22	0x0 RO	**CH7_LMS:** The value of this register is derived from the DMAH_CH7_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
21:19	0x4 RO	**CH7_DMS:** The value of this register is derived from the DMAH_CH7_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
18:16	0x2 RO	**CH7_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH7_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 4 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
15:14	0x0 RO	**CH7_FC:** The value of this register is derived from the DMAH_CH7_FC coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = DMA 0x1 = SRC 0x2 = DST 0x3 = ANY
13	0x0 RO	**CH7_HC_LLP:** The value of this register is derived from the DMAH_CH7_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. 0x0 = FALSE 0x1 = TRUE
12	0x0 RO	**CH7_CTL_WB_EN:** The value of this register is derived from the DMAH_CH7_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
11	0x0 RO	**CH7_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH7_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. 0x0 = FALSE 0x1 = TRUE
10	0x0 RO	**CH7_LOCK_EN:** The value of this register is derived from the DMAH_CH7_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = FALSE 0x1 = TRUE
9	0x1 RO	**CH7_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH7_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
8	0x1 RO	**CH7_DST_SCA_EN:** The value of this register is derived from the DMAH_CH7_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
7	0x0 RO	**CH7_STAT_SRC:** The value of this register is derived from the DMAH_CH7_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
6	0x0 RO	**CH7_STAT_DST:** The value of this register is derived from the DMAH_CH7_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
5:3	0x0 RO	**CH7_STW:** The value of this register is derived from the DMAH_CH7_STW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
2:0	0x0 RO	**CH7_DTW:** The value of this register is derived from the DMAH_CH7_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved

9.4.177 DW_ahb_dmac Component Parameters Register 5 - LOW (DMA_COMP_PARAMS_5_LO)—Offset 3D0h

DW_ahb_dmac Component Parameters Register 5

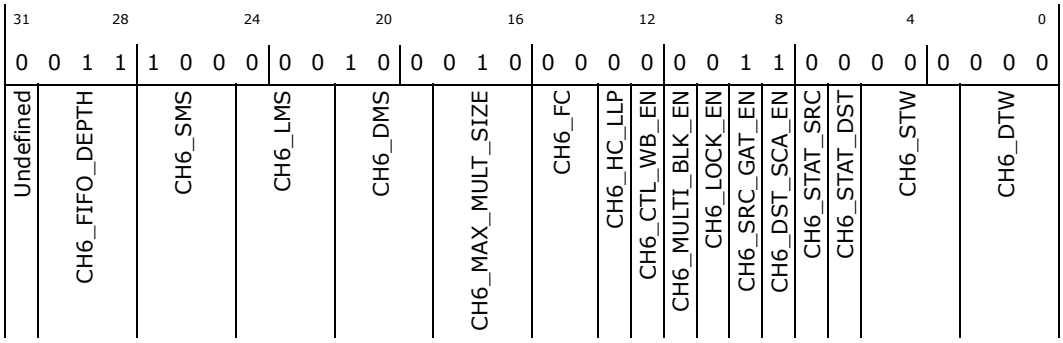
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3D0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Undefined:** Reserved
30:28	0x3 RO	**CH6_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH6_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 8 0x1 = 16 0x2 = 3 20x3 = 64 0x4 = 128
27:25	0x4 RO	**CH6_SMS:** The value of this register is derived from the DMAH_CH6_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
24:22	0x0 RO	**CH6_LMS:** The value of this register is derived from the DMAH_CH6_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
21:19	0x4 RO	**CH6_DMS:** The value of this register is derived from the DMAH_CH6_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
18:16	0x2 RO	**CH6_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH6_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 4 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
15:14	0x0 RO	**CH6_FC:** The value of this register is derived from the DMAH_CH6_FC coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = DMA 0x1 = SRC 0x2 = DST 0x3 = ANY

Bit Range	Default & Access	Field Name (ID): Description
13	0x0 RO	**CH6_HC_LLP:** The value of this register is derived from the DMAH_CH6_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. 0x0 = FALSE 0x1 = TRUE
12	0x0 RO	**CH6_CTL_WB_EN:** The value of this register is derived from the DMAH_CH6_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
11	0x0 RO	**CH6_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH6_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. 0x0 = FALSE 0x1 = TRUE
10	0x0 RO	**CH6_LOCK_EN:** The value of this register is derived from the DMAH_CH6_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = FALSE 0x1 = TRUE
9	0x1 RO	**CH6_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH6_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
8	0x1 RO	**CH6_DST_SCA_EN:** The value of this register is derived from the DMAH_CH6_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
7	0x0 RO	**CH6_STAT_SRC:** The value of this register is derived from the DMAH_CH6_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
6	0x0 RO	**CH6_STAT_DST:** The value of this register is derived from the DMAH_CH6_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
5:3	0x0 RO	**CH6_STW:** The value of this register is derived from the DMAH_CH6_STW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
2:0	0x0 RO	**CH6_DTW:** The value of this register is derived from the DMAH_CH6_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved

9.4.178 DW_ahb_dmac Component Parameters Register 5 - HIGH (DMA_COMP_PARAMS_5_HI)—Offset 3D4h

DW_ahb_dmac Component Parameters Register 5

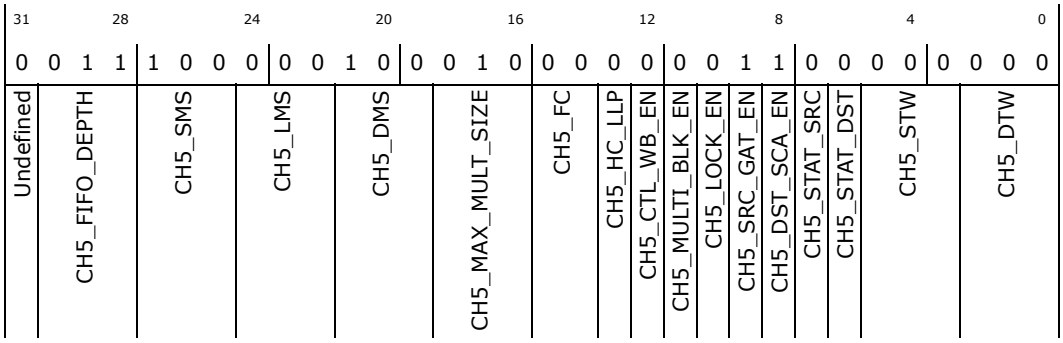
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3D4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Undefined:** Reserved
30:28	0x3 RO	**CH5_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH5_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 8 0x1 = 16 0x2 = 3 20x3 = 64 0x4 = 128
27:25	0x4 RO	**CH5_SMS:** The value of this register is derived from the DMAH_CH5_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
24:22	0x0 RO	**CH5_LMS:** The value of this register is derived from the DMAH_CH5_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
21:19	0x4 RO	**CH5_DMS:** The value of this register is derived from the DMAH_CH5_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
18:16	0x2 RO	**CH5_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH5_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 4 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
15:14	0x0 RO	**CH5_FC:** The value of this register is derived from the DMAH_CH5_FC coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = DMA 0x1 = SRC 0x2 = DST 0x3 = ANY
13	0x0 RO	**CH5_HC_LLP:** The value of this register is derived from the DMAH_CH5_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. 0x0 = FALSE 0x1 = TRUE
12	0x0 RO	**CH5_CTL_WB_EN:** The value of this register is derived from the DMAH_CH5_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
11	0x0 RO	**CH5_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH5_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. 0x0 = FALSE 0x1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RO	**CH5_LOCK_EN:** The value of this register is derived from the DMAH_CH5_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = FALSE 0x1 = TRUE
9	0x1 RO	**CH5_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH5_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
8	0x1 RO	**CH5_DST_SCA_EN:** The value of this register is derived from the DMAH_CH5_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
7	0x0 RO	**CH5_STAT_SRC:** The value of this register is derived from the DMAH_CH5_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
6	0x0 RO	**CH5_STAT_DST:** The value of this register is derived from the DMAH_CH5_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
5:3	0x0 RO	**CH5_STW:** The value of this register is derived from the DMAH_CH5_STW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
2:0	0x0 RO	**CH5_DTW:** The value of this register is derived from the DMAH_CH5_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved

9.4.179 DW_ahb_dmac Component Parameters Register 4 - LOW (DMA_COMP_PARAMS_4_LO)—Offset 3D8h

DW_ahb_dmac Component Parameters Register 4

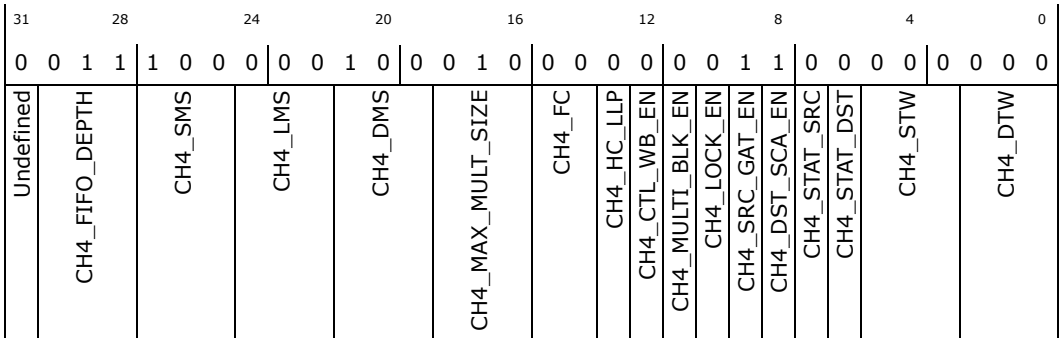
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3D8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Undefined:** Reserved
30:28	0x3 RO	**CH4_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH4_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 8 0x1 = 16 0x2 = 3 20x3 = 64 0x4 = 128
27:25	0x4 RO	**CH4_SMS:** The value of this register is derived from the DMAH_CH4_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
24:22	0x0 RO	**CH4_LMS:** The value of this register is derived from the DMAH_CH4_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
21:19	0x4 RO	**CH4_DMS:** The value of this register is derived from the DMAH_CH4_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
18:16	0x2 RO	**CH4_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH4_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 4 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
15:14	0x0 RO	**CH4_FC:** The value of this register is derived from the DMAH_CH4_FC coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = DMA 0x1 = SRC 0x2 = DST 0x3 = ANY
13	0x0 RO	**CH4_HC_LLP:** The value of this register is derived from the DMAH_CH4_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. 0x0 = FALSE 0x1 = TRUE
12	0x0 RO	**CH4_CTL_WB_EN:** The value of this register is derived from the DMAH_CH4_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
11	0x0 RO	**CH4_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH4_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. 0x0 = FALSE 0x1 = TRUE
10	0x0 RO	**CH4_LOCK_EN:** The value of this register is derived from the DMAH_CH4_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = FALSE 0x1 = TRUE
9	0x1 RO	**CH4_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH4_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
8	0x1 RO	**CH4_DST_SCA_EN:** The value of this register is derived from the DMAH_CH4_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
7	0x0 RO	**CH4_STAT_SRC:** The value of this register is derived from the DMAH_CH4_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
6	0x0 RO	**CH4_STAT_DST:** The value of this register is derived from the DMAH_CH4_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
5:3	0x0 RO	**CH4_STW:** The value of this register is derived from the DMAH_CH4_STW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
2:0	0x0 RO	**CH4_DTW:** The value of this register is derived from the DMAH_CH4_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved

9.4.180 DW_ahb_dmac Component Parameters Register 4 - HIGH (DMA_COMP_PARAMS_4_HI)—Offset 3DCh

DW_ahb_dmac Component Parameters Register 4

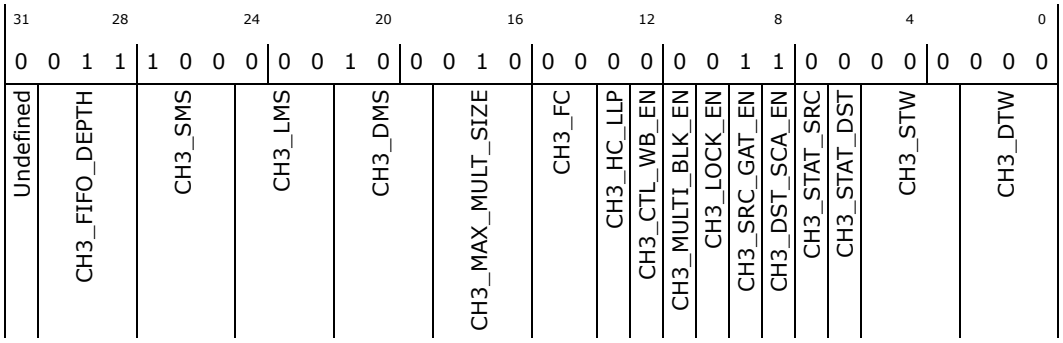
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3DCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Undefined:** Reserved
30:28	0x3 RO	**CH3_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH3_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 8 0x1 = 16 0x2 = 3 20x3 = 64 0x4 = 128
27:25	0x4 RO	**CH3_SMS:** The value of this register is derived from the DMAH_CH3_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE

Bit Range	Default & Access	Field Name (ID): Description
24:22	0x0 RO	**CH3_LMS:** The value of this register is derived from the DMAH_CH3_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
21:19	0x4 RO	**CH3_DMS:** The value of this register is derived from the DMAH_CH3_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
18:16	0x2 RO	**CH3_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH3_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 4 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
15:14	0x0 RO	**CH3_FC:** The value of this register is derived from the DMAH_CH3_FC coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = DMA 0x1 = SRC 0x2 = DST 0x3 = ANY
13	0x0 RO	**CH3_HC_LLP:** The value of this register is derived from the DMAH_CH3_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. 0x0 = FALSE 0x1 = TRUE
12	0x0 RO	**CH3_CTL_WB_EN:** The value of this register is derived from the DMAH_CH3_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
11	0x0 RO	**CH3_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH3_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. 0x0 = FALSE 0x1 = TRUE
10	0x0 RO	**CH3_LOCK_EN:** The value of this register is derived from the DMAH_CH3_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = FALSE 0x1 = TRUE
9	0x1 RO	**CH3_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH3_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
8	0x1 RO	**CH3_DST_SCA_EN:** The value of this register is derived from the DMAH_CH3_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
7	0x0 RO	**CH3_STAT_SRC:** he value of this register is derived from the DMAH_CH3_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
6	0x0 RO	**CH3_STAT_DST:** The value of this register is derived from the DMAH_CH3_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
5:3	0x0 RO	**CH3_STW:** The value of this register is derived from the DMAH_CH3_STW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
2:0	0x0 RO	**CH3_DTW:** The value of this register is derived from the DMAH_CH3_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved

9.4.181 DW_ahb_dmac Component Parameters Register 3 - LOW (DMA_COMP_PARAMS_3_LO)—Offset 3E0h

DW_ahb_dmac Component Parameters Register 3

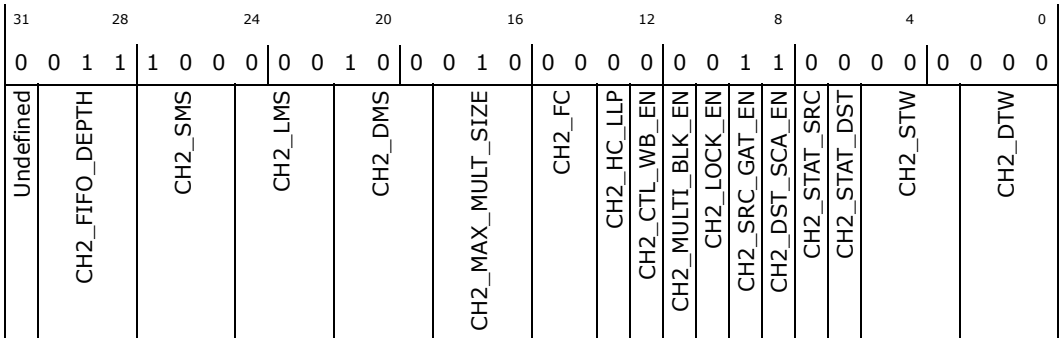
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3E0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Undefined:** Reserved
30:28	0x3 RO	**CH2_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH2_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 8 0x1 = 16 0x2 = 3 20x3 = 64 0x4 = 128
27:25	0x4 RO	**CH2_SMS:** The value of this register is derived from the DMAH_CH2_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
24:22	0x0 RO	**CH2_LMS:** The value of this register is derived from the DMAH_CH2_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
21:19	0x4 RO	**CH2_DMS:** The value of this register is derived from the DMAH_CH2_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
18:16	0x2 RO	**CH2_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH2_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 4 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
15:14	0x0 RO	**CH2_FC:** The value of this register is derived from the DMAH_CH2_FC coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = DMA 0x1 = SRC 0x2 = DST 0x3 = ANY

Bit Range	Default & Access	Field Name (ID): Description
13	0x0 RO	**CH2_HC_LLP:** The value of this register is derived from the DMAH_CH2_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. 0x0 = FALSE 0x1 = TRUE
12	0x0 RO	**CH2_CTL_WB_EN:** The value of this register is derived from the DMAH_CH2_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
11	0x0 RO	**CH2_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH2_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to . 0x0 = FALSE 0x1 = TRUE
10	0x0 RO	**CH2_LOCK_EN:** The value of this register is derived from the DMAH_CH2_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = FALSE 0x1 = TRUE
9	0x1 RO	**CH2_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH2_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
8	0x1 RO	**CH2_DST_SCA_EN:** The value of this register is derived from the DMAH_CH2_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
7	0x0 RO	**CH2_STAT_SRC:** The value of this register is derived from the DMAH_CH2_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
6	0x0 RO	**CH2_STAT_DST:** The value of this register is derived from the DMAH_CH2_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
5:3	0x0 RO	**CH2_STW:** The value of this register is derived from the DMAH_CH2_STW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
2:0	0x0 RO	**CH2_DTW:** The value of this register is derived from the DMAH_CH2_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved

9.4.182 DW_ahb_dmac Component Parameters Register 3 - HIGH (DMA_COMP_PARAMS_3_HI)—Offset 3E4h

DW_ahb_dmac Component Parameters Register 3

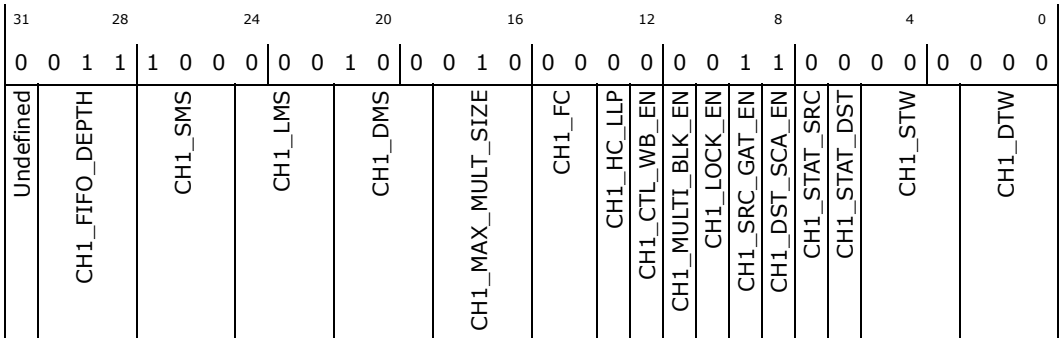
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3E4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Undefined:** Reserved
30:28	0x3 RO	**CH1_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH1_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 8 0x1 = 16 0x2 = 3 20x3 = 64 0x4 = 128
27:25	0x4 RO	**CH1_SMS:** The value of this register is derived from the DMAH_CH1_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
24:22	0x0 RO	**CH1_LMS:** The value of this register is derived from the DMAH_CH1_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
21:19	0x4 RO	**CH1_DMS:** The value of this register is derived from the DMAH_CH1_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
18:16	0x2 RO	**CH1_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH1_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 4 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
15:14	0x0 RO	**CH1_FC:** The value of this register is derived from the DMAH_CH1_FC coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = DMA 0x1 = SRC 0x2 = DST 0x3 = ANY
13	0x0 RO	**CH1_HC_LLP:** The value of this register is derived from the DMAH_CH1_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. 0x0 = FALSE 0x1 = TRUE
12	0x0 RO	**CH1_CTL_WB_EN:** The value of this register is derived from the DMAH_CH1_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
11	0x0 RO	**CH1_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH1_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. 0x0 = FALSE 0x1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RO	**CH1_LOCK_EN:** The value of this register is derived from the DMAH_CH1_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = FALSE 0x1 = TRUE
9	0x1 RO	**CH1_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH1_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
8	0x1 RO	**CH1_DST_SCA_EN:** The value of this register is derived from the DMAH_CH1_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
7	0x0 RO	**CH1_STAT_SRC:** The value of this register is derived from the DMAH_CH1_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
6	0x0 RO	**CH1_STAT_DST:** The value of this register is derived from the DMAH_CH1_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
5:3	0x0 RO	**CH1_STW:** The value of this register is derived from the DMAH_CH1_STW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
2:0	0x0 RO	**CH1_DTW:** The value of this register is derived from the DMAH_CH1_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved

9.4.183 DW_ahb_dmac Component Parameters Register 2 - LOW (DMA_COMP_PARAMS_2_LO)—Offset 3E8h

DW_ahb_dmac Component Parameters Register 2

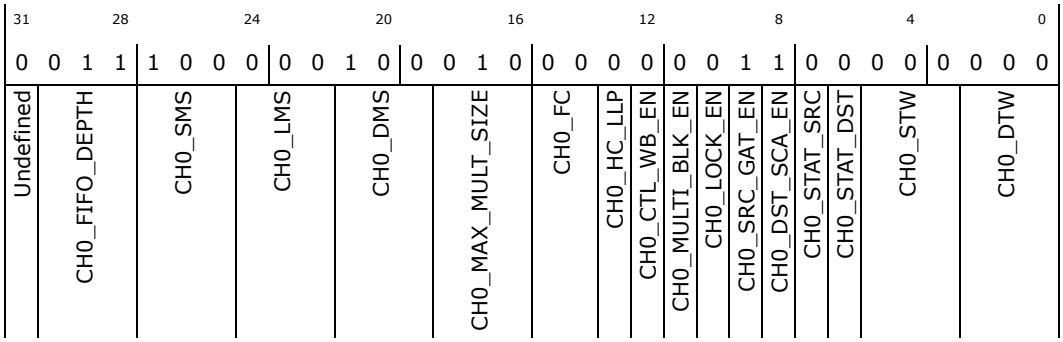
Access Method

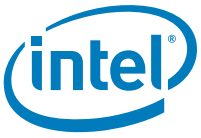
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3E8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 38220300h





Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Undefined:** Reserved
30:28	0x3 RO	**CH0_FIFO_DEPTH:** The value of this register is derived from the DMAH_CH0_FIFO_DEPTH coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 8 0x1 = 16 0x2 = 3 20x3 = 64 0x4 = 128
27:25	0x4 RO	**CH0_SMS:** The value of this register is derived from the DMAH_CH0_SMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
24:22	0x0 RO	**CH0_LMS:** The value of this register is derived from the DMAH_CH0_LMS coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
21:19	0x4 RO	**CH0_DMS:** The value of this register is derived from the DMAH_CH0_DMS coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = MASTER_1 0x1 = MASTER_2 0x2 = MASTER_3 0x3 = MASTER_4 0x4 = NO_HARDCODE
18:16	0x2 RO	**CH0_MAX_MULT_SIZE:** The value of this register is derived from the DMAH_CH0_MULT_SIZE coreConsultant parameter. For a description of this parameter, refer to page 106. 0x0 = 4 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
15:14	0x0 RO	**CH0_FC:** The value of this register is derived from the DMAH_CH0_FC coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = DMA 0x1 = SRC 0x2 = DST 0x3 = ANY
13	0x0 RO	**CH0_HC_LLP:** The value of this register is derived from the DMAH_CH0_HC_LLP coreConsultant parameter. For a description of this parameter, refer to page 110. 0x0 = FALSE 0x1 = TRUE
12	0x0 RO	**CH0_CTL_WB_EN:** The value of this register is derived from the DMAH_CH0_CTL_WB_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
11	0x0 RO	**CH0_MULTI_BLK_EN:** The value of this register is derived from the DMAH_CH0_MULTI_BLK_EN coreConsultant parameter. For a description of this parameter, refer to page 109. 0x0 = FALSE 0x1 = TRUE
10	0x0 RO	**CH0_LOCK_EN:** The value of this register is derived from the DMAH_CH0_LOCK_EN coreConsultant parameter. For a description of this parameter, refer to page 107. 0x0 = FALSE 0x1 = TRUE
9	0x1 RO	**CH0_SRC_GAT_EN:** The value of this register is derived from the DMAH_CH0_SRC_GAT_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
8	0x1 RO	**CH0_DST_SCA_EN:** The value of this register is derived from the DMAH_CH0_DST_SCA_EN coreConsultant parameter. For a description of this parameter, refer to page 112. 0x0 = FALSE 0x1 = TRUE
7	0x0 RO	**CH0_STAT_SRC:** The value of this register is derived from the DMAH_CH0_STAT_SRC coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE

Bit Range	Default & Access	Field Name (ID): Description
6	0x0 RO	**CH0_STAT_DST:** The value of this register is derived from the DMAH_CH0_STAT_DST coreConsultant parameter. For a description of this parameter, refer to page 111. 0x0 = FALSE 0x1 = TRUE
5:3	0x0 RO	**CH0_STW:** The value of this register is derived from the DMAH_CH0_STW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved
2:0	0x0 RO	**CH0_DTW:** The value of this register is derived from the DMAH_CH0_DTW coreConsultant parameter. For a description of this parameter, refer to page 108. 0x0 = NO_HARDCODE 0x1 = 8 0x2 = 16 0x3 = 32 0x4 = 64 0x5 = 128 0x6 = 256 0x7 = reserved

9.4.184 DW_ahb_dmac Component Parameters Register 2 - HIGH (DMA_COMP_PARAMS_2_HI)—Offset 3ECh

DW_ahb_dmac Component Parameters Register 2

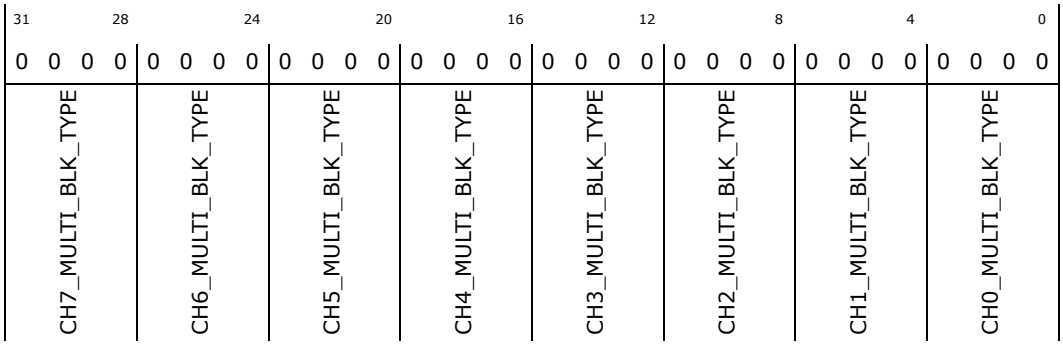
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3ECh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**CH7_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. 0x0 = NO_HARDCODE 0x1 = CONT_RELOAD 0x2 = RELOAD_CONT 0x3 = RELOAD_RELOAD 0x4 = CONT_LLP 0x5 = RELOAD_LLP 0x6 = LLP_CONT 0x7 = LLP_RELOAD 0x8 = LLP_LLP

Bit Range	Default & Access	Field Name (ID): Description
27:24	0x0 RO	**CH6_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. 0x0 = NO_HARDCODE 0x1 = CONT_RELOAD 0x2 = RELOAD_CONT 0x3 = RELOAD_RELOAD 0x4 = CONT_LLP 0x5 = RELOAD_LLP 0x6 = LLP_CONT 0x7 = LLP_RELOAD 0x8 = LLP_LLP
23:20	0x0 RO	**CH5_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. 0x0 = NO_HARDCODE 0x1 = CONT_RELOAD 0x2 = RELOAD_CONT 0x3 = RELOAD_RELOAD 0x4 = CONT_LLP 0x5 = RELOAD_LLP 0x6 = LLP_CONT 0x7 = LLP_RELOAD 0x8 = LLP_LLP
19:16	0x0 RO	**CH4_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. 0x0 = NO_HARDCODE 0x1 = CONT_RELOAD 0x2 = RELOAD_CONT 0x3 = RELOAD_RELOAD 0x4 = CONT_LLP 0x5 = RELOAD_LLP 0x6 = LLP_CONT 0x7 = LLP_RELOAD 0x8 = LLP_LLP
15:12	0x0 RO	**CH3_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. 0x0 = NO_HARDCODE 0x1 = CONT_RELOAD 0x2 = RELOAD_CONT 0x3 = RELOAD_RELOAD 0x4 = CONT_LLP 0x5 = RELOAD_LLP 0x6 = LLP_CONT 0x7 = LLP_RELOAD 0x8 = LLP_LLP
11:8	0x0 RO	**CH2_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. 0x0 = NO_HARDCODE 0x1 = CONT_RELOAD 0x2 = RELOAD_CONT 0x3 = RELOAD_RELOAD 0x4 = CONT_LLP 0x5 = RELOAD_LLP 0x6 = LLP_CONT 0x7 = LLP_RELOAD 0x8 = LLP_LLP
7:4	0x0 RO	**CH1_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. 0x0 = NO_HARDCODE 0x1 = CONT_RELOAD 0x2 = RELOAD_CONT 0x3 = RELOAD_RELOAD 0x4 = CONT_LLP 0x5 = RELOAD_LLP 0x6 = LLP_CONT 0x7 = LLP_RELOAD 0x8 = LLP_LLP
3:0	0x0 RO	**CH0_MULTI_BLK_TYPE:** The values of these bit fields are derived from the DMAH_CHx_MULTI_BLK_TYPE coreConsultant parameter. For a description of these parameters, refer to page 110. 0x0 = NO_HARDCODE 0x1 = CONT_RELOAD 0x2 = RELOAD_CONT 0x3 = RELOAD_RELOAD 0x4 = CONT_LLP 0x5 = RELOAD_LLP 0x6 = LLP_CONT 0x7 = LLP_RELOAD 0x8 = LLP_LLP

9.4.185 DW_ahb_dmac Component Parameters Register 1 - LOW (DMA_COMP_PARAMS_1_LO)—Offset 3F0h

DW_ahb_dmac Component Parameters Register 1

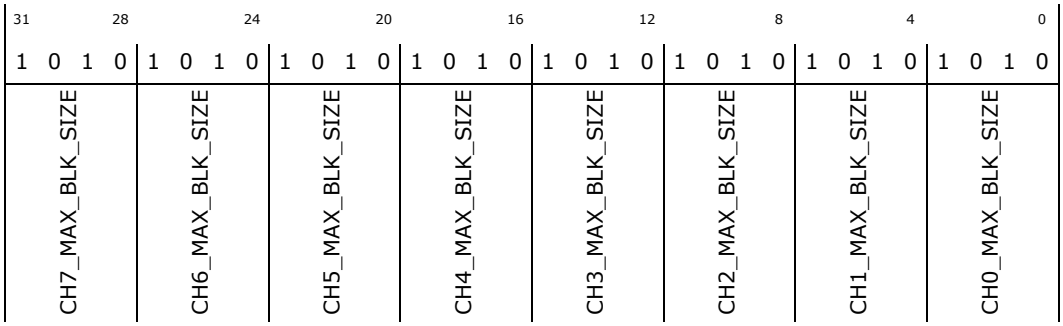
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3F0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: AAAAAAAAh



Bit Range	Default & Access	Field Name (ID): Description
31:28	0xa RO	**CH7_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. 0x0 = 3 0x1 = 7 0x2 =15 0x3 = 31 0x4 = 63 0x5 = 127 0x6 = 255 0x7 = 511 0x8 = 1023 0x9 = 2047 0xa = 4095
27:24	0xa RO	**CH6_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. 0x0 = 3 0x1 = 7 0x2 =15 0x3 = 31 0x4 = 63 0x5 = 127 0x6 = 255 0x7 = 511 0x8 = 1023 0x9 = 2047 0xa = 4095
23:20	0xa RO	**CH5_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. 0x0 = 3 0x1 = 7 0x2 =15 0x3 = 31 0x4 = 63 0x5 = 127 0x6 = 255 0x7 = 511 0x8 = 1023 0x9 = 2047 0xa = 4095
19:16	0xa RO	**CH4_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. 0x0 = 3 0x1 = 7 0x2 =15 0x3 = 31 0x4 = 63 0x5 = 127 0x6 = 255 0x7 = 511 0x8 = 1023 0x9 = 2047 0xa = 4095
15:12	0xa RO	**CH3_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. 0x0 = 3 0x1 = 7 0x2 =15 0x3 = 31 0x4 = 63 0x5 = 127 0x6 = 255 0x7 = 511 0x8 = 1023 0x9 = 2047 0xa = 4095
11:8	0xa RO	**CH2_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. 0x0 = 3 0x1 = 7 0x2 =15 0x3 = 31 0x4 = 63 0x5 = 127 0x6 = 255 0x7 = 511 0x8 = 1023 0x9 = 2047 0xa = 4095
7:4	0xa RO	**CH1_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. 0x0 = 3 0x1 = 7 0x2 =15 0x3 = 31 0x4 = 63 0x5 = 127 0x6 = 255 0x7 = 511 0x8 = 1023 0x9 = 2047 0xa = 4095
3:0	0xa RO	**CH0_MAX_BLK_SIZE:** The values of these bit fields are derived from the DMAH_CHx_MAX_BLK_SIZE coreConsultant parameter. For a description of these parameters, refer to page 107. 0x0 = 3 0x1 = 7 0x2 =15 0x3 = 31 0x4 = 63 0x5 = 127 0x6 = 255 0x7 = 511 0x8 = 1023 0x9 = 2047 0xa = 4095

9.4.186 DW_ahb_dmac Component Parameters Register 1 - HIGH (DMA_COMP_PARAMS_1_HI)—Offset 3F4h

DW_ahb_dmac Component Parameters Register 1

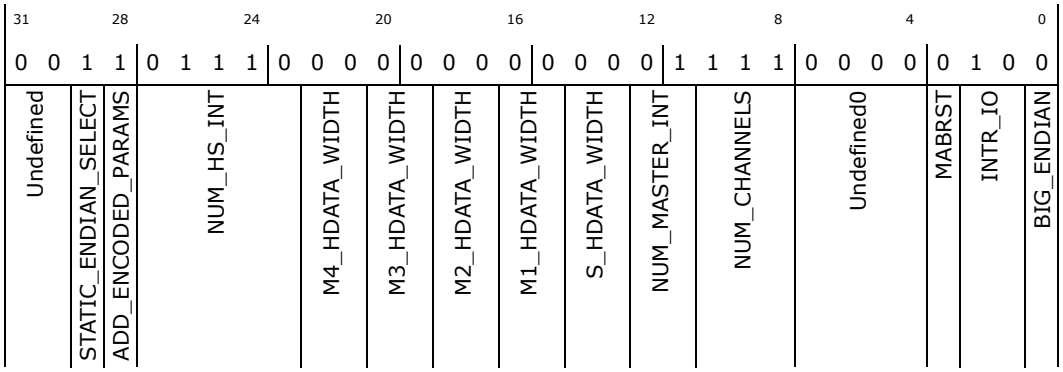
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 37000F04h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**Undefined:** Reserved
29	0x1 RO	**STATIC_ENDIAN_SELECT:** The value of this register is derived from the DMAH_STATIC_ENDIAN_SELECT coreConsultant parameter. For a description of this parameter, refer to page 104. 0 = FALSE 1 = TRUE
28	0x1 RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the DMAH_ADD_ENCODED_PARAMS coreConsultant parameter. For a description of this parameter, refer to page 104. 0 = FALSE 1 = TRUE
27:23	0xe RO	**NUM_HS_INT:** The value of this register is derived from the DMAH_NUM_HS_INT coreConsultant parameter. For a description of this parameter, refer to page 102. 0x00 = 0 to 0x10 = 16
22:21	0x0 RO	**M4_HDATA_WIDTH:** The value of this register is derived from the DMAH_M4_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. 0x0 = 32 bits 0x1 = 64 bits 0x2 = 128 bits 0x3 = 256 bits
20:19	0x0 RO	**M3_HDATA_WIDTH:** The value of this register is derived from the DMAH_M3_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. 0x0 = 32 bits 0x1 = 64 bits 0x2 = 128 bits 0x3 = 256 bits
18:17	0x0 RO	**M2_HDATA_WIDTH:** The value of this register is derived from the DMAH_M2_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. 0x0 = 32 bits 0x1 = 64 bits 0x2 = 128 bits 0x3 = 256 bits

Bit Range	Default & Access	Field Name (ID): Description
16:15	0x0 RO	**M1_HDATA_WIDTH:** The value of this register is derived from the DMAH_M1_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. 0x0 = 32 bits 0x1 = 64 bits 0x2 = 128 bits 0x3 = 256 bits
14:13	0x0 RO	**S_HDATA_WIDTH:** The value of this register is derived from the DMAH_S_HDATA_WIDTH coreConsultant parameter. For a description of this parameter, refer to page 105. 0x0 = 32 bits 0x1 = 64 bits 0x2 = 128 bits 0x3 = 256 bits
12:11	0x1 RO	**NUM_MASTER_INT:** The value of this register is derived from the DMAH_NUM_MASTER_INT coreConsultant parameter. For a description of this parameter, refer to page 102. 0x0 = 1 to 0x3 = 4
10:8	0x7 RO	**NUM_CHANNELS:** The value of this register is derived from the DMAH_NUM_CHANNELS coreConsultant parameter. For a description of this parameter, refer to page 102. 0x0 = 1 to 0x7 = 8
7:4	0x0 RW	**Undefined0:** Reserved
3	0x0 RO	**MABRST:** The value of this register is derived from the DMAH_MABRST coreConsultant parameter. For a description of this parameter, refer to page 103. 0 = FALSE 1 = TRUE
2:1	0x2 RO	**INTR_IO:** The value of this register is derived from the DMAH_INTR_IO coreConsultant parameter. For a description of this parameter, refer to page 103. 0x0 = ALL 0x1 = TYPE 0x2 = COMBINED 0x3 = reserved
0	0x0 RO	**BIG_ENDIAN:** The value of this register is derived from the DMAH_BIG_ENDIAN coreConsultant parameter. For a description of this parameter, refer to page 104. 0 = FALSE 1 = TRUE

9.4.187 DMA Component ID Register - LOW (DmaCompsID_LO)—Offset 3F8h

DMA Component ID Register

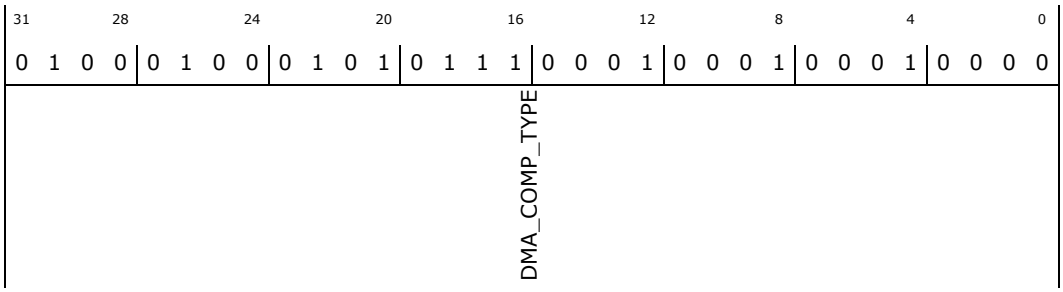
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 44571110h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x44571110 RO	**DMA_COMP_TYPE:** Designware Component Type number = 0x44_57_11_10. This assigned unique hex value is constant and is derived from the two ASCII letters -DW- followed by a 32-bit unsigned number.

9.4.188 DMA Component ID Register - HIGH (DmaCompsID_HI)—Offset 3FCh

DMA Component ID Register

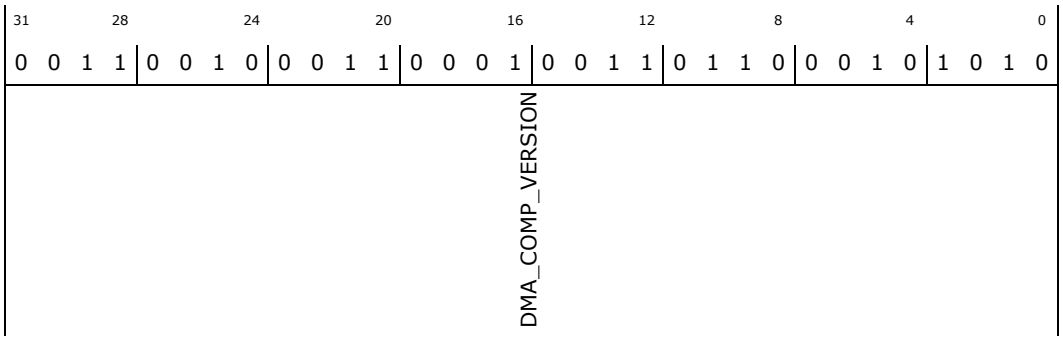
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:0] + 10h

Default: 3231362Ah



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x3231362a RO	**DMA_COMP_VERSION:** Version of the component

9.5 SIO SPI PCI Configuration Registers

Table 68. Summary of SIO SPI PCI Configuration Registers—0/30/5

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4195	00008086h
4–7h	4	"STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h" on page 4195	00100000h
8–Bh	4	"REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4197	00000000h
C–Fh	4	"CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4198	00800000h
10–13h	4	"BAR -Base Address Register (BAR)—Offset 10h" on page 4198	00000000h
14–17h	4	"BAR1 -Base Address Register1 (BAR1)—Offset 14h" on page 4199	00000000h
2C–2Fh	4	"SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4200	00000000h
30–33h	4	"EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4201	00000000h
34–37h	4	"CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4201	00000000h
3C–3Fh	4	"INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4202	00000100h
80–83h	4	"POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4202	00030001h
84–87h	4	"PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4203	00000008h
F8–FBh	4	"Manufacturers ID (MANID)—Offset F8h" on page 4204	00000000h

9.5.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

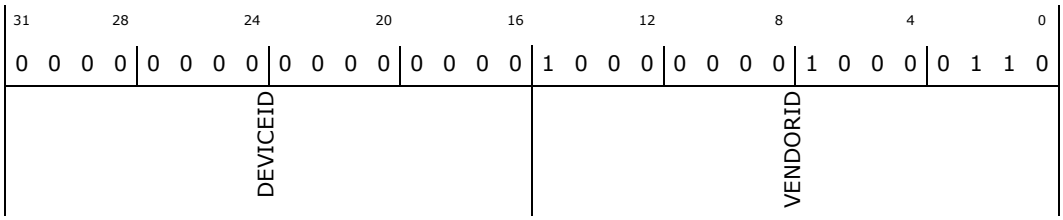
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**DEVICEID:** Device ID identifies the particular AHB/APB device. This is tied to a strap at the top level. Because of tool issues, the HTML files show this field as 0, but the following are the POR values for SoC: LPIO1 DMA: 0x2286 LPIO1 PWM1: 0x2288 LPIO1 PWM2: 0x2289 LPIO1 HSUART1: 0x228A LPIO1 HSUART2: 0x228C LPIO1 SPI1: 0x228E LPIO1 SPI2: 0x2290 LPIO1 SPI3: 0x22AC LPIO2 DMA: 0x22C0 LPIO2 I2C1: 0x22C1 LPIO2 I2C2: 0x22C2 LPIO2 I2C3: 0x22C3 LPIO2 I2C4: 0x22C4 LPIO2 I2C5: 0x22C5 LPIO2 I2C6: 0x22C6 LPIO2 I2C7: 0x22C7 For the final word on this, please see Ray Ng's SoC RevID and DevID HAS on Infofactory: https://ifcollaborate.intel.com/IFC/getdoc.aspx?docbase=InfoFactoryKBandchronid=09005ffd80e84b43andver=CURRENTandqepop=false
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap the top level.

9.5.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

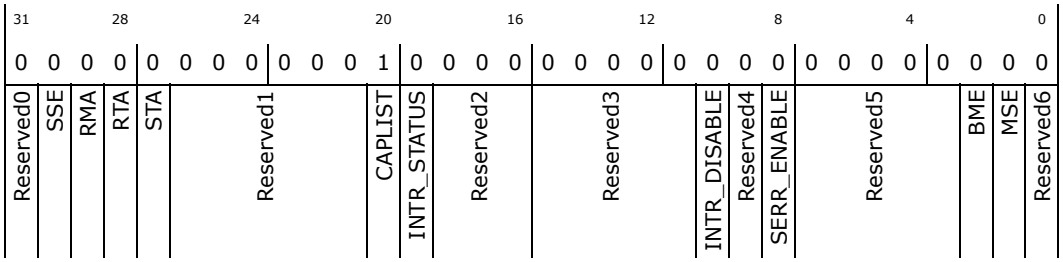
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved0:** Reserved
30	0x0 RW/1C	**SSE:** This bit is set when a device sends an DO_SERR message, and the SERR# Enable bit in the Command register is 1
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric PortReceived Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27	0x0 RW/1C	**STA:** The Bridge sets this bit whenever it responds to a transaction with CA abort. If the SERR# Enable bit is set, the Bridge sets the Signaled System Error bit and sends an DO_SERR message on the IOSF Sideband.
26:21	0x0 RO	**Reserved1:** Reserved
20	0x1 RO	**CAPLIST:** Capabilities List: Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt .i.e Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.. Reset value of this bit is 0.
9	0x0 RO	**Reserved4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: If both SERR# Enable and the Unsupported Request Reporting Enable (URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0x0 RO	**Reserved6:** Reserved

9.5.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

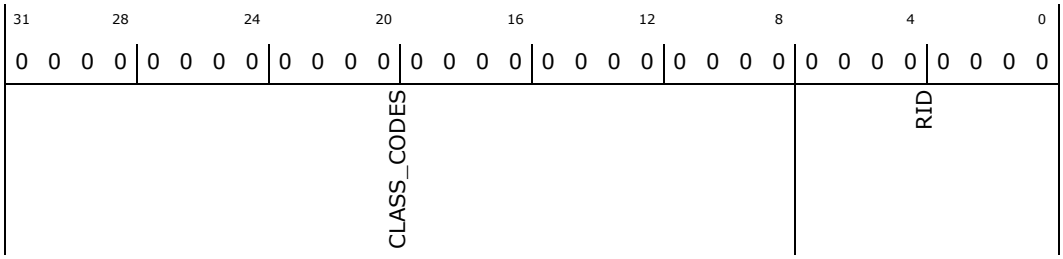
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

9.5.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

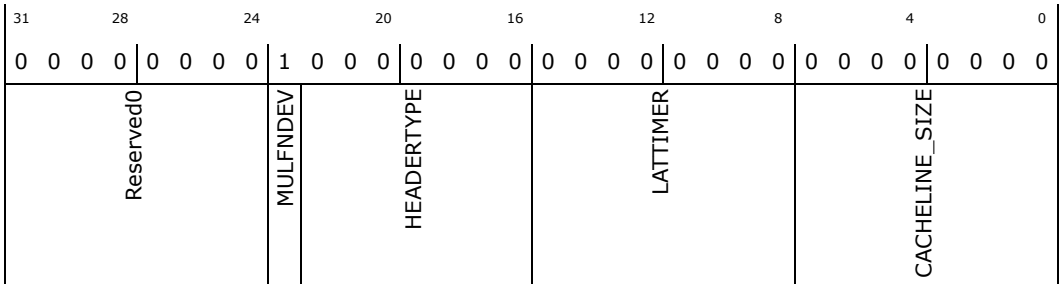
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + Ch

Default: 00800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x1 RO	**MULFNDEV:** Multi Function Device: This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. Value of 1 indicates multifunction device value of 0 indicates single function device
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	0x0 RO	**LATTIMER:** Latency Timer: Doesn.t apply to PCI Express. Hardwired to 00h.
7:0	0x0 RW	**CACHELINE_SIZE:** Cache Line Size: Doesn.t apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

9.5.5 BAR -Base Address Register (BAR)—Offset 10h

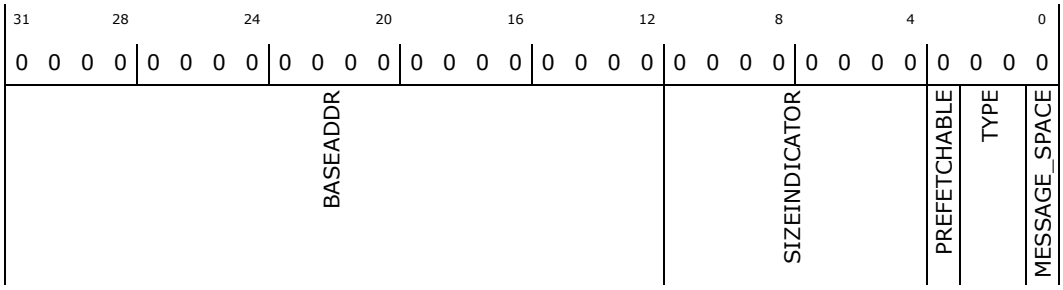
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the AHB device memory space. Taken from Strap values as 1's. Please note that for DMA this field goes from [31:14], or 16kbyte, and the SIZEINDICATOR field goes from [13:4].
11:4	0x0 RO	**SIZEINDICATOR:** Size Indicator Read Only: Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0x0 RO	**TYPE:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.5.6 BAR1 -Base Address Register1 (BAR1)—Offset 14h

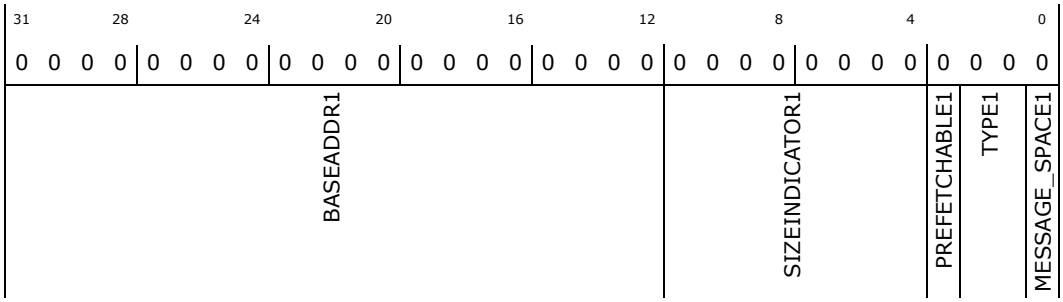
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	0x0 RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not
2:1	0x0 RO	**TYPE1:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.5.7 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

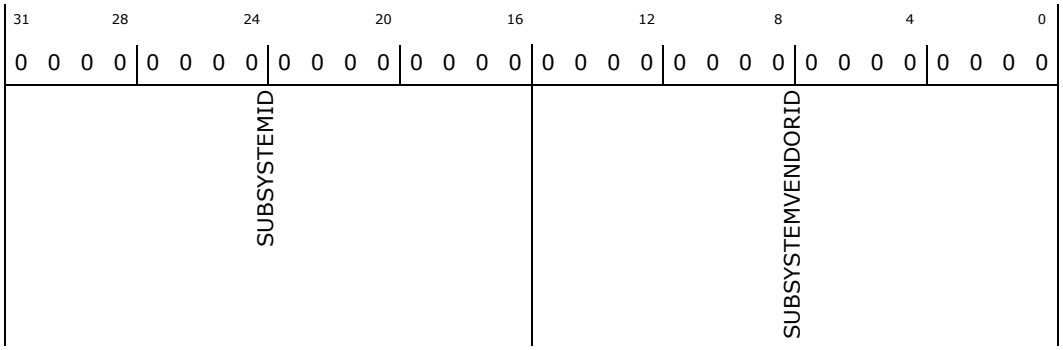
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

9.5.8 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

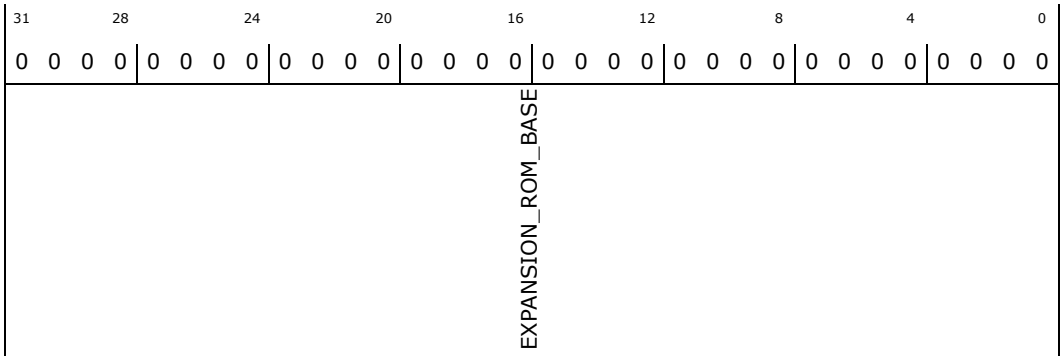
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** A value of all zeros indicates no support for expansion ROM.

9.5.9 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

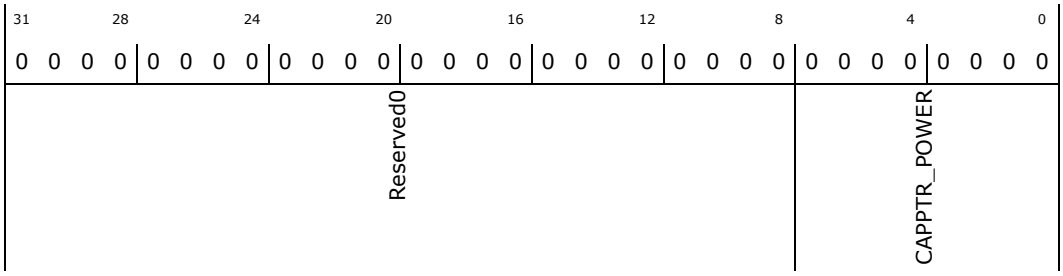
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x0 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

9.5.10 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

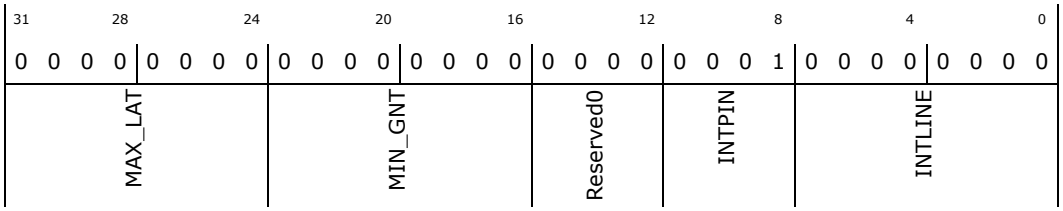
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

9.5.11 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

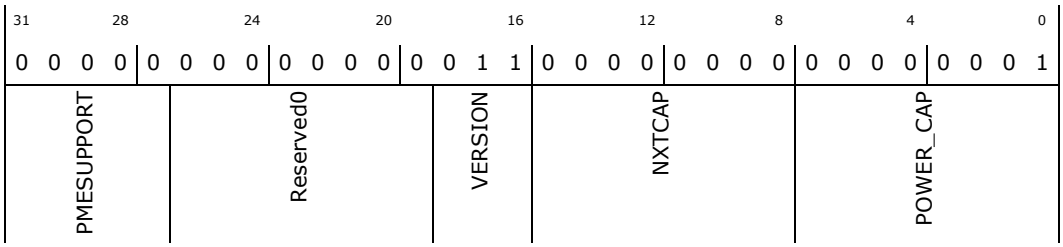
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** PME_Support - This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

9.5.12 PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

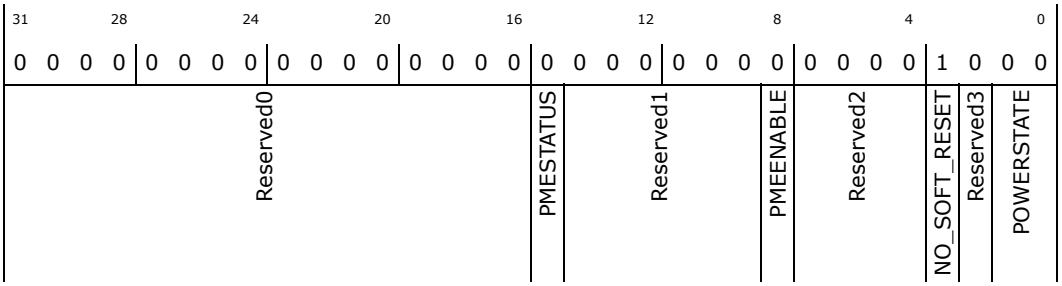
PMECTRLSTATUS - PME Control and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

9.5.13 Manufacturers ID (MANID)—Offset F8h

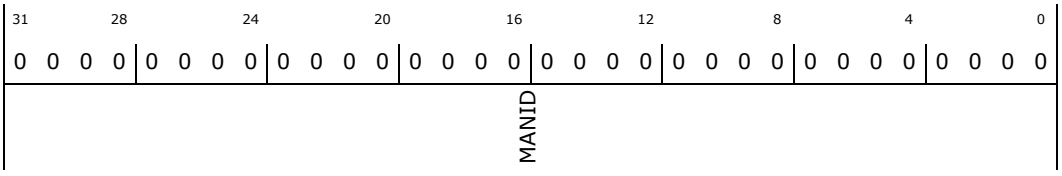
Manufacturers ID

Access Method

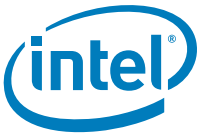
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:5] + F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: This register is brought out as straps to the top level.



9.6 SIO SPI Memory Mapped I/O Registers

Table 69. Summary of SIO SPI Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"SSP Cntrol Register 0 (SSCR0)—Offset 0h" on page 4207	00000000h
4–7h	4	"SSP Control Register 1 (SSCR1)—Offset 4h" on page 4208	00000000h
8–Bh	4	"SSP Status Register (SSSR)—Offset 8h" on page 4210	0000F004h
C–Fh	4	"SSP Interrupt Test Register (SSITR)—Offset Ch" on page 4211	00000000h
10–13h	4	"SSP Data (SSDR)—Offset 10h" on page 4212	00000000h
28–2Bh	4	"SSP Time Out (SSTO)—Offset 28h" on page 4213	00000000h
2C–2Fh	4	"SSP Programmable Serial Protocol (SSPSP)—Offset 2Ch" on page 4213	00000000h
30–33h	4	"SSP TX Time Slot Active (SSTSA)—Offset 30h" on page 4215	00000000h
34–37h	4	"SSP RX Time Slot Active (SSRSA)—Offset 34h" on page 4215	00000000h
38–3Bh	4	"SSP Time Slot Status (SSTSS)—Offset 38h" on page 4216	00000000h
3C–3Fh	4	"SSP Audio Clock Divider (SSACD)—Offset 3Ch" on page 4216	00000000h
40–43h	4	"I2S Transmit FIFO (ITF)—Offset 40h" on page 4217	00000000h
44–47h	4	"SPI Transmit FIFO (SITF)—Offset 44h" on page 4218	00000000h
48–4Bh	4	"SPI Receive FIFO (SIRF)—Offset 48h" on page 4218	00000000h
400–403h	4	"private clock params (PRV_CLOCK_PARAMS)—Offset 400h" on page 4219	00000000h
404–407h	4	"software reset (RESETS)—Offset 404h" on page 4220	00000000h
408–40Bh	4	"General purpose register (GENERAL)—Offset 408h" on page 4220	00000050h
40C–40Fh	4	"SPI misc register (SSP_REG)—Offset 40Ch" on page 4221	00000000h
418–41Bh	4	"SPI chip select control register (SPI_CS_CTRL)—Offset 418h" on page 4222	00000000h

9.6.1 SSP Cntrol Register 0 (SSCR0)—Offset 0h

The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

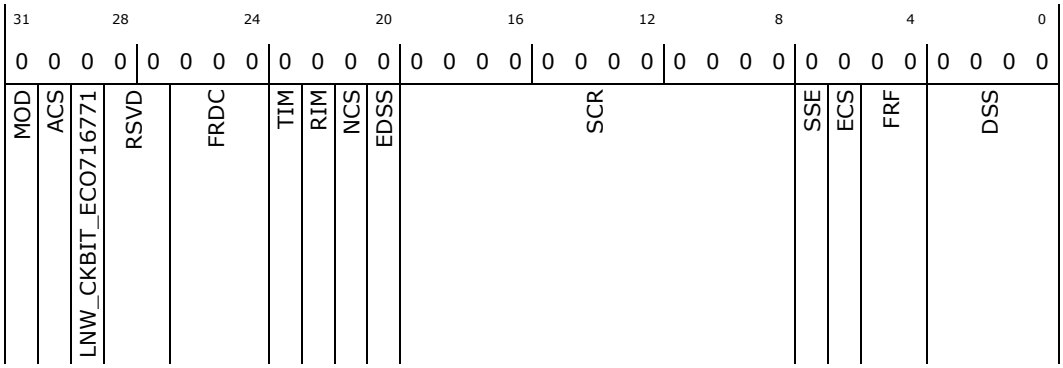
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**MOD:** Mode 0 - Normal SSP Mode 1 - Network Mode
30	0x0 RW	**ACS:** Audio Clock Select 0 - Clock selection is determined by the NCS and ECS bits 1 - Audio Clock (and Audio Clock Divider) are used to create the SSP's serial clock (SSPSCLK)
29	0x0 RW	**LNW_CKBIT_ECO716771:** in the TRM document for the customer.
28:27	0x0 RO	**RSVD:** Reserved
26:24	0x0 RW	**FRDC:** Frame Rate Divider Control Value 0-7 indicates the number of time slots per frame when in network mode (the actual number of time slots is FRDC+1, so 1 to 8 time slots).
23	0x0 RW	**TIM:** Transmit FIFO Under Run Interrupt Mask 0 - TUR events will generate an SSP interrupt 1 - TUR events will not generate an SSP interrupt
22	0x0 RW	**RIM:** Receive FIFO Over Run Interrupt Mask 0 - ROR events will generate an SSP interrupt 1 - ROR events will not generate an SSP interrupt
21	0x0 RW	**NCS:** Network Clock Select 0 - Clock selection is determined by ECS bit 1 - Network clock is used to create the SSP's serial clock (SSPSCLK)
20	0x0 RW	**EDSS:** Extended Data Size Select 0 - A zero is preappended to the DSS value which sets the DSS range from 4-16 bits 1 - A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits

Bit Range	Default & Access	Field Name (ID): Description
19:8	0x0 RW	**SCR:** Serial Clock Rate Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0x0 RW	**SSE:** Synchronous Serial Port Enable 0 - SSP operation disabled 1 - SSP operation enabled
6	0x0 RW	**ECS:** External Clock Select 0 - On-chip clock used to produce the SSP's serial clock (SSPSCLK) 1 - SSPEXTCLK/GPIO pin is used to create the SSP's SSPCLK
5:4	0x0 RW	**FRF:** Frame Format 00 - Motorola Serial Peripheral Interface (SPI) 01 - Texas Instruments Synchronous Serial Protocol (SSP) 10 - National Semiconductor Microwire 11 - Programmable Serial Protocol (PSP)
3:0	0x0 RW	**DSS:** Data Size Select With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

9.6.2 SSP Control Register 1 (SSCR1)—Offset 4h

The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

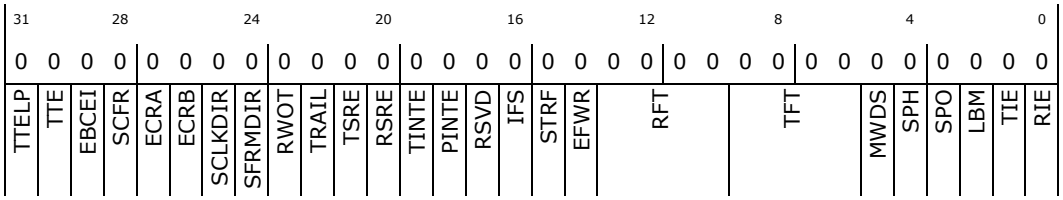
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

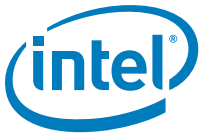
Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**TTELP:** TXD Tristate Enable on Last Phase 0 - TXD line will be tristated on same clock edge as TXD is to be flopped 1 - TXD line will be tristated clock edge after TXD is to be flopped
30	0x0 RW	**TTE:** TXD Tristate Enable 0 - TXD line will not be tristated 1 - TXD line will be tristated when no transmitting data
29	0x0 RW	**EBCEI:** Enable Bit Count Error Interrupt 0 - Interrupt due to a bit count error is disabled 1 - Interrupt due to a bit count error is enabled
28	0x0 RW	**SCFR:** Slave Clock Free Running 0 - clock input to SSPSCLK is continuously running 1 - clock input to SSPSCLK is only active durring transfers



Bit Range	Default & Access	Field Name (ID): Description
27	0x0 RW	**ECRA:** Enable Clock Request A 0 - clock request from other SSP is disabled 1 - clock request from other SSP is enabled
26	0x0 RW	**ECRB:** Enable Clock Request B 0 - clock request from other SSP is disabled 1 - clock request from other SSP is enabled
25	0x0 RW	**SCLKDIR:** SSP Serial Bit Rate Clock (SSPSCLK) Direction 0 - Master mode, SSP drives SSPSCLK 1 - Slave mode, SSP recieves SSPSCLK
24	0x0 RW	**SFRMDIR:** SSP Frame (SSPSFRM) Direction 0 - Master mode, SSP drives SSPSFRM 1 - Slave mode, SSP receives SSPSFRM
23	0x0 RW	**RWOT:** Receive With Out Transmit 0 - Transmit/Receive mode 1 - Receive without transmit mode
22	0x0 RW	**TRAIL:** Trailing Byte 0 - Processor based, trailing bytes are handled by processor 1 - DMA based, trailing bytes are handled by DMA
21	0x0 RW	**TSRE:** Transmit Service Request Enable 0 - DMA Service Request is disabled 1 - DMA Service Request is enabled
20	0x0 RW	**RSRE:** Receive Service Request Enable 0 - DMA Service Request is disabled 1 - DMA Service Request is enabled
19	0x0 RW	**TINTE:** Receiver Time-out Interrupt Enable 0 - Receiver Time-out interrupts are disabled 1 - Receiver Time-out interrupts are enabled
18	0x0 RW	**PINTE:** Peripheral Trailing Byte Interrupts Enable 0 - Peripheral Trailing Byte Interrupts are disabled 1 - Peripheral Trailing Byte Interrupts are enabled
17	0x0 RW	**RSVD:** Reserved
16	0x0 RW	**IFS:** Invert Frame Signal 0 - Frame polarity is determined by SSP format and PSP polarity bits 1 - Frame signal will be inverted from the normal SSP frame signal (as defined by the SSP format nad PSP polarity bits)
15	0x0 RW	**STRF:** Select FIFO for EFWR (test mode bit) (when EFWR=1) 0 - Transmit FIFO is selected for both writes and reads through the SSP Data Register (SSDR) 1 - Receive FIFO is selected for both writes and reads through the SSP Data Register (SSDR)
14	0x0 RW	**EFWR:** Enable FIFO Write/Read (test mode bit) 0 - FIFO write/read special function is disabled (normal SSP operational mode) 1 - FIFO write/read special function is enabled
13:10	0x0 RW	**RFT:** Receive FIFO Trigger Threshold Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.
9:6	0x0 RW	**TFT:** Transmit FIFO Trigger Threshold Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.
5	0x0 RW	**MWDS:** Microwire Transmit Data Size 0 - 8-bit command words are transmitted 1 - 16-bit command words are transmitted
4	0x0 RW	**SPH:** Motorola SPI SSPSCLK phase setting 0 - SSPSCLK is inactive one sycle at the start of a fram and cycle at the end of a frame 1 - SSPSCLK is inactive cycle at the start of a frame and one cycle at the end of a frame
3	0x0 RW	**SPO:** Motorola SPI SSPSCLK polarity setting 0 - The inactive or idle state of SSPSCLK is low 1 - The inactive or idle state of SSPSCLK is high

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**LBM:** Loop-Back Mode (test mode bit) 0 - Normal serial port operation enabled 1 - Output of transmit serial shifter connected to input of receive serial shifter, internally
1	0x0 RW	**TIE:** Transmit FIFO Interrupt Enable 0 - Transmit FIFO level interrupt is disabled 1 - Transmit FIFO level interrupt is enabled
0	0x0 RW	**RIE:** Receive FIFO Interrupt Enable 0 - Receive FIFO level interrupt is disabled 1 - Receive FIFO level interrupt is enabled

9.6.3 SSP Status Register (SSSR)—Offset 8h

The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

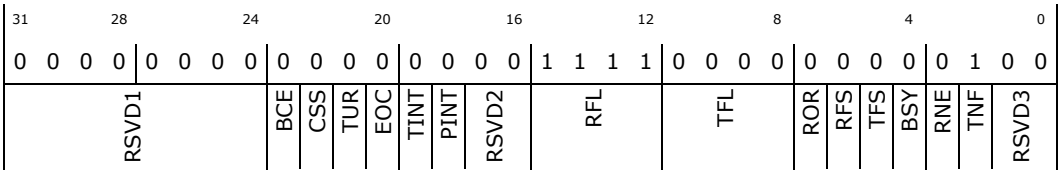
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 0000F004h



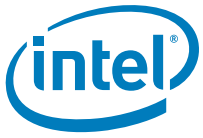
Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD1:** Reserved
23	0x0 RW/1C	**BCE:** Bit Count Error 0 - SSP has not experienced a bit count error 1 - SSPSFRM signal has been asserted when the bit counter was not 0
22	0x0 RO	**CSS:** Clock Synchronization Status 0 - SSP is ready for slave clock operations 1 - SSP is currently busy synchronizing slave mode signals
21	0x0 RW/1C	**TUR:** Transmit FIFO Under Run 0 - Transmit FIFO has not experienced an under run 1 - Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0x0 RW/1C	**EOC:** End of Chain 0 - DMA has not signaled an end of chain condition 1 - DMA has signaled an end of chain condition

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RW/1C	**TINT:** Receiver Time-out Interrupt 0 - No receiver time-out pending 1 - Receiver time-out pending
18	0x0 RW/1C	**PINT:** Peripheral Trailing Byte Interrupt 0 - No peripheral trailing byte interrupt pending 1 - Peripheral trailing byte interrupt pending
17:16	0x0 RO	**RSVD2:** Reserved
15:12	0xf RO	**RFL:** Receive FIFO Level Number of entries minus one in Receive FIFO. Note: When the value 0xF is read, the FIFO is either empty or full and the programmer should refer to the RNE bit
11:8	0x0 RO	**TFL:** Transmit FIFO Level Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the TNF bit.
7	0x0 RW/1C	**ROR:** Receive FIFO Overrun 0 - Receive FIFO has not experienced an overrun 1 - Attempted data write to full receive FIFO, request interrupt
6	0x0 RO	**RFS:** Receive FIFO Service Request 0 - Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 - Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0x0 RO	**TFS:** Transmit FIFO Service Request 0 - Transmit FIFO level exceeds the TFT threshold (TFT+1), or SSP disabled 1 - Transmit FIFO level is at or below TFT threshold (TFT+1), request interrupt
4	0x0 RO	**BSY:** SSP Busy 0 - SSP is idle or disabled 1 - SSP currently transmitting or receiving a frame
3	0x0 RO	**RNE:** Receive FIOF Not Empty 0 - Receive FIFO is empty 1 - Receive FIFO is not empty
2	0x1 RO	**TNF:** Transmit FIFO Not Full 0 - Transmit FIFO is full 1 - Transmit FIFO is not full
1:0	0x0 RO	**RSVD3:** Reserved

9.6.4 SSP Interrupt Test Register (SSITR)—Offset Ch

The read-write SSP Interrupt Test registers should be used only for testing purposes. Writing a 1 to the test transmit FIFO request SSITR.TTFS, bit 5, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Transmit FIFO. Writing a 1 to the test receive FIFO request SSITR.TRFS, bit 6, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Receive FIFO. Writing a 1 to the test receive FIFO overrun bit SSITR.TROR, bit 7, will generate a non-maskable Interrupt strobe signal to the Interrupt controller only, no DMA request will be made. Setting any of these bits will also cause the corresponding status bit(s) to be set in the Enhanced SSP Status register (SSSR). The Interrupt and/or service request, caused by the setting of one of these test bits, will remain active until the test bit is cleared by writing a 0 it. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

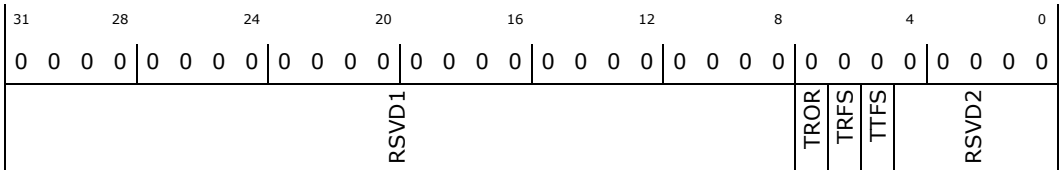


Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD1:** Reserved
7	0x0 RW	**TROR:** Test Receive FIFO overrun 0 - No receive FIFO overrun service request 1 - Generates non-maskable interrupt to CPU. No DMA request is generated
6	0x0 RW	**TRFS:** Test Receive FIFO service request 0 - No receive FIFO service request 1 - Generates non-maskable interrupt to CPU and a DMA request for receive FIFO
5	0x0 RW	**TTFS:** Test Transmit FIFO service request 0 - No transmit FIFO service request pending 1 - Generates non-maskable interrupt to CPU and a DMA request for transmit FIFO
4:0	0x0 RO	**RSVD2:** Reserved

9.6.5 SSP Data (SSDR)—Offset 10h

The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO, the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.TFL, SSSR.RFL, SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32-bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32-bits is automatically right-justified in the Receive FIFO. When the Enhanced SSP is programmed for National Semiconductor Microwire* frame format and if the size for Transmit data is 8-bits as selected by SSCR1.MWDS=0, then the most significant 24-bits are ignored. Similarly, if the size for the Transmit data is 16-bit as selected by SSCR1.MWDS=1, then most significant 16-bits are ignored. The SSCR0.DSS field controls the Receive data size.

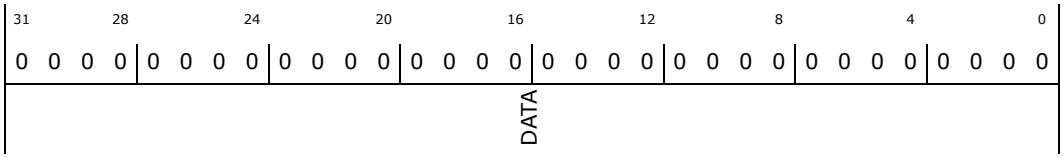
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**DATA:** Data word to be written to/read from transmit/receive FIFO

9.6.6 SSP Time Out (SSTO)—Offset 28h

The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

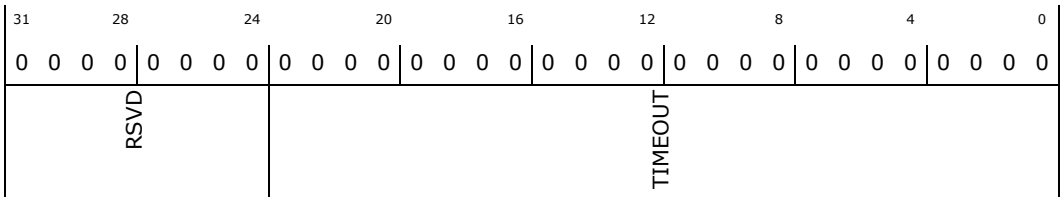
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD:** Reserved
23:0	0x0 RW	**TIMEOUT:** Timeout Value Is the value that defines the timeout interval, given by TIMEOUT/Peripheral Clock Frequency

9.6.7 SSP Programmable Serial Protocol (SSPSP)—Offset 2Ch

The Enhanced SSP Programmable Protocol registers are read-write registers that contain eight fields that are used to program the various programmable serial-protocol parameters. When using PSP format in Network mode, the parameters SFRMDLY,

STRTDLY, DMYSTP, DMYSTRT must be set to 0. Other parameters (such as FRMPOL, SCMODE, FSRT, SFRMDWDTH) are programmable. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

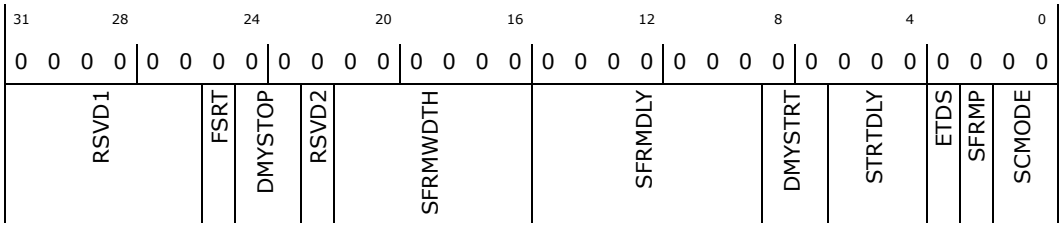
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD1:** Reserved
25	0x0 RW	**FSRT:** Frame Sync Relative Timing Bit 0 - Next frame is asserted after the end of the T4 timing 1 - Next frame is asserted with the LSB of the previous frame
24:23	0x0 RW	**DMYSTOP:** Dummy Stop Programmed value sets the number of SSPSCLK cycles that follow the transmitted data
22	0x0 RW	**RSVD2:** Reserved
21:16	0x0 RW	**SFRMWDTH:** Serial Frame Width Programmed value sets frame width (1-38)
15:9	0x0 RW	**SFRMDLY:** Serial Frame Delay Programmed value sets the number of half SSPSCLK cycles from TXD/RXD being driven to SSPSFRM being asserted (0-74)
8:7	0x0 RW	**DMYSTRT:** Dummy Start Programmed value sets the number of SSPSCLKs after STRTDLY is complete that precede the transmit/receive data
6:4	0x0 RW	**STRTDLY:** Start Delay Programmed value sets start delay that is used to set the idle time of SSPSCLK between transfers (0-7 SSPSCLK periods)
3	0x0 RW	**ETDS:** End of Transfer Data State 0 - Low 1 - Last value (bit 0)
2	0x0 RW	**SFRMP:** Serial Frame Polarity 0 - SSPSFRM is active low 1 - SSPSFRM is active high
1:0	0x0 RW	**SCMODE:** Serial bit-rate Clock Mode 00 - Data driven (falling), Data sampled (rising), Idle state (low) 01 - Data driven (rising), Data sampled (falling), Idle state (low) 10 - Data driven (rising), Data sampled (falling), Idle state (high) 11 - Data driven (falling), Data sampled (rising), Idle state (high)

9.6.8 SSP TX Time Slot Active (SSTSA)—Offset 30h

The Enhanced SSP TX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will transmit data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

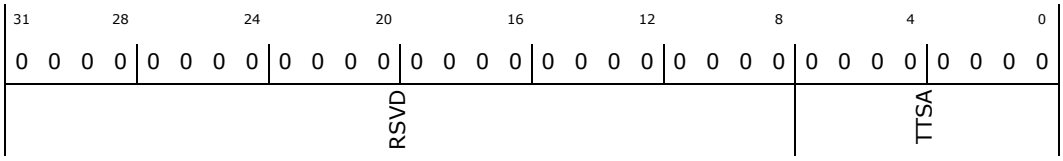
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RW	**TTSA:** TX Time Slot Active 0 - SSP will not transmit data in this time slot 1 - SSP will transmit data in this time slot

9.6.9 SSP RX Time Slot Active (SSRSA)—Offset 34h

The Enhanced SSP RX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will receive data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

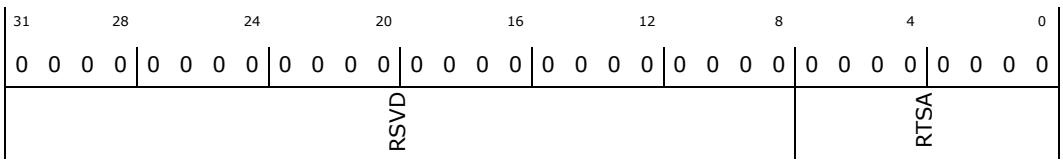
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RW	**RTSA:** RX Time Slot Active 0 - SSP will not receive data in this time slot 1 - SSP will receive data in this time slot

9.6.10 SSP Time Slot Status (SSTSS)—Offset 38h

The Enhanced SSP Time Slot Status registers are read only registers that indicate which Time Slot the Enhanced SSP is currently in when the Enhanced SSP is in Network Mode (SSCR0.MOD = 1). This register is not valid when the Enhanced SSP is not in Network Mode. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

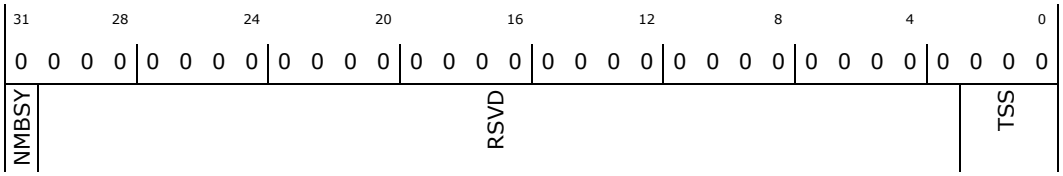
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**NMBSY:** Network Mode Busy 0 - No frame is currently active (in network mode only) 1 - SSP is in network mode and a frame is currently active
30:3	0x0 RO	**RSVD:** Reserved
2:0	0x0 RO	**TSS:** Time Slot Status Value indicates which time slot is currently active

9.6.11 SSP Audio Clock Divider (SSACD)—Offset 3Ch

The Enhanced SSP Audio Clock Divider registers are read-write registers that indicate which clock frequency is sent to the Enhanced SSP and to the SYSCLK pin. If SSCR0.SCR is not 0, then there is no guaranteed phase relationship between SYSCLK and SSPSCLK. The SSPSFRM Frame Synch Sampling Frequency is calculated by dividing the chosen PLL output clock frequency (SSACD.ACPS) by the chosen divider (SSACD.ACDS) which gives the SYSCLK frequency. The SYSCLK is then divided by 4 (or by 1) to get the SSPSCLK. The SSPSCLK is divided by the data size (EDSS, DSS values)

and by the number of time slots being used (SSCR0.FRDC value), if any, to give the SSPSFRM frequency. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

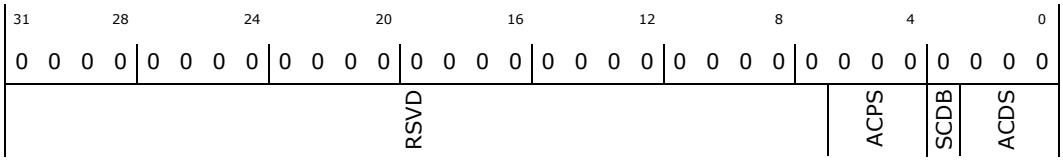
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**RSVD:** Reserved
6:4	0x0 RW	**ACPS:** Audio Clock PLL Select Value indicates which PLL output clock is sent to the clock divider in the clock unit 000: 5.622MHz, 001: 11.345MHz, 010: 12.235MHz, 011: 14.857MHz, 100: 32.842MHz, 101: 48.000MHz, 110, 111: Reserved
3	0x0 RW	**SCDB:** SYSCLK Divider Bypass 0 - SYSCLK is divided by 4 before being sent to SSP 1 - SYSCLK is not divided before being sent to SSP
2:0	0x0 RW	**ACDS:** Audio Clock Divider Select Value indicates which divider will be used by the clock unit to create the SYSCLK output pin. Clock divider value will be 2^ACDS, max ACDS = 5.

9.6.12 I2S Transmit FIFO (ITF)—Offset 40h

The I2S Transmit FIFO register is for writing the water mark for the I2S transmit FIFO and also for reading the number of entries in the I2S transmit FIFO

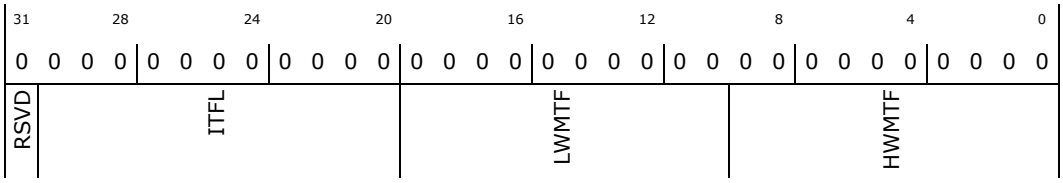
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RSVD:** Reserved
30:20	0x0 RO	**ITFL:** I2S Transmit FIFO Level Number of entries in I2S Transmit FIFO
19:10	0x0 RW	**LWMTF:** Low Water Mark Transmit FIFO.Set the low water mark of the I2S transmit FIFO.
9:0	0x0 RW	**HWMTF:** High Water Mark Transmit FIFO.Set the high water mark of the I2S transmit FIFO.

9.6.13 SPI Transmit FIFO (SITF)—Offset 44h

The SPI Transmit FIFO register is for writing the water mark for the SPI transmit FIFO and also for reading the number of entries in the SPI transmit FIFO

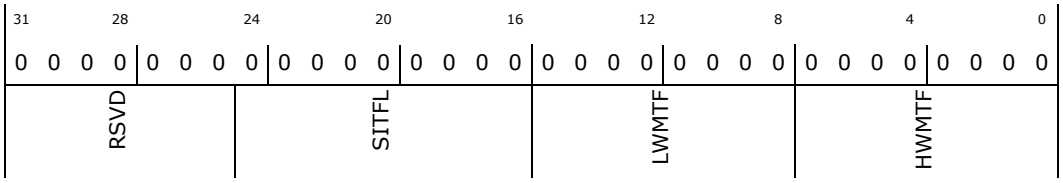
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD:** Reserved
24:16	0x0 RO	**SITFL:** SPI Transmit FIFO Level Number of entries in SPI Transmit FIFO.
15:8	0x0 RW	**LWMTF:** Low Water Mark Transmit FIFO. Set the low water mark of the SPI transmit FIFO.
7:0	0x0 RW	**HWMTF:** High Water Mark Transmit FIFO. Set the high water mark of the SPI transmit FIFO.

9.6.14 SPI Receive FIFO (SIRF)—Offset 48h

The SPI Receive FIFO register is for writing the water mark for the SPI receive FIFO and also for reading the number of entries in the SPI receive FIFO

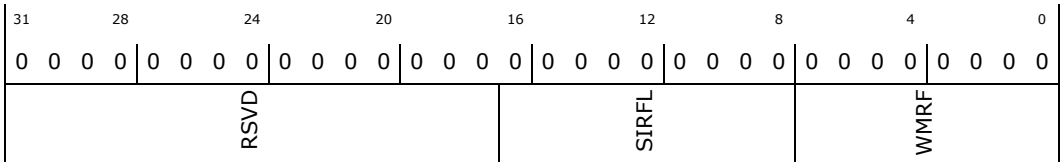
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RSVD:** Reserved
16:8	0x0 RO	**SIRFL:** SPI Receive FIFO Level Number of entries in SPI Receive FIFO.
7:0	0x0 RW	**WMRF:** Water Mark Receive FIFO. Set the water mark of the SPI receive FIFO.

9.6.15 private clock params (PRV_CLOCK_PARAMS)—Offset 400h

private clock params

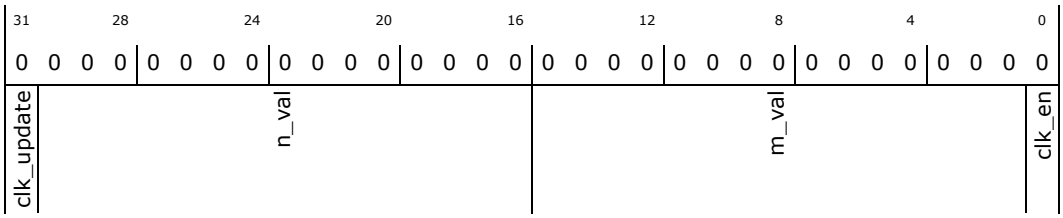
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 400h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**clk_update:** update the clock divider after seeting new m and n values
30:16	0x0 RW	**N_VAL (n_val):** n value for the m over n divider
15:1	0x0 RW	**M_VAL (m_val):** m value for the m over n divider
0	0x0 RW	**clk_en:** clk en of the m over n divider

9.6.16 software reset (RESETS)—Offset 404h

software reset

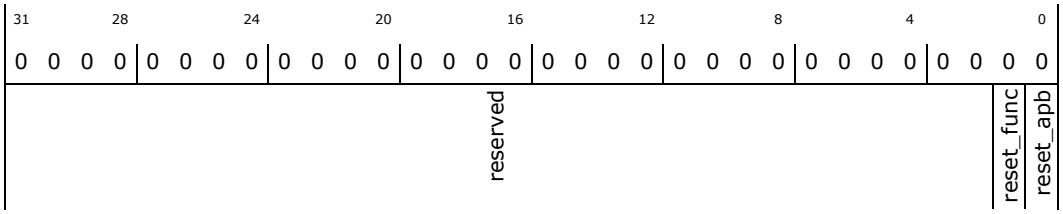
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 404h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (reserved):** Reserved
1	0x0 RW	**reset_func:** reset the func clock domain
0	0x0 RW	**reset_apb:** reset the apb domain

9.6.17 General purpose register (GENERAL)—Offset 408h

General purpose register

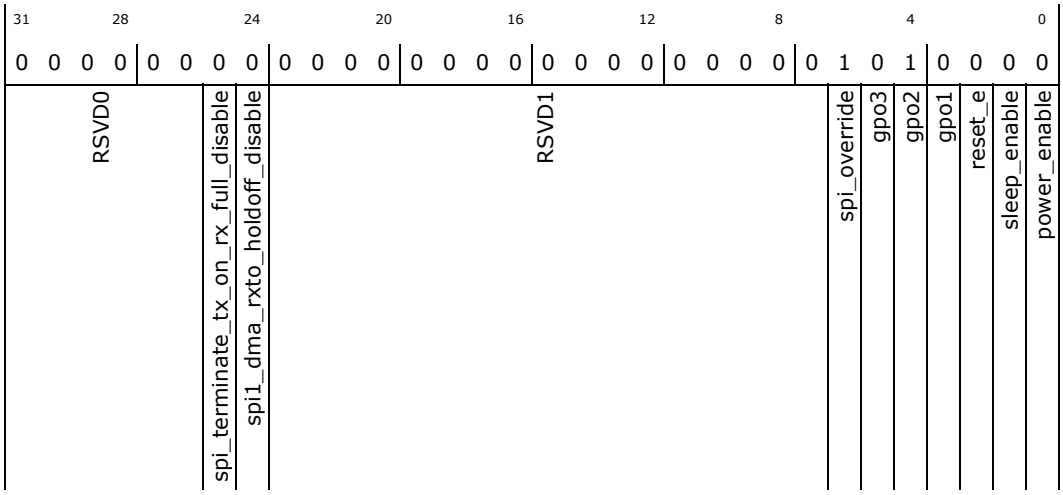
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 408h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000050h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD0:** Reserved
25	0x0 RW	**spi_terminate_tx_on_rx_full_disable:** disable terminate tx when rx full
24	0x0 RW	**spi1_dma_rxto_holdoff_disable:** disable dma hold off
23:7	0x0 RO	**RSVD1:** Reserved
6	0x1 RW	**spi_override:** not applicable
5	0x0 RW	**gpo3:** not applicable
4	0x1 RW	**gpo2:** not applicable
3	0x0 RW	**gpo1:** not applicable
2	0x0 RW	**reset_e:** not applicable
1	0x0 RW	**sleep_enable:** not applicable
0	0x0 RW	**power_enable:** not applicable

9.6.18 SPI misc register (SSP_REG)—Offset 40Ch

SPI misc register

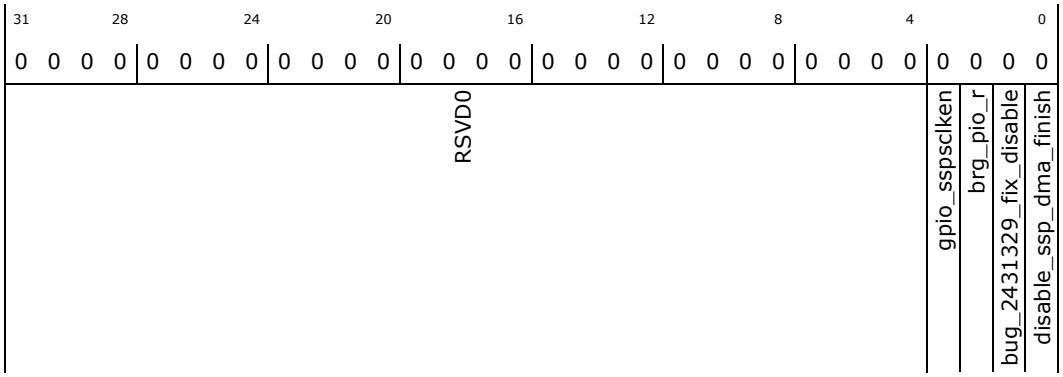
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RSVD0:** Reserved
3	0x0 RW	**gpio_sspsclken:** not applicable
2	0x0 RW	**brg_pio_r:** not applicable
1	0x0 RW	**bug_2431329_fix_disable:** not applicable
0	0x0 RW	**disable_ssp_dma_finish:** disable ssp dma finish

9.6.19 SPI chip select control register (SPI_CS_CTRL)—Offset 418h

SPI chip select control register

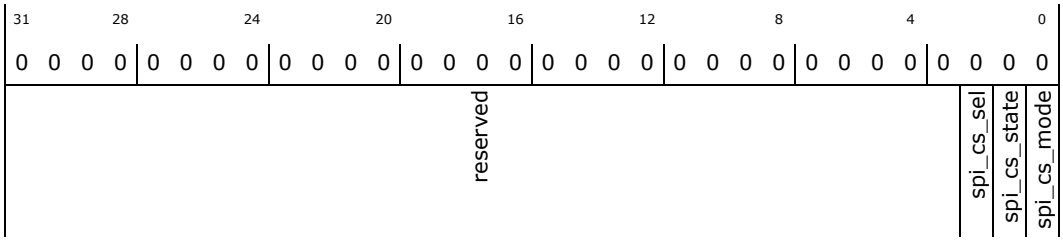
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 418h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RW	**reserved:** reserved
2	0x0 RW	**spi_cs_sel:** SW select bit to choose either CS0 or CS1 for spi
1	0x0 RW	**spi_cs_state:** SW override of CS line in SW mode for spi
0	0x0 RW	**spi_cs_mode:** selects HW mode or SW mode for chip select for spi

9.7 SIO SPI 1 PCI Configuration Registers

Table 70. Summary of SIO SPI 1 PCI Configuration Registers—0/30/6

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4225	00008086h
4–7h	4	"STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h" on page 4225	00100000h
8–Bh	4	"REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4227	00000000h
C–Fh	4	"CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4228	00800000h
10–13h	4	"BAR -Base Address Register (BAR)—Offset 10h" on page 4228	00000000h
14–17h	4	"BAR1 -Base Address Register1 (BAR1)—Offset 14h" on page 4229	00000000h
2C–2Fh	4	"SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4230	00000000h
30–33h	4	"EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4231	00000000h
34–37h	4	"CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4231	00000000h
3C–3Fh	4	"INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4232	00000100h
80–83h	4	"POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4232	00030001h
84–87h	4	"PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4233	00000008h
F8–FBh	4	"Manufacturers ID (MANID)—Offset F8h" on page 4234	00000000h

9.7.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

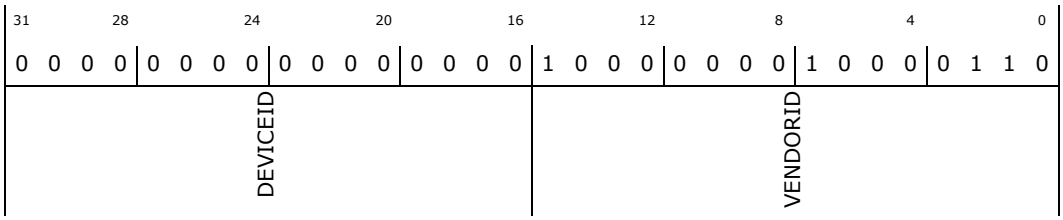
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:6] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**DEVICEID:** Device ID identifies the particular AHB/APB device. This is tied to a strap at the top level. Because of tool issues, the HTML files show this field as 0, but the following are the POR values for SoC: LPIO1 DMA: 0x2286 LPIO1 PWM1: 0x2288 LPIO1 PWM2: 0x2289 LPIO1 HSUART1: 0x228A LPIO1 HSUART2: 0x228C LPIO1 SPI1: 0x228E LPIO1 SPI2: 0x2290 LPIO1 SPI3: 0x22AC LPIO2 DMA: 0x22C0 LPIO2 I2C1: 0x22C1 LPIO2 I2C2: 0x22C2 LPIO2 I2C3: 0x22C3 LPIO2 I2C4: 0x22C4 LPIO2 I2C5: 0x22C5 LPIO2 I2C6: 0x22C6 LPIO2 I2C7: 0x22C7 For the final word on this, please see Ray Ng's SoC RevID and DevID HAS on Infofactory: https://ifcollaborate.intel.com/IFC/getdoc.aspx?docbase=InfoFactoryKBandchronid=09005ffd80e84b43andver=CURRENTandqepop=false
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap the top level.

9.7.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

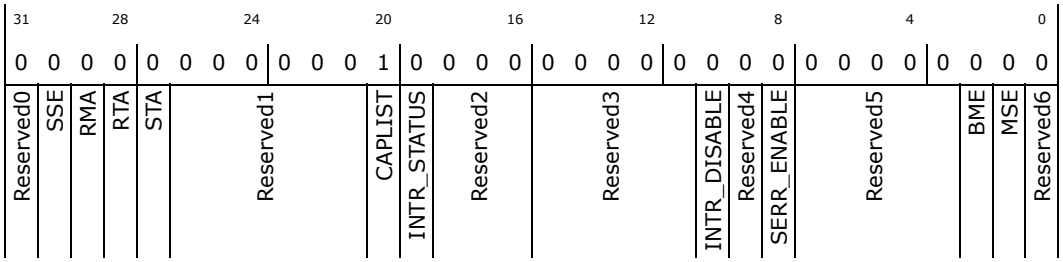
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:6] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved0:** Reserved
30	0x0 RW/1C	**SSE:** This bit is set when a device sends an DO_SERR message, and the SERR# Enable bit in the Command register is 1
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric PortReceived Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27	0x0 RW/1C	**STA:** The Bridge sets this bit whenever it responds to a transaction with CA abort. If the SERR# Enable bit is set, the Bridge sets the Signaled System Error bit and sends an DO_SERR message on the IOSF Sideband.
26:21	0x0 RO	**Reserved1:** Reserved
20	0x1 RO	**CAPLIST:** Capabilities List: Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt .i.e Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.. Reset value of this bit is 0.
9	0x0 RO	**Reserved4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: If both SERR# Enable and the Unsupported Request Reporting Enable (URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0x0 RO	**Reserved6:** Reserved

9.7.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

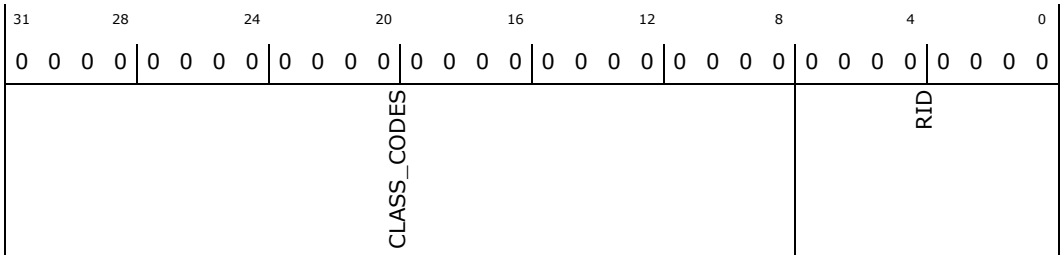
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:6] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

9.7.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

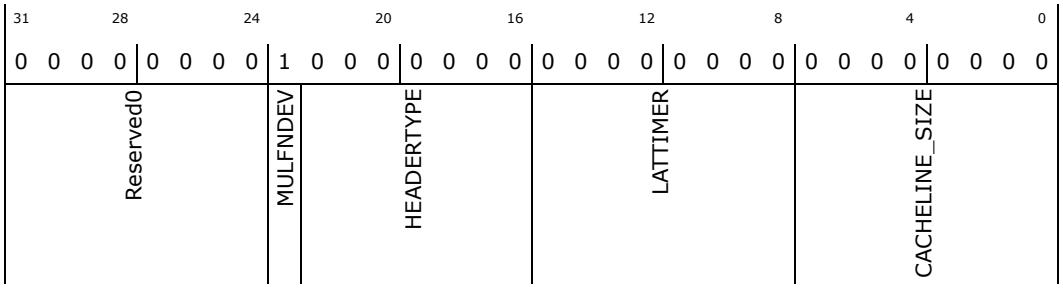
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:6] + Ch

Default: 00800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x1 RO	**MULFNDEV:** Multi Function Device: This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. Value of 1 indicates multifunction device value of 0 indicates single function device
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	0x0 RO	**LATTIMER:** Latency Timer: Doesn.t apply to PCI Express. Hardwired to 00h.
7:0	0x0 RW	**CACHELINE_SIZE:** Cache Line Size: Doesn.t apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

9.7.5 BAR -Base Address Register (BAR)—Offset 10h

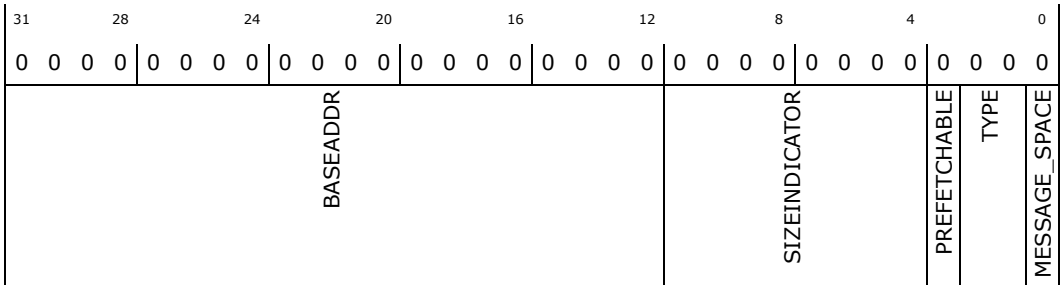
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the AHB device memory space. Taken from Strap values as 1's. Please note that for DMA this field goes from [31:14], or 16kbyte, and the SIZEINDICATOR field goes from [13:4].
11:4	0x0 RO	**SIZEINDICATOR:** Size Indicator Read Only: Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0x0 RO	**TYPE:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.7.6 BAR1 -Base Address Register1 (BAR1)—Offset 14h

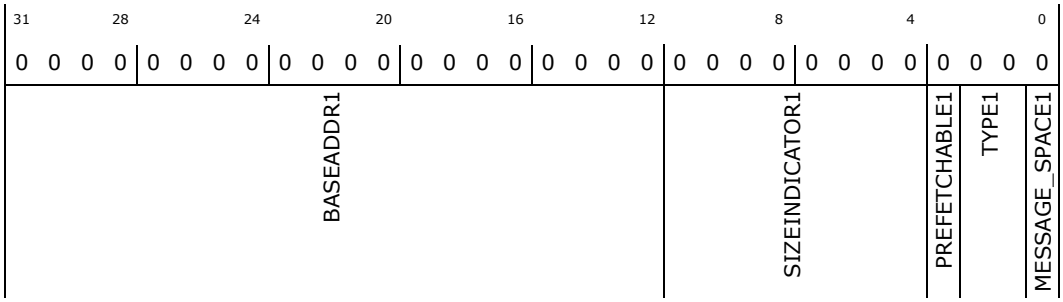
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:6] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	0x0 RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not
2:1	0x0 RO	**TYPE1:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.7.7 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

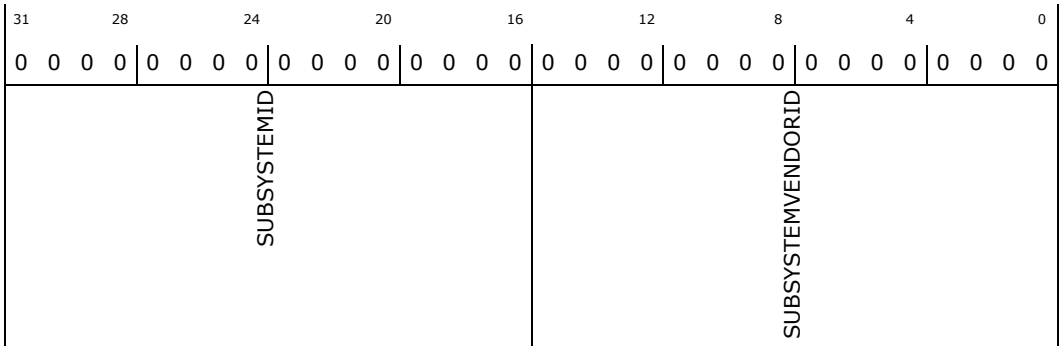
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:6] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

9.7.8 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

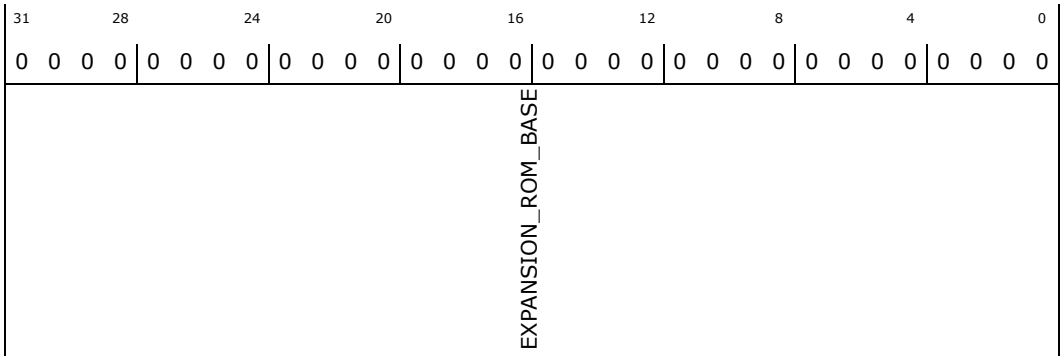
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:6] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** A value of all zeros indicates no support for expansion ROM.

9.7.9 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

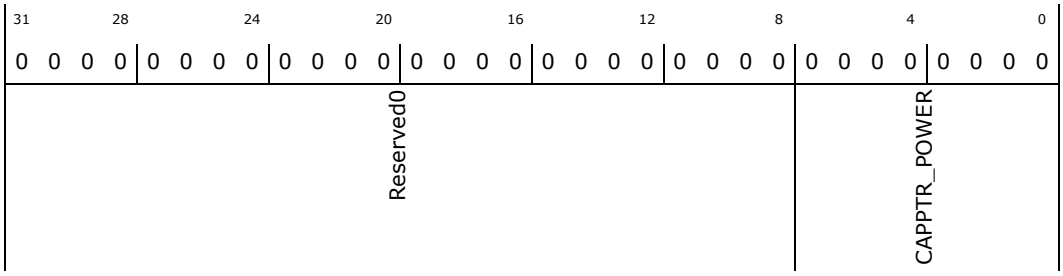
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:6] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x0 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

9.7.10 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

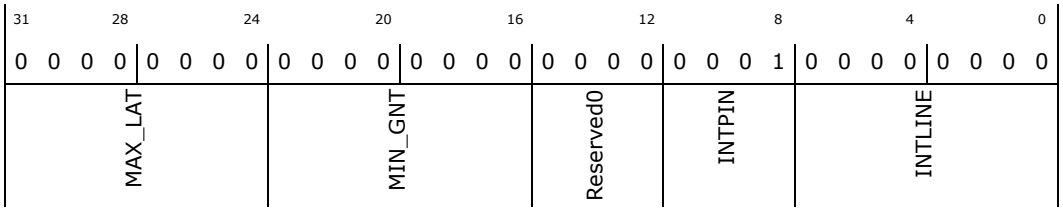
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:6] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

9.7.11 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

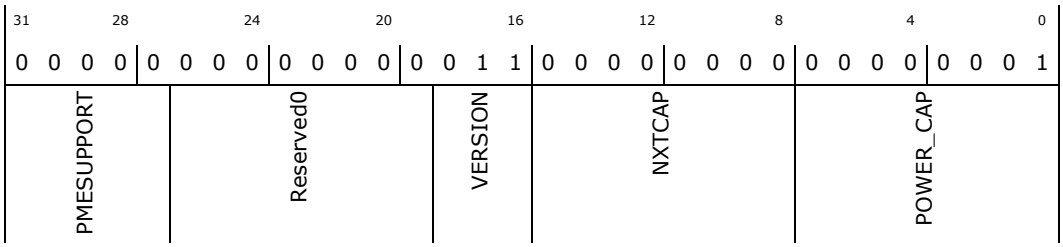
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:6] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** PME_Support - This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

9.7.12 PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

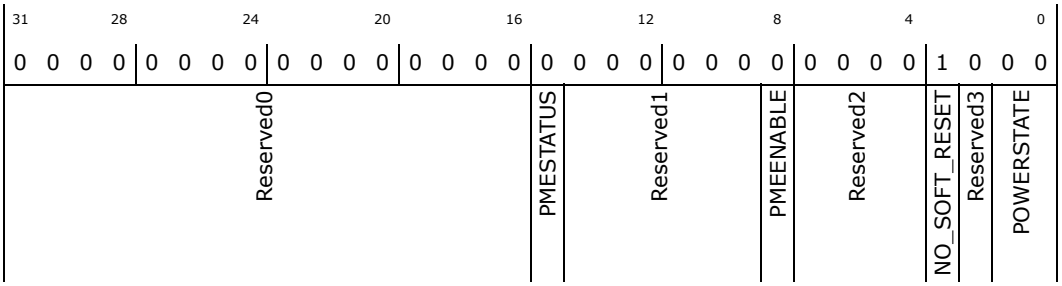
PMECTRLSTATUS - PME Control and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:6] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

9.7.13 Manufacturers ID (MANID)—Offset F8h

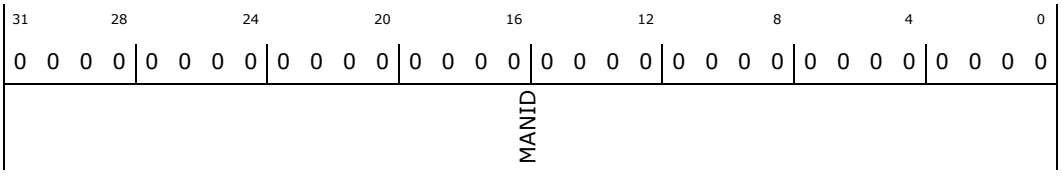
Manufacturers ID

Access Method

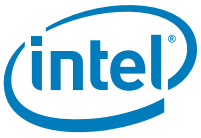
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:6] + F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: This register is brought out as straps to the top level.



9.8 SIO SPI 1 Memory Mapped I/O Registers

Table 71. Summary of SIO SPI 1 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"SSP Cntrol Register 0 (SSCR0)—Offset 0h" on page 4237	00000000h
4–7h	4	"SSP Control Register 1 (SSCR1)—Offset 4h" on page 4238	00000000h
8–Bh	4	"SSP Status Register (SSSR)—Offset 8h" on page 4240	0000F004h
C–Fh	4	"SSP Interrupt Test Register (SSITR)—Offset Ch" on page 4241	00000000h
10–13h	4	"SSP Data (SSDR)—Offset 10h" on page 4242	00000000h
28–2Bh	4	"SSP Time Out (SSTO)—Offset 28h" on page 4243	00000000h
2C–2Fh	4	"SSP Programmable Serial Protocol (SSPSP)—Offset 2Ch" on page 4243	00000000h
30–33h	4	"SSP TX Time Slot Active (SSTSA)—Offset 30h" on page 4245	00000000h
34–37h	4	"SSP RX Time Slot Active (SSRSA)—Offset 34h" on page 4245	00000000h
38–3Bh	4	"SSP Time Slot Status (SSTSS)—Offset 38h" on page 4246	00000000h
3C–3Fh	4	"SSP Audio Clock Divider (SSACD)—Offset 3Ch" on page 4246	00000000h
40–43h	4	"I2S Transmit FIFO (ITF)—Offset 40h" on page 4247	00000000h
44–47h	4	"SPI Transmit FIFO (SITF)—Offset 44h" on page 4248	00000000h
48–4Bh	4	"SPI Receive FIFO (SIRF)—Offset 48h" on page 4248	00000000h
400–403h	4	"private clock params (PRV_CLOCK_PARAMS)—Offset 400h" on page 4249	00000000h
404–407h	4	"software reset (RESETS)—Offset 404h" on page 4250	00000000h
408–40Bh	4	"General purpose register (GENERAL)—Offset 408h" on page 4250	00000050h
40C–40Fh	4	"SPI misc register (SSP_REG)—Offset 40Ch" on page 4251	00000000h
418–41Bh	4	"SPI chip select control register (SPI_CS_CTRL)—Offset 418h" on page 4252	00000000h

9.8.1 SSP Cntrol Register 0 (SSCR0)—Offset 0h

The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

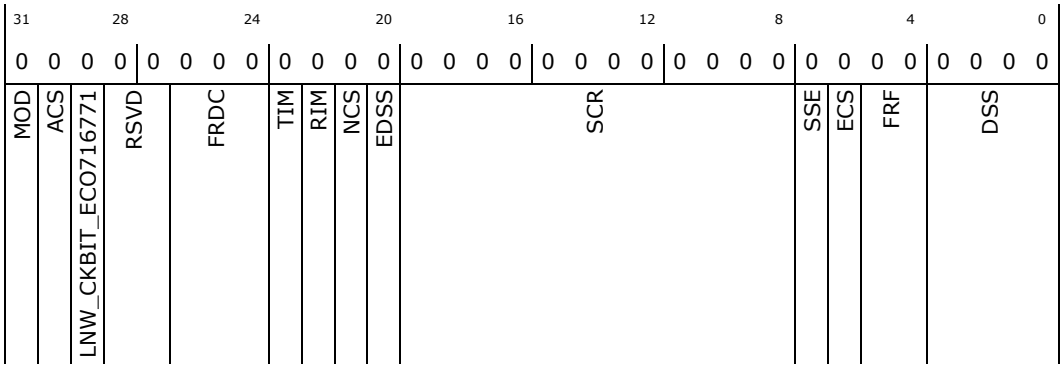
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**MOD:** Mode 0 - Normal SSP Mode 1 - Network Mode
30	0x0 RW	**ACS:** Audio Clock Select 0 - Clock selection is determined by the NCS and ECS bits 1 - Audio Clock (and Audio Clock Divider) are used to create the SSP's serial clock (SSPSCLK)
29	0x0 RW	**LNW_CKBIT_ECO716771:** in the TRM document for the customer.
28:27	0x0 RO	**RSVD:** Reserved
26:24	0x0 RW	**FRDC:** Frame Rate Divider Control Value 0-7 indicates the number of time slots per frame when in network mode (the actual number of time slots is FRDC+1, so 1 to 8 time slots).
23	0x0 RW	**TIM:** Transmit FIFO Under Run Interrupt Mask 0 - TUR events will generate an SSP interrupt 1 - TUR events will not generate an SSP interrupt
22	0x0 RW	**RIM:** Receive FIFO Over Run Interrupt Mask 0 - ROR events will generate an SSP interrupt 1 - ROR events will not generate an SSP interrupt
21	0x0 RW	**NCS:** Network Clock Select 0 - Clock selection is determined by ECS bit 1 - Network clock is used to create the SSP's serial clock (SSPSCLK)
20	0x0 RW	**EDSS:** Extended Data Size Select 0 - A zero is preappended to the DSS value which sets the DSS range from 4-16 bits 1 - A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits

Bit Range	Default & Access	Field Name (ID): Description
19:8	0x0 RW	**SCR:** Serial Clock Rate Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0x0 RW	**SSE:** Synchronous Serial Port Enable 0 - SSP operation disabled 1 - SSP operation enabled
6	0x0 RW	**ECS:** External Clock Select 0 - On-chip clock used to produce the SSP's serial clock (SSPSCLK) 1 - SSPEXTCLK/GPIO pin is used to create the SSP's SSPCLK
5:4	0x0 RW	**FRF:** Frame Format 00 - Motorola Serial Peripheral Interface (SPI) 01 - Texas Instruments Synchronous Serial Protocol (SSP) 10 - National Semiconductor Microwire 11 - Programmable Serial Protocol (PSP)
3:0	0x0 RW	**DSS:** Data Size Select With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

9.8.2 SSP Control Register 1 (SSCR1)—Offset 4h

The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

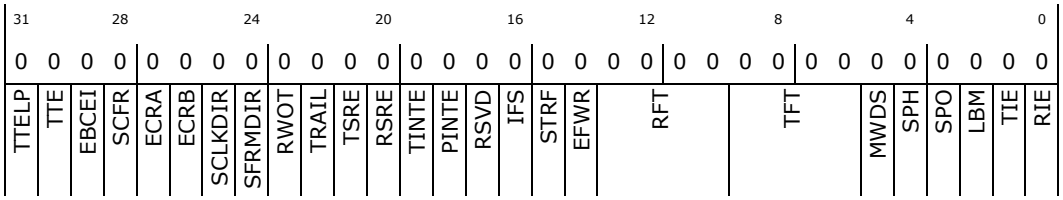
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

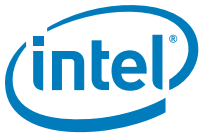
Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**TTELP:** TXD Tristate Enable on Last Phase 0 - TXD line will be tristated on same clock edge as TXD is to be flopped 1 - TXD line will be tristated clock edge after TXD is to be flopped
30	0x0 RW	**TTE:** TXD Tristate Enable 0 - TXD line will not be tristated 1 - TXD line will be tristated when no transmitting data
29	0x0 RW	**EBCEI:** Enable Bit Count Error Interrupt 0 - Interrupt due to a bit count error is disabled 1 - Interrupt due to a bit count error is enabled
28	0x0 RW	**SCFR:** Slave Clock Free Running 0 - clock input to SSPSCLK is continuously running 1 - clock input to SSPSCLK is only active durring transfers



Bit Range	Default & Access	Field Name (ID): Description
27	0x0 RW	**ECRA:** Enable Clock Request A 0 - clock request from other SSP is disabled 1 - clock request from other SSP is enabled
26	0x0 RW	**ECRB:** Enable Clock Request B 0 - clock request from other SSP is disabled 1 - clock request from other SSP is enabled
25	0x0 RW	**SCLKDIR:** SSP Serial Bit Rate Clock (SSPSCLK) Direction 0 - Master mode, SSP drives SSPSCLK 1 - Slave mode, SSP recieves SSPSCLK
24	0x0 RW	**SFRMDIR:** SSP Frame (SSPSFRM) Direction 0 - Master mode, SSP drives SSPSFRM 1 - Slave mode, SSP receives SSPSFRM
23	0x0 RW	**RWOT:** Receive With Out Transmit 0 - Transmit/Receive mode 1 - Receive without transmit mode
22	0x0 RW	**TRAIL:** Trailing Byte 0 - Processor based, trailing bytes are handled by processor 1 - DMA based, trailing bytes are handled by DMA
21	0x0 RW	**TSRE:** Transmit Service Request Enable 0 - DMA Service Request is disabled 1 - DMA Service Request is enabled
20	0x0 RW	**RSRE:** Receive Service Request Enable 0 - DMA Service Request is disabled 1 - DMA Service Request is enabled
19	0x0 RW	**TINTE:** Receiver Time-out Interrupt Enable 0 - Receiver Time-out interrupts are disabled 1 - Receiver Time-out interrupts are enabled
18	0x0 RW	**PINTE:** Peripheral Trailing Byte Interrupts Enable 0 - Peripheral Trailing Byte Interrupts are disabled 1 - Peripheral Trailing Byte Interrupts are enabled
17	0x0 RW	**RSVD:** Reserved
16	0x0 RW	**IFS:** Invert Frame Signal 0 - Frame polarity is determined by SSP format and PSP polarity bits 1 - Frame signal will be inverted from the normal SSP frame signal (as defined by the SSP format nad PSP polarity bits)
15	0x0 RW	**STRF:** Select FIFO for EFWR (test mode bit) (when EFWR=1) 0 - Transmit FIFO is selected for both writes and reads through the SSP Data Register (SSDR) 1 - Receive FIFO is selected for both writes and reads through the SSP Data Register (SSDR)
14	0x0 RW	**EFWR:** Enable FIFO Write/Read (test mode bit) 0 - FIFO write/read special function is disabled (normal SSP operational mode) 1 - FIFO write/read special function is enabled
13:10	0x0 RW	**RFT:** Receive FIFO Trigger Threshold Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.
9:6	0x0 RW	**TFT:** Transmit FIFO Trigger Threshold Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.
5	0x0 RW	**MWDS:** Microwire Transmit Data Size 0 - 8-bit command words are transmitted 1 - 16-bit command words are transmitted
4	0x0 RW	**SPH:** Motorola SPI SSPSCLK phase setting 0 - SSPSCLK is inactive one sycle at the start of a fram and cycle at the end of a frame 1 - SSPSCLK is inactive cycle at the start of a frame and one cycle at the end of a frame
3	0x0 RW	**SPO:** Motorola SPI SSPSCLK polarity setting 0 - The inactive or idle state of SSPSCLK is low 1 - The inactive or idle state of SSPSCLK is high

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**LBM:** Loop-Back Mode (test mode bit) 0 - Normal serial port operation enabled 1 - Output of transmit serial shifter connected to input of receive serial shifter, internally
1	0x0 RW	**TIE:** Transmit FIFO Interrupt Enable 0 - Transmit FIFO level interrupt is disabled 1 - Transmit FIFO level interrupt is enabled
0	0x0 RW	**RIE:** Receive FIFO Interrupt Enable 0 - Receive FIFO level interrupt is disabled 1 - Receive FIFO level interrupt is enabled

9.8.3 SSP Status Register (SSSR)—Offset 8h

The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

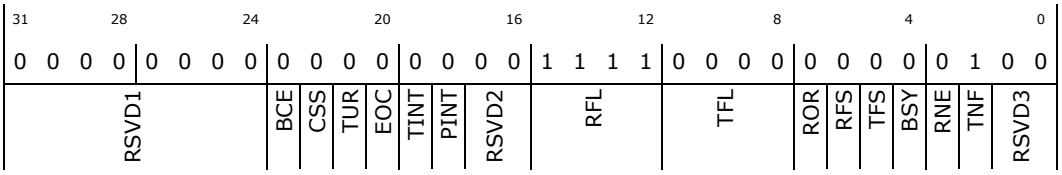
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 0000F004h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD1:** Reserved
23	0x0 RW/1C	**BCE:** Bit Count Error 0 - SSP has not experienced a bit count error 1 - SSPSFRM signal has been asserted when the bit counter was not 0
22	0x0 RO	**CSS:** Clock Synchronization Status 0 - SSP is ready for slave clock operations 1 - SSP is currently busy synchronizing slave mode signals
21	0x0 RW/1C	**TUR:** Transmit FIFO Under Run 0 - Transmit FIFO has not experienced an under run 1 - Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0x0 RW/1C	**EOC:** End of Chain 0 - DMA has not signaled an end of chain condition 1 - DMA has signaled an end of chain condition

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RW/1C	**TINT:** Receiver Time-out Interrupt 0 - No receiver time-out pending 1 - Receiver time-out pending
18	0x0 RW/1C	**PINT:** Peripheral Trailing Byte Interrupt 0 - No peripheral trailing byte interrupt pending 1 - Peripheral trailing byte interrupt pending
17:16	0x0 RO	**RSVD2:** Reserved
15:12	0xf RO	**RFL:** Receive FIFO Level Number of entries minus one in Receive FIFO. Note: When the value 0xF is read, the FIFO is either empty or full and the programmer should refer to the RNE bit
11:8	0x0 RO	**TFL:** Transmit FIFO Level Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the TNF bit.
7	0x0 RW/1C	**ROR:** Receive FIFO Overrun 0 - Receive FIFO has not experienced an overrun 1 - Attempted data write to full receive FIFO, request interrupt
6	0x0 RO	**RFS:** Receive FIFO Service Request 0 - Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 - Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0x0 RO	**TFS:** Transmit FIFO Service Request 0 - Transmit FIFO level exceeds the TFT threshold (TFT+1), or SSP disabled 1 - Transmit FIFO level is at or below TFT threshold (TFT+1), request interrupt
4	0x0 RO	**BSY:** SSP Busy 0 - SSP is idle or disabled 1 - SSP currently transmitting or receiving a frame
3	0x0 RO	**RNE:** Receive FIOF Not Empty 0 - Receive FIFO is empty 1 - Receive FIFO is not empty
2	0x1 RO	**TNF:** Transmit FIFO Not Full 0 - Transmit FIFO is full 1 - Transmit FIFO is not full
1:0	0x0 RO	**RSVD3:** Reserved

9.8.4 SSP Interrupt Test Register (SSITR)—Offset Ch

The read-write SSP Interrupt Test registers should be used only for testing purposes. Writing a 1 to the test transmit FIFO request SSITR.TTFS, bit 5, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Transmit FIFO. Writing a 1 to the test receive FIFO request SSITR.TRFS, bit 6, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Receive FIFO. Writing a 1 to the test receive FIFO overrun bit SSITR.TROR, bit 7, will generate a non-maskable Interrupt strobe signal to the Interrupt controller only, no DMA request will be made. Setting any of these bits will also cause the corresponding status bit(s) to be set in the Enhanced SSP Status register (SSSR). The Interrupt and/or service request, caused by the setting of one of these test bits, will remain active until the test bit is cleared by writing a 0 it. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

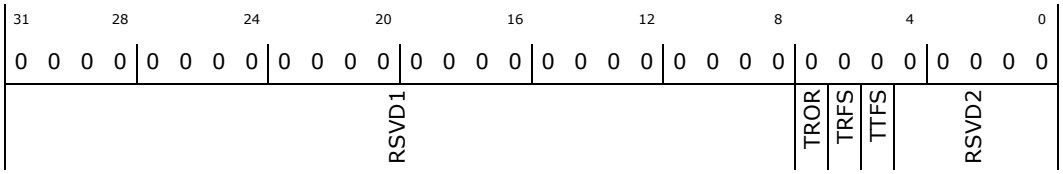
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD1:** Reserved
7	0x0 RW	**TROR:** Test Receive FIFO overrun 0 - No receive FIFO overrun service request 1 - Generates non-maskable interrupt to CPU. No DMA request is generated
6	0x0 RW	**TRFS:** Test Receive FIFO service request 0 - No receive FIFO service request 1 - Generates non-maskable interrupt to CPU and a DMA request for receive FIFO
5	0x0 RW	**TTFS:** Test Transmit FIFO service request 0 - No transmit FIFO service request pending 1 - Generates non-maskable interrupt to CPU and a DMA request for transmit FIFO
4:0	0x0 RO	**RSVD2:** Reserved

9.8.5 SSP Data (SSDR)—Offset 10h

The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO, the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.TFL, SSSR.RFL, SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32-bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32-bits is automatically right-justified in the Receive FIFO. When the Enhanced SSP is programmed for National Semiconductor Microwire* frame format and if the size for Transmit data is 8-bits as selected by SSCR1.MWDS=0, then the most significant 24-bits are ignored. Similarly, if the size for the Transmit data is 16-bit as selected by SSCR1.MWDS=1, then most significant 16-bits are ignored. The SSCR0.DSS field controls the Receive data size.

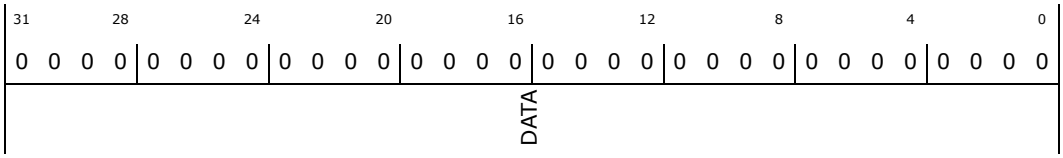
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**DATA:** Data word to be written to/read from transmit/receive FIFO

9.8.6 SSP Time Out (SSTO)—Offset 28h

The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

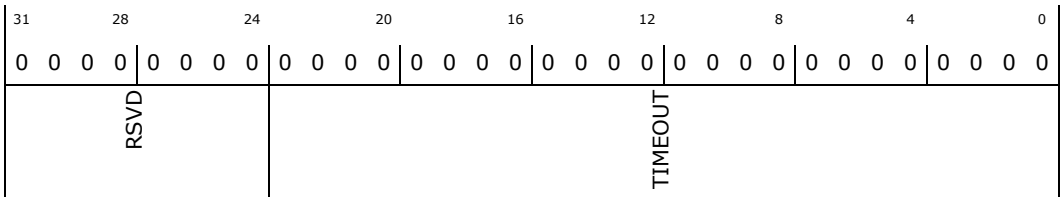
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD:** Reserved
23:0	0x0 RW	**TIMEOUT:** Timeout Value Is the value that defines the timeout interval, given by TIMEOUT/Peripheral Clock Frequency

9.8.7 SSP Programmable Serial Protocol (SSPSP)—Offset 2Ch

The Enhanced SSP Programmable Protocol registers are read-write registers that contain eight fields that are used to program the various programmable serial-protocol parameters. When using PSP format in Network mode, the parameters SFRMDLY,

STRTDLY, DMYSTP, DMYSTRT must be set to 0. Other parameters (such as FRMPOL, SCMODE, FSRT, SFRMDWDTH) are programmable. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

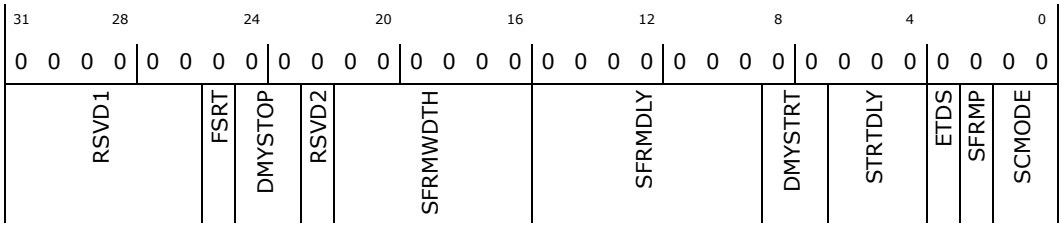
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD1:** Reserved
25	0x0 RW	**FSRT:** Frame Sync Relative Timing Bit 0 - Next frame is asserted after the end of the T4 timing 1 - Next frame is asserted with the LSB of the previous frame
24:23	0x0 RW	**DMYSTOP:** Dummy Stop Programmed value sets the number of SSPSCLK cycles that follow the transmitted data
22	0x0 RW	**RSVD2:** Reserved
21:16	0x0 RW	**SFRMWDTH:** Serial Frame Width Programmed value sets frame width (1-38)
15:9	0x0 RW	**SFRMDLY:** Serial Frame Delay Programmed value sets the number of half SSPSCLK cycles from TXD/RXD being driven to SSPSFRM being asserted (0-74)
8:7	0x0 RW	**DMYSTRT:** Dummy Start Programmed value sets the number of SSPSCLKs after STRTDLY is complete that precede the transmit/receive data
6:4	0x0 RW	**STRTDLY:** Start Delay Programmed value sets start delay that is used to set the idle time of SSPSCLK between transfers (0-7 SSPSCLK periods)
3	0x0 RW	**ETDS:** End of Transfer Data State 0 - Low 1 - Last value (bit 0)
2	0x0 RW	**SFRMP:** Serial Frame Polarity 0 - SSPSFRM is active low 1 - SSPSFRM is active high
1:0	0x0 RW	**SCMODE:** Serial bit-rate Clock Mode 00 - Data driven (falling), Data sampled (rising), Idle state (low) 01 - Data driven (rising), Data sampled (falling), Idle state (low) 10 - Data driven (rising), Data sampled (falling), Idle state (high) 11 - Data driven (falling), Data sampled (rising), Idle state (high)

9.8.8 SSP TX Time Slot Active (SSTSA)—Offset 30h

The Enhanced SSP TX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will transmit data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

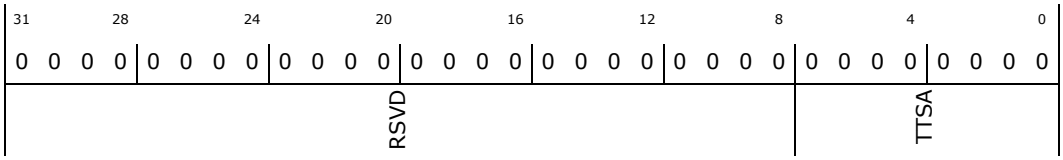
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RW	**TTSA:** TX Time Slot Active 0 - SSP will not transmit data in this time slot 1 - SSP will transmit data in this time slot

9.8.9 SSP RX Time Slot Active (SSRSA)—Offset 34h

The Enhanced SSP RX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will receive data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

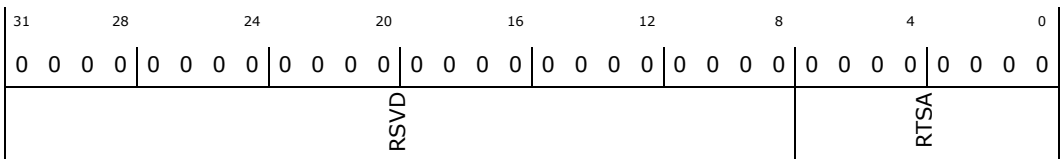
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RW	**RTSA:** RX Time Slot Active 0 - SSP will not receive data in this time slot 1 - SSP will receive data in this time slot

9.8.10 SSP Time Slot Status (SSTSS)—Offset 38h

The Enhanced SSP Time Slot Status registers are read only registers that indicate which Time Slot the Enhanced SSP is currently in when the Enhanced SSP is in Network Mode (SSCR0.MOD = 1). This register is not valid when the Enhanced SSP is not in Network Mode. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

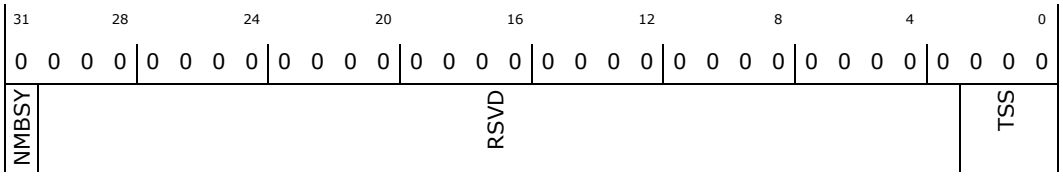
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**NMBSY:** Network Mode Busy 0 - No frame is currently active (in network mode only) 1 - SSP is in network mode and a frame is currently active
30:3	0x0 RO	**RSVD:** Reserved
2:0	0x0 RO	**TSS:** Time Slot Status Value indicates which time slot is currently active

9.8.11 SSP Audio Clock Divider (SSACD)—Offset 3Ch

The Enhanced SSP Audio Clock Divider registers are read-write registers that indicate which clock frequency is sent to the Enhanced SSP and to the SYSCLK pin. If SSCR0.SCR is not 0, then there is no guaranteed phase relationship between SYSCLK and SSPSCLK. The SSPSFRM Frame Synch Sampling Frequency is calculated by dividing the chosen PLL output clock frequency (SSACD.ACPS) by the chosen divider (SSACD.ACDS) which gives the SYSCLK frequency. The SYSCLK is then divided by 4 (or by 1) to get the SSPSCLK. The SSPSCLK is divided by the data size (EDSS, DSS values)

and by the number of time slots being used (SSCR0.FRDC value), if any, to give the SSPSFRM frequency. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

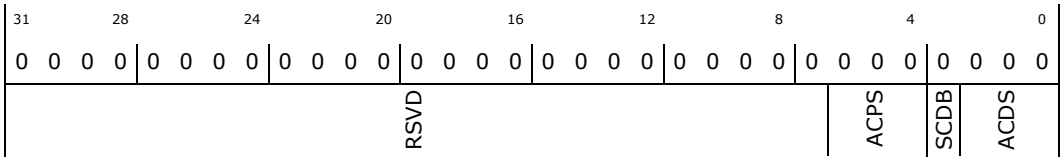
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**RSVD:** Reserved
6:4	0x0 RW	**ACPS:** Audio Clock PLL Select Value indicates which PLL output clock is sent to the clock divider in the clock unit 000: 5.622MHz, 001: 11.345MHz, 010: 12.235MHz, 011: 14.857MHz, 100: 32.842MHz, 101: 48.000MHz, 110, 111: Reserved
3	0x0 RW	**SCDB:** SYSCLK Divider Bypass 0 - SYSCLK is divided by 4 before being sent to SSP 1 - SYSCLK is not divided before being sent to SSP
2:0	0x0 RW	**ACDS:** Audio Clock Divider Select Value indicates which divider will be used by the clock unit to create the SYSCLK output pin. Clock divider value will be 2^ACDS, max ACDS = 5.

9.8.12 I2S Transmit FIFO (ITF)—Offset 40h

The I2S Transmit FIFO register is for writing the water mark for the I2S transmit FIFO and also for reading the number of entries in the I2S transmit FIFO

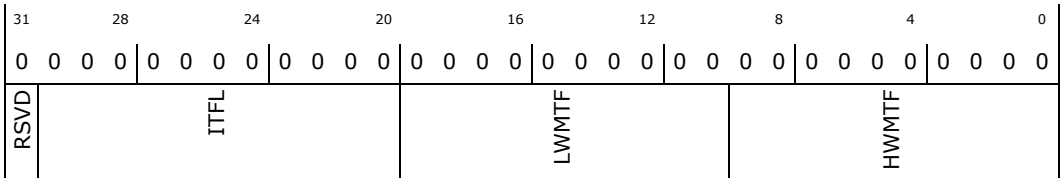
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RSVD:** Reserved
30:20	0x0 RO	**ITFL:** I2S Transmit FIFO Level Number of entries in I2S Transmit FIFO
19:10	0x0 RW	**LWMTF:** Low Water Mark Transmit FIFO.Set the low water mark of the I2S transmit FIFO.
9:0	0x0 RW	**HWMTF:** High Water Mark Transmit FIFO.Set the high water mark of the I2S transmit FIFO.

9.8.13 SPI Transmit FIFO (SITF)—Offset 44h

The SPI Transmit FIFO register is for writing the water mark for the SPI transmit FIFO and also for reading the number of entries in the SPI transmit FIFO

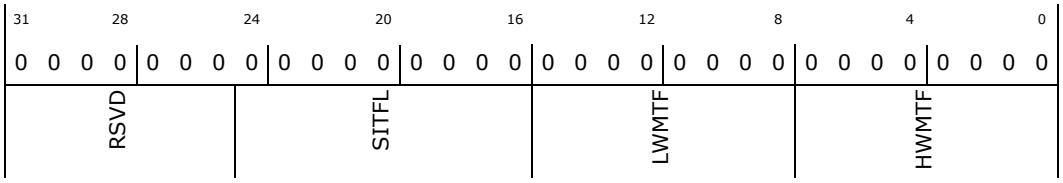
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD:** Reserved
24:16	0x0 RO	**SITFL:** SPI Transmit FIFO Level Number of entries in SPI Transmit FIFO.
15:8	0x0 RW	**LWMTF:** Low Water Mark Transmit FIFO. Set the low water mark of the SPI transmit FIFO.
7:0	0x0 RW	**HWMTF:** High Water Mark Transmit FIFO. Set the high water mark of the SPI transmit FIFO.

9.8.14 SPI Receive FIFO (SIRF)—Offset 48h

The SPI Receive FIFO register is for writing the water mark for the SPI receive FIFO and also for reading the number of entries in the SPI receive FIFO

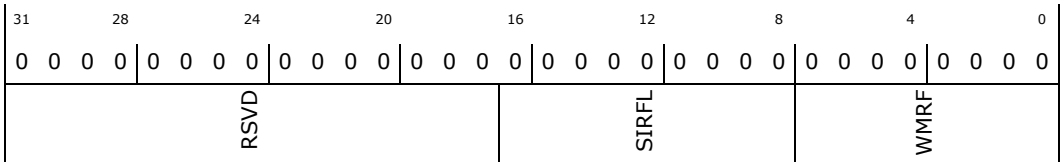
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RSVD:** Reserved
16:8	0x0 RO	**SIRFL:** SPI Receive FIFO Level Number of entries in SPI Receive FIFO.
7:0	0x0 RW	**WMRF:** Water Mark Receive FIFO. Set the water mark of the SPI receive FIFO.

9.8.15 private clock params (PRV_CLOCK_PARAMS)—Offset 400h

private clock params

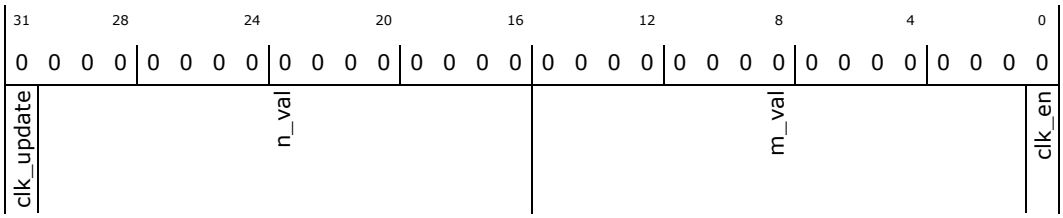
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 400h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**clk_update:** update the clock divider after seeting new m and n values
30:16	0x0 RW	**N_VAL (n_val):** n value for the m over n divider
15:1	0x0 RW	**M_VAL (m_val):** m value for the m over n divider
0	0x0 RW	**clk_en:** clk en of the m over n divider

9.8.16 software reset (RESETS)—Offset 404h

software reset

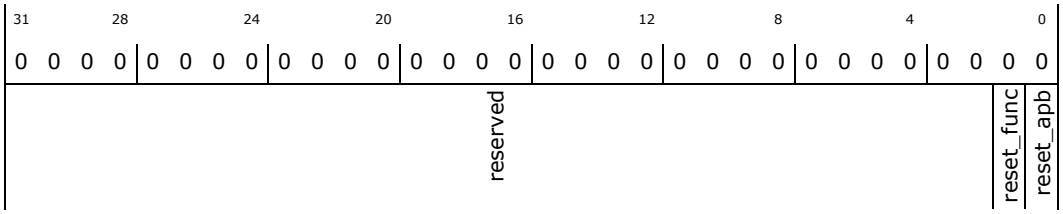
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 404h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (reserved):** Reserved
1	0x0 RW	**reset_func:** reset the func clock domain
0	0x0 RW	**reset_apb:** reset the apb domain

9.8.17 General purpose register (GENERAL)—Offset 408h

General purpose register

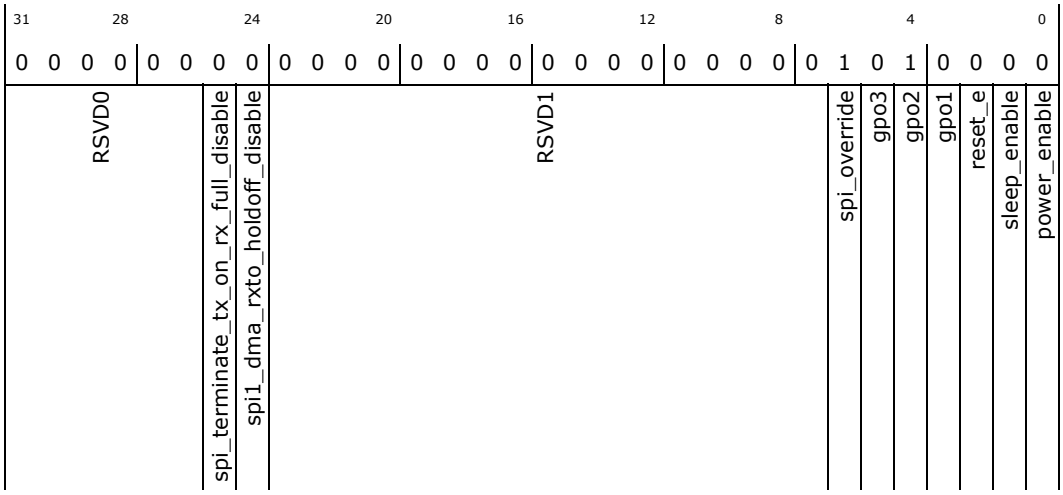
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 408h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 00000050h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD0:** Reserved
25	0x0 RW	**spi_terminate_tx_on_rx_full_disable:** disable terminate tx when rx full
24	0x0 RW	**spi1_dma_rxto_holdoff_disable:** disable dma hold off
23:7	0x0 RO	**RSVD1:** Reserved
6	0x1 RW	**spi_override:** not applicable
5	0x0 RW	**gpo3:** not applicable
4	0x1 RW	**gpo2:** not applicable
3	0x0 RW	**gpo1:** not applicable
2	0x0 RW	**reset_e:** not applicable
1	0x0 RW	**sleep_enable:** not applicable
0	0x0 RW	**power_enable:** not applicable

9.8.18 SPI misc register (SSP_REG)—Offset 40Ch

SPI misc register

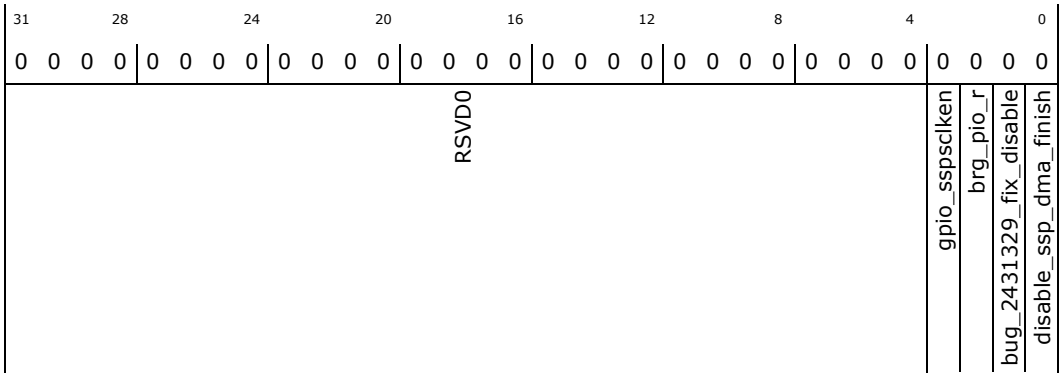
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RSVD0:** Reserved
3	0x0 RW	**gpio_sspsclken:** not applicable
2	0x0 RW	**brg_pio_r:** not applicable
1	0x0 RW	**bug_2431329_fix_disable:** not applicable
0	0x0 RW	**disable_ssp_dma_finish:** disable ssp dma finish

9.8.19 SPI chip select control register (SPI_CS_CTRL)—Offset 418h

SPI chip select control register

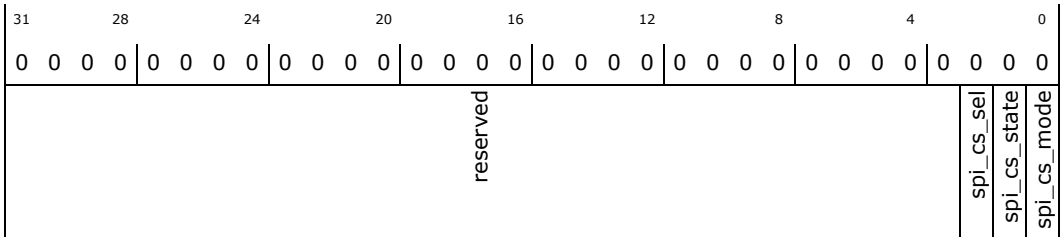
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 418h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:6] + 10h

Default: 00000000h

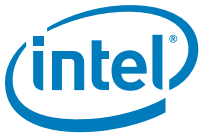


Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RW	**reserved:** reserved
2	0x0 RW	**spi_cs_sel:** SW select bit to choose either CS0 or CS1 for spi
1	0x0 RW	**spi_cs_state:** SW override of CS line in SW mode for spi
0	0x0 RW	**spi_cs_mode:** selects HW mode or SW mode for chip select for spi

9.9 SIO SPI 3 PCI Configuration Registers

Table 72. Summary of SIO SPI 2 PCI Configuration Registers—0/30/7

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4255	00008086h
4–7h	4	"STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h" on page 4255	00100000h
8–Bh	4	"REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4257	00000000h
C–Fh	4	"CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4258	00800000h
10–13h	4	"BAR -Base Address Register (BAR)—Offset 10h" on page 4258	00000000h
14–17h	4	"BAR1 -Base Address Register1 (BAR1)—Offset 14h" on page 4259	00000000h
2C–2Fh	4	"SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4260	00000000h
30–33h	4	"EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4261	00000000h
34–37h	4	"CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4261	00000000h
3C–3Fh	4	"INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4262	00000100h
80–83h	4	"POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4262	00030001h
84–87h	4	"PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4263	00000008h
F8–FBh	4	"Manufacturers ID (MANID)—Offset F8h" on page 4264	00000000h



9.9.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

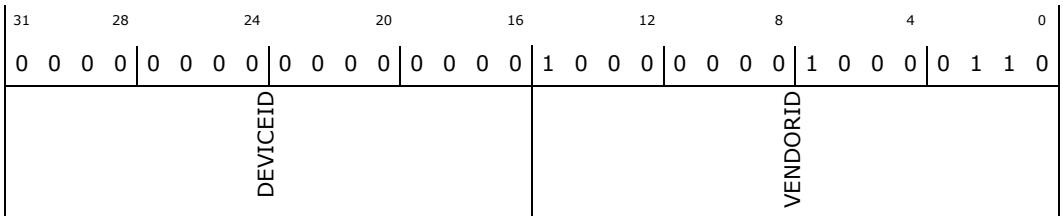
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:7] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**DEVICEID:** Device ID identifies the particular AHB/APB device. This is tied to a strap at the top level. Because of tool issues, the HTML files show this field as 0, but the following are the POR values for SoC: LPIO1 DMA: 0x2286 LPIO1 PWM1: 0x2288 LPIO1 PWM2: 0x2289 LPIO1 HSUART1: 0x228A LPIO1 HSUART2: 0x228C LPIO1 SPI1: 0x228E LPIO1 SPI2: 0x2290 LPIO1 SPI3: 0x22AC LPIO2 DMA: 0x22C0 LPIO2 I2C1: 0x22C1 LPIO2 I2C2: 0x22C2 LPIO2 I2C3: 0x22C3 LPIO2 I2C4: 0x22C4 LPIO2 I2C5: 0x22C5 LPIO2 I2C6: 0x22C6 LPIO2 I2C7: 0x22C7 For the final word on this, please see Ray Ng's SoC RevID and DevID HAS on Infofactory: https://ifcollaborate.intel.com/IFC/getdoc.aspx?docbase=InfoFactoryKBandchronid=09005ffd80e84b43andver=CURRENTandqepop=false
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap the top level.

9.9.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

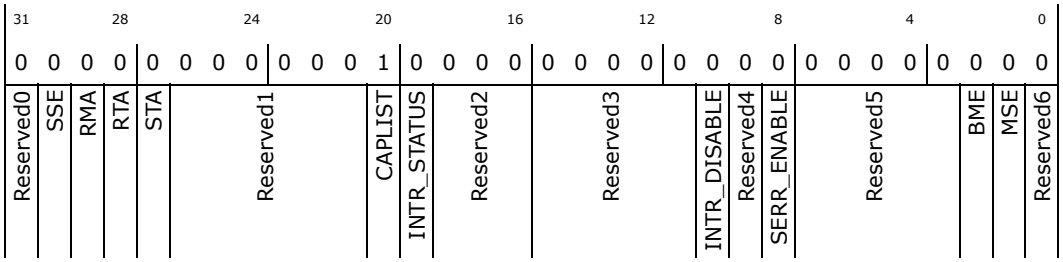
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:7] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved0:** Reserved
30	0x0 RW/1C	**SSE:** This bit is set when a device sends an DO_SERR message, and the SERR# Enable bit in the Command register is 1
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric PortReceived Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27	0x0 RW/1C	**STA:** The Bridge sets this bit whenever it responds to a transaction with CA abort. If the SERR# Enable bit is set, the Bridge sets the Signaled System Error bit and sends an DO_SERR message on the IOSF Sideband.
26:21	0x0 RO	**Reserved1:** Reserved
20	0x1 RO	**CAPLIST:** Capabilities List: Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt .i.e Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.. Reset value of this bit is 0.
9	0x0 RO	**Reserved4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: If both SERR# Enable and the Unsupported Request Reporting Enable (URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0x0 RO	**Reserved6:** Reserved

9.9.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

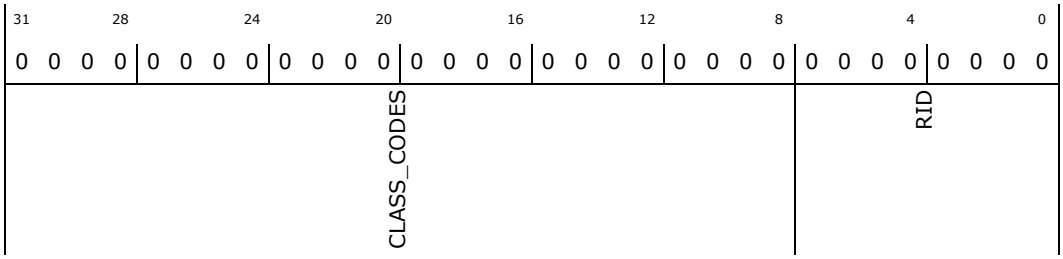
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:7] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

9.9.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

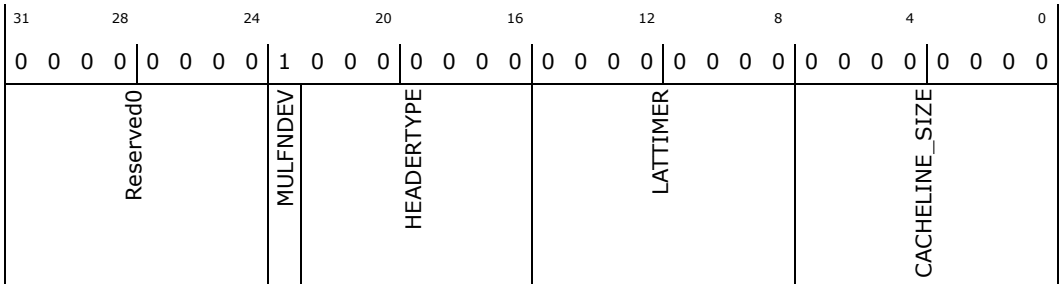
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:7] + Ch

Default: 00800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x1 RO	**MULFNDEV:** Multi Function Device: This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. Value of 1 indicates multifunction device value of 0 indicates single function device
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	0x0 RO	**LATTIMER:** Latency Timer: Doesn.t apply to PCI Express. Hardwired to 00h.
7:0	0x0 RW	**CACHELINE_SIZE:** Cache Line Size: Doesn.t apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

9.9.5 BAR -Base Address Register (BAR)—Offset 10h

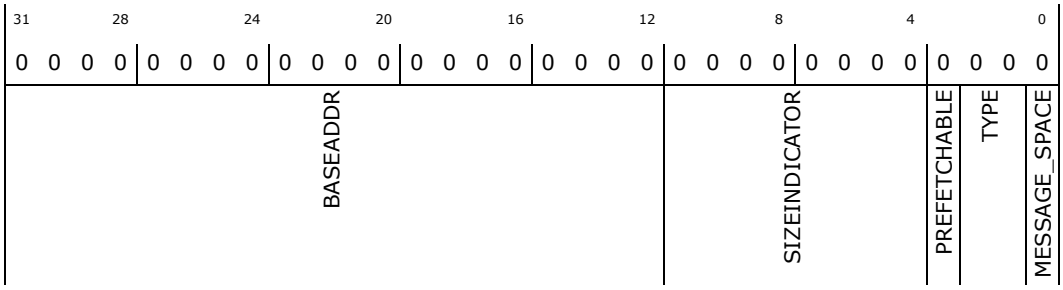
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the AHB device memory space. Taken from Strap values as 1's. Please note that for DMA this field goes from [31:14], or 16kbyte, and the SIZEINDICATOR field goes from [13:4].
11:4	0x0 RO	**SIZEINDICATOR:** Size Indicator Read Only: Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0x0 RO	**TYPE:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.9.6 BAR1 -Base Address Register1 (BAR1)—Offset 14h

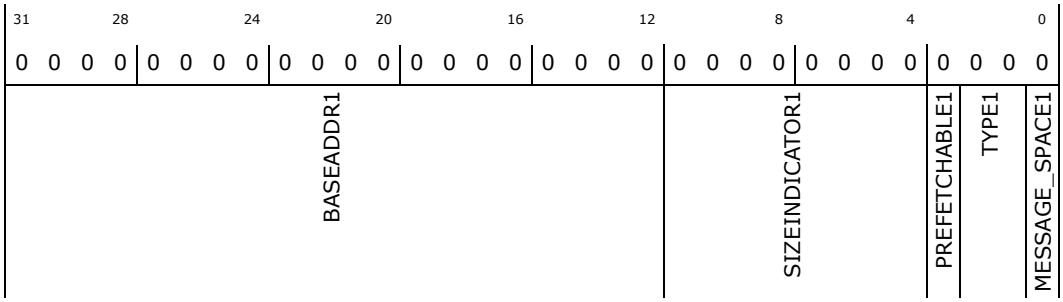
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:7] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	0x0 RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not
2:1	0x0 RO	**TYPE1:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.9.7 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

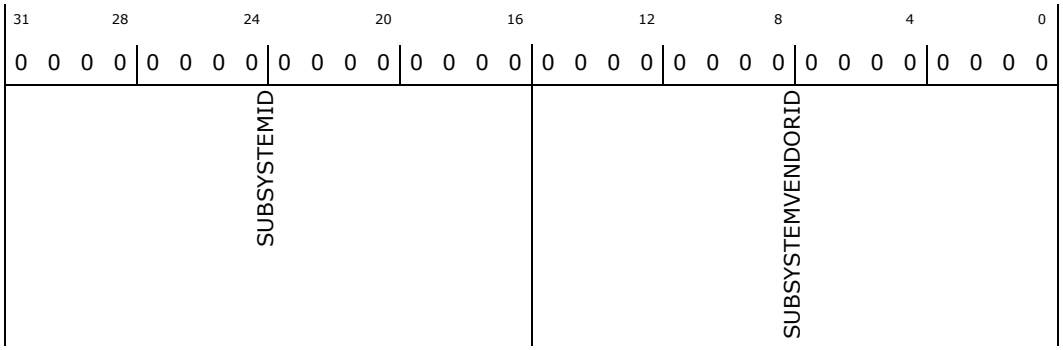
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:7] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

9.9.8 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

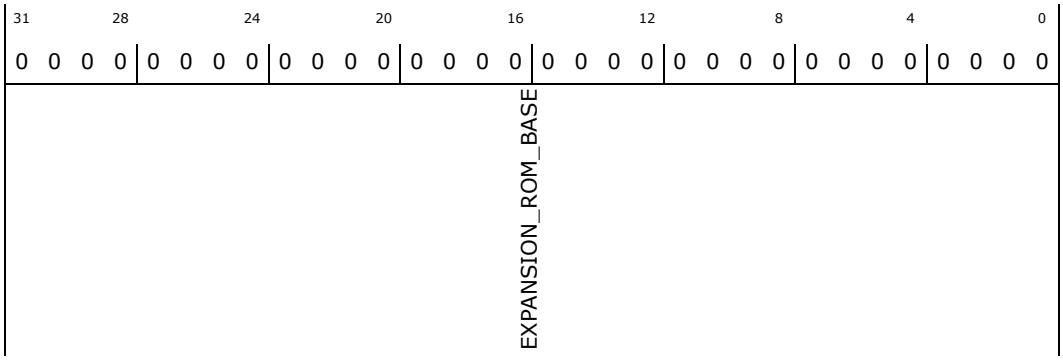
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:7] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** A value of all zeros indicates no support for expansion ROM.

9.9.9 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

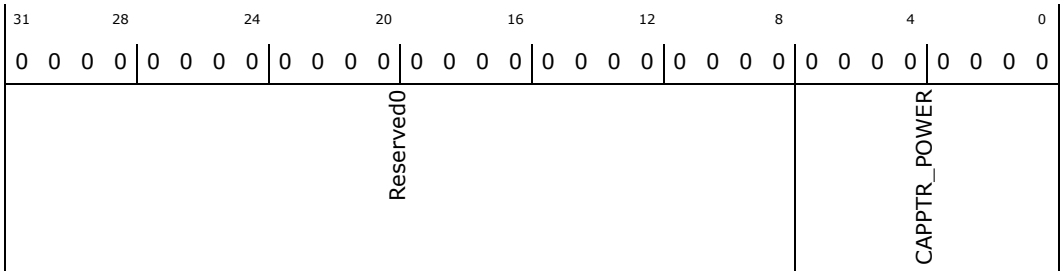
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:7] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x0 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

9.9.10 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

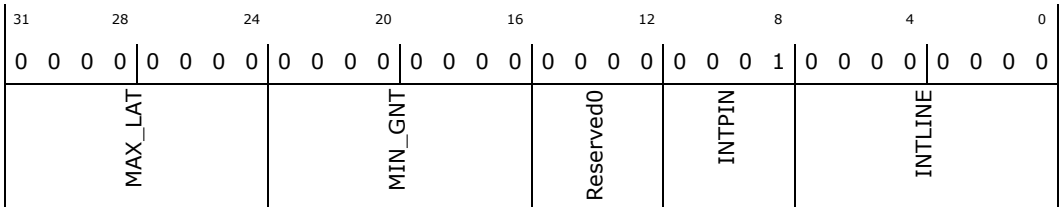
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:7] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

9.9.11 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

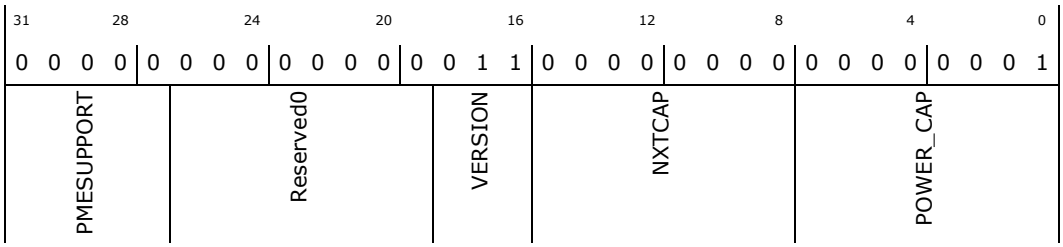
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:7] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** PME_Support - This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

9.9.12 PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

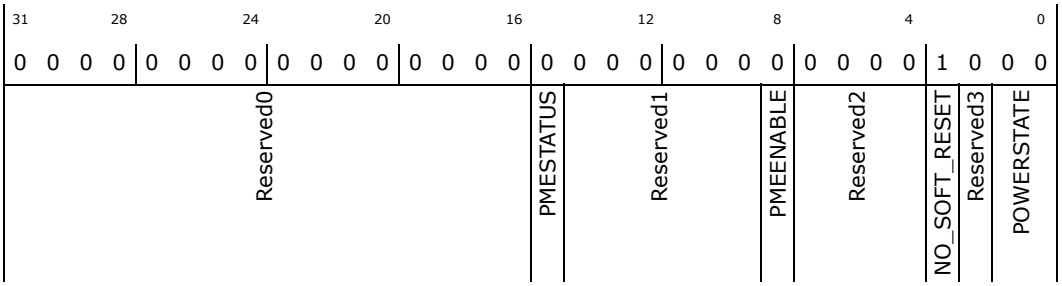
PMECTRLSTATUS - PME Control and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:7] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

9.9.13 Manufacturers ID (MANID)—Offset F8h

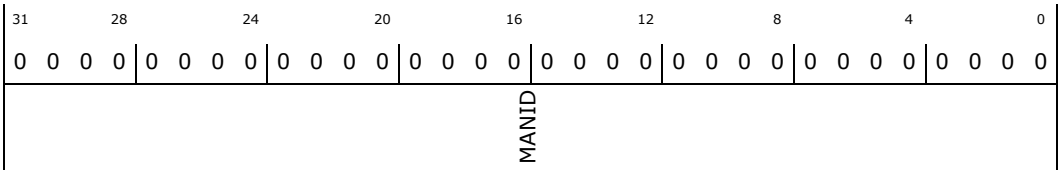
Manufacturers ID

Access Method

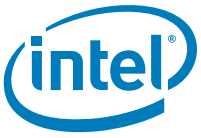
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:7] + F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: This register is brought out as straps to the top level.



9.10 SIO SPI 3 Memory Mapped I/O

Table 73. Summary of SIO SPI 3 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"SSP Cntrol Register 0 (SSCR0)—Offset 0h" on page 4267	00000000h
4–7h	4	"SSP Control Register 1 (SSCR1)—Offset 4h" on page 4268	00000000h
8–Bh	4	"SSP Status Register (SSSR)—Offset 8h" on page 4270	0000F004h
C–Fh	4	"SSP Interrupt Test Register (SSITR)—Offset Ch" on page 4271	00000000h
10–13h	4	"SSP Data (SSDR)—Offset 10h" on page 4272	00000000h
28–2Bh	4	"SSP Time Out (SSTO)—Offset 28h" on page 4273	00000000h
2C–2Fh	4	"SSP Programmable Serial Protocol (SSPSP)—Offset 2Ch" on page 4273	00000000h
30–33h	4	"SSP TX Time Slot Active (SSTSA)—Offset 30h" on page 4275	00000000h
34–37h	4	"SSP RX Time Slot Active (SSRSA)—Offset 34h" on page 4275	00000000h
38–3Bh	4	"SSP Time Slot Status (SSTSS)—Offset 38h" on page 4276	00000000h
3C–3Fh	4	"SSP Audio Clock Divider (SSACD)—Offset 3Ch" on page 4276	00000000h
40–43h	4	"I2S Transmit FIFO (ITF)—Offset 40h" on page 4277	00000000h
44–47h	4	"SPI Transmit FIFO (SITF)—Offset 44h" on page 4278	00000000h
48–4Bh	4	"SPI Receive FIFO (SIRF)—Offset 48h" on page 4278	00000000h
400–403h	4	"private clock params (PRV_CLOCK_PARAMS)—Offset 400h" on page 4279	00000000h
404–407h	4	"software reset (RESETS)—Offset 404h" on page 4280	00000000h
408–40Bh	4	"General purpose register (GENERAL)—Offset 408h" on page 4280	00000050h
40C–40Fh	4	"SPI misc register (SSP_REG)—Offset 40Ch" on page 4281	00000000h
418–41Bh	4	"SPI chip select control register (SPI_CS_CTRL)—Offset 418h" on page 4282	00000000h

9.10.1 SSP Cntrol Register 0 (SSCR0)—Offset 0h

The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

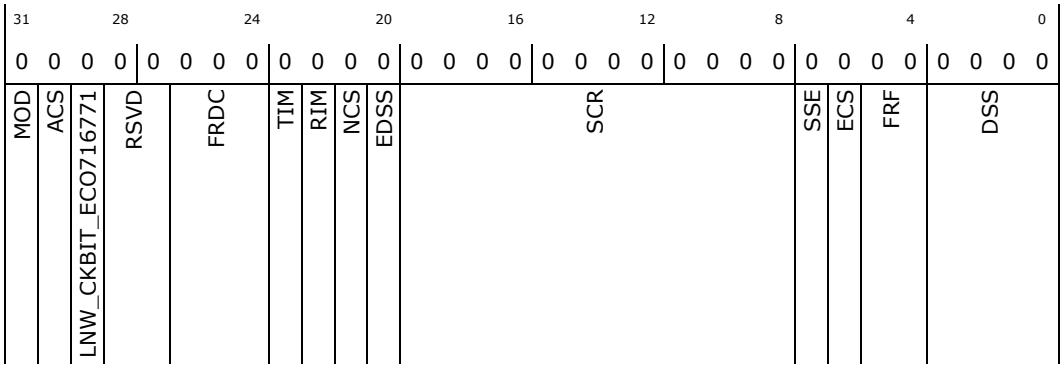
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**MOD:** Mode 0 - Normal SSP Mode 1 - Network Mode
30	0x0 RW	**ACS:** Audio Clock Select 0 - Clock selection is determined by the NCS and ECS bits 1 - Audio Clock (and Audio Clock Divider) are used to create the SSP's serial clock (SSPSCLK)
29	0x0 RW	**LNW_CKBIT_ECO716771:** in the TRM document for the customer.
28:27	0x0 RO	**RSVD:** Reserved
26:24	0x0 RW	**FRDC:** Frame Rate Divider Control Value 0-7 indicates the number of time slots per frame when in network mode (the actual number of time slots is FRDC+1, so 1 to 8 time slots).
23	0x0 RW	**TIM:** Transmit FIFO Under Run Interrupt Mask 0 - TUR events will generate an SSP interrupt 1 - TUR events will not generate an SSP interrupt
22	0x0 RW	**RIM:** Receive FIFO Over Run Interrupt Mask 0 - ROR events will generate an SSP interrupt 1 - ROR events will not generate an SSP interrupt
21	0x0 RW	**NCS:** Network Clock Select 0 - Clock selection is determined by ECS bit 1 - Network clock is used to create the SSP's serial clock (SSPSCLK)
20	0x0 RW	**EDSS:** Extended Data Size Select 0 - A zero is preappended to the DSS value which sets the DSS range from 4-16 bits 1 - A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits

Bit Range	Default & Access	Field Name (ID): Description
19:8	0x0 RW	**SCR:** Serial Clock Rate Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0x0 RW	**SSE:** Synchronous Serial Port Enable 0 - SSP operation disabled 1 - SSP operation enabled
6	0x0 RW	**ECS:** External Clock Select 0 - On-chip clock used to produce the SSP's serial clock (SSPSCLK) 1 - SSPEXTCLK/GPIO pin is used to create the SSP's SSPCLK
5:4	0x0 RW	**FRF:** Frame Format 00 - Motorola Serial Peripheral Interface (SPI) 01 - Texas Instruments Synchronous Serial Protocol (SSP) 10 - National Semiconductor Microwire 11 - Programmable Serial Protocol (PSP)
3:0	0x0 RW	**DSS:** Data Size Select With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

9.10.2 SSP Control Register 1 (SSCR1)—Offset 4h

The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

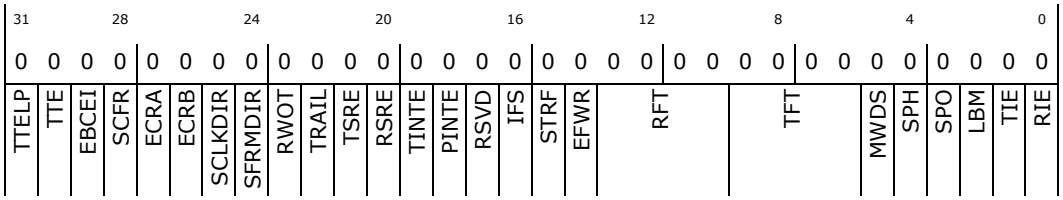
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

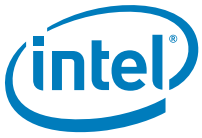
Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**TTELP:** TXD Tristate Enable on Last Phase 0 - TXD line will be tristated on same clock edge as TXD is to be flopped 1 - TXD line will be tristated clock edge after TXD is to be flopped
30	0x0 RW	**TTE:** TXD Tristate Enable 0 - TXD line will not be tristated 1 - TXD line will be tristated when no transmitting data
29	0x0 RW	**EBCEI:** Enable Bit Count Error Interrupt 0 - Interrupt due to a bit count error is disabled 1 - Interrupt due to a bit count error is enabled
28	0x0 RW	**SCFR:** Slave Clock Free Running 0 - clock input to SSPSCLK is continuously running 1 - clock input to SSPSCLK is only active durring transfers



Bit Range	Default & Access	Field Name (ID): Description
27	0x0 RW	**ECRA:** Enable Clock Request A 0 - clock request from other SSP is disabled 1 - clock request from other SSP is enabled
26	0x0 RW	**ECRB:** Enable Clock Request B 0 - clock request from other SSP is disabled 1 - clock request from other SSP is enabled
25	0x0 RW	**SCLKDIR:** SSP Serial Bit Rate Clock (SSPSCLK) Direction 0 - Master mode, SSP drives SSPSCLK 1 - Slave mode, SSP recieves SSPSCLK
24	0x0 RW	**SFRMDIR:** SSP Frame (SSPSFRM) Direction 0 - Master mode, SSP drives SSPSFRM 1 - Slave mode, SSP receives SSPSFRM
23	0x0 RW	**RWOT:** Receive With Out Transmit 0 - Transmit/Receive mode 1 - Receive without transmit mode
22	0x0 RW	**TRAIL:** Trailing Byte 0 - Processor based, trailing bytes are handled by processor 1 - DMA based, trailing bytes are handled by DMA
21	0x0 RW	**TSRE:** Transmit Service Request Enable 0 - DMA Service Request is disabled 1 - DMA Service Request is enabled
20	0x0 RW	**RSRE:** Receive Service Request Enable 0 - DMA Service Request is disabled 1 - DMA Service Request is enabled
19	0x0 RW	**TINTE:** Receiver Time-out Interrupt Enable 0 - Receiver Time-out interrupts are disabled 1 - Receiver Time-out interrupts are enabled
18	0x0 RW	**PINTE:** Peripheral Trailing Byte Interrupts Enable 0 - Peripheral Trailing Byte Interrupts are disabled 1 - Peripheral Trailing Byte Interrupts are enabled
17	0x0 RW	**RSVD:** Reserved
16	0x0 RW	**IFS:** Invert Frame Signal 0 - Frame polarity is determined by SSP format and PSP polarity bits 1 - Frame signal will be inverted from the normal SSP frame signal (as defined by the SSP format nad PSP polarity bits)
15	0x0 RW	**STRF:** Select FIFO for EFWR (test mode bit) (when EFWR=1) 0 - Transmit FIFO is selected for both writes and reads through the SSP Data Register (SSDR) 1 - Receive FIFO is selected for both writes and reads through the SSP Data Register (SSDR)
14	0x0 RW	**EFWR:** Enable FIFO Write/Read (test mode bit) 0 - FIFO write/read special function is disabled (normal SSP operational mode) 1 - FIFO write/read special function is enabled
13:10	0x0 RW	**RFT:** Receive FIFO Trigger Threshold Sets threshold level at which receive FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.
9:6	0x0 RW	**TFT:** Transmit FIFO Trigger Threshold Sets threshold level at which transmit FIFO asserts interrupt. This level should be set to the desired threshold value minus 1.
5	0x0 RW	**MWDS:** Microwire Transmit Data Size 0 - 8-bit command words are transmitted 1 - 16-bit command words are transmitted
4	0x0 RW	**SPH:** Motorola SPI SSPSCLK phase setting 0 - SSPSCLK is inactive one sycle at the start of a fram and cycle at the end of a frame 1 - SSPSCLK is inactive cycle at the start of a frame and one cycle at the end of a frame
3	0x0 RW	**SPO:** Motorola SPI SSPSCLK polarity setting 0 - The inactive or idle state of SSPSCLK is low 1 - The inactive or idle state of SSPSCLK is high

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**LBM:** Loop-Back Mode (test mode bit) 0 - Normal serial port operation enabled 1 - Output of transmit serial shifter connected to input of receive serial shifter, internally
1	0x0 RW	**TIE:** Transmit FIFO Interrupt Enable 0 - Transmit FIFO level interrupt is disabled 1 - Transmit FIFO level interrupt is enabled
0	0x0 RW	**RIE:** Receive FIFO Interrupt Enable 0 - Receive FIFO level interrupt is disabled 1 - Receive FIFO level interrupt is enabled

9.10.3 SSP Status Register (SSSR)—Offset 8h

The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

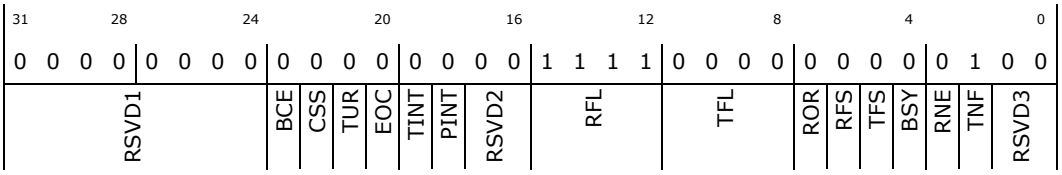
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

Default: 0000F004h



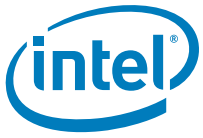
Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD1:** Reserved
23	0x0 RW/1C	**BCE:** Bit Count Error 0 - SSP has not experienced a bit count error 1 - SSPSFRM signal has been asserted when the bit counter was not 0
22	0x0 RO	**CSS:** Clock Synchronization Status 0 - SSP is ready for slave clock operations 1 - SSP is currently busy synchronizing slave mode signals
21	0x0 RW/1C	**TUR:** Transmit FIFO Under Run 0 - Transmit FIFO has not experienced an under run 1 - Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0x0 RW/1C	**EOC:** End of Chain 0 - DMA has not signaled an end of chain condition 1 - DMA has signaled an end of chain condition

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RW/1C	**TINT:** Receiver Time-out Interrupt 0 - No receiver time-out pending 1 - Receiver time-out pending
18	0x0 RW/1C	**PINT:** Peripheral Trailing Byte Interrupt 0 - No peripheral trailing byte interrupt pending 1 - Peripheral trailing byte interrupt pending
17:16	0x0 RO	**RSVD2:** Reserved
15:12	0xf RO	**RFL:** Receive FIFO Level Number of entries minus one in Receive FIFO. Note: When the value 0xF is read, the FIFO is either empty or full and the programmer should refer to the RNE bit
11:8	0x0 RO	**TFL:** Transmit FIFO Level Number of entries in Transmit FIFO. Note: When the value 0x0 is read, the FIFO is either empty or full and the programmer should refer to the TNF bit.
7	0x0 RW/1C	**ROR:** Receive FIFO Overrun 0 - Receive FIFO has not experienced an overrun 1 - Attempted data write to full receive FIFO, request interrupt
6	0x0 RO	**RFS:** Receive FIFO Service Request 0 - Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 - Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0x0 RO	**TFS:** Transmit FIFO Service Request 0 - Transmit FIFO level exceeds the TFT threshold (TFT+1), or SSP disabled 1 - Transmit FIFO level is at or below TFT threshold (TFT+1), request interrupt
4	0x0 RO	**BSY:** SSP Busy 0 - SSP is idle or disabled 1 - SSP currently transmitting or receiving a frame
3	0x0 RO	**RNE:** Receive FIOF Not Empty 0 - Receive FIFO is empty 1 - Receive FIFO is not empty
2	0x1 RO	**TNF:** Transmit FIFO Not Full 0 - Transmit FIFO is full 1 - Transmit FIFO is not full
1:0	0x0 RO	**RSVD3:** Reserved

9.10.4 SSP Interrupt Test Register (SSITR)—Offset Ch

The read-write SSP Interrupt Test registers should be used only for testing purposes. Writing a 1 to the test transmit FIFO request SSITR.TTFS, bit 5, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Transmit FIFO. Writing a 1 to the test receive FIFO request SSITR.TRFS, bit 6, will generate a non-maskable Interrupt strobe signal to the Interrupt controller, and a DMA request for the Receive FIFO. Writing a 1 to the test receive FIFO overrun bit SSITR.TROR, bit 7, will generate a non-maskable Interrupt strobe signal to the Interrupt controller only, no DMA request will be made. Setting any of these bits will also cause the corresponding status bit(s) to be set in the Enhanced SSP Status register (SSSR). The Interrupt and/or service request, caused by the setting of one of these test bits, will remain active until the test bit is cleared by writing a 0 it. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

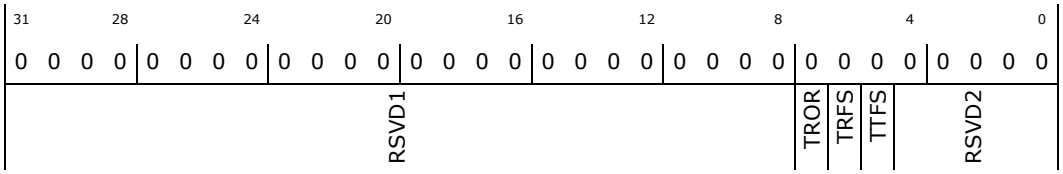


Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD1:** Reserved
7	0x0 RW	**TROR:** Test Receive FIFO overrun 0 - No receive FIFO overrun service request 1 - Generates non-maskable interrupt to CPU. No DMA request is generated
6	0x0 RW	**TRFS:** Test Receive FIFO service request 0 - No receive FIFO service request 1 - Generates non-maskable interrupt to CPU and a DMA request for receive FIFO
5	0x0 RW	**TTFS:** Test Transmit FIFO service request 0 - No transmit FIFO service request pending 1 - Generates non-maskable interrupt to CPU and a DMA request for transmit FIFO
4:0	0x0 RO	**RSVD2:** Reserved

9.10.5 SSP Data (SSDR)—Offset 10h

The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO, the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.TFL, SSSR.RFL, SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32-bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32-bits is automatically right-justified in the Receive FIFO. When the Enhanced SSP is programmed for National Semiconductor Microwire* frame format and if the size for Transmit data is 8-bits as selected by SSCR1.MWDS=0, then the most significant 24-bits are ignored. Similarly, if the size for the Transmit data is 16-bit as selected by SSCR1.MWDS=1, then most significant 16-bits are ignored. The SSCR0.DSS field controls the Receive data size.

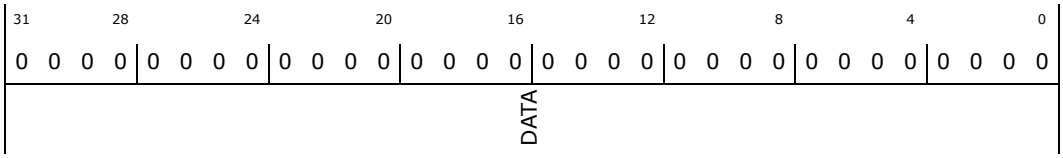
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**DATA:** Data word to be written to/read from transmit/receive FIFO

9.10.6 SSP Time Out (SSTO)—Offset 28h

The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

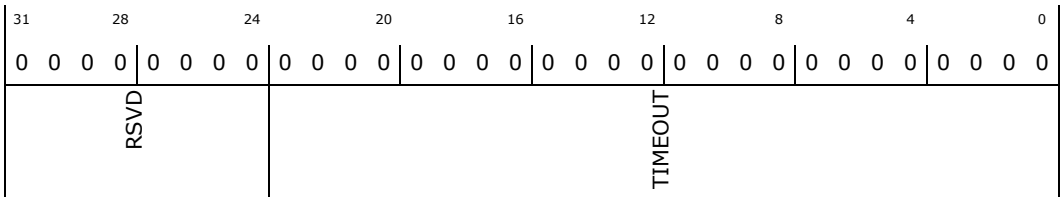
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

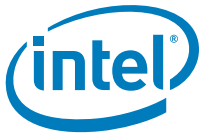
Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD:** Reserved
23:0	0x0 RW	**TIMEOUT:** Timeout Value Is the value that defines the timeout interval, given by TIMEOUT/Peripheral Clock Frequency

9.10.7 SSP Programmable Serial Protocol (SSPSP)—Offset 2Ch

The Enhanced SSP Programmable Protocol registers are read-write registers that contain eight fields that are used to program the various programmable serial-protocol parameters. When using PSP format in Network mode, the parameters SFRMDLY,



STRTDLY, DMYSTP, DMYSTRT must be set to 0. Other parameters (such as FRMPOL, SCMODE, FSRT, SFRMDWDTH) are programmable. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

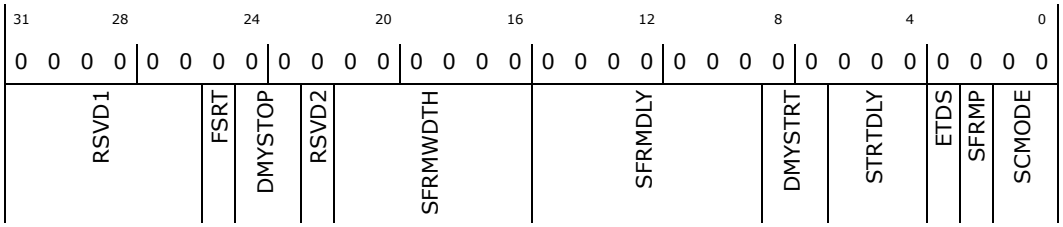
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD1:** Reserved
25	0x0 RW	**FSRT:** Frame Sync Relative Timing Bit 0 - Next frame is asserted after the end of the T4 timing 1 - Next frame is asserted with the LSB of the previous frame
24:23	0x0 RW	**DMYSTOP:** Dummy Stop Programmed value sets the number of SSPSCLK cycles that follow the transmitted data
22	0x0 RW	**RSVD2:** Reserved
21:16	0x0 RW	**SFRMWDTH:** Serial Frame Width Programmed value sets frame width (1-38)
15:9	0x0 RW	**SFRMDLY:** Serial Frame Delay Programmed value sets the number of half SSPSCLK cycles from TXD/RXD being driven to SSPSFRM being asserted (0-74)
8:7	0x0 RW	**DMYSTRT:** Dummy Start Programmed value sets the number of SSPSCLKs after STRTDLY is complete that precede the transmit/receive data
6:4	0x0 RW	**STRTDLY:** Start Delay Programmed value sets start delay that is used to set the idle time of SSPSCLK between transfers (0-7 SSPSCLK periods)
3	0x0 RW	**ETDS:** End of Transfer Data State 0 - Low 1 - Last value (bit 0)
2	0x0 RW	**SFRMP:** Serial Frame Polarity 0 - SSPSFRM is active low 1 - SSPSFRM is active high
1:0	0x0 RW	**SCMODE:** Serial bit-rate Clock Mode 00 - Data driven (falling), Data sampled (rising), Idle state (low) 01 - Data driven (rising), Data sampled (falling), Idle state (low) 10 - Data driven (rising), Data sampled (falling), Idle state (high) 11 - Data driven (falling), Data sampled (rising), Idle state (high)

9.10.8 SSP TX Time Slot Active (SSTSA)—Offset 30h

The Enhanced SSP TX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will transmit data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

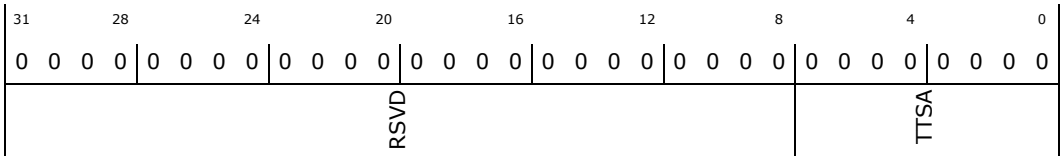
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RW	**TTSA:** TX Time Slot Active 0 - SSP will not transmit data in this time slot 1 - SSP will transmit data in this time slot

9.10.9 SSP RX Time Slot Active (SSRSA)—Offset 34h

The Enhanced SSP RX Time Slot Active registers are read-write registers that indicate which Time Slot the Enhanced SSP will receive data in and are ignored if the Enhanced SSP is not in Network Mode (SSCR0.MOD = 1). Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

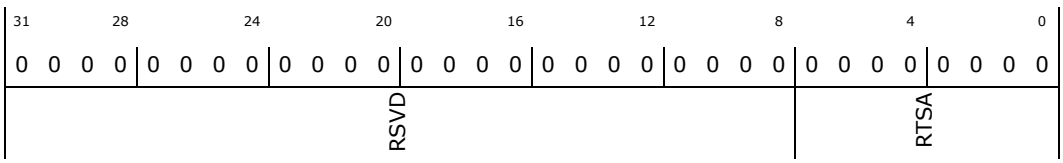
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD:** Reserved
7:0	0x0 RW	**RTSA:** RX Time Slot Active 0 - SSP will not receive data in this time slot 1 - SSP will receive data in this time slot

9.10.10 SSP Time Slot Status (SSTSS)—Offset 38h

The Enhanced SSP Time Slot Status registers are read only registers that indicate which Time Slot the Enhanced SSP is currently in when the Enhanced SSP is in Network Mode (SSCR0.MOD = 1). This register is not valid when the Enhanced SSP is not in Network Mode. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

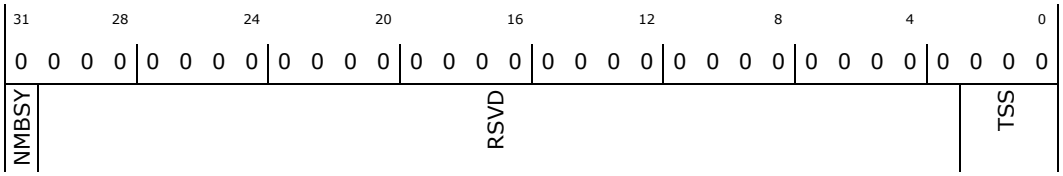
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**NMBSY:** Network Mode Busy 0 - No frame is currently active (in network mode only) 1 - SSP is in network mode and a frame is currently active
30:3	0x0 RO	**RSVD:** Reserved
2:0	0x0 RO	**TSS:** Time Slot Status Value indicates which time slot is currently active

9.10.11 SSP Audio Clock Divider (SSACD)—Offset 3Ch

The Enhanced SSP Audio Clock Divider registers are read-write registers that indicate which clock frequency is sent to the Enhanced SSP and to the SYSCLK pin. If SSCR0.SCR is not 0, then there is no guaranteed phase relationship between SYSCLK and SSPSCLK. The SSPSFRM Frame Synch Sampling Frequency is calculated by dividing the chosen PLL output clock frequency (SSACD.ACPS) by the chosen divider (SSACD.ACDS) which gives the SYSCLK frequency. The SYSCLK is then divided by 4 (or by 1) to get the SSPSCLK. The SSPSCLK is divided by the data size (EDSS, DSS values)

and by the number of time slots being used (SSCR0.FRDC value), if any, to give the SSPSFRM frequency. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

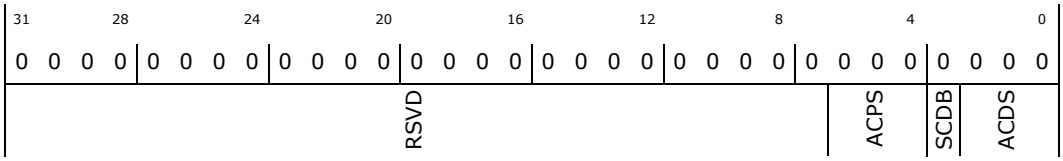
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**RSVD:** Reserved
6:4	0x0 RW	**ACPS:** Audio Clock PLL Select Value indicates which PLL output clock is sent to the clock divider in the clock unit 000: 5.622MHz, 001: 11.345MHz, 010: 12.235MHz, 011: 14.857MHz, 100: 32.842MHz, 101: 48.000MHz, 110, 111: Reserved
3	0x0 RW	**SCDB:** SYSCLK Divider Bypass 0 - SYSCLK is divided by 4 before being sent to SSP 1 - SYSCLK is not divided before being sent to SSP
2:0	0x0 RW	**ACDS:** Audio Clock Divider Select Value indicates which divider will be used by the clock unit to create the SYSCLK output pin. Clock divider value will be 2^ACDS, max ACDS = 5.

9.10.12 I2S Transmit FIFO (ITF)—Offset 40h

The I2S Transmit FIFO register is for writing the water mark for the I2S transmit FIFO and also for reading the number of entries in the I2S transmit FIFO

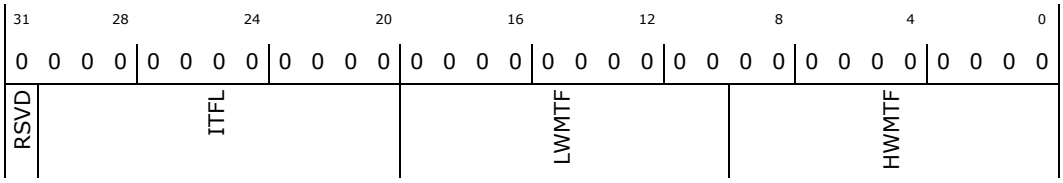
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RSVD:** Reserved
30:20	0x0 RO	**ITFL:** I2S Transmit FIFO Level Number of entries in I2S Transmit FIFO
19:10	0x0 RW	**LWMTF:** Low Water Mark Transmit FIFO.Set the low water mark of the I2S transmit FIFO.
9:0	0x0 RW	**HWMTF:** High Water Mark Transmit FIFO.Set the high water mark of the I2S transmit FIFO.

9.10.13 SPI Transmit FIFO (SITF)—Offset 44h

The SPI Transmit FIFO register is for writing the water mark for the SPI transmit FIFO and also for reading the number of entries in the SPI transmit FIFO

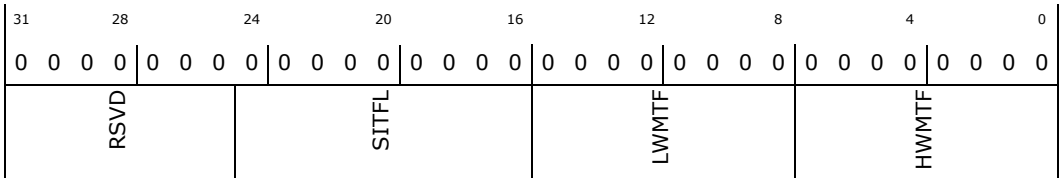
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**RSVD:** Reserved
24:16	0x0 RO	**SITFL:** SPI Transmit FIFO Level Number of entries in SPI Transmit FIFO.
15:8	0x0 RW	**LWMTF:** Low Water Mark Transmit FIFO. Set the low water mark of the SPI transmit FIFO.
7:0	0x0 RW	**HWMTF:** High Water Mark Transmit FIFO. Set the high water mark of the SPI transmit FIFO.

9.10.14 SPI Receive FIFO (SIRF)—Offset 48h

The SPI Receive FIFO register is for writing the water mark for the SPI receive FIFO and also for reading the number of entries in the SPI receive FIFO

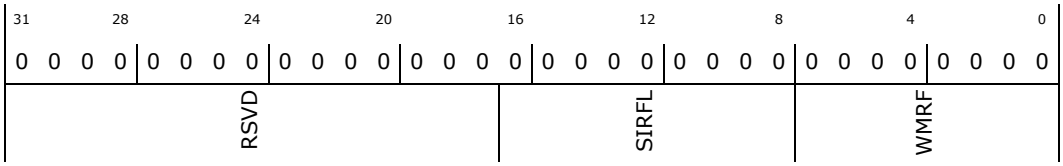
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RSVD:** Reserved
16:8	0x0 RO	**SIRFL:** SPI Receive FIFO Level Number of entries in SPI Receive FIFO.
7:0	0x0 RW	**WMRF:** Water Mark Receive FIFO. Set the water mark of the SPI receive FIFO.

9.10.15 private clock params (PRV_CLOCK_PARAMS)—Offset 400h

private clock params

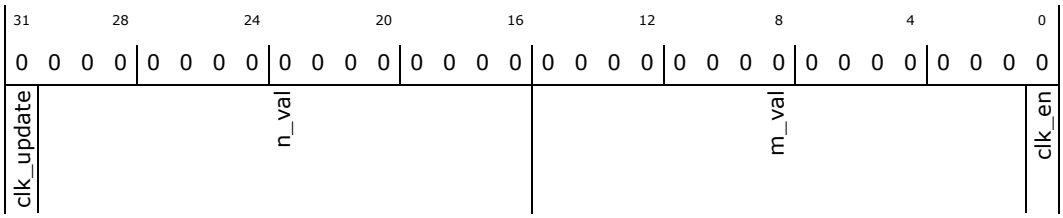
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 400h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**clk_update:** update the clock divider after seeting new m and n values
30:16	0x0 RW	**N_VAL (n_val):** n value for the m over n divider
15:1	0x0 RW	**M_VAL (m_val):** m value for the m over n divider
0	0x0 RW	**clk_en:** clk en of the m over n divider

9.10.16 software reset (RESETS)—Offset 404h

software reset

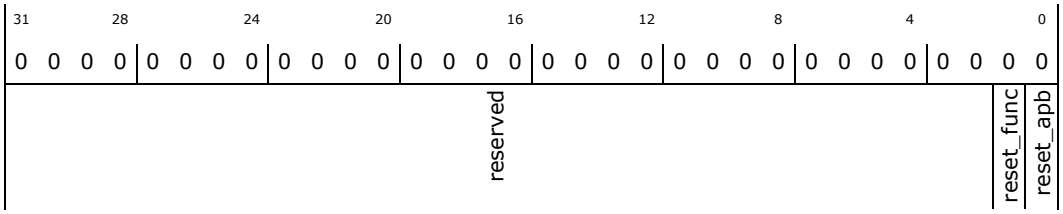
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 404h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (reserved):** Reserved
1	0x0 RW	**reset_func:** reset the func clock domain
0	0x0 RW	**reset_apb:** reset the apb domain

9.10.17 General purpose register (GENERAL)—Offset 408h

General purpose register

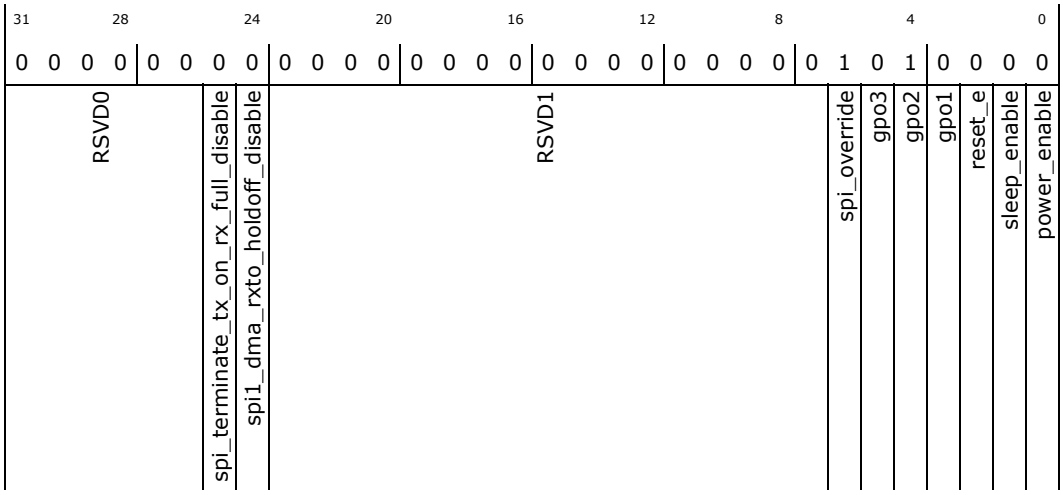
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 408h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

Default: 00000050h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**RSVD0:** Reserved
25	0x0 RW	**spi_terminate_tx_on_rx_full_disable:** disable terminate tx when rx full
24	0x0 RW	**spi1_dma_rxto_holdoff_disable:** disable dma hold off
23:7	0x0 RO	**RSVD1:** Reserved
6	0x1 RW	**spi_override:** not applicable
5	0x0 RW	**gpo3:** not applicable
4	0x1 RW	**gpo2:** not applicable
3	0x0 RW	**gpo1:** not applicable
2	0x0 RW	**reset_e:** not applicable
1	0x0 RW	**sleep_enable:** not applicable
0	0x0 RW	**power_enable:** not applicable

9.10.18 SPI misc register (SSP_REG)—Offset 40Ch

SPI misc register

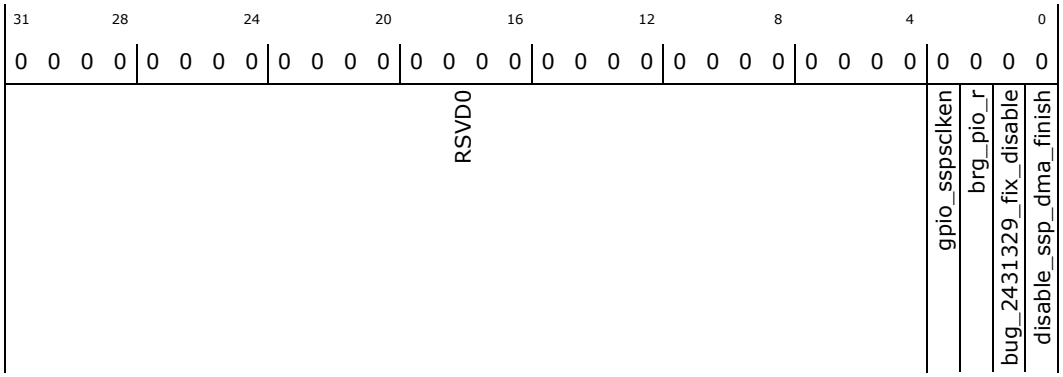
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RSVD0:** Reserved
3	0x0 RW	**gpio_sspsclken:** not applicable
2	0x0 RW	**brg_pio_r:** not applicable
1	0x0 RW	**bug_2431329_fix_disable:** not applicable
0	0x0 RW	**disable_ssp_dma_finish:** disable ssp dma finish

9.10.19 SPI chip select control register (SPI_CS_CTRL)—Offset 418h

SPI chip select control register

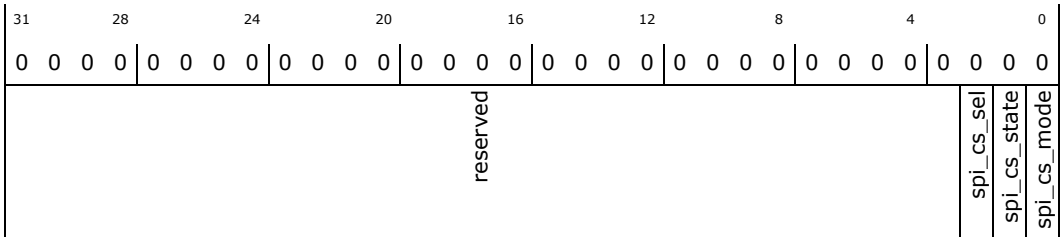
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 418h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RW	**reserved:** reserved
2	0x0 RW	**spi_cs_sel:** SW select bit to choose either CS0 or CS1 for spi
1	0x0 RW	**spi_cs_state:** SW override of CS line in SW mode for spi
0	0x0 RW	**spi_cs_mode:** selects HW mode or SW mode for chip select for spi

9.11 SIO I2C 0 PCI Configuration Registers

Table 74. Summary of SIO I2C 0 PCI Configuration Registers—0/24/1

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4285	00008086h
4–7h	4	"STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h" on page 4285	00100000h
8–Bh	4	"REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4287	00000000h
C–Fh	4	"CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4288	00800000h
10–13h	4	"BAR -Base Address Register (BAR)—Offset 10h" on page 4288	00000000h
14–17h	4	"BAR1 -Base Address Register1 (BAR1)—Offset 14h" on page 4289	00000000h
2C–2Fh	4	"SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4290	00000000h
30–33h	4	"EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4291	00000000h
34–37h	4	"CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4291	00000000h
3C–3Fh	4	"INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4292	00000100h
80–83h	4	"POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4292	00030001h
84–87h	4	"PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4293	00000008h
F8–FBh	4	"Manufacturers ID (MANID)—Offset F8h" on page 4294	00000000h

9.11.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

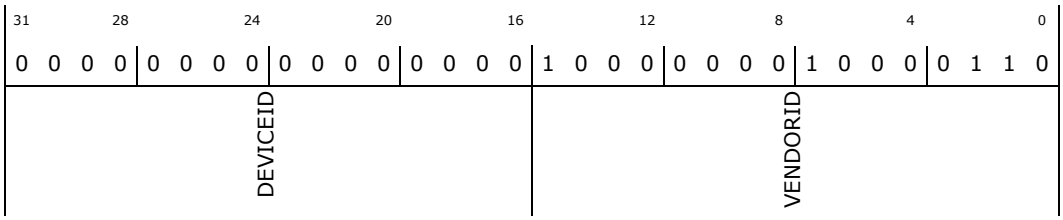
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**DEVICEID:** Device ID identifies the particular AHB/APB device. This is tied to a strap at the top level. Because of tool issues, the HTML files show this field as 0, but the following are the POR values for SoC: LPIO1 DMA: 0x2286 LPIO1 PWM1: 0x2288 LPIO1 PWM2: 0x2289 LPIO1 HSUART1: 0x228A LPIO1 HSUART2: 0x228C LPIO1 SPI1: 0x228E LPIO1 SPI2: 0x2290 LPIO1 SPI3: 0x22AC LPIO2 DMA: 0x22C0 LPIO2 I2C1: 0x22C1 LPIO2 I2C2: 0x22C2 LPIO2 I2C3: 0x22C3 LPIO2 I2C4: 0x22C4 LPIO2 I2C5: 0x22C5 LPIO2 I2C6: 0x22C6 LPIO2 I2C7: 0x22C7 For the final word on this, please see Ray Ng's SoC RevID and DevID HAS on Infofactory: https://ifcollaborate.intel.com/IFC/getdoc.aspx?docbase=InfoFactoryKBandchronid=09005ffd80e84b43andver=CURRENTandqepop=false
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap the top level.

9.11.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

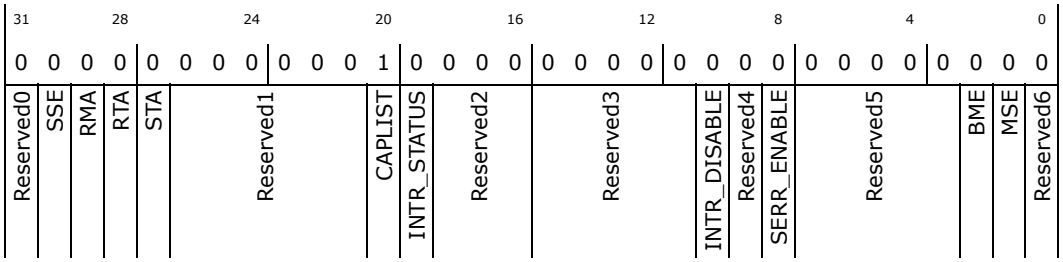
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved0:** Reserved
30	0x0 RW/1C	**SSE:** This bit is set when a device sends an DO_SERR message, and the SERR# Enable bit in the Command register is 1
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric PortReceived Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27	0x0 RW/1C	**STA:** The Bridge sets this bit whenever it responds to a transaction with CA abort. If the SERR# Enable bit is set, the Bridge sets the Signaled System Error bit and sends an DO_SERR message on the IOSF Sideband.
26:21	0x0 RO	**Reserved1:** Reserved
20	0x1 RO	**CAPLIST:** Capabilities List: Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt .i.e Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.. Reset value of this bit is 0.
9	0x0 RO	**Reserved4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: If both SERR# Enable and the Unsupported Request Reporting Enable (URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0x0 RO	**Reserved6:** Reserved

9.11.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

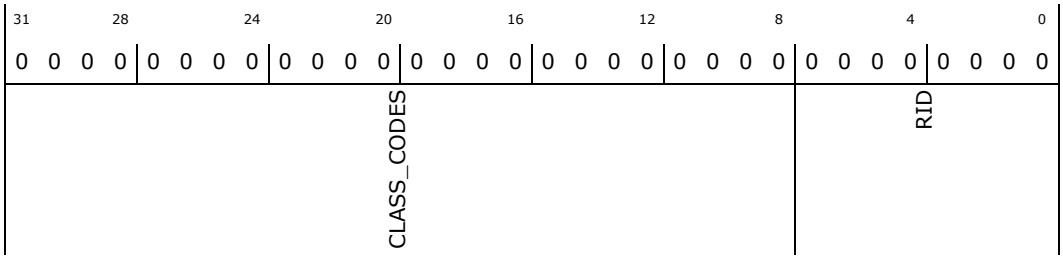
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

9.11.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

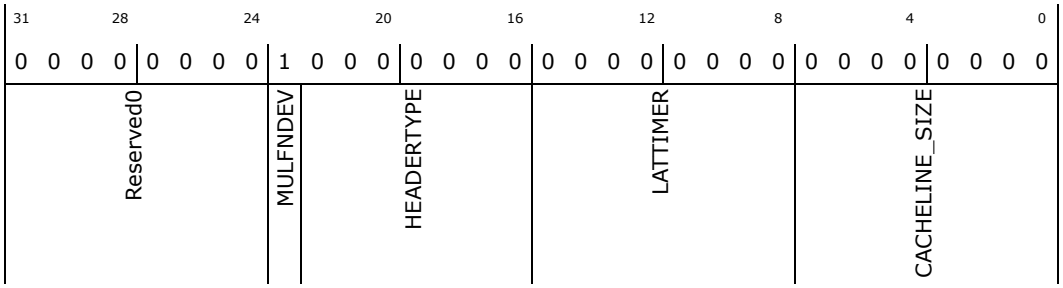
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + Ch

Default: 00800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x1 RO	**MULFNDEV:** Multi Function Device: This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. Value of 1 indicates multifunction device value of 0 indicates single function device
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	0x0 RO	**LATTIMER:** Latency Timer: Doesn.t apply to PCI Express. Hardwired to 00h.
7:0	0x0 RW	**CACHELINE_SIZE:** Cache Line Size: Doesn.t apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

9.11.5 BAR -Base Address Register (BAR)—Offset 10h

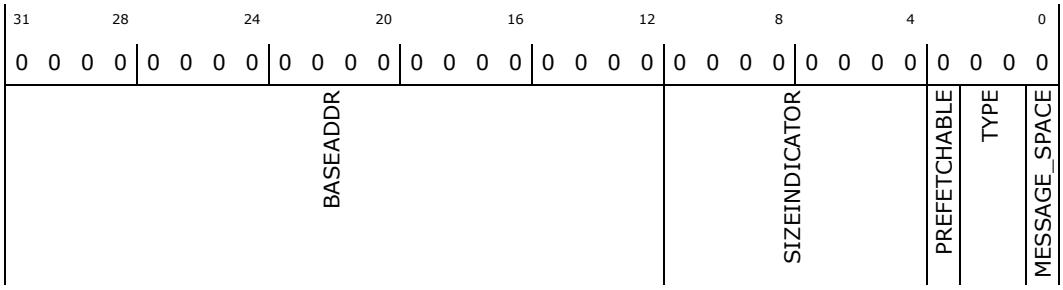
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the AHB device memory space. Taken from Strap values as 1's. Please note that for DMA this field goes from [31:14], or 16kbyte, and the SIZEINDICATOR field goes from [13:4].
11:4	0x0 RO	**SIZEINDICATOR:** Size Indicator Read Only: Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0x0 RO	**TYPE:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.11.6 BAR1 -Base Address Register1 (BAR1)—Offset 14h

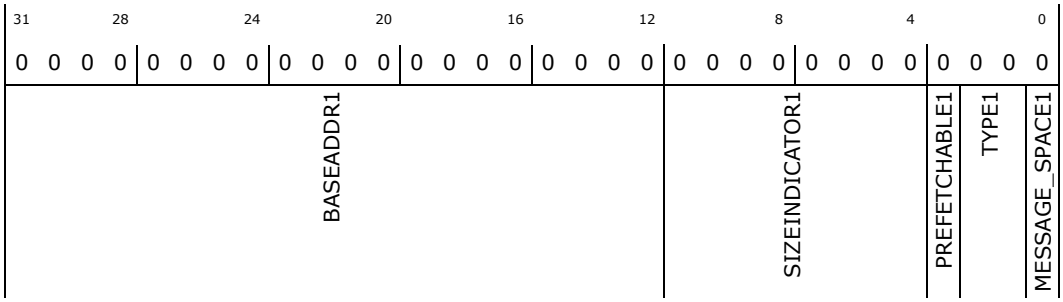
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	0x0 RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not
2:1	0x0 RO	**TYPE1:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.11.7 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

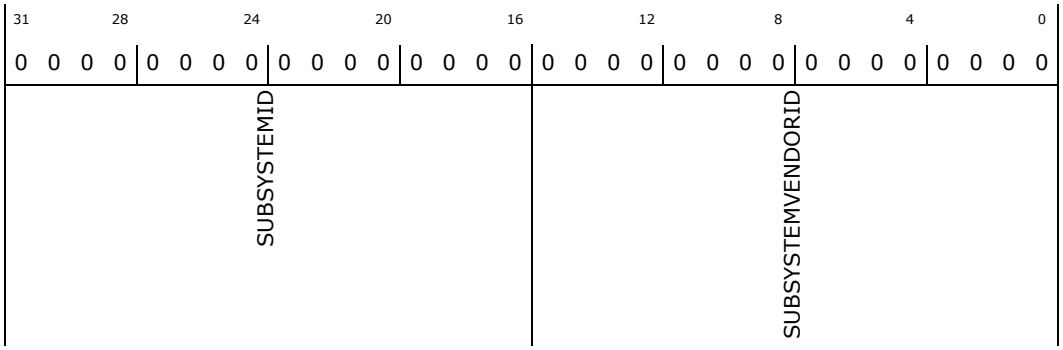
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

9.11.8 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

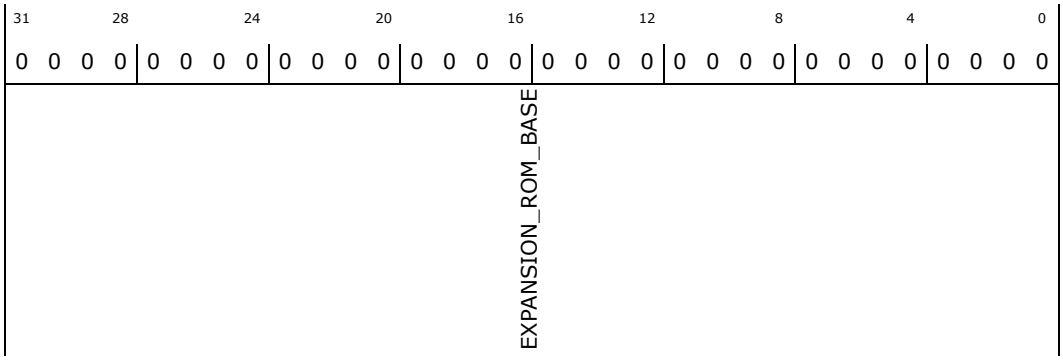
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** A value of all zeros indicates no support for expansion ROM.

9.11.9 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

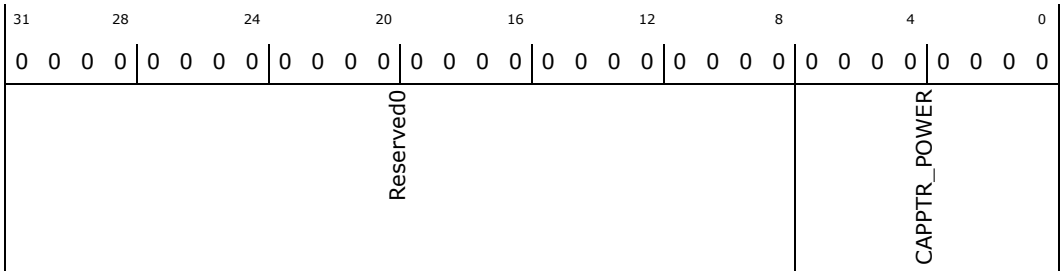
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x0 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

9.11.10 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

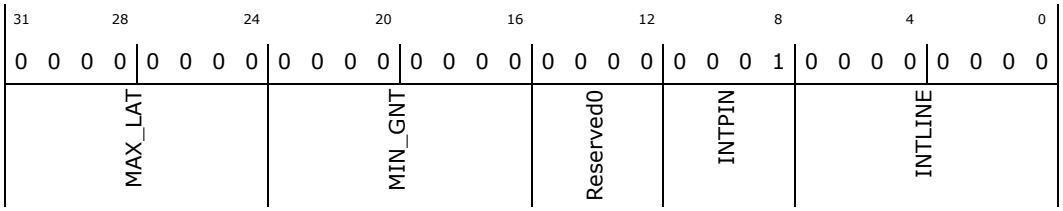
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

9.11.11 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

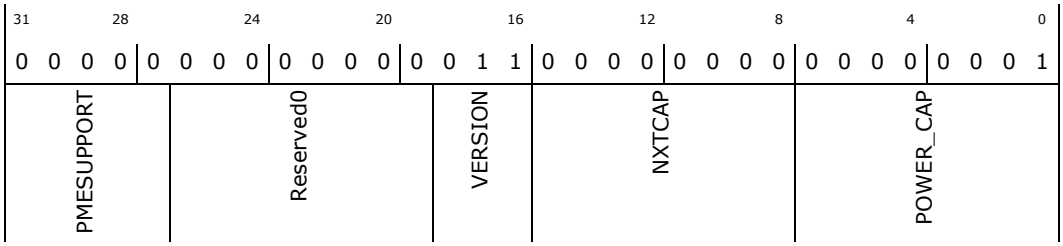
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** PME_Support - This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

9.11.12 PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

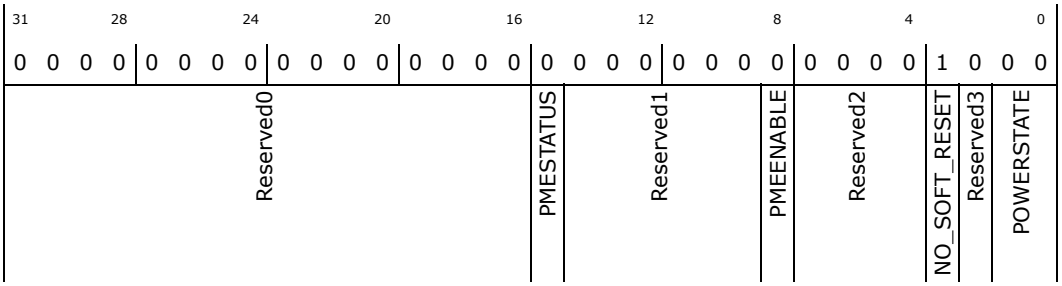
PMECTRLSTATUS - PME Control and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

9.11.13 Manufacturers ID (MANID)—Offset F8h

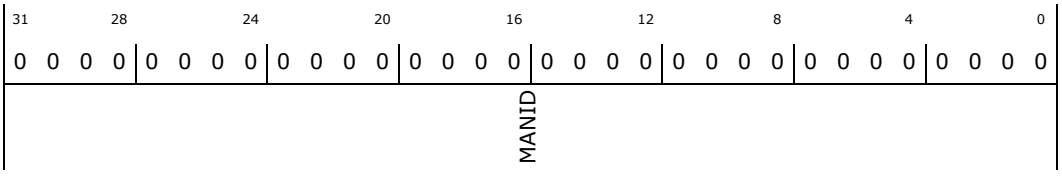
Manufacturers ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:1] + F8h

Default: 00000000h

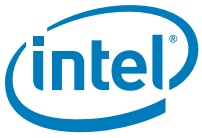


Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: This register is brought out as straps to the top level.

9.12 SIO I2C 0 Memory Mapped I/O Registers

Table 75. Summary of SIO I2C 0 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 4299	0000007Fh
4–7h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 4300	00001055h
8–Bh	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 4301	00000055h
C–Fh	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 4301	00000001h
10–13h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 4302	00000000h
14–17h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 4303	00000190h
18–1Bh	4	"Standard Speed I2C Clock SCL Low Count Register. (IC_SS_SCL_LCNT)—Offset 18h" on page 4304	000001D6h
1C–1Fh	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 4304	0000003Ch
20–23h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 4305	00000082h
24–27h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 4306	0000000Ch
28–2Bh	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 4306	00000020h
2C–2Fh	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 4307	00000000h
30–33h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 4308	000008FFh
34–37h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 4309	00000000h
38–3Bh	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 4310	00000010h
3C–3Fh	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 4311	00000010h
40–43h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 4312	00000000h
44–47h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 4312	00000000h
48–4Bh	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 4313	00000000h
4C–4Fh	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 4314	00000000h
50–53h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 4314	00000000h
54–57h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 4315	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
58–5Bh	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 4315	00000000h
5C–5Fh	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 4316	00000000h
60–63h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 4317	00000000h
64–67h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 4317	00000000h
68–6Bh	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 4318	00000000h
6C–6Fh	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 4318	00000000h
70–73h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 4319	00000006h
74–77h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 4320	00000000h
78–7Bh	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 4320	00000000h
7C–7Fh	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 4321	00000001h
80–83h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 4322	00000000h
84–87h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 4323	00000000h
88–8Bh	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 4324	00000000h
8C–8Fh	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 4324	00000000h
90–93h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 4325	00000000h
94–97h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 4326	00000064h
98–9Bh	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 4326	00000001h
9C–9Fh	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 4327	00000000h
A0–A3h	4	"SS/FS Mode Spike Length Register (IC_FS_SPKLEN)—Offset A0h" on page 4328	00000005h
A4–A7h	4	"HS Mode Spike Length Register (IC_HS_SPKLEN)—Offset A4h" on page 4328	00000002h
F4–F7h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 4329	00FFFFEEh
F8–FBh	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 4330	3131352Ah
FC–FFh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 4331	44570140h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
800–803h	4	"Clock params register (CLOCK_PARAMS)—Offset 800h" on page 4331	00000000h
804–807h	4	"software reset (RESETS)—Offset 804h" on page 4332	00000000h
808–80Bh	4	"General purpose register (GENERAL)—Offset 808h" on page 4332	55000000h
818–81Bh	4	"TX transaction counter (I2C_ACK_COUNT)—Offset 818h" on page 4334	00000000h
820–823h	4	"TX transaction complete interrupt status register (I2C_TX_COMPLETE_INTR_STAT)—Offset 820h" on page 4335	00000000h
824–827h	4	"TX transaction complete interrupt clear register (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 4335	00000000h

9.12.1 I2C Control Register (IC_CON)—Offset 0h

I2C Control Register

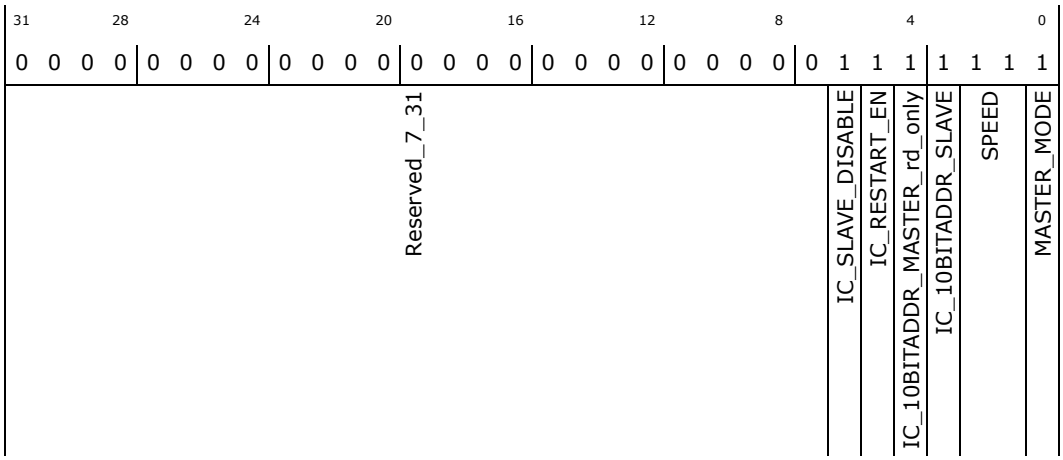
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 0000007Fh



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RW	**Reserved_7_31:** Reserved
6	0x1 RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	0x1 RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master.When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: Sending a START BYTE. Performing any high-speed mode operation. Performing direction changes in combined format mode. Performing a read operation with a 10-bit address
4	0x1 RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register
3	0x1 RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0x3 RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	0x1 RW	**MASTER_MODE:** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

9.12.2 I2C Target Address Register (IC_TAR)—Offset 4h

I2C Target Address Register

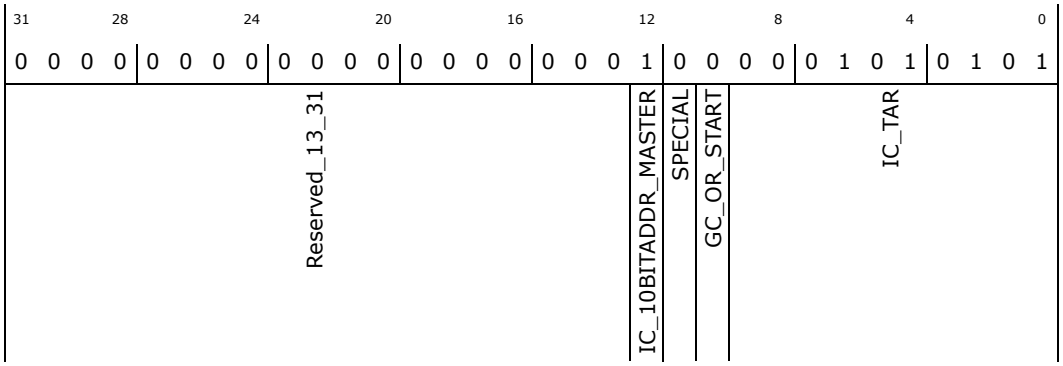
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00001055h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Reserved_13_31:** Reserved
12	0x1 RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master. This bit exists in this register only if the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 1
11	0x0 RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. 0: ignore bit 10 GC_OR_START and use IC_TAR normally. 1: perform special I2C command as specified in GC_OR_START bit
10	0x0 RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.

Bit Range	Default & Access	Field Name (ID): Description
9:0	0x55 RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

9.12.3 I2C Slave Address Register (IC_SAR)—Offset 8h

I2C Slave Address Register

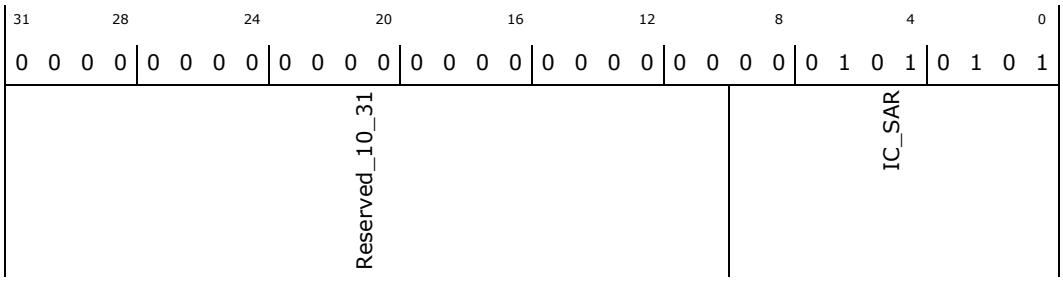
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000055h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**Reserved_10_31:** Reserved
9:0	0x55 RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.12.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

I2C High Speed Master Mode Code Address Register

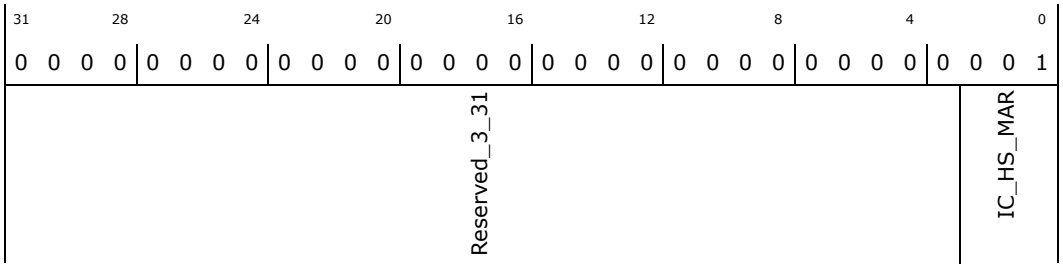
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved_3_31:** Reserved
2:0	0x1 RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.12.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

I2C Rx/Tx Data Buffer and Command Register; this is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO

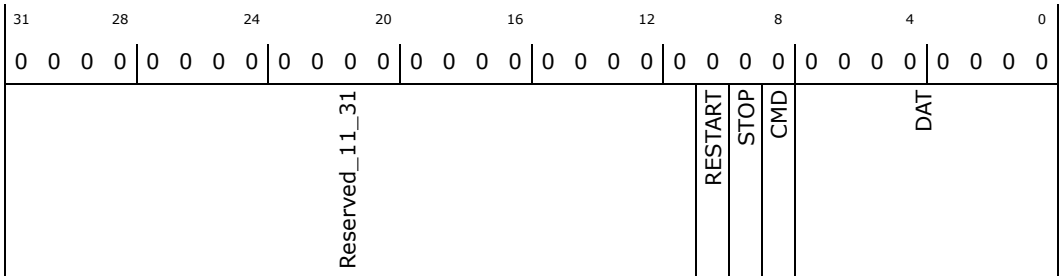
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:11	0x0 RW	**Reserved_11_31:** Reserved
10	0x0 RW	**RESTART:** RESTART
9	0x0 RW	**STOP:** STOP
8	0x0 RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It controls only the direction when it acts as a master. 1 = Read. 0 = Write
7:0	0x0 RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. However, when you read this register, these bits return the value of data received on the DW_apb_i2c interface.

9.12.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

Standard Speed I2C Clock SCL High Count Register.

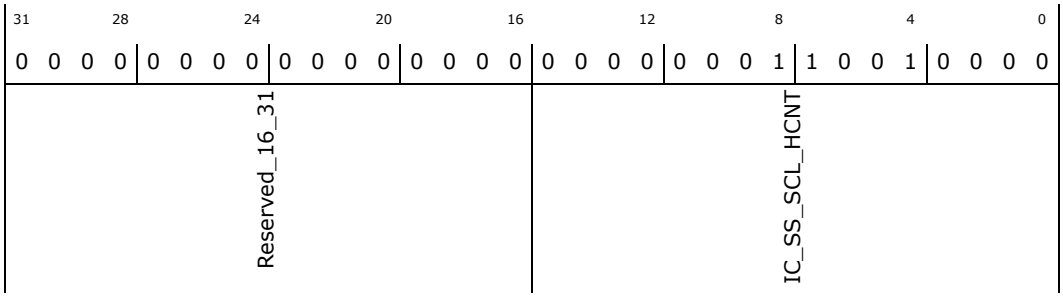
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000190h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x190 RW	**IC_SS_SCL_HCNT:** Standard Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.12.7 Standard Speed I2C Clock SCL Low Count Register. (IC_SS_SCL_LCNT)—Offset 18h

Standard Speed I2C Clock SCL Low Count Register.

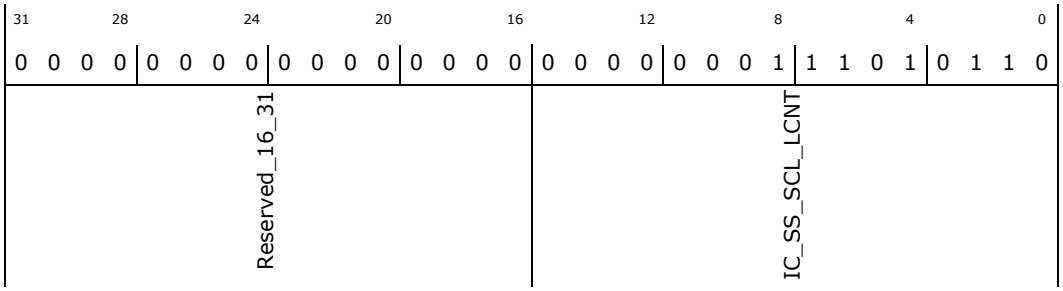
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 000001D6h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x1d6 RW	**IC_SS_SCL_LCNT:** Standard Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.12.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

Fast Speed I2C Clock SCL High Count Register

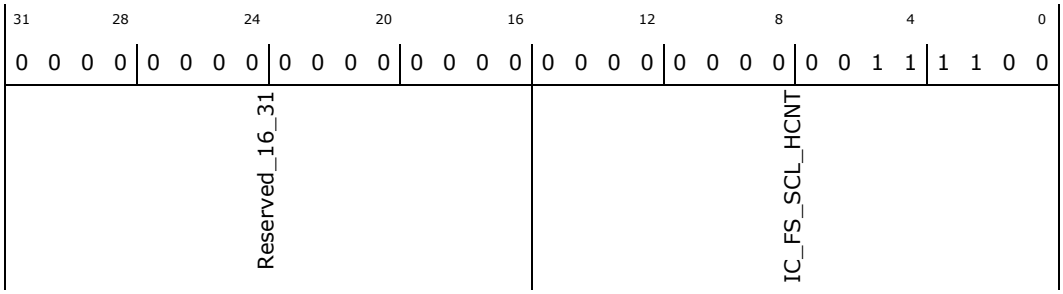
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 0000003Ch



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x3c RW	**IC_FS_SCL_HCNT:** Fast Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.12.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

Fast Speed I2C Clock SCL Low Count Register

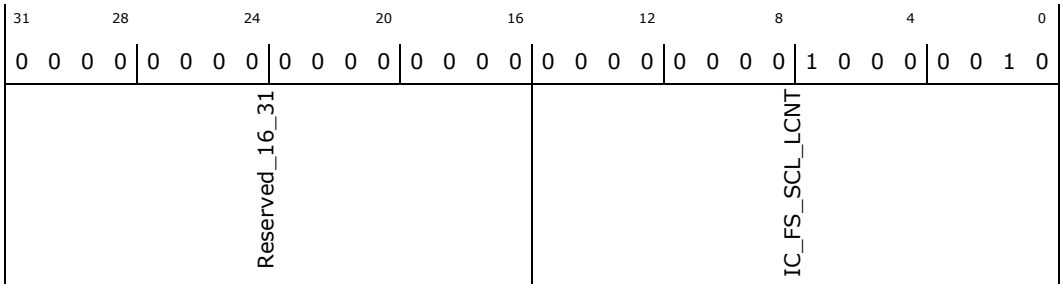
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000082h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x82 RW	**IC_FS_SCL_LCNT:** Fast Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.12.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

High Speed I2C Clock SCL High Count Register

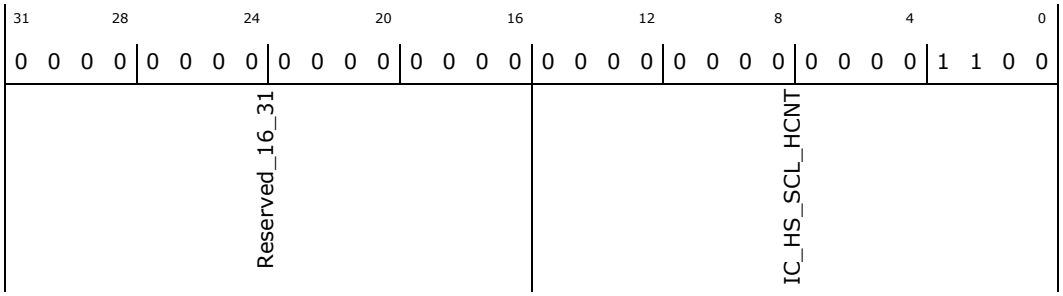
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 0000000Ch



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0xc RW	**IC_HS_SCL_HCNT:** High Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.12.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

High Speed I2C Clock SCL Low Count Register

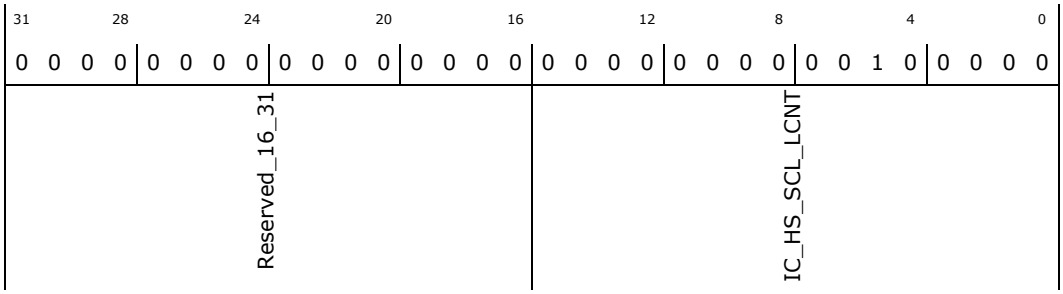
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000020h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x20 RW	**IC_HS_SCL_LCNT:** High Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.12.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

I2C Interrupt Status Register

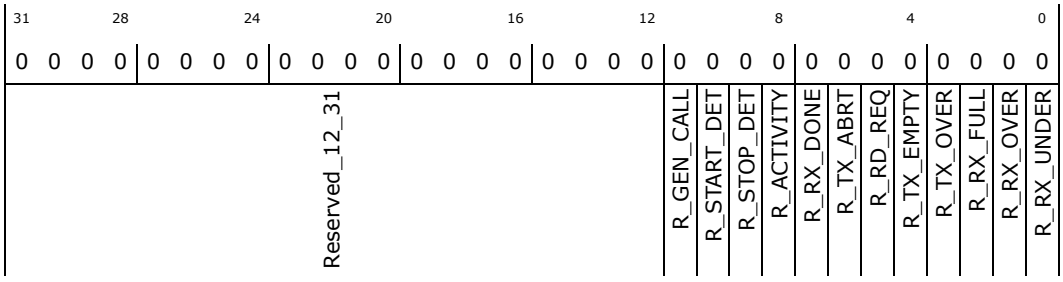
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x0 RO	**R_GEN_CALL:** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0x0 RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0x0 RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0x0 RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0x0 RO	**R_TX_ABRT:** This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0x0 RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.
4	0x0 RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0x0 RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0x0 RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0x0 RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0x0 RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

9.12.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

I2C Interrupt Mask Register

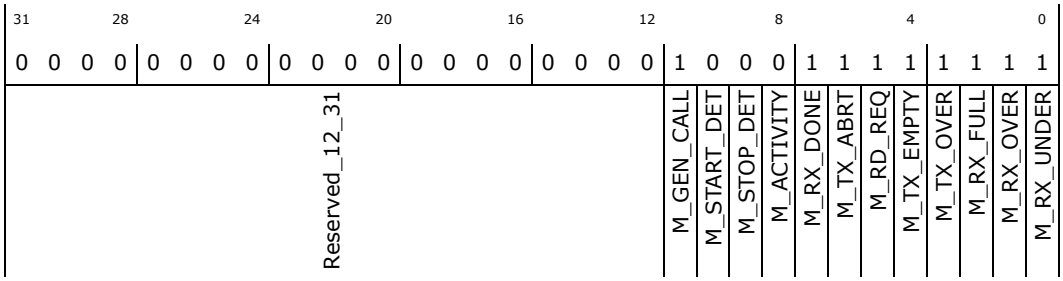
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 000008FFh



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x1 RW	**M_GEN_CALL:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
10	0x0 RW	**M_START_DET:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
9	0x0 RW	**M_STOP_DET:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
8	0x0 RW	**M_ACTIVITY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
7	0x1 RW	**M_RX_DONE:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
6	0x1 RW	**M_TX_ABRT:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
5	0x1 RW	**M_RD_REQ:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
4	0x1 RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
3	0x1 RW	**M_TX_OVER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
2	0x1 RW	**M_RX_FULL:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
1	0x1 RW	**M_RX_OVER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
0	0x1 RW	**M_RX_UNDER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.

9.12.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

I2C Raw Interrupt Status Register

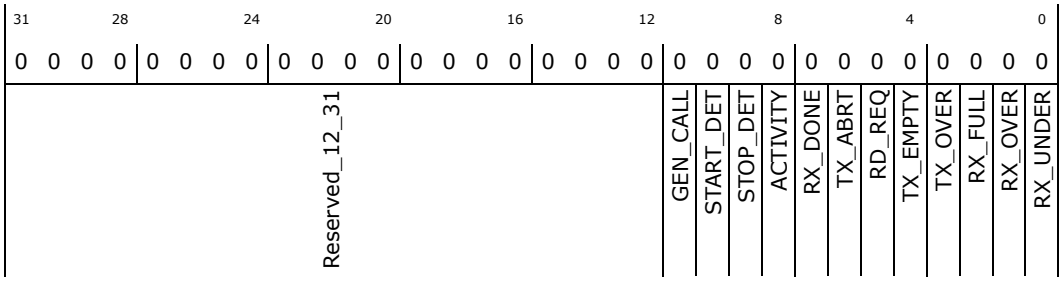
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x0 RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT
10	0x0 RO	**START_DET:** Same as in reg_IC_INTR_STAT
9	0x0 RO	**STOP_DET:** Same as in reg_IC_INTR_STAT
8	0x0 RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT
7	0x0 RO	**RX_DONE:** Same as in reg_IC_INTR_STAT
6	0x0 RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT
5	0x0 RO	**RD_REQ:** Same as in reg_IC_INTR_STAT
4	0x0 RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT
3	0x0 RO	**TX_OVER:** Same as in reg_IC_INTR_STAT
2	0x0 RO	**RX_FULL:** Same as in reg_IC_INTR_STAT
1	0x0 RO	**RX_OVER:** Same as in reg_IC_INTR_STAT
0	0x0 RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT

9.12.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

I2C Receive FIFO Threshold Register

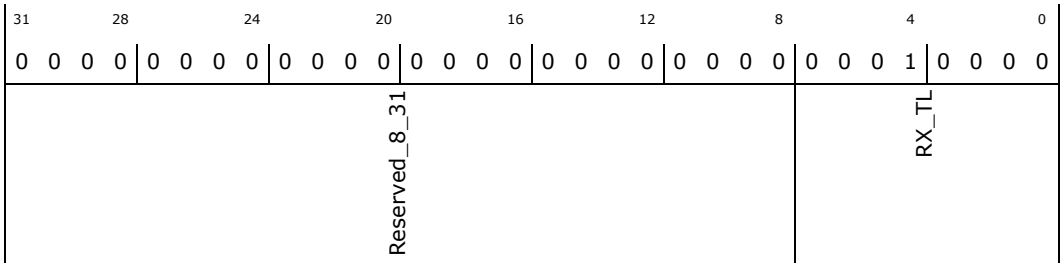
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x10 RW	**RX_TL:** Receive FIFO Threshold Level. The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

9.12.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

I2C Transmit FIFO Threshold Register

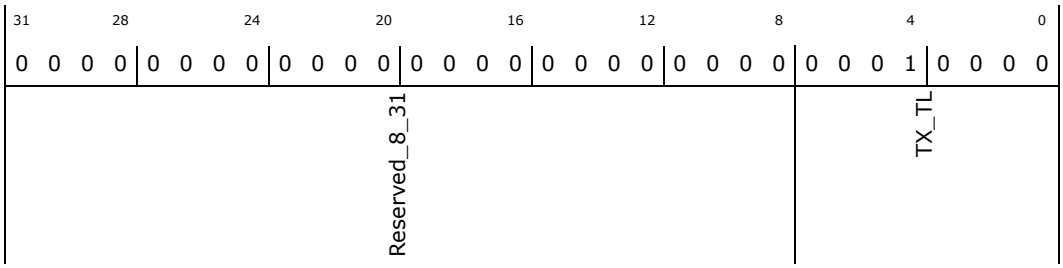
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x10 RW	**TX_TL:** Transmit FIFO Threshold Level. Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

9.12.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

Clear Combined and Individual Interrupt Register

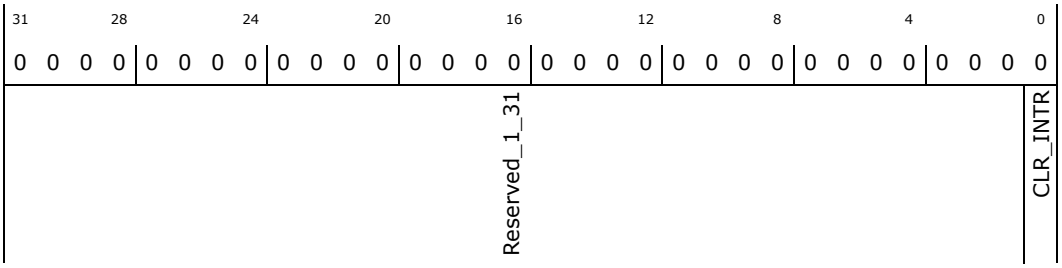
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

9.12.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

Clear RX_UNDER Interrupt Register

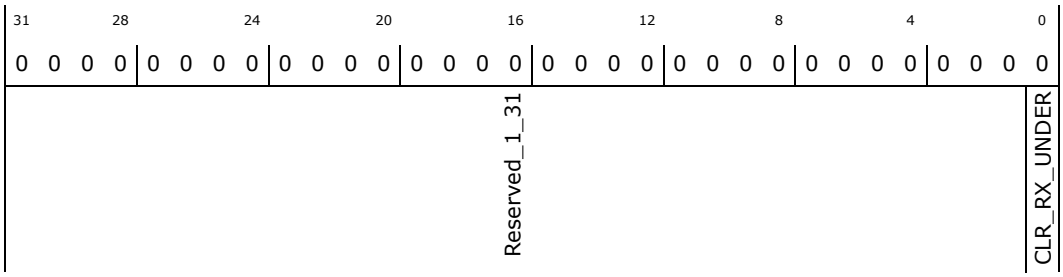
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

9.12.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

Clear RX_OVER Interrupt Register

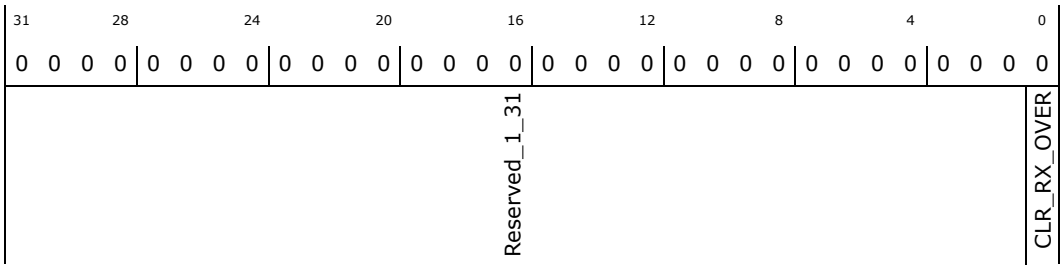
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

9.12.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

Clear TX_OVER Interrupt Register

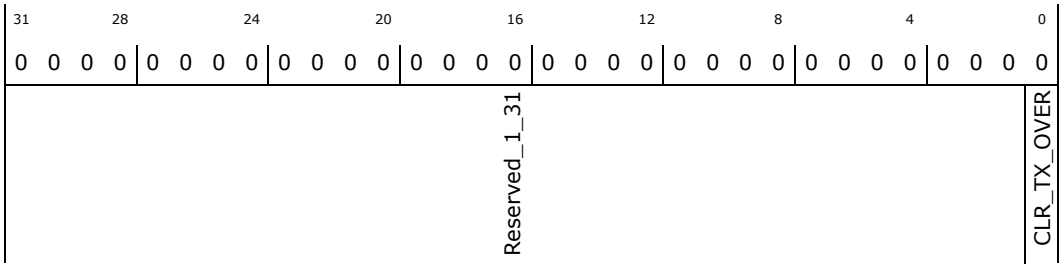
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

9.12.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

Clear RD_REQ Interrupt Register

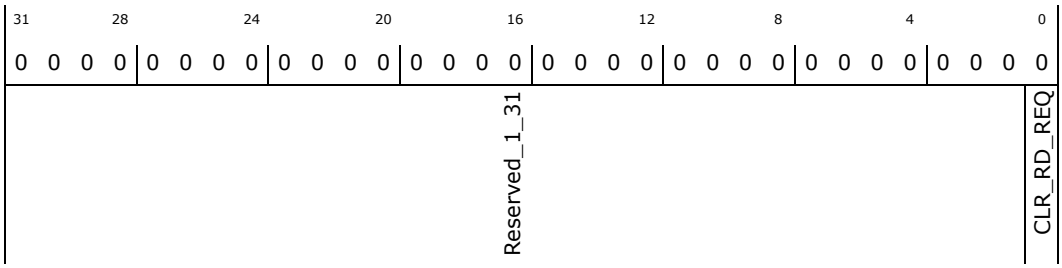
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

9.12.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

Clear TX_ABRT Interrupt Register

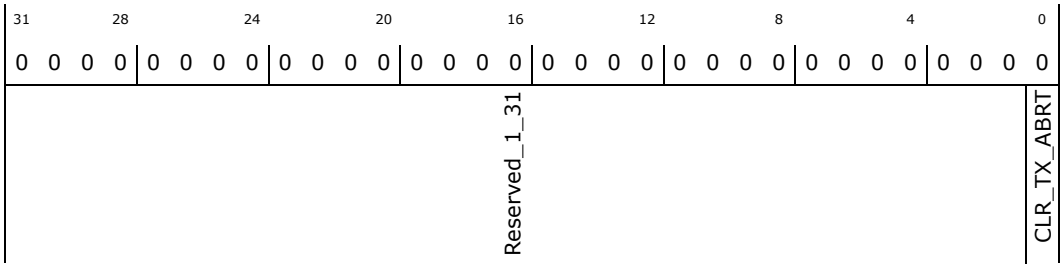
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

9.12.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

Clear RX_DONE Interrupt Register

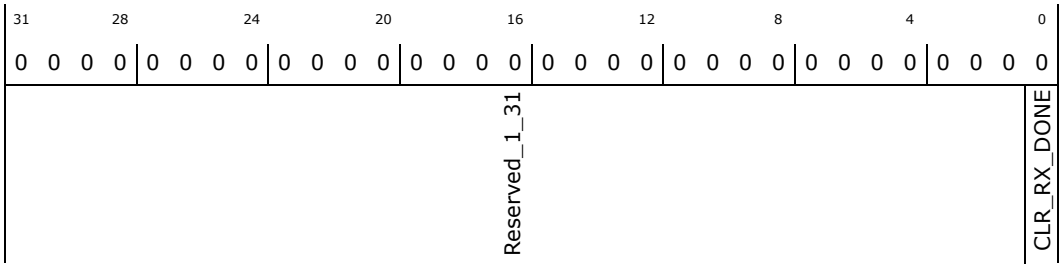
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

9.12.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

Clear ACTIVITY Interrupt Register

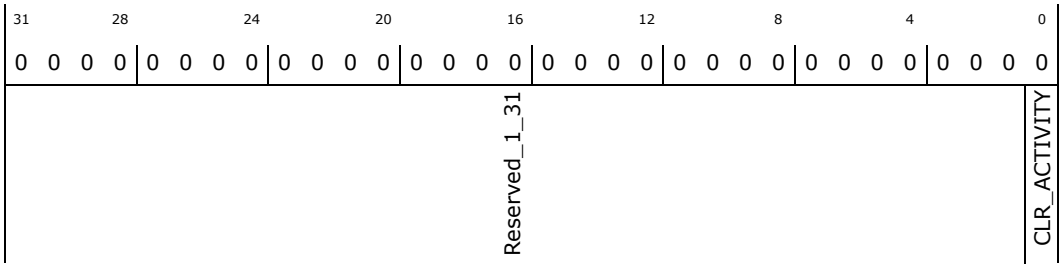
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

9.12.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

Clear STOP_DET Interrupt Register

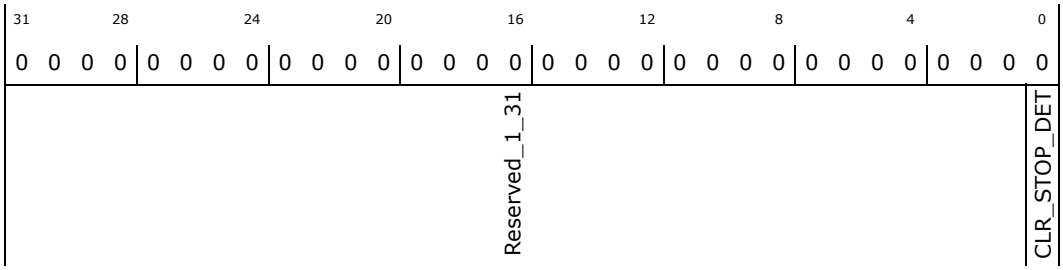
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

9.12.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

Clear START_DET Interrupt Register

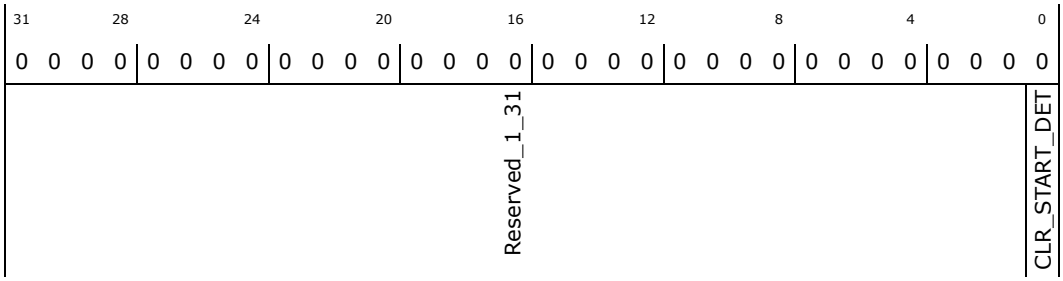
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

9.12.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

Clear GEN_CALL Interrupt Register

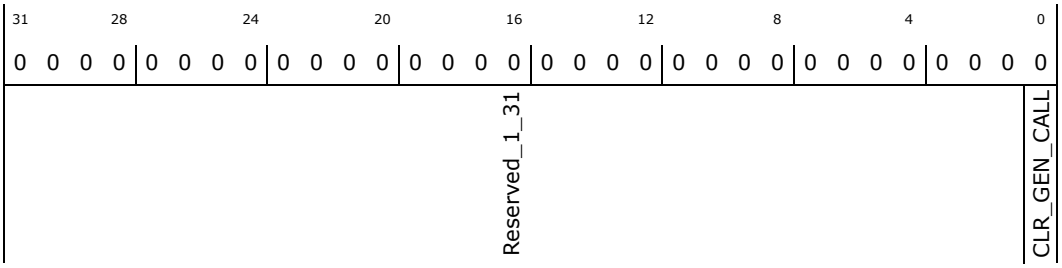
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

9.12.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

I2C Enable Register

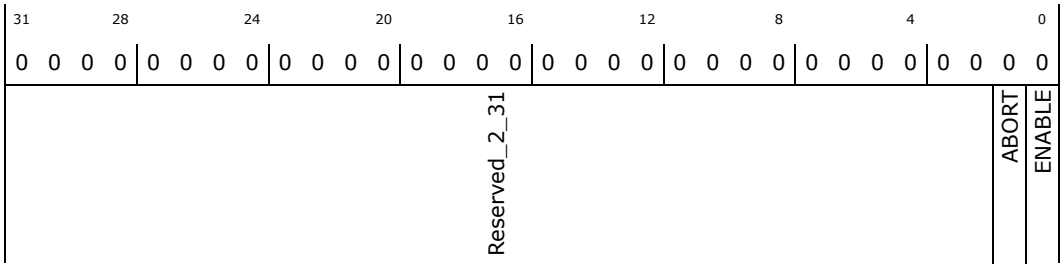
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved_2_31:** Reserved
1	0x0 WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.
0	0x0 RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) 1: Enables DW_apb_i2c

9.12.29 I2C Status Register (IC_STATUS)—Offset 70h

I2C Status Register

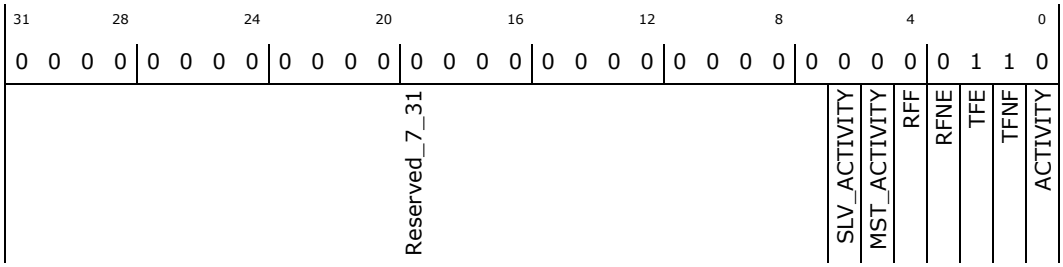
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000006h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RW	**Reserved_7_31:** Reserved
6	0x0 RO	**SLV_ACTIVITY:** Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0x0 RO	**MST_ACTIVITY:** Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RO	**RFF:** Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0x0 RO	**RFNE:** Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.
2	0x1 RO	**TFE:** Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	0x1 RO	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0x0 RO	**ACTIVITY:** I2C Activity Status

9.12.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

I2C Transmit FIFO Level Register

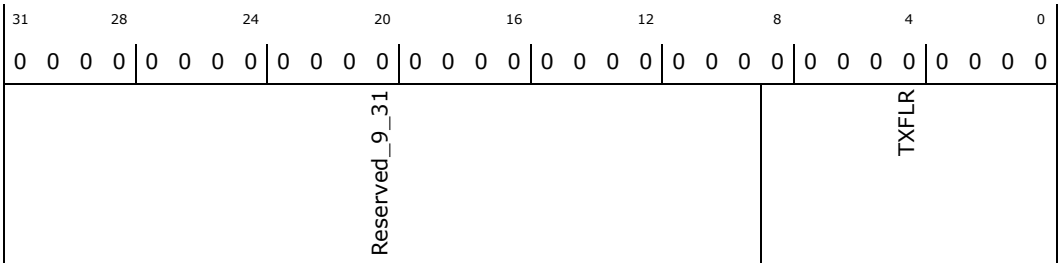
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved_9_31:** Reserved
8:0	0x0 RO	**TXFLR:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

9.12.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

I2C Receive FIFO Level Register

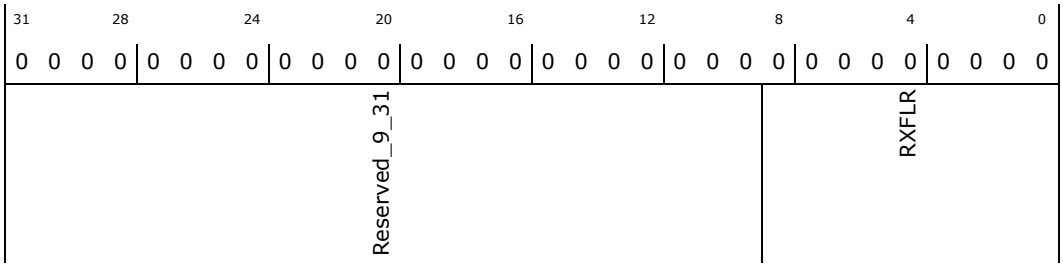
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved_9_31:** Reserved
8:0	0x0 RO	**RXFLR:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

9.12.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

I2C SDA Hold Time Length Register

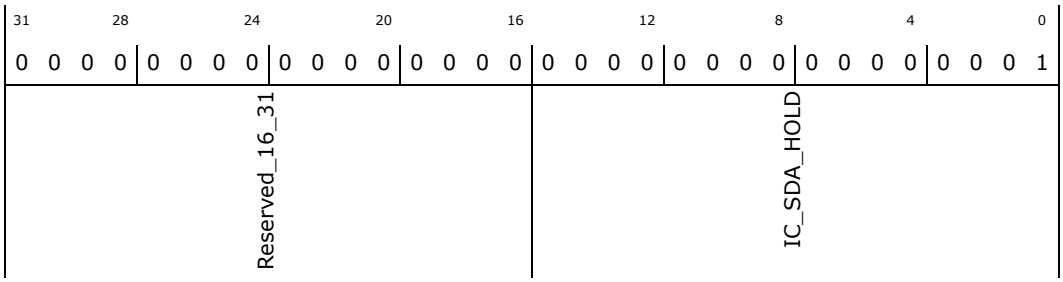
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x1 RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

9.12.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

I2C Transmit Abort Source Register

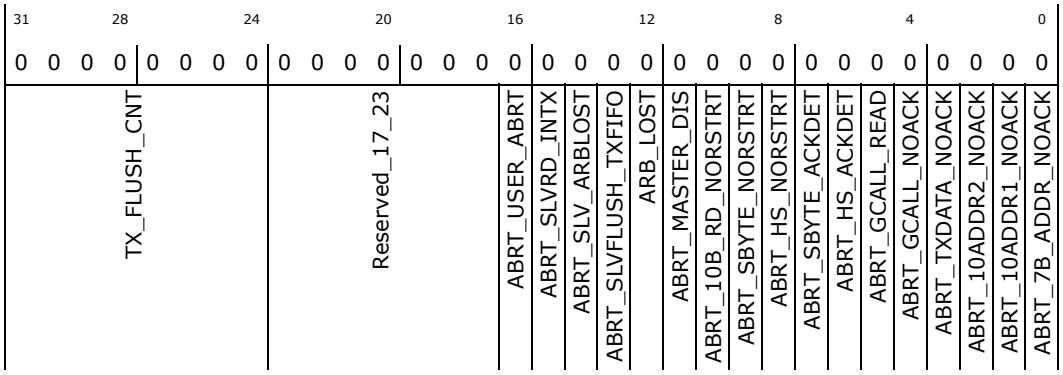
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0x0 RW	**Reserved_17_23:** Reserved
16	0x0 RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0x0 RO	**ABRT_SLVRD_INTX:** 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0x0 RO	**ABRT_SLV_ARBLOST:** 1: Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0x0 RO	**ABRT_SLVFLUSH_TXFIFO:** 1: Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0x0 RO	**ARB_LOST:** 1: Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0x0 RO	**ABRT_MASTER_DIS:** 1: User tries to initiate a Master operation with the Master mode disabled.
10	0x0 RO	**ABRT_10B_RD_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RO	**ABRT_SBYTE_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0x0 RO	**ABRT_HS_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0x0 RO	**ABRT_SBYTE_ACKDET:** 1: Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
6	0x0 RO	**ABRT_HS_ACKDET:** 1: Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
5	0x0 RO	**ABRT_GCALL_READ:** 1: DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0x0 RO	**ABRT_GCALL_NOACK:** 1: DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0x0 RO	**ABRT_TXDATA_NOACK:** 1: This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0x0 RO	**ABRT_10ADDR2_NOACK:** 1: Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0x0 RO	**ABRT_10ADDR1_NOACK:** 1: Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0x0 RO	**ABRT_7B_ADDR_NOACK:** 1: Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

9.12.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

Generate Slave Data NACK Register

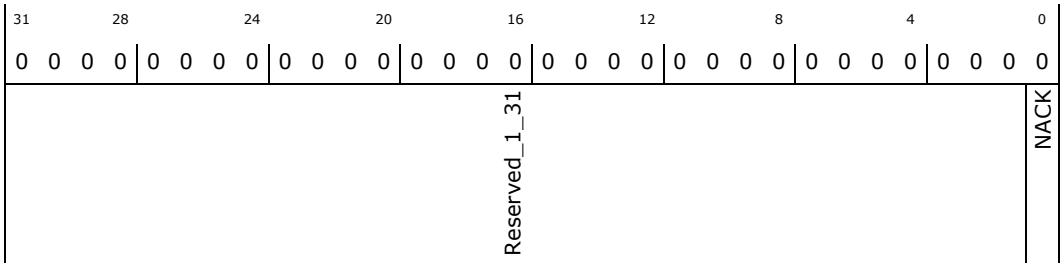
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RW	**NACK:** Generate NACK. This NACK generation only occurs when DW_apb_i2c is a slavereceiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. 1 = generate NACK after data byte received 0 = generate NACK/ACK normally

9.12.35 DMA Control Register (IC_DMA_CR)—Offset 88h

DMA Control Register

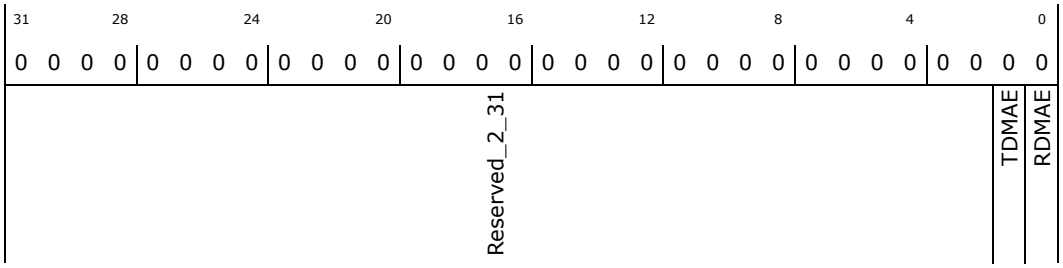
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved_2_31:** Reserved
1	0x0 RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel. 0 = Transmit DMA disabled 1 = Transmit DMA enabled
0	0x0 RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. 0 = Receive DMA disabled 1 = Receive DMA enabled

9.12.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

DMA Transmit Data Level Register

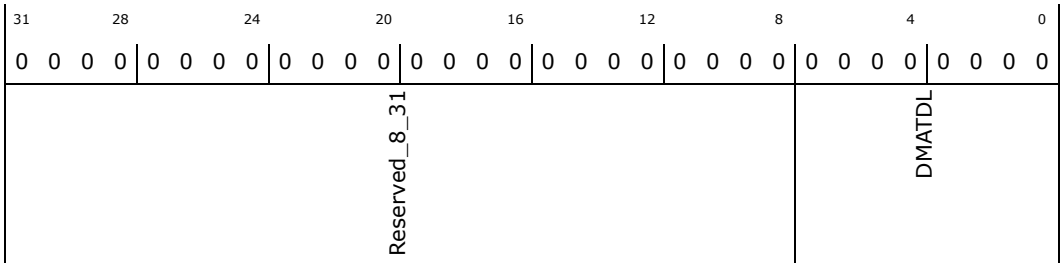
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x0 RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

9.12.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

I2C Receive Data Level Register

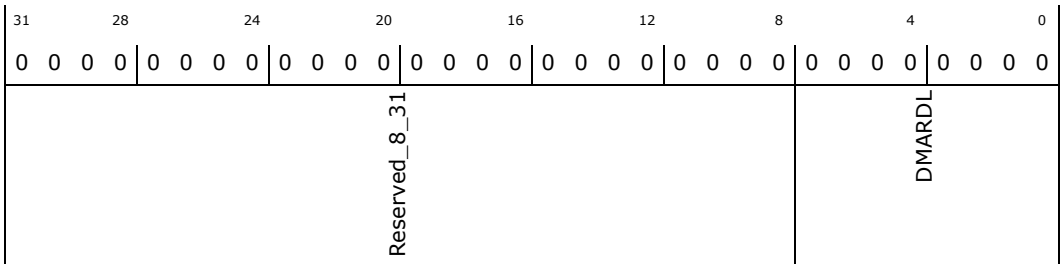
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x0 RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

9.12.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

I2C SDA Setup Register

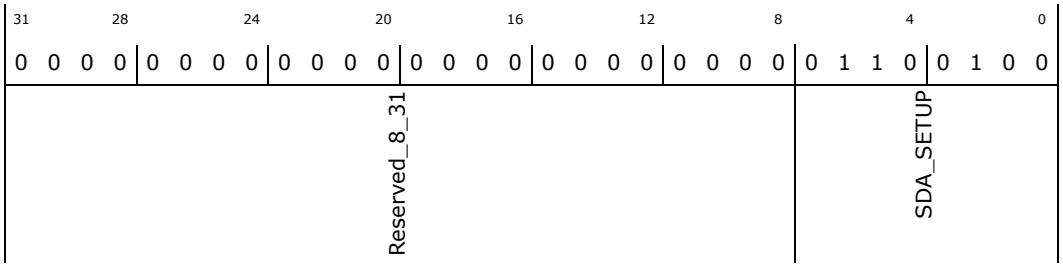
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000064h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x64 RW	**SDA_SETUP:** SDA Setup. It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

9.12.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

I2C ACK General Call Register

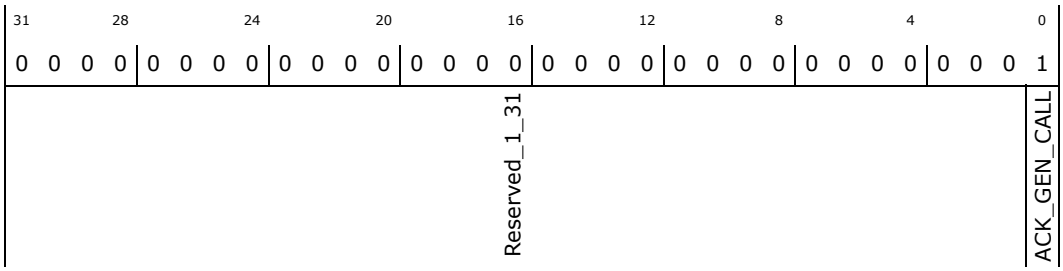
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x1 RW	**ACK_GEN_CALL:** ACK General Call. When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

9.12.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

I2C Enable Status Register

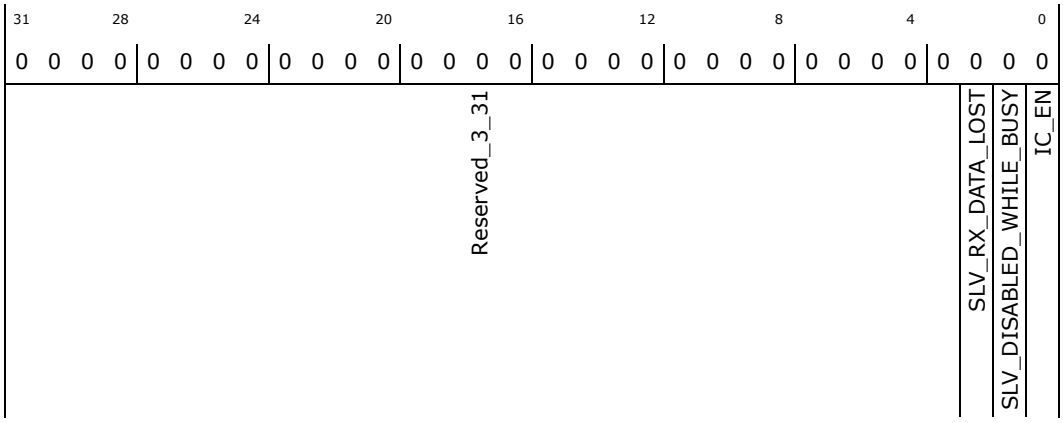
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved_3_31:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0x0 RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0x0 RO	**IC_EN:** ic_en Status. This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

9.12.41 SS/FS Mode Spike Length Register (IC_FS_SPKLEN)—Offset A0h

SS/FS Mode Spike Length Register

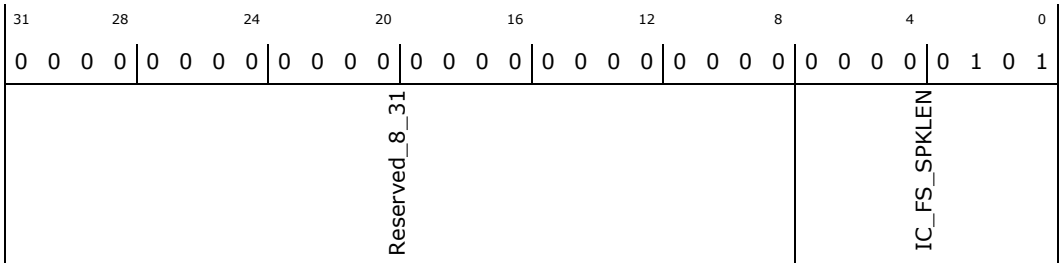
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000005h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x5 RW	**IC_FS_SPKLEN:** Maximum length (in ic_clk cycles) of suppressed spikes in SS and FS modes

9.12.42 HS Mode Spike Length Register (IC_HS_SPKLEN)—Offset A4h

HS Mode Spike Length Register

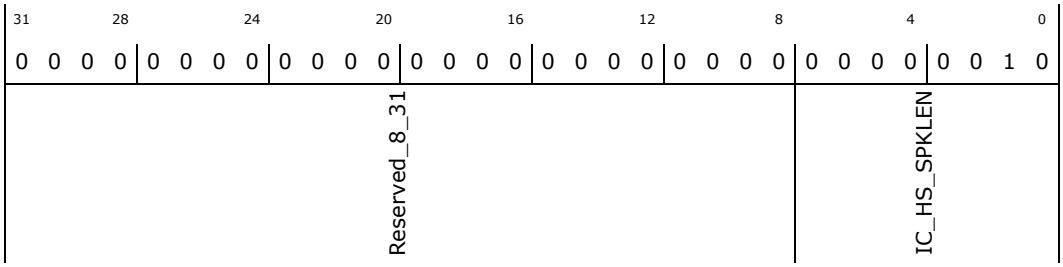
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x2 RW	**IC_HS_SPKLEN:** Maximum length (in ic_clk cycles) of suppressed spikes in HS mode

9.12.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

Component Parameter Register 1

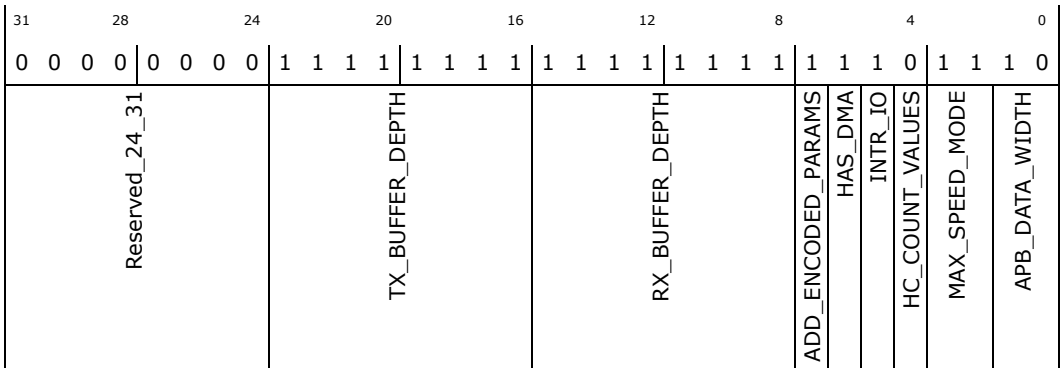
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00FFFFEEh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved_24_31:** Reserved
23:16	0xff RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	0xff RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	0x1 RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	0x1 RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	0x1 RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0x0 RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	0x3 RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	0x2 RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

9.12.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

I2C Component Version Register

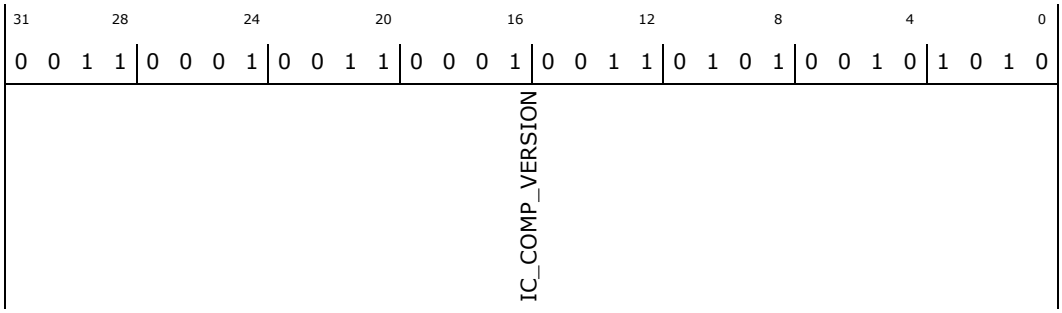
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 3131352Ah



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x3131352a RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes

9.12.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

I2C Component Type Register

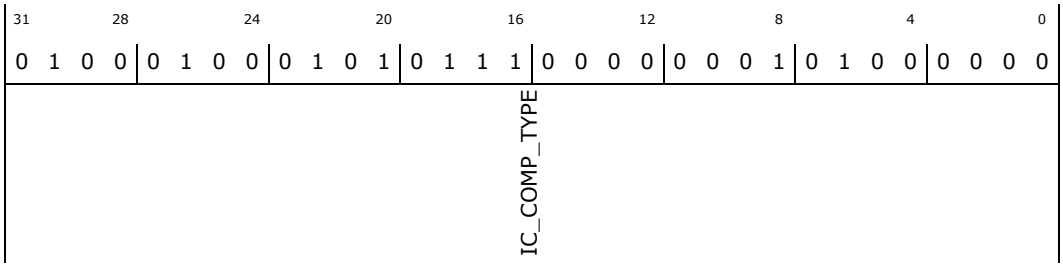
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 44570140h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x44570140 RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

9.12.46 Clock params register (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

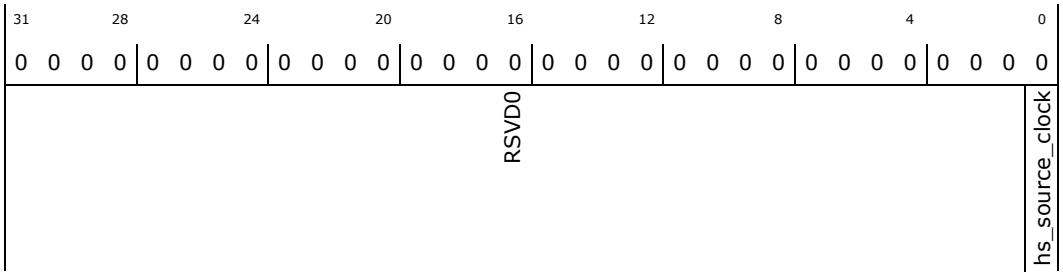
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz 1 -133MHz (high-speed operation compatible)

9.12.47 software reset (RESETS)—Offset 804h

software reset

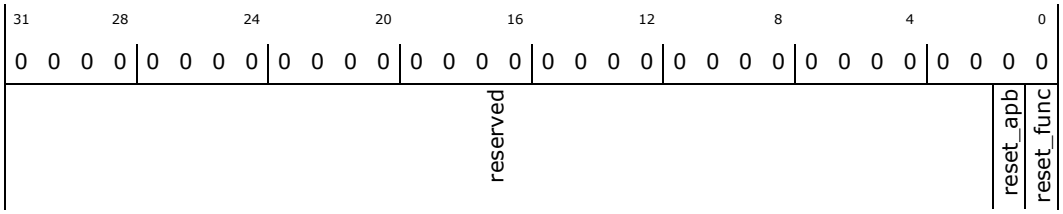
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (reserved):** Reserved
1	0x0 RW	**reset_apb:** reset the apb domain
0	0x0 RW	**reset_func:** reset the func clock domain

9.12.48 General purpose register (GENERAL)—Offset 808h

General purpose register

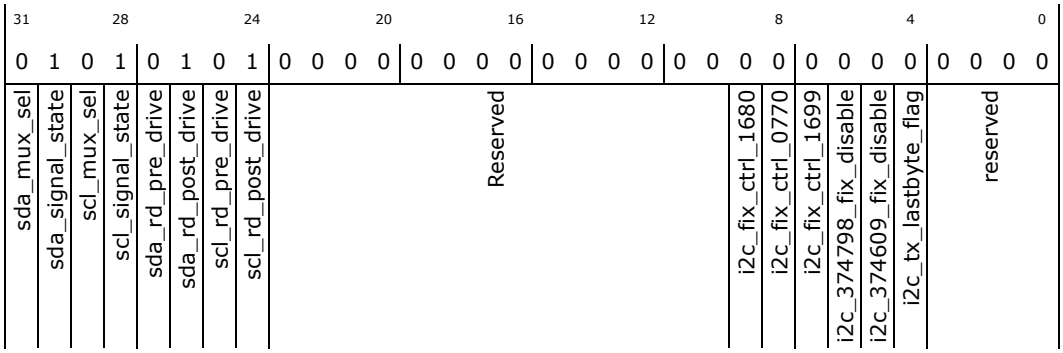
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 55000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**sda_mux_sel:** This bit selects the driver for the SDA signal: 1 = sda_signal_state, 0 = I2C logic
30	0x1 RW	**sda_signal_state:** This bit is used when sda_mux_sel = 1, used to drive the SDA signal on the I2C interface
29	0x0 RW	**scl_mux_sel:** This bit selects the driver for the SCL signal: 1 = scl_signal_state, 0 = I2C logic
28	0x1 RW	**scl_signal_state:** This bit is used when scl_mux_sel = 1, used to drive the SCL signal on the I2C interface
27	0x0 RO	**sda_rd_pre_drive:** Read only bit used to see the status of the SDA signal coming from the I2C logic
26	0x1 RO	**sda_rd_post_drive:** Read only bit used to see the status of the SDA signal coming from the pad
25	0x0 RO	**scl_rd_pre_drive:** Read only bit used to see the status of the SCL signal coming from the I2C logic
24	0x1 RO	**scl_rd_post_drive:** Read only bit used to see the status of the SCL signal coming from the pad
23:10	0x0 RO	**Reserved:** Reserved
9	0x0 RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0x0 RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0x0 RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0x0 RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)
5	0x0 RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0x0 RW	**reserved:** reserved

9.12.49 TX transaction counter (I2C_ACK_COUNT)—Offset 818h

TX transaction counter

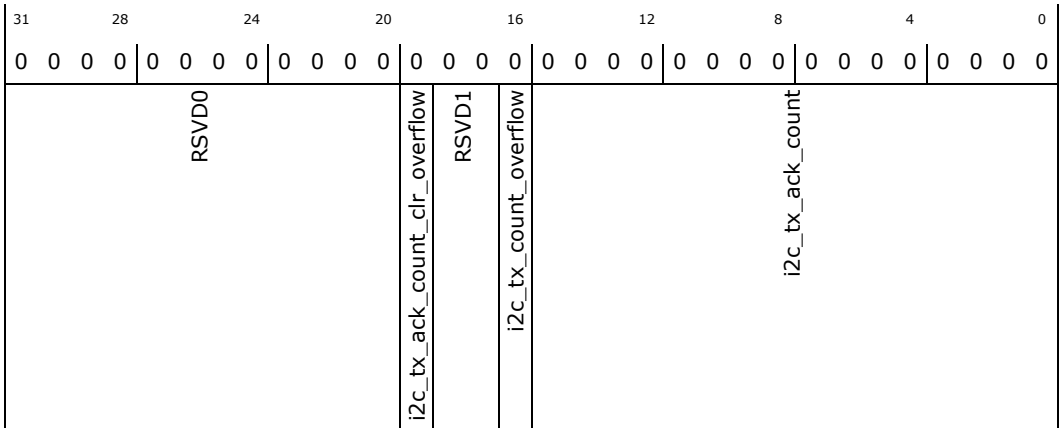
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RSVD0:** Reserved
19	0x0 RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0x0 RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

9.12.50 TX transaction complete interrupt status register (I2C_TX_COMPLETE_INTR_STAT)—Offset 820h

TX transaction has finished interrupt

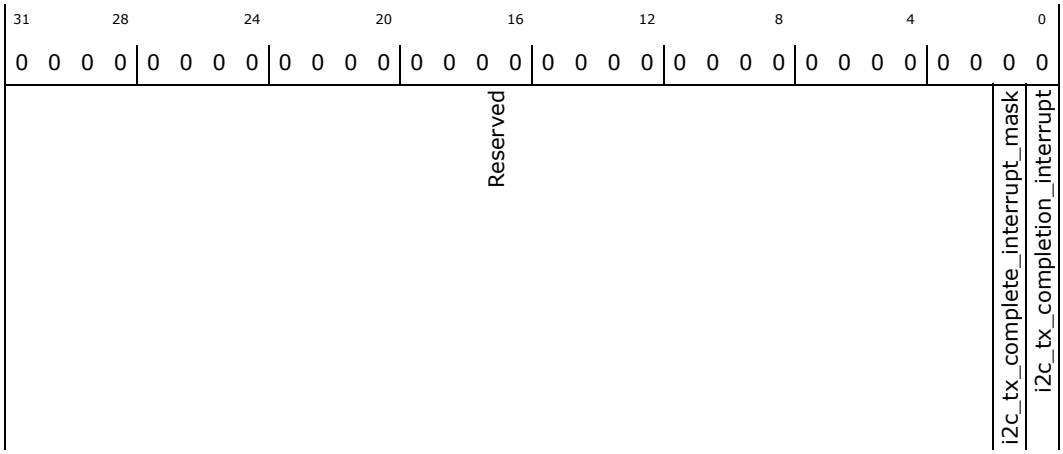
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved:** Reserved
1	0x0 RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0x0 RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

9.12.51 TX transaction complete interrupt clear register (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

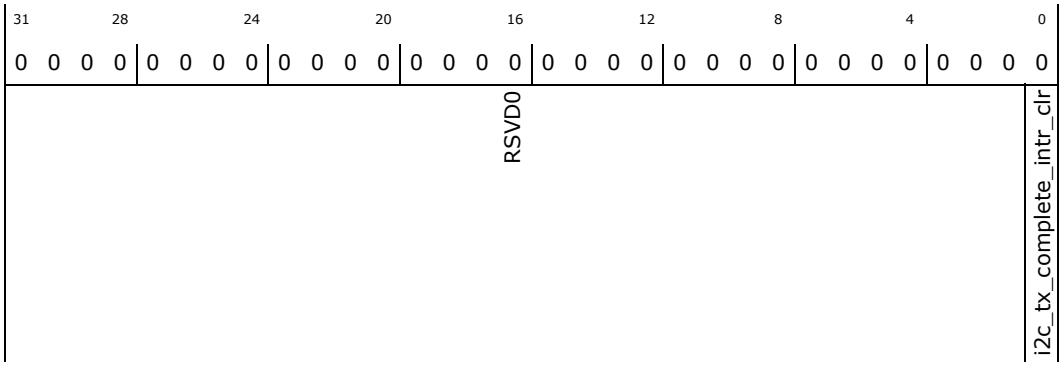
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt

9.13 SIO I2C 1 PCI Configuration Registers

Table 76. Summary of SIO I2C 1 PCI Configuration Registers—0/24/2

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4339	00008086h
4–7h	4	"STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h" on page 4339	00100000h
8–Bh	4	"REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4341	00000000h
C–Fh	4	"CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4342	00800000h
10–13h	4	"BAR -Base Address Register (BAR)—Offset 10h" on page 4342	00000000h
14–17h	4	"BAR1 -Base Address Register1 (BAR1)—Offset 14h" on page 4343	00000000h
2C–2Fh	4	"SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4344	00000000h
30–33h	4	"EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4345	00000000h
34–37h	4	"CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4345	00000000h
3C–3Fh	4	"INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4346	00000100h
80–83h	4	"POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4346	00030001h
84–87h	4	"PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4347	00000008h
F8–FBh	4	"Manufacturers ID (MANID)—Offset F8h" on page 4348	00000000h

9.13.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

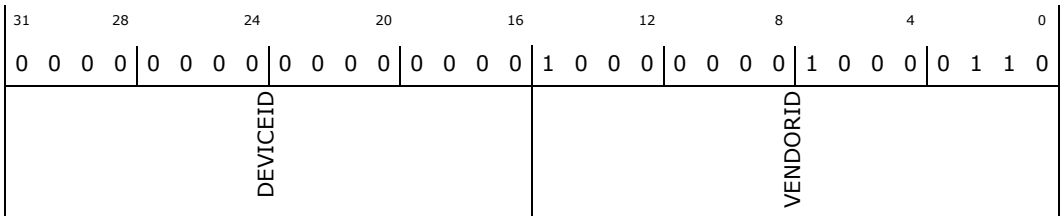
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:2] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**DEVICEID:** Device ID identifies the particular AHB/APB device. This is tied to a strap at the top level. Because of tool issues, the HTML files show this field as 0, but the following are the POR values for SoC: LPIO1 DMA: 0x2286 LPIO1 PWM1: 0x2288 LPIO1 PWM2: 0x2289 LPIO1 HSUART1: 0x228A LPIO1 HSUART2: 0x228C LPIO1 SPI1: 0x228E LPIO1 SPI2: 0x2290 LPIO1 SPI3: 0x22AC LPIO2 DMA: 0x22C0 LPIO2 I2C1: 0x22C1 LPIO2 I2C2: 0x22C2 LPIO2 I2C3: 0x22C3 LPIO2 I2C4: 0x22C4 LPIO2 I2C5: 0x22C5 LPIO2 I2C6: 0x22C6 LPIO2 I2C7: 0x22C7 For the final word on this, please see Ray Ng's SoC RevID and DevID HAS on Infofactory: https://ifcollaborate.intel.com/IFC/getdoc.aspx?docbase=InfoFactoryKBandchronid=09005ffd80e84b43andver=CURRENTandqepop=false
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap the top level.

9.13.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

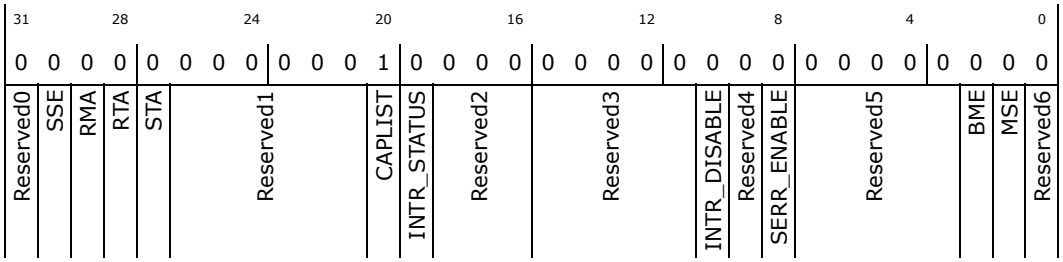
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:2] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved0:** Reserved
30	0x0 RW/1C	**SSE:** This bit is set when a device sends an DO_SERR message, and the SERR# Enable bit in the Command register is 1
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric PortReceived Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27	0x0 RW/1C	**STA:** The Bridge sets this bit whenever it responds to a transaction with CA abort. If the SERR# Enable bit is set, the Bridge sets the Signaled System Error bit and sends an DO_SERR message on the IOSF Sideband.
26:21	0x0 RO	**Reserved1:** Reserved
20	0x1 RO	**CAPLIST:** Capabilities List: Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt .i.e Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.. Reset value of this bit is 0.
9	0x0 RO	**Reserved4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: If both SERR# Enable and the Unsupported Request Reporting Enable (URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0x0 RO	**Reserved6:** Reserved

9.13.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

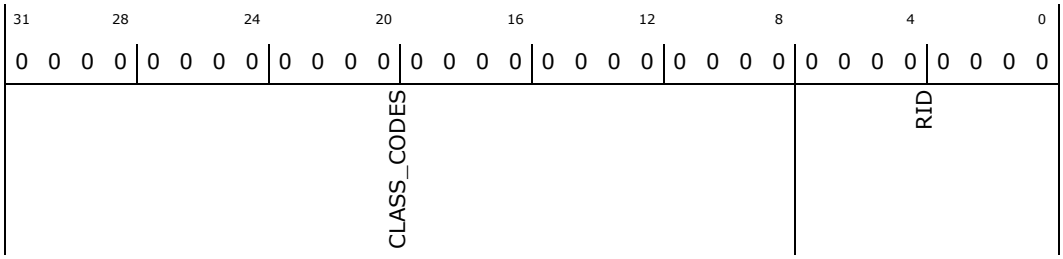
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:2] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

9.13.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

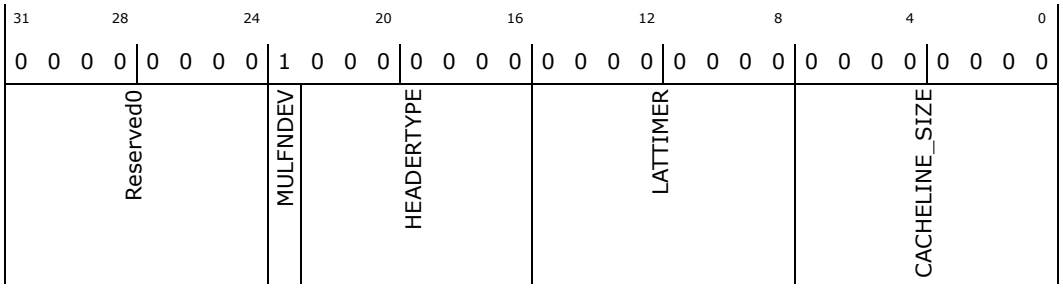
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:2] + Ch

Default: 00800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x1 RO	**MULFNDEV:** Multi Function Device: This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. Value of 1 indicates multifunction device value of 0 indicates single function device
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	0x0 RO	**LATTIMER:** Latency Timer: Doesn.t apply to PCI Express. Hardwired to 00h.
7:0	0x0 RW	**CACHELINE_SIZE:** Cache Line Size: Doesn.t apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

9.13.5 BAR -Base Address Register (BAR)—Offset 10h

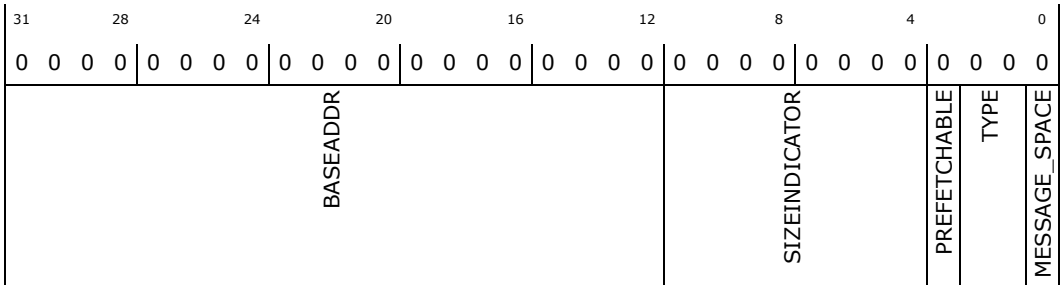
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the AHB device memory space. Taken from Strap values as 1's. Please note that for DMA this field goes from [31:14], or 16kbyte, and the SIZEINDICATOR field goes from [13:4].
11:4	0x0 RO	**SIZEINDICATOR:** Size Indicator Read Only: Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0x0 RO	**TYPE:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.13.6 BAR1 -Base Address Register1 (BAR1)—Offset 14h

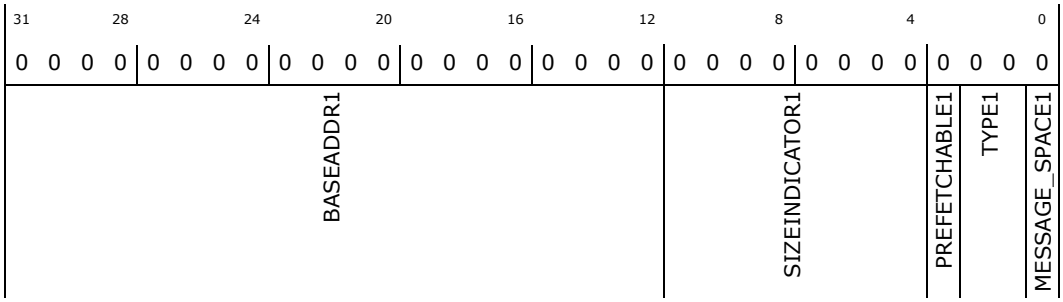
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:2] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	0x0 RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not
2:1	0x0 RO	**TYPE1:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.13.7 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

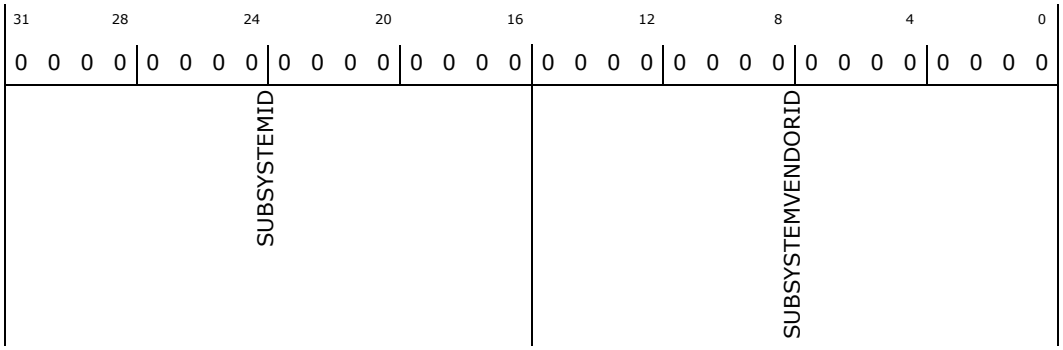
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:2] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

9.13.8 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

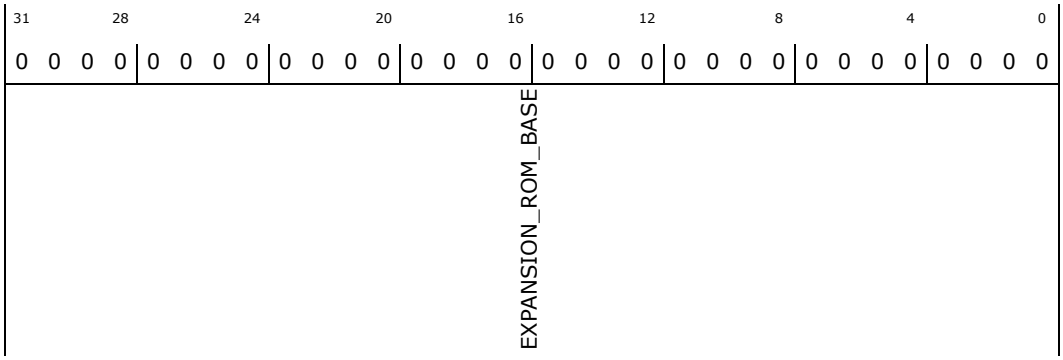
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:2] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** A value of all zeros indicates no support for expansion ROM.

9.13.9 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

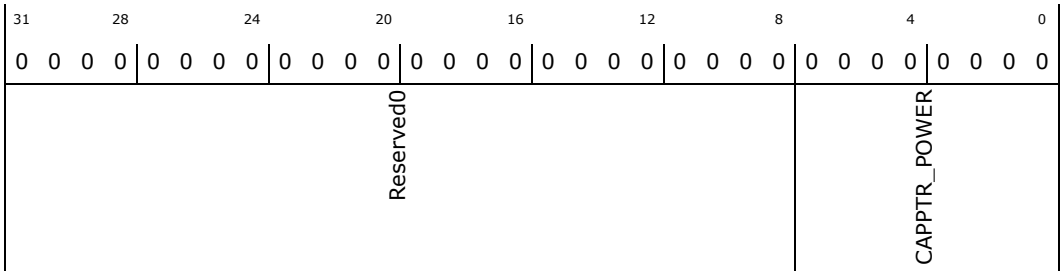
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:2] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x0 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

9.13.10 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

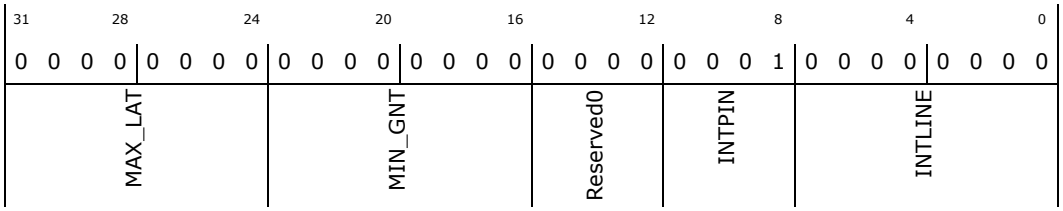
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:2] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

9.13.11 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

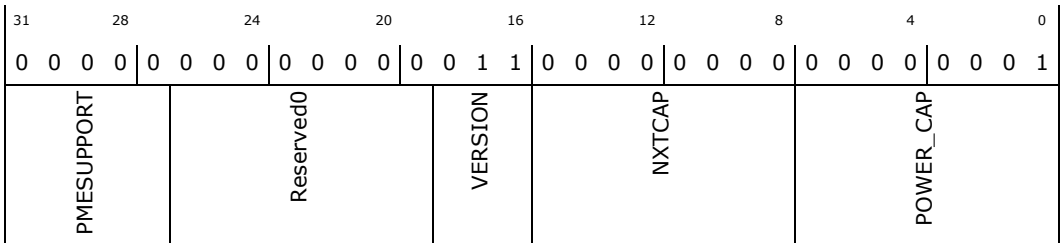
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:2] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** PME_Support - This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

9.13.12 PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

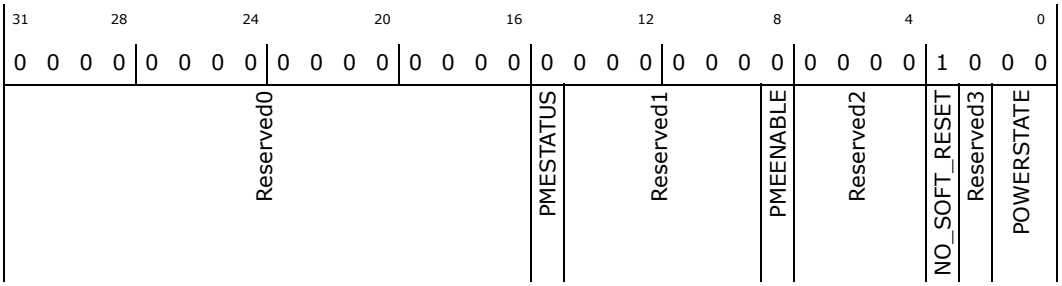
PMECTRLSTATUS - PME Control and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:2] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

9.13.13 Manufacturers ID (MANID)—Offset F8h

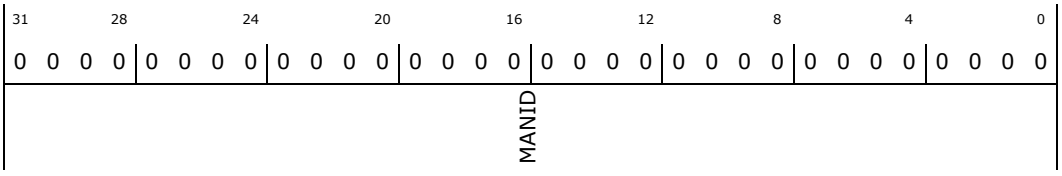
Manufacturers ID

Access Method

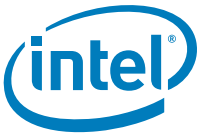
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:2] + F8h

Default: 00000000h



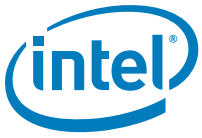
Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: This register is brought out as straps to the top level.



9.14 SIO I2C 1 Memory Mapped I/O Registers

Table 77. Summary of SIO I2C 1 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 4353	0000007Fh
4–7h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 4354	00001055h
8–Bh	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 4355	00000055h
C–Fh	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 4355	00000001h
10–13h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 4356	00000000h
14–17h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 4357	00000190h
18–1Bh	4	"Standard Speed I2C Clock SCL Low Count Register. (IC_SS_SCL_LCNT)—Offset 18h" on page 4358	000001D6h
1C–1Fh	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 4358	0000003Ch
20–23h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 4359	00000082h
24–27h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 4360	0000000Ch
28–2Bh	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 4360	00000020h
2C–2Fh	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 4361	00000000h
30–33h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 4362	000008FFh
34–37h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 4363	00000000h
38–3Bh	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 4364	00000010h
3C–3Fh	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 4365	00000010h
40–43h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 4366	00000000h
44–47h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 4366	00000000h
48–4Bh	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 4367	00000000h
4C–4Fh	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 4368	00000000h
50–53h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 4368	00000000h
54–57h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 4369	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
58–5Bh	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 4369	00000000h
5C–5Fh	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 4370	00000000h
60–63h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 4371	00000000h
64–67h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 4371	00000000h
68–6Bh	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 4372	00000000h
6C–6Fh	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 4372	00000000h
70–73h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 4373	00000006h
74–77h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 4374	00000000h
78–7Bh	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 4374	00000000h
7C–7Fh	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 4375	00000001h
80–83h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 4376	00000000h
84–87h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 4377	00000000h
88–8Bh	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 4378	00000000h
8C–8Fh	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 4378	00000000h
90–93h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 4379	00000000h
94–97h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 4380	00000064h
98–9Bh	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 4380	00000001h
9C–9Fh	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 4381	00000000h
A0–A3h	4	"SS/FS Mode Spike Length Register (IC_FS_SPKLEN)—Offset A0h" on page 4382	00000005h
A4–A7h	4	"HS Mode Spike Length Register (IC_HS_SPKLEN)—Offset A4h" on page 4382	00000002h
F4–F7h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 4383	00FFFFEEh
F8–FBh	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 4384	3131352Ah
FC–FFh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 4385	44570140h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
800–803h	4	"Clock params register (CLOCK_PARAMS)—Offset 800h" on page 4385	00000000h
804–807h	4	"software reset (RESETS)—Offset 804h" on page 4386	00000000h
808–80Bh	4	"General purpose register (GENERAL)—Offset 808h" on page 4386	55000000h
818–81Bh	4	"TX transaction counter (I2C_ACK_COUNT)—Offset 818h" on page 4388	00000000h
820–823h	4	"TX transaction complete interrupt status register (I2C_TX_COMPLETE_INTR_STAT)—Offset 820h" on page 4389	00000000h
824–827h	4	"TX transaction complete interrupt clear register (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 4389	00000000h

9.14.1 I2C Control Register (IC_CON)—Offset 0h

I2C Control Register

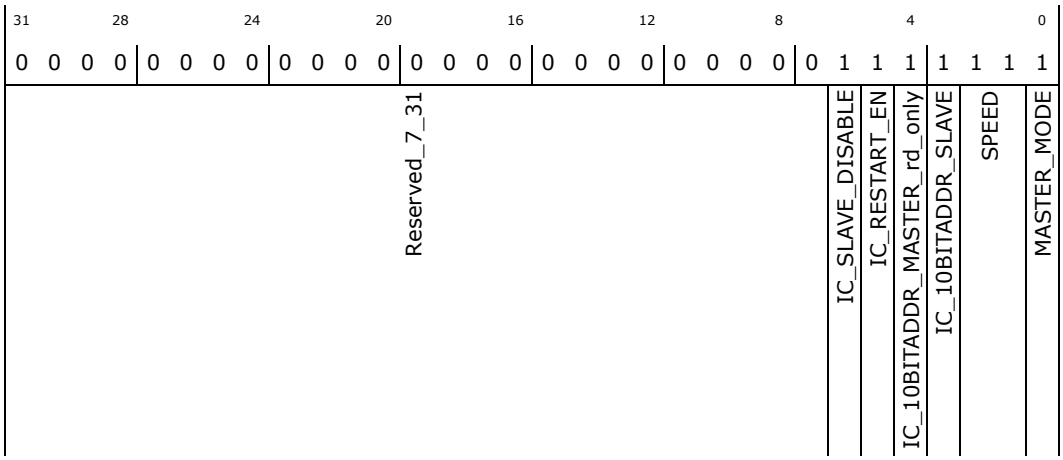
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 0000007Fh



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RW	**Reserved_7_31:** Reserved
6	0x1 RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	0x1 RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master.When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: Sending a START BYTE. Performing any high-speed mode operation. Performing direction changes in combined format mode. Performing a read operation with a 10-bit address
4	0x1 RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register
3	0x1 RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0x3 RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	0x1 RW	**MASTER_MODE:** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

9.14.2 I2C Target Address Register (IC_TAR)—Offset 4h

I2C Target Address Register

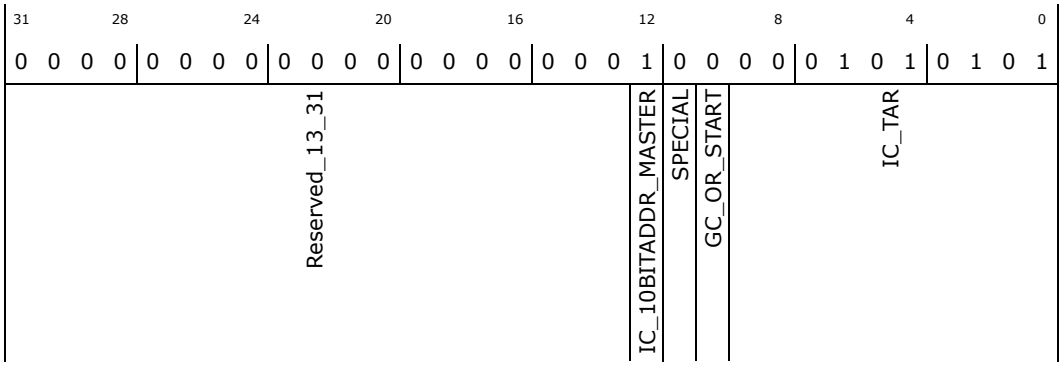
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00001055h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Reserved_13_31:** Reserved
12	0x1 RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master. This bit exists in this register only if the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 1
11	0x0 RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. 0: ignore bit 10 GC_OR_START and use IC_TAR normally. 1: perform special I2C command as specified in GC_OR_START bit
10	0x0 RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.

Bit Range	Default & Access	Field Name (ID): Description
9:0	0x55 RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

9.14.3 I2C Slave Address Register (IC_SAR)—Offset 8h

I2C Slave Address Register

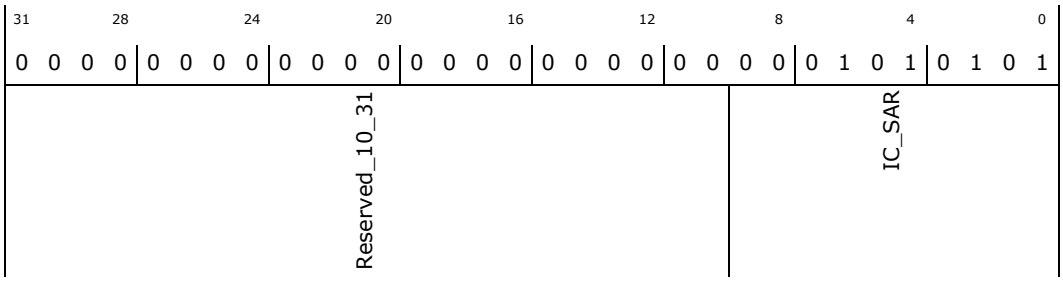
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000055h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**Reserved_10_31:** Reserved
9:0	0x55 RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.14.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

I2C High Speed Master Mode Code Address Register

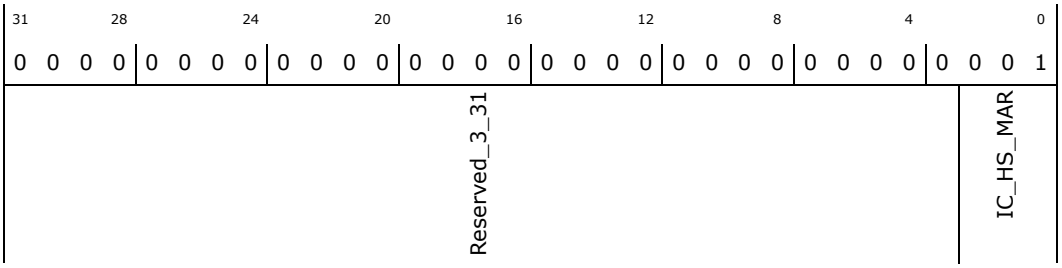
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved_3_31:** Reserved
2:0	0x1 RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.14.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

I2C Rx/Tx Data Buffer and Command Register; this is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO

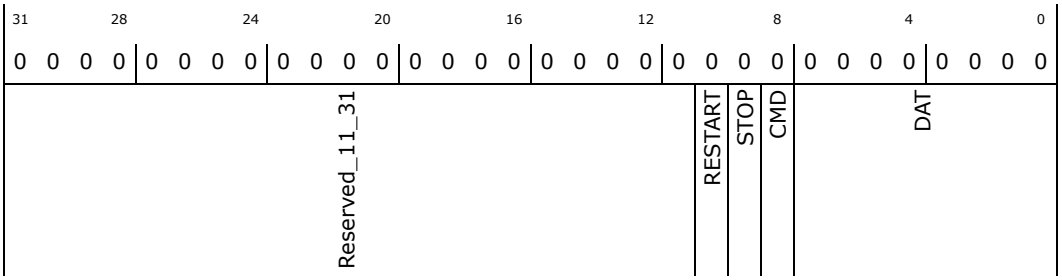
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:11	0x0 RW	**Reserved_11_31:** Reserved
10	0x0 RW	**RESTART:** RESTART
9	0x0 RW	**STOP:** STOP
8	0x0 RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It controls only the direction when it acts as a master. 1 = Read. 0 = Write
7:0	0x0 RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. However, when you read this register, these bits return the value of data received on the DW_apb_i2c interface.

9.14.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

Standard Speed I2C Clock SCL High Count Register.

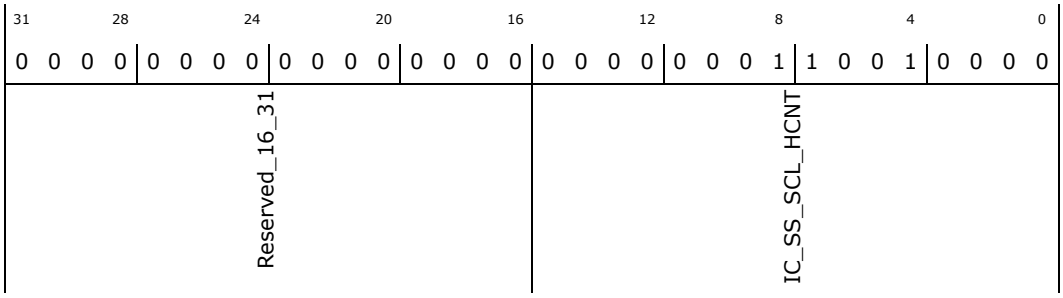
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000190h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x190 RW	**IC_SS_SCL_HCNT:** Standard Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.14.7 Standard Speed I2C Clock SCL Low Count Register. (IC_SS_SCL_LCNT)—Offset 18h

Standard Speed I2C Clock SCL Low Count Register.

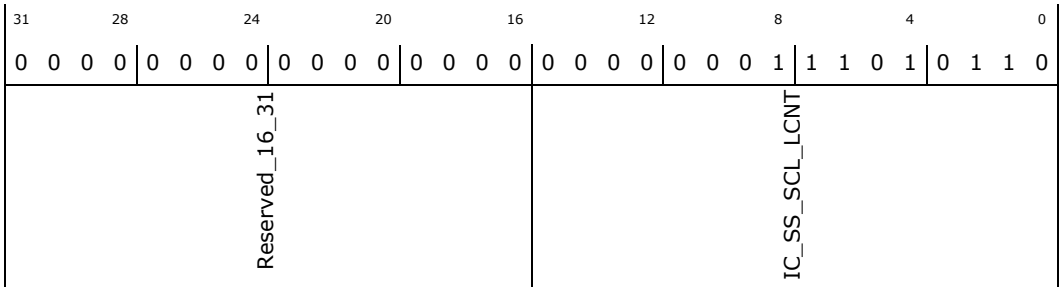
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 000001D6h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x1d6 RW	**IC_SS_SCL_LCNT:** Standard Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.14.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

Fast Speed I2C Clock SCL High Count Register

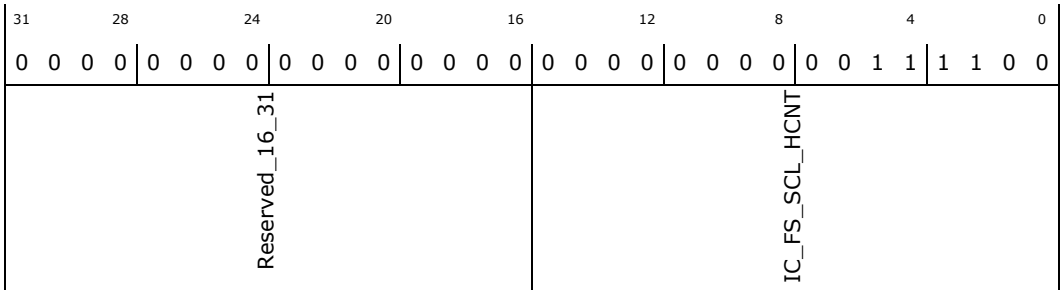
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 0000003Ch



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x3c RW	**IC_FS_SCL_HCNT:** Fast Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.14.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

Fast Speed I2C Clock SCL Low Count Register

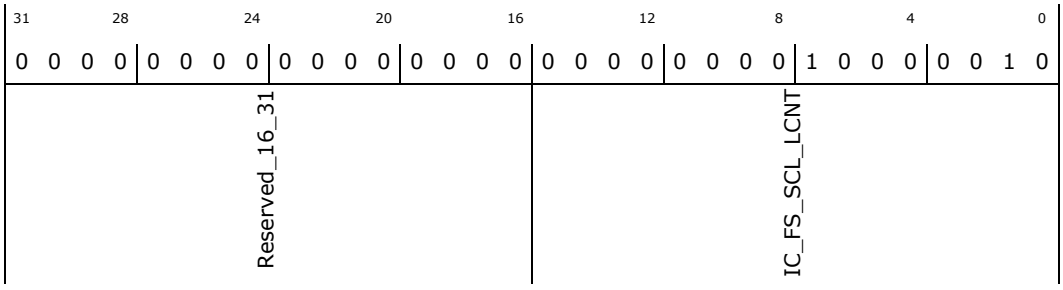
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000082h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x82 RW	**IC_FS_SCL_LCNT:** Fast Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.14.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

High Speed I2C Clock SCL High Count Register

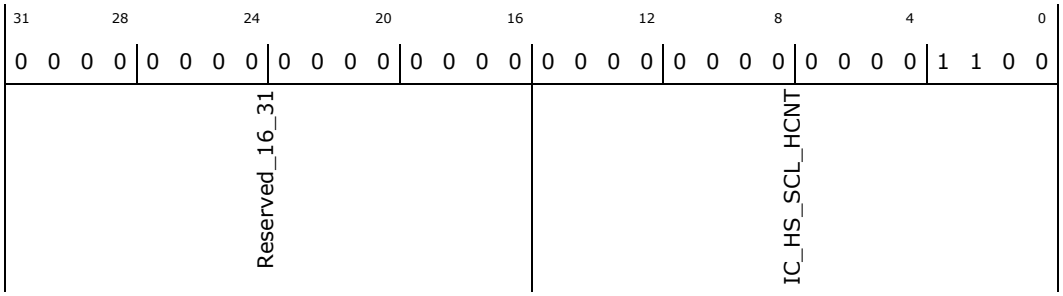
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 0000000Ch



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0xc RW	**IC_HS_SCL_HCNT:** High Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.14.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

High Speed I2C Clock SCL Low Count Register

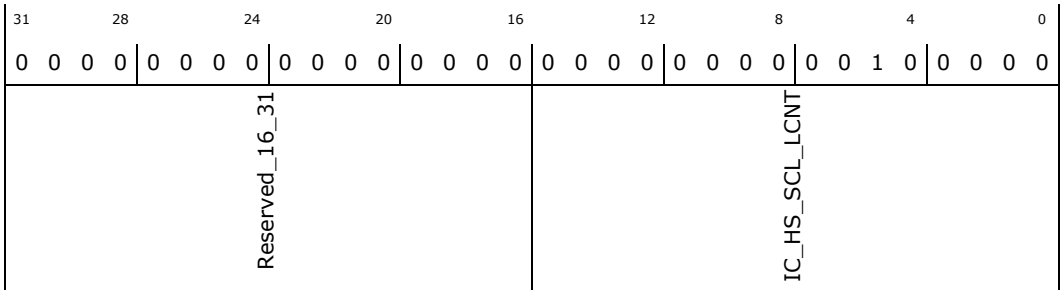
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000020h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x20 RW	**IC_HS_SCL_LCNT:** High Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.14.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

I2C Interrupt Status Register

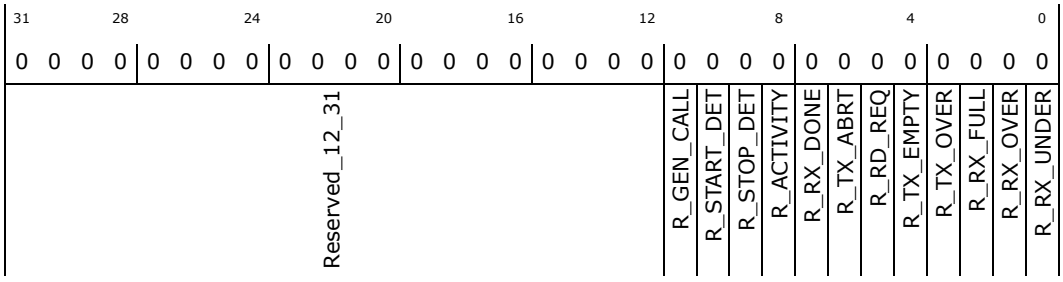
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x0 RO	**R_GEN_CALL:** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0x0 RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0x0 RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0x0 RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0x0 RO	**R_TX_ABRT:** This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0x0 RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.
4	0x0 RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0x0 RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0x0 RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0x0 RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0x0 RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

9.14.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

I2C Interrupt Mask Register

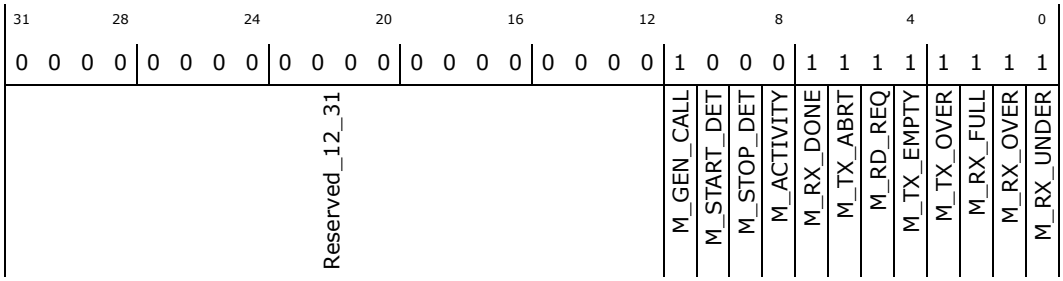
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 000008FFh



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x1 RW	**M_GEN_CALL:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
10	0x0 RW	**M_START_DET:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
9	0x0 RW	**M_STOP_DET:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
8	0x0 RW	**M_ACTIVITY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
7	0x1 RW	**M_RX_DONE:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
6	0x1 RW	**M_TX_ABRT:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
5	0x1 RW	**M_RD_REQ:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
4	0x1 RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
3	0x1 RW	**M_TX_OVER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
2	0x1 RW	**M_RX_FULL:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
1	0x1 RW	**M_RX_OVER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
0	0x1 RW	**M_RX_UNDER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.

9.14.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

I2C Raw Interrupt Status Register

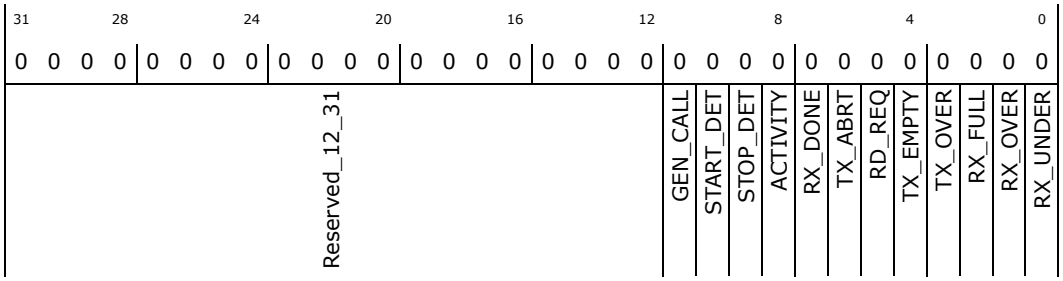
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x0 RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT
10	0x0 RO	**START_DET:** Same as in reg_IC_INTR_STAT
9	0x0 RO	**STOP_DET:** Same as in reg_IC_INTR_STAT
8	0x0 RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT
7	0x0 RO	**RX_DONE:** Same as in reg_IC_INTR_STAT
6	0x0 RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT
5	0x0 RO	**RD_REQ:** Same as in reg_IC_INTR_STAT
4	0x0 RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT
3	0x0 RO	**TX_OVER:** Same as in reg_IC_INTR_STAT
2	0x0 RO	**RX_FULL:** Same as in reg_IC_INTR_STAT
1	0x0 RO	**RX_OVER:** Same as in reg_IC_INTR_STAT
0	0x0 RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT

9.14.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

I2C Receive FIFO Threshold Register

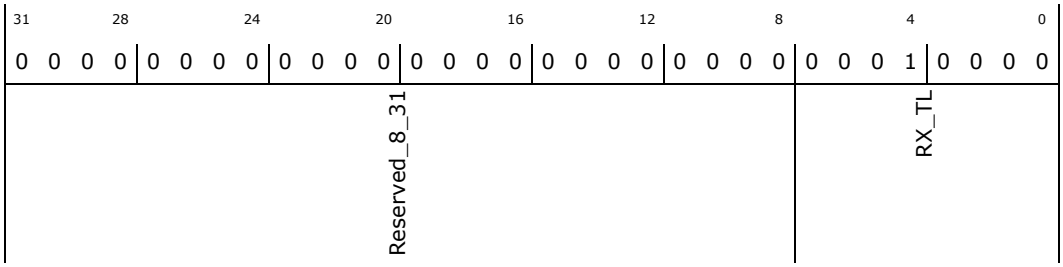
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x10 RW	**RX_TL:** Receive FIFO Threshold Level. The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

9.14.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

I2C Transmit FIFO Threshold Register

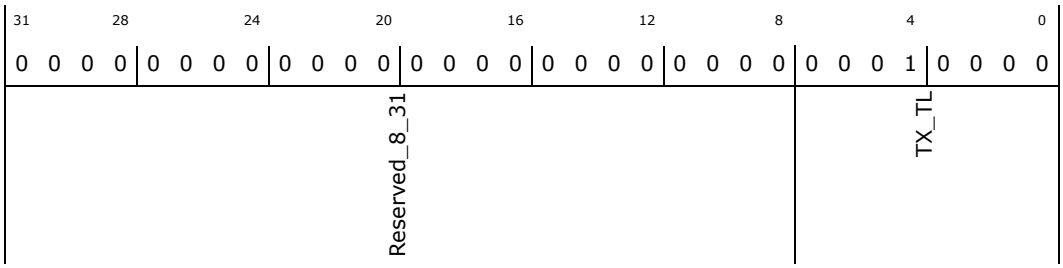
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x10 RW	**TX_TL:** Transmit FIFO Threshold Level. Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

9.14.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

Clear Combined and Individual Interrupt Register

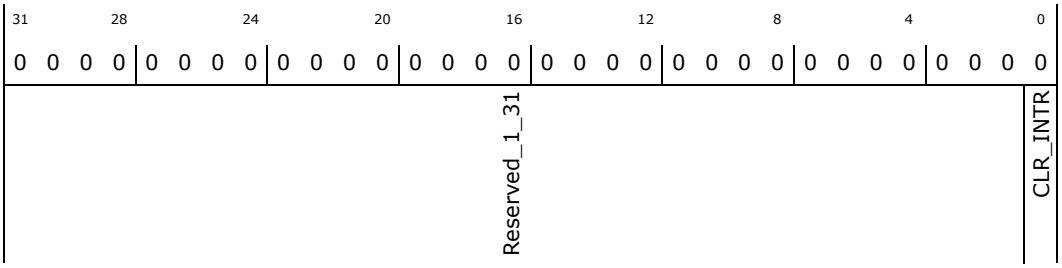
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

9.14.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

Clear RX_UNDER Interrupt Register

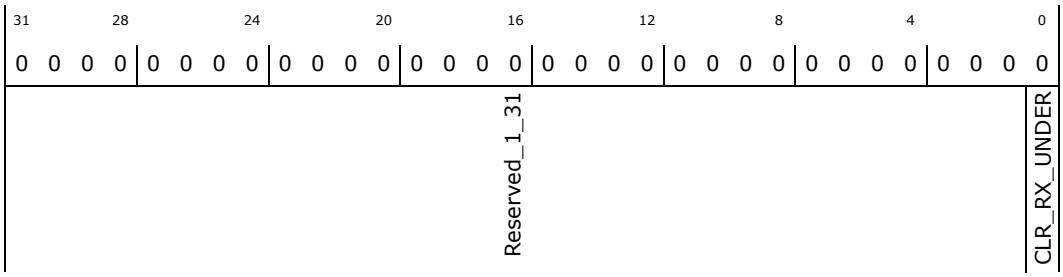
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

9.14.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

Clear RX_OVER Interrupt Register

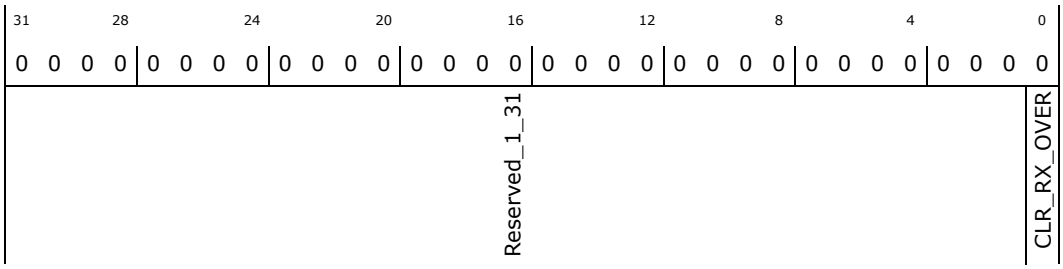
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

9.14.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

Clear TX_OVER Interrupt Register

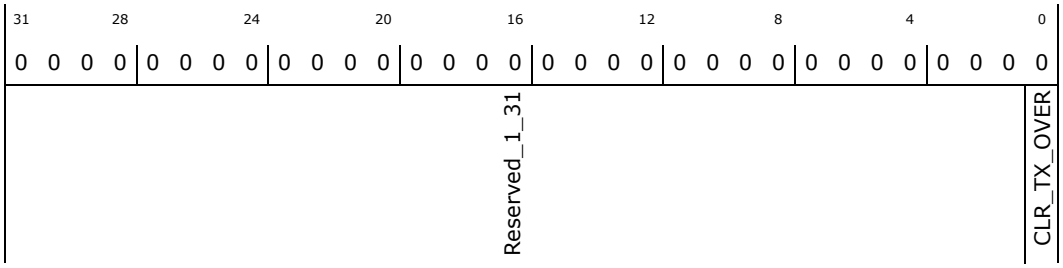
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

9.14.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

Clear RD_REQ Interrupt Register

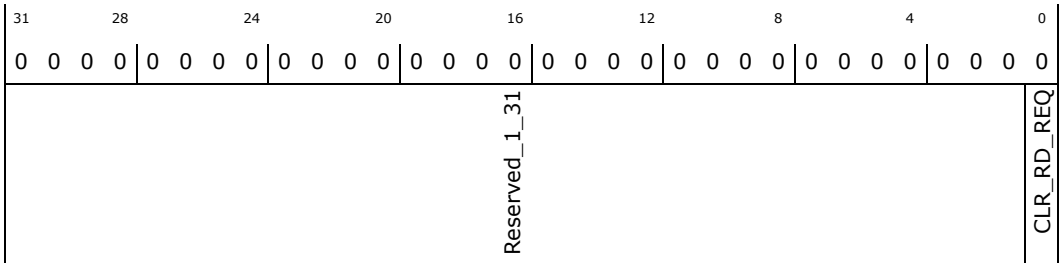
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

9.14.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

Clear TX_ABRT Interrupt Register

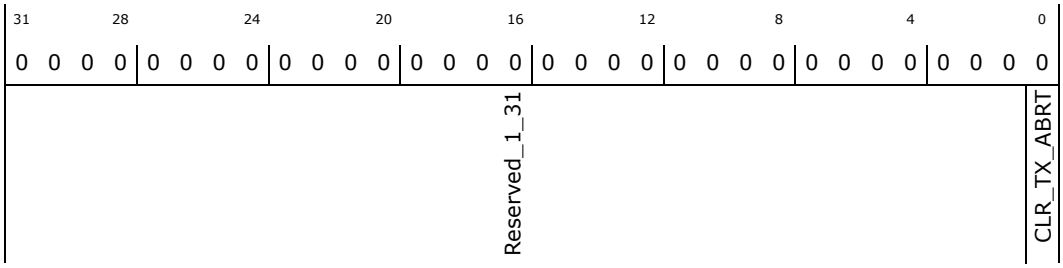
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

9.14.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

Clear RX_DONE Interrupt Register

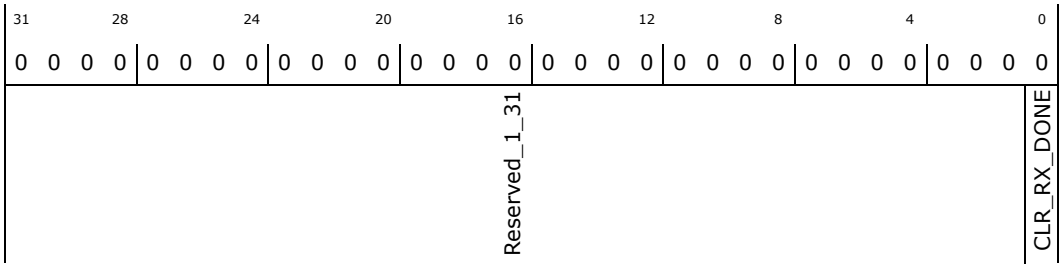
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

9.14.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

Clear ACTIVITY Interrupt Register

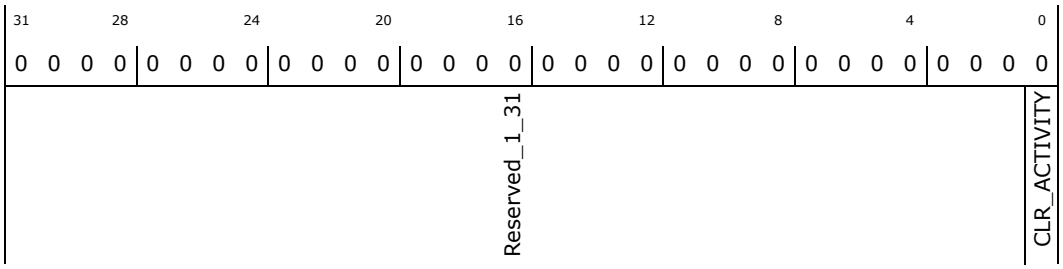
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

9.14.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

Clear STOP_DET Interrupt Register

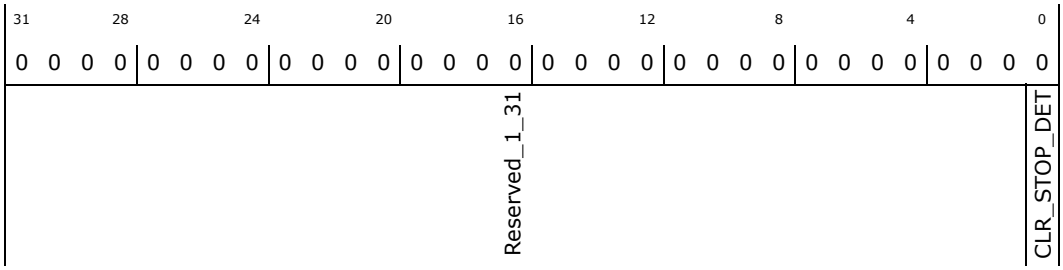
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

9.14.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

Clear START_DET Interrupt Register

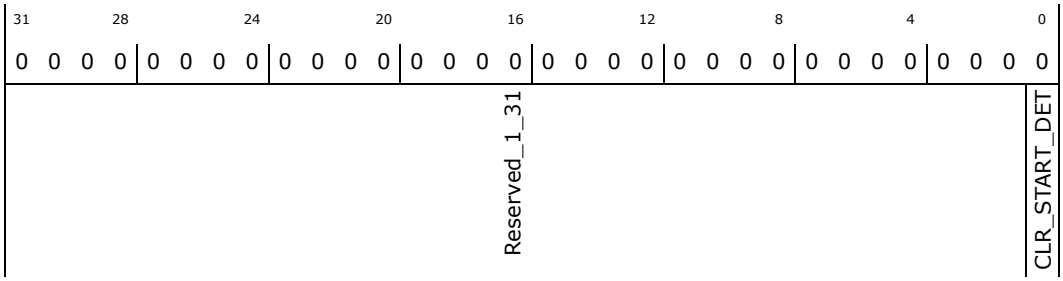
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

9.14.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

Clear GEN_CALL Interrupt Register

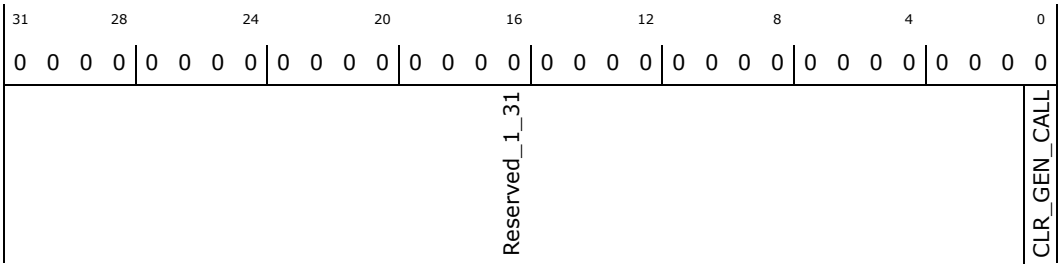
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

9.14.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

I2C Enable Register

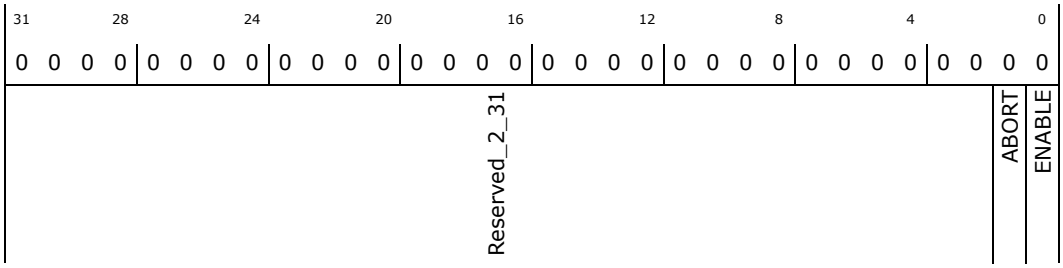
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved_2_31:** Reserved
1	0x0 WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.
0	0x0 RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) 1: Enables DW_apb_i2c

9.14.29 I2C Status Register (IC_STATUS)—Offset 70h

I2C Status Register

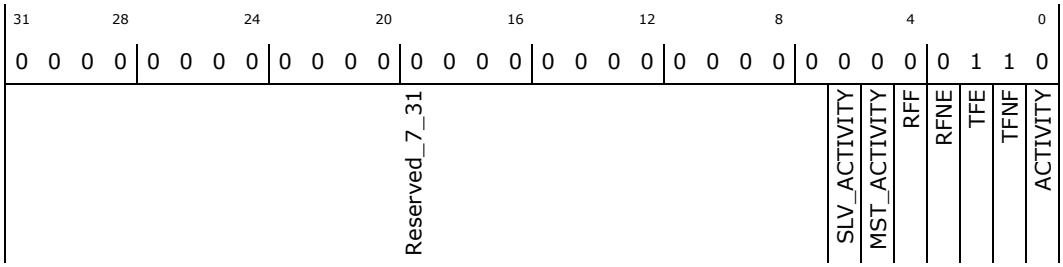
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000006h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RW	**Reserved_7_31:** Reserved
6	0x0 RO	**SLV_ACTIVITY:** Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0x0 RO	**MST_ACTIVITY:** Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RO	**RFF:** Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0x0 RO	**RFNE:** Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.
2	0x1 RO	**TFE:** Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	0x1 RO	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0x0 RO	**ACTIVITY:** I2C Activity Status

9.14.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

I2C Transmit FIFO Level Register

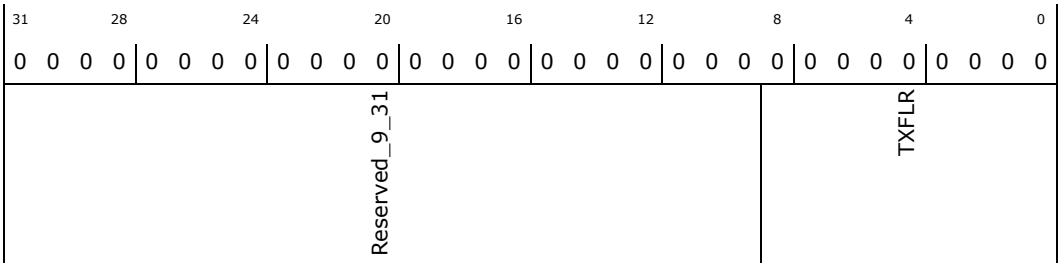
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved_9_31:** Reserved
8:0	0x0 RO	**TXFLR:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

9.14.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

I2C Receive FIFO Level Register

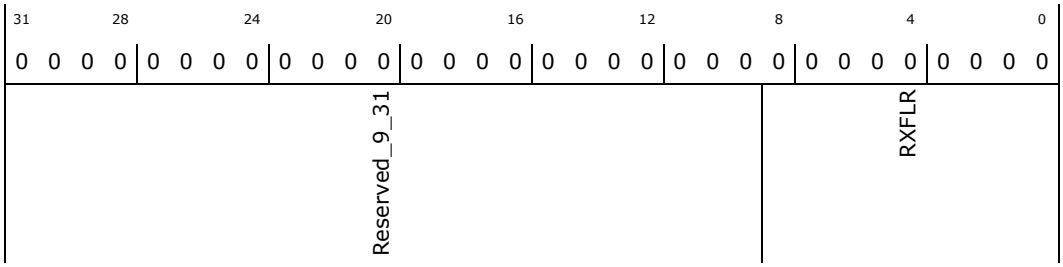
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved_9_31:** Reserved
8:0	0x0 RO	**RXFLR:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

9.14.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

I2C SDA Hold Time Length Register

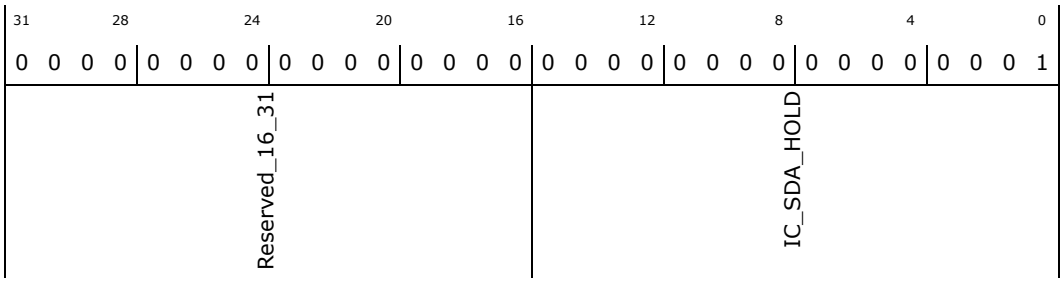
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x1 RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

9.14.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

I2C Transmit Abort Source Register

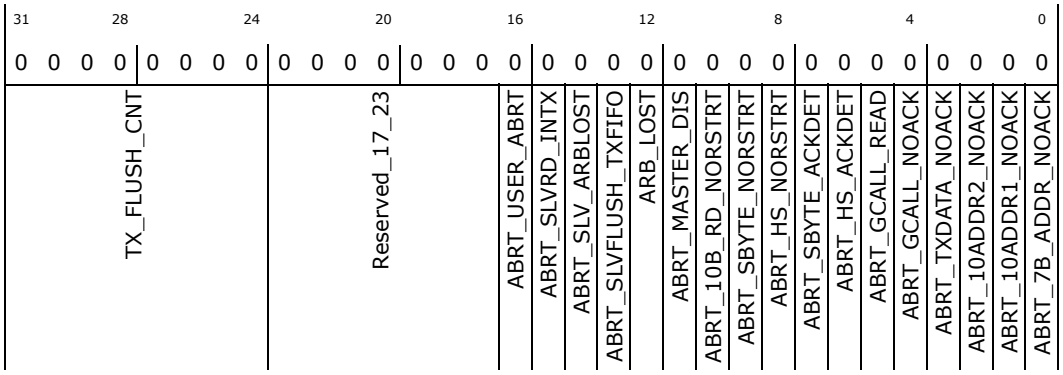
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0x0 RW	**Reserved_17_23:** Reserved
16	0x0 RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0x0 RO	**ABRT_SLVRD_INTX:** 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0x0 RO	**ABRT_SLV_ARBLOST:** 1: Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0x0 RO	**ABRT_SLVFLUSH_TXFIFO:** 1: Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0x0 RO	**ARB_LOST:** 1: Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0x0 RO	**ABRT_MASTER_DIS:** 1: User tries to initiate a Master operation with the Master mode disabled.
10	0x0 RO	**ABRT_10B_RD_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RO	**ABRT_SBYTE_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0x0 RO	**ABRT_HS_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0x0 RO	**ABRT_SBYTE_ACKDET:** 1: Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
6	0x0 RO	**ABRT_HS_ACKDET:** 1: Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
5	0x0 RO	**ABRT_GCALL_READ:** 1: DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0x0 RO	**ABRT_GCALL_NOACK:** 1: DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0x0 RO	**ABRT_TXDATA_NOACK:** 1: This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0x0 RO	**ABRT_10ADDR2_NOACK:** 1: Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0x0 RO	**ABRT_10ADDR1_NOACK:** 1: Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0x0 RO	**ABRT_7B_ADDR_NOACK:** 1: Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

9.14.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

Generate Slave Data NACK Register

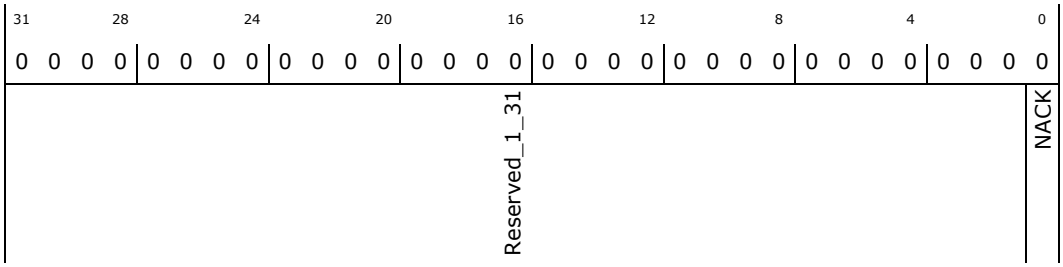
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RW	**NACK:** Generate NACK. This NACK generation only occurs when DW_apb_i2c is a slavereceiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. 1 = generate NACK after data byte received 0 = generate NACK/ACK normally

9.14.35 DMA Control Register (IC_DMA_CR)—Offset 88h

DMA Control Register

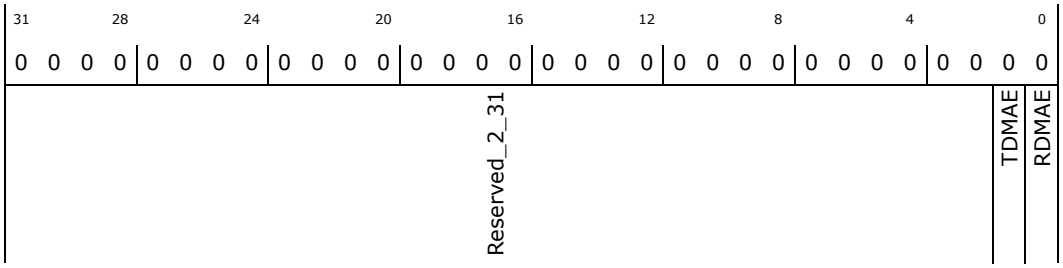
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved_2_31:** Reserved
1	0x0 RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel. 0 = Transmit DMA disabled 1 = Transmit DMA enabled
0	0x0 RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. 0 = Receive DMA disabled 1 = Receive DMA enabled

9.14.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

DMA Transmit Data Level Register

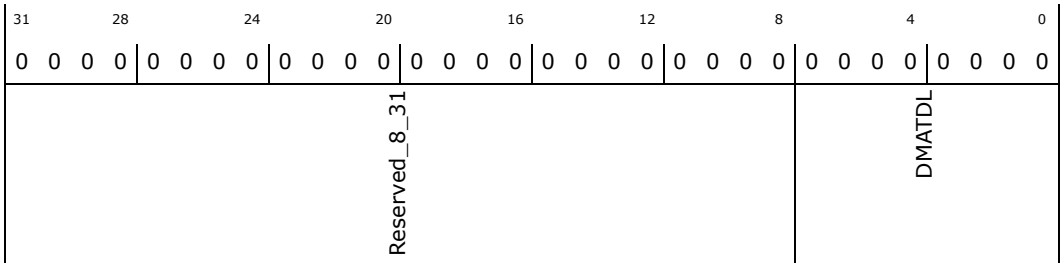
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x0 RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

9.14.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

I2C Receive Data Level Register

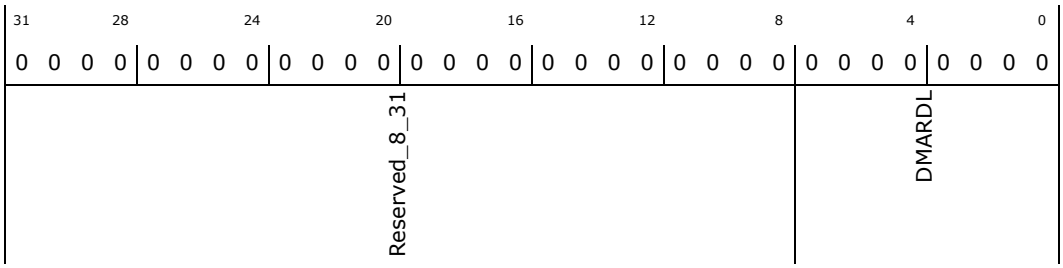
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x0 RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

9.14.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

I2C SDA Setup Register

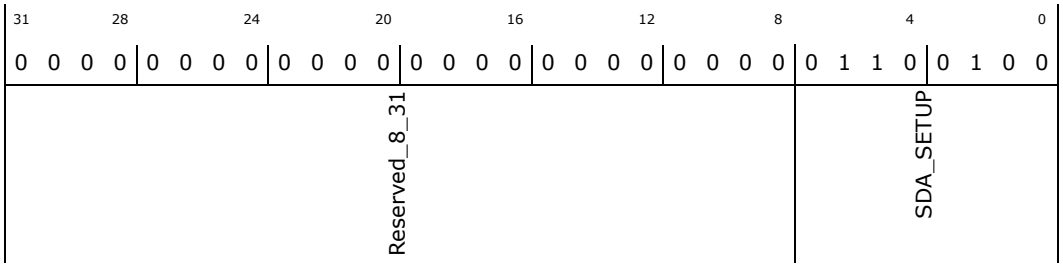
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000064h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x64 RW	**SDA_SETUP:** SDA Setup. It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

9.14.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

I2C ACK General Call Register

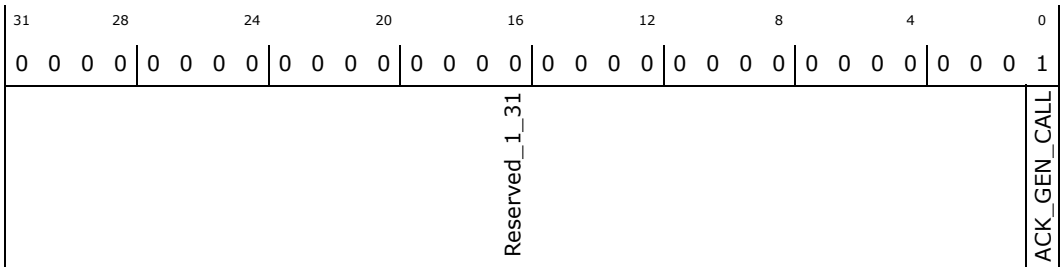
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x1 RW	**ACK_GEN_CALL:** ACK General Call. When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

9.14.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

I2C Enable Status Register

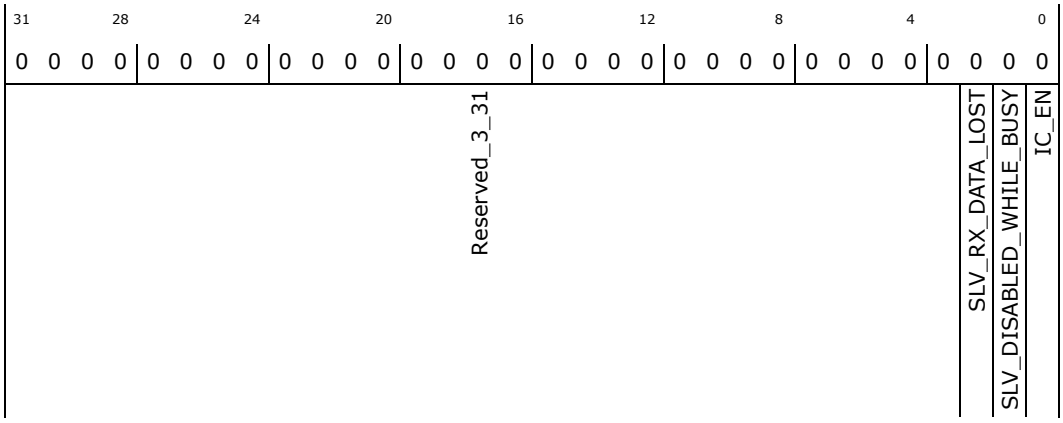
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved_3_31:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0x0 RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0x0 RO	**IC_EN:** ic_en Status. This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

9.14.41 SS/FS Mode Spike Length Register (IC_FS_SPKLEN)—Offset A0h

SS/FS Mode Spike Length Register

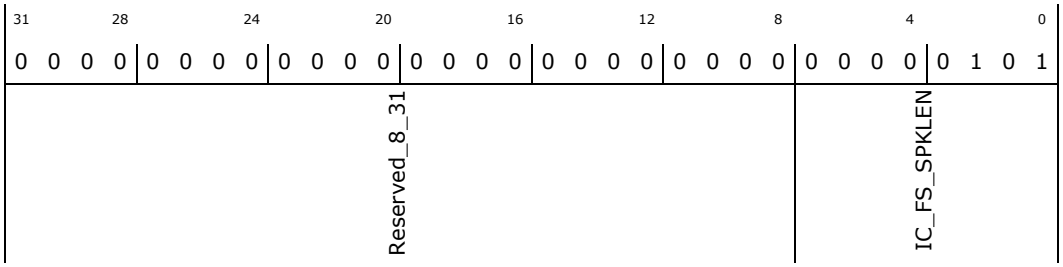
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000005h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x5 RW	**IC_FS_SPKLEN:** Maximum length (in ic_clk cycles) of suppressed spikes in SS and FS modes

9.14.42 HS Mode Spike Length Register (IC_HS_SPKLEN)—Offset A4h

HS Mode Spike Length Register

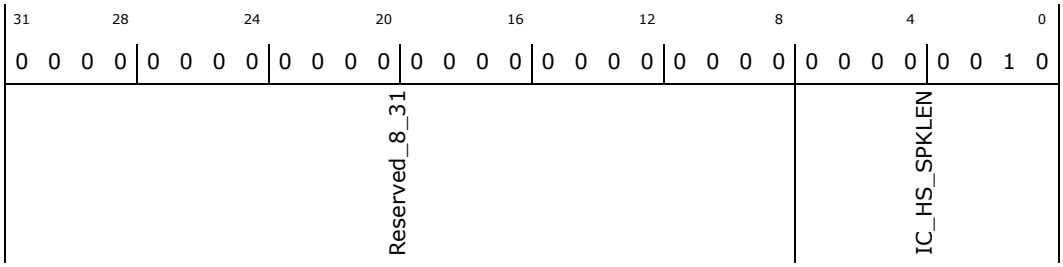
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x2 RW	**IC_HS_SPKLEN:** Maximum length (in ic_clk cycles) of suppressed spikes in HS mode

9.14.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

Component Parameter Register 1

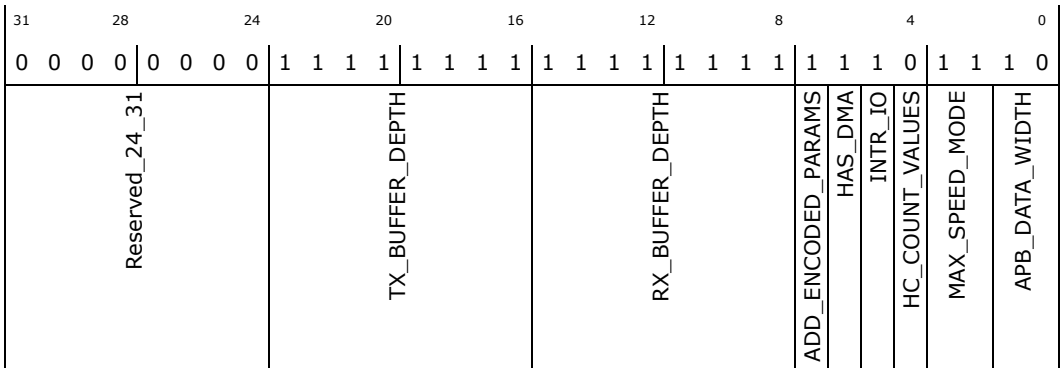
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00FFFFEEh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved_24_31:** Reserved
23:16	0xff RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	0xff RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	0x1 RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	0x1 RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	0x1 RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0x0 RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	0x3 RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	0x2 RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

9.14.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

I2C Component Version Register

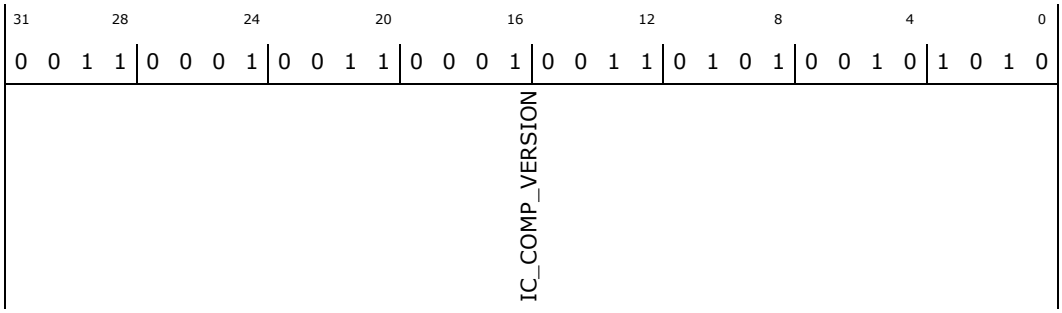
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 3131352Ah



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x3131352a RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes

9.14.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

I2C Component Type Register

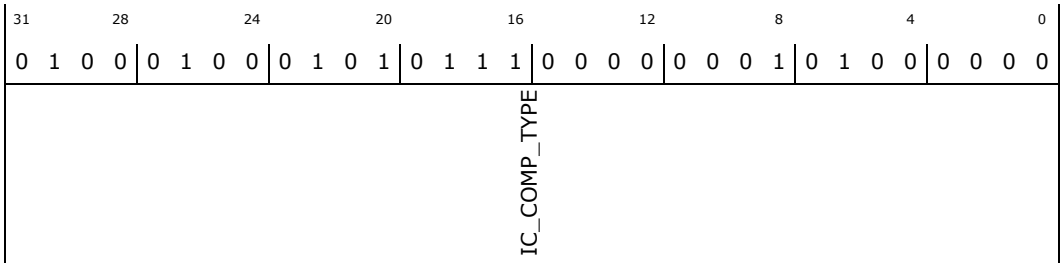
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 44570140h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x44570140 RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

9.14.46 Clock params register (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

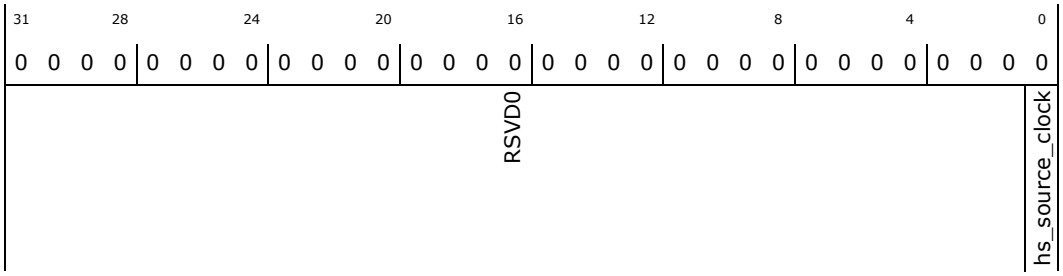
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz 1 -133MHz (high-speed operation compatible)

9.14.47 software reset (RESETS)—Offset 804h

software reset

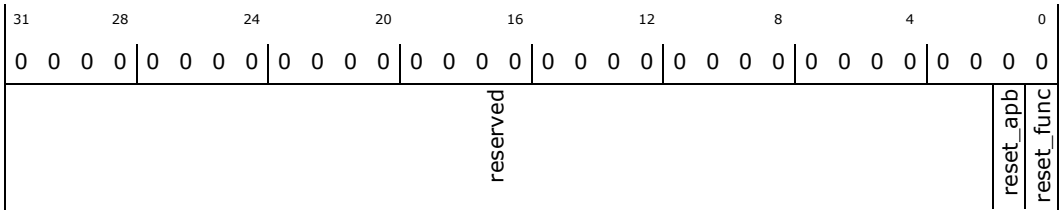
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (reserved):** Reserved
1	0x0 RW	**reset_apb:** reset the apb domain
0	0x0 RW	**reset_func:** reset the func clock domain

9.14.48 General purpose register (GENERAL)—Offset 808h

General purpose register

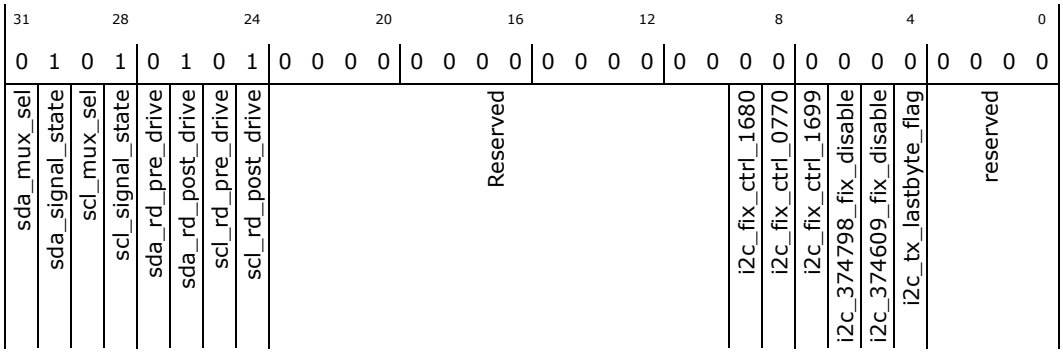
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 55000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**sda_mux_sel:** This bit selects the driver for the SDA signal: 1 = sda_signal_state, 0 = I2C logic
30	0x1 RW	**sda_signal_state:** This bit is used when sda_mux_sel = 1, used to drive the SDA signal on the I2C interface
29	0x0 RW	**scl_mux_sel:** This bit selects the driver for the SCL signal: 1 = scl_signal_state, 0 = I2C logic
28	0x1 RW	**scl_signal_state:** This bit is used when scl_mux_sel = 1, used to drive the SCL signal on the I2C interface
27	0x0 RO	**sda_rd_pre_drive:** Read only bit used to see the status of the SDA signal coming from the I2C logic
26	0x1 RO	**sda_rd_post_drive:** Read only bit used to see the status of the SDA signal coming from the pad
25	0x0 RO	**scl_rd_pre_drive:** Read only bit used to see the status of the SCL signal coming from the I2C logic
24	0x1 RO	**scl_rd_post_drive:** Read only bit used to see the status of the SCL signal coming from the pad
23:10	0x0 RO	**Reserved:** Reserved
9	0x0 RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0x0 RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0x0 RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0x0 RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)
5	0x0 RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0x0 RW	**reserved:** reserved

9.14.49 TX transaction counter (I2C_ACK_COUNT)—Offset 818h

TX transaction counter

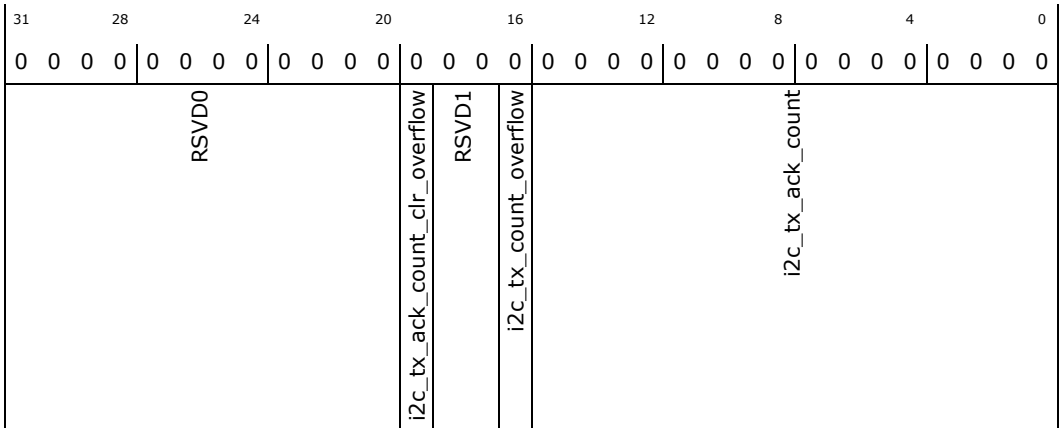
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RSVD0:** Reserved
19	0x0 RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0x0 RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

9.14.50 TX transaction complete interrupt status register (I2C_TX_COMPLETE_INTR_STAT)—Offset 820h

TX transaction has finished interrupt

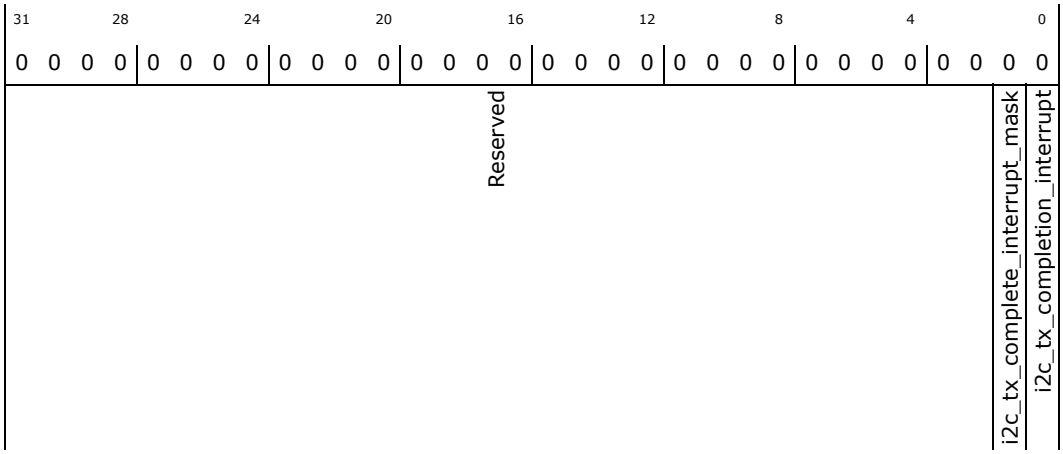
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved:** Reserved
1	0x0 RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0x0 RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

9.14.51 TX transaction complete interrupt clear register (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

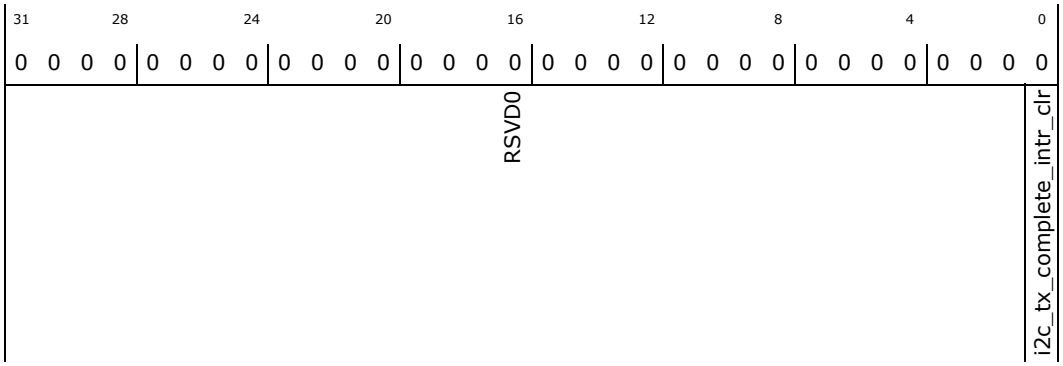
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt

9.15 SIO I2C 2 PCI Configuration Registers

Table 78. Summary of SIO I2C 2 PCI Configuration Registers—0/24/3

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4393	00008086h
4–7h	4	"STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h" on page 4393	00100000h
8–Bh	4	"REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4395	00000000h
C–Fh	4	"CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4396	00800000h
10–13h	4	"BAR -Base Address Register (BAR)—Offset 10h" on page 4396	00000000h
14–17h	4	"BAR1 -Base Address Register1 (BAR1)—Offset 14h" on page 4397	00000000h
2C–2Fh	4	"SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4398	00000000h
30–33h	4	"EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4399	00000000h
34–37h	4	"CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4399	00000000h
3C–3Fh	4	"INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4400	00000100h
80–83h	4	"POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4400	00030001h
84–87h	4	"PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4401	00000008h
F8–FBh	4	"Manufacturers ID (MANID)—Offset F8h" on page 4402	00000000h

9.15.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

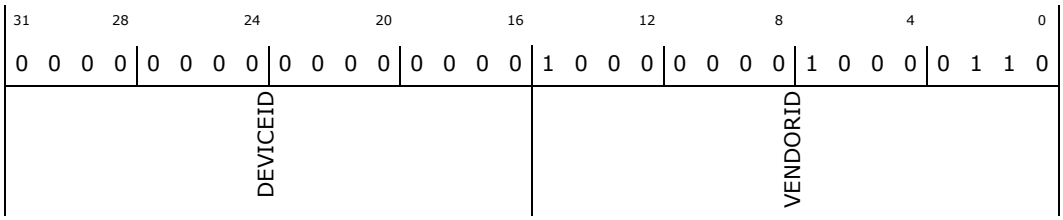
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**DEVICEID:** Device ID identifies the particular AHB/APB device. This is tied to a strap at the top level. Because of tool issues, the HTML files show this field as 0, but the following are the POR values for SoC: LPIO1 DMA: 0x2286 LPIO1 PWM1: 0x2288 LPIO1 PWM2: 0x2289 LPIO1 HSUART1: 0x228A LPIO1 HSUART2: 0x228C LPIO1 SPI1: 0x228E LPIO1 SPI2: 0x2290 LPIO1 SPI3: 0x22AC LPIO2 DMA: 0x22C0 LPIO2 I2C1: 0x22C1 LPIO2 I2C2: 0x22C2 LPIO2 I2C3: 0x22C3 LPIO2 I2C4: 0x22C4 LPIO2 I2C5: 0x22C5 LPIO2 I2C6: 0x22C6 LPIO2 I2C7: 0x22C7 For the final word on this, please see Ray Ng's SoC RevID and DevID HAS on Infofactory: https://ifcollaborate.intel.com/IFC/getdoc.aspx?docbase=InfoFactoryKBandchronid=09005ffd80e84b43andver=CURRENTandqepop=false
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap the top level.

9.15.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

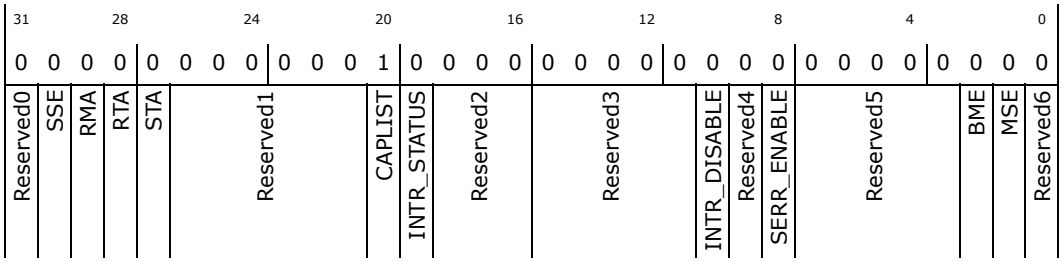
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved0:** Reserved
30	0x0 RW/1C	**SSE:** This bit is set when a device sends an DO_SERR message, and the SERR# Enable bit in the Command register is 1
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric PortReceived Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27	0x0 RW/1C	**STA:** The Bridge sets this bit whenever it responds to a transaction with CA abort. If the SERR# Enable bit is set, the Bridge sets the Signaled System Error bit and sends an DO_SERR message on the IOSF Sideband.
26:21	0x0 RO	**Reserved1:** Reserved
20	0x1 RO	**CAPLIST:** Capabilities List: Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt .i.e Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.. Reset value of this bit is 0.
9	0x0 RO	**Reserved4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: If both SERR# Enable and the Unsupported Request Reporting Enable (URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0x0 RO	**Reserved6:** Reserved

9.15.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

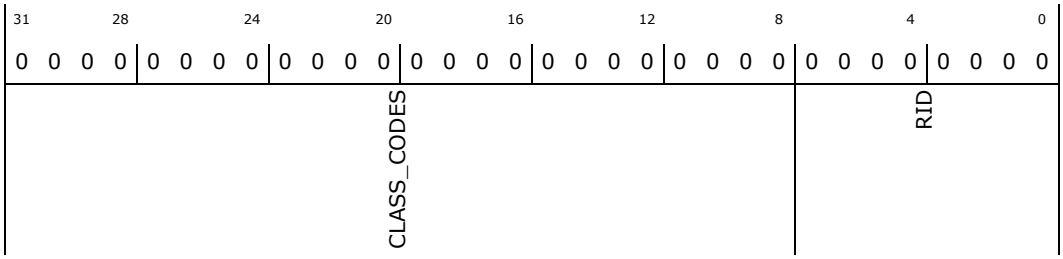
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

9.15.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

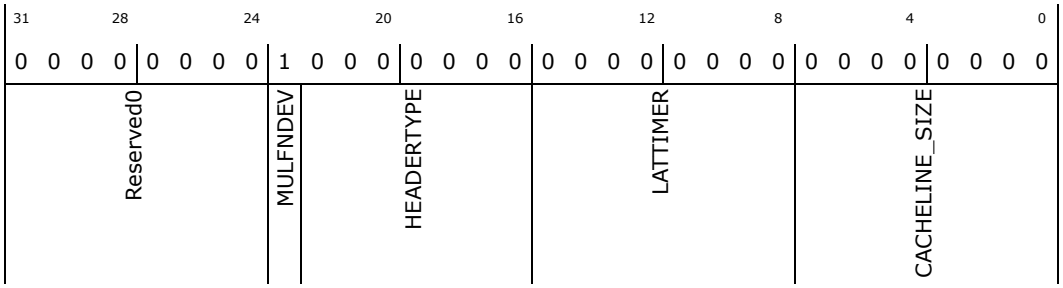
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + Ch

Default: 00800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x1 RO	**MULFNDEV:** Multi Function Device: This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. Value of 1 indicates multifunction device value of 0 indicates single function device
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	0x0 RO	**LATTIMER:** Latency Timer: Doesn.t apply to PCI Express. Hardwired to 00h.
7:0	0x0 RW	**CACHELINE_SIZE:** Cache Line Size: Doesn.t apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

9.15.5 BAR -Base Address Register (BAR)—Offset 10h

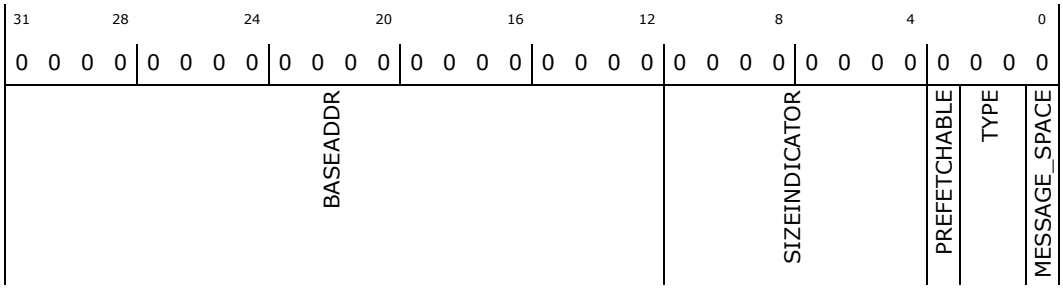
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the AHB device memory space. Taken from Strap values as 1's. Please note that for DMA this field goes from [31:14], or 16kbyte, and the SIZEINDICATOR field goes from [13:4].
11:4	0x0 RO	**SIZEINDICATOR:** Size Indicator Read Only: Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0x0 RO	**TYPE:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.15.6 BAR1 -Base Address Register1 (BAR1)—Offset 14h

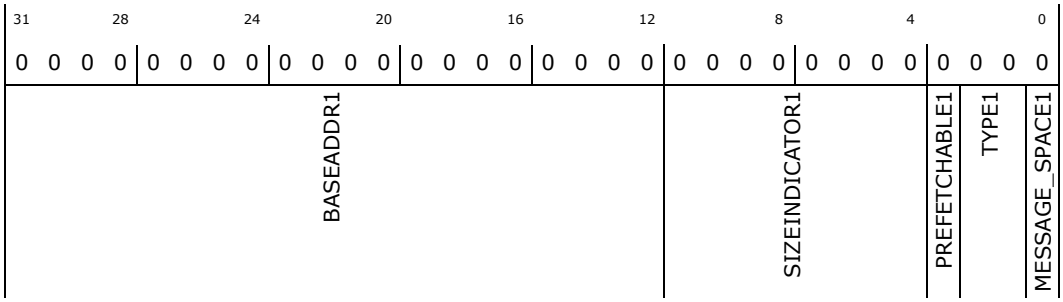
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	0x0 RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not
2:1	0x0 RO	**TYPE1:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.15.7 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

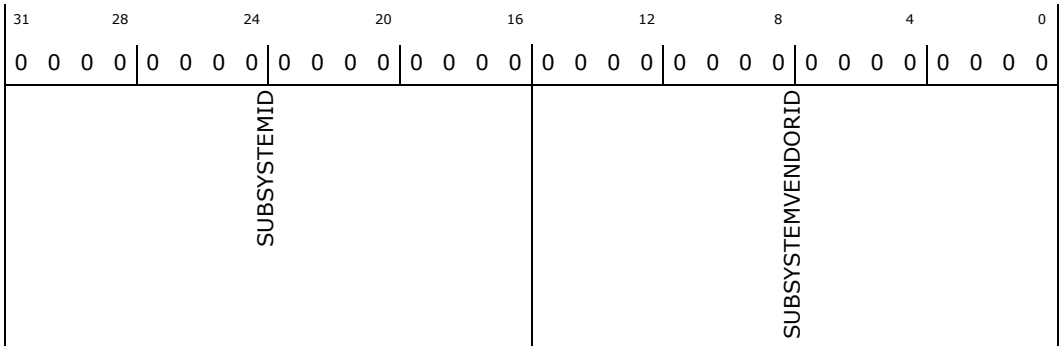
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

9.15.8 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

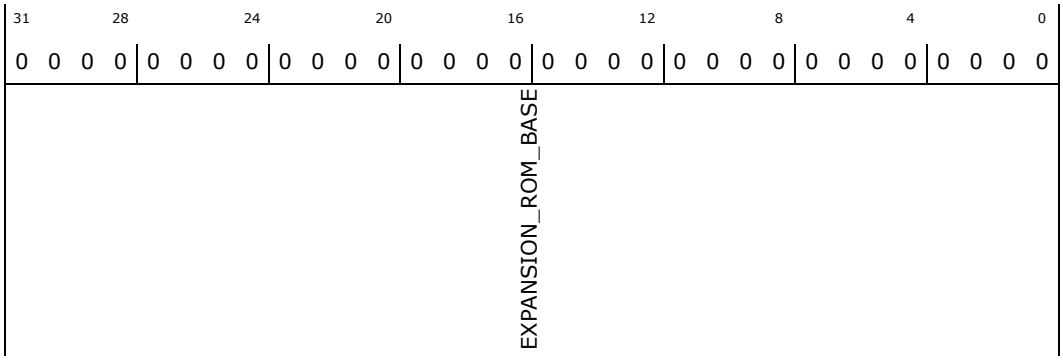
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** A value of all zeros indicates no support for expansion ROM.

9.15.9 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

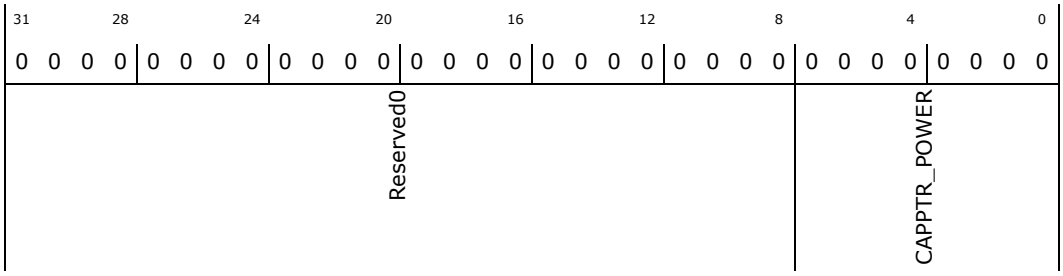
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x0 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

9.15.10 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

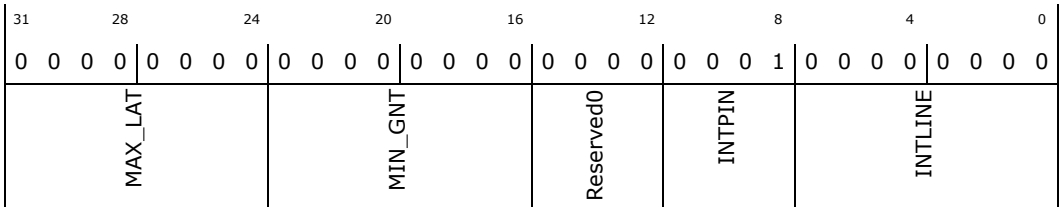
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

9.15.11 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

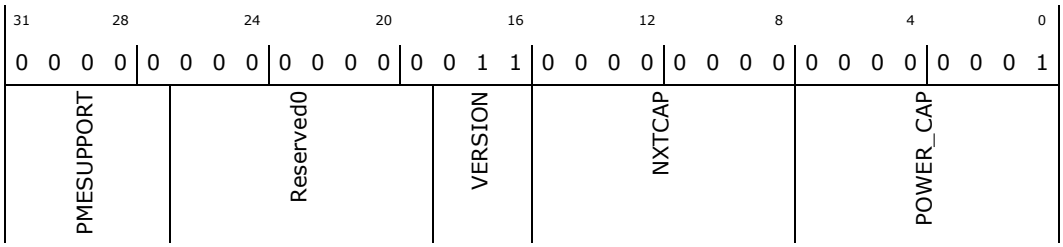
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** PME_Support - This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

9.15.12 PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

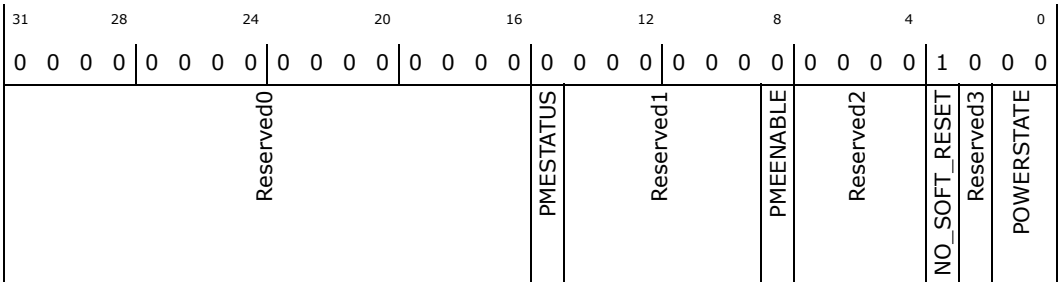
PMECTRLSTATUS - PME Control and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

9.15.13 Manufacturers ID (MANID)—Offset F8h

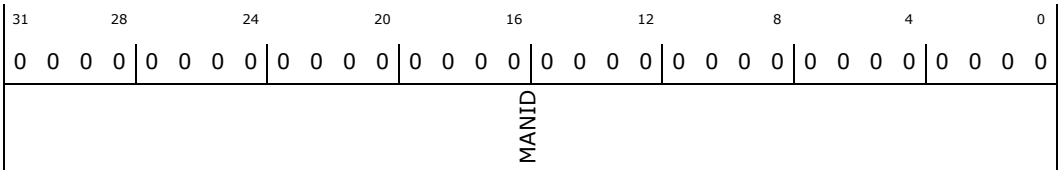
Manufacturers ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:3] + F8h

Default: 00000000h

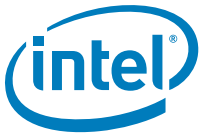


Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: This register is brought out as straps to the top level.

9.16 SIO I2C 2 Memory Mapped I/O Registers

Table 79. Summary of SIO I2C 2 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 4407	0000007Fh
4–7h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 4408	00001055h
8–Bh	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 4409	00000055h
C–Fh	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 4409	00000001h
10–13h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 4410	00000000h
14–17h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 4411	00000190h
18–1Bh	4	"Standard Speed I2C Clock SCL Low Count Register. (IC_SS_SCL_LCNT)—Offset 18h" on page 4412	000001D6h
1C–1Fh	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 4412	0000003Ch
20–23h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 4413	00000082h
24–27h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 4414	0000000Ch
28–2Bh	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 4414	00000020h
2C–2Fh	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 4415	00000000h
30–33h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 4416	000008FFh
34–37h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 4417	00000000h
38–3Bh	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 4418	00000010h
3C–3Fh	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 4419	00000010h
40–43h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 4420	00000000h
44–47h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 4420	00000000h
48–4Bh	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 4421	00000000h
4C–4Fh	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 4422	00000000h
50–53h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 4422	00000000h
54–57h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 4423	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
58–5Bh	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 4423	00000000h
5C–5Fh	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 4424	00000000h
60–63h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 4425	00000000h
64–67h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 4425	00000000h
68–6Bh	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 4426	00000000h
6C–6Fh	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 4426	00000000h
70–73h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 4427	00000006h
74–77h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 4428	00000000h
78–7Bh	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 4428	00000000h
7C–7Fh	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 4429	00000001h
80–83h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 4430	00000000h
84–87h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 4431	00000000h
88–8Bh	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 4432	00000000h
8C–8Fh	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 4432	00000000h
90–93h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 4433	00000000h
94–97h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 4434	00000064h
98–9Bh	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 4434	00000001h
9C–9Fh	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 4435	00000000h
A0–A3h	4	"SS/FS Mode Spike Length Register (IC_FS_SPKLEN)—Offset A0h" on page 4436	00000005h
A4–A7h	4	"HS Mode Spike Length Register (IC_HS_SPKLEN)—Offset A4h" on page 4436	00000002h
F4–F7h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 4437	00FFFFEEh
F8–FBh	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 4438	3131352Ah
FC–FFh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 4439	44570140h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
800–803h	4	"Clock params register (CLOCK_PARAMS)—Offset 800h" on page 4439	00000000h
804–807h	4	"software reset (RESETS)—Offset 804h" on page 4440	00000000h
808–80Bh	4	"General purpose register (GENERAL)—Offset 808h" on page 4440	55000000h
818–81Bh	4	"TX transaction counter (I2C_ACK_COUNT)—Offset 818h" on page 4442	00000000h
820–823h	4	"TX transaction complete interrupt status register (I2C_TX_COMPLETE_INTR_STAT)—Offset 820h" on page 4443	00000000h
824–827h	4	"TX transaction complete interrupt clear register (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 4443	00000000h

9.16.1 I2C Control Register (IC_CON)—Offset 0h

I2C Control Register

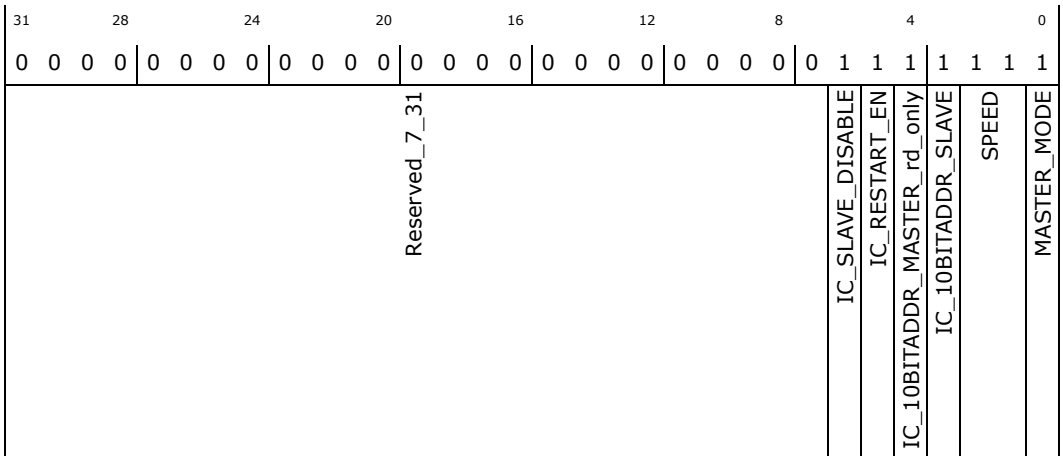
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 0000007Fh



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RW	**Reserved_7_31:** Reserved
6	0x1 RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	0x1 RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master.When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: Sending a START BYTE. Performing any high-speed mode operation. Performing direction changes in combined format mode. Performing a read operation with a 10-bit address
4	0x1 RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register
3	0x1 RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0x3 RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	0x1 RW	**MASTER_MODE:** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

9.16.2 I2C Target Address Register (IC_TAR)—Offset 4h

I2C Target Address Register

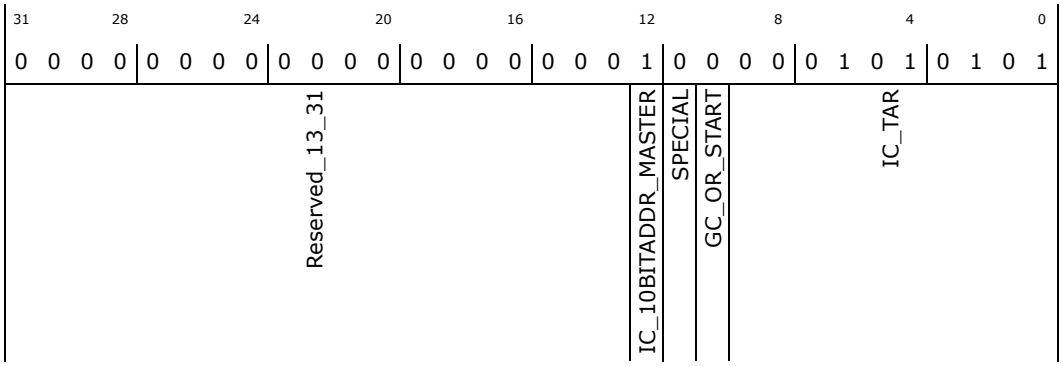
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00001055h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Reserved_13_31:** Reserved
12	0x1 RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master. This bit exists in this register only if the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 1
11	0x0 RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. 0: ignore bit 10 GC_OR_START and use IC_TAR normally. 1: perform special I2C command as specified in GC_OR_START bit
10	0x0 RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.

Bit Range	Default & Access	Field Name (ID): Description
9:0	0x55 RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

9.16.3 I2C Slave Address Register (IC_SAR)—Offset 8h

I2C Slave Address Register

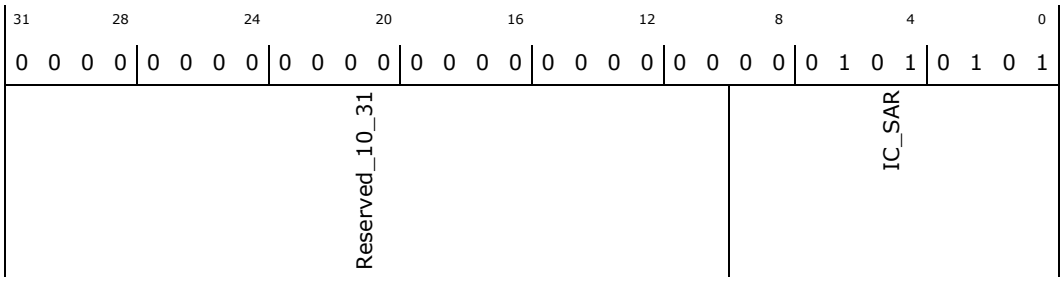
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000055h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**Reserved_10_31:** Reserved
9:0	0x55 RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.16.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

I2C High Speed Master Mode Code Address Register

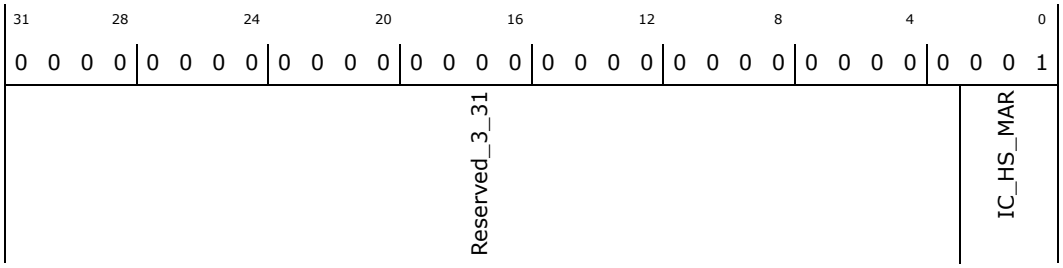
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved_3_31:** Reserved
2:0	0x1 RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.16.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

I2C Rx/Tx Data Buffer and Command Register; this is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO

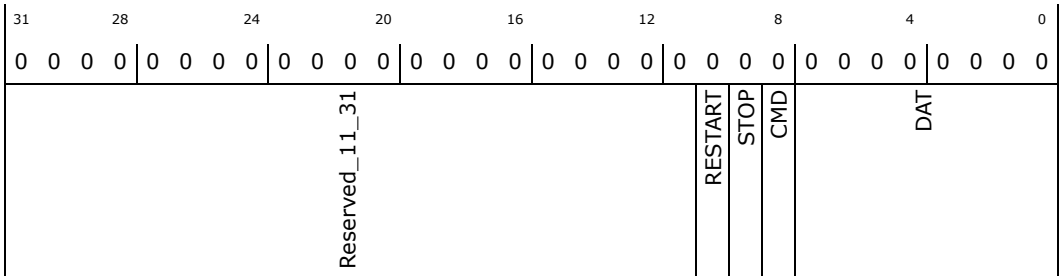
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:11	0x0 RW	**Reserved_11_31:** Reserved
10	0x0 RW	**RESTART:** RESTART
9	0x0 RW	**STOP:** STOP
8	0x0 RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It controls only the direction when it acts as a master. 1 = Read. 0 = Write
7:0	0x0 RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. However, when you read this register, these bits return the value of data received on the DW_apb_i2c interface.

9.16.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

Standard Speed I2C Clock SCL High Count Register.

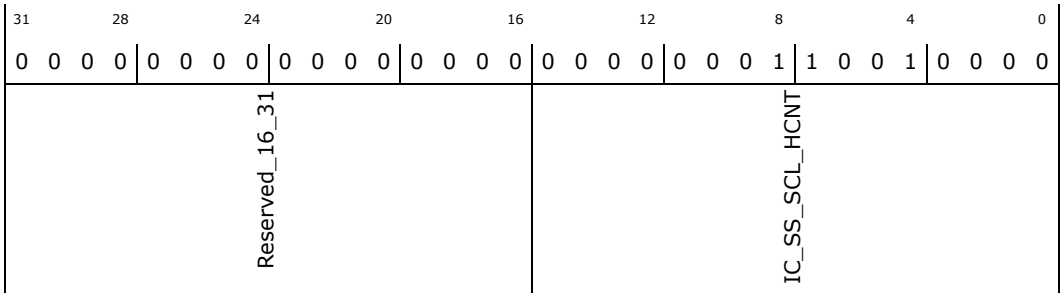
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000190h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x190 RW	**IC_SS_SCL_HCNT:** Standard Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.16.7 Standard Speed I2C Clock SCL Low Count Register. (IC_SS_SCL_LCNT)—Offset 18h

Standard Speed I2C Clock SCL Low Count Register.

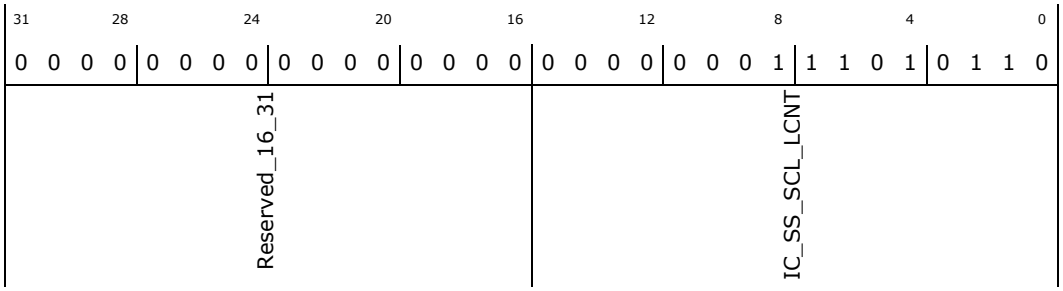
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 000001D6h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x1d6 RW	**IC_SS_SCL_LCNT:** Standard Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.16.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

Fast Speed I2C Clock SCL High Count Register

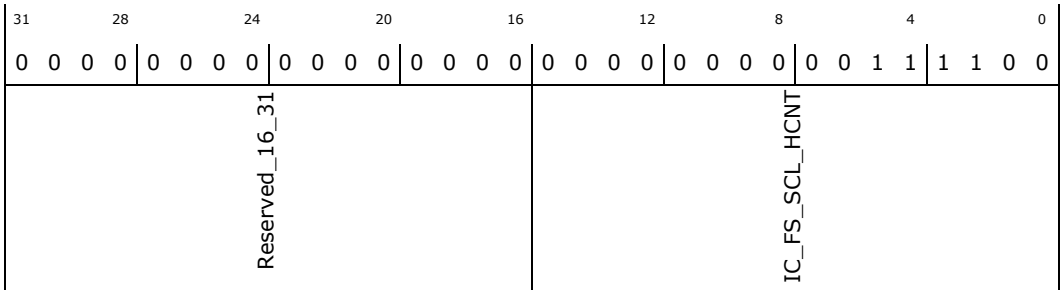
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 0000003Ch



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x3c RW	**IC_FS_SCL_HCNT:** Fast Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.16.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

Fast Speed I2C Clock SCL Low Count Register

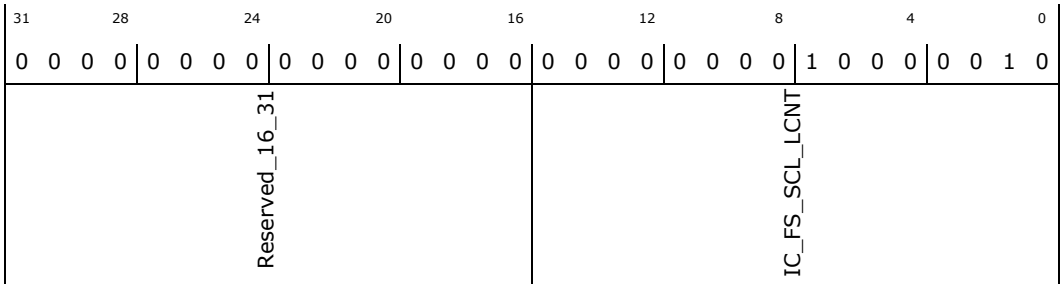
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000082h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x82 RW	**IC_FS_SCL_LCNT:** Fast Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.16.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

High Speed I2C Clock SCL High Count Register

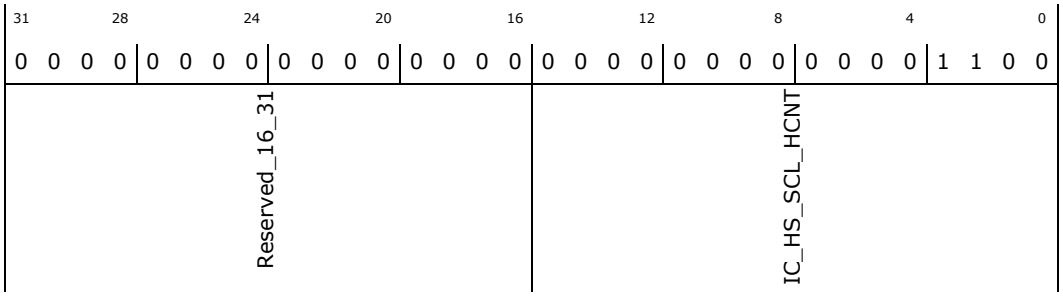
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 0000000Ch



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0xc RW	**IC_HS_SCL_HCNT:** High Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.16.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

High Speed I2C Clock SCL Low Count Register

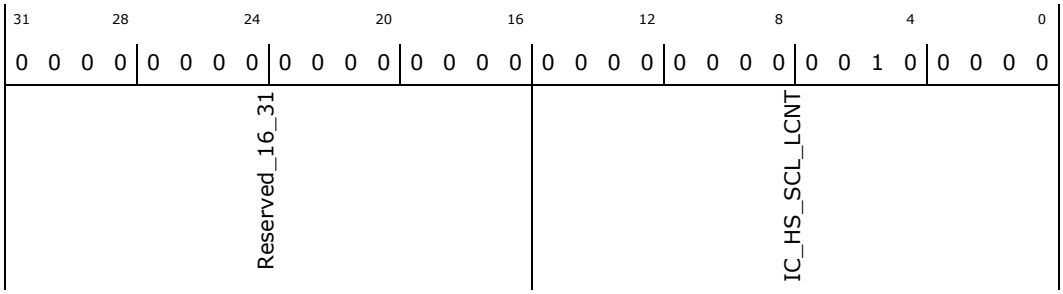
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000020h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x20 RW	**IC_HS_SCL_LCNT:** High Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.16.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

I2C Interrupt Status Register

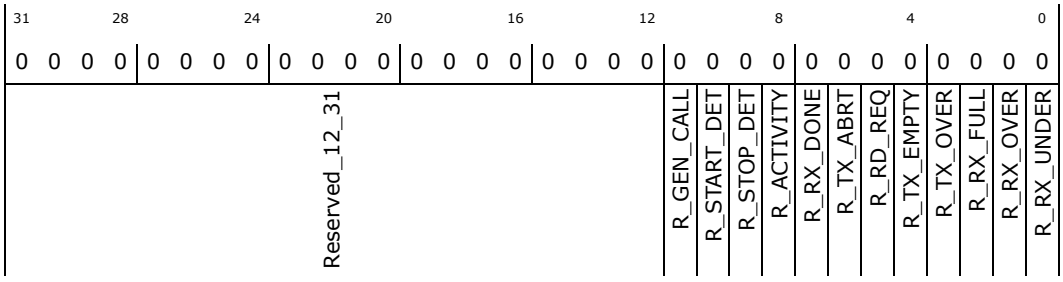
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x0 RO	**R_GEN_CALL:** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0x0 RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0x0 RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0x0 RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0x0 RO	**R_TX_ABRT:** This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0x0 RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.
4	0x0 RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0x0 RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0x0 RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0x0 RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0x0 RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

9.16.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

I2C Interrupt Mask Register

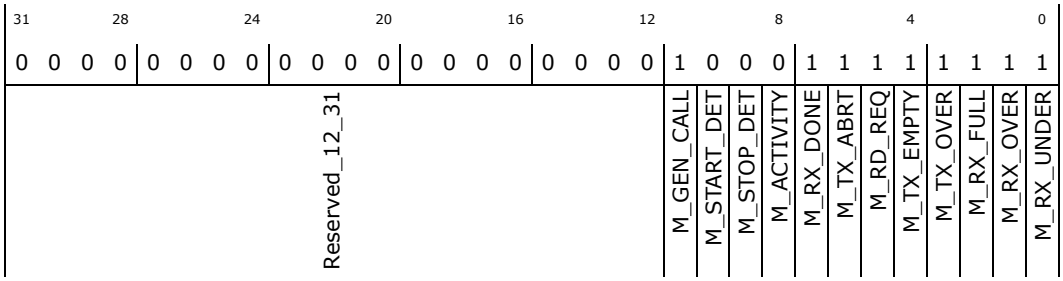
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 000008FFh



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x1 RW	**M_GEN_CALL:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
10	0x0 RW	**M_START_DET:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
9	0x0 RW	**M_STOP_DET:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
8	0x0 RW	**M_ACTIVITY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
7	0x1 RW	**M_RX_DONE:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
6	0x1 RW	**M_TX_ABRT:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
5	0x1 RW	**M_RD_REQ:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
4	0x1 RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
3	0x1 RW	**M_TX_OVER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
2	0x1 RW	**M_RX_FULL:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
1	0x1 RW	**M_RX_OVER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
0	0x1 RW	**M_RX_UNDER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.

9.16.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

I2C Raw Interrupt Status Register

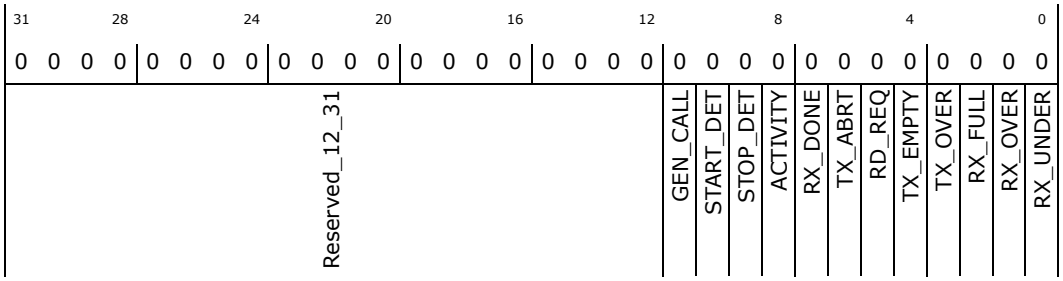
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x0 RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT
10	0x0 RO	**START_DET:** Same as in reg_IC_INTR_STAT
9	0x0 RO	**STOP_DET:** Same as in reg_IC_INTR_STAT
8	0x0 RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT
7	0x0 RO	**RX_DONE:** Same as in reg_IC_INTR_STAT
6	0x0 RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT
5	0x0 RO	**RD_REQ:** Same as in reg_IC_INTR_STAT
4	0x0 RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT
3	0x0 RO	**TX_OVER:** Same as in reg_IC_INTR_STAT
2	0x0 RO	**RX_FULL:** Same as in reg_IC_INTR_STAT
1	0x0 RO	**RX_OVER:** Same as in reg_IC_INTR_STAT
0	0x0 RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT

9.16.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

I2C Receive FIFO Threshold Register

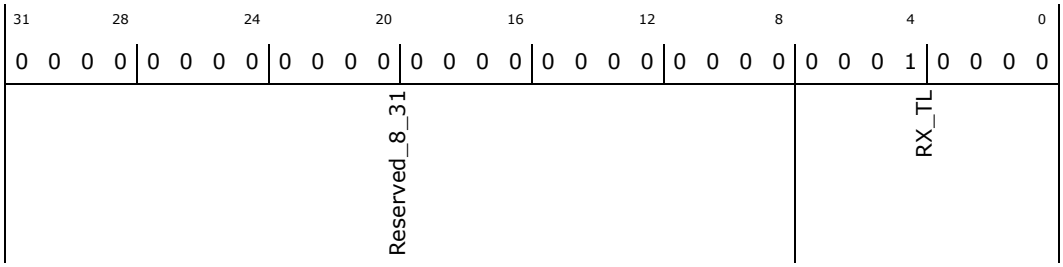
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x10 RW	**RX_TL:** Receive FIFO Threshold Level. The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

9.16.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

I2C Transmit FIFO Threshold Register

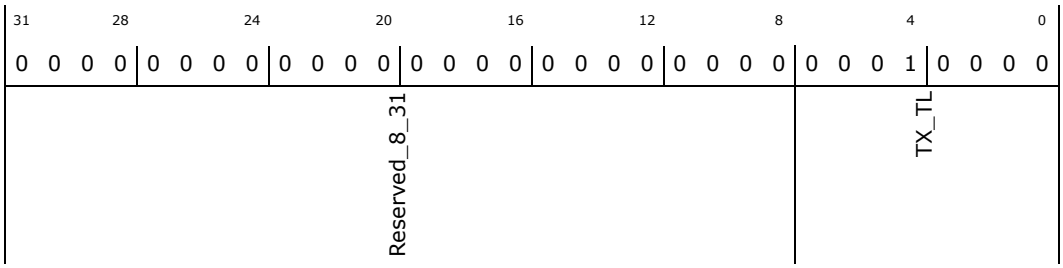
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x10 RW	**TX_TL:** Transmit FIFO Threshold Level. Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

9.16.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

Clear Combined and Individual Interrupt Register

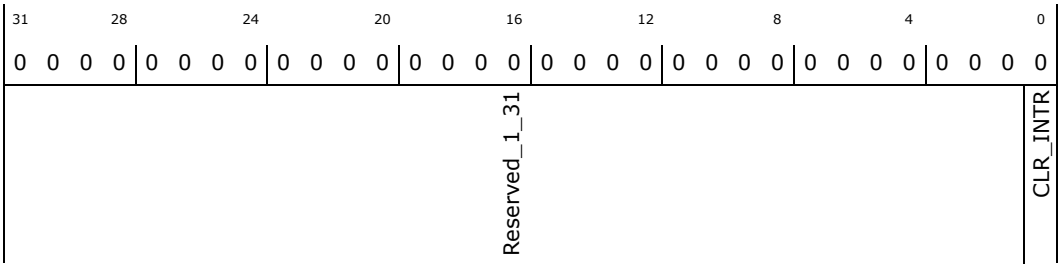
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

9.16.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

Clear RX_UNDER Interrupt Register

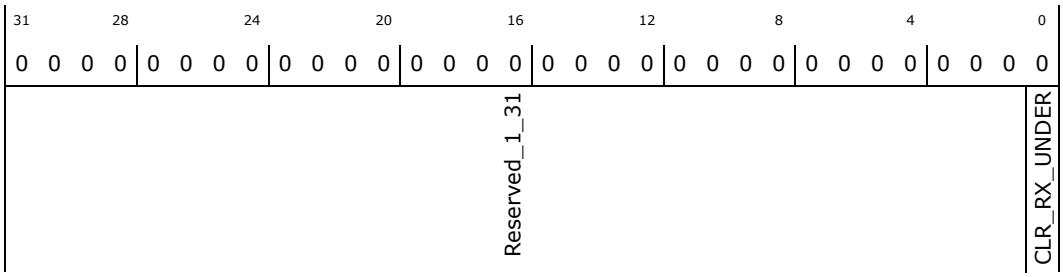
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

9.16.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

Clear RX_OVER Interrupt Register

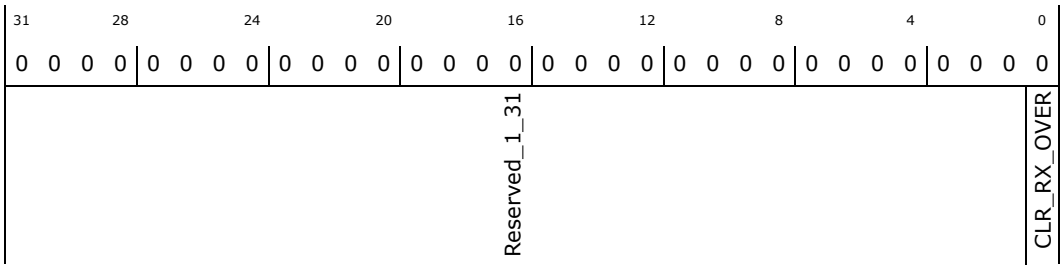
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

9.16.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

Clear TX_OVER Interrupt Register

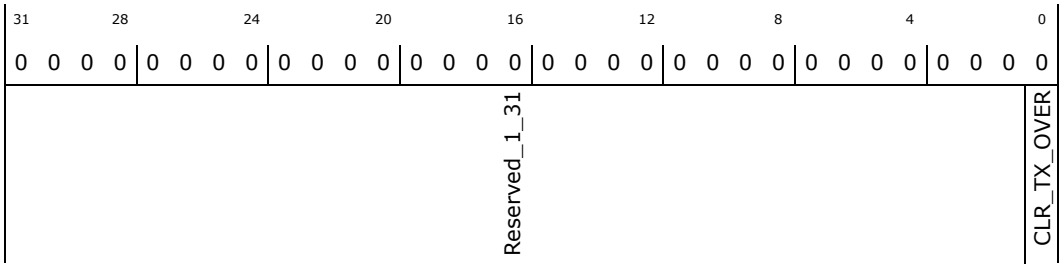
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

9.16.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

Clear RD_REQ Interrupt Register

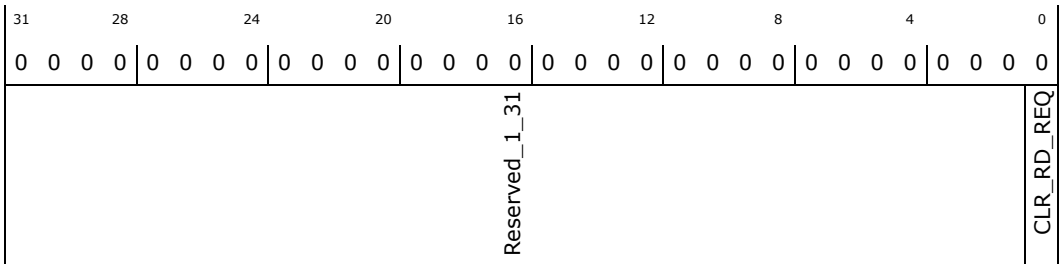
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

9.16.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

Clear TX_ABRT Interrupt Register

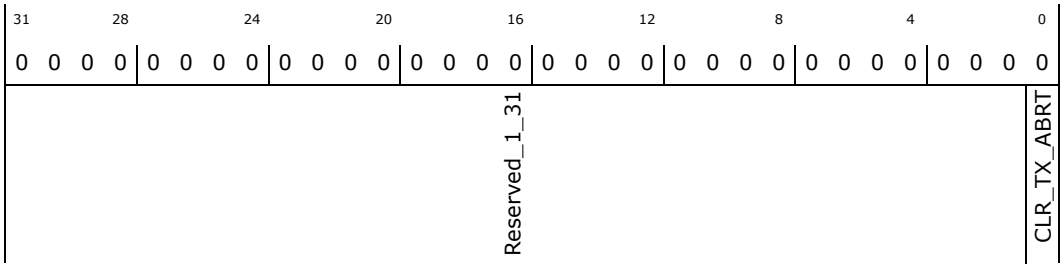
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

9.16.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

Clear RX_DONE Interrupt Register

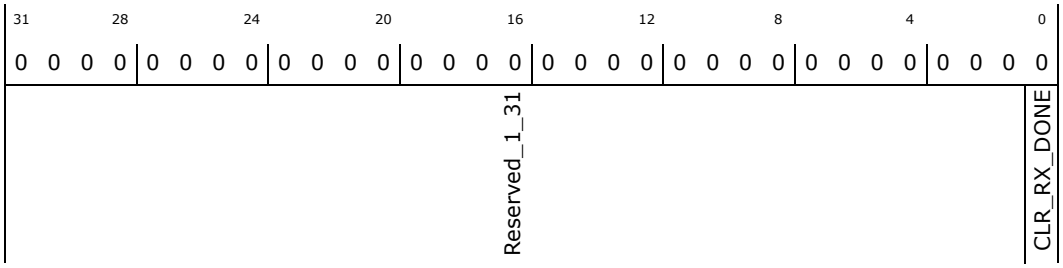
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

9.16.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

Clear ACTIVITY Interrupt Register

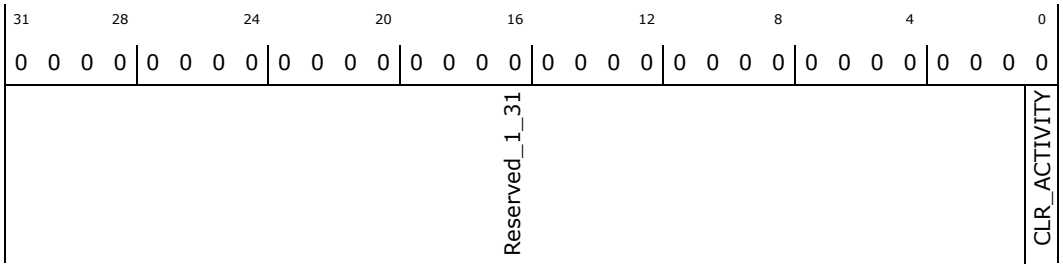
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

9.16.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

Clear STOP_DET Interrupt Register

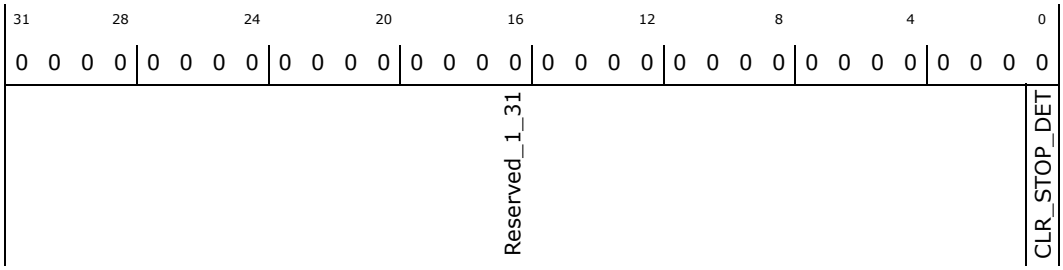
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

9.16.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

Clear START_DET Interrupt Register

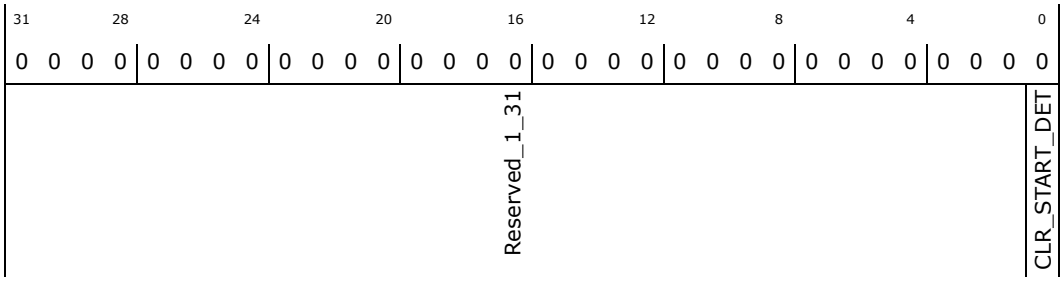
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

9.16.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

Clear GEN_CALL Interrupt Register

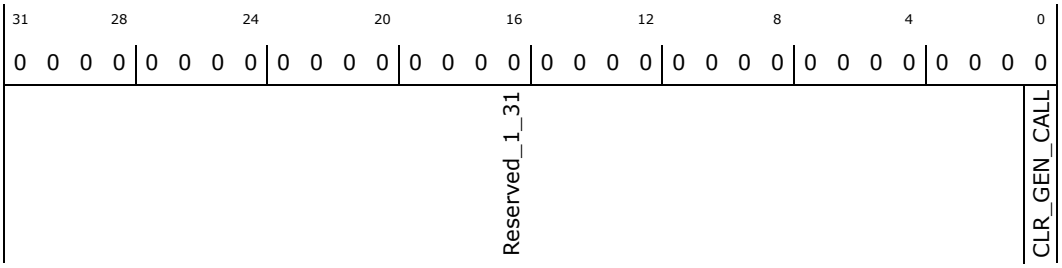
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

9.16.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

I2C Enable Register

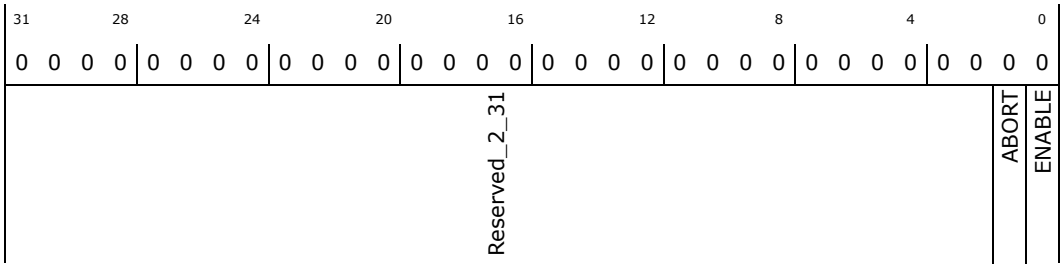
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved_2_31:** Reserved
1	0x0 WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.
0	0x0 RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) 1: Enables DW_apb_i2c

9.16.29 I2C Status Register (IC_STATUS)—Offset 70h

I2C Status Register

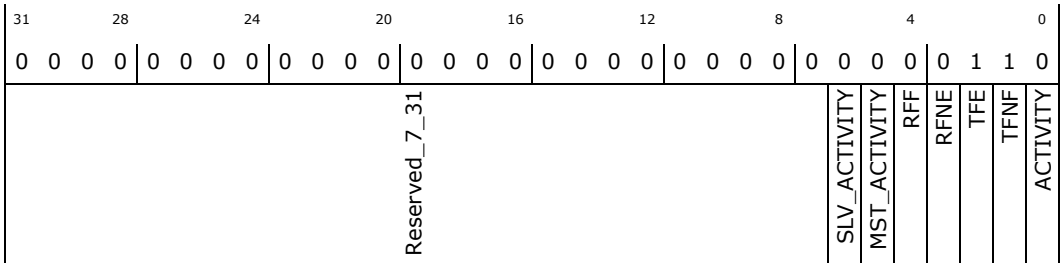
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000006h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RW	**Reserved_7_31:** Reserved
6	0x0 RO	**SLV_ACTIVITY:** Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0x0 RO	**MST_ACTIVITY:** Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RO	**RFF:** Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0x0 RO	**RFNE:** Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.
2	0x1 RO	**TFE:** Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	0x1 RO	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0x0 RO	**ACTIVITY:** I2C Activity Status

9.16.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

I2C Transmit FIFO Level Register

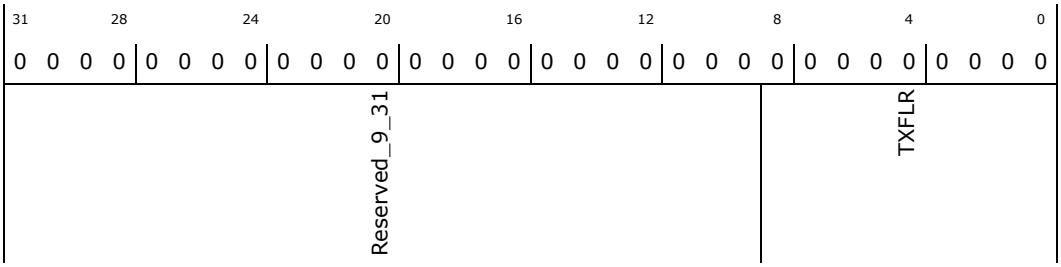
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved_9_31:** Reserved
8:0	0x0 RO	**TXFLR:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

9.16.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

I2C Receive FIFO Level Register

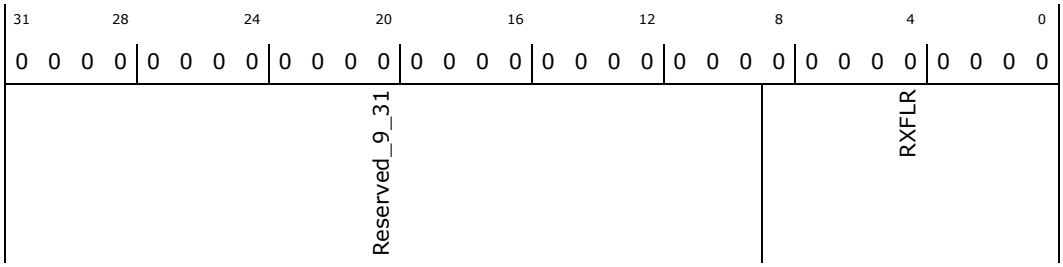
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved_9_31:** Reserved
8:0	0x0 RO	**RXFLR:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

9.16.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

I2C SDA Hold Time Length Register

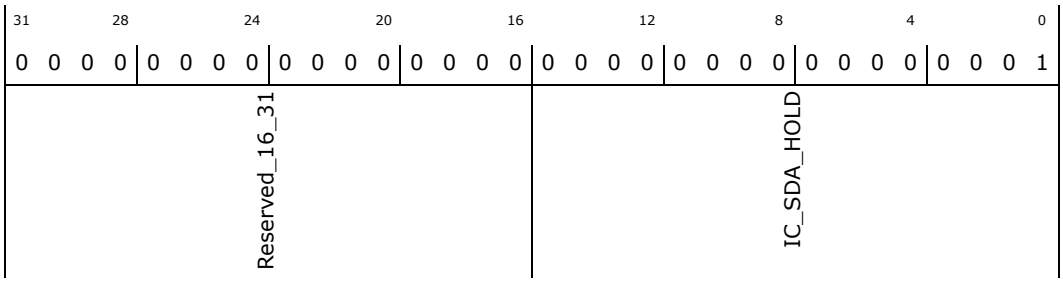
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x1 RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

9.16.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

I2C Transmit Abort Source Register

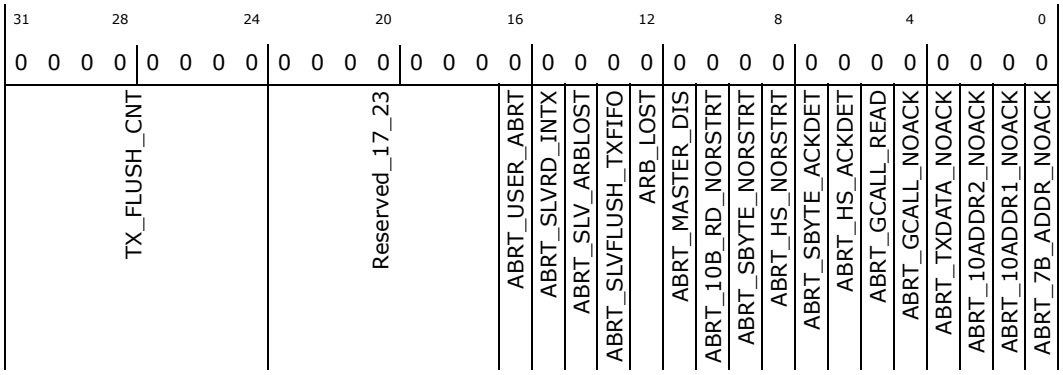
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0x0 RW	**Reserved_17_23:** Reserved
16	0x0 RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0x0 RO	**ABRT_SLVRD_INTX:** 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0x0 RO	**ABRT_SLV_ARBLOST:** 1: Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0x0 RO	**ABRT_SLVFLUSH_TXFIFO:** 1: Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0x0 RO	**ARB_LOST:** 1: Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0x0 RO	**ABRT_MASTER_DIS:** 1: User tries to initiate a Master operation with the Master mode disabled.
10	0x0 RO	**ABRT_10B_RD_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RO	**ABRT_SBYTE_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0x0 RO	**ABRT_HS_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0x0 RO	**ABRT_SBYTE_ACKDET:** 1: Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
6	0x0 RO	**ABRT_HS_ACKDET:** 1: Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
5	0x0 RO	**ABRT_GCALL_READ:** 1: DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0x0 RO	**ABRT_GCALL_NOACK:** 1: DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0x0 RO	**ABRT_TXDATA_NOACK:** 1: This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0x0 RO	**ABRT_10ADDR2_NOACK:** 1: Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0x0 RO	**ABRT_10ADDR1_NOACK:** 1: Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0x0 RO	**ABRT_7B_ADDR_NOACK:** 1: Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

9.16.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

Generate Slave Data NACK Register

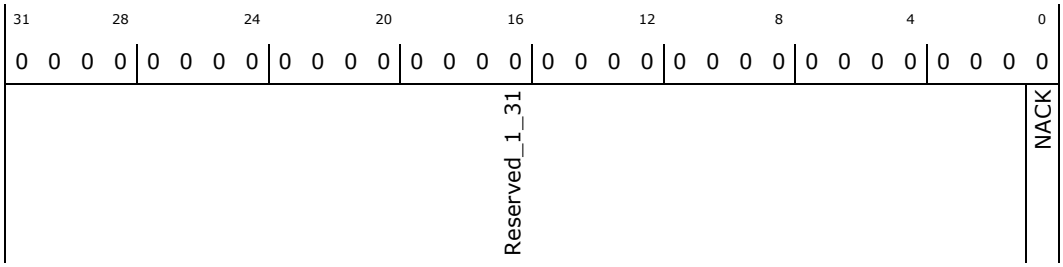
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RW	**NACK:** Generate NACK. This NACK generation only occurs when DW_apb_i2c is a slavereceiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. 1 = generate NACK after data byte received 0 = generate NACK/ACK normally

9.16.35 DMA Control Register (IC_DMA_CR)—Offset 88h

DMA Control Register

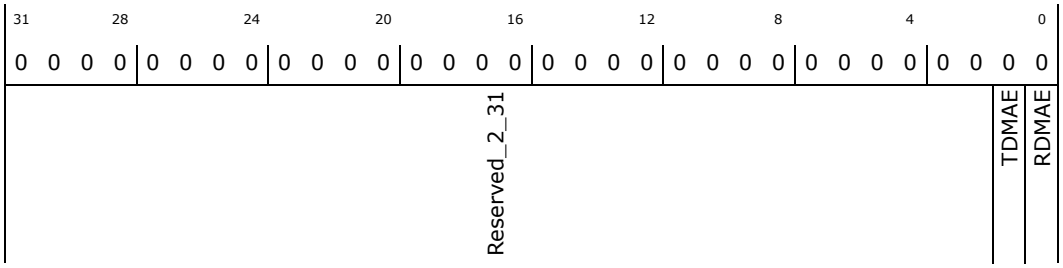
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved_2_31:** Reserved
1	0x0 RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel. 0 = Transmit DMA disabled 1 = Transmit DMA enabled
0	0x0 RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. 0 = Receive DMA disabled 1 = Receive DMA enabled

9.16.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

DMA Transmit Data Level Register

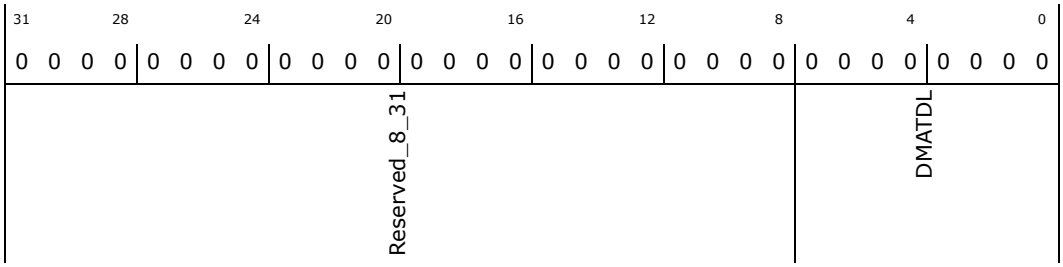
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x0 RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

9.16.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

I2C Receive Data Level Register

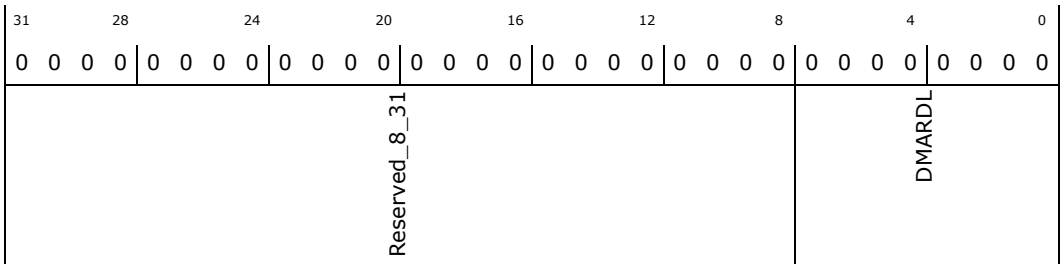
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x0 RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

9.16.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

I2C SDA Setup Register

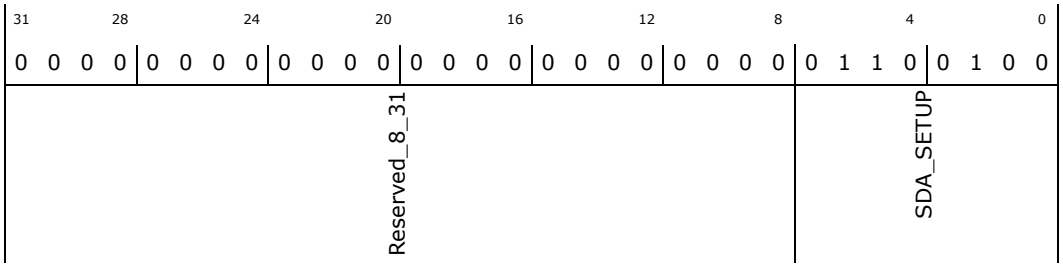
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000064h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x64 RW	**SDA_SETUP:** SDA Setup. It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

9.16.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

I2C ACK General Call Register

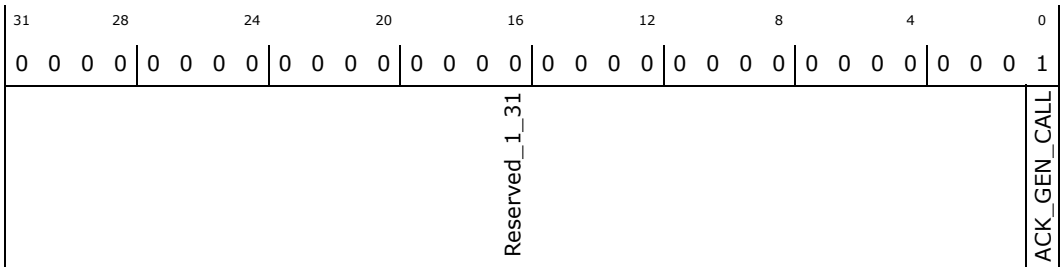
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x1 RW	**ACK_GEN_CALL:** ACK General Call. When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

9.16.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

I2C Enable Status Register

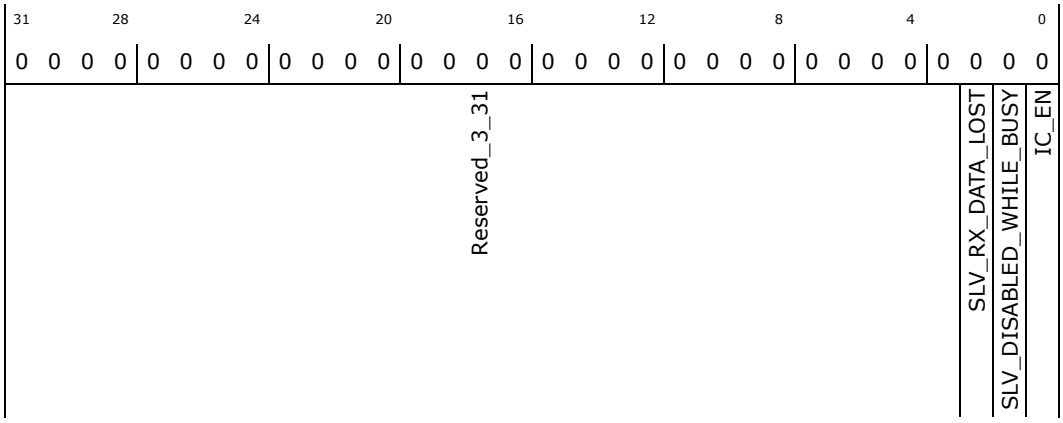
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved_3_31:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0x0 RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0x0 RO	**IC_EN:** ic_en Status. This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

9.16.41 SS/FS Mode Spike Length Register (IC_FS_SPKLEN)—Offset A0h

SS/FS Mode Spike Length Register

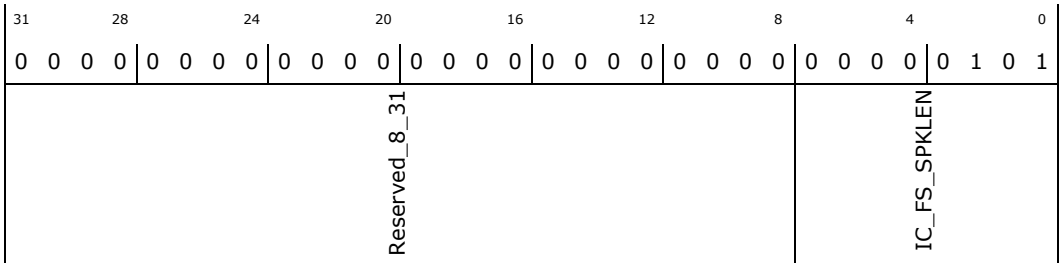
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000005h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x5 RW	**IC_FS_SPKLEN:** Maximum length (in ic_clk cycles) of suppressed spikes in SS and FS modes

9.16.42 HS Mode Spike Length Register (IC_HS_SPKLEN)—Offset A4h

HS Mode Spike Length Register

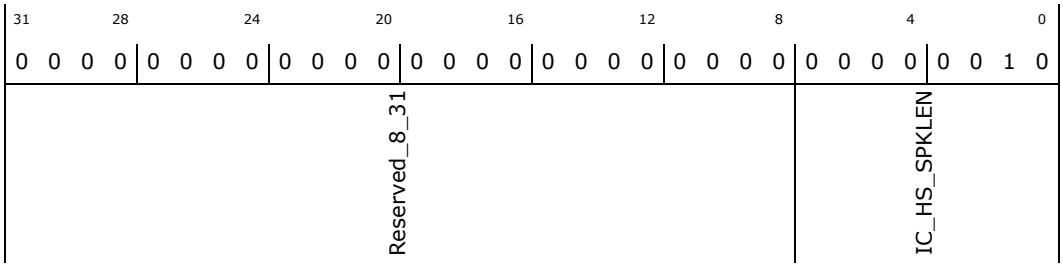
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x2 RW	**IC_HS_SPKLEN:** Maximum length (in ic_clk cycles) of suppressed spikes in HS mode

9.16.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

Component Parameter Register 1

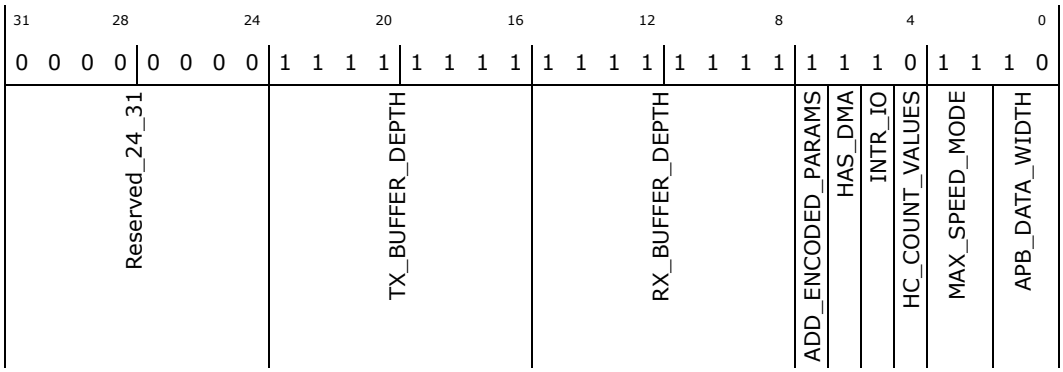
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00FFFFEEh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved_24_31:** Reserved
23:16	0xff RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	0xff RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	0x1 RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	0x1 RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	0x1 RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0x0 RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	0x3 RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	0x2 RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

9.16.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

I2C Component Version Register

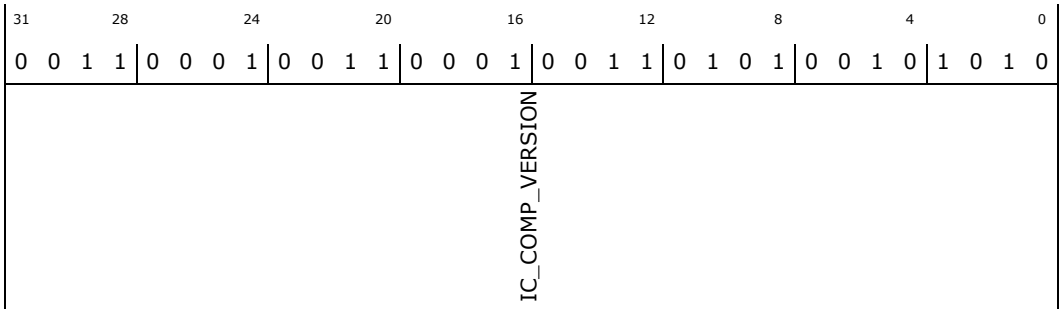
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 3131352Ah



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x3131352a RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes

9.16.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

I2C Component Type Register

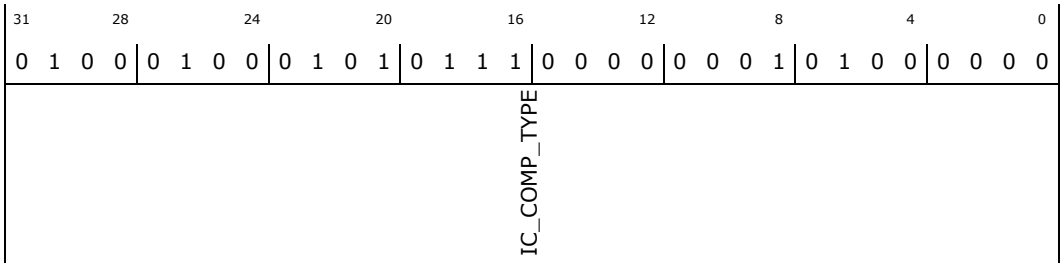
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 44570140h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x44570140 RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

9.16.46 Clock params register (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

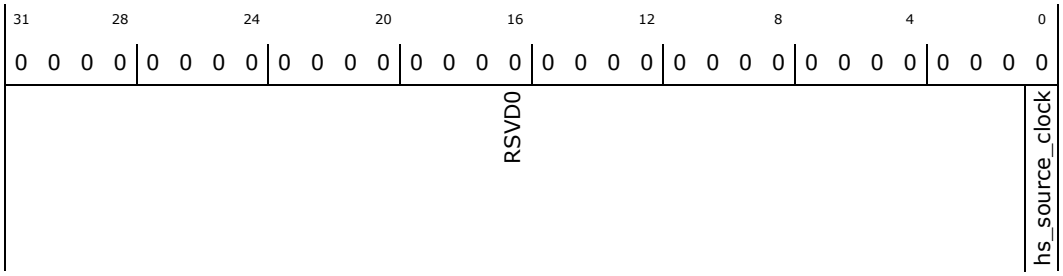
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz 1 -133MHz (high-speed operation compatible)

9.16.47 software reset (RESETS)—Offset 804h

software reset

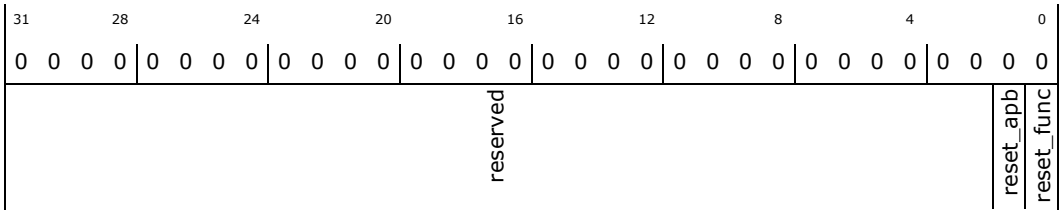
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (reserved):** Reserved
1	0x0 RW	**reset_apb:** reset the apb domain
0	0x0 RW	**reset_func:** reset the func clock domain

9.16.48 General purpose register (GENERAL)—Offset 808h

General purpose register

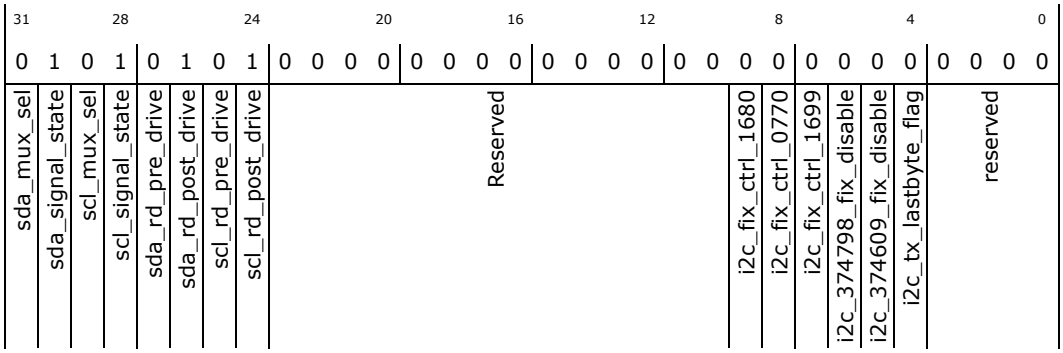
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 55000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**sda_mux_sel:** This bit selects the driver for the SDA signal: 1 = sda_signal_state, 0 = I2C logic
30	0x1 RW	**sda_signal_state:** This bit is used when sda_mux_sel = 1, used to drive the SDA signal on the I2C interface
29	0x0 RW	**scl_mux_sel:** This bit selects the driver for the SCL signal: 1 = scl_signal_state, 0 = I2C logic
28	0x1 RW	**scl_signal_state:** This bit is used when scl_mux_sel = 1, used to drive the SCL signal on the I2C interface
27	0x0 RO	**sda_rd_pre_drive:** Read only bit used to see the status of the SDA signal coming from the I2C logic
26	0x1 RO	**sda_rd_post_drive:** Read only bit used to see the status of the SDA signal coming from the pad
25	0x0 RO	**scl_rd_pre_drive:** Read only bit used to see the status of the SCL signal coming from the I2C logic
24	0x1 RO	**scl_rd_post_drive:** Read only bit used to see the status of the SCL signal coming from the pad
23:10	0x0 RO	**Reserved:** Reserved
9	0x0 RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0x0 RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0x0 RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0x0 RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)
5	0x0 RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0x0 RW	**reserved:** reserved

9.16.49 TX transaction counter (I2C_ACK_COUNT)—Offset 818h

TX transaction counter

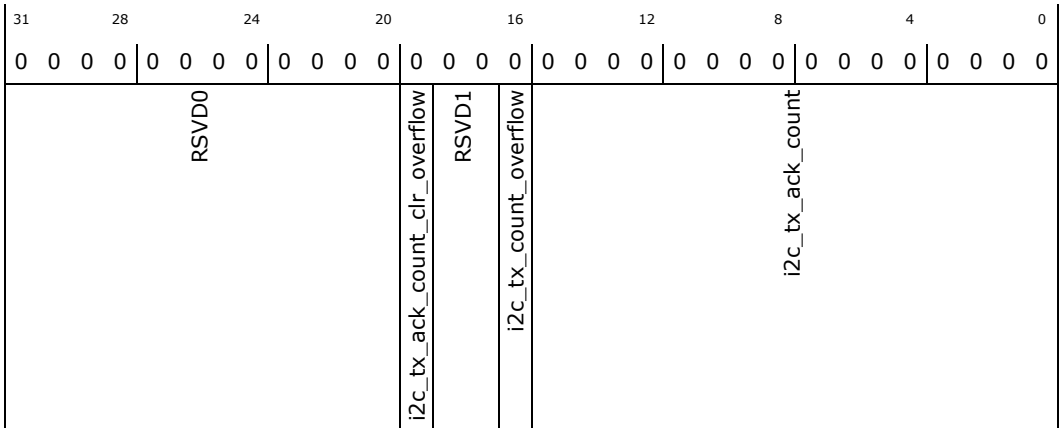
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RSVD0:** Reserved
19	0x0 RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0x0 RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

9.16.50 TX transaction complete interrupt status register (I2C_TX_COMPLETE_INTR_STAT)—Offset 820h

TX transaction has finished interrupt

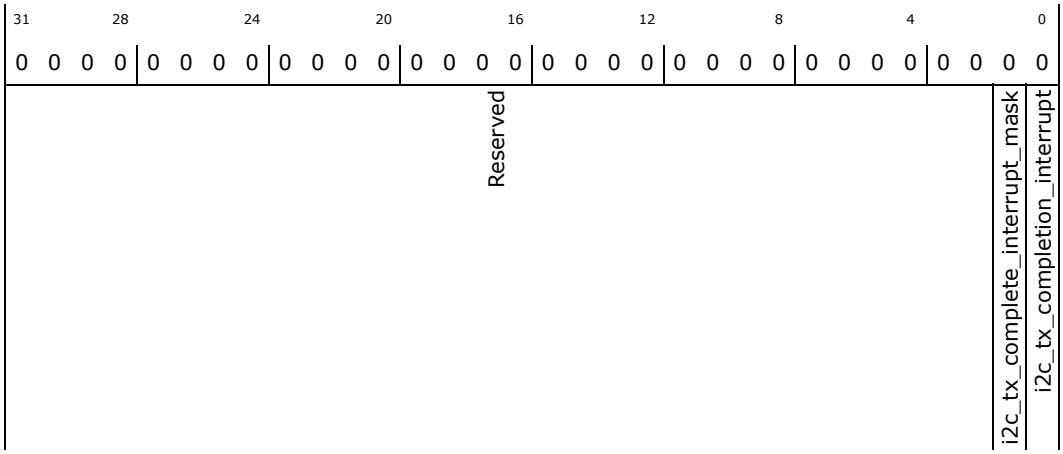
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved:** Reserved
1	0x0 RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0x0 RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

9.16.51 TX transaction complete interrupt clear register (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

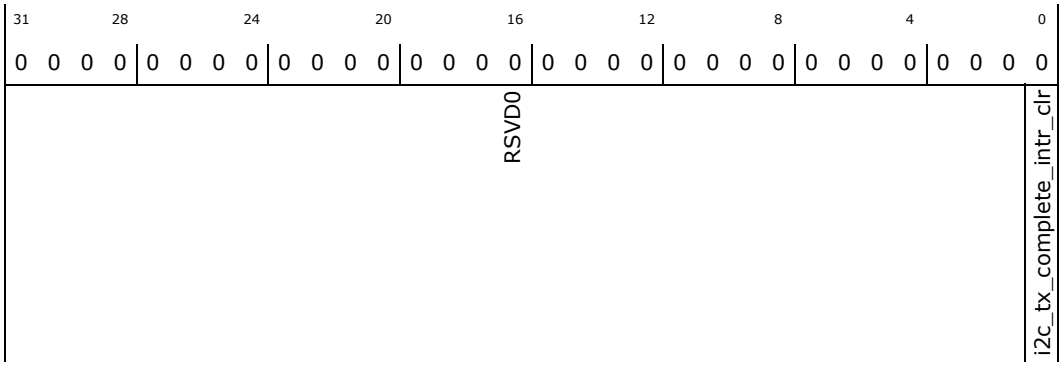
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt

9.17 SIO I2C 3 PCI Configuration Registers

Table 80. Summary of SIO I2C 3 PCI Configuration Registers—0/24/4

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4447	00008086h
4–7h	4	"STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h" on page 4447	00100000h
8–Bh	4	"REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4449	00000000h
C–Fh	4	"CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4450	00800000h
10–13h	4	"BAR -Base Address Register (BAR)—Offset 10h" on page 4450	00000000h
14–17h	4	"BAR1 -Base Address Register1 (BAR1)—Offset 14h" on page 4451	00000000h
2C–2Fh	4	"SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4452	00000000h
30–33h	4	"EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4453	00000000h
34–37h	4	"CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4453	00000000h
3C–3Fh	4	"INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4454	00000100h
80–83h	4	"POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4454	00030001h
84–87h	4	"PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4455	00000008h
F8–FBh	4	"Manufacturers ID (MANID)—Offset F8h" on page 4456	00000000h

9.17.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

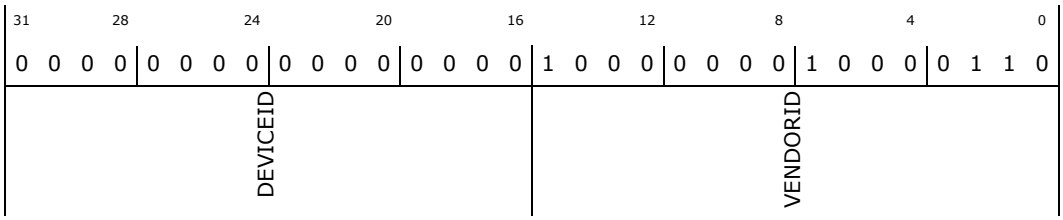
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**DEVICEID:** Device ID identifies the particular AHB/APB device. This is tied to a strap at the top level. Because of tool issues, the HTML files show this field as 0, but the following are the POR values for SoC: LPIO1 DMA: 0x2286 LPIO1 PWM1: 0x2288 LPIO1 PWM2: 0x2289 LPIO1 HSUART1: 0x228A LPIO1 HSUART2: 0x228C LPIO1 SPI1: 0x228E LPIO1 SPI2: 0x2290 LPIO1 SPI3: 0x22AC LPIO2 DMA: 0x22C0 LPIO2 I2C1: 0x22C1 LPIO2 I2C2: 0x22C2 LPIO2 I2C3: 0x22C3 LPIO2 I2C4: 0x22C4 LPIO2 I2C5: 0x22C5 LPIO2 I2C6: 0x22C6 LPIO2 I2C7: 0x22C7 For the final word on this, please see Ray Ng's SoC RevID and DevID HAS on Infofactory: https://ifcollaborate.intel.com/IFC/getdoc.aspx?docbase=InfoFactoryKBandchronid=09005ffd80e84b43andver=CURRENTandqepop=false
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap the top level.

9.17.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

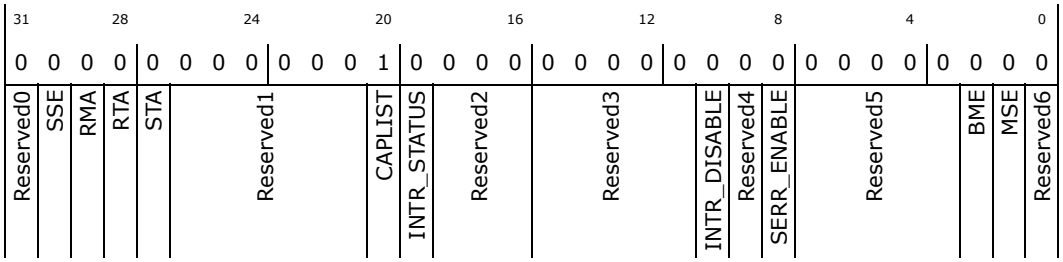
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved0:** Reserved
30	0x0 RW/1C	**SSE:** This bit is set when a device sends an DO_SERR message, and the SERR# Enable bit in the Command register is 1
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric PortReceived Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27	0x0 RW/1C	**STA:** The Bridge sets this bit whenever it responds to a transaction with CA abort. If the SERR# Enable bit is set, the Bridge sets the Signaled System Error bit and sends an DO_SERR message on the IOSF Sideband.
26:21	0x0 RO	**Reserved1:** Reserved
20	0x1 RO	**CAPLIST:** Capabilities List: Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt .i.e Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.. Reset value of this bit is 0.
9	0x0 RO	**Reserved4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: If both SERR# Enable and the Unsupported Request Reporting Enable (URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0x0 RO	**Reserved6:** Reserved

9.17.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

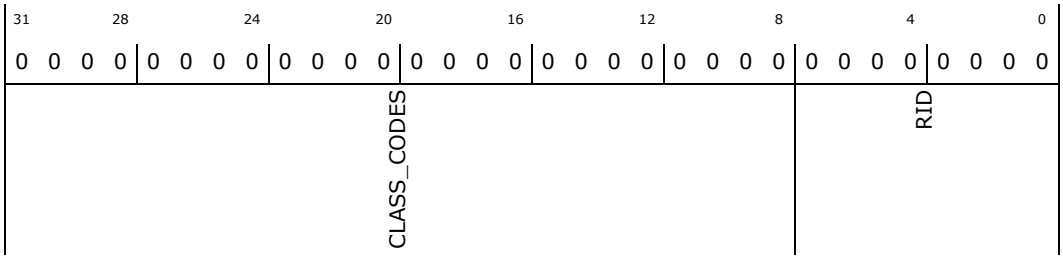
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

9.17.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

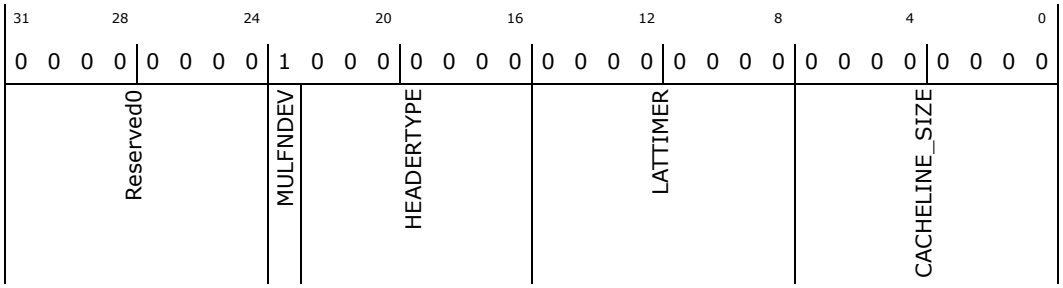
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + Ch

Default: 00800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x1 RO	**MULFNDEV:** Multi Function Device: This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. Value of 1 indicates multifunction device value of 0 indicates single function device
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	0x0 RO	**LATTIMER:** Latency Timer: Doesn.t apply to PCI Express. Hardwired to 00h.
7:0	0x0 RW	**CACHELINE_SIZE:** Cache Line Size: Doesn.t apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

9.17.5 BAR -Base Address Register (BAR)—Offset 10h

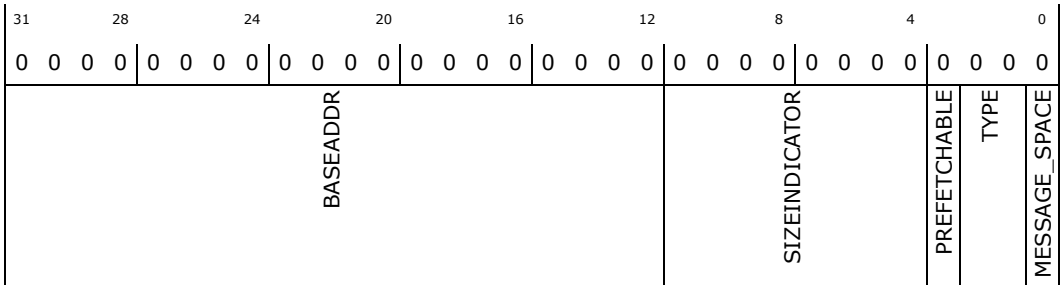
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the AHB device memory space. Taken from Strap values as 1's. Please note that for DMA this field goes from [31:14], or 16kbyte, and the SIZEINDICATOR field goes from [13:4].
11:4	0x0 RO	**SIZEINDICATOR:** Size Indicator Read Only: Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0x0 RO	**TYPE:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.17.6 BAR1 -Base Address Register1 (BAR1)—Offset 14h

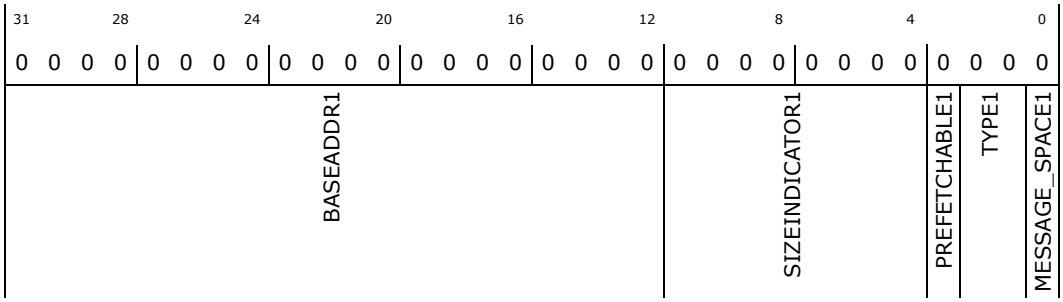
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	0x0 RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not
2:1	0x0 RO	**TYPE1:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.17.7 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

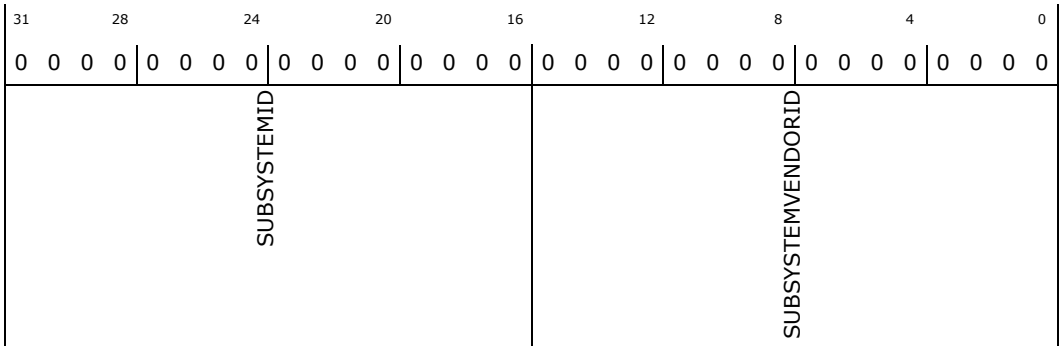
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

9.17.8 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

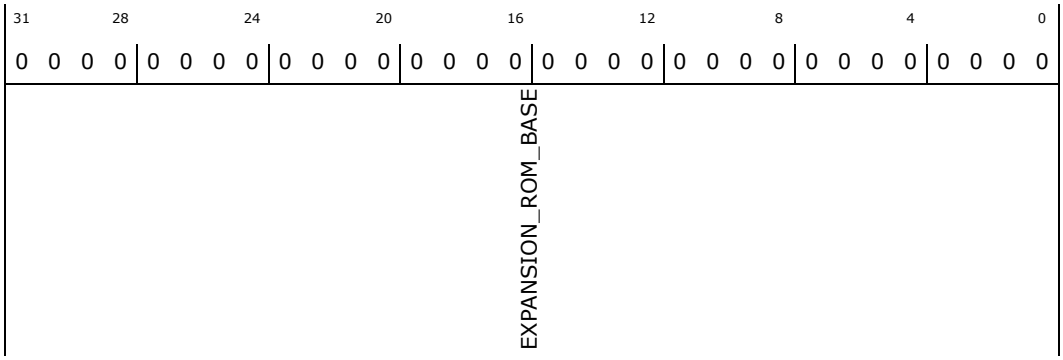
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** A value of all zeros indicates no support for expansion ROM.

9.17.9 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

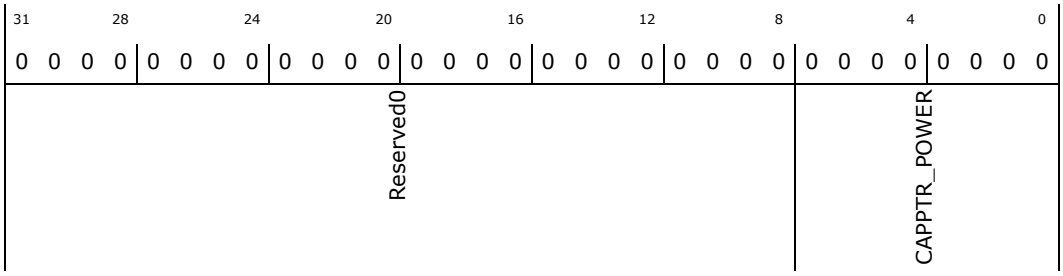
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x0 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

9.17.10 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

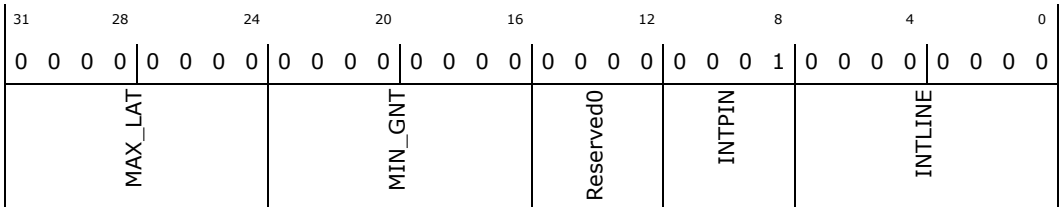
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

9.17.11 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

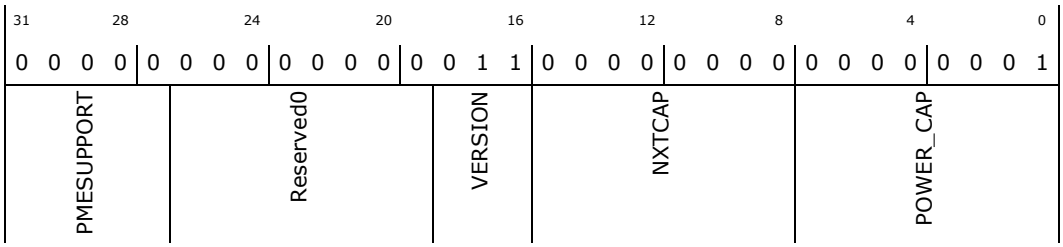
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** PME_Support - This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

9.17.12 PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

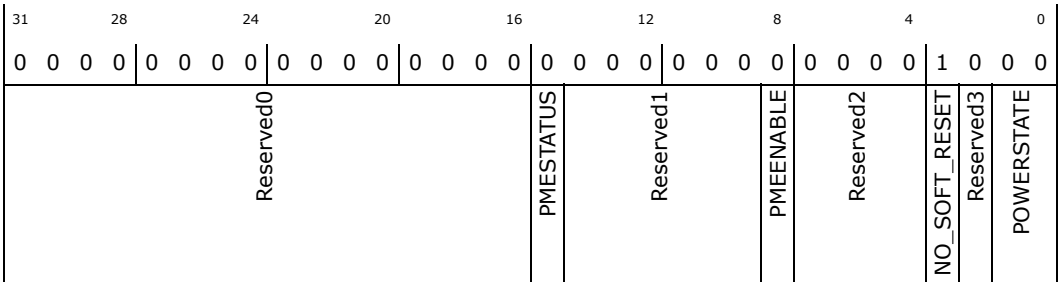
PMECTRLSTATUS - PME Control and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

9.17.13 Manufacturers ID (MANID)—Offset F8h

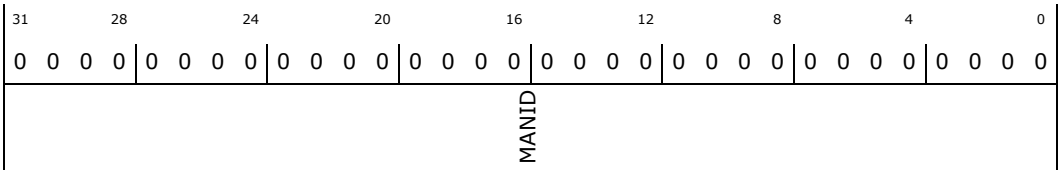
Manufacturers ID

Access Method

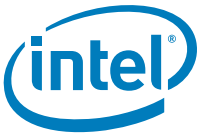
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:4] + F8h

Default: 00000000h



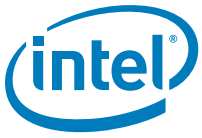
Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: This register is brought out as straps to the top level.



9.18 SIO I2C 3 Memory Mapped Registers

Table 81. Summary of SIO I2C 3 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 4461	0000007Fh
4–7h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 4462	00001055h
8–Bh	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 4463	00000055h
C–Fh	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 4463	00000001h
10–13h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 4464	00000000h
14–17h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 4465	00000190h
18–1Bh	4	"Standard Speed I2C Clock SCL Low Count Register. (IC_SS_SCL_LCNT)—Offset 18h" on page 4466	000001D6h
1C–1Fh	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 4466	0000003Ch
20–23h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 4467	00000082h
24–27h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 4468	0000000Ch
28–2Bh	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 4468	00000020h
2C–2Fh	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 4469	00000000h
30–33h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 4470	000008FFh
34–37h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 4471	00000000h
38–3Bh	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 4472	00000010h
3C–3Fh	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 4473	00000010h
40–43h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 4474	00000000h
44–47h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 4474	00000000h
48–4Bh	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 4475	00000000h
4C–4Fh	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 4476	00000000h
50–53h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 4476	00000000h
54–57h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 4477	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
58–5Bh	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 4477	00000000h
5C–5Fh	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 4478	00000000h
60–63h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 4479	00000000h
64–67h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 4479	00000000h
68–6Bh	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 4480	00000000h
6C–6Fh	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 4480	00000000h
70–73h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 4481	00000006h
74–77h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 4482	00000000h
78–7Bh	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 4482	00000000h
7C–7Fh	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 4483	00000001h
80–83h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 4484	00000000h
84–87h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 4485	00000000h
88–8Bh	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 4486	00000000h
8C–8Fh	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 4486	00000000h
90–93h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 4487	00000000h
94–97h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 4488	00000064h
98–9Bh	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 4488	00000001h
9C–9Fh	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 4489	00000000h
A0–A3h	4	"SS/FS Mode Spike Length Register (IC_FS_SPKLEN)—Offset A0h" on page 4490	00000005h
A4–A7h	4	"HS Mode Spike Length Register (IC_HS_SPKLEN)—Offset A4h" on page 4490	00000002h
F4–F7h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 4491	00FFFFEEh
F8–FBh	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 4492	3131352Ah
FC–FFh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 4493	44570140h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
800–803h	4	"Clock params register (CLOCK_PARAMS)—Offset 800h" on page 4493	00000000h
804–807h	4	"software reset (RESETS)—Offset 804h" on page 4494	00000000h
808–80Bh	4	"General purpose register (GENERAL)—Offset 808h" on page 4494	55000000h
818–81Bh	4	"TX transaction counter (I2C_ACK_COUNT)—Offset 818h" on page 4496	00000000h
820–823h	4	"TX transaction complete interrupt status register (I2C_TX_COMPLETE_INTR_STAT)—Offset 820h" on page 4497	00000000h
824–827h	4	"TX transaction complete interrupt clear register (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 4497	00000000h

9.18.1 I2C Control Register (IC_CON)—Offset 0h

I2C Control Register

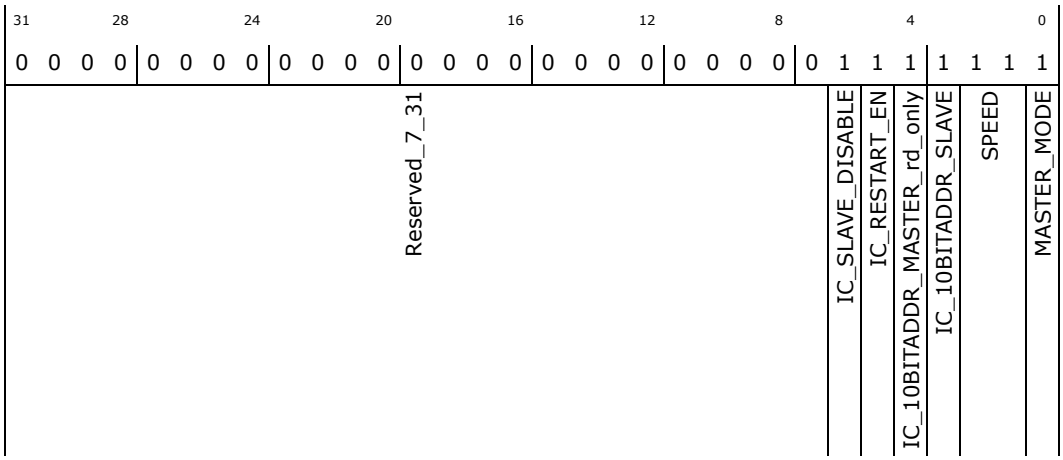
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 0000007Fh



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RW	**Reserved_7_31:** Reserved
6	0x1 RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	0x1 RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master.When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: Sending a START BYTE. Performing any high-speed mode operation. Performing direction changes in combined format mode. Performing a read operation with a 10-bit address
4	0x1 RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register
3	0x1 RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0x3 RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	0x1 RW	**MASTER_MODE:** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

9.18.2 I2C Target Address Register (IC_TAR)—Offset 4h

I2C Target Address Register

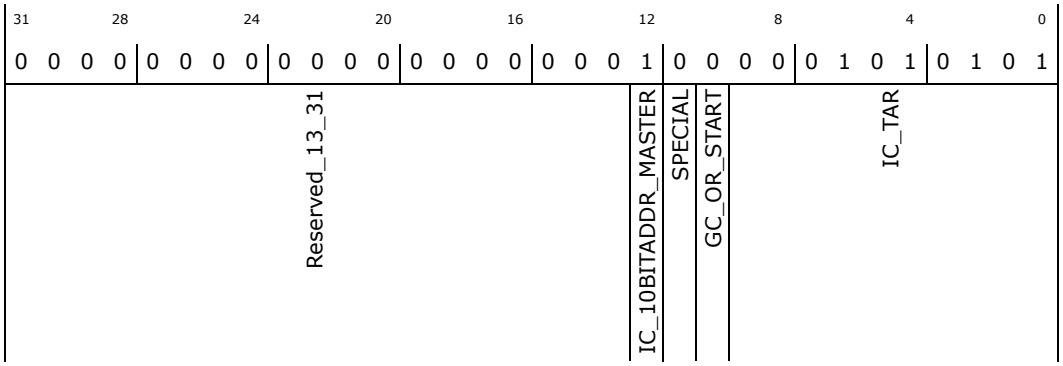
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00001055h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Reserved_13_31:** Reserved
12	0x1 RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master. This bit exists in this register only if the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 1
11	0x0 RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. 0: ignore bit 10 GC_OR_START and use IC_TAR normally. 1: perform special I2C command as specified in GC_OR_START bit
10	0x0 RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.

Bit Range	Default & Access	Field Name (ID): Description
9:0	0x55 RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

9.18.3 I2C Slave Address Register (IC_SAR)—Offset 8h

I2C Slave Address Register

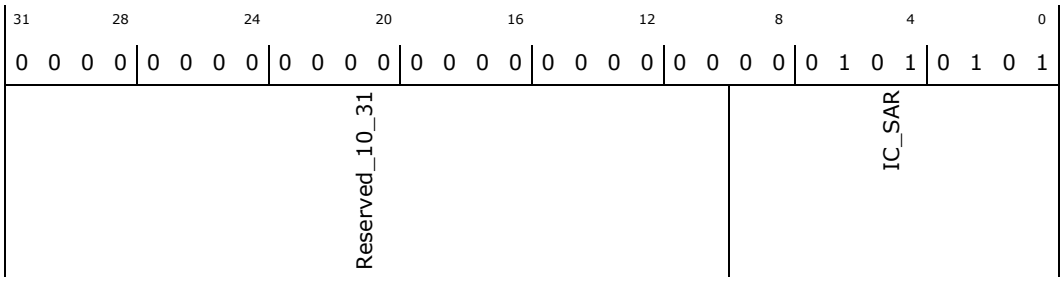
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000055h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**Reserved_10_31:** Reserved
9:0	0x55 RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.18.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

I2C High Speed Master Mode Code Address Register

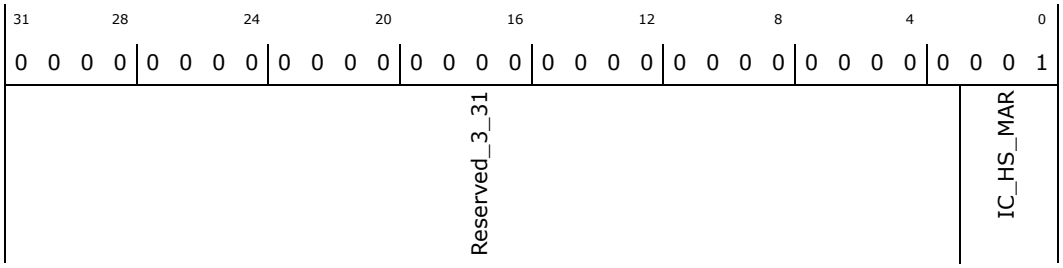
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved_3_31:** Reserved
2:0	0x1 RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.18.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

I2C Rx/Tx Data Buffer and Command Register; this is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO

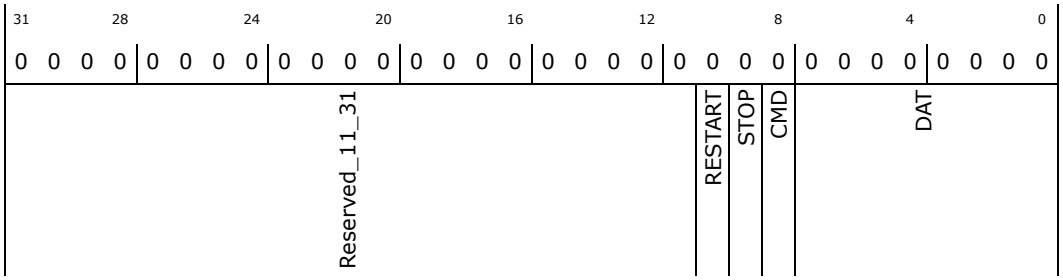
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:11	0x0 RW	**Reserved_11_31:** Reserved
10	0x0 RW	**RESTART:** RESTART
9	0x0 RW	**STOP:** STOP
8	0x0 RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It controls only the direction when it acts as a master. 1 = Read. 0 = Write
7:0	0x0 RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. However, when you read this register, these bits return the value of data received on the DW_apb_i2c interface.

9.18.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

Standard Speed I2C Clock SCL High Count Register.

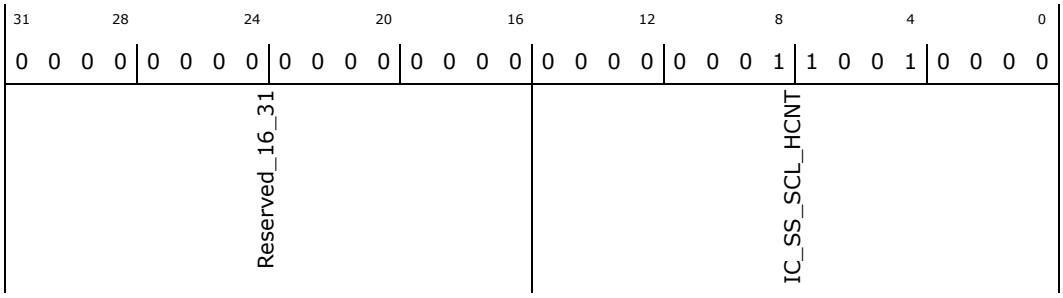
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000190h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x190 RW	**IC_SS_SCL_HCNT:** Standard Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.18.7 Standard Speed I2C Clock SCL Low Count Register. (IC_SS_SCL_LCNT)—Offset 18h

Standard Speed I2C Clock SCL Low Count Register.

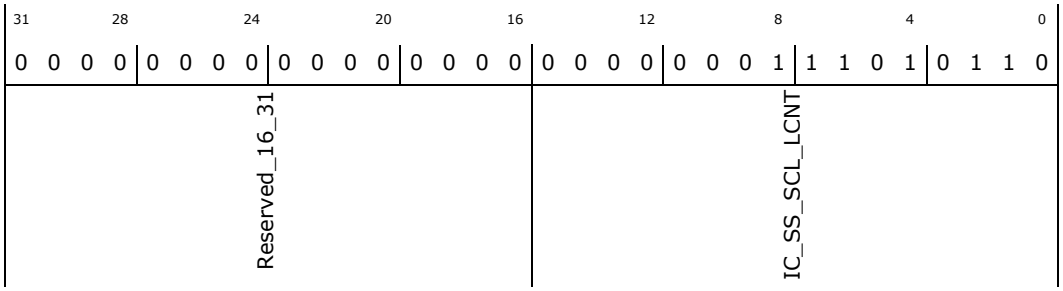
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 000001D6h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x1d6 RW	**IC_SS_SCL_LCNT:** Standard Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.18.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

Fast Speed I2C Clock SCL High Count Register

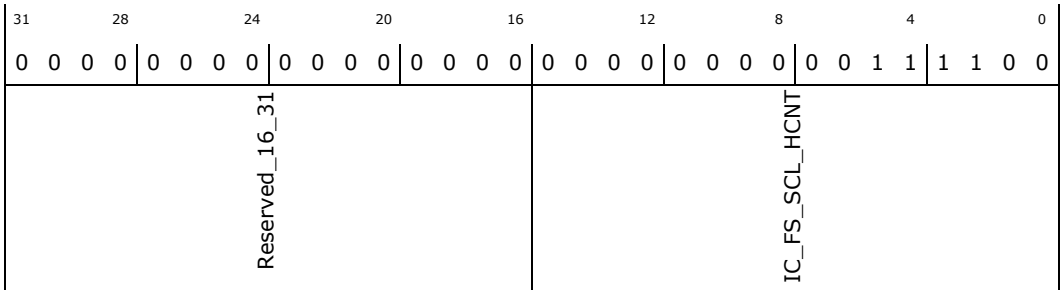
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 0000003Ch



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x3c RW	**IC_FS_SCL_HCNT:** Fast Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.18.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

Fast Speed I2C Clock SCL Low Count Register

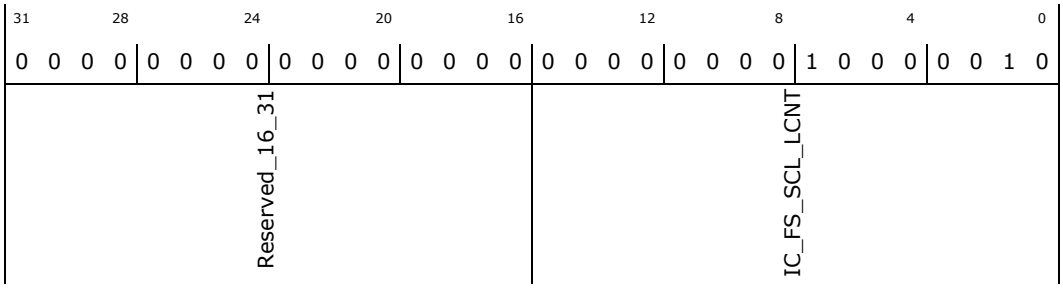
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000082h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x82 RW	**IC_FS_SCL_LCNT:** Fast Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.18.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

High Speed I2C Clock SCL High Count Register

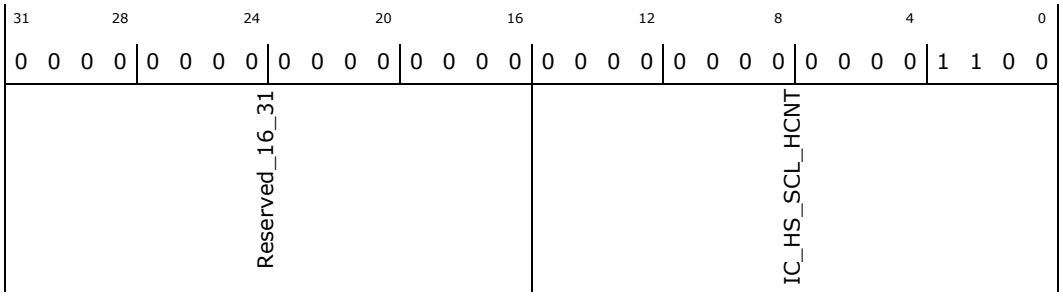
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 0000000Ch



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0xc RW	**IC_HS_SCL_HCNT:** High Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.18.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

High Speed I2C Clock SCL Low Count Register

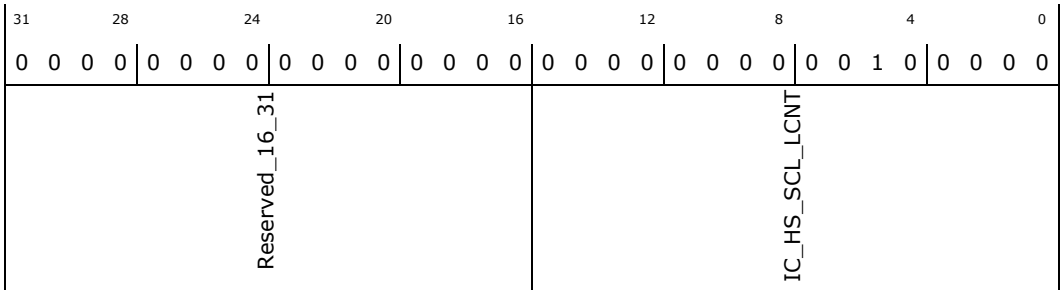
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000020h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x20 RW	**IC_HS_SCL_LCNT:** High Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.18.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

I2C Interrupt Status Register

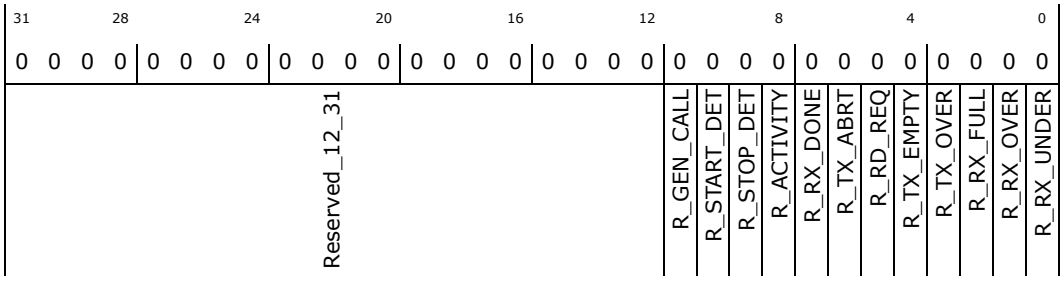
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x0 RO	**R_GEN_CALL:** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0x0 RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0x0 RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0x0 RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0x0 RO	**R_TX_ABRT:** This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0x0 RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.
4	0x0 RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0x0 RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0x0 RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0x0 RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0x0 RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

9.18.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

I2C Interrupt Mask Register

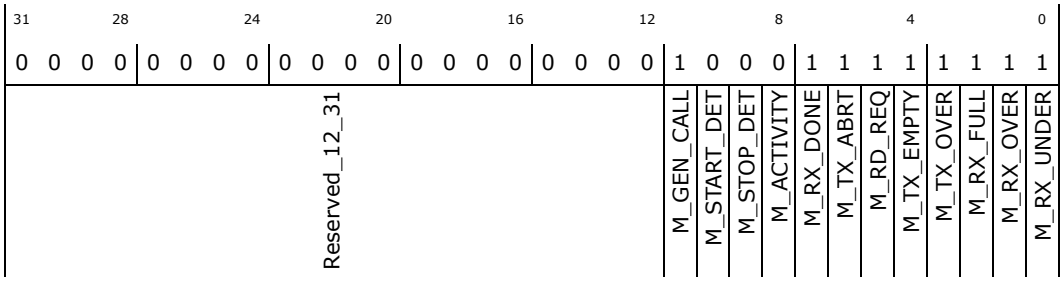
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 000008FFh



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x1 RW	**M_GEN_CALL:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
10	0x0 RW	**M_START_DET:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
9	0x0 RW	**M_STOP_DET:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
8	0x0 RW	**M_ACTIVITY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
7	0x1 RW	**M_RX_DONE:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
6	0x1 RW	**M_TX_ABRT:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
5	0x1 RW	**M_RD_REQ:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
4	0x1 RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
3	0x1 RW	**M_TX_OVER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
2	0x1 RW	**M_RX_FULL:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
1	0x1 RW	**M_RX_OVER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
0	0x1 RW	**M_RX_UNDER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.

9.18.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

I2C Raw Interrupt Status Register

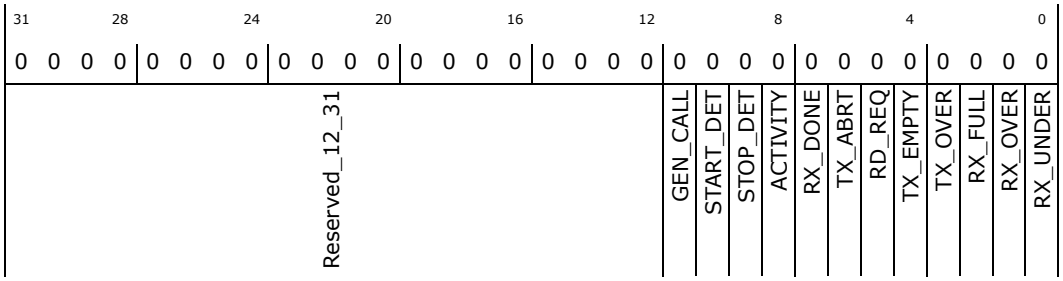
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x0 RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT
10	0x0 RO	**START_DET:** Same as in reg_IC_INTR_STAT
9	0x0 RO	**STOP_DET:** Same as in reg_IC_INTR_STAT
8	0x0 RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT
7	0x0 RO	**RX_DONE:** Same as in reg_IC_INTR_STAT
6	0x0 RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT
5	0x0 RO	**RD_REQ:** Same as in reg_IC_INTR_STAT
4	0x0 RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT
3	0x0 RO	**TX_OVER:** Same as in reg_IC_INTR_STAT
2	0x0 RO	**RX_FULL:** Same as in reg_IC_INTR_STAT
1	0x0 RO	**RX_OVER:** Same as in reg_IC_INTR_STAT
0	0x0 RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT

9.18.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

I2C Receive FIFO Threshold Register

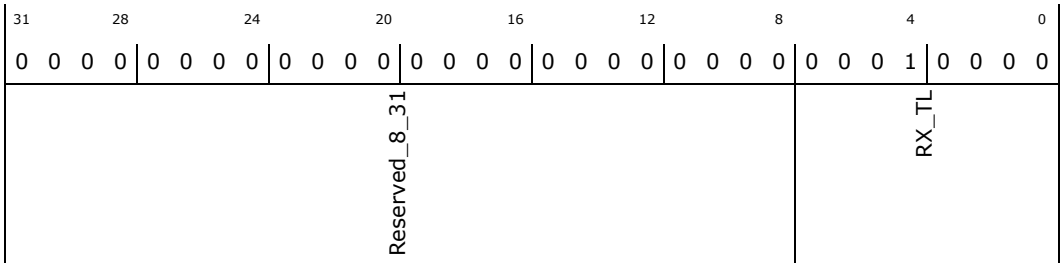
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x10 RW	**RX_TL:** Receive FIFO Threshold Level. The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

9.18.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

I2C Transmit FIFO Threshold Register

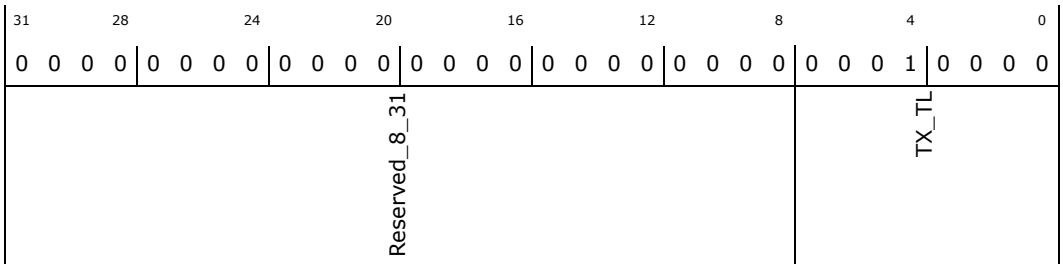
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x10 RW	**TX_TL:** Transmit FIFO Threshold Level. Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

9.18.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

Clear Combined and Individual Interrupt Register

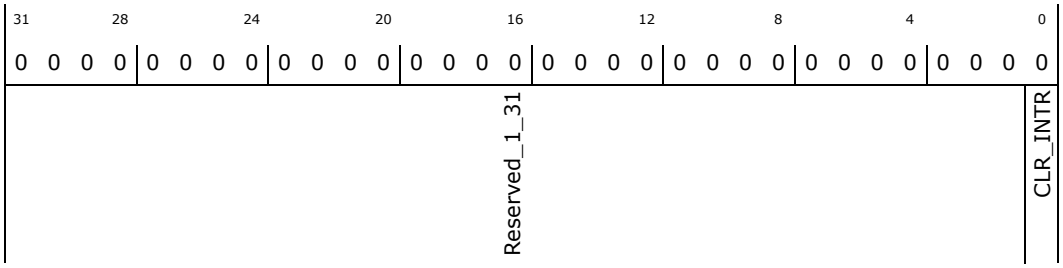
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

9.18.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

Clear RX_UNDER Interrupt Register

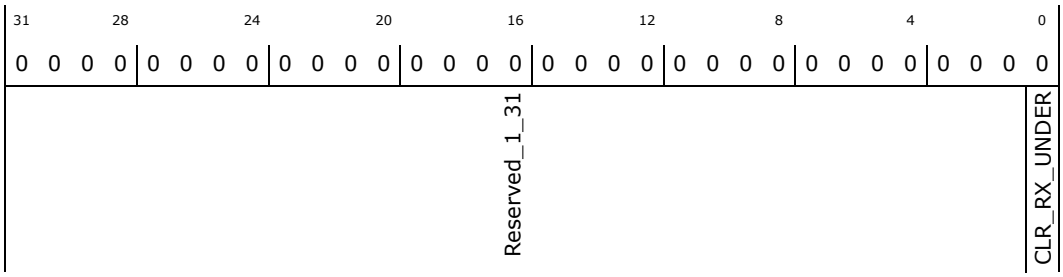
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

9.18.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

Clear RX_OVER Interrupt Register

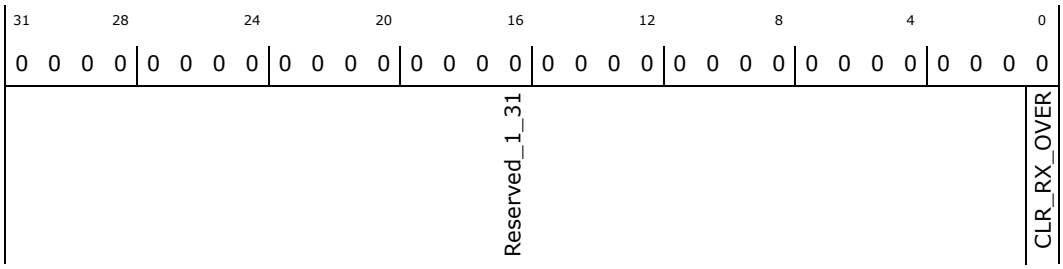
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

9.18.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

Clear TX_OVER Interrupt Register

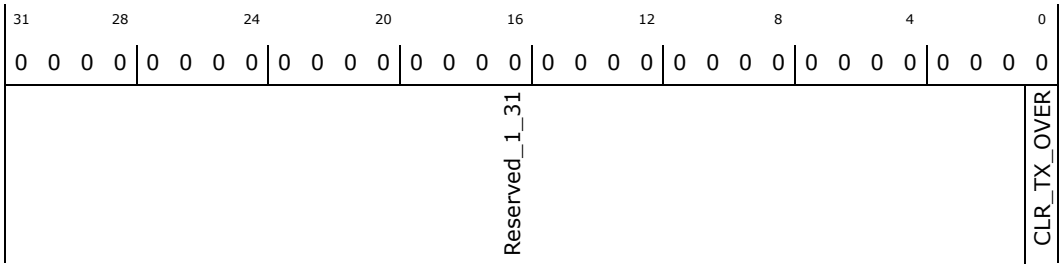
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

9.18.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

Clear RD_REQ Interrupt Register

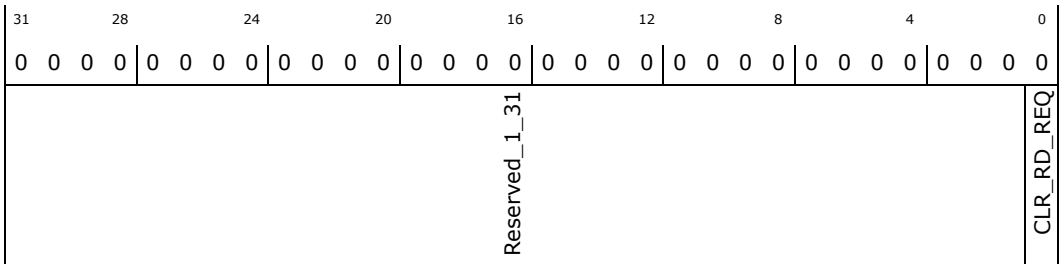
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

9.18.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

Clear TX_ABRT Interrupt Register

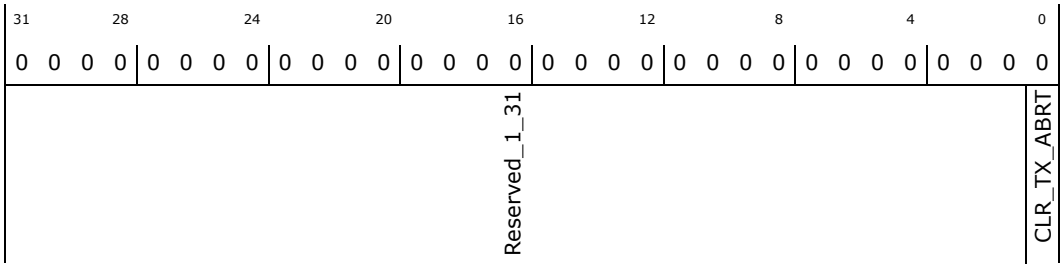
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

9.18.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

Clear RX_DONE Interrupt Register

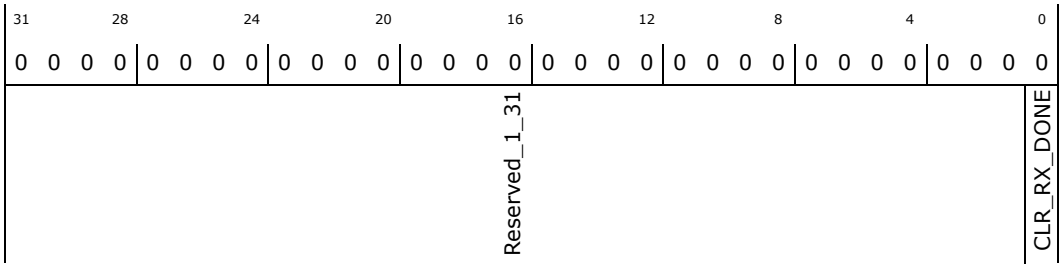
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

9.18.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

Clear ACTIVITY Interrupt Register

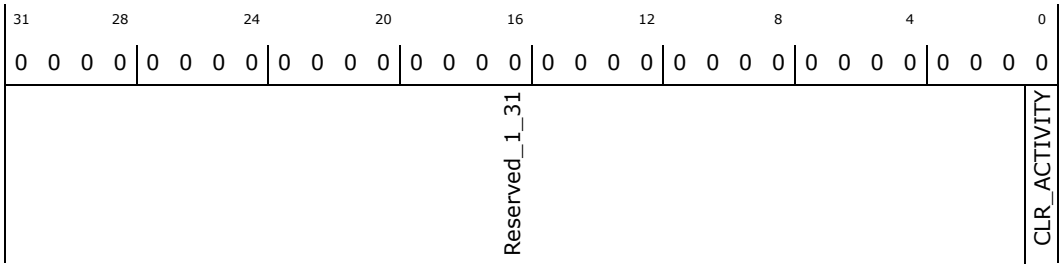
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

9.18.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

Clear STOP_DET Interrupt Register

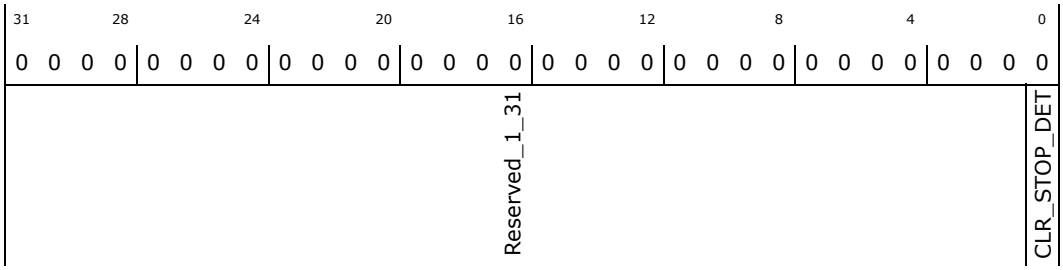
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

9.18.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

Clear START_DET Interrupt Register

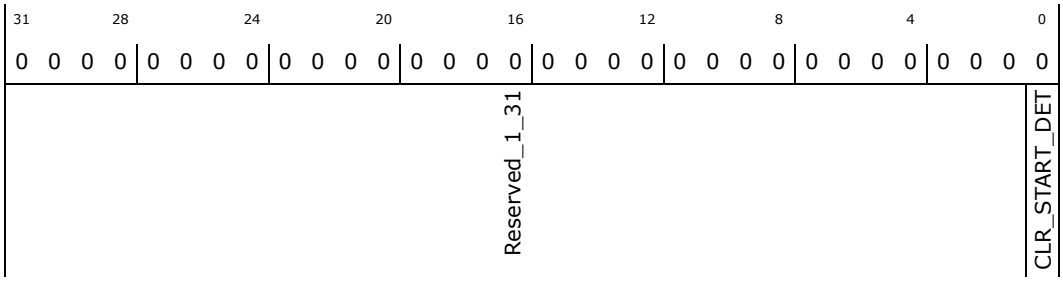
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

9.18.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

Clear GEN_CALL Interrupt Register

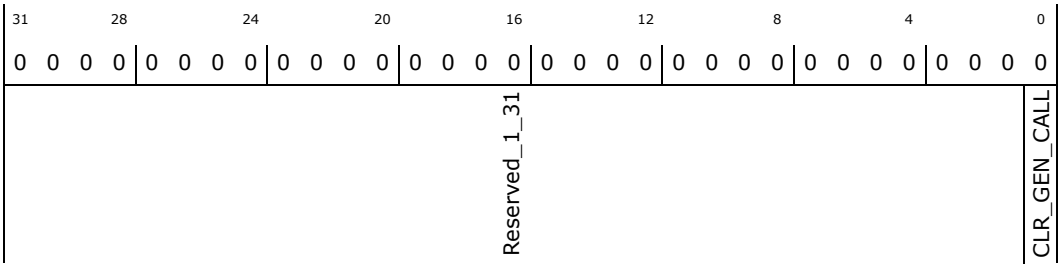
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

9.18.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

I2C Enable Register

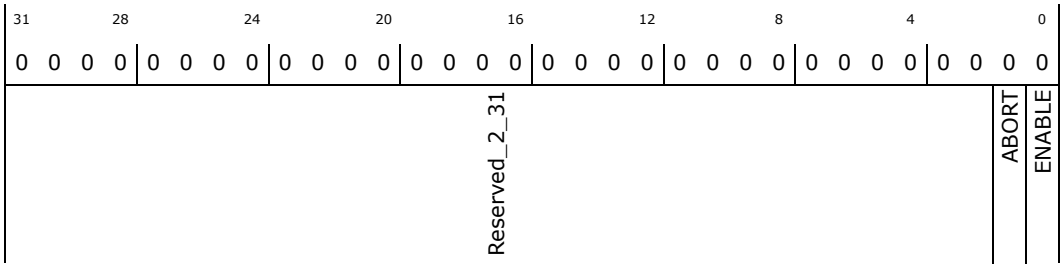
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved_2_31:** Reserved
1	0x0 WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.
0	0x0 RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) 1: Enables DW_apb_i2c

9.18.29 I2C Status Register (IC_STATUS)—Offset 70h

I2C Status Register

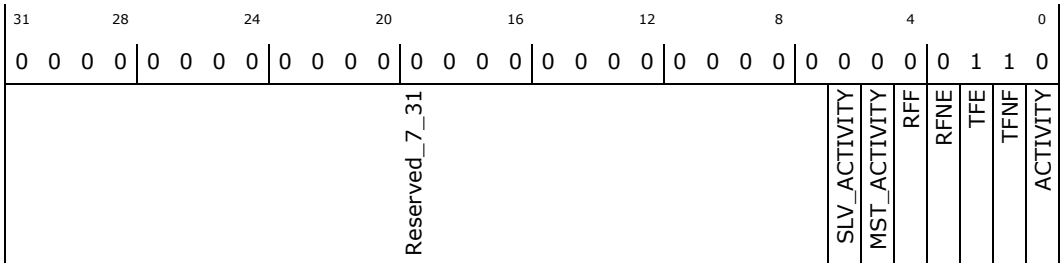
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000006h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RW	**Reserved_7_31:** Reserved
6	0x0 RO	**SLV_ACTIVITY:** Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0x0 RO	**MST_ACTIVITY:** Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RO	**RFF:** Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0x0 RO	**RFNE:** Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.
2	0x1 RO	**TFE:** Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	0x1 RO	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0x0 RO	**ACTIVITY:** I2C Activity Status

9.18.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

I2C Transmit FIFO Level Register

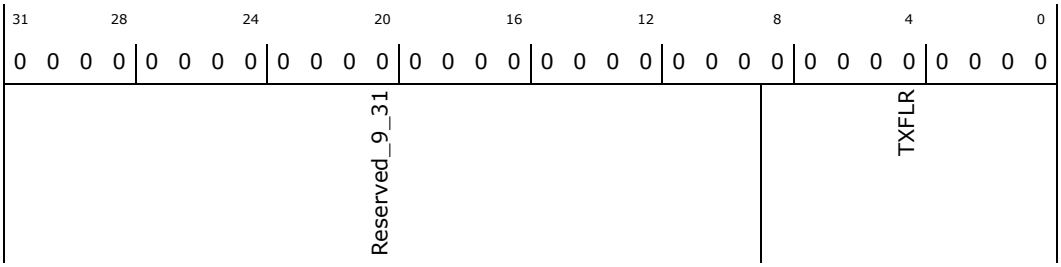
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved_9_31:** Reserved
8:0	0x0 RO	**TXFLR:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

9.18.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

I2C Receive FIFO Level Register

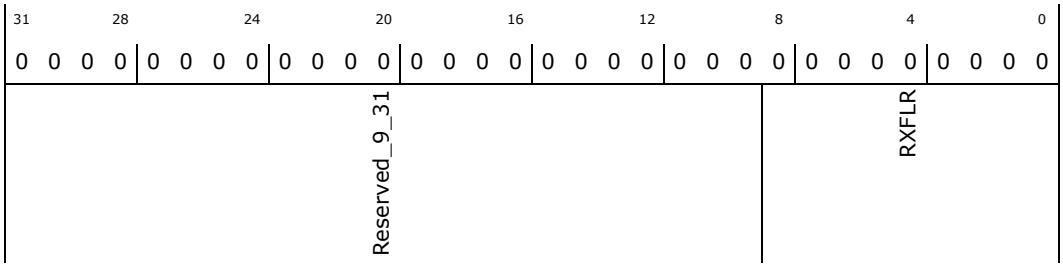
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved_9_31:** Reserved
8:0	0x0 RO	**RXFLR:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

9.18.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

I2C SDA Hold Time Length Register

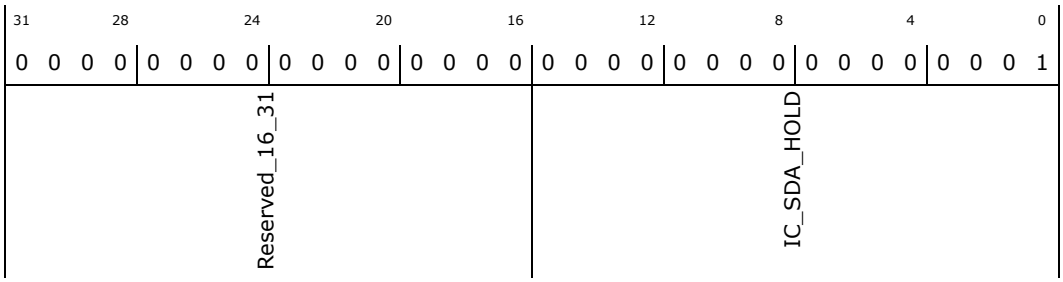
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x1 RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

9.18.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

I2C Transmit Abort Source Register

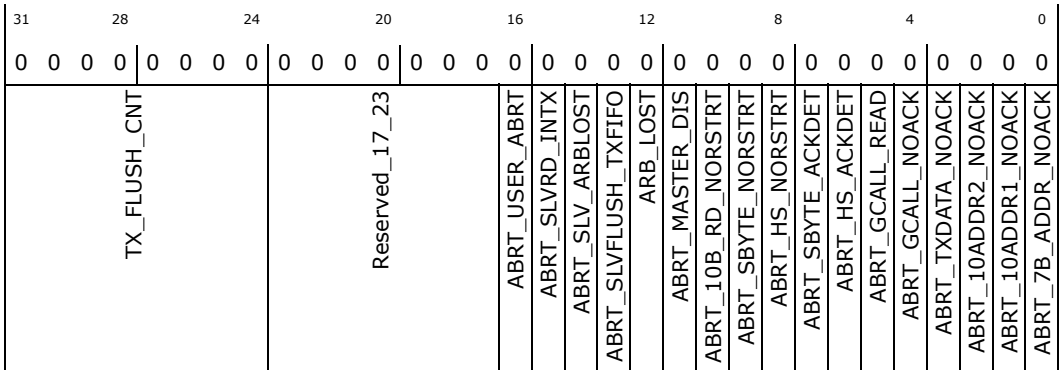
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0x0 RW	**Reserved_17_23:** Reserved
16	0x0 RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0x0 RO	**ABRT_SLVRD_INTX:** 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0x0 RO	**ABRT_SLV_ARBLOST:** 1: Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0x0 RO	**ABRT_SLVFLUSH_TXFIFO:** 1: Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0x0 RO	**ARB_LOST:** 1: Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0x0 RO	**ABRT_MASTER_DIS:** 1: User tries to initiate a Master operation with the Master mode disabled.
10	0x0 RO	**ABRT_10B_RD_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RO	**ABRT_SBYTE_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0x0 RO	**ABRT_HS_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0x0 RO	**ABRT_SBYTE_ACKDET:** 1: Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
6	0x0 RO	**ABRT_HS_ACKDET:** 1: Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
5	0x0 RO	**ABRT_GCALL_READ:** 1: DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0x0 RO	**ABRT_GCALL_NOACK:** 1: DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0x0 RO	**ABRT_TXDATA_NOACK:** 1: This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0x0 RO	**ABRT_10ADDR2_NOACK:** 1: Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0x0 RO	**ABRT_10ADDR1_NOACK:** 1: Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0x0 RO	**ABRT_7B_ADDR_NOACK:** 1: Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

9.18.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

Generate Slave Data NACK Register

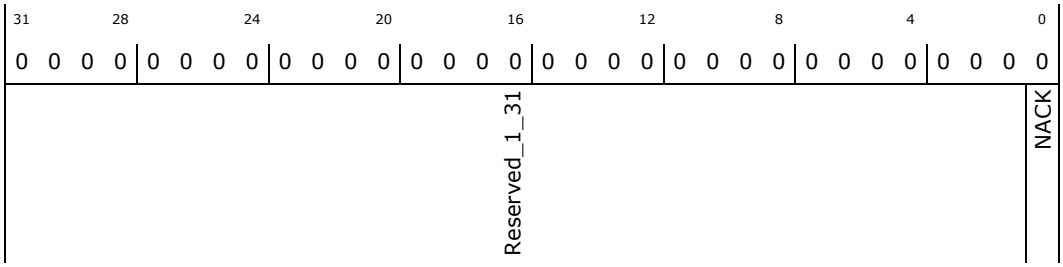
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RW	**NACK:** Generate NACK. This NACK generation only occurs when DW_apb_i2c is a slavereceiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. 1 = generate NACK after data byte received 0 = generate NACK/ACK normally

9.18.35 DMA Control Register (IC_DMA_CR)—Offset 88h

DMA Control Register

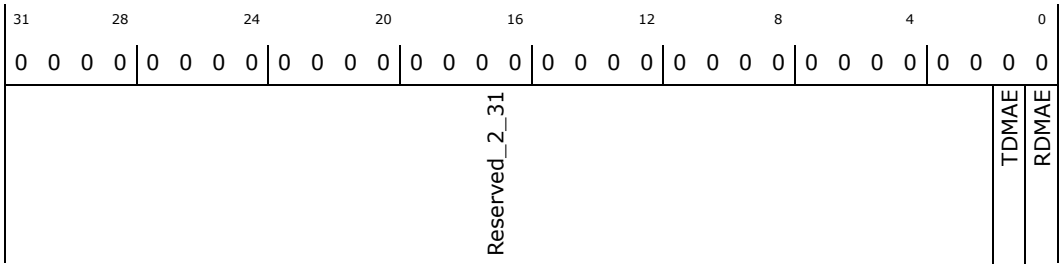
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved_2_31:** Reserved
1	0x0 RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel. 0 = Transmit DMA disabled 1 = Transmit DMA enabled
0	0x0 RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. 0 = Receive DMA disabled 1 = Receive DMA enabled

9.18.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

DMA Transmit Data Level Register

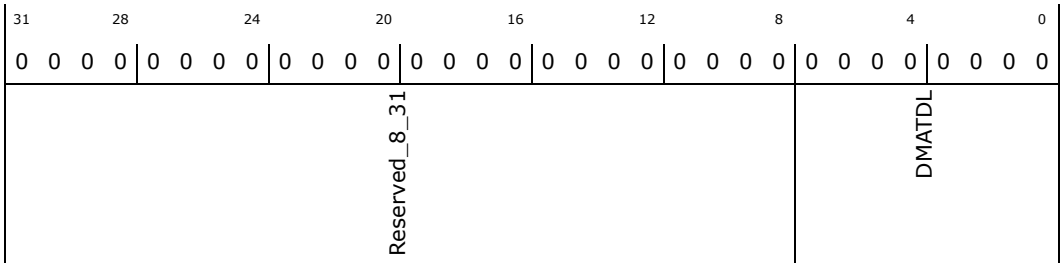
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x0 RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

9.18.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

I2C Receive Data Level Register

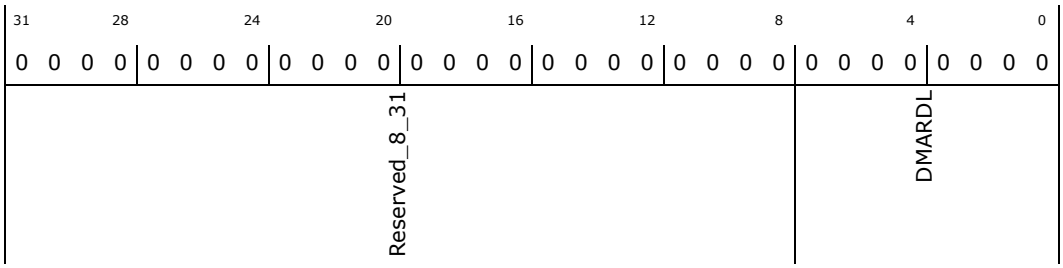
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x0 RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

9.18.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

I2C SDA Setup Register

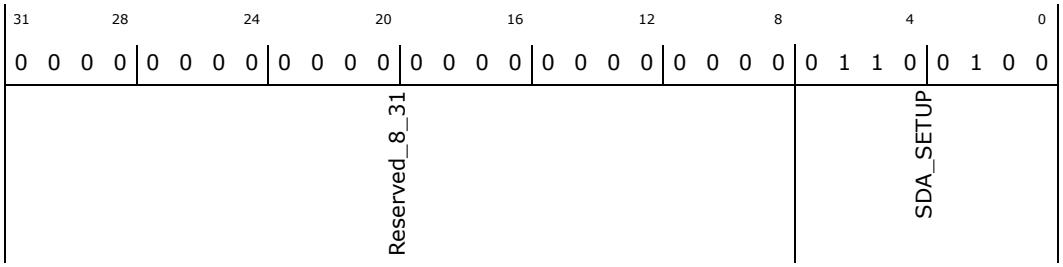
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000064h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x64 RW	**SDA_SETUP:** SDA Setup. It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

9.18.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

I2C ACK General Call Register

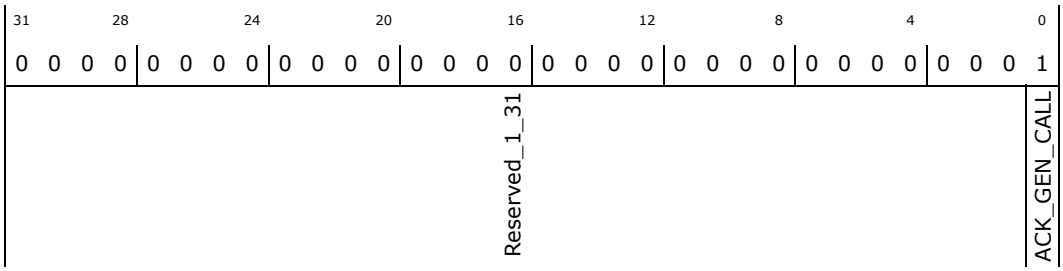
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x1 RW	**ACK_GEN_CALL:** ACK General Call. When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

9.18.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

I2C Enable Status Register

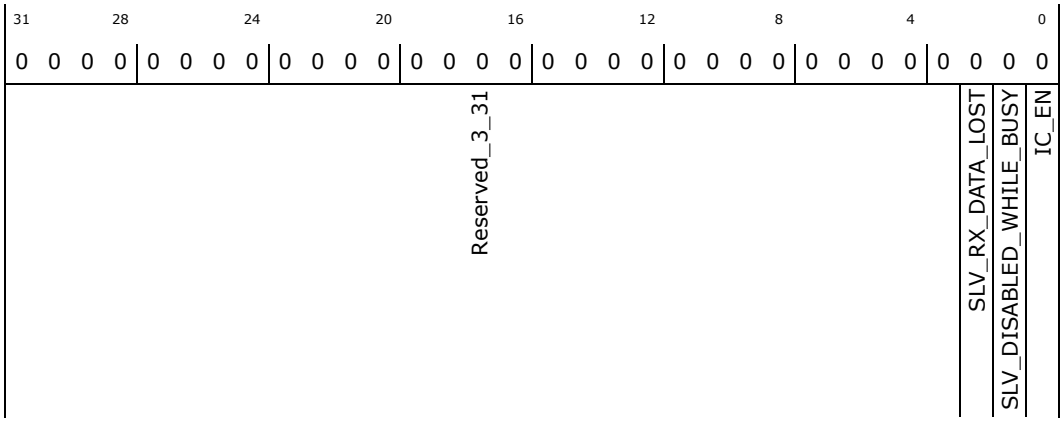
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved_3_31:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0x0 RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0x0 RO	**IC_EN:** ic_en Status. This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

9.18.41 SS/FS Mode Spike Length Register (IC_FS_SPKLEN)—Offset A0h

SS/FS Mode Spike Length Register

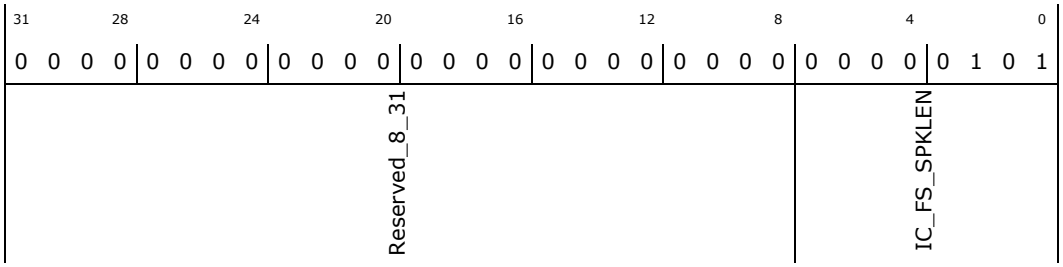
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000005h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x5 RW	**IC_FS_SPKLEN:** Maximum length (in ic_clk cycles) of suppressed spikes in SS and FS modes

9.18.42 HS Mode Spike Length Register (IC_HS_SPKLEN)—Offset A4h

HS Mode Spike Length Register

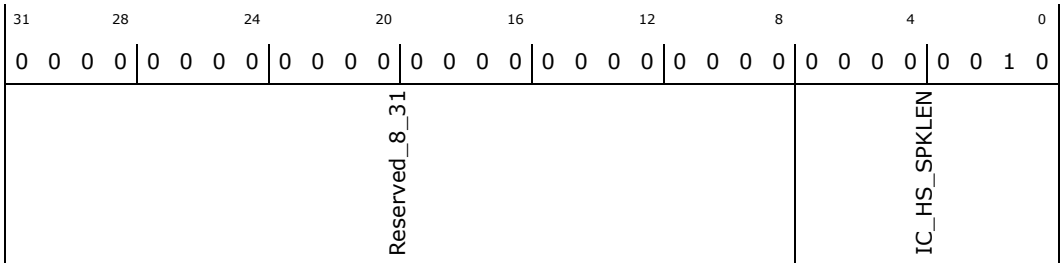
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x2 RW	**IC_HS_SPKLEN:** Maximum length (in ic_clk cycles) of suppressed spikes in HS mode

9.18.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

Component Parameter Register 1

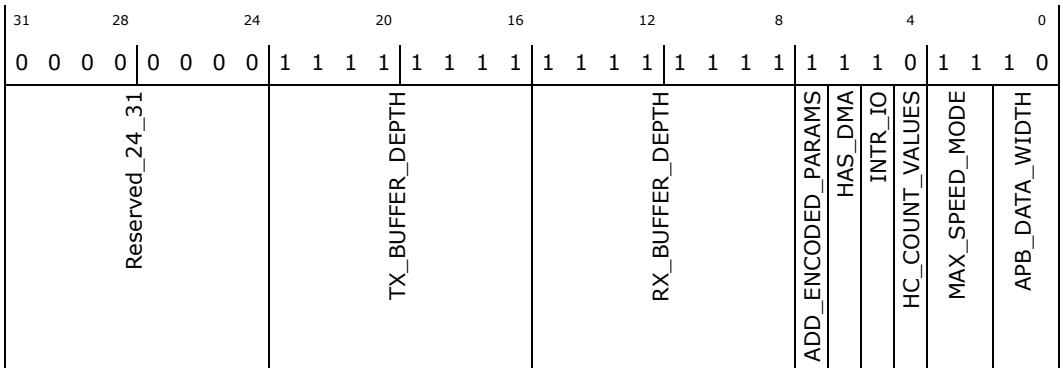
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00FFFFEEh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved_24_31:** Reserved
23:16	0xff RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	0xff RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	0x1 RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	0x1 RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	0x1 RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0x0 RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	0x3 RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	0x2 RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

9.18.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

I2C Component Version Register

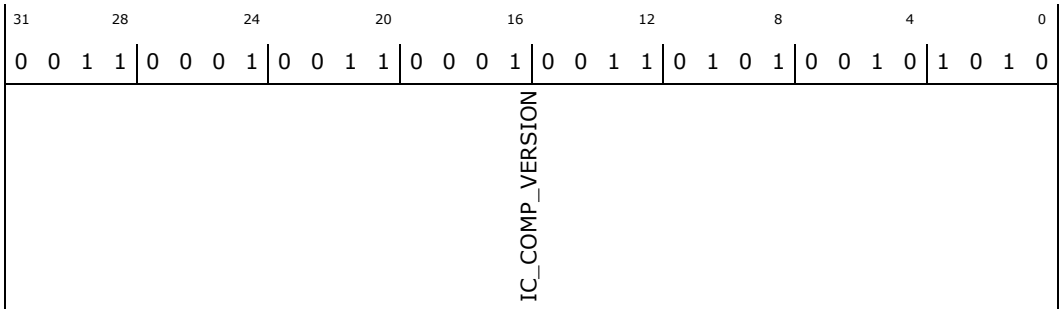
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 3131352Ah



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x3131352a RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes

9.18.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

I2C Component Type Register

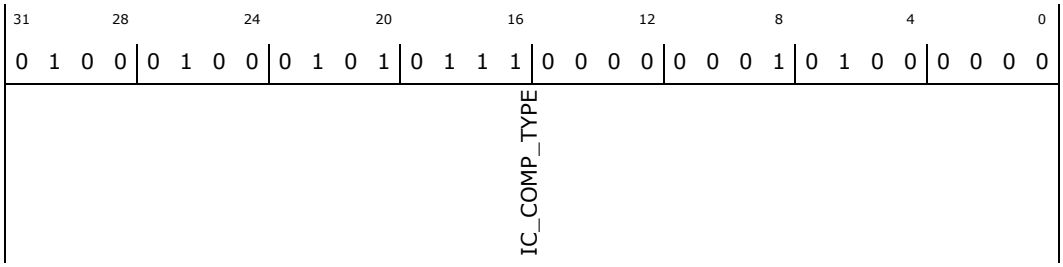
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 44570140h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x44570140 RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

9.18.46 Clock params register (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

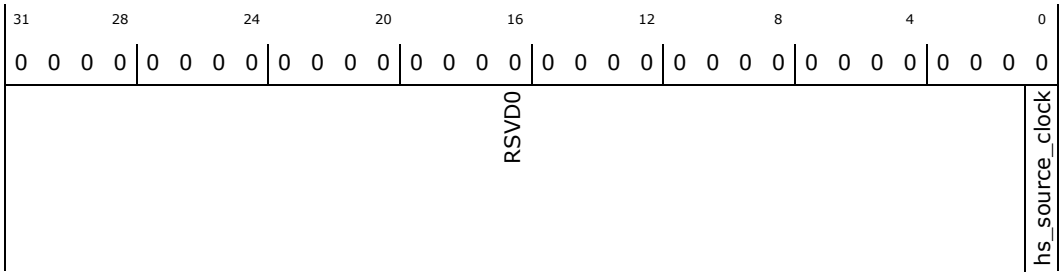
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz 1 -133MHz (high-speed operation compatible)

9.18.47 software reset (RESETS)—Offset 804h

software reset

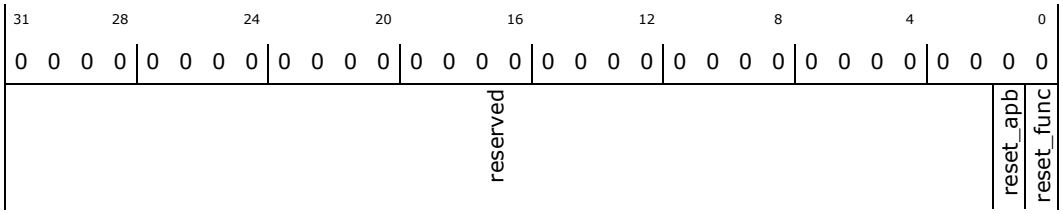
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (reserved):** Reserved
1	0x0 RW	**reset_apb:** reset the apb domain
0	0x0 RW	**reset_func:** reset the func clock domain

9.18.48 General purpose register (GENERAL)—Offset 808h

General purpose register

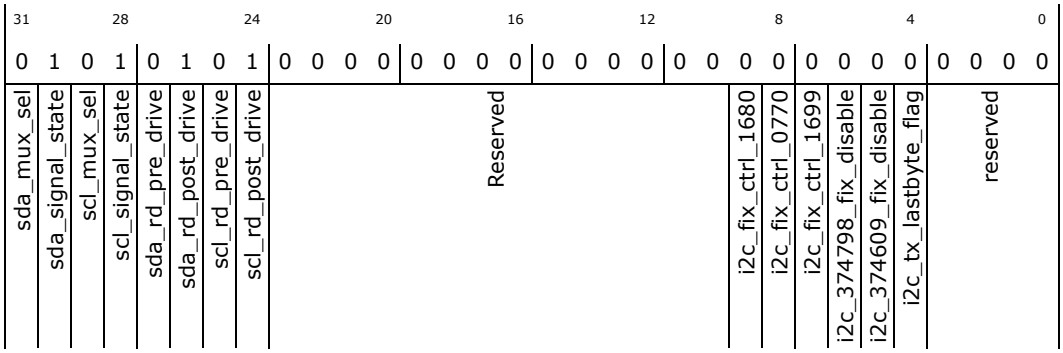
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 55000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**sda_mux_sel:** This bit selects the driver for the SDA signal: 1 = sda_signal_state, 0 = I2C logic
30	0x1 RW	**sda_signal_state:** This bit is used when sda_mux_sel = 1, used to drive the SDA signal on the I2C interface
29	0x0 RW	**scl_mux_sel:** This bit selects the driver for the SCL signal: 1 = scl_signal_state, 0 = I2C logic
28	0x1 RW	**scl_signal_state:** This bit is used when scl_mux_sel = 1, used to drive the SCL signal on the I2C interface
27	0x0 RO	**sda_rd_pre_drive:** Read only bit used to see the status of the SDA signal coming from the I2C logic
26	0x1 RO	**sda_rd_post_drive:** Read only bit used to see the status of the SDA signal coming from the pad
25	0x0 RO	**scl_rd_pre_drive:** Read only bit used to see the status of the SCL signal coming from the I2C logic
24	0x1 RO	**scl_rd_post_drive:** Read only bit used to see the status of the SCL signal coming from the pad
23:10	0x0 RO	**Reserved:** Reserved
9	0x0 RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0x0 RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0x0 RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0x0 RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)
5	0x0 RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0x0 RW	**reserved:** reserved

9.18.49 TX transaction counter (I2C_ACK_COUNT)—Offset 818h

TX transaction counter

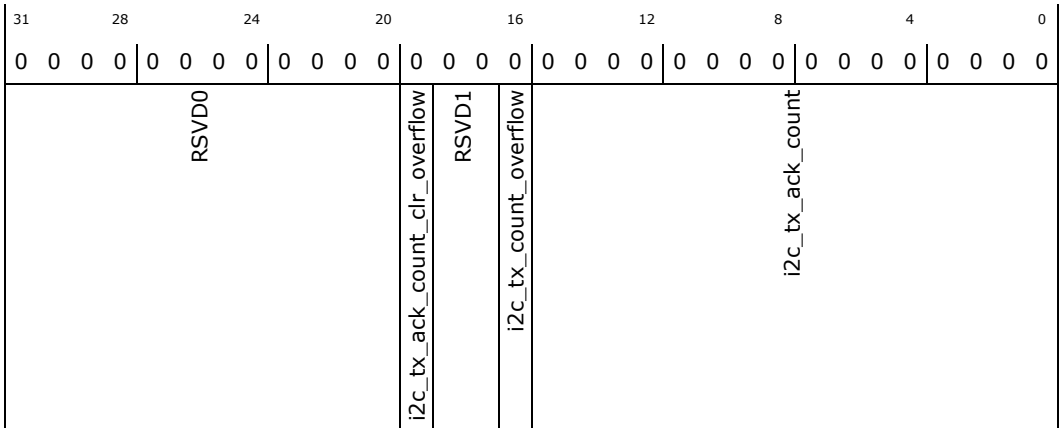
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RSVD0:** Reserved
19	0x0 RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0x0 RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

9.18.50 TX transaction complete interrupt status register (I2C_TX_COMPLETE_INTR_STAT)—Offset 820h

TX transaction has finished interrupt

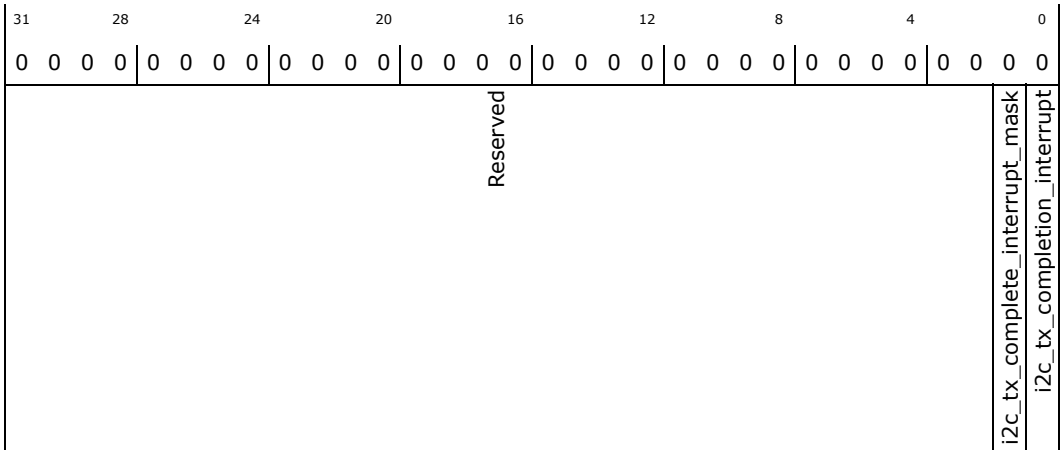
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved:** Reserved
1	0x0 RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0x0 RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

9.18.51 TX transaction complete interrupt clear register (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

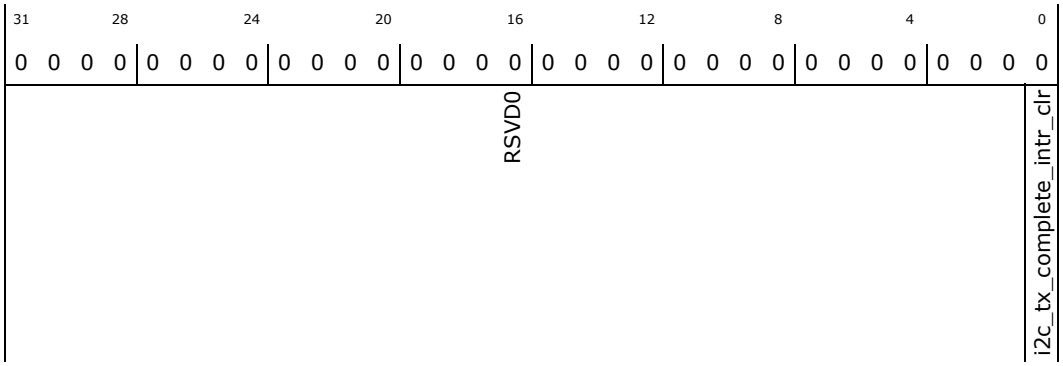
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

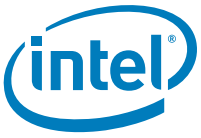
Offset: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt



9.19 SIO I2C 4 PCI Configuration Registers

Table 82. Summary of SIO I2C 4 PCI Configuration Registers—0/24/5

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4501	00008086h
4–7h	4	"STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h" on page 4501	00100000h
8–Bh	4	"REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4503	00000000h
C–Fh	4	"CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4504	00800000h
10–13h	4	"BAR -Base Address Register (BAR)—Offset 10h" on page 4504	00000000h
14–17h	4	"BAR1 -Base Address Register1 (BAR1)—Offset 14h" on page 4505	00000000h
2C–2Fh	4	"SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4506	00000000h
30–33h	4	"EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4507	00000000h
34–37h	4	"CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4507	00000000h
3C–3Fh	4	"INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4508	00000100h
80–83h	4	"POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4508	00030001h
84–87h	4	"PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4509	00000008h
F8–FBh	4	"Manufacturers ID (MANID)—Offset F8h" on page 4510	00000000h

9.19.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

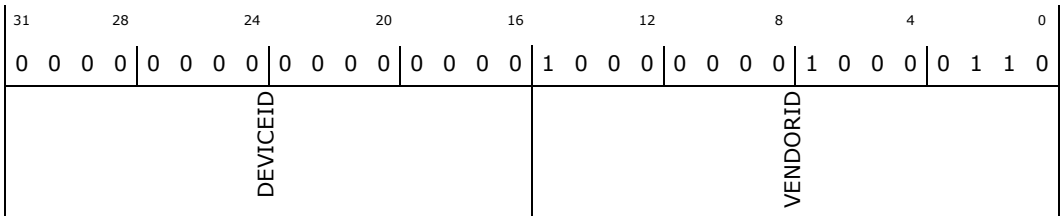
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**DEVICEID:** Device ID identifies the particular AHB/APB device. This is tied to a strap at the top level. Because of tool issues, the HTML files show this field as 0, but the following are the POR values for SoC: LPIO1 DMA: 0x2286 LPIO1 PWM1: 0x2288 LPIO1 PWM2: 0x2289 LPIO1 HSUART1: 0x228A LPIO1 HSUART2: 0x228C LPIO1 SPI1: 0x228E LPIO1 SPI2: 0x2290 LPIO1 SPI3: 0x22AC LPIO2 DMA: 0x22C0 LPIO2 I2C1: 0x22C1 LPIO2 I2C2: 0x22C2 LPIO2 I2C3: 0x22C3 LPIO2 I2C4: 0x22C4 LPIO2 I2C5: 0x22C5 LPIO2 I2C6: 0x22C6 LPIO2 I2C7: 0x22C7 For the final word on this, please see Ray Ng's SoC RevID and DevID HAS on Infofactory: https://ifcollaborate.intel.com/IFC/getdoc.aspx?docbase=InfoFactoryKBandchronid=09005ffd80e84b43andver=CURRENTandqepop=false
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap the top level.

9.19.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

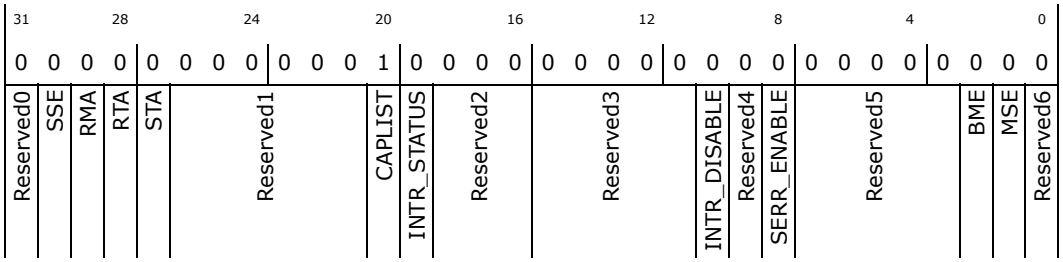
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved0:** Reserved
30	0x0 RW/1C	**SSE:** This bit is set when a device sends an DO_SERR message, and the SERR# Enable bit in the Command register is 1
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric PortReceived Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27	0x0 RW/1C	**STA:** The Bridge sets this bit whenever it responds to a transaction with CA abort. If the SERR# Enable bit is set, the Bridge sets the Signaled System Error bit and sends an DO_SERR message on the IOSF Sideband.
26:21	0x0 RO	**Reserved1:** Reserved
20	0x1 RO	**CAPLIST:** Capabilities List: Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt .i.e Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.. Reset value of this bit is 0.
9	0x0 RO	**Reserved4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: If both SERR# Enable and the Unsupported Request Reporting Enable (URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0x0 RO	**Reserved6:** Reserved

9.19.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

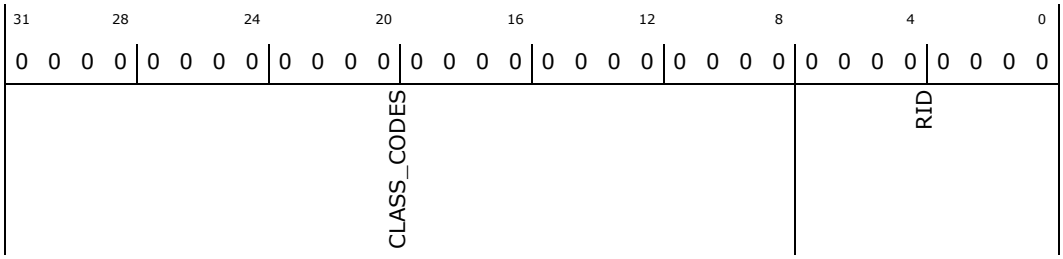
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

9.19.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

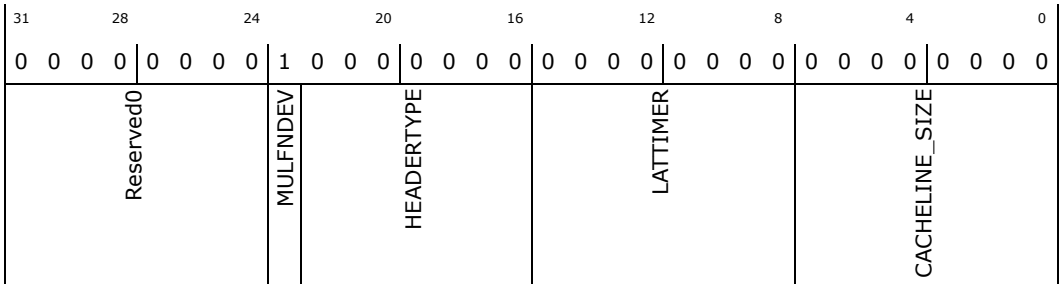
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + Ch

Default: 00800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x1 RO	**MULFNDEV:** Multi Function Device: This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. Value of 1 indicates multifunction device value of 0 indicates single function device
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	0x0 RO	**LATTIMER:** Latency Timer: Doesn.t apply to PCI Express. Hardwired to 00h.
7:0	0x0 RW	**CACHELINE_SIZE:** Cache Line Size: Doesn.t apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

9.19.5 BAR -Base Address Register (BAR)—Offset 10h

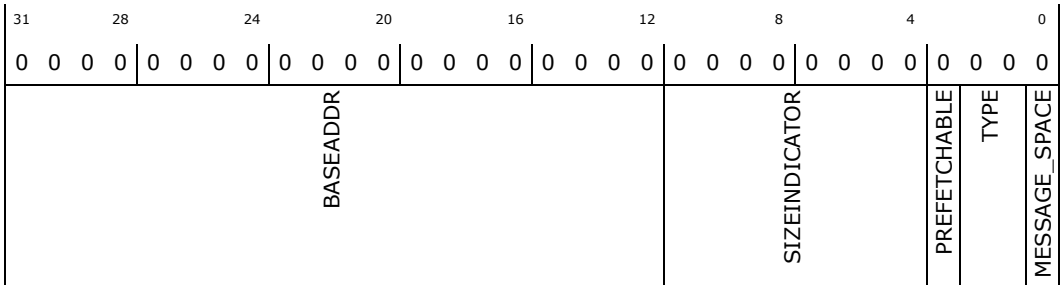
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the AHB device memory space. Taken from Strap values as 1's. Please note that for DMA this field goes from [31:14], or 16kbyte, and the SIZEINDICATOR field goes from [13:4].
11:4	0x0 RO	**SIZEINDICATOR:** Size Indicator Read Only: Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0x0 RO	**TYPE:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.19.6 BAR1 -Base Address Register1 (BAR1)—Offset 14h

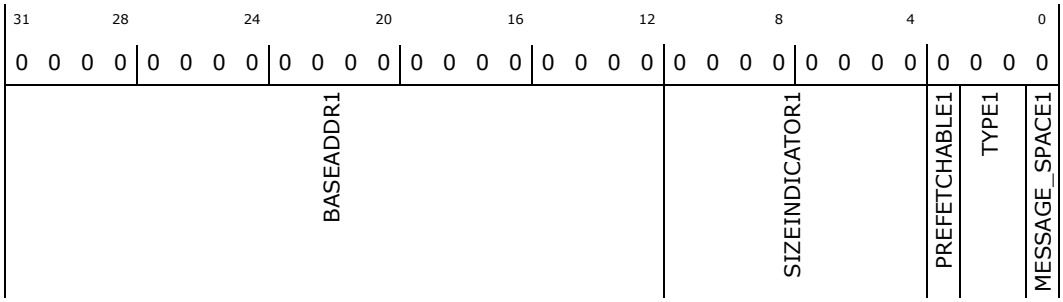
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	0x0 RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not
2:1	0x0 RO	**TYPE1:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.19.7 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

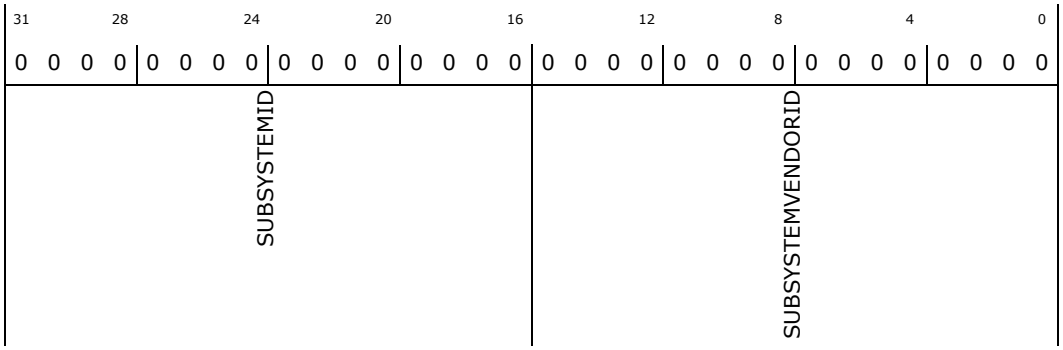
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

9.19.8 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

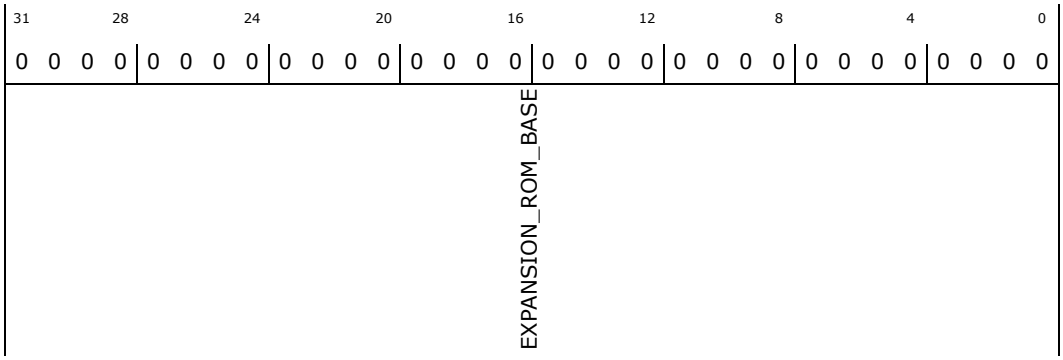
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** A value of all zeros indicates no support for expansion ROM.

9.19.9 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

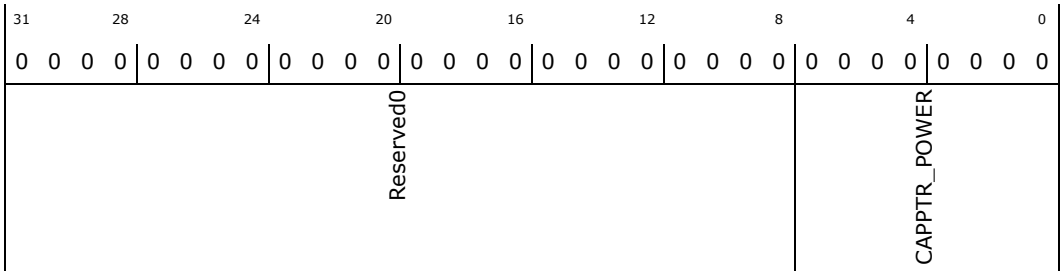
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x0 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

9.19.10 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

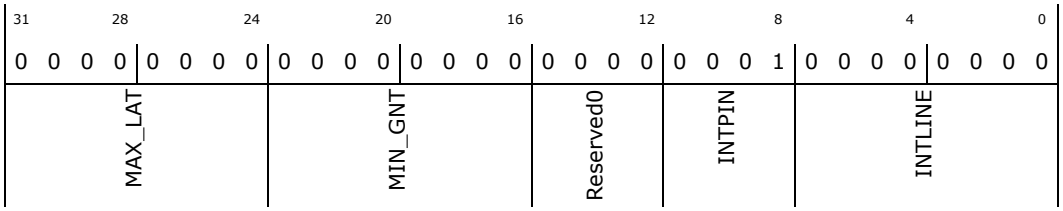
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

9.19.11 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

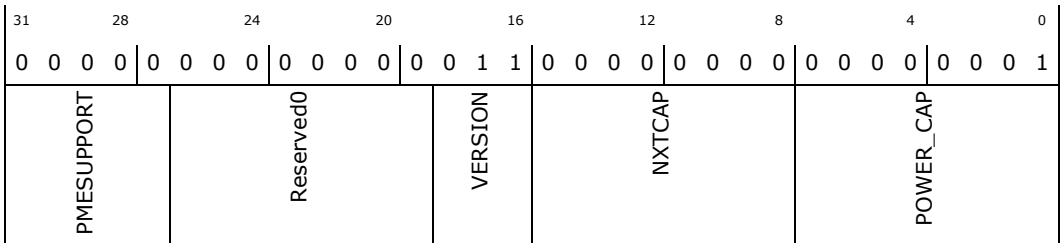
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** PME_Support - This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

9.19.12 PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

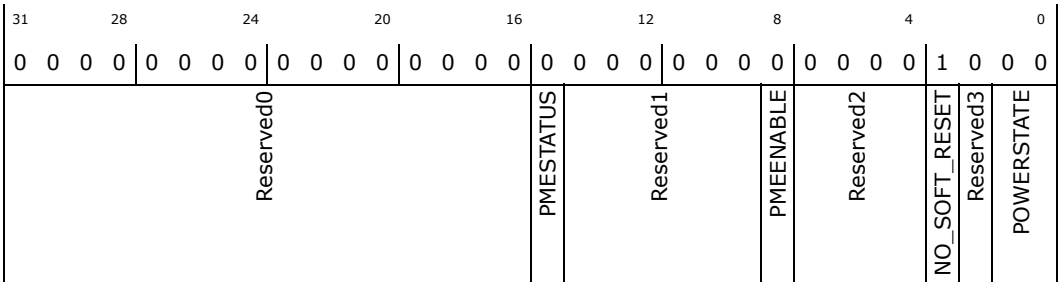
PMECTRLSTATUS - PME Control and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

9.19.13 Manufacturers ID (MANID)—Offset F8h

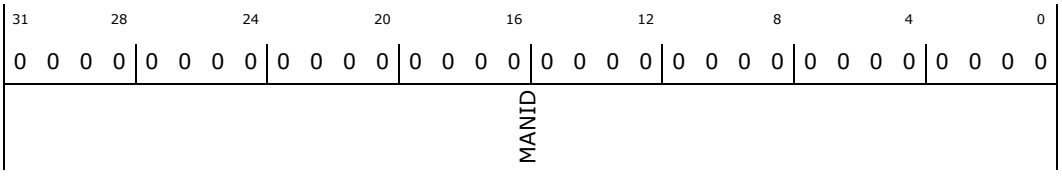
Manufacturers ID

Access Method

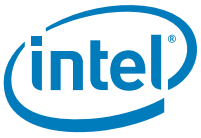
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:5] + F8h

Default: 00000000h



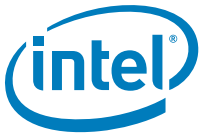
Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: This register is brought out as straps to the top level.



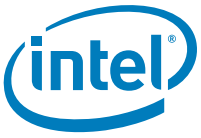
9.20 SIO I2C 4 Memory Mapped Registers

Table 83. Summary of SIO I2C 4 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 4515	0000007Fh
4–7h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 4516	00001055h
8–Bh	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 4517	00000055h
C–Fh	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 4517	00000001h
10–13h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 4518	00000000h
14–17h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 4519	00000190h
18–1Bh	4	"Standard Speed I2C Clock SCL Low Count Register. (IC_SS_SCL_LCNT)—Offset 18h" on page 4520	000001D6h
1C–1Fh	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 4520	0000003Ch
20–23h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 4521	00000082h
24–27h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 4522	0000000Ch
28–2Bh	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 4522	00000020h
2C–2Fh	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 4523	00000000h
30–33h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 4524	000008FFh
34–37h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 4525	00000000h
38–3Bh	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 4526	00000010h
3C–3Fh	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 4527	00000010h
40–43h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 4528	00000000h
44–47h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 4528	00000000h
48–4Bh	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 4529	00000000h
4C–4Fh	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 4530	00000000h
50–53h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 4530	00000000h
54–57h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 4531	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
58–5Bh	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 4531	00000000h
5C–5Fh	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 4532	00000000h
60–63h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 4533	00000000h
64–67h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 4533	00000000h
68–6Bh	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 4534	00000000h
6C–6Fh	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 4534	00000000h
70–73h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 4535	00000006h
74–77h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 4536	00000000h
78–7Bh	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 4536	00000000h
7C–7Fh	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 4537	00000001h
80–83h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 4538	00000000h
84–87h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 4539	00000000h
88–8Bh	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 4540	00000000h
8C–8Fh	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 4540	00000000h
90–93h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 4541	00000000h
94–97h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 4542	00000064h
98–9Bh	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 4542	00000001h
9C–9Fh	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 4543	00000000h
A0–A3h	4	"SS/FS Mode Spike Length Register (IC_FS_SPKLEN)—Offset A0h" on page 4544	00000005h
A4–A7h	4	"HS Mode Spike Length Register (IC_HS_SPKLEN)—Offset A4h" on page 4544	00000002h
F4–F7h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 4545	00FFFFEEh
F8–FBh	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 4546	3131352Ah
FC–FFh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 4547	44570140h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
800–803h	4	"Clock params register (CLOCK_PARAMS)—Offset 800h" on page 4547	00000000h
804–807h	4	"software reset (RESETS)—Offset 804h" on page 4548	00000000h
808–80Bh	4	"General purpose register (GENERAL)—Offset 808h" on page 4548	55000000h
818–81Bh	4	"TX transaction counter (I2C_ACK_COUNT)—Offset 818h" on page 4550	00000000h
820–823h	4	"TX transaction complete interrupt status register (I2C_TX_COMPLETE_INTR_STAT)—Offset 820h" on page 4551	00000000h
824–827h	4	"TX transaction complete interrupt clear register (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 4551	00000000h

9.20.1 I2C Control Register (IC_CON)—Offset 0h

I2C Control Register

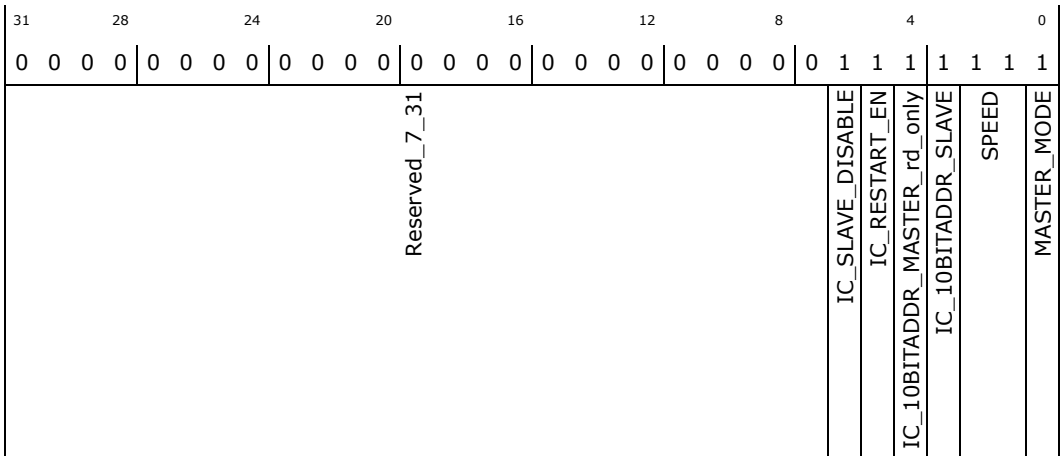
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 0000007Fh



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RW	**Reserved_7_31:** Reserved
6	0x1 RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	0x1 RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master.When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: Sending a START BYTE. Performing any high-speed mode operation. Performing direction changes in combined format mode. Performing a read operation with a 10-bit address
4	0x1 RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register
3	0x1 RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0x3 RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	0x1 RW	**MASTER_MODE:** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

9.20.2 I2C Target Address Register (IC_TAR)—Offset 4h

I2C Target Address Register

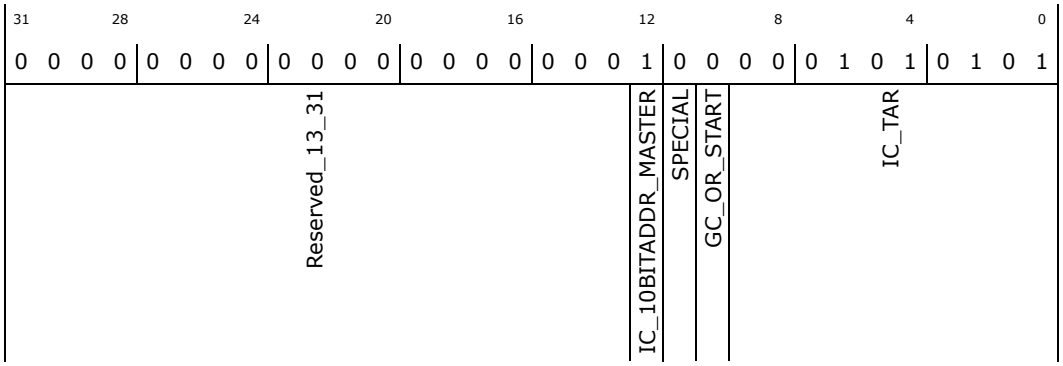
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00001055h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Reserved_13_31:** Reserved
12	0x1 RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master. This bit exists in this register only if the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 1
11	0x0 RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. 0: ignore bit 10 GC_OR_START and use IC_TAR normally. 1: perform special I2C command as specified in GC_OR_START bit
10	0x0 RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.

Bit Range	Default & Access	Field Name (ID): Description
9:0	0x55 RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

9.20.3 I2C Slave Address Register (IC_SAR)—Offset 8h

I2C Slave Address Register

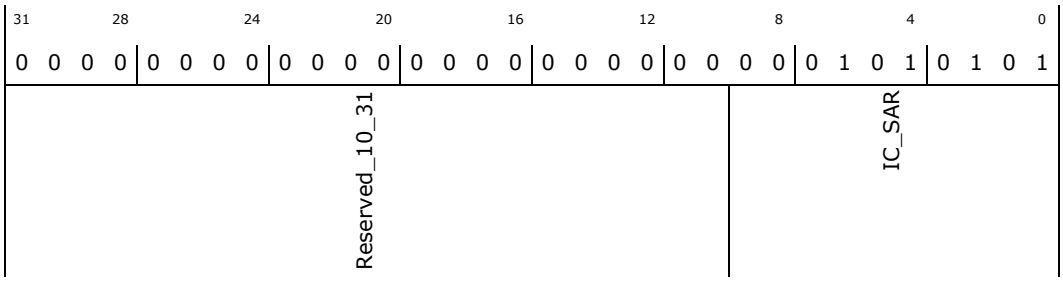
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000055h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**Reserved_10_31:** Reserved
9:0	0x55 RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.20.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

I2C High Speed Master Mode Code Address Register

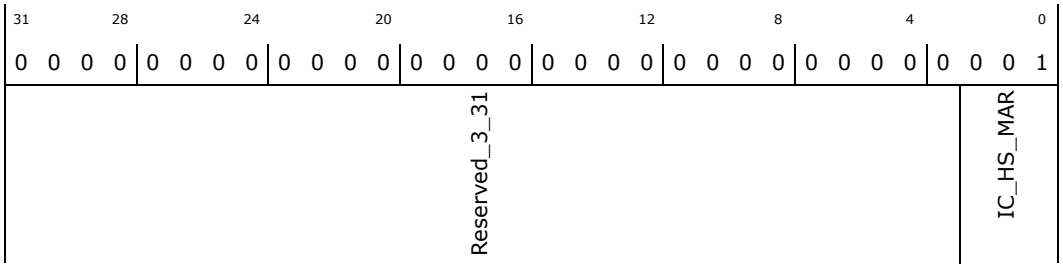
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved_3_31:** Reserved
2:0	0x1 RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.20.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

I2C Rx/Tx Data Buffer and Command Register; this is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO

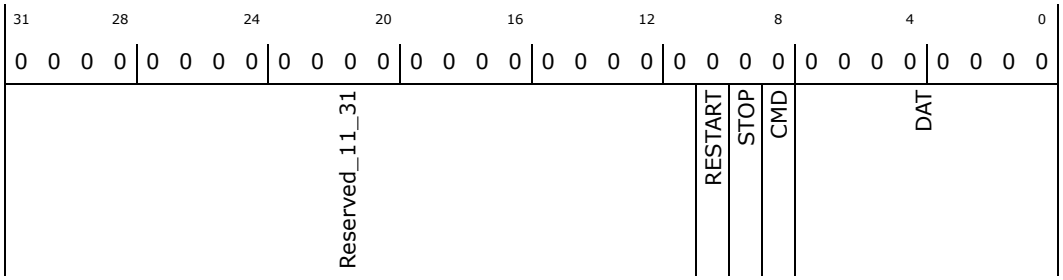
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:11	0x0 RW	**Reserved_11_31:** Reserved
10	0x0 RW	**RESTART:** RESTART
9	0x0 RW	**STOP:** STOP
8	0x0 RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It controls only the direction when it acts as a master. 1 = Read. 0 = Write
7:0	0x0 RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. However, when you read this register, these bits return the value of data received on the DW_apb_i2c interface.

9.20.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

Standard Speed I2C Clock SCL High Count Register.

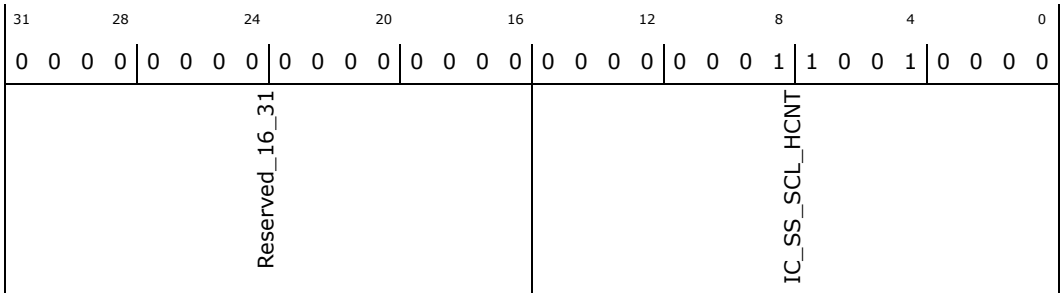
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000190h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x190 RW	**IC_SS_SCL_HCNT:** Standard Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.20.7 Standard Speed I2C Clock SCL Low Count Register. (IC_SS_SCL_LCNT)—Offset 18h

Standard Speed I2C Clock SCL Low Count Register.

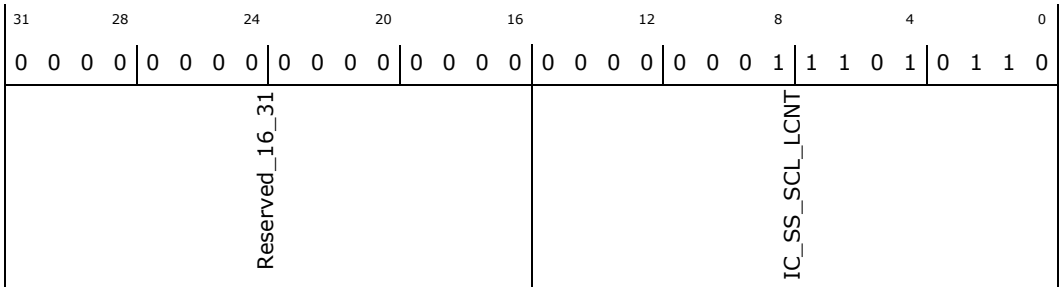
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 000001D6h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x1d6 RW	**IC_SS_SCL_LCNT:** Standard Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.20.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

Fast Speed I2C Clock SCL High Count Register

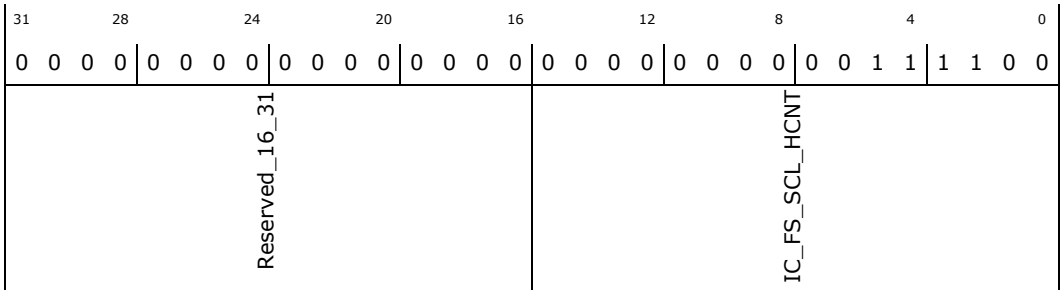
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 0000003Ch



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x3c RW	**IC_FS_SCL_HCNT:** Fast Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.20.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

Fast Speed I2C Clock SCL Low Count Register

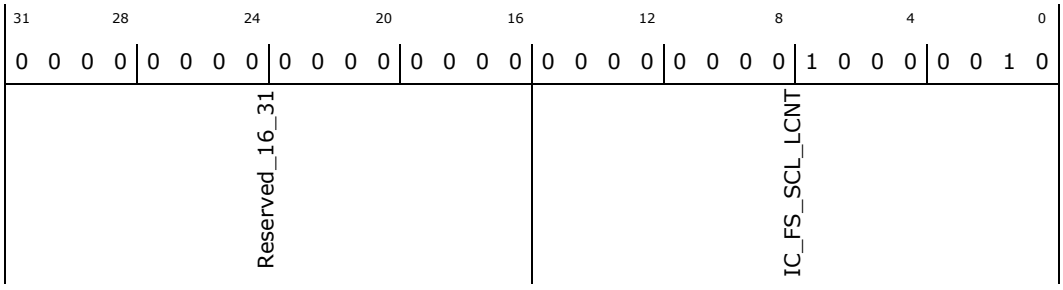
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000082h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x82 RW	**IC_FS_SCL_LCNT:** Fast Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.20.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

High Speed I2C Clock SCL High Count Register

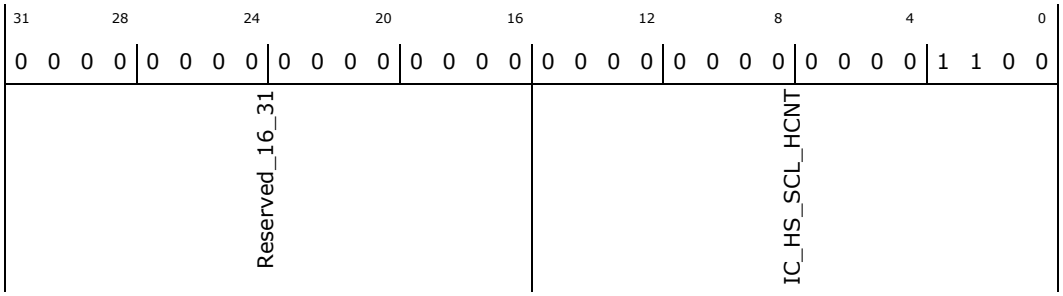
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 0000000Ch



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0xc RW	**IC_HS_SCL_HCNT:** High Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.20.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

High Speed I2C Clock SCL Low Count Register

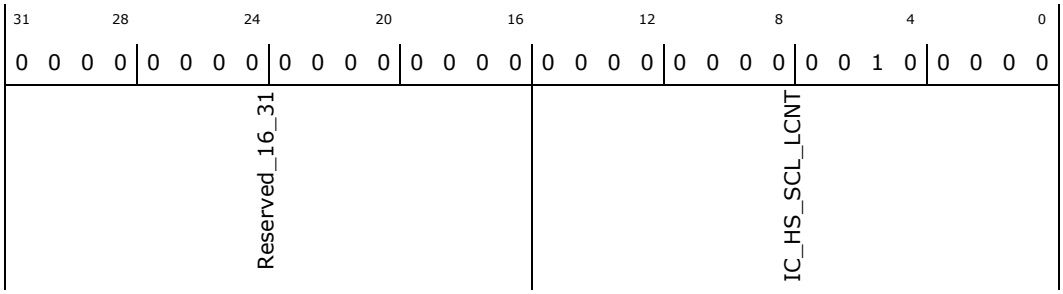
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000020h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x20 RW	**IC_HS_SCL_LCNT:** High Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.20.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

I2C Interrupt Status Register

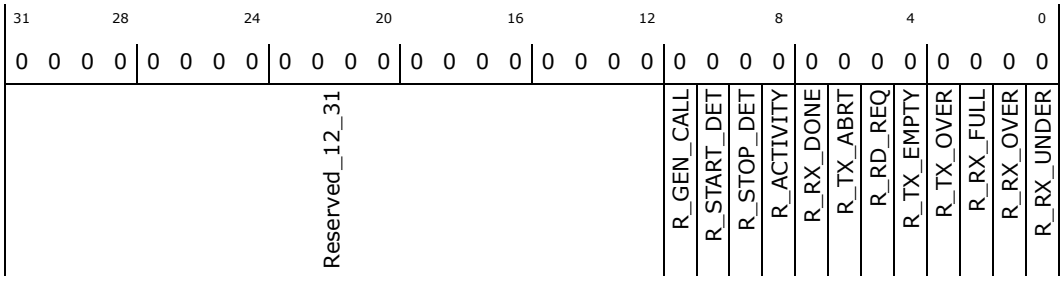
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x0 RO	**R_GEN_CALL:** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0x0 RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0x0 RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0x0 RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0x0 RO	**R_TX_ABRT:** This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0x0 RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.
4	0x0 RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0x0 RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0x0 RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0x0 RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0x0 RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

9.20.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

I2C Interrupt Mask Register

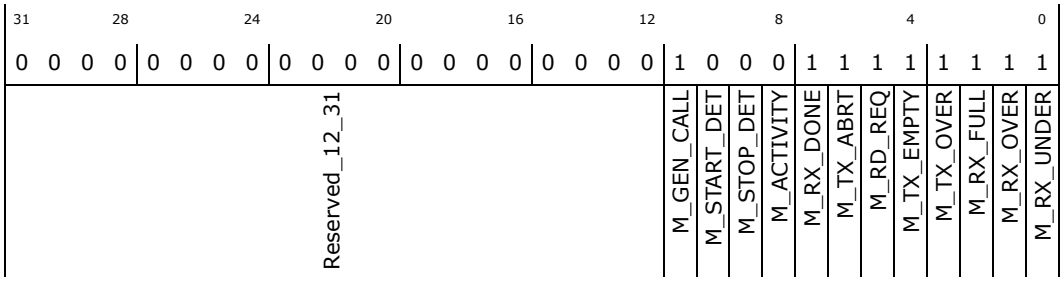
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 000008FFh



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x1 RW	**M_GEN_CALL:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
10	0x0 RW	**M_START_DET:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
9	0x0 RW	**M_STOP_DET:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
8	0x0 RW	**M_ACTIVITY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
7	0x1 RW	**M_RX_DONE:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
6	0x1 RW	**M_TX_ABRT:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
5	0x1 RW	**M_RD_REQ:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
4	0x1 RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
3	0x1 RW	**M_TX_OVER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
2	0x1 RW	**M_RX_FULL:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
1	0x1 RW	**M_RX_OVER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
0	0x1 RW	**M_RX_UNDER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.

9.20.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

I2C Raw Interrupt Status Register

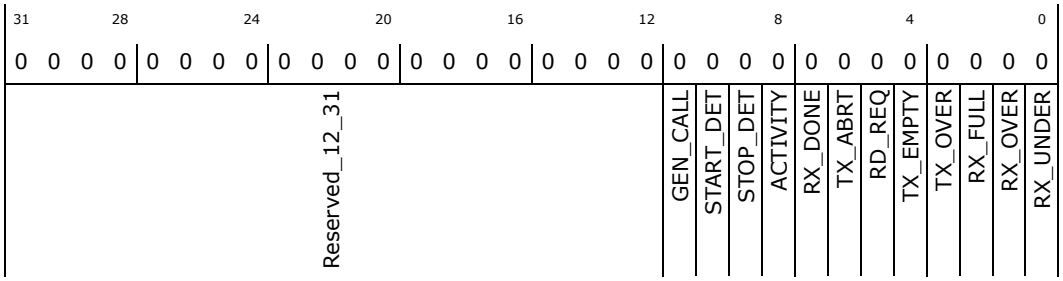
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x0 RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT
10	0x0 RO	**START_DET:** Same as in reg_IC_INTR_STAT
9	0x0 RO	**STOP_DET:** Same as in reg_IC_INTR_STAT
8	0x0 RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT
7	0x0 RO	**RX_DONE:** Same as in reg_IC_INTR_STAT
6	0x0 RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT
5	0x0 RO	**RD_REQ:** Same as in reg_IC_INTR_STAT
4	0x0 RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT
3	0x0 RO	**TX_OVER:** Same as in reg_IC_INTR_STAT
2	0x0 RO	**RX_FULL:** Same as in reg_IC_INTR_STAT
1	0x0 RO	**RX_OVER:** Same as in reg_IC_INTR_STAT
0	0x0 RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT

9.20.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

I2C Receive FIFO Threshold Register

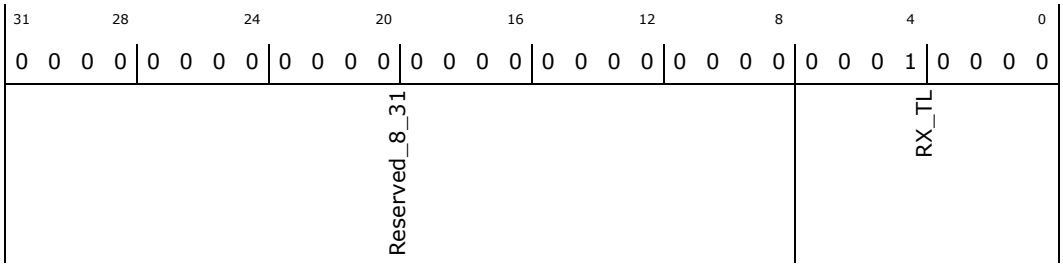
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x10 RW	**RX_TL:** Receive FIFO Threshold Level. The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

9.20.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

I2C Transmit FIFO Threshold Register

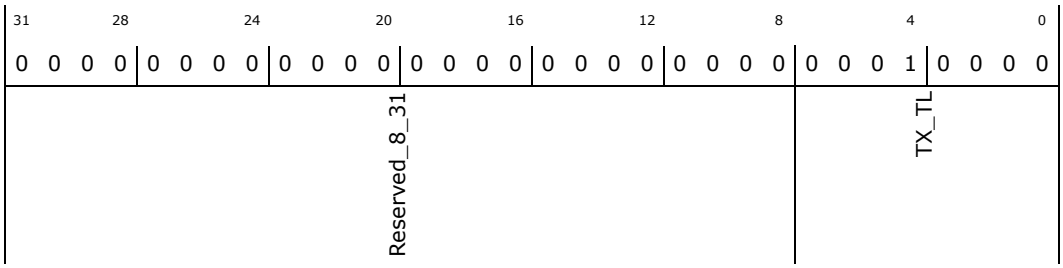
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x10 RW	**TX_TL:** Transmit FIFO Threshold Level. Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

9.20.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

Clear Combined and Individual Interrupt Register

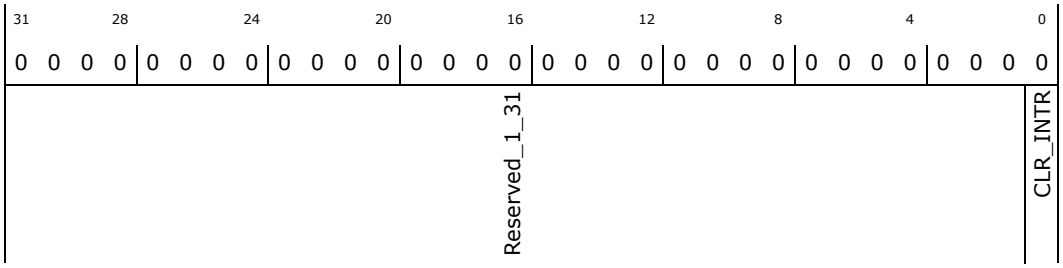
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

9.20.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

Clear RX_UNDER Interrupt Register

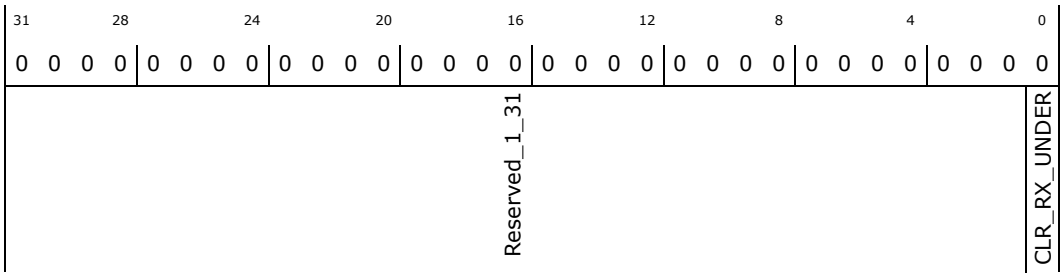
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

9.20.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

Clear RX_OVER Interrupt Register

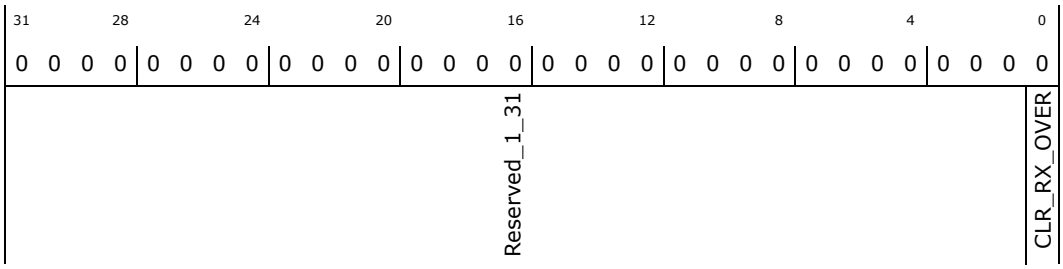
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

9.20.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

Clear TX_OVER Interrupt Register

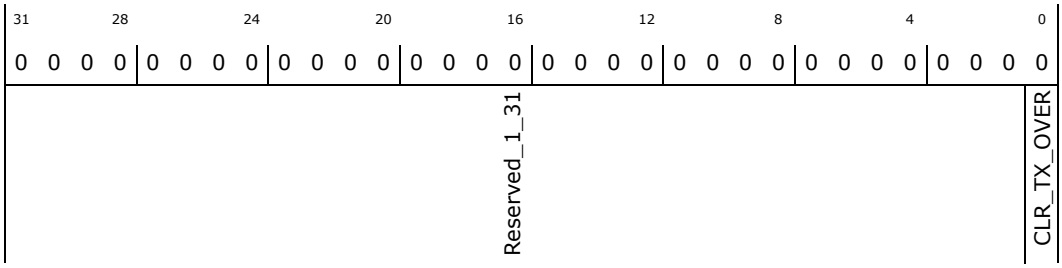
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

9.20.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

Clear RD_REQ Interrupt Register

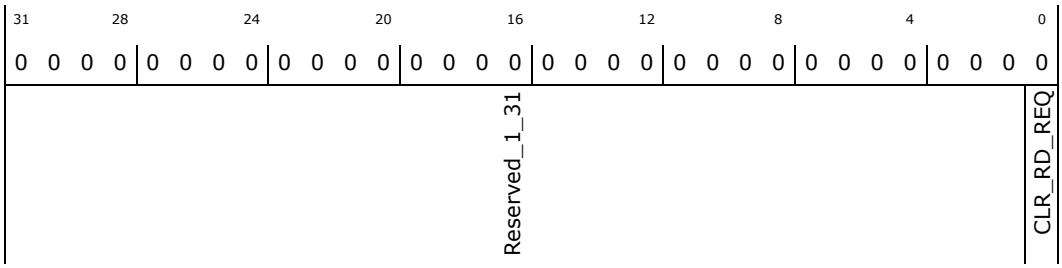
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

9.20.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

Clear TX_ABRT Interrupt Register

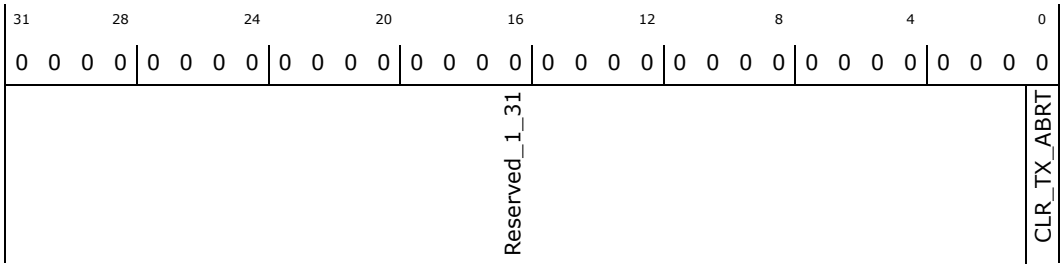
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

9.20.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

Clear RX_DONE Interrupt Register

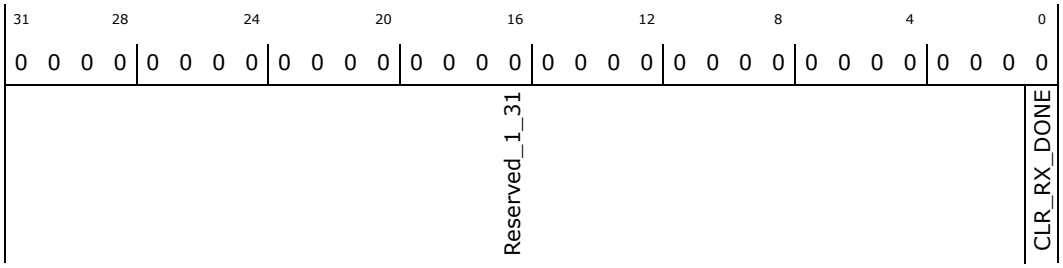
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

9.20.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

Clear ACTIVITY Interrupt Register

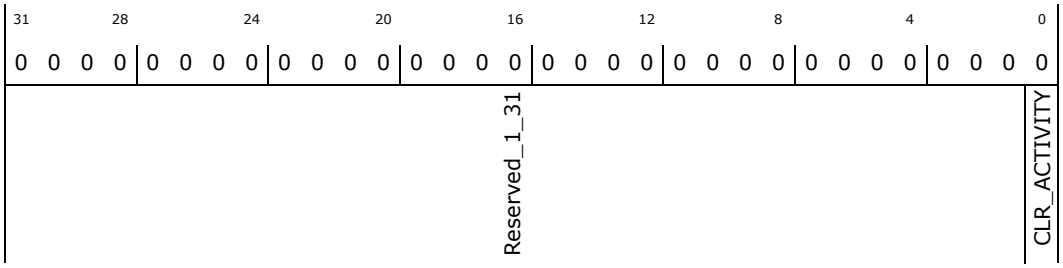
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

9.20.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

Clear STOP_DET Interrupt Register

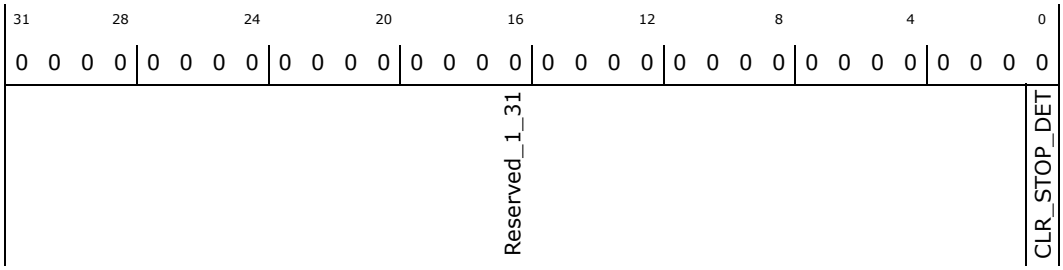
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

9.20.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

Clear START_DET Interrupt Register

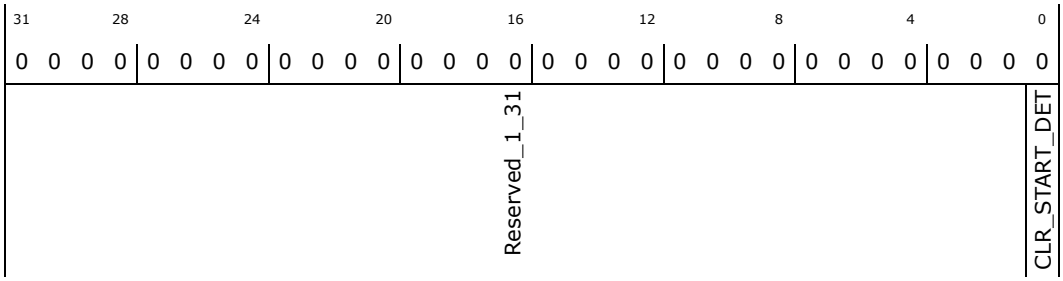
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

9.20.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

Clear GEN_CALL Interrupt Register

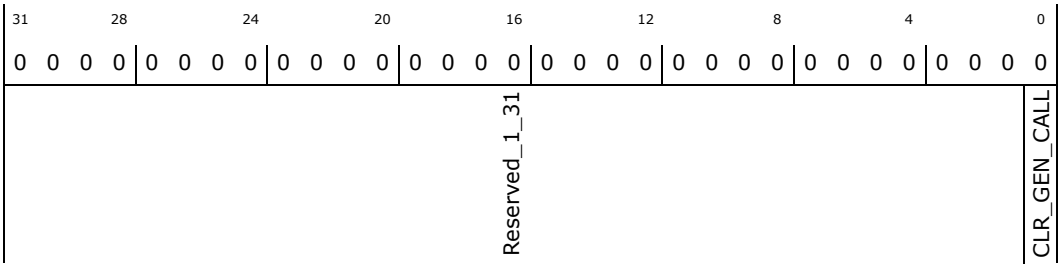
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

9.20.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

I2C Enable Register

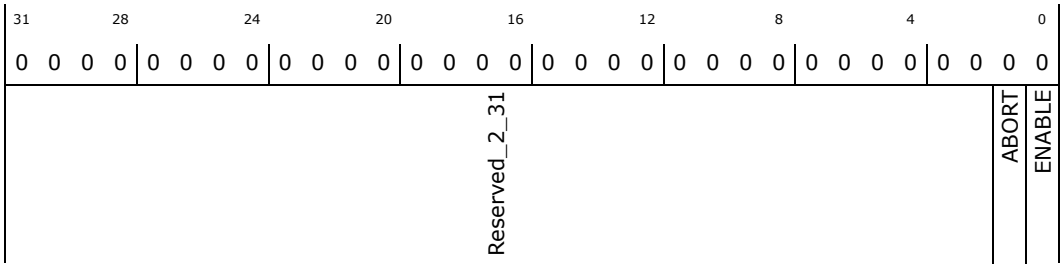
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved_2_31:** Reserved
1	0x0 WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.
0	0x0 RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) 1: Enables DW_apb_i2c

9.20.29 I2C Status Register (IC_STATUS)—Offset 70h

I2C Status Register

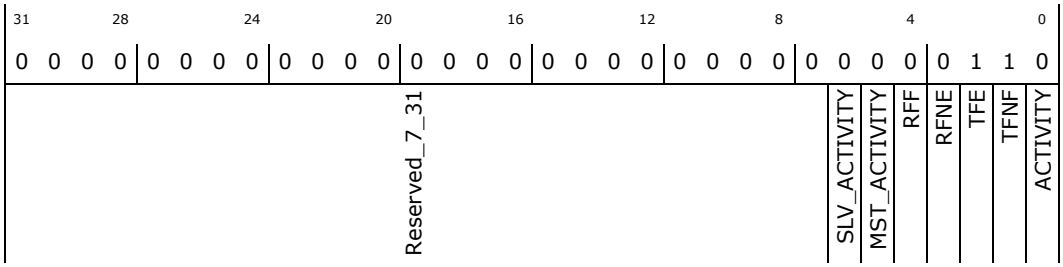
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000006h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RW	**Reserved_7_31:** Reserved
6	0x0 RO	**SLV_ACTIVITY:** Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0x0 RO	**MST_ACTIVITY:** Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RO	**RFF:** Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0x0 RO	**RFNE:** Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.
2	0x1 RO	**TFE:** Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	0x1 RO	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0x0 RO	**ACTIVITY:** I2C Activity Status

9.20.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

I2C Transmit FIFO Level Register

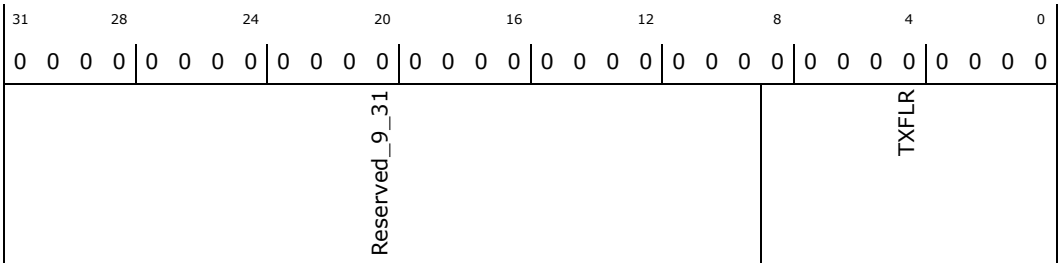
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved_9_31:** Reserved
8:0	0x0 RO	**TXFLR:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

9.20.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

I2C Receive FIFO Level Register

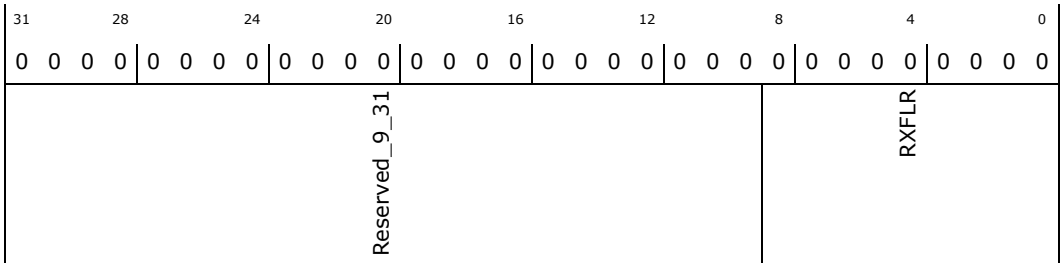
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved_9_31:** Reserved
8:0	0x0 RO	**RXFLR:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

9.20.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

I2C SDA Hold Time Length Register

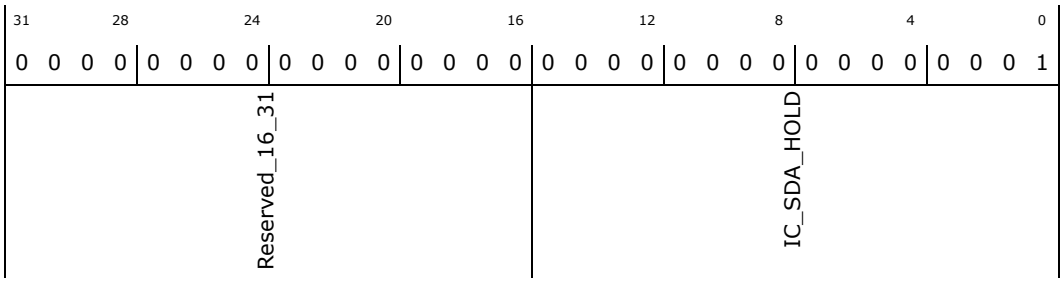
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x1 RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

9.20.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

I2C Transmit Abort Source Register

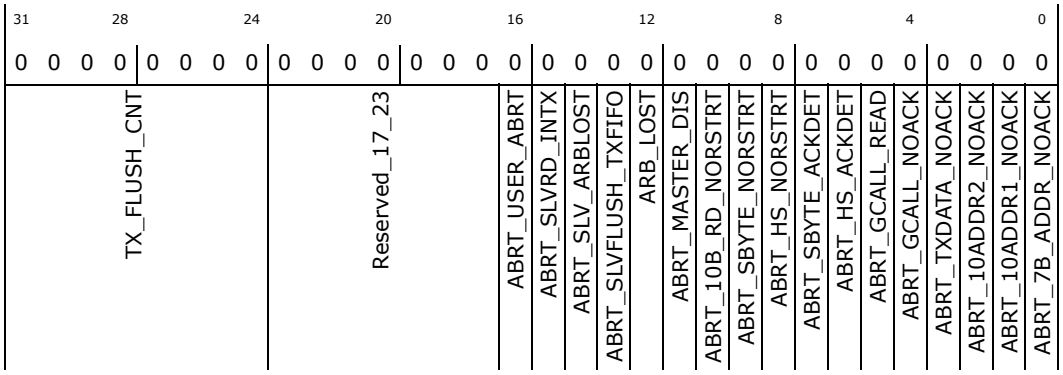
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0x0 RW	**Reserved_17_23:** Reserved
16	0x0 RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0x0 RO	**ABRT_SLVRD_INTX:** 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0x0 RO	**ABRT_SLV_ARBLOST:** 1: Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0x0 RO	**ABRT_SLVFLUSH_TXFIFO:** 1: Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0x0 RO	**ARB_LOST:** 1: Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0x0 RO	**ABRT_MASTER_DIS:** 1: User tries to initiate a Master operation with the Master mode disabled.
10	0x0 RO	**ABRT_10B_RD_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RO	**ABRT_SBYTE_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0x0 RO	**ABRT_HS_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0x0 RO	**ABRT_SBYTE_ACKDET:** 1: Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
6	0x0 RO	**ABRT_HS_ACKDET:** 1: Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
5	0x0 RO	**ABRT_GCALL_READ:** 1: DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0x0 RO	**ABRT_GCALL_NOACK:** 1: DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0x0 RO	**ABRT_TXDATA_NOACK:** 1: This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0x0 RO	**ABRT_10ADDR2_NOACK:** 1: Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0x0 RO	**ABRT_10ADDR1_NOACK:** 1: Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0x0 RO	**ABRT_7B_ADDR_NOACK:** 1: Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

9.20.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

Generate Slave Data NACK Register

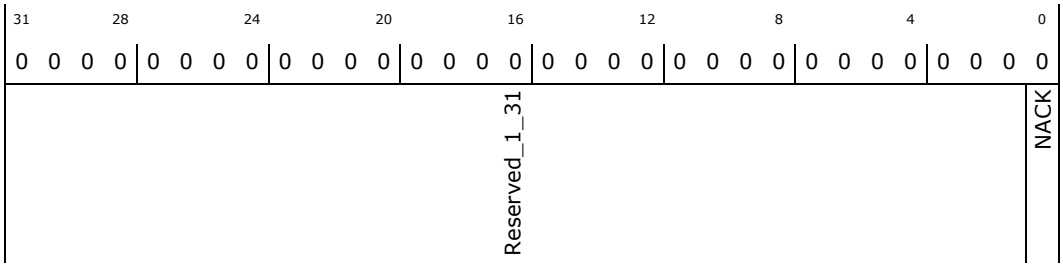
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RW	**NACK:** Generate NACK. This NACK generation only occurs when DW_apb_i2c is a slavereceiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. 1 = generate NACK after data byte received 0 = generate NACK/ACK normally

9.20.35 DMA Control Register (IC_DMA_CR)—Offset 88h

DMA Control Register

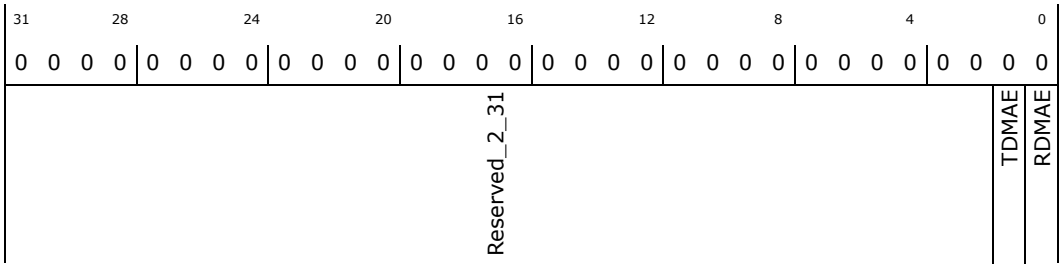
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved_2_31:** Reserved
1	0x0 RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel. 0 = Transmit DMA disabled 1 = Transmit DMA enabled
0	0x0 RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. 0 = Receive DMA disabled 1 = Receive DMA enabled

9.20.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

DMA Transmit Data Level Register

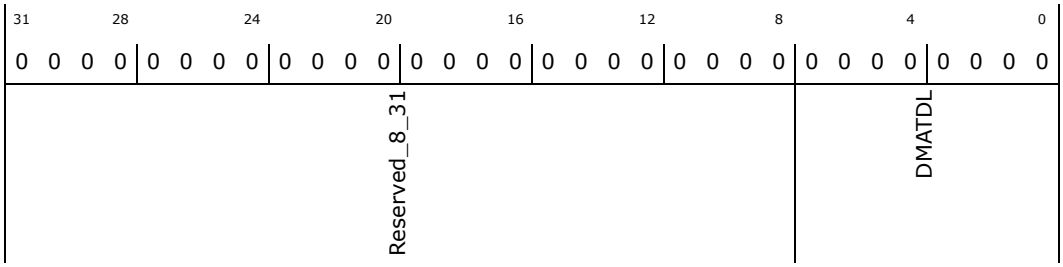
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x0 RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

9.20.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

I2C Receive Data Level Register

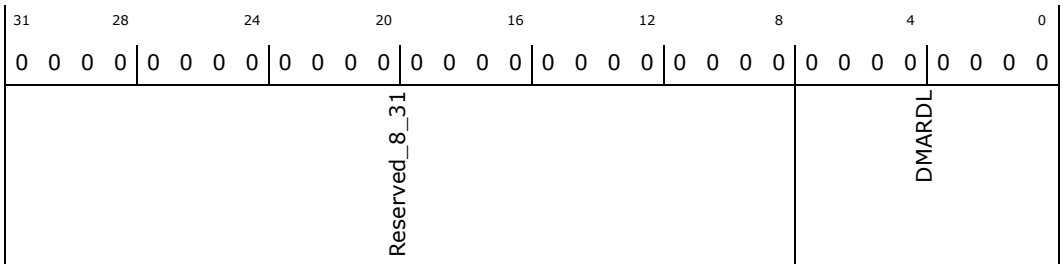
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x0 RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

9.20.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

I2C SDA Setup Register

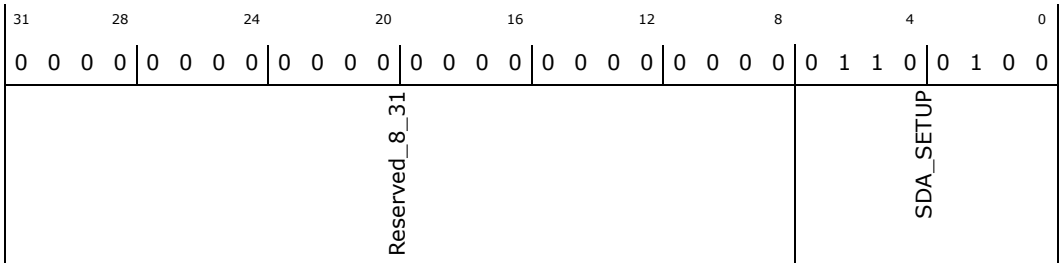
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000064h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x64 RW	**SDA_SETUP:** SDA Setup. It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

9.20.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

I2C ACK General Call Register

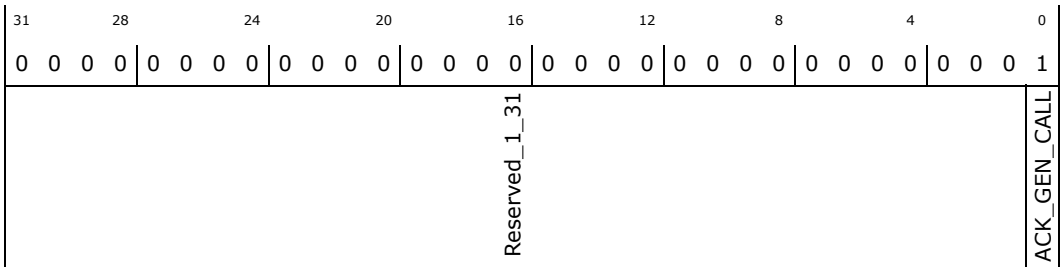
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x1 RW	**ACK_GEN_CALL:** ACK General Call. When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

9.20.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

I2C Enable Status Register

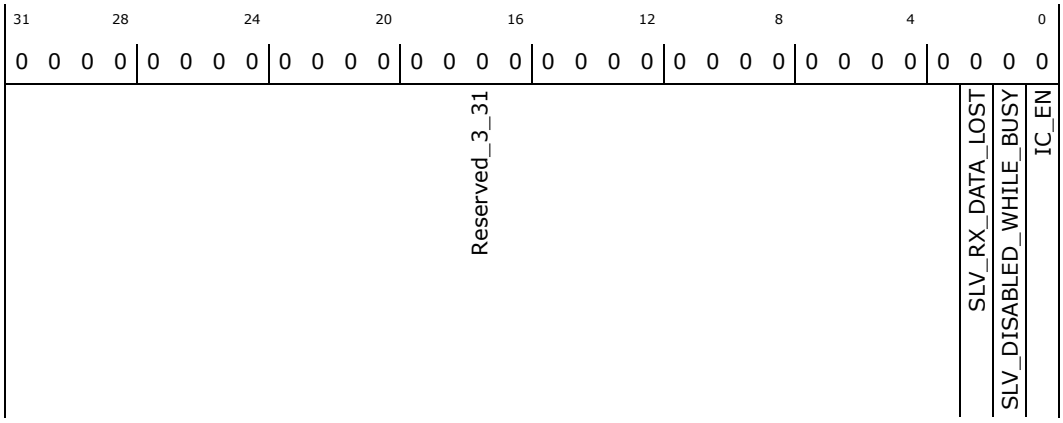
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved_3_31:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0x0 RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0x0 RO	**IC_EN:** ic_en Status. This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

9.20.41 SS/FS Mode Spike Length Register (IC_FS_SPKLEN)—Offset A0h

SS/FS Mode Spike Length Register

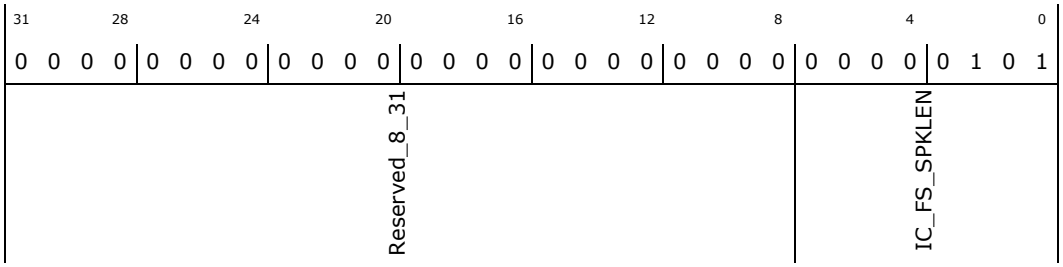
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000005h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x5 RW	**IC_FS_SPKLEN:** Maximum length (in ic_clk cycles) of suppressed spikes in SS and FS modes

9.20.42 HS Mode Spike Length Register (IC_HS_SPKLEN)—Offset A4h

HS Mode Spike Length Register

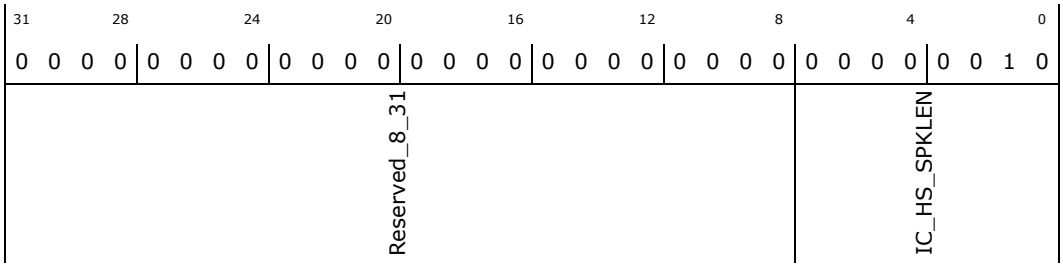
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x2 RW	**IC_HS_SPKLEN:** Maximum length (in ic_clk cycles) of suppressed spikes in HS mode

9.20.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

Component Parameter Register 1

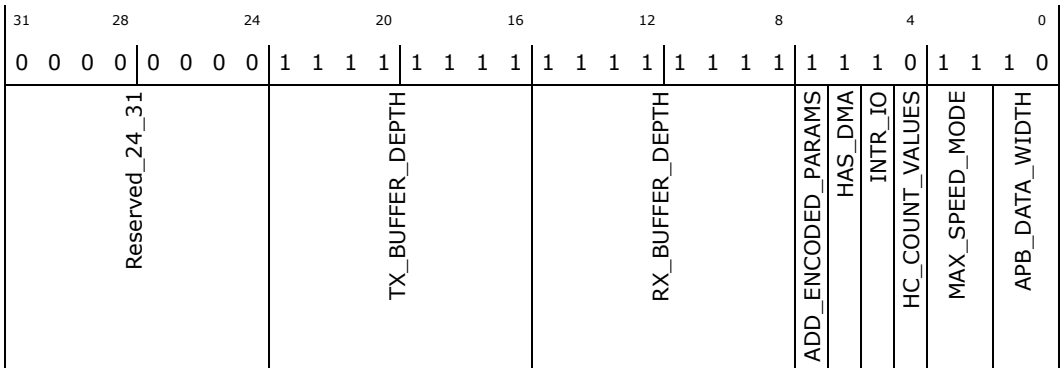
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00FFFFEEh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved_24_31:** Reserved
23:16	0xff RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	0xff RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	0x1 RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	0x1 RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	0x1 RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0x0 RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	0x3 RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	0x2 RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

9.20.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

I2C Component Version Register

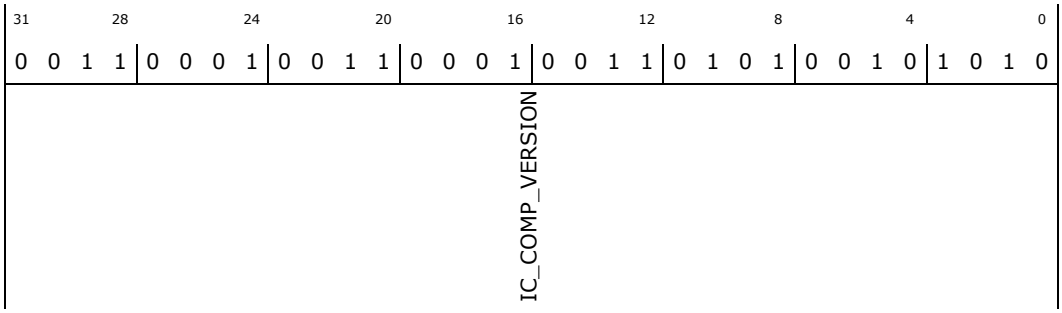
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 3131352Ah



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x3131352a RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes

9.20.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

I2C Component Type Register

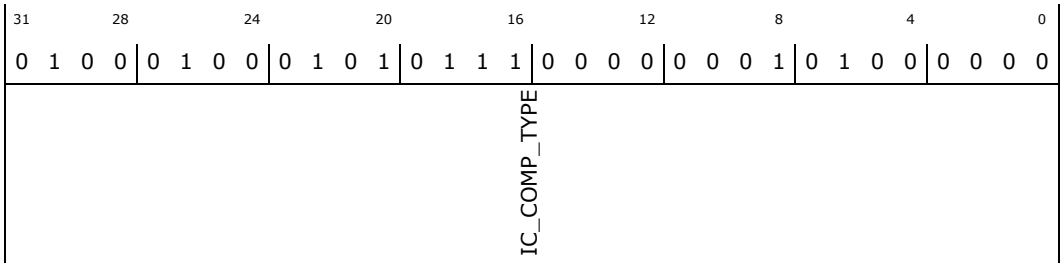
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 44570140h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x44570140 RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

9.20.46 Clock params register (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

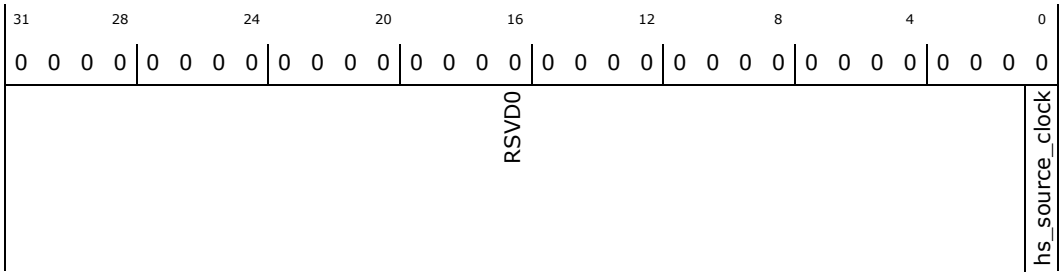
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz 1 -133MHz (high-speed operation compatible)

9.20.47 software reset (RESETS)—Offset 804h

software reset

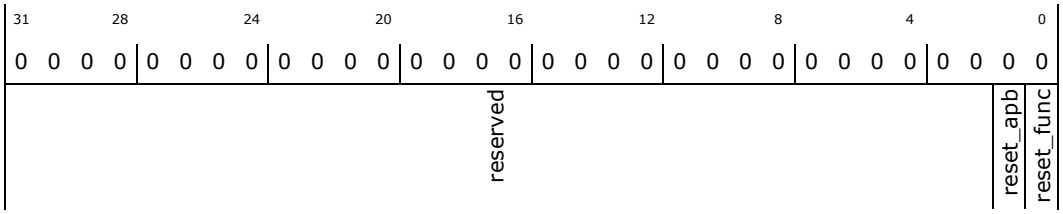
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (reserved):** Reserved
1	0x0 RW	**reset_apb:** reset the apb domain
0	0x0 RW	**reset_func:** reset the func clock domain

9.20.48 General purpose register (GENERAL)—Offset 808h

General purpose register

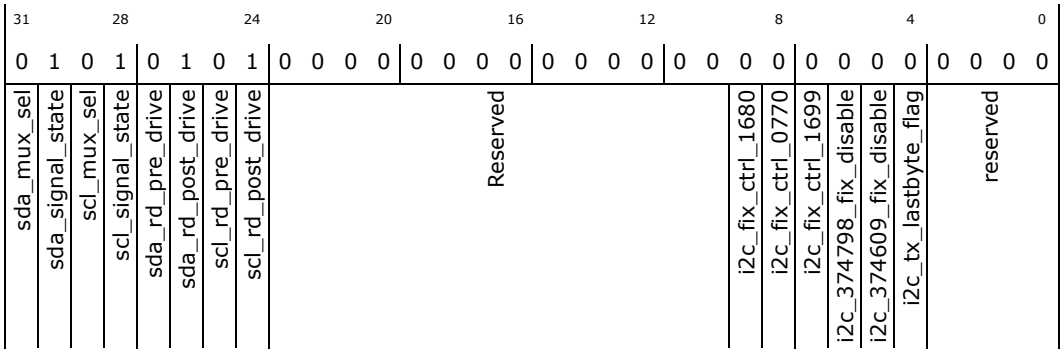
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 55000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**sda_mux_sel:** This bit selects the driver for the SDA signal: 1 = sda_signal_state, 0 = I2C logic
30	0x1 RW	**sda_signal_state:** This bit is used when sda_mux_sel = 1, used to drive the SDA signal on the I2C interface
29	0x0 RW	**scl_mux_sel:** This bit selects the driver for the SCL signal: 1 = scl_signal_state, 0 = I2C logic
28	0x1 RW	**scl_signal_state:** This bit is used when scl_mux_sel = 1, used to drive the SCL signal on the I2C interface
27	0x0 RO	**sda_rd_pre_drive:** Read only bit used to see the status of the SDA signal coming from the I2C logic
26	0x1 RO	**sda_rd_post_drive:** Read only bit used to see the status of the SDA signal coming from the pad
25	0x0 RO	**scl_rd_pre_drive:** Read only bit used to see the status of the SCL signal coming from the I2C logic
24	0x1 RO	**scl_rd_post_drive:** Read only bit used to see the status of the SCL signal coming from the pad
23:10	0x0 RO	**Reserved:** Reserved
9	0x0 RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0x0 RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0x0 RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0x0 RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)
5	0x0 RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0x0 RW	**reserved:** reserved

9.20.49 TX transaction counter (I2C_ACK_COUNT)—Offset 818h

TX transaction counter

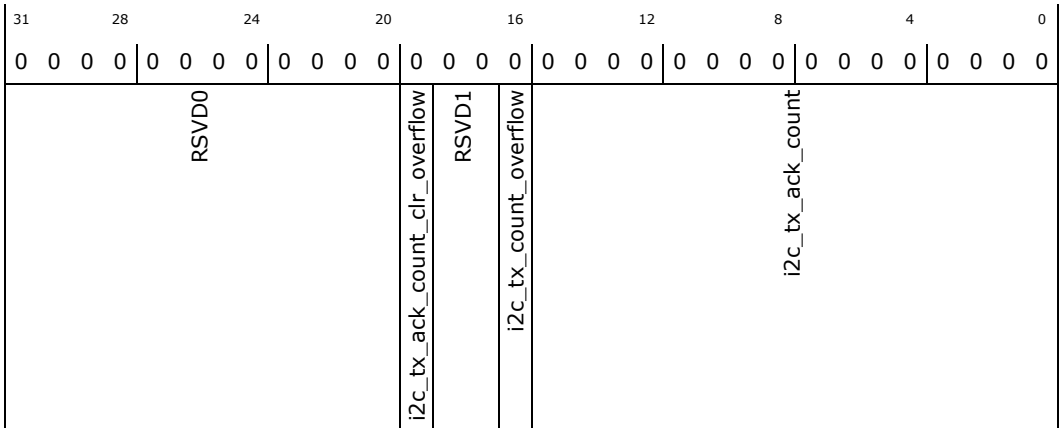
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RSVD0:** Reserved
19	0x0 RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0x0 RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

9.20.50 TX transaction complete interrupt status register (I2C_TX_COMPLETE_INTR_STAT)—Offset 820h

TX transaction has finished interrupt

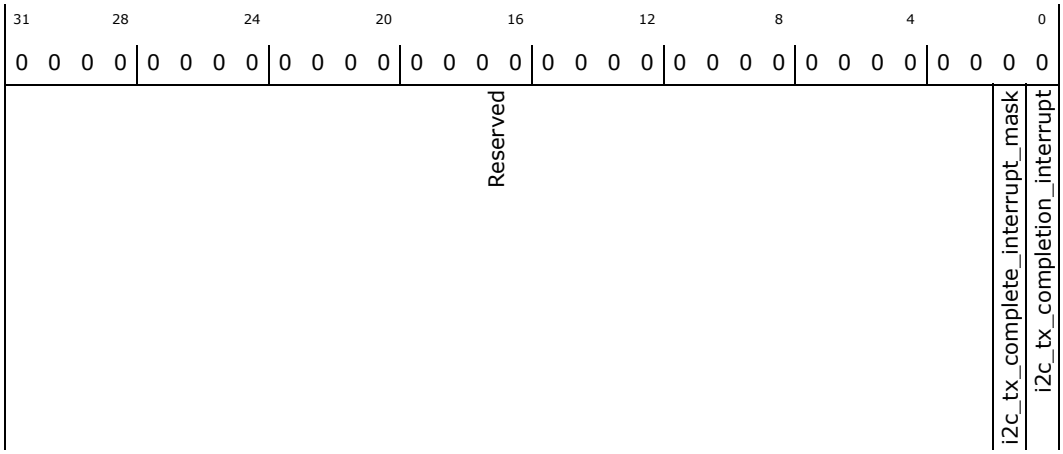
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved:** Reserved
1	0x0 RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0x0 RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

9.20.51 TX transaction complete interrupt clear register (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

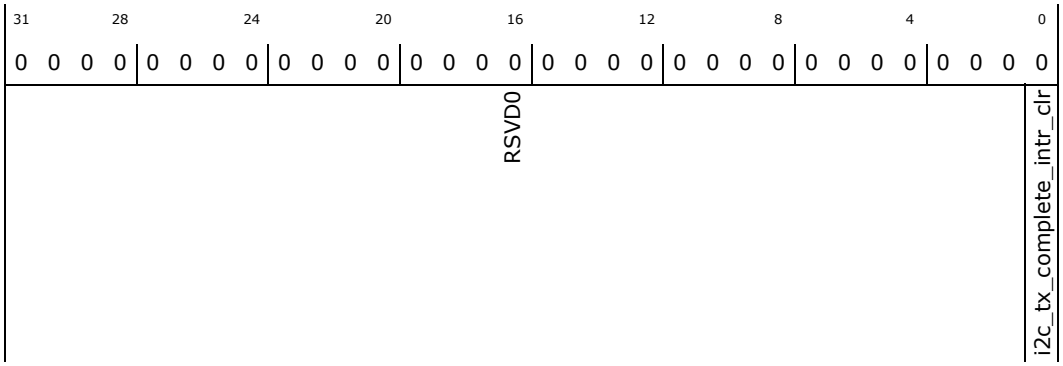
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:5] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt

9.21 SIO I2C 5 PCI Configuration Registers

Table 84. Summary of SIO I2C 5 PCI Configuration Registers—0/24/6

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4555	00008086h
4–7h	4	"STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h" on page 4555	00100000h
8–Bh	4	"REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4557	00000000h
C–Fh	4	"CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4558	00800000h
10–13h	4	"BAR -Base Address Register (BAR)—Offset 10h" on page 4558	00000000h
14–17h	4	"BAR1 -Base Address Register1 (BAR1)—Offset 14h" on page 4559	00000000h
2C–2Fh	4	"SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4560	00000000h
30–33h	4	"EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4561	00000000h
34–37h	4	"CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4561	00000000h
3C–3Fh	4	"INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4562	00000100h
80–83h	4	"POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4562	00030001h
84–87h	4	"PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4563	00000008h
F8–FBh	4	"Manufacturers ID (MANID)—Offset F8h" on page 4564	00000000h

9.21.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

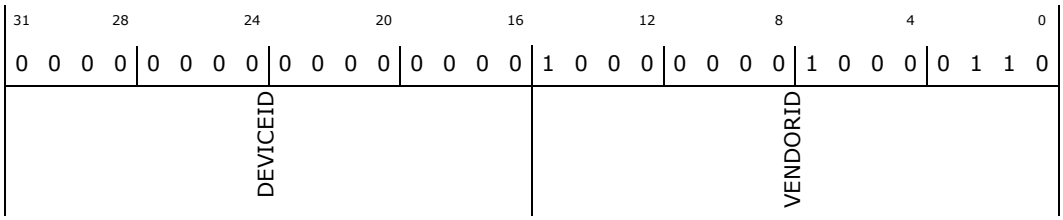
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**DEVICEID:** Device ID identifies the particular AHB/APB device. This is tied to a strap at the top level. Because of tool issues, the HTML files show this field as 0, but the following are the POR values for SoC: LPIO1 DMA: 0x2286 LPIO1 PWM1: 0x2288 LPIO1 PWM2: 0x2289 LPIO1 HSUART1: 0x228A LPIO1 HSUART2: 0x228C LPIO1 SPI1: 0x228E LPIO1 SPI2: 0x2290 LPIO1 SPI3: 0x22AC LPIO2 DMA: 0x22C0 LPIO2 I2C1: 0x22C1 LPIO2 I2C2: 0x22C2 LPIO2 I2C3: 0x22C3 LPIO2 I2C4: 0x22C4 LPIO2 I2C5: 0x22C5 LPIO2 I2C6: 0x22C6 LPIO2 I2C7: 0x22C7 For the final word on this, please see Ray Ng's SoC RevID and DevID HAS on Infofactory: https://ifcollaborate.intel.com/IFC/getdoc.aspx?docbase=InfoFactoryKBandchronid=09005ffd80e84b43andver=CURRENTandqepop=false
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap the top level.

9.21.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

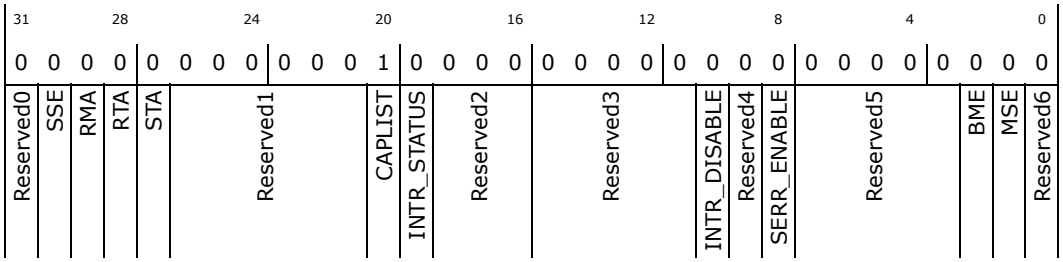
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved0:** Reserved
30	0x0 RW/1C	**SSE:** This bit is set when a device sends an DO_SERR message, and the SERR# Enable bit in the Command register is 1
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric PortReceived Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27	0x0 RW/1C	**STA:** The Bridge sets this bit whenever it responds to a transaction with CA abort. If the SERR# Enable bit is set, the Bridge sets the Signaled System Error bit and sends an DO_SERR message on the IOSF Sideband.
26:21	0x0 RO	**Reserved1:** Reserved
20	0x1 RO	**CAPLIST:** Capabilities List: Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt .i.e Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.. Reset value of this bit is 0.
9	0x0 RO	**Reserved4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: If both SERR# Enable and the Unsupported Request Reporting Enable (URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0x0 RO	**Reserved6:** Reserved

9.21.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

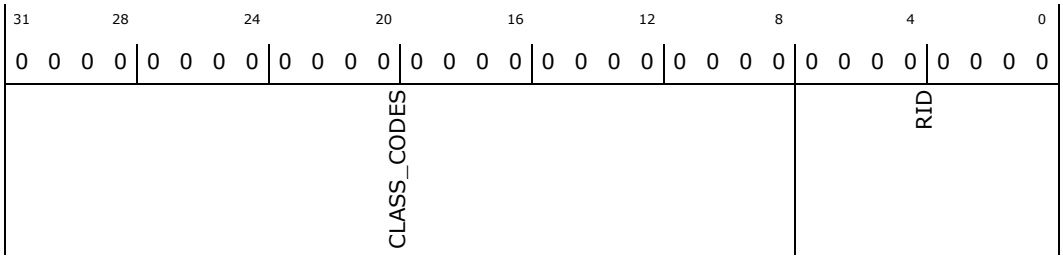
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

9.21.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

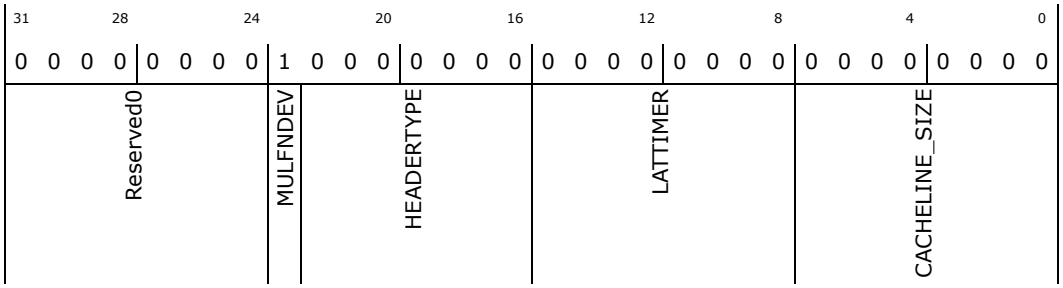
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + Ch

Default: 00800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x1 RO	**MULFNDEV:** Multi Function Device: This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. Value of 1 indicates multifunction device value of 0 indicates single function device
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	0x0 RO	**LATTIMER:** Latency Timer: Doesn.t apply to PCI Express. Hardwired to 00h.
7:0	0x0 RW	**CACHELINE_SIZE:** Cache Line Size: Doesn.t apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

9.21.5 BAR -Base Address Register (BAR)—Offset 10h

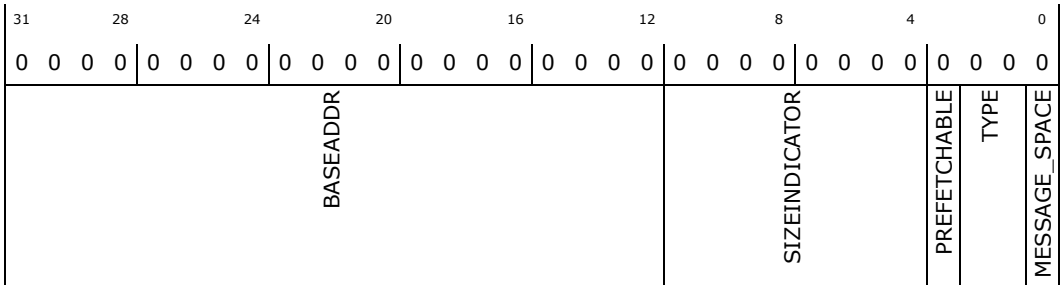
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the AHB device memory space. Taken from Strap values as 1's. Please note that for DMA this field goes from [31:14], or 16kbyte, and the SIZEINDICATOR field goes from [13:4].
11:4	0x0 RO	**SIZEINDICATOR:** Size Indicator Read Only: Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0x0 RO	**TYPE:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.21.6 BAR1 -Base Address Register1 (BAR1)—Offset 14h

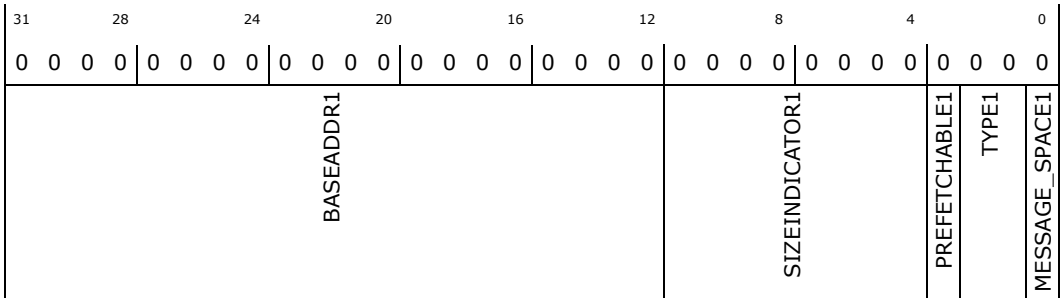
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	0x0 RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not
2:1	0x0 RO	**TYPE1:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.21.7 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

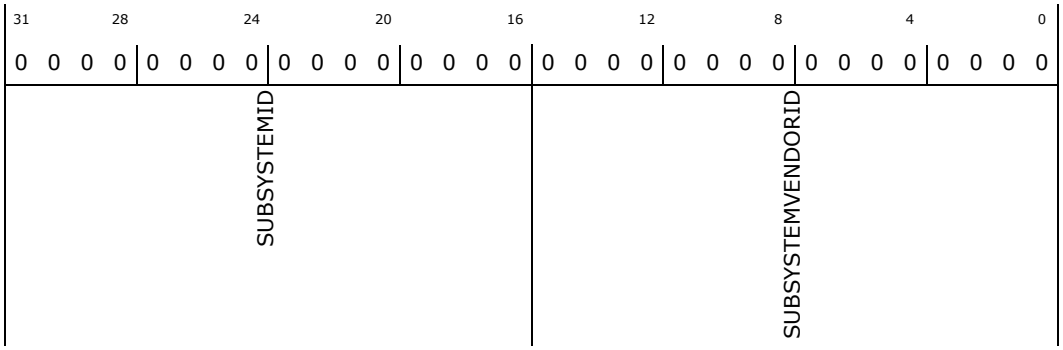
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

9.21.8 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

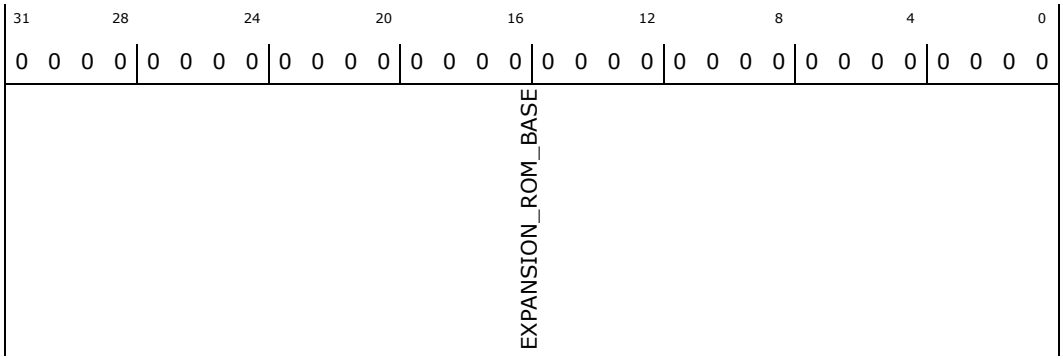
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** A value of all zeros indicates no support for expansion ROM.

9.21.9 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

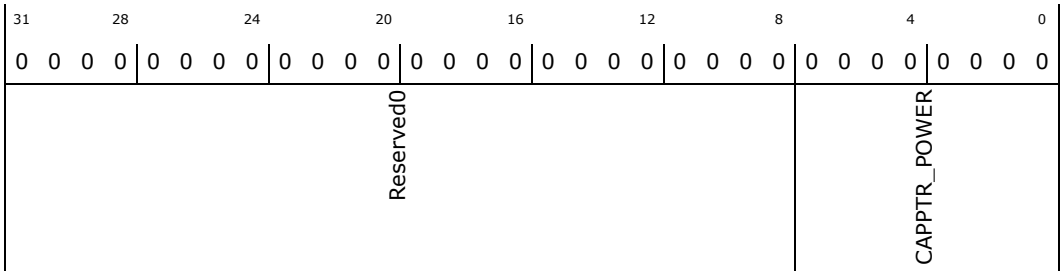
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x0 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

9.21.10 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

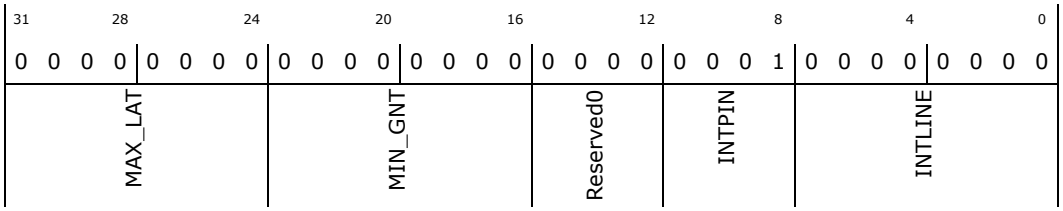
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

9.21.11 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

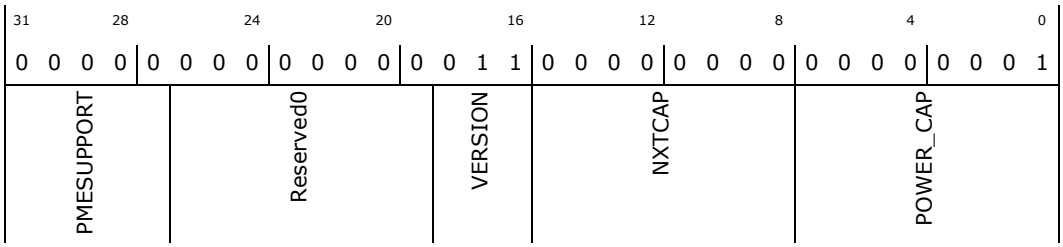
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** PME_Support - This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

9.21.12 PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

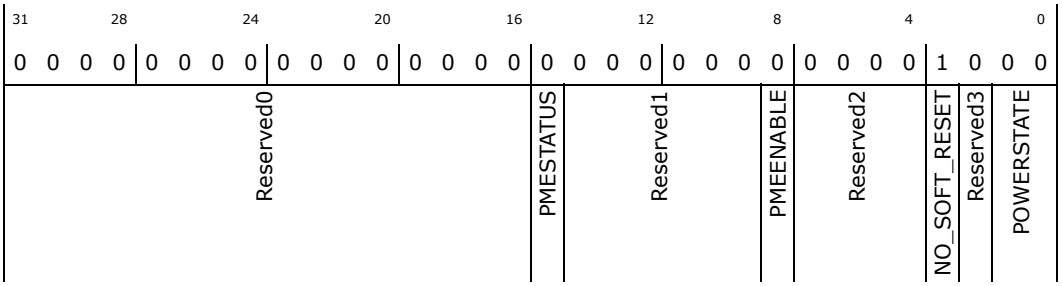
PMECTRLSTATUS - PME Control and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

9.21.13 Manufacturers ID (MANID)—Offset F8h

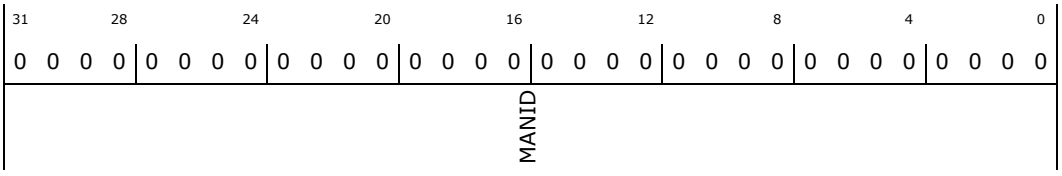
Manufacturers ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:6] + F8h

Default: 00000000h

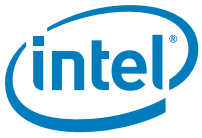


Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: This register is brought out as straps to the top level.

9.22 SIO I2C 5 Memory Mapped Registers

Table 85. Summary of SIO I2C 5 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 4569	0000007Fh
4–7h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 4570	00001055h
8–Bh	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 4571	00000055h
C–Fh	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 4571	00000001h
10–13h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 4572	00000000h
14–17h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 4573	00000190h
18–1Bh	4	"Standard Speed I2C Clock SCL Low Count Register. (IC_SS_SCL_LCNT)—Offset 18h" on page 4574	000001D6h
1C–1Fh	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 4574	0000003Ch
20–23h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 4575	00000082h
24–27h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 4576	0000000Ch
28–2Bh	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 4576	00000020h
2C–2Fh	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 4577	00000000h
30–33h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 4578	000008FFh
34–37h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 4579	00000000h
38–3Bh	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 4580	00000010h
3C–3Fh	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 4581	00000010h
40–43h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 4582	00000000h
44–47h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 4582	00000000h
48–4Bh	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 4583	00000000h
4C–4Fh	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 4584	00000000h
50–53h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 4584	00000000h
54–57h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 4585	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
58–5Bh	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 4585	00000000h
5C–5Fh	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 4586	00000000h
60–63h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 4587	00000000h
64–67h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 4587	00000000h
68–6Bh	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 4588	00000000h
6C–6Fh	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 4588	00000000h
70–73h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 4589	00000006h
74–77h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 4590	00000000h
78–7Bh	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 4590	00000000h
7C–7Fh	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 4591	00000001h
80–83h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 4592	00000000h
84–87h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 4593	00000000h
88–8Bh	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 4594	00000000h
8C–8Fh	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 4594	00000000h
90–93h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 4595	00000000h
94–97h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 4596	00000064h
98–9Bh	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 4596	00000001h
9C–9Fh	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 4597	00000000h
A0–A3h	4	"SS/FS Mode Spike Length Register (IC_FS_SPKLEN)—Offset A0h" on page 4598	00000005h
A4–A7h	4	"HS Mode Spike Length Register (IC_HS_SPKLEN)—Offset A4h" on page 4598	00000002h
F4–F7h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 4599	00FFFFEEh
F8–FBh	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 4600	3131352Ah
FC–FFh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 4601	44570140h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
800–803h	4	"Clock params register (CLOCK_PARAMS)—Offset 800h" on page 4601	00000000h
804–807h	4	"software reset (RESETS)—Offset 804h" on page 4602	00000000h
808–80Bh	4	"General purpose register (GENERAL)—Offset 808h" on page 4602	55000000h
818–81Bh	4	"TX transaction counter (I2C_ACK_COUNT)—Offset 818h" on page 4604	00000000h
820–823h	4	"TX transaction complete interrupt status register (I2C_TX_COMPLETE_INTR_STAT)—Offset 820h" on page 4605	00000000h
824–827h	4	"TX transaction complete interrupt clear register (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 4605	00000000h

9.22.1 I2C Control Register (IC_CON)—Offset 0h

I2C Control Register

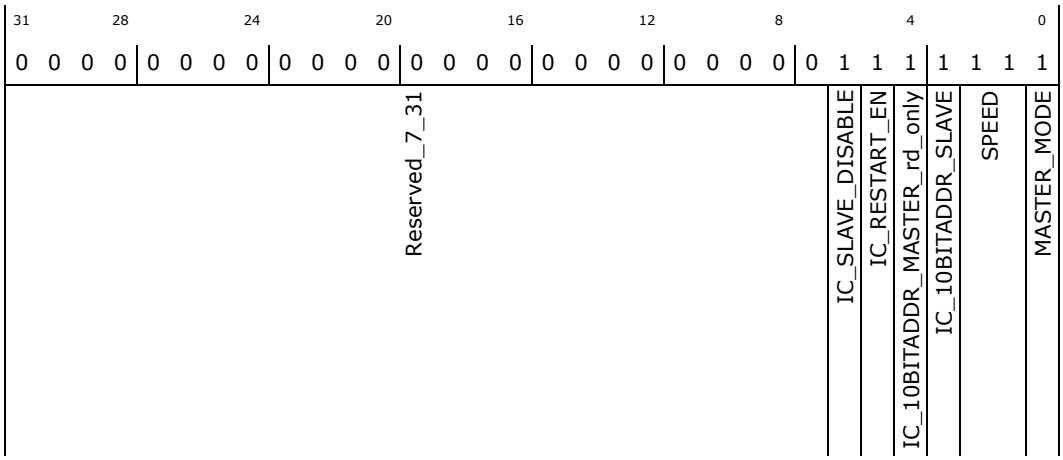
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 0000007Fh



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RW	**Reserved_7_31:** Reserved
6	0x1 RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	0x1 RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master.When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: Sending a START BYTE. Performing any high-speed mode operation. Performing direction changes in combined format mode. Performing a read operation with a 10-bit address
4	0x1 RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register
3	0x1 RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0x3 RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	0x1 RW	**MASTER_MODE:** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

9.22.2 I2C Target Address Register (IC_TAR)—Offset 4h

I2C Target Address Register

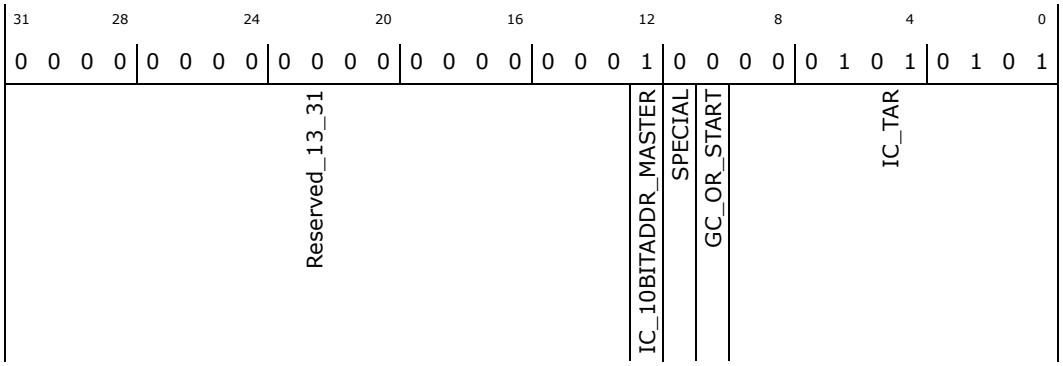
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00001055h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Reserved_13_31:** Reserved
12	0x1 RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master. This bit exists in this register only if the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 1
11	0x0 RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. 0: ignore bit 10 GC_OR_START and use IC_TAR normally. 1: perform special I2C command as specified in GC_OR_START bit
10	0x0 RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.

Bit Range	Default & Access	Field Name (ID): Description
9:0	0x55 RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

9.22.3 I2C Slave Address Register (IC_SAR)—Offset 8h

I2C Slave Address Register

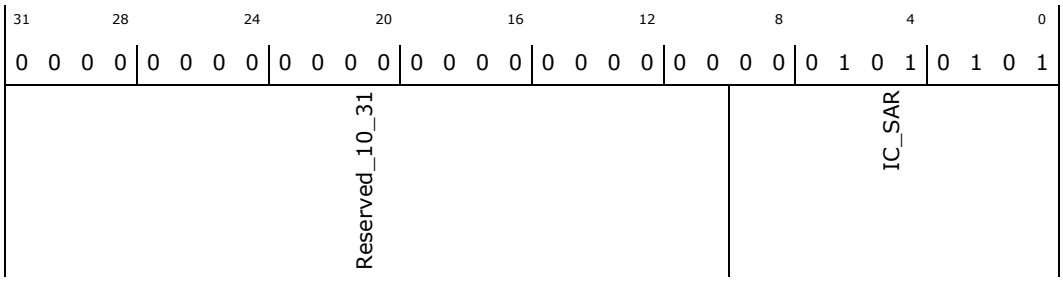
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000055h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**Reserved_10_31:** Reserved
9:0	0x55 RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.22.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

I2C High Speed Master Mode Code Address Register

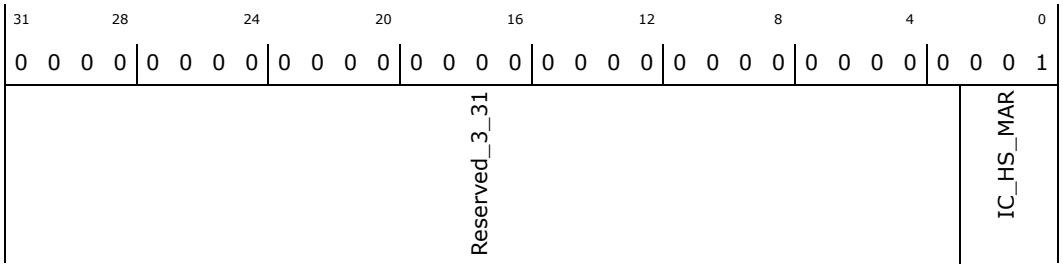
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved_3_31:** Reserved
2:0	0x1 RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.22.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

I2C Rx/Tx Data Buffer and Command Register; this is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO

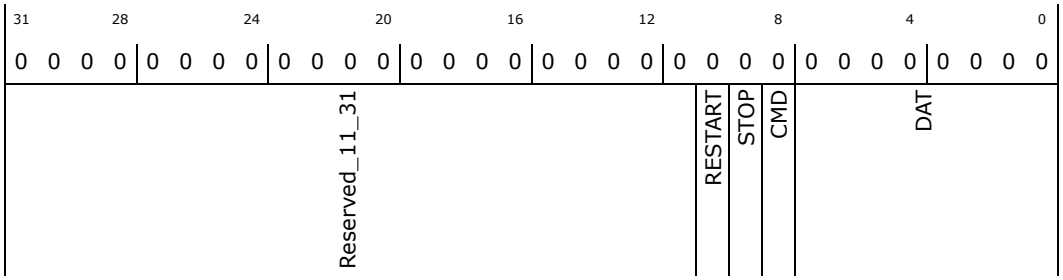
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:11	0x0 RW	**Reserved_11_31:** Reserved
10	0x0 RW	**RESTART:** RESTART
9	0x0 RW	**STOP:** STOP
8	0x0 RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It controls only the direction when it acts as a master. 1 = Read. 0 = Write
7:0	0x0 RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. However, when you read this register, these bits return the value of data received on the DW_apb_i2c interface.

9.22.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

Standard Speed I2C Clock SCL High Count Register.

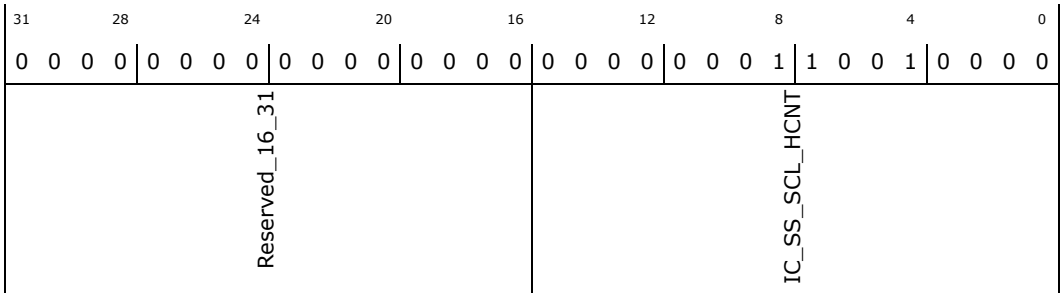
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000190h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x190 RW	**IC_SS_SCL_HCNT:** Standard Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.22.7 Standard Speed I2C Clock SCL Low Count Register. (IC_SS_SCL_LCNT)—Offset 18h

Standard Speed I2C Clock SCL Low Count Register.

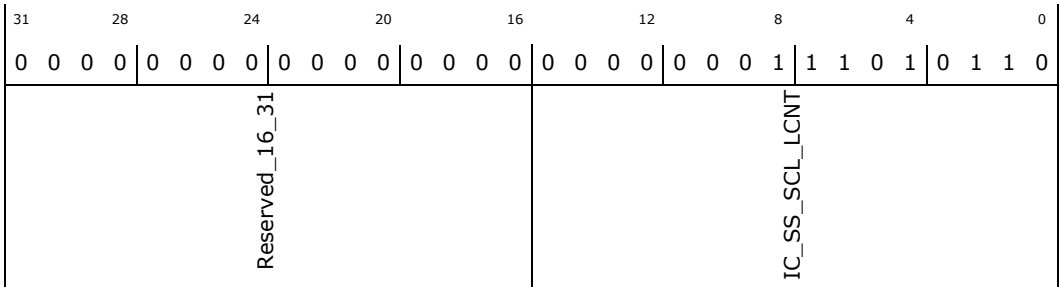
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 000001D6h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x1d6 RW	**IC_SS_SCL_LCNT:** Standard Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.22.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

Fast Speed I2C Clock SCL High Count Register

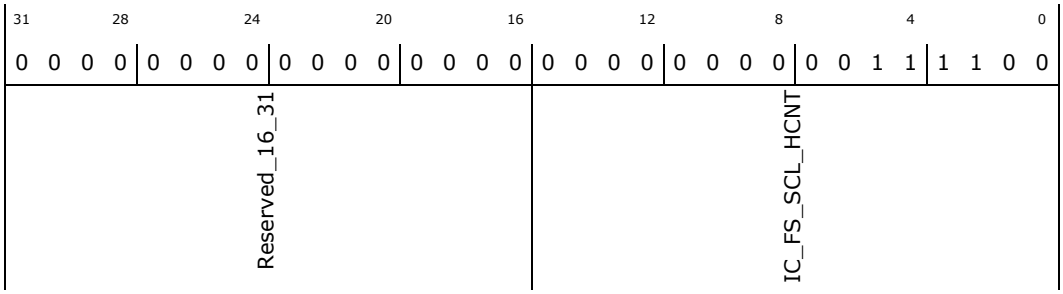
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 0000003Ch



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x3c RW	**IC_FS_SCL_HCNT:** Fast Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.22.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

Fast Speed I2C Clock SCL Low Count Register

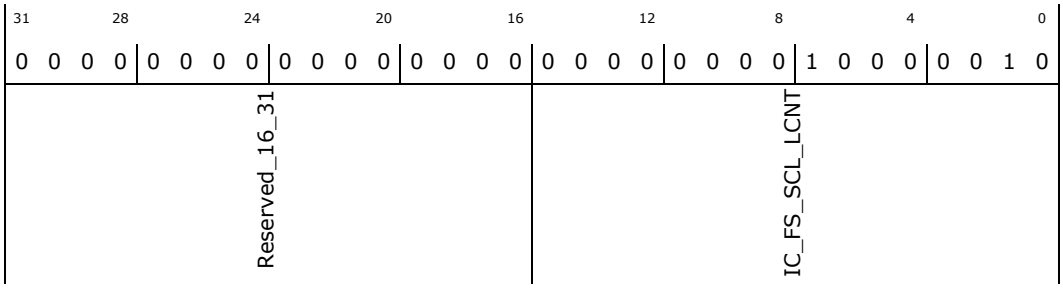
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000082h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x82 RW	**IC_FS_SCL_LCNT:** Fast Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.22.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

High Speed I2C Clock SCL High Count Register

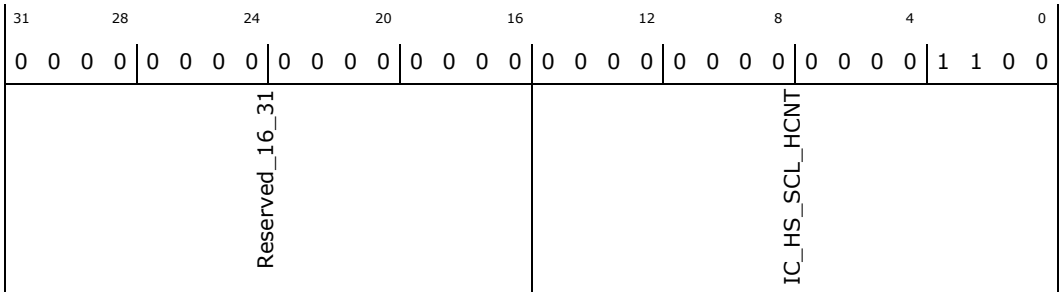
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 0000000Ch



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0xc RW	**IC_HS_SCL_HCNT:** High Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.22.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

High Speed I2C Clock SCL Low Count Register

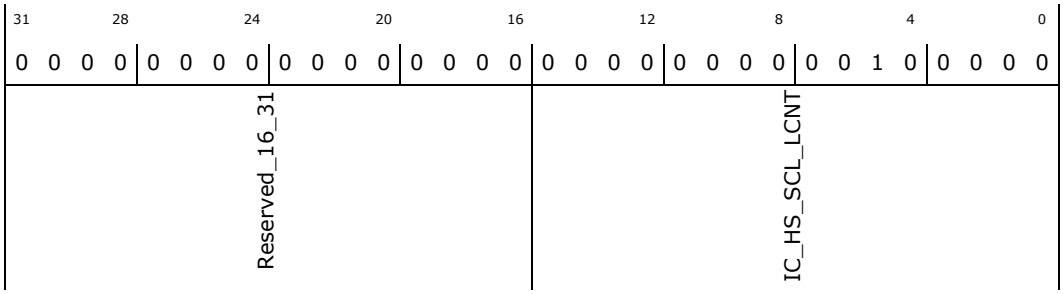
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000020h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x20 RW	**IC_HS_SCL_LCNT:** High Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.22.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

I2C Interrupt Status Register

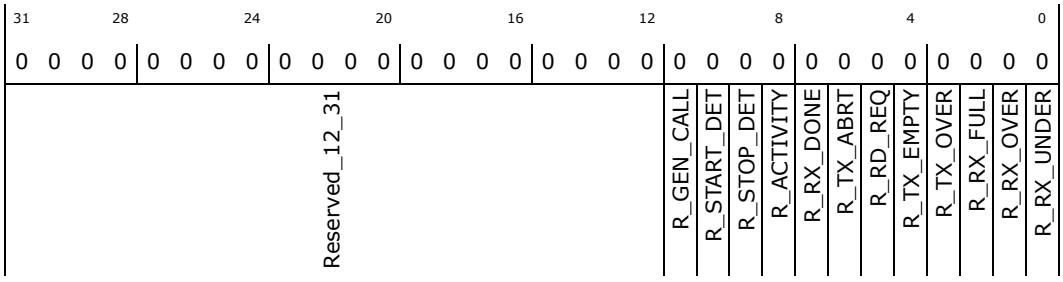
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x0 RO	**R_GEN_CALL:** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0x0 RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0x0 RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0x0 RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0x0 RO	**R_TX_ABRT:** This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0x0 RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.
4	0x0 RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0x0 RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0x0 RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0x0 RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0x0 RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

9.22.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

I2C Interrupt Mask Register

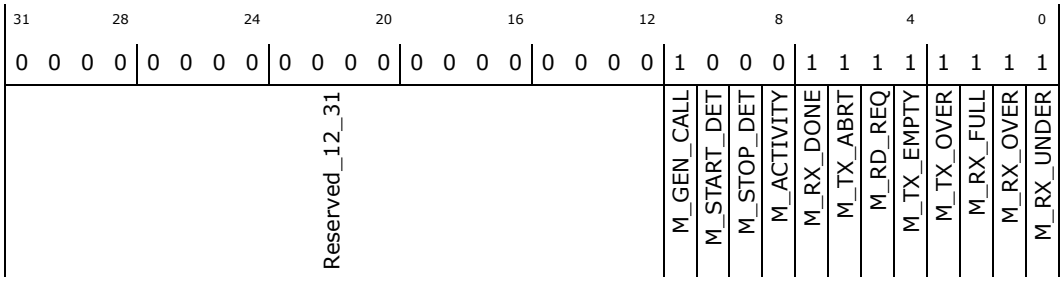
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 000008FFh



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x1 RW	**M_GEN_CALL:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
10	0x0 RW	**M_START_DET:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
9	0x0 RW	**M_STOP_DET:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
8	0x0 RW	**M_ACTIVITY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
7	0x1 RW	**M_RX_DONE:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
6	0x1 RW	**M_TX_ABRT:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
5	0x1 RW	**M_RD_REQ:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
4	0x1 RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
3	0x1 RW	**M_TX_OVER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
2	0x1 RW	**M_RX_FULL:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
1	0x1 RW	**M_RX_OVER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
0	0x1 RW	**M_RX_UNDER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.

9.22.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

I2C Raw Interrupt Status Register

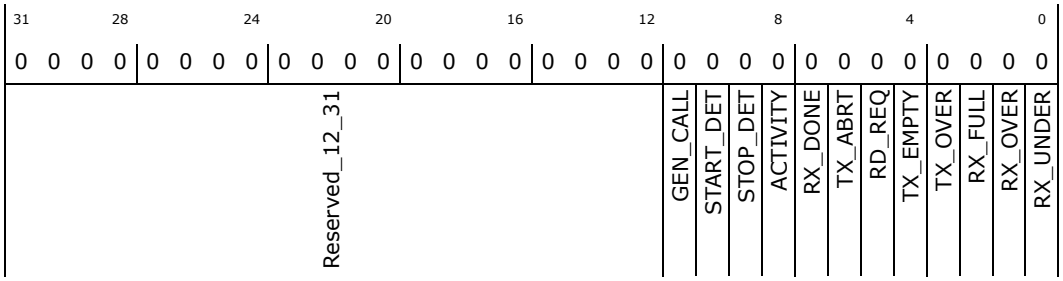
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x0 RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT
10	0x0 RO	**START_DET:** Same as in reg_IC_INTR_STAT
9	0x0 RO	**STOP_DET:** Same as in reg_IC_INTR_STAT
8	0x0 RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT
7	0x0 RO	**RX_DONE:** Same as in reg_IC_INTR_STAT
6	0x0 RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT
5	0x0 RO	**RD_REQ:** Same as in reg_IC_INTR_STAT
4	0x0 RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT
3	0x0 RO	**TX_OVER:** Same as in reg_IC_INTR_STAT
2	0x0 RO	**RX_FULL:** Same as in reg_IC_INTR_STAT
1	0x0 RO	**RX_OVER:** Same as in reg_IC_INTR_STAT
0	0x0 RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT

9.22.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

I2C Receive FIFO Threshold Register

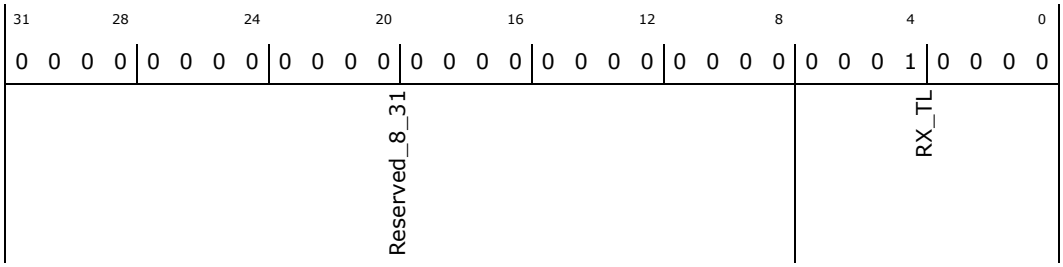
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x10 RW	**RX_TL:** Receive FIFO Threshold Level. The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

9.22.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

I2C Transmit FIFO Threshold Register

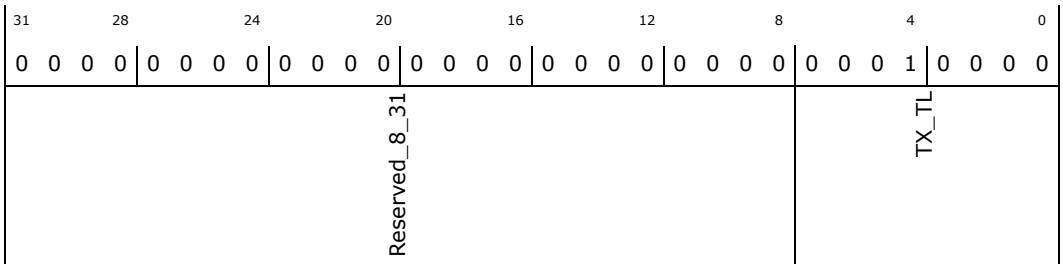
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x10 RW	**TX_TL:** Transmit FIFO Threshold Level. Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

9.22.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

Clear Combined and Individual Interrupt Register

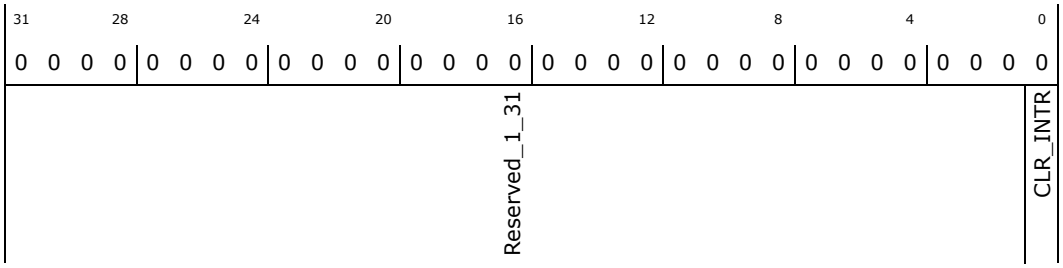
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

9.22.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

Clear RX_UNDER Interrupt Register

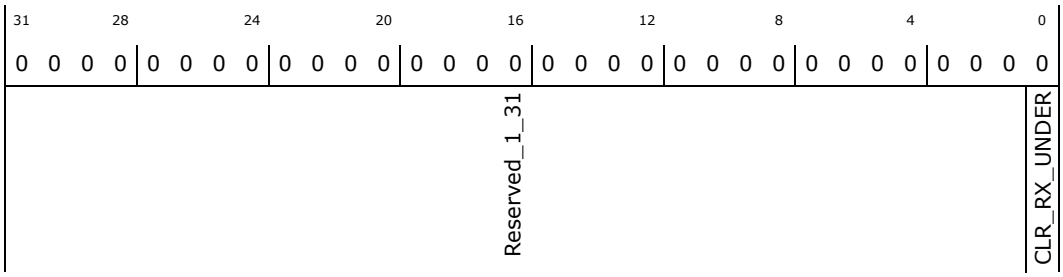
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

9.22.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

Clear RX_OVER Interrupt Register

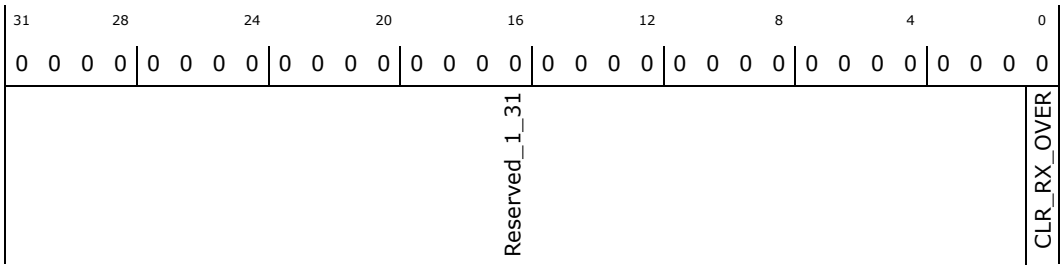
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

9.22.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

Clear TX_OVER Interrupt Register

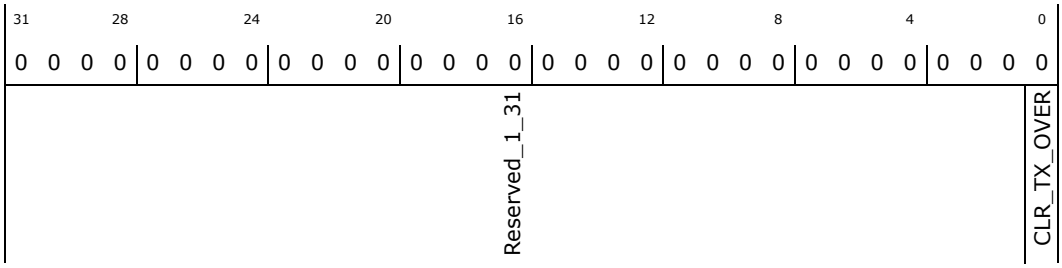
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

9.22.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

Clear RD_REQ Interrupt Register

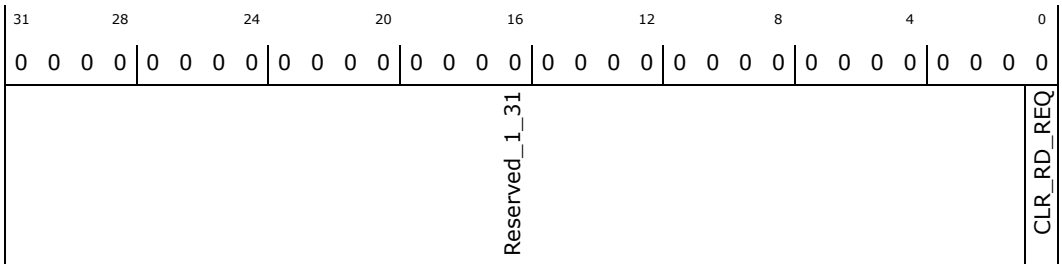
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

9.22.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

Clear TX_ABRT Interrupt Register

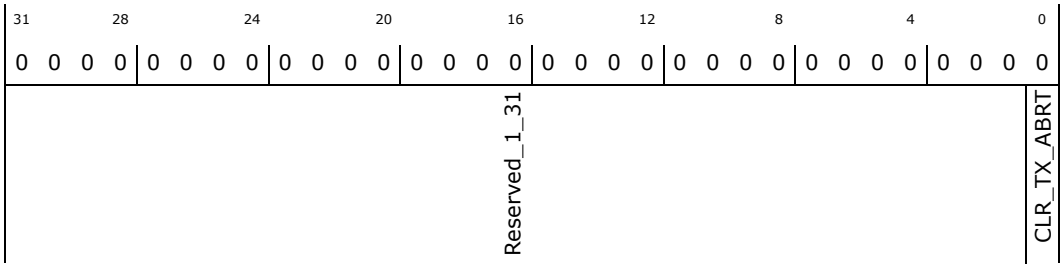
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

9.22.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

Clear RX_DONE Interrupt Register

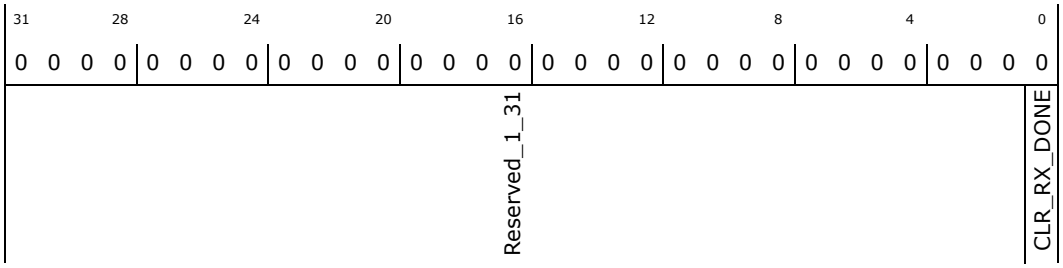
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

9.22.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

Clear ACTIVITY Interrupt Register

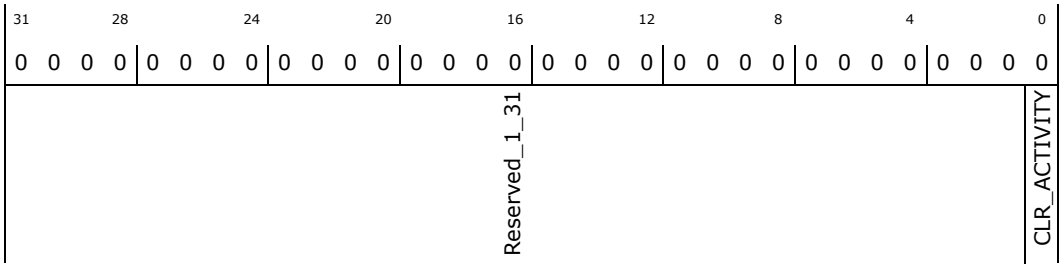
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

9.22.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

Clear STOP_DET Interrupt Register

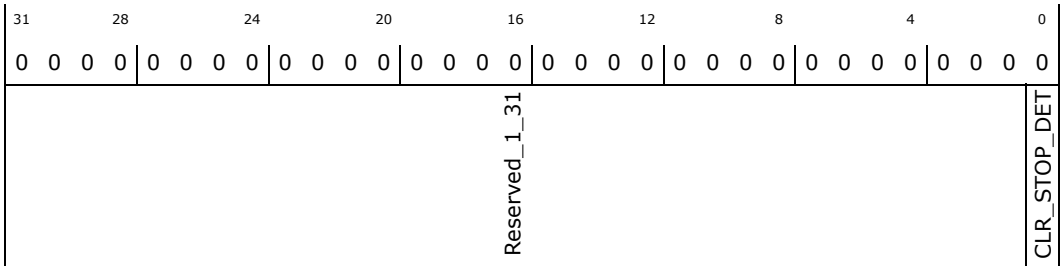
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

9.22.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

Clear START_DET Interrupt Register

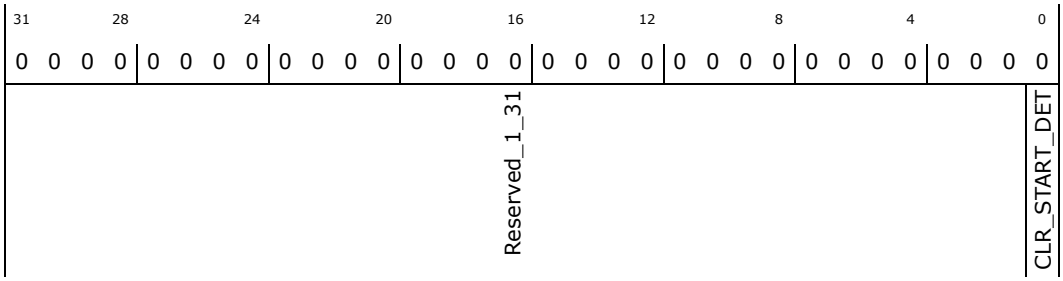
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

9.22.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

Clear GEN_CALL Interrupt Register

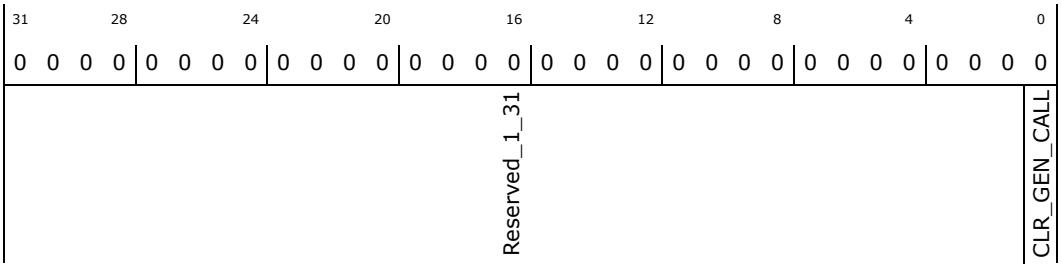
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

9.22.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

I2C Enable Register

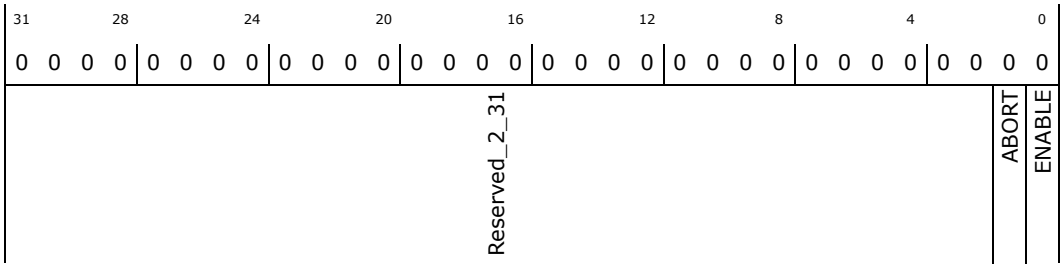
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved_2_31:** Reserved
1	0x0 WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.
0	0x0 RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) 1: Enables DW_apb_i2c

9.22.29 I2C Status Register (IC_STATUS)—Offset 70h

I2C Status Register

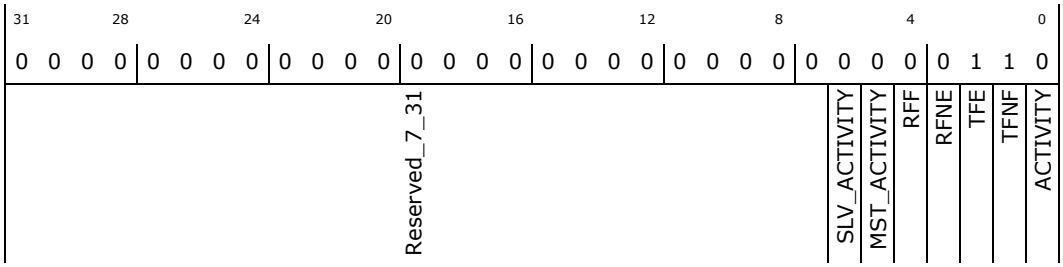
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000006h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RW	**Reserved_7_31:** Reserved
6	0x0 RO	**SLV_ACTIVITY:** Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0x0 RO	**MST_ACTIVITY:** Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RO	**RFF:** Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0x0 RO	**RFNE:** Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.
2	0x1 RO	**TFE:** Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	0x1 RO	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0x0 RO	**ACTIVITY:** I2C Activity Status

9.22.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

I2C Transmit FIFO Level Register

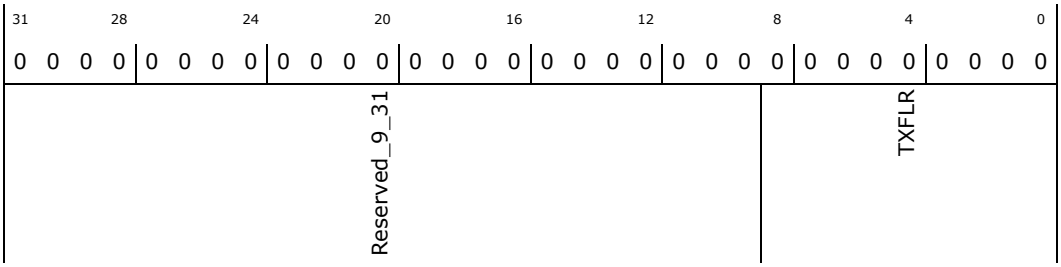
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved_9_31:** Reserved
8:0	0x0 RO	**TXFLR:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

9.22.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

I2C Receive FIFO Level Register

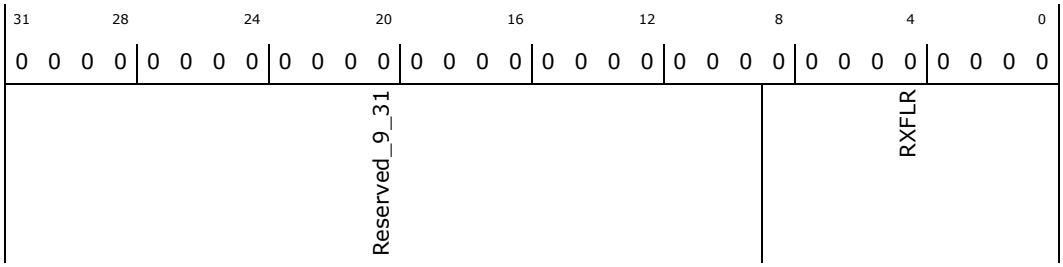
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved_9_31:** Reserved
8:0	0x0 RO	**RXFLR:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

9.22.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

I2C SDA Hold Time Length Register

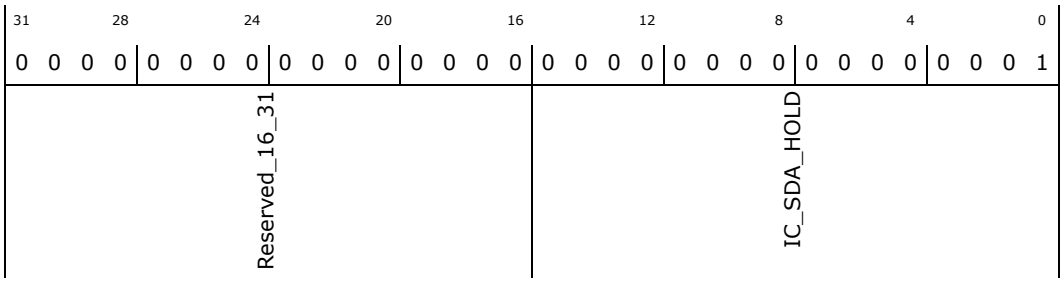
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x1 RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

9.22.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

I2C Transmit Abort Source Register

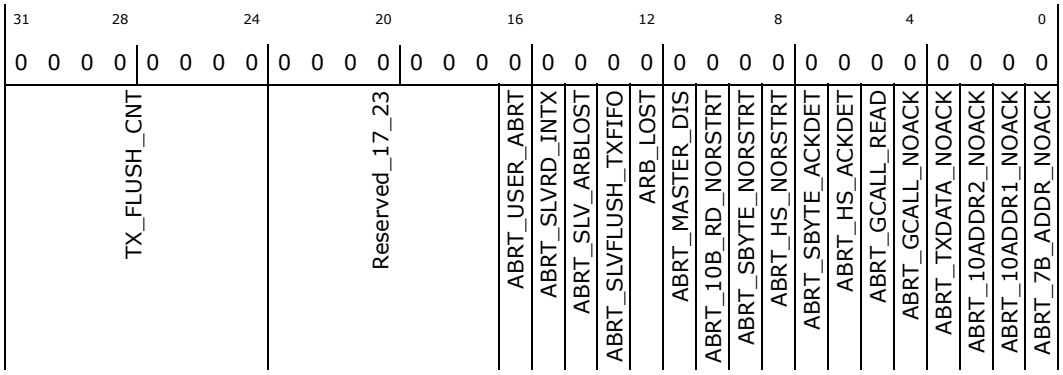
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0x0 RW	**Reserved_17_23:** Reserved
16	0x0 RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0x0 RO	**ABRT_SLVRD_INTX:** 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0x0 RO	**ABRT_SLV_ARBLOST:** 1: Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0x0 RO	**ABRT_SLVFLUSH_TXFIFO:** 1: Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0x0 RO	**ARB_LOST:** 1: Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0x0 RO	**ABRT_MASTER_DIS:** 1: User tries to initiate a Master operation with the Master mode disabled.
10	0x0 RO	**ABRT_10B_RD_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RO	**ABRT_SBYTE_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0x0 RO	**ABRT_HS_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0x0 RO	**ABRT_SBYTE_ACKDET:** 1: Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
6	0x0 RO	**ABRT_HS_ACKDET:** 1: Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
5	0x0 RO	**ABRT_GCALL_READ:** 1: DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0x0 RO	**ABRT_GCALL_NOACK:** 1: DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0x0 RO	**ABRT_TXDATA_NOACK:** 1: This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0x0 RO	**ABRT_10ADDR2_NOACK:** 1: Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0x0 RO	**ABRT_10ADDR1_NOACK:** 1: Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0x0 RO	**ABRT_7B_ADDR_NOACK:** 1: Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

9.22.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

Generate Slave Data NACK Register

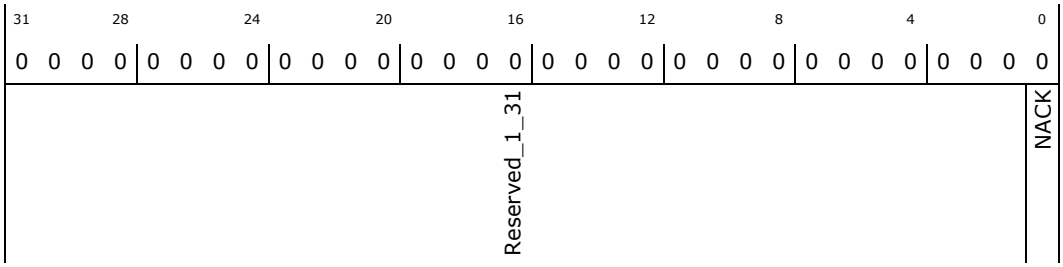
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RW	**NACK:** Generate NACK. This NACK generation only occurs when DW_apb_i2c is a slavereceiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. 1 = generate NACK after data byte received 0 = generate NACK/ACK normally

9.22.35 DMA Control Register (IC_DMA_CR)—Offset 88h

DMA Control Register

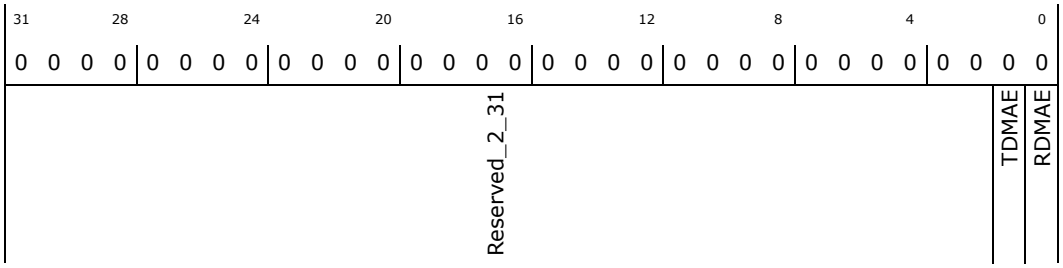
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved_2_31:** Reserved
1	0x0 RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel. 0 = Transmit DMA disabled 1 = Transmit DMA enabled
0	0x0 RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. 0 = Receive DMA disabled 1 = Receive DMA enabled

9.22.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

DMA Transmit Data Level Register

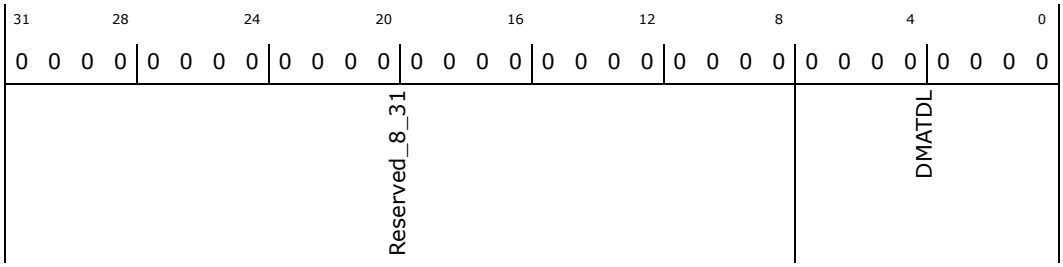
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x0 RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

9.22.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

I2C Receive Data Level Register

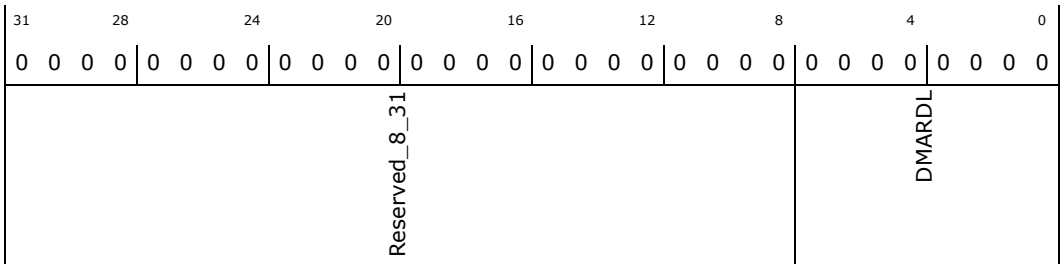
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x0 RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

9.22.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

I2C SDA Setup Register

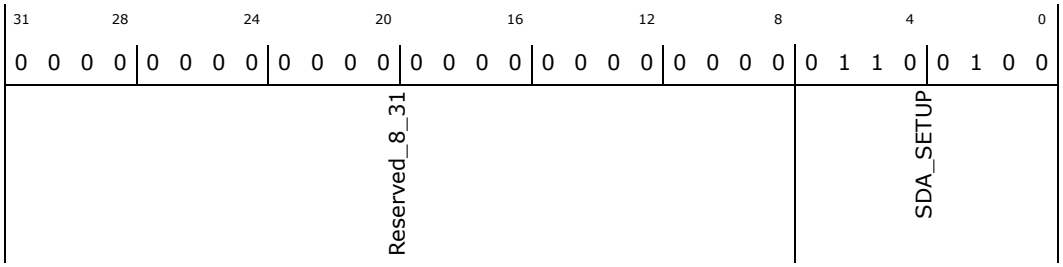
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000064h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x64 RW	**SDA_SETUP:** SDA Setup. It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

9.22.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

I2C ACK General Call Register

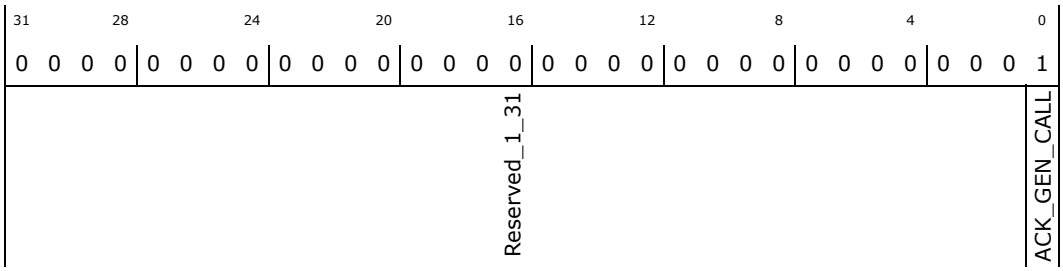
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x1 RW	**ACK_GEN_CALL:** ACK General Call. When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

9.22.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

I2C Enable Status Register

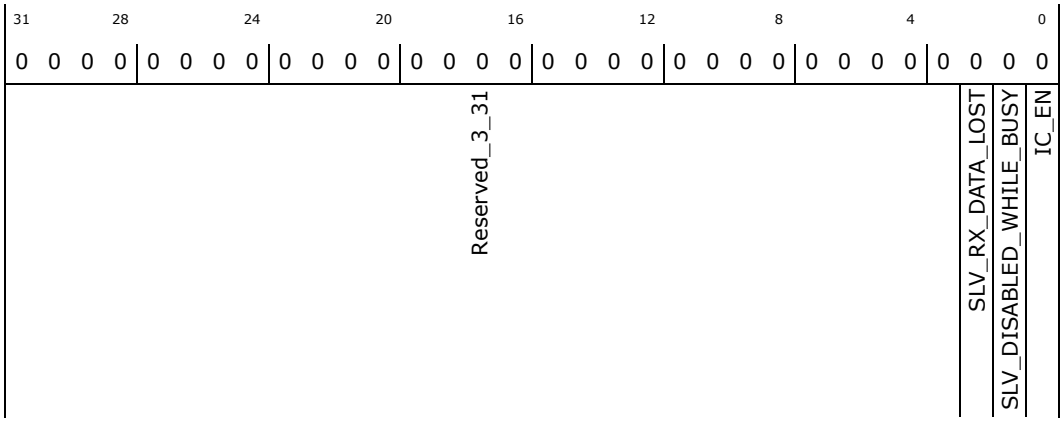
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved_3_31:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0x0 RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0x0 RO	**IC_EN:** ic_en Status. This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

9.22.41 SS/FS Mode Spike Length Register (IC_FS_SPKLEN)—Offset A0h

SS/FS Mode Spike Length Register

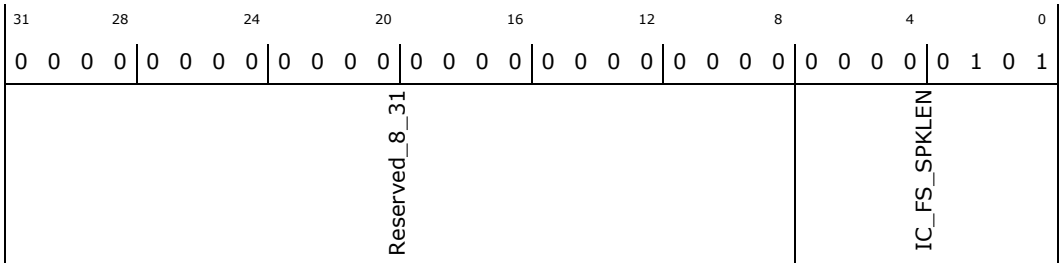
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000005h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x5 RW	**IC_FS_SPKLEN:** Maximum length (in ic_clk cycles) of suppressed spikes in SS and FS modes

9.22.42 HS Mode Spike Length Register (IC_HS_SPKLEN)—Offset A4h

HS Mode Spike Length Register

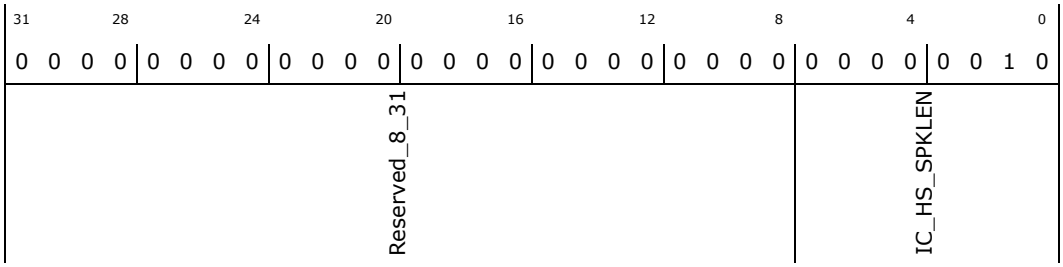
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x2 RW	**IC_HS_SPKLEN:** Maximum length (in ic_clk cycles) of suppressed spikes in HS mode

9.22.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

Component Parameter Register 1

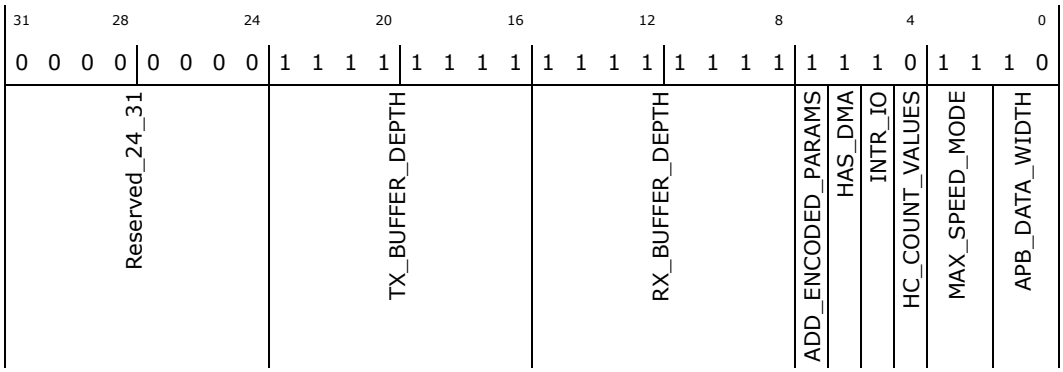
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00FFFFEEh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved_24_31:** Reserved
23:16	0xff RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	0xff RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	0x1 RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	0x1 RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	0x1 RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0x0 RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	0x3 RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	0x2 RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

9.22.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

I2C Component Version Register

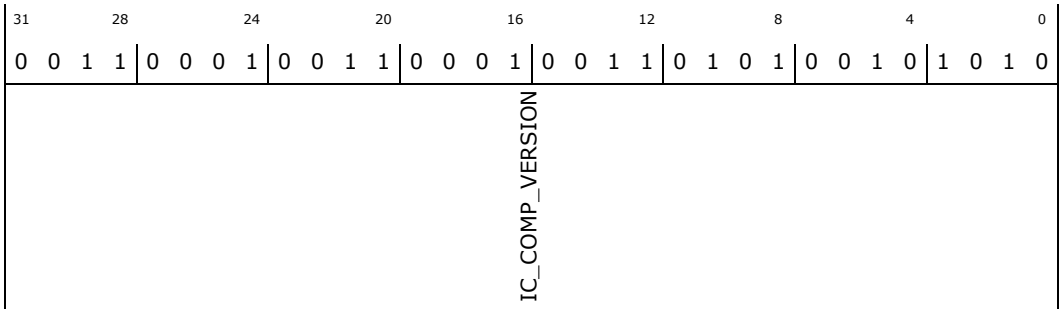
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 3131352Ah



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x3131352a RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes

9.22.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

I2C Component Type Register

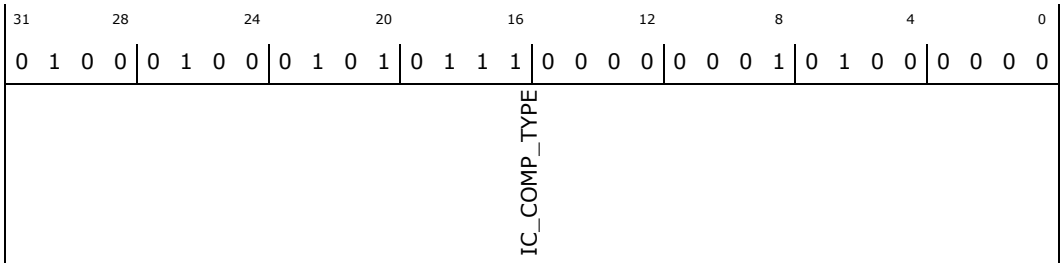
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 44570140h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x44570140 RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

9.22.46 Clock params register (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

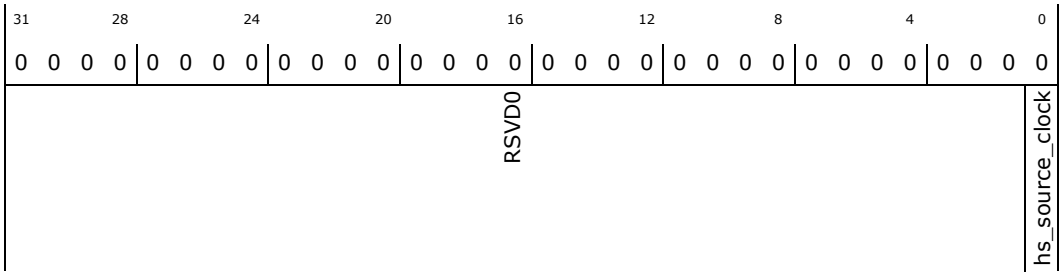
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz 1 -133MHz (high-speed operation compatible)

9.22.47 software reset (RESETS)—Offset 804h

software reset

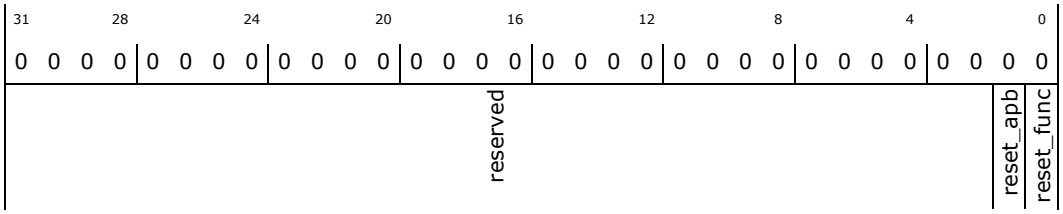
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (reserved):** Reserved
1	0x0 RW	**reset_apb:** reset the apb domain
0	0x0 RW	**reset_func:** reset the func clock domain

9.22.48 General purpose register (GENERAL)—Offset 808h

General purpose register

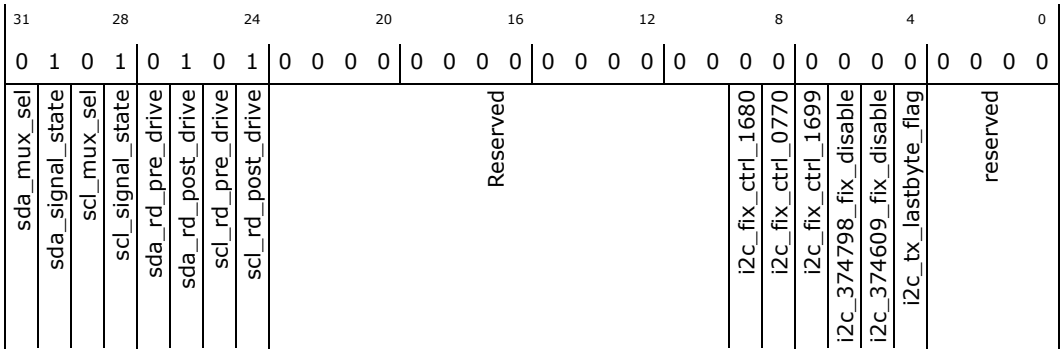
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 55000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**sda_mux_sel:** This bit selects the driver for the SDA signal: 1 = sda_signal_state, 0 = I2C logic
30	0x1 RW	**sda_signal_state:** This bit is used when sda_mux_sel = 1, used to drive the SDA signal on the I2C interface
29	0x0 RW	**scl_mux_sel:** This bit selects the driver for the SCL signal: 1 = scl_signal_state, 0 = I2C logic
28	0x1 RW	**scl_signal_state:** This bit is used when scl_mux_sel = 1, used to drive the SCL signal on the I2C interface
27	0x0 RO	**sda_rd_pre_drive:** Read only bit used to see the status of the SDA signal coming from the I2C logic
26	0x1 RO	**sda_rd_post_drive:** Read only bit used to see the status of the SDA signal coming from the pad
25	0x0 RO	**scl_rd_pre_drive:** Read only bit used to see the status of the SCL signal coming from the I2C logic
24	0x1 RO	**scl_rd_post_drive:** Read only bit used to see the status of the SCL signal coming from the pad
23:10	0x0 RO	**Reserved:** Reserved
9	0x0 RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0x0 RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0x0 RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0x0 RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)
5	0x0 RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0x0 RW	**reserved:** reserved

9.22.49 TX transaction counter (I2C_ACK_COUNT)—Offset 818h

TX transaction counter

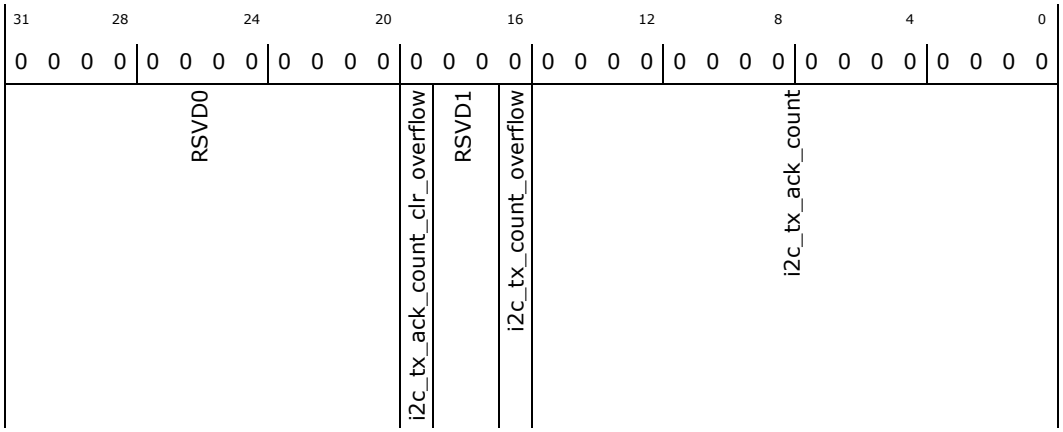
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RSVD0:** Reserved
19	0x0 RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0x0 RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

9.22.50 TX transaction complete interrupt status register (I2C_TX_COMPLETE_INTR_STAT)—Offset 820h

TX transaction has finished interrupt

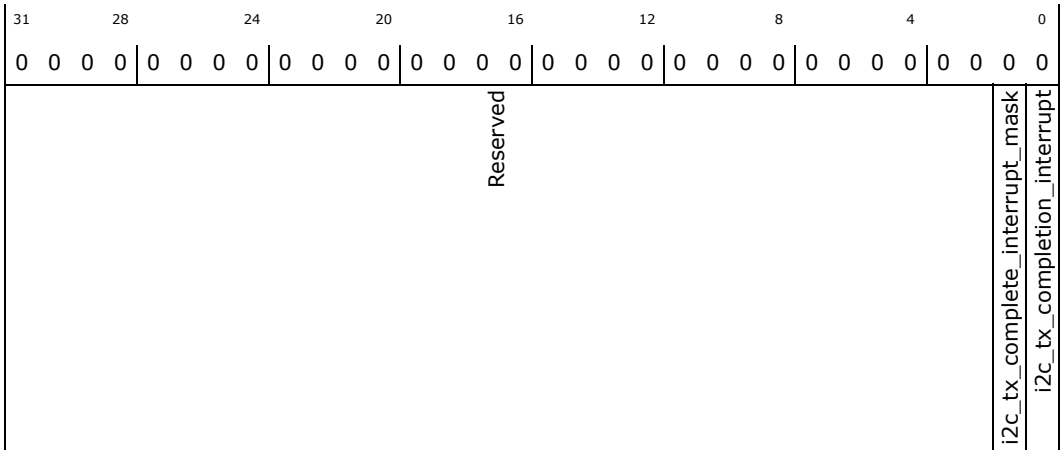
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved:** Reserved
1	0x0 RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0x0 RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

9.22.51 TX transaction complete interrupt clear register (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

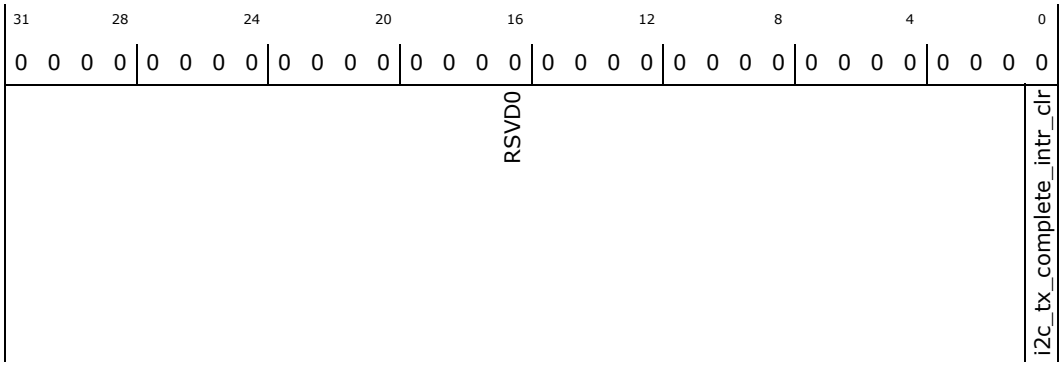
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

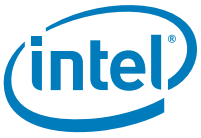
Offset: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:6] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt



9.23 SIO I2C 6 PCI Configuration Registers

Table 86. Summary of SIO I2C 6 PCI Configuration Registers—0/24/7

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4609	00008086h
4–7h	4	"STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h" on page 4609	00100000h
8–Bh	4	"REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4611	00000000h
C–Fh	4	"CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4612	00800000h
10–13h	4	"BAR -Base Address Register (BAR)—Offset 10h" on page 4612	00000000h
14–17h	4	"BAR1 -Base Address Register1 (BAR1)—Offset 14h" on page 4613	00000000h
2C–2Fh	4	"SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4614	00000000h
30–33h	4	"EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4615	00000000h
34–37h	4	"CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4615	00000000h
3C–3Fh	4	"INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4616	00000100h
80–83h	4	"POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4616	00030001h
84–87h	4	"PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4617	00000008h
F8–FBh	4	"Manufacturers ID (MANID)—Offset F8h" on page 4618	00000000h

9.23.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

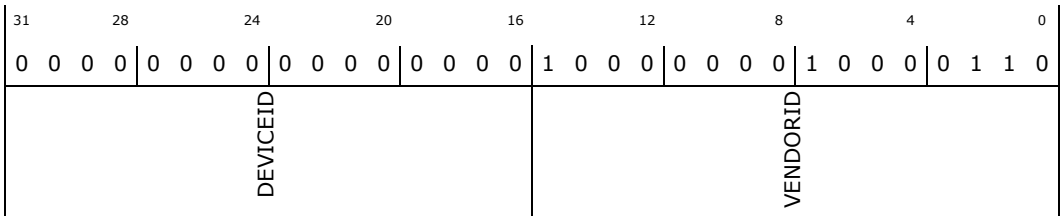
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**DEVICEID:** Device ID identifies the particular AHB/APB device. This is tied to a strap at the top level. Because of tool issues, the HTML files show this field as 0, but the following are the POR values for SoC: LPIO1 DMA: 0x2286 LPIO1 PWM1: 0x2288 LPIO1 PWM2: 0x2289 LPIO1 HSUART1: 0x228A LPIO1 HSUART2: 0x228C LPIO1 SPI1: 0x228E LPIO1 SPI2: 0x2290 LPIO1 SPI3: 0x22AC LPIO2 DMA: 0x22C0 LPIO2 I2C1: 0x22C1 LPIO2 I2C2: 0x22C2 LPIO2 I2C3: 0x22C3 LPIO2 I2C4: 0x22C4 LPIO2 I2C5: 0x22C5 LPIO2 I2C6: 0x22C6 LPIO2 I2C7: 0x22C7 For the final word on this, please see Ray Ng's SoC RevID and DevID HAS on Infofactory: https://ifcollaborate.intel.com/IFC/getdoc.aspx?docbase=InfoFactoryKBandchronid=09005ffd80e84b43andver=CURRENTandqepop=false
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap the top level.

9.23.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

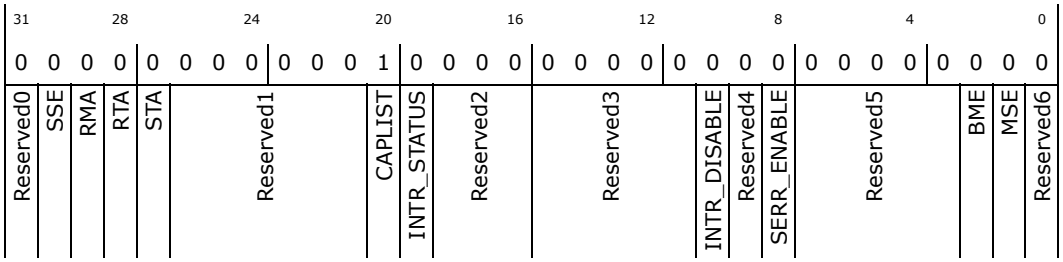
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved0:** Reserved
30	0x0 RW/1C	**SSE:** This bit is set when a device sends an DO_SERR message, and the SERR# Enable bit in the Command register is 1
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric PortReceived Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27	0x0 RW/1C	**STA:** The Bridge sets this bit whenever it responds to a transaction with CA abort. If the SERR# Enable bit is set, the Bridge sets the Signaled System Error bit and sends an DO_SERR message on the IOSF Sideband.
26:21	0x0 RO	**Reserved1:** Reserved
20	0x1 RO	**CAPLIST:** Capabilities List: Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt .i.e Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.. Reset value of this bit is 0.
9	0x0 RO	**Reserved4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: If both SERR# Enable and the Unsupported Request Reporting Enable (URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0x0 RO	**Reserved6:** Reserved

9.23.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

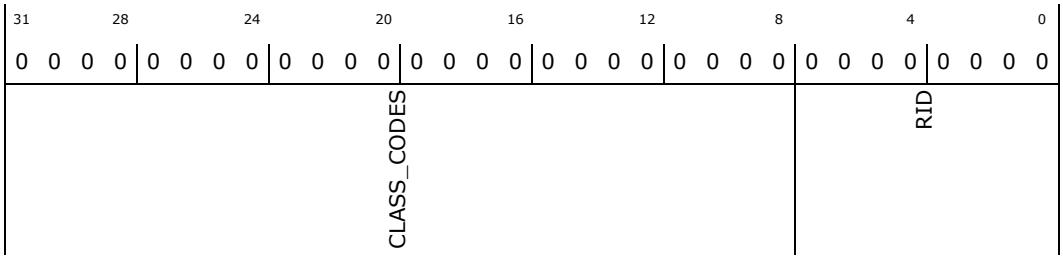
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

9.23.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

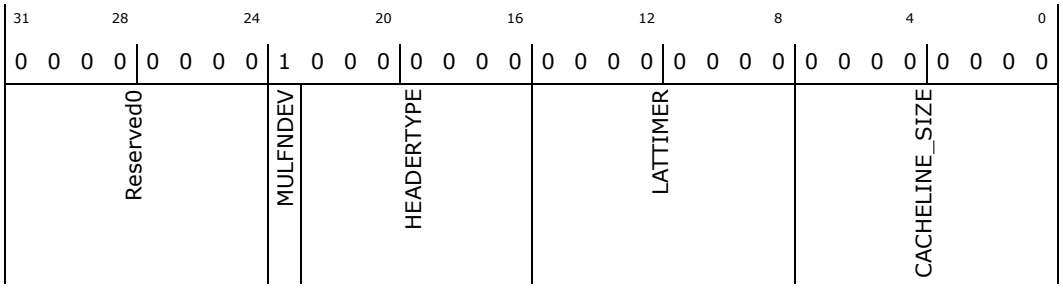
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + Ch

Default: 00800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x1 RO	**MULFNDEV:** Multi Function Device: This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. Value of 1 indicates multifunction device value of 0 indicates single function device
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	0x0 RO	**LATTIMER:** Latency Timer: Doesn.t apply to PCI Express. Hardwired to 00h.
7:0	0x0 RW	**CACHELINE_SIZE:** Cache Line Size: Doesn.t apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

9.23.5 BAR -Base Address Register (BAR)—Offset 10h

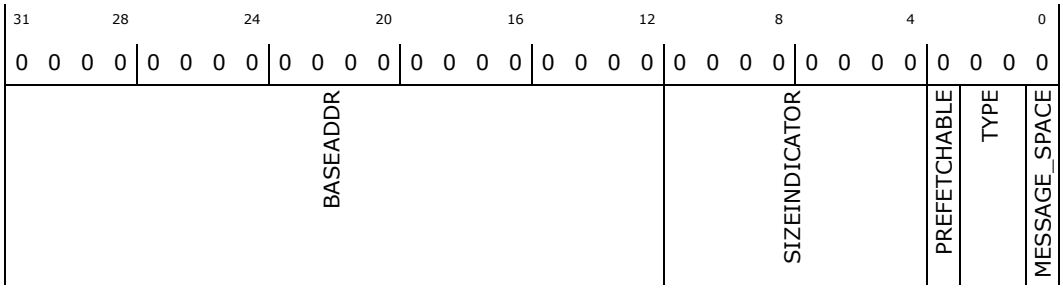
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the AHB device memory space. Taken from Strap values as 1's. Please note that for DMA this field goes from [31:14], or 16kbyte, and the SIZEINDICATOR field goes from [13:4].
11:4	0x0 RO	**SIZEINDICATOR:** Size Indicator Read Only: Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0x0 RO	**TYPE:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.23.6 BAR1 -Base Address Register1 (BAR1)—Offset 14h

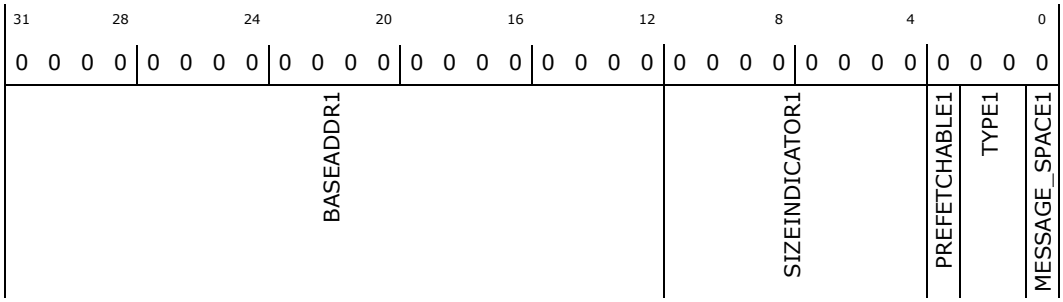
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	0x0 RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not
2:1	0x0 RO	**TYPE1:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.23.7 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

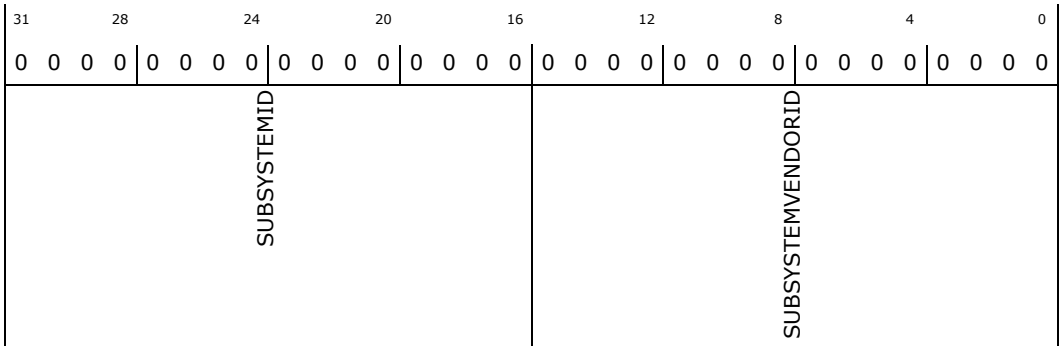
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

9.23.8 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

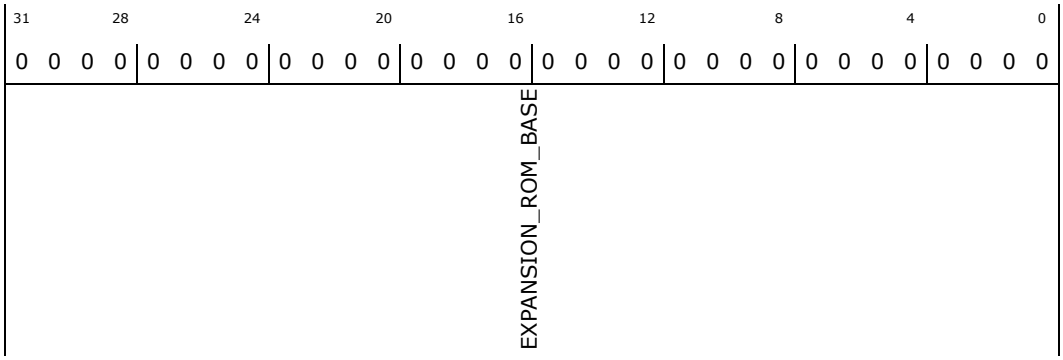
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** A value of all zeros indicates no support for expansion ROM.

9.23.9 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

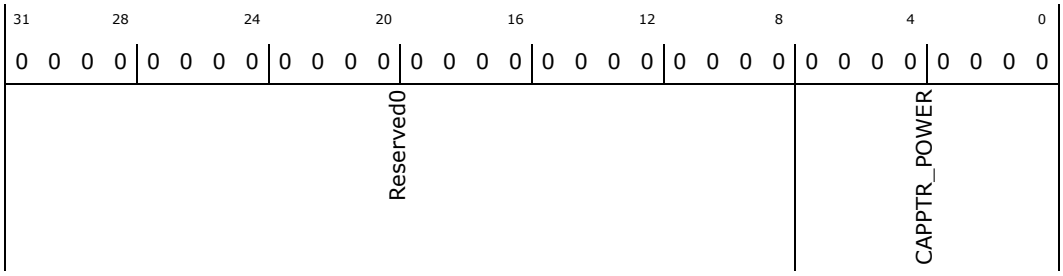
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x0 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

9.23.10 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

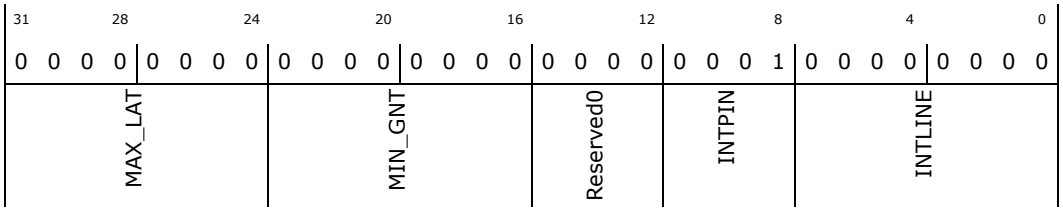
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

9.23.11 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

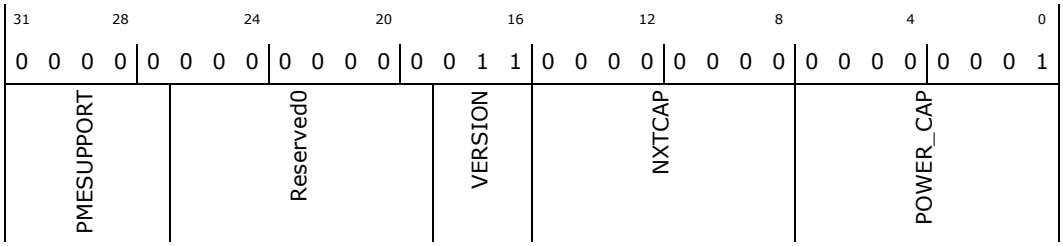
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** PME_Support - This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

9.23.12 PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

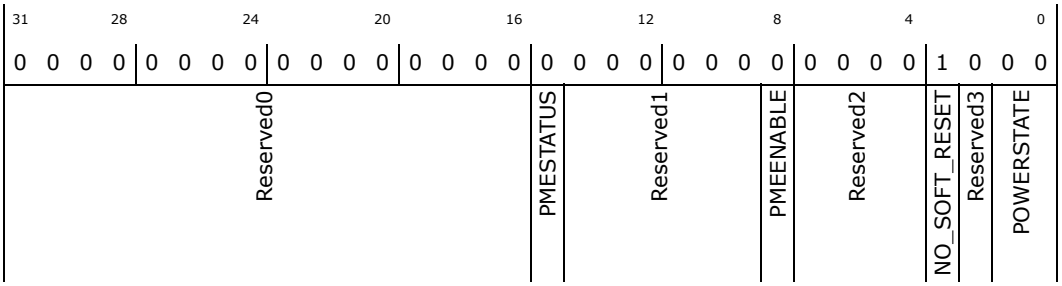
PMECTRLSTATUS - PME Control and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

9.23.13 Manufacturers ID (MANID)—Offset F8h

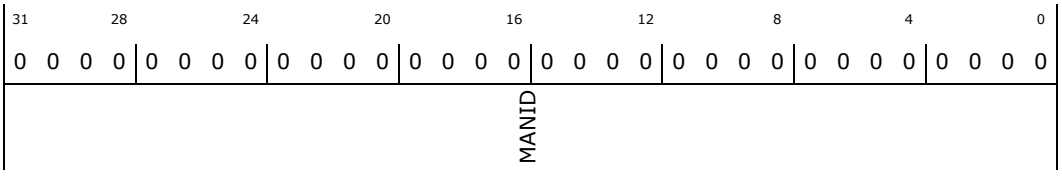
Manufacturers ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:24, F:7] + F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: This register is brought out as straps to the top level.

9.24 SIO I2C 6 Memory Mapped Registers

Table 87. Summary of SIO I2C 6 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"I2C Control Register (IC_CON)—Offset 0h" on page 4623	0000007Fh
4–7h	4	"I2C Target Address Register (IC_TAR)—Offset 4h" on page 4624	00001055h
8–Bh	4	"I2C Slave Address Register (IC_SAR)—Offset 8h" on page 4625	00000055h
C–Fh	4	"I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch" on page 4625	00000001h
10–13h	4	"I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h" on page 4626	00000000h
14–17h	4	"Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h" on page 4627	00000190h
18–1Bh	4	"Standard Speed I2C Clock SCL Low Count Register. (IC_SS_SCL_LCNT)—Offset 18h" on page 4628	000001D6h
1C–1Fh	4	"Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch" on page 4628	0000003Ch
20–23h	4	"Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h" on page 4629	00000082h
24–27h	4	"High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h" on page 4630	0000000Ch
28–2Bh	4	"High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h" on page 4630	00000020h
2C–2Fh	4	"I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch" on page 4631	00000000h
30–33h	4	"I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h" on page 4632	000008FFh
34–37h	4	"I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h" on page 4633	00000000h
38–3Bh	4	"I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h" on page 4634	00000010h
3C–3Fh	4	"I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch" on page 4635	00000010h
40–43h	4	"Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h" on page 4636	00000000h
44–47h	4	"Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h" on page 4636	00000000h
48–4Bh	4	"Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h" on page 4637	00000000h
4C–4Fh	4	"Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch" on page 4638	00000000h
50–53h	4	"Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h" on page 4638	00000000h
54–57h	4	"Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h" on page 4639	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
58–5Bh	4	"Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h" on page 4639	00000000h
5C–5Fh	4	"Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch" on page 4640	00000000h
60–63h	4	"Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h" on page 4641	00000000h
64–67h	4	"Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h" on page 4641	00000000h
68–6Bh	4	"Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h" on page 4642	00000000h
6C–6Fh	4	"I2C Enable Register (IC_ENABLE)—Offset 6Ch" on page 4642	00000000h
70–73h	4	"I2C Status Register (IC_STATUS)—Offset 70h" on page 4643	00000006h
74–77h	4	"I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h" on page 4644	00000000h
78–7Bh	4	"I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h" on page 4644	00000000h
7C–7Fh	4	"I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch" on page 4645	00000001h
80–83h	4	"I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h" on page 4646	00000000h
84–87h	4	"Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h" on page 4647	00000000h
88–8Bh	4	"DMA Control Register (IC_DMA_CR)—Offset 88h" on page 4648	00000000h
8C–8Fh	4	"DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch" on page 4648	00000000h
90–93h	4	"I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h" on page 4649	00000000h
94–97h	4	"I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h" on page 4650	00000064h
98–9Bh	4	"I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h" on page 4650	00000001h
9C–9Fh	4	"I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch" on page 4651	00000000h
A0–A3h	4	"SS/FS Mode Spike Length Register (IC_FS_SPKLEN)—Offset A0h" on page 4652	00000005h
A4–A7h	4	"HS Mode Spike Length Register (IC_HS_SPKLEN)—Offset A4h" on page 4652	00000002h
F4–F7h	4	"Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h" on page 4653	00FFFFEEh
F8–FBh	4	"I2C Component Version Register (IC_COMP_VERSION)—Offset F8h" on page 4654	3131352Ah
FC–FFh	4	"I2C Component Type Register (IC_COMP_TYPE)—Offset FCh" on page 4655	44570140h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
800–803h	4	"Clock params register (CLOCK_PARAMS)—Offset 800h" on page 4655	00000000h
804–807h	4	"software reset (RESETS)—Offset 804h" on page 4656	00000000h
808–80Bh	4	"General purpose register (GENERAL)—Offset 808h" on page 4656	55000000h
818–81Bh	4	"TX transaction counter (I2C_ACK_COUNT)—Offset 818h" on page 4658	00000000h
820–823h	4	"TX transaction complete interrupt status register (I2C_TX_COMPLETE_INTR_STAT)—Offset 820h" on page 4659	00000000h
824–827h	4	"TX transaction complete interrupt clear register (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h" on page 4659	00000000h

9.24.1 I2C Control Register (IC_CON)—Offset 0h

I2C Control Register

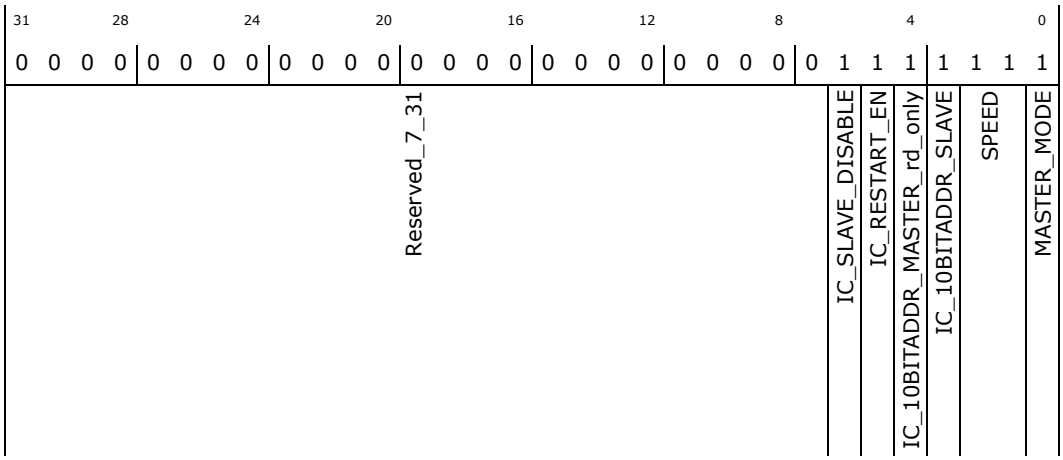
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 0000007Fh



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RW	**Reserved_7_31:** Reserved
6	0x1 RW	**IC_SLAVE_DISABLE:** This bit controls whether I2C has its slave disabled. By default, the slave is always enabled (in reset state as well). If you need to disable it after reset, set this bit to 1. If this bit is set (slave is disabled), DW_apb_i2c functions only as a master and does not perform any action that requires a slave.
5	0x1 RW	**IC_RESTART_EN:** Determines whether RESTART conditions may be sent when acting as a master.When the RESTART is disabled, the DW_apb_i2c master is incapable of performing the following functions: Sending a START BYTE. Performing any high-speed mode operation. Performing direction changes in combined format mode. Performing a read operation with a 10-bit address
4	0x1 RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** controls whether the DW_apb_i2c starts its transfers in 7- or 10-bit addressing mode when acting as a master. If I2C_DYNAMIC_TAR_UPDATE = 1, then this bit is read-only copy of bit 12 of IC_TAR register
3	0x1 RW	**IC_10BITADDR_SLAVE:** When acting as a slave, this bit controls whether the DW_apb_i2c responds to 7- or 10-bit addresses.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0x3 RW	**SPEED:** These bits control at which speed the DW_apb_i2c operates; its setting is relevant only if one is operating the DW_apb_i2c in master mode. Hardware protects against illegal values being programmed by software. This register should be programmed only with a value in the range of 1 to IC_MAX_SPEED_MODE; otherwise, hardware updates this register with the value of IC_MAX_SPEED_MODE.
0	0x1 RW	**MASTER_MODE:** This bit controls whether the DW_apb_i2c master is enabled. Software should ensure that if this bit is set to X, then bit 6 should also be set to X.

9.24.2 I2C Target Address Register (IC_TAR)—Offset 4h

I2C Target Address Register

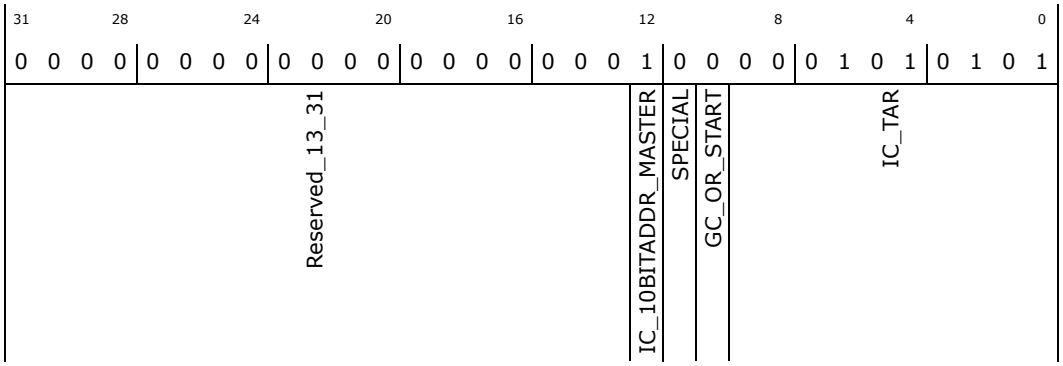
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00001055h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Reserved_13_31:** Reserved
12	0x1 RW	**IC_10BITADDR_MASTER:** This bit controls whether the DW_apb_i2c starts its transfers in 7-or 10-bit addressing mode when acting as a master. This bit exists in this register only if the I2C_DYNAMIC_TAR_UPDATE configuration parameter is set to 1
11	0x0 RW	**SPECIAL:** This bit indicates whether software performs a General Call or START BYTE command. 0: ignore bit 10 GC_OR_START and use IC_TAR normally. 1: perform special I2C command as specified in GC_OR_START bit
10	0x0 RW	**GC_OR_START:** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call(0) or START(1) byte command is to be performed by the DW_apb_i2c.

Bit Range	Default & Access	Field Name (ID): Description
9:0	0x55 RW	**IC_TAR:** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

9.24.3 I2C Slave Address Register (IC_SAR)—Offset 8h

I2C Slave Address Register

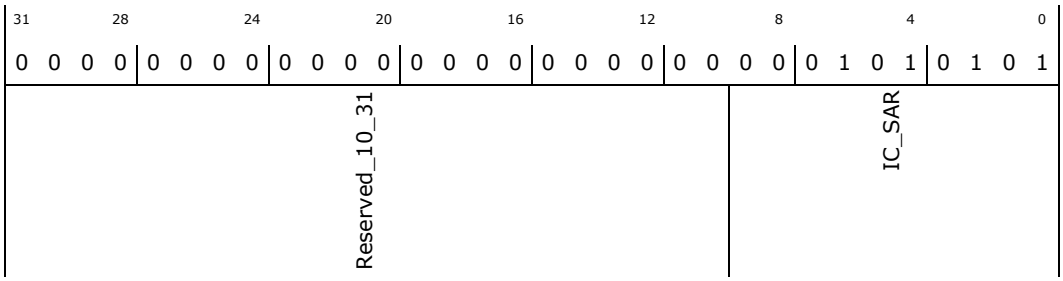
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000055h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**Reserved_10_31:** Reserved
9:0	0x55 RW	**IC_SAR:** The IC_SAR holds the slave address when the I2C is operating as a slave. For 7-bit addressing, only IC_SAR[6:0] is used. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.24.4 I2C High Speed Master Mode Code Address Register (IC_HS_MADDR)—Offset Ch

I2C High Speed Master Mode Code Address Register

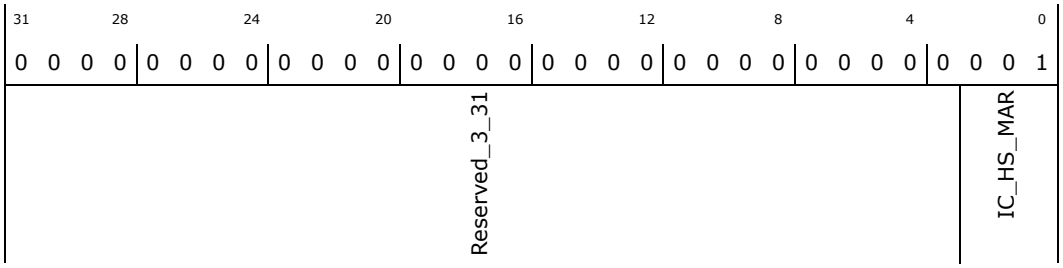
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved_3_31:** Reserved
2:0	0x1 RW	**IC_HS_MAR:** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2). This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.24.5 I2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD)—Offset 10h

I2C Rx/Tx Data Buffer and Command Register; this is the register the CPU writes to when filling the TX FIFO and the CPU reads from when retrieving bytes from RX FIFO

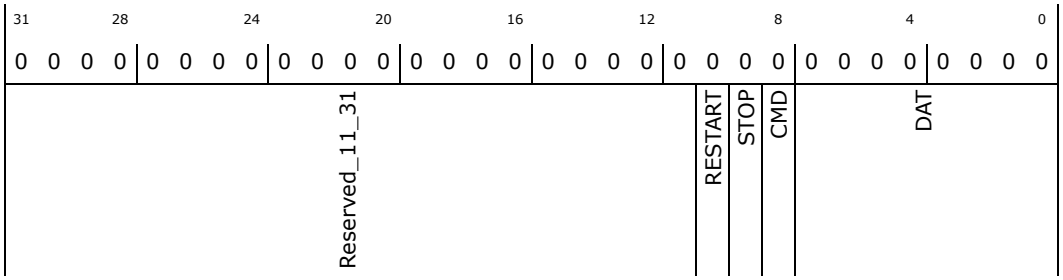
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:11	0x0 RW	**Reserved_11_31:** Reserved
10	0x0 RW	**RESTART:** RESTART
9	0x0 RW	**STOP:** STOP
8	0x0 RW	**CMD:** This bit controls whether a read or a write is performed. This bit does not control the direction when the DW_apb_i2c acts as a slave. It controls only the direction when it acts as a master. 1 = Read. 0 = Write
7:0	0x0 RW	**DAT:** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the DW_apb_i2c. However, when you read this register, these bits return the value of data received on the DW_apb_i2c interface.

9.24.6 Standard Speed I2C Clock SCL High Count Register (IC_SS_SCL_HCNT)—Offset 14h

Standard Speed I2C Clock SCL High Count Register.

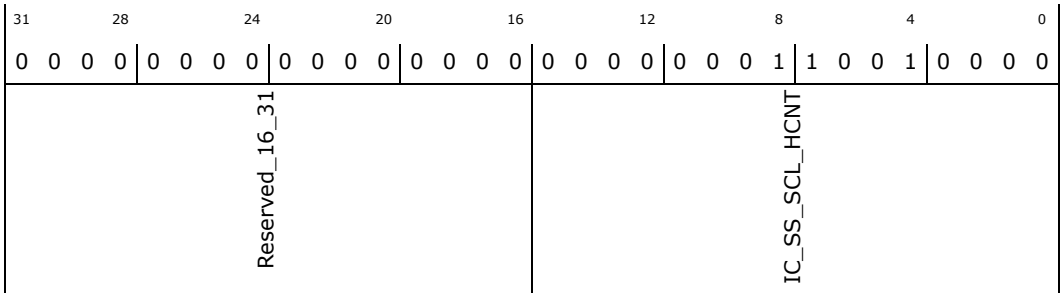
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000190h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x190 RW	**IC_SS_SCL_HCNT:** Standard Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.24.7 Standard Speed I2C Clock SCL Low Count Register. (IC_SS_SCL_LCNT)—Offset 18h

Standard Speed I2C Clock SCL Low Count Register.

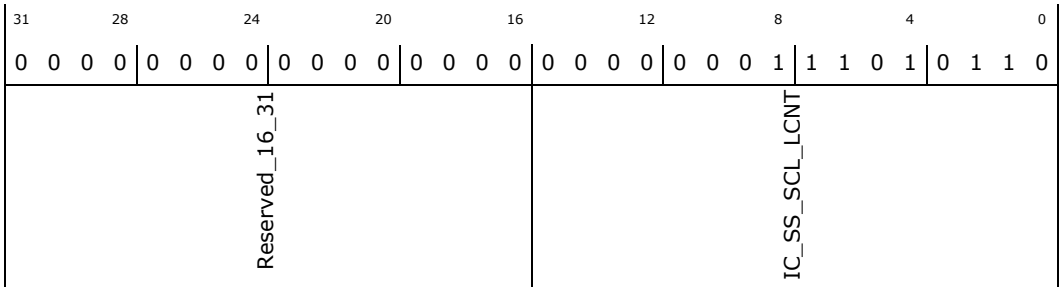
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 000001D6h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x1d6 RW	**IC_SS_SCL_LCNT:** Standard Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.24.8 Fast Speed I2C Clock SCL High Count Register (IC_FS_SCL_HCNT)—Offset 1Ch

Fast Speed I2C Clock SCL High Count Register

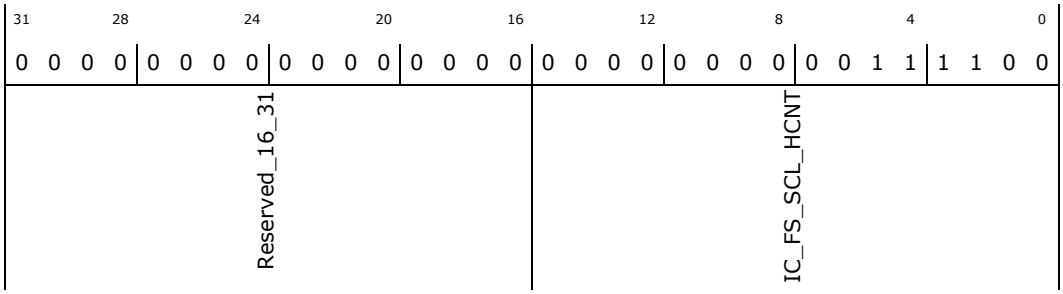
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 0000003Ch



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x3c RW	**IC_FS_SCL_HCNT:** Fast Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.24.9 Fast Speed I2C Clock SCL Low Count Register (IC_FS_SCL_LCNT)—Offset 20h

Fast Speed I2C Clock SCL Low Count Register

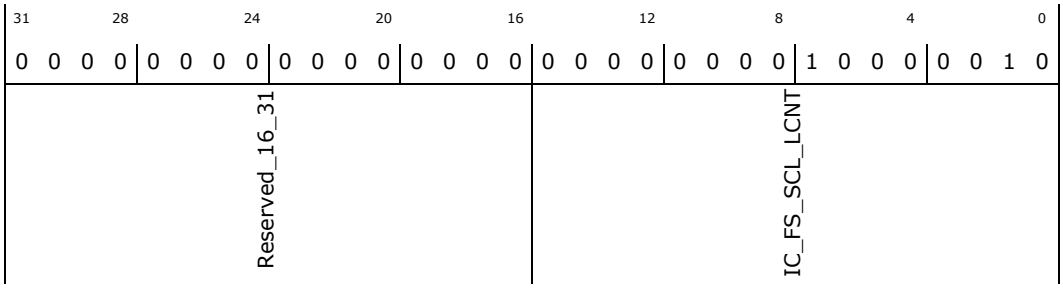
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 20h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000082h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x82 RW	**IC_FS_SCL_LCNT:** Fast Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.24.10 High Speed I2C Clock SCL High Count Register (IC_HS_SCL_HCNT)—Offset 24h

High Speed I2C Clock SCL High Count Register

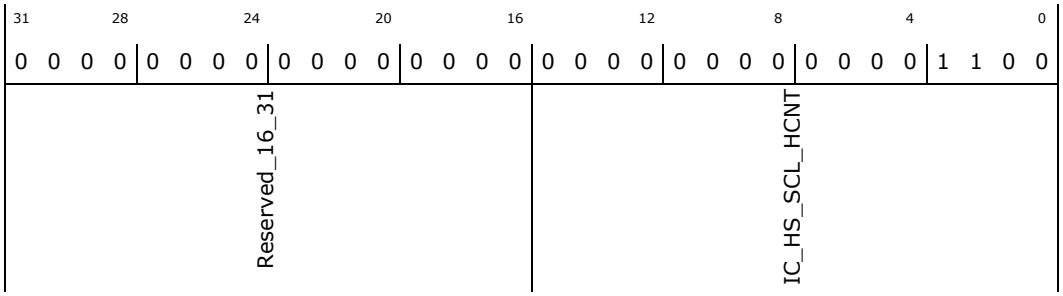
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 24h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 0000000Ch



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0xc RW	**IC_HS_SCL_HCNT:** High Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.24.11 High Speed I2C Clock SCL Low Count Register (IC_HS_SCL_LCNT)—Offset 28h

High Speed I2C Clock SCL Low Count Register

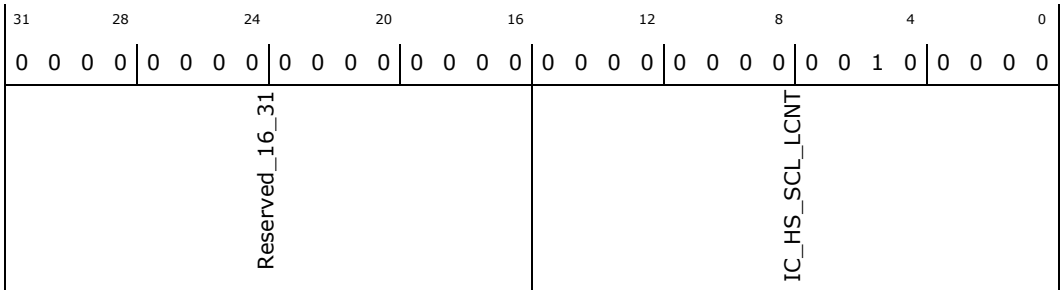
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 28h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000020h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x20 RW	**IC_HS_SCL_LCNT:** High Speed I2C Clock SCL Low Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

9.24.12 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

I2C Interrupt Status Register

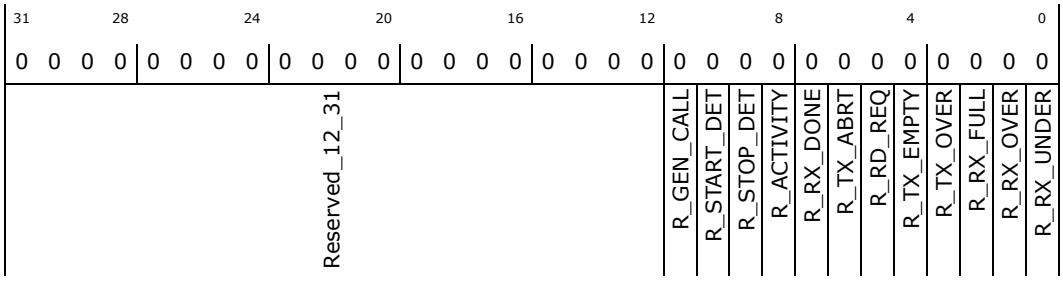
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 2Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x0 RO	**R_GEN_CALL:** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling DW_apb_i2c or when the CPU reads bit 0 of the IC_CLR_GEN_CALL register.

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RO	**R_START_DET:** Indicates whether a START or RESTART condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
9	0x0 RO	**R_STOP_DET:** Indicates whether a STOP condition has occurred on the I2C interface regardless of whether DW_apb_i2c is operating in slave or master mode.
8	0x0 RO	**R_ACTIVITY:** This bit captures DW_apb_i2c activity and stays set until it is cleared. There are four ways to clear it: Disabling the DW_apb_i2c, Reading the IC_CLR_ACTIVITY register, Reading the IC_CLR_INTR register, System reset
7	0x0 RO	**R_RX_DONE:** When the DW_apb_i2c is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.
6	0x0 RO	**R_TX_ABRT:** This bit indicates if DW_apb_i2c, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	0x0 RO	**R_RD_REQ:** This bit is set to 1 when DW_apb_i2c is acting as a slave and another I2C master is attempting to read data from DW_apb_i2c.
4	0x0 RO	**R_TX_EMPTY:** This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register.
3	0x0 RO	**R_TX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0x0 RO	**R_RX_FULL:** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register.
1	0x0 RO	**R_RX_OVER:** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
0	0x0 RO	**R_RX_UNDER:** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

9.24.13 I2C Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

I2C Interrupt Mask Register

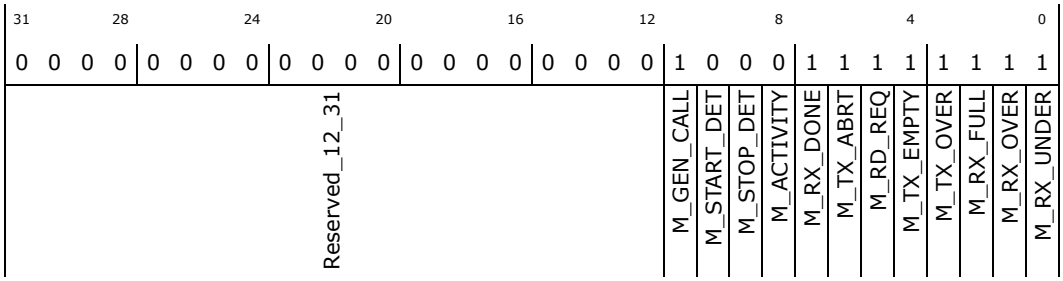
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 000008FFh



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x1 RW	**M_GEN_CALL:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
10	0x0 RW	**M_START_DET:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
9	0x0 RW	**M_STOP_DET:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
8	0x0 RW	**M_ACTIVITY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
7	0x1 RW	**M_RX_DONE:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
6	0x1 RW	**M_TX_ABRT:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
5	0x1 RW	**M_RD_REQ:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
4	0x1 RW	**M_TX_EMPTY:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
3	0x1 RW	**M_TX_OVER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
2	0x1 RW	**M_RX_FULL:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
1	0x1 RW	**M_RX_OVER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.
0	0x1 RW	**M_RX_UNDER:** These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register.

9.24.14 I2C Raw Interrupt Status Register (IC_RAW_INTR_STAT)—Offset 34h

I2C Raw Interrupt Status Register

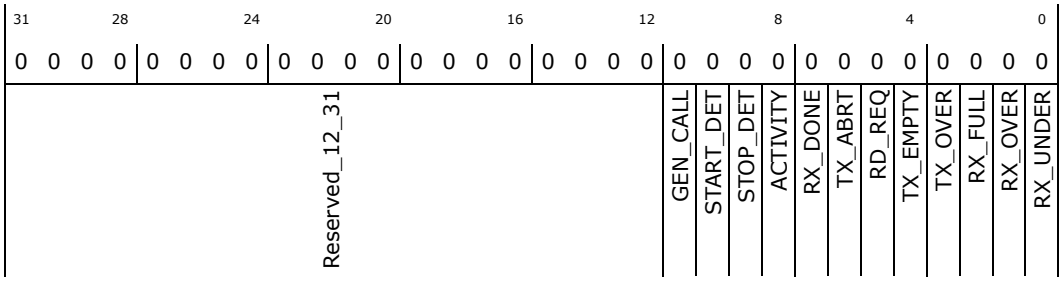
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**Reserved_12_31:** Reserved
11	0x0 RO	**GEN_CALL:** Same as in reg_IC_INTR_STAT
10	0x0 RO	**START_DET:** Same as in reg_IC_INTR_STAT
9	0x0 RO	**STOP_DET:** Same as in reg_IC_INTR_STAT
8	0x0 RO	**ACTIVITY:** Same as in reg_IC_INTR_STAT
7	0x0 RO	**RX_DONE:** Same as in reg_IC_INTR_STAT
6	0x0 RO	**TX_ABRT:** Same as in reg_IC_INTR_STAT
5	0x0 RO	**RD_REQ:** Same as in reg_IC_INTR_STAT
4	0x0 RO	**TX_EMPTY:** Same as in reg_IC_INTR_STAT
3	0x0 RO	**TX_OVER:** Same as in reg_IC_INTR_STAT
2	0x0 RO	**RX_FULL:** Same as in reg_IC_INTR_STAT
1	0x0 RO	**RX_OVER:** Same as in reg_IC_INTR_STAT
0	0x0 RO	**RX_UNDER:** Same as in reg_IC_INTR_STAT

9.24.15 I2C Receive FIFO Threshold Register (IC_RX_TL)—Offset 38h

I2C Receive FIFO Threshold Register

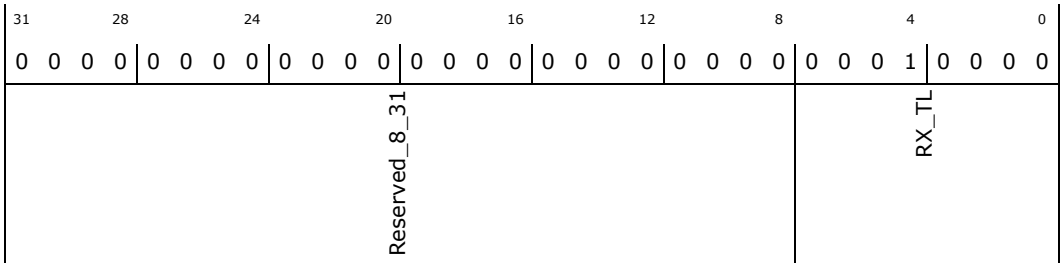
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x10 RW	**RX_TL:** Receive FIFO Threshold Level. The valid range is 0-255, with the additional restriction that hardware does not allow this value to be set to a value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

9.24.16 I2C Transmit FIFO Threshold Register (IC_TX_TL)—Offset 3Ch

I2C Transmit FIFO Threshold Register

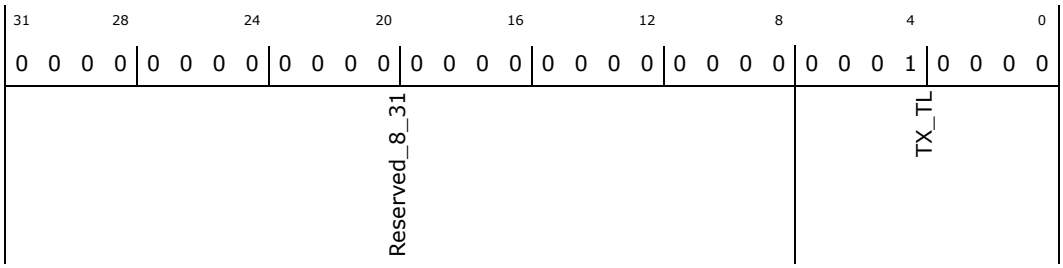
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x10 RW	**TX_TL:** Transmit FIFO Threshold Level. Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer.

9.24.17 Clear Combined and Individual Interrupt Register (IC_CLR_INTR)—Offset 40h

Clear Combined and Individual Interrupt Register

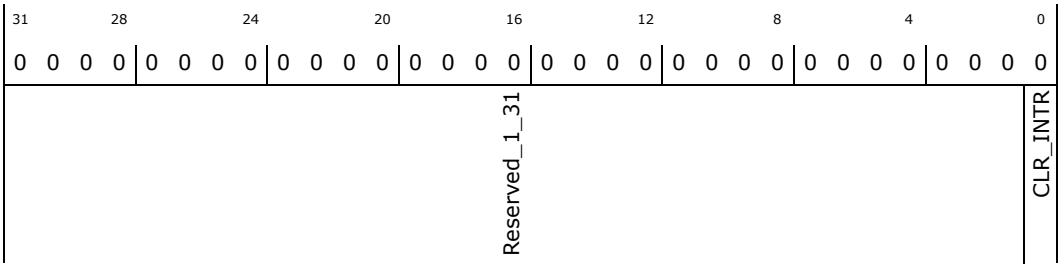
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_INTR:** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts.

9.24.18 Clear RX_UNDER Interrupt Register (IC_CLR_RX_UNDER)—Offset 44h

Clear RX_UNDER Interrupt Register

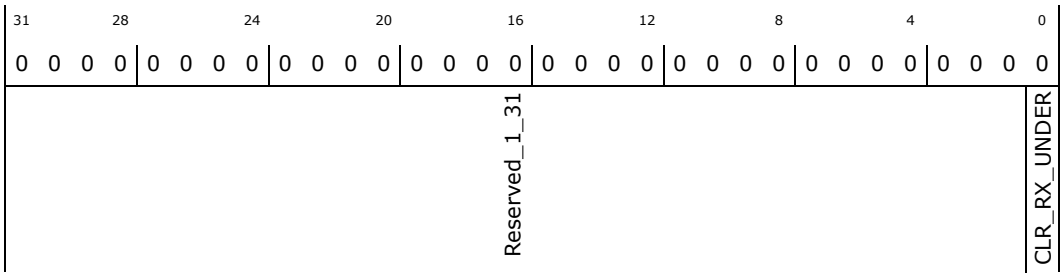
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_UNDER:** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

9.24.19 Clear RX_OVER Interrupt Register (IC_CLR_RX_OVER)—Offset 48h

Clear RX_OVER Interrupt Register

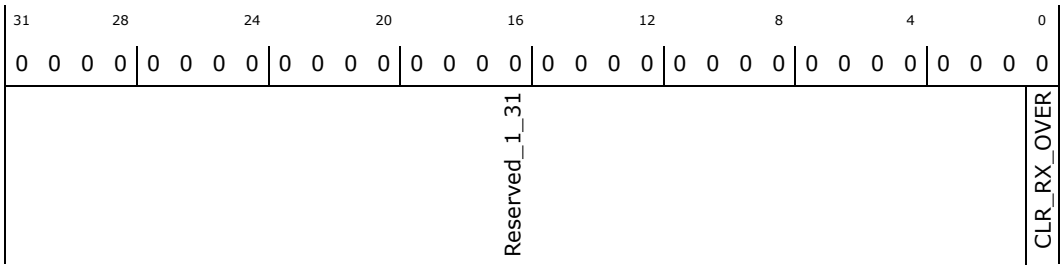
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_OVER:** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

9.24.20 Clear TX_OVER Interrupt Register (IC_CLR_TX_OVER)—Offset 4Ch

Clear TX_OVER Interrupt Register

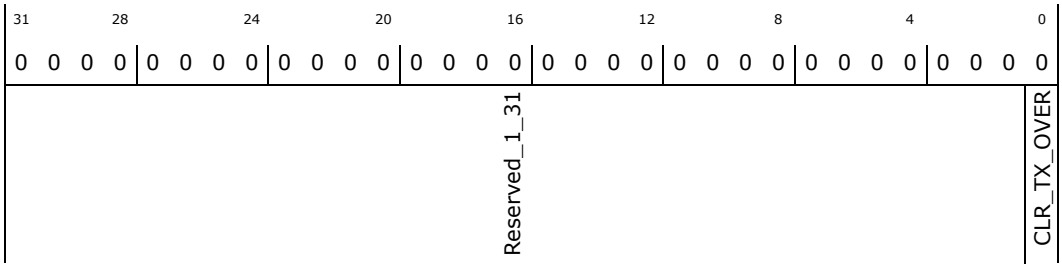
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_TX_OVER:** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

9.24.21 Clear RD_REQ Interrupt Register (IC_CLR_RD_REQ)—Offset 50h

Clear RD_REQ Interrupt Register

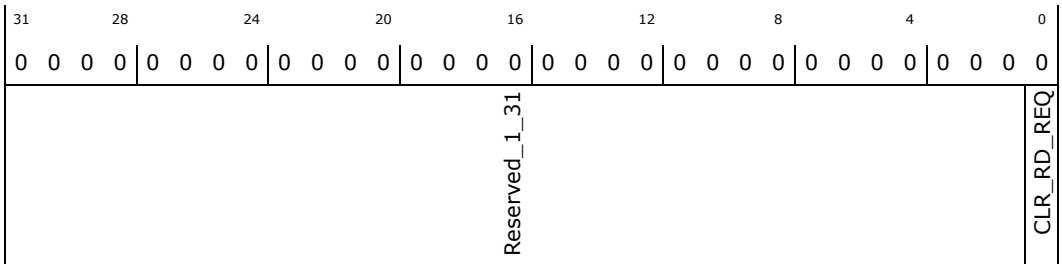
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RD_REQ:** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

9.24.22 Clear TX_ABRT Interrupt Register (IC_CLR_TX_ABRT)—Offset 54h

Clear TX_ABRT Interrupt Register

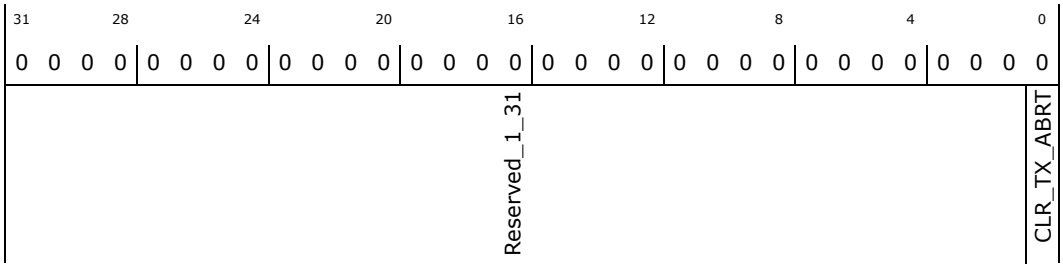
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_TX_ABRT:** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.

9.24.23 Clear RX_DONE Interrupt Register (IC_CLR_RX_DONE)—Offset 58h

Clear RX_DONE Interrupt Register

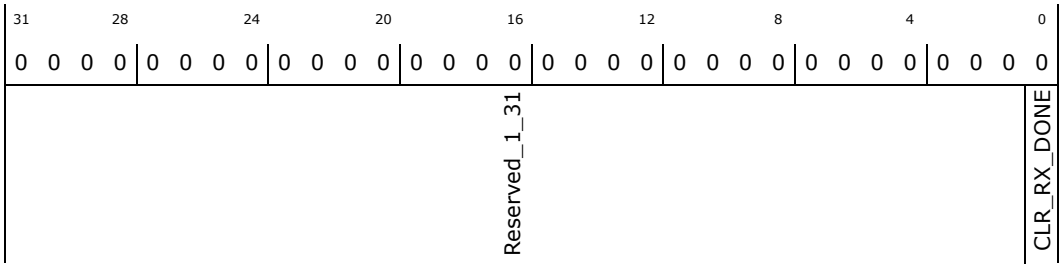
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_RX_DONE:** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

9.24.24 Clear ACTIVITY Interrupt Register (IC_CLR_ACTIVITY)—Offset 5Ch

Clear ACTIVITY Interrupt Register

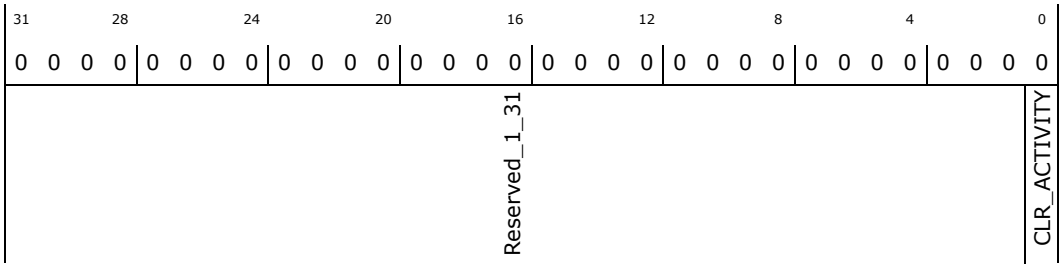
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_ACTIVITY:** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

9.24.25 Clear STOP_DET Interrupt Register (IC_CLR_STOP_DET)—Offset 60h

Clear STOP_DET Interrupt Register

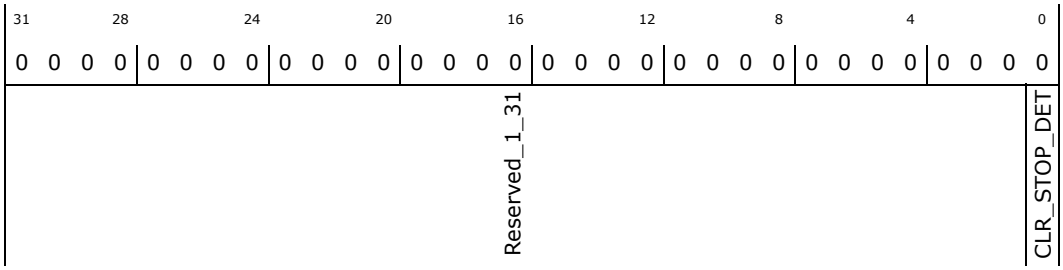
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_STOP_DET:** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

9.24.26 Clear START_DET Interrupt Register (IC_CLR_START_DET)—Offset 64h

Clear START_DET Interrupt Register

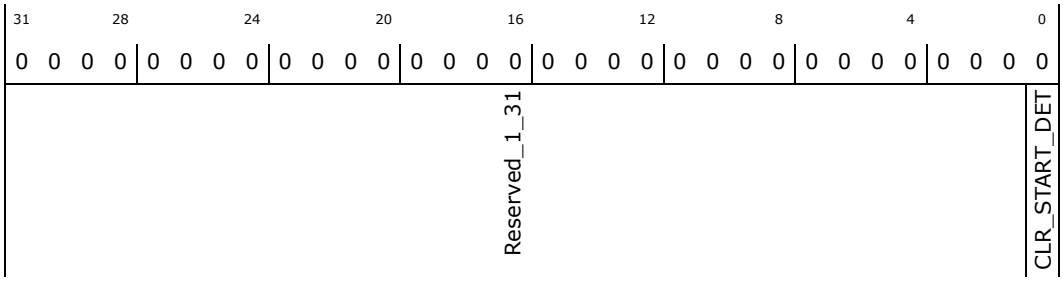
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_START_DET:** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

9.24.27 Clear GEN_CALL Interrupt Register (IC_CLR_GEN_CALL)—Offset 68h

Clear GEN_CALL Interrupt Register

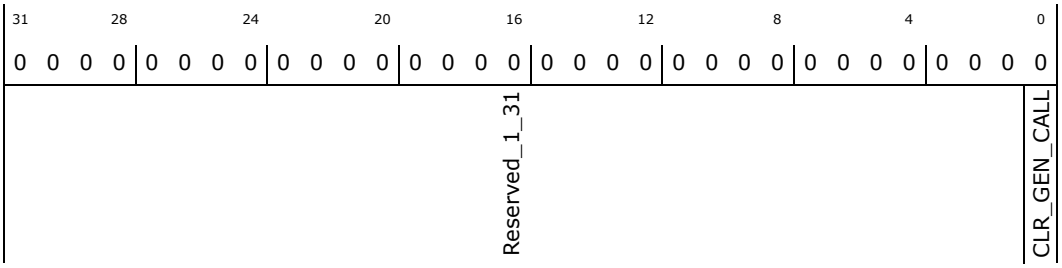
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RO	**CLR_GEN_CALL:** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

9.24.28 I2C Enable Register (IC_ENABLE)—Offset 6Ch

I2C Enable Register

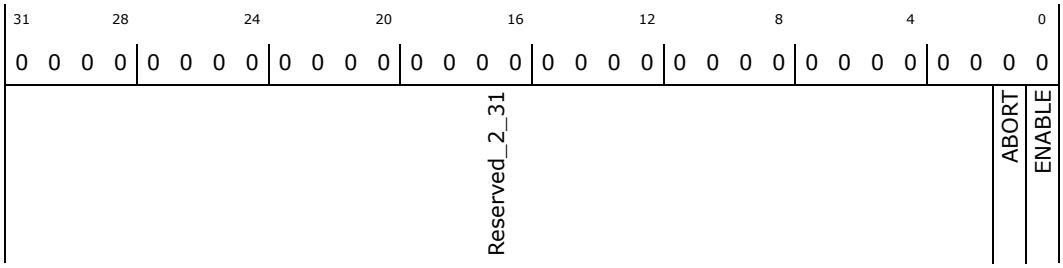
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved_2_31:** Reserved
1	0x0 WO	**ABORT:** Software can abort the I2C transfer by setting this bit. This bit can be set only when ENABLE =1 and fix_ctrl_1680 = 1. The HW will clear the ABORT bit once the STOP condition has been sent.
0	0x0 RW	**ENABLE:** Controls whether the DW_apb_i2c is enabled. 0: Disables DW_apb_i2c (TX and RX FIFOs are held in an erased state) 1: Enables DW_apb_i2c

9.24.29 I2C Status Register (IC_STATUS)—Offset 70h

I2C Status Register

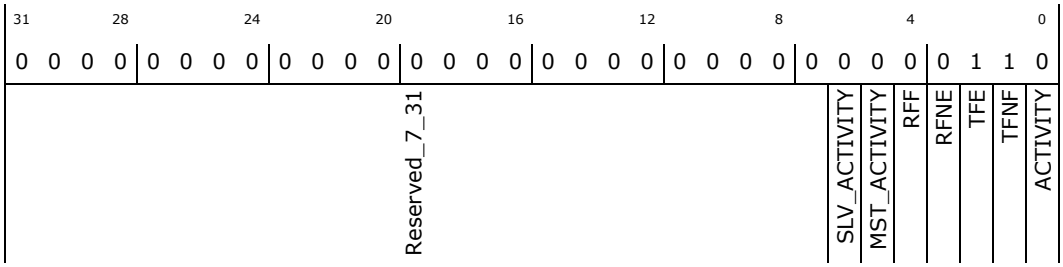
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000006h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RW	**Reserved_7_31:** Reserved
6	0x0 RO	**SLV_ACTIVITY:** Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set.
5	0x0 RO	**MST_ACTIVITY:** Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set.

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RO	**RFF:** Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.
3	0x0 RO	**RFNE:** Receive FIFO Not Empty. This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty.
2	0x1 RO	**TFE:** Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.
1	0x1 RO	**TFNF:** Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	0x0 RO	**ACTIVITY:** I2C Activity Status

9.24.30 I2C Transmit FIFO Level Register (IC_TXFLR)—Offset 74h

I2C Transmit FIFO Level Register

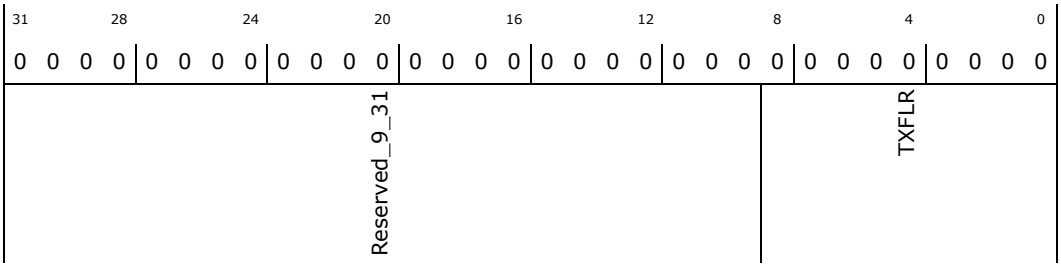
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved_9_31:** Reserved
8:0	0x0 RO	**TXFLR:** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.

9.24.31 I2C Receive FIFO Level Register (IC_RXFLR)—Offset 78h

I2C Receive FIFO Level Register

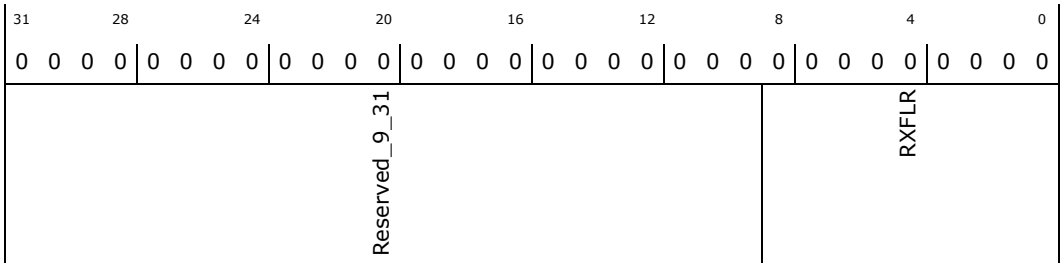
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RW	**Reserved_9_31:** Reserved
8:0	0x0 RO	**RXFLR:** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

9.24.32 I2C SDA Hold Time Length Register (IC_SDA_HOLD)—Offset 7Ch

I2C SDA Hold Time Length Register

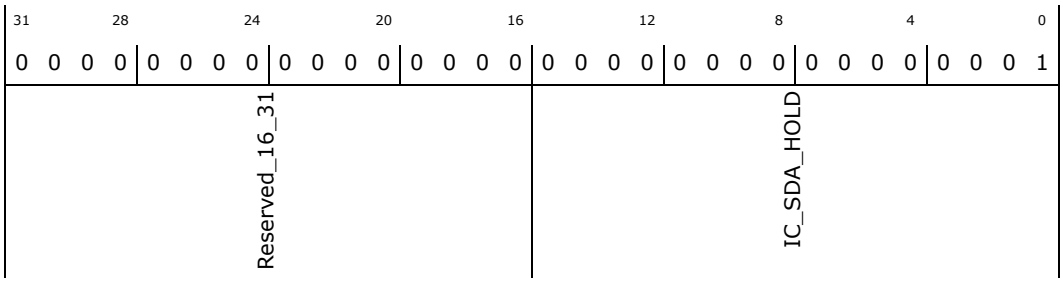
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Reserved_16_31:** Reserved
15:0	0x1 RW	**IC_SDA_HOLD:** Sets the required SDA hold time in units of ic_clk period.

9.24.33 I2C Transmit Abort Source Register (IC_TX_ABRT_SOURCE)—Offset 80h

I2C Transmit Abort Source Register

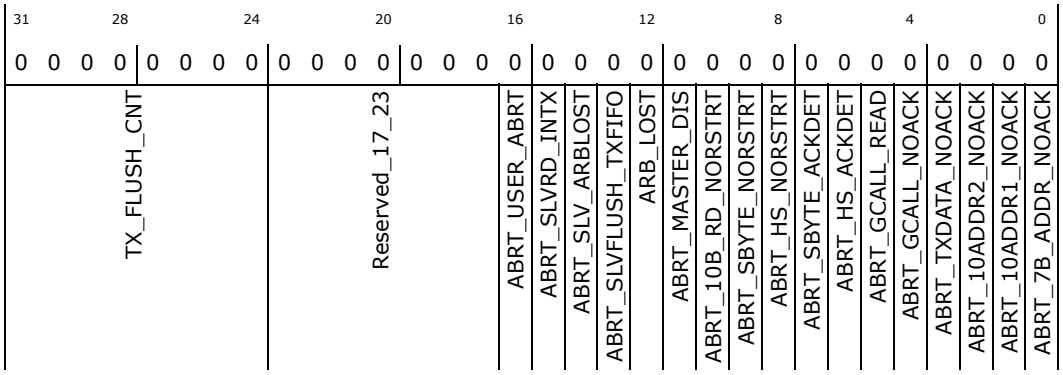
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**TX_FLUSH_CNT:** This field preserves the TXFLR value prior to the last TX_ABRT event. It is enabled when fix_ctrl_1680 =1 .It is cleared whenever I2C is disabled.
23:17	0x0 RW	**Reserved_17_23:** Reserved
16	0x0 RO	**ABRT_USER_ABRT:** This is a master-mode only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]). It is enabled only when fix_ctrl_1680 =1
15	0x0 RO	**ABRT_SLVRD_INTX:** 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register.
14	0x0 RO	**ABRT_SLV_ARBLOST:** 1: Slave lost the bus while transmitting data to a remote master. IC_TX_ABRT_SOURCE[12] is set at the same time.
13	0x0 RO	**ABRT_SLVFLUSH_TXFIFO:** 1: Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.
12	0x0 RO	**ARB_LOST:** 1: Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0x0 RO	**ABRT_MASTER_DIS:** 1: User tries to initiate a Master operation with the Master mode disabled.
10	0x0 RO	**ABRT_10B_RD_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RO	**ABRT_SBYTE_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte.
8	0x0 RO	**ABRT_HS_NORSTRT:** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0x0 RO	**ABRT_SBYTE_ACKDET:** 1: Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
6	0x0 RO	**ABRT_HS_ACKDET:** 1: Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
5	0x0 RO	**ABRT_GCALL_READ:** 1: DW_apb_i2c in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0x0 RO	**ABRT_GCALL_NOACK:** 1: DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0x0 RO	**ABRT_TXDATA_NOACK:** 1: This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0x0 RO	**ABRT_10ADDR2_NOACK:** 1: Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0x0 RO	**ABRT_10ADDR1_NOACK:** 1: Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0x0 RO	**ABRT_7B_ADDR_NOACK:** 1: Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

9.24.34 Generate Slave Data NACK Register (IC_SLV_DATA_NACK_ONLY)—Offset 84h

Generate Slave Data NACK Register

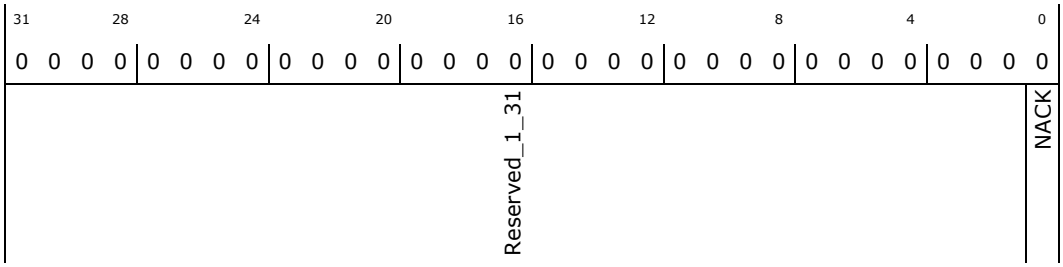
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x0 RW	**NACK:** Generate NACK. This NACK generation only occurs when DW_apb_i2c is a slavereceiver. If this register is set to a value of 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to a value of 0, it generates NACK/ACK, depending on normal criteria. 1 = generate NACK after data byte received 0 = generate NACK/ACK normally

9.24.35 DMA Control Register (IC_DMA_CR)—Offset 88h

DMA Control Register

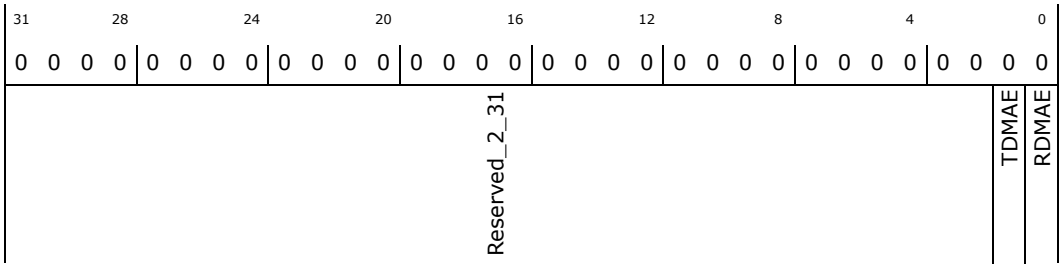
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved_2_31:** Reserved
1	0x0 RW	**TDMAE:** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel. 0 = Transmit DMA disabled 1 = Transmit DMA enabled
0	0x0 RW	**RDMAE:** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. 0 = Receive DMA disabled 1 = Receive DMA enabled

9.24.36 DMA Transmit Data Level Register (IC_DMA_TDLR)—Offset 8Ch

DMA Transmit Data Level Register

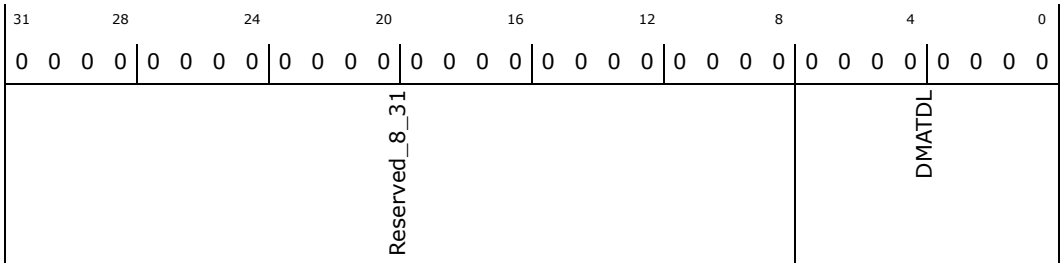
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x0 RW	**DMATDL:** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

9.24.37 I2C Receive Data Level Register (IC_DMA_RDLR)—Offset 90h

I2C Receive Data Level Register

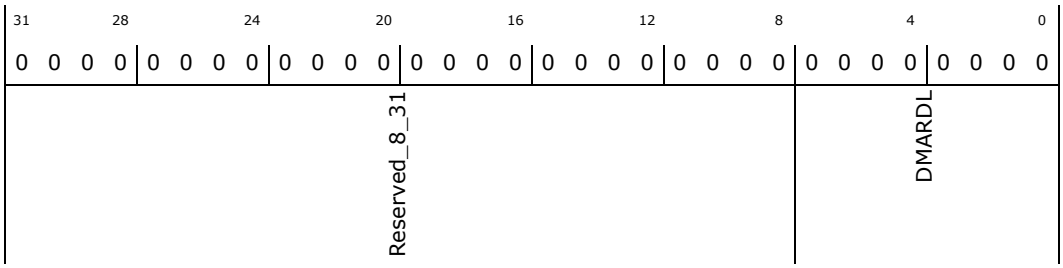
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x0 RW	**DMARDL:** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

9.24.38 I2C SDA Setup Register (IC_SDA_SETUP)—Offset 94h

I2C SDA Setup Register

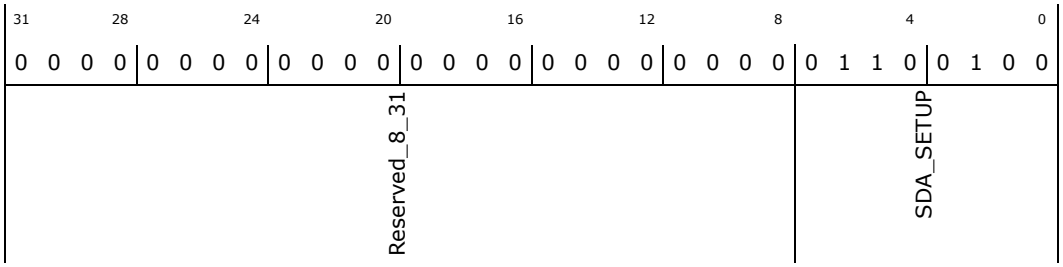
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000064h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x64 RW	**SDA_SETUP:** SDA Setup. It is recommended that if the required delay is 1000ns, then for an ic_clk frequency of 10 MHz, IC_SDA_SETUP should be programmed to a value of 11.

9.24.39 I2C ACK General Call Register (IC_ACK_GENERAL_CALL)—Offset 98h

I2C ACK General Call Register

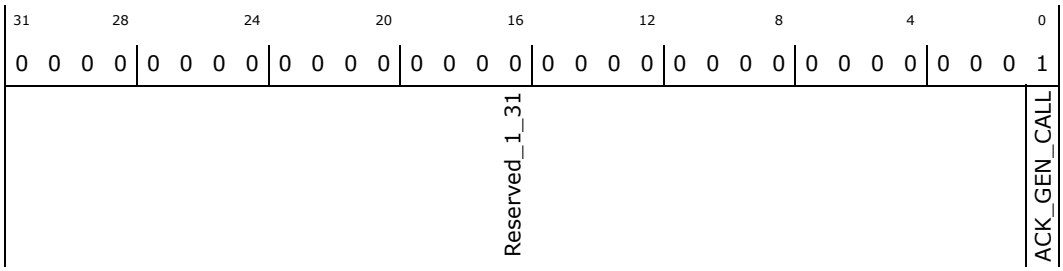
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RW	**Reserved_1_31:** Reserved
0	0x1 RW	**ACK_GEN_CALL:** ACK General Call. When set to 1, DW_apb_i2c responds with a ACK (by asserting ic_data_oe) when it receives a General Call. When set to 0, the DW_apb_i2c does not generate General Call interrupts.

9.24.40 I2C Enable Status Register (IC_ENABLE_STATUS)—Offset 9Ch

I2C Enable Status Register

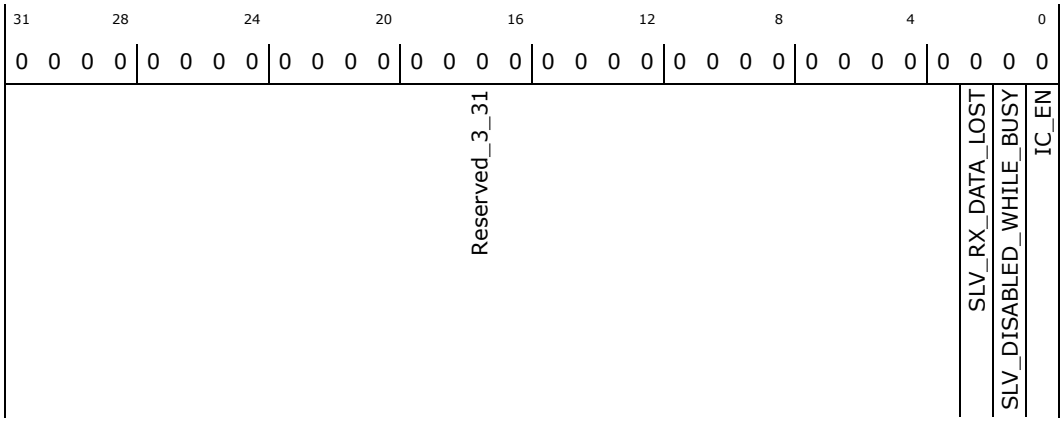
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RW	**Reserved_3_31:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RO	**SLV_RX_DATA_LOST:** This bit indicates if a Slave-Receiver operation has been aborted with at least one data byte received from an I2C transfer due to the setting of IC_ENABLE from 1 to 0.
1	0x0 RO	**SLV_DISABLED_WHILE_BUSY:** This bit indicates if a potential or active Slave operation has been aborted due to the setting of the IC_ENABLE register from 1 to 0.
0	0x0 RO	**IC_EN:** ic_en Status. This bit always reflects the value driven on the output port ic_en. When read as 1, DW_apb_i2c is deemed to be in an enabled state. When read as 0, DW_apb_i2c is deemed completely inactive.

9.24.41 SS/FS Mode Spike Length Register (IC_FS_SPKLEN)—Offset A0h

SS/FS Mode Spike Length Register

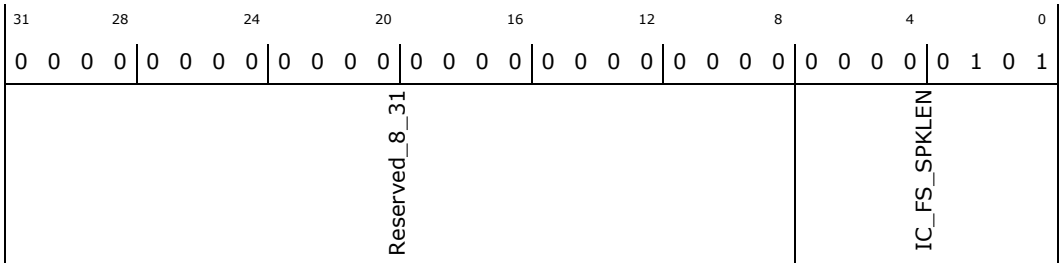
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000005h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x5 RW	**IC_FS_SPKLEN:** Maximum length (in ic_clk cycles) of suppressed spikes in SS and FS modes

9.24.42 HS Mode Spike Length Register (IC_HS_SPKLEN)—Offset A4h

HS Mode Spike Length Register

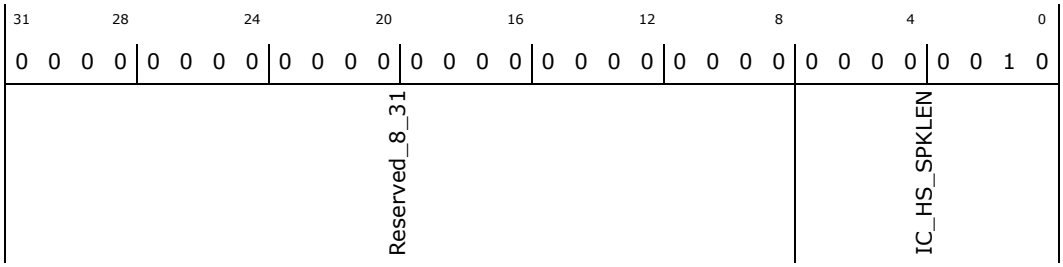
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RW	**Reserved_8_31:** Reserved
7:0	0x2 RW	**IC_HS_SPKLEN:** Maximum length (in ic_clk cycles) of suppressed spikes in HS mode

9.24.43 Component Parameter Register 1 (IC_COMP_PARAM_1)—Offset F4h

Component Parameter Register 1

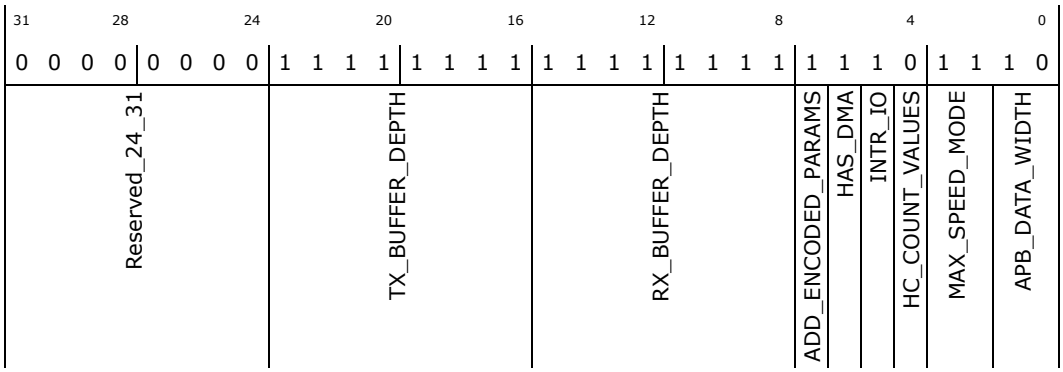
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00FFFFEEh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**Reserved_24_31:** Reserved
23:16	0xff RO	**TX_BUFFER_DEPTH:** The value of this register is derived from the IC_TX_BUFFER_DEPTH coreConsultant parameter.
15:8	0xff RO	**RX_BUFFER_DEPTH:** The value of this register is derived from the IC_RX_BUFFER_DEPTH coreConsultant parameter.
7	0x1 RO	**ADD_ENCODED_PARAMS:** The value of this register is derived from the IC_ADD_ENCODED_PARAMS coreConsultant parameter.
6	0x1 RO	**HAS_DMA:** The value of this register is derived from the IC_HAS_DMA coreConsultant parameter.
5	0x1 RO	**INTR_IO:** The value of this register is derived from the IC_INTR_IO coreConsultant parameter.
4	0x0 RO	**HC_COUNT_VALUES:** The value of this register is derived from the IC_HC_COUNT_VALUES coreConsultant parameter.
3:2	0x3 RO	**MAX_SPEED_MODE:** The value of this register is derived from the IC_MAX_SPEED_MODE coreConsultant parameter.
1:0	0x2 RO	**APB_DATA_WIDTH:** The value of this register is derived from the APB_DATA_WIDTH coreConsultant parameter.

9.24.44 I2C Component Version Register (IC_COMP_VERSION)—Offset F8h

I2C Component Version Register

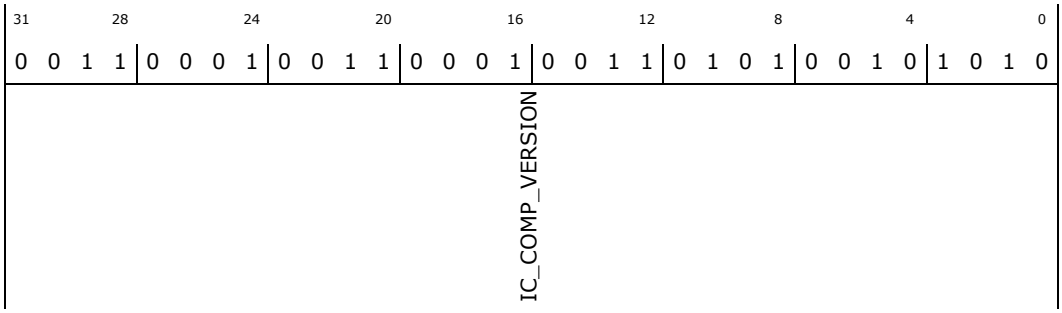
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 3131352Ah



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x3131352a RO	**IC_COMP_VERSION:** Specific values for this register are described in the Releases Table in the AMBA 2 release notes

9.24.45 I2C Component Type Register (IC_COMP_TYPE)—Offset FCh

I2C Component Type Register

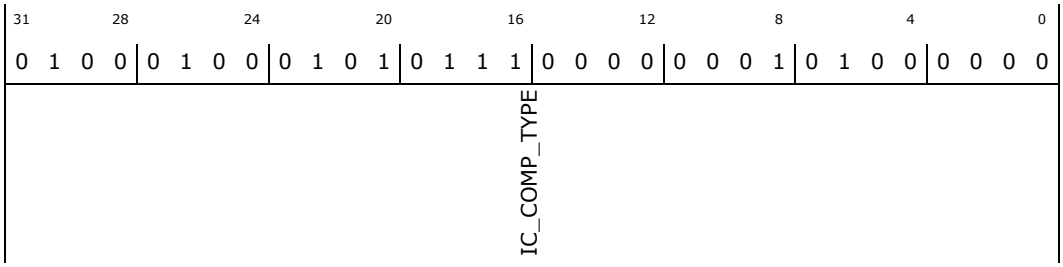
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 44570140h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x44570140 RO	**IC_COMP_TYPE:** Designware Component Type number = 0x44_57_01_40. This assigned unique hex value is constant and is derived from the two ASCII letters DW followed by a 16-bit unsigned number.

9.24.46 Clock params register (CLOCK_PARAMS)—Offset 800h

indicate if the i2c uses 133MHz or 100MHz

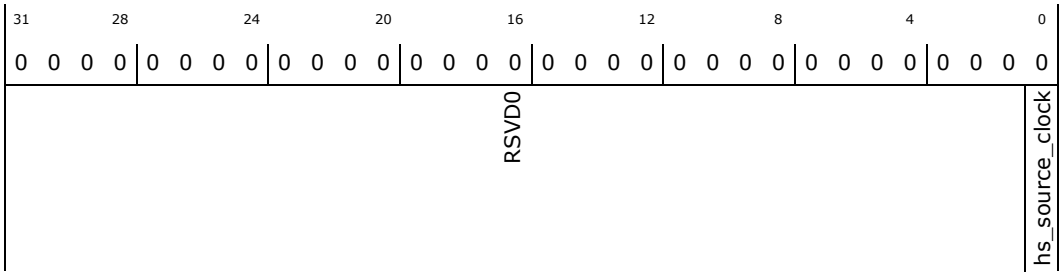
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RO	**hs_source_clock:** Reflects the value configured in hs_source_clock_sel in GPIODEF0. 0 -100MHz 1 -133MHz (high-speed operation compatible)

9.24.47 software reset (RESETS)—Offset 804h

software reset

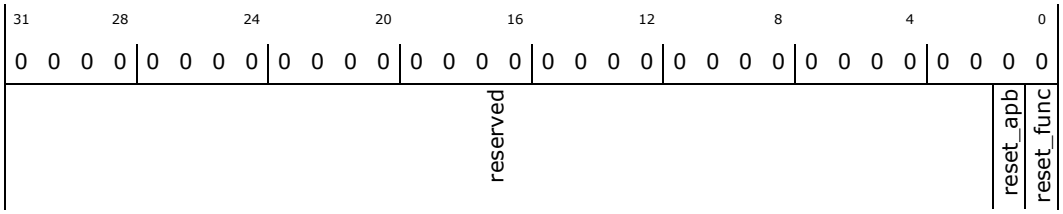
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (reserved):** Reserved
1	0x0 RW	**reset_apb:** reset the apb domain
0	0x0 RW	**reset_func:** reset the func clock domain

9.24.48 General purpose register (GENERAL)—Offset 808h

General purpose register

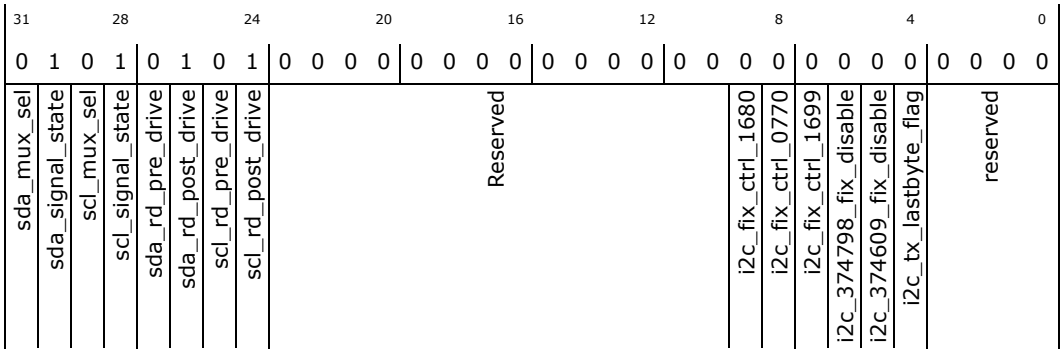
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 55000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**sda_mux_sel:** This bit selects the driver for the SDA signal: 1 = sda_signal_state, 0 = I2C logic
30	0x1 RW	**sda_signal_state:** This bit is used when sda_mux_sel = 1, used to drive the SDA signal on the I2C interface
29	0x0 RW	**scl_mux_sel:** This bit selects the driver for the SCL signal: 1 = scl_signal_state, 0 = I2C logic
28	0x1 RW	**scl_signal_state:** This bit is used when scl_mux_sel = 1, used to drive the SCL signal on the I2C interface
27	0x0 RO	**sda_rd_pre_drive:** Read only bit used to see the status of the SDA signal coming from the I2C logic
26	0x1 RO	**sda_rd_post_drive:** Read only bit used to see the status of the SDA signal coming from the pad
25	0x0 RO	**scl_rd_pre_drive:** Read only bit used to see the status of the SCL signal coming from the I2C logic
24	0x1 RO	**scl_rd_post_drive:** Read only bit used to see the status of the SCL signal coming from the pad
23:10	0x0 RO	**Reserved:** Reserved
9	0x0 RW	**i2c_fix_ctrl_1680:** Control port to enable fix 9000521680,Generation of STOP condition without data transfer
8	0x0 RW	**i2c_fix_ctrl_0770:** Control port to enable fix 9000530770,Stop generating DMA requests during Tx FIFO flush conditions
7	0x0 RW	**i2c_fix_ctrl_1699:** Control port to enable fix 9000481699,Rx data is pushed to Rx FIFO only after Tx FIFO is not-empty
6	0x0 RW	**i2c_374798_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374798)
5	0x0 RW	**i2c_374609_fix_disable:** chicken bit for Fix for NACK bug (HSD # 374609)

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**i2c_tx_lastbyte_flag:** SW indicates it's last byte for TX transaction (HSD # 374798)
3:0	0x0 RW	**reserved:** reserved

9.24.49 TX transaction counter (I2C_ACK_COUNT)—Offset 818h

TX transaction counter

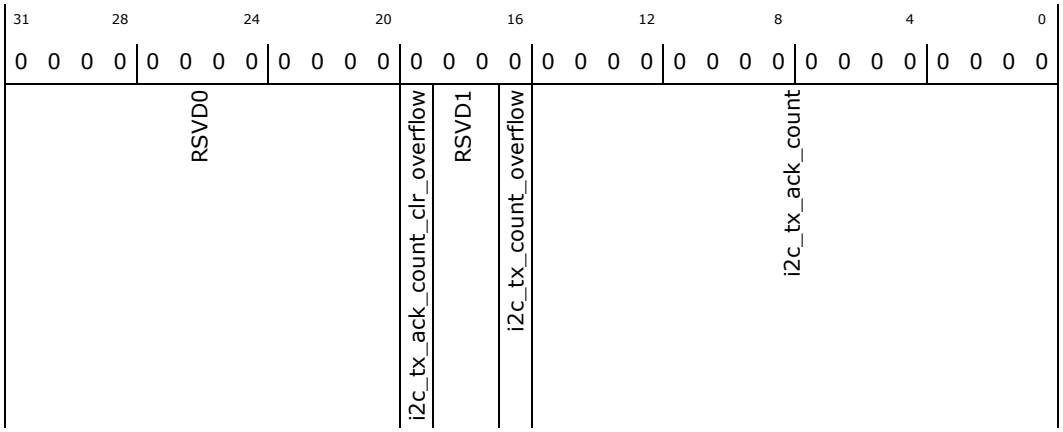
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**RSVD0:** Reserved
19	0x0 RW	**i2c_tx_ack_count_clr_overflow:** SW clear of TX transaction (byte) counter
18:17	0x0 RO	**RSVD1:** Reserved
16	0x0 RO	**i2c_tx_count_overflow:** indicate there was count overflow
15:0	0x0 RO	**i2c_tx_ack_count:** indicate TX transaction count for SW to read

9.24.50 TX transaction complete interrupt status register (I2C_TX_COMPLETE_INTR_STAT)—Offset 820h

TX transaction has finished interrupt

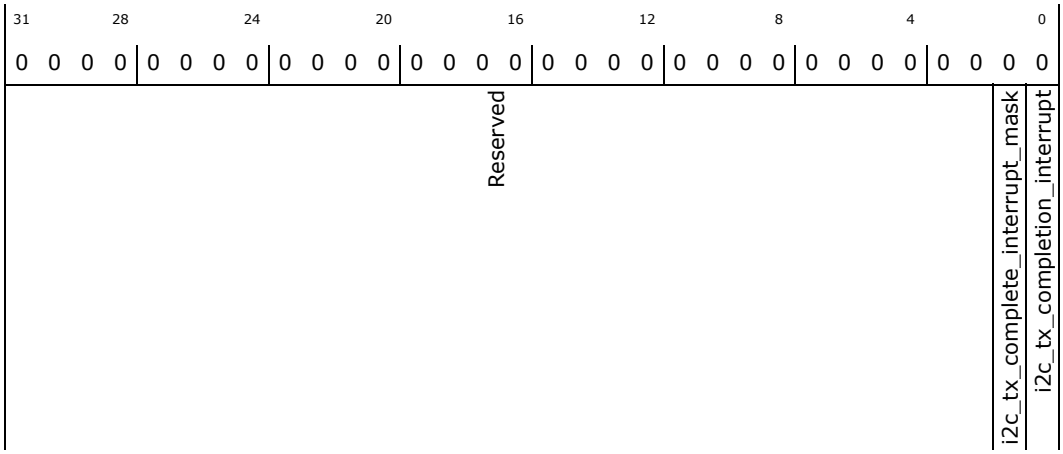
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved:** Reserved
1	0x0 RW	**i2c_tx_complete_interrupt_mask:** Mask TX transaction has finished interrupt
0	0x0 RO	**i2c_tx_completion_interrupt:** indicate TX transaction has finished

9.24.51 TX transaction complete interrupt clear register (I2C_TX_COMPLETE_INTR_CLR)—Offset 824h

indicate TX transaction has finished write 1 to clear the interrupt

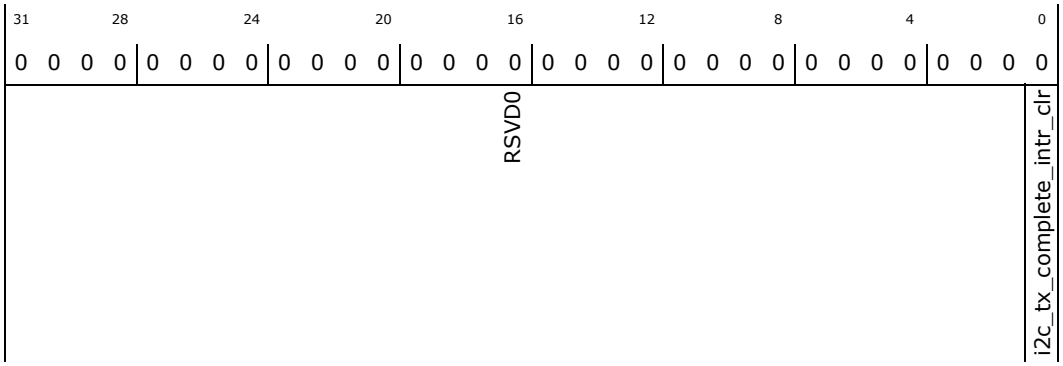
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 824h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:24, F:7] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RW	**i2c_tx_complete_intr_clr:** indicate TX transaction has finished write 1 to clear the interrupt

9.25 SIO HSUART 0 PCI Configuration Registers

Table 88. Summary of SIO HSUART 0 PCI Configuration Registers—0/30/3

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4663	00008086h
4–7h	4	"STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h" on page 4663	00100000h
8–Bh	4	"REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4665	00000000h
C–Fh	4	"CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4666	00800000h
10–13h	4	"BAR -Base Address Register (BAR)—Offset 10h" on page 4666	00000000h
14–17h	4	"BAR1 -Base Address Register1 (BAR1)—Offset 14h" on page 4667	00000000h
2C–2Fh	4	"SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4668	00000000h
30–33h	4	"EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4669	00000000h
34–37h	4	"CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4669	00000000h
3C–3Fh	4	"INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4670	00000100h
80–83h	4	"POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4670	00030001h
84–87h	4	"PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4671	00000008h
F8–FBh	4	"Manufacturers ID (MANID)—Offset F8h" on page 4672	00000000h

9.25.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

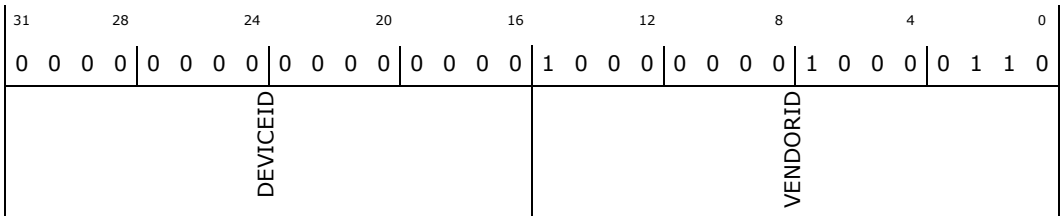
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**DEVICEID:** Device ID identifies the particular AHB/APB device. This is tied to a strap at the top level. Because of tool issues, the HTML files show this field as 0, but the following are the POR values for SoC: LPIO1 DMA: 0x2286 LPIO1 PWM1: 0x2288 LPIO1 PWM2: 0x2289 LPIO1 HSUART1: 0x228A LPIO1 HSUART2: 0x228C LPIO1 SPI1: 0x228E LPIO1 SPI2: 0x2290 LPIO1 SPI3: 0x22AC LPIO2 DMA: 0x22C0 LPIO2 I2C1: 0x22C1 LPIO2 I2C2: 0x22C2 LPIO2 I2C3: 0x22C3 LPIO2 I2C4: 0x22C4 LPIO2 I2C5: 0x22C5 LPIO2 I2C6: 0x22C6 LPIO2 I2C7: 0x22C7 For the final word on this, please see Ray Ng's SoC RevID and DevID HAS on Infofactory: https://ifcollaborate.intel.com/IFC/getdoc.aspx?docbase=InfoFactoryKBandchronid=09005ffd80e84b43andver=CURRENTandqepop=false
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap the top level.

9.25.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

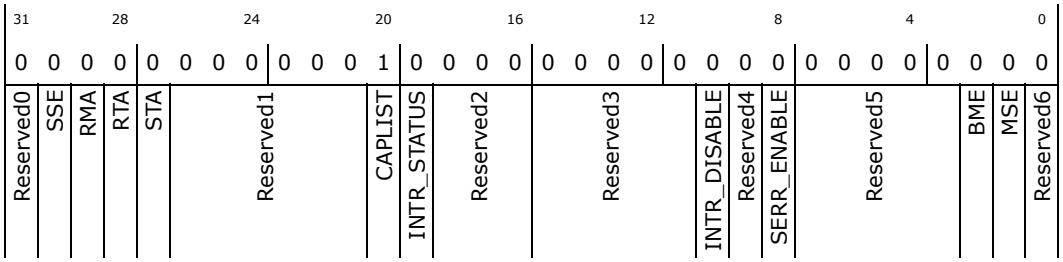
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved0:** Reserved
30	0x0 RW/1C	**SSE:** This bit is set when a device sends an DO_SERR message, and the SERR# Enable bit in the Command register is 1
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric PortReceived Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27	0x0 RW/1C	**STA:** The Bridge sets this bit whenever it responds to a transaction with CA abort. If the SERR# Enable bit is set, the Bridge sets the Signaled System Error bit and sends an DO_SERR message on the IOSF Sideband.
26:21	0x0 RO	**Reserved1:** Reserved
20	0x1 RO	**CAPLIST:** Capabilities List: Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt .i.e Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.. Reset value of this bit is 0.
9	0x0 RO	**Reserved4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: If both SERR# Enable and the Unsupported Request Reporting Enable (URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0x0 RO	**Reserved6:** Reserved

9.25.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

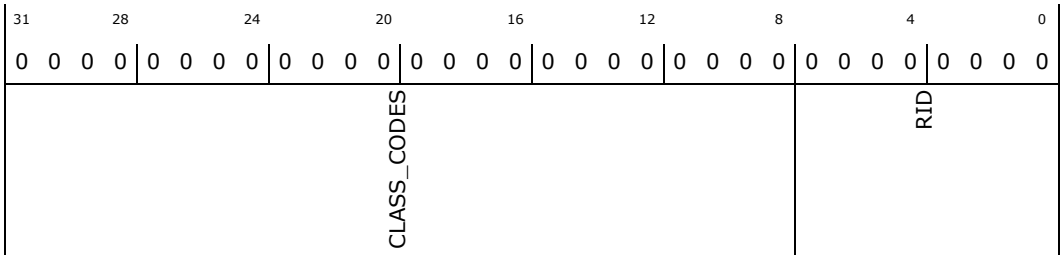
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

9.25.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

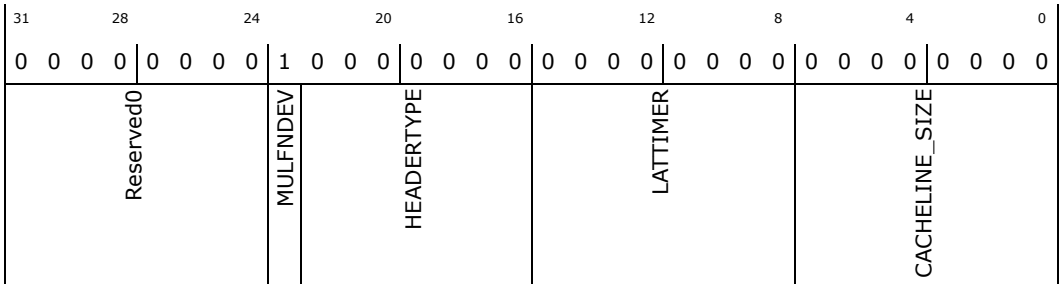
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + Ch

Default: 00800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x1 RO	**MULFNDEV:** Multi Function Device: This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. Value of 1 indicates multifunction device value of 0 indicates single function device
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	0x0 RO	**LATTIMER:** Latency Timer: Doesn.t apply to PCI Express. Hardwired to 00h.
7:0	0x0 RW	**CACHELINE_SIZE:** Cache Line Size: Doesn.t apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

9.25.5 BAR -Base Address Register (BAR)—Offset 10h

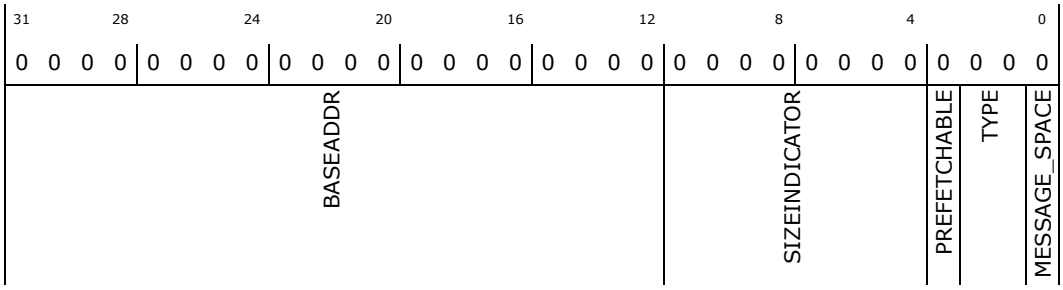
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the AHB device memory space. Taken from Strap values as 1's. Please note that for DMA this field goes from [31:14], or 16kbyte, and the SIZEINDICATOR field goes from [13:4].
11:4	0x0 RO	**SIZEINDICATOR:** Size Indicator Read Only: Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0x0 RO	**TYPE:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.25.6 BAR1 -Base Address Register1 (BAR1)—Offset 14h

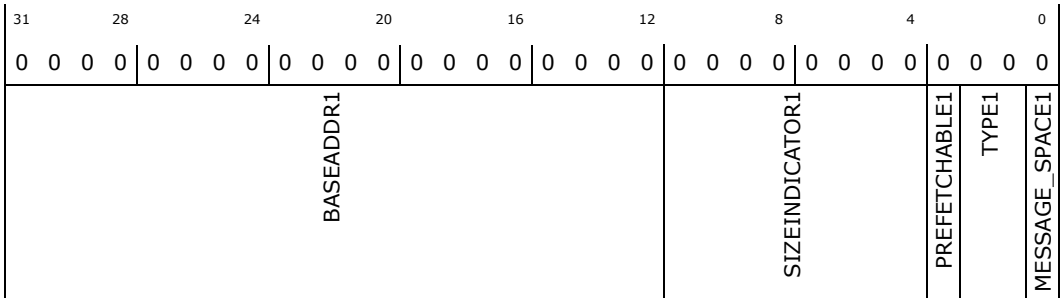
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	0x0 RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not
2:1	0x0 RO	**TYPE1:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.25.7 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

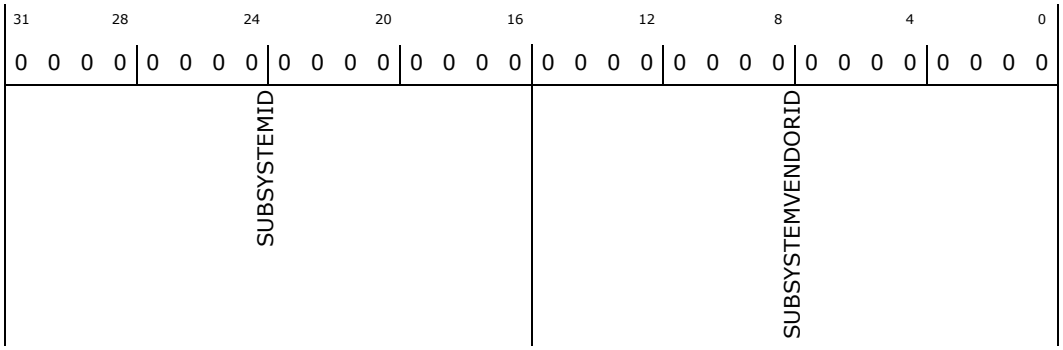
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

9.25.8 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

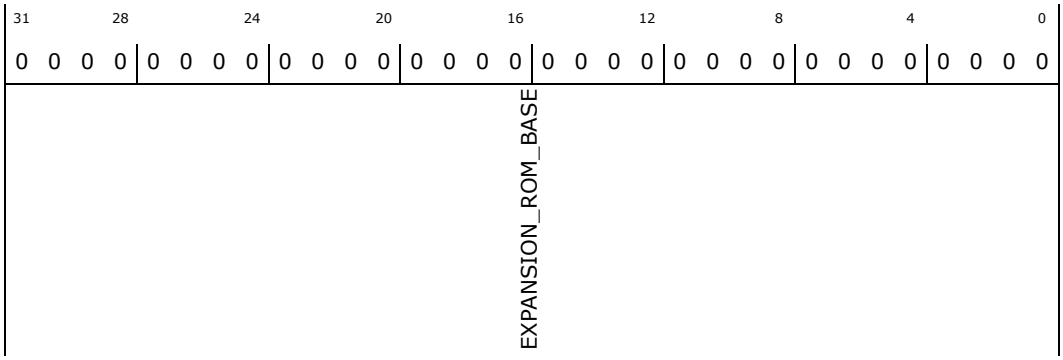
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** A value of all zeros indicates no support for expansion ROM.

9.25.9 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

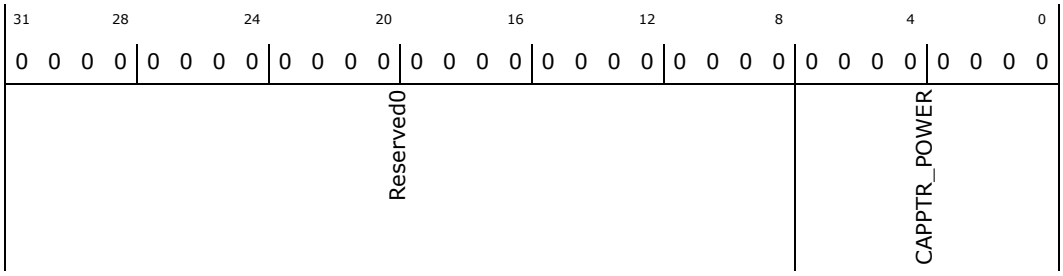
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x0 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

9.25.10 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

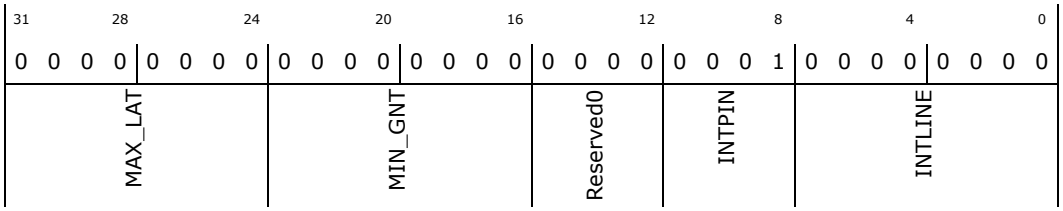
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

9.25.11 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

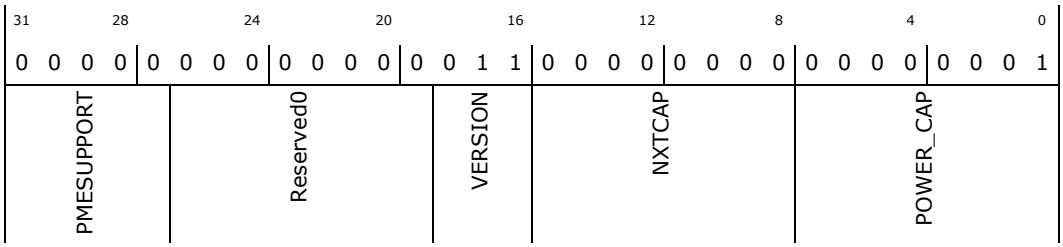
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** PME_Support - This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

9.25.12 PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

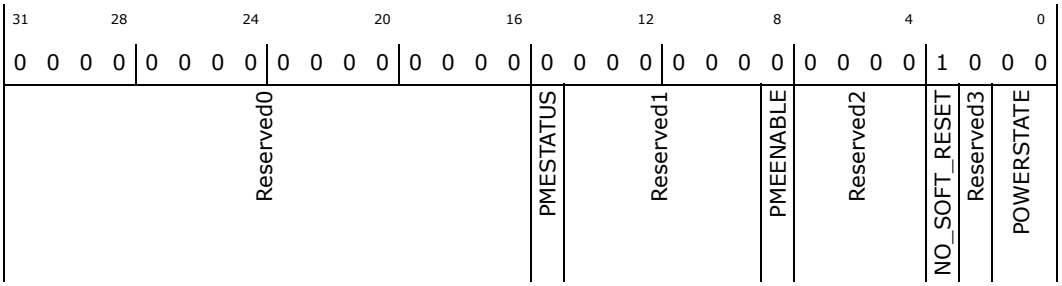
PMECTRLSTATUS - PME Control and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

9.25.13 Manufacturers ID (MANID)—Offset F8h

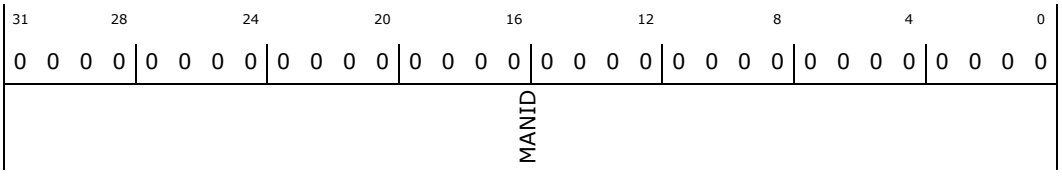
Manufacturers ID

Access Method

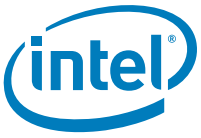
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:3] + F8h

Default: 00000000h



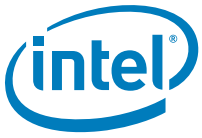
Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: This register is brought out as straps to the top level.



9.26 SIO HSUART 0 Memory Mapped I/O Registers

Table 89. Summary of SIO HSUART 0 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Receive Buffer Register/ Transmit Holding Register/ Divisor Latch (Low) (RBR_THR_DLL)—Offset 0h" on page 4676	00000000h
4–7h	4	"Divisor Latch (High)/ Interrupt Enable Register (IER_DLH)—Offset 4h" on page 4676	00000000h
8–Bh	4	"Interrupt Identification Register and FIFO Control Register (IIR_FCR)—Offset 8h" on page 4677	00000001h
C–Fh	4	"Line Control Register (LCR)—Offset Ch" on page 4678	00000000h
10–13h	4	"Modem Control Register (MCR)—Offset 10h" on page 4680	00000000h
14–17h	4	"Line Status Register (LSR)—Offset 14h" on page 4681	00000060h
18–1Bh	4	"Modem Status Register (MSR)—Offset 18h" on page 4683	00000000h
1C–1Fh	4	"Scratchpad Register (SCR)—Offset 1Ch" on page 4684	00000000h
30–33h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 0 (SRBR_STHR0)—Offset 30h" on page 4685	00000000h
34–37h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 1 (SRBR_STHR1)—Offset 34h" on page 4686	00000000h
38–3Bh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 2 (SRBR_STHR2)—Offset 38h" on page 4687	00000000h
3C–3Fh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 3 (SRBR_STHR3)—Offset 3Ch" on page 4688	00000000h
40–43h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 4 (SRBR_STHR4)—Offset 40h" on page 4689	00000000h
44–47h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 5 (SRBR_STHR5)—Offset 44h" on page 4690	00000000h
48–4Bh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 6 (SRBR_STHR6)—Offset 48h" on page 4691	00000000h
4C–4Fh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 7 (SRBR_STHR7)—Offset 4Ch" on page 4692	00000000h
50–53h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 8 (SRBR_STHR8)—Offset 50h" on page 4693	00000000h
54–57h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 9 (SRBR_STHR9)—Offset 54h" on page 4694	00000000h
58–5Bh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 10 (SRBR_STHR10)—Offset 58h" on page 4695	00000000h
5C–5Fh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 11 (SRBR_STHR11)—Offset 5Ch" on page 4696	00000000h
60–63h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 12 (SRBR_STHR12)—Offset 60h" on page 4697	00000000h
64–67h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 13 (SRBR_STHR13)—Offset 64h" on page 4698	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
68–6Bh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 14 (SRBR_STHR14)—Offset 68h" on page 4699	00000000h
6C–6Fh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 15 (SRBR_STHR15)—Offset 6Ch" on page 4700	00000000h
70–73h	4	"FIFO Access Register (FAR)—Offset 70h" on page 4701	00000000h
74–77h	4	"Transmit FIFO Read (TFR)—Offset 74h" on page 4701	00000000h
78–7Bh	4	"Receive FIFO Write (RFW)—Offset 78h" on page 4702	00000000h
7C–7Fh	4	"UART Status Register (USR)—Offset 7Ch" on page 4703	00000006h
80–83h	4	"Transmit FIFO Level (TFL)—Offset 80h" on page 4704	00000000h
84–87h	4	"Receive FIFO Level (RFL)—Offset 84h" on page 4705	00000000h
88–8Bh	4	"Software Reset Register (SRR)—Offset 88h" on page 4705	00000000h
8C–8Fh	4	"Shadow Request to Send (SRTS)—Offset 8Ch" on page 4706	00000000h
90–93h	4	"Shadow Break Control Register (SBCR)—Offset 90h" on page 4707	00000000h
94–97h	4	"Shadow DMA Mode (SDMAM)—Offset 94h" on page 4707	00000000h
98–9Bh	4	"Shadow FIFO Enable (SFE)—Offset 98h" on page 4708	00000000h
9C–9Fh	4	"Shadow Request to Send (SRTS)—Offset 8Ch" on page 4706	00000000h
A0–A3h	4	"Shadow TX Empty Trigger (STET)—Offset A0h" on page 4709	00000000h
A4–A7h	4	"Halt TX (HTX)—Offset A4h" on page 4710	00000000h
A8–ABh	4	"DMA Software Acknowledge (DMASA)—Offset A8h" on page 4711	00000000h
F4–F7h	4	"Component Parameter Register (CPR)—Offset F4h" on page 4711	00043F32h
F8–FBh	4	"UART Component Version (UCV)—Offset F8h" on page 4713	3330382Ah
FC–FFh	4	"Component Type Register (CTR)—Offset FCh" on page 4713	44570110h
800–803h	4	"private clock params (PRV_CLOCK_PARAMS)—Offset 800h" on page 4713	00000000h
804–807h	4	"software reset (RESETS)—Offset 804h" on page 4714	00000000h
808–80Bh	4	"General purpose register (GENERAL)—Offset 808h" on page 4715	00000050h
818–81Bh	4	"Transaction counter (UART_BYTE_COUNT)—Offset 818h" on page 4716	00000000h
820–823h	4	"Overflow interrupt (UART_OVERFLOW_INTR_STAT)—Offset 820h" on page 4716	00000000h

9.26.1 Receive Buffer Register/ Transmit Holding Register/ Divisor Latch (Low) (RBR_THR_DLL)—Offset 0h

Receive Buffer Register/ Transmit Holding Register/ Divisor Latch (Low)

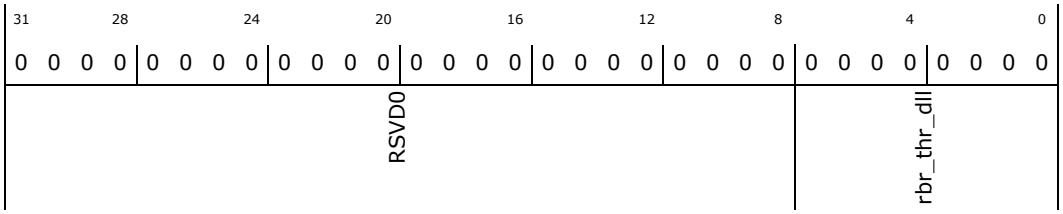
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7:0	0x0 RW	**rbr_thr_dll:** Can be referred to 3 registers with different descriptions- go to Synopsys DesignWare DW_apb_uart Databook Spec in order to learn more

9.26.2 Divisor Latch (High)/ Interrupt Enable Register (IER_DLH)—Offset 4h

Divisor Latch (High)/ Interrupt Enable Register

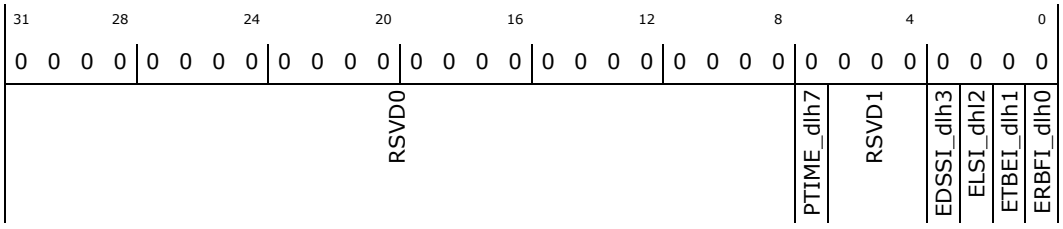
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7	0x0 RW	**PTIME_dlh7:** Can be referred to 2 registers with different descriptions- go to Synopsys DesignWare DW_apb_uart Databook Spec in order to learn more
6:4	0x0 RO	**RSVD1:** Reserved
3	0x0 RW	**EDSSI_dlh3:** Can be referred to 2 registers with different descriptions- go to Synopsys DesignWare DW_apb_uart Databook Spec in order to learn more
2	0x0 RW	**ELSI_dhl2:** Can be referred to 2 registers with different descriptions- go to Synopsys DesignWare DW_apb_uart Databook Spec in order to learn more
1	0x0 RW	**ETBEI_dlh1:** Can be referred to 2 registers with different descriptions- go to Synopsys DesignWare DW_apb_uart Databook Spec in order to learn more
0	0x0 RW	**ERBFI_dlh0:** Can be referred to 2 registers with different descriptions- go to Synopsys DesignWare DW_apb_uart Databook Spec in order to learn more

9.26.3 Interrupt Identification Register and FIFO Control Register (IIR_FCR)—Offset 8h

Interrupt Identification Register and FIFO Control Register

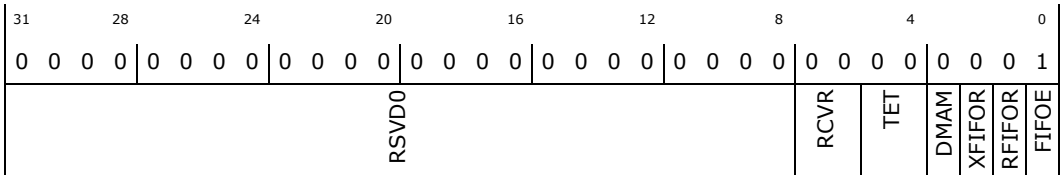
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7:6	0x0 RW	**FIFOSE_RCVR (RCVR):** RCVR Trigger. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. For details on DMA support, refer to DMA Support on page 43. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO full 10 = FIFO full 11 = FIFO 2 less than full Reset Value: 0x0

Bit Range	Default & Access	Field Name (ID): Description
5:4	0x0 RW	**Res_TET (TET):** TX Empty Trigger. Writes have no effect when THRE_MODE_USER == Disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. For details on DMA support, refer to DMA Support on page 43. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO full 11 = FIFO full Reset Value: 0x0
3	0x0 RW	**IID3_DMAM (DMAM):** DMA Mode. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == No). For details on DMA support, refer to DMA Support on page 43. 0 = mode 0 1 = mode 1 Reset Value: 0x0
2	0x0 RW	**IID2_XFIFOR (XFIFOR):** XMIT FIFO Reset. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0
1	0x0 RW	**IID1_RFIFOR (RFIFOR):** RCVR FIFO Reset. This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0
0	0x1 RW	**IID0_FIFOE (FIFOE):** FIFO Enable. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset. Reset Value: 0x0

9.26.4 Line Control Register (LCR)—Offset Ch

Line Control Register

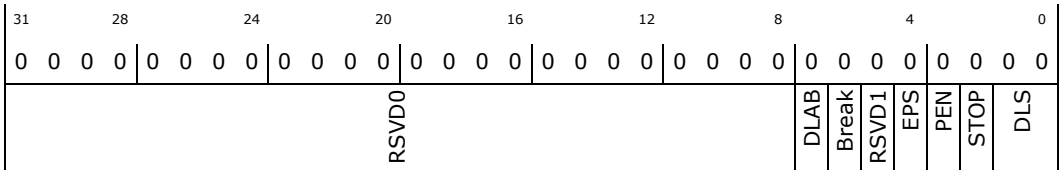
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW	**DLAB:** Divisor Latch Access Bit. If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. Reset Value: 0x0
6	0x0 RW	**Break:** Break Control Bit.This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low. Reset Value: 0x0
5	0x0 RO	**RSVD1:** Reserved
4	0x0 RW	**EPS:** Even Parity Select. If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked. Reset Value: 0x0
3	0x0 RW	**PEN:** Parity Enable. If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0 = parity disabled 1 = parity enabled Reset Value: 0x0
2	0x0 RW	**STOP:** Number of stop bits. If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0 = 1 stop bit 1 = 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit Reset Value: 0x0
1:0	0x0 RW	**DLS:** Data Length Select. If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits Reset Value: 0x0

9.26.5 Modem Control Register (MCR)—Offset 10h

Modem Control Register

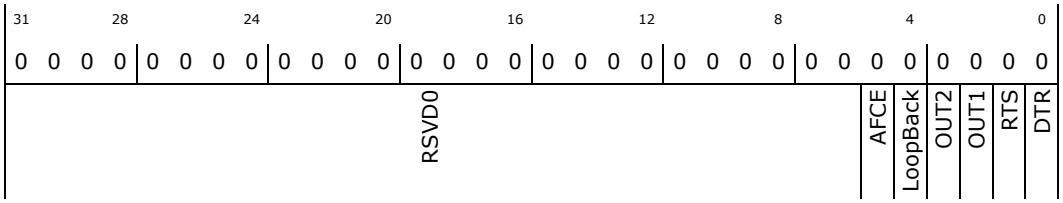
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**RSVD0:** Reserved
5	0x0 RW	**AFCE:** Auto Flow Control Enable. Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled as described in Auto Flow Control on page 37. 0 = Auto Flow Control Mode disabled 1 = Auto Flow Control Mode enabled Reset Value: 0x0
4	0x0 RW	**LoopBack:** LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line. Reset Value: 0x0
3	0x0 RW	**OUT2:** OUT2. This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: 0 = out2_n de-asserted (logic 1) 1 = out2_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0
2	0x0 RW	**OUT1:** OUT1. This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n, that is: 0 = out1_n de-asserted (logic 1) 1 = out1_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**RTS:** Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0
0	0x0 RW	**DTR:** Data Terminal Ready. This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is: 0 = dtr_n de-asserted (logic 1) 1 = dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0

9.26.6 Line Status Register (LSR)—Offset 14h

Line Status Register

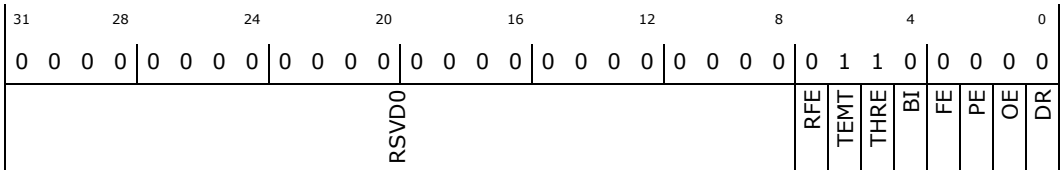
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

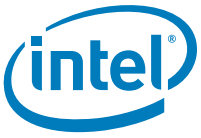
Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000060h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7	0x0 RO	**RFE:** Receiver FIFO Error bit. This bit is only relevant when FIFO_MODE != NONE AND FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. 0 = no error in RX FIFO 1 = error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO. Reset Value: 0x0



Bit Range	Default & Access	Field Name (ID): Description
6	0x1 RO	**TEMT:** Transmitter Empty bit. If in FIFO mode (FIFO_MODE != NONE) and FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty. Reset Value: 0x1
5	0x1 RO	**THRE:** Transmit Holding Register Empty bit. If THRE_MODE_USER == Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting. For more details, see Programmable THRE Interrupt on page 40. Reset Value: 0x1
4	0x0 RO	**BI:** Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read. Reset Value: 0x0
3	0x0 RO	**FE:** Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no framing error 1 = framing error Reading the LSR clears the FE bit. Reset Value: 0x0
2	0x0 RO	**PE:** Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no parity error 1 = parity error Reading the LSR clears the PE bit. Reset Value: 0x0

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RO	**OE:** Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0 = no overrun error 1 = overrun error Reading the LSR clears the OE bit. Reset Value: 0x0
0	0x0 RO	**DR:** Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0 = no data ready 1 = data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode. Reset Value: 0x0

9.26.7 Modem Status Register (MSR)—Offset 18h

Modem Status Register

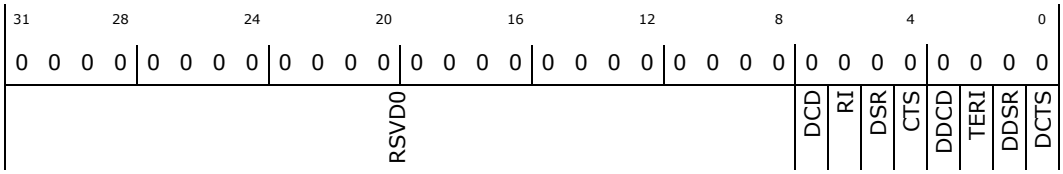
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7	0x0 RO	**DCD:** Data Carrier Detect. This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0 = dcd_n input is de-asserted (logic 1) 1 = dcd_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2). Reset Value: 0x0
6	0x0 RO	**RI:** Ring Indicator. This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0 = ri_n input is de-asserted (logic 1) 1 = ri_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1). Reset Value: 0x0

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RO	**DSR:** Data Set Ready. This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. 0 = dsr_n input is de-asserted (logic 1) 1 = dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR). Reset Value: 0x0
4	0x0 RO	**CTS:** Clear to Send. This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. 0 = cts_n input is de-asserted (logic 1) 1 = cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS). Reset Value: 0x0
3	0x0 RO	**DDCD:** Delta Data Carrier Detect. This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0 = no change on dcd_n since last read of MSR 1 = change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] = 1), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted. Reset Value: 0x0
2	0x0 RO	**TERI:** Trailing Edge of Ring Indicator. This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 0 = no change on ri_n since last read of MSR 1 = change on ri_n since last read of MSR Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] = 1), TERI reflects when MCR[2] (Out1) has changed state from a high to a low. Reset Value: 0x0
1	0x0 RO	**DDSR:** Delta Data Set Ready. This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0 = no change on dsr_n since last read of MSR 1 = change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted. Reset Value: 0x0
0	0x0 RO	**DCTS:** Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0 = no change on cts_n since last read of MSR 1 = change on cts_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted. Reset Value: 0x0

9.26.8 Scratchpad Register (SCR)—Offset 1Ch

Scratchpad Register

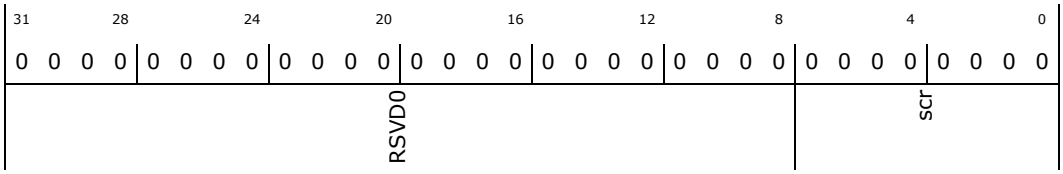
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7:0	0x0 RW	**scr:** This register is for programmers to use as a temporary storage space. It has no defined purpose in the DW_apb_uart. Reset Value: 0x0

9.26.9 Shadow Receive Buffer Register and Shadow Transmit Holding Register 0 (SRBR_STHR0)—Offset 30h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 0

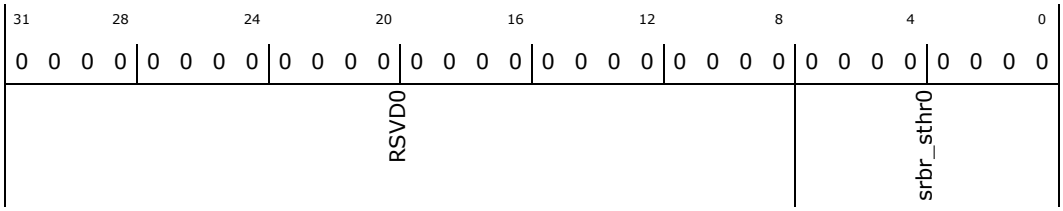
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr0:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.26.10 Shadow Receive Buffer Register and Shadow Transmit Holding Register 1 (SRBR_STHR1)—Offset 34h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 1

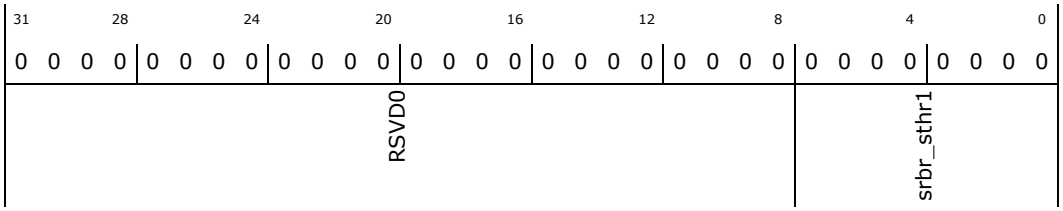
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr1:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.26.11 Shadow Receive Buffer Register and Shadow Transmit Holding Register 2 (SRBR_STHR2)—Offset 38h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 2

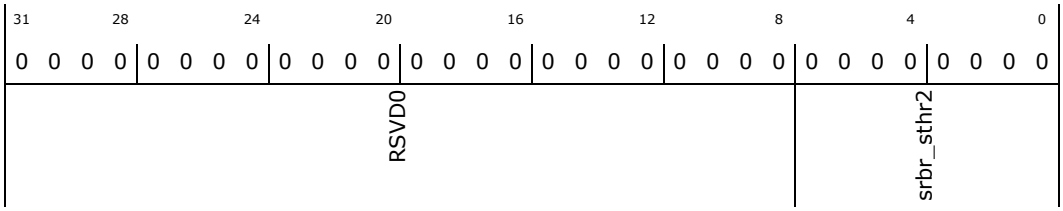
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr2:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.26.12 Shadow Receive Buffer Register and Shadow Transmit Holding Register 3 (SRBR_STHR3)—Offset 3Ch

Shadow Receive Buffer Register and Shadow Transmit Holding Register 3

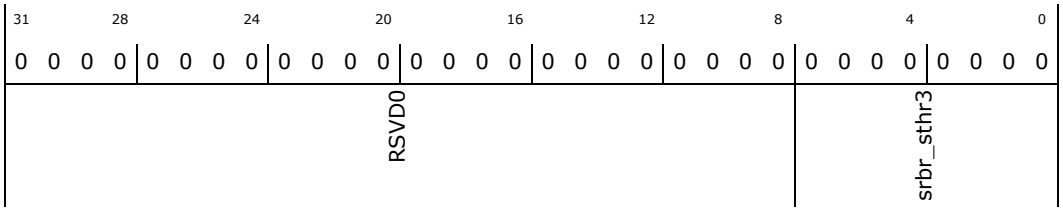
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr3:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.26.13 Shadow Receive Buffer Register and Shadow Transmit Holding Register 4 (SRBR_STHR4)—Offset 40h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 4

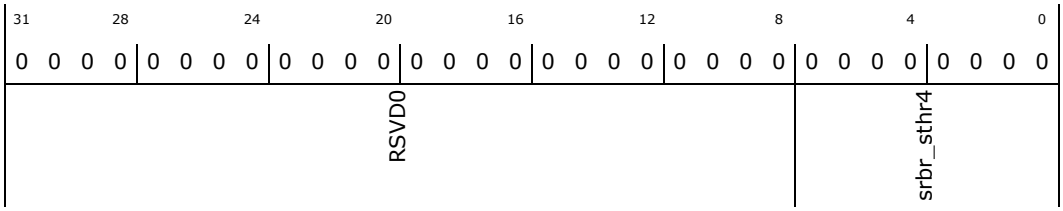
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr4:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.26.14 Shadow Receive Buffer Register and Shadow Transmit Holding Register 5 (SRBR_STHR5)—Offset 44h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 5

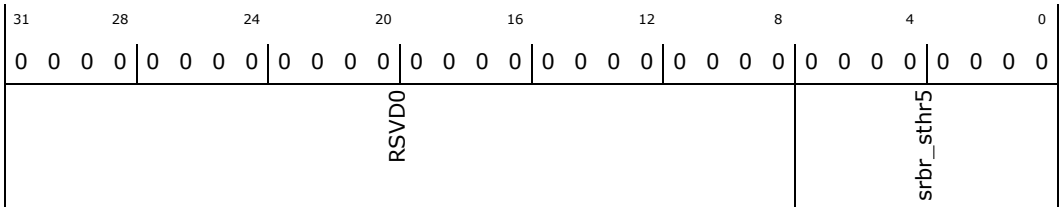
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr5:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.26.15 Shadow Receive Buffer Register and Shadow Transmit Holding Register 6 (SRBR_STHR6)—Offset 48h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 6

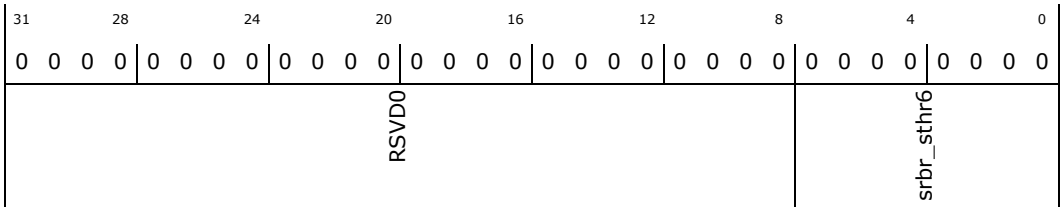
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr6:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.26.16 Shadow Receive Buffer Register and Shadow Transmit Holding Register 7 (SRBR_STHR7)—Offset 4Ch

Shadow Receive Buffer Register and Shadow Transmit Holding Register 7

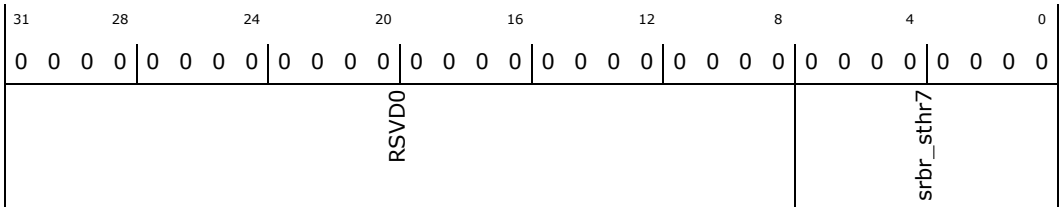
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr7:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.26.17 Shadow Receive Buffer Register and Shadow Transmit Holding Register 8 (SRBR_STHR8)—Offset 50h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 8

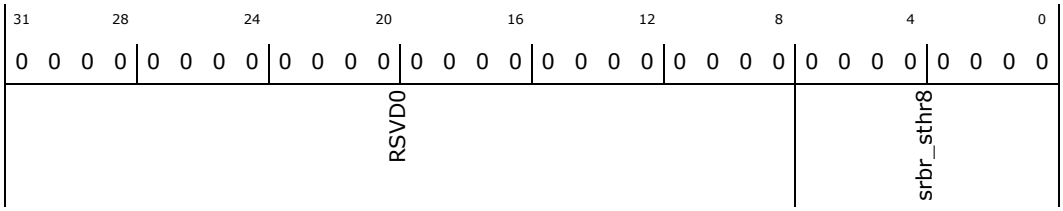
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr8:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.26.18 Shadow Receive Buffer Register and Shadow Transmit Holding Register 9 (SRBR_STHR9)—Offset 54h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 9

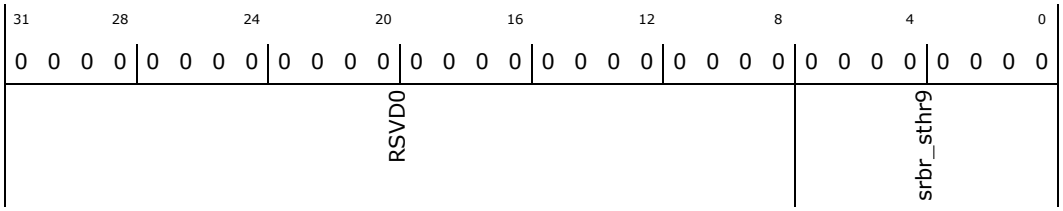
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr9:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.26.19 Shadow Receive Buffer Register and Shadow Transmit Holding Register 10 (SRBR_STHR10)—Offset 58h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 10

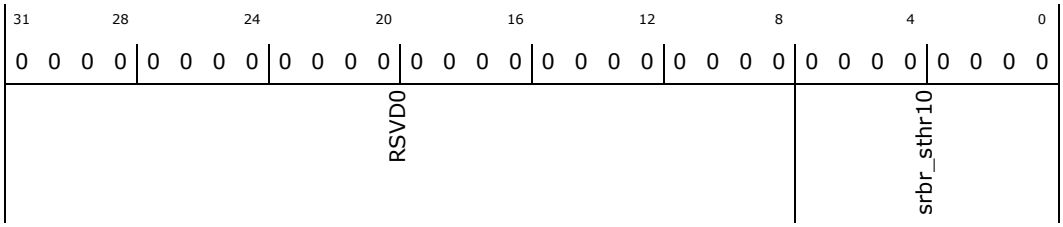
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr10:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.26.20 Shadow Receive Buffer Register and Shadow Transmit Holding Register 11 (SRBR_STHR11)—Offset 5Ch

Shadow Receive Buffer Register and Shadow Transmit Holding Register 11

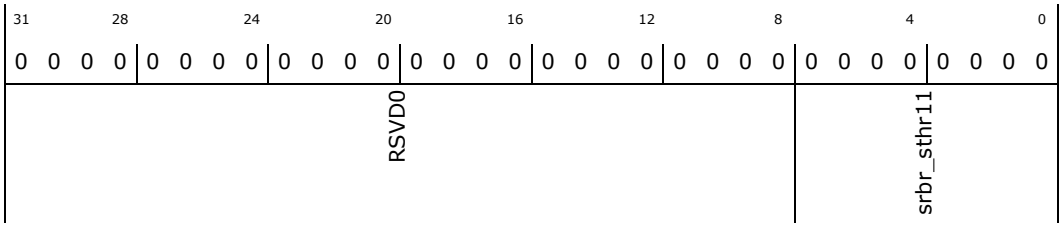
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr11:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.26.21 Shadow Receive Buffer Register and Shadow Transmit Holding Register 12 (SRBR_STHR12)—Offset 60h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 12

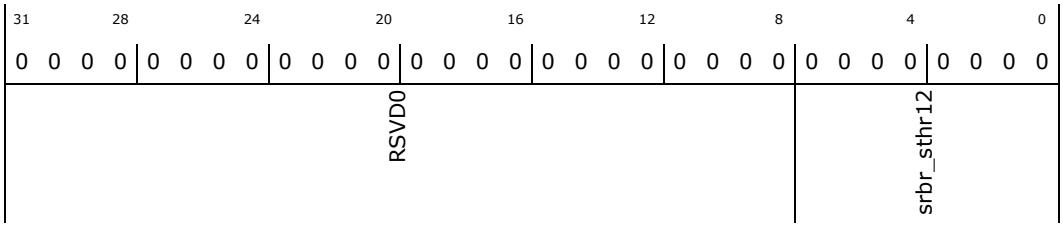
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr12:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.26.22 Shadow Receive Buffer Register and Shadow Transmit Holding Register 13 (SRBR_STHR13)—Offset 64h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 13

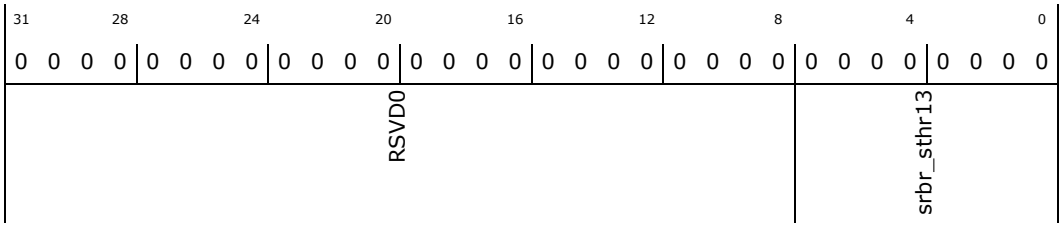
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr13:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.26.23 Shadow Receive Buffer Register and Shadow Transmit Holding Register 14 (SRBR_STHR14)—Offset 68h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 14

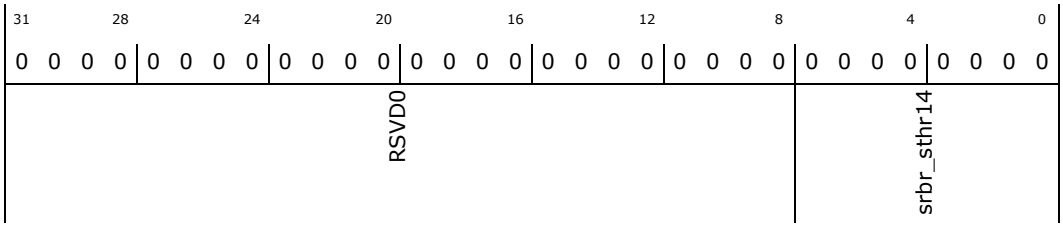
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr14:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.26.24 Shadow Receive Buffer Register and Shadow Transmit Holding Register 15 (SRBR_STHR15)—Offset 6Ch

Shadow Receive Buffer Register and Shadow Transmit Holding Register 15

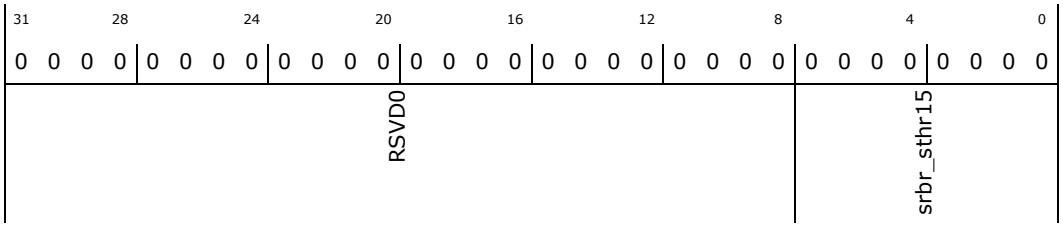
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr15:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.26.25 FIFO Access Register (FAR)—Offset 70h

FIFO Access Register

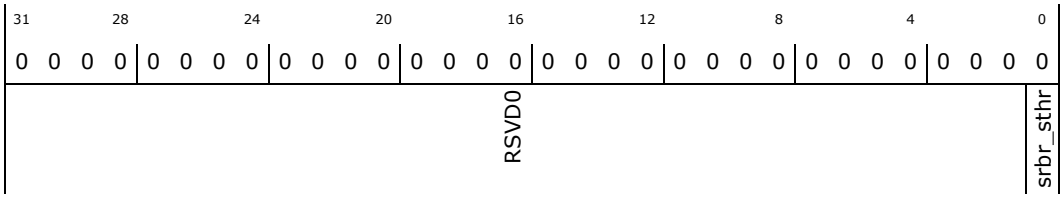
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RW	**srbr_sthr:** Writes have no effect when FIFO_ACCESS == No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. 0 = FIFO access mode disabled 1 = FIFO access mode enabled Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty. Reset Value: 0x0

9.26.26 Transmit FIFO Read (TFR)—Offset 74h

Transmit FIFO Read

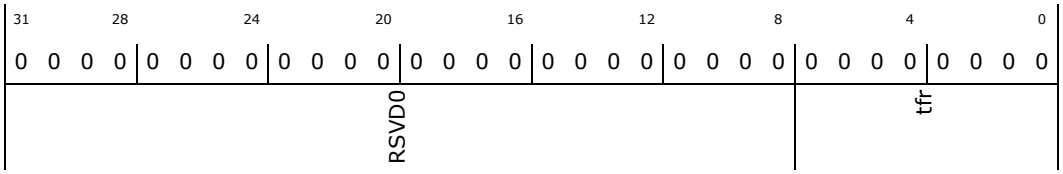
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7:0	0x0 RW	**tfr:** Transmit FIFO Read. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not implemented or not enabled, reading this register gives the data in the THR. Reset Value: 0x0

9.26.27 Receive FIFO Write (RFW)—Offset 78h

Receive FIFO Write

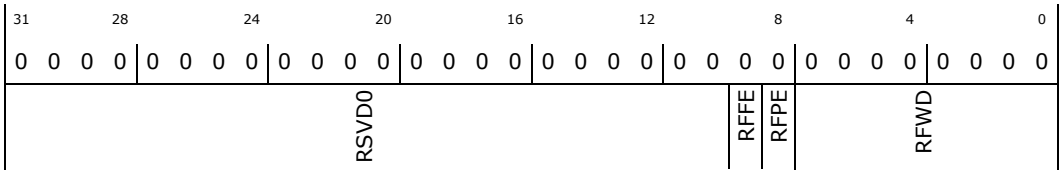
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RW	**RFFE:** Receive FIFO Framing Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR. Reset Value: 0x0
8	0x0 RW	**RFPE:** Receive FIFO Parity Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the RBR. Reset Value: 0x0
7:0	0x0 RW	**RFWD:** Receive FIFO Write Data. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR. Reset Value: 0x0

9.26.28 UART Status Register (USR)—Offset 7Ch

UART Status Register

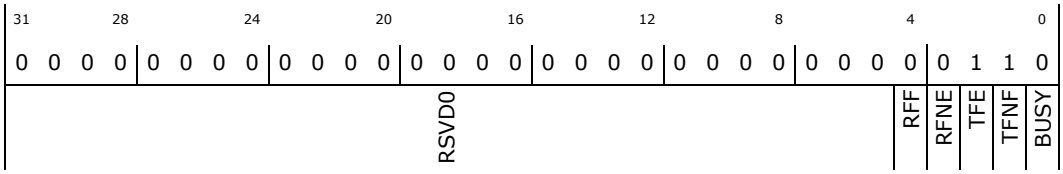
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000006h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RO	**RSVD0:** Reserved
4	0x0 RO	**RFF:** Receive FIFO Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. 0 = Receive FIFO not full 1 = Receive FIFO Full This bit is cleared when the RX FIFO is no longer full. Reset Value: 0x0
3	0x0 RO	**RFNE:** Receive FIFO Not Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. 0 = Receive FIFO is empty 1 = Receive FIFO is not empty This bit is cleared when the RX FIFO is empty. Reset Value: 0x0

Bit Range	Default & Access	Field Name (ID): Description
2	0x1 RO	**TFE:** Transmit FIFO Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. 0 = Transmit FIFO is not empty 1 = Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty. Reset Value: 0x1
1	0x1 RO	**TFNF:** Transmit FIFO Not Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO in not full. 0 = Transmit FIFO is full 1 = Transmit FIFO is not full This bit is cleared when the TX FIFO is full. Reset Value: 0x1
0	0x0 RO	**BUSY:** UART Busy. This bit is valid only when UART_16550_COMPATIBLE == NO and indicates that a serial transfer is in progress, ; when cleared, indicates that the DW_apb_uart is idle or inactive. 0 = DW_apb_uart is idle or inactive 1 = DW_apb_uart is busy (actively transferring data) NOTE: It is possible for the UART Busy bit to be cleared even though a new character may have been sent from another device. That is, if the DW_apb_uart has no data in THR and RBR and there is no transmission in progress and a start bit of a new character has just reached the DW_apb_uart. This is due to the fact that a valid start is not seen until the middle of the bit period and this duration is dependent on the baud divisor that has been programmed. If a second system clock has been implemented (CLOCK_MODE == Enabled), the assertion of this bit is also delayed by several cycles of the slower clock. Reset Value: 0x0

9.26.29 Transmit FIFO Level (TFL)—Offset 80h

Transmit FIFO Level

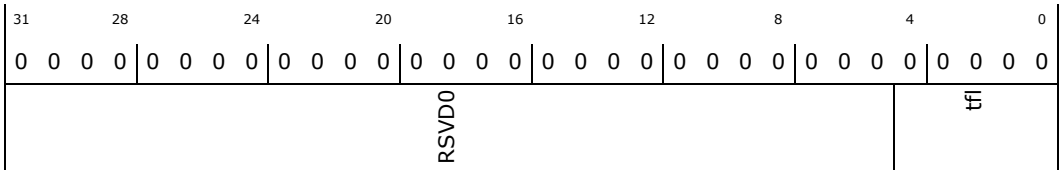
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RO	**RSVD0:** Reserved
4:0	0x0 RW	**tfl:** Transmit FIFO Level. This is indicates the number of data entries in the transmit FIFO. Reset Value: 0x0

9.26.30 Receive FIFO Level (RFL)—Offset 84h

Receive FIFO Level

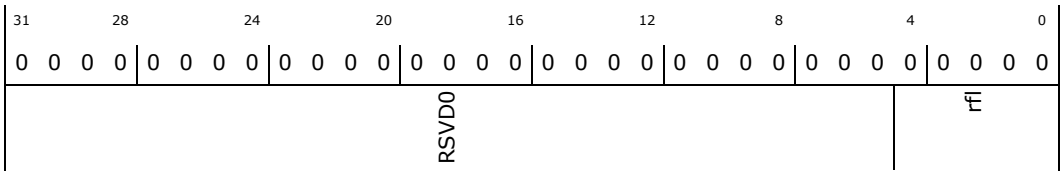
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RO	**RSVD0:** Reserved
4:0	0x0 RW	**rfl:** Receive FIFO Level. This is indicates the number of data entries in the receive FIFO. Reset Value: 0x0

9.26.31 Software Reset Register (SRR)—Offset 88h

Software Reset Register

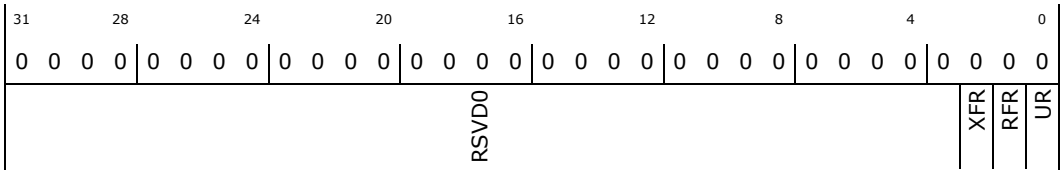
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**XFR:** XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0 Dependencies: Writes have no effect when FIFO_MODE == None.
1	0x0 RW	**RFR:** RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0 Dependencies: Writes have no effect when FIFO_MODE == None.
0	0x0 RW	**UR:** UART Reset. This asynchronously resets the DW_apb_uart and synchronously removes the reset assertion. For a two clock implementation both pclk and sclk domains are reset. Reset Value: 0x0

9.26.32 Shadow Request to Send (SRTS)—Offset 8Ch

Shadow Request to Send

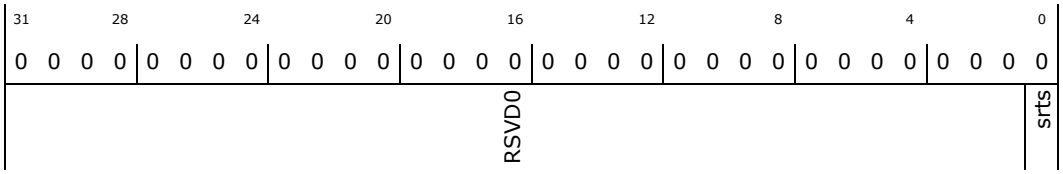
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**srts:** Shadow Request to Send. This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the DW_apb_uart is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input. Reset Value: 0x0

9.26.33 Shadow Break Control Register (SBCR)—Offset 90h

Shadow Break Control Bit. This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] = 1) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver. Reset Value: 0x0

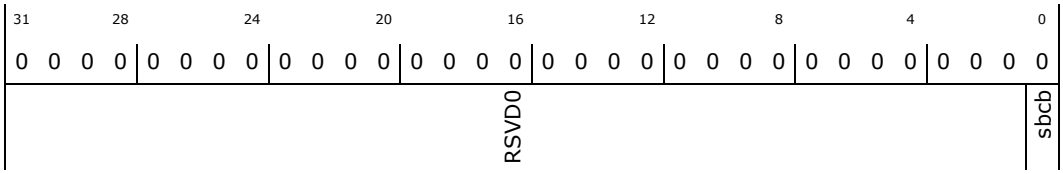
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RW	**sbcb:** Shadow Break Control Register

9.26.34 Shadow DMA Mode (SDMAM)—Offset 94h

Shadow DMA Mode

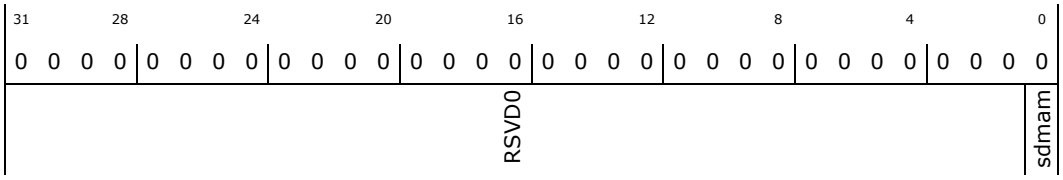
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RW	**sdmam:** Shadow DMA Mode. This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == NO). 0 = mode 0 1 = mode 1 Reset Value: 0x0

9.26.35 Shadow FIFO Enable (SFE)—Offset 98h

Shadow FIFO Enable

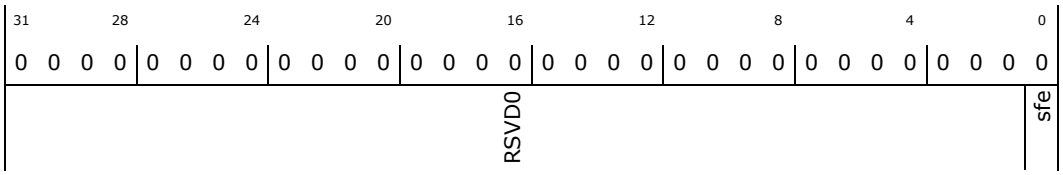
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**sfe:** Shadow FIFO Enable. This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated.This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset. Reset Value: 0x0

9.26.36 Shadow RCVR Trigger (SRT)—Offset 9Ch

Shadow RCVR Trigger

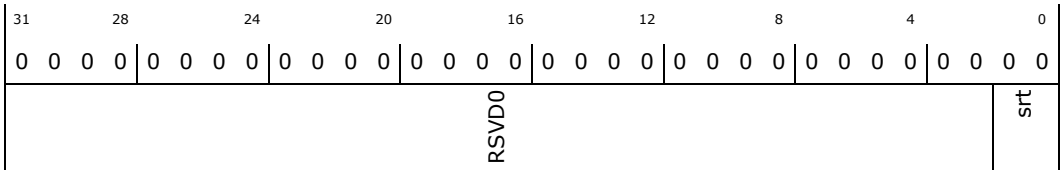
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RW	**srt:** Shadow RCVR Trigger. This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO full 10 = FIFO full 11 = FIFO 2 less than full Reset Value: 0x0

9.26.37 Shadow TX Empty Trigger (STET)—Offset A0h

Shadow TX Empty Trigger. This is a shadow register for the TX empty trigger bits (FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following

trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO full 11 = FIFO full Reset Value: 0x0 Dependencies: Writes have no effect when THRE_MODE_USER == Disabled.

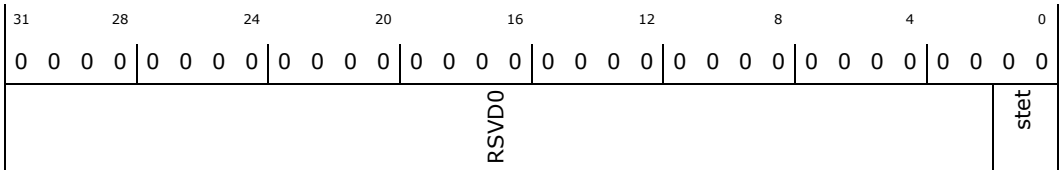
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RW	**stet:** Shadow TX Empty Trigger

9.26.38 Halt TX (HTX)—Offset A4h

Halt TX

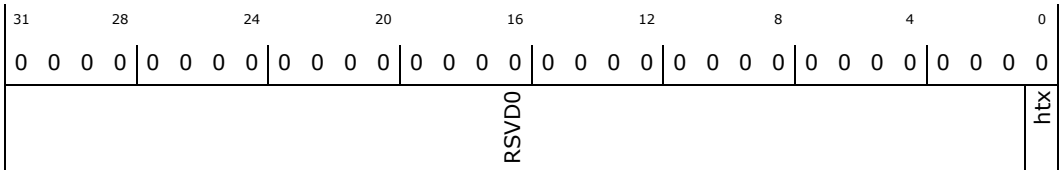
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**htx:** This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 = Halt TX disabled 1 = Halt TX enabled Note, if FIFOs are implemented and not enabled, the setting of the halt TX register has no effect on operation. Reset Value: 0x0 Dependencies: Writes have no effect when FIFO_MODE == None.

9.26.39 DMA Software Acknowledge (DMASA)—Offset A8h

DMA Software Acknowledge

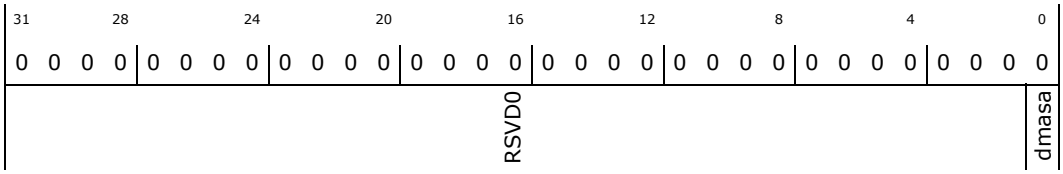
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RW	**dmasa:** This register is use to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This causes the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0 Dependencies: Writes have no effect when DMA_EXTRA == No.

9.26.40 Component Parameter Register (CPR)—Offset F4h

Component Parameter Register

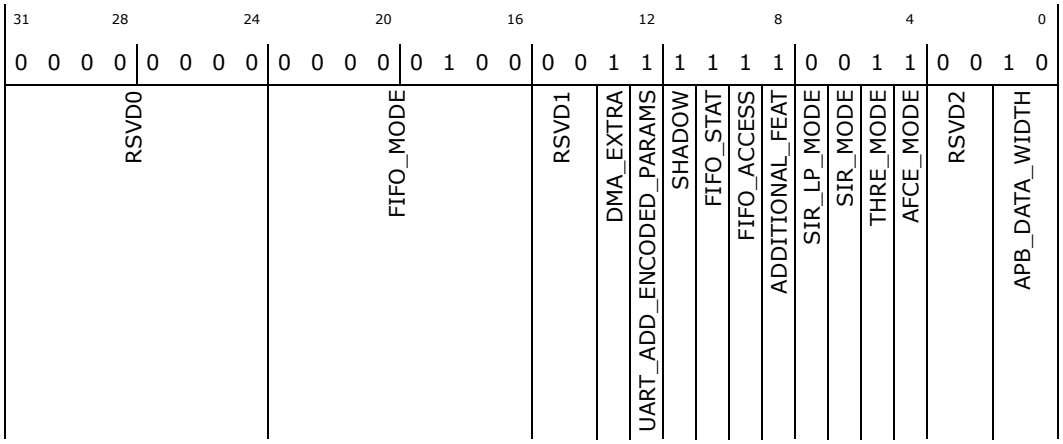
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00043F32h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD0:** Reserved
23:16	0x4 RO	**FIFO_MODE:** 0x00 = 0 0x01 = 16 0x02 = 32 to 0x80 = 2048 0x81- 0xff = reserved
15:14	0x0 RO	**RSVD1:** Reserved
13	0x1 RO	**DMA_EXTRA:** 0 = FALSE, 1 = TRUE
12	0x1 RO	**UART_ADD_ENCODED_PARAMS:** 0 = FALSE, 1 = TRUE
11	0x1 RO	**SHADOW:** 0 = FALSE, 1 = TRUE
10	0x1 RO	**FIFO_STAT:** 0 = FALSE, 1 = TRUE
9	0x1 RO	**FIFO_ACCESS:** 0 = FALSE, 1 = TRUE
8	0x1 RO	**ADDITIONAL_FEAT:** 0 = FALSE, 1 = TRUE
7	0x0 RO	**SIR_LP_MODE:** 0 = FALSE, 1 = TRUE
6	0x0 RO	**SIR_MODE:** 0 = FALSE, 1 = TRUE
5	0x1 RO	**THRE_MODE:** 0 = FALSE, 1 = TRUE
4	0x1 RO	**AFCE_MODE:** 0 = FALSE, 1 = TRUE
3:2	0x0 RO	**RSVD2:** Reserved
1:0	0x2 RO	**APB_DATA_WIDTH:** 00 = 8 bits 01 = 16 bits 10 = 32 bits 11 = reserved

9.26.41 UART Component Version (UCV)—Offset F8h

UART Component Version

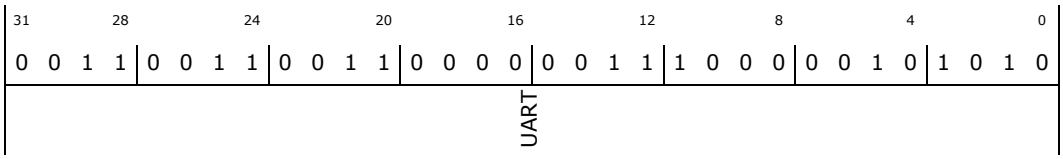
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 3330382Ah



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x3330382a RO	**UART:** ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01* Reset Value: See the releases table in the AMBA 2 release notes.

9.26.42 Component Type Register (CTR)—Offset FCh

Component Type Register

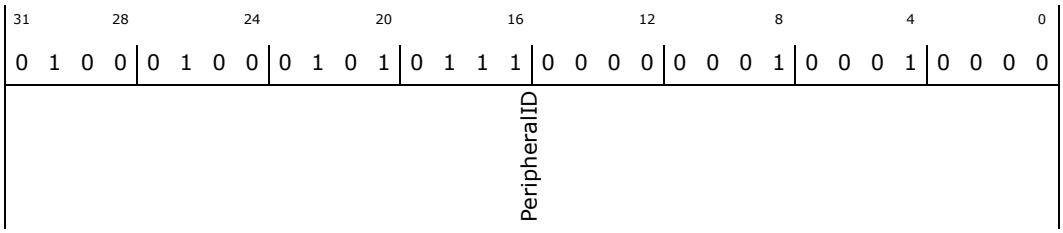
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 44570110h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x44570110 RO	**PeripheralID:** This register contains the peripherals identification code. Reset Value: 0x44570110

9.26.43 private clock params (PRV_CLOCK_PARAMS)—Offset 800h

private clock params

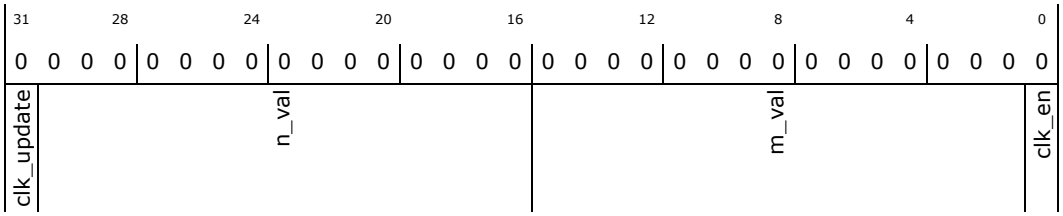
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**clk_update:** update the clock divider after seeting new m and n values
30:16	0x0 RW	**N_VAL (n_val):** n value for the m over n divider
15:1	0x0 RW	**M_VAL (m_val):** m value for the m over n divider
0	0x0 RW	**clk_en:** clk en of the m over n divider

9.26.44 software reset (RESETS)—Offset 804h

software reset

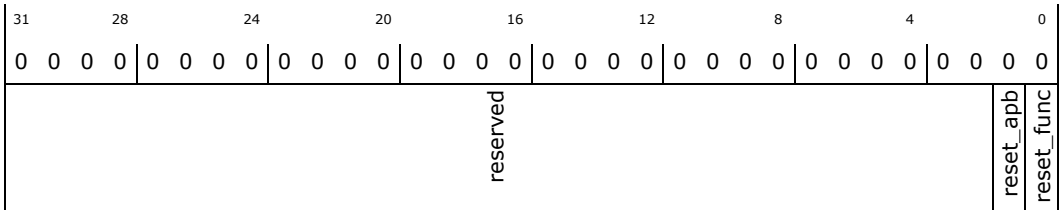
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (reserved):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**reset_apb:** reset the apb domain
0	0x0 RW	**reset_func:** reset the func clock domain

9.26.45 General purpose register (GENERAL)—Offset 808h

General purpose register

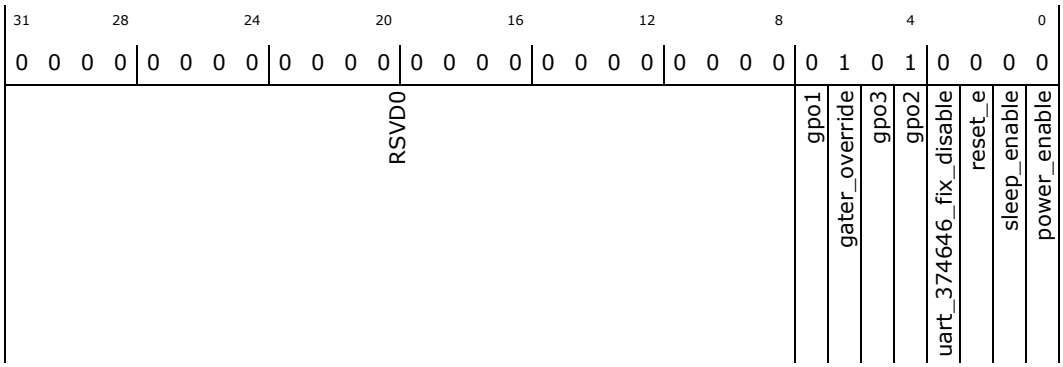
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000050h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7	0x0 RW	**gpo1:** not applicable
6	0x1 RW	**gater_override:** not applicable
5	0x0 RW	**gpo3:** not applicable
4	0x1 RW	**gpo2:** this bit select if the uart clock req will be dynamic or control by the uart clock en: 1 - control by the clk en, 0 - dynamic. Default value - 1
3	0x0 RW	**uart_374646_fix_disable:** Disable rts_n override
2	0x0 RW	**reset_e:** not applicable
1	0x0 RW	**sleep_enable:** not applicable

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**power_enable:** not applicable

9.26.46 Transaction counter (UART_BYTE_COUNT)—Offset 818h

Transaction counter

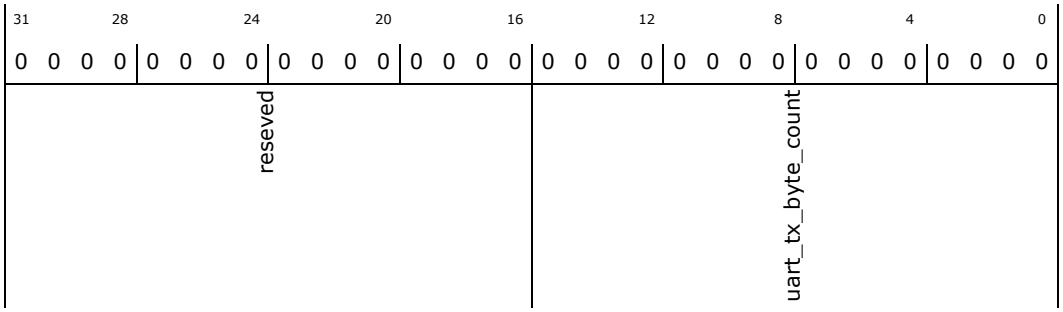
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**reserved (reseved):** reserved
15:0	0x0 RO	**uart_tx_byte_count:** UART transaction counter

9.26.47 Overflow interrupt (UART_OVERFLOW_INTR_STAT)—Offset 820h

Overflow interrupt

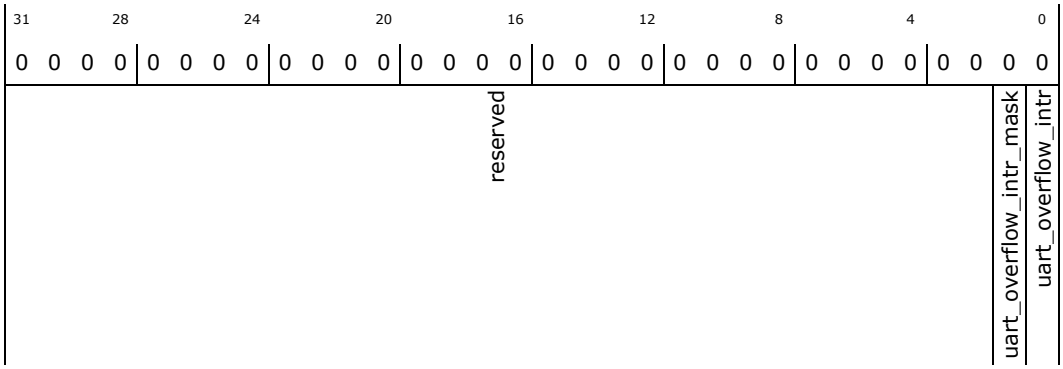
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

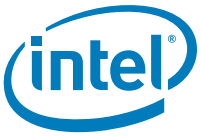
Offset: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**reserved:** reserved
1	0x0 RW	**uart1_overflow_intr_mask (uart_overflow_intr_mask):** Mask the overflow intr
0	0x0 RO	**uart_overflow_intr:** Indicate there was count overflow



9.27 SIO HSUART 1 PCI Configuration Registers

Table 90. Summary of SIO HSUART 1 PCI Configuration Registers—0/30/4

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4719	00008086h
4–7h	4	"STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h" on page 4719	00100000h
8–Bh	4	"REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4721	00000000h
C–Fh	4	"CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4722	00800000h
10–13h	4	"BAR -Base Address Register (BAR)—Offset 10h" on page 4722	00000000h
14–17h	4	"BAR1 -Base Address Register1 (BAR1)—Offset 14h" on page 4723	00000000h
2C–2Fh	4	"SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4724	00000000h
30–33h	4	"EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4725	00000000h
34–37h	4	"CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4725	00000000h
3C–3Fh	4	"INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4726	00000100h
80–83h	4	"POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4726	00030001h
84–87h	4	"PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4727	00000008h
F8–FBh	4	"Manufacturers ID (MANID)—Offset F8h" on page 4728	00000000h

9.27.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

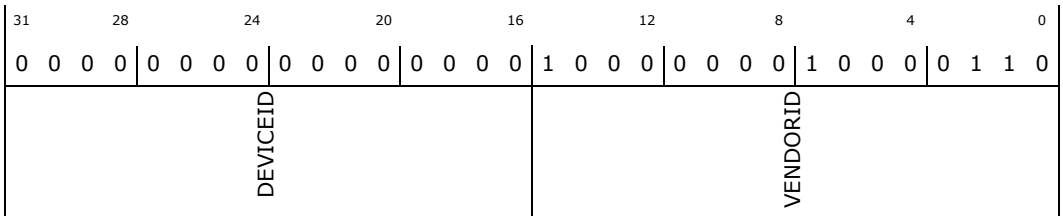
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**DEVICEID:** Device ID identifies the particular AHB/APB device. This is tied to a strap at the top level. Because of tool issues, the HTML files show this field as 0, but the following are the POR values for SoC: LPIO1 DMA: 0x2286 LPIO1 PWM1: 0x2288 LPIO1 PWM2: 0x2289 LPIO1 HSUART1: 0x228A LPIO1 HSUART2: 0x228C LPIO1 SPI1: 0x228E LPIO1 SPI2: 0x2290 LPIO1 SPI3: 0x22AC LPIO2 DMA: 0x22C0 LPIO2 I2C1: 0x22C1 LPIO2 I2C2: 0x22C2 LPIO2 I2C3: 0x22C3 LPIO2 I2C4: 0x22C4 LPIO2 I2C5: 0x22C5 LPIO2 I2C6: 0x22C6 LPIO2 I2C7: 0x22C7 For the final word on this, please see Ray Ng's SoC RevID and DevID HAS on Infofactory: https://ifcollaborate.intel.com/IFC/getdoc.aspx?docbase=InfoFactoryKBandchronid=09005ffd80e84b43andver=CURRENTandqepop=false
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap the top level.

9.27.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

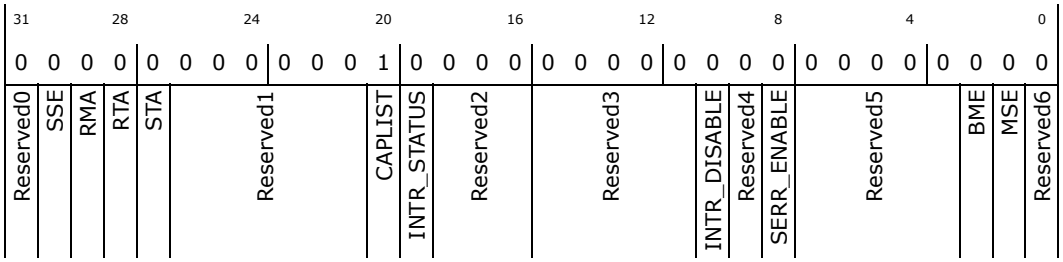
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved0:** Reserved
30	0x0 RW/1C	**SSE:** This bit is set when a device sends an DO_SERR message, and the SERR# Enable bit in the Command register is 1
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric PortReceived Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27	0x0 RW/1C	**STA:** The Bridge sets this bit whenever it responds to a transaction with CA abort. If the SERR# Enable bit is set, the Bridge sets the Signaled System Error bit and sends an DO_SERR message on the IOSF Sideband.
26:21	0x0 RO	**Reserved1:** Reserved
20	0x1 RO	**CAPLIST:** Capabilities List: Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt .i.e Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.. Reset value of this bit is 0.
9	0x0 RO	**Reserved4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: If both SERR# Enable and the Unsupported Request Reporting Enable (URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0x0 RO	**Reserved6:** Reserved

9.27.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

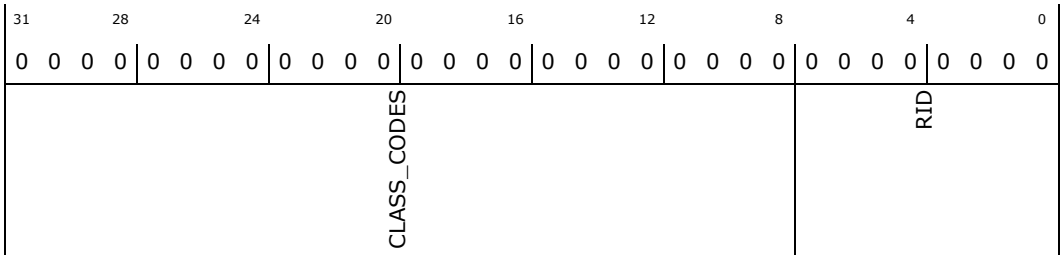
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

9.27.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

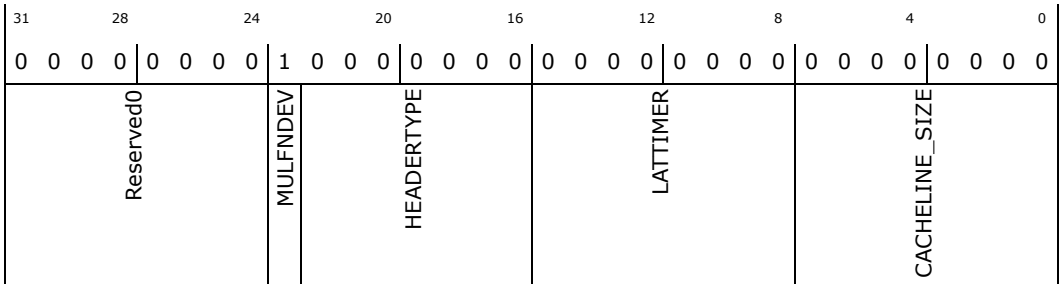
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + Ch

Default: 00800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x1 RO	**MULFNDEV:** Multi Function Device: This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. Value of 1 indicates multifunction device value of 0 indicates single function device
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	0x0 RO	**LATTIMER:** Latency Timer: Doesn.t apply to PCI Express. Hardwired to 00h.
7:0	0x0 RW	**CACHELINE_SIZE:** Cache Line Size: Doesn.t apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

9.27.5 BAR -Base Address Register (BAR)—Offset 10h

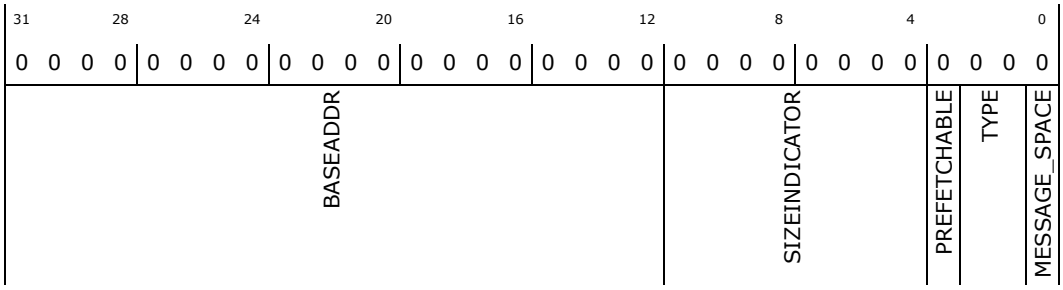
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the AHB device memory space. Taken from Strap values as 1's. Please note that for DMA this field goes from [31:14], or 16kbyte, and the SIZEINDICATOR field goes from [13:4].
11:4	0x0 RO	**SIZEINDICATOR:** Size Indicator Read Only: Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0x0 RO	**TYPE:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.27.6 BAR1 -Base Address Register1 (BAR1)—Offset 14h

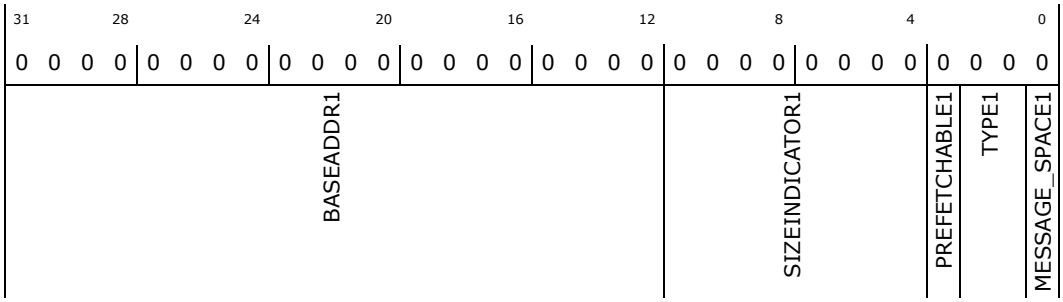
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	0x0 RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not
2:1	0x0 RO	**TYPE1:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.27.7 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

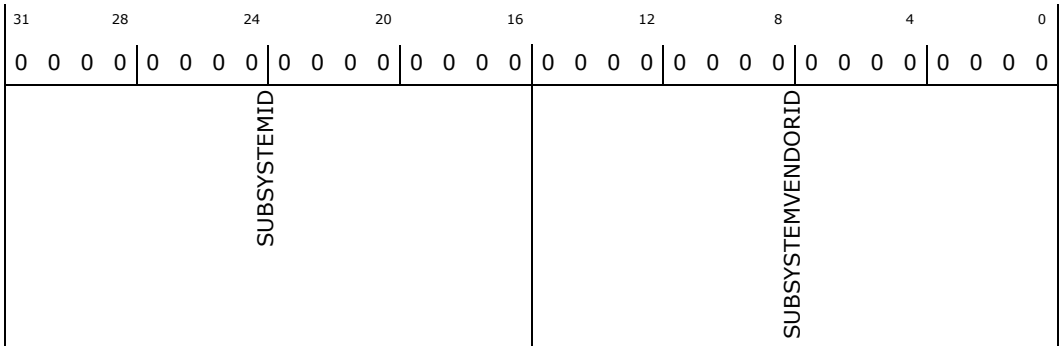
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

9.27.8 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

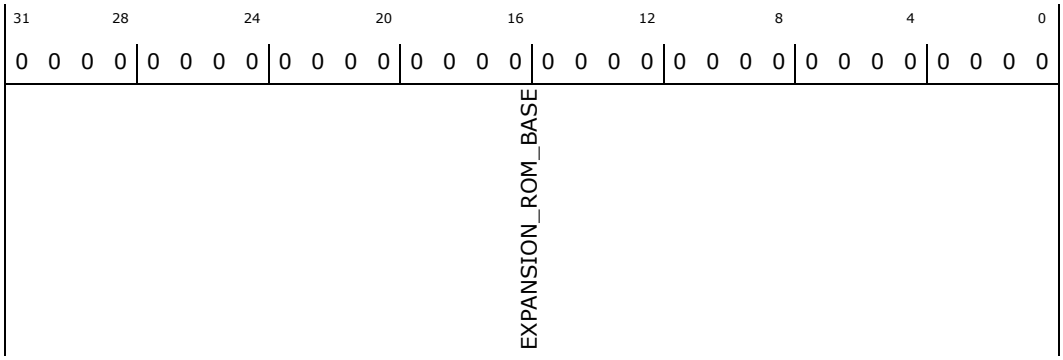
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** A value of all zeros indicates no support for expansion ROM.

9.27.9 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

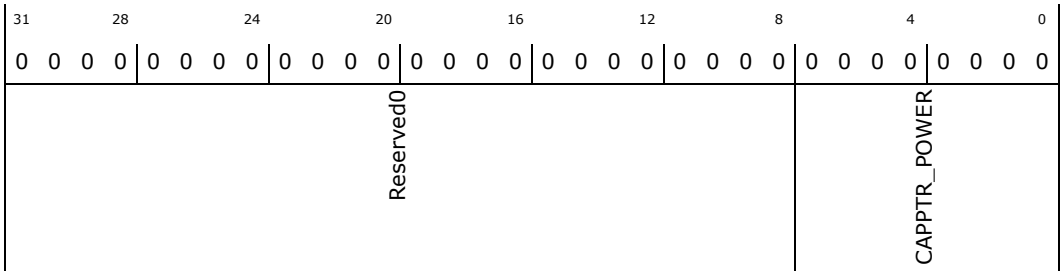
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x0 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

9.27.10 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

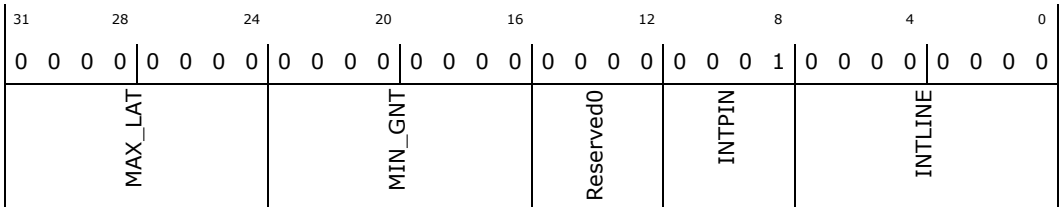
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

9.27.11 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

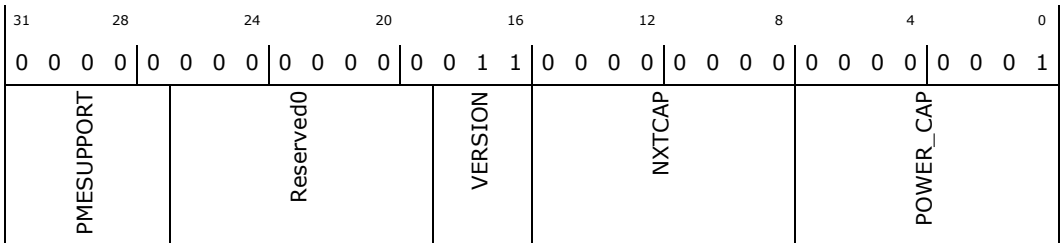
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** PME_Support - This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

9.27.12 PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

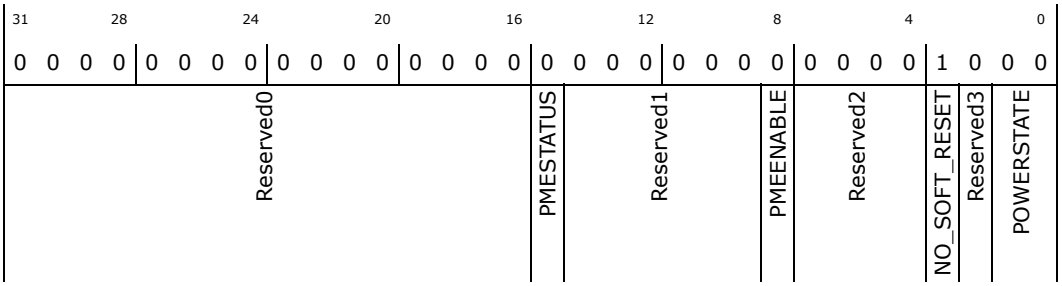
PMECTRLSTATUS - PME Control and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

9.27.13 Manufacturers ID (MANID)—Offset F8h

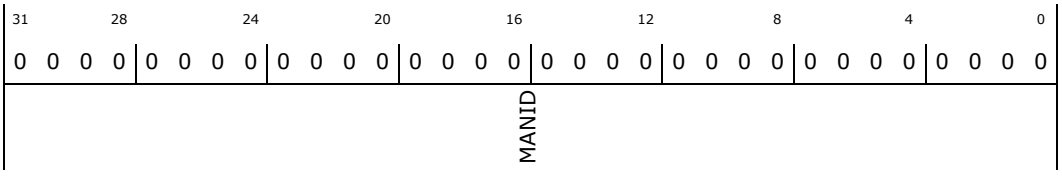
Manufacturers ID

Access Method

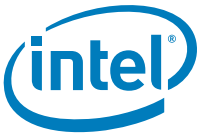
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:4] + F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: This register is brought out as straps to the top level.



9.28 SIO HSUART 1 Memory Mapped I/O Registers

Table 91. Summary of SIO HSUART 0 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Receive Buffer Register/ Transmit Holding Register/ Divisor Latch (Low) (RBR_THR_DLL)—Offset 0h" on page 4732	00000000h
4–7h	4	"Divisor Latch (High)/ Interrupt Enable Register (IER_DLH)—Offset 4h" on page 4732	00000000h
8–Bh	4	"Interrupt Identification Register and FIFO Control Register (IIR_FCR)—Offset 8h" on page 4733	00000001h
C–Fh	4	"Line Control Register (LCR)—Offset Ch" on page 4734	00000000h
10–13h	4	"Modem Control Register (MCR)—Offset 10h" on page 4736	00000000h
14–17h	4	"Line Status Register (LSR)—Offset 14h" on page 4737	00000060h
18–1Bh	4	"Modem Status Register (MSR)—Offset 18h" on page 4739	00000000h
1C–1Fh	4	"Scratchpad Register (SCR)—Offset 1Ch" on page 4740	00000000h
30–33h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 0 (SRBR_STHR0)—Offset 30h" on page 4741	00000000h
34–37h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 1 (SRBR_STHR1)—Offset 34h" on page 4742	00000000h
38–3Bh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 2 (SRBR_STHR2)—Offset 38h" on page 4743	00000000h
3C–3Fh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 3 (SRBR_STHR3)—Offset 3Ch" on page 4744	00000000h
40–43h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 4 (SRBR_STHR4)—Offset 40h" on page 4745	00000000h
44–47h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 5 (SRBR_STHR5)—Offset 44h" on page 4746	00000000h
48–4Bh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 6 (SRBR_STHR6)—Offset 48h" on page 4747	00000000h
4C–4Fh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 7 (SRBR_STHR7)—Offset 4Ch" on page 4748	00000000h
50–53h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 8 (SRBR_STHR8)—Offset 50h" on page 4749	00000000h
54–57h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 9 (SRBR_STHR9)—Offset 54h" on page 4750	00000000h
58–5Bh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 10 (SRBR_STHR10)—Offset 58h" on page 4751	00000000h
5C–5Fh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 11 (SRBR_STHR11)—Offset 5Ch" on page 4752	00000000h
60–63h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 12 (SRBR_STHR12)—Offset 60h" on page 4753	00000000h
64–67h	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 13 (SRBR_STHR13)—Offset 64h" on page 4754	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
68–6Bh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 14 (SRBR_STHR14)—Offset 68h" on page 4755	00000000h
6C–6Fh	4	"Shadow Receive Buffer Register and Shadow Transmit Holding Register 15 (SRBR_STHR15)—Offset 6Ch" on page 4756	00000000h
70–73h	4	"FIFO Access Register (FAR)—Offset 70h" on page 4757	00000000h
74–77h	4	"Transmit FIFO Read (TFR)—Offset 74h" on page 4757	00000000h
78–7Bh	4	"Receive FIFO Write (RFW)—Offset 78h" on page 4758	00000000h
7C–7Fh	4	"UART Status Register (USR)—Offset 7Ch" on page 4759	00000006h
80–83h	4	"Transmit FIFO Level (TFL)—Offset 80h" on page 4760	00000000h
84–87h	4	"Receive FIFO Level (RFL)—Offset 84h" on page 4761	00000000h
88–8Bh	4	"Software Reset Register (SRR)—Offset 88h" on page 4761	00000000h
8C–8Fh	4	"Shadow Request to Send (SRTS)—Offset 8Ch" on page 4762	00000000h
90–93h	4	"Shadow Break Control Register (SBCR)—Offset 90h" on page 4763	00000000h
94–97h	4	"Shadow DMA Mode (SDMAM)—Offset 94h" on page 4763	00000000h
98–9Bh	4	"Shadow FIFO Enable (SFE)—Offset 98h" on page 4764	00000000h
9C–9Fh	4	"Shadow Request to Send (SRTS)—Offset 8Ch" on page 4762	00000000h
A0–A3h	4	"Shadow TX Empty Trigger (STET)—Offset A0h" on page 4765	00000000h
A4–A7h	4	"Halt TX (HTX)—Offset A4h" on page 4766	00000000h
A8–ABh	4	"DMA Software Acknowledge (DMASA)—Offset A8h" on page 4767	00000000h
F4–F7h	4	"Component Parameter Register (CPR)—Offset F4h" on page 4767	00043F32h
F8–FBh	4	"UART Component Version (UCV)—Offset F8h" on page 4769	3330382Ah
FC–FFh	4	"Component Type Register (CTR)—Offset FCh" on page 4769	44570110h
800–803h	4	"private clock params (PRV_CLOCK_PARAMS)—Offset 800h" on page 4769	00000000h
804–807h	4	"software reset (RESETS)—Offset 804h" on page 4770	00000000h
808–80Bh	4	"General purpose register (GENERAL)—Offset 808h" on page 4771	00000050h
818–81Bh	4	"Transaction counter (UART_BYTE_COUNT)—Offset 818h" on page 4772	00000000h
820–823h	4	"Overflow interrupt (UART_OVERFLOW_INTR_STAT)—Offset 820h" on page 4772	00000000h

9.28.1 Receive Buffer Register/ Transmit Holding Register/ Divisor Latch (Low) (RBR_THR_DLL)—Offset 0h

Receive Buffer Register/ Transmit Holding Register/ Divisor Latch (Low)

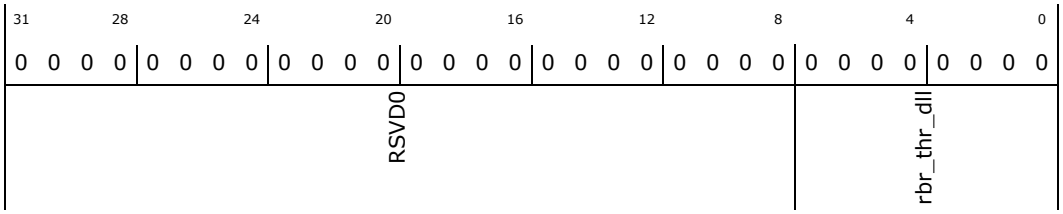
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7:0	0x0 RW	**rbr_thr_dll:** Can be referred to 3 registers with different descriptions- go to Synopsys DesignWare DW_apb_uart Databook Spec in order to learn more

9.28.2 Divisor Latch (High)/ Interrupt Enable Register (IER_DLH)—Offset 4h

Divisor Latch (High)/ Interrupt Enable Register

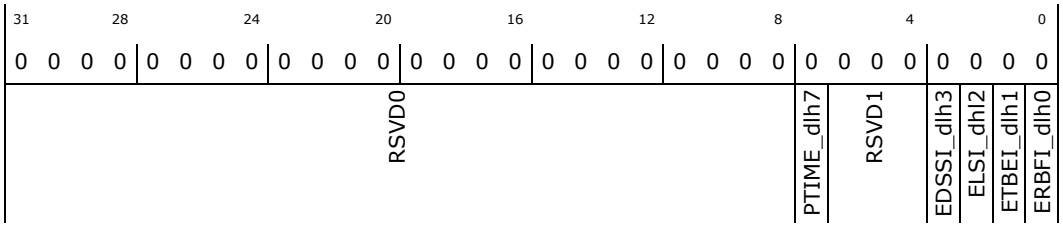
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7	0x0 RW	**PTIME_dlh7:** Can be referred to 2 registers with different descriptions- go to Synopsys DesignWare DW_apb_uart Databook Spec in order to learn more
6:4	0x0 RO	**RSVD1:** Reserved
3	0x0 RW	**EDSSI_dlh3:** Can be referred to 2 registers with different descriptions- go to Synopsys DesignWare DW_apb_uart Databook Spec in order to learn more
2	0x0 RW	**ELSI_dhl2:** Can be referred to 2 registers with different descriptions- go to Synopsys DesignWare DW_apb_uart Databook Spec in order to learn more
1	0x0 RW	**ETBEI_dlh1:** Can be referred to 2 registers with different descriptions- go to Synopsys DesignWare DW_apb_uart Databook Spec in order to learn more
0	0x0 RW	**ERBFI_dlh0:** Can be referred to 2 registers with different descriptions- go to Synopsys DesignWare DW_apb_uart Databook Spec in order to learn more

9.28.3 Interrupt Identification Register and FIFO Control Register (IIR_FCR)—Offset 8h

Interrupt Identification Register and FIFO Control Register

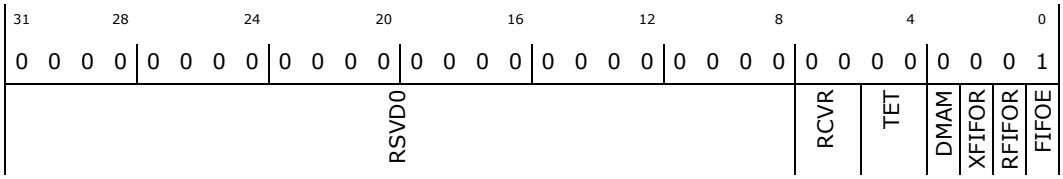
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7:6	0x0 RW	**FIFOSE_RCVR (RCVR):** RCVR Trigger. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. For details on DMA support, refer to DMA Support on page 43. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO full 10 = FIFO full 11 = FIFO 2 less than full Reset Value: 0x0

Bit Range	Default & Access	Field Name (ID): Description
5:4	0x0 RW	**Res_TET (TET):** TX Empty Trigger. Writes have no effect when THRE_MODE_USER == Disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. For details on DMA support, refer to DMA Support on page 43. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO full 11 = FIFO full Reset Value: 0x0
3	0x0 RW	**IID3_DMAM (DMAM):** DMA Mode. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == No). For details on DMA support, refer to DMA Support on page 43. 0 = mode 0 1 = mode 1 Reset Value: 0x0
2	0x0 RW	**IID2_XFIFOR (XFIFOR):** XMIT FIFO Reset. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0
1	0x0 RW	**IID1_RFIFOR (RFIFOR):** RCVR FIFO Reset. This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0
0	0x1 RW	**IID0_FIFOE (FIFOE):** FIFO Enable. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset. Reset Value: 0x0

9.28.4 Line Control Register (LCR)—Offset Ch

Line Control Register

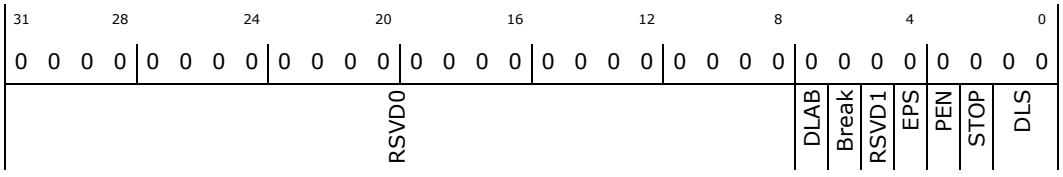
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



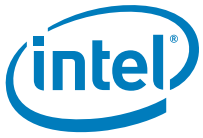
Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW	**DLAB:** Divisor Latch Access Bit. If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. Reset Value: 0x0
6	0x0 RW	**Break:** Break Control Bit.This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low. Reset Value: 0x0
5	0x0 RO	**RSVD1:** Reserved
4	0x0 RW	**EPS:** Even Parity Select. If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked. Reset Value: 0x0
3	0x0 RW	**PEN:** Parity Enable. If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0 = parity disabled 1 = parity enabled Reset Value: 0x0
2	0x0 RW	**STOP:** Number of stop bits. If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0 = 1 stop bit 1 = 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit Reset Value: 0x0
1:0	0x0 RW	**DLS:** Data Length Select. If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits Reset Value: 0x0

9.28.5 Modem Control Register (MCR)—Offset 10h

Modem Control Register

Access Method

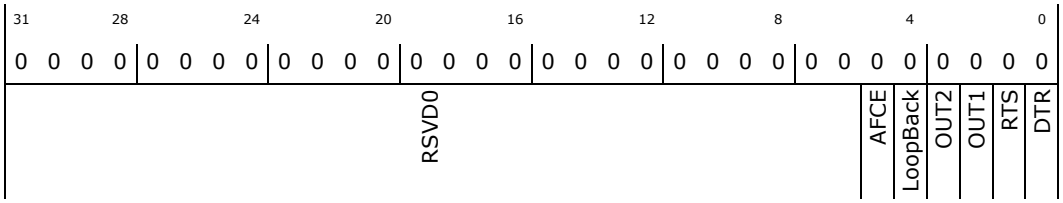


Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 10h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**RSVD0:** Reserved
5	0x0 RW	**AFCE:** Auto Flow Control Enable. Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled as described in Auto Flow Control on page 37. 0 = Auto Flow Control Mode disabled 1 = Auto Flow Control Mode enabled Reset Value: 0x0
4	0x0 RW	**LoopBack:** LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line. Reset Value: 0x0
3	0x0 RW	**OUT2:** OUT2. This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: 0 = out2_n de-asserted (logic 1) 1 = out2_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0
2	0x0 RW	**OUT1:** OUT1. This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n, that is: 0 = out1_n de-asserted (logic 1) 1 = out1_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**RTS:** Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0
0	0x0 RW	**DTR:** Data Terminal Ready. This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is: 0 = dtr_n de-asserted (logic 1) 1 = dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input. Reset Value: 0x0

9.28.6 Line Status Register (LSR)—Offset 14h

Line Status Register

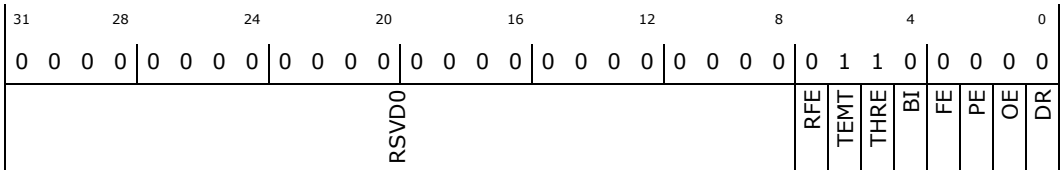
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

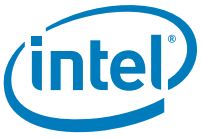
Offset: [BAR] + 14h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000060h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7	0x0 RO	**RFE:** Receiver FIFO Error bit. This bit is only relevant when FIFO_MODE != NONE AND FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. 0 = no error in RX FIFO 1 = error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO. Reset Value: 0x0



Bit Range	Default & Access	Field Name (ID): Description
6	0x1 RO	**TEMT:** Transmitter Empty bit. If in FIFO mode (FIFO_MODE != NONE) and FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty. Reset Value: 0x1
5	0x1 RO	**THRE:** Transmit Holding Register Empty bit. If THRE_MODE_USER == Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting. For more details, see Programmable THRE Interrupt on page 40. Reset Value: 0x1
4	0x0 RO	**BI:** Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read. Reset Value: 0x0
3	0x0 RO	**FE:** Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no framing error 1 = framing error Reading the LSR clears the FE bit. Reset Value: 0x0
2	0x0 RO	**PE:** Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no parity error 1 = parity error Reading the LSR clears the PE bit. Reset Value: 0x0

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RO	**OE:** Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0 = no overrun error 1 = overrun error Reading the LSR clears the OE bit. Reset Value: 0x0
0	0x0 RO	**DR:** Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0 = no data ready 1 = data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode. Reset Value: 0x0

9.28.7 Modem Status Register (MSR)—Offset 18h

Modem Status Register

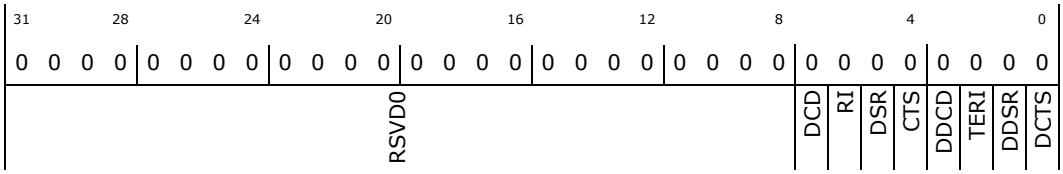
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 18h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7	0x0 RO	**DCD:** Data Carrier Detect. This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0 = dcd_n input is de-asserted (logic 1) 1 = dcd_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2). Reset Value: 0x0
6	0x0 RO	**RI:** Ring Indicator. This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0 = ri_n input is de-asserted (logic 1) 1 = ri_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1). Reset Value: 0x0

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RO	**DSR:** Data Set Ready. This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. 0 = dsr_n input is de-asserted (logic 1) 1 = dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR). Reset Value: 0x0
4	0x0 RO	**CTS:** Clear to Send. This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. 0 = cts_n input is de-asserted (logic 1) 1 = cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS). Reset Value: 0x0
3	0x0 RO	**DDCD:** Delta Data Carrier Detect. This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0 = no change on dcd_n since last read of MSR 1 = change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] = 1), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted. Reset Value: 0x0
2	0x0 RO	**TERI:** Trailing Edge of Ring Indicator. This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 0 = no change on ri_n since last read of MSR 1 = change on ri_n since last read of MSR Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] = 1), TERI reflects when MCR[2] (Out1) has changed state from a high to a low. Reset Value: 0x0
1	0x0 RO	**DDSR:** Delta Data Set Ready. This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0 = no change on dsr_n since last read of MSR 1 = change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted. Reset Value: 0x0
0	0x0 RO	**DCTS:** Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0 = no change on cts_n since last read of MSR 1 = change on cts_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted. Reset Value: 0x0

9.28.8 Scratchpad Register (SCR)—Offset 1Ch

Scratchpad Register

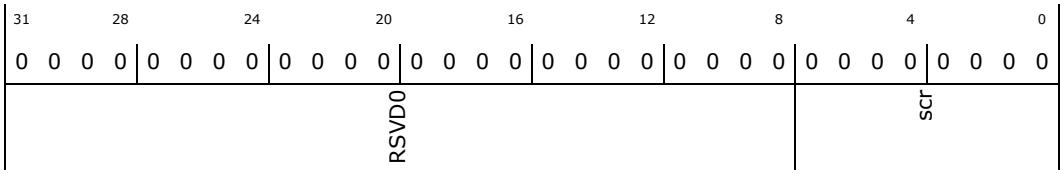
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 1Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7:0	0x0 RW	**scr:** This register is for programmers to use as a temporary storage space. It has no defined purpose in the DW_apb_uart. Reset Value: 0x0

9.28.9 Shadow Receive Buffer Register and Shadow Transmit Holding Register 0 (SRBR_STHR0)—Offset 30h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 0

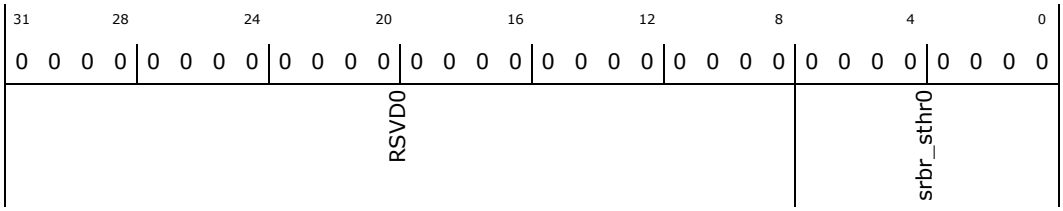
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 30h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr0:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.28.10 Shadow Receive Buffer Register and Shadow Transmit Holding Register 1 (SRBR_STHR1)—Offset 34h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 1

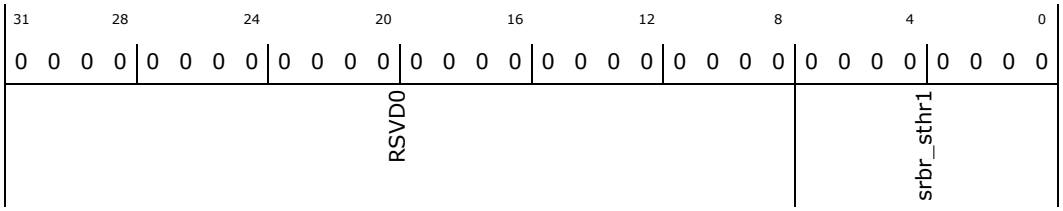
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 34h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr1:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.28.11 Shadow Receive Buffer Register and Shadow Transmit Holding Register 2 (SRBR_STHR2)—Offset 38h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 2

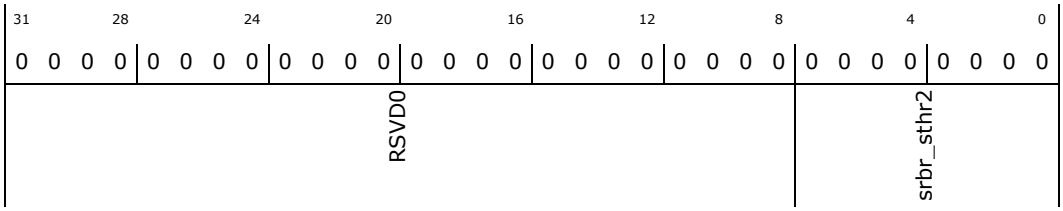
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 38h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr2:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.28.12 Shadow Receive Buffer Register and Shadow Transmit Holding Register 3 (SRBR_STHR3)—Offset 3Ch

Shadow Receive Buffer Register and Shadow Transmit Holding Register 3

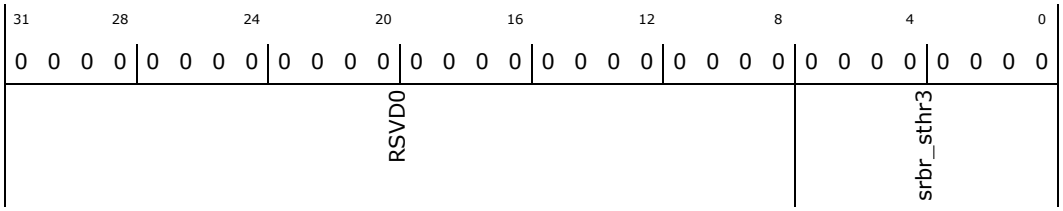
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 3Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr3:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.28.13 Shadow Receive Buffer Register and Shadow Transmit Holding Register 4 (SRBR_STHR4)—Offset 40h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 4

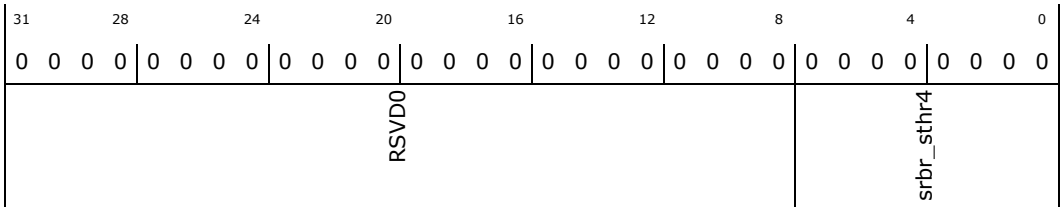
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 40h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr4:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.28.14 Shadow Receive Buffer Register and Shadow Transmit Holding Register 5 (SRBR_STHR5)—Offset 44h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 5

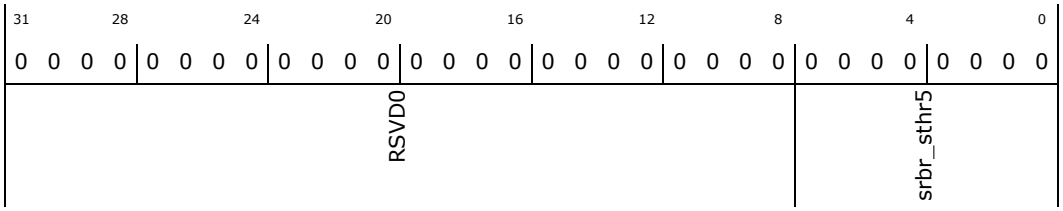
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 44h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr5:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.28.15 Shadow Receive Buffer Register and Shadow Transmit Holding Register 6 (SRBR_STHR6)—Offset 48h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 6

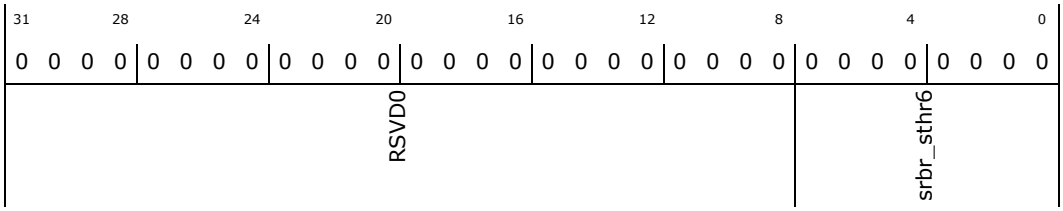
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 48h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr6:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.28.16 Shadow Receive Buffer Register and Shadow Transmit Holding Register 7 (SRBR_STHR7)—Offset 4Ch

Shadow Receive Buffer Register and Shadow Transmit Holding Register 7

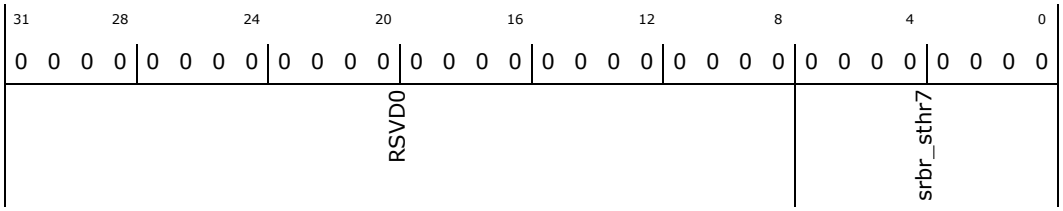
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 4Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr7:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.28.17 Shadow Receive Buffer Register and Shadow Transmit Holding Register 8 (SRBR_STHR8)—Offset 50h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 8

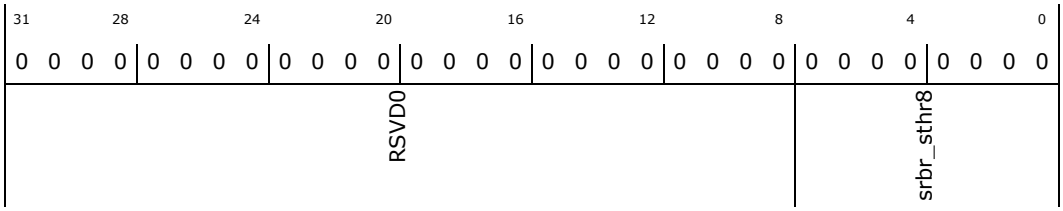
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 50h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr8:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.28.18 Shadow Receive Buffer Register and Shadow Transmit Holding Register 9 (SRBR_STHR9)—Offset 54h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 9

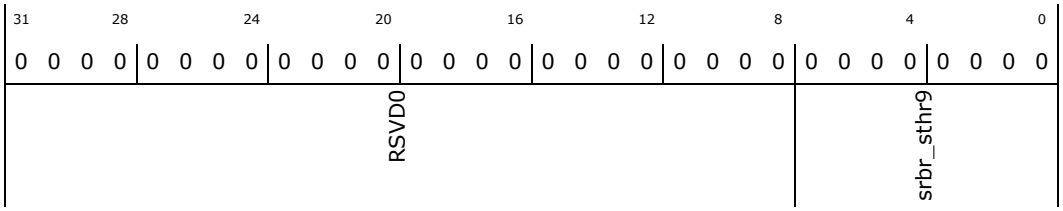
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 54h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr9:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.28.19 Shadow Receive Buffer Register and Shadow Transmit Holding Register 10 (SRBR_STHR10)—Offset 58h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 10

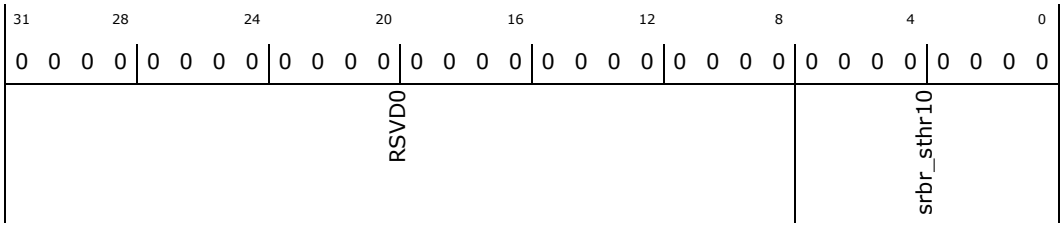
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 58h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr10:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.28.20 Shadow Receive Buffer Register and Shadow Transmit Holding Register 11 (SRBR_STHR11)—Offset 5Ch

Shadow Receive Buffer Register and Shadow Transmit Holding Register 11

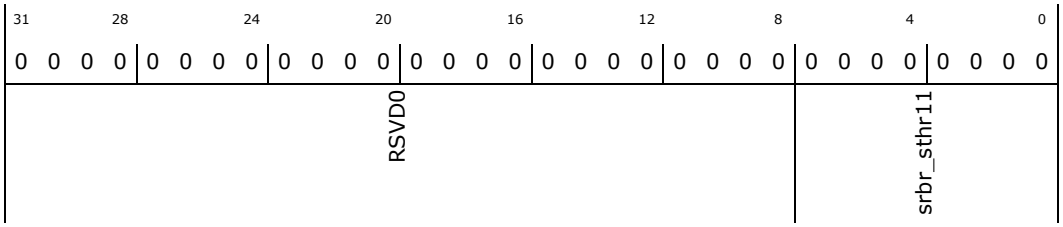
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 5Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr11:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.28.21 Shadow Receive Buffer Register and Shadow Transmit Holding Register 12 (SRBR_STHR12)—Offset 60h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 12

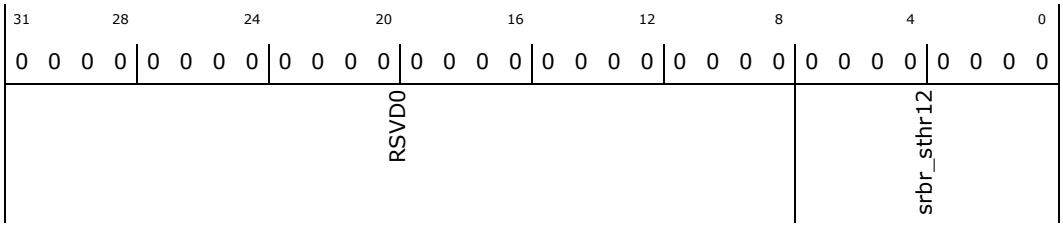
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 60h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr12:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.28.22 Shadow Receive Buffer Register and Shadow Transmit Holding Register 13 (SRBR_STHR13)—Offset 64h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 13

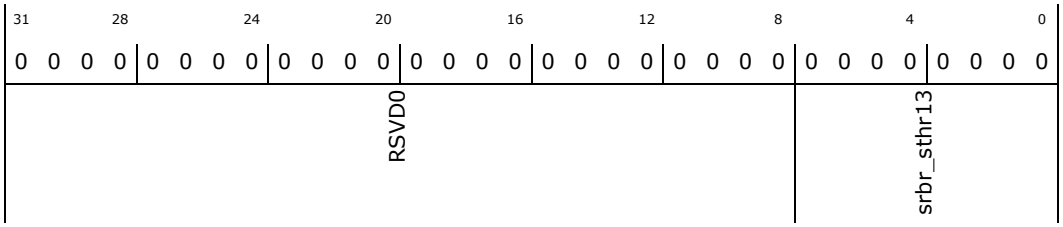
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 64h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr13:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.28.23 Shadow Receive Buffer Register and Shadow Transmit Holding Register 14 (SRBR_STHR14)—Offset 68h

Shadow Receive Buffer Register and Shadow Transmit Holding Register 14

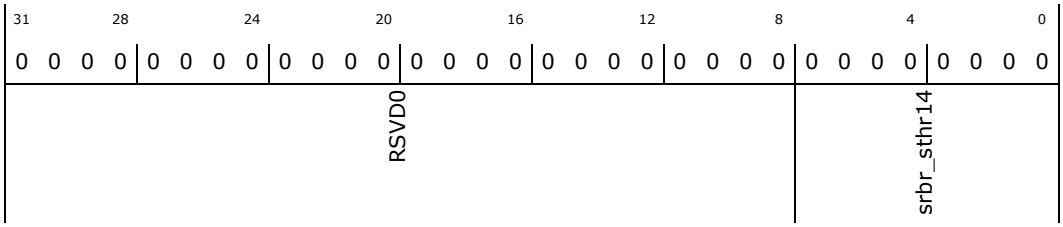
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 68h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr14:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.28.24 Shadow Receive Buffer Register and Shadow Transmit Holding Register 15 (SRBR_STHR15)—Offset 6Ch

Shadow Receive Buffer Register and Shadow Transmit Holding Register 15

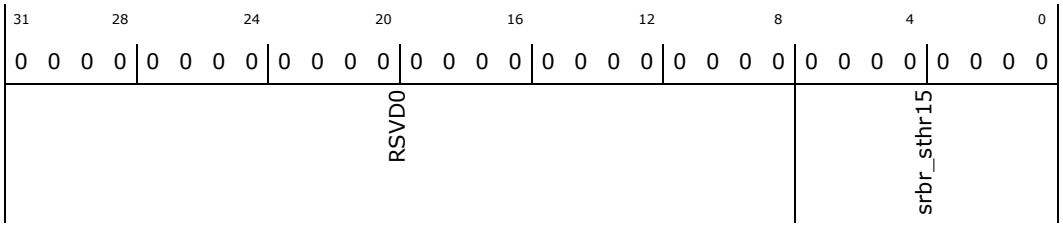
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 6Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**srbr_sthr15:** This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Reset Value: 0x0

9.28.25 FIFO Access Register (FAR)—Offset 70h

FIFO Access Register

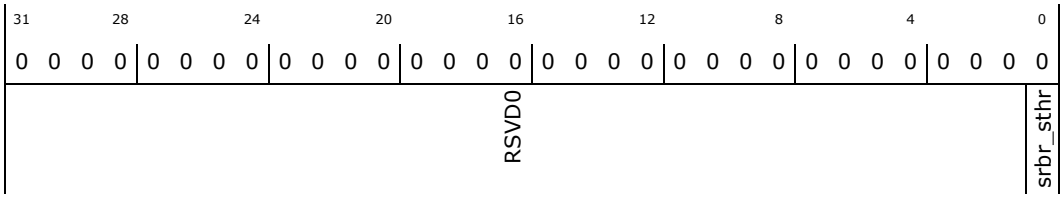
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 70h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RW	**srbr_sthr:** Writes have no effect when FIFO_ACCESS == No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. 0 = FIFO access mode disabled 1 = FIFO access mode enabled Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty. Reset Value: 0x0

9.28.26 Transmit FIFO Read (TFR)—Offset 74h

Transmit FIFO Read

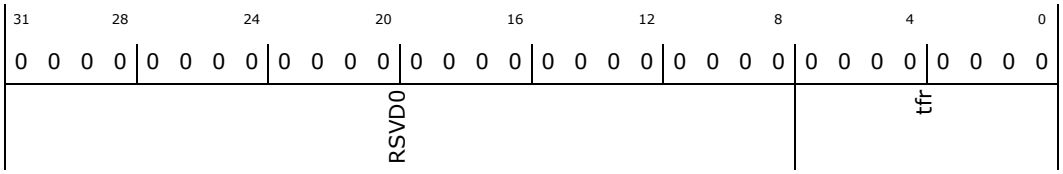
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 74h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7:0	0x0 RW	**tfr:** Transmit FIFO Read. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not implemented or not enabled, reading this register gives the data in the THR. Reset Value: 0x0

9.28.27 Receive FIFO Write (RFW)—Offset 78h

Receive FIFO Write

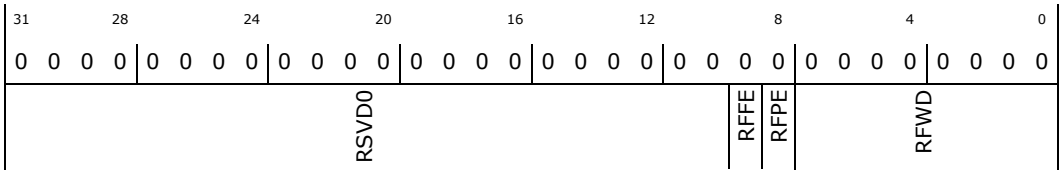
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 78h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RW	**RFFE:** Receive FIFO Framing Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR. Reset Value: 0x0
8	0x0 RW	**RFPE:** Receive FIFO Parity Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the RBR. Reset Value: 0x0
7:0	0x0 RW	**RFWD:** Receive FIFO Write Data. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR. Reset Value: 0x0

9.28.28 UART Status Register (USR)—Offset 7Ch

UART Status Register

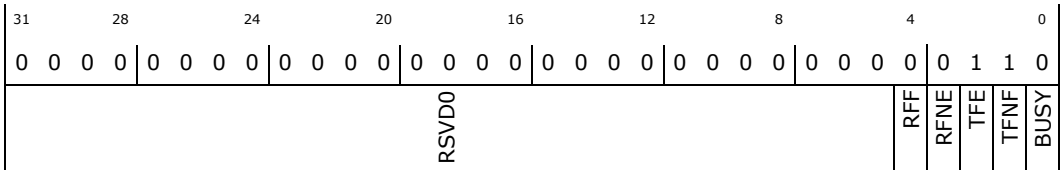
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 7Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000006h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RO	**RSVD0:** Reserved
4	0x0 RO	**RFF:** Receive FIFO Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. 0 = Receive FIFO not full 1 = Receive FIFO Full This bit is cleared when the RX FIFO is no longer full. Reset Value: 0x0
3	0x0 RO	**RFNE:** Receive FIFO Not Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. 0 = Receive FIFO is empty 1 = Receive FIFO is not empty This bit is cleared when the RX FIFO is empty. Reset Value: 0x0

Bit Range	Default & Access	Field Name (ID): Description
2	0x1 RO	**TFE:** Transmit FIFO Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. 0 = Transmit FIFO is not empty 1 = Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty. Reset Value: 0x1
1	0x1 RO	**TFNF:** Transmit FIFO Not Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO in not full. 0 = Transmit FIFO is full 1 = Transmit FIFO is not full This bit is cleared when the TX FIFO is full. Reset Value: 0x1
0	0x0 RO	**BUSY:** UART Busy. This bit is valid only when UART_16550_COMPATIBLE == NO and indicates that a serial transfer is in progress, ; when cleared, indicates that the DW_apb_uart is idle or inactive. 0 = DW_apb_uart is idle or inactive 1 = DW_apb_uart is busy (actively transferring data) NOTE: It is possible for the UART Busy bit to be cleared even though a new character may have been sent from another device. That is, if the DW_apb_uart has no data in THR and RBR and there is no transmission in progress and a start bit of a new character has just reached the DW_apb_uart. This is due to the fact that a valid start is not seen until the middle of the bit period and this duration is dependent on the baud divisor that has been programmed. If a second system clock has been implemented (CLOCK_MODE == Enabled), the assertion of this bit is also delayed by several cycles of the slower clock. Reset Value: 0x0

9.28.29 Transmit FIFO Level (TFL)—Offset 80h

Transmit FIFO Level

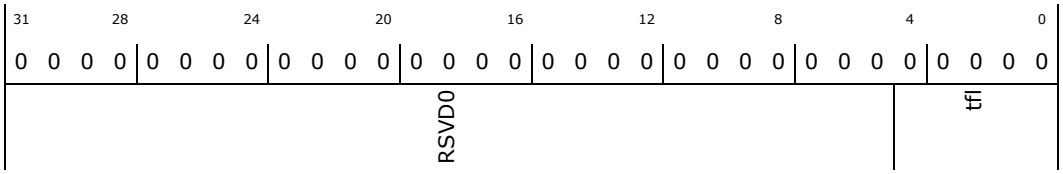
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 80h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RO	**RSVD0:** Reserved
4:0	0x0 RW	**tfl:** Transmit FIFO Level. This is indicates the number of data entries in the transmit FIFO. Reset Value: 0x0

9.28.30 Receive FIFO Level (RFL)—Offset 84h

Receive FIFO Level

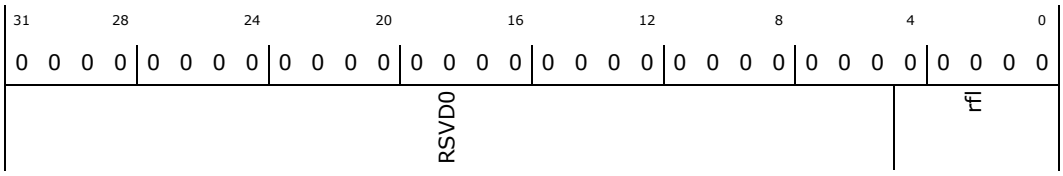
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 84h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RO	**RSVD0:** Reserved
4:0	0x0 RW	**rfl:** Receive FIFO Level. This is indicates the number of data entries in the receive FIFO. Reset Value: 0x0

9.28.31 Software Reset Register (SRR)—Offset 88h

Software Reset Register

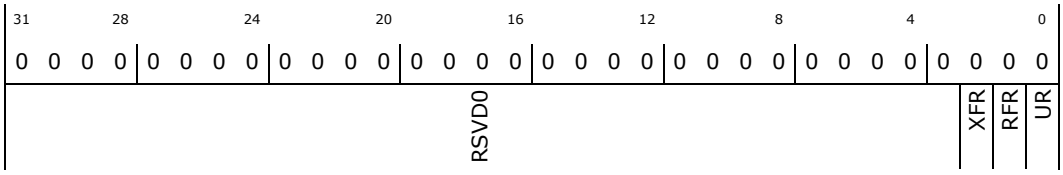
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 88h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**XFR:** XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0 Dependencies: Writes have no effect when FIFO_MODE == None.
1	0x0 RW	**RFR:** RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0 Dependencies: Writes have no effect when FIFO_MODE == None.
0	0x0 RW	**UR:** UART Reset. This asynchronously resets the DW_apb_uart and synchronously removes the reset assertion. For a two clock implementation both pclk and sclk domains are reset. Reset Value: 0x0

9.28.32 Shadow Request to Send (SRTS)—Offset 8Ch

Shadow Request to Send

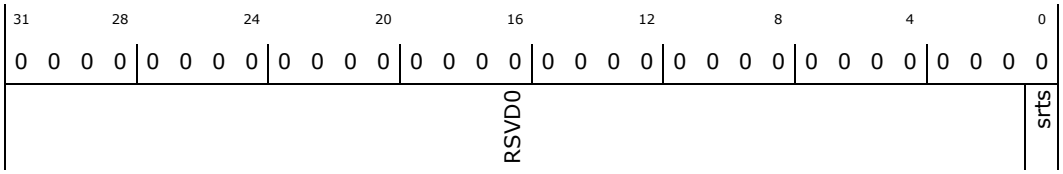
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 8Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**srts:** Shadow Request to Send. This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the DW_apb_uart is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input. Reset Value: 0x0

9.28.33 Shadow Break Control Register (SBCR)—Offset 90h

Shadow Break Control Bit. This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] = 1) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver. Reset Value: 0x0

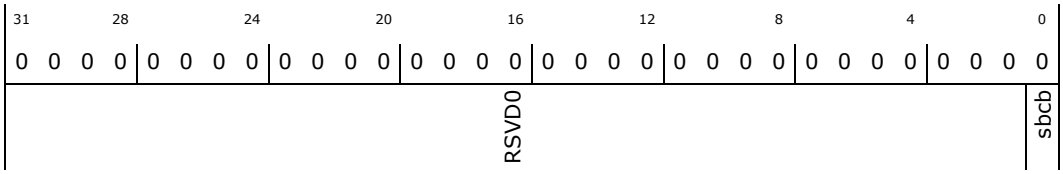
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 90h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RW	**sbcb:** Shadow Break Control Register

9.28.34 Shadow DMA Mode (SDMAM)—Offset 94h

Shadow DMA Mode

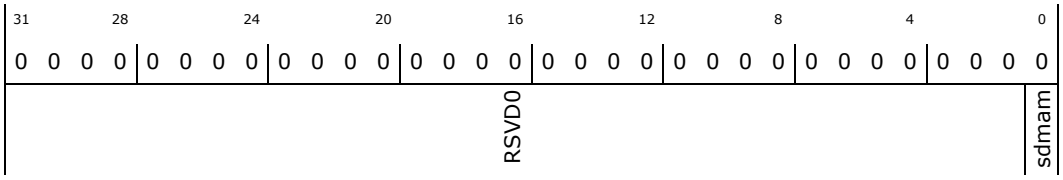
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 94h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RW	**sdmam:** Shadow DMA Mode. This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == NO). 0 = mode 0 1 = mode 1 Reset Value: 0x0

9.28.35 Shadow FIFO Enable (SFE)—Offset 98h

Shadow FIFO Enable

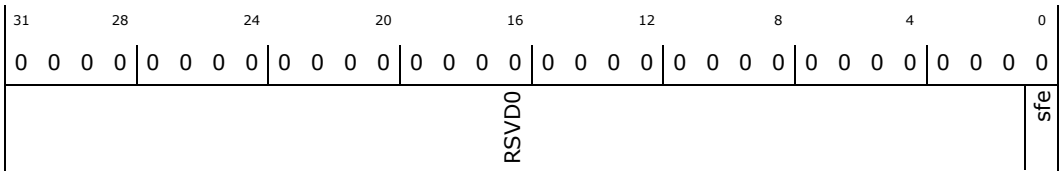
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 98h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**sfe:** Shadow FIFO Enable. This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated.This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset. Reset Value: 0x0

9.28.36 Shadow RCVR Trigger (SRT)—Offset 9Ch

Shadow RCVR Trigger

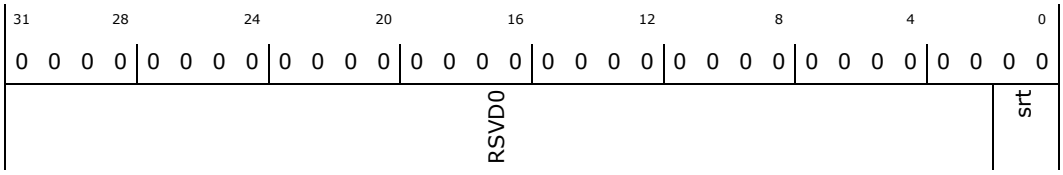
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 9Ch

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RW	**srt:** Shadow RCVR Trigger. This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO full 10 = FIFO full 11 = FIFO 2 less than full Reset Value: 0x0

9.28.37 Shadow TX Empty Trigger (STET)—Offset A0h

Shadow TX Empty Trigger. This is a shadow register for the TX empty trigger bits (FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following

trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO full 11 = FIFO full Reset Value: 0x0 Dependencies: Writes have no effect when THRE_MODE_USER == Disabled.

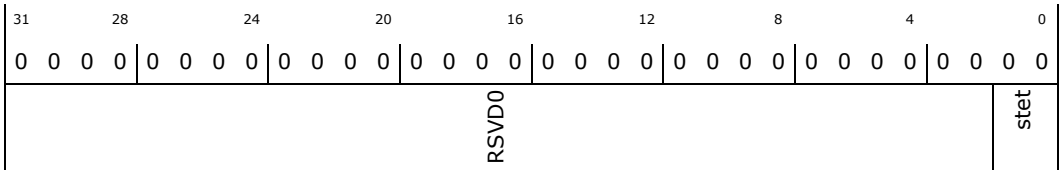
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**RSVD0:** Reserved
1:0	0x0 RW	**stet:** Shadow TX Empty Trigger

9.28.38 Halt TX (HTX)—Offset A4h

Halt TX

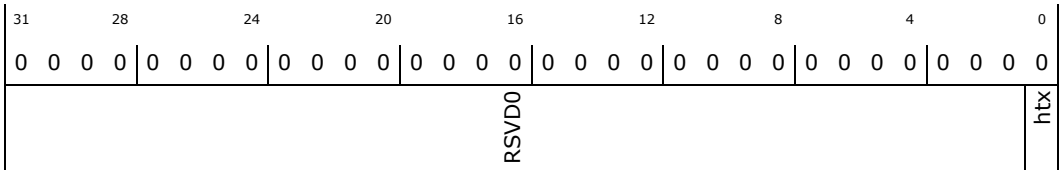
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**htx:** This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 = Halt TX disabled 1 = Halt TX enabled Note, if FIFOs are implemented and not enabled, the setting of the halt TX register has no effect on operation. Reset Value: 0x0 Dependencies: Writes have no effect when FIFO_MODE == None.

9.28.39 DMA Software Acknowledge (DMASA)—Offset A8h

DMA Software Acknowledge

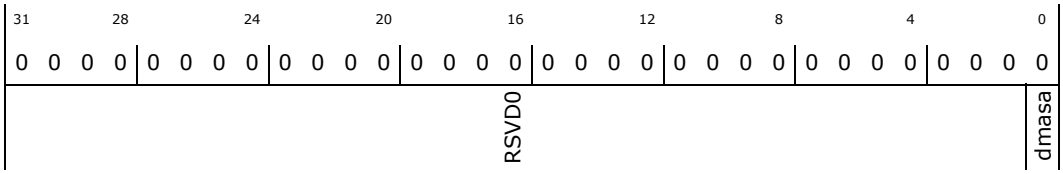
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + A8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RW	**dmasa:** This register is use to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the DW_apb_uart should clear its request. This causes the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Reset Value: 0x0 Dependencies: Writes have no effect when DMA_EXTRA == No.

9.28.40 Component Parameter Register (CPR)—Offset F4h

Component Parameter Register

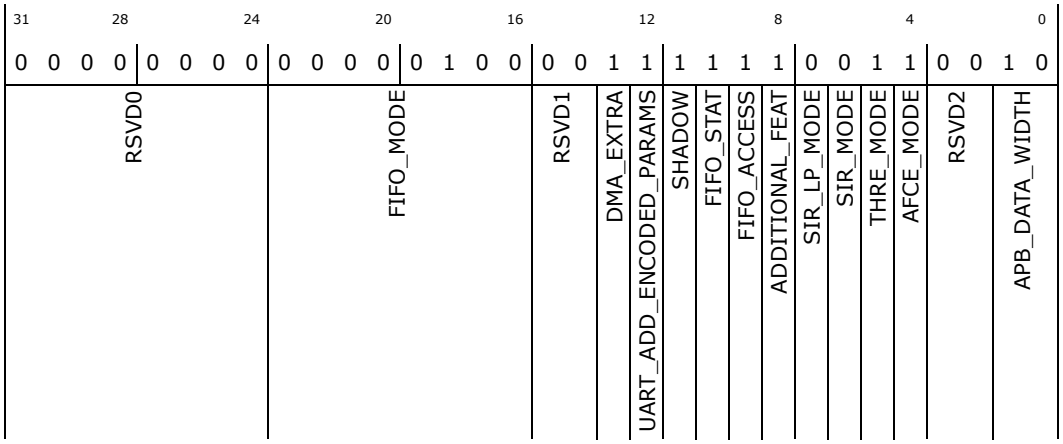
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F4h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00043F32h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**RSVD0:** Reserved
23:16	0x4 RO	**FIFO_MODE:** 0x00 = 0 0x01 = 16 0x02 = 32 to 0x80 = 2048 0x81- 0xff = reserved
15:14	0x0 RO	**RSVD1:** Reserved
13	0x1 RO	**DMA_EXTRA:** 0 = FALSE, 1 = TRUE
12	0x1 RO	**UART_ADD_ENCODED_PARAMS:** 0 = FALSE, 1 = TRUE
11	0x1 RO	**SHADOW:** 0 = FALSE, 1 = TRUE
10	0x1 RO	**FIFO_STAT:** 0 = FALSE, 1 = TRUE
9	0x1 RO	**FIFO_ACCESS:** 0 = FALSE, 1 = TRUE
8	0x1 RO	**ADDITIONAL_FEAT:** 0 = FALSE, 1 = TRUE
7	0x0 RO	**SIR_LP_MODE:** 0 = FALSE, 1 = TRUE
6	0x0 RO	**SIR_MODE:** 0 = FALSE, 1 = TRUE
5	0x1 RO	**THRE_MODE:** 0 = FALSE, 1 = TRUE
4	0x1 RO	**AFCE_MODE:** 0 = FALSE, 1 = TRUE
3:2	0x0 RO	**RSVD2:** Reserved
1:0	0x2 RO	**APB_DATA_WIDTH:** 00 = 8 bits 01 = 16 bits 10 = 32 bits 11 = reserved

9.28.41 UART Component Version (UCV)—Offset F8h

UART Component Version

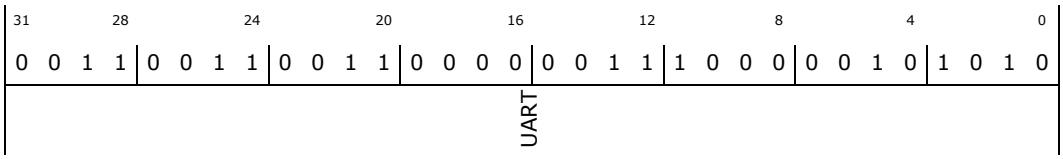
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + F8h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 3330382Ah



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x3330382a RO	**UART:** ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01* Reset Value: See the releases table in the AMBA 2 release notes.

9.28.42 Component Type Register (CTR)—Offset FCh

Component Type Register

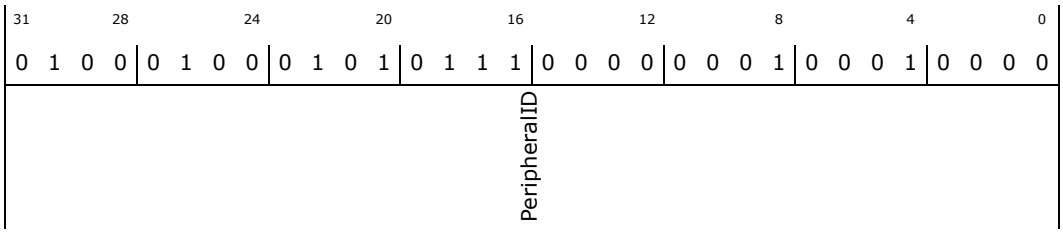
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + FCh

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 44570110h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x44570110 RO	**PeripheralID:** This register contains the peripherals identification code. Reset Value: 0x44570110

9.28.43 private clock params (PRV_CLOCK_PARAMS)—Offset 800h

private clock params

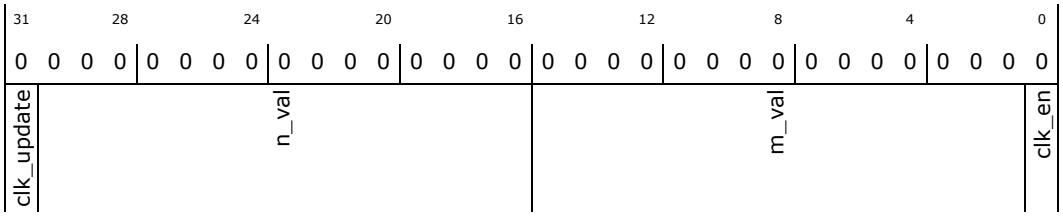
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 800h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**clk_update:** update the clock divider after seeting new m and n values
30:16	0x0 RW	**N_VAL (n_val):** n value for the m over n divider
15:1	0x0 RW	**M_VAL (m_val):** m value for the m over n divider
0	0x0 RW	**clk_en:** clk en of the m over n divider

9.28.44 software reset (RESETS)—Offset 804h

software reset

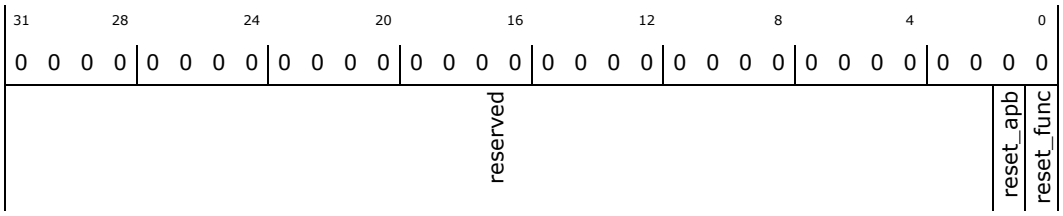
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (reserved):** Reserved

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**reset_apb:** reset the apb domain
0	0x0 RW	**reset_func:** reset the func clock domain

9.28.45 General purpose register (GENERAL)—Offset 808h

General purpose register

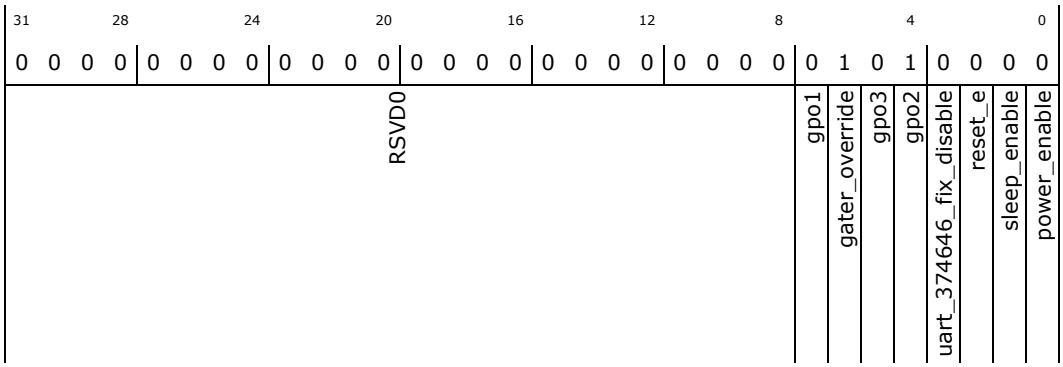
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000050h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7	0x0 RW	**gpo1:** not applicable
6	0x1 RW	**gater_override:** not applicable
5	0x0 RW	**gpo3:** not applicable
4	0x1 RW	**gpo2:** this bit select if the uart clock req will be dynamic or control by the uart clock en: 1 - control by the clk en, 0 - dynamic. Default value - 1
3	0x0 RW	**uart_374646_fix_disable:** Disable rts_n override
2	0x0 RW	**reset_e:** not applicable
1	0x0 RW	**sleep_enable:** not applicable

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**power_enable:** not applicable

9.28.46 Transaction counter (UART_BYTE_COUNT)—Offset 818h

Transaction counter

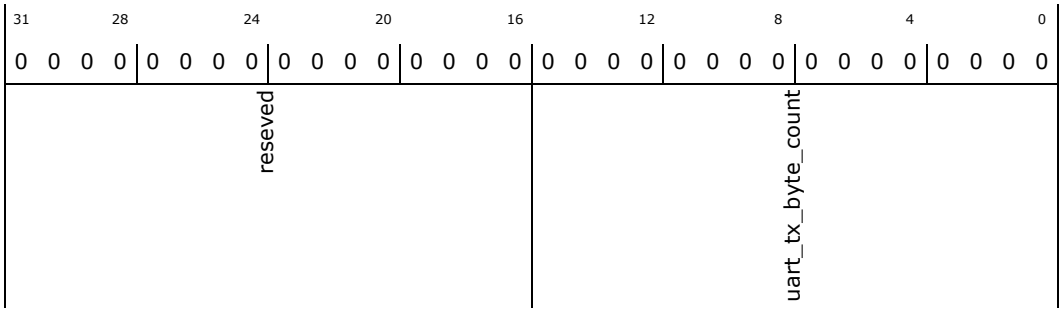
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 818h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**reserved (reseved):** reserved
15:0	0x0 RO	**uart_tx_byte_count:** UART transaction counter

9.28.47 Overflow interrupt (UART_OVERFLOW_INTR_STAT)—Offset 820h

Overflow interrupt

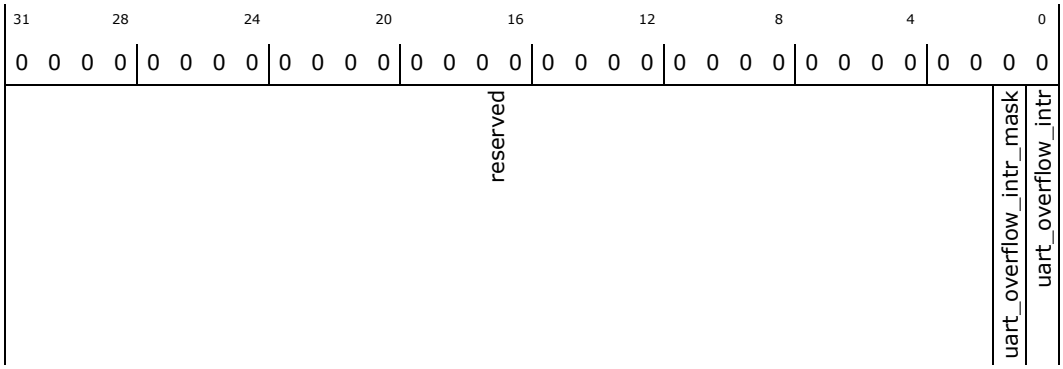
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

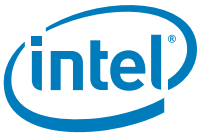
Offset: [BAR] + 820h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:4] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**reserved:** reserved
1	0x0 RW	**uart1_overflow_intr_mask (uart_overflow_intr_mask):** Mask the overflow intr
0	0x0 RO	**uart_overflow_intr:** Indicate there was count overflow



9.29 SIO PWM 0 PCI Configuration Registers

Table 92. Summary of SIO PWM 0 PCI Configuration Registers—0/30/1

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4775	00008086h
4–7h	4	"STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h" on page 4775	00100000h
8–Bh	4	"REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4777	00000000h
C–Fh	4	"CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4778	00800000h
10–13h	4	"BAR -Base Address Register (BAR)—Offset 10h" on page 4778	00000000h
14–17h	4	"BAR1 -Base Address Register1 (BAR1)—Offset 14h" on page 4779	00000000h
2C–2Fh	4	"SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4780	00000000h
30–33h	4	"EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4781	00000000h
34–37h	4	"CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4781	00000000h
3C–3Fh	4	"INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4782	00000100h
80–83h	4	"POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4782	00030001h
84–87h	4	"PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4783	00000008h
F8–FBh	4	"Manufacturers ID (MANID)—Offset F8h" on page 4784	00000000h

9.29.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

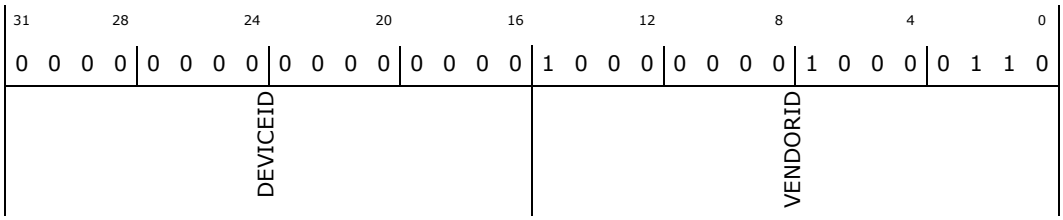
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**DEVICEID:** Device ID identifies the particular AHB/APB device. This is tied to a strap at the top level. Because of tool issues, the HTML files show this field as 0, but the following are the POR values for SoC: LPIO1 DMA: 0x2286 LPIO1 PWM1: 0x2288 LPIO1 PWM2: 0x2289 LPIO1 HSUART1: 0x228A LPIO1 HSUART2: 0x228C LPIO1 SPI1: 0x228E LPIO1 SPI2: 0x2290 LPIO1 SPI3: 0x22AC LPIO2 DMA: 0x22C0 LPIO2 I2C1: 0x22C1 LPIO2 I2C2: 0x22C2 LPIO2 I2C3: 0x22C3 LPIO2 I2C4: 0x22C4 LPIO2 I2C5: 0x22C5 LPIO2 I2C6: 0x22C6 LPIO2 I2C7: 0x22C7 For the final word on this, please see Ray Ng's SoC RevID and DevID HAS on Infofactory: https://ifcollaborate.intel.com/IFC/getdoc.aspx?docbase=InfoFactoryKBandchronid=09005ffd80e84b43andver=CURRENTandqepop=false
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap the top level.

9.29.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

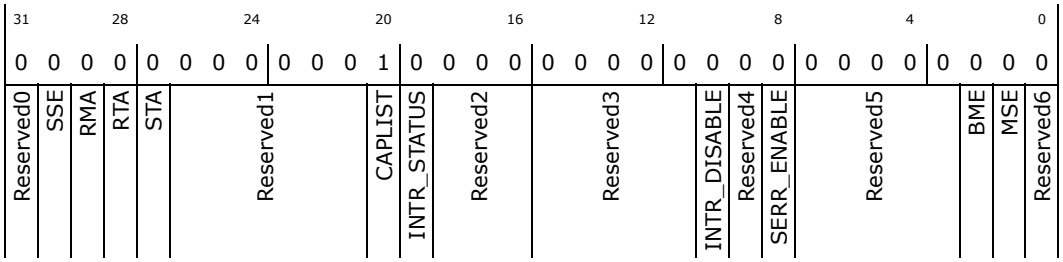
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved0:** Reserved
30	0x0 RW/1C	**SSE:** This bit is set when a device sends an DO_SERR message, and the SERR# Enable bit in the Command register is 1
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric PortReceived Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27	0x0 RW/1C	**STA:** The Bridge sets this bit whenever it responds to a transaction with CA abort. If the SERR# Enable bit is set, the Bridge sets the Signaled System Error bit and sends an DO_SERR message on the IOSF Sideband.
26:21	0x0 RO	**Reserved1:** Reserved
20	0x1 RO	**CAPLIST:** Capabilities List: Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt .i.e Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.. Reset value of this bit is 0.
9	0x0 RO	**Reserved4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: If both SERR# Enable and the Unsupported Request Reporting Enable (URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0x0 RO	**Reserved6:** Reserved

9.29.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

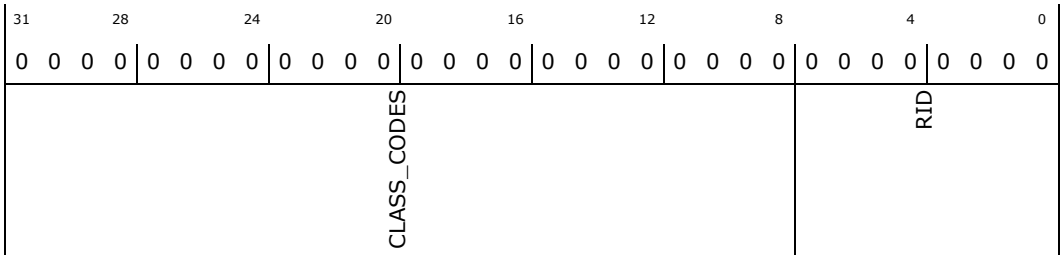
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

9.29.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

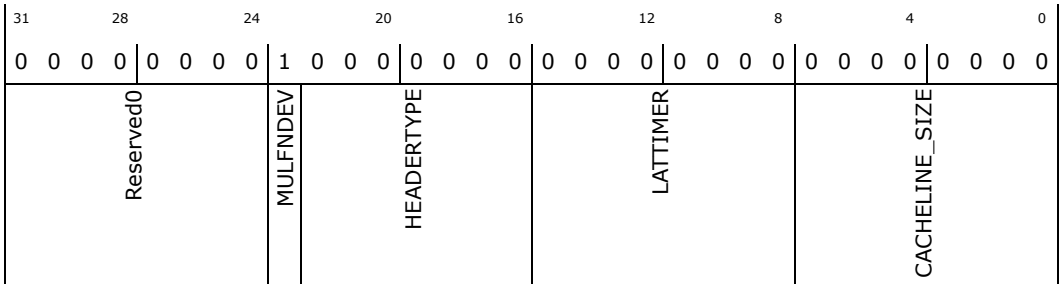
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + Ch

Default: 00800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x1 RO	**MULFNDEV:** Multi Function Device: This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. Value of 1 indicates multifunction device value of 0 indicates single function device
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	0x0 RO	**LATTIMER:** Latency Timer: Doesn.t apply to PCI Express. Hardwired to 00h.
7:0	0x0 RW	**CACHELINE_SIZE:** Cache Line Size: Doesn.t apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

9.29.5 BAR -Base Address Register (BAR)—Offset 10h

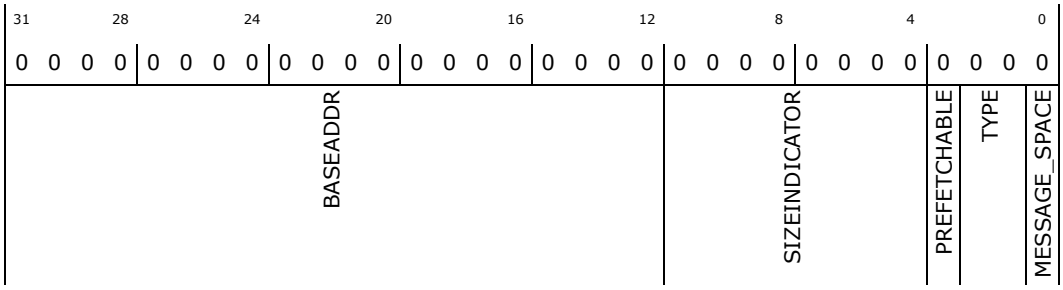
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the AHB device memory space. Taken from Strap values as 1's. Please note that for DMA this field goes from [31:14], or 16kbyte, and the SIZEINDICATOR field goes from [13:4].
11:4	0x0 RO	**SIZEINDICATOR:** Size Indicator Read Only: Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0x0 RO	**TYPE:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.29.6 BAR1 -Base Address Register1 (BAR1)—Offset 14h

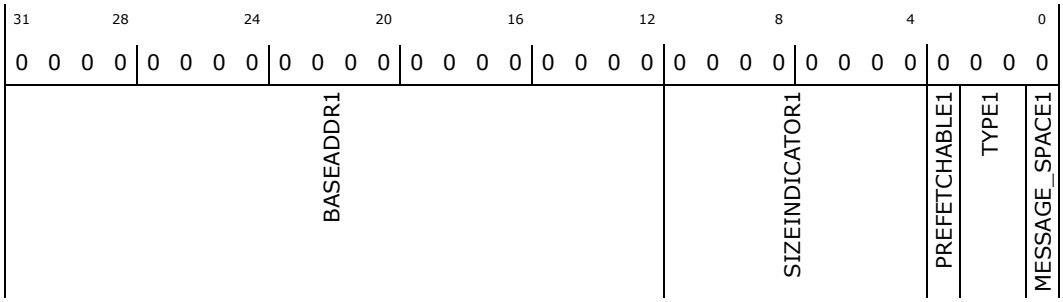
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	0x0 RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not
2:1	0x0 RO	**TYPE1:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.29.7 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

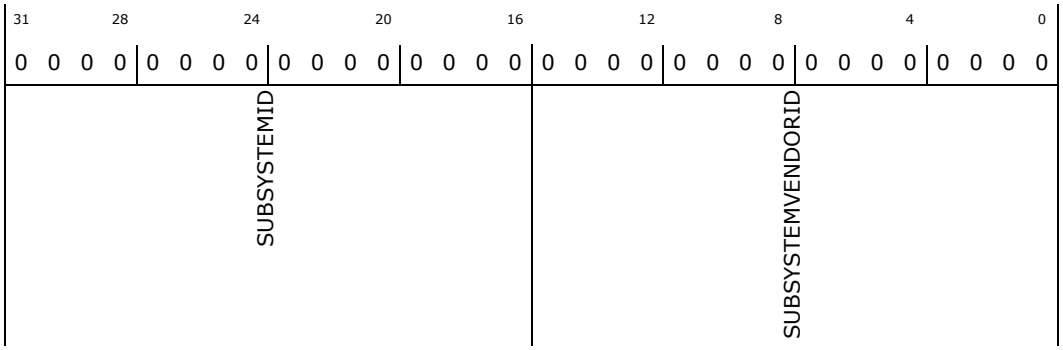
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

9.29.8 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

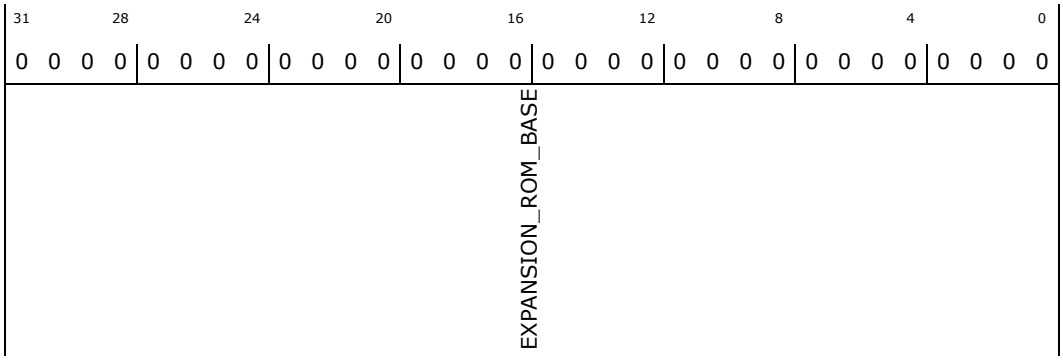
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** A value of all zeros indicates no support for expansion ROM.

9.29.9 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

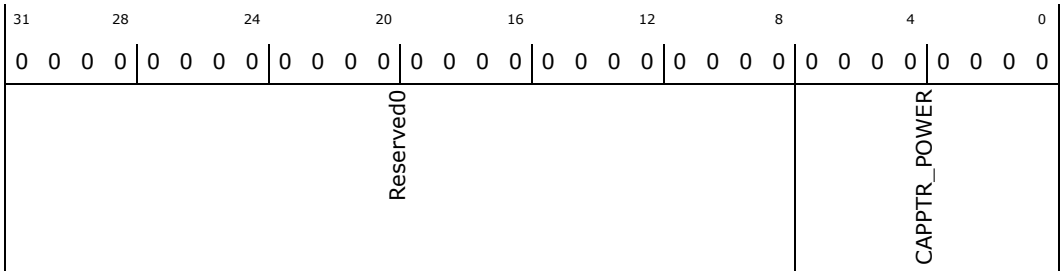
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x0 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

9.29.10 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

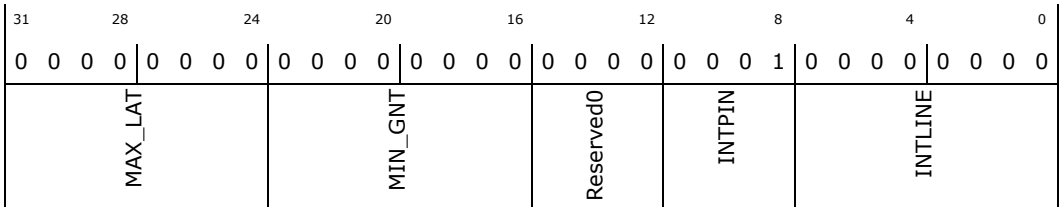
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

9.29.11 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

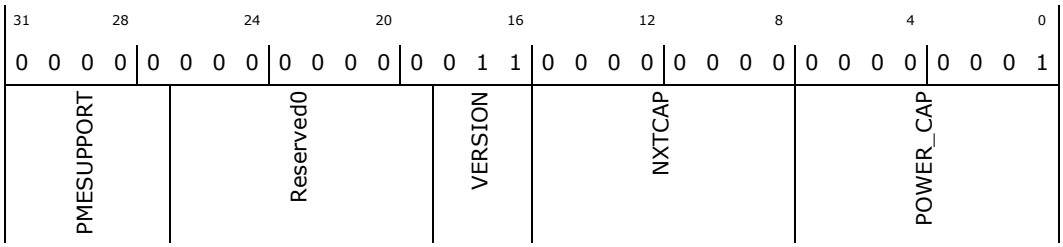
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** PME_Support - This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

9.29.12 PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

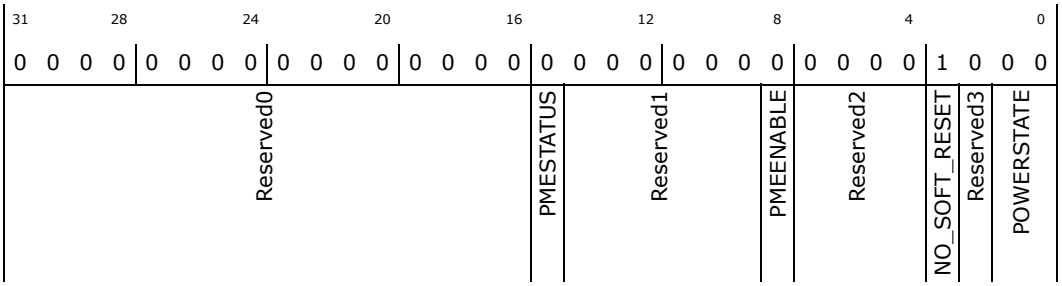
PMECTRLSTATUS - PME Control and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

9.29.13 Manufacturers ID (MANID)—Offset F8h

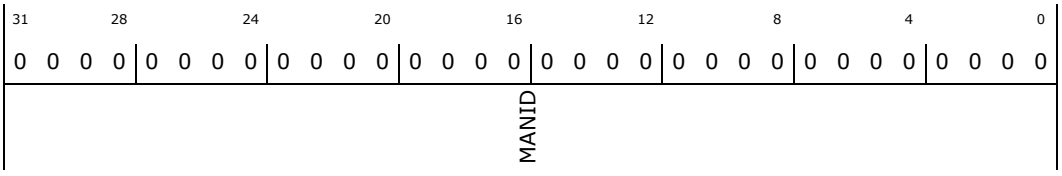
Manufacturers ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:1] + F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: This register is brought out as straps to the top level.

9.30 SIO PWM 0 Memory Mapped I/O

Table 93. Summary of SIO PWM 0 Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"PWM Control Register (PWMCTRL)—Offset 0h" on page 4787	00010000h
804–807h	4	"software reset (RESETS)—Offset 804h" on page 4787	00000000h
808–80Bh	4	"General purpose register (GENERAL)—Offset 808h" on page 4788	00000010h

9.30.1 PWM Control Register (PWMCTRL)—Offset 0h

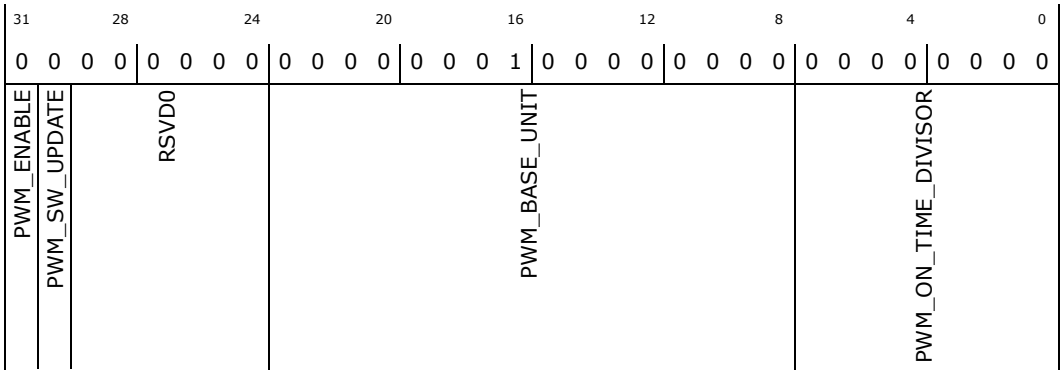
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:1] + 10h

Default: 00010000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**PWM Enable (PWM_ENABLE):** 0 = Disable PWM Output 1 = Enable PWM Output
30	0x0 RW	**PWM Software Update (PWM_SW_UPDATE):** Indication that there is an update to PWM settings pending. SW sets this bit to 1 when updating the PWM_base_unit or PWM_on_time_divisor fields. The PWM module will apply the new settings at the end of the current cycle and reset this bit. 0 = No updates pending 1 = Update pending
29:24	0x0 RO	**RSVD0:** Reserved
23:8	0x100 RW	**PWM Base Unit (PWM_BASE_UNIT):** Base unit register. Unsigned 8 integer bits, 8 fraction bits. Used to determine PWM output frequency.
7:0	0x0 RW	**PWM On Time Divisor (PWM_ON_TIME_DIVISOR):** PWM duty cycle = PWM_on-time_divisor/256.

9.30.2 software reset (RESETS)—Offset 804h

software reset

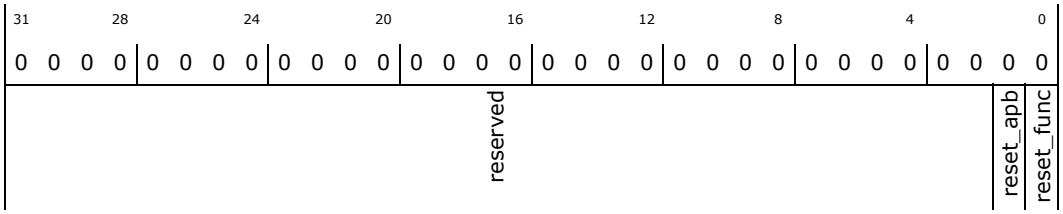
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:1] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (reserved):** Reserved
1	0x0 RW	**reset_apb:** reset the apb domain
0	0x0 RW	**reset_func:** reset the func clock domain

9.30.3 General purpose register (GENERAL)—Offset 808h

General purpose register

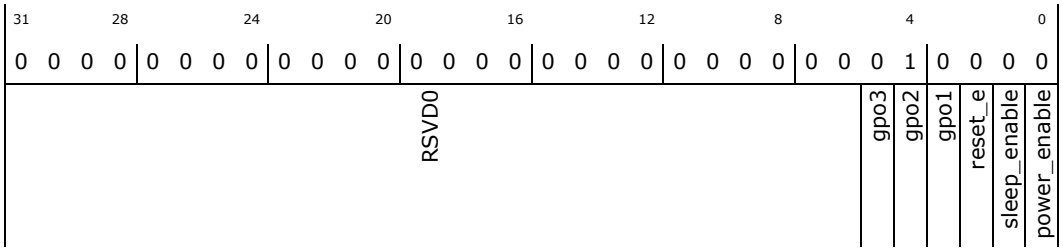
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:1] + 10h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**RSVD0:** Reserved
5	0x0 RW	**gpo3:** not applicable
4	0x1 RW	**gpo2:** not applicable
3	0x0 RW	**gpo1:** This bit is re-used to support 32kHz slow mode. Default is 19.2MHz as PWM source clock
2	0x0 RW	**reset_e:** not applicable

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**sleep_enable:** not applicable
0	0x0 RW	**power_enable:** not applicable

9.31 SIO PWM 1 PCI Configuration Registers

Table 94. Summary of SIO PWM 1 PCI Configuration Registers—0/30/2

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h" on page 4791	00008086h
4–7h	4	"STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h" on page 4791	00100000h
8–Bh	4	"REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h" on page 4793	00000000h
C–Fh	4	"CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch" on page 4794	00800000h
10–13h	4	"BAR -Base Address Register (BAR)—Offset 10h" on page 4794	00000000h
14–17h	4	"BAR1 -Base Address Register1 (BAR1)—Offset 14h" on page 4795	00000000h
2C–2Fh	4	"SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch" on page 4796	00000000h
30–33h	4	"EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 4797	00000000h
34–37h	4	"CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h" on page 4797	00000000h
3C–3Fh	4	"INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch" on page 4798	00000100h
80–83h	4	"POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h" on page 4798	00030001h
84–87h	4	"PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h" on page 4799	00000008h
F8–FBh	4	"Manufacturers ID (MANID)—Offset F8h" on page 4800	00000000h

9.31.1 DEVICEVENDORID - Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

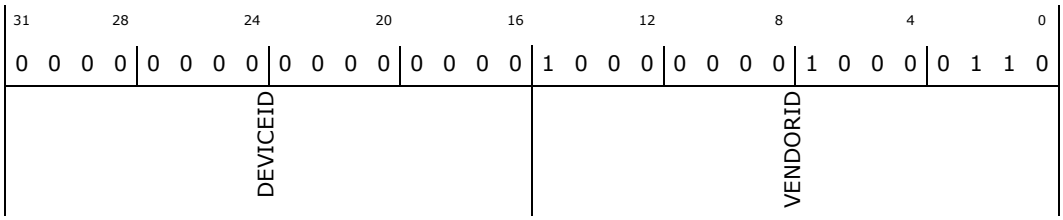
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**DEVICEID:** Device ID identifies the particular AHB/APB device. This is tied to a strap at the top level. Because of tool issues, the HTML files show this field as 0, but the following are the POR values for SoC: LPIO1 DMA: 0x2286 LPIO1 PWM1: 0x2288 LPIO1 PWM2: 0x2289 LPIO1 HSUART1: 0x228A LPIO1 HSUART2: 0x228C LPIO1 SPI1: 0x228E LPIO1 SPI2: 0x2290 LPIO1 SPI3: 0x22AC LPIO2 DMA: 0x22C0 LPIO2 I2C1: 0x22C1 LPIO2 I2C2: 0x22C2 LPIO2 I2C3: 0x22C3 LPIO2 I2C4: 0x22C4 LPIO2 I2C5: 0x22C5 LPIO2 I2C6: 0x22C6 LPIO2 I2C7: 0x22C7 For the final word on this, please see Ray Ng's SoC RevID and DevID HAS on Infofactory: https://ifcollaborate.intel.com/IFC/getdoc.aspx?docbase=InfoFactoryKBandchronid=09005ffd80e84b43andver=CURRENTandqepop=false
15:0	0x8086 RO	**VENDORID:** Vendor ID is a unique ID provided by PCI SIG which identifies the manufacturer of the device. This is tied to a strap the top level.

9.31.2 STATUSCOMMAND- Status and Command (STATUSCOMMAND)—Offset 4h

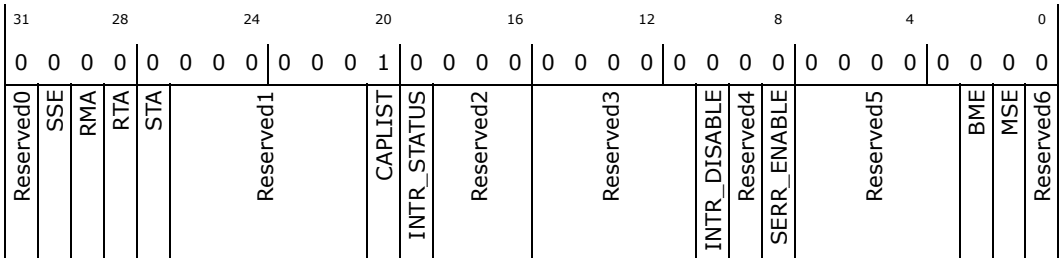
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved0:** Reserved
30	0x0 RW/1C	**SSE:** This bit is set when a device sends an DO_SERR message, and the SERR# Enable bit in the Command register is 1
29	0x0 RW/1C	**RMA:** Received Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric PortReceived Master Abort: If the completion status received from IOSF is UR, Bridge sets this bit. S/W writes a 1. to this bit to clear it. This bit will not be set for the Fabric port. This bit is not used for the Fabric Port
28	0x0 RW/1C	**RTA:** Received Target Abort: If the completion status received from IOSF is CA, Bridge sets this bit. S/W writes a 1.1 to this bit to clear it. This bit will not be set for the fabric port. This bit is not used for the Fabric Port
27	0x0 RW/1C	**STA:** The Bridge sets this bit whenever it responds to a transaction with CA abort. If the SERR# Enable bit is set, the Bridge sets the Signaled System Error bit and sends an DO_SERR message on the IOSF Sideband.
26:21	0x0 RO	**Reserved1:** Reserved
20	0x1 RO	**CAPLIST:** Capabilities List: Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h. If PM capability is not required then this bit should be tied to 0
19	0x0 RO	**INTR_STATUS:** Interrupt Status: This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device.s/function.s INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:16	0x0 RO	**Reserved2:** Reserved
15:11	0x0 RO	**Reserved3:** Reserved
10	0x0 RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt .i.e Bridge does not send Interrupt Assert message through the IOSF SideBand Channel.. Reset value of this bit is 0.
9	0x0 RO	**Reserved4:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW	**SERR_ENABLE:** SERR# Enable: If both SERR# Enable and the Unsupported Request Reporting Enable (URRE) register are 1., the agent sets the Signaled System Error bit in the PCI Status Register and sends an ERR_NONFATAL message on the IOSF sideband interface.
7:3	0x0 RO	**Reserved5:** Reserved
2	0x0 RW	**BME:** Bus Master Enable: If this bit is 0, Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0x0 RW	**MSE:** Memory Space Enable: This bit controls Bridge's response to downstream Memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0x0 RO	**Reserved6:** Reserved

9.31.3 REVCLASSCODE - Revision ID and Class Code (REVCLASSCODE)—Offset 8h

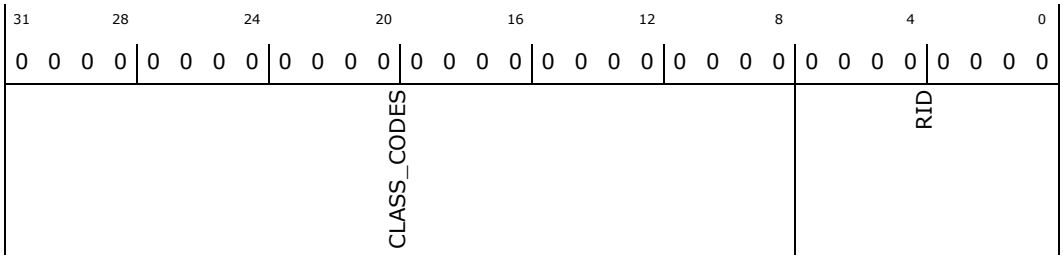
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register level programming interface. The register is broken into three byte size fields. The upper byte (at offset 0Bh) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset 0Ah) is a sub-class code which identifies more specifically the function of the device. The lower byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0x0 RO	**RID:** Revision ID identifies the revision of particular AHB device. This is tied to a strap at the top level.

9.31.4 CLLATHEADERBIST - Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

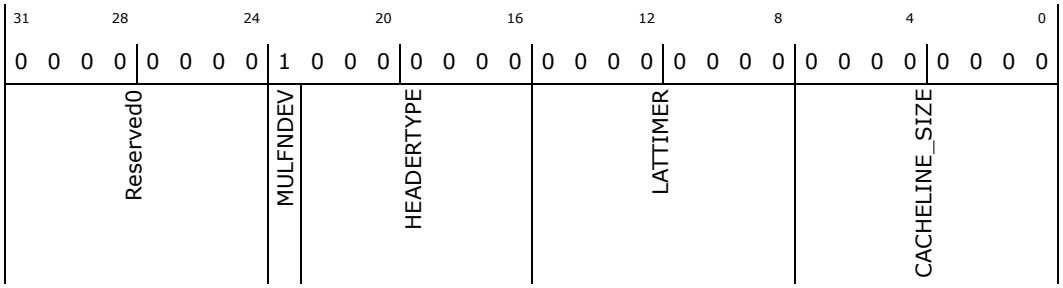
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + Ch

Default: 00800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved
23	0x1 RO	**MULFNDEV:** Multi Function Device: This bit is always 0 for non fabric ports. For Fabric ports it is driven from fabric_mult_function strap. Value of 1 indicates multifunction device value of 0 indicates single function device
22:16	0x0 RO	**HEADERTYPE:** Header Type: Implements Type 0 Configuration header.
15:8	0x0 RO	**LATTIMER:** Latency Timer: Doesn.t apply to PCI Express. Hardwired to 00h.
7:0	0x0 RW	**CACHELINE_SIZE:** Cache Line Size: Doesn.t apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the AHB Device connected.

9.31.5 BAR -Base Address Register (BAR)—Offset 10h

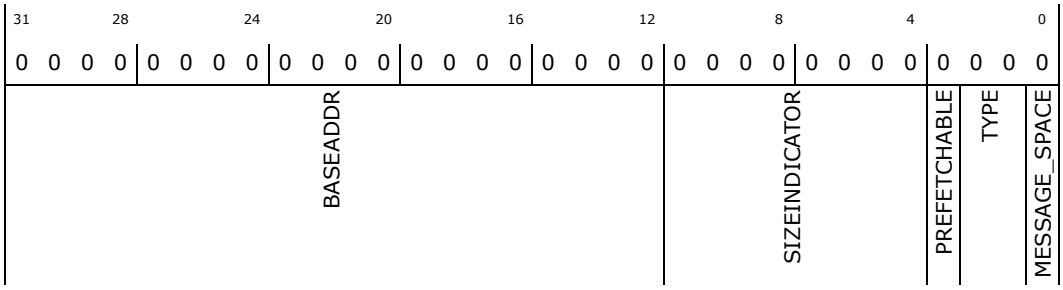
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR:** Base Address: Base address of the AHB device memory space. Taken from Strap values as 1's. Please note that for DMA this field goes from [31:14], or 16kbyte, and the SIZEINDICATOR field goes from [13:4].
11:4	0x0 RO	**SIZEINDICATOR:** Size Indicator Read Only: Always returns zero. The size of this register depends on the size of the Memory space. This size is determined by a top level of STRAP values as 0.s. Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE:** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0x0 RO	**TYPE:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.31.6 BAR1 -Base Address Register1 (BAR1)—Offset 14h

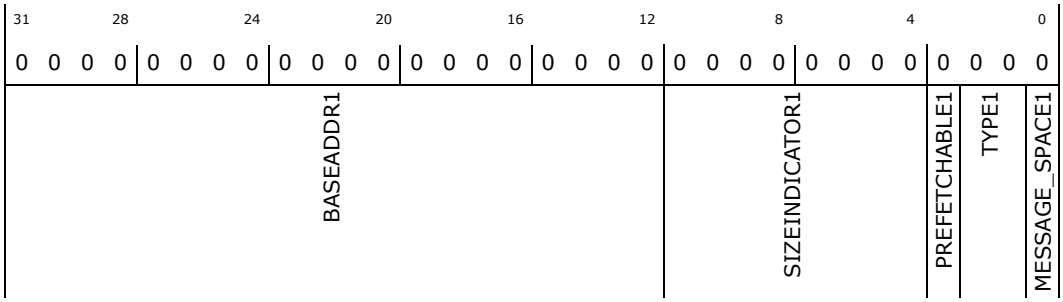
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Base Address Register1: BAR1 of the LPIO device.

Bit Range	Default & Access	Field Name (ID): Description
11:4	0x0 RO	**SIZEINDICATOR1:** Always will be zero as minimum size is 4K
3	0x0 RO	**PREFETCHABLE1:** Prefetchable: Indicates that this BAR is not
2:1	0x0 RO	**TYPE1:** Type: 00 Indicates BAR lies in 32 bit address range.
0	0x0 RO	**MESSAGE_SPACE1:** Memory Space Indicator: 0. Indicates this BAR is present in the memory space.

9.31.7 SUBSYSTEMID -Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

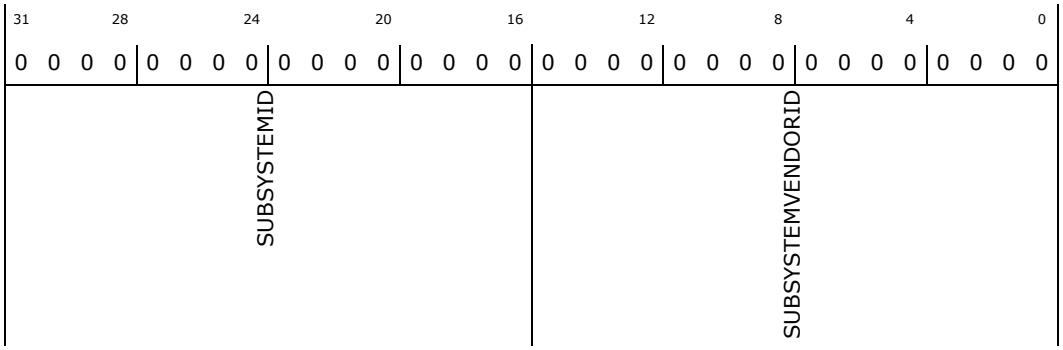
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Subsystem ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other. This register is a Read Write Once type register.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Subsystem Vendor ID: This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

9.31.8 EXPANSION ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

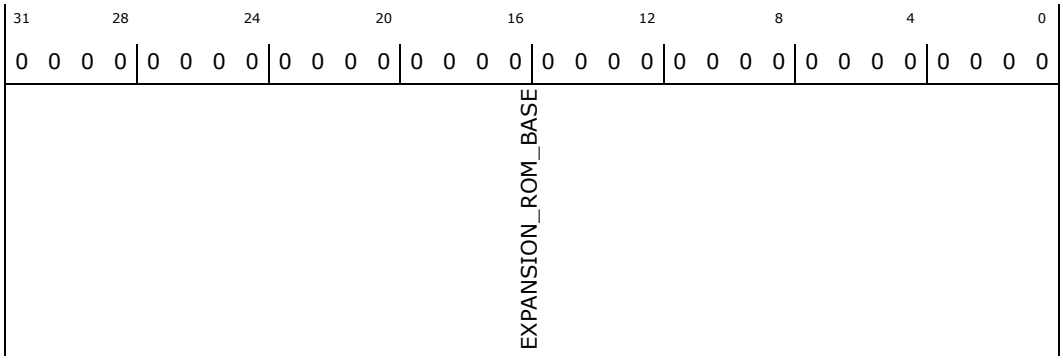
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** A value of all zeros indicates no support for expansion ROM.

9.31.9 CAPABILITYPTR - Capabilities Pointer (CAPABILITYPTR)—Offset 34h

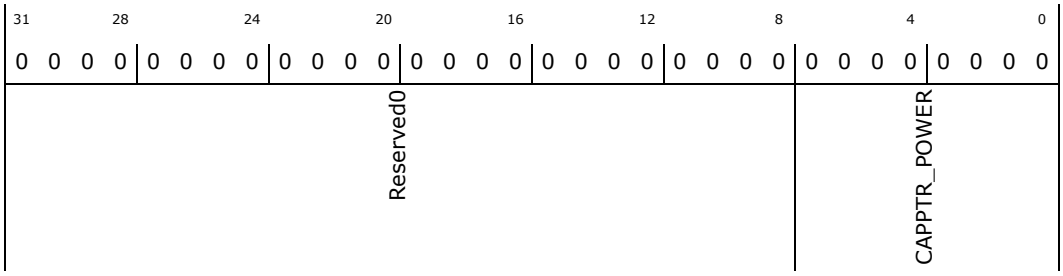
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved
7:0	0x0 RO	**CAPPTR_POWER:** Capabilities Pointer: Indicates what the next capability is. This capability can be programmed to be PM Capability (0x80) if PM Capability is enabled in SB. If PM capability is disabled then this register has 00h.

9.31.10 INTERRUPTREG - Interrupt Register (INTERRUPTREG)—Offset 3Ch

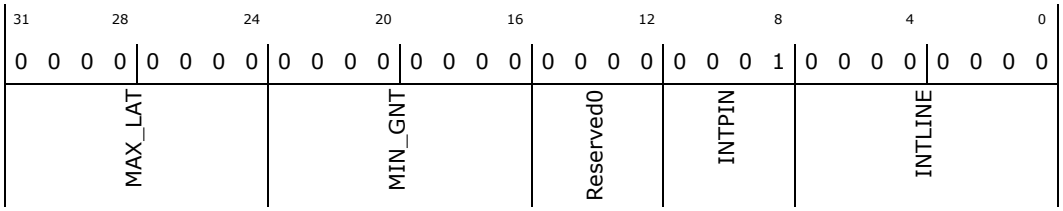
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Max_Lat: Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0x0 RO	**MIN_GNT:** Min_Gnt: Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0x0 RO	**Reserved0:** Reserved
11:8	0x1 RO	**INTPIN:** Interrupt Pin: Each AHB IP on Bridge is a Single function device. Hence Bridge only generates INTA on IOSF SB. The Fabric on AHB Bridge appears as a Multifunction device. Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space.
7:0	0x0 RW	**INTLINE:** Interrupt Line: Bridge does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

9.31.11 POWERCAPID - PowerManagement Capability ID (POWERCAPID)—Offset 80h

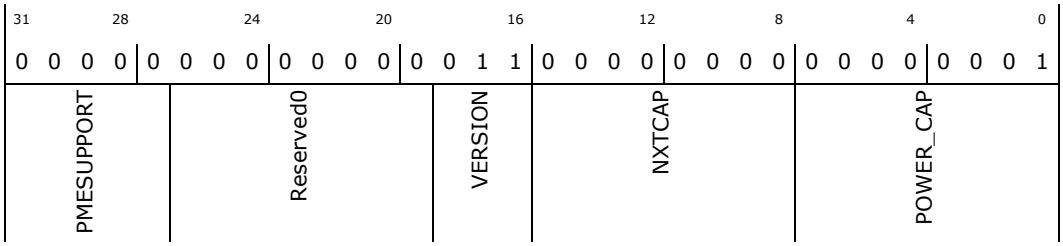
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** PME_Support - This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb - PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the strap strap_pme_support.
26:19	0x0 RO	**Reserved0:** Reserved
18:16	0x3 RO	**VERSION:** Version: Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0x0 RO	**NXTCAP:** Next Capability: Points to the next capability structure. This points to NULL.
7:0	0x1 RO	**POWER_CAP:** Power Management Capability: Indicates this is power management capability.

9.31.12 PMECTRLSTATUS - PME Control and Status Register (PMECTRLSTATUS)—Offset 84h

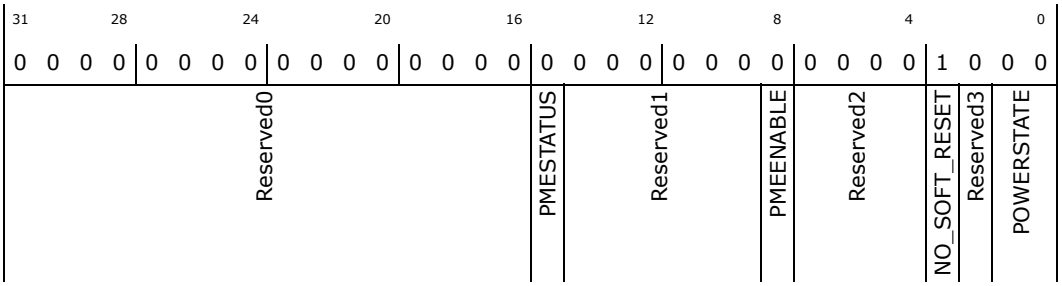
PMECTRLSTATUS - PME Control and Status Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved
15	0x0 RW/1C	**PMESTATUS:** PME Status: 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the AHB Device would normally assert the PME# signal independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0x0 RO	**Reserved1:** Reserved
8	0x0 RW	**PMEENABLE:** PME Enable: A 1 enables the function to assert PME#. When 0, PME# message on SB is disabled.
7:4	0x0 RO	**Reserved2:** Reserved
3	0x1 RO	**NO_SOFT_RESET:** No_Soft_Reset: This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0x0 RO	**Reserved3:** Reserved
1:0	0x0 RW	**POWERSTATE:** Power State : This field is used both to determine the current power state of the AHB IP and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked. D3Hot will not be used for Downstream decode on fabric ports.

9.31.13 Manufacturers ID (MANID)—Offset F8h

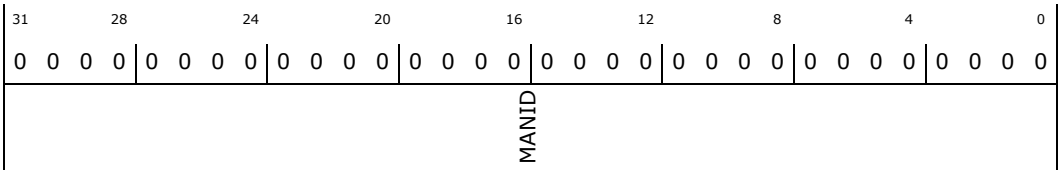
Manufacturers ID

Access Method

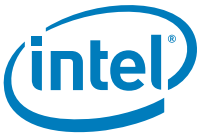
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:30, F:2] + F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Manufacturer ID: This register is brought out as straps to the top level.



9.32 SIO PWM 1 Memory Mapped I/O

Table 95. Summary of SIO PWM Memory Mapped I/O Registers—BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"PWM Control Register (PWMCTRL)—Offset 0h" on page 4803	00010000h
804–807h	4	"software reset (RESETS)—Offset 804h" on page 4803	00000000h
808–80Bh	4	"General purpose register (GENERAL)—Offset 808h" on page 4804	00000010h

9.32.1 PWM Control Register (PWMCTRL)—Offset 0h

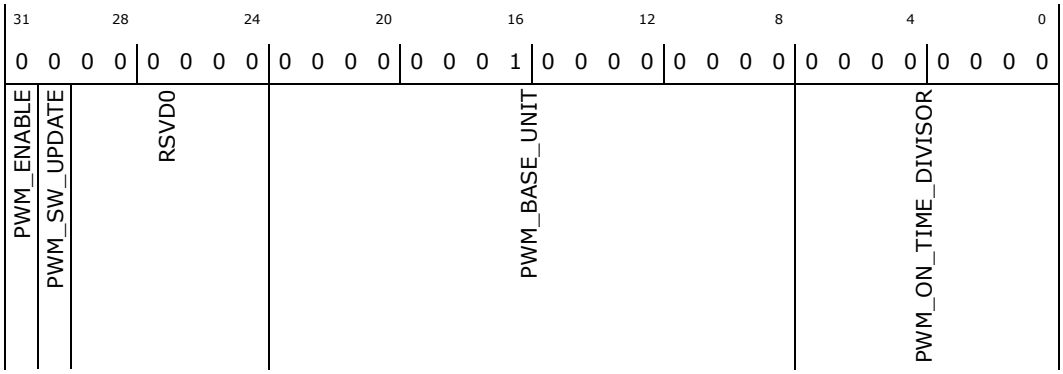
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 0h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:2] + 10h

Default: 00010000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**PWM Enable (PWM_ENABLE):** 0 = Disable PWM Output 1 = Enable PWM Output
30	0x0 RW	**PWM Software Update (PWM_SW_UPDATE):** Indication that there is an update to PWM settings pending. SW sets this bit to 1 when updating the PWM_base_unit or PWM_on_time_divisor fields. The PWM module will apply the new settings at the end of the current cycle and reset this bit. 0 = No updates pending 1 = Update pending
29:24	0x0 RO	**RSVD0:** Reserved
23:8	0x100 RW	**PWM Base Unit (PWM_BASE_UNIT):** Base unit register. Unsigned 8 integer bits, 8 fraction bits. Used to determine PWM output frequency.
7:0	0x0 RW	**PWM On Time Divisor (PWM_ON_TIME_DIVISOR):** PWM duty cycle = PWM_on-time_divisor/256.

9.32.2 software reset (RESETS)—Offset 804h

software reset

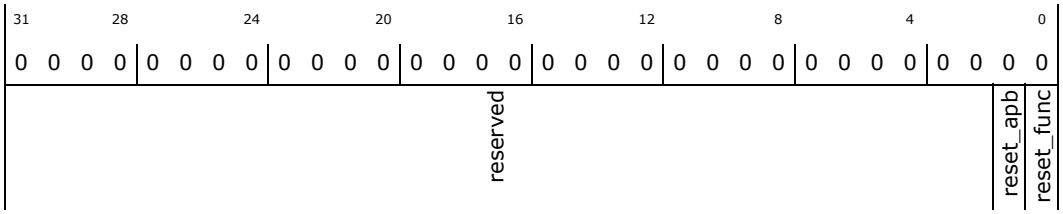
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 804h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:2] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Reserved (reserved):** Reserved
1	0x0 RW	**reset_apb:** reset the apb domain
0	0x0 RW	**reset_func:** reset the func clock domain

9.32.3 General purpose register (GENERAL)—Offset 808h

General purpose register

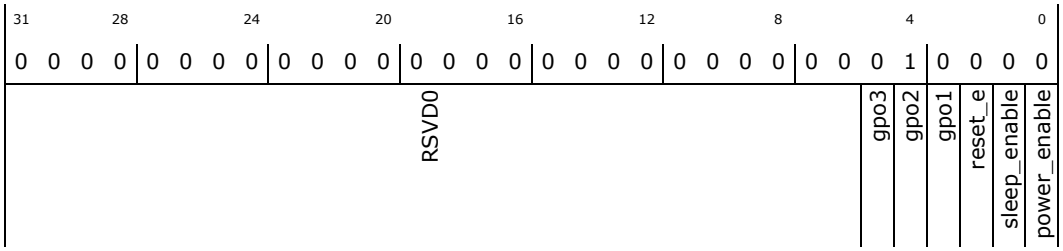
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [BAR] + 808h

BAR Type: PCI Configuration Register (Size: 32 bits)
BAR Reference: [B:0, D:30, F:2] + 10h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**RSVD0:** Reserved
5	0x0 RW	**gpo3:** not applicable
4	0x1 RW	**gpo2:** not applicable
3	0x0 RW	**gpo1:** This bit is re-used to support 32kHz slow mode. Default is 19.2MHz as PWM source clock
2	0x0 RW	**reset_e:** not applicable

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**sleep_enable:** not applicable
0	0x0 RW	**power_enable:** not applicable

10 Platform Controller Unit (PCU)

10.1 PCU iLB LPC Port 80h I/O Registers

Table 96. Summary of PCU iLB LPC Port 80h I/O Registers—

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
80–80h	1	"PC80—Offset 80h" on page 4807	00h
81–81h	1	"PC81—Offset 81h" on page 4807	00h
82–82h	1	"PC82—Offset 82h" on page 4807	00h
83–83h	1	"PC83—Offset 83h" on page 4808	00h
84–84h	1	"PC84—Offset 84h" on page 4808	00h
85–85h	1	"PC85—Offset 85h" on page 4809	00h
86–86h	1	"PC86—Offset 86h" on page 4809	00h
87–87h	1	"PC87—Offset 87h" on page 4810	00h
88–88h	1	"PC88—Offset 88h" on page 4810	00h
89–89h	1	"PC89—Offset 89h" on page 4810	00h
8A–8Ah	1	"PC8A—Offset 8Ah" on page 4811	00h
8B–8Bh	1	"PC8B—Offset 8Bh" on page 4811	00h
8C–8Ch	1	"PC8C—Offset 8Ch" on page 4812	00h
8D–8Dh	1	"PC8D—Offset 8Dh" on page 4812	00h
8E–8Eh	1	"PC8E—Offset 8Eh" on page 4813	00h
8F–8Fh	1	"PC8F—Offset 8Fh" on page 4813	00h

10.1.1 PC80—Offset 80h

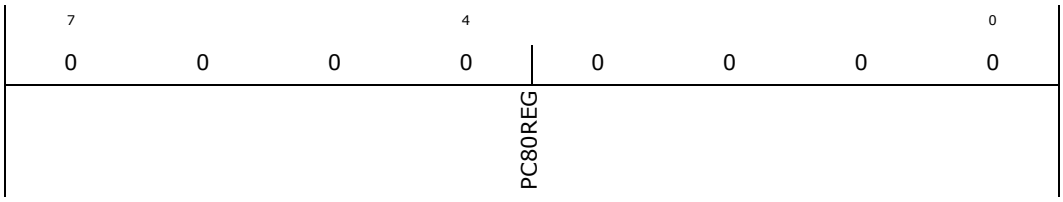
Post Code 80 regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 80h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**PC80REG:** Post Code 80 regsiter

10.1.2 PC81—Offset 81h

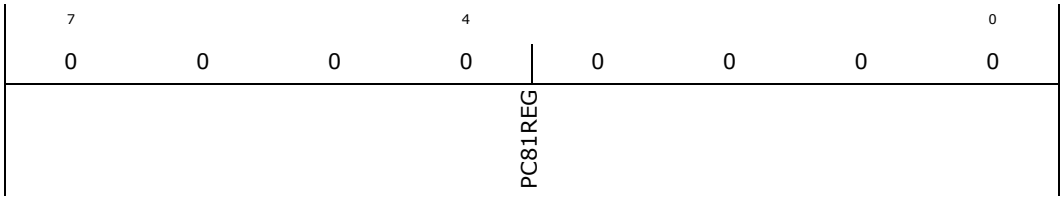
Post Code 81 regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 81h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	X RW	**PC81REG:** Post Code 81 regsiter

10.1.3 PC82—Offset 82h

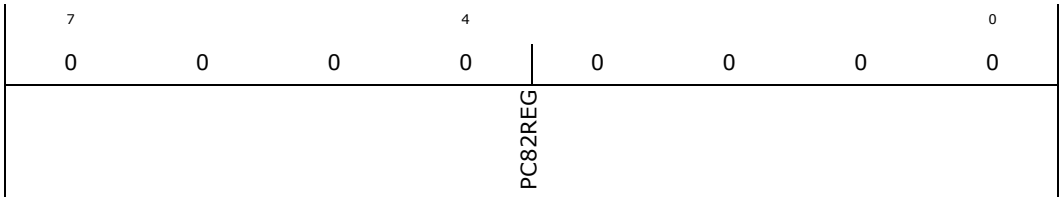
Post Code 82 regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 82h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	X RW	**PC82REG:** Post Code 82 regsiter

10.1.4 PC83—Offset 83h

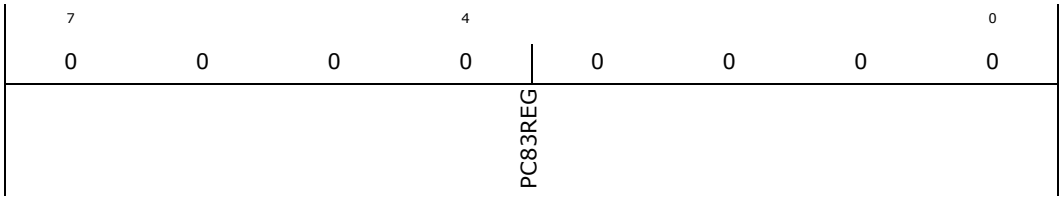
Post Code 83 regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 83h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	X RW	**PC83REG:** Post Code 83 regsiter

10.1.5 PC84—Offset 84h

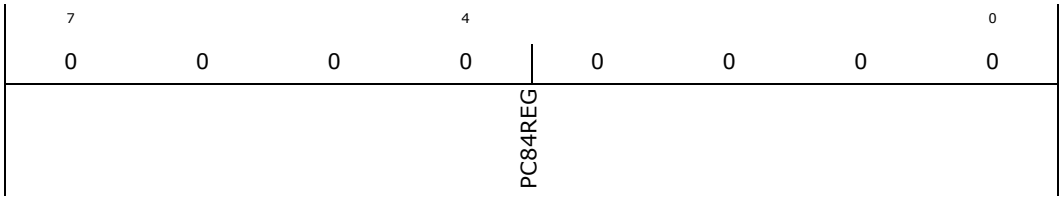
Post Code 84 regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 84h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	X RW	**PC80REG (PC84REG):** Post Code 84 regsiter

10.1.6 PC85—Offset 85h

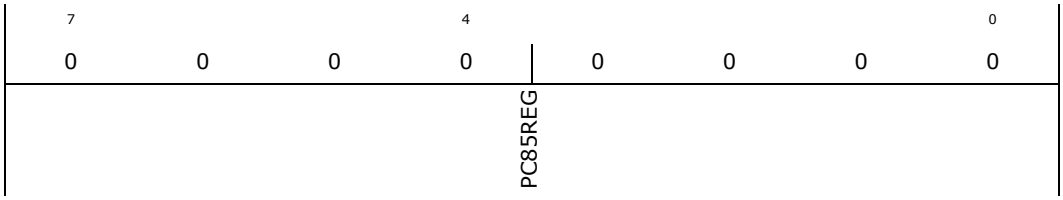
Post Code 85 regsiter

Access Method

Type: I/O Register (Size: 8 bits)

Offset: 85h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	X RW	**PC85REG:** Post Code 85 regsiter

10.1.7 PC86—Offset 86h

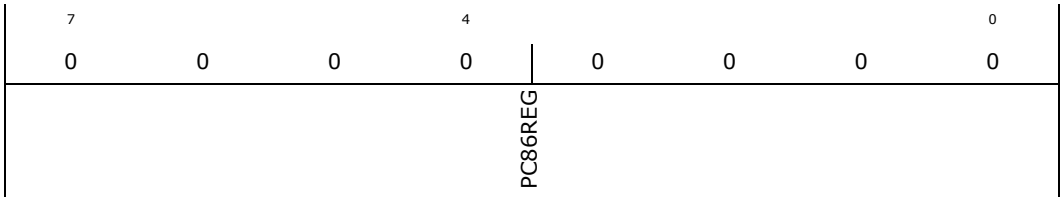
Post Code 86 regsiter

Access Method

Type: I/O Register (Size: 8 bits)

Offset: 86h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	X RW	**PC86REG:** Post Code 86 regsiter

10.1.8 PC87—Offset 87h

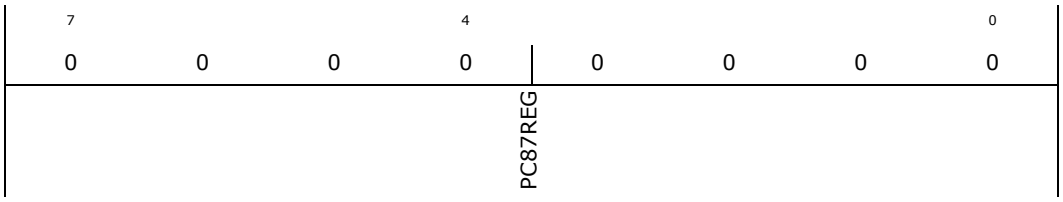
Post Code 87 regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 87h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	X RW	**PC87REG:** Post Code 87 regsiter

10.1.9 PC88—Offset 88h

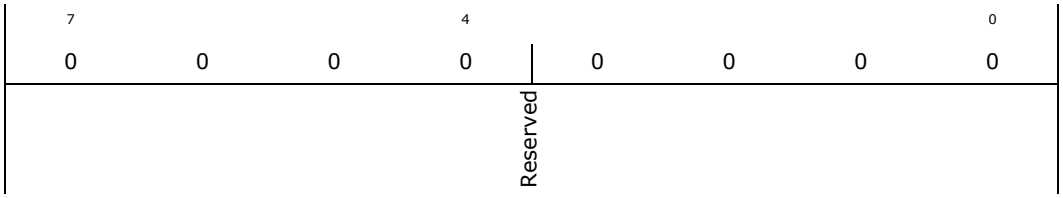
Post Code 88 regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 88h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**Reserved:** Reserved.

10.1.10 PC89—Offset 89h

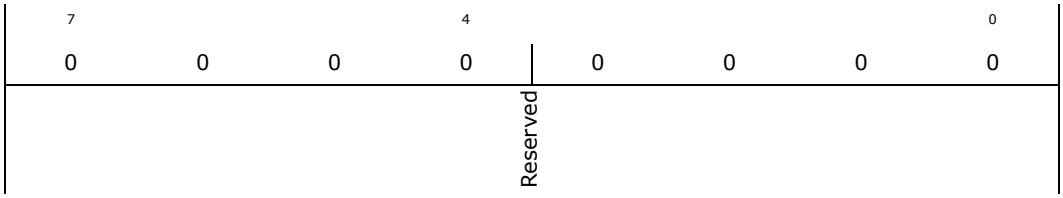
Post Code 89 regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 89h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**Reserved:** Reserved.

10.1.11 PC8A—Offset 8Ah

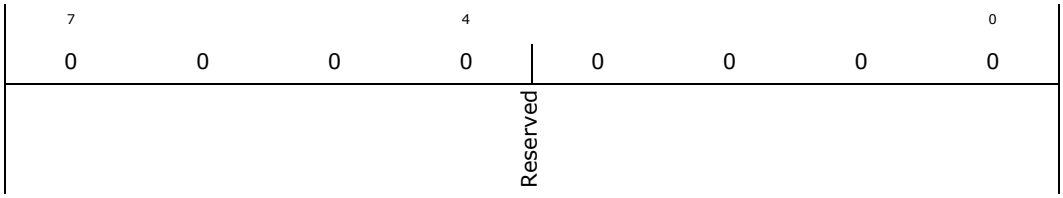
Post Code 8A regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 8Ah

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**Reserved:** Reserved.

10.1.12 PC8B—Offset 8Bh

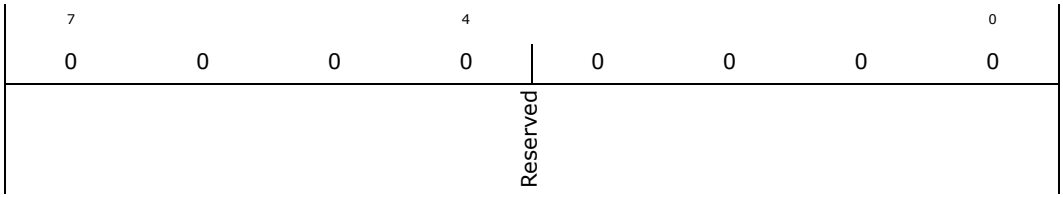
Post Code 8B regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 8Bh

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**Reserved:** Reserved.

10.1.13 PC8C—Offset 8Ch

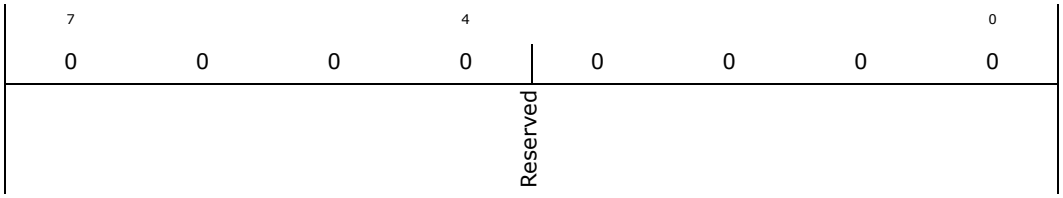
Post Code 8C regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 8Ch

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**Reserved:** Reserved.

10.1.14 PC8D—Offset 8Dh

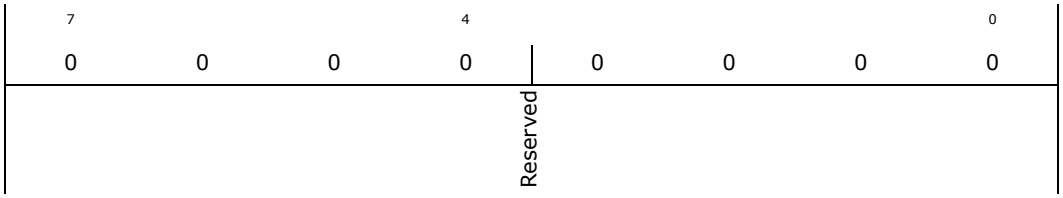
Post Code 8D regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 8Dh

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**Reserved:** Reserved.

10.1.15 PC8E—Offset 8Eh

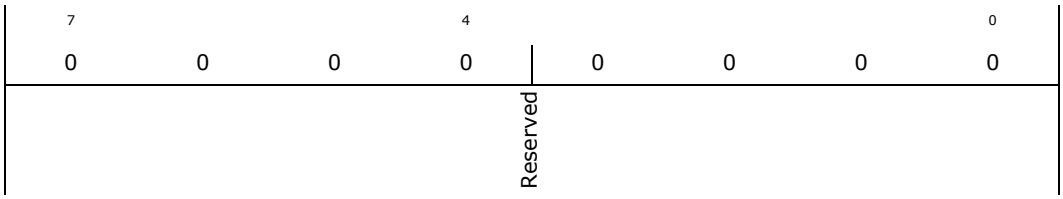
Post Code 8E regsiter

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 8Eh

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**Reserved:** Reserved.

10.1.16 PC8F—Offset 8Fh

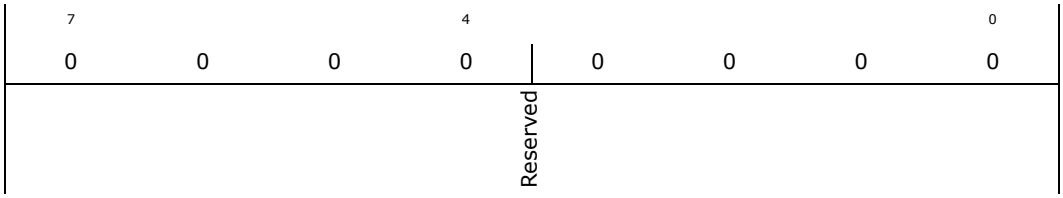
Post Code 8F regsiter

Access Method

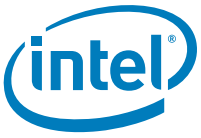
Type: I/O Register
(Size: 8 bits)

Offset: 8Fh

Default: 00h



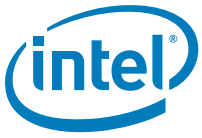
Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RO	**Reserved:** Reserved.



10.2 PCU PMC Memory Mapped I/O Registers

Table 97. Summary of PCU PMC Memory Mapped I/O Registers—PMC_BASE_ADDRESS

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"PRSTS - Power and Reset Status (PRSTS)—Offset 0h" on page 4817	00000000h
4–7h	4	"Bios communication register for PMC (BIOS_COMM_SPARE1)—Offset 4h" on page 4818	00000000h
8–Bh	4	"PM_CFG - Power Management Configuration (PMC_CFG)—Offset 8h" on page 4819	00000000h
C–Fh	4	"MTPMC - Message to PMC (MTPMC)—Offset 10h" on page 4820	00000000h
10–13h	4	"MTPMC - Message to PMC (MTPMC)—Offset 10h" on page 4820	00000000h
14–17h	4	"Bios communication register for PMC (BIOS_COMM_SPARE2)—Offset 14h" on page 4821	00000000h
18–1Bh	4	"Bios communication register for PMC (BIOS_COMM_SPARE3)—Offset 18h" on page 4822	00000000h
1C–1Fh	4	"Bios communication register for PMC (BIOS_COMM_SPARE4)—Offset 1Ch" on page 4823	00000000h
20–23h	4	"General PM Configuration 1 (GEN_PMCON1)—Offset 20h" on page 4824	00004004h
24–27h	4	"General PM Configuration 2 (GEN_PMCON2)—Offset 24h" on page 4828	00000000h
28–2Bh	4	"MFPMC - Message from PMC (MFPMC)—Offset 28h" on page 4830	00000000h
2C–2Fh	4	"SEC_STS - SEC Status (SEC_STS)—Offset 2Ch" on page 4830	00000000h
30–33h	4	"Configured Revision ID (CRID)—Offset 30h" on page 4831	00000000h
34–37h	4	"Function Disable (FUNC_DIS)—Offset 34h" on page 4831	00000000h
38–3Bh	4	"Function Disable 2 (FUNC_DIS_2)—Offset 38h" on page 4832	00000000h
3C–3Fh	4	"S0ix wake enable (S0IX_WAKE_EN)—Offset 3Ch" on page 4833	0FFFFFFFh
40–43h	4	"S0ix wake Status (S0IX_WAKE_STS)—Offset 40h" on page 4834	00000000h
44–47h	4	"S0ix control (S0IX_CTL)—Offset 44h" on page 4836	00000050h
48–4Bh	4	"ETR - Extended Test Mode Register (ETR)—Offset 48h" on page 4837	00230000h
4C–4Fh	4	"TNTE_TMR - Always running timer - can be used to create events timer status (TNTE_TMR)—Offset 4Ch" on page 4838	00000000h
50–53h	4	"VLT - Voltage Detect Register (VLT)—Offset 50h" on page 4838	00000000h
54–57h	4	"S0IA_TMR_UPPER - S0I Ready Residency Timer (S0IA_TMR_UPPER)—Offset 54h" on page 4839	00000000h
58–5Bh	4	"GPIO_ROUT - GPIO_ROUT register (GPIO_ROUT)—Offset 58h" on page 4839	00000000h
5C–5Fh	4	"S0IA_TMR_UPPER - S0I Ready Residency Timer (S0IA_TMR_UPPER)—Offset 54h" on page 4839	00000000h
60–63h	4	"PLT_CLK_CTL_0 - Platform Clock Control 0 (PLT_CLK_CTL_0)—Offset 60h" on page 4840	00000003h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
64–67h	4	"PLT_CLK_CTL_1 - Platform Clock Control 1 (PLT_CLK_CTL_1)—Offset 64h" on page 4841	00000003h
68–6Bh	4	"PLT_CLK_CTL_2 - Platform Clock Control 2 (PLT_CLK_CTL_2)—Offset 68h" on page 4841	00000003h
6C–6Fh	4	"PLT_CLK_CTL_3 - Platform Clock Control 3 (PLT_CLK_CTL_3)—Offset 6Ch" on page 4842	00000003h
70–73h	4	"PLT_CLK_CTL_4 - Platform Clock Control 4 (PLT_CLK_CTL_4)—Offset 70h" on page 4843	00000003h
74–77h	4	"PLT_CLK_CTL_5 - Platform Clock Control 5 (PLT_CLK_CTL_5)—Offset 74h" on page 4843	00000003h
78–7Bh	4	"S0IR_TMR_UPPER - S0I Ready Residency Timer (S0IR_TMR_UPPER)—Offset 78h" on page 4844	00000000h
7C–7Fh	4	"S0I1_TMR_UPPER - S0I1 Ready Residency Timer (S0I1_TMR_UPPER)—Offset 7Ch" on page 4844	00000000h
80–83h	4	"S0IR_TMR_UPPER - S0I Ready Residency Timer (S0IR_TMR_UPPER)—Offset 78h" on page 4844	00000000h
84–87h	4	"S0I1_TMR_UPPER - S0I1 Ready Residency Timer (S0I1_TMR_UPPER)—Offset 7Ch" on page 4844	00000000h
88–8Bh	4	"S0I2_TMR - S0I2 Residency Timer (S0I2_TMR)—Offset 88h" on page 4846	00000000h
8C–8Fh	4	"S0I3_TMR - S0I3 Residency Timer (S0I3_TMR)—Offset 8Ch" on page 4846	00000000h
90–93h	4	"S0_TMR - S0 Residency Timer (S0_TMR)—Offset 90h" on page 4846	00000000h
94–97h	4	"S0I2_TMR_UPPER - S0I2 Residency Timer (S0I2_TMR_UPPER)—Offset 94h" on page 4847	00000000h
98–9Bh	4	"PSS - Power island Power Status (PSS)—Offset 98h" on page 4847	00006680h
9C–9Fh	4	"S0I3_TMR_UPPER - S0I3 Residency Timer (S0I3_TMR_UPPER)—Offset 9Ch" on page 4848	00000000h
A0–A3h	4	"D3_STS_0 - D3 Status register 0 (D3_STS_0)—Offset A0h" on page 4849	00000000h
A4–A7h	4	"D3_STS_1 - D3 Status register 1 (D3_STS_1)—Offset A4h" on page 4849	00000000h
A8–ABh	4	"D3_STDBY_STS_0 - D3 Standby Status register 0 (D3_STDBY_STS_0)—Offset A8h" on page 4850	00000000h
AC–AFh	4	"D3_STDBY_STS_1 - D3 Standby Status register 1 (D3_STDBY_STS_1)—Offset ACh" on page 4851	00000000h
B0–B3h	4	"MTPMC_1 - Message to PMC 1 (MTPMC_1)—Offset B0h" on page 4851	00000000h
B4–B7h	4	"MTPMC_2 - Message to PMC 2 (MTPMC_2)—Offset B4h" on page 4852	00000000h
B8–BBh	4	"MTPMC_3 - Message to PMC 3 (MTPMC_3)—Offset B8h" on page 4852	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
BC–BFh	4	"MTPMC_4 - Message to PMC 4 (MTPMC_4)—Offset BCh" on page 4852	00000000h
C0–C3h	4	"PME Status 0 - Status bit for PME messages (PME_STS)—Offset C0h" on page 4853	00000000h
C4–C7h	4	"GPE Level Edge mode (GPE_LEVEL_EDGE)—Offset C4h" on page 4853	00000000h
C8–CBh	4	"GPE polarity mode (GPE_POLARITY)—Offset C8h" on page 4854	00000000h
CC–CFh	4	"Lock Register (LOCK)—Offset CCh" on page 4854	00000000h
D0–D3h	4	"PCIE LTR (PCIE_LTR)—Offset D0h" on page 4855	00000000h
D4–D7h	4	"D3 Cold (D3_COLD)—Offset D4h" on page 4856	00000000h
D8–DBh	4	"DISABLE IPs (DISABLE_IPs_1)—Offset D8h" on page 4856	00000000h
DC–DFh	4	"DISABLE IPs (DISABLE_IPs_2)—Offset DCh" on page 4857	00000000h
E0–E3h	4	"D3 Defer for PMC FW (D3_DEFER_0)—Offset E0h" on page 4857	00000000h
E4–E7h	4	"D3 Defer for PMC FW (D3_DEFER_1)—Offset E4h" on page 4858	00000000h
EC–EFh	4	"Bios communication register for PMC (BIOS_COMM_SPARE0)—Offset ECh" on page 4858	00000000h
F0–F3h	4	"Virtual UART register (VUART1)—Offset F0h" on page 4859	00000000h
F4–F7h	4	"Virtual UART register (VUART2)—Offset F4h" on page 4860	00000000h
F8–FBh	4	"Virtual UART register (VUART3)—Offset F8h" on page 4860	00000000h
FC–FFh	4	"Virtual UART register (VUART4)—Offset FCh" on page 4860	00000000h

10.2.1 PRSTS - Power and Reset Status (PRSTS)—Offset 0h

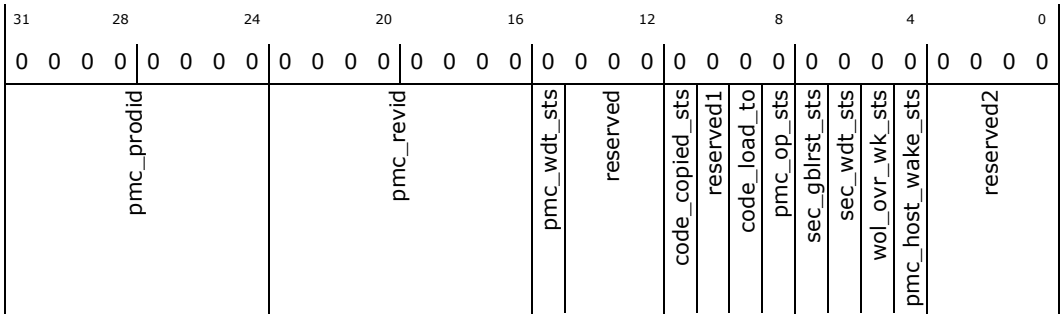
Bits in this register only need to be valid for reading when the Main power well is up. However, since some of the events may initially be detected while the Main power well is down, they are marked as suspend well bits. All suspend well bits in this register are reset by global reset#.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Power Management Controller Product ID (PMC_PRODID) (pmc_prodid):** This field communicates the Product Family of the power management functionality
23:16	0x0 RO	**Power Management Controller Revision ID (PMC_REVID) (pmc_revid):** This field communicates the implementation revision of the power management functionality.
15	0x0 RW/1C	**PMC Watchdog Timer Status (PMC_WDT_STS) (pmc_wdt_sts):** This bit will be set to '1' when the PMC Watch Dog Timer triggers a reset. It will be cleared by a write of '1' by software.
14:12	0x0 RO	**reserved:** Reserved.
11	0x0 RO	**Code Copied Over Status (CODE_COPIED_STS) (code_copied_sts):** The SOC sets this bit when PMC code is successfully authenticated and loaded from the flash
10	0x0 RO	**reserved (reserved1):** Reserved.
9	0x0 RO	**Code Load Timeout Status (CODE_LOAD_TO) (code_load_to):** The SOC sets this bit if the loading function fails to complete within a reasonable time limit. This bit remains valid after a PMC Code load is attempted until the next global reset
8	0x0 RO	**PMC Operational Status (PMC_OP_STS) (pmc_op_sts):** The SOC sets this bit when the PMC becomes operational after completing the Code Load. BIOS must wait for this bit to be set before performing resets or sleep events. This bit remains valid after a PMC Code load until the next global reset

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW/1C	**SEC Watch Dog Timer Status (SEC_GBLRST_STS) (sec_gblrst_sts):** This bit will be set to '1' when the SEC FW triggers a reset. It will be cleared by a write of '1' by software.
6	0x0 RW/1C	**SEC Watch Dog Timer Status (SEC_WDT_STS) (sec_wdt_sts):** This bit will be set to '1' when the SEC Watch Dog Timer triggers a reset. It will be cleared by a write of '1' by software.
5	0x0 RW/1C	**Wake On LAN Override Wake Status (WOL_OVR_WK_STS) (wol_ovr_wk_sts):** This bit gets set when integrated LAN Signals a Power Management Event AND the system is in S5. BIOS can read this status bit to determine this wake source. Software clears this bit by writing a 1 to it.
4	0x0 RW/1C	**PMC_HOST_WAKE_STS (PMC_HOST_WAKE_STS) (pmc_host_wake_sts):** The SOC Power Management Controller sets this bit if it wakes the host for reasons other than typical host-visible wake events. This status bit provides information to BIOS that the PMC caused the wake.
3:0	0x0 RO	**reserved2:** Reserved.

10.2.2 Bios communication register for PMC (BIOS_COMM_SPARE1)—Offset 4h

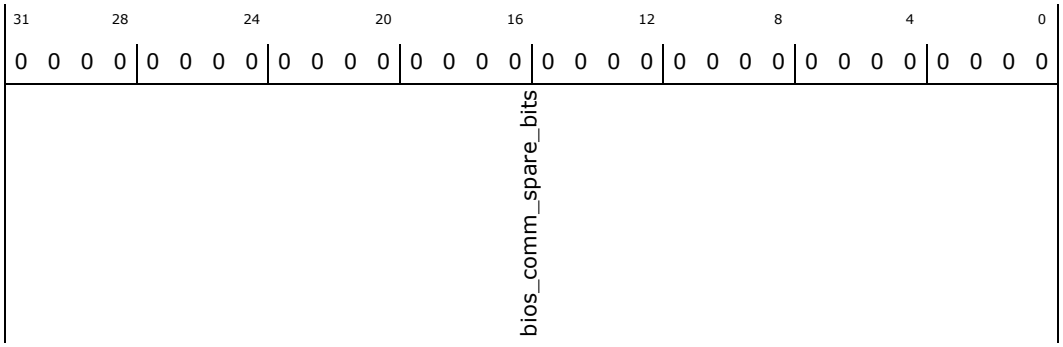
Bios communication requirements we may need/discover

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**BIOS_COMM_SPARE (bios_comm_spare_bits):** Bios communication register - enables BIOS communication flags to be posted to PMC FW for later use NOTE: Access needs to be through IOSF primary in order for PMC to service a request BIOS_COMM_SPARE_0/1/2/3/4 [31] : PMC FW Update in progress 1'b1 - PMC FW has acknowledged the request from BIOS to update PMC behavior, is processing request 1'b0 - PMC FW not processing a BIOS update BIOS_COMM_SPARE_0/1/2/3/4 [30:16] : RESERVED BIOS_COMM_SPARE_0/1/2/3/4 [15] : BIOS Update request 1'b1 - BIOS RMWs setting this bit to 1'b1 when requesting a change in behavior on PMCs part 1'b0 - PMC FW only write 1'b0 to this bit when firmware update request has completed (PMC FW will also set BIOS_COMM[31] = 0 BIOS_COMM_SPARE_0 [14:2] : RESERVED FOR FUTURE USE BIOS_COMM_SPARE_0 [3] : LPE OSC force ON enable 1'b1 - Force LPE OSC clock on (CCU CLGATE_EN_3) 1'b0 - Release LPE OSC clock force on (CCU CLGATE_EN_3) BIOS_COMM_SPARE_0 [2] : RESERVED FOR FUTURE USE BIOS_COMM_SPARE_0 [1] : SSIC PHY common power lane request change (pmu_mphy_cmnln_core_pwr_up) 1'b1 - assert power 1'b0 - deassert power BIOS_COMM_SPARE_0 [0] : PERIODIC_GPIO_RCOMP_Enable, BIOS flag to PMC which specifies that PMC FW is required to periodically update the GPIO RCOMP values for LPC and Fast SPI 1'b1 - enable 1'b0 - disable BIOS_COMM_SPARE_1/2/3/4 [14:0] : RESERVED FOR FUTURE USE

10.2.3 PM_CFG - Power Management Configuration (PMC_CFG)—Offset 8h

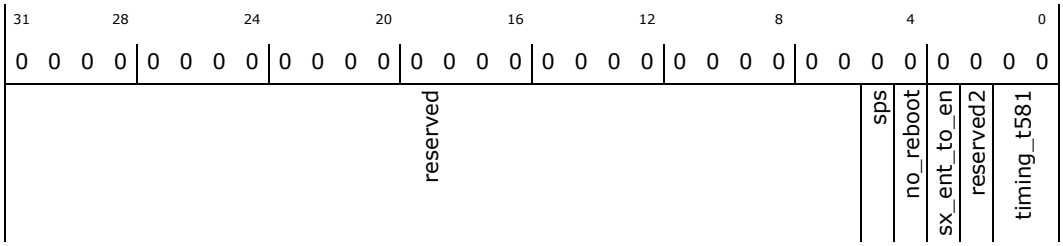
This register contains misc. fields used to configure the SOC's power management behavior.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**reserved:** Reserved.
5	0x0 RW	**Shutdown Policy Select (SPS) (sps):** When cleared (default) the SOC will drive INIT# in response to the shutdown Message. When set to 1, SOC will treat the shutdown message similar to receiving a CF9h I/O write, and will drive PMU_PLTRST active. Note: This register is reset any time PMU_PLTRST asserts.
4	0x0 RW	**No Reboot (NO_REBOOT) (no_reboot):** This bit is set when the No Reboot strap is sampled high on COREPWROK. This bit may be set or cleared by software if the strap is sampled low but may not override the strap when it indicates No Reboot. When set, the TCO timer will count down and generate the SMI# on the first timeout, but will not reboot on the second timeout.
3	0x0 RW	**S1/3/4/5 Entry Timeout Enable (SX_ENT_TO_EN) (sx_ent_to_en):** This policy bit determines whether the SOC will apply a timeout to the S1/S3/S4/S5 entry flow. If this timeout is enabled and the entry flow appears to be hung, the SOC will trigger a straight-to-S5 global reset. Encodings: 0: Timeout disabled (default) 1: Timeout enabled reset_type=RSMRST_B
2	0x0 RO	**reserved (reserved2):** Reserved.
1:0	0x0 RW	**Timing t581 (TIMING_T581) (timing_t581):** This field configures the t581 timing involved in the power down flow (CPU Power Good indication inactive to PLL Enable inactive). Encodings (all min timings): 00: 10 us (default) 01: 100 us 10: 1 ms 11: 10 ms reset_type=Resume Well Reset#

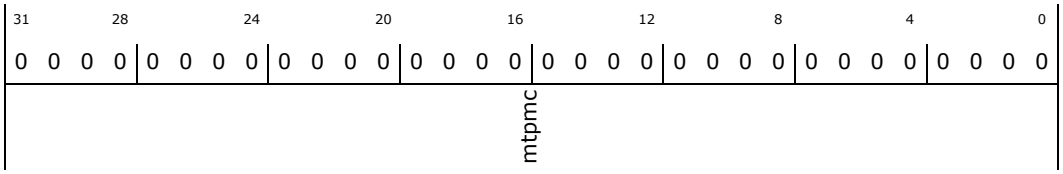
10.2.4 MTPMC - Message to PMC (MTPMC)—Offset 10h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Message to PMC (MTPMC) (mtpmc):** A write to any of the bytes in this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_1_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. In the case of a message that involves a response from the PMC (such as a PMC XRAM read), the host must also consume any data returned by the PMC in the Message from PMC register (MFPMC) before initiating another message

10.2.5 Bios communication register for PMC (BIOS_COMM_SPARE2)—Offset 14h

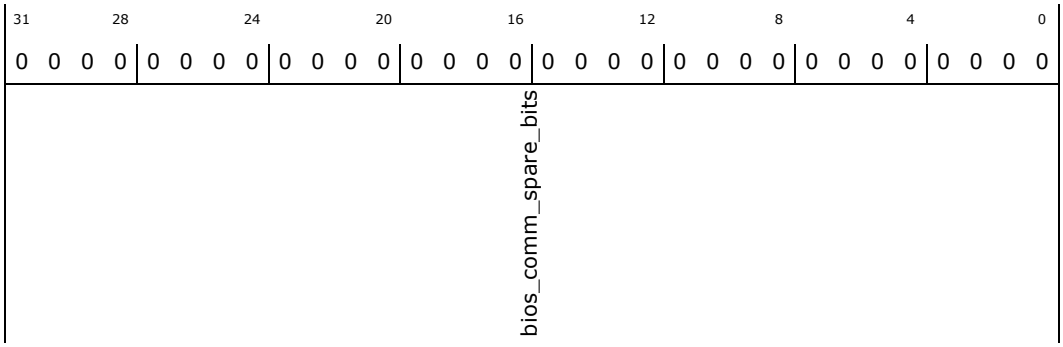
Bios communication requirements we may need/discover

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**BIOS_COMM_SPARE (bios_comm_spare_bits):** Bios communication register - enables BIOS communication flags to be posted to PMC FW for later use NOTE: Access needs to be through IOSF primary in order for PMC to service a request BIOS_COMM_SPARE_0/1/2/3/4 [31] : PMC FW Update in progress 1'b1 - PMC FW has acknowledged the request from BIOS to update PMC behavior, is processing request 1'b0 - PMC FW not processing a BIOS update BIOS_COMM_SPARE_0/1/2/3/4 [30:16] : RESERVED BIOS_COMM_SPARE_0/1/2/3/4 [15] : BIOS Update request 1'b1 - BIOS RMWs setting this bit to 1'b1 when requesting a change in behavior on PMCs part 1'b0 - PMC FW only write 1'b0 to this bit when firmware update request has completed (PMC FW will also set BIOS_COMM[31] = 0 BIOS_COMM_SPARE_0 [14:2] : RESERVED FOR FUTURE USE BIOS_COMM_SPARE_0 [3] : LPE OSC force ON enable 1'b1 - Force LPE OSC clock on (CCU CLGATE_EN_3) 1'b0 - Release LPE OSC clock force on (CCU CLGATE_EN_3) BIOS_COMM_SPARE_0 [2] : RESERVED FOR FUTURE USE BIOS_COMM_SPARE_0 [1] : SSIC PHY common power lane request change (pmu_mphy_cmnln_core_pwr_up) 1'b1 - assert power 1'b0 - deassert power BIOS_COMM_SPARE_0 [0] : PERIODIC_GPIO_RCOMP_Enable, BIOS flag to PMC which specifies that PMC FW is required to periodically update the GPIO RCOMP values for LPC and Fast SPI 1'b1 - enable 1'b0 - disable BIOS_COMM_SPARE_1/2/3/4 [14:0] : RESERVED FOR FUTURE USE

10.2.6 Bios communication register for PMC (BIOS_COMM_SPARE3)—Offset 18h

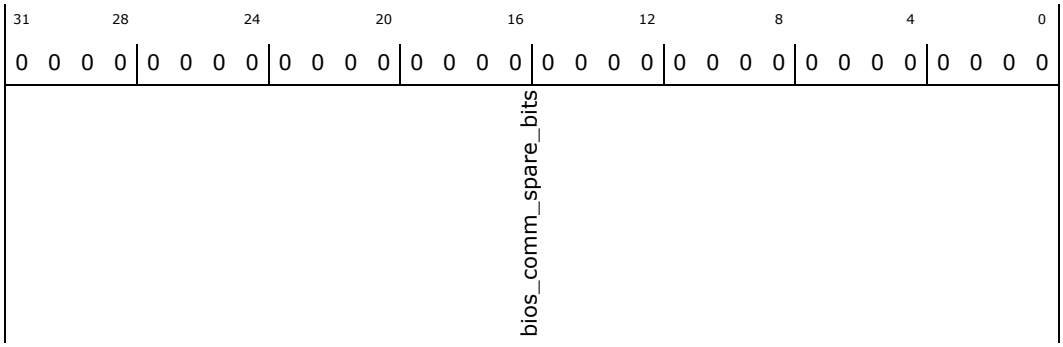
Bios communication requirements we may need/discover

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 18h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**BIOS_COMM_SPARE (bios_comm_spare_bits):** Bios communication register - enables BIOS communication flags to be posted to PMC FW for later use NOTE: Access needs to be through IOSF primary in order for PMC to service a request BIOS_COMM_SPARE_0/1/2/3/4 [31] : PMC FW Update in progress 1'b1 - PMC FW has acknowledged the request from BIOS to update PMC behavior, is processing request 1'b0 - PMC FW not processing a BIOS update BIOS_COMM_SPARE_0/1/2/3/4 [30:16] : RESERVED BIOS_COMM_SPARE_0/1/2/3/4 [15] : BIOS Update request 1'b1 - BIOS RMWs setting this bit to 1'b1 when requesting a change in behavior on PMCs part 1'b0 - PMC FW only write 1'b0 to this bit when firmware update request has completed (PMC FW will also set BIOS_COMM[31] = 0 BIOS_COMM_SPARE_0 [14:2] : RESERVED FOR FUTURE USE BIOS_COMM_SPARE_0 [3] : LPE OSC force ON enable 1'b1 - Force LPE OSC clock on (CCU CLGATE_EN_3) 1'b0 - Release LPE OSC clock force on (CCU CLGATE_EN_3) BIOS_COMM_SPARE_0 [2] : RESERVED FOR FUTURE USE BIOS_COMM_SPARE_0 [1] : SSIC PHY common power lane request change (pmu_mphy_cmnln_core_pwr_up) 1'b1 - assert power 1'b0 - deassert power BIOS_COMM_SPARE_0 [0] : PERIODIC_GPIO_RCOMP_Enable, BIOS flag to PMC which specifies that PMC FW is required to periodically update the GPIO RCOMP values for LPC and Fast SPI 1'b1 - enable 1'b0 - disable BIOS_COMM_SPARE_1/2/3/4 [14:0] : RESERVED FOR FUTURE USE

10.2.7 Bios communication register for PMC (BIOS_COMM_SPARE4)—Offset 1Ch

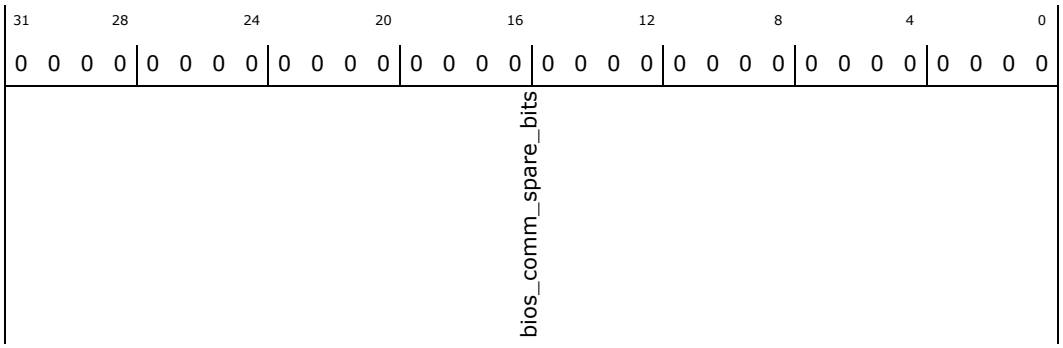
Bios communication requirements we may need/discover

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 1Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**BIOS_COMM_SPARE (bios_comm_spare_bits):** Bios communication register - enables BIOS communication flags to be posted to PMC FW for later use NOTE: Access needs to be through IOSF primary in order for PMC to service a request BIOS_COMM_SPARE_0/1/2/3/4 [31] : PMC FW Update in progress 1'b1 - PMC FW has acknowledged the request from BIOS to update PMC behavior, is processing request 1'b0 - PMC FW not processing a BIOS update BIOS_COMM_SPARE_0/1/2/3/4 [30:16] : RESERVED BIOS_COMM_SPARE_0/1/2/3/4 [15] : BIOS Update request 1'b1 - BIOS RMWs setting this bit to 1'b1 when requesting a change in behavior on PMCs part 1'b0 - PMC FW only write 1'b0 to this bit when firmware update request has completed (PMC FW will also set BIOS_COMM[31] = 0 BIOS_COMM_SPARE_0 [14:2] : RESERVED FOR FUTURE USE BIOS_COMM_SPARE_0 [3] : LPE OSC force ON enable 1'b1 - Force LPE OSC clock on (CCU CLGATE_EN_3) 1'b0 - Release LPE OSC clock force on (CCU CLGATE_EN_3) BIOS_COMM_SPARE_0 [2] : RESERVED FOR FUTURE USE BIOS_COMM_SPARE_0 [1] : SSIC PHY common power lane request change (pmu_mphy_cmnln_core_pwr_up) 1'b1 - assert power 1'b0 - deassert power BIOS_COMM_SPARE_0 [0] : PERIODIC_GPIO_RCOMP_Enable, BIOS flag to PMC which specifies that PMC FW is required to periodically update the GPIO RCOMP values for LPC and Fast SPI 1'b1 - enable 1'b0 - disable BIOS_COMM_SPARE_1/2/3/4 [14:0] : RESERVED FOR FUTURE USE

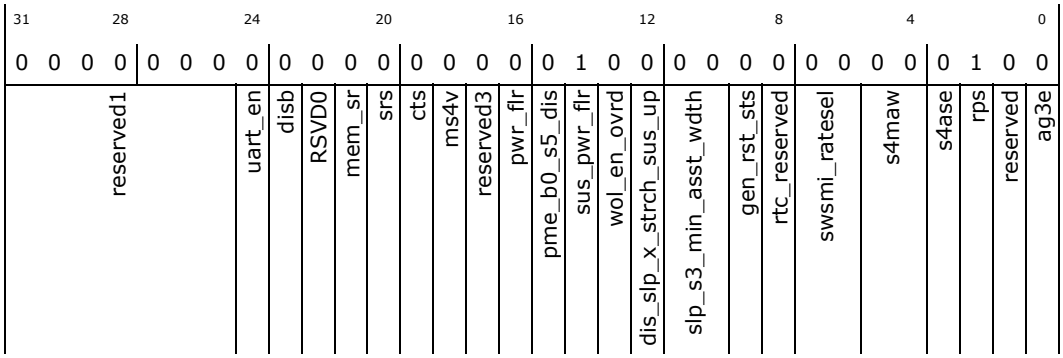
10.2.8 General PM Configuration 1 (GEN_PMCON1)—Offset 20h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 20h

Default: 00004004h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**reserved1:** Reserved.
24	0x0 RW	**UART Enable (UART_EN) (uart_en):** When set, PMC enables UART debug port
23	0x0 RW	**DRAM Initialization Scratchpad Bit (DISB) (disb):** This bit does not effect hardware functionality in any way. It is provided as a scratchpad bit that is maintained through main power well resets and CF9h-initiated resets. BIOS is expected to set this bit prior to starting the DRAM initialization sequence and to clear this bit after completing the DRAM initialization sequence. BIOS can detect that a DRAM initialization sequence was interrupted by a reset by reading this bit during the boot sequence. If the bit is 1, then the DRAM initialization was interrupted. This bit is reset by the assertion of the RSMRST_B pin.
22	0x0 RO	**RSVD0:** Reserved
21	0x0 RO	**Memory Placed in Self-Refresh (MEM_SR) (mem_sr):** This bit will be set to 1 if DRAM should have remained powered and held in Self-Refresh through the last power state transition (i.e. the last time the system left S0). The scenarios where this should be the case are: - successful S3 entry and exit - successful Host partition reset without power cycle This bit will be cleared whenever the SOC begins a transition out of S0. Note: This bit should not be consulted upon wake from S1, as that state does not involve the same type of handshake or placing memory into Self-Refresh. It is assumed that software is already aware that memory context is not impacted by S1 and therefore does not need to check this bit. reset_type=global reset
20	0x0 RW/1C	**System Reset Status (SRS) (srs):** SOC sets this bit when the PMU_RESETBUTTON_B# button is pressed. BIOS is expected to read this bit and clear it if it is set. This bit is also reset by RSMRST_B and CF9h resets. reset_type=Resume Well Reset#
19	0x0 RW/1C	**CPU Thermal Trip Status (CTS) (cts):** This bit is set when the SOC thermal trip active while the system is in a valid state to honor the pin. This bit is also reset by RSMRST_B and CF9h resets. It is not reset by the shutdown and reboot associated with the thermal trip event. reset_type=Resume Well Reset#

Bit Range	Default & Access	Field Name (ID): Description
18	0x0 RW/1C	**Minimum PMU_SLP_S4_B Assertion Width Violation Status (MS4V) (ms4v):** Hardware sets this bit when the PMU_SLP_S4_B assertion width is less than the time programmed in the PMU_SLP_S4_B Minimum Assertion Width field. The SOC begins the timer when PMU_SLP_S4_B pin is asserted during S4/S5 entry, or when the RSMRST_B input is deasserted during SUS well power-up. The status bit is cleared by software writing a 1 to the bit. Note that this bit is functional regardless of the value in the PMU_SLP_S4_B Assertion Stretch Enable and the Disable-SLP_X-Stretching-After-SUS-Power-Failure bits. This bit is reset by the assertion of the RSMRST_B pin, but can be set in some cases before the default value is readable. reset_type=RSMRST_B
17	0x0 RO	**reserved3:** Reserved.
16	0x0 RW/1C	**COREPWROK Failure (PWR_FLR) (pwr_flr):** Intel SOC sets this bit any time COREPWROK goes low if the system was in an S0 or S1 state. The bit will be cleared only by software writing a 1 back to the bit or by SUS well power loss. reset_type=global reset
15	0x0 RW	**PME B0 S5 Disable (PME_B0_S5_DIS) (pme_b0_s5_dis):** When set to '1', this bit blocks wake events from PME_B0_STS in S5, regardless of the state of PME_B0_EN. When cleared (default), wake events from PME_B0_STS are allowed in S5 if PME_B0_EN = '1'. Wakes from power states other than S5 are not affected by this policy bit. The net effect of setting PME_B0_S5_DIS = '1' is described by the truth table below: Y = Wake N = Don't wake B0 = PME_B0_EN OV = WOL Enable Override B0/OV | S1/S3/S4 | S5 00 | N | N 01 | N | Y (LAN only) 11 | Y (all PME B0 sources) | Y (LAN only) 10 | Y (all PME B0 sources) | N This bit is cleared by the SRTCRST_B pin. reset_type=SRTCRST_B
14	0x1 RW/1C	**SUS Well Power Failure (SUS_PWR_FLR) (sus_pwr_flr):** This bit is set to '1' whenever SUS well power is lost, as indicated by RSMRST_B assertion. Software writes a 1 to this bit to clear it. This bit is in the SUS well, and defaults to '1' based on RSMRST_B assertion (not cleared by any type of reset). Implementation Note: RSMRST_B is an asynchronous set term to this bit. reset_type=RSMRST_B
13	0x0 RW	**WOL Enable Override (WOL_EN_OVRD) (wol_en_ovrd):** When this bit is set to 1, the integrated LAN is enabled to wake the system from S5 regardless of the value in the PME_B0_EN bit in the GPE0a_EN register. This allows the system BIOS to enable Wake-On-LAN regardless of the policies selected through the operating system. This bit is maintained in the RTC power well, therefore permitting WOL following a surprise power failure even in cases in which the system may have been running in S0 without the PME Enables set. (Note that the LAN NVRAM configuration must support WOL after SUS power loss.) When this bit is cleared to 0, the wake-on-LAN policies are determined by OS-visible bits. This bit has no effect on wakes from S1, S3, or S4. This bit is cleared by the SRTCRST_B pin reset_type=SRTCRST_B

Bit Range	Default & Access	Field Name (ID): Description
12	0x0 RW	**Disable SLP_X Stretching After SUS Well Power Up (DIS_SLP_X_STRCH_SUS_UP) (dis_slp_x_strch_sus_up):** When this bit is set to 1, all SLP_* pin stretching is disabled when powering up after a SUS well power loss. When this bit is left at 0, SLP_* stretching will be performed after SUS power failure as enabled in various other fields. Note that if this bit is a 0, SLP_* stretch timers start on SUS well power up (the SOC has no ability to count stretch time while the SUS well is powered down). Setting this bit can therefore prevent long delays after SUS power loss which may be common in mobile platforms and in manufacturing flow testing, while still allowing for the full power cycling during S3, S4 and S5 states. If the platform guarantees minimum SUS power down residence in other ways, an additional SOC-induced delay is not needed or wanted. This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by the SRTCRST_B pin.
11:10	0x0 RW	**PMU_SLP_S3_B Minimum Assertion Width (SLP_S3_MIN_ASST_WDTH) (slp_s3_min_asst_wdth):** This 2-bit value indicates the minimum assertion width of the PMU_SLP_S3_B signal to guarantee that the Main power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00: 60 usec 01: 1 ms 10: 50 ms 11: 2 sec This field is not writable when the SLP_Sx# Stretching Policy Lock- Down bit is set. This bit is cleared by the RSMRST_B pin. reset_type=RSMRST_B
9	0x0 RW/1C	**General Reset Status (GEN_RST_STS) (gen_rst_sts):** This bit is set by hardware whenever PMU_PLTRST asserts for any reason other than going into a software-entered sleep state (via PM1_CNT.SLP_EN write). This bit is an optional tool to help BIOS determine when a reset might have collided with a wake from a valid sleep state. A possible usage model would be to consult and then write a '1' to clear this bit during the boot flow before determing what action to take based on reading PM1_STS.WAK_STS = '1'. If GEN_RST_STS = '1', the cold reset boot path could be followed rather than the resume path, regardless of the setting of WAK_STS. This bit does not affect SOC operation in any way, and can therefore be left set if BIOS chooses not to use it. This bit is set by global reset. reset_type=global reset
8	0x0 RW	**RTC_reserved (rtc_reserved):** reset_type=SRTCRST_B
7:6	0x0 RW	**SWSMI Rate Select (SWSMI_RATESEL) (swsmi_ratesel):** This 2-bit value indicates when the SWSMI timer will time out. Valid values are: 00 1.5ms +/- 0.6ms 01 16ms +/- 4ms 10 32ms +/- 4ms 11 64ms +/- 4ms These bits are not cleared by any type of reset except SRTCRST_B. Implementation Note: SWSMI is generated based on the internal free-running 1ms tick (to be accurate, it is 0.983ms/tick generated from 30ns * 2^15). Since the tick is free-running, the accuracy is within the following range. # of 0.983ms tick count SWSMI range 64ms SWSMI 62 -to- 63 60.946ms -to- 61.929ms 32ms SWSMI 31 -to- 32 30.473ms -to- 31.456ms 16ms SWSMI 15 -to- 16 14.745ms -to- 15.728ms 1.5ms SWSMI 1 -to- 2 0.983ms -to- 1.966ms reset_type=SRTCRST_B

Bit Range	Default & Access	Field Name (ID): Description
5:4	0x0 RW	**PMU_SLP_S4_B Minimum Assertion Width (S4MAW) (s4maw):** This 2-bit value indicates the minimum assertion width of the PMU_SLP_S4_B signal to guarantee that the DRAMs have been safely power-cycled. This value may be modified per platform depending on DRAM types, power supply capacitance, etc. Valid values are: - 11: 1 second - 10: 2 seconds - 01: 3 seconds - 00: 4 seconds This value is used in two ways: 1. If the PMU_SLP_S4_B assertion width is ever shorter than this time, a status bit is set for BIOS to read when S0 is entered 2. If enabled by bit 3 in this register, the hardware will prevent the PMU_SLP_S4_B signal from deasserting within this minimum time period after asserting. Note that the logic that measures this time is in the suspend power well. Therefore, when leaving a G3 state, the minimum time is measured from the deassertion of the internal suspend well reset (unless the Disable SLP_X Stretching After SUS Power Failure bit is set). This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. SRTCRST_B forces this field to the conservative default state (00b). reset_type=SRTCRST_B
3	0x0 RW	**PMU_SLP_S4_B Assertion Stretch Enable (S4ASE) (s4ase):** When set to 1, the PMU_SLP_S4_B pin will minimally assert for the time specified in bits 5:4 of this register. This bit is provided so that all DIMMs in the system can deterministically detect a power-cycle event for proper initialization. Note that there are behavioral changes that may be noticeable to the end-user when this bit is set. Resume times from S4 and S5 and power-up times from G3 may be delayed by several seconds. Cases in which this feature may not be desirable and therefore keeping the bit cleared are: - A customer decides the user confusion due to the hardware delay is a bigger issue than the potential DRAM issue - A customer decides the software status bit solution is adequate - A different DRAM type is used or the platform provides an external solution to solve the power-cycling issue - Validation regressions are impacted by the delay (especially after RSMRST_B deassertion) - Avoid potential resume time WHQL violations This bit is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by SRTCRST_B. reset_type=SRTCRST_B
2	0x1 RW	**RTC_PWR_STS (RPS) (rps):** Intel SOC will set this bit to 1 when RTEST_B indicates a weak or missing battery. The bit will remain set until the software clears it by writing a 0 back to this bit position. This bit is not cleared by any type of reset. reset_type=RTEST_B
1	0x0 RO	**reserved:** Reserved.
0	0x0 RW	**AFTERG3_EN (AG3E) (ag3e):** Determines what state to go to when power is reapplied after a power failure (G3 state). 0 = System will return to an S0 state (boot) after power is re-applied. 1 = System will return to the S5 state (except if it was in S4, in which case it will return to S4-like state). In the S5 state, the only enabled wake-up event is the Power Button or any enabled wake event that was preserved through the power failure. This bit is in the RTC well and is only cleared by SRTCRST_B assertion. reset_type=SRTCRST_B

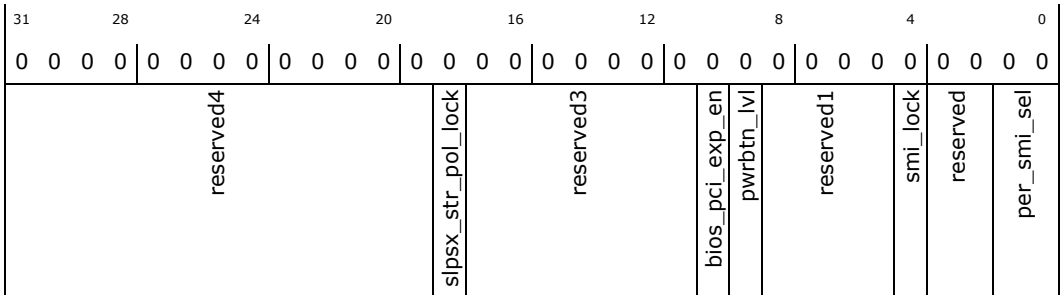
10.2.9 General PM Configuration 2 (GEN_PMCON2)—Offset 24h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 24h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0x0 RO	**reserved (reserved4):** Reserved.
18	0x0 RW	**SLP_Sx# Stretching Policy Lock-Down (SLPSX_STR_POL_LOCK) (slpsx_str_pol_lock):** When set to 1, this bit locks down the following fields: - GEN_PMCON_1.DIS_SLP_X_STRCH_SUSPF - GEN_PMCON_1.SLP_S3_MIN_ASST_WDTH - GEN_PMCON_1.S4MAW - GEN_PMCON_1.S4ASE Those bits become read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset.
17:11	0x0 RO	**reserved (reserved3):** Reserved.
10	0x0 RW	**BIOS PCI Express Enable (BIOS_PCI_EXP_EN) (bios_pci_exp_en):** This bit acts as a global enable for the SCI associated with the PCI express ports. If this bit is not set, then the various PCI Express ports cannot cause the PCI_EXP_STS bit to go active.
9	0x0 RO	**Power Button Level (PWRBTN_LVL) (pwrbtn_lvl):** This read-only bit indicates the current state of the PMU_PWRBTN_B signal. 1= High, 0 = Low. The value reflected in this bit is the debounced PMU_PWRBTN_B pin value that is seen at the output of a 16ms debouncer.
8:5	0x0 RO	**reserved (reserved1):** Reserved.
4	0x0 RW	**SMI Lock (SMI_LOCK) (smi_lock):** When this bit is set, writes to the GBL_SMI_EN bit will have no effect. Once the SMI_LOCK bit is set, writes of 0 to SMI_LOCK bit will have no effect (i.e. once set, this bit can only be cleared by PMU_PLTRST).
3:2	0x0 RO	**reserved:** Reserved.
1:0	0x0 RW	**Period SMI Select (PER_SMI_SEL) (per_smi_sel):** Software sets these bits to control the rate at which the periodic SMI# is generated: 00 = 64 seconds (default), 01 = 32 seconds, 10 = 16 seconds, 11 = 8 seconds Tolerance for the timer is +/- 1 second.

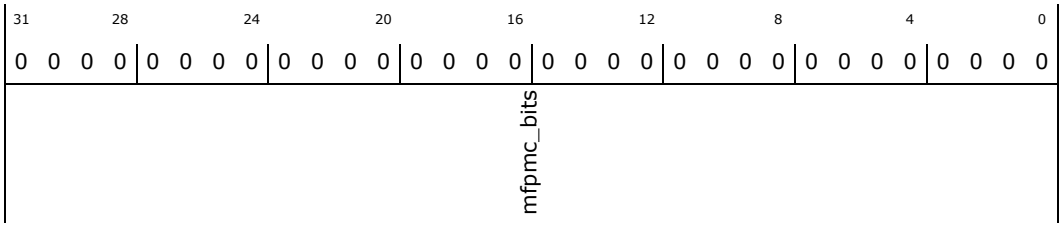
10.2.10 MFPMC - Message from PMC (MFPMC)—Offset 28h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 28h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Message from PMC (MFPMC) (mfpmc_bits):** The data in this register is typically updated in response to a host write to the MTPMC register.

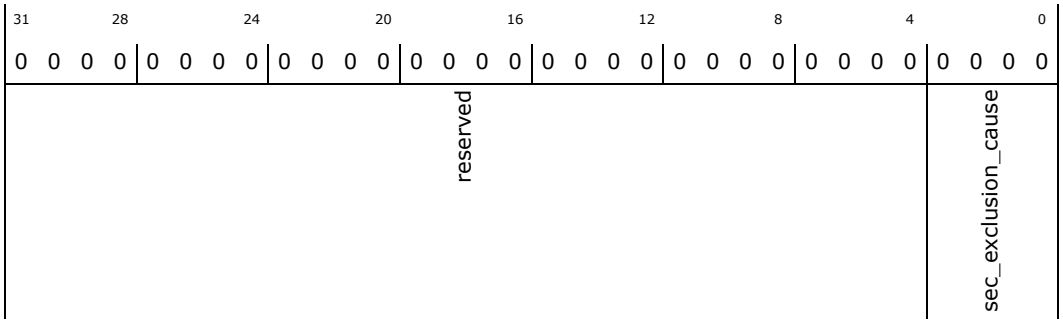
10.2.11 SEC_STS - SEC Status (SEC_STS)—Offset 2Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**reserved:** Reserved.
3:0	0x0 RW	**SEC_EXCLUSION_CAUSE (sec_exclusion_cause):** The cause associated with SeC setting requesting exclusion from power flows in SEC_EXCLUSION_REQ field. 0000b: SeC FW Fault Tolerant Initialization failed. 0001b: SeC FLASH Descriptor Override invoked. 0010b: SeC disabled using SW means (such as OEM setting). 0011b: Post-boot SeC applications not supported. 0100b: ROM BIST failure. 0101b: Fuse unit completed with unsupported request for group 1. 0110b: Invalid fuses bit at line 3 of group 1 fuses wasn't written with value 0. 0111b: DRAM Initializaiton by BIOS failed. Other values reserved.

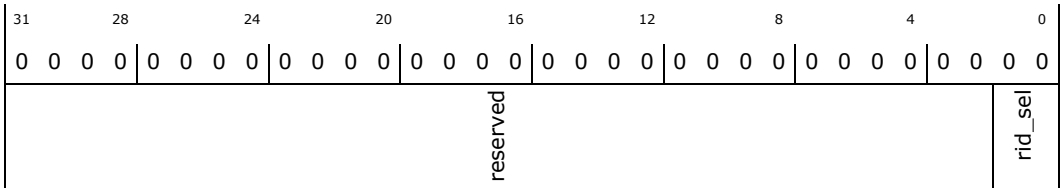
10.2.12 Configured Revision ID (CRID)—Offset 30h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**reserved:** Reserved.
1:0	0x0 RW	**RID Select(RID_SEL) (rid_sel):** Software writes this field to select the Revision ID reflected in PCI config space. The decoding is: 00 - Revision ID 01 - CRID 0 10 - CRID 1 11 - CRID 2 Once written, this field can only be cleared by a platform reset. reset_type=PMU_PLTRST

10.2.13 Function Disable (FUNC_DIS)—Offset 34h

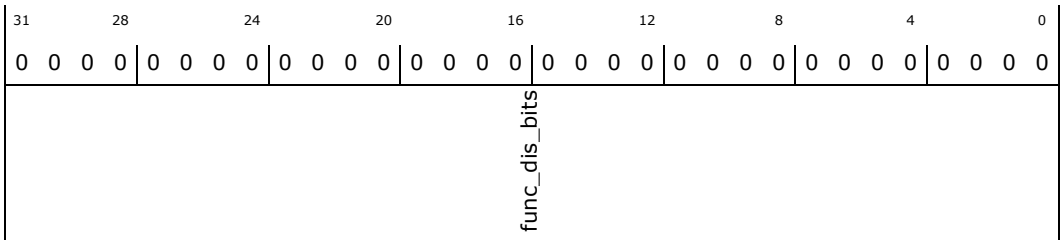
BIOS uses this register to disable specific function. Upon writing this register PMC will set the corresponding Function Disable bit in the PSF

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**FUNC_DIS_BITS (func_dis_bits):** When a bit is set, the corresponding function should be disabled. For more information regarding the specific PSF addresses and any contextual implications, please refer to the SoC PMC HAS 0 - LPSS 0 function 0 1 - LPSS 0 function 1 2 - LPSS 0 function 2 3 - LPSS 0 function 3 4 - LPSS 0 function 4 5 - LPSS 0 function 5 6 - LPSS 0 function 6 7 - LPSS 0 function 7 8 - SCC function 0 9 - SCC function 1 10 - SCC function 2 11 - MIPI 13 - LPE 14 - xDCI (OTG) 18 - xHCI (USB) 19 - SEC 20 - PCIE function 0 21 - PCIE function 1 22 - PCIE function 2 23 - PCIE function 3 24 - LPSS 1 function 0 25 - LPSS 1 function 1 26 - LPSS 1 function 2 27 - LPSS 1 function 3 28 - LPSS 1 function 4 29 - LPSS 1 function 5 30 - LPSS 1 function 6 31 - LPSS 1 function 7

10.2.14 Function Disable 2 (FUNC_DIS_2)—Offset 38h

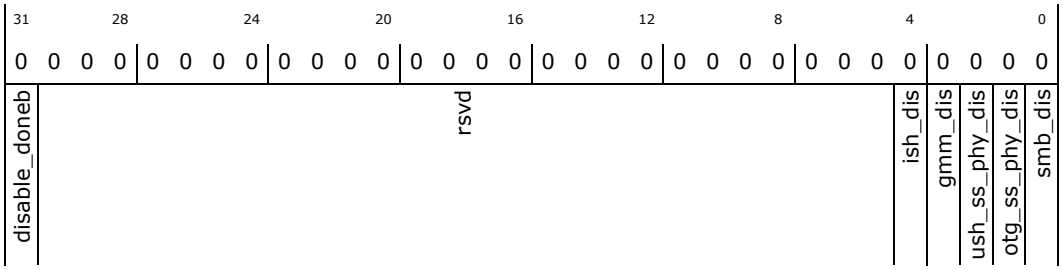
BIOS uses this register to disable specific function. Upon writing this register PMC will set the corresponding Function Disable bit in the PSF

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 38h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**DISABLE_DONEb (disable_doneb):** its is written to 1 by the BIOS and cleared by the PMC FW when the IPs have been functionally disabled
30:5	0x0 RW	**RSVD (rsvd):** reserved
4	0x0 RW	**ISH_DIS (ish_dis):** When this bit is set, ISH should be disabled.
3	0x0 RW	**GMM_DIS (gmm_dis):** When this bit is set, GMM should be disabled.
2	0x0 RW	**RESERVED (USH_SS_PHY_DIS) (ush_ss_phy_dis):** UNUSED
1	0x0 RW	**RESERVED (OTG_SS_PHY_DIS) (otg_ss_phy_dis):** UNUSED
0	0x0 RW	**SMB_DIS (smb_dis):** When this bit is set, SMB function should be disabled.

10.2.15 S0ix wake enable (S0IX_WAKE_EN)—Offset 3Ch

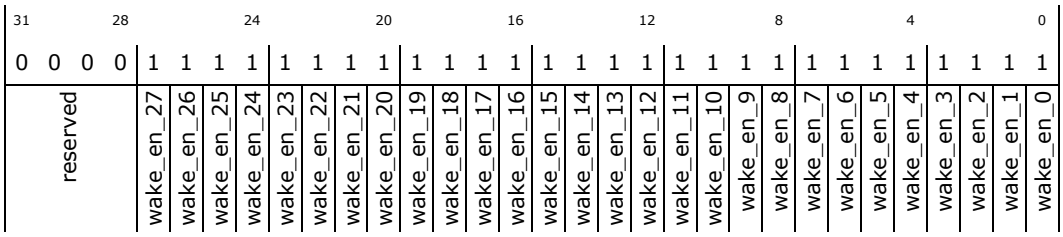
This register contains wake enable bit per S0ix wake event. Note: Common wake events with sleep sates have their wake enables in the ACPI space.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 3Ch

Default: 0FFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (reserved):** Reserved.
27	0x1 RW	**WAKE_EN_27 (RESERVED) (wake_en_27):** wake enable bit 27
26	0x1 RW	**WAKE_EN_26 (RESERVED) (wake_en_26):** wake enable bit 26
25	0x1 RW	**WAKE_EN_25 (RESERVED) (wake_en_25):** wake enable bit 25
24	0x1 RW	**WAKE_EN_24 (SC_IDLE_B) (wake_en_24):** wake enable bit 24
23	0x1 RW	**WAKE_EN_23 (GPIO SOUTHEAST WAKE EVENT) (wake_en_23):** wake enable bit 23
22	0x1 RW	**WAKE_EN_22 (ISH PMC WAKE EVENT) (wake_en_22):** wake enable bit 22
21	0x1 RW	**WAKE_EN_21 (ISH PMC IPC POPUP EVENT) (wake_en_21):** wake enable bit 21
20	0x1 RW	**WAKE_EN_20 (GPIO NORTH IRQEVENT) (wake_en_20):** wake enable bit 20
19	0x1 RW	**WAKE_EN_19 (GPIO SOUTHWEST IOxAPIC WAKE EVENT) (wake_en_19):** wake enable bit 19
18	0x1 RW	**WAKE_EN_18 (GPIO NORTH IOxAPIC WAKE EVENT) (wake_en_18):** wake enable bit 18
17	0x1 RW	**WAKE_EN_17 (WAKE_LAN_B WAKE EVENT) (wake_en_17):** wake enable bit 17
16	0x1 RW	**WAKE_EN_16 (ILB NMI WAKE EVENT) (wake_en_16):** wake enable bit 16
15	0x1 RW	**WAKE_EN_15 (SCI REQ WAKE EVENT) (wake_en_15):** wake enable bit 15

Bit Range	Default & Access	Field Name (ID): Description
14	0x1 RW	**WAKE_EN_14 (SMI PENDING WAKE EVENT) (wake_en_14):** wake enable bit 14
13	0x1 RW	**WAKE_EN_13 (UXD PCU WAKE EVENT) (wake_en_13):** wake enable bit 13
12	0x1 RW	**WAKE_EN_12 (AOT S0I3 WAKE EVENT) (wake_en_12):** wake enable bit 12
11	0x1 RW	**WAKE_EN_11 (AOT S0I2 WAKE EVENT) (wake_en_11):** wake enable bit 11
10	0x1 RW	**WAKE_EN_10 (AOT S0I1 WAKE EVENT) (wake_en_10):** wake enable bit 10
9	0x1 RW	**WAKE_EN_9 (IOxAPIC WAKE EVENT) (wake_en_9):** wake enable bit 9
8	0x1 RW	**WAKE_EN_8 (GPIO EAST WAKE EVENT) (wake_en_8):** wake enable bit 8
7	0x1 RW	**WAKE_EN_7 (GPIO NORTH GPE WAKE EVENT) (wake_en_7):** wake enable bit 7
6	0x1 RW	**WAKE_EN_6 (GPIO SOUTHWEST GPE WAKE EVENT) (wake_en_6):** wake enable bit 6
5	0x1 RW	**WAKE_EN_5 (GPIO SOUTWEST WAKE EVENT) (wake_en_5):** wake enable bit 5
4	0x1 RW	**WAKE_EN_4 (LPC CLKRUNB WAKE POPUP EVENT) (wake_en_4):** wake enable bit 4
3	0x1 RW	**WAKE_EN_3 (SEC TIMER WAKE POPUP EVENT) (wake_en_3):** wake enable bit 3
2	0x1 RW	**WAKE_EN_2 (LPE PMC IPC POPUP EVENT) (wake_en_2):** wake enable bit 2
1	0x1 RW	**WAKE_EN_1 (LPE PMC WAKE POPUP EVENT) (wake_en_1):** wake enable bit 1
0	0x1 RW	**WAKE_EN_0 (NFC WAKE POPUP EVENT) (wake_en_0):** wake enable bit 0

10.2.16 S0ix wake Status (S0IX_WAKE_STS)—Offset 40h

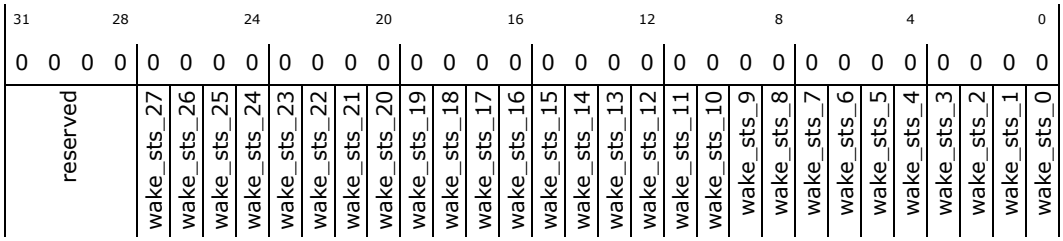
This register contains wake status bits per S0ix wake event. There is a 1:1 correspondence between S0ix_WAKE_STS and S0ix_WAKE_EN bits. Please refer to teh S0iX_WAKE_EN Register for the associated bit definitions. Note: Common wake events with sleep sates have their wake enables in the ACPI space.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 40h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (reserved):** Reserved.
27	0x0 RW/1C	**WAKE_STS_27 (wake_sts_27):** wake status bit 27
26	0x0 RW/1C	**WAKE_STS_26 (wake_sts_26):** wake status bit 26
25	0x0 RW/1C	**WAKE_STS_25 (wake_sts_25):** wake status bit 25
24	0x0 RW/1C	**WAKE_STS_24 (wake_sts_24):** wake status bit 24
23	0x0 RW/1C	**WAKE_STS_23 (wake_sts_23):** wake status bit 23
22	0x0 RW/1C	**WAKE_STS_22 (wake_sts_22):** wake status bit 22
21	0x0 RW/1C	**WAKE_STS_21 (wake_sts_21):** wake status bit 21
20	0x0 RW/1C	**WAKE_STS_20 (wake_sts_20):** wake status bit 20
19	0x0 RW/1C	**WAKE_STS_19 (wake_sts_19):** wake status bit 19
18	0x0 RW/1C	**WAKE_STS_18 (wake_sts_18):** wake status bit 18
17	0x0 RW/1C	**WAKE_STS_17 (wake_sts_17):** wake status bit 17
16	0x0 RW/1C	**WAKE_STS_16 (wake_sts_16):** wake status bit 16
15	0x0 RW/1C	**WAKE_STS_15 (wake_sts_15):** wake status bit 15
14	0x0 RW/1C	**WAKE_STS_14 (wake_sts_14):** wake status bit 14
13	0x0 RW/1C	**WAKE_STS_13 (wake_sts_13):** wake status bit 13
12	0x0 RW/1C	**WAKE_STS_12 (wake_sts_12):** wake status bit 12
11	0x0 RW/1C	**WAKE_STS_11 (wake_sts_11):** wake status bit 11
10	0x0 RW/1C	**WAKE_STS_10 (wake_sts_10):** wake status bit 10

Bit Range	Default & Access	Field Name (ID): Description
9	0x0 RW/1C	**WAKE_STS_9 (wake_sts_9):** wake status bit 9
8	0x0 RW/1C	**WAKE_STS_8 (wake_sts_8):** wake status bit 8
7	0x0 RW/1C	**WAKE_STS_7 (wake_sts_7):** wake status bit 7
6	0x0 RW/1C	**WAKE_STS_6 (wake_sts_6):** wake status bit 6
5	0x0 RW/1C	**WAKE_STS_5 (wake_sts_5):** wake status bit 5
4	0x0 RW/1C	**WAKE_STS_4 (wake_sts_4):** wake status bit 4
3	0x0 RW/1C	**WAKE_STS_3 (wake_sts_3):** wake status bit 3
2	0x0 RW/1C	**WAKE_STS_2 (wake_sts_2):** wake status bit 2
1	0x0 RW/1C	**WAKE_STS_1 (wake_sts_1):** wake status bit 1
0	0x0 RW/1C	**WAKE_STS_0 (wake_sts_0):** wake status bit 0

10.2.17 S0ix control (S0IX_CTL)—Offset 44h

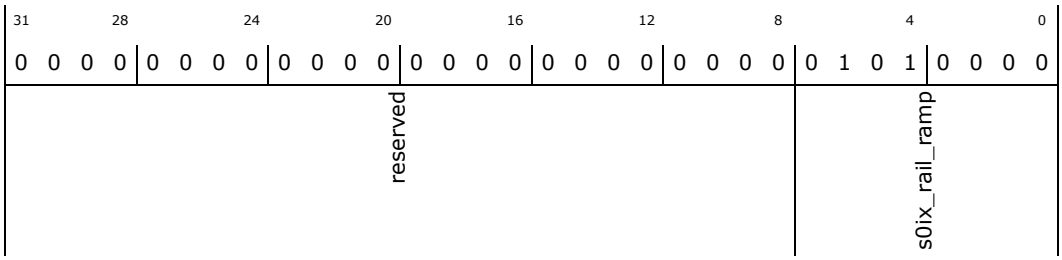
This register contains S0ix miscellaneous controls

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 44h

Default: 00000050h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (reserved):** Reserved.
7:0	0x50 RW	**S0IX_RAIL_RAMP (s0ix_rail_ramp):** specifies S0IX rail ramp time

10.2.18 ETR - Extended Test Mode Register (ETR)—Offset 48h

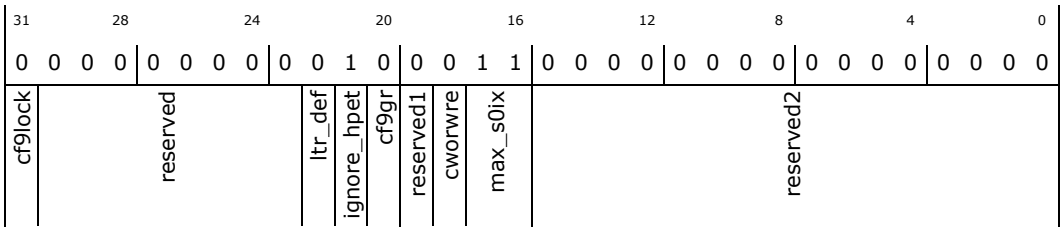
This register resides in the resume well. All bits except bit[23:16] are reset by internal Resume Well Reset. Bit[23:16] are reset by RSMRST_B only.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 48h

Default: 00230000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**CF9h Lockdown (CF9LOCK) (cf9lock):** When set, this will lock the CF9h-Global-Reset bit. When set, this register locks itself. This register is reset by a CF9h reset.
30:23	0x0 RO	**reserved:** Reserved.
22	0x0 RW	**LTR default (LTR_DEF) (ltr_def):** When this bit is cleared, PMC will assume low LTR by default. When set, PMC will assume high LTR by default
21	0x1 RW	**Ignore HPET When going to S0i2 (IGNORE_HPET) (ignore_hpet):** When this bit is set, PMC will not check for HPET disabled before going to S0i2
20	0x0 RW	**CF9h Global Reset (CF9GR) (cf9gr):** When this bit is set, a CF9h write of 6h or Eh will cause a Global Reset of the Host partition. If this bit is cleared, a CF9h write of 6h or Eh will only reset the Host partition. It is recommended that BIOS should set this bit early on in the boot sequence, and then clear it and set the CF9LOCK bit prior to loading the OS. When this bit is set, the hardware assumes that bit 18 (CF9h Without Resume Well Reset Enable) is cleared. This register is locked by the CF9 Lockdown (CF9LOCK) bit. This register is not reset by a CF9h reset. reset_type=RSMRST_B
19	0x0 RO	**reserved (reserved1):** Reserved.
18	0x0 RW	**CF9h Without Resume Well Reset Enable (CWORWRE) (cworwre):** When this bit is set, a CF9h write of 6h or Eh will not cause internal Resume Well Reset (WrsmrstB) to be asserted and thus resume well logic will maintain its state. When this bit is cleared, CF9h write of 6h or Eh will also reset resume well logic. This bit is to be used when a second reset through CF9 write is desired upon power up or after resume from low power states. This bit has to be set prior to the write to CF9 register and has to be cleared upon completing the reset. Failing to do so prevents resume well registers from being reset in the future CF9 writes. reset_type=RSMRST_B
17:16	0x3 RW	**MAX_S0IX (MAX_S0IX (max_s0ix):** Indicated the maximum S0i state SOC can go

Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RO	**reserved (reserved2):** Reserved.

10.2.19 TNTE_TMR - Always running timer - can be used to create events timer status (TNTE_TMR)—Offset 4Ch

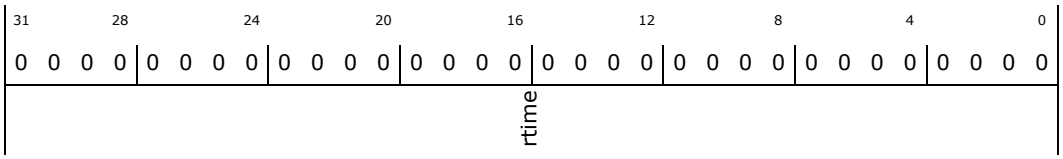
This timer acumulates time when enabled

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**TNTE Timer value (rtime):** always running timer based on rtc clock period @ 32 uS

10.2.20 VLT - Voltage Detect Register (VLT)—Offset 50h

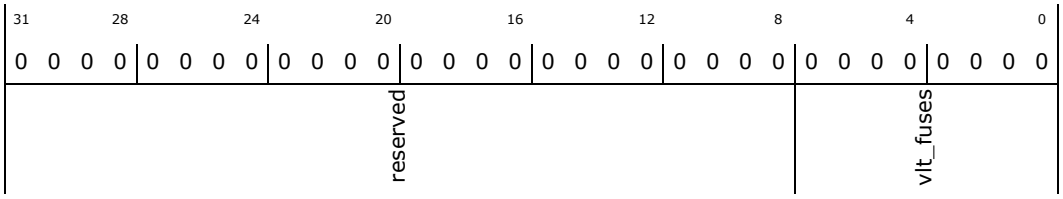
This register reflects the Voltage detect fuses.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 50h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**reserved:** Reserved.
7:0	0x0 RO	**VLT Fuses (VLT_FUSES) (vlt_fuses):** These bits reflects the Voltage detect fuses

10.2.21 S0IA_TMR_UPPER - S0I Ready Residency Timer (S0IA_TMR_UPPER)—Offset 54h

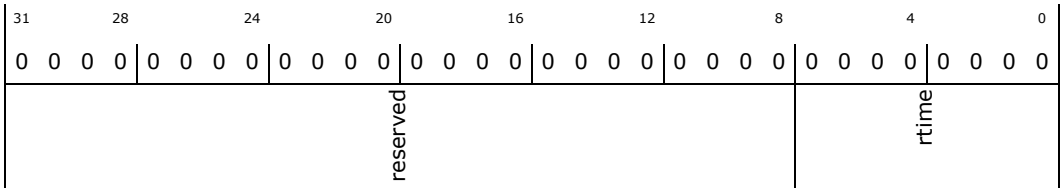
This timer acumulates time spent in S0IA Ready state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 54h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**reserved:** reserved bits
7:0	0x0 RW	**RTIME (Residency Time) (rtime):** time spent in S0IA Ready state, in units of 8 uS

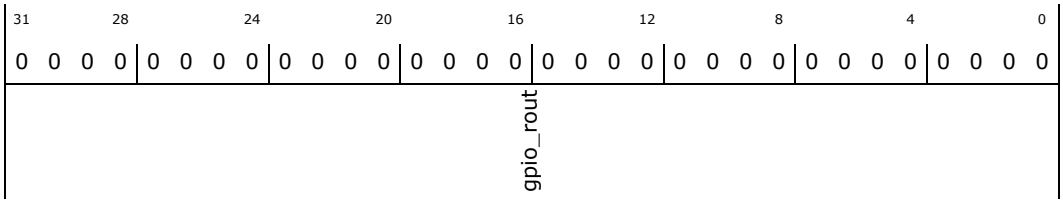
10.2.22 GPIO_ROUT - GPIO_ROUT register (GPIO_ROUT)—Offset 58h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 58h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GPIO Rout (GPIO_ROUT) (gpio_rout):** Bits [15:0] determines GPIO SUS (GPIO NORTH) events rout. Bits [31:16] determines GPIO CORE (GPIO SOUTHWEST) events rout. Bits [1:0] determines GPIO SUS event 0. Bits [3:2] determines GPIO SUS event 1 and so on. Bits [17:16] determines GPIO CORE event 0. Bits [19:18] determines GPIO CORE event 1 and so on. If the corresponding GPIO is implemented and is set to an input, a '1' in the GP_LVL bit can be routed to cause an interrupt. If the GPIO is not set to an input, this field has no effect. * 00 No effect (or GPIO unimplemented), * 01 SMI# (if corresponding ALT_GPIO_SMI bit also set), * 10 SCI (if corresponding GPE0a_EN bit also set), * 11 Reserved If the system is in an S0-S5 state and if the GPE0a_EN bit is also set, then the GPIO can cause a Wake event, even if the GPIO is NOT routed to cause an interrupt. Exception: If the system is in S5 state due to a powerbutton override, then the GPIO's will not cause wake events. Note: Core well GPIO's are not capable of waking the system from sleep states where the core well is not powered.

10.2.23 S0IA_TMR - S0I Ready Residency Timer (S0IA_TMR)—Offset 5Ch

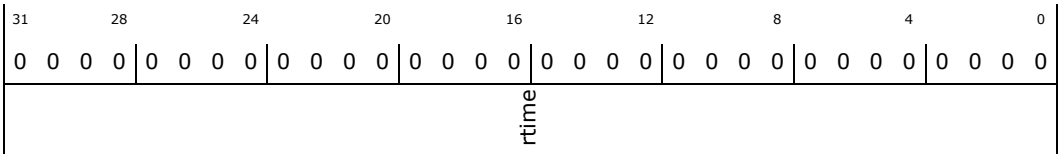
This timer acumulates time spent in S0I Ready state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 5Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RTIME (Residency Time) (rtime):** time spent in S0IA Ready state, in units of 32 uS

10.2.24 PLT_CLK_CTL_0 - Platform Clock Control 0 (PLT_CLK_CTL_0)—Offset 60h

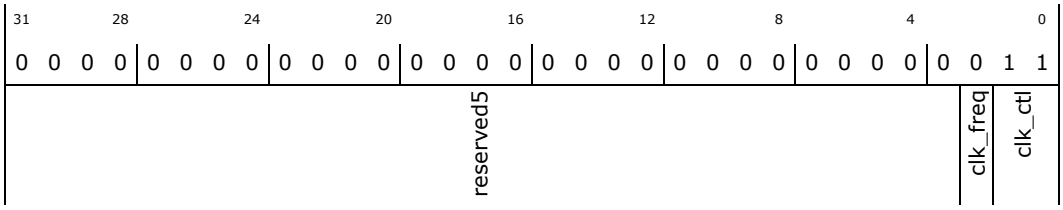
This register controls Platform clocks.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 60h

Default: 00000003h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**reserved (reserved5):** Reserved.
2	0x0 RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	0x3 RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 10 - force off, 11 - Reserved (should not be used)

10.2.25 PLT_CLK_CTL_1 - Platform Clock Control 1 (PLT_CLK_CTL_1)—Offset 64h

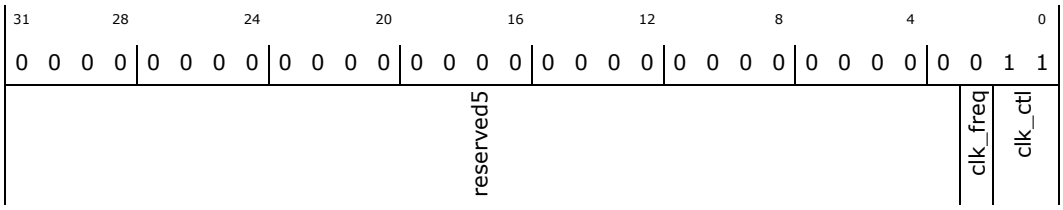
This register controls Platform clocks.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 64h

Default: 00000003h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**reserved (reserved5):** Reserved.
2	0x0 RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	0x3 RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 10 - force off, 11 - Reserved (should not be used)

10.2.26 PLT_CLK_CTL_2 - Platform Clock Control 2 (PLT_CLK_CTL_2)—Offset 68h

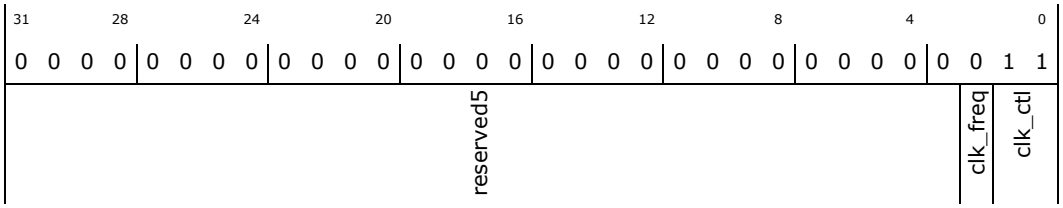
This register controls Platform clocks.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 68h

Default: 00000003h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**reserved (reserved5):** Reserved.
2	0x0 RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	0x3 RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 10 - force off, 11 - Reserved (should not be used)

10.2.27 PLT_CLK_CTL_3 - Platform Clock Control 3 (PLT_CLK_CTL_3)—Offset 6Ch

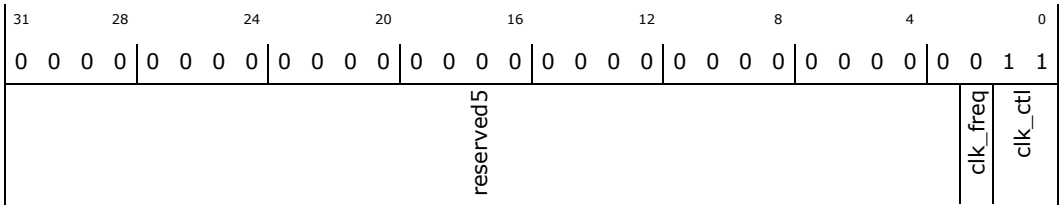
This register controls Platform clocks.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 6Ch

Default: 00000003h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**reserved (reserved5):** Reserved.
2	0x0 RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	0x3 RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 10 - force off, 11 - Reserved (should not be used)

10.2.28 PLT_CLK_CTL_4 - Platform Clock Control 4 (PLT_CLK_CTL_4)—Offset 70h

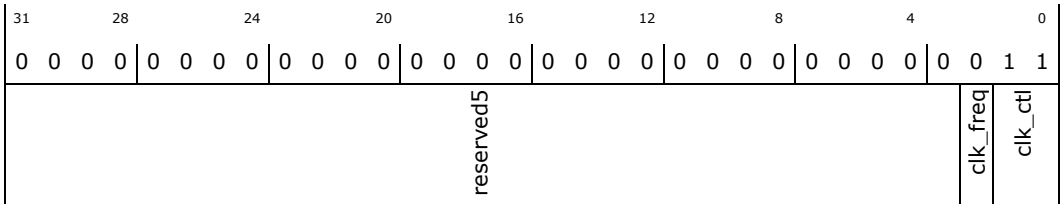
This register controls Platform clocks.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 70h

Default: 00000003h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**reserved (reserved5):** Reserved.
2	0x0 RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	0x3 RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 10 - force off, 11 - Reserved (should not be used)

10.2.29 PLT_CLK_CTL_5 - Platform Clock Control 5 (PLT_CLK_CTL_5)—Offset 74h

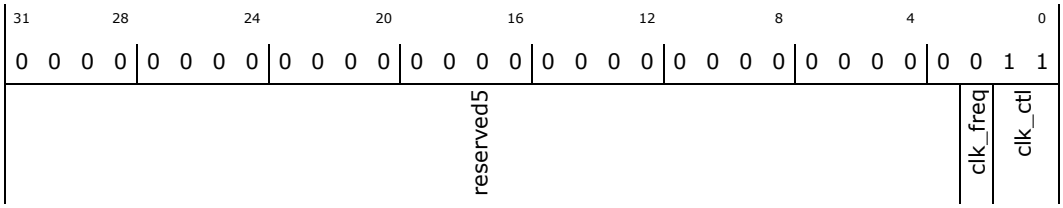
This register controls Platform clocks.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 74h

Default: 00000003h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**reserved (reserved5):** Reserved.
2	0x0 RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)

Bit Range	Default & Access	Field Name (ID): Description
1:0	0x3 RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 10 - force off, 11 - Reserved (should not be used)

10.2.30 S0IR_TMR_UPPER - S0I Ready Residency Timer (S0IR_TMR_UPPER)—Offset 78h

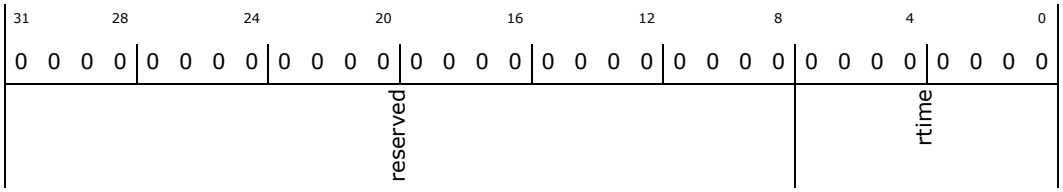
This timer acumulates time spent in S0I Ready state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 78h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**reserved:** reserved bits
7:0	0x0 RW	**RTIME (Residency Time) (rtime):** time spent in S0I Ready state, in units of 8 uS

10.2.31 S0I1_TMR_UPPER - S0I1 Ready Residency Timer (S0I1_TMR_UPPER)—Offset 7Ch

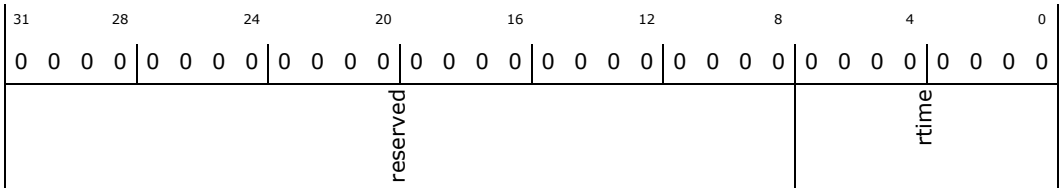
This timer acumulates time spent in S0I1 Ready state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 7Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**reserved:** reserved bits
7:0	0x0 RW	**RTIME (Residency Time) (rtime):** time spent in S0I1 Ready state, in units of 8 uS

10.2.32 S0IR_TMR - S0I Ready Residency Timer (S0IR_TMR)—Offset 80h

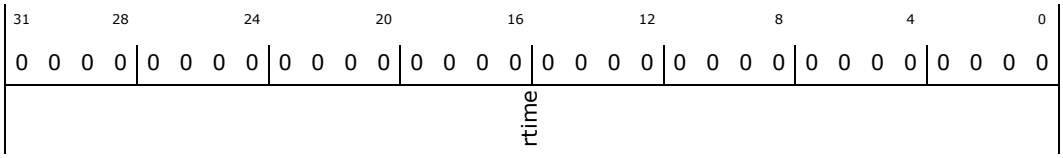
This timer acumulates time spent in S0I Ready state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 80h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RTIME (Residency Time) (rtime):** time spent in S0I Ready state, in units of 32 uS

10.2.33 S0I1_TMR - S0I1 Residency Timer (S0I1_TMR)—Offset 84h

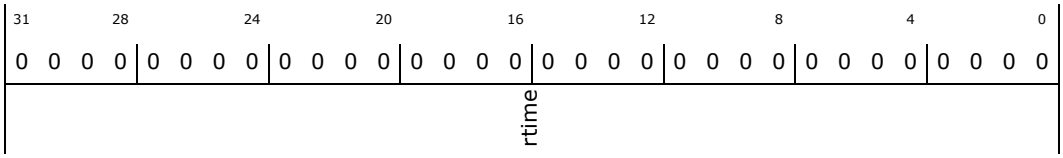
This timer acumulates time spent in S0I1 state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 84h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RTIME (Residency Time) (rtime):** time spent in S0I1 state, in units of 32 uS

10.2.34 S0I2_TMR - S0I2 Residency Timer (S0I2_TMR)—Offset 88h

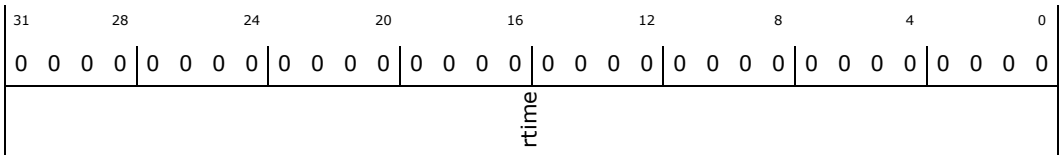
This timer acumulates time spent in S0I2 state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 88h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RTIME (Residency Time) (rtime):** time spent in S0I2 state, in units of 32 uS

10.2.35 S0I3_TMR - S0I3 Residency Timer (S0I3_TMR)—Offset 8Ch

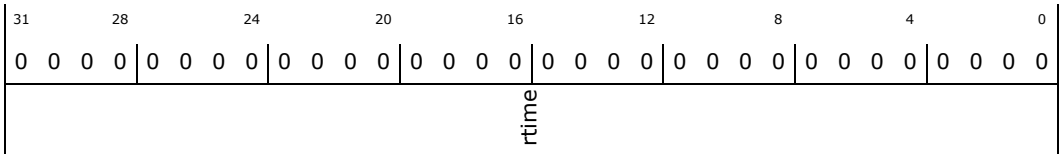
This timer acumulates time spent in S0I3 state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 8Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RTIME (Residency Time) (rtime):** time spent in S0I3 state, in units of 32 uS

10.2.36 S0_TMR - S0 Residency Timer (S0_TMR)—Offset 90h

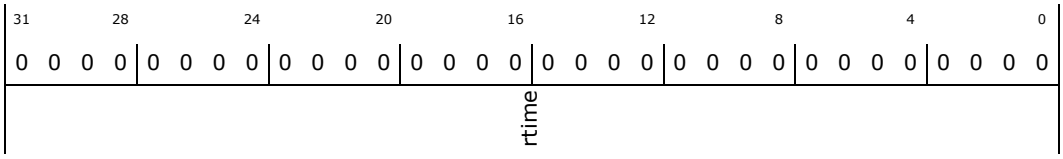
This timer acumulates time spent in S0 state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 90h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**RTIME (Residency Time) (rtime):** time spent in S0 state, in units of 32 uS

10.2.37 S0I2_TMR_UPPER - S0I2 Residency Timer (S0I2_TMR_UPPER)—Offset 94h

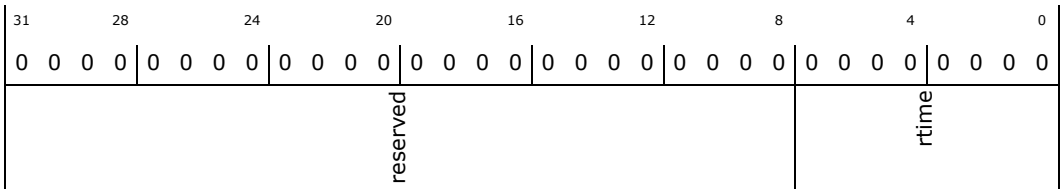
This timer acumulates time spent in S0I2 state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 94h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**reserved:** reserved bits
7:0	0x0 RW	**RTIME (Residency Time) (rtime):** time spent in S0I2 state, in units of 8 uS

10.2.38 PSS - Power island Power Status (PSS)—Offset 98h

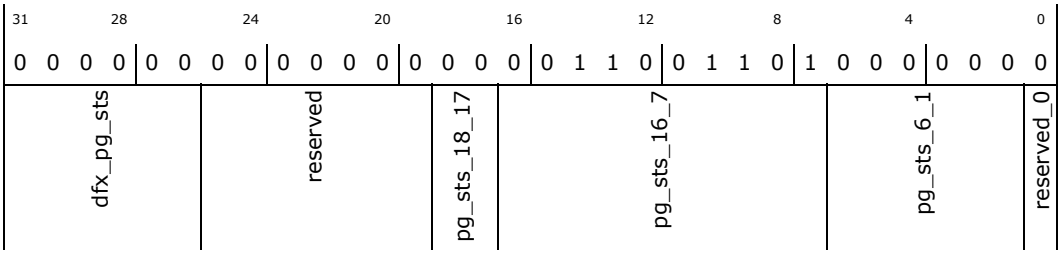
This register reflects the power status for each physical power island controlled by PMC - TAP OVERRIDE Register value does not influence the value of this register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 98h

Default: 00006680h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**DFX_PG_STS (DFX POWER GATE status) (dfx_pg_sts):** reflects the power gate status of all power islands bit value of 0 - power island is powered on. 1 - power island is powered off bits mapping: 0 - DFX Master 1:5 - DFX Cluster n
25:19	0x0 RO	**reserved:** Reserved.
18:17	0x0 RO	**PG_STS (POWER GATE status) (pg_sts_18_17):** reflects the power gate status of all power islands 0 - power island is powered on. 1 - power island is powered off bits mapping: 18 - ISH
16:7	0xcd RO	**PG_STS_16_7 (POWER GATE status of USB devices) (pg_sts_16_7):** SoC Power Island Power Gate Status 0 - power island is powered on. 1 - power island is powered off bits mapping: 8 - Reserved 9 - Reserved 10 - reserved 11 - UXD Power Gate Status (xDCI) 12 - UXD FD SX Power Gate Status (xDCI) 13 - Reserved 14 - Reserved 15 - UX Engine Power Gate Status (xHCI) 16 - USB SUS
6:1	0x0 RO	**PG_STS_6_1 (POWER GATE status) (pg_sts_6_1):** reflects the power gate status of all power islands 0 - power island is powered on. 1 - power island is powered off bits mapping: 3 - SEC 4 - PCIE 5 - LPSS 6 - LPE
0	0x0 RO	**reserved_0:** Reserved.

10.2.39 S0I3_TMR_UPPER - S0I3 Residency Timer (S0I3_TMR_UPPER)—Offset 9Ch

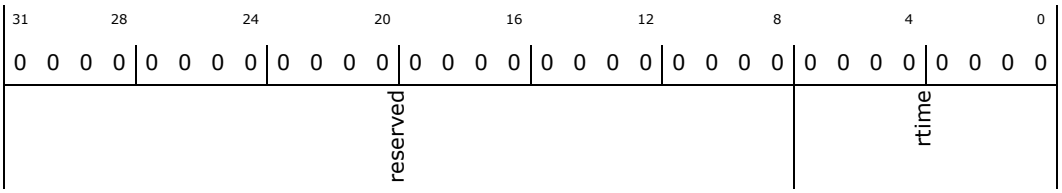
This timer acumulates time spent in S0I3 state

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + 9Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**reserved:** reserved bits
7:0	0x0 RW	**RTIME (Residency Time) (rtime):** time spent in S0I3 state, in units of 8 uS

10.2.40 D3_STS_0 - D3 Status register 0 (D3_STS_0)—Offset A0h

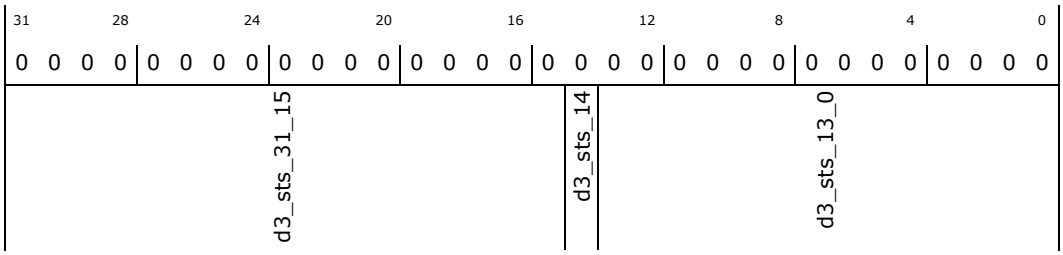
This register reflects D3 status of functions

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RO	**D3_STS 31-15 (D3 status) (d3_sts_31_15):** reflects D3 status of the following functions. 0 - Function is in D0. 1 - Function is in D3 bits mapping: 18 - USB (~ux_pmc_engine_pwrup_req) 19 - SEC 20 - PCIE function 0 21 - PCIE function 1 22 - PCIE function 2 23 - PCIE function 3 24 - LPSS 1 function 0 25 - LPSS 1 function 1 26 - LPSS 1 function 2 27 - LPSS 1 function 3 28 - LPSS 1 function 4 29 - LPSS 1 function 5 30 - LPSS 1 function 6 31 - LPSS 1 function 7
14	0x0 RO	**D3_STS_14 (USB SIP Bridge Power Interface (d3_sts_14):** D3 indication status for USB SIP Bridge Power Interface 0 - Function is in D0. 1 - Function is in D3 bits mapping: 14 - USB SIP Bridge
13:0	0x0 RO	**D3_STS 13-0 (D3 status) (d3_sts_13_0):** reflects D3 status of the following functions. 0 - Function is in D0. 1 - Function is in D3 bits mapping: 0 - LPSS 0 function 0 1 - LPSS 0 function 1 2 - LPSS 0 function 2 3 - LPSS 0 function 3 4 - LPSS 0 function 4 5 - LPSS 0 function 5 6 - LPSS 0 function 6 7 - LPSS 0 function 7 8 - SCC function 0 9 - SCC function 1 10 - SCC function 2 11 - MIPI 13 - LPE

10.2.41 D3_STS_1 - D3 Status register 1 (D3_STS_1)—Offset A4h

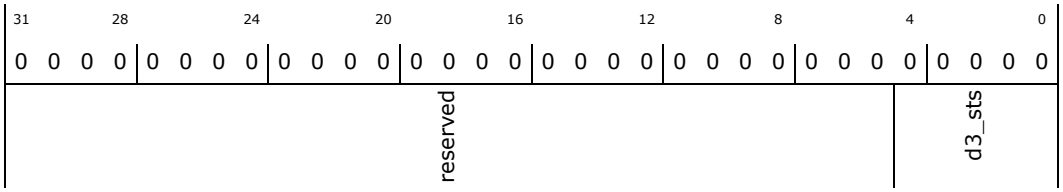
This register reflects D3 status of functions

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RO	**reserved:** Reserved.
4:0	0x0 RO	**D3_STS (D3 status) (d3_sts):** reflects D3 status of the following functions. 0 - Function is in D0. 1 - Function is in D3 bits mapping: 2 - ISH 3 - RESERVED

10.2.42 D3_STDBY_STS_0 - D3 Standby Status register 0 (D3_STDBY_STS_0)—Offset A8h

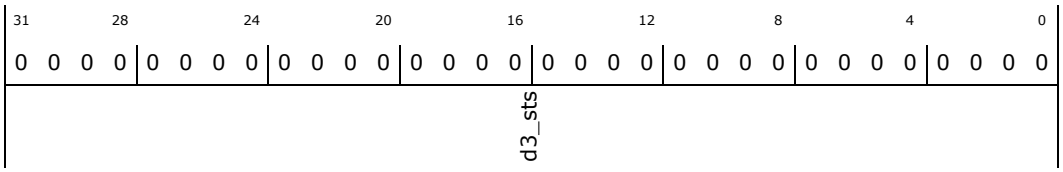
This register reflects D3 status of functions at the moment standby ready message received

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**D3_STS (D3 status) (d3_sts):** reflects D3 status of the following functions. 0 - Function is in D0. 1 - Function is in D3 bits mapping: 0 - LPSS 0 function 0 1 - LPSS 0 function 1 2 - LPSS 0 function 2 3 - LPSS 0 function 3 4 - LPSS 0 function 4 5 - LPSS 0 function 5 6 - LPSS 0 function 6 7 - LPSS 0 function 7 8 - SCC function 0 9 - SCC function 1 10 - SCC function 2 11 - MIPI 13 - LPE 14 - OTG/xDCI 18 - USB/xHCI 19 - SEC 20 - PCIE function 0 21 - PCIE function 1 22 - PCIE function 2 23 - PCIE function 3 24 - LPSS 1 function 0 25 - LPSS 1 function 1 26 - LPSS 1 function 2 27 - LPSS 1 function 3 28 - LPSS 1 function 4 29 - LPSS 1 function 5 30 - LPSS 1 function 6 31 - LPSS 1 function 7

10.2.43 D3_STDBY_STS_1 - D3 Standby Status register 1 (D3_STDBY_STS_1)—Offset ACh

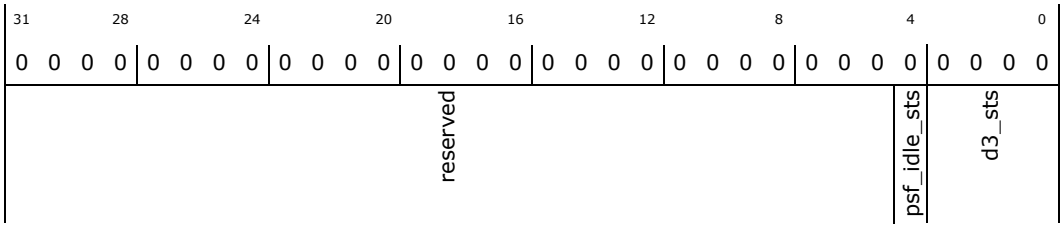
This register reflects D3 status of functions at the moment Standby Ready Message was received

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0x0 RO	**reserved:** Reserved.
4	0x0 RO	**PSF IDLE (status) (psf_idle_sts):** Reflect if S0IX flow was stoped because PSF isnt IDLE
3:0	0x0 RO	**D3_STS (D3 status) (d3_sts):** reflects D3 status of the following functions. 0 - Function is in D0. 1 - Function is in D3 bits mapping: 1 - ISH 3 - DFX

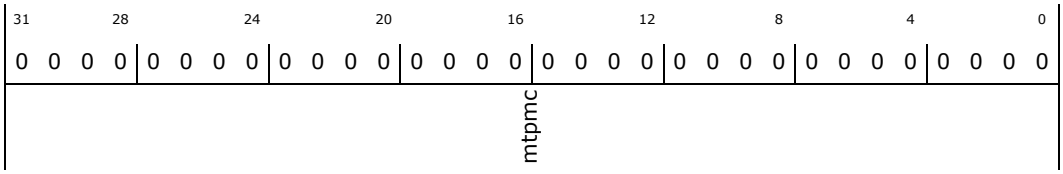
10.2.44 MTPMC_1 - Message to PMC 1 (MTPMC_1)—Offset B0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Message to PMC (MTPMC) (mtpmc):** A write to this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_1_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS

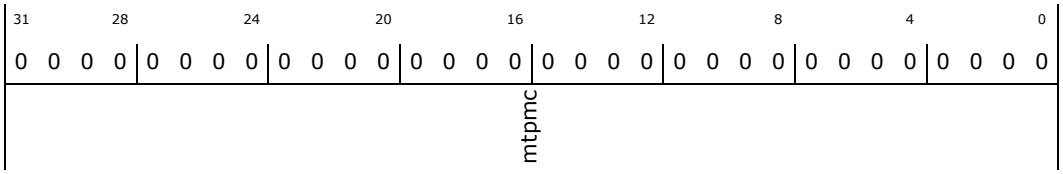
10.2.45 MTPMC_2 - Message to PMC 2 (MTPMC_2)—Offset B4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + B4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Message to PMC (MTPMC) (mtpmc):** A write to this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_2_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS

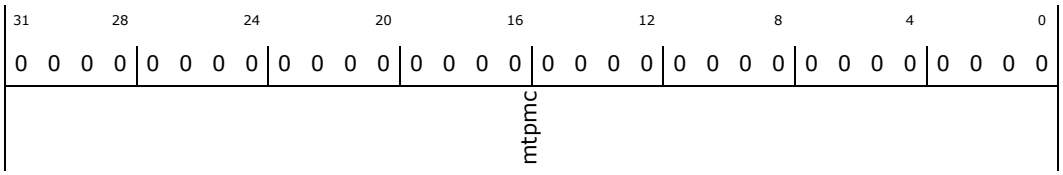
10.2.46 MTPMC_3 - Message to PMC 3 (MTPMC_3)—Offset B8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Message to PMC (MTPMC) (mtpmc):** A write to this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_3_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS

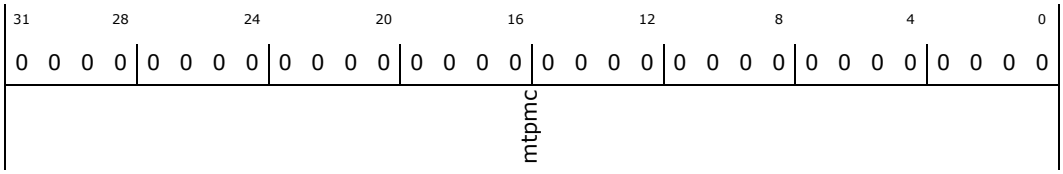
10.2.47 MTPMC_4 - Message to PMC 4 (MTPMC_4)—Offset BCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + BCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Message to PMC (MTPMC) (mtpmc):** A write to this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_4_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS

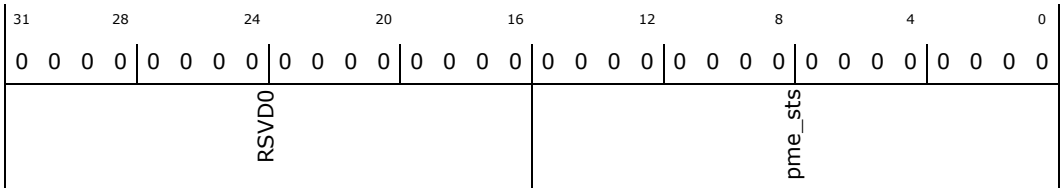
10.2.48 PME Status 0 - Status bit for PME messages (PME_STS)—Offset C0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD0:** Reserved
15:0	0x0 RO	**PME Status (pme_sts):** when set PME was recived from the following agents 3 = SCCSDIO 4 = SCCSDCARD 5 = LPSDIO1; 6 = SECEP 7 = LPE 8 = LPSDIO2 9 = OTG 10 = SCCEMMC 11 = SCCMIPIHSI 12 = UNUSED 13 = usb_pmc_wake_b 14 = ush_pmc_ux_wa_xepnfwh 15 = WAKE_LANB

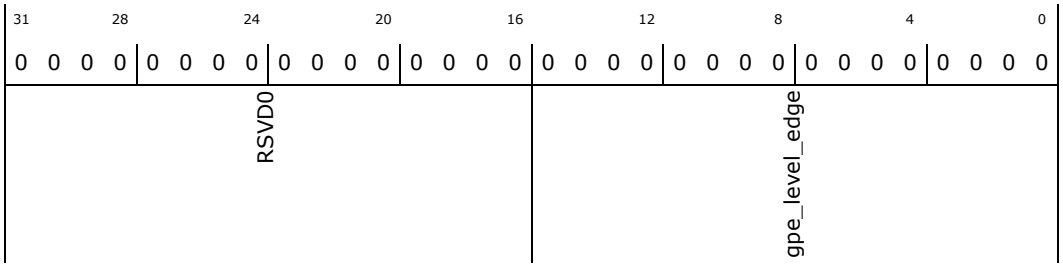
10.2.49 GPE Level Edge mode (GPE_LEVEL_EDGE)—Offset C4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + C4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD0:** Reserved
15:0	0x0 RW	**Edge Level mode (gpe_level_edge):** When set GPE is in level mode when clear GPE is in edge mode gpe_level_edge[15:8] used for GPIO SOUTHWEST gpe_level_edge[7:0] used for GPIO NORTH

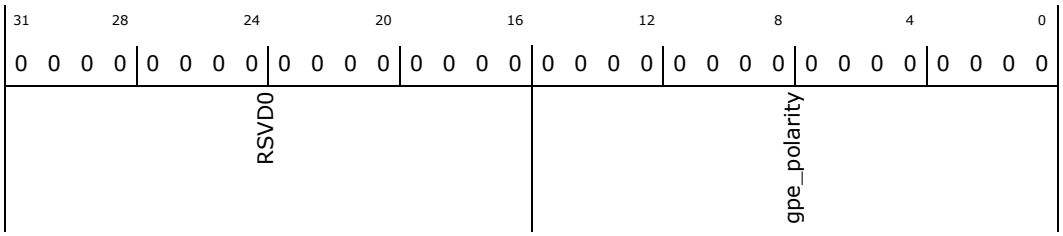
10.2.50 GPE polarity mode (GPE_POLARITY)—Offset C8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + C8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD0:** Reserved
15:0	0x0 RW	**Polarity (gpe_polarity):** When set GPE is active high when clear GPE is active low gpe_polarity[15:8] used for GPIO SOUTHWEST gpe_polarity[7:0] used for GPIO NORTH

10.2.51 Lock Register (LOCK)—Offset CCh

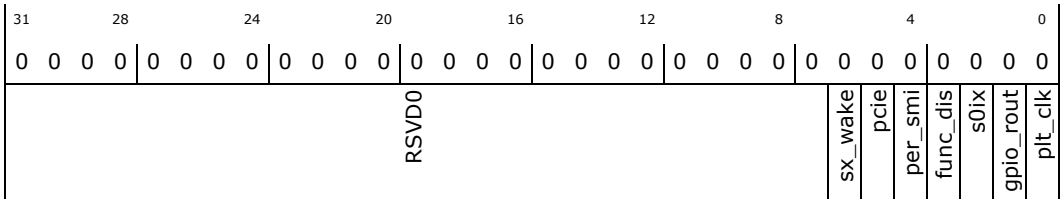
Register Field Lock bit ---------- GEN_PMCON1 PME_B0_S5_DIS LOCK.Sx_WAKE GEN_PMCON1 WOL_EN_OVRD LOCK.Sx_WAKE GEN_PMCON1 AG3E LOCK.Sx_WAKE GEN_PMCON2 BIOS_PCI_EXP_EN LOCK.PCIE GEN_PMCON2 PER_SMI_SEL LOCK.PER_SMI FUNC_DIS all LOCK.FUNC_DIS FUNC_DIS_2 all LOCK.FUNC_DIS S0IX_WAKE_EN all LOCK.SOIX S0IX_CTL S0IX_RAIL_RAMP LOCK.SOIX ETR IGNORE_HPET LOCK.SOIX ETR MAX_S0IX

LOCK.SOIX GPIO_ROUT all LOCK.GPIO_ROUT PLT_CLK_CTL_0 all LOCK.PLT_CLK PLT_CLK_CTL_1 all LOCK.PLT_CLK PLT_CLK_CTL_2 all LOCK.PLT_CLK PLT_CLK_CTL_3 all LOCK.PLT_CLK PLT_CLK_CTL_4 all LOCK.PLT_CLK PLT_CLK_CTL_5 all LOCK.PLT_CLK

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** [PMC_BASE_ADDRESS] + CCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**RSVD0:** Reserved
6	0x0 RW	**SX_WAKE lock (sx_wake):** Reserved.
5	0x0 RW	**PCIE lock (pcie):** Reserved.
4	0x0 RW	**PER_SMI lock (per_smi):** Reserved.
3	0x0 RW	**FUNC_DIS (func_dis):** Reserved.
2	0x0 RW	**S0IX lock (s0ix):** Reserved.
1	0x0 RW	**GPIO_ROUT lock (gpio_rout):** Reserved.
0	0x0 RW	**PLT_CLK lock (plt_clk):** Reserved.

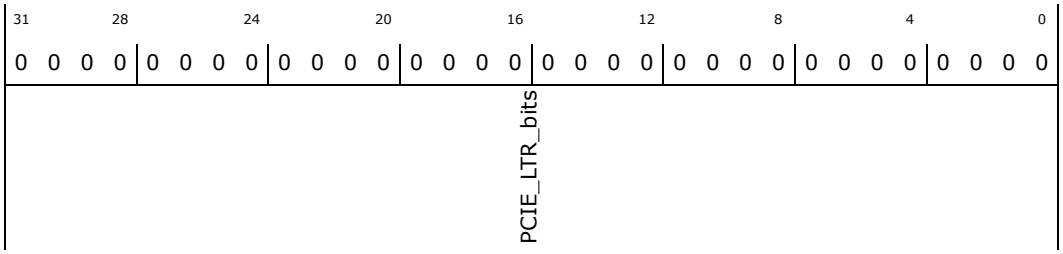
10.2.52 PCIE LTR (PCIE_LTR)—Offset D0h

BIOS uses this register to enable PCIE_LTR for IPs

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** [PMC_BASE_ADDRESS] + D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**PCIE LTR (PCIE_LTR_bits):** When a bit is set, the corresponding function should be disabled.

10.2.53 D3 Cold (D3_COLD)—Offset D4h

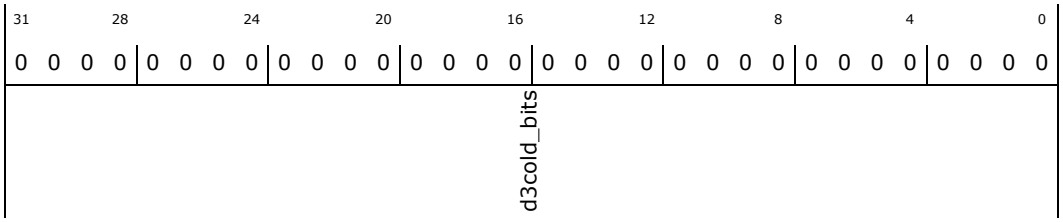
BIOS uses this register to enable D3cold for IPs

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + D4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**D3 COLD (d3cold_bits):** Special register to handle D3 Cold entry/exit request. 31:2 - RESERVED

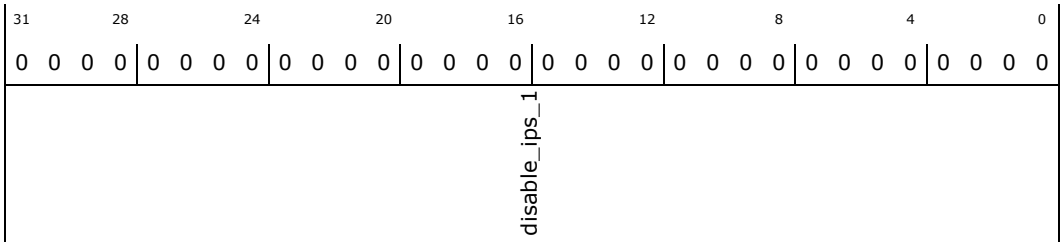
10.2.54 DISABLE IPs (DISABLE_IPs_1)—Offset D8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + D8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**DISABLE IPs (disable_ips_1):** IPs disabled by fuses/ straps

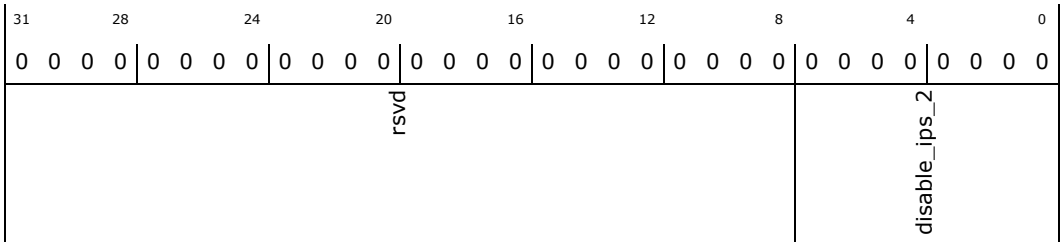
10.2.55 DISABLE IPs (DISABLE_IPs_2)—Offset DCh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + DCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**reserved (rsvd):** rsvd
7:0	0x0 RO	**DISABLE IPs (disable_ips_2):** IPs disabled by fuses/ straps

10.2.56 D3 Defer for PMC FW (D3_DEFER_0)—Offset E0h

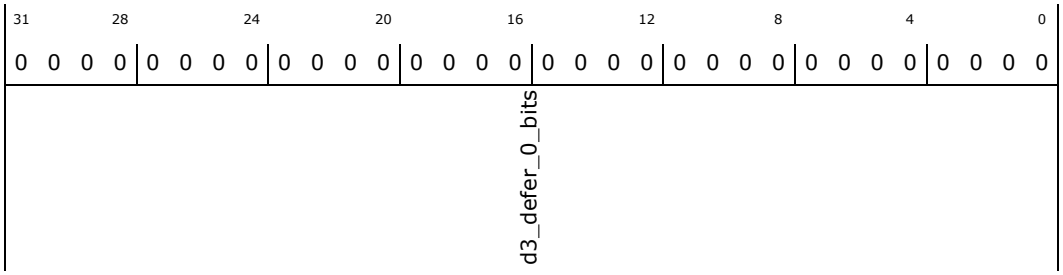
D3 defer for IPs

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + E0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**D3 DEFER - 0 (d3_defer_0_bits):** When a bit is set, the corresponding function should be disabled - refer to D3_STS_0 for mappings

10.2.57 D3 Defer for PMC FW (D3_DEFER_1)—Offset E4h

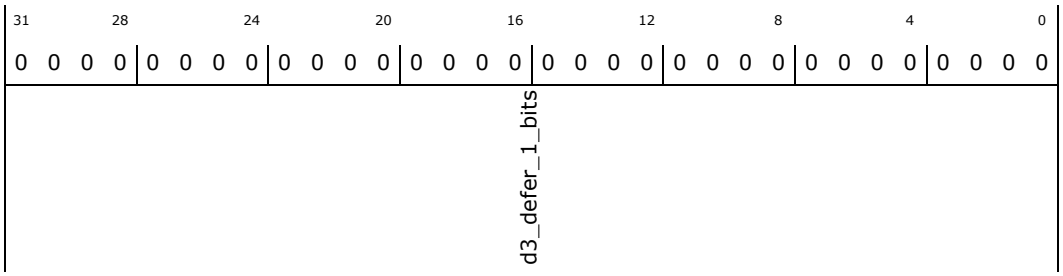
D3 defer for IPs

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + E4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**D3 DEFER - 1 (d3_defer_1_bits):** When a bit is set, the corresponding function should be disabled - refer to D3_STS_1 for mappings

10.2.58 Bios communication register for PMC (BIOS_COMM_SPARE0)—Offset ECh

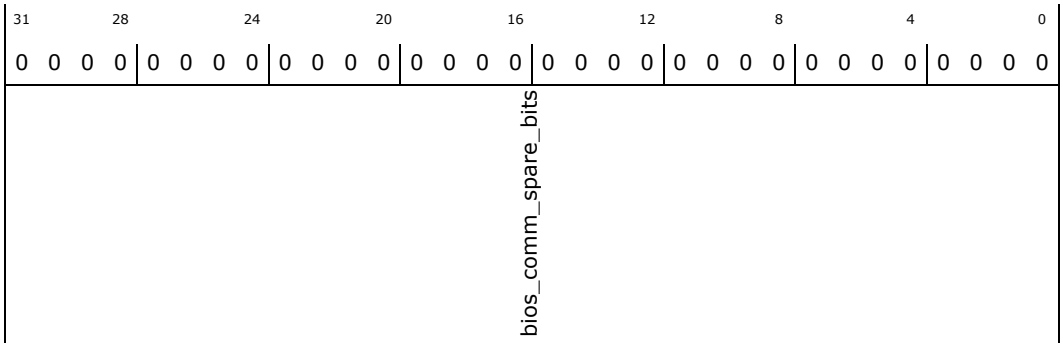
Bios communication requirements we may need/discover

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + ECh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**BIOS_COMM_SPARE (bios_comm_spare_bits):** Bios communication register - enables BIOS communication flags to be posted to PMC FW for later use NOTE: Access needs to be through IOSF primary in order for PMC to service a request BIOS_COMM_SPARE_0/1/2/3/4 [31] : PMC FW Update in progress 1'b1 - PMC FW has acknowledged the request from BIOS to update PMC behavior, is processing request 1'b0 - PMC FW not processing a BIOS update BIOS_COMM_SPARE_0/1/2/3/4 [30:16] : RESERVED BIOS_COMM_SPARE_0/1/2/3/4 [15] : BIOS Update request 1'b1 - BIOS RMWs setting this bit to 1'b1 when requesting a change in behavior on PMCs part 1'b0 - PMC FW only write 1'b0 to this bit when firmware update request has completed (PMC FW will also set BIOS_COMM[31] = 0 BIOS_COMM_SPARE_0 [14:2] : RESERVED FOR FUTURE USE BIOS_COMM_SPARE_0 [3] : LPE OSC force ON enable 1'b1 - Force LPE OSC clock on (CCU CLGATE_EN_3) 1'b0 - Release LPE OSC clock force on (CCU CLGATE_EN_3) BIOS_COMM_SPARE_0 [2] : RESERVED FOR FUTURE USE BIOS_COMM_SPARE_0 [1] : SSIC PHY common power lane request change (pmu_mphy_cmnln_core_pwr_up) 1'b1 - assert power 1'b0 - deassert power BIOS_COMM_SPARE_0 [0] : PERIODIC_GPIO_RCOMP_Enable, BIOS flag to PMC which specifies that PMC FW is required to periodically update the GPIO RCOMP values for LPC and Fast SPI 1'b1 - enable 1'b0 - disable BIOS_COMM_SPARE_1/2/3/4 [14:0] : RESERVED FOR FUTURE USE

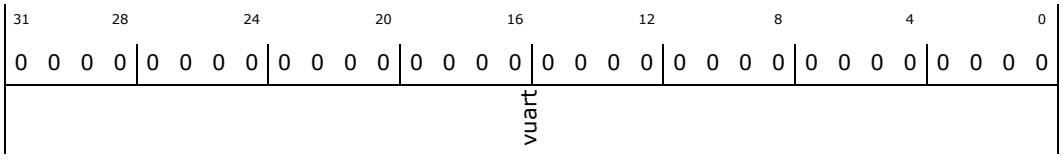
10.2.59 Virtual UART register (VUART1)—Offset F0h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + F0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Virtual UART register (vuart):** Reserved.

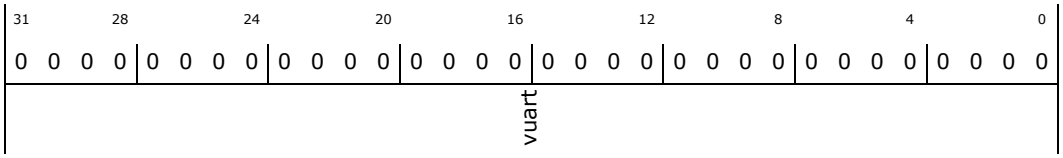
10.2.60 Virtual UART register (VUART2)—Offset F4h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + F4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Virtual UART register (vuart):** Reserved.

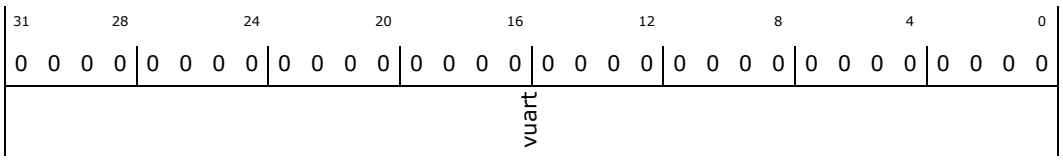
10.2.61 Virtual UART register (VUART3)—Offset F8h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Virtual UART register (vuart):** Reserved.

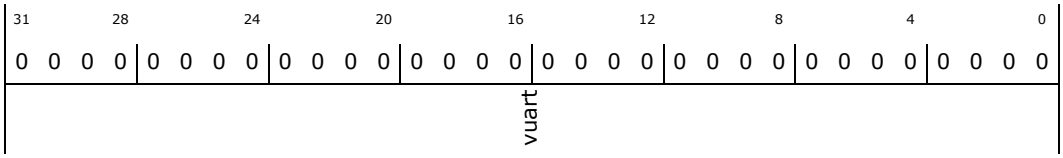
10.2.62 Virtual UART register (VUART4)—Offset FCh

Access Method

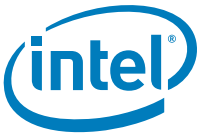
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [PMC_BASE_ADDRESS] + FCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Virtual UART register (vuart):** Reserved.



10.3 PCU PMC I/O Registers

Table 98. Summary of PCU PMC I/O Registers—

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
92–92h	1	"PORT92: Init Register (PORT92)—Offset 92h" on page 4863	00h
B2–B2h	1	"APM Register (APM)—Offset B2h" on page 4863	00h
B3–B3h	1	"APM_STS Register (APM_STS)—Offset B3h" on page 4863	00h
CF9–CF9h	1	"RST_CNT: Reset Control Register (RST_CNT)—Offset CF9h" on page 4864	00h

10.3.1 PORT92: Init Register (PORT92)—Offset 92h

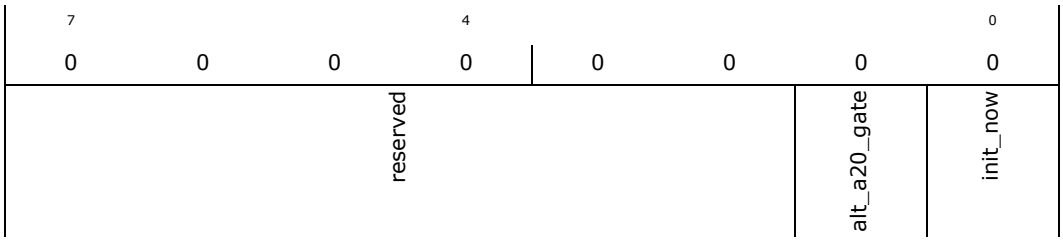
PORT92 initialization register (for BIOS)

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 92h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:2	0x0 RO	**reserved:** Reserved.
1	0x0 RW	**ALT_A20_GATE - Alternate A20 Gate (alt_a20_gate):** Legacy bit - kept just in case DOS expects it to be read/write
0	0x0 RW	**INIT_NOW (init_now):** When this bit transitions from a 0 to a 1, PMC will sent an INIT# VLW to T-Unit

10.3.2 APM Register (APM)—Offset B2h

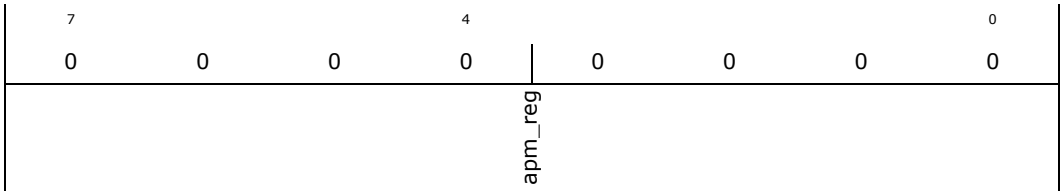
Advanced Power Management Register

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: B2h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**APM_Register (apm_reg):** TBD

10.3.3 APM_STS Register (APM_STS)—Offset B3h

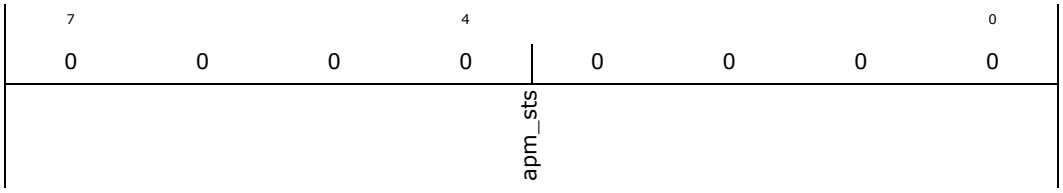
Advanced Power Management Status Register

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: B3h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**APM_STS (apm_sts):** Advanced Power Managment Status Port. used to pass data between the OS and the SMI handler. Basically, this is scratchpad register and is not effected by any other register or function (other than a PCI reset)

10.3.4 RST_CNT: Reset Control Register (RST_CNT)—Offset CF9h

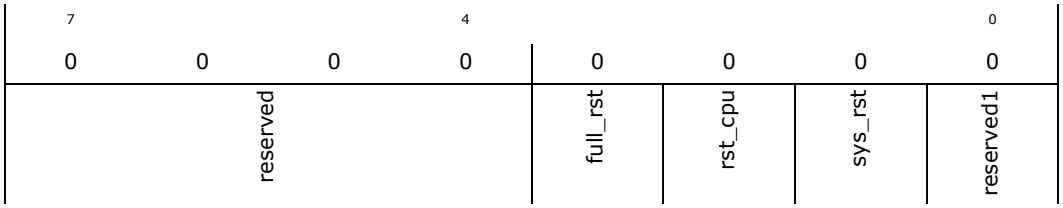
Reset Control Register

Access Method

Type: I/O Register
(Size: 8 bits)

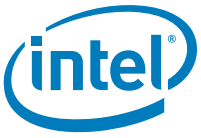
Offset: CF9h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:4	0x0 RO	**reserved:** Reserved.
3	0x0 RW	**Full Reset (FULL_RST) (full_rst):** When this bit is set to 1 and bit 1 is set to 1 (indicating Hard Reset, not Soft Reset), and the RST_CPU bit (bit 2) is written from 0 to 1, the PMC will do a full reset, including driving PMU_SLP_S3_B and PMU_SLP_S4_B active (low) for at least 3 (and no more than 6) seconds. When this bit is set, it also causes the full power cycle (PMU_SLP_S3/4_B assertion) in response to PMU_RESETBUTTON_B, COREPWROK, and Watchdog timer reset sources.
2	0x0 RW	**Reset CPU (RST_CPU) (rst_cpu):** This bit will cause either a hard or soft reset to the CPU depending on the state of the SYS_RST bit (bit 1 in this same register). The software will cause the reset by setting bit 2 from a 0 to a 1.

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**System Reset (SYS_RST) (sys_rst):** This bit determines the type of reset caused via RST_CPU (bit 2 of this register). If SYS_RST is 0 when RST_CPU goes from 0 to 1, then the PMC will force INIT# active for 16 PCI clocks. If SYS_RST is 1 when RST_CPU goes from 0 to 1, then the PMC will force PCI reset active for about 1 ms, however the PMU_SLP_S3_B and PMU_SLP_S4_B signals assertion is dependent on the value of the FULL_RST (bit3 of this register).
0	0x0 RO	**reserved1:** Reserved.



10.4 GPIO_EAST_Registers Address Map

Table 99. Summary of Message Bus Registers—0xA8

Offset	Register Name (Register Symbol)	Default Value
0–3h	"GPIO Read Access Control (gpio_read_access_policy_access_reg)—Offset 0h" on page 4868	FFFFFFFFh
4–7h	"GPIO Read Access Control (gpio_read_access_policy_wake_reg)—Offset 4h" on page 4868	FFFFFFFFh
8–Bh	"GPIO Read Access Control (gpio_read_access_policy_interrupt_reg)—Offset 8h" on page 4869	FFFFFFFFh
C–Fh	"GPIO Read Access Control (gpio_read_access_policy_community_reg)—Offset Ch" on page 4869	FFFFFFFFh
10–13h	"GPIO Read Access Control (gpio_read_access_policy_family_broadcast_reg)—Offset 10h" on page 4870	FFFFFFFFh
14–17h	"GPIO Read Access Control (gpio_read_access_policy_family_reg)—Offset 14h" on page 4870	FFFFFFFFh
18–1Bh	"GPIO Read Access Control (gpio_read_access_policy_pad_broadcast_reg)—Offset 18h" on page 4871	FFFFFFFFh
1C–1Fh	"GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_4x2_12_0_regs)—Offset 1Ch" on page 4872	FFFFFFFFh
20–23h	"GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_4x2_12_1_regs)—Offset 20h" on page 4872	FFFFFFFFh
100–103h	"GPIO Write Access Control (gpio_write_access_policy_access_reg)—Offset 100h" on page 4873	FFFFFFFFh
104–107h	"GPIO Write Access Control (gpio_write_access_policy_wake_reg)—Offset 104h" on page 4873	FFFFFFFFh
108–10Bh	"GPIO Write Access Control (gpio_write_access_policy_interrupt_reg)—Offset 108h" on page 4874	FFFFFFFFh
10C–10Fh	"GPIO Write Access Control (gpio_write_access_policy_community_reg)—Offset 10Ch" on page 4874	FFFFFFFFh
110–113h	"GPIO Write Access Control (gpio_write_access_policy_family_broadcast_reg)—Offset 110h" on page 4875	FFFFFFFFh
114–117h	"GPIO Write Access Control (gpio_write_access_policy_family_reg)—Offset 114h" on page 4876	FFFFFFFFh
118–11Bh	"GPIO Write Access Control (gpio_write_access_policy_pad_broadcast_reg)—Offset 118h" on page 4876	FFFFFFFFh
11C–11Fh	"GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_4x2_12_0_regs)—Offset 11Ch" on page 4877	FFFFFFFFh
120–123h	"GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_4x2_12_1_regs)—Offset 120h" on page 4877	FFFFFFFFh
200–203h	"GPIO_WAKE_STATUS_REG #0 (gpio_wake_status_reg_0)—Offset 200h" on page 4878	00000000h

Offset	Register Name (Register Symbol)	Default Value
280–283h	"GPIO_WAKE_MASK_REG #0 (gpio_wake_mask_reg_0)—Offset 280h" on page 4880	00000000h
300–303h	"GPIO Interrupt Status (gpio_interrupt_status)—Offset 300h" on page 4881	00000000h
380–383h	"GPIO Interrupt Status (gpio_interrupt_mask)—Offset 380h" on page 4882	00000000h
1000–1003h	"GPIO Broadcast Data Mask bit Register (gpio_family_bw_mask_31_0)—Offset 1000h" on page 4882	00000000h
1004–1007h	"GPIO Broadcast Data Register (gpio_family_bw_data_31_0)—Offset 1004h" on page 4883	00000000h
1008–100Bh	"gpio_family_broadcast_reg_mask #0 (gpio_family_broadcast_reg_mask_0)—Offset 1008h" on page 4883	00000000h
1080–1083h	"RCOMP Control Register (ulpmsmvfamily_4x2_12_0_family_rcomp_control_reg)—Offset 1080h" on page 4885	00941D1Dh
1084–1087h	"RCOMP Offset Register (ulpmsmvfamily_4x2_12_0_family_rcomp_offset_reg)—Offset 1084h" on page 4887	00000000h
1088–108Bh	"RCOMP Override Register (ulpmsmvfamily_4x2_12_0_family_rcomp_override_reg)—Offset 1088h" on page 4888	00110202h
108C–108Fh	"RCOMP Value Register (ulpmsmvfamily_4x2_12_0_family_rcomp_value_reg)—Offset 108Ch" on page 4889	00110202h
1090–1093h	"family_config_rcomp_reg (ulpmsmvfamily_4x2_12_0_family_config_rcomp_reg)—Offset 1090h" on page 4889	02020311h
1094–1097h	"gpio_family_configuration_register (ulpmsmvfamily_4x2_12_0_family_config_reg)—Offset 1094h" on page 4890	05C00000h

10.4.1 GPIO Read Access Control (gpio_read_access_policy_access_reg)—Offset 0h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access. Refer Security HAS

Access Method

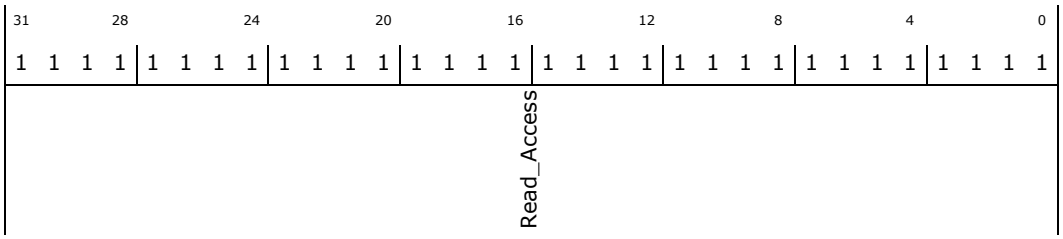
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 0h

Op Codes:

h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.4.2 GPIO Read Access Control (gpio_read_access_policy_wake_reg)—Offset 4h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access. Refer Security HAS

Access Method

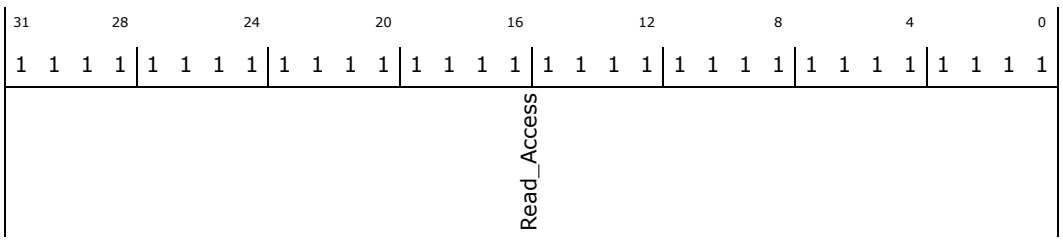
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 4h

Op Codes:

h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.4.3 GPIO Read Access Control (gpio_read_access_policy_interrupt_reg)—Offset 8h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access. Refer Security HAS

Access Method

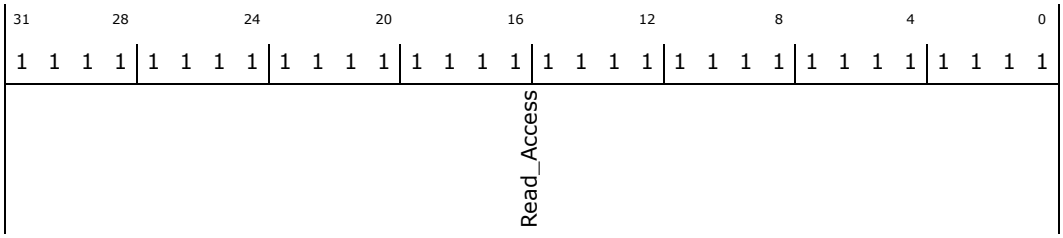
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 8h

Op Codes:

h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.4.4 GPIO Read Access Control (gpio_read_access_policy_community_reg)—Offset Ch

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access. Refer Security HAS

Access Method

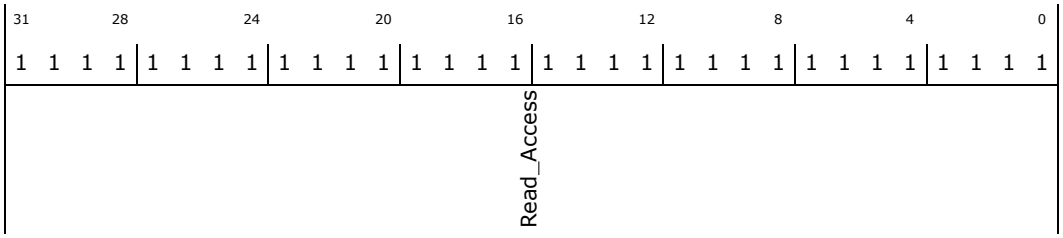
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + Ch

Op Codes:

h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.4.5 GPIO Read Access Control (gpio_read_access_policy_family_broadcast_reg)—Offset 10h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access. Refer Security HAS

Access Method

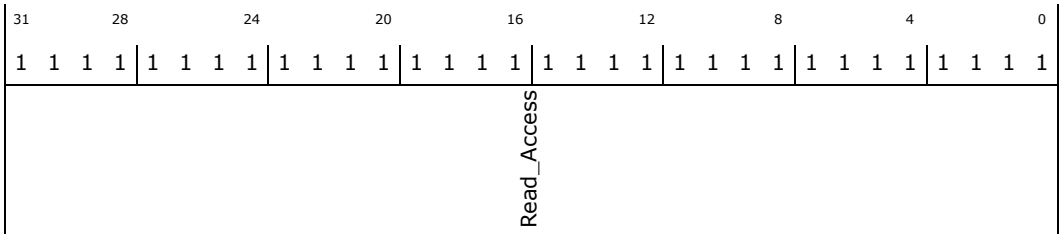
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 10h

Op Codes:

h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.4.6 GPIO Read Access Control (gpio_read_access_policy_family_reg)—Offset 14h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access. Refer Security HAS

Access Method

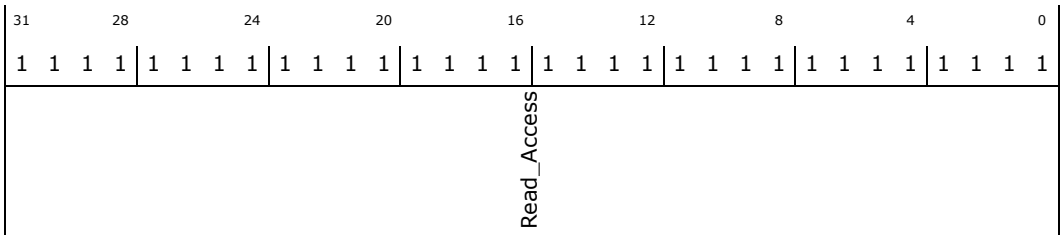
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 14h

Op Codes:

h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.4.7 GPIO Read Access Control (gpio_read_access_policy_pad_broadcast_reg)—Offset 18h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access. Refer Security HAS

Access Method

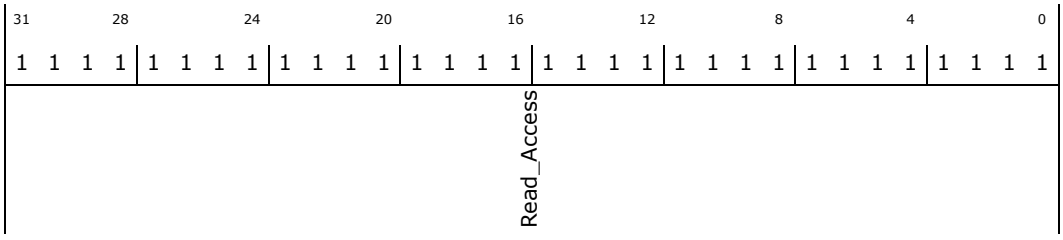
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 18h

Op Codes:

h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.4.8 GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_4x2_12_0_regs)—Offset 1Ch

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access. Refer Security HAS

Access Method

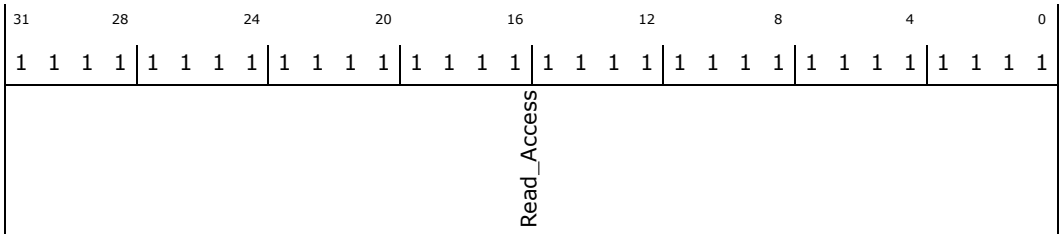
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 1Ch

Op Codes:

h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.4.9 GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_4x2_12_1_regs)—Offset 20h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access. Refer Security HAS

Access Method

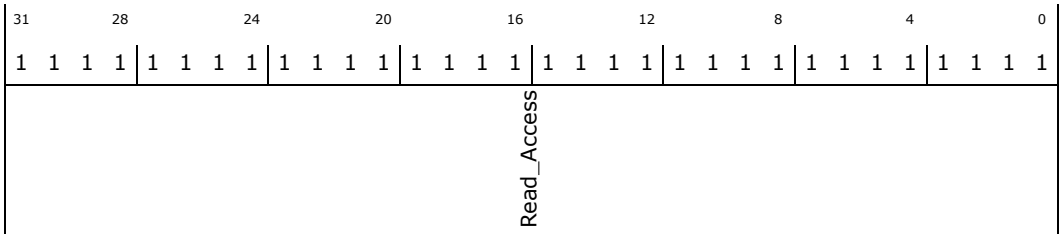
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 20h

Op Codes:

h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.4.10 GPIO Write Access Control (gpio_write_access_policy_access_reg)—Offset 100h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access. Refer Security HAS

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 100h

Op Codes:

h - Read, h - Write

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.4.11 GPIO Write Access Control (gpio_write_access_policy_wake_reg)—Offset 104h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access. Refer Security HAS

Access Method

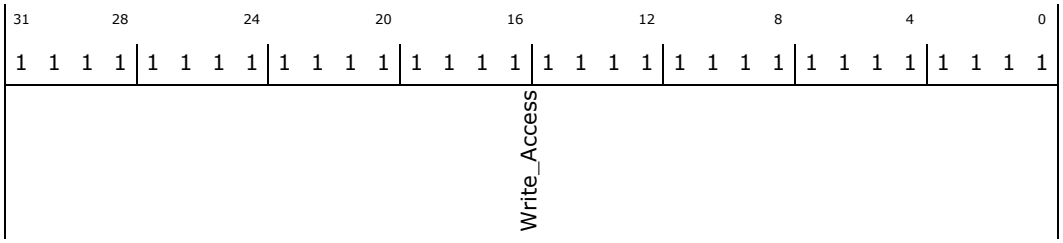
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 104h

Op Codes:

h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.4.12 GPIO Write Access Control (gpio_write_access_policy_interrupt_reg)—Offset 108h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access. Refer Security HAS

Access Method

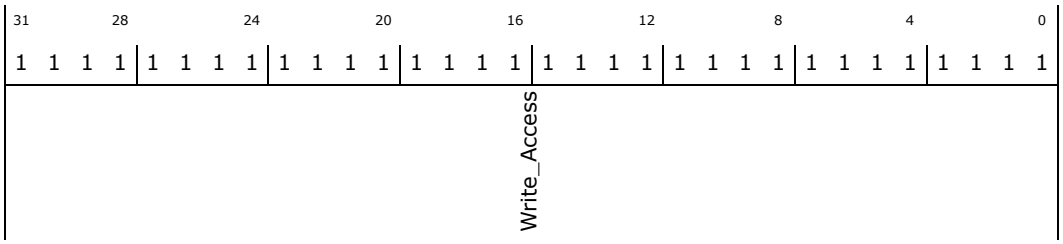
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 108h

Op Codes:

h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.4.13 GPIO Write Access Control (gpio_write_access_policy_community_reg)—Offset 10Ch

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access. Refer Security HAS

Access Method

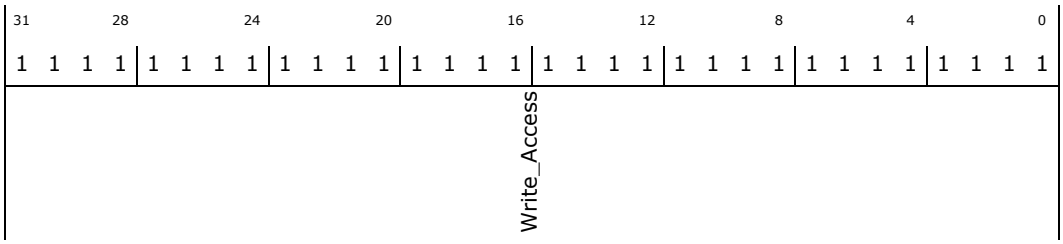
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 10Ch

Op Codes:

h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.4.14 GPIO Write Access Control (gpio_write_access_policy_family_broadcast_reg)—Offset 110h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access. Refer Security HAS

Access Method

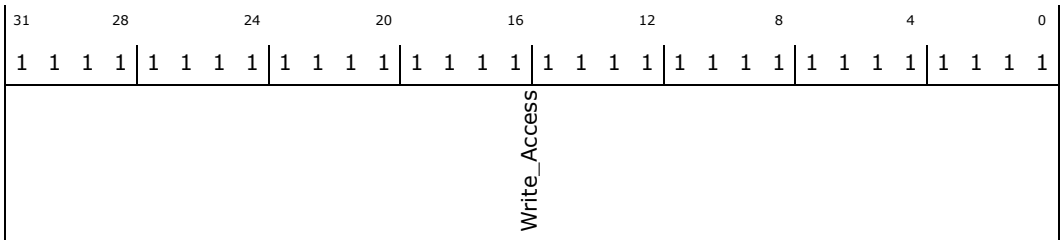
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 110h

Op Codes:

h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.4.15 GPIO Write Access Control (gpio_write_access_policy_family_reg)—Offset 114h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access. Refer Security HAS

Access Method

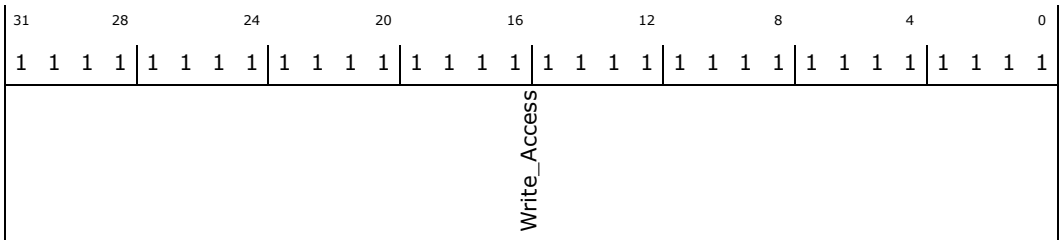
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 114h

Op Codes:

h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.4.16 GPIO Write Access Control (gpio_write_access_policy_pad_broadcast_reg)—Offset 118h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access. Refer Security HAS

Access Method

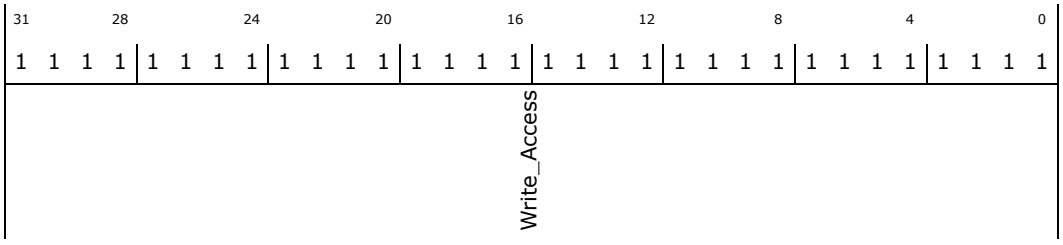
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 118h

Op Codes:

h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.4.17 GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_4x2_12_0_regs)—Offset 11Ch

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access. Refer Security HAS

Access Method

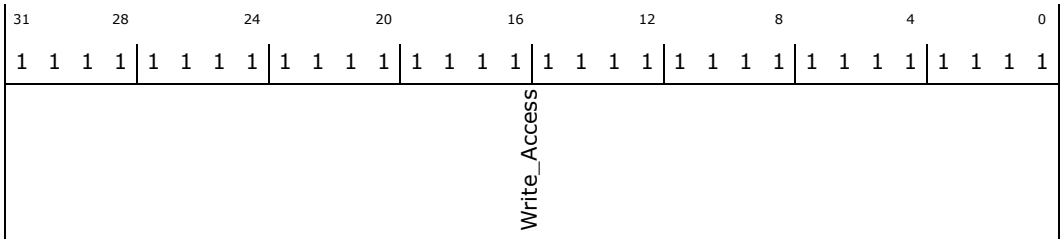
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 11Ch

Op Codes:

h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.4.18 GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_4x2_12_1_regs)—Offset 120h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access. Refer Security HAS

Access Method

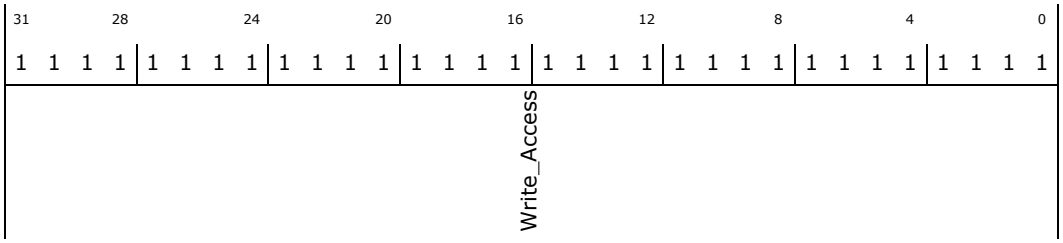
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 120h

Op Codes:

h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.4.19 GPIO_WAKE_STATUS_REG #0 (gpio_wake_status_reg_0)—Offset 200h

GPIO Wake Status Register write 1 to clear.

Access Method

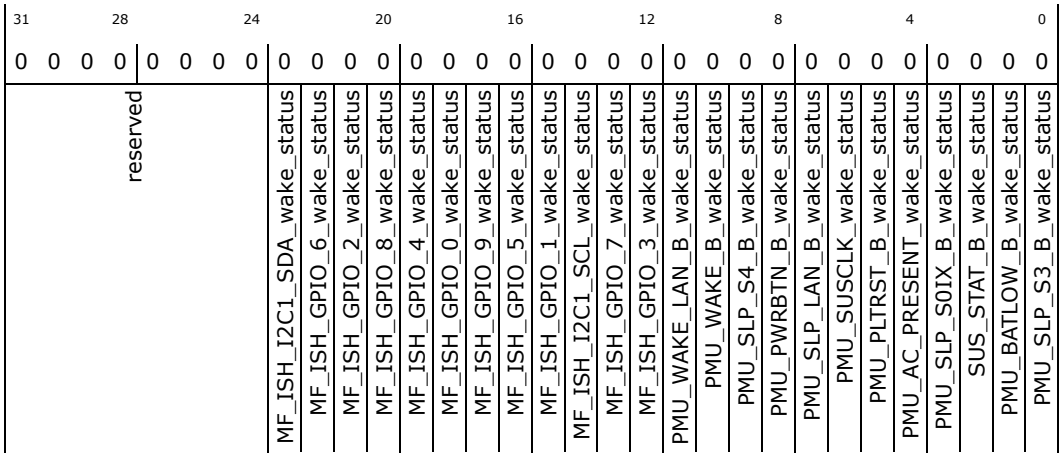
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 200h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW/1C	**reserved:** Reserved.
23	0x0 RW/1C	**MF_ISH_I2C1_SDA_wake_status:** Reserved.
22	0x0 RW/1C	**MF_ISH_GPIO_6_wake_status:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21	0x0 RW/1C	**MF_ISH_GPIO_2_wake_status:** Reserved.
20	0x0 RW/1C	**MF_ISH_GPIO_8_wake_status:** Reserved.
19	0x0 RW/1C	**MF_ISH_GPIO_4_wake_status:** Reserved.
18	0x0 RW/1C	**MF_ISH_GPIO_0_wake_status:** Reserved.
17	0x0 RW/1C	**MF_ISH_GPIO_9_wake_status:** Reserved.
16	0x0 RW/1C	**MF_ISH_GPIO_5_wake_status:** Reserved.
15	0x0 RW/1C	**MF_ISH_GPIO_1_wake_status:** Reserved.
14	0x0 RW/1C	**MF_ISH_I2C1_SCL_wake_status:** Reserved.
13	0x0 RW/1C	**MF_ISH_GPIO_7_wake_status:** Reserved.
12	0x0 RW/1C	**MF_ISH_GPIO_3_wake_status:** Reserved.
11	0x0 RW/1C	**PMU_WAKE_LAN_B_wake_status:** Reserved.
10	0x0 RW/1C	**PMU_WAKE_B_wake_status:** Reserved.
9	0x0 RW/1C	**PMU_SLP_S4_B_wake_status:** Reserved.
8	0x0 RW/1C	**PMU_PWRBTN_B_wake_status:** Reserved.
7	0x0 RW/1C	**PMU_SLP_LAN_B_wake_status:** Reserved.
6	0x0 RW/1C	**PMU_SUSCLK_wake_status:** Reserved.
5	0x0 RW/1C	**PMU_PLTRST_B_wake_status:** Reserved.
4	0x0 RW/1C	**PMU_AC_PRESENT_wake_status:** Reserved.
3	0x0 RW/1C	**PMU_SLP_S0IX_B_wake_status:** Reserved.
2	0x0 RW/1C	**SUS_STAT_B_wake_status:** Reserved.
1	0x0 RW/1C	**PMU_BATLOW_B_wake_status:** Reserved.
0	0x0 RW/1C	**PMU_SLP_S3_B_wake_status:** Reserved.

10.4.20 GPIO_WAKE_MASK_REG #0 (gpio_wake_mask_reg_0)—Offset 280h

GPIO Wake Register 0 Masks Wake.

Access Method

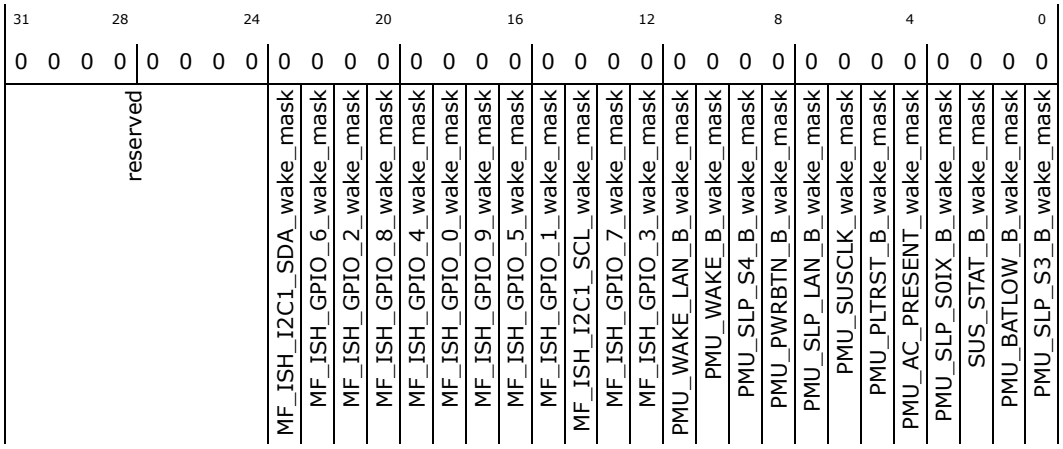
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 280h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**reserved:** Reserved.
23	0x0 RW	**MF_ISH_I2C1_SDA_wake_mask:** Reserved.
22	0x0 RW	**MF_ISH_GPIO_6_wake_mask:** Reserved.
21	0x0 RW	**MF_ISH_GPIO_2_wake_mask:** Reserved.
20	0x0 RW	**MF_ISH_GPIO_8_wake_mask:** Reserved.
19	0x0 RW	**MF_ISH_GPIO_4_wake_mask:** Reserved.
18	0x0 RW	**MF_ISH_GPIO_0_wake_mask:** Reserved.
17	0x0 RW	**MF_ISH_GPIO_9_wake_mask:** Reserved.
16	0x0 RW	**MF_ISH_GPIO_5_wake_mask:** Reserved.
15	0x0 RW	**MF_ISH_GPIO_1_wake_mask:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW	**MF_ISH_I2C1_SCL_wake_mask:** Reserved.
13	0x0 RW	**MF_ISH_GPIO_7_wake_mask:** Reserved.
12	0x0 RW	**MF_ISH_GPIO_3_wake_mask:** Reserved.
11	0x0 RW	**PMU_WAKE_LAN_B_wake_mask:** Reserved.
10	0x0 RW	**PMU_WAKE_B_wake_mask:** Reserved.
9	0x0 RW	**PMU_SLP_S4_B_wake_mask:** Reserved.
8	0x0 RW	**PMU_PWRBTN_B_wake_mask:** Reserved.
7	0x0 RW	**PMU_SLP_LAN_B_wake_mask:** Reserved.
6	0x0 RW	**PMU_SUSCLK_wake_mask:** Reserved.
5	0x0 RW	**PMU_PLTRST_B_wake_mask:** Reserved.
4	0x0 RW	**PMU_AC_PRESENT_wake_mask:** Reserved.
3	0x0 RW	**PMU_SLP_S0IX_B_wake_mask:** Reserved.
2	0x0 RW	**SUS_STAT_B_wake_mask:** Reserved.
1	0x0 RW	**PMU_BATLOW_B_wake_mask:** Reserved.
0	0x0 RW	**PMU_SLP_S3_B_wake_mask:** Reserved.

10.4.21 GPIO Interrupt Status (gpio_interrupt_status)—Offset 300h

Status bits for the 16 interrupts.

Access Method

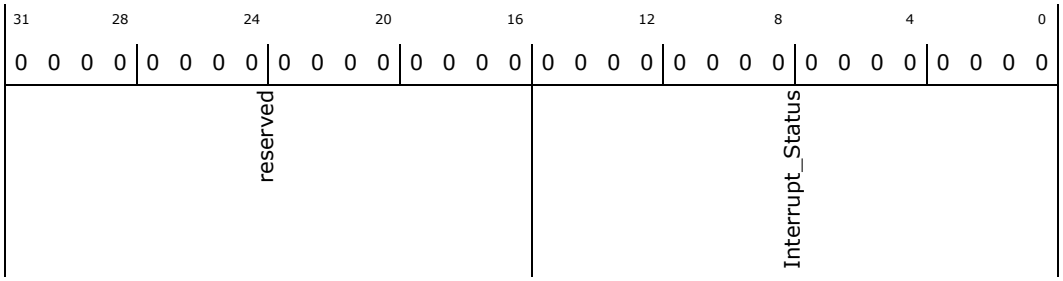
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 300h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/1C	**reserved:** reserved
15:0	0x0 RW/1C	**Interrupt Status (Interrupt_Status):** Status bits for the 16 interrupts. Write 1 to Clear

10.4.22 GPIO Interrupt Status (gpio_interrupt_mask)—Offset 380h

Mask bits for the 16 interrupts.

Access Method

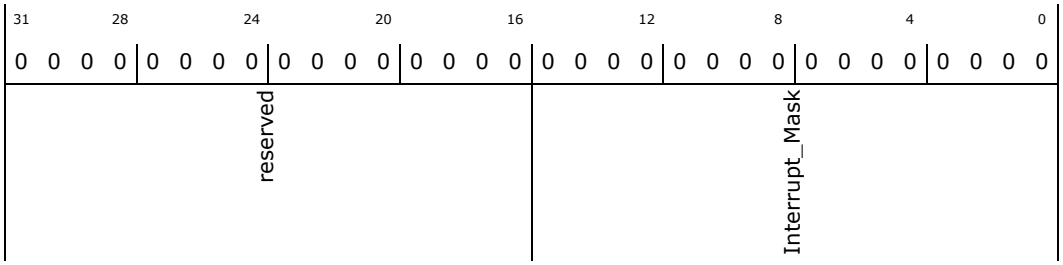
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 380h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**reserved:** reserved
15:0	0x0 RW	**Interrupt Mask (Interrupt_Mask):** Mask bits for the 16 interrupts. Interrupt masked when 0.

10.4.23 GPIO Broadcast Data Mask bit Register (gpio_family_bw_mask_31_0)—Offset 1000h

Write Mask that masks bit by bit the data written to BWData

Access Method

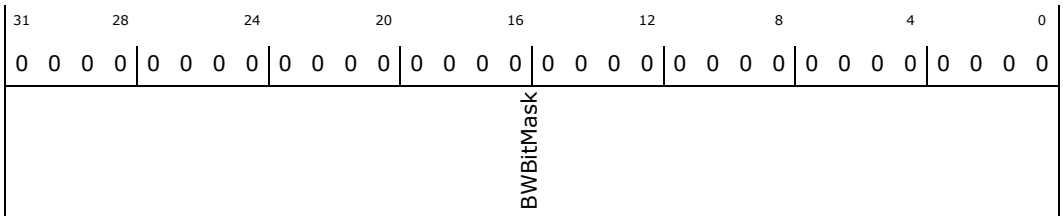
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 1000h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**BWBitMask:** Reserved.

10.4.24 GPIO Broadcast Data Register (gpio_family_bw_data_31_0)—Offset 1004h

Broadcast Write Data

Access Method

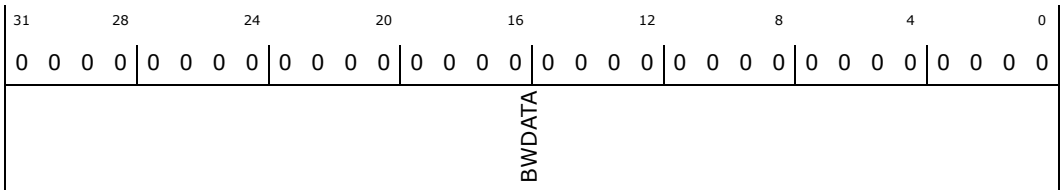
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 1004h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 WO	**BWDATA:** Reserved.

10.4.25 gpio_family_broadcast_reg_mask #0 (gpio_family_broadcast_reg_mask_0)—Offset 1008h

Family Broadcast Register Masking

Access Method

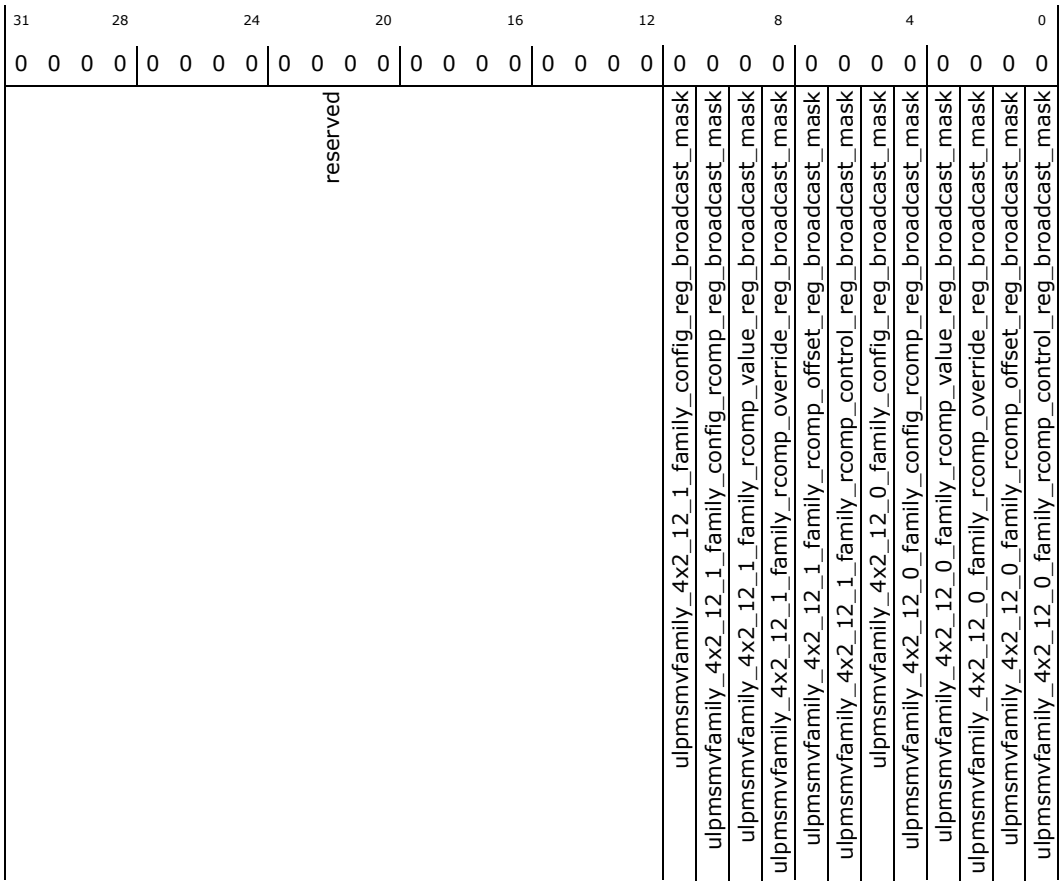
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 1008h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**reserved:** Reserved.
11	0x0 RW	**ulpmsmvfamily_4x2_12_1_family_config_reg_broadcast_mask:** Reserved.
10	0x0 RW	**ulpmsmvfamily_4x2_12_1_family_config_rcomp_reg_broadcast_mask:** Reserved.
9	0x0 RW	**ulpmsmvfamily_4x2_12_1_family_rcomp_value_reg_broadcast_mask:** Reserved.
8	0x0 RW	**ulpmsmvfamily_4x2_12_1_family_rcomp_override_reg_broadcast_mask:** Reserved.
7	0x0 RW	**ulpmsmvfamily_4x2_12_1_family_rcomp_offset_reg_broadcast_mask:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
6	0x0 RW	**ulpmsmvfamily_4x2_12_1_family_rcomp_control_reg_broadcast_mask:** Reserved.
5	0x0 RW	**ulpmsmvfamily_4x2_12_0_family_config_reg_broadcast_mask:** Reserved.
4	0x0 RW	**ulpmsmvfamily_4x2_12_0_family_config_rcomp_reg_broadcast_mask:** Reserved.
3	0x0 RW	**ulpmsmvfamily_4x2_12_0_family_rcomp_value_reg_broadcast_mask:** Reserved.
2	0x0 RW	**ulpmsmvfamily_4x2_12_0_family_rcomp_override_reg_broadcast_mask:** Reserved.
1	0x0 RW	**ulpmsmvfamily_4x2_12_0_family_rcomp_offset_reg_broadcast_mask:** Reserved.
0	0x0 RW	**ulpmsmvfamily_4x2_12_0_family_rcomp_control_reg_broadcast_mask:** Reserved.

10.4.26 RCOMP Control Register (ulpmsmvfamily_4x2_12_0_family_rcomp_control_reg)—Offset 1080h

RCOMP Control Register

Access Method

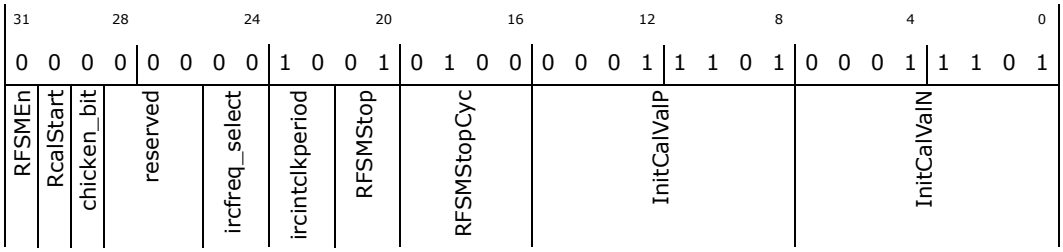
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 1080h

Op Codes:

h - Read, h - Write

Default: 00941D1Dh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**RCOMP FSM Enable (RFSMEn):** 0 = state machine disabled (clock gated) 1 = state machine enabled It is important to have this bit enabled in order for all internal clocks inside the RCOMP FSM to run.

Bit Range	Default & Access	Field Name (ID): Description
30	0x0 RW	**RCOMP Calibration Start (RcalStart):** When set to 1 this bit triggers the RCOMP FSM to start hunting for the correct values for strength and slew. This bit should be cleared after calibration has finished. Before setting the RcalStart bit RFSMEn must have been asserted for at least 5 clock cycles. The first calibration takes 10us to complete and subsequent calibrations take 3us. Details of this process are in the CFIP RCOMP Aspec.
29	0x0 RW	**RCOMP FSM Binary Chicken Bit (chicken_bit):** Toggling this bit Simulates a V1P8 Mode change. This will allow Binary re-calibration
28:26	0x0 RW	**reserved:** reserved
25:24	0x0 RW	**IRCCLK Frequency Select (ircfreq_select):** Clock ircclk frequency. This signals indicate what frequency ircclk is. This is used for 1ms and 10ms counters. 00 if clk input is 25MHz (default, and SoC Clock) 01 if 50MHz 10 if 100MHz 11 if 125MHz
23:22	0x2 RW	**IRC Internal Clock Period (ircintclkperiod):** To select rcomp clock period. This is the compensation clock frequency/period. Clock is derived from ircclk (which can be 25MHz, 50MHz, 100MHz or 125MHz user must set ircfreq_select[1:0] accordingly) 00 40ns (64ns for ircclk=125MHz) 01 80ns (96ns for ircclk=125MHz) 10 120ns (128ns for ircclk=125MHz) (default) 11 160ns (192ns for ircclk=125MHz)
21:20	0x1 RW	**RCOMP FSM Stop Condition (RFSMStop):** RCOMP FSM Stop calibration condition. RCOMP FSM (pullup and pulldown) will finish calibrating once orcpupen/orcpdnen toggles. The toggling indicates the compensation value has been reached. This option is programmable for toggle once (single edge), toggle twice (double edge), toggle thrice (triple edge) or forcing it to finish after a certain cycle (defined by RFSMStopCyc). 00b = single edge detect (10 or 01) 01b = double egde detect (101 or 010) (default) 10b = triple edge detect (1010 or 0101) 11b = stop after x cycles (depending on ircstpcyc[3:0] value -- This is meant for debug)
19:16	0x4 RW	**RCOMP FSM Stop Cycles (RFSMStopCyc):** Number of cycles to stop RCOMP FSM from searching for strength and slew settings. RFSMStop must be set to 11b for this option to take affect. 0000b = 0 cycle (illegal option) 0001b = 1 cycle (illegal option) 0010b = 2 cycles (illegal option) 0011b = 3 cycles (illegal option) 0100b = 4 cycles ... 1110b = 14 cycles 1111b = 15 cycles (maximum allowed) This is meant for debug.
15:8	0x1d RW	**Initial Pull Up Value (InitCalValP):** Initial pleg calibration value. RCOMP FSM will always start with this values for pullup calibration.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x1d RW	**Initial Pull Down Value (InitCalValN):** Initial nleg calibration value. RCOMP FSM will always start with this values for pulldown calibration.

10.4.27 RCOMP Offset Register (ulpmsmvfamily_4x2_12_0_family_rcomp_offset_reg)—Offset 1084h

RCOMP Offset Register

Access Method

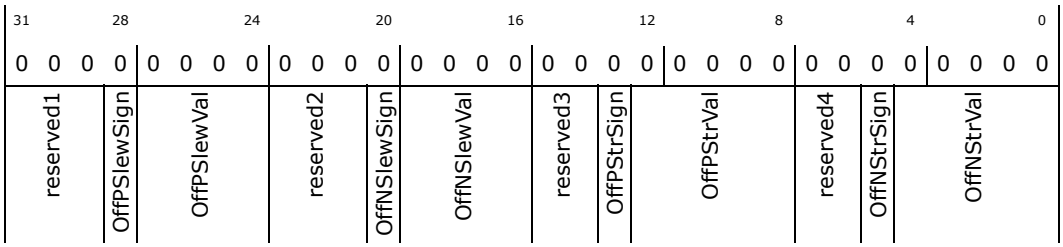
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 1084h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**Reserved (reserved1):** Reserved
28	0x0 RW	**Pull Up Offset Slew Sign (OffPSlewSign):** Sign Bit for PSlew Offset strength value.
27:24	0x0 RW	**Pull Up Slew Offset (OffPSlewVal):** Offset slew value for pleg.
23:21	0x0 RW	**Reserved (reserved2):** Reserved
20	0x0 RW	**Pull Down Offset Slew Sign (OffNSlewSign):** Sign Bit for NSlew Offset strength value.
19:16	0x0 RW	**Pull Down Slew Offset (OffNSlewVal):** Offset slew value for nleg.
15:14	0x0 RW	**Reserved (reserved3):** Reserved
13	0x0 RW	**Pull Up Offset Strength Sign (OffPStrSign):** Sign Bit for PStrength Offset value.
12:8	0x0 RW	**Pull Up Offset Strength Value (OffPStrVal):** PStrength Offset Value.

Bit Range	Default & Access	Field Name (ID): Description
7:6	0x0 RW	**Reserved (reserved4):** Reserved
5	0x0 RW	**Pull Down Offset Strength Sign (OffNStrSign):** Sign Bit for NStrength Offset value.
4:0	0x0 RW	**Pull Down Offset Strength Value (OffNStrVal):** NStrength Offset Value.

10.4.28 RCOMP Override Register (ulpmsmvfamily_4x2_12_0_family_rcomp_override_reg) —Offset 1088h

RCOMP Override Register

Access Method

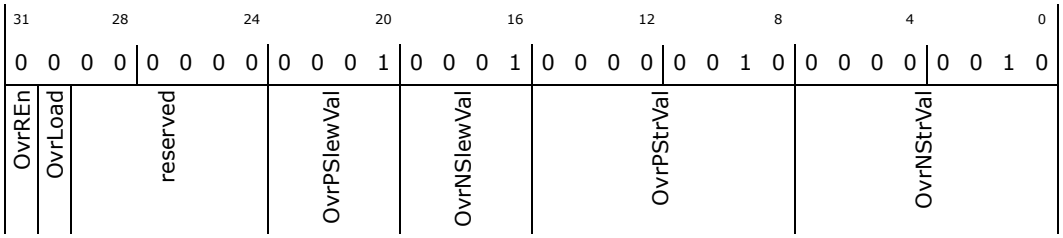
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 1088h

Op Codes:

h - Read, h - Write

Default: 00110202h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**Override RCOMP Enable (OvrREn):** Override enable bit to override the strength and slew values driven by the RCOMP FSM. The override values are driven through config registers. 0 = Override Disable 1 = Override Enable
30	0x0 RW	**Override Load (OvrLoad):** Load the override values into the RCOMP FSM and drive these values to the CFIO buffer. This is only valid when OvrRen = 1. 0 = Unload Values 1 = Load Values to CFIO
29:24	0x0 RW	**reserved:** reserved
23:20	0x1 RW	**Override P Slew Value (OvrPSlewVal):** Override slew values for pullup settings.
19:16	0x1 RW	**Override N Slew Value (OvrNSlewVal):** Override slew values for pulldown settings.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x2 RW	**Override Pull Up Strength Value (OvrPStrVal):** Override strength value for pullup settings. Should be 50ohm typical corner.
7:0	0x2 RW	**Override Pull Down Strength Value (OvrNStrVal):** Override strength value for pulldown settings. Should be 50ohm typical corner.

10.4.29 RCOMP Value Register (ulpmsmvfamily_4x2_12_0_family_rcomp_value_reg)—Offset 108Ch

RCOMP Value Register

Access Method

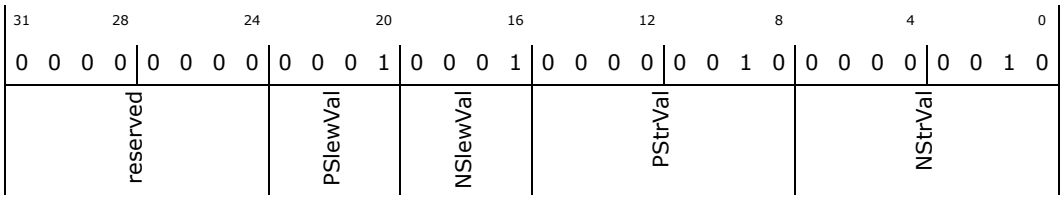
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 108Ch

Op Codes:

h - Read, h - Write

Default: 00110202h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**reserved_fam1 (reserved):** reserved
23:20	0x1 RO	**P Slew Value (PSlewVal):** P Slew values. Valid only after calibration is done.
19:16	0x1 RO	**N Slew Value (NSlewVal):** N Slew values. Valid only after calibration is done.
15:8	0x2 RO	**Pull Up Strength Value (PStrVal):** Compensation strength for pleg. This is valid only after calibration is done.
7:0	0x2 RO	**Pull Down Strength Value (NStrVal):** Compensation strength for nleg. This is valid only after calibration is done.

10.4.30 family_config_rcomp_reg (ulpmsmvfamily_4x2_12_0_family_config_rcomp_reg)—Offset 1090h

GPIO Family RCOMP Register

Access Method

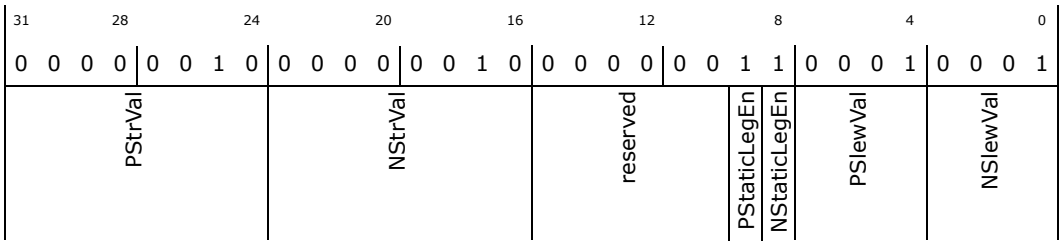
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 1090h

Op Codes:

h - Read, h - Write

Default: 02020311h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x2 RW	**Pull Up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per pull down and pull up.
23:16	0x2 RW	**Pull Down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per pull down and pull up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable
7:4	0x1 RW	**P Slew Value (PSlewVal):** Slew values for pullup settings.
3:0	0x1 RW	**N Slew Value (NSlewVal):** Slew values for pulldown settings.

10.4.31 gpio_family_configuration_register (ulpmsmvfamily_4x2_12_0_family_config_reg)—Offset 1094h

GPIO Family CFIO Configuration Register

Access Method

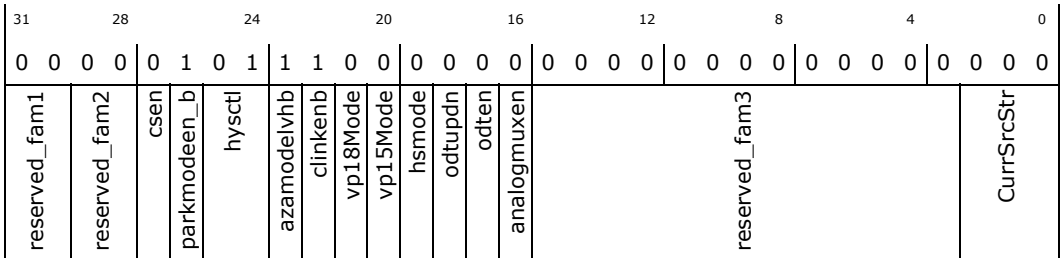
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xA8] + 1094h

Op Codes:

h - Read, h - Write

Default: 05C00000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces IO leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x1 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when IO is operating at 1.8V This ***must***

10.5 Summary of GPIO NORTH Message Bus Registers

Table 10-100.Summary of GPIO North Message Bus Registers—0x13

Offset	Register Name (Register Symbol)	Default Value
0–3h	"GPIO Read Access Control (gpio_read_access_policy_access_reg)—Offset 0h" on page 4899	FFFFFFFFh
4–7h	"GPIO Read Access Control (gpio_read_access_policy_wake_reg)—Offset 4h" on page 4899	FFFFFFFFh
8–Bh	"GPIO Read Access Control (gpio_read_access_policy_interrupt_reg)—Offset 8h" on page 4900	FFFFFFFFh
C–Fh	"GPIO Read Access Control (gpio_read_access_policy_community_reg)—Offset Ch" on page 4900	FFFFFFFFh
10–13h	"GPIO Read Access Control (gpio_read_access_policy_family_broadcast_reg)—Offset 10h" on page 4901	FFFFFFFFh
14–17h	"GPIO Read Access Control (gpio_read_access_policy_family_reg)—Offset 14h" on page 4901	FFFFFFFFh
18–1Bh	"GPIO Read Access Control (gpio_read_access_policy_pad_broadcast_reg)—Offset 18h" on page 4902	FFFFFFFFh
1C–1Fh	"GPIO Read Access Control (gpio_read_access_policy_ulphsmvfamily_2x4_rcomp_10_0_regs)—Offset 1Ch" on page 4903	FFFFFFFFh
20–23h	"GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_2x4_13_0_regs)—Offset 20h" on page 4903	FFFFFFFFh

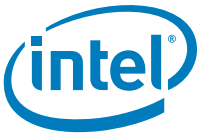


Table 10-100.Summary of GPIO North Message Bus Registers—0x13 (Continued)

Offset	Register Name (Register Symbol)	Default Value
24–27h	"GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_3x4_12_0_regs)—Offset 24h" on page 4904	FFFFFFFFh
28–2Bh	"GPIO Read Access Control (gpio_read_access_policy_ulphsmvfamily_2x4_12_0_regs)—Offset 28h" on page 4904	FFFFFFFFh
2C–2Fh	"GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_3x4_13_0_regs)—Offset 2Ch" on page 4905	FFFFFFFFh
100–103h	"GPIO Write Access Control (gpio_write_access_policy_access_reg)—Offset 100h" on page 4905	FFFFFFFFh
104–107h	"GPIO Write Access Control (gpio_write_access_policy_wake_reg)—Offset 104h" on page 4906	FFFFFFFFh
108–10Bh	"GPIO Write Access Control (gpio_write_access_policy_interrupt_reg)—Offset 108h" on page 4906	FFFFFFFFh
10C–10Fh	"GPIO Write Access Control (gpio_write_access_policy_community_reg)—Offset 10Ch" on page 4907	FFFFFFFFh
110–113h	"GPIO Write Access Control (gpio_write_access_policy_family_broadcast_reg)—Offset 110h" on page 4908	FFFFFFFFh
114–117h	"GPIO Write Access Control (gpio_write_access_policy_family_reg)—Offset 114h" on page 4908	FFFFFFFFh
118–11Bh	"GPIO Write Access Control (gpio_write_access_policy_pad_broadcast_reg)—Offset 118h" on page 4909	FFFFFFFFh
11C–11Fh	"GPIO Write Access Control (gpio_write_access_policy_ulphsmvfamily_2x4_rcomp_10_0_regs)—Offset 11Ch" on page 4909	FFFFFFFFh
120–123h	"GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_2x4_13_0_regs)—Offset 120h" on page 4910	FFFFFFFFh
124–127h	"GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_3x4_12_0_regs)—Offset 124h" on page 4910	FFFFFFFFh
128–12Bh	"GPIO Write Access Control (gpio_write_access_policy_ulphsmvfamily_2x4_12_0_regs)—Offset 128h" on page 4911	FFFFFFFFh
12C–12Fh	"GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_3x4_13_0_regs)—Offset 12Ch" on page 4912	FFFFFFFFh
200–203h	"GPIO_WAKE_STATUS_REG #0 (gpio_wake_status_reg_0)—Offset 200h" on page 4912	00000000h
204–207h	"GPIO_WAKE_STATUS_REG #1 (gpio_wake_status_reg_1)—Offset 204h" on page 4914	00000000h
280–283h	"GPIO_WAKE_MASK_REG #0 (gpio_wake_mask_reg_0)—Offset 280h" on page 4916	00000000h
284–287h	"GPIO_WAKE_MASK_REG #1 (gpio_wake_mask_reg_1)—Offset 284h" on page 4918	00000000h
300–303h	"GPIO Interrupt Status (gpio_interrupt_status)—Offset 300h" on page 4920	00000000h
380–383h	"GPIO Interrupt Status (gpio_interrupt_mask)—Offset 380h" on page 4921	00000000h
1000–1003h	"GPIO Broadcast Data Mask bit Register (gpio_family_bw_mask_31_0)—Offset 1000h" on page 4921	00000000h
1004–1007h	"GPIO Broadcast Data Register (gpio_family_bw_data_31_0)—Offset 1004h" on page 4922	00000000h
1008–100Bh	"gpio_family_broadcast_reg_mask #0 (gpio_family_broadcast_reg_mask_0)—Offset 1008h" on page 4922	00000000h
1080–1083h	"RCOMP Control Register (ulphsmvfamily_2x4_rcomp_10_0_family_rcomp_control_reg)—Offset 1080h" on page 4925	00D41D1Dh
1084–1087h	"RCOMP Offset Register (ulphsmvfamily_2x4_rcomp_10_0_family_rcomp_offset_reg)—Offset 1084h" on page 4926	00000000h
1088–108Bh	"RCOMP Override Register (ulphsmvfamily_2x4_rcomp_10_0_family_rcomp_override_reg)—Offset 1088h" on page 4927	00FF4141h
108C–108Fh	"RCOMP Value Register (ulphsmvfamily_2x4_rcomp_10_0_family_rcomp_value_reg)—Offset 108Ch" on page 4928	00FF4141h

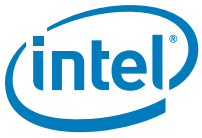


Table 10-100.Summary of GPIO North Message Bus Registers—0x13 (Continued)

Offset	Register Name (Register Symbol)	Default Value
1090–1093h	"family_config_rcomp_reg (ulphsmvfamily_2x4_rcomp_10_0_family_config_rcomp_reg)—Offset 1090h" on page 4929	414103FFh
1094–1097h	"gpio_family_configuration_register (ulphsmvfamily_2x4_rcomp_10_0_family_config_reg)—Offset 1094h" on page 4930	05C00000h
1110–1113h	"family_config_rcomp_reg (ulpmsmvfamily_2x4_13_0_family_config_rcomp_reg)—Offset 1110h" on page 4931	02020311h
1114–1117h	"gpio_family_configuration_register (ulpmsmvfamily_2x4_13_0_family_config_reg)—Offset 1114h" on page 4932	04C00000h
1190–1193h	"family_config_rcomp_reg (ulpmsmvfamily_3x4_12_0_family_config_rcomp_reg)—Offset 1190h" on page 4933	03030311h
1194–1197h	"gpio_family_configuration_register (ulpmsmvfamily_3x4_12_0_family_config_reg)—Offset 1194h" on page 4934	05C00000h
1210–1213h	"family_config_rcomp_reg (ulphsmvfamily_2x4_12_0_family_config_rcomp_reg)—Offset 1210h" on page 4935	414103FFh
1214–1217h	"gpio_family_configuration_register (ulphsmvfamily_2x4_12_0_family_config_reg)—Offset 1214h" on page 4936	05C00000h
1290–1293h	"family_config_rcomp_reg (ulpmsmvfamily_3x4_13_0_family_config_rcomp_reg)—Offset 1290h" on page 4937	02020311h
1294–1297h	"gpio_family_configuration_register (ulpmsmvfamily_3x4_13_0_family_config_reg)—Offset 1294h" on page 4938	05C00000h
4000–4003h	"GPIO Broadcast Data Mask bit Register (gpio_pad_bw_mask_31_0)—Offset 4000h" on page 4939	00000000h
4004–4007h	"GPIO Broadcast Data Register (gpio_pad_bw_data_31_0)—Offset 4004h" on page 4939	00000000h
4008–400Bh	"gpio_pad_broadcast_reg_mask #0 (gpio_pad_broadcast_reg_mask_0)—Offset 4008h" on page 4940	00000000h
400C–400Fh	"gpio_pad_broadcast_reg_mask #1 (gpio_pad_broadcast_reg_mask_1)—Offset 400Ch" on page 4942	00000000h
4010–4013h	"gpio_pad_broadcast_reg_mask #2 (gpio_pad_broadcast_reg_mask_2)—Offset 4010h" on page 4944	00000000h
4014–4017h	"gpio_pad_broadcast_reg_mask #3 (gpio_pad_broadcast_reg_mask_3)—Offset 4014h" on page 4946	00000000h
4400–4403h	"Pad Control Register 0 (GPIO_DFX0_PAD_CFG0)—Offset 4400h" on page 4948	00110300h
4404–4407h	"Pad Control Register 1 (GPIO_DFX0_PAD_CFG1)—Offset 4404h" on page 4949	05C00000h
4408–440Bh	"Pad Control Register 0 (GPIO_DFX3_PAD_CFG0)—Offset 4408h" on page 4951	00110300h
440C–440Fh	"Pad Control Register 1 (GPIO_DFX3_PAD_CFG1)—Offset 440Ch" on page 4953	05C00000h
4410–4413h	"Pad Control Register 0 (GPIO_DFX7_PAD_CFG0)—Offset 4410h" on page 4955	00910300h
4414–4417h	"Pad Control Register 1 (GPIO_DFX7_PAD_CFG1)—Offset 4414h" on page 4956	05C00000h
4418–441Bh	"Pad Control Register 0 (GPIO_DFX1_PAD_CFG0)—Offset 4418h" on page 4958	00110300h
441C–441Fh	"Pad Control Register 1 (GPIO_DFX1_PAD_CFG1)—Offset 441Ch" on page 4959	05C00000h

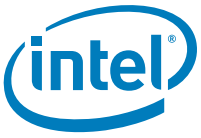


Table 10-100.Summary of GPIO North Message Bus Registers—0x13 (Continued)

Offset	Register Name (Register Symbol)	Default Value
4420–4423h	"Pad Control Register 0 (GPIO_DFX5_PAD_CFG0)—Offset 4420h" on page 4961	00910300h
4424–4427h	"Pad Control Register 1 (GPIO_DFX5_PAD_CFG1)—Offset 4424h" on page 4963	05C00000h
4428–442Bh	"Pad Control Register 0 (GPIO_DFX4_PAD_CFG0)—Offset 4428h" on page 4965	00110300h
442C–442Fh	"Pad Control Register 1 (GPIO_DFX4_PAD_CFG1)—Offset 442Ch" on page 4966	05C00000h
4430–4433h	"Pad Control Register 0 (GPIO_DFX8_PAD_CFG0)—Offset 4430h" on page 4968	00910300h
4434–4437h	"Pad Control Register 1 (GPIO_DFX8_PAD_CFG1)—Offset 4434h" on page 4969	05C00000h
4438–443Bh	"Pad Control Register 0 (GPIO_DFX2_PAD_CFG0)—Offset 4438h" on page 4971	00110300h
443C–443Fh	"Pad Control Register 1 (GPIO_DFX2_PAD_CFG1)—Offset 443Ch" on page 4973	05C00000h
4440–4443h	"Pad Control Register 0 (GPIO_DFX6_PAD_CFG0)—Offset 4440h" on page 4975	00910300h
4444–4447h	"Pad Control Register 1 (GPIO_DFX6_PAD_CFG1)—Offset 4444h" on page 4976	05C00000h
4800–4803h	"Pad Control Register 0 (GPIO_SUS0_PAD_CFG0)—Offset 4800h" on page 4978	00118200h
4804–4807h	"Pad Control Register 1 (GPIO_SUS0_PAD_CFG1)—Offset 4804h" on page 4979	05C00000h
4808–480Bh	"Pad Control Register 0 (SEC_GPIO_SUS10_PAD_CFG0)—Offset 4808h" on page 4981	00118200h
480C–480Fh	"Pad Control Register 1 (SEC_GPIO_SUS10_PAD_CFG1)—Offset 480Ch" on page 4983	05C00000h
4810–4813h	"Pad Control Register 0 (GPIO_SUS3_PAD_CFG0)—Offset 4810h" on page 4985	00110300h
4814–4817h	"Pad Control Register 1 (GPIO_SUS3_PAD_CFG1)—Offset 4814h" on page 4986	05C00000h
4818–481Bh	"Pad Control Register 0 (GPIO_SUS7_PAD_CFG0)—Offset 4818h" on page 4988	00918200h
481C–481Fh	"Pad Control Register 1 (GPIO_SUS7_PAD_CFG1)—Offset 481Ch" on page 4989	05C00000h
4820–4823h	"Pad Control Register 0 (GPIO_SUS1_PAD_CFG0)—Offset 4820h" on page 4991	00110300h
4824–4827h	"Pad Control Register 1 (GPIO_SUS1_PAD_CFG1)—Offset 4824h" on page 4993	05C00000h
4828–482Bh	"Pad Control Register 0 (GPIO_SUS5_PAD_CFG0)—Offset 4828h" on page 4995	00918200h
482C–482Fh	"Pad Control Register 1 (GPIO_SUS5_PAD_CFG1)—Offset 482Ch" on page 4996	05C00000h
4830–4833h	"Pad Control Register 0 (SEC_GPIO_SUS11_PAD_CFG0)—Offset 4830h" on page 4998	00110300h
4834–4837h	"Pad Control Register 1 (SEC_GPIO_SUS11_PAD_CFG1)—Offset 4834h" on page 4999	05C00000h

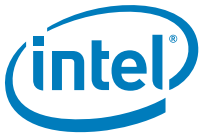


Table 10-100.Summary of GPIO North Message Bus Registers—0x13 (Continued)

Offset	Register Name (Register Symbol)	Default Value
4838–483Bh	"Pad Control Register 0 (GPIO_SUS4_PAD_CFG0)—Offset 4838h" on page 5001	00910300h
483C–483Fh	"Pad Control Register 1 (GPIO_SUS4_PAD_CFG1)—Offset 483Ch" on page 5003	05C00000h
4840–4843h	"Pad Control Register 0 (SEC_GPIO_SUS8_PAD_CFG0)—Offset 4840h" on page 5005	00910300h
4844–4847h	"Pad Control Register 1 (SEC_GPIO_SUS8_PAD_CFG1)—Offset 4844h" on page 5006	05C00000h
4848–484Bh	"Pad Control Register 0 (GPIO_SUS2_PAD_CFG0)—Offset 4848h" on page 5008	00910300h
484C–484Fh	"Pad Control Register 1 (GPIO_SUS2_PAD_CFG1)—Offset 484Ch" on page 5009	05C00000h
4850–4853h	"Pad Control Register 0 (GPIO_SUS6_PAD_CFG0)—Offset 4850h" on page 5011	00918200h
4854–4857h	"Pad Control Register 1 (GPIO_SUS6_PAD_CFG1)—Offset 4854h" on page 5013	05C00000h
4858–485Bh	"Pad Control Register 0 (CX_PREQ_B_PAD_CFG0)—Offset 4858h" on page 5015	00A10300h
485C–485Fh	"Pad Control Register 1 (CX_PREQ_B_PAD_CFG1)—Offset 485Ch" on page 5016	05C00000h
4860–4863h	"Pad Control Register 0 (SEC_GPIO_SUS9_PAD_CFG0)—Offset 4860h" on page 5018	00118200h
4864–4867h	"Pad Control Register 1 (SEC_GPIO_SUS9_PAD_CFG1)—Offset 4864h" on page 5019	05C00000h
4C00–4C03h	"Pad Control Register 0 (TRST_B_PAD_CFG0)—Offset 4C00h" on page 5021	00A10300h
4C04–4C07h	"Pad Control Register 1 (TRST_B_PAD_CFG1)—Offset 4C04h" on page 5023	05C00000h
4C08–4C0Bh	"Pad Control Register 0 (TCK_PAD_CFG0)—Offset 4C08h" on page 5025	00210300h
4C0C–4C0Fh	"Pad Control Register 1 (TCK_PAD_CFG1)—Offset 4C0Ch" on page 5026	05C00000h
4C10–4C13h	"Pad Control Register 0 (PROCHOT_B_PAD_CFG0)—Offset 4C10h" on page 5028	00010300h
4C14–4C17h	"Pad Control Register 1 (PROCHOT_B_PAD_CFG1)—Offset 4C14h" on page 5029	05C00060h
4C18–4C1Bh	"Pad Control Register 0 (SVID0_DATA_PAD_CFG0)—Offset 4C18h" on page 5031	00000300h
4C1C–4C1Fh	"Pad Control Register 1 (SVID0_DATA_PAD_CFG1)—Offset 4C1Ch" on page 5033	05C00020h
4C20–4C23h	"Pad Control Register 0 (TMS_PAD_CFG0)—Offset 4C20h" on page 5035	00A10300h
4C24–4C27h	"Pad Control Register 1 (TMS_PAD_CFG1)—Offset 4C24h" on page 5036	05C00000h
4C28–4C2Bh	"Pad Control Register 0 (CX_PRDY_B_2_PAD_CFG0)—Offset 4C28h" on page 5038	00A10300h
4C2C–4C2Fh	"Pad Control Register 1 (CX_PRDY_B_2_PAD_CFG1)—Offset 4C2Ch" on page 5039	05C00000h

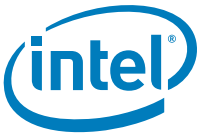


Table 10-100.Summary of GPIO North Message Bus Registers—0x13 (Continued)

Offset	Register Name (Register Symbol)	Default Value
4C30–4C33h	"Pad Control Register 0 (TDO_2_PAD_CFG0)—Offset 4C30h" on page 5041	00010300h
4C34–4C37h	"Pad Control Register 1 (TDO_2_PAD_CFG1)—Offset 4C34h" on page 5043	05C00000h
4C38–4C3Bh	"Pad Control Register 0 (CX_PRDY_B_PAD_CFG0)—Offset 4C38h" on page 5045	00A10300h
4C3C–4C3Fh	"Pad Control Register 1 (CX_PRDY_B_PAD_CFG1)—Offset 4C3Ch" on page 5046	05C00000h
4C40–4C43h	"Pad Control Register 0 (SVID0_ALERT_B_PAD_CFG0)—Offset 4C40h" on page 5048	00010300h
4C44–4C47h	"Pad Control Register 1 (SVID0_ALERT_B_PAD_CFG1)—Offset 4C44h" on page 5049	05C00040h
4C48–4C4Bh	"Pad Control Register 0 (TDO_PAD_CFG0)—Offset 4C48h" on page 5051	00010300h
4C4C–4C4Fh	"Pad Control Register 1 (TDO_PAD_CFG1)—Offset 4C4Ch" on page 5053	05C00000h
4C50–4C53h	"Pad Control Register 0 (SVID0_CLK_PAD_CFG0)—Offset 4C50h" on page 5055	00010300h
4C54–4C57h	"Pad Control Register 1 (SVID0_CLK_PAD_CFG1)—Offset 4C54h" on page 5056	05C00000h
4C58–4C5Bh	"Pad Control Register 0 (TDI_PAD_CFG0)—Offset 4C58h" on page 5058	00A10300h
4C5C–4C5Fh	"Pad Control Register 1 (TDI_PAD_CFG1)—Offset 4C5Ch" on page 5059	05C00000h
5000–5003h	"Pad Control Register 0 (GP_CAMERASB05_PAD_CFG0)—Offset 5000h" on page 5061	00110300h
5004–5007h	"Pad Control Register 1 (GP_CAMERASB05_PAD_CFG1)—Offset 5004h" on page 5063	05C00020h
5008–500Bh	"Pad Control Register 0 (GP_CAMERASB02_PAD_CFG0)—Offset 5008h" on page 5065	00110300h
500C–500Fh	"Pad Control Register 1 (GP_CAMERASB02_PAD_CFG1)—Offset 500Ch" on page 5066	05C00020h
5010–5013h	"Pad Control Register 0 (GP_CAMERASB08_PAD_CFG0)—Offset 5010h" on page 5068	00110300h
5014–5017h	"Pad Control Register 1 (GP_CAMERASB08_PAD_CFG1)—Offset 5014h" on page 5069	05C00020h
5018–501Bh	"Pad Control Register 0 (GP_CAMERASB00_PAD_CFG0)—Offset 5018h" on page 5071	00110300h
501C–501Fh	"Pad Control Register 1 (GP_CAMERASB00_PAD_CFG1)—Offset 501Ch" on page 5073	05C00020h
5020–5023h	"Pad Control Register 0 (GP_CAMERASB06_PAD_CFG0)—Offset 5020h" on page 5075	00110300h
5024–5027h	"Pad Control Register 1 (GP_CAMERASB06_PAD_CFG1)—Offset 5024h" on page 5076	05C00020h
5028–502Bh	"Pad Control Register 0 (GP_CAMERASB10_PAD_CFG0)—Offset 5028h" on page 5078	00130300h
502C–502Fh	"Pad Control Register 1 (GP_CAMERASB10_PAD_CFG1)—Offset 502Ch" on page 5079	05C00000h

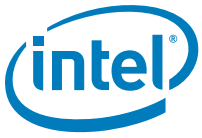


Table 10-100.Summary of GPIO North Message Bus Registers—0x13 (Continued)

Offset	Register Name (Register Symbol)	Default Value
5030–5033h	"Pad Control Register 0 (GP_CAMERASB03_PAD_CFG0)—Offset 5030h" on page 5081	00110300h
5034–5037h	"Pad Control Register 1 (GP_CAMERASB03_PAD_CFG1)—Offset 5034h" on page 5083	05C00020h
5038–503Bh	"Pad Control Register 0 (GP_CAMERASB09_PAD_CFG0)—Offset 5038h" on page 5085	00110300h
503C–503Fh	"Pad Control Register 1 (GP_CAMERASB09_PAD_CFG1)—Offset 503Ch" on page 5086	05C00020h
5040–5043h	"Pad Control Register 0 (GP_CAMERASB01_PAD_CFG0)—Offset 5040h" on page 5088	00110300h
5044–5047h	"Pad Control Register 1 (GP_CAMERASB01_PAD_CFG1)—Offset 5044h" on page 5089	05C00020h
5048–504Bh	"Pad Control Register 0 (GP_CAMERASB07_PAD_CFG0)—Offset 5048h" on page 5091	00110300h
504C–504Fh	"Pad Control Register 1 (GP_CAMERASB07_PAD_CFG1)—Offset 504Ch" on page 5093	05C00020h
5050–5053h	"Pad Control Register 0 (GP_CAMERASB11_PAD_CFG0)—Offset 5050h" on page 5095	00110300h
5054–5057h	"Pad Control Register 1 (GP_CAMERASB11_PAD_CFG1)—Offset 5054h" on page 5096	05C00020h
5058–505Bh	"Pad Control Register 0 (GP_CAMERASB04_PAD_CFG0)—Offset 5058h" on page 5098	00110300h
505C–505Fh	"Pad Control Register 1 (GP_CAMERASB04_PAD_CFG1)—Offset 505Ch" on page 5099	05C00020h
5400–5403h	"Pad Control Register 0 (PANEL0_BKLTEN_PAD_CFG0)—Offset 5400h" on page 5101	00010300h
5404–5407h	"Pad Control Register 1 (PANEL0_BKLTEN_PAD_CFG1)—Offset 5404h" on page 5103	05C00000h
5408–540Bh	"Pad Control Register 0 (HV_DDI0_HPD_PAD_CFG0)—Offset 5408h" on page 5105	00110300h
540C–540Fh	"Pad Control Register 1 (HV_DDI0_HPD_PAD_CFG1)—Offset 540Ch" on page 5106	05C00020h
5410–5413h	"Pad Control Register 0 (HV_DDI2_DDC_SDA_PAD_CFG0)—Offset 5410h" on page 5108	00910300h
5414–5417h	"Pad Control Register 1 (HV_DDI2_DDC_SDA_PAD_CFG1)—Offset 5414h" on page 5109	05C00000h
5418–541Bh	"Pad Control Register 0 (PANEL1_BKLTCTL_PAD_CFG0)—Offset 5418h" on page 5111	00010300h
541C–541Fh	"Pad Control Register 1 (PANEL1_BKLTCTL_PAD_CFG1)—Offset 541Ch" on page 5113	05C00000h
5420–5423h	"Pad Control Register 0 (HV_DDI1_HPD_PAD_CFG0)—Offset 5420h" on page 5115	00110300h
5424–5427h	"Pad Control Register 1 (HV_DDI1_HPD_PAD_CFG1)—Offset 5424h" on page 5116	05C00020h
5428–542Bh	"Pad Control Register 0 (PANEL0_BKLTCTL_PAD_CFG0)—Offset 5428h" on page 5118	00010300h
542C–542Fh	"Pad Control Register 1 (PANEL0_BKLTCTL_PAD_CFG1)—Offset 542Ch" on page 5119	05C00000h

Table 10-100.Summary of GPIO North Message Bus Registers—0x13 (Continued)

Offset	Register Name (Register Symbol)	Default Value
5430–5433h	"Pad Control Register 0 (HV_DDI0_DDC_SDA_PAD_CFG0)—Offset 5430h" on page 5121	00910300h
5434–5437h	"Pad Control Register 1 (HV_DDI0_DDC_SDA_PAD_CFG1)—Offset 5434h" on page 5123	05C00000h
5438–543Bh	"Pad Control Register 0 (HV_DDI2_DDC_SCL_PAD_CFG0)—Offset 5438h" on page 5125	00910300h
543C–543Fh	"Pad Control Register 1 (HV_DDI2_DDC_SCL_PAD_CFG1)—Offset 543Ch" on page 5126	05C00000h
5440–5443h	"Pad Control Register 0 (HV_DDI2_HPD_PAD_CFG0)—Offset 5440h" on page 5128	00110300h
5444–5447h	"Pad Control Register 1 (HV_DDI2_HPD_PAD_CFG1)—Offset 5444h" on page 5129	05C00020h
5448–544Bh	"Pad Control Register 0 (PANEL1_VDDEN_PAD_CFG0)—Offset 5448h" on page 5131	00010300h
544C–544Fh	"Pad Control Register 1 (PANEL1_VDDEN_PAD_CFG1)—Offset 544Ch" on page 5133	05C00000h
5450–5453h	"Pad Control Register 0 (PANEL1_BKLTEN_PAD_CFG0)—Offset 5450h" on page 5135	00010300h
5454–5457h	"Pad Control Register 1 (PANEL1_BKLTEN_PAD_CFG1)—Offset 5454h" on page 5136	05C00000h
5458–545Bh	"Pad Control Register 0 (HV_DDI0_DDC_SCL_PAD_CFG0)—Offset 5458h" on page 5138	00910300h
545C–545Fh	"Pad Control Register 1 (HV_DDI0_DDC_SCL_PAD_CFG1)—Offset 545Ch" on page 5139	05C00000h
5460–5463h	"Pad Control Register 0 (PANEL0_VDDEN_PAD_CFG0)—Offset 5460h" on page 5141	00010300h
5464–5467h	"Pad Control Register 1 (PANEL0_VDDEN_PAD_CFG1)—Offset 5464h" on page 5143	05C00000h

10.5.1 GPIO Read Access Control (gpio_read_access_policy_access_reg)—Offset 0h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

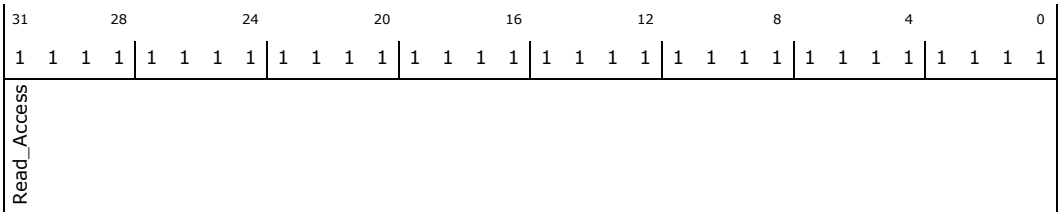
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 0h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.5.2 GPIO Read Access Control (gpio_read_access_policy_wake_reg)—Offset 4h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

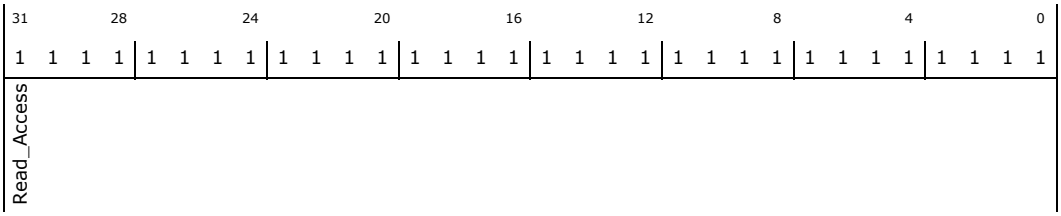
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.5.3 GPIO Read Access Control (gpio_read_access_policy_interrupt_reg)—Offset 8h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

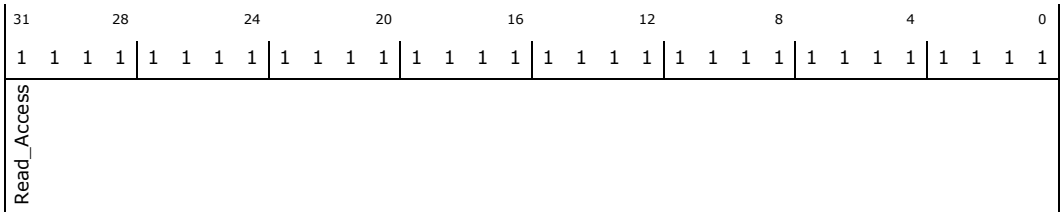
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 8h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.5.4 GPIO Read Access Control (gpio_read_access_policy_community_reg)—Offset Ch

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

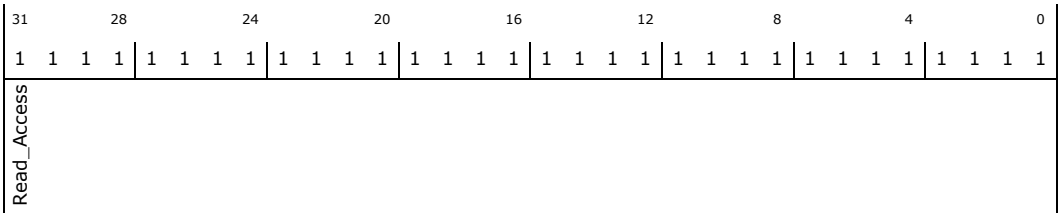
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.5.5 GPIO Read Access Control (gpio_read_access_policy_family_broadcast_reg)—Offset 10h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

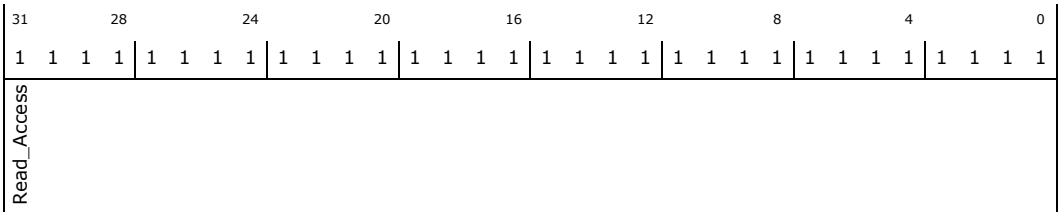
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 10h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.5.6 GPIO Read Access Control (gpio_read_access_policy_family_reg)—Offset 14h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

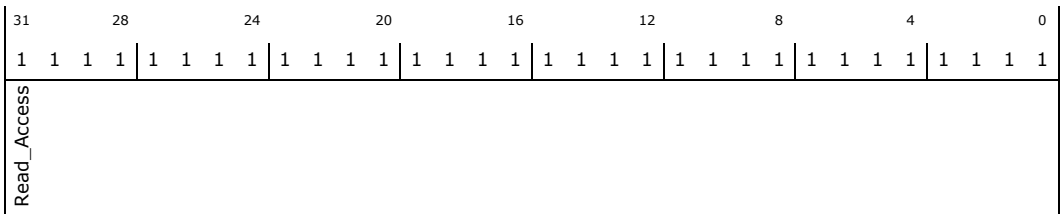
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 14h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.5.7 GPIO Read Access Control (gpio_read_access_policy_pad_broadcast_reg)—Offset 18h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

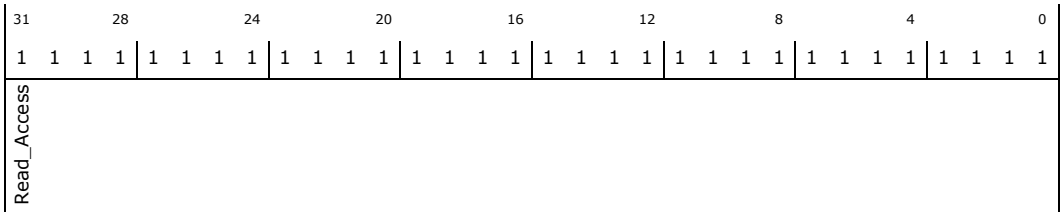
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 18h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.5.8 GPIO Read Access Control (gpio_read_access_policy_ulphsmvfamily_2x4_rcomp_10_0_regs)—Offset 1Ch

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

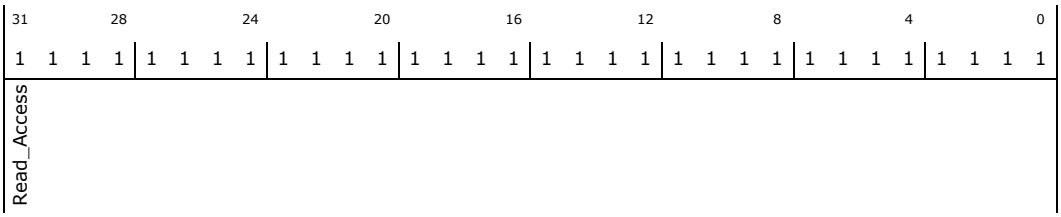
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 1Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.5.9 GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_2x4_13_0_regs)—Offset 20h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

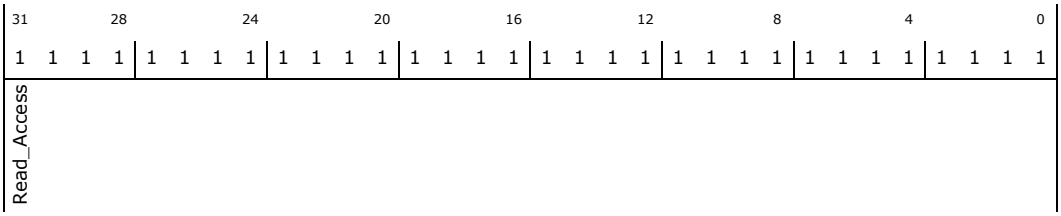
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 20h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.5.10 GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_3x4_12_0_regs)—Offset 24h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

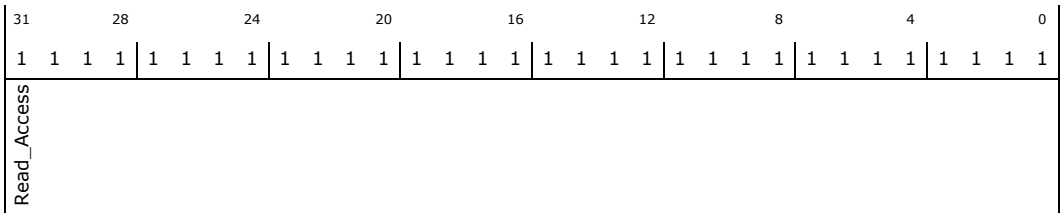
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 24h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.5.11 GPIO Read Access Control (gpio_read_access_policy_ulphsmvfamily_2x4_12_0_regs)—Offset 28h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

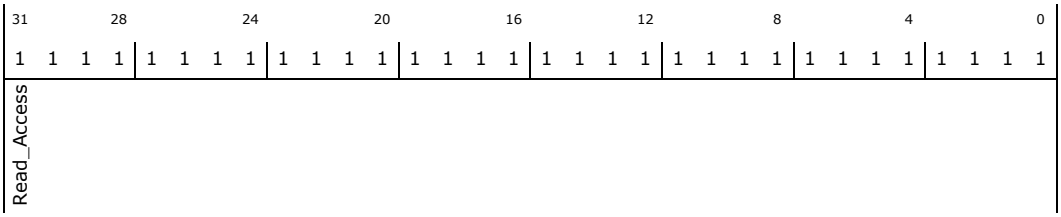
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 28h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.5.12 GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_3x4_13_0_regs)—Offset 2Ch

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

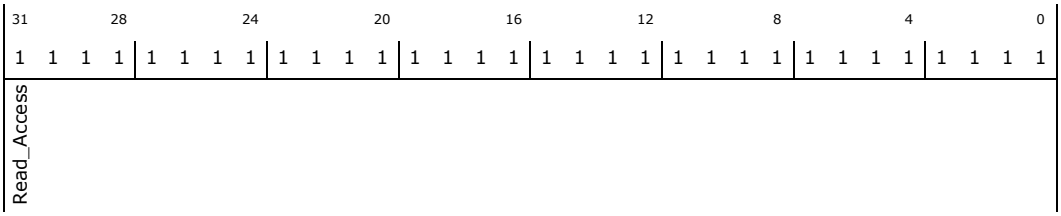
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 2Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.5.13 GPIO Write Access Control (gpio_write_access_policy_access_reg)—Offset 100h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

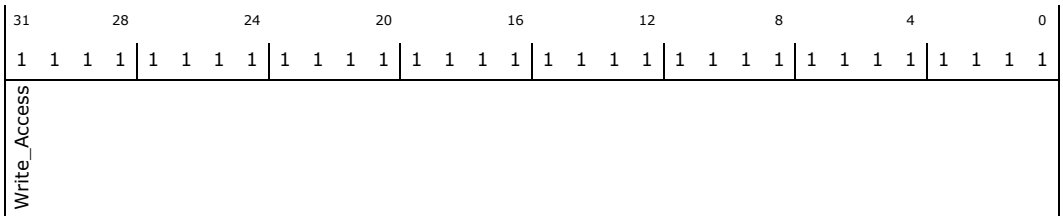
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 100h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.5.14 GPIO Write Access Control (gpio_write_access_policy_wake_reg)—Offset 104h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

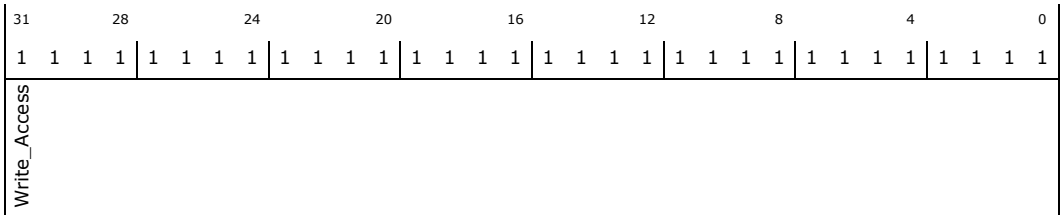
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 104h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.5.15 GPIO Write Access Control (gpio_write_access_policy_interrupt_reg)—Offset 108h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

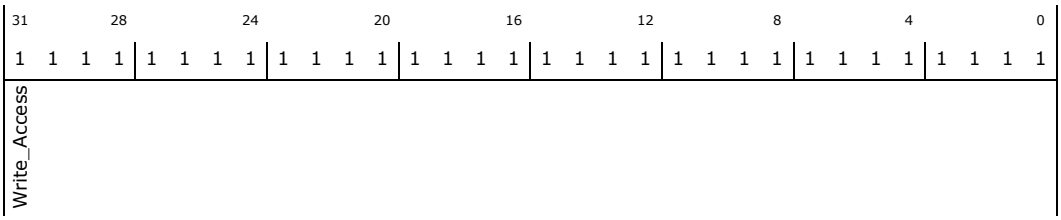
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 108h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.5.16 GPIO Write Access Control (gpio_write_access_policy_community_reg)—Offset 10Ch

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

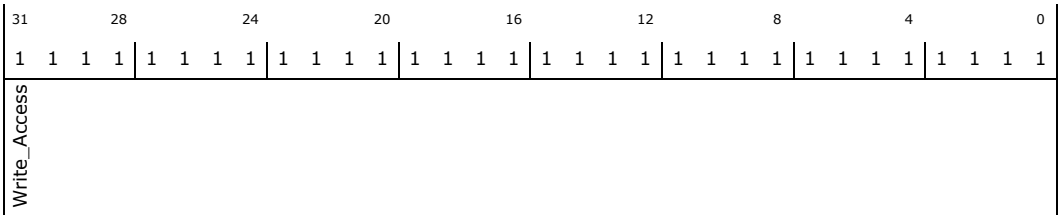
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 10Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.5.17 GPIO Write Access Control (gpio_write_access_policy_family_broadcast_reg)—Offset 110h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

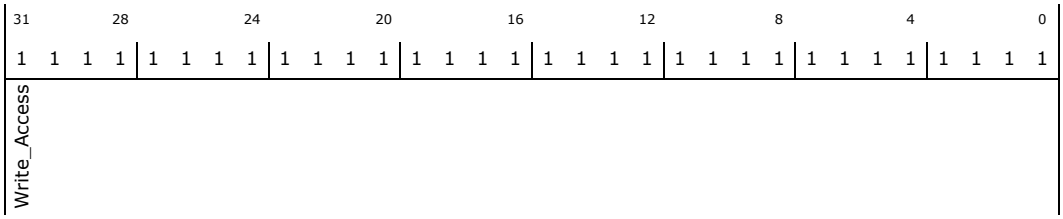
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 110h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.5.18 GPIO Write Access Control (gpio_write_access_policy_family_reg)—Offset 114h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

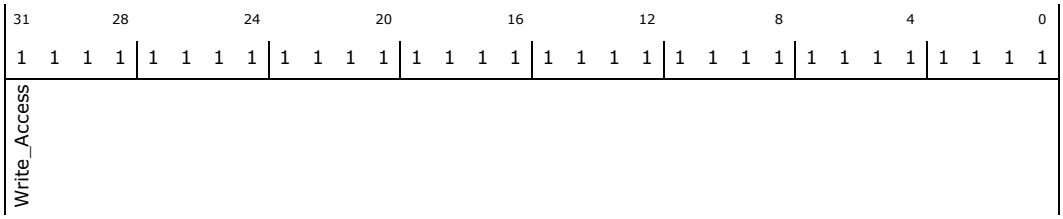
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 114h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.5.19 GPIO Write Access Control (gpio_write_access_policy_pad_broadcast_reg)—Offset 118h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

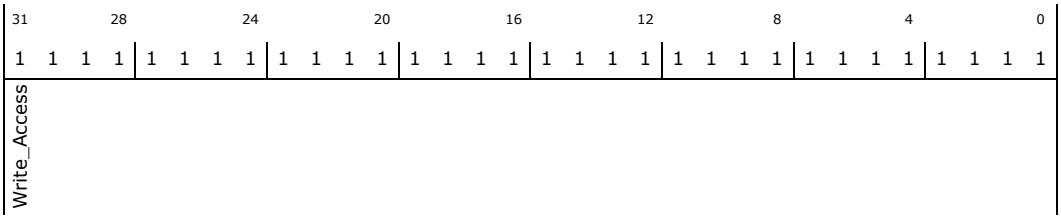
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 118h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.5.20 GPIO Write Access Control (gpio_write_access_policy_ulphsmvfamily_2x4_rcomp_10_0_regs)—Offset 11Ch

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

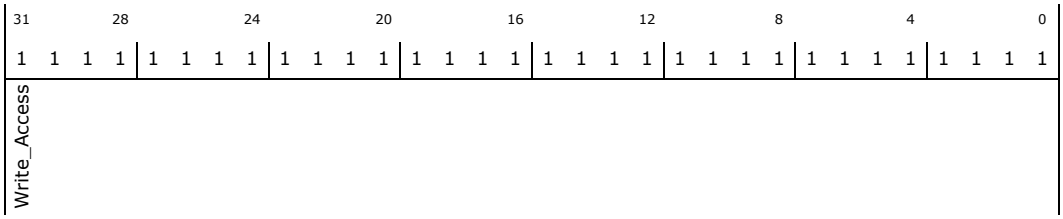
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 11Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.5.21 GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_2x4_13_0_regs)—Offset 120h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

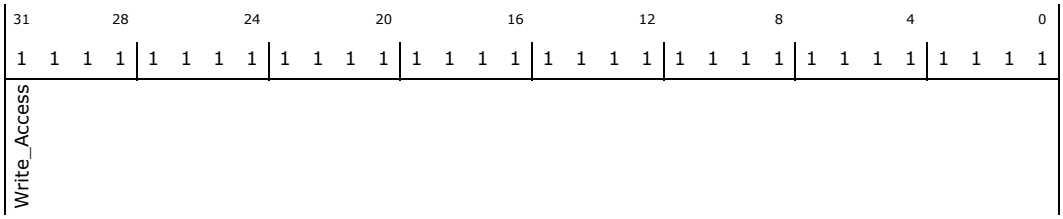
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 120h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.5.22 GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_3x4_12_0_regs)—Offset 124h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

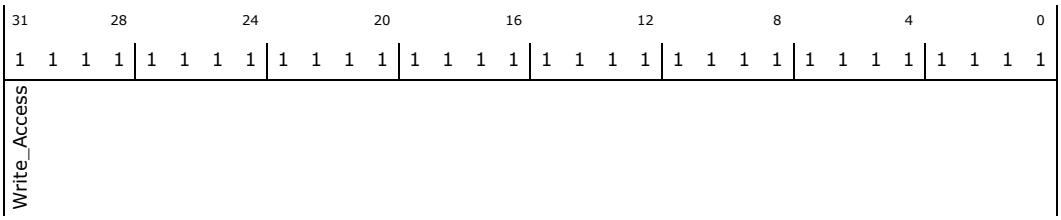
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 124h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.5.23 GPIO Write Access Control (gpio_write_access_policy_ulphsmvfamily_2x4_12_0_regs)—Offset 128h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

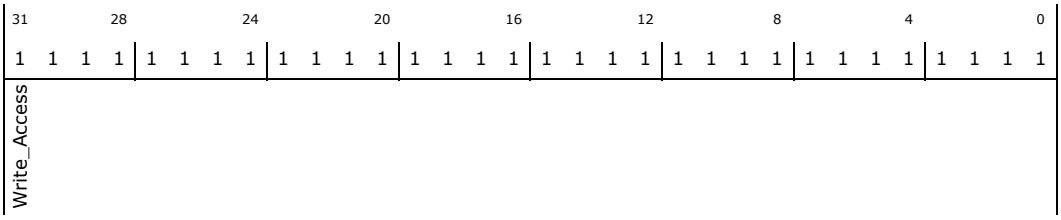
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 128h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.5.24 GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_3x4_13_0_regs)—Offset 12Ch

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

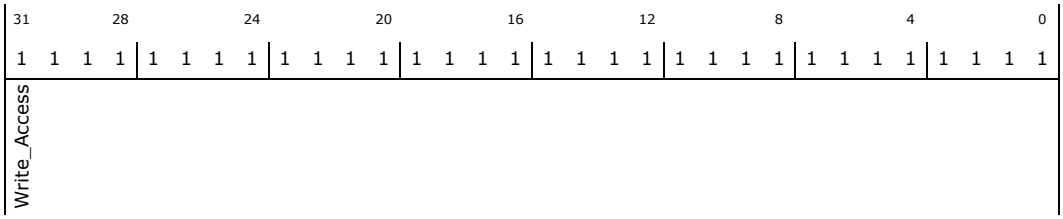
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 12Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.5.25 GPIO_WAKE_STATUS_REG #0 (gpio_wake_status_reg_0)—Offset 200h

GPIO Wake Status Register write 1 to clear.

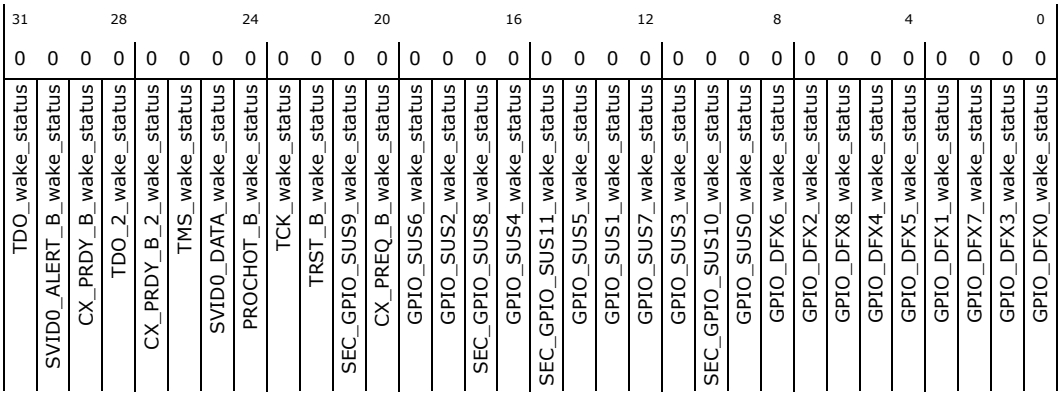
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 200h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1C	**TDO_wake_status:** Reserved.
30	0x0 RW/1C	**SVID0_ALERT_B_wake_status:** Reserved.
29	0x0 RW/1C	**CX_PRDY_B_wake_status:** Reserved.
28	0x0 RW/1C	**TDO_2_wake_status:** Reserved.
27	0x0 RW/1C	**CX_PRDY_B_2_wake_status:** Reserved.
26	0x0 RW/1C	**TMS_wake_status:** Reserved.
25	0x0 RW/1C	**SVID0_DATA_wake_status:** Reserved.
24	0x0 RW/1C	**PROCHOT_B_wake_status:** Reserved.
23	0x0 RW/1C	**TCK_wake_status:** Reserved.
22	0x0 RW/1C	**TRST_B_wake_status:** Reserved.
21	0x0 RW/1C	**SEC_GPIO_SUS9_wake_status:** Reserved.
20	0x0 RW/1C	**CX_PREQ_B_wake_status:** Reserved.
19	0x0 RW/1C	**GPIO_SUS6_wake_status:** Reserved.
18	0x0 RW/1C	**GPIO_SUS2_wake_status:** Reserved.
17	0x0 RW/1C	**SEC_GPIO_SUS8_wake_status:** Reserved.
16	0x0 RW/1C	**GPIO_SUS4_wake_status:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
15	0x0 RW/1C	**SEC_GPIO_SUS11_wake_status:** Reserved.
14	0x0 RW/1C	**GPIO_SUS5_wake_status:** Reserved.
13	0x0 RW/1C	**GPIO_SUS1_wake_status:** Reserved.
12	0x0 RW/1C	**GPIO_SUS7_wake_status:** Reserved.
11	0x0 RW/1C	**GPIO_SUS3_wake_status:** Reserved.
10	0x0 RW/1C	**SEC_GPIO_SUS10_wake_status:** Reserved.
9	0x0 RW/1C	**GPIO_SUS0_wake_status:** Reserved.
8	0x0 RW/1C	**GPIO_DFX6_wake_status:** Reserved.
7	0x0 RW/1C	**GPIO_DFX2_wake_status:** Reserved.
6	0x0 RW/1C	**GPIO_DFX8_wake_status:** Reserved.
5	0x0 RW/1C	**GPIO_DFX4_wake_status:** Reserved.
4	0x0 RW/1C	**GPIO_DFX5_wake_status:** Reserved.
3	0x0 RW/1C	**GPIO_DFX1_wake_status:** Reserved.
2	0x0 RW/1C	**GPIO_DFX7_wake_status:** Reserved.
1	0x0 RW/1C	**GPIO_DFX3_wake_status:** Reserved.
0	0x0 RW/1C	**GPIO_DFX0_wake_status:** Reserved.

10.5.26 GPIO_WAKE_STATUS_REG #1 (gpio_wake_status_reg_1)—Offset 204h

GPIO Wake Status Register write 1 to clear.

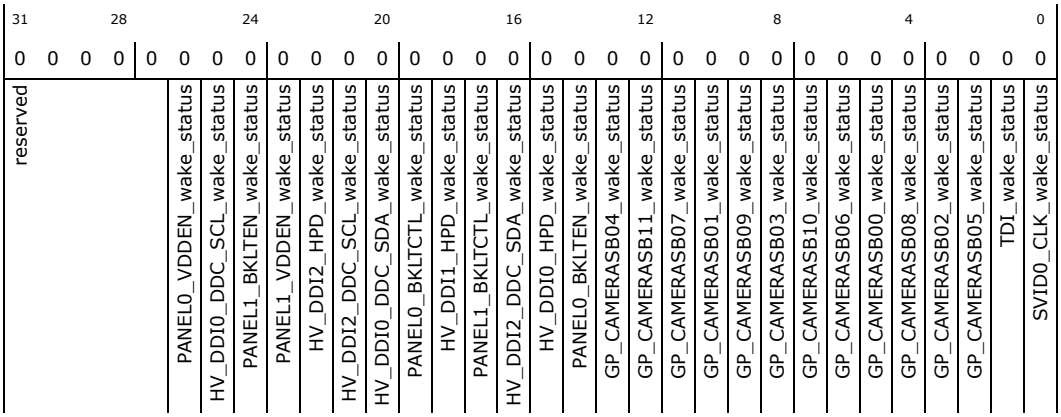
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 204h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:27	0x0 RW/1C	**reserved:** Reserved.
26	0x0 RW/1C	**PANEL0_VDDEN_wake_status:** Reserved.
25	0x0 RW/1C	**HV_DDI0_DDC_SCL_wake_status:** Reserved.
24	0x0 RW/1C	**PANEL1_BKLTEN_wake_status:** Reserved.
23	0x0 RW/1C	**PANEL1_VDDEN_wake_status:** Reserved.
22	0x0 RW/1C	**HV_DDI2_HPD_wake_status:** Reserved.
21	0x0 RW/1C	**HV_DDI2_DDC_SCL_wake_status:** Reserved.
20	0x0 RW/1C	**HV_DDI0_DDC_SDA_wake_status:** Reserved.
19	0x0 RW/1C	**PANEL0_BKLTCTL_wake_status:** Reserved.
18	0x0 RW/1C	**HV_DDI1_HPD_wake_status:** Reserved.
17	0x0 RW/1C	**PANEL1_BKLTCTL_wake_status:** Reserved.
16	0x0 RW/1C	**HV_DDI2_DDC_SDA_wake_status:** Reserved.
15	0x0 RW/1C	**HV_DDI0_HPD_wake_status:** Reserved.
14	0x0 RW/1C	**PANEL0_BKLTEN_wake_status:** Reserved.
13	0x0 RW/1C	**GP_CAMERASB04_wake_status:** Reserved.
12	0x0 RW/1C	**GP_CAMERASB11_wake_status:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
11	0x0 RW/1C	**GP_CAMERASB07_wake_status:** Reserved.
10	0x0 RW/1C	**GP_CAMERASB01_wake_status:** Reserved.
9	0x0 RW/1C	**GP_CAMERASB09_wake_status:** Reserved.
8	0x0 RW/1C	**GP_CAMERASB03_wake_status:** Reserved.
7	0x0 RW/1C	**GP_CAMERASB10_wake_status:** Reserved.
6	0x0 RW/1C	**GP_CAMERASB06_wake_status:** Reserved.
5	0x0 RW/1C	**GP_CAMERASB00_wake_status:** Reserved.
4	0x0 RW/1C	**GP_CAMERASB08_wake_status:** Reserved.
3	0x0 RW/1C	**GP_CAMERASB02_wake_status:** Reserved.
2	0x0 RW/1C	**GP_CAMERASB05_wake_status:** Reserved.
1	0x0 RW/1C	**TDI_wake_status:** Reserved.
0	0x0 RW/1C	**SVID0_CLK_wake_status:** Reserved.

10.5.27 GPIO_WAKE_MASK_REG #0 (gpio_wake_mask_reg_0)—Offset 280h

GPIO Wake Register 0 Masks Wake.

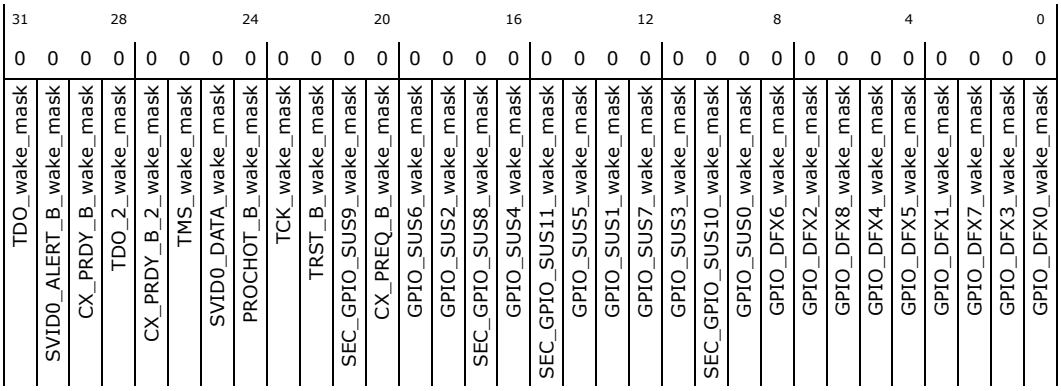
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 280h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**TDO_wake_mask:** Reserved.
30	0x0 RW	**SVID0_ALERT_B_wake_mask:** Reserved.
29	0x0 RW	**CX_PRDY_B_wake_mask:** Reserved.
28	0x0 RW	**TDO_2_wake_mask:** Reserved.
27	0x0 RW	**CX_PRDY_B_2_wake_mask:** Reserved.
26	0x0 RW	**TMS_wake_mask:** Reserved.
25	0x0 RW	**SVID0_DATA_wake_mask:** Reserved.
24	0x0 RW	**PROCHOT_B_wake_mask:** Reserved.
23	0x0 RW	**TCK_wake_mask:** Reserved.
22	0x0 RW	**TRST_B_wake_mask:** Reserved.
21	0x0 RW	**SEC_GPIO_SUS9_wake_mask:** Reserved.
20	0x0 RW	**CX_PREQ_B_wake_mask:** Reserved.
19	0x0 RW	**GPIO_SUS6_wake_mask:** Reserved.
18	0x0 RW	**GPIO_SUS2_wake_mask:** Reserved.
17	0x0 RW	**SEC_GPIO_SUS8_wake_mask:** Reserved.
16	0x0 RW	**GPIO_SUS4_wake_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
15	0x0 RW	**SEC_GPIO_SUS11_wake_mask:** Reserved.
14	0x0 RW	**GPIO_SUS5_wake_mask:** Reserved.
13	0x0 RW	**GPIO_SUS1_wake_mask:** Reserved.
12	0x0 RW	**GPIO_SUS7_wake_mask:** Reserved.
11	0x0 RW	**GPIO_SUS3_wake_mask:** Reserved.
10	0x0 RW	**SEC_GPIO_SUS10_wake_mask:** Reserved.
9	0x0 RW	**GPIO_SUS0_wake_mask:** Reserved.
8	0x0 RW	**GPIO_DFX6_wake_mask:** Reserved.
7	0x0 RW	**GPIO_DFX2_wake_mask:** Reserved.
6	0x0 RW	**GPIO_DFX8_wake_mask:** Reserved.
5	0x0 RW	**GPIO_DFX4_wake_mask:** Reserved.
4	0x0 RW	**GPIO_DFX5_wake_mask:** Reserved.
3	0x0 RW	**GPIO_DFX1_wake_mask:** Reserved.
2	0x0 RW	**GPIO_DFX7_wake_mask:** Reserved.
1	0x0 RW	**GPIO_DFX3_wake_mask:** Reserved.
0	0x0 RW	**GPIO_DFX0_wake_mask:** Reserved.

10.5.28 GPIO_WAKE_MASK_REG #1 (gpio_wake_mask_reg_1)—Offset 284h

GPIO Wake Register 0 Masks Wake.

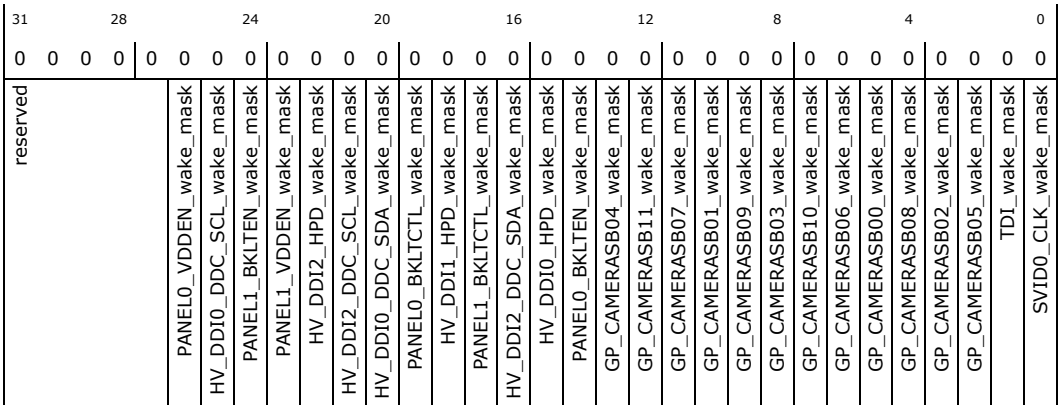
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 284h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:27	0x0 RW	**reserved:** Reserved.
26	0x0 RW	**PANEL0_VDDEN_wake_mask:** Reserved.
25	0x0 RW	**HV_DDI0_DDC_SCL_wake_mask:** Reserved.
24	0x0 RW	**PANEL1_BKLTEN_wake_mask:** Reserved.
23	0x0 RW	**PANEL1_VDDEN_wake_mask:** Reserved.
22	0x0 RW	**HV_DDI2_HPD_wake_mask:** Reserved.
21	0x0 RW	**HV_DDI2_DDC_SCL_wake_mask:** Reserved.
20	0x0 RW	**HV_DDI0_DDC_SDA_wake_mask:** Reserved.
19	0x0 RW	**PANEL0_BKLTCTL_wake_mask:** Reserved.
18	0x0 RW	**HV_DDI1_HPD_wake_mask:** Reserved.
17	0x0 RW	**PANEL1_BKLTCTL_wake_mask:** Reserved.
16	0x0 RW	**HV_DDI2_DDC_SDA_wake_mask:** Reserved.
15	0x0 RW	**HV_DDI0_HPD_wake_mask:** Reserved.
14	0x0 RW	**PANEL0_BKLTEN_wake_mask:** Reserved.
13	0x0 RW	**GP_CAMERASB04_wake_mask:** Reserved.
12	0x0 RW	**GP_CAMERASB11_wake_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
11	0x0 RW	**GP_CAMERASB07_wake_mask:** Reserved.
10	0x0 RW	**GP_CAMERASB01_wake_mask:** Reserved.
9	0x0 RW	**GP_CAMERASB09_wake_mask:** Reserved.
8	0x0 RW	**GP_CAMERASB03_wake_mask:** Reserved.
7	0x0 RW	**GP_CAMERASB10_wake_mask:** Reserved.
6	0x0 RW	**GP_CAMERASB06_wake_mask:** Reserved.
5	0x0 RW	**GP_CAMERASB00_wake_mask:** Reserved.
4	0x0 RW	**GP_CAMERASB08_wake_mask:** Reserved.
3	0x0 RW	**GP_CAMERASB02_wake_mask:** Reserved.
2	0x0 RW	**GP_CAMERASB05_wake_mask:** Reserved.
1	0x0 RW	**TDI_wake_mask:** Reserved.
0	0x0 RW	**SVID0_CLK_wake_mask:** Reserved.

10.5.29 GPIO Interrupt Status (gpio_interrupt_status)—Offset 300h

Status bits for the 16 interrupts.

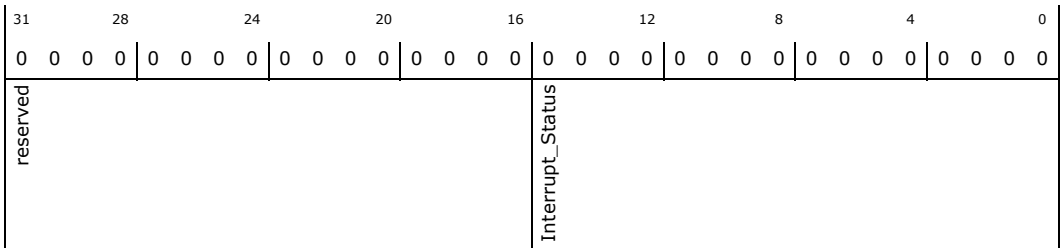
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 300h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW/1C	**reserved:** reserved
15:0	0x0 RW/1C	**Interrupt Status (Interrupt_Status):** Status bits for the 16 interrupts. Write 1 to Clear

10.5.30 GPIO Interrupt Status (gpio_interrupt_mask)—Offset 380h

Mask bits for the 16 interrupts.

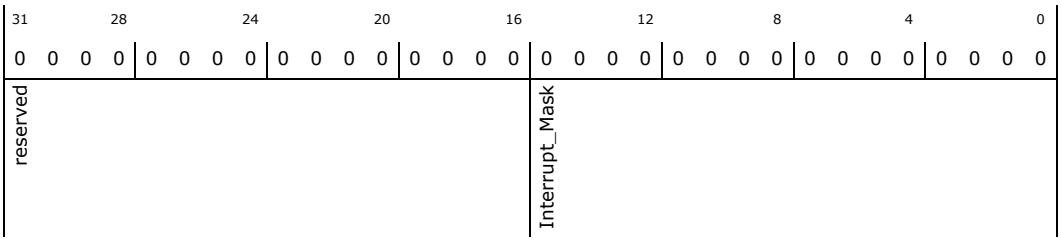
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 380h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**reserved:** reserved
15:0	0x0 RW	**Interrupt Mask (Interrupt_Mask):** Mask bits for the 16 interrupts. Interrupt masked when 0.

10.5.31 GPIO Broadcast Data Mask bit Register (gpio_family_bw_mask_31_0)—Offset 1000h

Write Mask that masks bit by bit the data written to BWData

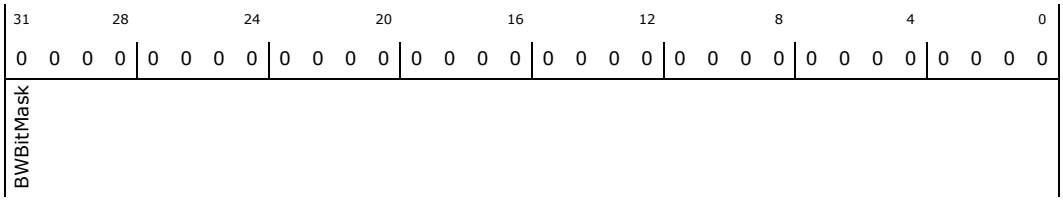
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 1000h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**BWBitMask:** Reserved.

10.5.32 GPIO Broadcast Data Register (gpio_family_bw_data_31_0)—Offset 1004h

Broadcast Write Data

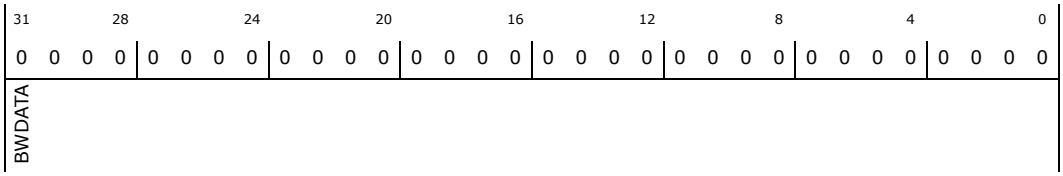
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 1004h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 WO	**BWDATA:** Reserved.

10.5.33 gpio_family_broadcast_reg_mask #0 (gpio_family_broadcast_reg_mask_0)—Offset 1008h

Family Broadcast Register Masking

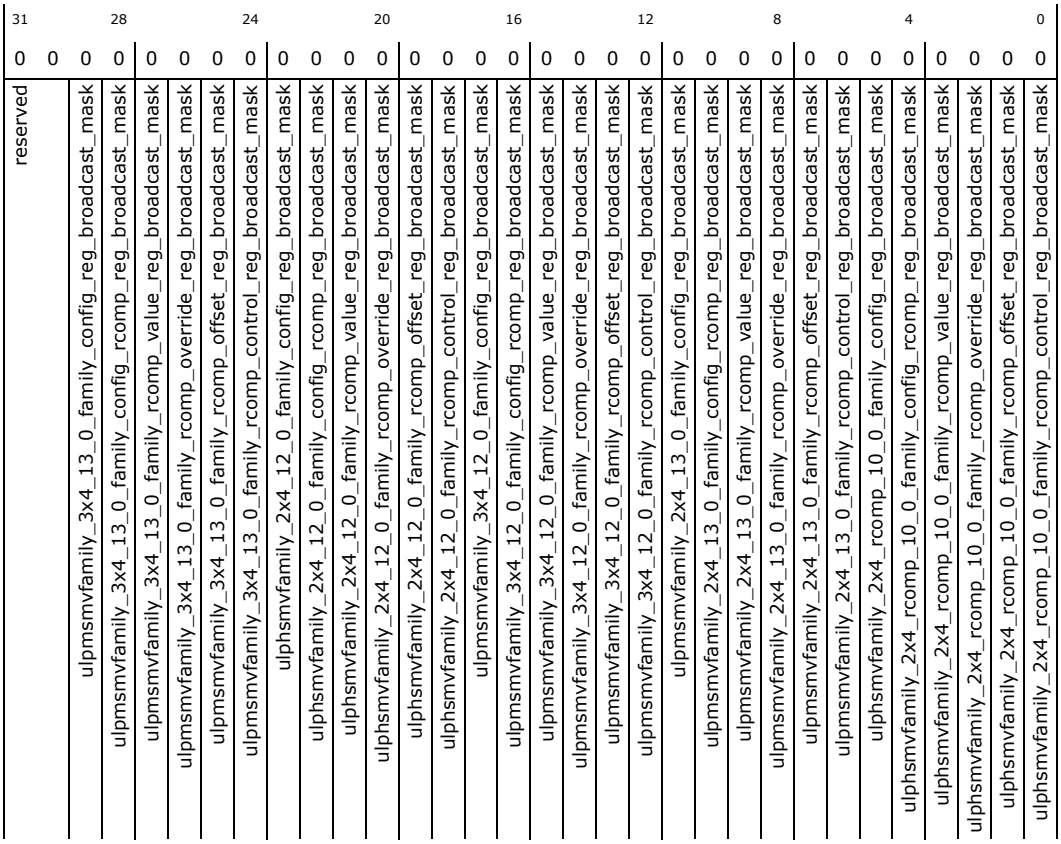
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 1008h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved:** Reserved.
29	0x0 RW	**ulpmsmvfamily_3x4_13_0_family_config_reg_broadcast_mask:** Reserved.
28	0x0 RW	**ulpmsmvfamily_3x4_13_0_family_config_rcomp_reg_broadcast_mask:** Reserved.
27	0x0 RW	**ulpmsmvfamily_3x4_13_0_family_rcomp_value_reg_broadcast_mask:** Reserved.
26	0x0 RW	**ulpmsmvfamily_3x4_13_0_family_rcomp_override_reg_broadcast_mask:** Reserved.
25	0x0 RW	**ulpmsmvfamily_3x4_13_0_family_rcomp_offset_reg_broadcast_mask:** Reserved.
24	0x0 RW	**ulpmsmvfamily_3x4_13_0_family_rcomp_control_reg_broadcast_mask:** Reserved.
23	0x0 RW	**ulphsmvfamily_2x4_12_0_family_config_reg_broadcast_mask:** Reserved.
22	0x0 RW	**ulphsmvfamily_2x4_12_0_family_config_rcomp_reg_broadcast_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
21	0x0 RW	**ulphsmvfamily_2x4_12_0_family_rcomp_value_reg_broadcast_mask:** Reserved.
20	0x0 RW	**ulphsmvfamily_2x4_12_0_family_rcomp_override_reg_broadcast_mask:** Reserved.
19	0x0 RW	**ulphsmvfamily_2x4_12_0_family_rcomp_offset_reg_broadcast_mask:** Reserved.
18	0x0 RW	**ulphsmvfamily_2x4_12_0_family_rcomp_control_reg_broadcast_mask:** Reserved.
17	0x0 RW	**ulpmsmvfamily_3x4_12_0_family_config_reg_broadcast_mask:** Reserved.
16	0x0 RW	**ulpmsmvfamily_3x4_12_0_family_config_rcomp_reg_broadcast_mask:** Reserved.
15	0x0 RW	**ulpmsmvfamily_3x4_12_0_family_rcomp_value_reg_broadcast_mask:** Reserved.
14	0x0 RW	**ulpmsmvfamily_3x4_12_0_family_rcomp_override_reg_broadcast_mask:** Reserved.
13	0x0 RW	**ulpmsmvfamily_3x4_12_0_family_rcomp_offset_reg_broadcast_mask:** Reserved.
12	0x0 RW	**ulpmsmvfamily_3x4_12_0_family_rcomp_control_reg_broadcast_mask:** Reserved.
11	0x0 RW	**ulpmsmvfamily_2x4_13_0_family_config_reg_broadcast_mask:** Reserved.
10	0x0 RW	**ulpmsmvfamily_2x4_13_0_family_config_rcomp_reg_broadcast_mask:** Reserved.
9	0x0 RW	**ulpmsmvfamily_2x4_13_0_family_rcomp_value_reg_broadcast_mask:** Reserved.
8	0x0 RW	**ulpmsmvfamily_2x4_13_0_family_rcomp_override_reg_broadcast_mask:** Reserved.
7	0x0 RW	**ulpmsmvfamily_2x4_13_0_family_rcomp_offset_reg_broadcast_mask:** Reserved.
6	0x0 RW	**ulpmsmvfamily_2x4_13_0_family_rcomp_control_reg_broadcast_mask:** Reserved.
5	0x0 RW	**ulphsmvfamily_2x4_rcomp_10_0_family_config_reg_broadcast_mask:** Reserved.
4	0x0 RW	**ulphsmvfamily_2x4_rcomp_10_0_family_config_rcomp_reg_broadcast_mask:** Reserved.
3	0x0 RW	**ulphsmvfamily_2x4_rcomp_10_0_family_rcomp_value_reg_broadcast_mask:** Reserved.
2	0x0 RW	**ulphsmvfamily_2x4_rcomp_10_0_family_rcomp_override_reg_broadcast_mask:** Reserved.
1	0x0 RW	**ulphsmvfamily_2x4_rcomp_10_0_family_rcomp_offset_reg_broadcast_mask:** Reserved.
0	0x0 RW	**ulphsmvfamily_2x4_rcomp_10_0_family_rcomp_control_reg_broadcast_mask:** Reserved.

10.5.34 RCOMP Control Register (ulphsmvfamily_2x4_rcomp_10_0_family_rcomp_control_reg)—Offset 1080h

RCOMP Control Register

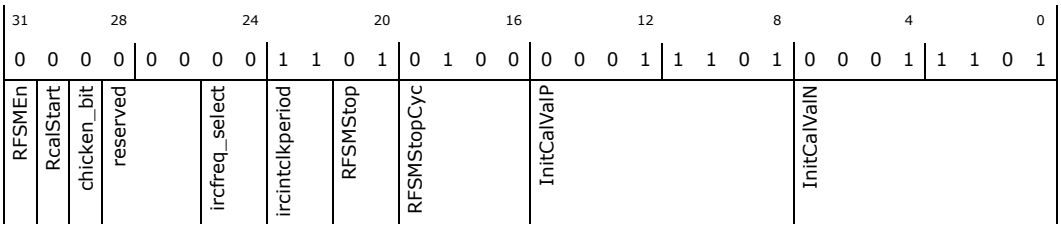
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 1080h

Op Codes:
h - Read, h - Write

Default: 00D41D1Dh



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**RCOMP FSM Enable (RFSMEn):** 0 = state machine disabled (clock gated) 1 = state machine enabled It is important to have this bit enabled in order for all internal clocks inside the RCOMP FSM to run.
30	0x0 RW	**RCOMP Calibration Start (RcalStart):** When set to 1 this bit triggers the RCOMP FSM to start hunting for the correct values for strength and slew. This bit should be cleared after calibration has finished. Before setting the RcalStart bit RFSMEn must have been asserted for at least 5 clock cycles. The first calibration takes 10us to complete and subsequent calibrations take 3us. Details of this process are in the CFIP RCOMP A Specification
29	0x0 RW	**RCOMP FSM Binary Chicken Bit (chicken_bit):** Toggling this bit Simulates a V1P8 Mode change. This will allow Binary re-calibration
28:26	0x0 RW	**reserved:** reserved
25:24	0x0 RW	**IRCCLK Frequency Select (ircfreq_select):** Clock ircclk frequency. This signals indicate what frequency ircclk is. This is used for 1 ms and 10 ms counters. 00 if clk input is 25 MHz (default, and SoC Clock) 01 if 50 MHz 10 if 100 MHz 11 if 125 MHz
23:22	0x3 RW	**IRC Internal Clock Period (ircintclkperiod):** To select rcomp clock period. This is the compensation clock frequency/period. Clock is derived from ircclk (which can be 25 MHz, 50 MHz, 100 MHz or 125 MHz user must set ircfreq_select[1:0] accordingly) 00 40 ns (64 ns for ircclk=125 MHz) 01 80 ns (96 ns for ircclk=125 MHz) 10 120 ns (128 ns for ircclk=125 MHz) (default) 11 160 ns (192 ns for ircclk=125 MHz)

Bit Range	Default and Access	Field Name (ID): Description
21:20	0x1 RW	**RCOMP FSM Stop Condition (RFSMStop):** RCOMP FSM Stop calibration condition. RCOMP FSM (Pull-up and Pull-down) will finish calibrating once orcpupen/orcpdnen toggles. The toggling indicates the compensation value has been reached. This option is programmable for toggle once (single edge), toggle twice (double edge), toggle thrice (triple edge) or forcing it to finish after a certain cycle (defined by RFSMStopCyc). 00b = single edge detect (10 or 01) 01b = double edge detect (101 or 010) (default) 10b = triple edge detect (1010 or 0101) 11b = stop after x cycles (depending on ircstpcyc[3:0] value -- This is meant for debug)
19:16	0x4 RW	**RCOMP FSM Stop Cycles (RFSMStopCyc):** Number of cycles to stop RCOMP FSM from searching for strength and slew settings. RFSMStop must be set to 11b for this option to take affect. 0000b = 0 cycle (illegal option) 0001b = 1 cycle (illegal option) 0010b = 2 cycles (illegal option) 0011b = 3 cycles (illegal option) 0100b = 4 cycles ... 1110b = 14 cycles 1111b = 15 cycles (maximum allowed) This is meant for debug.
15:8	0x1d RW	**Initial Pull-up Value (InitCalValP):** Initial pleg calibration value. RCOMP FSM will always start with this values for Pull-up calibration.
7:0	0x1d RW	**Initial Pull-down Value (InitCalValN):** Initial nleg calibration value. RCOMP FSM will always start with this values for Pull-down calibration.

10.5.35 RCOMP Offset Register (ulphsmvfamily_2x4_rcomp_10_0_family_rcomp_offset_reg)—Offset 1084h

RCOMP Offset Register

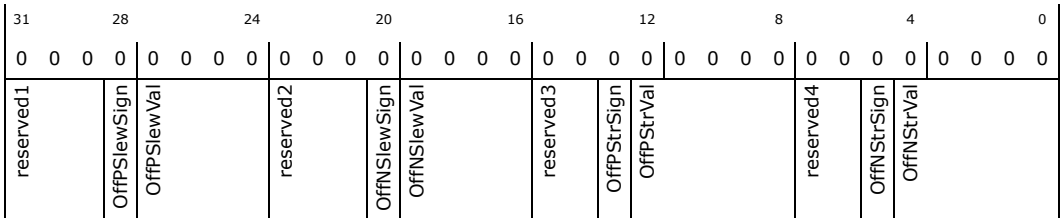
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 1084h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:29	0x0 RW	**Reserved (reserved1):** Reserved

Bit Range	Default and Access	Field Name (ID): Description
28	0x0 RW	**Pull-up Offset Slew Sign (OffPSlewSign):** Sign Bit for PSlew Offset strength value.
27:24	0x0 RW	**Pull-up Slew Offset (OffPSlewVal):** Offset slew value for pleg.
23:21	0x0 RW	**Reserved (reserved2):** Reserved
20	0x0 RW	**Pull-down Offset Slew Sign (OffNSlewSign):** Sign Bit for NSlew Offset strength value.
19:16	0x0 RW	**Pull-down Slew Offset (OffNSlewVal):** Offset slew value for nleg.
15:14	0x0 RW	**Reserved (reserved3):** Reserved
13	0x0 RW	**Pull-up Offset Strength Sign (OffPStrSign):** Sign Bit for PStrength Offset value.
12:8	0x0 RW	**Pull-up Offset Strength Value (OffPStrVal):** PStrength Offset Value.
7:6	0x0 RW	**Reserved (reserved4):** Reserved
5	0x0 RW	**Pull-down Offset Strength Sign (OffNStrSign):** Sign Bit for NStrength Offset value.
4:0	0x0 RW	**Pull-down Offset Strength Value (OffNStrVal):** NStrength Offset Value.

10.5.36 RCOMP Override Register (ulphsmvfamily_2x4_rcomp_10_0_family_rcomp_override_reg)—Offset 1088h

RCOMP Override Register

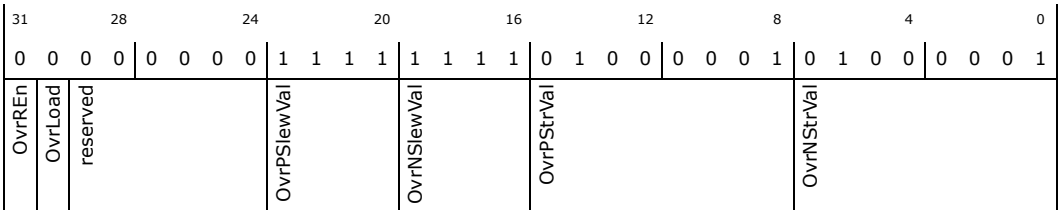
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 1088h

Op Codes:
h - Read, h - Write

Default: 00FF4141h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**Override RCOMP Enable (OvrREn):** Override enable bit to override the strength and slew values driven by the RCOMP FSM. The override values are driven through config registers. 0 = Override Disable 1 = Override Enable
30	0x0 RW	**Override Load (OvrLoad):** Load the override values into the RCOMP FSM and drive these values to the CFIO buffer. This is only valid when OvrRen = 1. 0 = Unload Values 1 = Load Values to CFIO
29:24	0x0 RW	**reserved:** reserved
23:20	0xf RW	**Override P Slew Value (OvrPSlewVal):** Override slew values for Pull-up settings.
19:16	0xf RW	**Override N Slew Value (OvrNSlewVal):** Override slew values for Pull-down settings.
15:8	0x41 RW	**Override Pull-up Strength Value (OvrPStrVal):** Override strength value for Pull-up settings. Should be 50ohm typical corner.
7:0	0x41 RW	**Override Pull-down Strength Value (OvrNStrVal):** Override strength value for Pull-down settings. Should be 50ohm typical corner.

10.5.37 RCOMP Value Register (ulphsmvfamily_2x4_rcomp_10_0_family_rcomp_value_reg)—Offset 108Ch

RCOMP Value Register

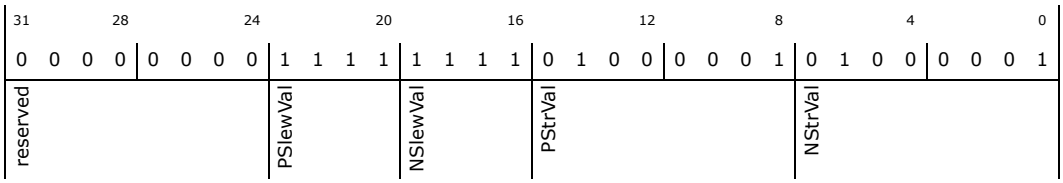
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 108Ch

Op Codes:
h - Read, h - Write

Default: 00FF4141h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RO	**reserved_fam1 (reserved):** reserved
23:20	0xf RO	**P Slew Value (PSlewVal):** P Slew values. Valid only after calibration is done.
19:16	0xf RO	**N Slew Value (NSlewVal):** N Slew values. Valid only after calibration is done.

Bit Range	Default and Access	Field Name (ID): Description
15:8	0x41 RO	**Pull-up Strength Value (PStrVal):** Compensation strength for pleg. This is valid only after calibration is done.
7:0	0x41 RO	**Pull-down Strength Value (NStrVal):** Compensation strength for nleg. This is valid only after calibration is done.

10.5.38 family_config_rcomp_reg (ulphsmvfamily_2x4_rcomp_10_0_family_config_rcomp_reg)—Offset 1090h

GPIO Family RCOMP Register

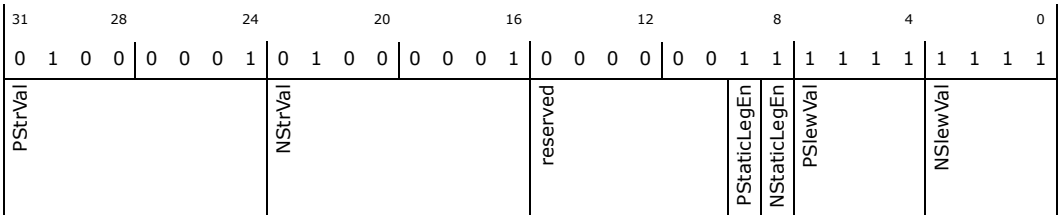
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 1090h

Op Codes:
h - Read, h - Write

Default: 414103FFh



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x41 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x41 RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable
7:4	0xf RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.
3:0	0xf RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.5.39 gpio_family_configuration_register (ulphsmvfamily_2x4_rcomp_10_0_family_config_reg)—Offset 1094h

GPIO Family CFIO Configuration Register

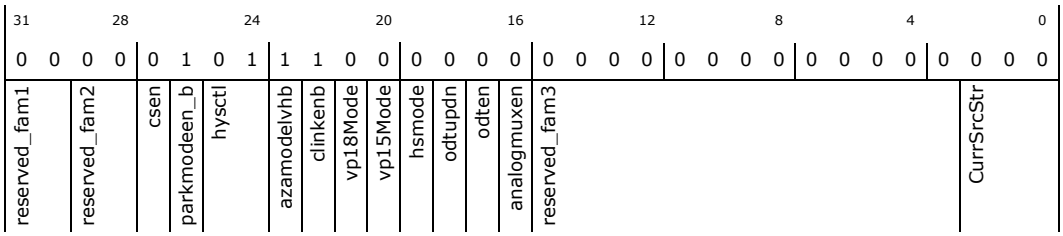
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 1094h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x1 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.5.40 family_config_rcomp_reg (ulpmsmvfamily_2x4_13_0_family_config_rcomp_reg)—Offset 1110h

GPIO Family RCOMP Register

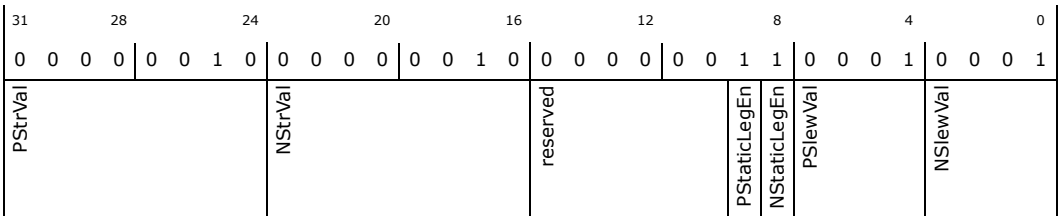
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 1110h

Op Codes:
h - Read, h - Write

Default: 02020311h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x2 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x2 RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable
7:4	0x1 RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.
3:0	0x1 RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.5.41 gpio_family_configuration_register (ulpmsmvfamily_2x4_13_0_family_config_reg)—Offset 1114h

GPIO Family CFIO Configuration Register

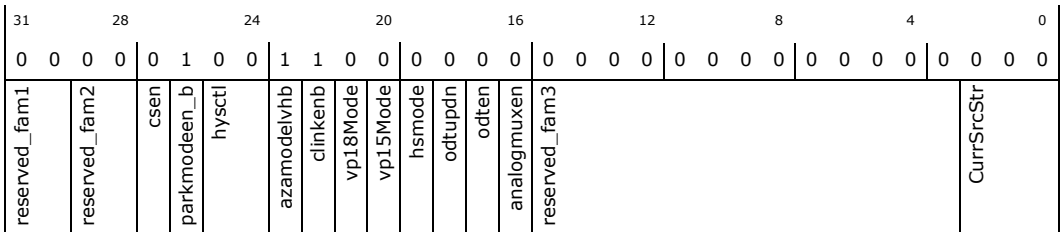
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 1114h

Op Codes:
h - Read, h - Write

Default: 04C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x0 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.5.42 family_config_rcomp_reg (ulpmsmvfamily_3x4_12_0_family_config_rcomp_reg)—Offset 1190h

GPIO Family RCOMP Register

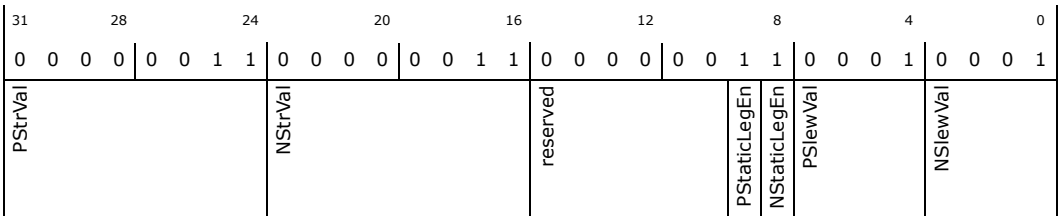
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 1190h

Op Codes:
h - Read, h - Write

Default: 03030311h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x3 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x3 RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable
7:4	0x1 RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.
3:0	0x1 RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.5.43 gpio_family_configuration_register (ulpmsmvfamily_3x4_12_0_family_config_reg)—Offset 1194h

GPIO Family CFIO Configuration Register

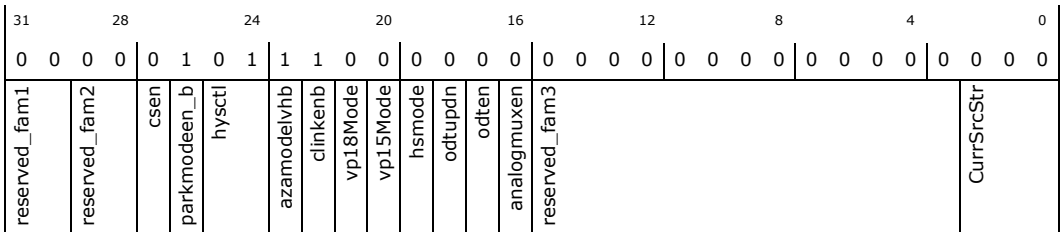
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 1194h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x1 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.5.44 family_config_rcomp_reg (ulphsmvfamily_2x4_12_0_family_config_rcomp_reg)—Offset 1210h

GPIO Family RCOMP Register

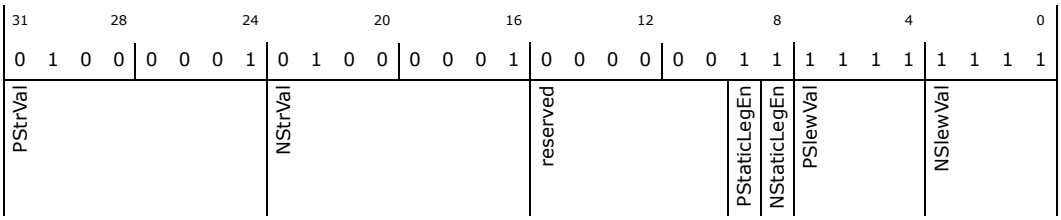
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 1210h

Op Codes:
h - Read, h - Write

Default: 414103FFh



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x41 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x41 RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable
7:4	0xf RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.
3:0	0xf RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.5.45 gpio_family_configuration_register (ulphsmvfamily_2x4_12_0_family_config_reg)—Offset 1214h

GPIO Family CFIO Configuration Register

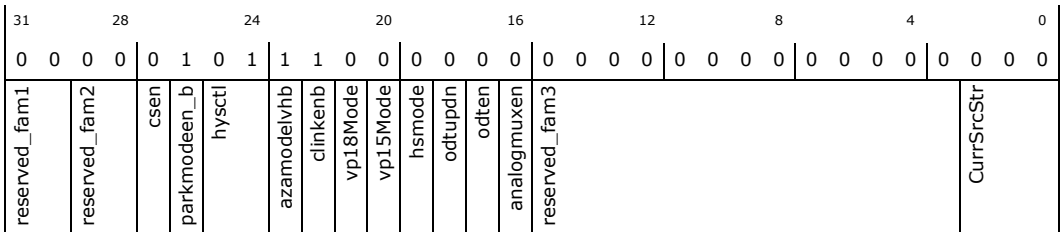
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 1214h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x1 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.5.46 family_config_rcomp_reg (ulpmsmvfamily_3x4_13_0_family_config_rcomp_reg)—Offset 1290h

GPIO Family RCOMP Register

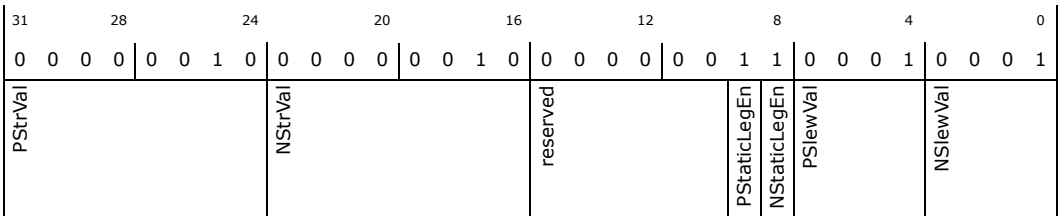
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 1290h

Op Codes:
h - Read, h - Write

Default: 02020311h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x2 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x2 RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable
7:4	0x1 RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.
3:0	0x1 RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.5.47 gpio_family_configuration_register (ulpmsmvfamily_3x4_13_0_family_config_reg)—Offset 1294h

GPIO Family CFIO Configuration Register

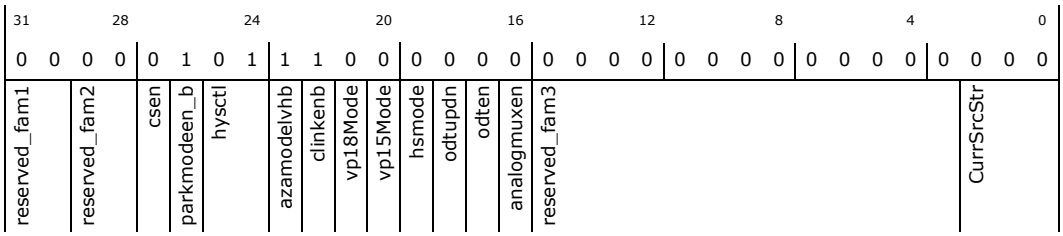
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 1294h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x1 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.5.48 GPIO Broadcast Data Mask bit Register (gpio_pad_bw_mask_31_0)—Offset 4000h

Write Mask that masks bit by bit the data written to BWData

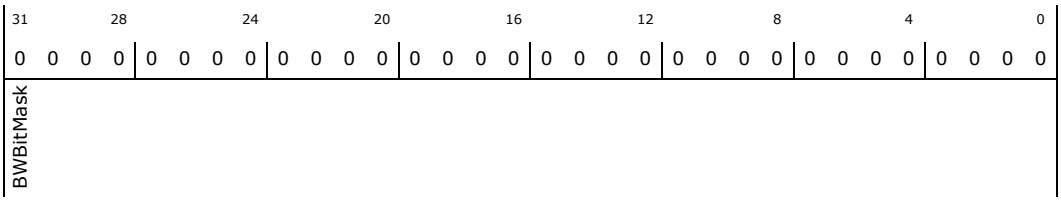
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4000h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**BWBitMask:** Reserved.

10.5.49 GPIO Broadcast Data Register (gpio_pad_bw_data_31_0)—Offset 4004h

Broadcast Write Data

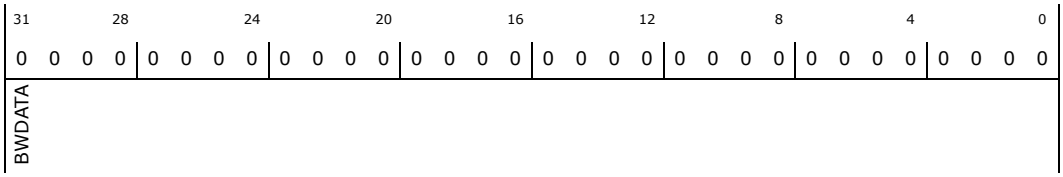
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4004h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 WO	**BWDATA:** Reserved.

10.5.50 gpio_pad_broadcast_reg_mask #0 (gpio_pad_broadcast_reg_mask_0)—Offset 4008h

Pad Broadcast Register Masking

Access Method

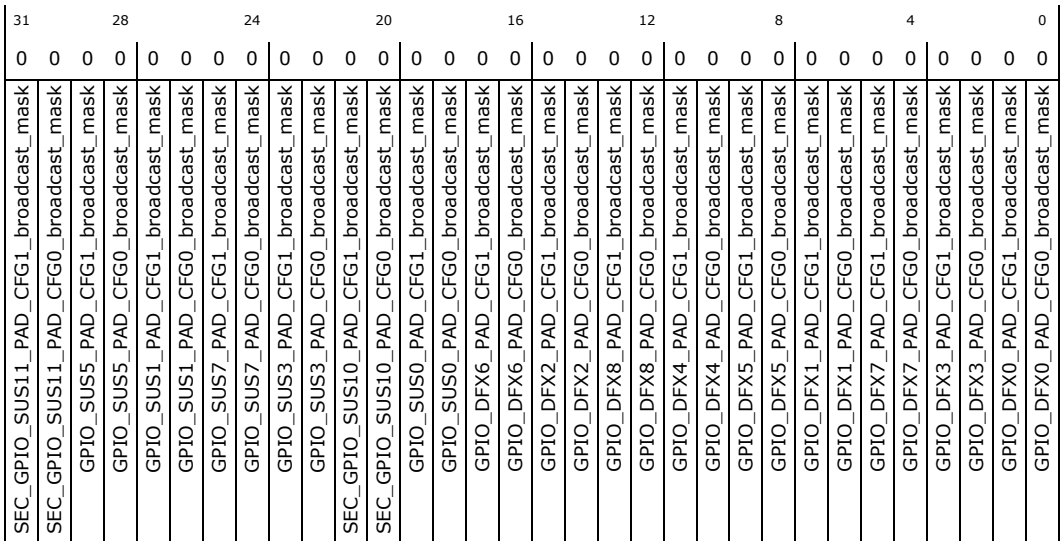
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4008h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**SEC_GPIO_SUS11_PAD_CFG1_broadcast_mask:** Reserved.
30	0x0 RW	**SEC_GPIO_SUS11_PAD_CFG0_broadcast_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
29	0x0 RW	**GPIO_SUS5_PAD_CFG1_broadcast_mask:** Reserved.
28	0x0 RW	**GPIO_SUS5_PAD_CFG0_broadcast_mask:** Reserved.
27	0x0 RW	**GPIO_SUS1_PAD_CFG1_broadcast_mask:** Reserved.
26	0x0 RW	**GPIO_SUS1_PAD_CFG0_broadcast_mask:** Reserved.
25	0x0 RW	**GPIO_SUS7_PAD_CFG1_broadcast_mask:** Reserved.
24	0x0 RW	**GPIO_SUS7_PAD_CFG0_broadcast_mask:** Reserved.
23	0x0 RW	**GPIO_SUS3_PAD_CFG1_broadcast_mask:** Reserved.
22	0x0 RW	**GPIO_SUS3_PAD_CFG0_broadcast_mask:** Reserved.
21	0x0 RW	**SEC_GPIO_SUS10_PAD_CFG1_broadcast_mask:** Reserved.
20	0x0 RW	**SEC_GPIO_SUS10_PAD_CFG0_broadcast_mask:** Reserved.
19	0x0 RW	**GPIO_SUS0_PAD_CFG1_broadcast_mask:** Reserved.
18	0x0 RW	**GPIO_SUS0_PAD_CFG0_broadcast_mask:** Reserved.
17	0x0 RW	**GPIO_DFX6_PAD_CFG1_broadcast_mask:** Reserved.
16	0x0 RW	**GPIO_DFX6_PAD_CFG0_broadcast_mask:** Reserved.
15	0x0 RW	**GPIO_DFX2_PAD_CFG1_broadcast_mask:** Reserved.
14	0x0 RW	**GPIO_DFX2_PAD_CFG0_broadcast_mask:** Reserved.
13	0x0 RW	**GPIO_DFX8_PAD_CFG1_broadcast_mask:** Reserved.
12	0x0 RW	**GPIO_DFX8_PAD_CFG0_broadcast_mask:** Reserved.
11	0x0 RW	**GPIO_DFX4_PAD_CFG1_broadcast_mask:** Reserved.
10	0x0 RW	**GPIO_DFX4_PAD_CFG0_broadcast_mask:** Reserved.
9	0x0 RW	**GPIO_DFX5_PAD_CFG1_broadcast_mask:** Reserved.
8	0x0 RW	**GPIO_DFX5_PAD_CFG0_broadcast_mask:** Reserved.
7	0x0 RW	**GPIO_DFX1_PAD_CFG1_broadcast_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
6	0x0 RW	**GPIO_DFX1_PAD_CFG0_broadcast_mask:** Reserved.
5	0x0 RW	**GPIO_DFX7_PAD_CFG1_broadcast_mask:** Reserved.
4	0x0 RW	**GPIO_DFX7_PAD_CFG0_broadcast_mask:** Reserved.
3	0x0 RW	**GPIO_DFX3_PAD_CFG1_broadcast_mask:** Reserved.
2	0x0 RW	**GPIO_DFX3_PAD_CFG0_broadcast_mask:** Reserved.
1	0x0 RW	**GPIO_DFX0_PAD_CFG1_broadcast_mask:** Reserved.
0	0x0 RW	**GPIO_DFX0_PAD_CFG0_broadcast_mask:** Reserved.

10.5.51 gpio_pad_broadcast_reg_mask #1 (gpio_pad_broadcast_reg_mask_1)—Offset 400Ch

Pad Broadcast Register Masking

Access Method

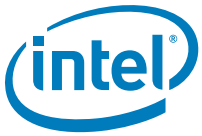
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 400Ch

Op Codes:
h - Read, h - Write

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TDO_PAD_CFG1_broadcast_mask	TDO_PAD_CFG0_broadcast_mask	SVID0_ALERT_B_PAD_CFG1_broadcast_mask	SVID0_ALERT_B_PAD_CFG0_broadcast_mask	CX_PRDY_B_PAD_CFG1_broadcast_mask	CX_PRDY_B_PAD_CFG0_broadcast_mask	TDO_2_PAD_CFG1_broadcast_mask	TDO_2_PAD_CFG0_broadcast_mask	CX_PRDY_B_2_PAD_CFG1_broadcast_mask	CX_PRDY_B_2_PAD_CFG0_broadcast_mask	TMS_PAD_CFG1_broadcast_mask	TMS_PAD_CFG0_broadcast_mask	SVID0_DATA_PAD_CFG1_broadcast_mask	SVID0_DATA_PAD_CFG0_broadcast_mask	PROCHOT_B_PAD_CFG1_broadcast_mask	PROCHOT_B_PAD_CFG0_broadcast_mask	TCK_PAD_CFG1_broadcast_mask	TCK_PAD_CFG0_broadcast_mask	TRST_B_PAD_CFG1_broadcast_mask	TRST_B_PAD_CFG0_broadcast_mask	SEC_GPIO_SUS9_PAD_CFG1_broadcast_mask	SEC_GPIO_SUS9_PAD_CFG0_broadcast_mask	CX_PREQ_B_PAD_CFG1_broadcast_mask	CX_PREQ_B_PAD_CFG0_broadcast_mask	GPIO_SUS6_PAD_CFG1_broadcast_mask	GPIO_SUS6_PAD_CFG0_broadcast_mask	GPIO_SUS2_PAD_CFG1_broadcast_mask	GPIO_SUS2_PAD_CFG0_broadcast_mask	SEC_GPIO_SUS8_PAD_CFG1_broadcast_mask	SEC_GPIO_SUS8_PAD_CFG0_broadcast_mask	GPIO_SUS4_PAD_CFG1_broadcast_mask	GPIO_SUS4_PAD_CFG0_broadcast_mask



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**TDO_PAD_CFG1_broadcast_mask:** Reserved.
30	0x0 RW	**TDO_PAD_CFG0_broadcast_mask:** Reserved.
29	0x0 RW	**SVID0_ALERT_B_PAD_CFG1_broadcast_mask:** Reserved.
28	0x0 RW	**SVID0_ALERT_B_PAD_CFG0_broadcast_mask:** Reserved.
27	0x0 RW	**CX_PRDY_B_PAD_CFG1_broadcast_mask:** Reserved.
26	0x0 RW	**CX_PRDY_B_PAD_CFG0_broadcast_mask:** Reserved.
25	0x0 RW	**TDO_2_PAD_CFG1_broadcast_mask:** Reserved.
24	0x0 RW	**TDO_2_PAD_CFG0_broadcast_mask:** Reserved.
23	0x0 RW	**CX_PRDY_B_2_PAD_CFG1_broadcast_mask:** Reserved.
22	0x0 RW	**CX_PRDY_B_2_PAD_CFG0_broadcast_mask:** Reserved.
21	0x0 RW	**TMS_PAD_CFG1_broadcast_mask:** Reserved.
20	0x0 RW	**TMS_PAD_CFG0_broadcast_mask:** Reserved.
19	0x0 RW	**SVID0_DATA_PAD_CFG1_broadcast_mask:** Reserved.
18	0x0 RW	**SVID0_DATA_PAD_CFG0_broadcast_mask:** Reserved.
17	0x0 RW	**PROCHOT_B_PAD_CFG1_broadcast_mask:** Reserved.
16	0x0 RW	**PROCHOT_B_PAD_CFG0_broadcast_mask:** Reserved.
15	0x0 RW	**TCK_PAD_CFG1_broadcast_mask:** Reserved.
14	0x0 RW	**TCK_PAD_CFG0_broadcast_mask:** Reserved.
13	0x0 RW	**TRST_B_PAD_CFG1_broadcast_mask:** Reserved.
12	0x0 RW	**TRST_B_PAD_CFG0_broadcast_mask:** Reserved.
11	0x0 RW	**SEC_GPIO_SUS9_PAD_CFG1_broadcast_mask:** Reserved.
10	0x0 RW	**SEC_GPIO_SUS9_PAD_CFG0_broadcast_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
9	0x0 RW	**CX_PREQ_B_PAD_CFG1_broadcast_mask:** Reserved.
8	0x0 RW	**CX_PREQ_B_PAD_CFG0_broadcast_mask:** Reserved.
7	0x0 RW	**GPIO_SUS6_PAD_CFG1_broadcast_mask:** Reserved.
6	0x0 RW	**GPIO_SUS6_PAD_CFG0_broadcast_mask:** Reserved.
5	0x0 RW	**GPIO_SUS2_PAD_CFG1_broadcast_mask:** Reserved.
4	0x0 RW	**GPIO_SUS2_PAD_CFG0_broadcast_mask:** Reserved.
3	0x0 RW	**SEC_GPIO_SUS8_PAD_CFG1_broadcast_mask:** Reserved.
2	0x0 RW	**SEC_GPIO_SUS8_PAD_CFG0_broadcast_mask:** Reserved.
1	0x0 RW	**GPIO_SUS4_PAD_CFG1_broadcast_mask:** Reserved.
0	0x0 RW	**GPIO_SUS4_PAD_CFG0_broadcast_mask:** Reserved.

10.5.52 gpio_pad_broadcast_reg_mask #2 (gpio_pad_broadcast_reg_mask_2)—Offset 4010h

Pad Broadcast Register Masking

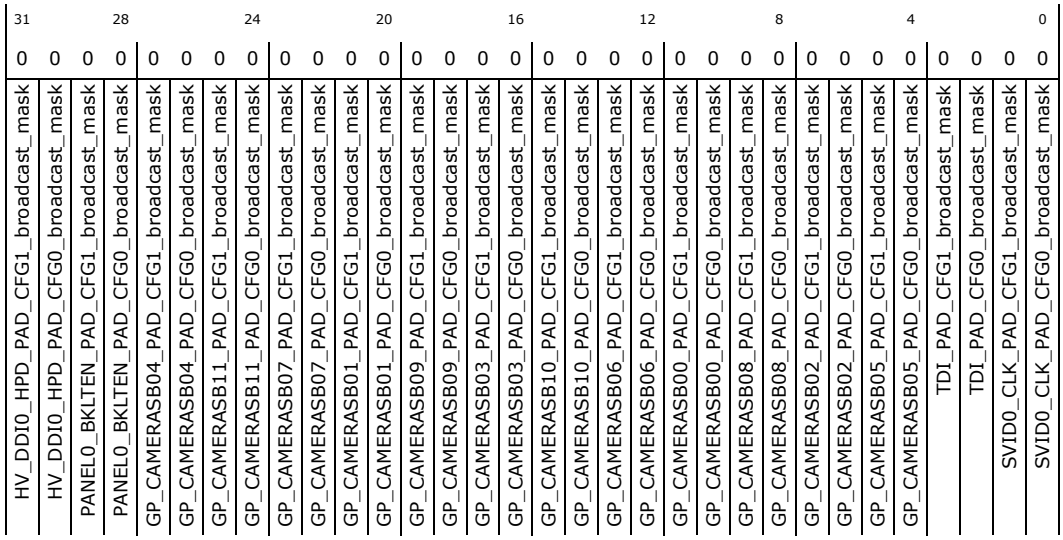
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4010h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**HV_DDI0_HPD_PAD_CFG1_broadcast_mask:** Reserved.
30	0x0 RW	**HV_DDI0_HPD_PAD_CFG0_broadcast_mask:** Reserved.
29	0x0 RW	**PANEL0_BKLTEN_PAD_CFG1_broadcast_mask:** Reserved.
28	0x0 RW	**PANEL0_BKLTEN_PAD_CFG0_broadcast_mask:** Reserved.
27	0x0 RW	**GP_CAMERASB04_PAD_CFG1_broadcast_mask:** Reserved.
26	0x0 RW	**GP_CAMERASB04_PAD_CFG0_broadcast_mask:** Reserved.
25	0x0 RW	**GP_CAMERASB11_PAD_CFG1_broadcast_mask:** Reserved.
24	0x0 RW	**GP_CAMERASB11_PAD_CFG0_broadcast_mask:** Reserved.
23	0x0 RW	**GP_CAMERASB07_PAD_CFG1_broadcast_mask:** Reserved.
22	0x0 RW	**GP_CAMERASB07_PAD_CFG0_broadcast_mask:** Reserved.
21	0x0 RW	**GP_CAMERASB01_PAD_CFG1_broadcast_mask:** Reserved.
20	0x0 RW	**GP_CAMERASB01_PAD_CFG0_broadcast_mask:** Reserved.
19	0x0 RW	**GP_CAMERASB09_PAD_CFG1_broadcast_mask:** Reserved.
18	0x0 RW	**GP_CAMERASB09_PAD_CFG0_broadcast_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
17	0x0 RW	**GP_CAMERASB03_PAD_CFG1_broadcast_mask:** Reserved.
16	0x0 RW	**GP_CAMERASB03_PAD_CFG0_broadcast_mask:** Reserved.
15	0x0 RW	**GP_CAMERASB10_PAD_CFG1_broadcast_mask:** Reserved.
14	0x0 RW	**GP_CAMERASB10_PAD_CFG0_broadcast_mask:** Reserved.
13	0x0 RW	**GP_CAMERASB06_PAD_CFG1_broadcast_mask:** Reserved.
12	0x0 RW	**GP_CAMERASB06_PAD_CFG0_broadcast_mask:** Reserved.
11	0x0 RW	**GP_CAMERASB00_PAD_CFG1_broadcast_mask:** Reserved.
10	0x0 RW	**GP_CAMERASB00_PAD_CFG0_broadcast_mask:** Reserved.
9	0x0 RW	**GP_CAMERASB08_PAD_CFG1_broadcast_mask:** Reserved.
8	0x0 RW	**GP_CAMERASB08_PAD_CFG0_broadcast_mask:** Reserved.
7	0x0 RW	**GP_CAMERASB02_PAD_CFG1_broadcast_mask:** Reserved.
6	0x0 RW	**GP_CAMERASB02_PAD_CFG0_broadcast_mask:** Reserved.
5	0x0 RW	**GP_CAMERASB05_PAD_CFG1_broadcast_mask:** Reserved.
4	0x0 RW	**GP_CAMERASB05_PAD_CFG0_broadcast_mask:** Reserved.
3	0x0 RW	**TDI_PAD_CFG1_broadcast_mask:** Reserved.
2	0x0 RW	**TDI_PAD_CFG0_broadcast_mask:** Reserved.
1	0x0 RW	**SVID0_CLK_PAD_CFG1_broadcast_mask:** Reserved.
0	0x0 RW	**SVID0_CLK_PAD_CFG0_broadcast_mask:** Reserved.

10.5.53 gpio_pad_broadcast_reg_mask #3 (gpio_pad_broadcast_reg_mask_3)—Offset 4014h

Pad Broadcast Register Masking

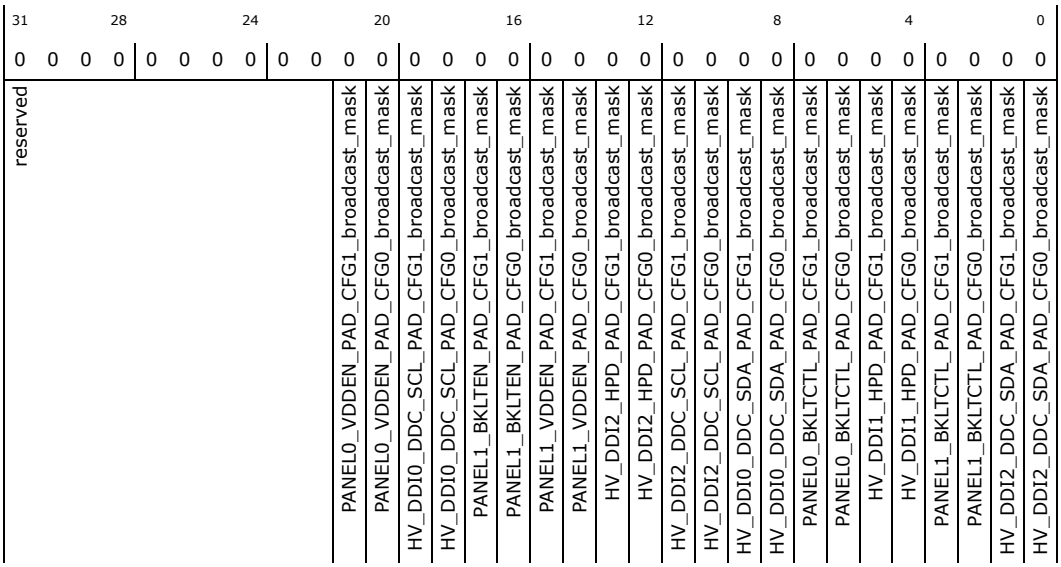
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4014h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:22	0x0 RW	**reserved:** Reserved.
21	0x0 RW	**PANEL0_VDDEN_PAD_CFG1_broadcast_mask:** Reserved.
20	0x0 RW	**PANEL0_VDDEN_PAD_CFG0_broadcast_mask:** Reserved.
19	0x0 RW	**HV_DDI0_DDC_SCL_PAD_CFG1_broadcast_mask:** Reserved.
18	0x0 RW	**HV_DDI0_DDC_SCL_PAD_CFG0_broadcast_mask:** Reserved.
17	0x0 RW	**PANEL1_BKLTEN_PAD_CFG1_broadcast_mask:** Reserved.
16	0x0 RW	**PANEL1_BKLTEN_PAD_CFG0_broadcast_mask:** Reserved.
15	0x0 RW	**PANEL1_VDDEN_PAD_CFG1_broadcast_mask:** Reserved.
14	0x0 RW	**PANEL1_VDDEN_PAD_CFG0_broadcast_mask:** Reserved.
13	0x0 RW	**HV_DDI2_HPD_PAD_CFG1_broadcast_mask:** Reserved.
12	0x0 RW	**HV_DDI2_HPD_PAD_CFG0_broadcast_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
11	0x0 RW	**HV_DDI2_DDC_SCL_PAD_CFG1_broadcast_mask:** Reserved.
10	0x0 RW	**HV_DDI2_DDC_SCL_PAD_CFG0_broadcast_mask:** Reserved.
9	0x0 RW	**HV_DDI0_DDC_SDA_PAD_CFG1_broadcast_mask:** Reserved.
8	0x0 RW	**HV_DDI0_DDC_SDA_PAD_CFG0_broadcast_mask:** Reserved.
7	0x0 RW	**PANEL0_BKLTCTL_PAD_CFG1_broadcast_mask:** Reserved.
6	0x0 RW	**PANEL0_BKLTCTL_PAD_CFG0_broadcast_mask:** Reserved.
5	0x0 RW	**HV_DDI1_HPD_PAD_CFG1_broadcast_mask:** Reserved.
4	0x0 RW	**HV_DDI1_HPD_PAD_CFG0_broadcast_mask:** Reserved.
3	0x0 RW	**PANEL1_BKLTCTL_PAD_CFG1_broadcast_mask:** Reserved.
2	0x0 RW	**PANEL1_BKLTCTL_PAD_CFG0_broadcast_mask:** Reserved.
1	0x0 RW	**HV_DDI2_DDC_SDA_PAD_CFG1_broadcast_mask:** Reserved.
0	0x0 RW	**HV_DDI2_DDC_SDA_PAD_CFG0_broadcast_mask:** Reserved.

10.5.54 Pad Control Register 0 (GPIO_DFX0_PAD_CFG0)—Offset 4400h

Pad Control Register 0

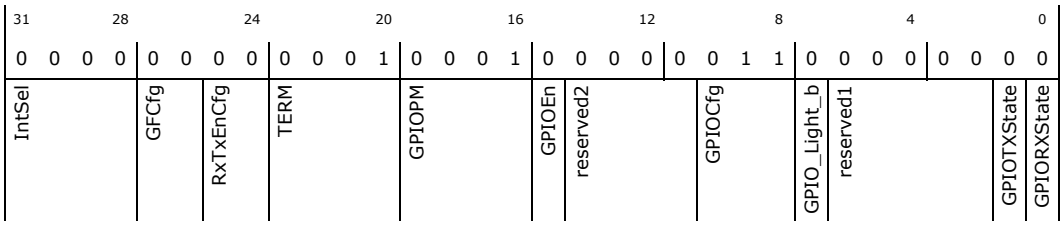
Access Method

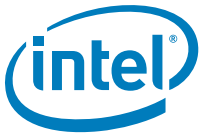
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4400h

Op Codes:
h - Read, h - Write

Default: 00110300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.55 Pad Control Register 1 (GPIO_DFX0_PAD_CFG1)—Offset 4404h

Pad Control Register 1

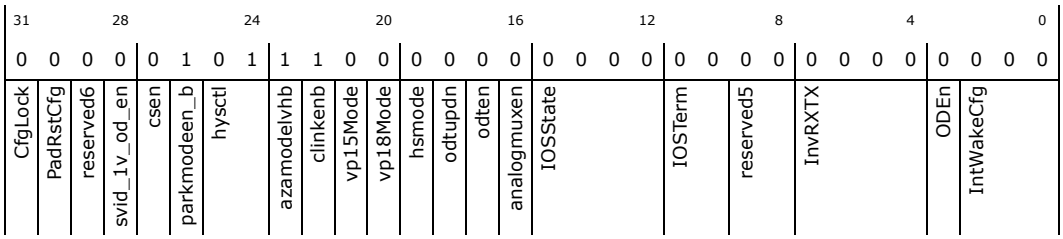
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4404h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.56 Pad Control Register 0 (GPIO_DFX3_PAD_CFG0)—Offset 4408h

Pad Control Register 0

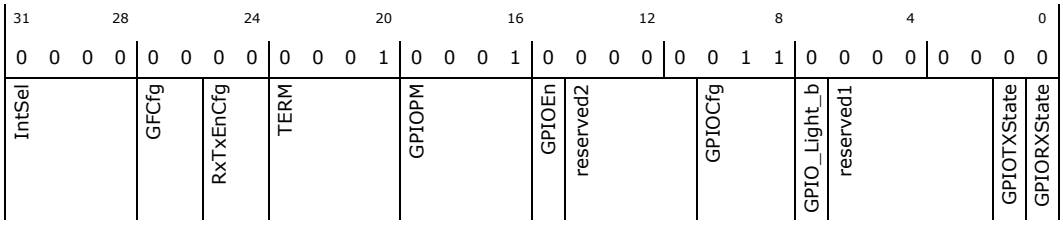
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4408h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.57 Pad Control Register 1 (GPIO_DFX3_PAD_CFG1)—Offset 440Ch

Pad Control Register 1

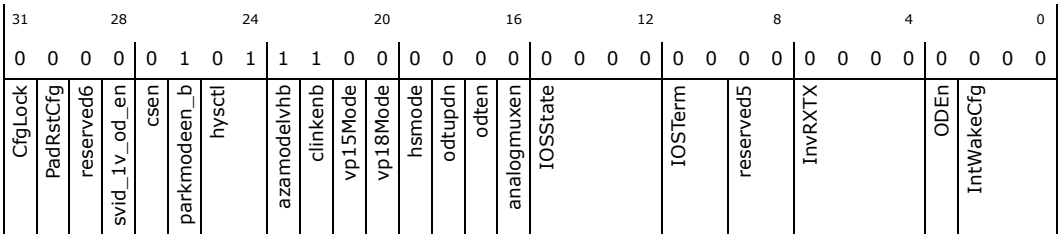
Access Method

Type: Message Bus Register (Size: 32 bits)

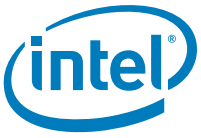
Offset: [Port: 0x13] + 440Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.



Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.58 Pad Control Register 0 (GPIO_DFX7_PAD_CFG0)—Offset 4410h

Pad Control Register 0

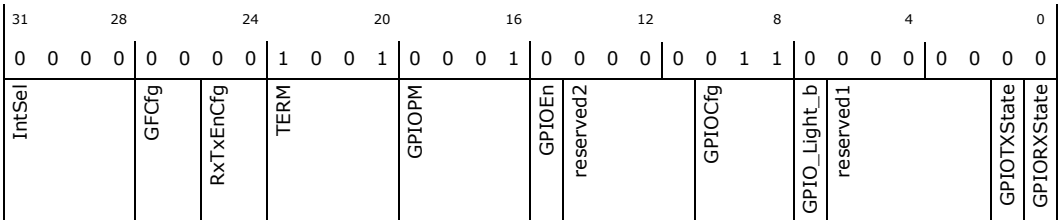
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4410h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.59 Pad Control Register 1 (GPIO_DFX7_PAD_CFG1)—Offset 4414h

Pad Control Register 1

Access Method

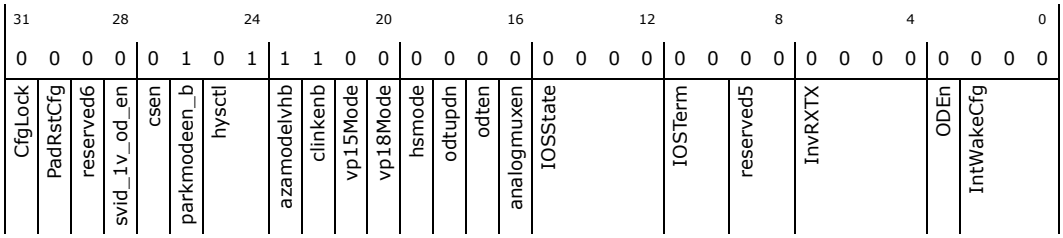
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4414h

Op Codes:

h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.60 Pad Control Register 0 (GPIO_DFX1_PAD_CFG0)—Offset 4418h

Pad Control Register 0

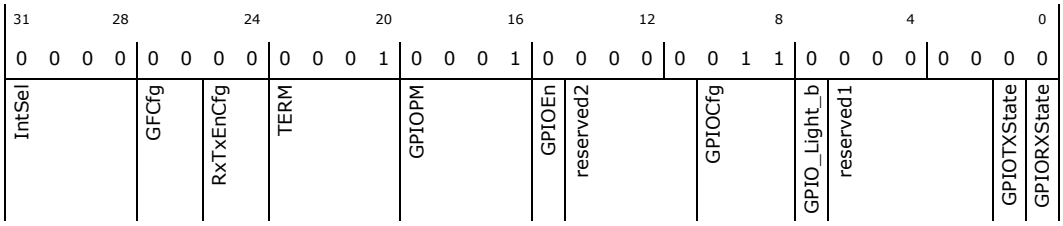
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4418h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.61 Pad Control Register 1 (GPIO_DFX1_PAD_CFG1)—Offset 441Ch

Pad Control Register 1

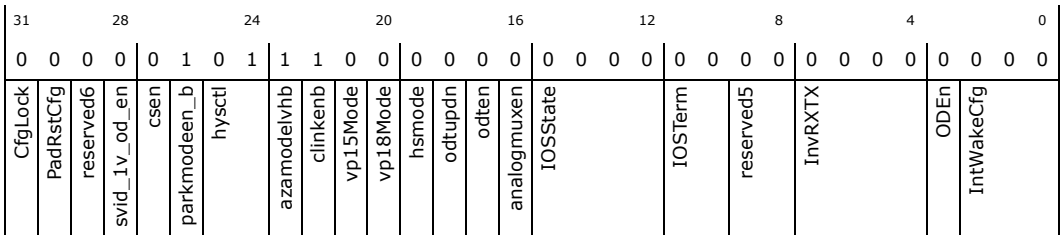
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 441Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.62 Pad Control Register 0 (GPIO_DFX5_PAD_CFG0)—Offset 4420h

Pad Control Register 0

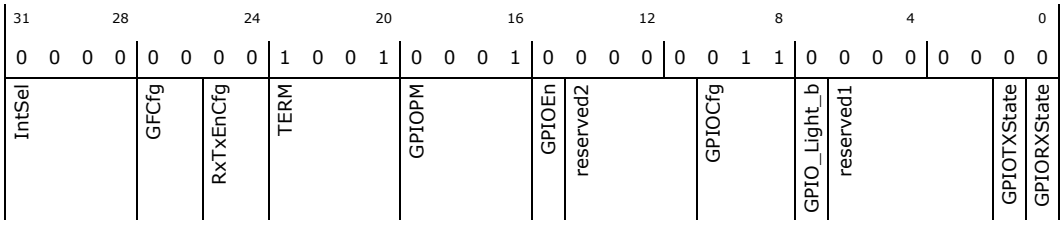
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4420h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.63 Pad Control Register 1 (GPIO_DFX5_PAD_CFG1)—Offset 4424h

Pad Control Register 1

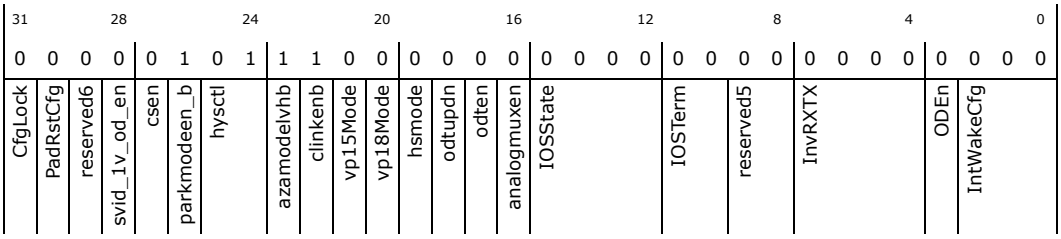
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4424h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.64 Pad Control Register 0 (GPIO_DFX4_PAD_CFG0)—Offset 4428h

Pad Control Register 0

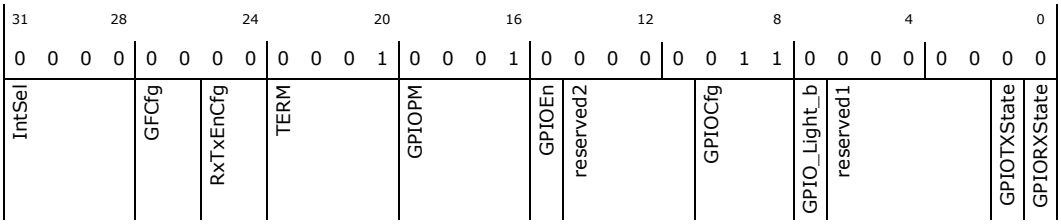
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4428h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.65 Pad Control Register 1 (GPIO_DFX4_PAD_CFG1)—Offset 442Ch

Pad Control Register 1

Access Method

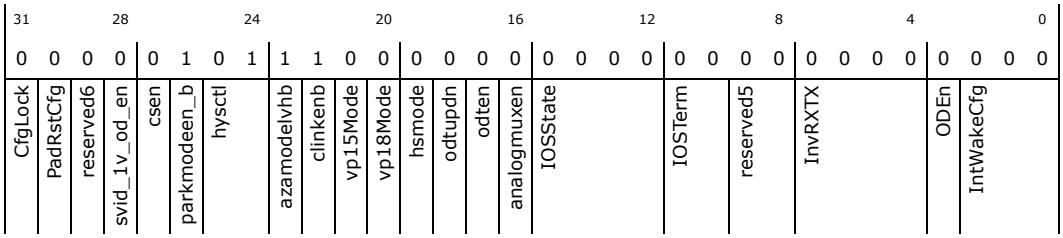
Type: Message Bus Register (Size: 32 bits)

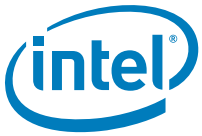
Offset: [Port: 0x13] + 442Ch

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.66 Pad Control Register 0 (GPIO_DFX8_PAD_CFG0)—Offset 4430h

Pad Control Register 0

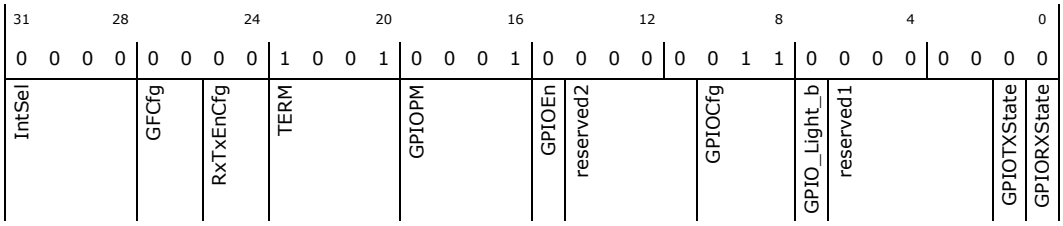
Access Method

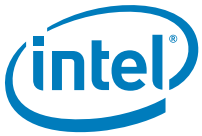
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4430h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.67 Pad Control Register 1 (GPIO_DFX8_PAD_CFG1)—Offset 4434h

Pad Control Register 1

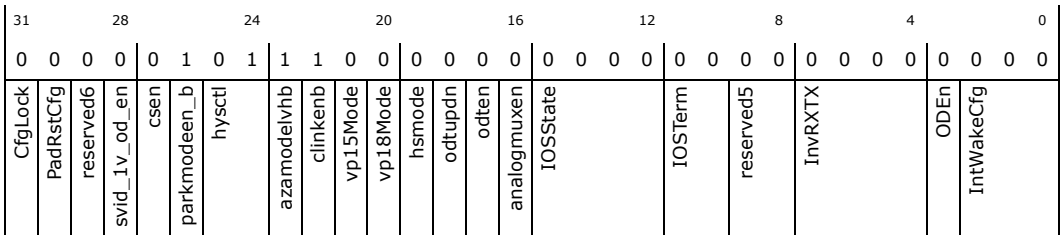
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4434h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.68 Pad Control Register 0 (GPIO_DFX2_PAD_CFG0)—Offset 4438h

Pad Control Register 0

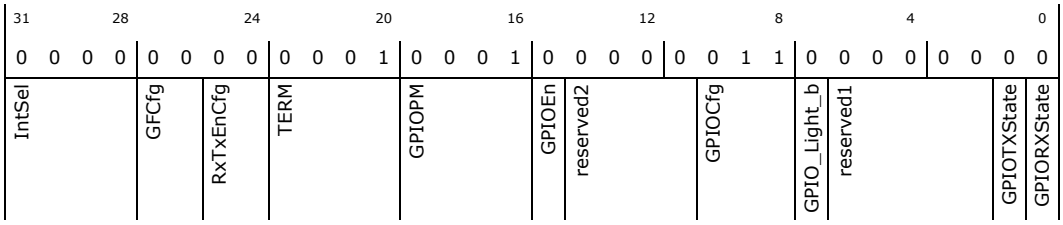
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4438h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.69 Pad Control Register 1 (GPIO_DFX2_PAD_CFG1)—Offset 443Ch

Pad Control Register 1

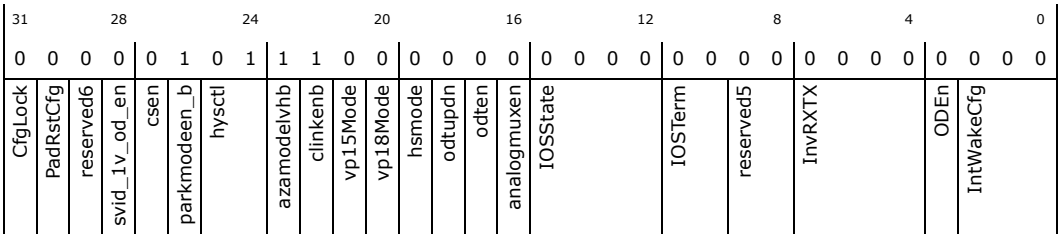
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 443Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.70 Pad Control Register 0 (GPIO_DFX6_PAD_CFG0)—Offset 4440h

Pad Control Register 0

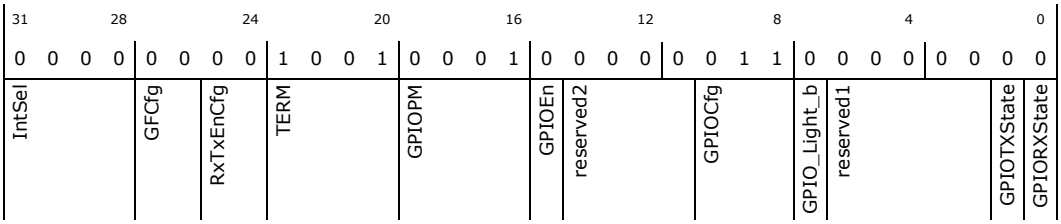
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4440h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.71 Pad Control Register 1 (GPIO_DFX6_PAD_CFG1)—Offset 4444h

Pad Control Register 1

Access Method

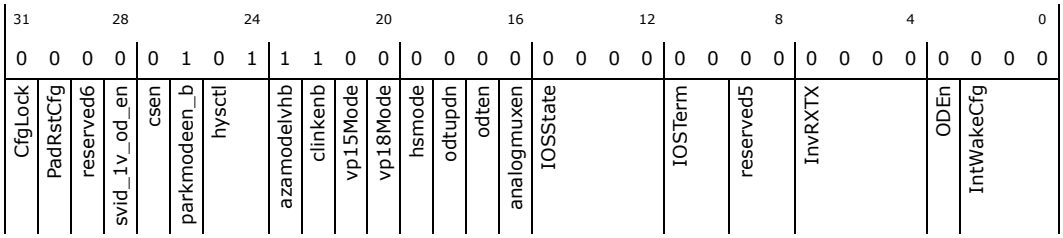
Type: Message Bus Register (Size: 32 bits)

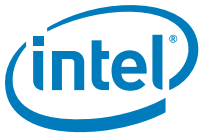
Offset: [Port: 0x13] + 4444h

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.72 Pad Control Register 0 (GPIO_SUS0_PAD_CFG0)—Offset 4800h

Pad Control Register 0

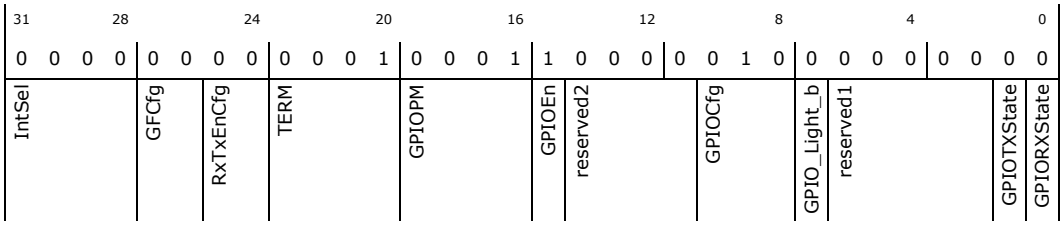
Access Method

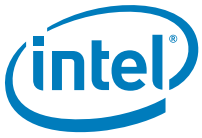
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4800h

Op Codes:
h - Read, h - Write

Default: 00118200h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x1 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x2 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.73 Pad Control Register 1 (GPIO_SUS0_PAD_CFG1)—Offset 4804h

Pad Control Register 1

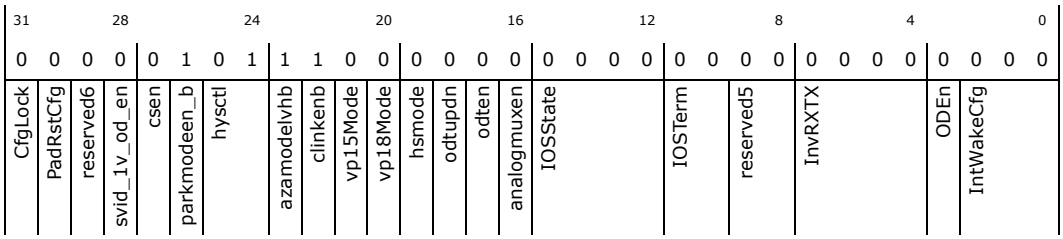
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4804h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.74 Pad Control Register 0 (SEC_GPIO_SUS10_PAD_CFG0)—Offset 4808h

Pad Control Register 0

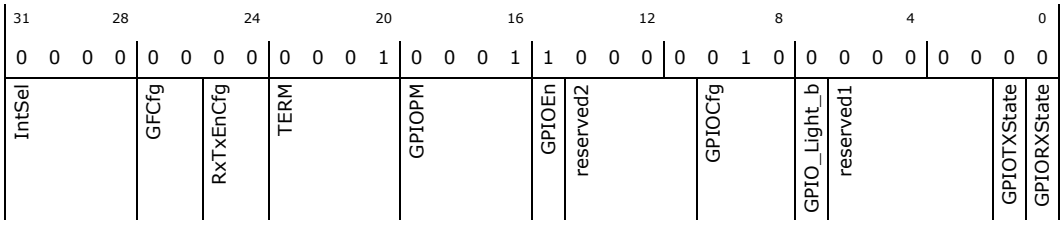
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4808h

Op Codes:
h - Read, h - Write

Default: 00118200h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x1 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x2 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.75 Pad Control Register 1 (SEC_GPIO_SUS10_PAD_CFG1)—Offset 480Ch

Pad Control Register 1

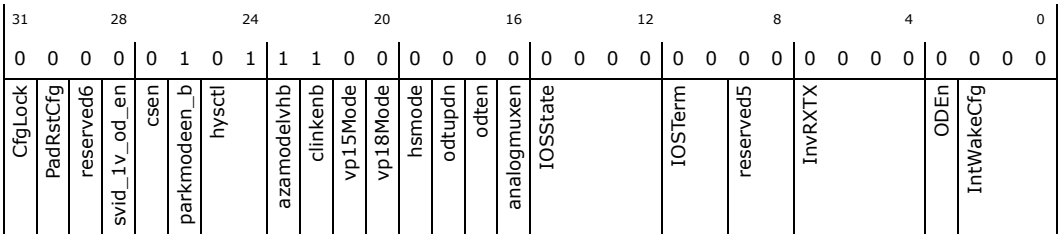
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 480Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.76 Pad Control Register 0 (GPIO_SUS3_PAD_CFG0)—Offset 4810h

Pad Control Register 0

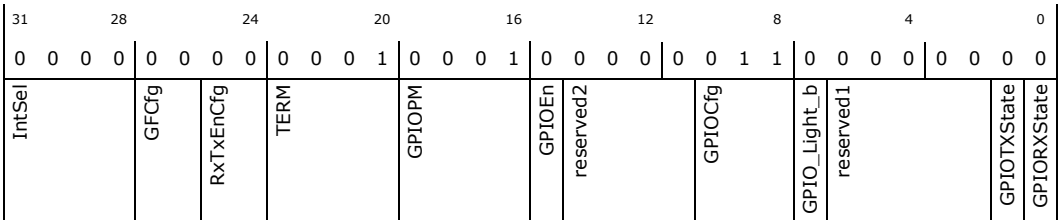
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4810h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.77 Pad Control Register 1 (GPIO_SUS3_PAD_CFG1)—Offset 4814h

Pad Control Register 1

Access Method

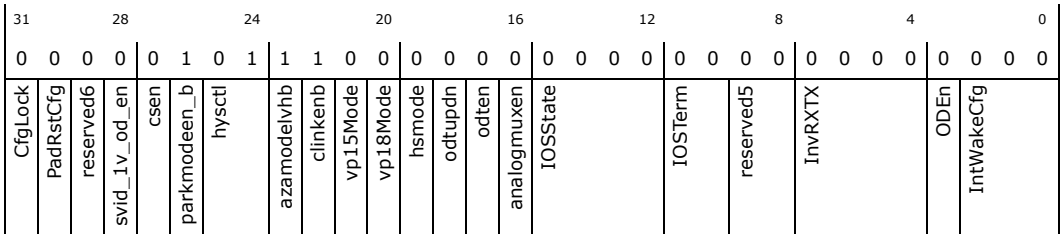
Type: Message Bus Register (Size: 32 bits)

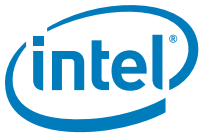
Offset: [Port: 0x13] + 4814h

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.78 Pad Control Register 0 (GPIO_SUS7_PAD_CFG0)—Offset 4818h

Pad Control Register 0

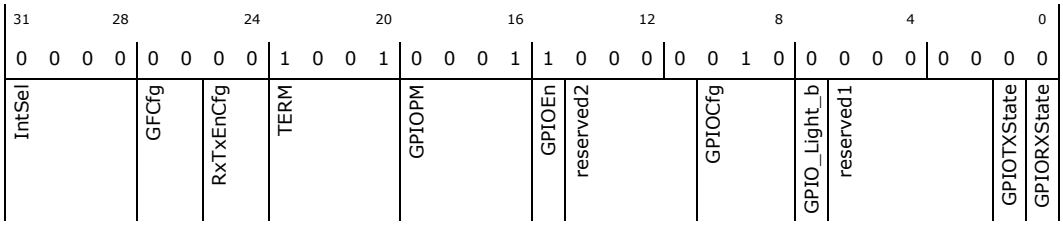
Access Method

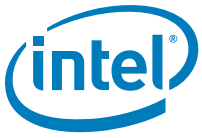
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4818h

Op Codes:
h - Read, h - Write

Default: 00918200h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x1 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x2 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.79 Pad Control Register 1 (GPIO_SUS7_PAD_CFG1)—Offset 481Ch

Pad Control Register 1

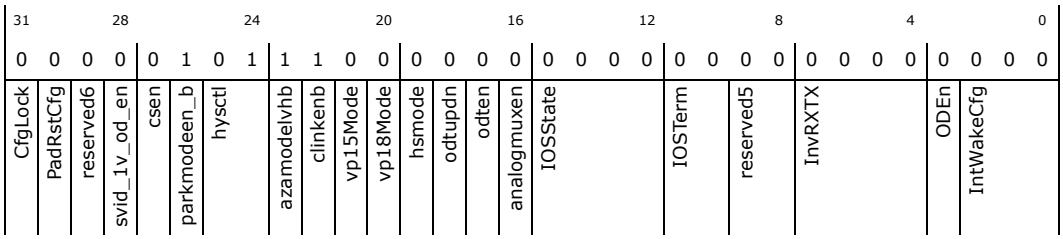
Access Method

Type: Message Bus Register (Size: 32 bits)

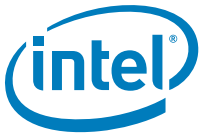
Offset: [Port: 0x13] + 481Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.



Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.80 Pad Control Register 0 (GPIO_SUS1_PAD_CFG0)—Offset 4820h

Pad Control Register 0

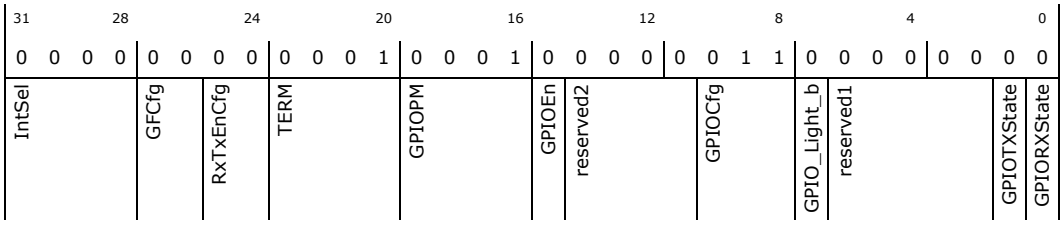
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4820h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.81 Pad Control Register 1 (GPIO_SUS1_PAD_CFG1)—Offset 4824h

Pad Control Register 1

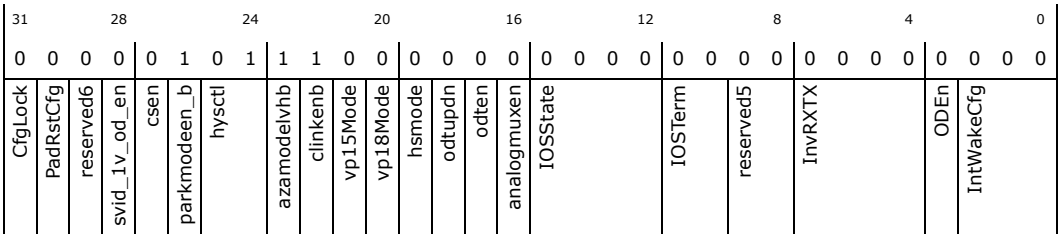
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4824h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.82 Pad Control Register 0 (GPIO_SUS5_PAD_CFG0)—Offset 4828h

Pad Control Register 0

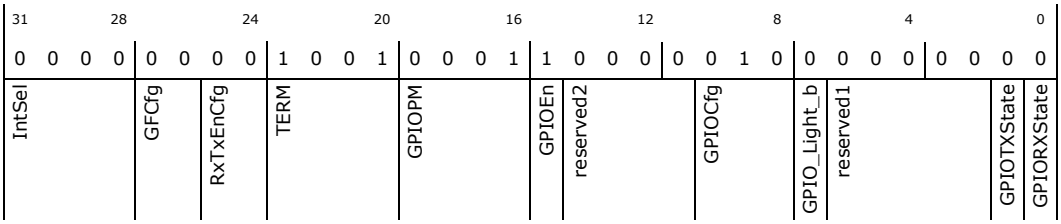
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4828h

Op Codes:
h - Read, h - Write

Default: 00918200h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x1 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x2 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.83 Pad Control Register 1 (GPIO_SUS5_PAD_CFG1)—Offset 482Ch

Pad Control Register 1

Access Method

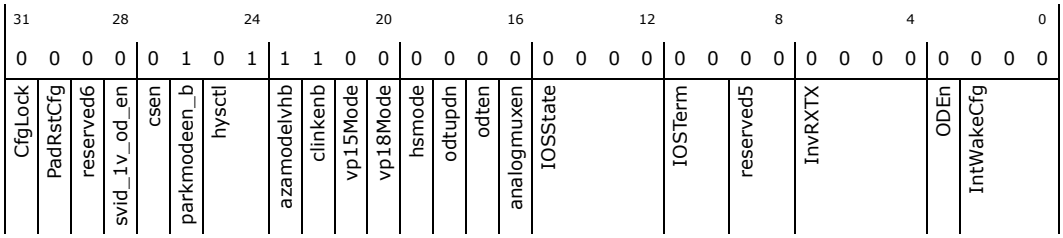
Type: Message Bus Register (Size: 32 bits)

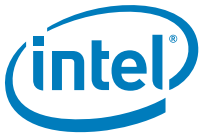
Offset: [Port: 0x13] + 482Ch

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.84 Pad Control Register 0 (SEC_GPIO_SUS11_PAD_CFG0)—Offset 4830h

Pad Control Register 0

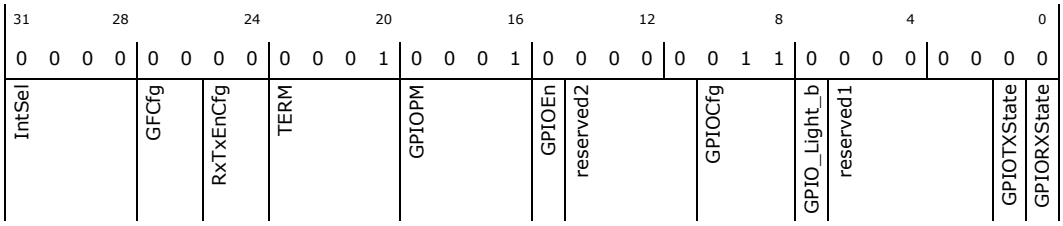
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4830h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.85 Pad Control Register 1 (SEC_GPIO_SUS11_PAD_CFG1)—Offset 4834h

Pad Control Register 1

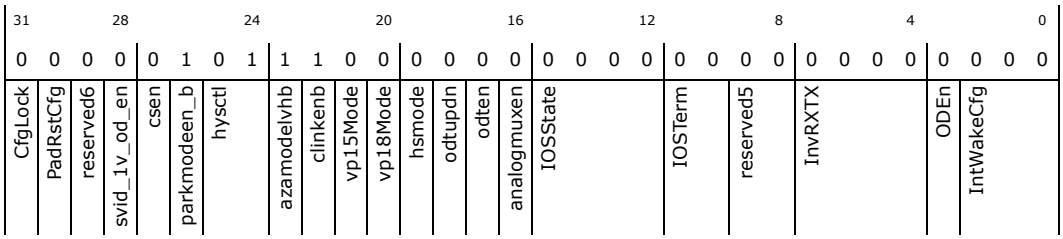
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4834h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.86 Pad Control Register 0 (GPIO_SUS4_PAD_CFG0)—Offset 4838h

Pad Control Register 0

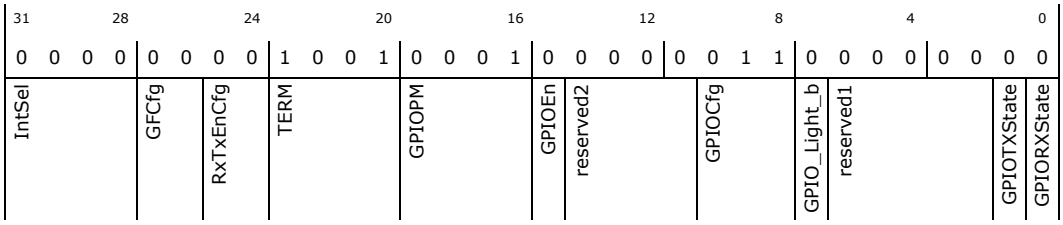
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4838h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.87 Pad Control Register 1 (GPIO_SUS4_PAD_CFG1)—Offset 483Ch

Pad Control Register 1

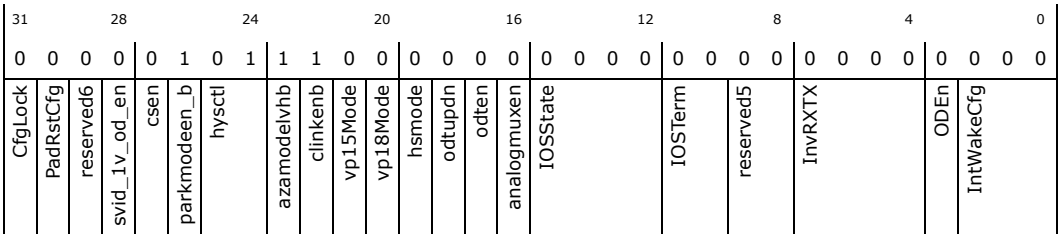
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 483Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.88 Pad Control Register 0 (SEC_GPIO_SUS8_PAD_CFG0)—Offset 4840h

Pad Control Register 0

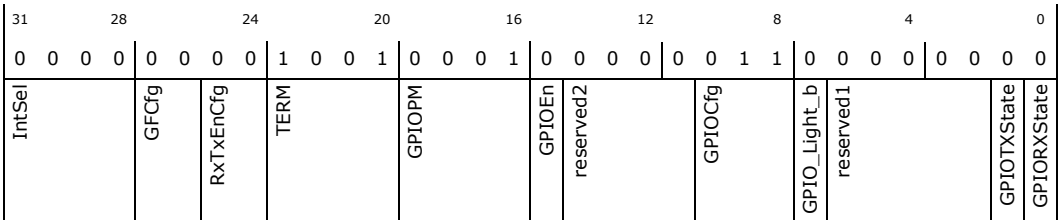
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4840h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.89 Pad Control Register 1 (SEC_GPIO_SUS8_PAD_CFG1)—Offset 4844h

Pad Control Register 1

Access Method

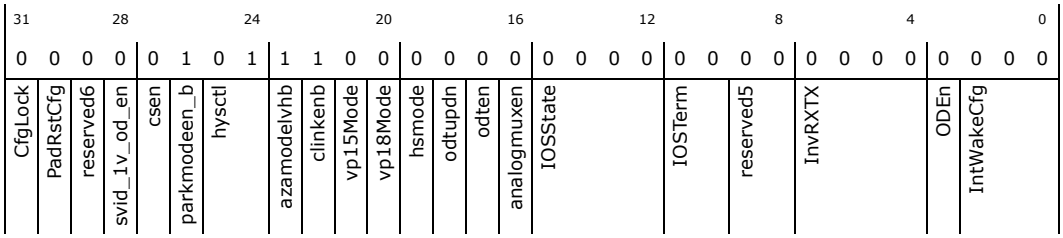
Type: Message Bus Register (Size: 32 bits)

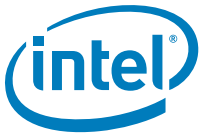
Offset: [Port: 0x13] + 4844h

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.90 Pad Control Register 0 (GPIO_SUS2_PAD_CFG0)—Offset 4848h

Pad Control Register 0

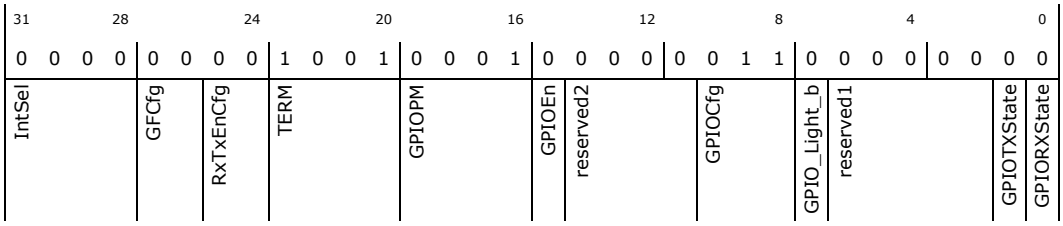
Access Method

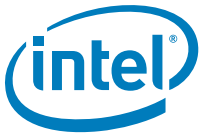
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4848h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.91 Pad Control Register 1 (GPIO_SUS2_PAD_CFG1)—Offset 484Ch

Pad Control Register 1

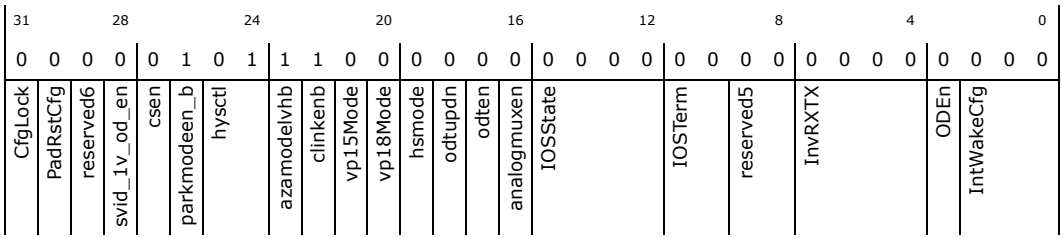
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 484Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.92 Pad Control Register 0 (GPIO_SUS6_PAD_CFG0)—Offset 4850h

Pad Control Register 0

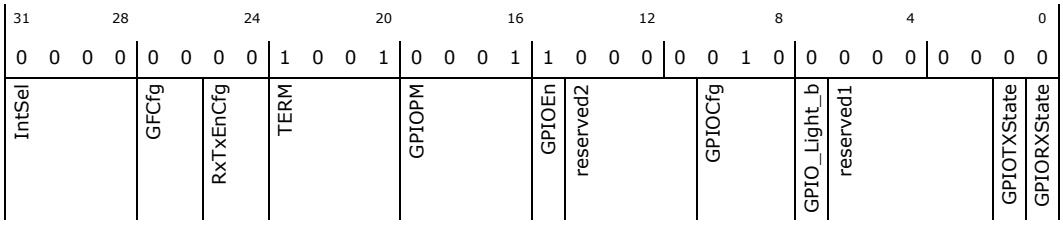
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4850h

Op Codes:
h - Read, h - Write

Default: 00918200h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x1 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x2 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.93 Pad Control Register 1 (GPIO_SUS6_PAD_CFG1)—Offset 4854h

Pad Control Register 1

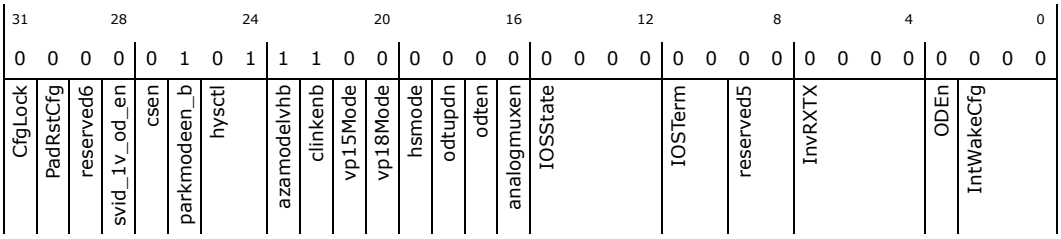
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4854h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.94 Pad Control Register 0 (CX_PREQ_B_PAD_CFG0)—Offset 4858h

Pad Control Register 0

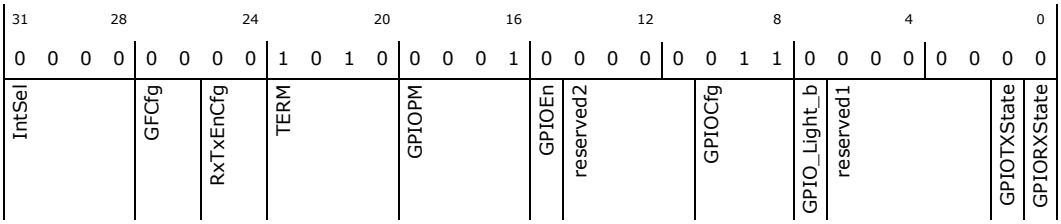
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4858h

Op Codes:
h - Read, h - Write

Default: 00A10300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0xa RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.95 Pad Control Register 1 (CX_PREQ_B_PAD_CFG1)—Offset 485Ch

Pad Control Register 1

Access Method

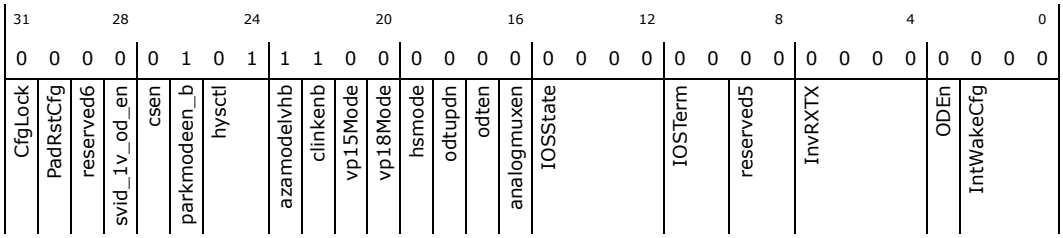
Type: Message Bus Register (Size: 32 bits)

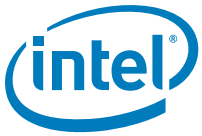
Offset: [Port: 0x13] + 485Ch

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.96 Pad Control Register 0 (SEC_GPIO_SUS9_PAD_CFG0)—Offset 4860h

Pad Control Register 0

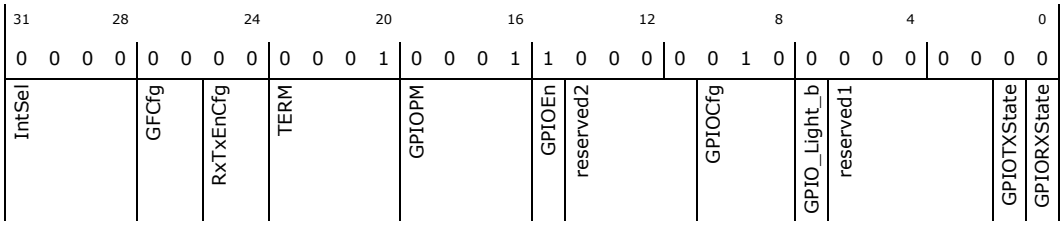
Access Method

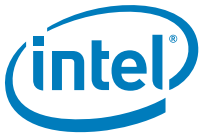
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4860h

Op Codes:
h - Read, h - Write

Default: 00118200h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x1 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x2 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.97 Pad Control Register 1 (SEC_GPIO_SUS9_PAD_CFG1)—Offset 4864h

Pad Control Register 1

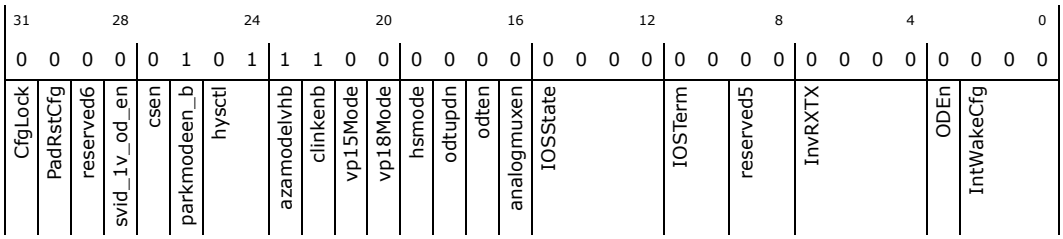
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4864h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.98 Pad Control Register 0 (TRST_B_PAD_CFG0)—Offset 4C00h

Pad Control Register 0

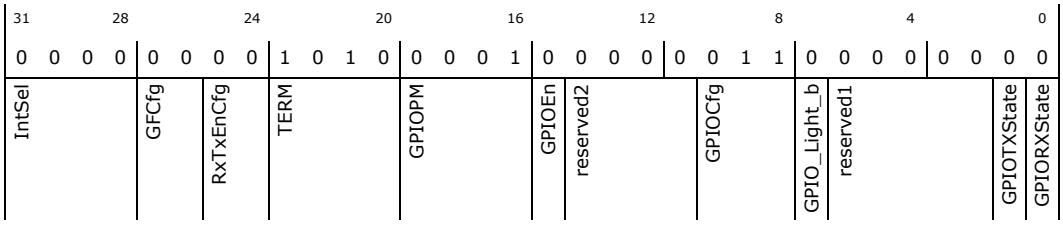
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C00h

Op Codes:
h - Read, h - Write

Default: 00A10300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0xa RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.99 Pad Control Register 1 (TRST_B_PAD_CFG1)—Offset 4C04h

Pad Control Register 1

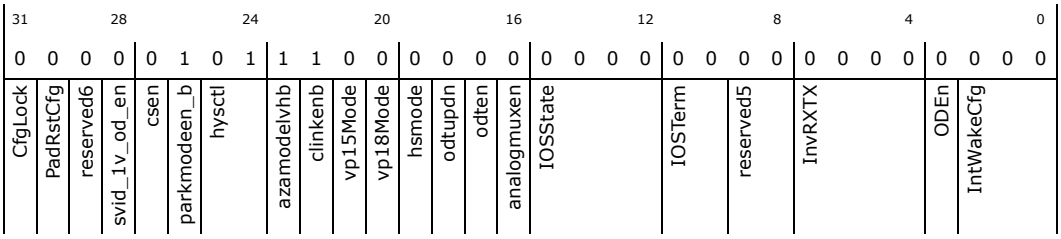
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C04h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.100 Pad Control Register 0 (TCK_PAD_CFG0)—Offset 4C08h

Pad Control Register 0

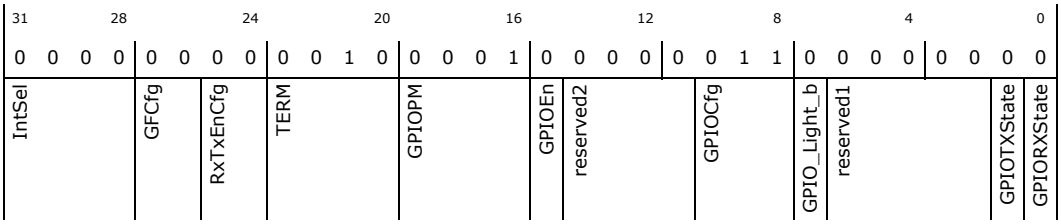
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C08h

Op Codes:
h - Read, h - Write

Default: 00210300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x2 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.101 Pad Control Register 1 (TCK_PAD_CFG1)—Offset 4C0Ch

Pad Control Register 1

Access Method

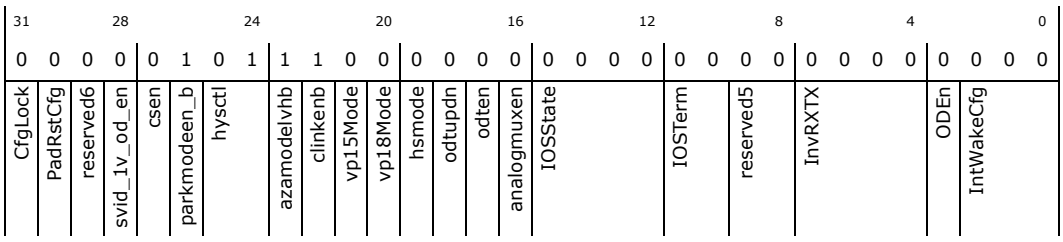
Type: Message Bus Register (Size: 32 bits)

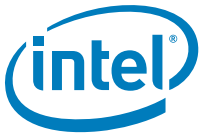
Offset: [Port: 0x13] + 4C0Ch

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.102 Pad Control Register 0 (PROCHOT_B_PAD_CFG0)—Offset 4C10h

Pad Control Register 0

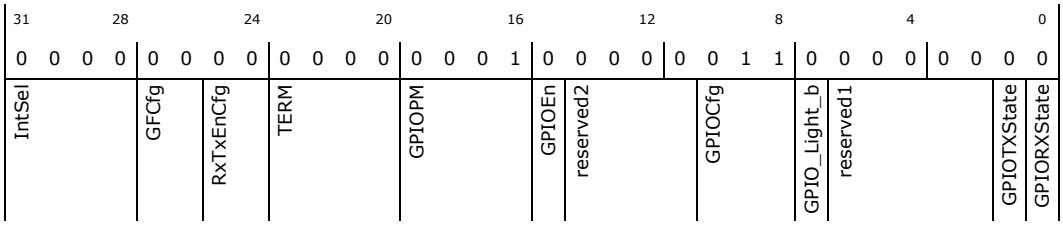
Access Method

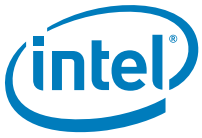
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C10h

Op Codes:
h - Read, h - Write

Default: 00010300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.103 Pad Control Register 1 (PROCHOT_B_PAD_CFG1)—Offset 4C14h

Pad Control Register 1

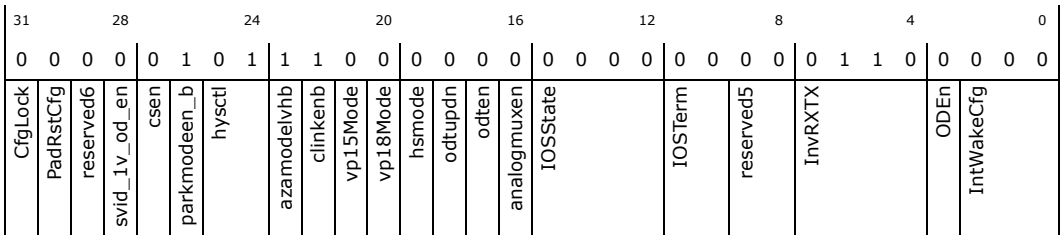
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C14h

Op Codes:
h - Read, h - Write

Default: 05C00060h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x6 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.104 Pad Control Register 0 (SVID0_DATA_PAD_CFG0)—Offset 4C18h

Pad Control Register 0

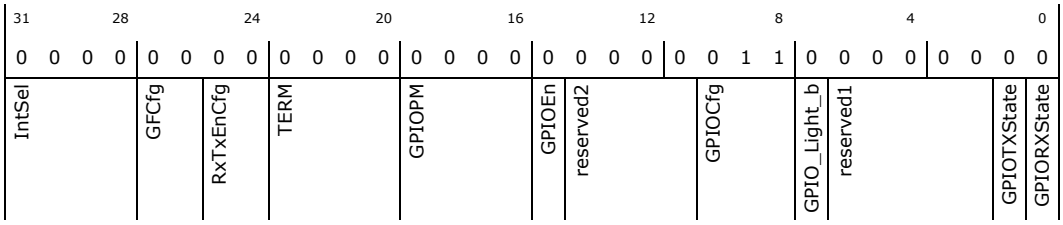
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C18h

Op Codes:
h - Read, h - Write

Default: 00000300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x0 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.105 Pad Control Register 1 (SVID0_DATA_PAD_CFG1)—Offset 4C1Ch

Pad Control Register 1

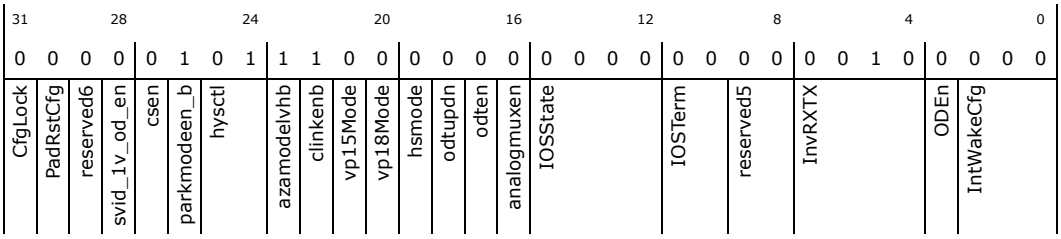
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C1Ch

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x2 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.106 Pad Control Register 0 (TMS_PAD_CFG0)—Offset 4C20h

Pad Control Register 0

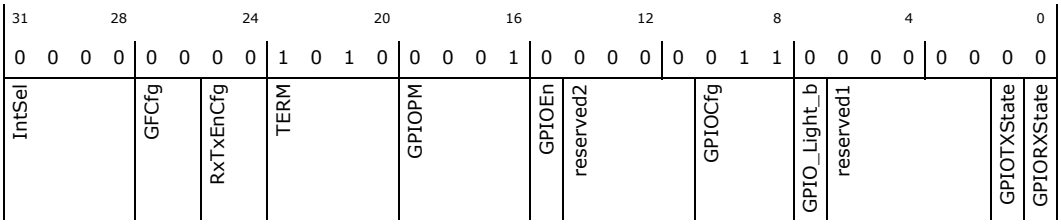
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C20h

Op Codes:
h - Read, h - Write

Default: 00A10300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0xa RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.107 Pad Control Register 1 (TMS_PAD_CFG1)—Offset 4C24h

Pad Control Register 1

Access Method

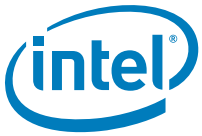
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C24h

Op Codes:
h - Read, h - Write

Default: 05C00000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CfgLock	PadRstCfg	reserved6	svid_1v_od_en	csen	parkmodeen_b	hysctl		azamodelvhb	clinkenb	vp15Mode	vp18Mode	hsmode	odtupdn	odten	analogmuxen	IOSState				IOSTerm			reserved5	InvRXTX				ODEn	IntWakeCfg		



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.108 Pad Control Register 0 (CX_PRDY_B_2_PAD_CFG0)—Offset 4C28h

Pad Control Register 0

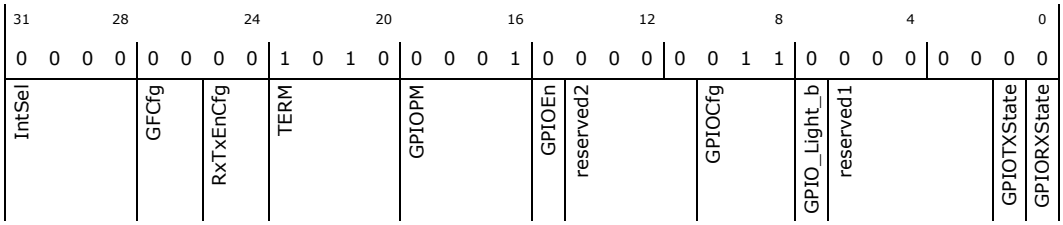
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C28h

Op Codes:
h - Read, h - Write

Default: 00A10300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0xa RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.109 Pad Control Register 1 (CX_PRDY_B_2_PAD_CFG1)—Offset 4C2Ch

Pad Control Register 1

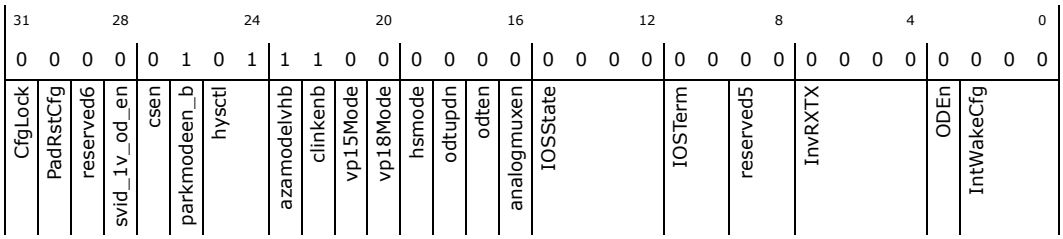
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C2Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.110 Pad Control Register 0 (TDO_2_PAD_CFG0)—Offset 4C30h

Pad Control Register 0

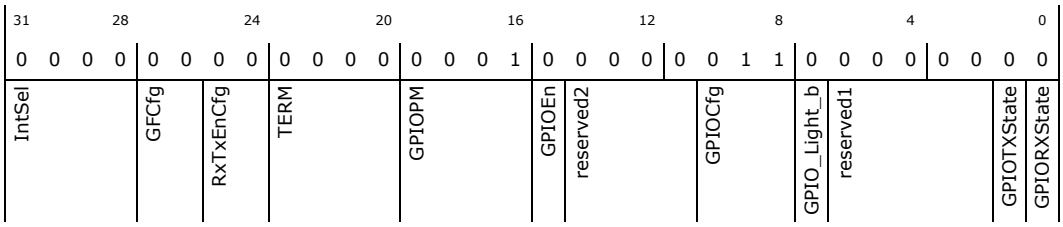
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C30h

Op Codes:
h - Read, h - Write

Default: 00010300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.

Bit Range	Default and Access	Field Name (ID): Description
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.111 Pad Control Register 1 (TDO_2_PAD_CFG1)—Offset 4C34h

Pad Control Register 1

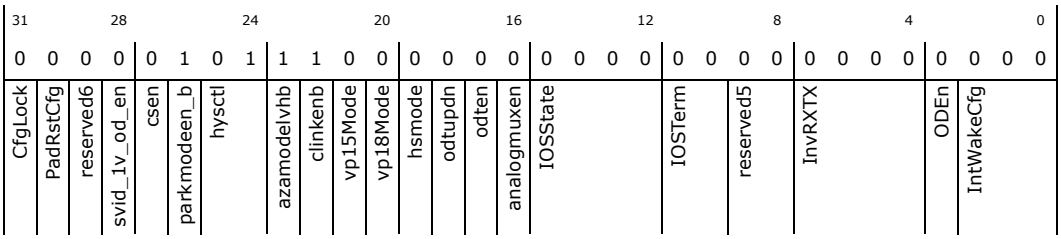
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C34h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC

Bit Range	Default and Access	Field Name (ID): Description
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.112 Pad Control Register 0 (CX_PRDY_B_PAD_CFG0)—Offset 4C38h

Pad Control Register 0

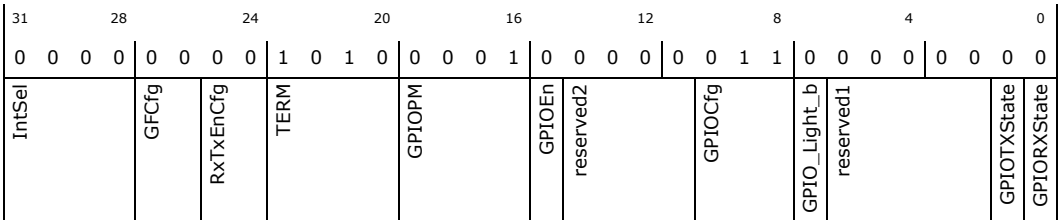
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C38h

Op Codes:
h - Read, h - Write

Default: 00A10300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0xa RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.113 Pad Control Register 1 (CX_PRDY_B_PAD_CFG1)—Offset 4C3Ch

Pad Control Register 1

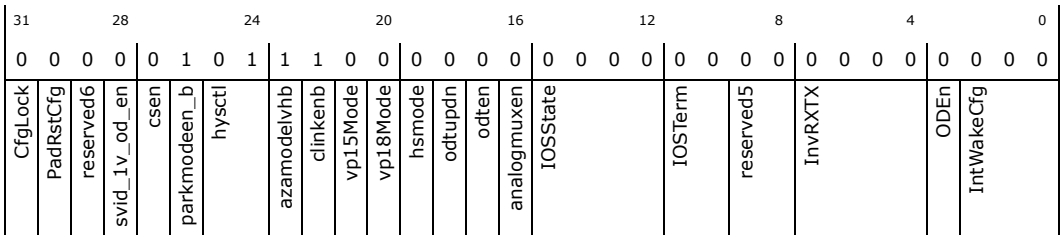
Access Method

Type: Message Bus Register (Size: 32 bits)

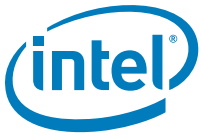
Offset: [Port: 0x13] + 4C3Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6



Bit Range	Default and Access	Field Name (ID): Description
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.114 Pad Control Register 0 (SVID0_ALERT_B_PAD_CFG0)—Offset 4C40h

Pad Control Register 0

Access Method

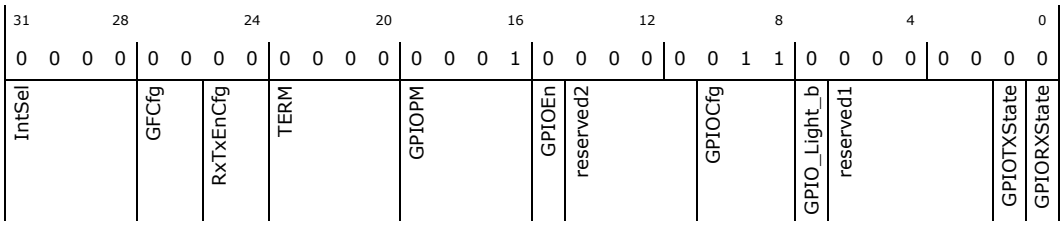
Type: Message Bus Register (Size: 32 bits)

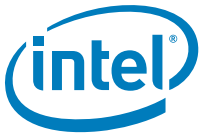
Offset: [Port: 0x13] + 4C40h

Op Codes:

h - Read, h - Write

Default: 00010300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.115 Pad Control Register 1 (SVID0_ALERT_B_PAD_CFG1)—Offset 4C44h

Pad Control Register 1

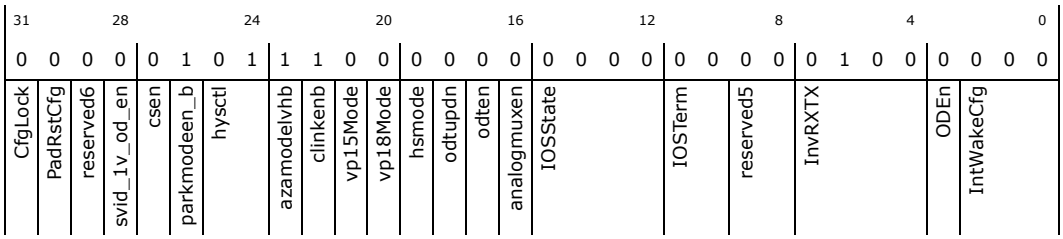
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C44h

Op Codes:
h - Read, h - Write

Default: 05C00040h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x4 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.116 Pad Control Register 0 (TDO_PAD_CFG0)—Offset 4C48h

Pad Control Register 0

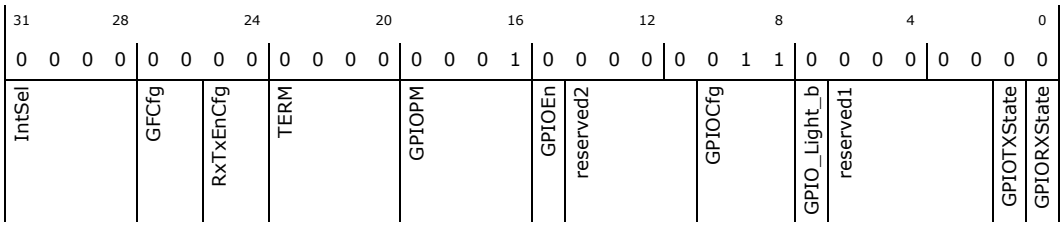
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C48h

Op Codes:
h - Read, h - Write

Default: 00010300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.

Bit Range	Default and Access	Field Name (ID): Description
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.117 Pad Control Register 1 (TDO_PAD_CFG1)—Offset 4C4Ch

Pad Control Register 1

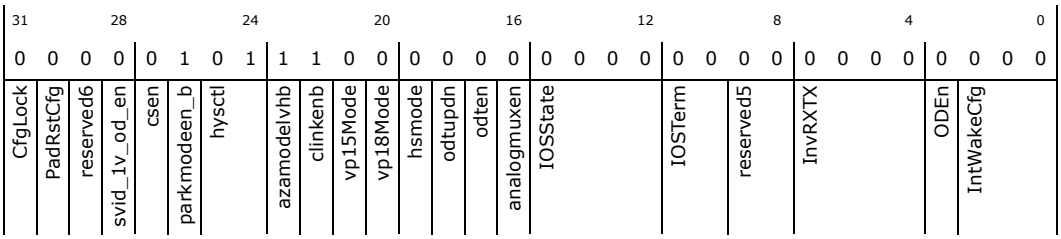
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C4Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC

Bit Range	Default and Access	Field Name (ID): Description
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.118 Pad Control Register 0 (SVID0_CLK_PAD_CFG0)—Offset 4C50h

Pad Control Register 0

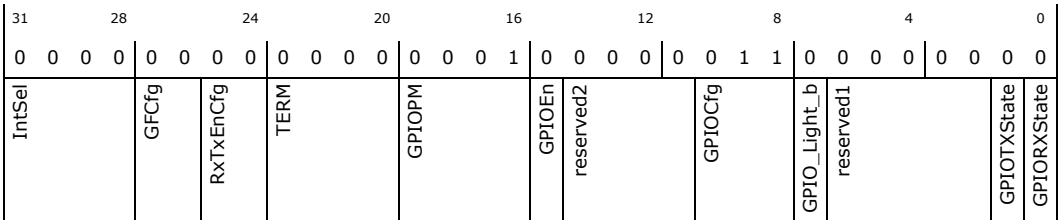
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C50h

Op Codes:
h - Read, h - Write

Default: 00010300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.119 Pad Control Register 1 (SVID0_CLK_PAD_CFG1)—Offset 4C54h

Pad Control Register 1

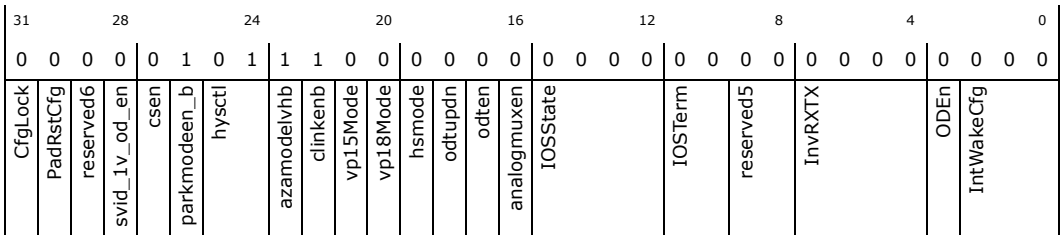
Access Method

Type: Message Bus Register (Size: 32 bits)

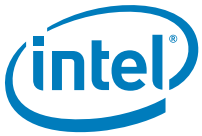
Offset: [Port: 0x13] + 4C54h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6



Bit Range	Default and Access	Field Name (ID): Description
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.120 Pad Control Register 0 (TDI_PAD_CFG0)—Offset 4C58h

Pad Control Register 0

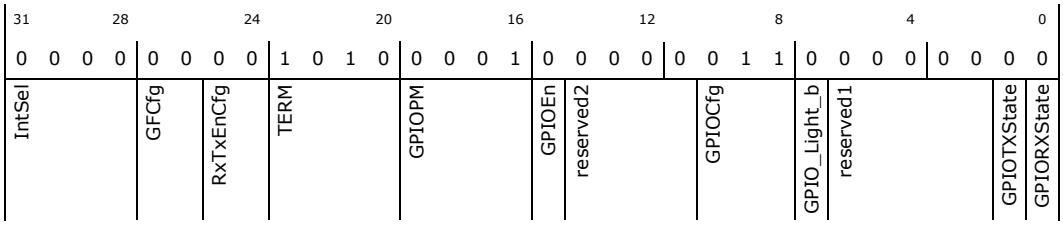
Access Method

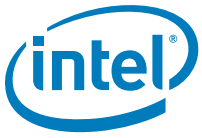
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C58h

Op Codes:
h - Read, h - Write

Default: 00A10300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0xa RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.121 Pad Control Register 1 (TDI_PAD_CFG1)—Offset 4C5Ch

Pad Control Register 1

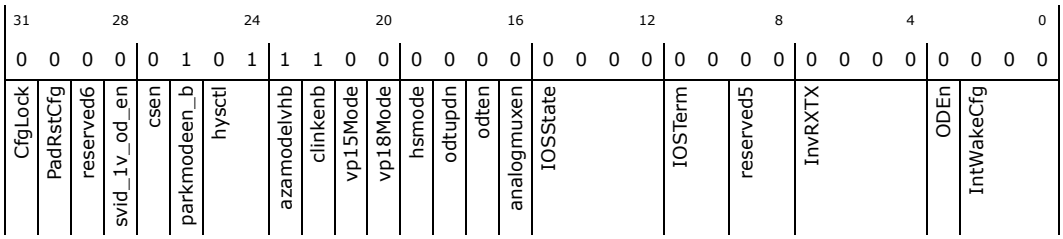
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 4C5Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.122 Pad Control Register 0 (GP_CAMERASB05_PAD_CFG0)—Offset 5000h

Pad Control Register 0

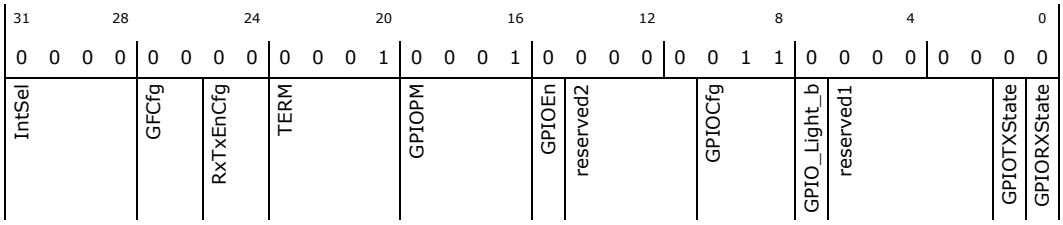
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5000h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.123 Pad Control Register 1 (GP_CAMERASB05_PAD_CFG1)—Offset 5004h

Pad Control Register 1

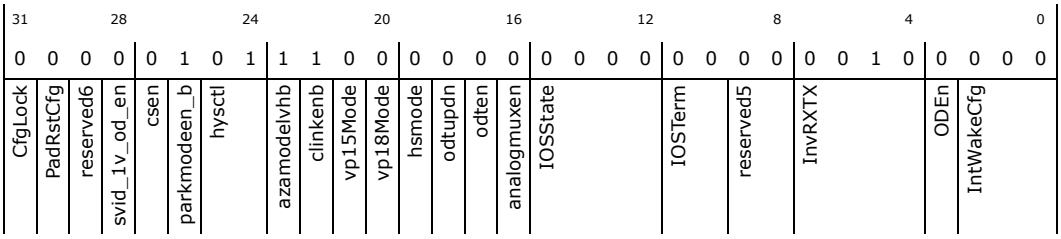
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5004h

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.124 Pad Control Register 0 (GP_CAMERASB02_PAD_CFG0)—Offset 5008h

Pad Control Register 0

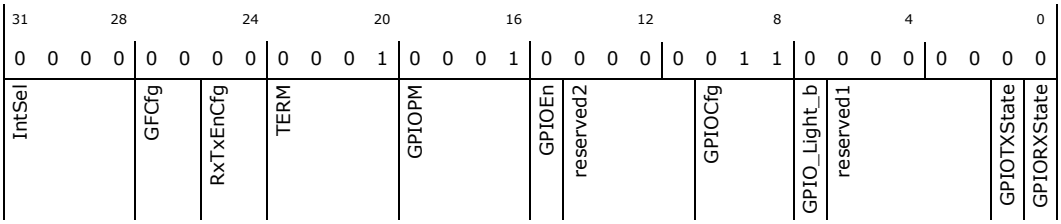
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5008h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.125 Pad Control Register 1 (GP_CAMERASB02_PAD_CFG1)—Offset 500Ch

Pad Control Register 1

Access Method

Type: Message Bus Register (Size: 32 bits)

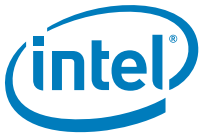
Offset: [Port: 0x13] + 500Ch

Op Codes:

h - Read, h - Write

Default: 05C00020h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
CfgLock	PadRstCfg	reserved6	svid_1v_od_en	csen	parkmodeen_b	hysctl		azamodelvhb	clinkenb	vp15Mode	vp18Mode	hsmode	odtupdn	odten	analogmuxen	IOSState				IOSTerm		reserved5		InvRXTX				ODEn	IntWakeCfg		



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x2 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.126 Pad Control Register 0 (GP_CAMERASB08_PAD_CFG0)—Offset 5010h

Pad Control Register 0

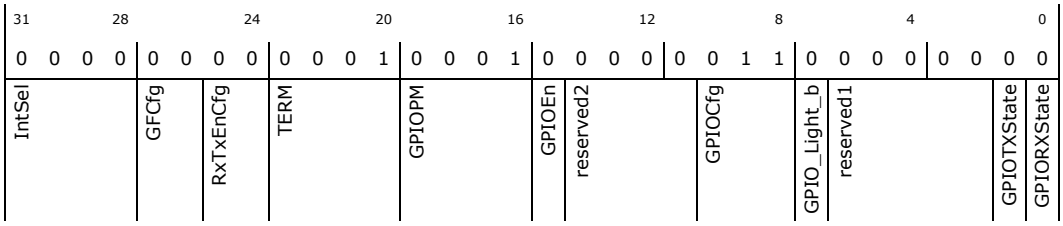
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5010h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.127 Pad Control Register 1 (GP_CAMERASB08_PAD_CFG1)—Offset 5014h

Pad Control Register 1

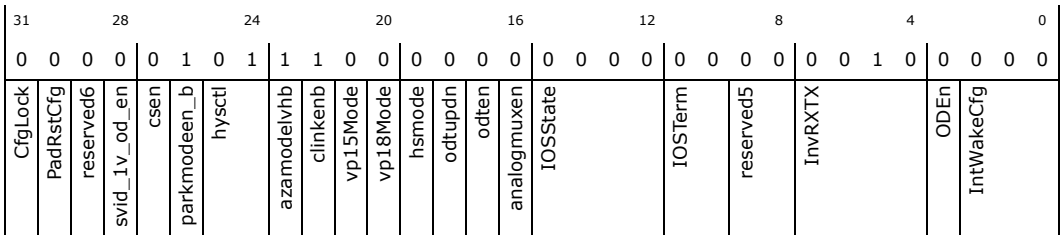
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5014h

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x2 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.128 Pad Control Register 0 (GP_CAMERASB00_PAD_CFG0)—Offset 5018h

Pad Control Register 0

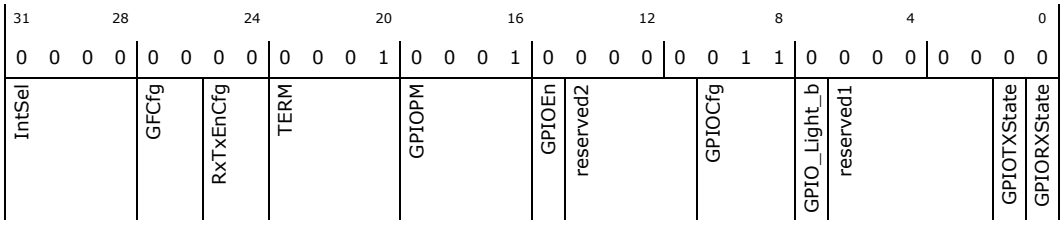
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5018h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.129 Pad Control Register 1 (GP_CAMERASB00_PAD_CFG1)—Offset 501Ch

Pad Control Register 1

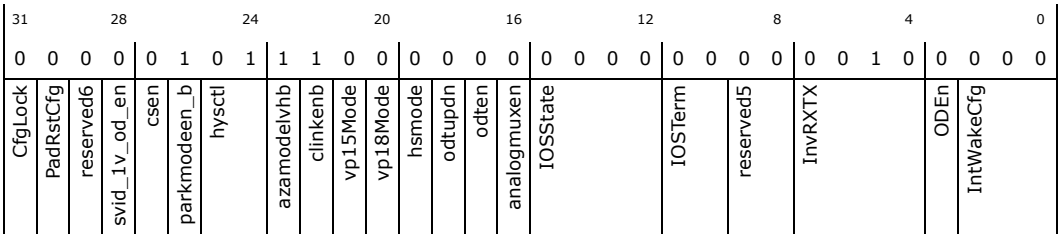
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 501Ch

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x2 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.130 Pad Control Register 0 (GP_CAMERASB06_PAD_CFG0)—Offset 5020h

Pad Control Register 0

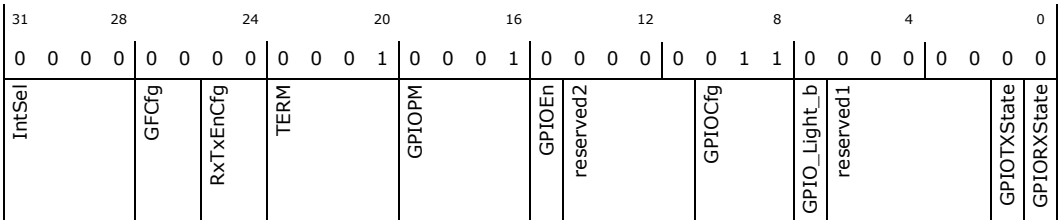
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5020h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.131 Pad Control Register 1 (GP_CAMERASB06_PAD_CFG1)—Offset 5024h

Pad Control Register 1

Access Method

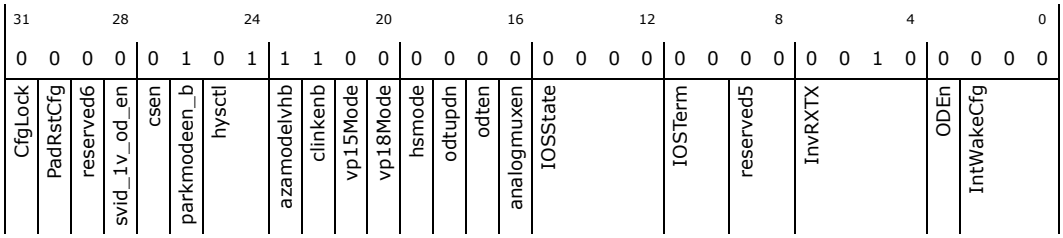
Type: Message Bus Register (Size: 32 bits)

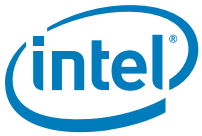
Offset: [Port: 0x13] + 5024h

Op Codes:

h - Read, h - Write

Default: 05C00020h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x2 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.132 Pad Control Register 0 (GP_CAMERASB10_PAD_CFG0)—Offset 5028h

Pad Control Register 0

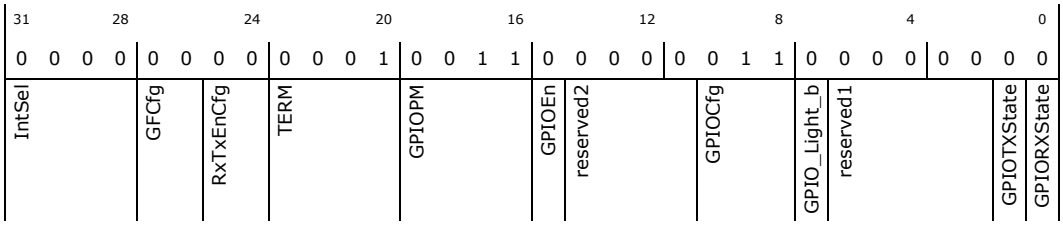
Access Method

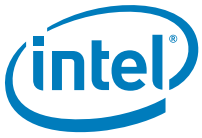
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5028h

Op Codes:
h - Read, h - Write

Default: 00130300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x3 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.133 Pad Control Register 1 (GP_CAMERASB10_PAD_CFG1)—Offset 502Ch

Pad Control Register 1

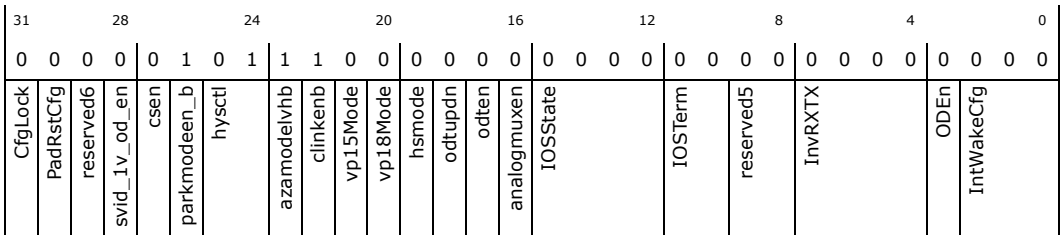
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 502Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.134 Pad Control Register 0 (GP_CAMERASB03_PAD_CFG0)—Offset 5030h

Pad Control Register 0

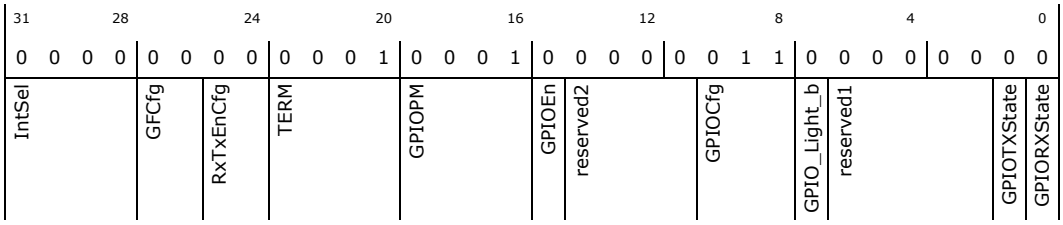
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5030h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.135 Pad Control Register 1 (GP_CAMERASB03_PAD_CFG1)—Offset 5034h

Pad Control Register 1

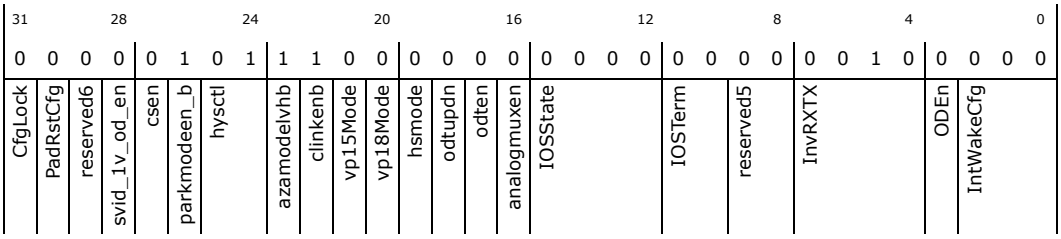
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5034h

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x2 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.136 Pad Control Register 0 (GP_CAMERASB09_PAD_CFG0)—Offset 5038h

Pad Control Register 0

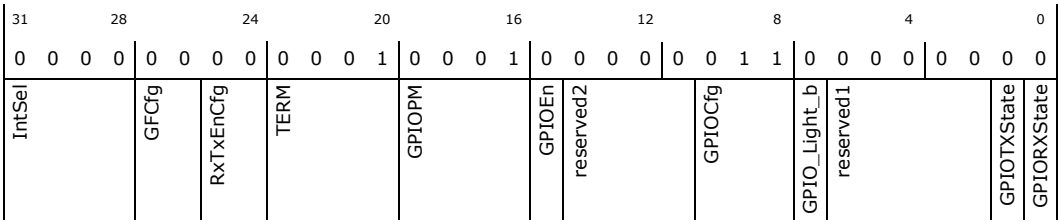
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5038h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.137 Pad Control Register 1 (GP_CAMERASB09_PAD_CFG1)—Offset 503Ch

Pad Control Register 1

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 503Ch

Op Codes:

h - Read, h - Write

Default: 05C00020h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
CfgLock	PadRstCfg	reserved6	svid_1v_od_en	csen	parkmodeen_b	hysctl		azamodelvhb	clinkenb	vp15Mode	vp18Mode	hsmode	odtupdn	odten	analogmuxen	IOSState				IOSTerm		reserved5		InvRXTX				ODEn	IntWakeCfg		

Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x2 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.138 Pad Control Register 0 (GP_CAMERASB01_PAD_CFG0)—Offset 5040h

Pad Control Register 0

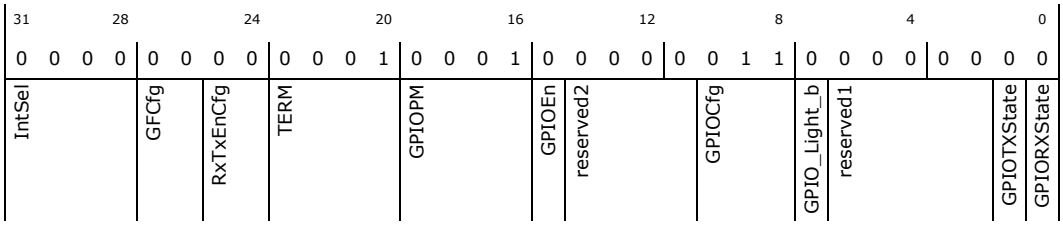
Access Method

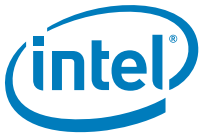
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5040h

Op Codes:
h - Read, h - Write

Default: 00110300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.139 Pad Control Register 1 (GP_CAMERASB01_PAD_CFG1)—Offset 5044h

Pad Control Register 1

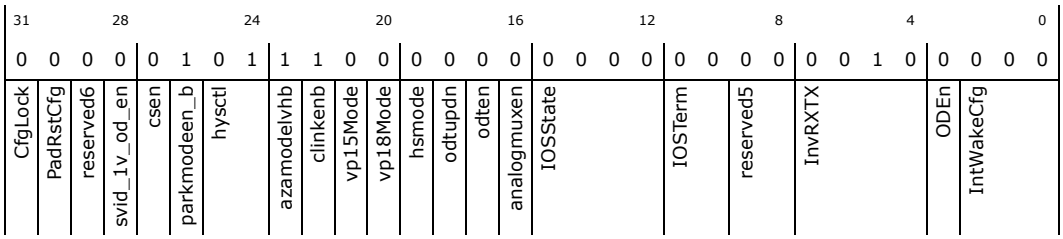
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5044h

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.140 Pad Control Register 0 (GP_CAMERASB07_PAD_CFG0)—Offset 5048h

Pad Control Register 0

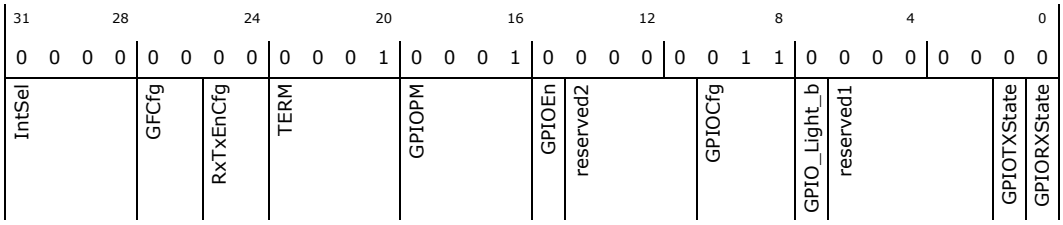
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5048h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.141 Pad Control Register 1 (GP_CAMERASB07_PAD_CFG1)—Offset 504Ch

Pad Control Register 1

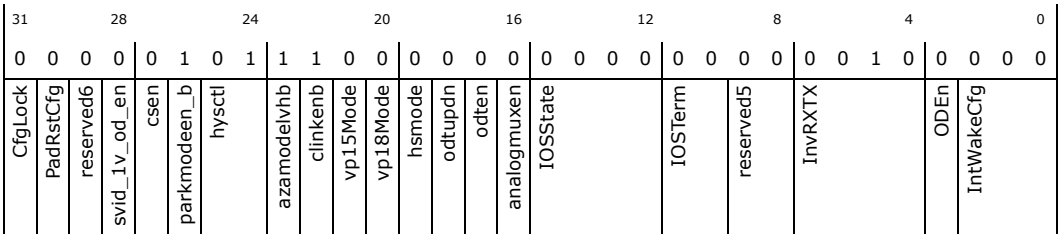
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 504Ch

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x2 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.142 Pad Control Register 0 (GP_CAMERASB11_PAD_CFG0)—Offset 5050h

Pad Control Register 0

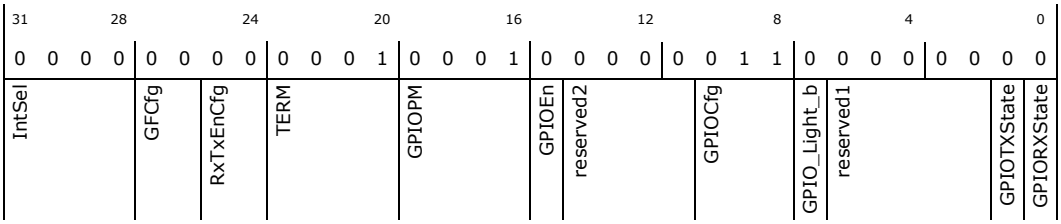
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5050h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.143 Pad Control Register 1 (GP_CAMERASB11_PAD_CFG1)—Offset 5054h

Pad Control Register 1

Access Method

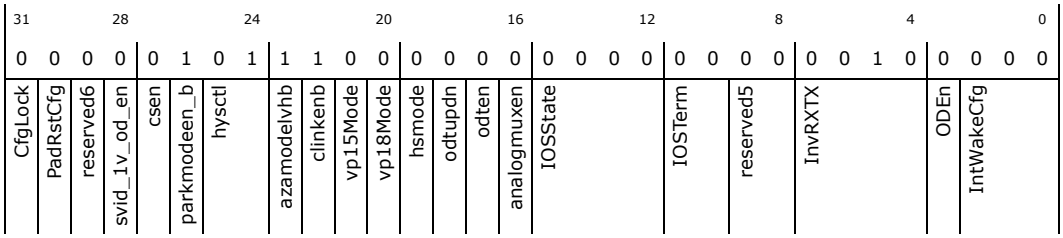
Type: Message Bus Register (Size: 32 bits)

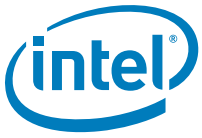
Offset: [Port: 0x13] + 5054h

Op Codes:

h - Read, h - Write

Default: 05C00020h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x2 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.144 Pad Control Register 0 (GP_CAMERASB04_PAD_CFG0)—Offset 5058h

Pad Control Register 0

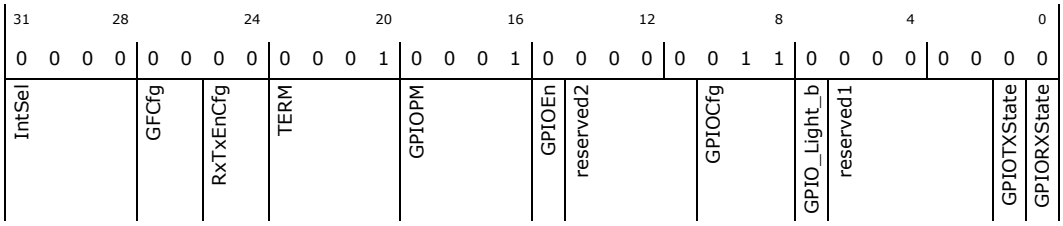
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5058h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.145 Pad Control Register 1 (GP_CAMERASB04_PAD_CFG1)—Offset 505Ch

Pad Control Register 1

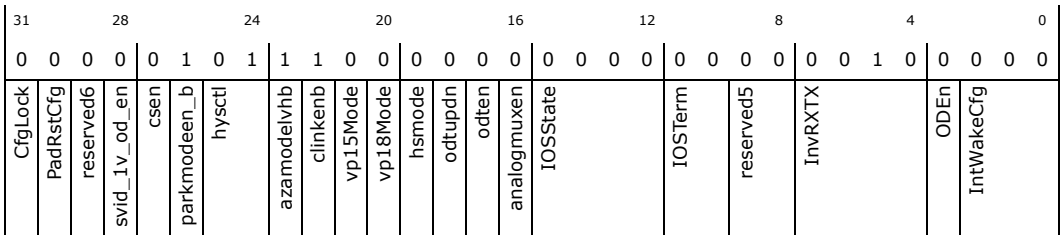
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 505Ch

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x2 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.146 Pad Control Register 0 (PANEL0_BKLTEN_PAD_CFG0)—Offset 5400h

Pad Control Register 0

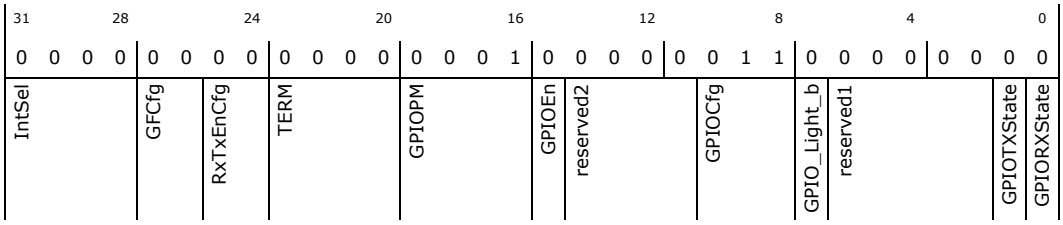
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5400h

Op Codes:
h - Read, h - Write

Default: 00010300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.147 Pad Control Register 1 (PANEL0_BKLTEN_PAD_CFG1)—Offset 5404h

Pad Control Register 1

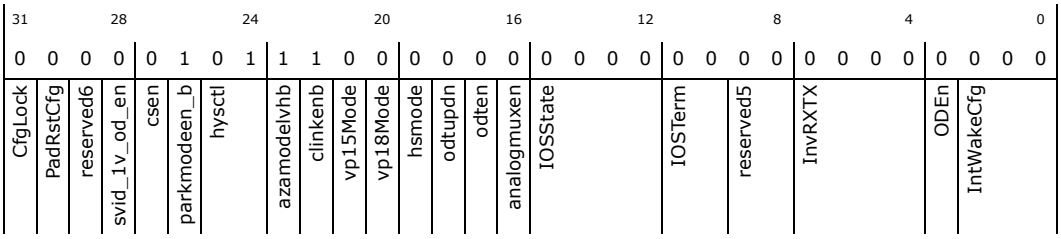
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5404h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.148 Pad Control Register 0 (HV_DDI0_HPD_PAD_CFG0)—Offset 5408h

Pad Control Register 0

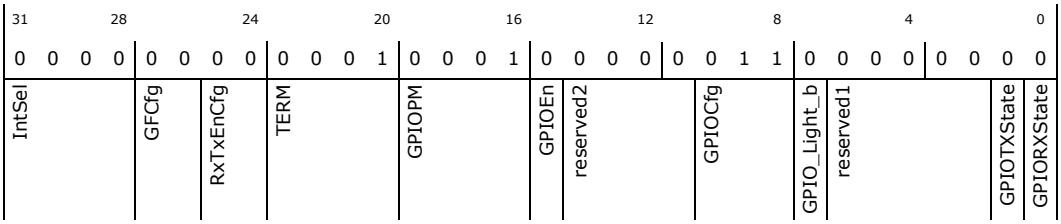
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5408h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.149 Pad Control Register 1 (HV_DDI0_HPD_PAD_CFG1)—Offset 540Ch

Pad Control Register 1

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 540Ch

Op Codes:

h - Read, h - Write

Default: 05C00020h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
CfgLock	PadRstCfg	reserved6	svid_1v_od_en	csen	parkmodeen_b	hysctl		azamodelvhb	clinkenb	vp15Mode	vp18Mode	hsmode	odtupdn	odten	analogmuxen	IOSState				IOSTerm			reserved5	InvRXTX				ODEn	IntWakeCfg		

Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x2 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.150 Pad Control Register 0 (HV_DDI2_DDC_SDA_PAD_CFG0)—Offset 5410h

Pad Control Register 0

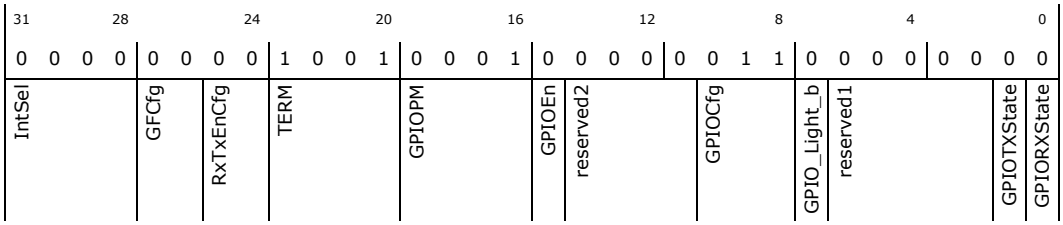
Access Method

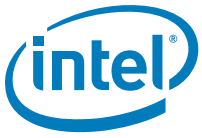
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5410h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.151 Pad Control Register 1 (HV_DDI2_DDC_SDA_PAD_CFG1)—Offset 5414h

Pad Control Register 1

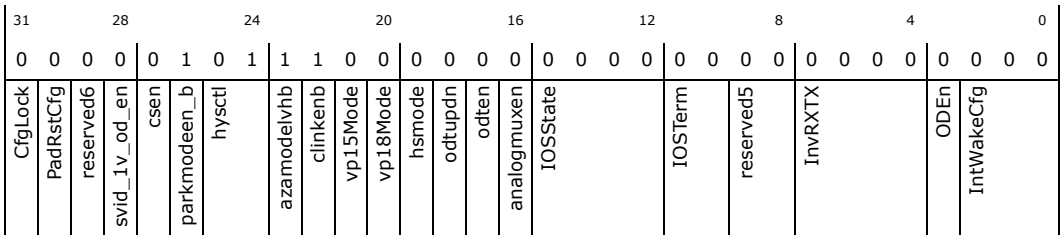
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5414h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.152 Pad Control Register 0 (PANEL1_BKLTCTL_PAD_CFG0)—Offset 5418h

Pad Control Register 0

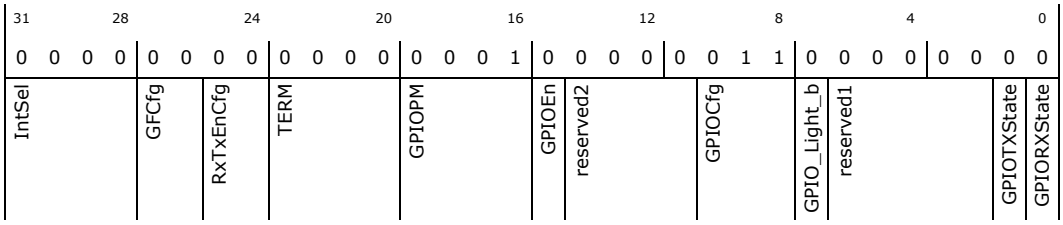
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5418h

Op Codes:
h - Read, h - Write

Default: 00010300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.153 Pad Control Register 1 (PANEL1_BKLTCTL_PAD_CFG1)—Offset 541Ch

Pad Control Register 1

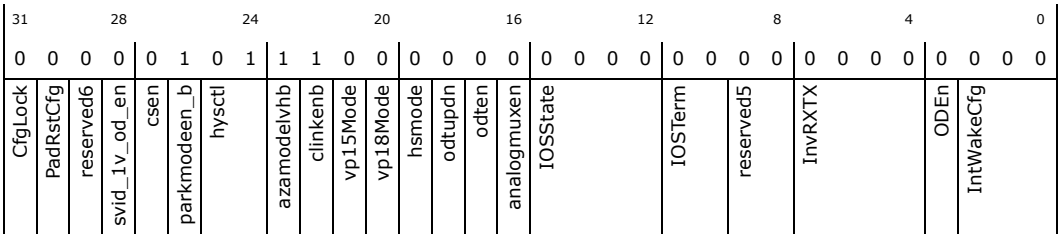
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 541Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.154 Pad Control Register 0 (HV_DDI1_HPD_PAD_CFG0)—Offset 5420h

Pad Control Register 0

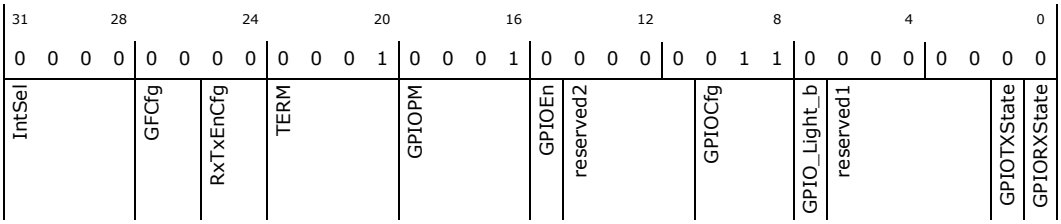
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5420h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.155 Pad Control Register 1 (HV_DDI1_HPD_PAD_CFG1)—Offset 5424h

Pad Control Register 1

Access Method

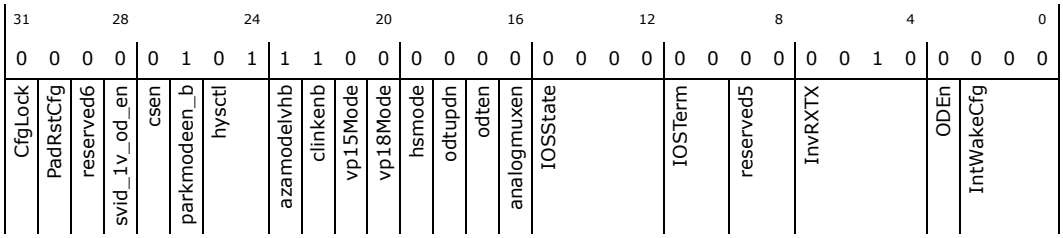
Type: Message Bus Register (Size: 32 bits)

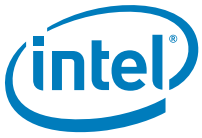
Offset: [Port: 0x13] + 5424h

Op Codes:

h - Read, h - Write

Default: 05C00020h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x2 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.156 Pad Control Register 0 (PANEL0_BKLTCTL_PAD_CFG0)—Offset 5428h

Pad Control Register 0

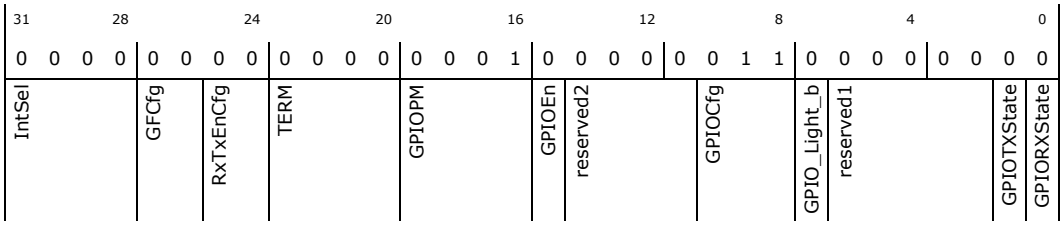
Access Method

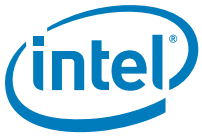
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5428h

Op Codes:
h - Read, h - Write

Default: 00010300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.157 Pad Control Register 1 (PANEL0_BKLTCTL_PAD_CFG1)—Offset 542Ch

Pad Control Register 1

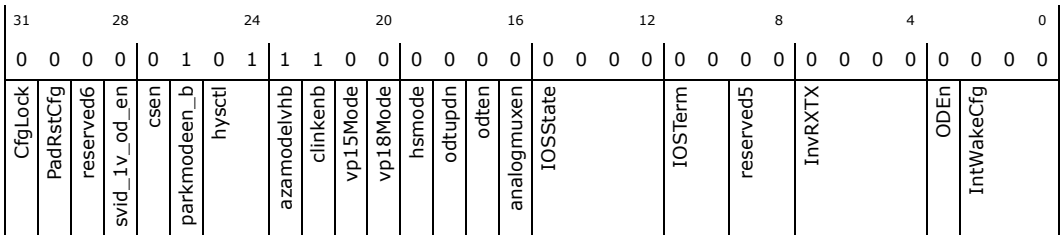
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 542Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.158 Pad Control Register 0 (HV_DDI0_DDC_SDA_PAD_CFG0)—Offset 5430h

Pad Control Register 0

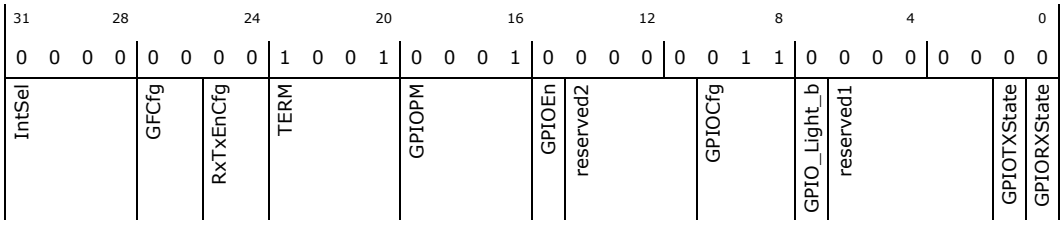
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5430h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.159 Pad Control Register 1 (HV_DDI0_DDC_SDA_PAD_CFG1)—Offset 5434h

Pad Control Register 1

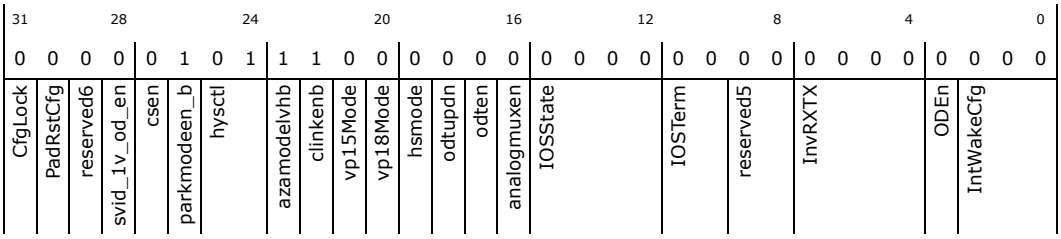
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5434h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.160 Pad Control Register 0 (HV_DDI2_DDC_SCL_PAD_CFG0)—Offset 5438h

Pad Control Register 0

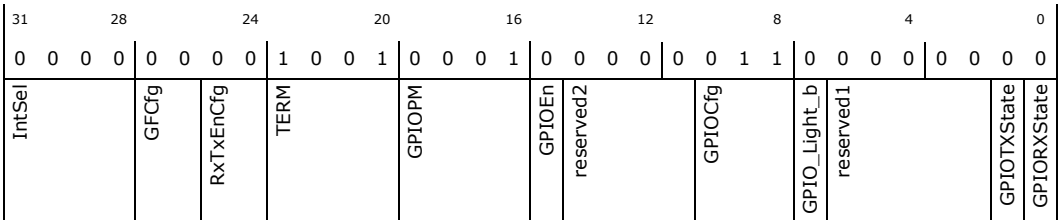
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5438h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.161 Pad Control Register 1 (HV_DDI2_DDC_SCL_PAD_CFG1)—Offset 543Ch

Pad Control Register 1

Access Method

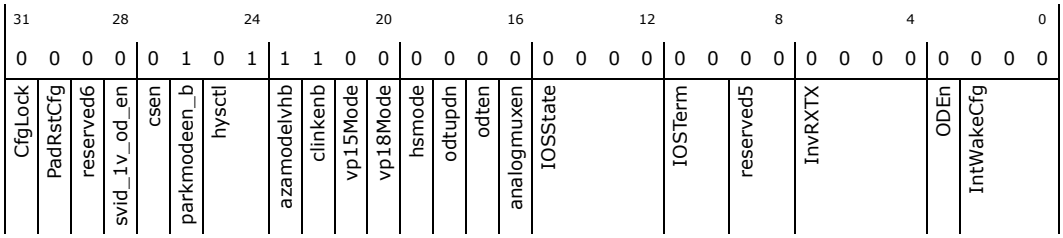
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 543Ch

Op Codes:

h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.162 Pad Control Register 0 (HV_DDI2_HPD_PAD_CFG0)—Offset 5440h

Pad Control Register 0

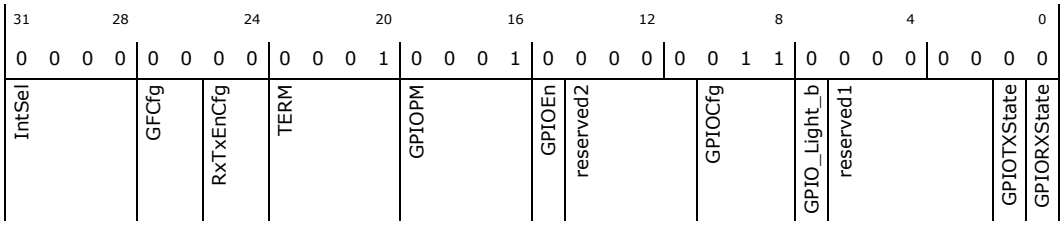
Access Method

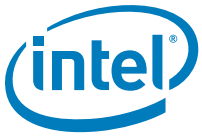
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5440h

Op Codes:
h - Read, h - Write

Default: 00110300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.163 Pad Control Register 1 (HV_DDI2_HPD_PAD_CFG1)—Offset 5444h

Pad Control Register 1

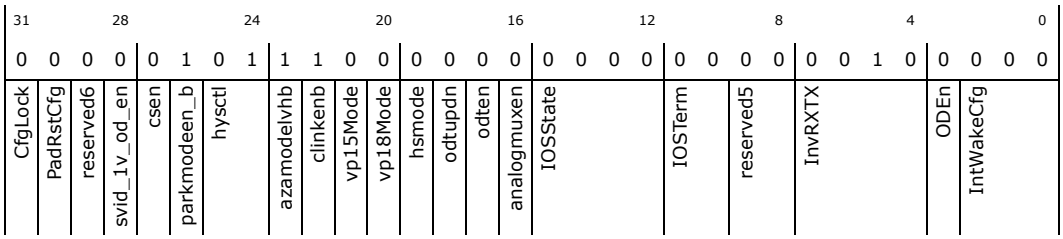
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5444h

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x2 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.164 Pad Control Register 0 (PANEL1_VDDEN_PAD_CFG0)—Offset 5448h

Pad Control Register 0

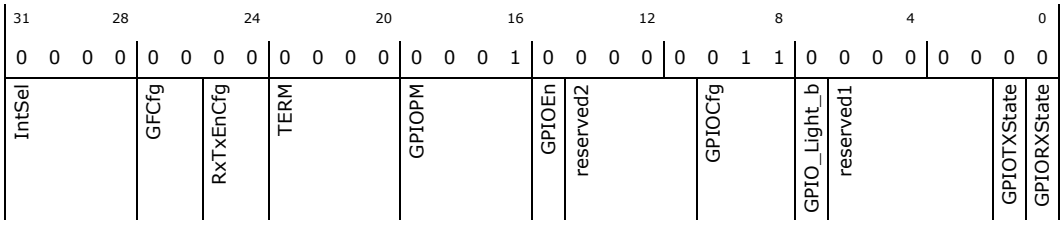
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5448h

Op Codes:
h - Read, h - Write

Default: 00010300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.165 Pad Control Register 1 (PANEL1_VDDEN_PAD_CFG1)—Offset 544Ch

Pad Control Register 1

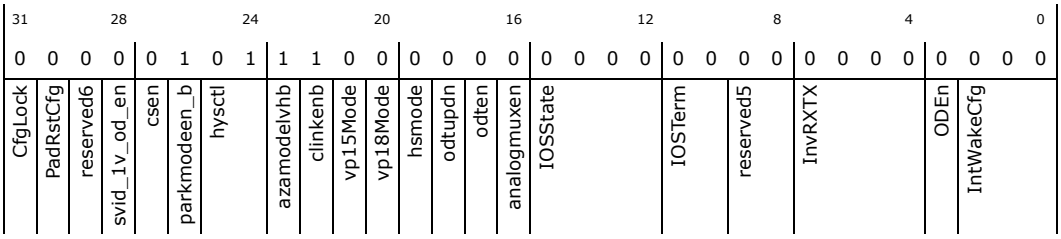
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 544Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.166 Pad Control Register 0 (PANEL1_BKLTEN_PAD_CFG0)—Offset 5450h

Pad Control Register 0

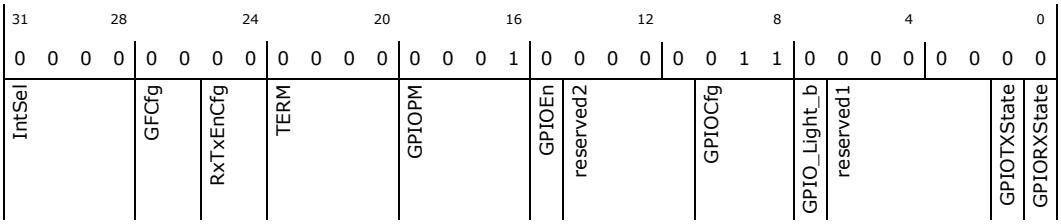
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5450h

Op Codes:
h - Read, h - Write

Default: 00010300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.167 Pad Control Register 1 (PANEL1_BKLTEN_PAD_CFG1)—Offset 5454h

Pad Control Register 1

Access Method

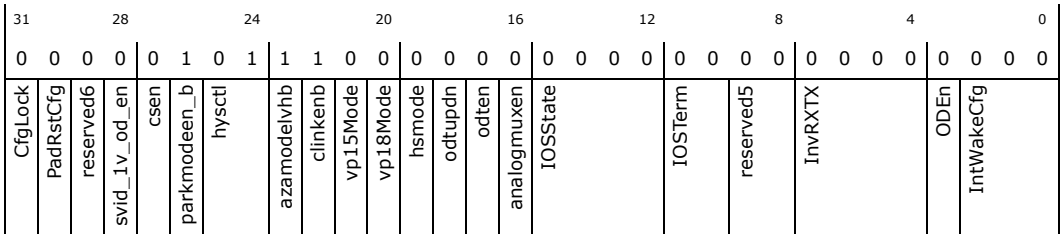
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5454h

Op Codes:

h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.168 Pad Control Register 0 (HV_DDI0_DDC_SCL_PAD_CFG0)—Offset 5458h

Pad Control Register 0

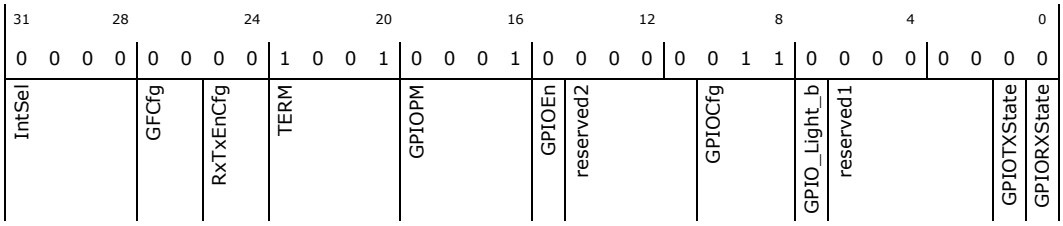
Access Method

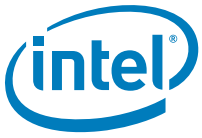
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5458h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.169 Pad Control Register 1 (HV_DDI0_DDC_SCL_PAD_CFG1)—Offset 545Ch

Pad Control Register 1

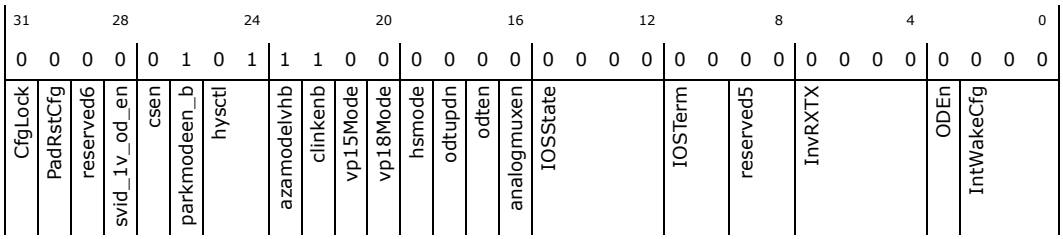
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 545Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.5.170 Pad Control Register 0 (PANEL0_VDDEN_PAD_CFG0)—Offset 5460h

Pad Control Register 0

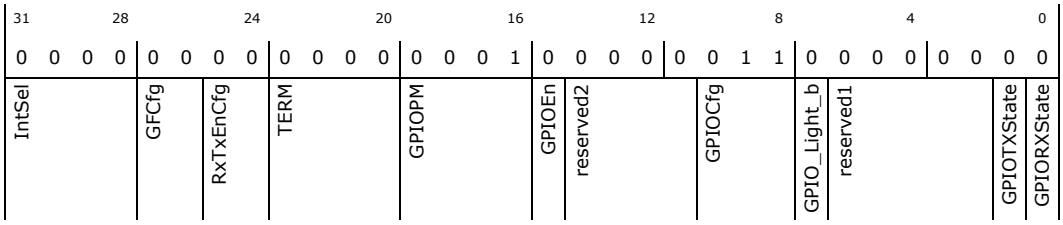
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5460h

Op Codes:
h - Read, h - Write

Default: 00010300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.5.171 Pad Control Register 1 (PANEL0_VDDEN_PAD_CFG1)—Offset 5464h

Pad Control Register 1

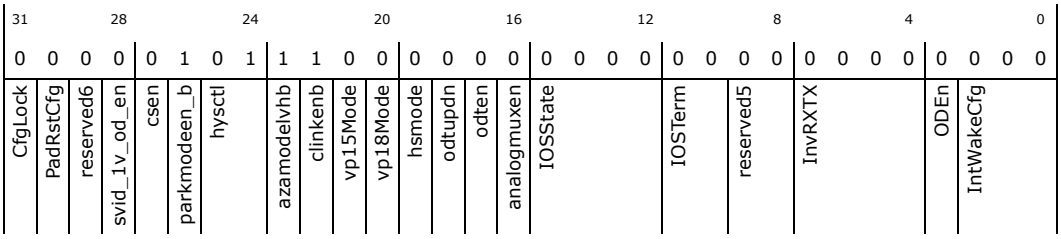
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x13] + 5464h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6 Summary of GPIO SOUTHEAST Message Bus Registers

Table 10-101.Summary of GPIO SouthEast Message Bus Registers—0x48

Offset	Register Name (Register Symbol)	Default Value
0–3h	"GPIO Read Access Control (gpio_read_access_policy_access_reg)—Offset 0h" on page 5153	FFFFFFFFh
4–7h	"GPIO Read Access Control (gpio_read_access_policy_wake_reg)—Offset 4h" on page 5153	FFFFFFFFh
8–Bh	"GPIO Read Access Control (gpio_read_access_policy_interrupt_reg)—Offset 8h" on page 5154	FFFFFFFFh
C–Fh	"GPIO Read Access Control (gpio_read_access_policy_community_reg)—Offset Ch" on page 5154	FFFFFFFFh
10–13h	"GPIO Read Access Control (gpio_read_access_policy_family_broadcast_reg)—Offset 10h" on page 5155	FFFFFFFFh
14–17h	"GPIO Read Access Control (gpio_read_access_policy_family_reg)—Offset 14h" on page 5155	FFFFFFFFh
18–1Bh	"GPIO Read Access Control (gpio_read_access_policy_pad_broadcast_reg)—Offset 18h" on page 5156	FFFFFFFFh
1C–1Fh	"GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_2x3_8_2_regs)—Offset 1Ch" on page 5157	FFFFFFFFh
20–23h	"GPIO Read Access Control (gpio_read_access_policy_ulphsmvfamily_3x3_rcomp_13_0_regs)—Offset 20h" on page 5157	FFFFFFFFh
24–27h	"GPIO Read Access Control (gpio_read_access_policy_hshvfamily_2x3_rcomp_7_0_regs)—Offset 24h" on page 5158	FFFFFFFFh
28–2Bh	"GPIO Read Access Control (gpio_read_access_policy_hshvfamily_3x3_rcomp_9_0_regs)—Offset 28h" on page 5158	FFFFFFFFh
2C–2Fh	"GPIO Read Access Control (gpio_read_access_policy_ulphsmvfamily_3x3_10_0_regs)—Offset 2Ch" on page 5159	FFFFFFFFh
30–33h	"GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_3x3_11_0_regs)—Offset 30h" on page 5159	FFFFFFFFh
100–103h	"GPIO Write Access Control (gpio_write_access_policy_access_reg)—Offset 100h" on page 5160	FFFFFFFFh
104–107h	"GPIO Write Access Control (gpio_write_access_policy_wake_reg)—Offset 104h" on page 5160	FFFFFFFFh
108–10Bh	"GPIO Write Access Control (gpio_write_access_policy_interrupt_reg)—Offset 108h" on page 5161	FFFFFFFFh
10C–10Fh	"GPIO Write Access Control (gpio_write_access_policy_community_reg)—Offset 10Ch" on page 5162	FFFFFFFFh
110–113h	"GPIO Write Access Control (gpio_write_access_policy_family_broadcast_reg)—Offset 110h" on page 5162	FFFFFFFFh
114–117h	"GPIO Write Access Control (gpio_write_access_policy_family_reg)—Offset 114h" on page 5163	FFFFFFFFh

Table 10-101.Summary of GPIO SouthEast Message Bus Registers—0x48 (Continued)

Offset	Register Name (Register Symbol)	Default Value
118–11Bh	"GPIO Write Access Control (gpio_write_access_policy_pad_broadcast_reg)—Offset 118h" on page 5163	FFFFFFFFh
11C–11Fh	"GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_2x3_8_2_regs)—Offset 11Ch" on page 5164	FFFFFFFFh
120–123h	"GPIO Write Access Control (gpio_write_access_policy_ulphsmvfamily_3x3_rcomp_13_0_regs)—Offset 120h" on page 5164	FFFFFFFFh
124–127h	"GPIO Write Access Control (gpio_write_access_policy_hshvfamily_2x3_rcomp_7_0_regs)—Offset 124h" on page 5165	FFFFFFFFh
128–12Bh	"GPIO Write Access Control (gpio_write_access_policy_hshvfamily_3x3_rcomp_9_0_regs)—Offset 128h" on page 5166	FFFFFFFFh
12C–12Fh	"GPIO Write Access Control (gpio_write_access_policy_ulphsmvfamily_3x3_10_0_regs)—Offset 12Ch" on page 5166	FFFFFFFFh
130–133h	"GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_3x3_11_0_regs)—Offset 130h" on page 5167	FFFFFFFFh
200–203h	"GPIO_WAKE_STATUS_REG #0 (gpio_wake_status_reg_0)—Offset 200h" on page 5167	00000000h
204–207h	"GPIO_WAKE_STATUS_REG #1 (gpio_wake_status_reg_1)—Offset 204h" on page 5169	00000000h
280–283h	"GPIO_WAKE_MASK_REG #0 (gpio_wake_mask_reg_0)—Offset 280h" on page 5171	00000000h
284–287h	"GPIO_WAKE_MASK_REG #1 (gpio_wake_mask_reg_1)—Offset 284h" on page 5173	00000000h
300–303h	"GPIO Interrupt Status (gpio_interrupt_status)—Offset 300h" on page 5175	00000000h
380–383h	"GPIO Interrupt Status (gpio_interrupt_mask)—Offset 380h" on page 5175	00000000h
600–603h	"Slave Delay Line Override Register (slave_delay_line_override)—Offset 600h" on page 5176	00000000h
604–607h	"SDR104 Mode Output Delay Selects (sdr104_mode_output_delay_selects)—Offset 604h" on page 5177	00000000h
608–60Bh	"SDR50 Mode Output Delay Selects (sdr50_mode_output_delay_selects)—Offset 608h" on page 5178	00000000h
60C–60Fh	"DDR50 Mode Output Delay Selects (ddr50_mode_output_delay_selects)—Offset 60Ch" on page 5179	00000000h
610–613h	"High Speed Mode Output Delay Selects (hs_mode_output_delay_selects)—Offset 610h" on page 5180	00000000h
614–617h	"Normal Mode Output Delay Selects (normal_mode_output_delay_selects)—Offset 614h" on page 5181	00000000h
618–61Bh	"Master Delay Line Override Register (master_delay_line_override)—Offset 618h" on page 5182	00000000h
61C–61Fh	"Master DLL Status Register (master_dll_status)—Offset 61Ch" on page 5184	00000000h
620–623h	"Master DLL Control Register (master_dll_control)—Offset 620h" on page 5185	00000000h
624–627h	"e-MMC* Interface Receive Delay Select Register (emmc_interface_receive_delay_select)—Offset 624h" on page 5186	00000000h
628–62Bh	"SDIO Interface Receive Delay Select Register (sdio_interface_receive_delay_select)—Offset 628h" on page 5187	00000000h
62C–62Fh	"SD Interface Receive Delay Select Register (sd_interface_receive_delay_select)—Offset 62Ch" on page 5188	00000000h
1000–1003h	"GPIO Broadcast Data Mask bit Register (gpio_family_bw_mask_31_0)—Offset 1000h" on page 5190	00000000h
1004–1007h	"GPIO Broadcast Data Register (gpio_family_bw_data_31_0)—Offset 1004h" on page 5190	00000000h
1008–100Bh	"gpio_family_broadcast_reg_mask #0 (gpio_family_broadcast_reg_mask_0)—Offset 1008h" on page 5191	00000000h

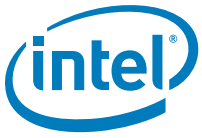


Table 10-101.Summary of GPIO SouthEast Message Bus Registers—0x48 (Continued)

Offset	Register Name (Register Symbol)	Default Value
100C–100Fh	"gpio_family_broadcast_reg_mask #1 (gpio_family_broadcast_reg_mask_1)—Offset 100Ch" on page 5193	00000000h
1090–1093h	"family_config_rcomp_reg (ulpmsmvfamily_2x3_8_2_family_config_rcomp_reg)—Offset 1090h" on page 5194	02020311h
1094–1097h	"gpio_family_configuration_register (ulpmsmvfamily_2x3_8_2_family_config_reg)—Offset 1094h" on page 5195	05C00000h
1100–1103h	"RCOMP Control Register (ulphsmvfamily_3x3_rcomp_13_0_family_rcomp_control_reg)—Offset 1100h" on page 5197	00D41D1Dh
1104–1107h	"RCOMP Offset Register (ulphsmvfamily_3x3_rcomp_13_0_family_rcomp_offset_reg)—Offset 1104h" on page 5198	00000000h
1108–110Bh	"RCOMP Override Register (ulphsmvfamily_3x3_rcomp_13_0_family_rcomp_override_reg)—Offset 1108h" on page 5199	00FF4141h
110C–110Fh	"RCOMP Value Register (ulphsmvfamily_3x3_rcomp_13_0_family_rcomp_value_reg)—Offset 110Ch" on page 5200	00FF4141h
1110–1113h	"family_config_rcomp_reg (ulphsmvfamily_3x3_rcomp_13_0_family_config_rcomp_reg)—Offset 1110h" on page 5201	414103FFh
1114–1117h	"gpio_family_configuration_register (ulphsmvfamily_3x3_rcomp_13_0_family_config_reg)—Offset 1114h" on page 5202	05C00000h
1180–1183h	"RCOMP Control Register (hshvfamily_2x3_rcomp_7_0_family_rcomp_control_reg)—Offset 1180h" on page 5203	00D41D1Dh
1184–1187h	"RCOMP Offset Register (hshvfamily_2x3_rcomp_7_0_family_rcomp_offset_reg)—Offset 1184h" on page 5204	00000000h
1188–118Bh	"RCOMP Override Register (hshvfamily_2x3_rcomp_7_0_family_rcomp_override_reg)—Offset 1188h" on page 5205	00FF354Dh
118C–118Fh	"RCOMP Value Register (hshvfamily_2x3_rcomp_7_0_family_rcomp_value_reg)—Offset 118Ch" on page 5206	00FF354Dh
1190–1193h	"family_config_rcomp_reg (hshvfamily_2x3_rcomp_7_0_family_config_rcomp_reg)—Offset 1190h" on page 5207	354D03FFh
1194–1197h	"gpio_family_configuration_register (hshvfamily_2x3_rcomp_7_0_family_config_reg)—Offset 1194h" on page 5208	05C00000h
1200–1203h	"RCOMP Control Register (hshvfamily_3x3_rcomp_9_0_family_rcomp_control_reg)—Offset 1200h" on page 5209	00D41D1Dh
1204–1207h	"RCOMP Offset Register (hshvfamily_3x3_rcomp_9_0_family_rcomp_offset_reg)—Offset 1204h" on page 5210	00000000h
1208–120Bh	"RCOMP Override Register (hshvfamily_3x3_rcomp_9_0_family_rcomp_override_reg)—Offset 1208h" on page 5211	00FF354Dh
120C–120Fh	"RCOMP Value Register (hshvfamily_3x3_rcomp_9_0_family_rcomp_value_reg)—Offset 120Ch" on page 5212	00FF354Dh
1210–1213h	"family_config_rcomp_reg (hshvfamily_3x3_rcomp_9_0_family_config_rcomp_reg)—Offset 1210h" on page 5213	354D03FFh
1214–1217h	"gpio_family_configuration_register (hshvfamily_3x3_rcomp_9_0_family_config_reg)—Offset 1214h" on page 5214	05C00000h
1290–1293h	"family_config_rcomp_reg (ulphsmvfamily_3x3_10_0_family_config_rcomp_reg)—Offset 1290h" on page 5215	414103FFh
1294–1297h	"gpio_family_configuration_register (ulphsmvfamily_3x3_10_0_family_config_reg)—Offset 1294h" on page 5216	05C00000h
1310–1313h	"family_config_rcomp_reg (ulpmsmvfamily_3x3_11_0_family_config_rcomp_reg)—Offset 1310h" on page 5217	02020311h

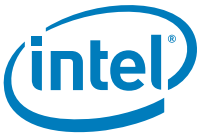


Table 10-101.Summary of GPIO SouthEast Message Bus Registers—0x48 (Continued)

Offset	Register Name (Register Symbol)	Default Value
1314–1317h	"gpio_family_configuration_register (ulpmsmvfamily_3x3_11_0_family_config_reg)—Offset 1314h" on page 5218	05C00000h
4000–4003h	"GPIO Broadcast Data Mask bit Register (gpio_pad_bw_mask_31_0)—Offset 4000h" on page 5219	00000000h
4004–4007h	"GPIO Broadcast Data Register (gpio_pad_bw_data_31_0)—Offset 4004h" on page 5219	00000000h
4008–400Bh	"gpio_pad_broadcast_reg_mask #0 (gpio_pad_broadcast_reg_mask_0)—Offset 4008h" on page 5220	00000000h
400C–400Fh	"gpio_pad_broadcast_reg_mask #1 (gpio_pad_broadcast_reg_mask_1)—Offset 400Ch" on page 5222	00000000h
4010–4013h	"gpio_pad_broadcast_reg_mask #2 (gpio_pad_broadcast_reg_mask_2)—Offset 4010h" on page 5224	00000000h
4014–4017h	"gpio_pad_broadcast_reg_mask #3 (gpio_pad_broadcast_reg_mask_3)—Offset 4014h" on page 5227	00000000h
4400–4403h	"Pad Control Register 0 (MF_PLT_CLK0_PAD_CFG0)—Offset 4400h" on page 5228	00110300h
4404–4407h	"Pad Control Register 1 (MF_PLT_CLK0_PAD_CFG1)—Offset 4404h" on page 5229	05C00000h
4408–440Bh	"Pad Control Register 0 (PWM1_PAD_CFG0)—Offset 4408h" on page 5231	00110300h
440C–440Fh	"Pad Control Register 1 (PWM1_PAD_CFG1)—Offset 440Ch" on page 5233	05C00000h
4410–4413h	"Pad Control Register 0 (MF_PLT_CLK1_PAD_CFG0)—Offset 4410h" on page 5235	00110300h
4414–4417h	"Pad Control Register 1 (MF_PLT_CLK1_PAD_CFG1)—Offset 4414h" on page 5236	05C00000h
4418–441Bh	"Pad Control Register 0 (MF_PLT_CLK4_PAD_CFG0)—Offset 4418h" on page 5238	00110300h
441C–441Fh	"Pad Control Register 1 (MF_PLT_CLK4_PAD_CFG1)—Offset 441Ch" on page 5239	05C00000h
4420–4423h	"Pad Control Register 0 (MF_PLT_CLK3_PAD_CFG0)—Offset 4420h" on page 5241	00110300h
4424–4427h	"Pad Control Register 1 (MF_PLT_CLK3_PAD_CFG1)—Offset 4424h" on page 5243	05C00000h
4428–442Bh	"Pad Control Register 0 (PWM0_PAD_CFG0)—Offset 4428h" on page 5245	00110300h
442C–442Fh	"Pad Control Register 1 (PWM0_PAD_CFG1)—Offset 442Ch" on page 5246	05C00000h
4430–4433h	"Pad Control Register 0 (MF_PLT_CLK5_PAD_CFG0)—Offset 4430h" on page 5248	00110300h
4434–4437h	"Pad Control Register 1 (MF_PLT_CLK5_PAD_CFG1)—Offset 4434h" on page 5249	05C00000h
4438–443Bh	"Pad Control Register 0 (MF_PLT_CLK2_PAD_CFG0)—Offset 4438h" on page 5251	00110300h
443C–443Fh	"Pad Control Register 1 (MF_PLT_CLK2_PAD_CFG1)—Offset 443Ch" on page 5253	05C00000h
4800–4803h	"Pad Control Register 0 (SDMMC2_D3_CD_B_PAD_CFG0)—Offset 4800h" on page 5255	00910300h

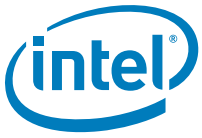


Table 10-101.Summary of GPIO SouthEast Message Bus Registers—0x48 (Continued)

Offset	Register Name (Register Symbol)	Default Value
4804–4807h	"Pad Control Register 1 (SDMMC2_D3_CD_B_PAD_CFG1)—Offset 4804h" on page 5256	05C00000h
4808–480Bh	"Pad Control Register 0 (SDMMC1_CLK_PAD_CFG0)—Offset 4808h" on page 5258	00110300h
480C–480Fh	"Pad Control Register 1 (SDMMC1_CLK_PAD_CFG1)—Offset 480Ch" on page 5259	05C00000h
4810–4813h	"Pad Control Register 0 (SDMMC1_D0_PAD_CFG0)—Offset 4810h" on page 5261	00910300h
4814–4817h	"Pad Control Register 1 (SDMMC1_D0_PAD_CFG1)—Offset 4814h" on page 5263	05C00000h
4818–481Bh	"Pad Control Register 0 (SDMMC2_D1_PAD_CFG0)—Offset 4818h" on page 5265	00910300h
481C–481Fh	"Pad Control Register 1 (SDMMC2_D1_PAD_CFG1)—Offset 481Ch" on page 5266	05C00000h
4820–4823h	"Pad Control Register 0 (SDMMC2_CLK_PAD_CFG0)—Offset 4820h" on page 5268	00110300h
4824–4827h	"Pad Control Register 1 (SDMMC2_CLK_PAD_CFG1)—Offset 4824h" on page 5269	05C00000h
4828–482Bh	"Pad Control Register 0 (SDMMC1_D2_PAD_CFG0)—Offset 4828h" on page 5271	00910300h
482C–482Fh	"Pad Control Register 1 (SDMMC1_D2_PAD_CFG1)—Offset 482Ch" on page 5273	05C00000h
4830–4833h	"Pad Control Register 0 (SDMMC2_D2_PAD_CFG0)—Offset 4830h" on page 5275	00910300h
4834–4837h	"Pad Control Register 1 (SDMMC2_D2_PAD_CFG1)—Offset 4834h" on page 5276	05C00000h
4838–483Bh	"Pad Control Register 0 (SDMMC2_CMD_PAD_CFG0)—Offset 4838h" on page 5278	00910300h
483C–483Fh	"Pad Control Register 1 (SDMMC2_CMD_PAD_CFG1)—Offset 483Ch" on page 5279	05C00000h
4840–4843h	"Pad Control Register 0 (SDMMC1_CMD_PAD_CFG0)—Offset 4840h" on page 5281	00910300h
4844–4847h	"Pad Control Register 1 (SDMMC1_CMD_PAD_CFG1)—Offset 4844h" on page 5283	05C00000h
4848–484Bh	"Pad Control Register 0 (SDMMC1_D1_PAD_CFG0)—Offset 4848h" on page 5285	00910300h
484C–484Fh	"Pad Control Register 1 (SDMMC1_D1_PAD_CFG1)—Offset 484Ch" on page 5286	05C00000h
4850–4853h	"Pad Control Register 0 (SDMMC2_D0_PAD_CFG0)—Offset 4850h" on page 5288	00910300h
4854–4857h	"Pad Control Register 1 (SDMMC2_D0_PAD_CFG1)—Offset 4854h" on page 5289	05C00000h
4858–485Bh	"Pad Control Register 0 (SDMMC1_D3_CD_B_PAD_CFG0)—Offset 4858h" on page 5291	00910300h
485C–485Fh	"Pad Control Register 1 (SDMMC1_D3_CD_B_PAD_CFG1)—Offset 485Ch" on page 5293	05C00000h
4C00–4C03h	"Pad Control Register 0 (SDMMC3_D1_PAD_CFG0)—Offset 4C00h" on page 5295	00910300h

Table 10-101.Summary of GPIO SouthEast Message Bus Registers—0x48 (Continued)

Offset	Register Name (Register Symbol)	Default Value
4C04–4C07h	"Pad Control Register 1 (SDMMC3_D1_PAD_CFG1)—Offset 4C04h" on page 5296	05C00000h
4C08–4C0Bh	"Pad Control Register 0 (SDMMC3_CLK_PAD_CFG0)—Offset 4C08h" on page 5298	00110300h
4C0C–4C0Fh	"Pad Control Register 1 (SDMMC3_CLK_PAD_CFG1)—Offset 4C0Ch" on page 5299	05C00000h
4C10–4C13h	"Pad Control Register 0 (SDMMC3_D3_PAD_CFG0)—Offset 4C10h" on page 5301	00910300h
4C14–4C17h	"Pad Control Register 1 (SDMMC3_D3_PAD_CFG1)—Offset 4C14h" on page 5303	05C00000h
4C18–4C1Bh	"Pad Control Register 0 (SDMMC3_D2_PAD_CFG0)—Offset 4C18h" on page 5305	00910300h
4C1C–4C1Fh	"Pad Control Register 1 (SDMMC3_D2_PAD_CFG1)—Offset 4C1Ch" on page 5306	05C00000h
4C20–4C23h	"Pad Control Register 0 (SDMMC3_CMD_PAD_CFG0)—Offset 4C20h" on page 5308	00910300h
4C24–4C27h	"Pad Control Register 1 (SDMMC3_CMD_PAD_CFG1)—Offset 4C24h" on page 5309	05C00000h
4C28–4C2Bh	"Pad Control Register 0 (SDMMC3_D0_PAD_CFG0)—Offset 4C28h" on page 5311	00910300h
4C2C–4C2Fh	"Pad Control Register 1 (SDMMC3_D0_PAD_CFG1)—Offset 4C2Ch" on page 5313	05C00000h
5000–5003h	"Pad Control Register 0 (MF_LPC_AD2_PAD_CFG0)—Offset 5000h" on page 5315	00910300h
5004–5007h	"Pad Control Register 1 (MF_LPC_AD2_PAD_CFG1)—Offset 5004h" on page 5316	05C00000h
5008–500Bh	"Pad Control Register 0 (LPC_CLKRUNB_PAD_CFG0)—Offset 5008h" on page 5318	00910300h
500C–500Fh	"Pad Control Register 1 (LPC_CLKRUNB_PAD_CFG1)—Offset 500Ch" on page 5319	05C00000h
5010–5013h	"Pad Control Register 0 (MF_LPC_AD0_PAD_CFG0)—Offset 5010h" on page 5321	00910300h
5014–5017h	"Pad Control Register 1 (MF_LPC_AD0_PAD_CFG1)—Offset 5014h" on page 5323	05C00000h
5018–501Bh	"Pad Control Register 0 (LPC_FRAMEB_PAD_CFG0)—Offset 5018h" on page 5325	00910300h
501C–501Fh	"Pad Control Register 1 (LPC_FRAMEB_PAD_CFG1)—Offset 501Ch" on page 5326	05C00000h
5020–5023h	"Pad Control Register 0 (MF_LPC_CLKOUT1_PAD_CFG0)—Offset 5020h" on page 5328	00110300h
5024–5027h	"Pad Control Register 1 (MF_LPC_CLKOUT1_PAD_CFG1)—Offset 5024h" on page 5329	05C00000h
5028–502Bh	"Pad Control Register 0 (MF_LPC_AD3_PAD_CFG0)—Offset 5028h" on page 5331	00910300h
502C–502Fh	"Pad Control Register 1 (MF_LPC_AD3_PAD_CFG1)—Offset 502Ch" on page 5333	05C00000h
5030–5033h	"Pad Control Register 0 (MF_LPC_CLKOUT0_PAD_CFG0)—Offset 5030h" on page 5335	00110300h

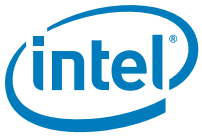


Table 10-101.Summary of GPIO SouthEast Message Bus Registers—0x48 (Continued)

Offset	Register Name (Register Symbol)	Default Value
5034–5037h	"Pad Control Register 1 (MF_LPC_CLKOUT0_PAD_CFG1)—Offset 5034h" on page 5336	05C00000h
5038–503Bh	"Pad Control Register 0 (MF_LPC_AD1_PAD_CFG0)—Offset 5038h" on page 5338	00910300h
503C–503Fh	"Pad Control Register 1 (MF_LPC_AD1_PAD_CFG1)—Offset 503Ch" on page 5339	05C00000h
5400–5403h	"Pad Control Register 0 (SPI1_MISO_PAD_CFG0)—Offset 5400h" on page 5341	00910300h
5404–5407h	"Pad Control Register 1 (SPI1_MISO_PAD_CFG1)—Offset 5404h" on page 5343	05C00000h
5408–540Bh	"Pad Control Register 0 (SPI1_CS0_B_PAD_CFG0)—Offset 5408h" on page 5345	00910300h
540C–540Fh	"Pad Control Register 1 (SPI1_CS0_B_PAD_CFG1)—Offset 540Ch" on page 5346	05C00000h
5410–5413h	"Pad Control Register 0 (SPI1_CLK_PAD_CFG0)—Offset 5410h" on page 5348	00910300h
5414–5417h	"Pad Control Register 1 (SPI1_CLK_PAD_CFG1)—Offset 5414h" on page 5349	05C00000h
5418–541Bh	"Pad Control Register 0 (MMC1_D6_PAD_CFG0)—Offset 5418h" on page 5351	00910300h
541C–541Fh	"Pad Control Register 1 (MMC1_D6_PAD_CFG1)—Offset 541Ch" on page 5353	05C00000h
5420–5423h	"Pad Control Register 0 (SPI1_MOSI_PAD_CFG0)—Offset 5420h" on page 5355	00910300h
5424–5427h	"Pad Control Register 1 (SPI1_MOSI_PAD_CFG1)—Offset 5424h" on page 5356	05C00000h
5428–542Bh	"Pad Control Register 0 (MMC1_D5_PAD_CFG0)—Offset 5428h" on page 5358	00910300h
542C–542Fh	"Pad Control Register 1 (MMC1_D5_PAD_CFG1)—Offset 542Ch" on page 5359	05C00000h
5430–5433h	"Pad Control Register 0 (SPI1_CS1_B_PAD_CFG0)—Offset 5430h" on page 5361	00910300h
5434–5437h	"Pad Control Register 1 (SPI1_CS1_B_PAD_CFG1)—Offset 5434h" on page 5363	05C00000h
5438–543Bh	"Pad Control Register 0 (MMC1_D4_SD_WE_PAD_CFG0)—Offset 5438h" on page 5365	00910300h
543C–543Fh	"Pad Control Register 1 (MMC1_D4_SD_WE_PAD_CFG1)—Offset 543Ch" on page 5366	05C00000h
5440–5443h	"Pad Control Register 0 (MMC1_D7_PAD_CFG0)—Offset 5440h" on page 5368	00910300h
5444–5447h	"Pad Control Register 1 (MMC1_D7_PAD_CFG1)—Offset 5444h" on page 5369	05C00000h
5448–544Bh	"Pad Control Register 0 (MMC1_RCLK_PAD_CFG0)—Offset 5448h" on page 5371	00110300h
544C–544Fh	"Pad Control Register 1 (MMC1_RCLK_PAD_CFG1)—Offset 544Ch" on page 5373	05C00000h
5800–5803h	"Pad Control Register 0 (USB_OC1_B_PAD_CFG0)—Offset 5800h" on page 5375	00910300h

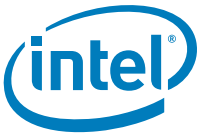


Table 10-101.Summary of GPIO SouthEast Message Bus Registers—0x48 (Continued)

Offset	Register Name (Register Symbol)	Default Value
5804–5807h	"Pad Control Register 1 (USB_OC1_B_PAD_CFG1)—Offset 5804h" on page 5376	05C00000h
5808–580Bh	"Pad Control Register 0 (PMU_RESETBUTTON_B_PAD_CFG0)—Offset 5808h" on page 5378	00910300h
580C–580Fh	"Pad Control Register 1 (PMU_RESETBUTTON_B_PAD_CFG1)—Offset 580Ch" on page 5379	05C00000h
5810–5813h	"Pad Control Register 0 (GPIO_ALERT_PAD_CFG0)—Offset 5810h" on page 5381	00910300h
5814–5817h	"Pad Control Register 1 (GPIO_ALERT_PAD_CFG1)—Offset 5814h" on page 5383	05C00000h
5818–581Bh	"Pad Control Register 0 (SDMMC3_PWR_EN_B_PAD_CFG0)—Offset 5818h" on page 5385	00110300h
581C–581Fh	"Pad Control Register 1 (SDMMC3_PWR_EN_B_PAD_CFG1)—Offset 581Ch" on page 5386	05C00000h
5820–5823h	"Pad Control Register 0 (ILB_SERIRQ_PAD_CFG0)—Offset 5820h" on page 5388	00918300h
5824–5827h	"Pad Control Register 1 (ILB_SERIRQ_PAD_CFG1)—Offset 5824h" on page 5389	05C00000h
5828–582Bh	"Pad Control Register 0 (USB_OC0_B_PAD_CFG0)—Offset 5828h" on page 5391	00910300h
582C–582Fh	"Pad Control Register 1 (USB_OC0_B_PAD_CFG1)—Offset 582Ch" on page 5393	05C00000h
5830–5833h	"Pad Control Register 0 (SDMMC3_CD_B_PAD_CFG0)—Offset 5830h" on page 5395	00910300h
5834–5837h	"Pad Control Register 1 (SDMMC3_CD_B_PAD_CFG1)—Offset 5834h" on page 5396	05C00000h
5838–583Bh	"Pad Control Register 0 (SPKR_PAD_CFG0)—Offset 5838h" on page 5398	00910300h
583C–583Fh	"Pad Control Register 1 (SPKR_PAD_CFG1)—Offset 583Ch" on page 5399	05C00000h
5840–5843h	"Pad Control Register 0 (SUSPWRDNACK_PAD_CFG0)—Offset 5840h" on page 5401	00110300h
5844–5847h	"Pad Control Register 1 (SUSPWRDNACK_PAD_CFG1)—Offset 5844h" on page 5403	05C00000h
5848–584Bh	"Pad Control Register 0 (SPARE_PIN_PAD_CFG0)—Offset 5848h" on page 5405	00110300h
584C–584Fh	"Pad Control Register 1 (SPARE_PIN_PAD_CFG1)—Offset 584Ch" on page 5406	05C00000h
5850–5853h	"Pad Control Register 0 (SDMMC3_1P8_EN_PAD_CFG0)—Offset 5850h" on page 5408	00110300h
5854–5857h	"Pad Control Register 1 (SDMMC3_1P8_EN_PAD_CFG1)—Offset 5854h" on page 5409	05C00000h

10.6.1 GPIO Read Access Control (gpio_read_access_policy_access_reg)—Offset 0h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

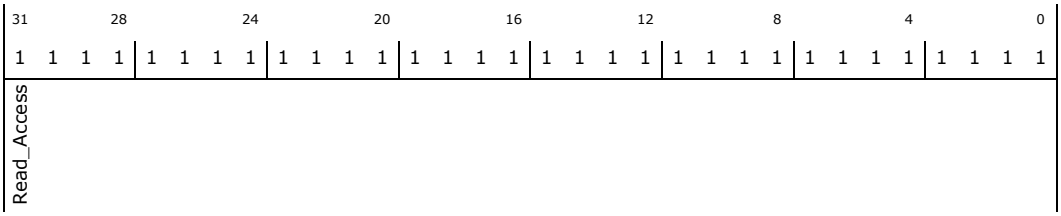
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 0h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.6.2 GPIO Read Access Control (gpio_read_access_policy_wake_reg)—Offset 4h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

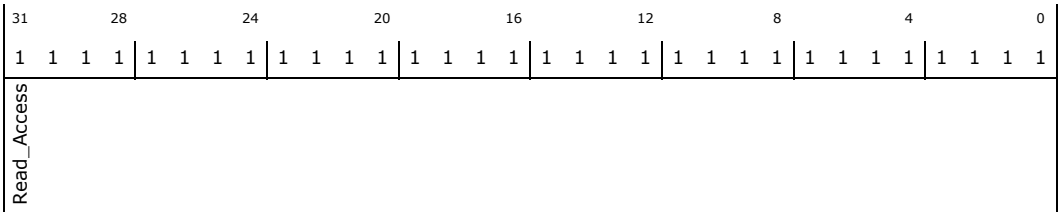
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.6.3 GPIO Read Access Control (gpio_read_access_policy_interrupt_reg)—Offset 8h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

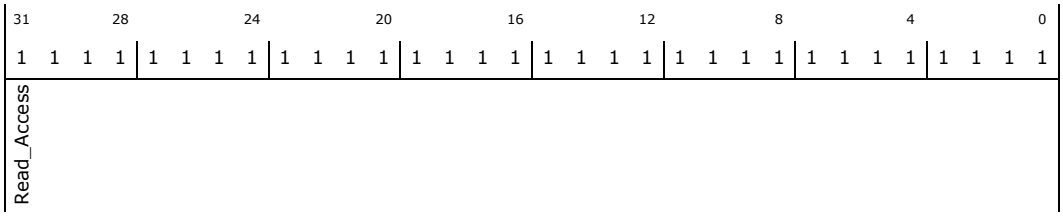
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 8h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.6.4 GPIO Read Access Control (gpio_read_access_policy_community_reg)—Offset Ch

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

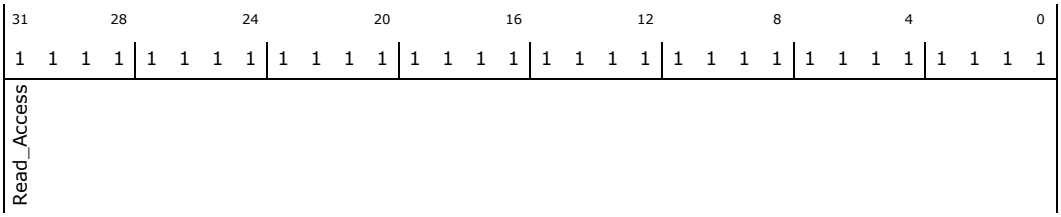
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.6.5 GPIO Read Access Control (gpio_read_access_policy_family_broadcast_reg)—Offset 10h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

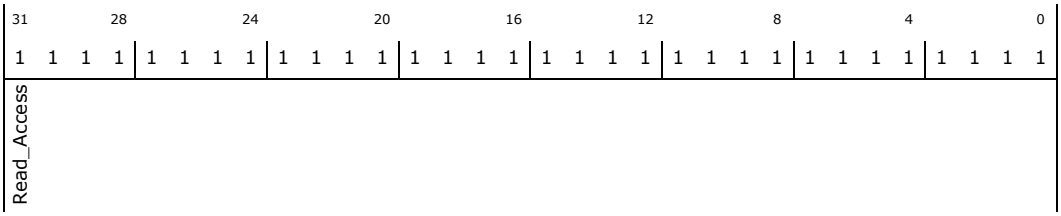
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 10h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.6.6 GPIO Read Access Control (gpio_read_access_policy_family_reg)—Offset 14h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

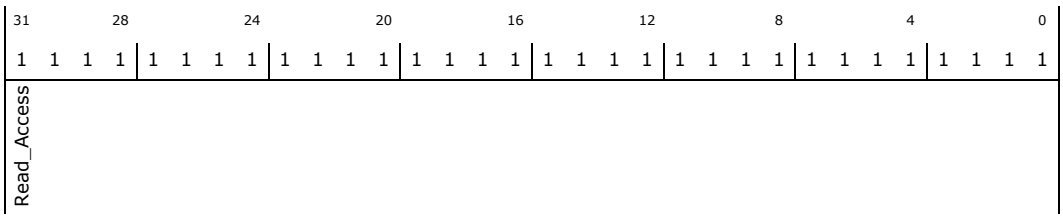
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 14h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.6.7 GPIO Read Access Control (gpio_read_access_policy_pad_broadcast_reg)—Offset 18h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

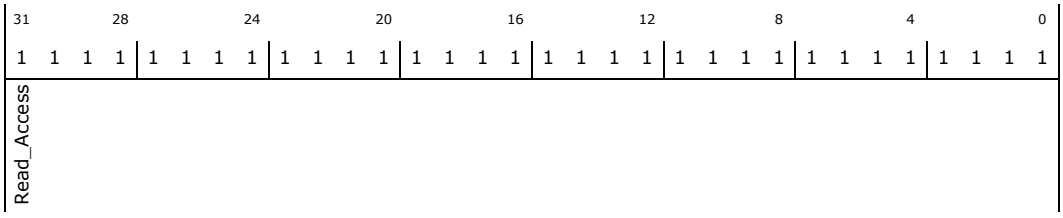
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 18h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.6.8 GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_2x3_8_2_regs)—Offset 1Ch

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

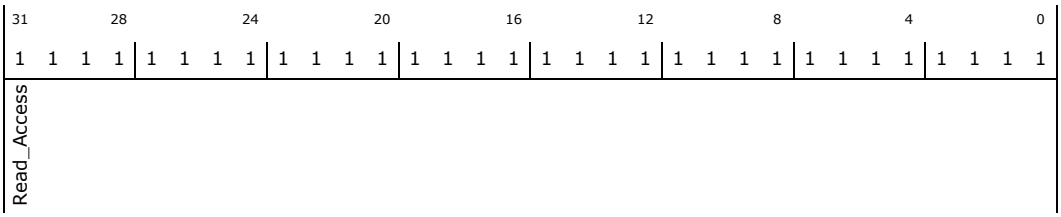
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.6.9 GPIO Read Access Control (gpio_read_access_policy_ulphsmvfamily_3x3_rcomp_13_0_regs)—Offset 20h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

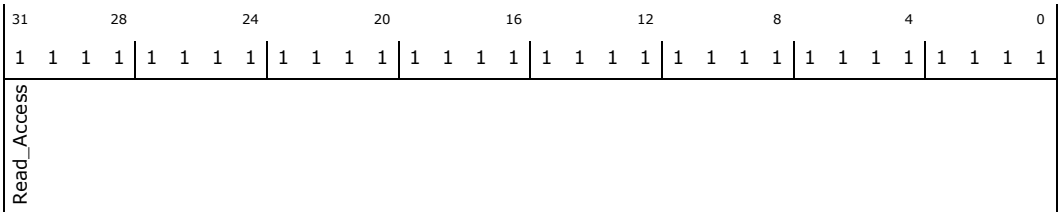
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 20h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.6.10 GPIO Read Access Control (gpio_read_access_policy_hshvfamily_2x3_rcomp_7_0_regs)—Offset 24h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

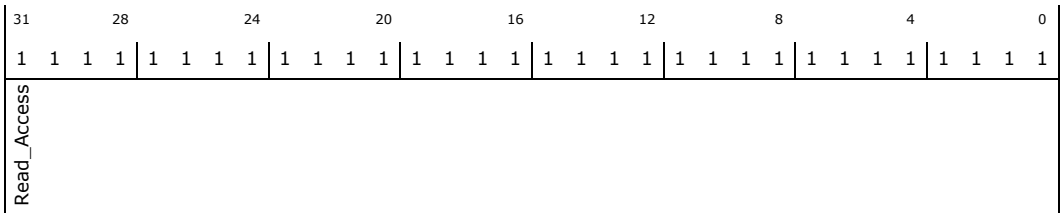
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 24h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.6.11 GPIO Read Access Control (gpio_read_access_policy_hshvfamily_3x3_rcomp_9_0_regs)—Offset 28h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

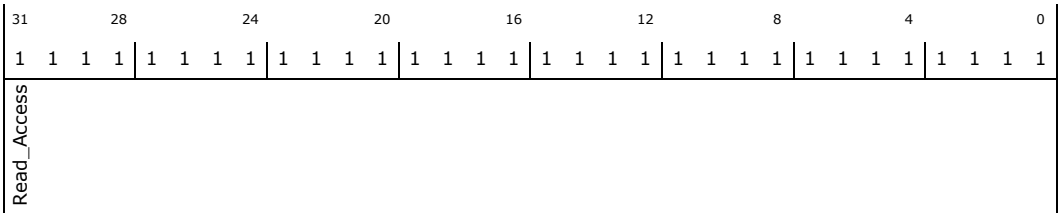
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 28h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.6.12 GPIO Read Access Control (gpio_read_access_policy_ulphsmvfamily_3x3_10_0_regs)—Offset 2Ch

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

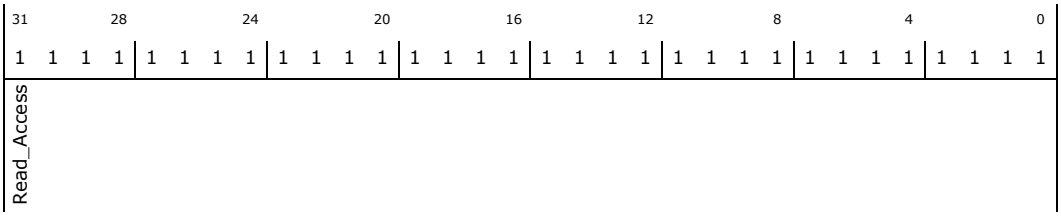
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 2Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.6.13 GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_3x3_11_0_regs)—Offset 30h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

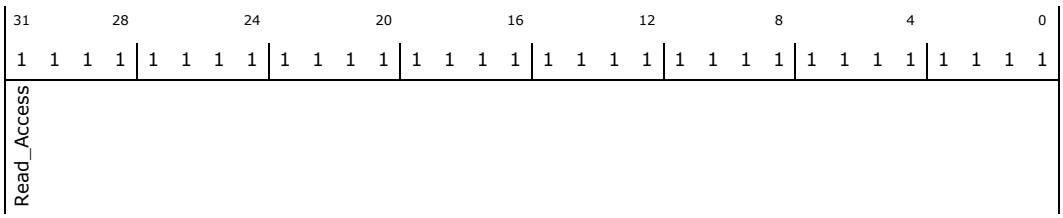
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 30h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.6.14 GPIO Write Access Control (gpio_write_access_policy_access_reg)—Offset 100h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

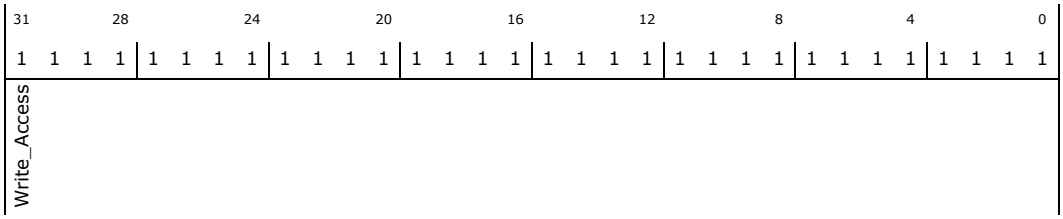
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 100h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.6.15 GPIO Write Access Control (gpio_write_access_policy_wake_reg)—Offset 104h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

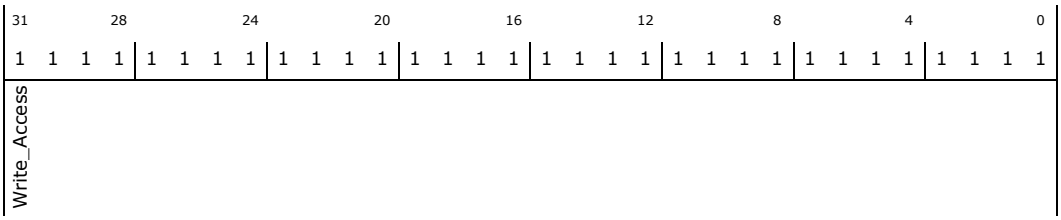
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 104h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.6.16 GPIO Write Access Control (gpio_write_access_policy_interrupt_reg)—Offset 108h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

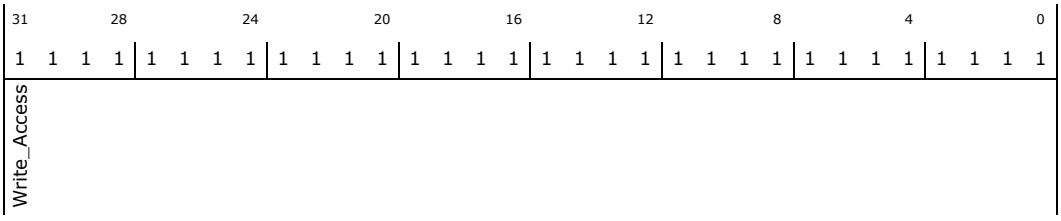
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 108h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.6.17 GPIO Write Access Control (gpio_write_access_policy_community_reg)—Offset 10Ch

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

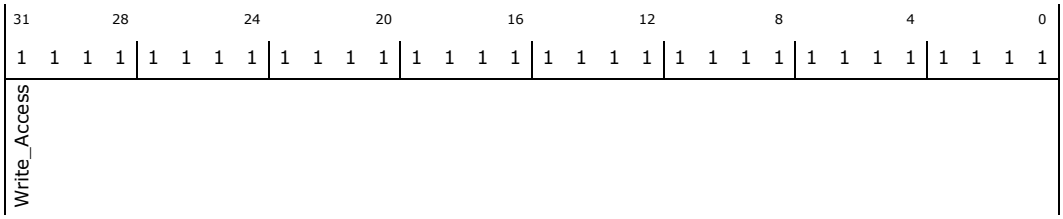
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 10Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.6.18 GPIO Write Access Control (gpio_write_access_policy_family_broadcast_reg)—Offset 110h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

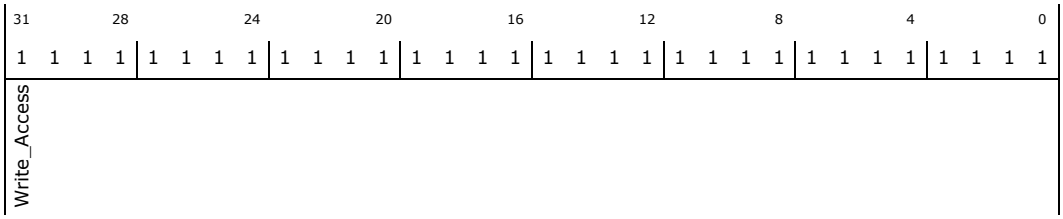
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 110h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.6.19 GPIO Write Access Control (gpio_write_access_policy_family_reg)—Offset 114h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

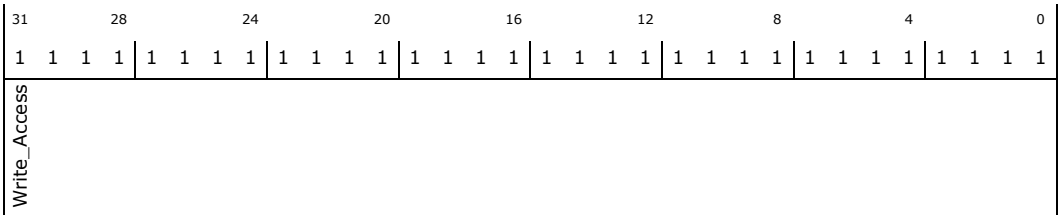
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 114h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.6.20 GPIO Write Access Control (gpio_write_access_policy_pad_broadcast_reg)—Offset 118h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

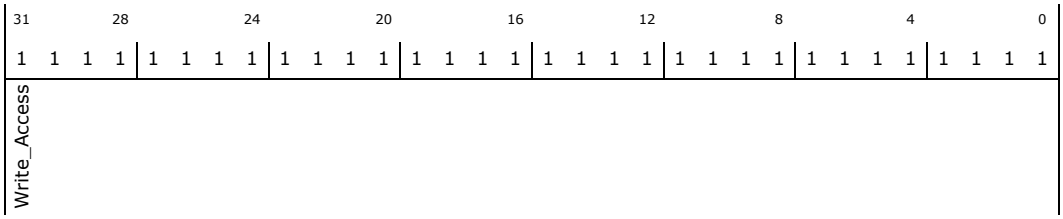
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 118h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.6.21 GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_2x3_8_2_regs)—Offset 11Ch

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

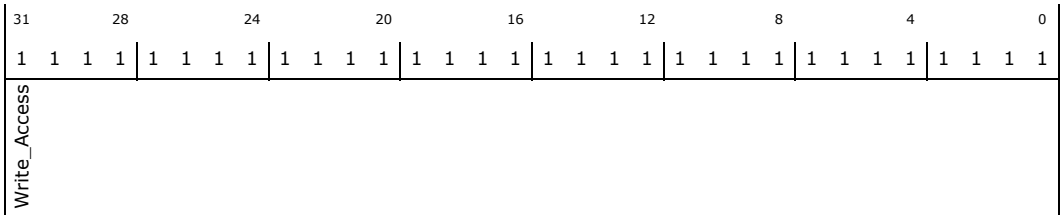
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 11Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.6.22 GPIO Write Access Control (gpio_write_access_policy_ulphsmvfamily_3x3_rcomp_13_0_regs)—Offset 120h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

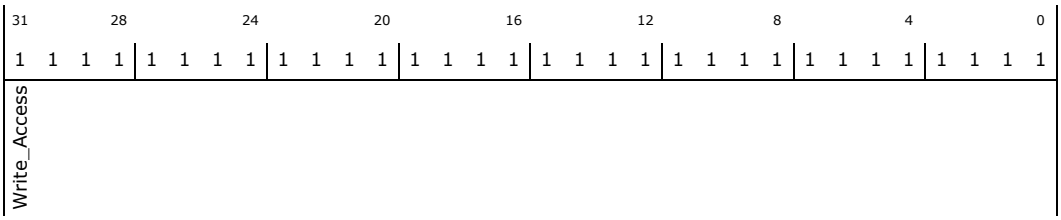
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 120h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.6.23 GPIO Write Access Control (gpio_write_access_policy_hshvfamily_2x3_rcomp_7_0_regs)—Offset 124h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

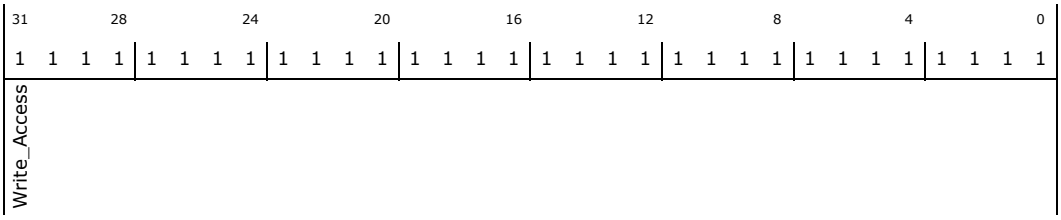
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 124h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.6.24 GPIO Write Access Control (gpio_write_access_policy_hshvfamily_3x3_rcomp_9_0_regs)—Offset 128h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

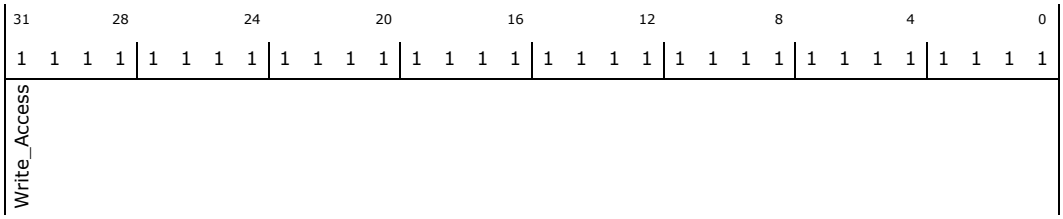
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 128h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.6.25 GPIO Write Access Control (gpio_write_access_policy_ulphsmvfamily_3x3_10_0_regs)—Offset 12Ch

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

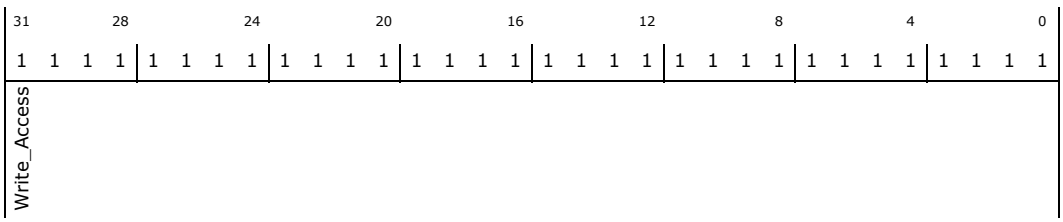
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 12Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.6.26 GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_3x3_11_0_regs)—Offset 130h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

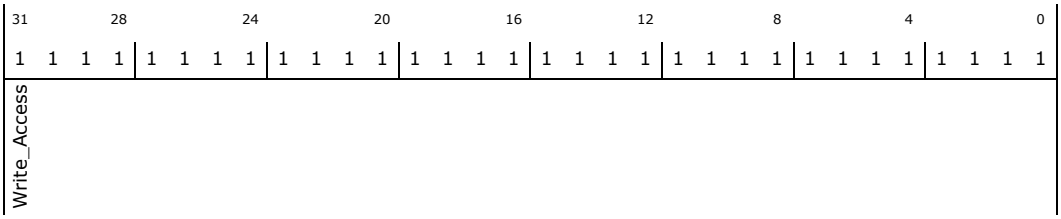
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 130h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.6.27 GPIO_WAKE_STATUS_REG #0 (gpio_wake_status_reg_0)—Offset 200h

GPIO Wake Status Register write 1 to clear.

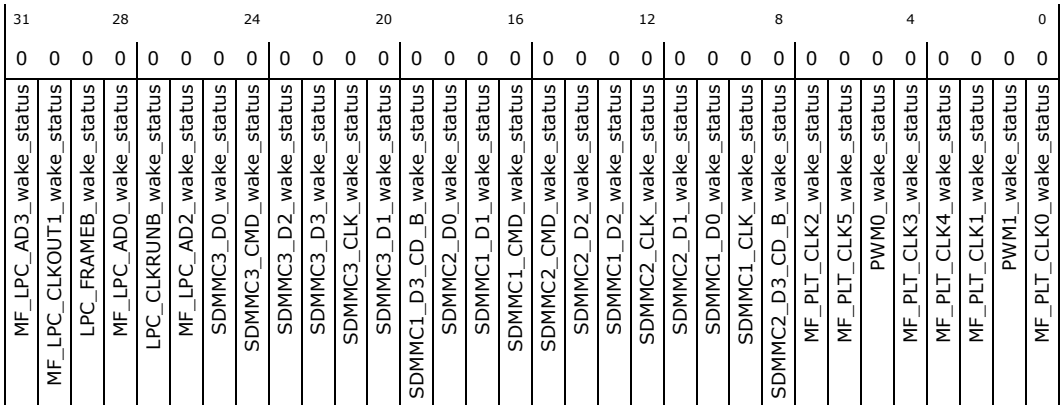
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 200h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1C	**MF_LPC_AD3_wake_status:** Reserved.
30	0x0 RW/1C	**MF_LPC_CLKOUT1_wake_status:** Reserved.
29	0x0 RW/1C	**LPC_FRAMEB_wake_status:** Reserved.
28	0x0 RW/1C	**MF_LPC_AD0_wake_status:** Reserved.
27	0x0 RW/1C	**LPC_CLKRUNB_wake_status:** Reserved.
26	0x0 RW/1C	**MF_LPC_AD2_wake_status:** Reserved.
25	0x0 RW/1C	**SDMMC3_D0_wake_status:** Reserved.
24	0x0 RW/1C	**SDMMC3_CMD_wake_status:** Reserved.
23	0x0 RW/1C	**SDMMC3_D2_wake_status:** Reserved.
22	0x0 RW/1C	**SDMMC3_D3_wake_status:** Reserved.
21	0x0 RW/1C	**SDMMC3_CLK_wake_status:** Reserved.
20	0x0 RW/1C	**SDMMC3_D1_wake_status:** Reserved.
19	0x0 RW/1C	**SDMMC1_D3_CD_B_wake_status:** Reserved.
18	0x0 RW/1C	**SDMMC2_D0_wake_status:** Reserved.
17	0x0 RW/1C	**SDMMC1_D1_wake_status:** Reserved.
16	0x0 RW/1C	**SDMMC1_CMD_wake_status:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
15	0x0 RW/1C	**SDMMC2_CMD_wake_status:** Reserved.
14	0x0 RW/1C	**SDMMC2_D2_wake_status:** Reserved.
13	0x0 RW/1C	**SDMMC1_D2_wake_status:** Reserved.
12	0x0 RW/1C	**SDMMC2_CLK_wake_status:** Reserved.
11	0x0 RW/1C	**SDMMC2_D1_wake_status:** Reserved.
10	0x0 RW/1C	**SDMMC1_D0_wake_status:** Reserved.
9	0x0 RW/1C	**SDMMC1_CLK_wake_status:** Reserved.
8	0x0 RW/1C	**SDMMC2_D3_CD_B_wake_status:** Reserved.
7	0x0 RW/1C	**MF_PLT_CLK2_wake_status:** Reserved.
6	0x0 RW/1C	**MF_PLT_CLK5_wake_status:** Reserved.
5	0x0 RW/1C	**PWM0_wake_status:** Reserved.
4	0x0 RW/1C	**MF_PLT_CLK3_wake_status:** Reserved.
3	0x0 RW/1C	**MF_PLT_CLK4_wake_status:** Reserved.
2	0x0 RW/1C	**MF_PLT_CLK1_wake_status:** Reserved.
1	0x0 RW/1C	**PWM1_wake_status:** Reserved.
0	0x0 RW/1C	**MF_PLT_CLK0_wake_status:** Reserved.

10.6.28 GPIO_WAKE_STATUS_REG #1 (gpio_wake_status_reg_1)—Offset 204h

GPIO Wake Status Register write 1 to clear.

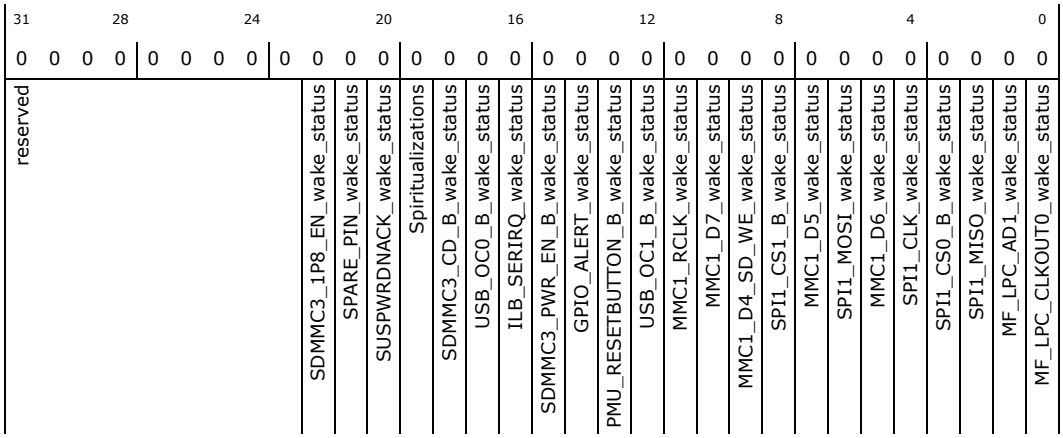
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 204h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:23	0x0 RW/1C	**reserved:** Reserved.
22	0x0 RW/1C	**SDMMC3_1P8_EN_wake_status:** Reserved.
21	0x0 RW/1C	**SPARE_PIN_wake_status:** Reserved.
20	0x0 RW/1C	**SUSPWRDNACK_wake_status:** Reserved.
19	0x0 RW/1C	**SPKR_wake_status:** Reserved.
18	0x0 RW/1C	**SDMMC3_CD_B_wake_status:** Reserved.
17	0x0 RW/1C	**USB_OC0_B_wake_status:** Reserved.
16	0x0 RW/1C	**ILB_SERIRQ_wake_status:** Reserved.
15	0x0 RW/1C	**SDMMC3_PWR_EN_B_wake_status:** Reserved.
14	0x0 RW/1C	**GPIO_ALERT_wake_status:** Reserved.
13	0x0 RW/1C	**PMU_RESETBUTTON_B_wake_status:** Reserved.
12	0x0 RW/1C	**USB_OC1_B_wake_status:** Reserved.
11	0x0 RW/1C	**MMC1_RCLK_wake_status:** Reserved.
10	0x0 RW/1C	**MMC1_D7_wake_status:** Reserved.
9	0x0 RW/1C	**MMC1_D4_SD_WE_wake_status:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
8	0x0 RW/1C	**SPI1_CS1_B_wake_status:** Reserved.
7	0x0 RW/1C	**MMC1_D5_wake_status:** Reserved.
6	0x0 RW/1C	**SPI1_MOSI_wake_status:** Reserved.
5	0x0 RW/1C	**MMC1_D6_wake_status:** Reserved.
4	0x0 RW/1C	**SPI1_CLK_wake_status:** Reserved.
3	0x0 RW/1C	**SPI1_CS0_B_wake_status:** Reserved.
2	0x0 RW/1C	**SPI1_MISO_wake_status:** Reserved.
1	0x0 RW/1C	**MF_LPC_AD1_wake_status:** Reserved.
0	0x0 RW/1C	**MF_LPC_CLKOUT0_wake_status:** Reserved.

10.6.29 GPIO_WAKE_MASK_REG #0 (gpio_wake_mask_reg_0)—Offset 280h

GPIO Wake Register 0 Masks Wake.

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 280h

Op Codes:
h - Read, h - Write

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MF_LPC_AD3_wake_mask	MF_LPC_CLKOUT1_wake_mask	LPC_FRAMEB_wake_mask	MF_LPC_AD0_wake_mask	LPC_CLKRUNB_wake_mask	MF_LPC_AD2_wake_mask	SDMMC3_D0_wake_mask	SDMMC3_CMD_wake_mask	SDMMC3_D2_wake_mask	SDMMC3_D3_wake_mask	SDMMC3_CLK_wake_mask	SDMMC3_D1_wake_mask	SDMMC1_D3_CD_B_wake_mask	SDMMC2_D0_wake_mask	SDMMC1_D1_wake_mask	SDMMC1_CMD_wake_mask	SDMMC2_CMD_wake_mask	SDMMC2_D2_wake_mask	SDMMC1_D2_wake_mask	SDMMC2_CLK_wake_mask	SDMMC2_D1_wake_mask	SDMMC1_D0_wake_mask	SDMMC1_CLK_wake_mask	SDMMC2_D3_CD_B_wake_mask	MF_PLT_CLK2_wake_mask	MF_PLT_CLK5_wake_mask	PWM0_wake_mask	MF_PLT_CLK3_wake_mask	MF_PLT_CLK4_wake_mask	MF_PLT_CLK1_wake_mask	PWM1_wake_mask	MF_PLT_CLK0_wake_mask

Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**MF_LPC_AD3_wake_mask:** Reserved.
30	0x0 RW	**MF_LPC_CLKOUT1_wake_mask:** Reserved.
29	0x0 RW	**LPC_FRAMEB_wake_mask:** Reserved.
28	0x0 RW	**MF_LPC_AD0_wake_mask:** Reserved.
27	0x0 RW	**LPC_CLKRUNB_wake_mask:** Reserved.
26	0x0 RW	**MF_LPC_AD2_wake_mask:** Reserved.
25	0x0 RW	**SDMMC3_D0_wake_mask:** Reserved.
24	0x0 RW	**SDMMC3_CMD_wake_mask:** Reserved.
23	0x0 RW	**SDMMC3_D2_wake_mask:** Reserved.
22	0x0 RW	**SDMMC3_D3_wake_mask:** Reserved.
21	0x0 RW	**SDMMC3_CLK_wake_mask:** Reserved.
20	0x0 RW	**SDMMC3_D1_wake_mask:** Reserved.
19	0x0 RW	**SDMMC1_D3_CD_B_wake_mask:** Reserved.
18	0x0 RW	**SDMMC2_D0_wake_mask:** Reserved.
17	0x0 RW	**SDMMC1_D1_wake_mask:** Reserved.
16	0x0 RW	**SDMMC1_CMD_wake_mask:** Reserved.
15	0x0 RW	**SDMMC2_CMD_wake_mask:** Reserved.
14	0x0 RW	**SDMMC2_D2_wake_mask:** Reserved.
13	0x0 RW	**SDMMC1_D2_wake_mask:** Reserved.
12	0x0 RW	**SDMMC2_CLK_wake_mask:** Reserved.
11	0x0 RW	**SDMMC2_D1_wake_mask:** Reserved.
10	0x0 RW	**SDMMC1_D0_wake_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
9	0x0 RW	**SDMMC1_CLK_wake_mask:** Reserved.
8	0x0 RW	**SDMMC2_D3_CD_B_wake_mask:** Reserved.
7	0x0 RW	**MF_PLT_CLK2_wake_mask:** Reserved.
6	0x0 RW	**MF_PLT_CLK5_wake_mask:** Reserved.
5	0x0 RW	**PWM0_wake_mask:** Reserved.
4	0x0 RW	**MF_PLT_CLK3_wake_mask:** Reserved.
3	0x0 RW	**MF_PLT_CLK4_wake_mask:** Reserved.
2	0x0 RW	**MF_PLT_CLK1_wake_mask:** Reserved.
1	0x0 RW	**PWM1_wake_mask:** Reserved.
0	0x0 RW	**MF_PLT_CLK0_wake_mask:** Reserved.

10.6.30 GPIO_WAKE_MASK_REG #1 (gpio_wake_mask_reg_1)—Offset 284h

GPIO Wake Register 0 Masks Wake.

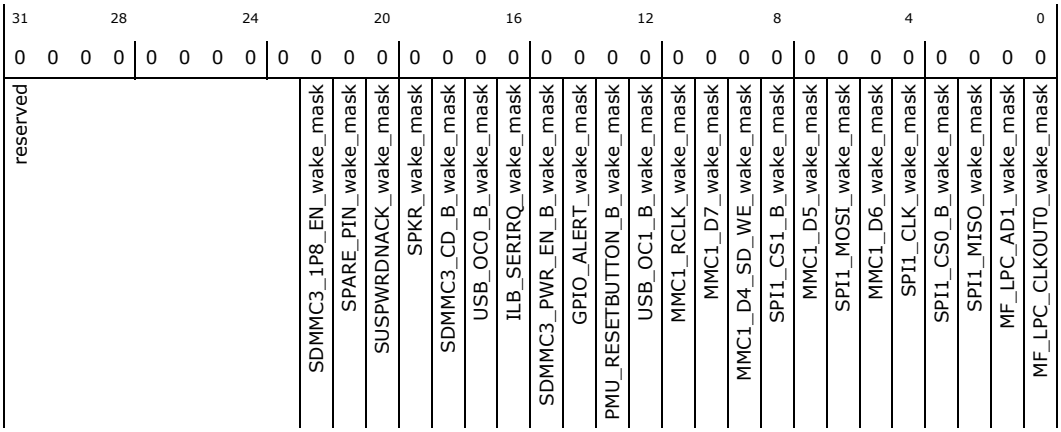
Access Method

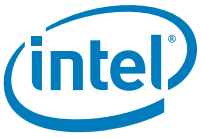
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 284h

Op Codes:
h - Read, h - Write

Default: 00000000h





Bit Range	Default and Access	Field Name (ID): Description
31:23	0x0 RW	**reserved:** Reserved.
22	0x0 RW	**SDMMC3_1P8_EN_wake_mask:** Reserved.
21	0x0 RW	**SPARE_PIN_wake_mask:** Reserved.
20	0x0 RW	**SUSPWRDNACK_wake_mask:** Reserved.
19	0x0 RW	**SPKR_wake_mask:** Reserved.
18	0x0 RW	**SDMMC3_CD_B_wake_mask:** Reserved.
17	0x0 RW	**USB_OC0_B_wake_mask:** Reserved.
16	0x0 RW	**ILB_SERIRQ_wake_mask:** Reserved.
15	0x0 RW	**SDMMC3_PWR_EN_B_wake_mask:** Reserved.
14	0x0 RW	**GPIO_ALERT_wake_mask:** Reserved.
13	0x0 RW	**PMU_RESETBUTTON_B_wake_mask:** Reserved.
12	0x0 RW	**USB_OC1_B_wake_mask:** Reserved.
11	0x0 RW	**MMC1_RCLK_wake_mask:** Reserved.
10	0x0 RW	**MMC1_D7_wake_mask:** Reserved.
9	0x0 RW	**MMC1_D4_SD_WE_wake_mask:** Reserved.
8	0x0 RW	**SPI1_CS1_B_wake_mask:** Reserved.
7	0x0 RW	**MMC1_D5_wake_mask:** Reserved.
6	0x0 RW	**SPI1_MOSI_wake_mask:** Reserved.
5	0x0 RW	**MMC1_D6_wake_mask:** Reserved.
4	0x0 RW	**SPI1_CLK_wake_mask:** Reserved.
3	0x0 RW	**SPI1_CS0_B_wake_mask:** Reserved.
2	0x0 RW	**SPI1_MISO_wake_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
1	0x0 RW	**MF_LPC_AD1_wake_mask:** Reserved.
0	0x0 RW	**MF_LPC_CLKOUT0_wake_mask:** Reserved.

10.6.31 GPIO Interrupt Status (gpio_interrupt_status)—Offset 300h

Status bits for the 16 interrupts.

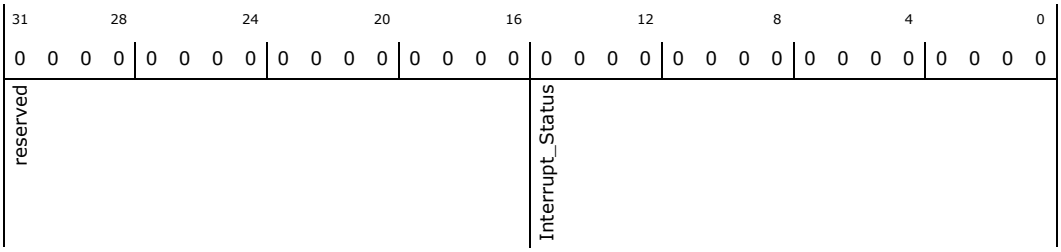
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 300h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW/1C	**reserved:** reserved
15:0	0x0 RW/1C	**Interrupt Status (Interrupt_Status):** Status bits for the 16 interrupts. Write 1 to Clear

10.6.32 GPIO Interrupt Status (gpio_interrupt_mask)—Offset 380h

Mask bits for the 16 interrupts.

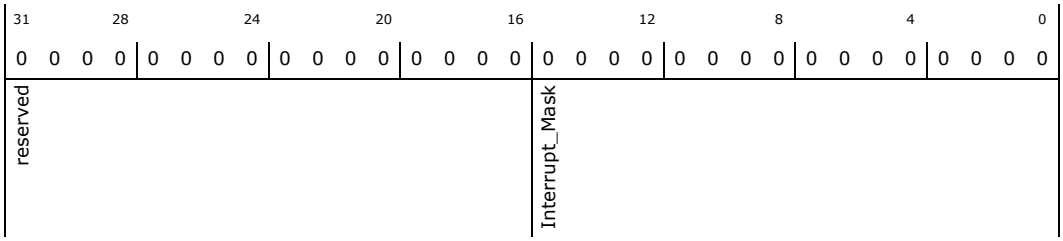
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 380h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**reserved:** reserved
15:0	0x0 RW	**Interrupt Mask (Interrupt_Mask):** Mask bits for the 16 interrupts. Interrupt masked when 0.

10.6.33 Slave Delay Line Override Register (slave_delay_line_override)—Offset 600h

This register allows us to override the coarse and fine codes sent by the Master DLL to the Slave Delay Lines

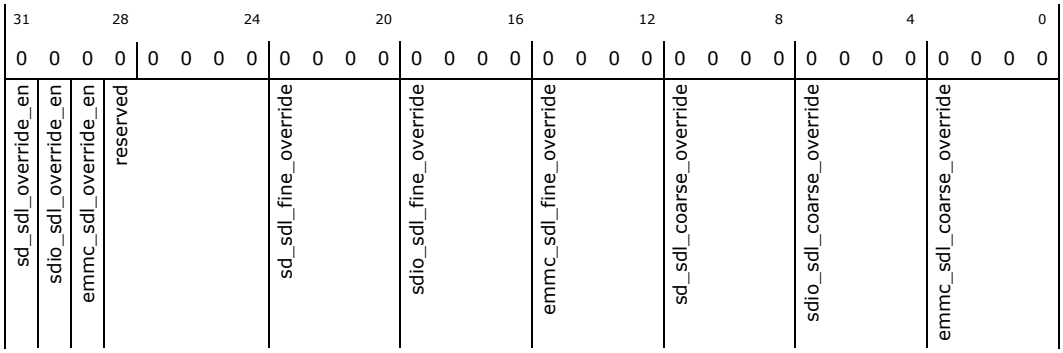
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 600h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**sd_sdl_override_en:** Enable override of coarse/fine codes to the SD interface DLLs; 0; use coarse/fine codes from Master DLL; 1: use coarse/fine codes from this register
30	0x0 RW	**sdio_sdl_override_en:** Enable override of coarse/fine codes to the SDIO interface DLLs; 0; use coarse/fine codes from Master DLL; 1: use coarse/fine codes from this register

Bit Range	Default and Access	Field Name (ID): Description
29	0x0 RW	**emmc_sdl_override_en:** Enable override of coarse/fine codes to the e-MMC* interface DLLs; 0; use coarse/fine codes from Master DLL; 1: use coarse/fine codes from this register
28:24	0x0 RW	**Reserved (reserved):** Reserved
23:20	0x0 RW	**sd_sdl_fine_override:** Fine code override value for SD slave delay lines
19:16	0x0 RW	**sdio_sdl_fine_override:** Fine code override value for SDIO slave delay lines
15:12	0x0 RW	**emmc_sdl_fine_override:** Fine code override value for e-MMC* slave delay lines
11:8	0x0 RW	**sd_sdl_coarse_override:** Coarse code override value for SD slave delay lines
7:4	0x0 RW	**sdio_sdl_coarse_override:** Coarse code override value for SDIO slave delay lines
3:0	0x0 RW	**emmc_sdl_coarse_override:** Coarse code override value for e-MMC* slave delay lines

10.6.34 SDR104 Mode Output Delay Selects (sdr104_mode_output_delay_selects)—Offset 604h

This register is used to select the tap delays for the Tx slave delay lines in SDR104 mode

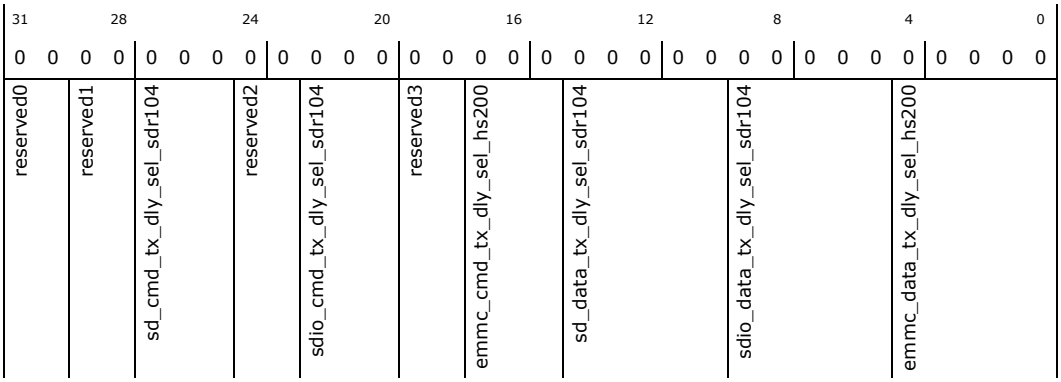
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 604h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**Reserved0 (reserved0):** Reserved0
29:28	0x0 RW	**Reserved1 (reserved1):** Reserved1
27:25	0x0 RW	**sd_cmd_tx_dly_sel_sdr104:** SD interface CMD output delay tap select for SDR104 mode
24:23	0x0 RW	**Reserved2 (reserved2):** Reserved2
22:20	0x0 RW	**sdio_cmd_tx_dly_sel_sdr104:** SDIO interface CMD output delay tap select for SDR104 mode
19:18	0x0 RW	**Reserved3 (reserved3):** Reserved3
17:15	0x0 RW	**emmc_cmd_tx_dly_sel_hs200:** e-MMC* interface CMD output delay tap select for HS200 mode
14:10	0x0 RW	**sd_data_tx_dly_sel_sdr104:** SD interface DATA output delay tap select for SDR104 mode
9:5	0x0 RW	**sdio_data_tx_dly_sel_sdr104:** SDIO interface DATA output delay tap select for SDR104 mode
4:0	0x0 RW	**emmc_data_tx_dly_sel_hs200:** e-MMC* interface DATA output delay tap select for HS200 mode

10.6.35 SDR50 Mode Output Delay Selects (sdr50_mode_output_delay_selects)—Offset 608h

This register is used to select the tap delays for the Tx slave delay lines in SDR50 mode

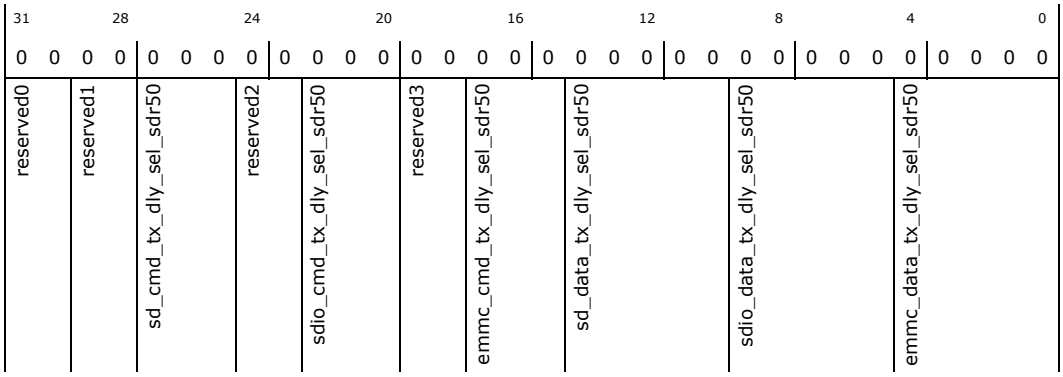
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 608h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**Reserved0 (reserved0):** Reserved0
29:28	0x0 RW	**Reserved1 (reserved1):** Reserved1
27:25	0x0 RW	**sd_cmd_tx_dly_sel_sdr50:** SD interface CMD output delay tap select for SDR50 mode
24:23	0x0 RW	**Reserved2 (reserved2):** Reserved2
22:20	0x0 RW	**sdio_cmd_tx_dly_sel_sdr50:** SDIO interface CMD output delay tap select for SDR50 mode
19:18	0x0 RW	**Reserved3 (reserved3):** Reserved3
17:15	0x0 RW	**emmc_cmd_tx_dly_sel_sdr50:** e-MMC* interface CMD output delay tap select for SDR50 mode
14:10	0x0 RW	**sd_data_tx_dly_sel_sdr50:** SD interface DATA output delay tap select for SDR50 mode
9:5	0x0 RW	**sdio_data_tx_dly_sel_sdr50:** SDIO interface DATA output delay tap select for SDR50 mode
4:0	0x0 RW	**emmc_data_tx_dly_sel_sdr50:** e-MMC* interface DATA output delay tap select for SDR50 mode

10.6.36 DDR50 Mode Output Delay Selects (ddr50_mode_output_delay_selects)—Offset 60Ch

This register is used to select the tap delays for the Tx slave delay lines in DDR50 mode

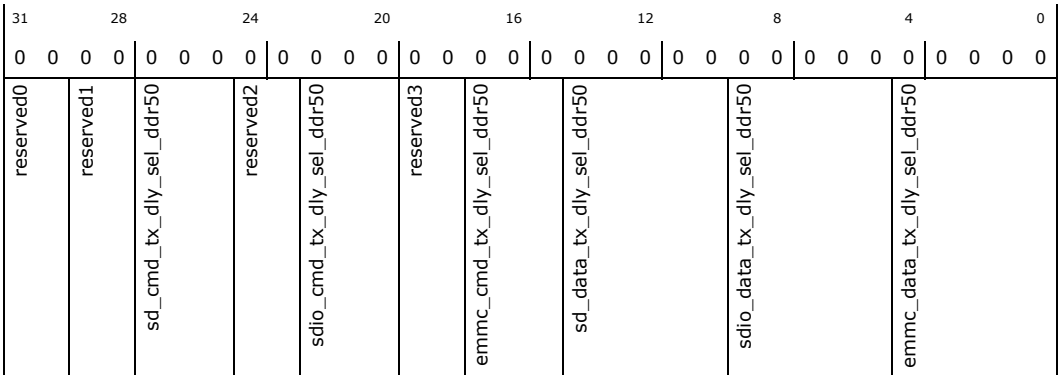
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 60Ch

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**Reserved0 (reserved0):** Reserved0
29:28	0x0 RW	**Reserved1 (reserved1):** Reserved1
27:25	0x0 RW	**sd_cmd_tx_dly_sel_ddr50:** SD interface CMD output delay tap select for DDR50 mode
24:23	0x0 RW	**Reserved2 (reserved2):** Reserved2
22:20	0x0 RW	**sdio_cmd_tx_dly_sel_ddr50:** SDIO interface CMD output delay tap select for DDR50 mode
19:18	0x0 RW	**Reserved3 (reserved3):** Reserved3
17:15	0x0 RW	**emmc_cmd_tx_dly_sel_ddr50:** e-MMC* interface CMD output delay tap select for DDR50 mode
14:10	0x0 RW	**sd_data_tx_dly_sel_ddr50:** SD interface DATA output delay tap select for DDR50 mode
9:5	0x0 RW	**sdio_data_tx_dly_sel_ddr50:** SDIO interface DATA output delay tap select for DDR50 mode
4:0	0x0 RW	**emmc_data_tx_dly_sel_ddr50:** e-MMC* interface DATA output delay tap select for DDR50 mode

10.6.37 High Speed Mode Output Delay Selects (hs_mode_output_delay_selects)—Offset 610h

This register is used to select the tap delays for the Tx slave delay lines in High Speed mode

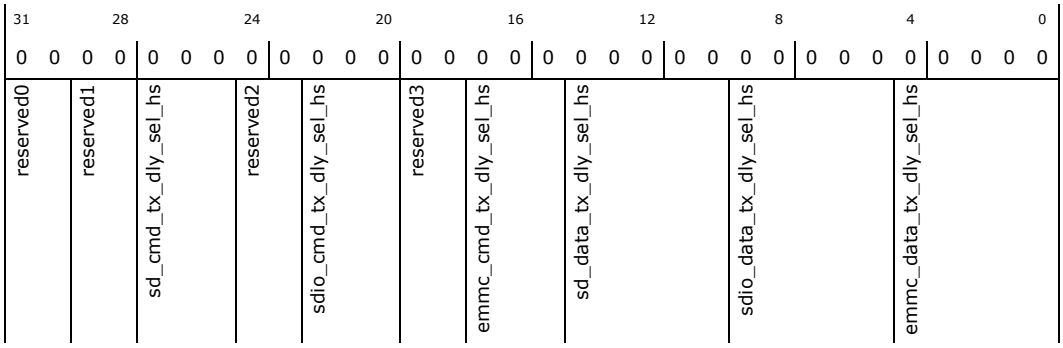
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 610h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**Reserved0 (reserved0):** Reserved0
29:28	0x0 RW	**Reserved1 (reserved1):** Reserved1
27:25	0x0 RW	**sd_cmd_tx_dly_sel_hs:** SD interface CMD output delay tap select for High Speed mode
24:23	0x0 RW	**Reserved2 (reserved2):** Reserved2
22:20	0x0 RW	**sdio_cmd_tx_dly_sel_hs:** SDIO interface CMD output delay tap select for High Speed mode
19:18	0x0 RW	**Reserved3 (reserved3):** Reserved3
17:15	0x0 RW	**emmc_cmd_tx_dly_sel_hs:** e-MMC* interface CMD output delay tap select for High Speed mode
14:10	0x0 RW	**sd_data_tx_dly_sel_hs:** SD interface DATA output delay tap select for High Speed mode
9:5	0x0 RW	**sdio_data_tx_dly_sel_hs:** SDIO interface DATA output delay tap select for High Speed mode
4:0	0x0 RW	**emmc_data_tx_dly_sel_hs:** e-MMC* interface DATA output delay tap select for High Speed mode

10.6.38 Normal Mode Output Delay Selects (normal_mode_output_delay_selects)—Offset 614h

This register is used to select the tap delays for the Tx slave delay lines in Normal mode

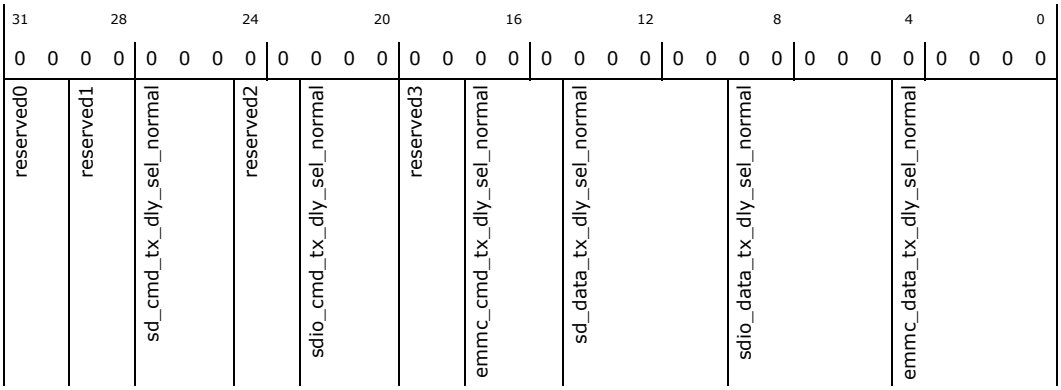
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 614h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**Reserved0 (reserved0):** Reserved0
29:28	0x0 RW	**Reserved1 (reserved1):** Reserved1
27:25	0x0 RW	**sd_cmd_tx_dly_sel_normal:** SD interface CMD output delay tap select for Normal mode
24:23	0x0 RW	**Reserved2 (reserved2):** Reserved2
22:20	0x0 RW	**sdio_cmd_tx_dly_sel_normal:** SDIO interface CMD output delay tap select for Normal mode
19:18	0x0 RW	**Reserved3 (reserved3):** Reserved3
17:15	0x0 RW	**emmc_cmd_tx_dly_sel_normal:** e-MMC* interface CMD output delay tap select for Normal mode
14:10	0x0 RW	**sd_data_tx_dly_sel_normal:** SD interface DATA output delay tap select for Normal mode
9:5	0x0 RW	**sdio_data_tx_dly_sel_normal:** SDIO interface DATA output delay tap select for Normal mode
4:0	0x0 RW	**emmc_data_tx_dly_sel_normal:** e-MMC* interface DATA output delay tap select for Normal mode

10.6.39 Master Delay Line Override Register (master_delay_line_override)—Offset 618h

This register is used to select the tap delays for the Tx slave delay lines in DDR50 mode

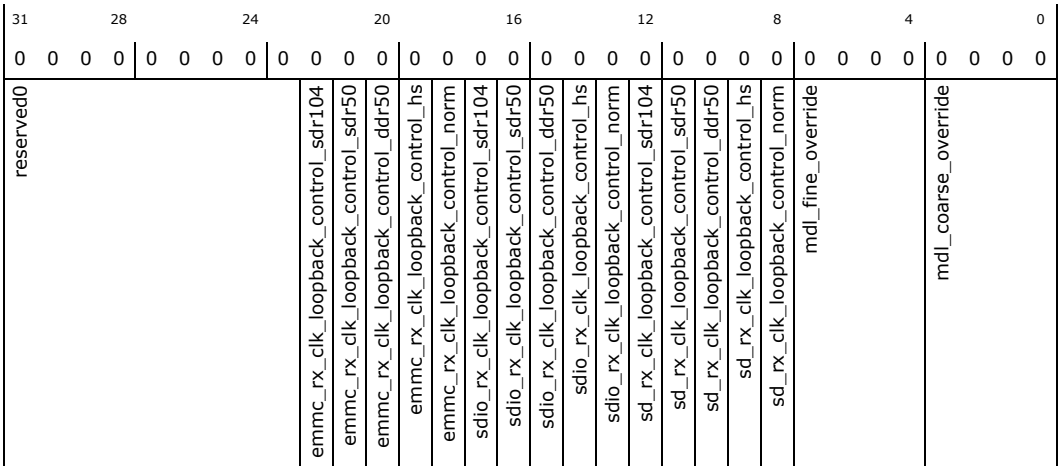
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 618h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:23	0x0 RW	**Reserved (reserved0):** Reserved
22	0x0 RW	**emmc_rx_clk_loopback_control_sdr104:** 0: (default) use external clock loopback; 1: use internal clock loopback
21	0x0 RW	**emmc_rx_clk_loopback_control_sdr50:** 0: (default) use external clock loopback; 1: use internal clock loopback
20	0x0 RW	**emmc_rx_clk_loopback_control_ddr50:** 0: (default) use external clock loopback; 1: use internal clock loopback
19	0x0 RW	**emmc_rx_clk_loopback_control_hs:** 0: (default) use external clock loopback; 1: use internal clock loopback
18	0x0 RW	**emmc_rx_clk_loopback_control_norm:** 0: (default) use external clock loopback; 1: use internal clock loopback
17	0x0 RW	**sdio_rx_clk_loopback_control_sdr104:** 0: (default) use external clock loopback; 1: use internal clock loopback
16	0x0 RW	**sdio_rx_clk_loopback_control_sdr50:** 0: (default) use external clock loopback; 1: use internal clock loopback
15	0x0 RW	**sdio_rx_clk_loopback_control_ddr50:** 0: (default) use external clock loopback; 1: use internal clock loopback
14	0x0 RW	**sdio_rx_clk_loopback_control_hs:** 0: (default) use external clock loopback; 1: use internal clock loopback
13	0x0 RW	**emmc_rx_clk_loopback_control_norm (sdio_rx_clk_loopback_control_norm):** 0: (default) use external clock loopback; 1: use internal clock loopback
12	0x0 RW	**sd_rx_clk_loopback_control_sdr104:** 0: (default) use external clock loopback; 1: use internal clock loopback
11	0x0 RW	**sd_rx_clk_loopback_control_sdr50:** 0: (default) use external clock loopback; 1: use internal clock loopback
10	0x0 RW	**sd_rx_clk_loopback_control_ddr50:** 0: (default) use external clock loopback; 1: use internal clock loopback
9	0x0 RW	**sd_rx_clk_loopback_control_hs:** 0: (default) use external clock loopback; 1: use internal clock loopback

Bit Range	Default and Access	Field Name (ID): Description
8	0x0 RW	**emmc_rx_clk_loopback_control_norm (sd_rx_clk_loopback_control_norm):** 0: (default) use external clock loopback; 1: use internal clock loopback
7:4	0x0 RW	**mdl_fine_override:** Fine code override for master delay line
3:0	0x0 RW	**mdl_coarse_override:** Coarse code override for master delay line

10.6.40 Master DLL Status Register (master_dll_status)—Offset 61Ch

This register is used to provide status for the Master DLL

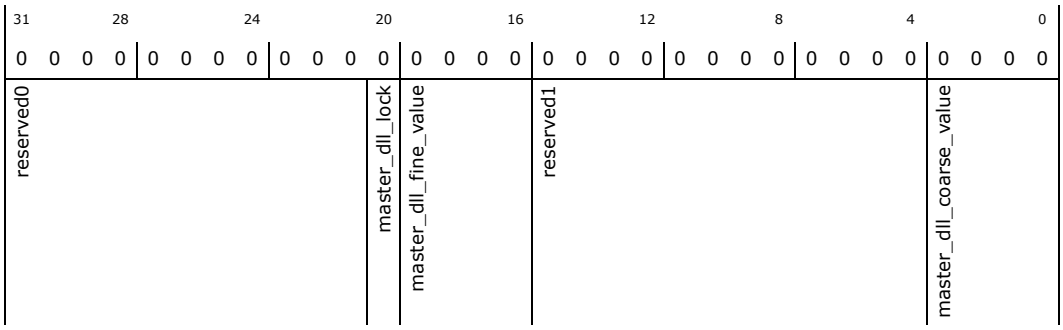
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 61Ch

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:21	0x0 RO	**Reserved (reserved0):** Reserved
20	0x0 RO	**master_dll_lock:** Lock signal from Master DLL. Used for debug only.
19:16	0x0 RO	**master_dll_fine_value:** Fine code from Master DLL. Used for debug only.
15:4	0x0 RO	**Reserved (reserved1):** Reserved
3:0	0x0 RO	**master_dll_coarse_value:** Coarse code from Master DLL. Used for debug only.

10.6.41 Master DLL Control Register (master_dll_control)—Offset 620h

This register is used to configure and control the Master DLL

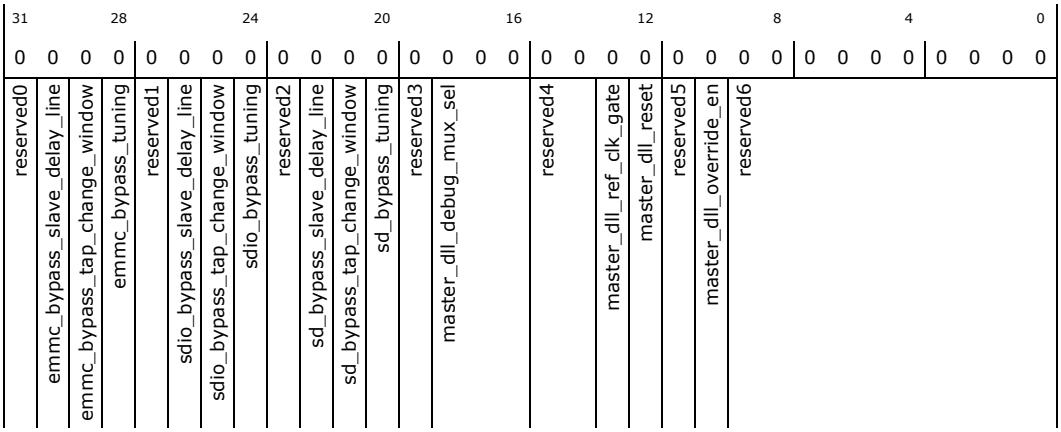
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 620h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**Reserved0 (reserved0):** Reserved0
30	0x0 RW	**emmc_bypass_slave_delay_line:** If set, completely bypasses the Rx Slave Delay Line.
29	0x0 RW	**emmc_bypass_tap_change_window:** Setting this bit forces the Rx clock to be gated; it is used when manually changing tap select values to prevent glitches from appearing on the Rx clock.
28	0x0 RW	**emmc_bypass_tuning:** If set, bypasses tuning control from the host controller on the Rx Slave Delay Line; all tap selects will come from the Receive Delay Select registers.
27	0x0 RW	**Reserved1 (reserved1):** Reserved1
26	0x0 RW	**sdio_bypass_slave_delay_line:** If set, completely bypasses the Rx Slave Delay Line.
25	0x0 RW	**sdio_bypass_tap_change_window:** Setting this bit forces the Rx clock to be gated; it is used when manually changing tap select values to prevent glitches from appearing on the Rx clock.
24	0x0 RW	**sdio_bypass_tuning:** If set, bypasses tuning control from the host controller on the Rx Slave Delay Line; all tap selects will come from the Receive Delay Select registers.
23	0x0 RW	**Reserved2 (reserved2):** Reserved2

Bit Range	Default and Access	Field Name (ID): Description
22	0x0 RW	**sd_bypass_slave_delay_line:** If set, completely bypasses the Rx Slave Delay Line.
21	0x0 RW	**sd_bypass_tap_change_window:** Setting this bit forces the Rx clock to be gated; it is used when manually changing tap select values to prevent glitches from appearing on the Rx clock.
20	0x0 RW	**sd_bypass_tuning:** If set, bypasses tuning control from the host controller on the Rx Slave Delay Line; all tap selects will come from the Receive Delay Select registers.
19	0x0 RW	**Reserved3 (reserved3):** Reserved3
18:16	0x0 RW	**master_dll_debug_mux_sel:** This is used to select which set of signals appears on the Master DLL debug outputs. 0xx: more, less; 100: fine_clk, fine_clk; 101: coarse_clk, fine_clk; 110: ref_clk, fine_clk; 111: fdbk_clk, fine_clk
15:14	0x0 RW	**Reserved4 (reserved4):** Reserved4
13	0x0 RW	**master_dll_ref_clk_gate:** When set, this bit gates the reference clock to the Master DLL.
12	0x0 RW	**master_dll_reset:** Setting this bit resets the Master DLL. 0: active; 1: reset
11	0x0 RW	**Reserved5 (reserved5):** Reserved5
10	0x0 RW	**master_dll_override_en:** 0: Send coarse/fine codes from Master DLL to slave delay lines; 1: send coarse/fine codes from Master Delay Line Override Register to slave delay lines.
9:0	0x0 RW	**Reserved6 (reserved6):** Reserved6

10.6.42 e-MMC* Interface Receive Delay Select Register (emmc_interface_receive_delay_select)—Offset 624h

This register is used to select the tap on the Rx slave delay line

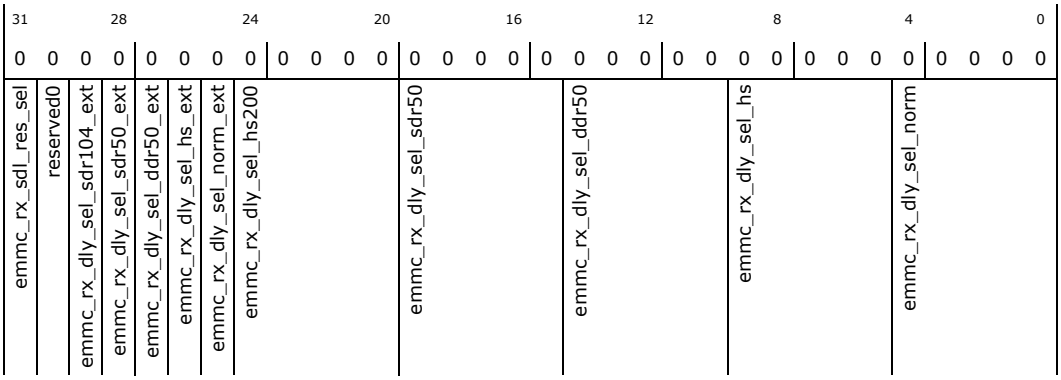
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 624h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**emmc_rx_sdl_res_sel:** e-MMC* Rx Slave Delay Line Resolution Select; 0: (default) 250 ps resolution; 1: 500 ps resolution; intended for debug use only
30	0x0 RW	**Reserved0 (reserved0):** Reserved0
29	0x0 RW	**emmc_rx_dly_sel_sdr104_ext:** e-MMC* input tap delay extension bit for HS200 mode. Used only if auto-tuning is disabled.
28	0x0 RW	**emmc_rx_dly_sel_sdr50_ext:** e-MMC* input tap delay extension bit for SDR50 mode. Used only if auto-tuning is disabled. **Note**: SDR50 is not a supported mode in e-MMC*.
27	0x0 RW	**emmc_rx_dly_sel_ddr50_ext:** e-MMC* input tap delay extension bit for DDR50 mode. Used only if auto-tuning is disabled.
26	0x0 RW	**emmc_rx_dly_sel_hs_ext:** e-MMC* input tap delay extension bit for DDR50 mode. Used only if auto-tuning is disabled.
25	0x0 RW	**emmc_rx_dly_sel_norm_ext:** e-MMC* input tap delay extension bit for Normal mode. Used only if auto-tuning is disabled.
24:20	0x0 RW	**emmc_rx_dly_sel_hs200:** e-MMC* interface input tap delay select for HS200 mode. Used only if auto-tuning is disabled.
19:15	0x0 RW	**emmc_rx_dly_sel_sdr50:** e-MMC* interface input tap delay select for SDR50 mode. Used only if auto-tuning is disabled. **Note**: SDR50 is not a supported mode in e-MMC*.
14:10	0x0 RW	**emmc_rx_dly_sel_ddr50:** e-MMC* interface input tap delay select for DDR50 mode.
9:5	0x0 RW	**emmc_rx_dly_sel_hs:** e-MMC* interface input tap delay select for High Speed mode.
4:0	0x0 RW	**emmc_rx_dly_sel_norm:** e-MMC* interface input tap delay select for Normal mode.

10.6.43 SDIO Interface Receive Delay Select Register (sdio_interface_receive_delay_select)—Offset 628h

This register is used to select the tap on the Rx slave delay line

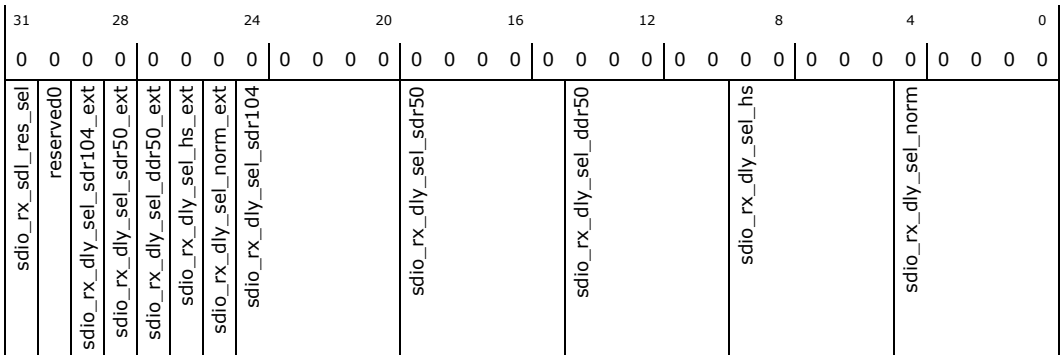
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 628h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**sdio_rx_sdl_res_sel:** SDIO Rx Slave Delay Line Resolution Select; 0: (default) 250 ps resolution; 1: 500 ps resolution; intended for debug use only
30	0x0 RW	**Reserved0 (reserved0):** Reserved0
29	0x0 RW	**sdio_rx_dly_sel_sdr104_ext:** SDIO input tap delay extension bit for SDR104 mode. Used only if auto-tuning is disabled.
28	0x0 RW	**sdio_rx_dly_sel_sdr50_ext:** SDIO input tap delay extension bit for SDR50 mode. Used only if auto-tuning is disabled.
27	0x0 RW	**sdio_rx_dly_sel_ddr50_ext:** SDIO input tap delay extension bit for DDR50 mode. Used only if auto-tuning is disabled.
26	0x0 RW	**sdio_rx_dly_sel_hs_ext:** SDIO input tap delay extension bit for DDR50 mode. Used only if auto-tuning is disabled.
25	0x0 RW	**sdio_rx_dly_sel_norm_ext:** SDIO input tap delay extension bit for Normal mode. Used only if auto-tuning is disabled.
24:20	0x0 RW	**sdio_rx_dly_sel_sdr104:** SDIO interface input tap delay select for SDR104 mode. Used only if auto-tuning is disabled.
19:15	0x0 RW	**sdio_rx_dly_sel_sdr50:** SDIO interface input tap delay select for SDR50 mode. Used only if auto-tuning is disabled.
14:10	0x0 RW	**sdio_rx_dly_sel_ddr50:** SDIO interface input tap delay select for DDR50 mode.
9:5	0x0 RW	**sdio_rx_dly_sel_hs:** SDIO interface input tap delay select for High Speed mode.
4:0	0x0 RW	**sdio_rx_dly_sel_norm:** SDIO interface input tap delay select for Normal mode.

10.6.44 SD Interface Receive Delay Select Register (sd_interface_receive_delay_select)—Offset 62Ch

This register is used to select the tap on the Rx slave delay line

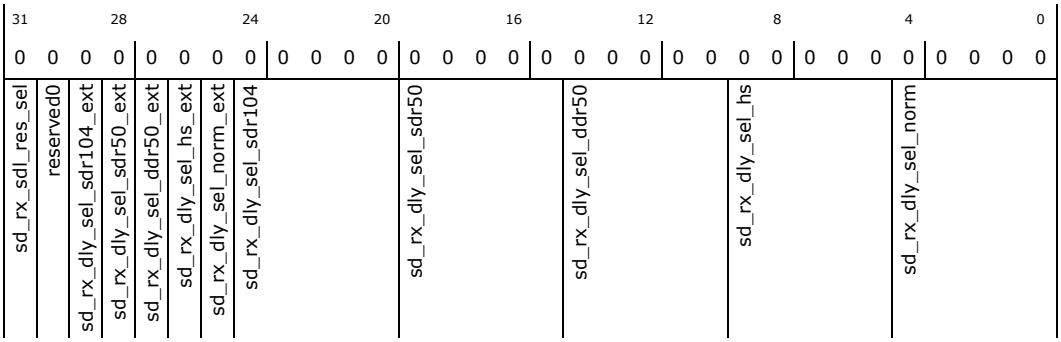
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 62Ch

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**sd_rx_sdl_res_sel:** SDIO Rx Slave Delay Line Resolution Select; 0: (default) 250 ps resolution; 1: 500 ps resolution; intended for debug use only
30	0x0 RW	**Reserved0 (reserved0):** Reserved0
29	0x0 RW	**sd_rx_dly_sel_sdr104_ext:** SD input tap delay extension bit for SDR104 mode. Used only if auto-tuning is disabled.
28	0x0 RW	**sd_rx_dly_sel_sdr50_ext:** SD input tap delay extension bit for SDR50 mode. Used only if auto-tuning is disabled.
27	0x0 RW	**sd_rx_dly_sel_ddr50_ext:** SD input tap delay extension bit for DDR50 mode. Used only if auto-tuning is disabled.
26	0x0 RW	**sd_rx_dly_sel_hs_ext:** SD input tap delay extension bit for DDR50 mode. Used only if auto-tuning is disabled.
25	0x0 RW	**sd_rx_dly_sel_norm_ext:** SD input tap delay extension bit for Normal mode. Used only if auto-tuning is disabled.
24:20	0x0 RW	**sd_rx_dly_sel_sdr104:** SD interface input tap delay select for SDR104 mode. Used only if auto-tuning is disabled.
19:15	0x0 RW	**sd_rx_dly_sel_sdr50:** SD interface input tap delay select for SDR50 mode. Used only if auto-tuning is disabled.
14:10	0x0 RW	**sd_rx_dly_sel_ddr50:** SD interface input tap delay select for DDR50 mode.
9:5	0x0 RW	**sd_rx_dly_sel_hs:** SD interface input tap delay select for High Speed mode.
4:0	0x0 RW	**sd_rx_dly_sel_norm:** SD interface input tap delay select for Normal mode.

10.6.45 GPIO Broadcast Data Mask bit Register (gpio_family_bw_mask_31_0)—Offset 1000h

Write Mask that masks bit by bit the data written to BWData

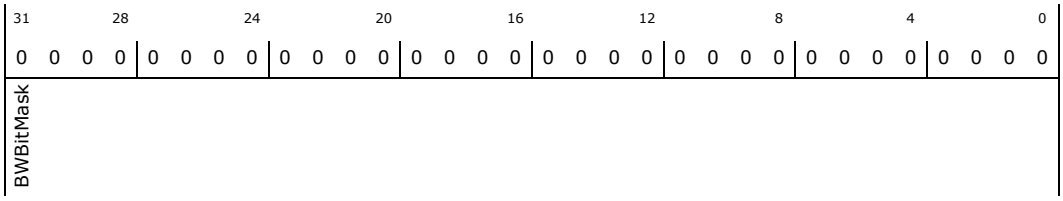
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1000h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**BWBitMask:** Reserved.

10.6.46 GPIO Broadcast Data Register (gpio_family_bw_data_31_0)—Offset 1004h

Broadcast Write Data

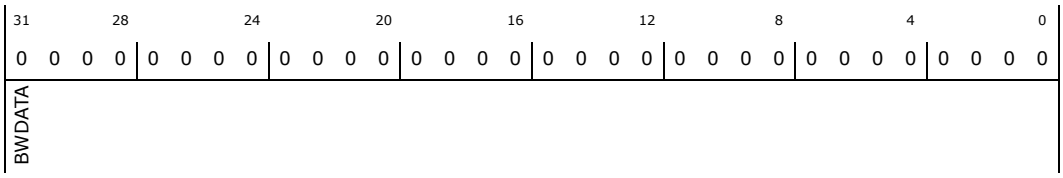
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1004h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 WO	**BWDATA:** Reserved.

10.6.47 gpio_family_broadcast_reg_mask #0 (gpio_family_broadcast_reg_mask_0)—Offset 1008h

Family Broadcast Register Masking

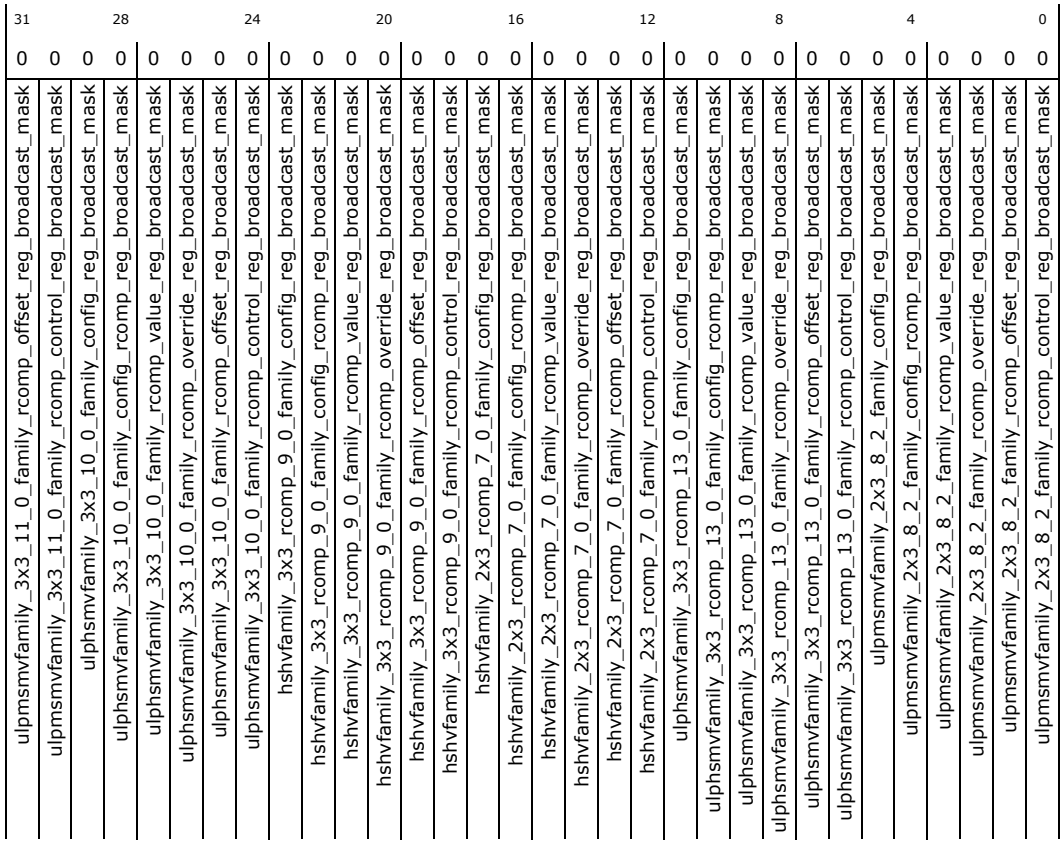
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1008h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**ulpmsmvfamily_3x3_11_0_family_rcomp_offset_reg_broadcast_mask:** Reserved.
30	0x0 RW	**ulpmsmvfamily_3x3_11_0_family_rcomp_control_reg_broadcast_mask:** Reserved.
29	0x0 RW	**ulphsmvfamily_3x3_10_0_family_config_reg_broadcast_mask:** Reserved.
28	0x0 RW	**ulphsmvfamily_3x3_10_0_family_config_rcomp_reg_broadcast_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
27	0x0 RW	**ulphsmvfamily_3x3_10_0_family_rcomp_value_reg_broadcast_mask:** Reserved.
26	0x0 RW	**ulphsmvfamily_3x3_10_0_family_rcomp_override_reg_broadcast_mask:** Reserved.
25	0x0 RW	**ulphsmvfamily_3x3_10_0_family_rcomp_offset_reg_broadcast_mask:** Reserved.
24	0x0 RW	**ulphsmvfamily_3x3_10_0_family_rcomp_control_reg_broadcast_mask:** Reserved.
23	0x0 RW	**hshvfamily_3x3_rcomp_9_0_family_config_reg_broadcast_mask:** Reserved.
22	0x0 RW	**hshvfamily_3x3_rcomp_9_0_family_config_rcomp_reg_broadcast_mask:** Reserved.
21	0x0 RW	**hshvfamily_3x3_rcomp_9_0_family_rcomp_value_reg_broadcast_mask:** Reserved.
20	0x0 RW	**hshvfamily_3x3_rcomp_9_0_family_rcomp_override_reg_broadcast_mask:** Reserved.
19	0x0 RW	**hshvfamily_3x3_rcomp_9_0_family_rcomp_offset_reg_broadcast_mask:** Reserved.
18	0x0 RW	**hshvfamily_3x3_rcomp_9_0_family_rcomp_control_reg_broadcast_mask:** Reserved.
17	0x0 RW	**hshvfamily_2x3_rcomp_7_0_family_config_reg_broadcast_mask:** Reserved.
16	0x0 RW	**hshvfamily_2x3_rcomp_7_0_family_config_rcomp_reg_broadcast_mask:** Reserved.
15	0x0 RW	**hshvfamily_2x3_rcomp_7_0_family_rcomp_value_reg_broadcast_mask:** Reserved.
14	0x0 RW	**hshvfamily_2x3_rcomp_7_0_family_rcomp_override_reg_broadcast_mask:** Reserved.
13	0x0 RW	**hshvfamily_2x3_rcomp_7_0_family_rcomp_offset_reg_broadcast_mask:** Reserved.
12	0x0 RW	**hshvfamily_2x3_rcomp_7_0_family_rcomp_control_reg_broadcast_mask:** Reserved.
11	0x0 RW	**ulphsmvfamily_3x3_rcomp_13_0_family_config_reg_broadcast_mask:** Reserved.
10	0x0 RW	**ulphsmvfamily_3x3_rcomp_13_0_family_config_rcomp_reg_broadcast_mask:** Reserved.
9	0x0 RW	**ulphsmvfamily_3x3_rcomp_13_0_family_rcomp_value_reg_broadcast_mask:** Reserved.
8	0x0 RW	**ulphsmvfamily_3x3_rcomp_13_0_family_rcomp_override_reg_broadcast_mask:** Reserved.
7	0x0 RW	**ulphsmvfamily_3x3_rcomp_13_0_family_rcomp_offset_reg_broadcast_mask:** Reserved.
6	0x0 RW	**ulphsmvfamily_3x3_rcomp_13_0_family_rcomp_control_reg_broadcast_mask:** Reserved.
5	0x0 RW	**ulpmsmvfamily_2x3_8_2_family_config_reg_broadcast_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
4	0x0 RW	**ulpmsmvfamily_2x3_8_2_family_config_rcomp_reg_broadcast_mask:** Reserved.
3	0x0 RW	**ulpmsmvfamily_2x3_8_2_family_rcomp_value_reg_broadcast_mask:** Reserved.
2	0x0 RW	**ulpmsmvfamily_2x3_8_2_family_rcomp_override_reg_broadcast_mask:** Reserved.
1	0x0 RW	**ulpmsmvfamily_2x3_8_2_family_rcomp_offset_reg_broadcast_mask:** Reserved.
0	0x0 RW	**ulpmsmvfamily_2x3_8_2_family_rcomp_control_reg_broadcast_mask:** Reserved.

10.6.48 gpio_family_broadcast_reg_mask #1 (gpio_family_broadcast_reg_mask_1)—Offset 100Ch

Family Broadcast Register Masking

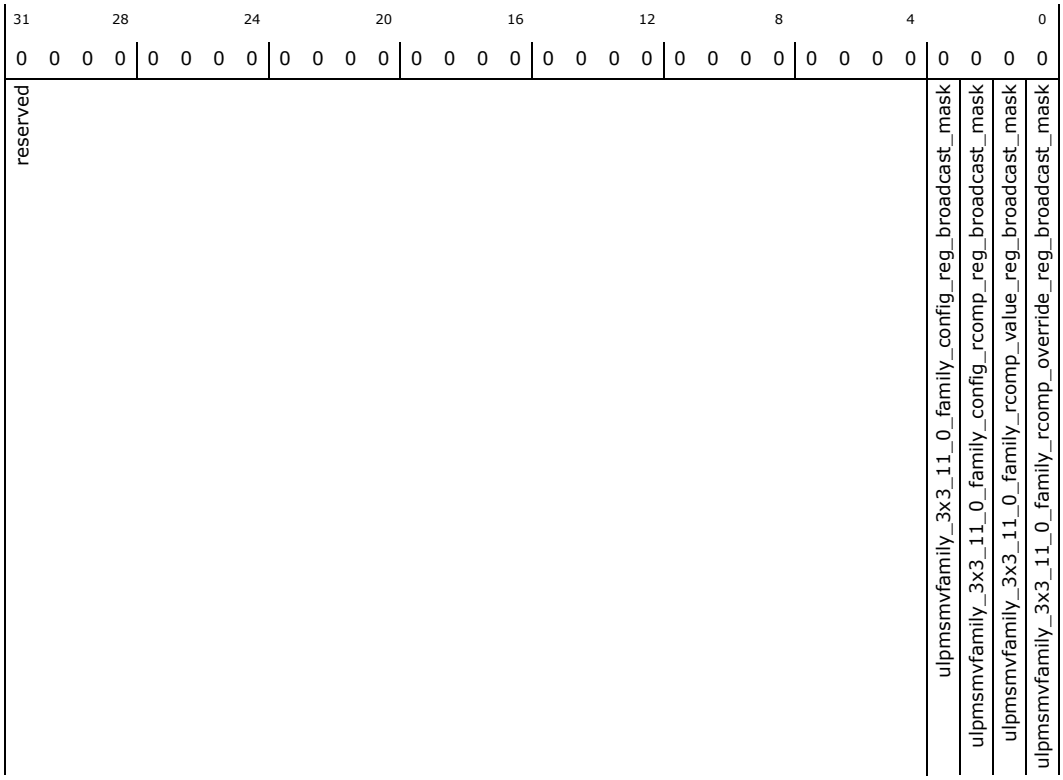
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 100Ch

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:4	0x0 RW	**reserved:** Reserved.
3	0x0 RW	**ulpmsmvfamily_3x3_11_0_family_config_reg_broadcast_mask:** Reserved.
2	0x0 RW	**ulpmsmvfamily_3x3_11_0_family_config_rcomp_reg_broadcast_mask:** Reserved.
1	0x0 RW	**ulpmsmvfamily_3x3_11_0_family_rcomp_value_reg_broadcast_mask:** Reserved.
0	0x0 RW	**ulpmsmvfamily_3x3_11_0_family_rcomp_override_reg_broadcast_mask:** Reserved.

10.6.49 family_config_rcomp_reg (ulpmsmvfamily_2x3_8_2_family_config_rcomp_reg)—Offset 1090h

GPIO Family RCOMP Register

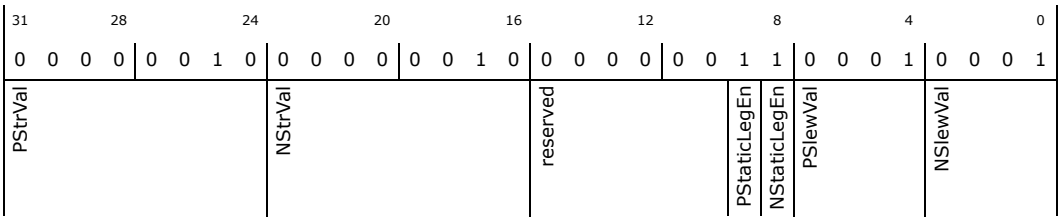
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1090h

Op Codes:
h - Read, h - Write

Default: 02020311h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x2 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x2 RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable
7:4	0x1 RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.
3:0	0x1 RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.6.50 gpio_family_configuration_register (ulpmsmvfamily_2x3_8_2_family_config_reg)—Offset 1094h

GPIO Family CFIO Configuration Register

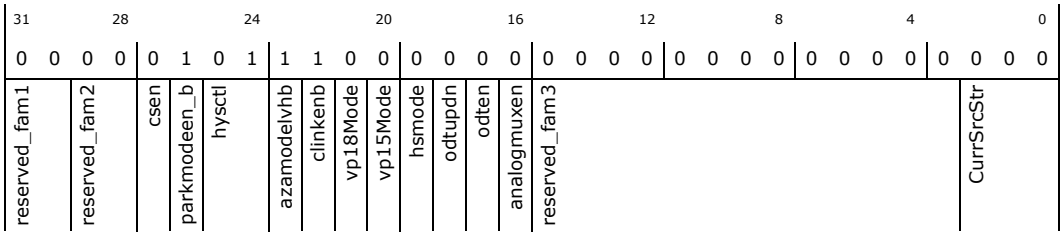
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1094h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x1 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.6.51 RCOMP Control Register (ulphsmvfamily_3x3_rcomp_13_0_family_rcomp_control_reg)—Offset 1100h

RCOMP Control Register

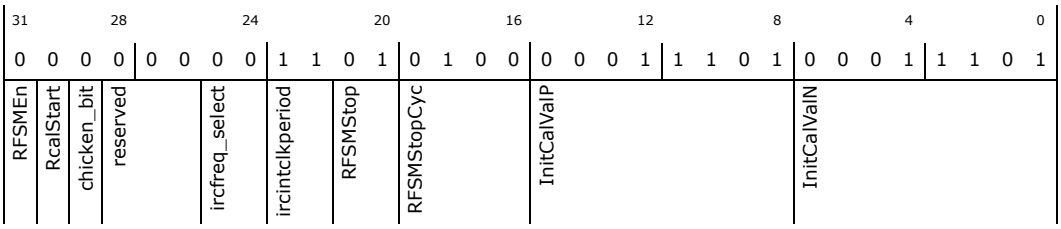
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1100h

Op Codes:
h - Read, h - Write

Default: 00D41D1Dh



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**RCOMP FSM Enable (RFSMEn):** 0 = state machine disabled (clock gated) 1 = state machine enabled It is important to have this bit enabled in order for all internal clocks inside the RCOMP FSM to run.
30	0x0 RW	**RCOMP Calibration Start (RcalStart):** When set to 1 this bit triggers the RCOMP FSM to start hunting for the correct values for strength and slew. This bit should be cleared after calibration has finished. Before setting the RcalStart bit RFSMEn must have been asserted for at least 5 clock cycles. The first calibration takes 10us to complete and subsequent calibrations take 3us. Details of this process are in the CFIP RCOMP A Specification
29	0x0 RW	**RCOMP FSM Binary Chicken Bit (chicken_bit):** Toggling this bit Simulates a V1P8 Mode change. This will allow Binary re-calibration
28:26	0x0 RW	**reserved:** reserved
25:24	0x0 RW	**IRCCLK Frequency Select (ircfreq_select):** Clock ircclk frequency. This signals indicate what frequency ircclk is. This is used for 1 ms and 10 ms counters. 00 if clk input is 25 MHz (default, and SoC Clock) 01 if 50 MHz 10 if 100 MHz 11 if 125 MHz
23:22	0x3 RW	**IRC Internal Clock Period (ircintclkperiod):** To select rcomp clock period. This is the compensation clock frequency/period. Clock is derived from ircclk (which can be 25 MHz, 50 MHz, 100 MHz or 125 MHz user must set ircfreq_select[1:0] accordingly) 00 40 ns (64 ns for ircclk=125 MHz) 01 80 ns (96 ns for ircclk=125 MHz) 10 120 ns (128 ns for ircclk=125 MHz) (default) 11 160 ns (192 ns for ircclk=125 MHz)

Bit Range	Default and Access	Field Name (ID): Description
21:20	0x1 RW	**RCOMP FSM Stop Condition (RFSMStop):** RCOMP FSM Stop calibration condition. RCOMP FSM (Pull-up and Pull-down) will finish calibrating once orcpupen/orcpdnen toggles. The toggling indicates the compensation value has been reached. This option is programmable for toggle once (single edge), toggle twice (double edge), toggle thrice (triple edge) or forcing it to finish after a certain cycle (defined by RFSMStopCyc). 00b = single edge detect (10 or 01) 01b = double edge detect (101 or 010) (default) 10b = triple edge detect (1010 or 0101) 11b = stop after x cycles (depending on ircstpcyc[3:0] value -- This is meant for debug)
19:16	0x4 RW	**RCOMP FSM Stop Cycles (RFSMStopCyc):** Number of cycles to stop RCOMP FSM from searching for strength and slew settings. RFSMStop must be set to 11b for this option to take affect. 0000b = 0 cycle (illegal option) 0001b = 1 cycle (illegal option) 0010b = 2 cycles (illegal option) 0011b = 3 cycles (illegal option) 0100b = 4 cycles ... 1110b = 14 cycles 1111b = 15 cycles (maximum allowed) This is meant for debug.
15:8	0x1d RW	**Initial Pull-up Value (InitCalValP):** Initial pleg calibration value. RCOMP FSM will always start with this values for Pull-up calibration.
7:0	0x1d RW	**Initial Pull-down Value (InitCalValN):** Initial nleg calibration value. RCOMP FSM will always start with this values for Pull-down calibration.

10.6.52 RCOMP Offset Register (ulphsmvfamily_3x3_rcomp_13_0_family_rcomp_offset_reg)—Offset 1104h

RCOMP Offset Register

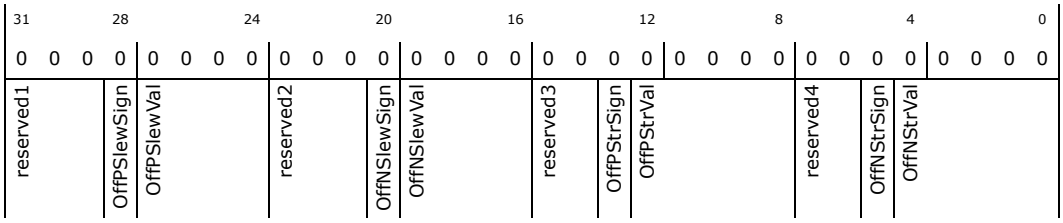
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1104h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:29	0x0 RW	**Reserved (reserved1):** Reserved

Bit Range	Default and Access	Field Name (ID): Description
28	0x0 RW	**Pull-up Offset Slew Sign (OffPSlewSign):** Sign Bit for PSlew Offset strength value.
27:24	0x0 RW	**Pull-up Slew Offset (OffPSlewVal):** Offset slew value for pleg.
23:21	0x0 RW	**Reserved (reserved2):** Reserved
20	0x0 RW	**Pull-down Offset Slew Sign (OffNSlewSign):** Sign Bit for NSlew Offset strength value.
19:16	0x0 RW	**Pull-down Slew Offset (OffNSlewVal):** Offset slew value for nleg.
15:14	0x0 RW	**Reserved (reserved3):** Reserved
13	0x0 RW	**Pull-up Offset Strength Sign (OffPStrSign):** Sign Bit for PStrength Offset value.
12:8	0x0 RW	**Pull-up Offset Strength Value (OffPStrVal):** PStrength Offset Value.
7:6	0x0 RW	**Reserved (reserved4):** Reserved
5	0x0 RW	**Pull-down Offset Strength Sign (OffNStrSign):** Sign Bit for NStrength Offset value.
4:0	0x0 RW	**Pull-down Offset Strength Value (OffNStrVal):** NStrength Offset Value.

10.6.53 RCOMP Override Register (ulphsmvfamily_3x3_rcomp_13_0_family_rcomp_override_reg)—Offset 1108h

RCOMP Override Register

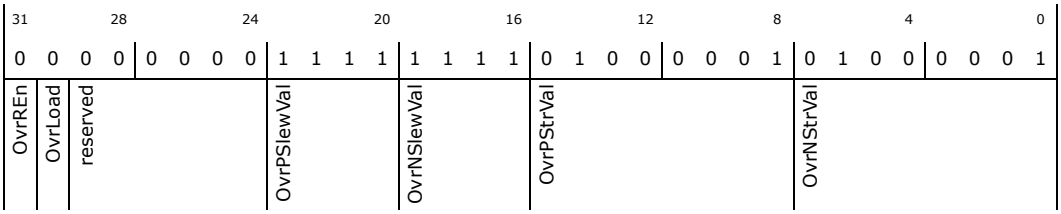
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1108h

Op Codes:
h - Read, h - Write

Default: 00FF4141h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**Override RCOMP Enable (OvrREn):** Override enable bit to override the strength and slew values driven by the RCOMP FSM. The override values are driven through config registers. 0 = Override Disable 1 = Override Enable
30	0x0 RW	**Override Load (OvrLoad):** Load the override values into the RCOMP FSM and drive these values to the CFIO buffer. This is only valid when OvrRen = 1. 0 = Unload Values 1 = Load Values to CFIO
29:24	0x0 RW	**reserved:** reserved
23:20	0xf RW	**Override P Slew Value (OvrPSlewVal):** Override slew values for Pull-up settings.
19:16	0xf RW	**Override N Slew Value (OvrNSlewVal):** Override slew values for Pull-down settings.
15:8	0x41 RW	**Override Pull-up Strength Value (OvrPStrVal):** Override strength value for Pull-up settings. Should be 50ohm typical corner.
7:0	0x41 RW	**Override Pull-down Strength Value (OvrNStrVal):** Override strength value for Pull-down settings. Should be 50ohm typical corner.

10.6.54 RCOMP Value Register (ulphsmvfamily_3x3_rcomp_13_0_family_rcomp_value_reg)—Offset 110Ch

RCOMP Value Register

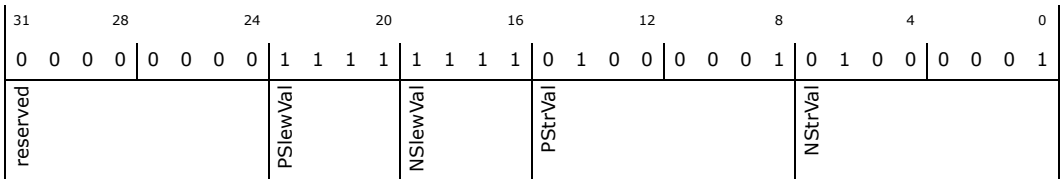
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 110Ch

Op Codes:
h - Read, h - Write

Default: 00FF4141h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RO	**reserved_fam1 (reserved):** reserved
23:20	0xf RO	**P Slew Value (PSlewVal):** P Slew values. Valid only after calibration is done.
19:16	0xf RO	**N Slew Value (NSlewVal):** N Slew values. Valid only after calibration is done.

Bit Range	Default and Access	Field Name (ID): Description
15:8	0x41 RO	**Pull-up Strength Value (PStrVal):** Compensation strength for pleg. This is valid only after calibration is done.
7:0	0x41 RO	**Pull-down Strength Value (NStrVal):** Compensation strength for nleg. This is valid only after calibration is done.

10.6.55 family_config_rcomp_reg (ulphsmvfamily_3x3_rcomp_13_0_family_config_rcomp_reg)—Offset 1110h

GPIO Family RCOMP Register

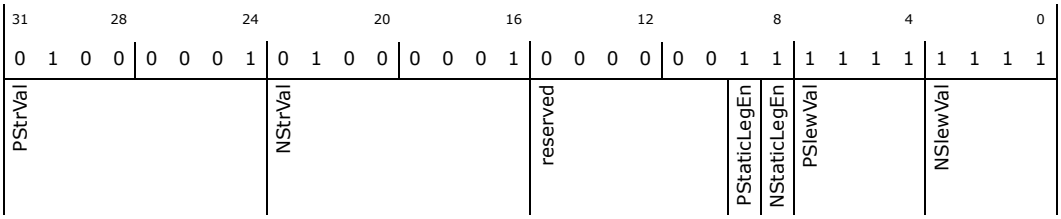
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1110h

Op Codes:
h - Read, h - Write

Default: 414103FFh



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x41 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x41 RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable
7:4	0xf RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.
3:0	0xf RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.6.56 gpio_family_configuration_register (ulphsmvfamily_3x3_rcomp_13_0_family_config_reg)—Offset 1114h

GPIO Family CFIO Configuration Register

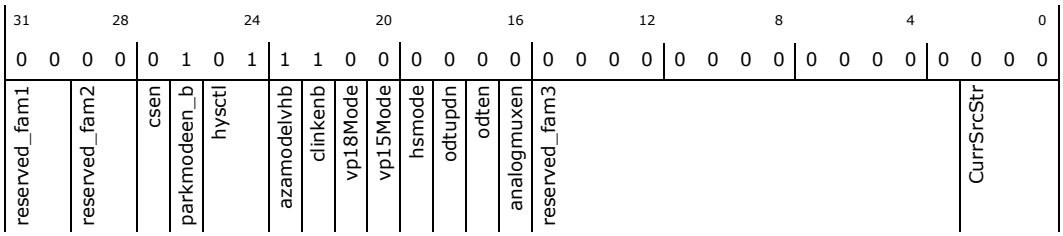
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1114h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x1 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.6.57 RCOMP Control Register (hshvfamily_2x3_rcomp_7_0_family_rcomp_control_reg)—Offset 1180h

RCOMP Control Register

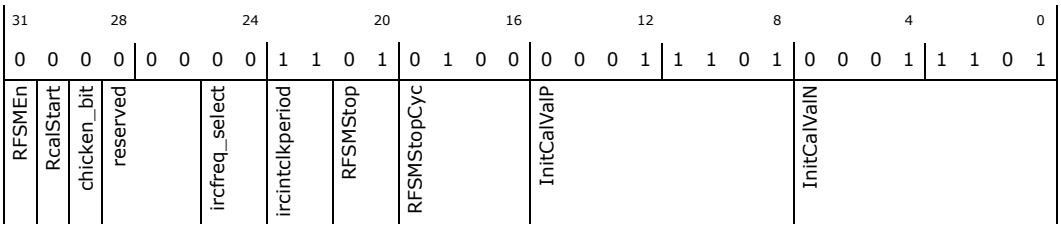
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1180h

Op Codes:
h - Read, h - Write

Default: 00D41D1Dh



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**RCOMP FSM Enable (RFSMEn):** 0 = state machine disabled (clock gated) 1 = state machine enabled It is important to have this bit enabled in order for all internal clocks inside the RCOMP FSM to run.
30	0x0 RW	**RCOMP Calibration Start (RcalStart):** When set to 1 this bit triggers the RCOMP FSM to start hunting for the correct values for strength and slew. This bit should be cleared after calibration has finished. Before setting the RcalStart bit RFSMEn must have been asserted for at least 5 clock cycles. The first calibration takes 10us to complete and subsequent calibrations take 3us. Details of this process are in the CFIP RCOMP A Specification
29	0x0 RW	**RCOMP FSM Binary Chicken Bit (chicken_bit):** Toggling this bit Simulates a V1P8 Mode change. This will allow Binary re-calibration
28:26	0x0 RW	**reserved:** reserved

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x0 RW	**IRCCLK Frequency Select (ircfreq_select):** Clock ircclk frequency. This signals indicate what frequency ircclk is. This is used for 1ms and 10ms counters. 00 if clk input is 25 MHz (default, and SoC Clock) 01 if 50 MHz 10 if 100 MHz 11 if 125 MHz
23:22	0x3 RW	**IRC Internal Clock Period (ircintclkperiod):** To select rcomp clock period. This is the compensation clock frequency/period. Clock is derived from ircclk (which can be 25 MHz, 50 MHz, 100 MHz or 125 MHz user must set ircfreq_select[1:0] accordingly) 00 40 ns (64 ns for ircclk=125 MHz) 01 80 ns (96 ns for ircclk=125 MHz) 10 120 ns (128 ns for ircclk=125 MHz) (default) 11 160 ns (192 ns for ircclk=125 MHz)
21:20	0x1 RW	**RCOMP FSM Stop Condition (RFSMStop):** RCOMP FSM Stop calibration condition. RCOMP FSM (Pull-up and Pull-down) will finish calibrating once orcpupen/orcpdnen toggles. The toggling indicates the compensation value has been reached. This option is programmable for toggle once (single edge), toggle twice (double edge), toggle thrice (triple edge) or forcing it to finish after a certain cycle (defined by RFSMStopCyc). 00b = single edge detect (10 or 01) 01b = double edge detect (101 or 010) (default) 10b = triple edge detect (1010 or 0101) 11b = stop after x cycles (depending on ircstpcyc[3:0] value -- This is meant for debug)
19:16	0x4 RW	**RCOMP FSM Stop Cycles (RFSMStopCyc):** Number of cycles to stop RCOMP FSM from searching for strength and slew settings. RFSMStop must be set to 11b for this option to take affect. 0000b = 0 cycle (illegal option) 0001b = 1 cycle (illegal option) 0010b = 2 cycles (illegal option) 0011b = 3 cycles (illegal option) 0100b = 4 cycles ... 1110b = 14 cycles 1111b = 15 cycles (maximum allowed) This is meant for debug.
15:8	0x1d RW	**Initial Pull-up Value (InitCalValP):** Initial pleg calibration value. RCOMP FSM will always start with this values for Pull-up calibration.
7:0	0x1d RW	**Initial Pull-down Value (InitCalValN):** Initial nleg calibration value. RCOMP FSM will always start with this values for Pull-down calibration.

10.6.58 RCOMP Offset Register (hshvfamily_2x3_rcomp_7_0_family_rcomp_offset_reg) —Offset 1184h

RCOMP Offset Register

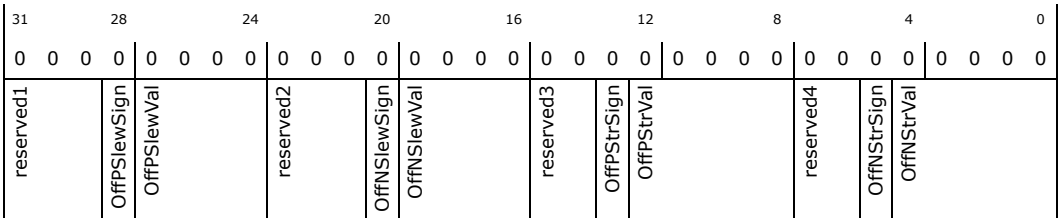
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1184h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:29	0x0 RW	**Reserved (reserved1):** Reserved
28	0x0 RW	**Pull-up Offset Slew Sign (OffPSlewSign):** Sign Bit for PSlew Offset strength value.
27:24	0x0 RW	**Pull-up Slew Offset (OffPSlewVal):** Offset slew value for pleg.
23:21	0x0 RW	**Reserved (reserved2):** Reserved
20	0x0 RW	**Pull-down Offset Slew Sign (OffNSlewSign):** Sign Bit for NSlew Offset strength value.
19:16	0x0 RW	**Pull-down Slew Offset (OffNSlewVal):** Offset slew value for nleg.
15:14	0x0 RW	**Reserved (reserved3):** Reserved
13	0x0 RW	**Pull-up Offset Strength Sign (OffPStrSign):** Sign Bit for PStrength Offset value.
12:8	0x0 RW	**Pull-up Offset Strength Value (OffPStrVal):** PStrength Offset Value.
7:6	0x0 RW	**Reserved (reserved4):** Reserved
5	0x0 RW	**Pull-down Offset Strength Sign (OffNStrSign):** Sign Bit for NStrength Offset value.
4:0	0x0 RW	**Pull-down Offset Strength Value (OffNStrVal):** NStrength Offset Value.

10.6.59 RCOMP Override Register (hshvfamily_2x3_rcomp_7_0_family_rcomp_override_reg)—Offset 1188h

RCOMP Override Register

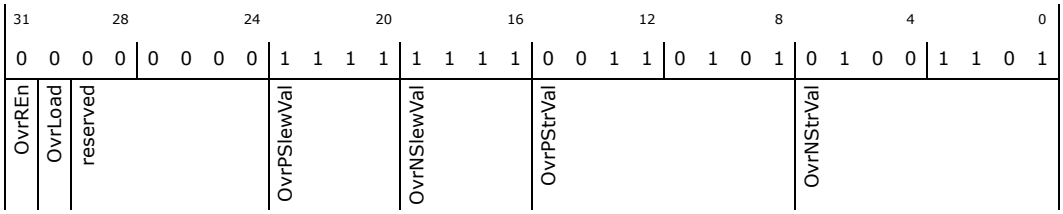
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1188h

Op Codes:
h - Read, h - Write

Default: 00FF354Dh



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**Override RCOMP Enable (OvrREn):** Override enable bit to override the strength and slew values driven by the RCOMP FSM. The override values are driven through config registers. 0 = Override Disable 1 = Override Enable
30	0x0 RW	**Override Load (OvrLoad):** Load the override values into the RCOMP FSM and drive these values to the CFIO buffer. This is only valid when OvrRen = 1. 0 = Unload Values 1 = Load Values to CFIO
29:24	0x0 RW	**reserved:** reserved
23:20	0xf RW	**Override P Slew Value (OvrPSlewVal):** Override slew values for Pull-up settings.
19:16	0xf RW	**Override N Slew Value (OvrNSlewVal):** Override slew values for Pull-down settings.
15:8	0x35 RW	**Override Pull-up Strength Value (OvrPStrVal):** Override strength value for Pull-up settings. Should be 50ohm typical corner.
7:0	0x4d RW	**Override Pull-down Strength Value (OvrNStrVal):** Override strength value for Pull-down settings. Should be 50ohm typical corner.

10.6.60 RCOMP Value Register (hshvfamily_2x3_rcomp_7_0_family_rcomp_value_reg)—Offset 118Ch

RCOMP Value Register

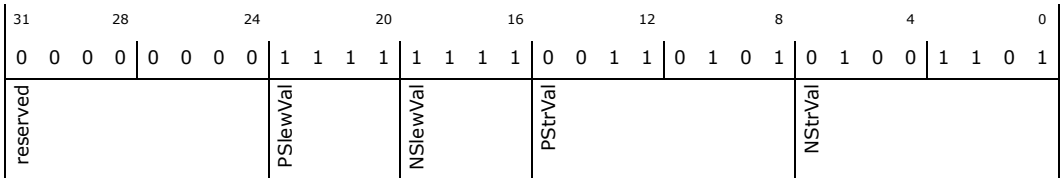
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 118Ch

Op Codes:
h - Read, h - Write

Default: 00FF354Dh



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RO	**reserved_fam1 (reserved):** reserved
23:20	0xf RO	**P Slew Value (PSlewVal):** P Slew values. Valid only after calibration is done.
19:16	0xf RO	**N Slew Value (NSlewVal):** N Slew values. Valid only after calibration is done.
15:8	0x35 RO	**Pull-up Strength Value (PStrVal):** Compensation strength for pleg. This is valid only after calibration is done.
7:0	0x4d RO	**Pull-down Strength Value (NStrVal):** Compensation strength for nleg. This is valid only after calibration is done.

10.6.61 family_config_rcomp_reg (hshvfamily_2x3_rcomp_7_0_family_config_rcomp_reg) —Offset 1190h

GPIO Family RCOMP Register

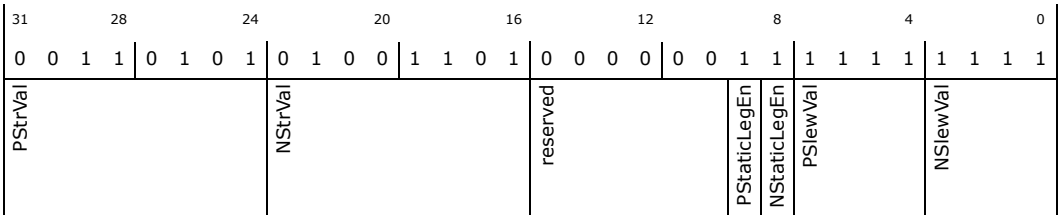
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1190h

Op Codes:
h - Read, h - Write

Default: 354D03FFh



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x35 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x4d RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable
7:4	0xf RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.

Bit Range	Default and Access	Field Name (ID): Description
3:0	0xf RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.6.62 gpio_family_configuration_register (hshvfamily_2x3_rcomp_7_0_family_config_reg)—Offset 1194h

GPIO Family CFIO Configuration Register

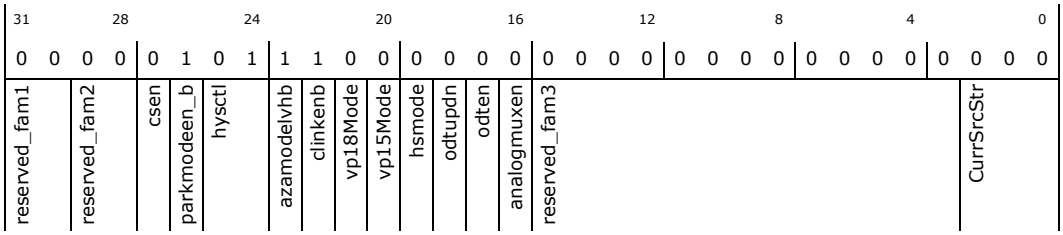
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1194h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x1 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC

Bit Range	Default and Access	Field Name (ID): Description
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.6.63 RCOMP Control Register (hshvfamily_3x3_rcomp_9_0_family_rcomp_control_reg) —Offset 1200h

RCOMP Control Register

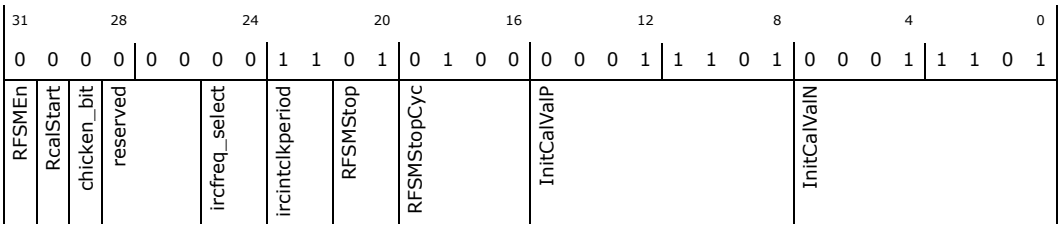
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1200h

Op Codes:
h - Read, h - Write

Default: 00D41D1Dh



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**RCOMP FSM Enable (RFSMEn):** 0 = state machine disabled (clock gated) 1 = state machine enabled It is important to have this bit enabled in order for all internal clocks inside the RCOMP FSM to run.
30	0x0 RW	**RCOMP Calibration Start (RcalStart):** When set to 1 this bit triggers the RCOMP FSM to start hunting for the correct values for strength and slew. This bit should be cleared after calibration has finished. Before setting the RcalStart bit RFSMEn must have been asserted for at least 5 clock cycles. The first calibration takes 10us to complete and subsequent calibrations take 3us. Details of this process are in the CFIP RCOMP A Specification
29	0x0 RW	**RCOMP FSM Binary Chicken Bit (chicken_bit):** Toggling this bit Simulates a V1P8 Mode change. This will allow Binary re-calibration

Bit Range	Default and Access	Field Name (ID): Description
28:26	0x0 RW	**reserved:** reserved
25:24	0x0 RW	**IRCCLK Frequency Select (ircfreq_select):** Clock ircclk frequency. This signals indicate what frequency ircclk is. This is used for 1ms and 10ms counters. 00 if clk input is 25 MHz (default, and SoC Clock) 01 if 50 MHz 10 if 100 MHz 11 if 125 MHz
23:22	0x3 RW	**IRC Internal Clock Period (ircintclkperiod):** To select rcomp clock period. This is the compensation clock frequency/period. Clock is derived from ircclk (which can be 25 MHz, 50 MHz, 100 MHz or 125 MHz user must set ircfreq_select[1:0] accordingly) 00 40 ns (64 ns for ircclk=125 MHz) 01 80 ns (96 ns for ircclk=125 MHz) 10 120 ns (128 ns for ircclk=125 MHz) (default) 11 160 ns (192 ns for ircclk=125 MHz)
21:20	0x1 RW	**RCOMP FSM Stop Condition (RFSMStop):** RCOMP FSM Stop calibration condition. RCOMP FSM (Pull-up and Pull-down) will finish calibrating once orcpupen/orcpdnen toggles. The toggling indicates the compensation value has been reached. This option is programmable for toggle once (single edge), toggle twice (double edge), toggle thrice (triple edge) or forcing it to finish after a certain cycle (defined by RFSMStopCyc). 00b = single edge detect (10 or 01) 01b = double edge detect (101 or 010) (default) 10b = triple edge detect (1010 or 0101) 11b = stop after x cycles (depending on ircstpcyc[3:0] value -- This is meant for debug)
19:16	0x4 RW	**RCOMP FSM Stop Cycles (RFSMStopCyc):** Number of cycles to stop RCOMP FSM from searching for strength and slew settings. RFSMStop must be set to 11b for this option to take affect. 0000b = 0 cycle (illegal option) 0001b = 1 cycle (illegal option) 0010b = 2 cycles (illegal option) 0011b = 3 cycles (illegal option) 0100b = 4 cycles ... 1110b = 14 cycles 1111b = 15 cycles (maximum allowed) This is meant for debug.
15:8	0x1d RW	**Initial Pull-up Value (InitCalValP):** Initial pleg calibration value. RCOMP FSM will always start with this values for Pull-up calibration.
7:0	0x1d RW	**Initial Pull-down Value (InitCalValN):** Initial nleg calibration value. RCOMP FSM will always start with this values for Pull-down calibration.

10.6.64 RCOMP Offset Register (hshvfamily_3x3_rcomp_9_0_family_rcomp_offset_reg) —Offset 1204h

RCOMP Offset Register

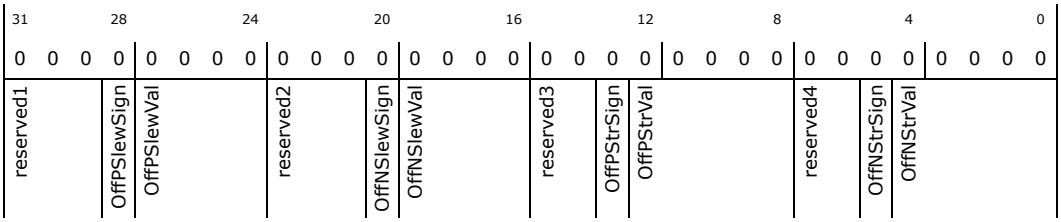
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1204h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:29	0x0 RW	**Reserved (reserved1):** Reserved
28	0x0 RW	**Pull-up Offset Slew Sign (OffPSlewSign):** Sign Bit for PSlew Offset strength value.
27:24	0x0 RW	**Pull-up Slew Offset (OffPSlewVal):** Offset slew value for pleg.
23:21	0x0 RW	**Reserved (reserved2):** Reserved
20	0x0 RW	**Pull-down Offset Slew Sign (OffNSlewSign):** Sign Bit for NSlew Offset strength value.
19:16	0x0 RW	**Pull-down Slew Offset (OffNSlewVal):** Offset slew value for nleg.
15:14	0x0 RW	**Reserved (reserved3):** Reserved
13	0x0 RW	**Pull-up Offset Strength Sign (OffPStrSign):** Sign Bit for PStrength Offset value.
12:8	0x0 RW	**Pull-up Offset Strength Value (OffPStrVal):** PStrength Offset Value.
7:6	0x0 RW	**Reserved (reserved4):** Reserved
5	0x0 RW	**Pull-down Offset Strength Sign (OffNStrSign):** Sign Bit for NStrength Offset value.
4:0	0x0 RW	**Pull-down Offset Strength Value (OffNStrVal):** NStrength Offset Value.

10.6.65 RCOMP Override Register (hshvfamily_3x3_rcomp_9_0_family_rcomp_override_reg)—Offset 1208h

RCOMP Override Register

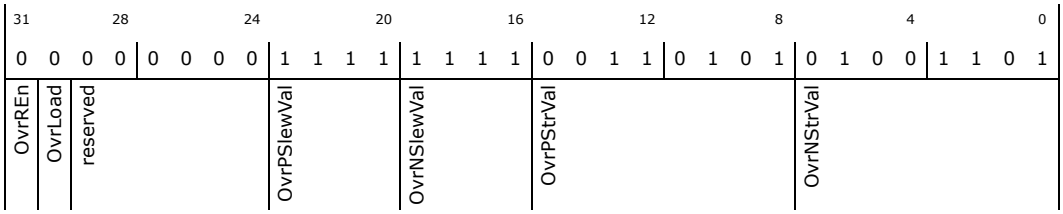
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1208h

Op Codes:
h - Read, h - Write

Default: 00FF354Dh



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**Override RCOMP Enable (OvrREn):** Override enable bit to override the strength and slew values driven by the RCOMP FSM. The override values are driven through config registers. 0 = Override Disable 1 = Override Enable
30	0x0 RW	**Override Load (OvrLoad):** Load the override values into the RCOMP FSM and drive these values to the CFIO buffer. This is only valid when OvrRen = 1. 0 = Unload Values 1 = Load Values to CFIO
29:24	0x0 RW	**reserved:** reserved
23:20	0xf RW	**Override P Slew Value (OvrPSlewVal):** Override slew values for Pull-up settings.
19:16	0xf RW	**Override N Slew Value (OvrNSlewVal):** Override slew values for Pull-down settings.
15:8	0x35 RW	**Override Pull-up Strength Value (OvrPStrVal):** Override strength value for Pull-up settings. Should be 50ohm typical corner.
7:0	0x4d RW	**Override Pull-down Strength Value (OvrNStrVal):** Override strength value for Pull-down settings. Should be 50ohm typical corner.

10.6.66 RCOMP Value Register (hshvfamily_3x3_rcomp_9_0_family_rcomp_value_reg)—Offset 120Ch

RCOMP Value Register

Access Method

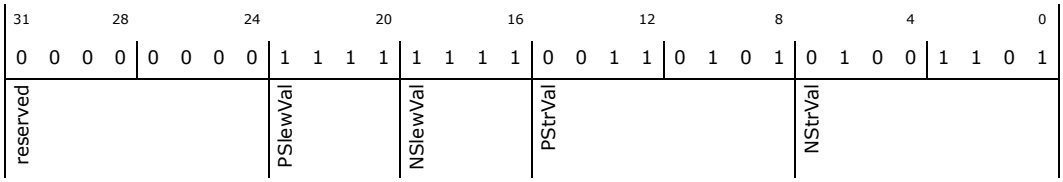
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 120Ch

Op Codes:

h - Read, h - Write

Default: 00FF354Dh



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RO	**reserved_fam1 (reserved):** reserved
23:20	0xf RO	**P Slew Value (PSlewVal):** P Slew values. Valid only after calibration is done.
19:16	0xf RO	**N Slew Value (NSlewVal):** N Slew values. Valid only after calibration is done.
15:8	0x35 RO	**Pull-up Strength Value (PStrVal):** Compensation strength for pleg. This is valid only after calibration is done.
7:0	0x4d RO	**Pull-down Strength Value (NStrVal):** Compensation strength for nleg. This is valid only after calibration is done.

10.6.67 family_config_rcomp_reg (hshvfamily_3x3_rcomp_9_0_family_config_rcomp_reg) —Offset 1210h

GPIO Family RCOMP Register

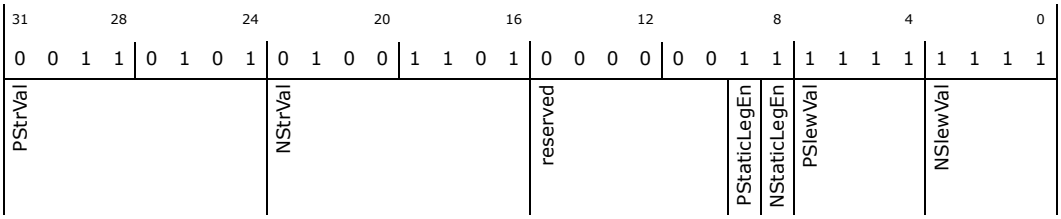
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1210h

Op Codes:
h - Read, h - Write

Default: 354D03FFh



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x35 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x4d RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable
7:4	0xf RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.

Bit Range	Default and Access	Field Name (ID): Description
3:0	0xf RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.6.68 gpio_family_configuration_register (hshvfamily_3x3_rcomp_9_0_family_config_reg)—Offset 1214h

GPIO Family CFIO Configuration Register

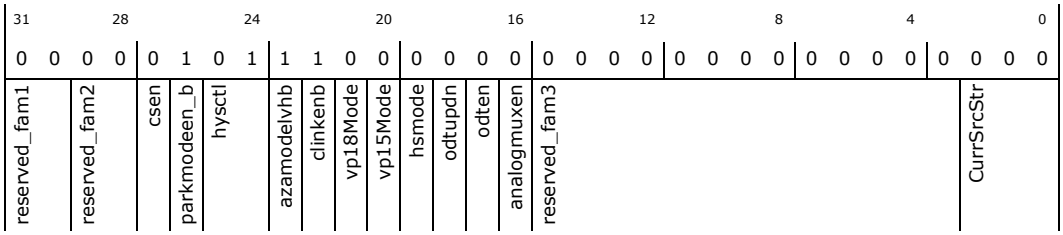
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1214h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x1 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC

Bit Range	Default and Access	Field Name (ID): Description
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.6.69 family_config_rcomp_reg (ulphsmvfamily_3x3_10_0_family_config_rcomp_reg)—Offset 1290h

GPIO Family RCOMP Register

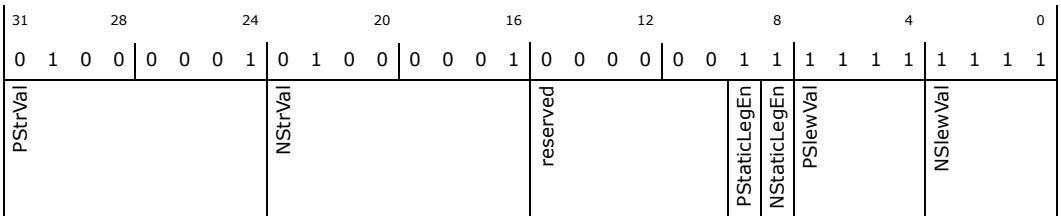
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1290h

Op Codes:
h - Read, h - Write

Default: 414103FFh



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x41 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x41 RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable

Bit Range	Default and Access	Field Name (ID): Description
7:4	0xf RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.
3:0	0xf RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.6.70 gpio_family_configuration_register (ulphsmvfamily_3x3_10_0_family_config_reg)—Offset 1294h

GPIO Family CFIO Configuration Register

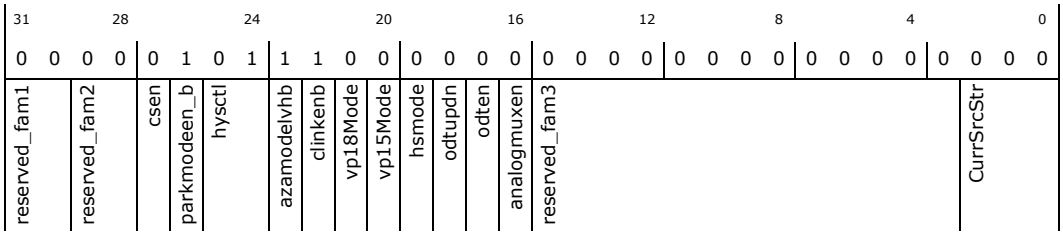
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1294h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x1 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.

Bit Range	Default and Access	Field Name (ID): Description
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.6.71 family_config_rcomp_reg (ulpmsmvfamily_3x3_11_0_family_config_rcomp_reg)—Offset 1310h

GPIO Family RCOMP Register

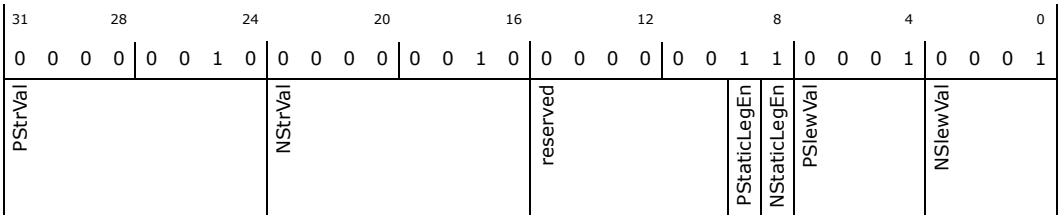
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1310h

Op Codes:
h - Read, h - Write

Default: 02020311h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x2 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x2 RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable

Bit Range	Default and Access	Field Name (ID): Description
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable
7:4	0x1 RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.
3:0	0x1 RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.6.72 gpio_family_configuration_register (ulpmsmvfamily_3x3_11_0_family_config_reg)—Offset 1314h

GPIO Family CFIO Configuration Register

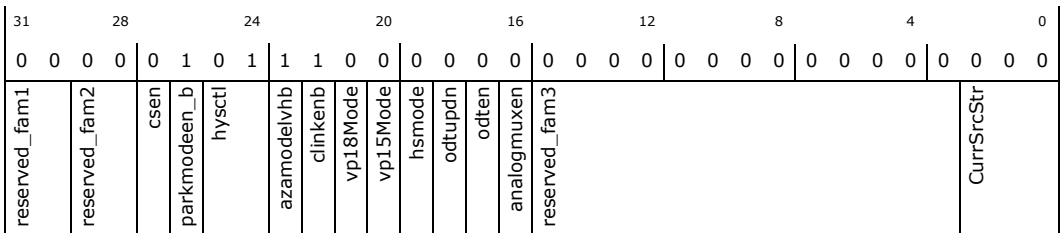
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 1314h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x1 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC

Bit Range	Default and Access	Field Name (ID): Description
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.6.73 GPIO Broadcast Data Mask bit Register (gpio_pad_bw_mask_31_0)—Offset 4000h

Write Mask that masks bit by bit the data written to BWData

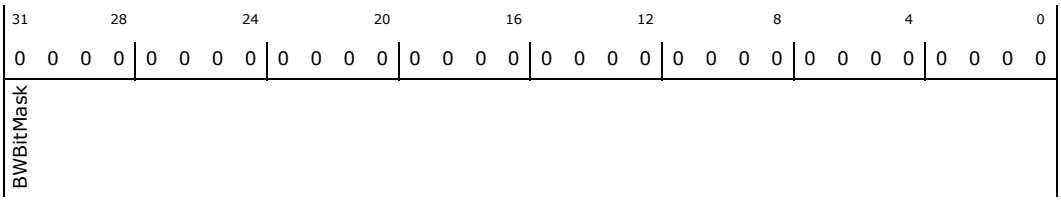
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4000h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**BWBitMask:** Reserved.

10.6.74 GPIO Broadcast Data Register (gpio_pad_bw_data_31_0)—Offset 4004h

Broadcast Write Data

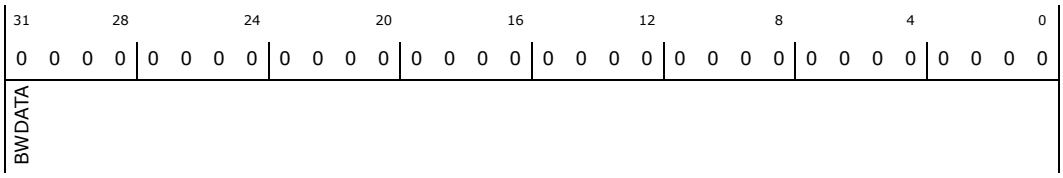
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4004h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 WO	**BWDATA:** Reserved.

10.6.75 gpio_pad_broadcast_reg_mask #0 (gpio_pad_broadcast_reg_mask_0)—Offset 4008h

Pad Broadcast Register Masking

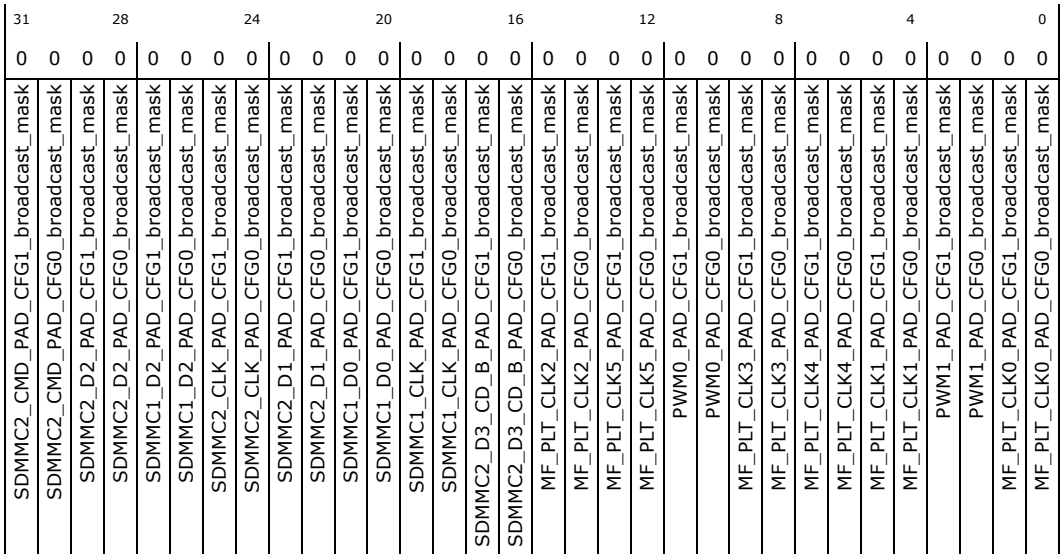
Access Method

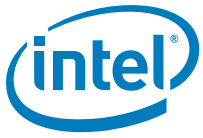
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4008h

Op Codes:
h - Read, h - Write

Default: 00000000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**SDMMC2_CMD_PAD_CFG1_broadcast_mask:** Reserved.
30	0x0 RW	**SDMMC2_CMD_PAD_CFG0_broadcast_mask:** Reserved.
29	0x0 RW	**SDMMC2_D2_PAD_CFG1_broadcast_mask:** Reserved.
28	0x0 RW	**SDMMC2_D2_PAD_CFG0_broadcast_mask:** Reserved.
27	0x0 RW	**SDMMC1_D2_PAD_CFG1_broadcast_mask:** Reserved.
26	0x0 RW	**SDMMC1_D2_PAD_CFG0_broadcast_mask:** Reserved.
25	0x0 RW	**SDMMC2_CLK_PAD_CFG1_broadcast_mask:** Reserved.
24	0x0 RW	**SDMMC2_CLK_PAD_CFG0_broadcast_mask:** Reserved.
23	0x0 RW	**SDMMC2_D1_PAD_CFG1_broadcast_mask:** Reserved.
22	0x0 RW	**SDMMC2_D1_PAD_CFG0_broadcast_mask:** Reserved.
21	0x0 RW	**SDMMC1_D0_PAD_CFG1_broadcast_mask:** Reserved.
20	0x0 RW	**SDMMC1_D0_PAD_CFG0_broadcast_mask:** Reserved.
19	0x0 RW	**SDMMC1_CLK_PAD_CFG1_broadcast_mask:** Reserved.
18	0x0 RW	**SDMMC1_CLK_PAD_CFG0_broadcast_mask:** Reserved.
17	0x0 RW	**SDMMC2_D3_CD_B_PAD_CFG1_broadcast_mask:** Reserved.
16	0x0 RW	**SDMMC2_D3_CD_B_PAD_CFG0_broadcast_mask:** Reserved.
15	0x0 RW	**MF_PLT_CLK2_PAD_CFG1_broadcast_mask:** Reserved.
14	0x0 RW	**MF_PLT_CLK2_PAD_CFG0_broadcast_mask:** Reserved.
13	0x0 RW	**MF_PLT_CLK5_PAD_CFG1_broadcast_mask:** Reserved.
12	0x0 RW	**MF_PLT_CLK5_PAD_CFG0_broadcast_mask:** Reserved.
11	0x0 RW	**PWM0_PAD_CFG1_broadcast_mask:** Reserved.
10	0x0 RW	**PWM0_PAD_CFG0_broadcast_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
9	0x0 RW	**MF_PLT_CLK3_PAD_CFG1_broadcast_mask:** Reserved.
8	0x0 RW	**MF_PLT_CLK3_PAD_CFG0_broadcast_mask:** Reserved.
7	0x0 RW	**MF_PLT_CLK4_PAD_CFG1_broadcast_mask:** Reserved.
6	0x0 RW	**MF_PLT_CLK4_PAD_CFG0_broadcast_mask:** Reserved.
5	0x0 RW	**MF_PLT_CLK1_PAD_CFG1_broadcast_mask:** Reserved.
4	0x0 RW	**MF_PLT_CLK1_PAD_CFG0_broadcast_mask:** Reserved.
3	0x0 RW	**PWM1_PAD_CFG1_broadcast_mask:** Reserved.
2	0x0 RW	**PWM1_PAD_CFG0_broadcast_mask:** Reserved.
1	0x0 RW	**MF_PLT_CLK0_PAD_CFG1_broadcast_mask:** Reserved.
0	0x0 RW	**MF_PLT_CLK0_PAD_CFG0_broadcast_mask:** Reserved.

10.6.76 gpio_pad_broadcast_reg_mask #1 (gpio_pad_broadcast_reg_mask_1)—Offset 400Ch

Pad Broadcast Register Masking

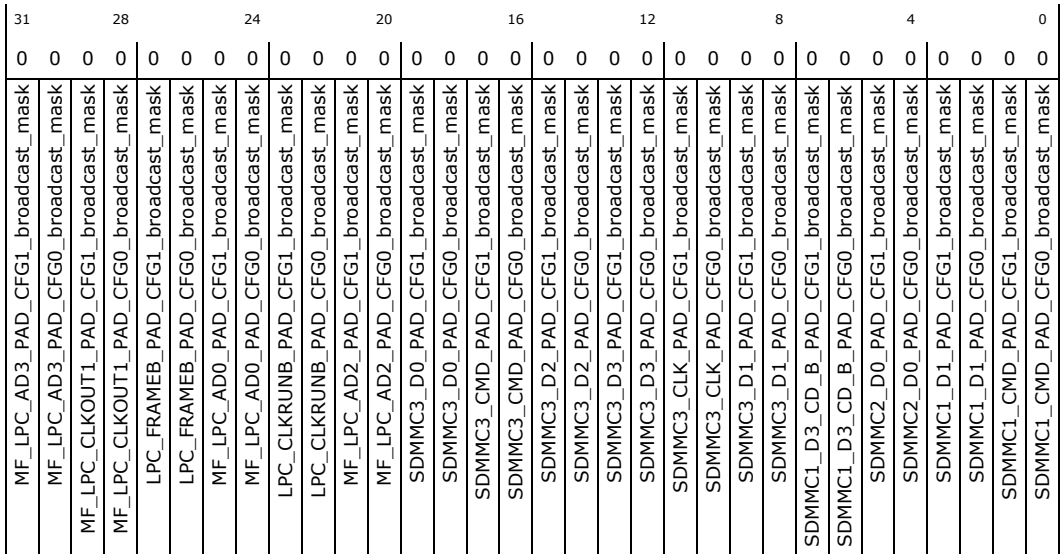
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 400Ch

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**MF_LPC_AD3_PAD_CFG1_broadcast_mask:** Reserved.
30	0x0 RW	**MF_LPC_AD3_PAD_CFG0_broadcast_mask:** Reserved.
29	0x0 RW	**MF_LPC_CLKOUT1_PAD_CFG1_broadcast_mask:** Reserved.
28	0x0 RW	**MF_LPC_CLKOUT1_PAD_CFG0_broadcast_mask:** Reserved.
27	0x0 RW	**LPC_FRAMEB_PAD_CFG1_broadcast_mask:** Reserved.
26	0x0 RW	**LPC_FRAMEB_PAD_CFG0_broadcast_mask:** Reserved.
25	0x0 RW	**MF_LPC_AD0_PAD_CFG1_broadcast_mask:** Reserved.
24	0x0 RW	**MF_LPC_AD0_PAD_CFG0_broadcast_mask:** Reserved.
23	0x0 RW	**LPC_CLKRUNB_PAD_CFG1_broadcast_mask:** Reserved.
22	0x0 RW	**LPC_CLKRUNB_PAD_CFG0_broadcast_mask:** Reserved.
21	0x0 RW	**MF_LPC_AD2_PAD_CFG1_broadcast_mask:** Reserved.
20	0x0 RW	**MF_LPC_AD2_PAD_CFG0_broadcast_mask:** Reserved.
19	0x0 RW	**SDMMC3_D0_PAD_CFG1_broadcast_mask:** Reserved.
18	0x0 RW	**SDMMC3_D0_PAD_CFG0_broadcast_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
17	0x0 RW	**SDMMC3_CMD_PAD_CFG1_broadcast_mask:** Reserved.
16	0x0 RW	**SDMMC3_CMD_PAD_CFG0_broadcast_mask:** Reserved.
15	0x0 RW	**SDMMC3_D2_PAD_CFG1_broadcast_mask:** Reserved.
14	0x0 RW	**SDMMC3_D2_PAD_CFG0_broadcast_mask:** Reserved.
13	0x0 RW	**SDMMC3_D3_PAD_CFG1_broadcast_mask:** Reserved.
12	0x0 RW	**SDMMC3_D3_PAD_CFG0_broadcast_mask:** Reserved.
11	0x0 RW	**SDMMC3_CLK_PAD_CFG1_broadcast_mask:** Reserved.
10	0x0 RW	**SDMMC3_CLK_PAD_CFG0_broadcast_mask:** Reserved.
9	0x0 RW	**SDMMC3_D1_PAD_CFG1_broadcast_mask:** Reserved.
8	0x0 RW	**SDMMC3_D1_PAD_CFG0_broadcast_mask:** Reserved.
7	0x0 RW	**SDMMC1_D3_CD_B_PAD_CFG1_broadcast_mask:** Reserved.
6	0x0 RW	**SDMMC1_D3_CD_B_PAD_CFG0_broadcast_mask:** Reserved.
5	0x0 RW	**SDMMC2_D0_PAD_CFG1_broadcast_mask:** Reserved.
4	0x0 RW	**SDMMC2_D0_PAD_CFG0_broadcast_mask:** Reserved.
3	0x0 RW	**SDMMC1_D1_PAD_CFG1_broadcast_mask:** Reserved.
2	0x0 RW	**SDMMC1_D1_PAD_CFG0_broadcast_mask:** Reserved.
1	0x0 RW	**SDMMC1_CMD_PAD_CFG1_broadcast_mask:** Reserved.
0	0x0 RW	**SDMMC1_CMD_PAD_CFG0_broadcast_mask:** Reserved.

10.6.77 gpio_pad_broadcast_reg_mask #2 (gpio_pad_broadcast_reg_mask_2)—Offset 4010h

Pad Broadcast Register Masking

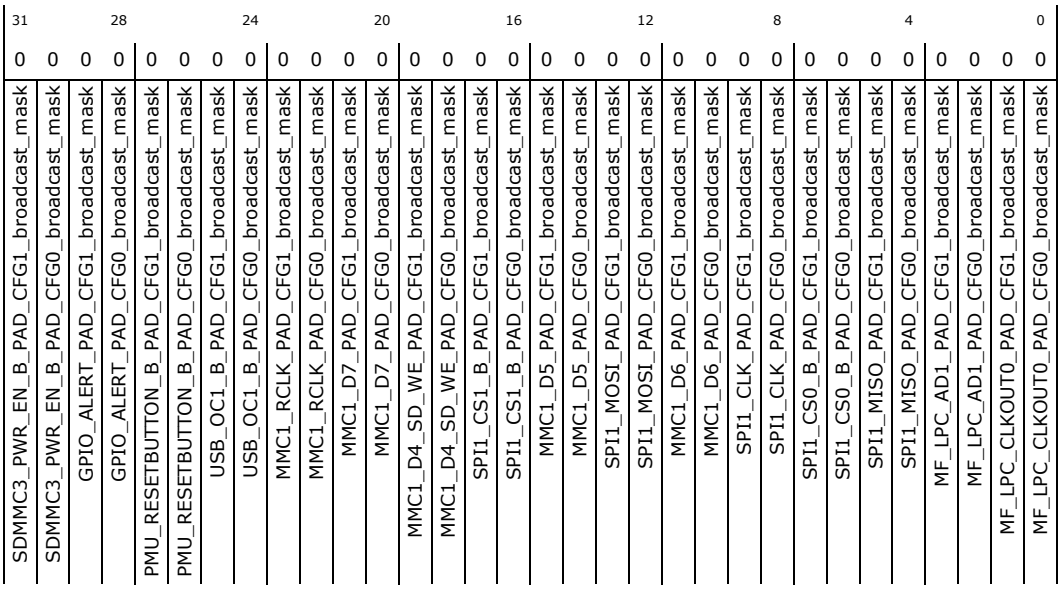
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4010h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**SDMMC3_PWR_EN_B_PAD_CFG1_broadcast_mask:** Reserved.
30	0x0 RW	**SDMMC3_PWR_EN_B_PAD_CFG0_broadcast_mask:** Reserved.
29	0x0 RW	**GPIO_ALERT_PAD_CFG1_broadcast_mask:** Reserved.
28	0x0 RW	**GPIO_ALERT_PAD_CFG0_broadcast_mask:** Reserved.
27	0x0 RW	**PMU_RESETBUTTON_B_PAD_CFG1_broadcast_mask:** Reserved.
26	0x0 RW	**PMU_RESETBUTTON_B_PAD_CFG0_broadcast_mask:** Reserved.
25	0x0 RW	**USB_OC1_B_PAD_CFG1_broadcast_mask:** Reserved.
24	0x0 RW	**USB_OC1_B_PAD_CFG0_broadcast_mask:** Reserved.
23	0x0 RW	**MMC1_RCLK_PAD_CFG1_broadcast_mask:** Reserved.
22	0x0 RW	**MMC1_RCLK_PAD_CFG0_broadcast_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
21	0x0 RW	**MMC1_D7_PAD_CFG1_broadcast_mask:** Reserved.
20	0x0 RW	**MMC1_D7_PAD_CFG0_broadcast_mask:** Reserved.
19	0x0 RW	**MMC1_D4_SD_WE_PAD_CFG1_broadcast_mask:** Reserved.
18	0x0 RW	**MMC1_D4_SD_WE_PAD_CFG0_broadcast_mask:** Reserved.
17	0x0 RW	**SPI1_CS1_B_PAD_CFG1_broadcast_mask:** Reserved.
16	0x0 RW	**SPI1_CS1_B_PAD_CFG0_broadcast_mask:** Reserved.
15	0x0 RW	**MMC1_D5_PAD_CFG1_broadcast_mask:** Reserved.
14	0x0 RW	**MMC1_D5_PAD_CFG0_broadcast_mask:** Reserved.
13	0x0 RW	**SPI1_MOSI_PAD_CFG1_broadcast_mask:** Reserved.
12	0x0 RW	**SPI1_MOSI_PAD_CFG0_broadcast_mask:** Reserved.
11	0x0 RW	**MMC1_D6_PAD_CFG1_broadcast_mask:** Reserved.
10	0x0 RW	**MMC1_D6_PAD_CFG0_broadcast_mask:** Reserved.
9	0x0 RW	**SPI1_CLK_PAD_CFG1_broadcast_mask:** Reserved.
8	0x0 RW	**SPI1_CLK_PAD_CFG0_broadcast_mask:** Reserved.
7	0x0 RW	**SPI1_CS0_B_PAD_CFG1_broadcast_mask:** Reserved.
6	0x0 RW	**SPI1_CS0_B_PAD_CFG0_broadcast_mask:** Reserved.
5	0x0 RW	**SPI1_MISO_PAD_CFG1_broadcast_mask:** Reserved.
4	0x0 RW	**SPI1_MISO_PAD_CFG0_broadcast_mask:** Reserved.
3	0x0 RW	**MF_LPC_AD1_PAD_CFG1_broadcast_mask:** Reserved.
2	0x0 RW	**MF_LPC_AD1_PAD_CFG0_broadcast_mask:** Reserved.
1	0x0 RW	**MF_LPC_CLKOUT0_PAD_CFG1_broadcast_mask:** Reserved.
0	0x0 RW	**MF_LPC_CLKOUT0_PAD_CFG0_broadcast_mask:** Reserved.

10.6.78 gpio_pad_broadcast_reg_mask #3 (gpio_pad_broadcast_reg_mask_3)—Offset 4014h

Pad Broadcast Register Masking

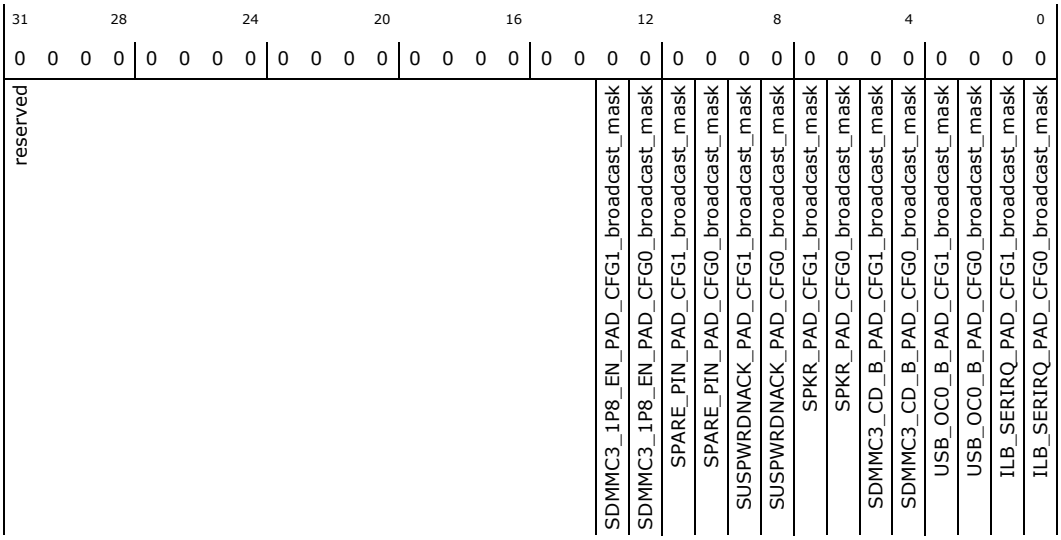
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4014h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:14	0x0 RW	**reserved:** Reserved.
13	0x0 RW	**SDMMC3_1P8_EN_PAD_CFG1_broadcast_mask:** Reserved.
12	0x0 RW	**SDMMC3_1P8_EN_PAD_CFG0_broadcast_mask:** Reserved.
11	0x0 RW	**SPARE_PIN_PAD_CFG1_broadcast_mask:** Reserved.
10	0x0 RW	**SPARE_PIN_PAD_CFG0_broadcast_mask:** Reserved.
9	0x0 RW	**SUSPWRDNACK_PAD_CFG1_broadcast_mask:** Reserved.
8	0x0 RW	**SUSPWRDNACK_PAD_CFG0_broadcast_mask:** Reserved.
7	0x0 RW	**SPKR_PAD_CFG1_broadcast_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
6	0x0 RW	**SPKR_PAD_CFG0_broadcast_mask:** Reserved.
5	0x0 RW	**SDMMC3_CD_B_PAD_CFG1_broadcast_mask:** Reserved.
4	0x0 RW	**SDMMC3_CD_B_PAD_CFG0_broadcast_mask:** Reserved.
3	0x0 RW	**USB_OC0_B_PAD_CFG1_broadcast_mask:** Reserved.
2	0x0 RW	**USB_OC0_B_PAD_CFG0_broadcast_mask:** Reserved.
1	0x0 RW	**ILB_SERIRQ_PAD_CFG1_broadcast_mask:** Reserved.
0	0x0 RW	**ILB_SERIRQ_PAD_CFG0_broadcast_mask:** Reserved.

10.6.79 Pad Control Register 0 (MF_PLT_CLK0_PAD_CFG0)—Offset 4400h

Pad Control Register 0

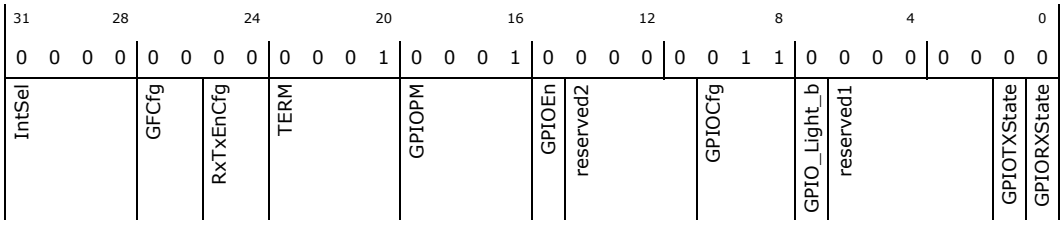
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4400h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15

Bit Range	Default and Access	Field Name (ID): Description
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.80 Pad Control Register 1 (MF_PLT_CLK0_PAD_CFG1)—Offset 4404h

Pad Control Register 1

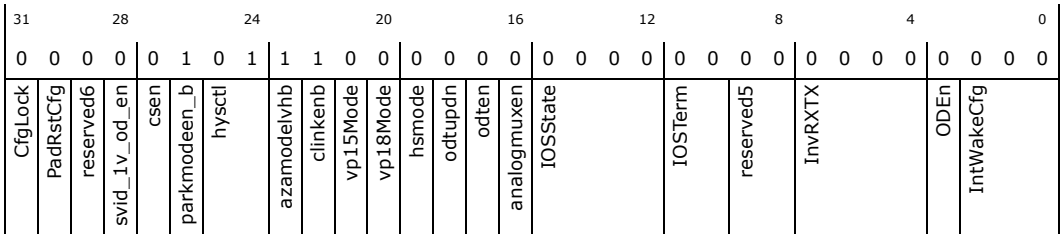
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4404h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP

Bit Range	Default and Access	Field Name (ID): Description
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.81 Pad Control Register 0 (PWM1_PAD_CFG0)—Offset 4408h

Pad Control Register 0

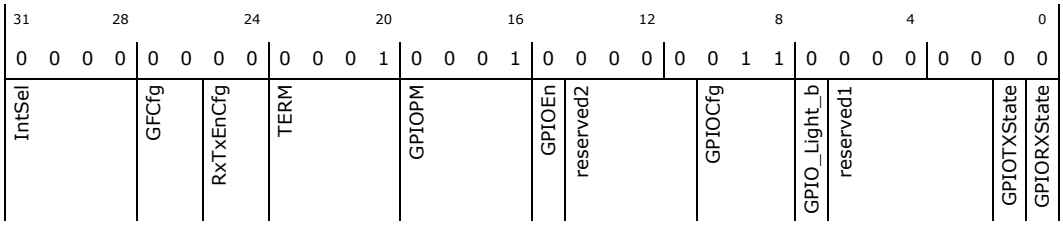
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4408h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.

Bit Range	Default and Access	Field Name (ID): Description
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.82 Pad Control Register 1 (PWM1_PAD_CFG1)—Offset 440Ch

Pad Control Register 1

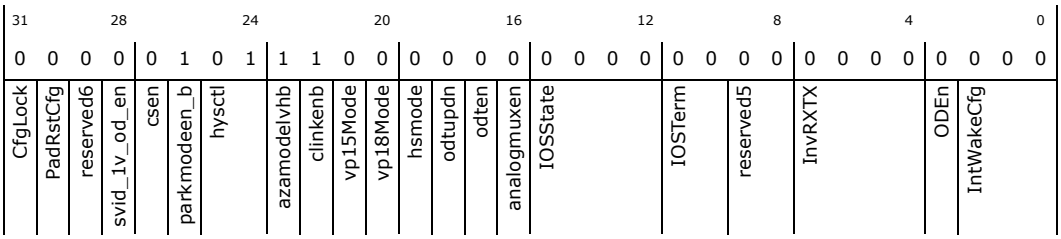
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 440Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC

Bit Range	Default and Access	Field Name (ID): Description
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.83 Pad Control Register 0 (MF_PLT_CLK1_PAD_CFG0)—Offset 4410h

Pad Control Register 0

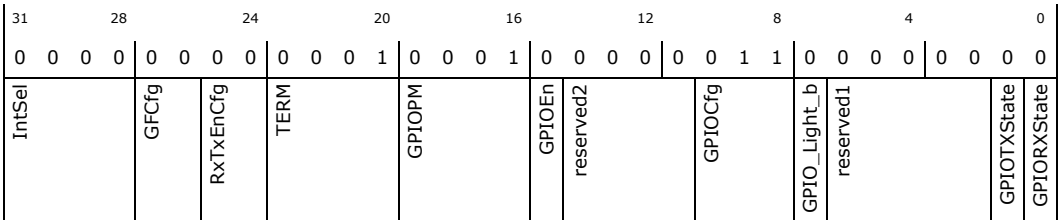
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4410h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.84 Pad Control Register 1 (MF_PLT_CLK1_PAD_CFG1)—Offset 4414h

Pad Control Register 1

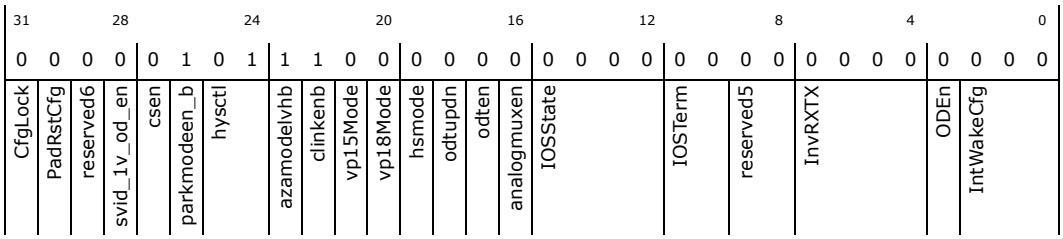
Access Method

Type: Message Bus Register (Size: 32 bits)

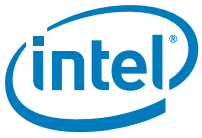
Offset: [Port: 0x48] + 4414h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6



Bit Range	Default and Access	Field Name (ID): Description
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.85 Pad Control Register 0 (MF_PLT_CLK4_PAD_CFG0)—Offset 4418h

Pad Control Register 0

Access Method

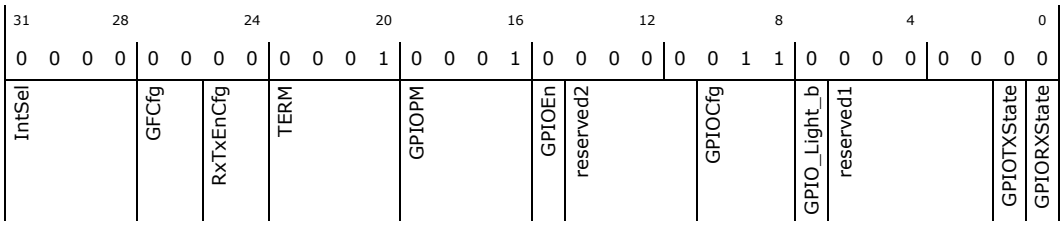
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4418h

Op Codes:

h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.86 Pad Control Register 1 (MF_PLT_CLK4_PAD_CFG1)—Offset 441Ch

Pad Control Register 1

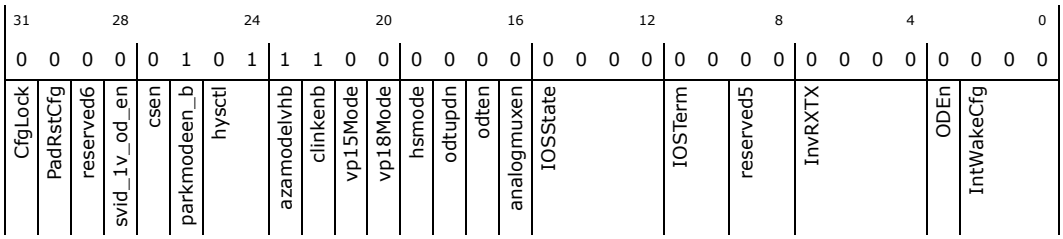
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 441Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.87 Pad Control Register 0 (MF_PLT_CLK3_PAD_CFG0)—Offset 4420h

Pad Control Register 0

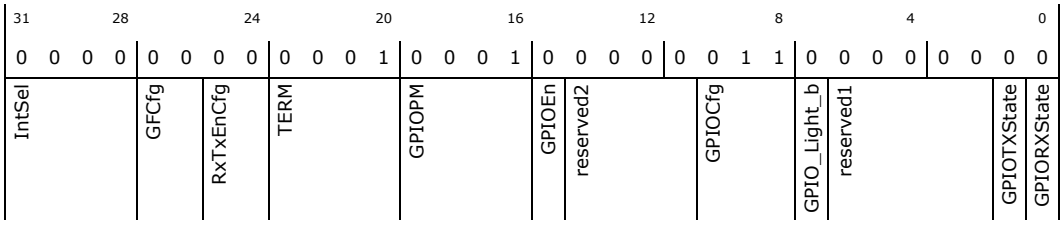
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4420h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.88 Pad Control Register 1 (MF_PLT_CLK3_PAD_CFG1)—Offset 4424h

Pad Control Register 1

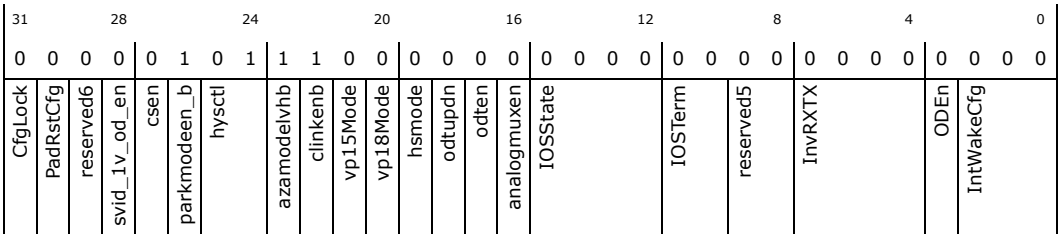
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4424h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.89 Pad Control Register 0 (PWM0_PAD_CFG0)—Offset 4428h

Pad Control Register 0

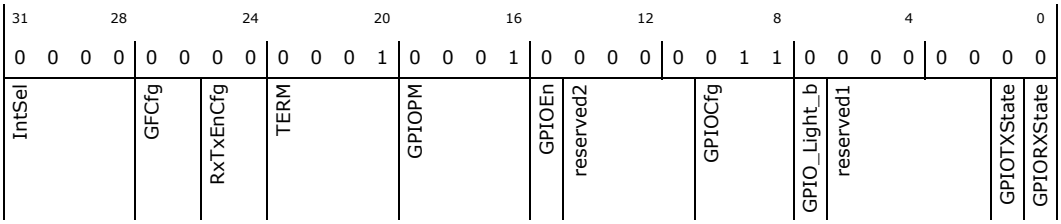
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4428h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.90 Pad Control Register 1 (PWM0_PAD_CFG1)—Offset 442Ch

Pad Control Register 1

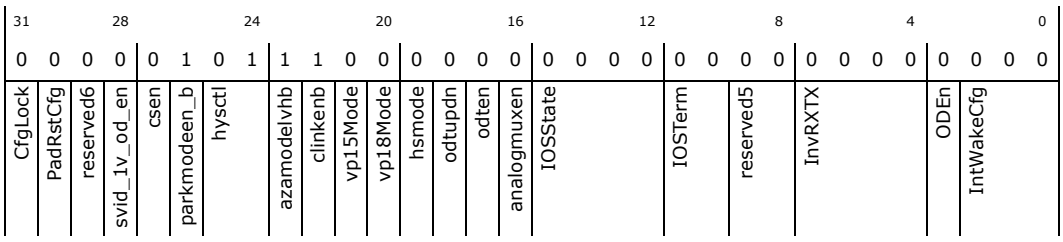
Access Method

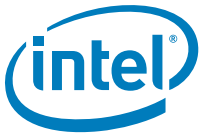
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 442Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.91 Pad Control Register 0 (MF_PLT_CLK5_PAD_CFG0)—Offset 4430h

Pad Control Register 0

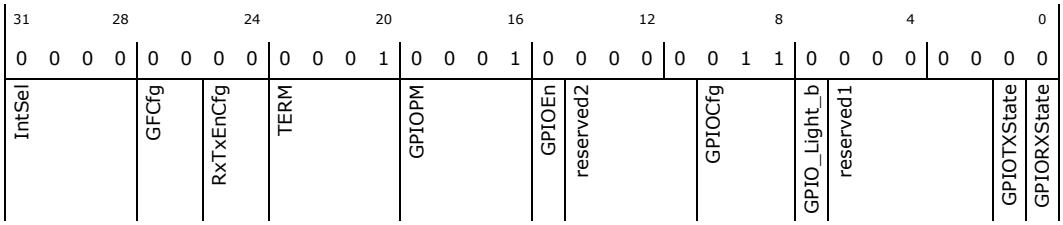
Access Method

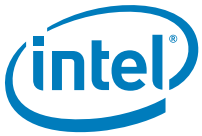
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4430h

Op Codes:
h - Read, h - Write

Default: 00110300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.92 Pad Control Register 1 (MF_PLT_CLK5_PAD_CFG1)—Offset 4434h

Pad Control Register 1

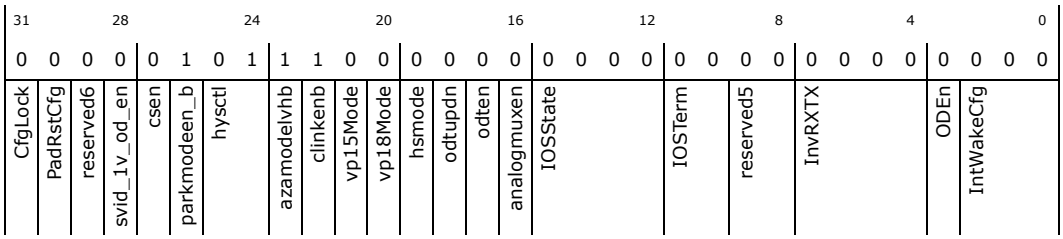
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4434h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.93 Pad Control Register 0 (MF_PLT_CLK2_PAD_CFG0)—Offset 4438h

Pad Control Register 0

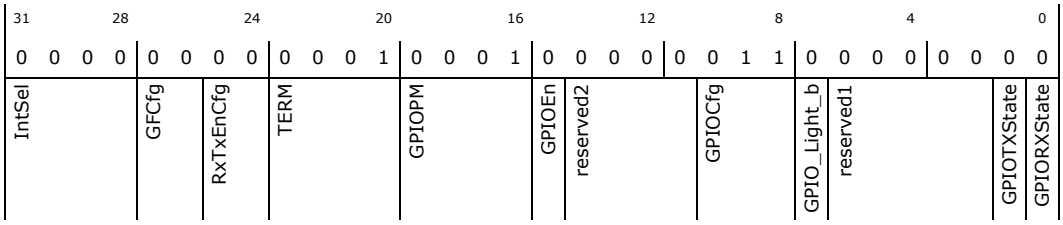
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4438h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.94 Pad Control Register 1 (MF_PLT_CLK2_PAD_CFG1)—Offset 443Ch

Pad Control Register 1

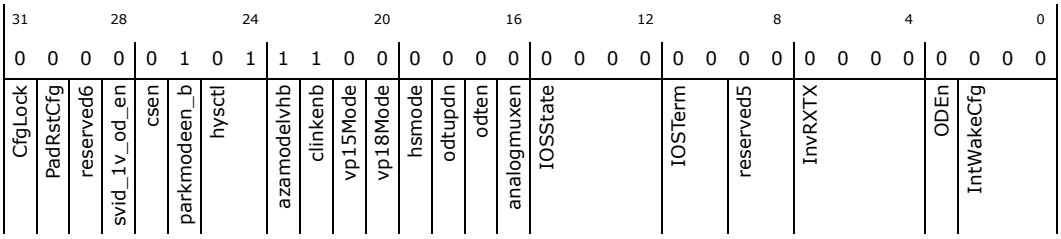
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 443Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.95 Pad Control Register 0 (SDMMC2_D3_CD_B_PAD_CFG0)—Offset 4800h

Pad Control Register 0

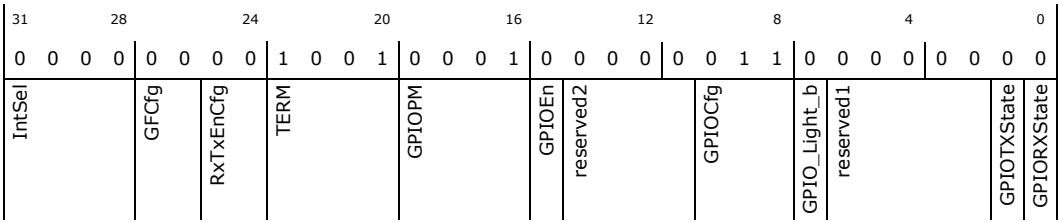
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4800h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.96 Pad Control Register 1 (SDMMC2_D3_CD_B_PAD_CFG1)—Offset 4804h

Pad Control Register 1

Access Method

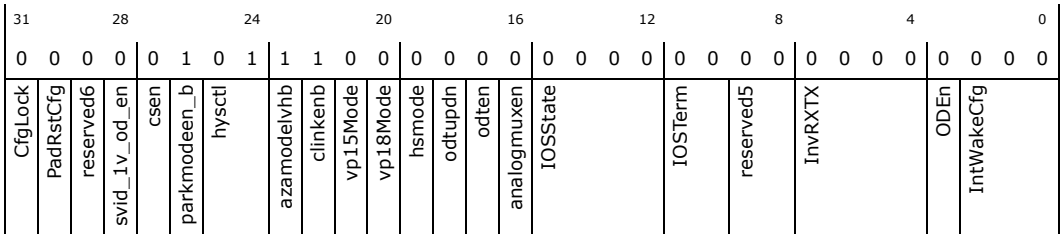
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4804h

Op Codes:

h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.97 Pad Control Register 0 (SDMMC1_CLK_PAD_CFG0)—Offset 4808h

Pad Control Register 0

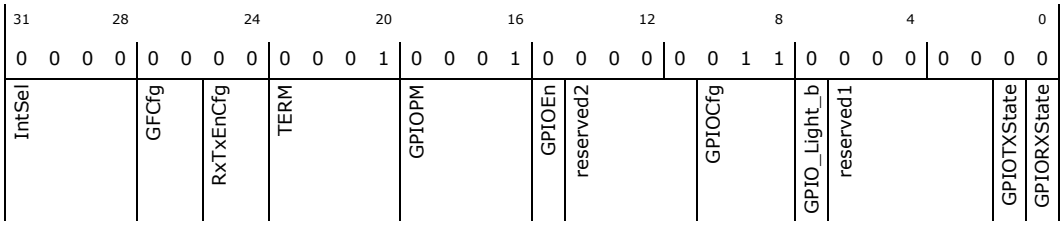
Access Method

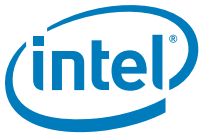
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4808h

Op Codes:
h - Read, h - Write

Default: 00110300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.98 Pad Control Register 1 (SDMMC1_CLK_PAD_CFG1)—Offset 480Ch

Pad Control Register 1

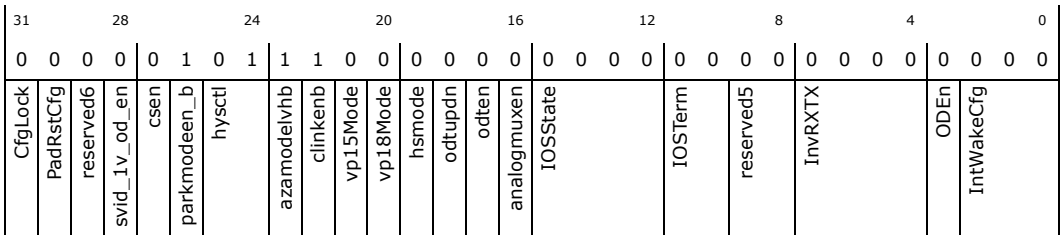
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 480Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.99 Pad Control Register 0 (SDMMC1_D0_PAD_CFG0)—Offset 4810h

Pad Control Register 0

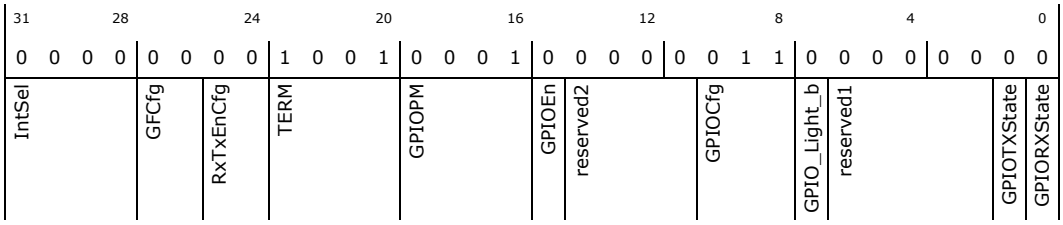
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4810h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.100 Pad Control Register 1 (SDMMC1_D0_PAD_CFG1)—Offset 4814h

Pad Control Register 1

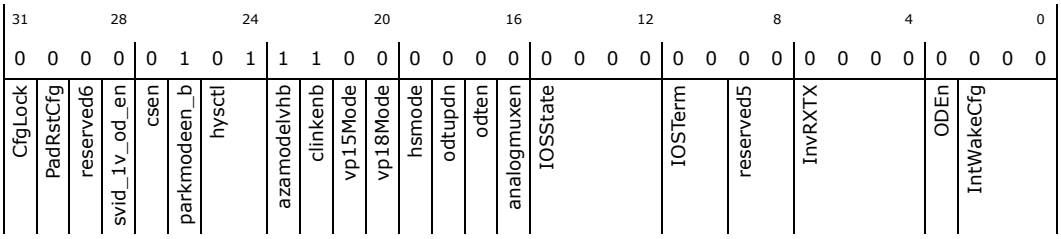
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4814h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.101 Pad Control Register 0 (SDMMC2_D1_PAD_CFG0)—Offset 4818h

Pad Control Register 0

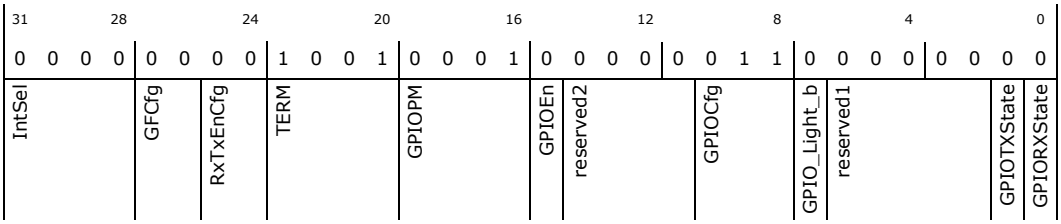
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4818h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.102 Pad Control Register 1 (SDMMC2_D1_PAD_CFG1)—Offset 481Ch

Pad Control Register 1

Access Method

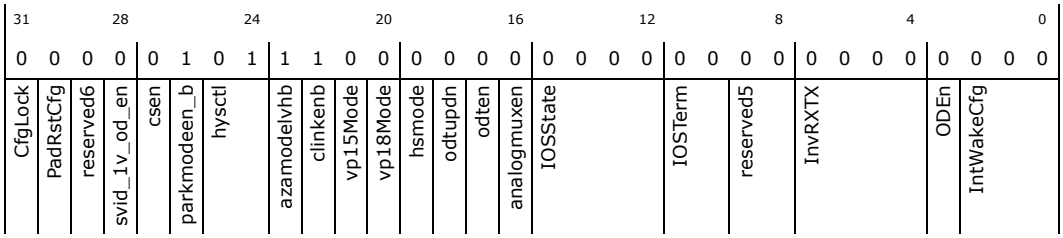
Type: Message Bus Register (Size: 32 bits)

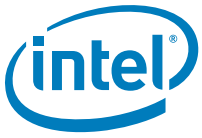
Offset: [Port: 0x48] + 481Ch

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.103 Pad Control Register 0 (SDMMC2_CLK_PAD_CFG0)—Offset 4820h

Pad Control Register 0

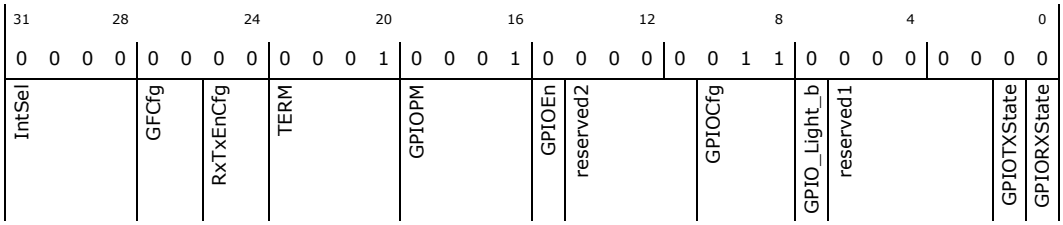
Access Method

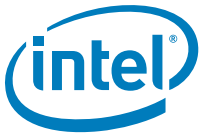
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4820h

Op Codes:
h - Read, h - Write

Default: 00110300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.104 Pad Control Register 1 (SDMMC2_CLK_PAD_CFG1)—Offset 4824h

Pad Control Register 1

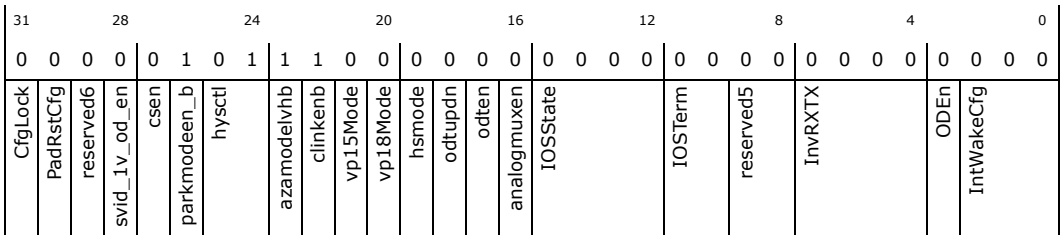
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4824h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.105 Pad Control Register 0 (SDMMC1_D2_PAD_CFG0)—Offset 4828h

Pad Control Register 0

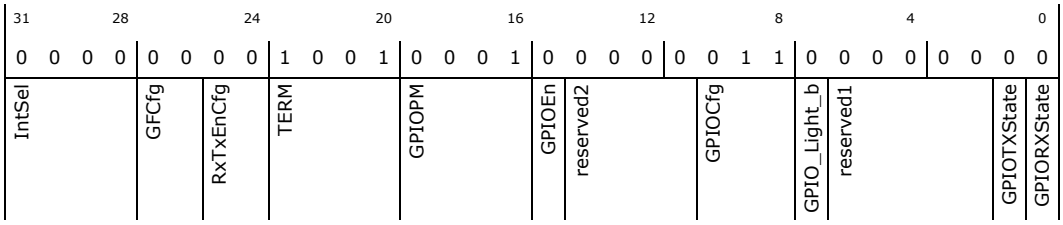
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4828h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.106 Pad Control Register 1 (SDMMC1_D2_PAD_CFG1)—Offset 482Ch

Pad Control Register 1

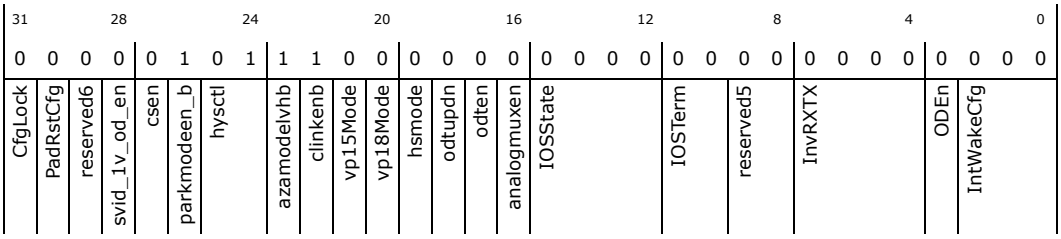
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 482Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.107 Pad Control Register 0 (SDMMC2_D2_PAD_CFG0)—Offset 4830h

Pad Control Register 0

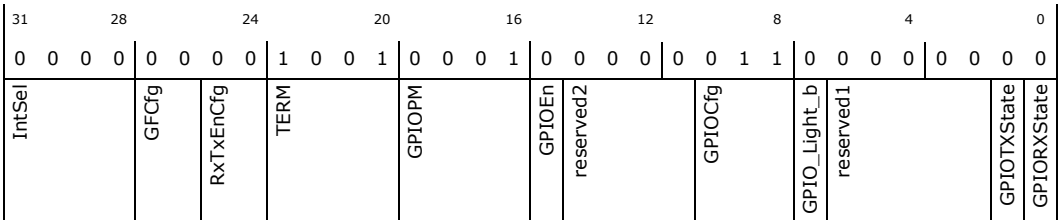
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4830h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.108 Pad Control Register 1 (SDMMC2_D2_PAD_CFG1)—Offset 4834h

Pad Control Register 1

Access Method

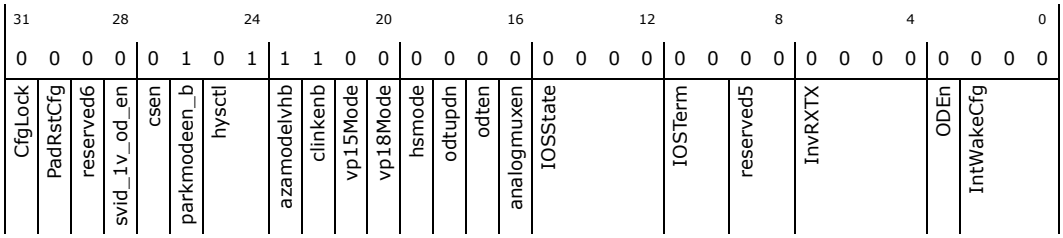
Type: Message Bus Register (Size: 32 bits)

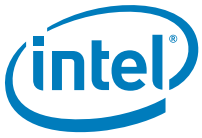
Offset: [Port: 0x48] + 4834h

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.109 Pad Control Register 0 (SDMMC2_CMD_PAD_CFG0)—Offset 4838h

Pad Control Register 0

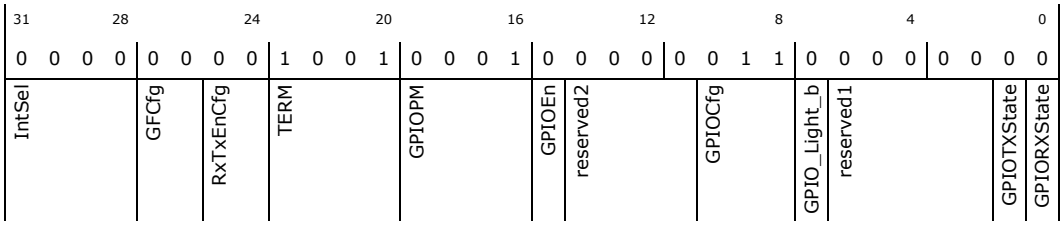
Access Method

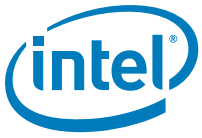
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4838h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.110 Pad Control Register 1 (SDMMC2_CMD_PAD_CFG1)—Offset 483Ch

Pad Control Register 1

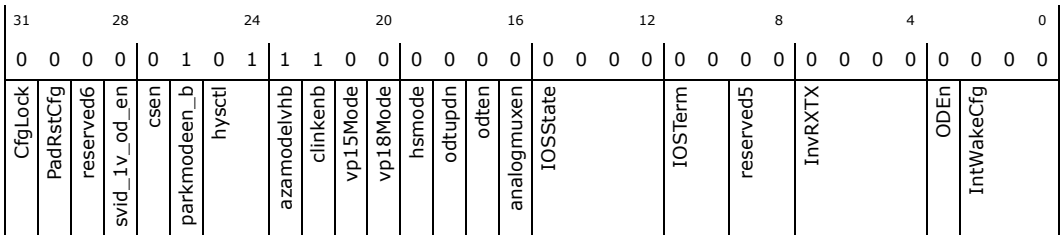
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 483Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.111 Pad Control Register 0 (SDMMC1_CMD_PAD_CFG0)—Offset 4840h

Pad Control Register 0

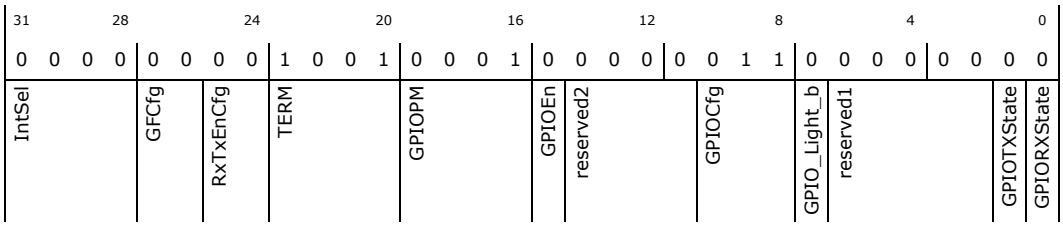
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4840h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.

Bit Range	Default and Access	Field Name (ID): Description
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.112 Pad Control Register 1 (SDMMC1_CMD_PAD_CFG1)—Offset 4844h

Pad Control Register 1

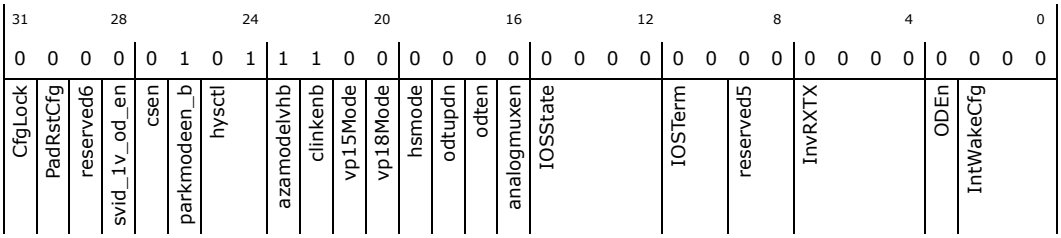
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4844h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC

Bit Range	Default and Access	Field Name (ID): Description
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.113 Pad Control Register 0 (SDMMC1_D1_PAD_CFG0)—Offset 4848h

Pad Control Register 0

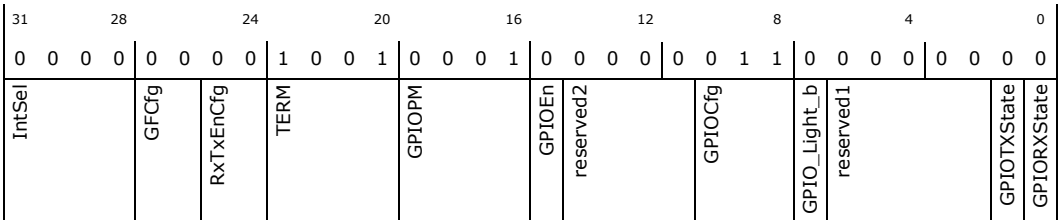
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4848h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.114 Pad Control Register 1 (SDMMC1_D1_PAD_CFG1)—Offset 484Ch

Pad Control Register 1

Access Method

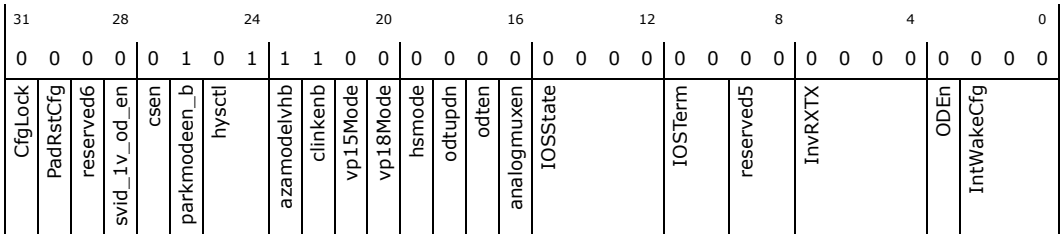
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 484Ch

Op Codes:

h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.115 Pad Control Register 0 (SDMMC2_D0_PAD_CFG0)—Offset 4850h

Pad Control Register 0

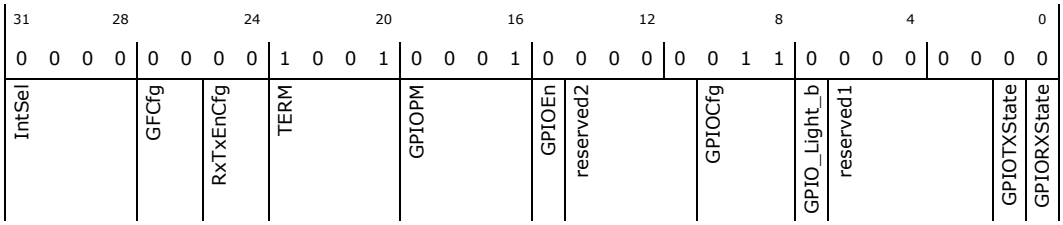
Access Method

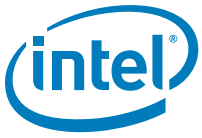
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4850h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.116 Pad Control Register 1 (SDMMC2_D0_PAD_CFG1)—Offset 4854h

Pad Control Register 1

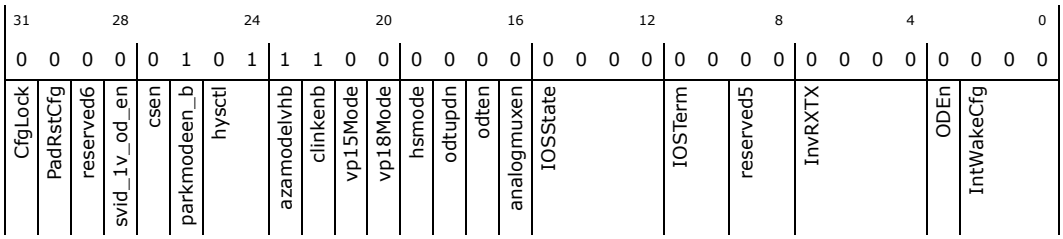
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4854h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.117 Pad Control Register 0 (SDMMC1_D3_CD_B_PAD_CFG0)—Offset 4858h

Pad Control Register 0

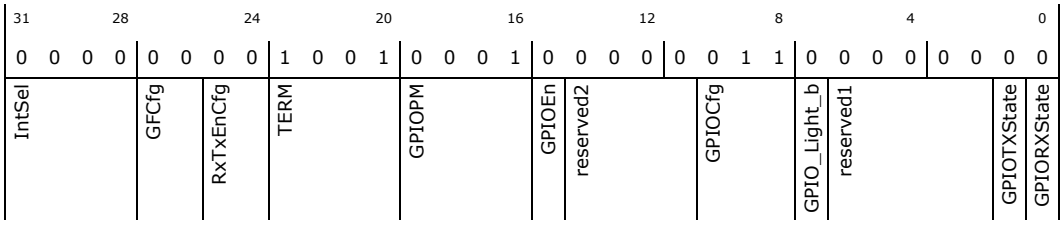
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4858h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.118 Pad Control Register 1 (SDMMC1_D3_CD_B_PAD_CFG1)—Offset 485Ch

Pad Control Register 1

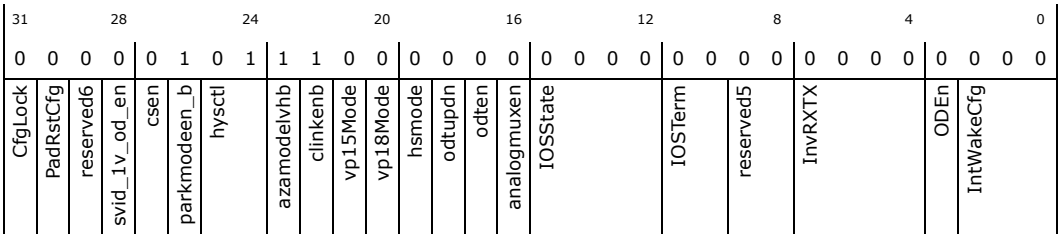
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 485Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.119 Pad Control Register 0 (SDMMC3_D1_PAD_CFG0)—Offset 4C00h

Pad Control Register 0

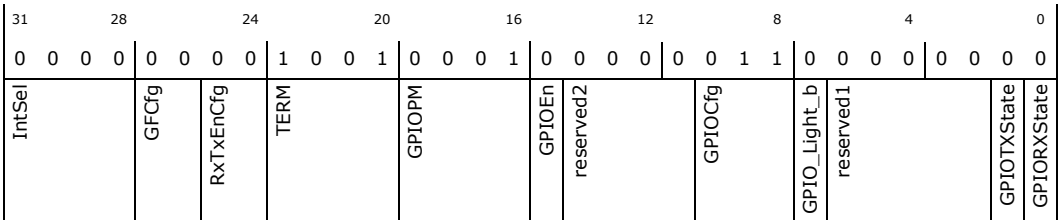
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4C00h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.120 Pad Control Register 1 (SDMMC3_D1_PAD_CFG1)—Offset 4C04h

Pad Control Register 1

Access Method

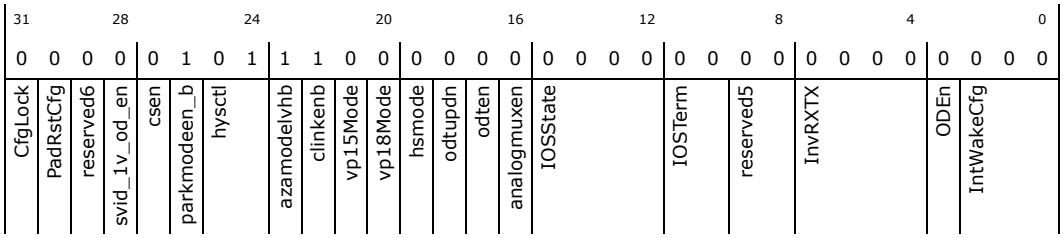
Type: Message Bus Register (Size: 32 bits)

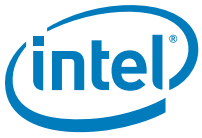
Offset: [Port: 0x48] + 4C04h

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.121 Pad Control Register 0 (SDMMC3_CLK_PAD_CFG0)—Offset 4C08h

Pad Control Register 0

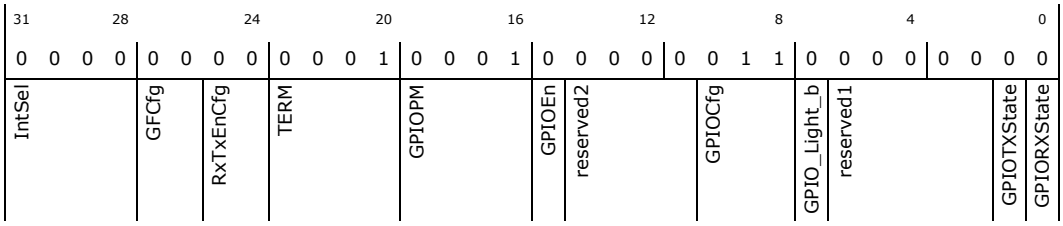
Access Method

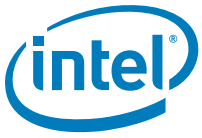
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4C08h

Op Codes:
h - Read, h - Write

Default: 00110300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.122 Pad Control Register 1 (SDMMC3_CLK_PAD_CFG1)—Offset 4C0Ch

Pad Control Register 1

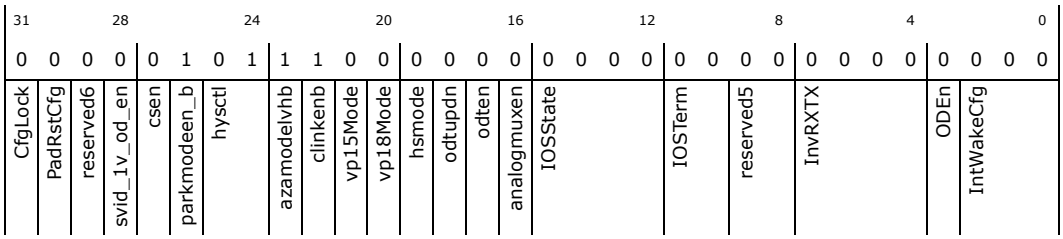
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4C0Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.123 Pad Control Register 0 (SDMMC3_D3_PAD_CFG0)—Offset 4C10h

Pad Control Register 0

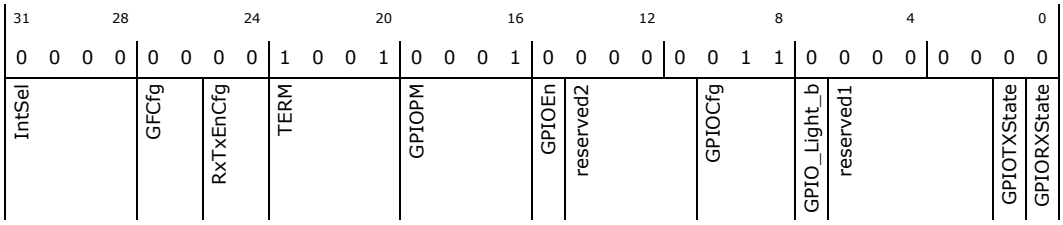
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4C10h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.124 Pad Control Register 1 (SDMMC3_D3_PAD_CFG1)—Offset 4C14h

Pad Control Register 1

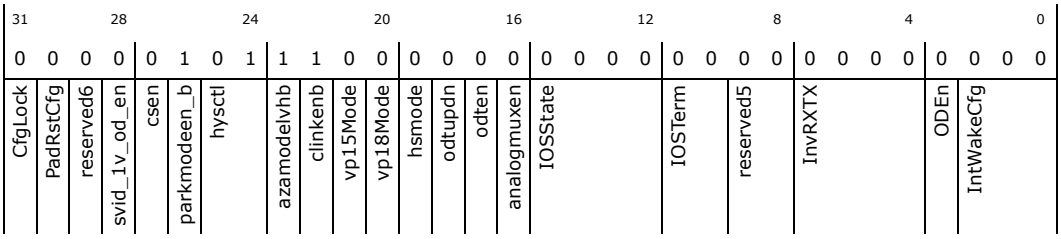
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4C14h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.125 Pad Control Register 0 (SDMMC3_D2_PAD_CFG0)—Offset 4C18h

Pad Control Register 0

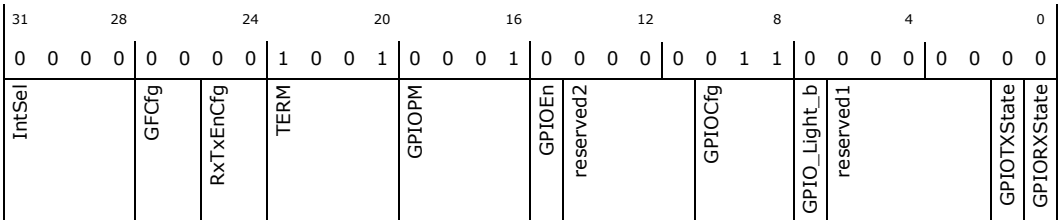
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4C18h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.126 Pad Control Register 1 (SDMMC3_D2_PAD_CFG1)—Offset 4C1Ch

Pad Control Register 1

Access Method

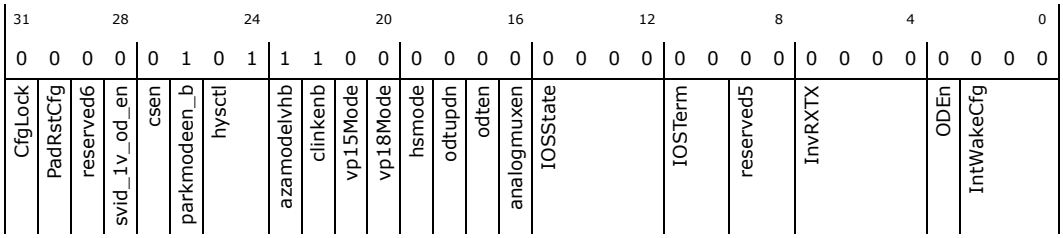
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4C1Ch

Op Codes:

h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.127 Pad Control Register 0 (SDMMC3_CMD_PAD_CFG0)—Offset 4C20h

Pad Control Register 0

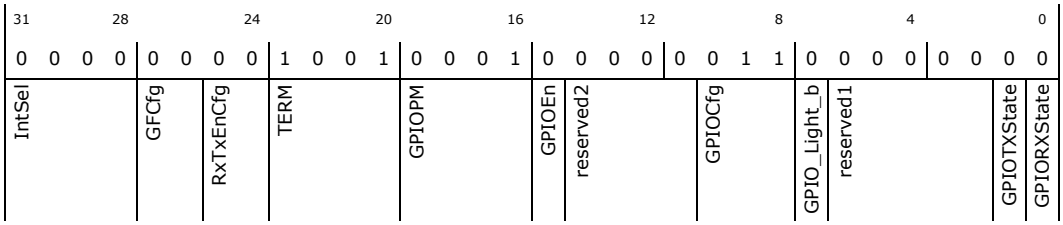
Access Method

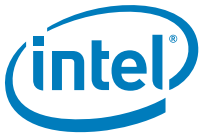
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4C20h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.128 Pad Control Register 1 (SDMMC3_CMD_PAD_CFG1)—Offset 4C24h

Pad Control Register 1

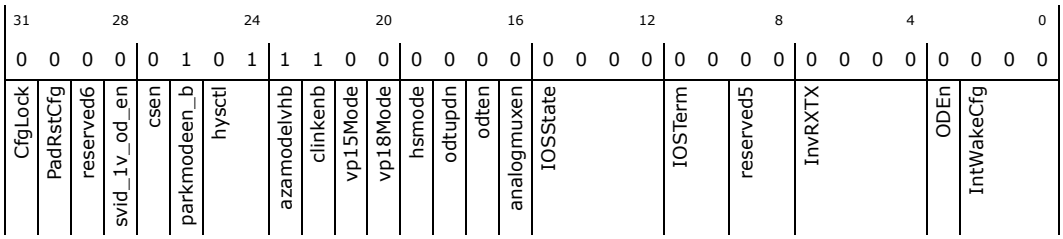
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4C24h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.129 Pad Control Register 0 (SDMMC3_D0_PAD_CFG0)—Offset 4C28h

Pad Control Register 0

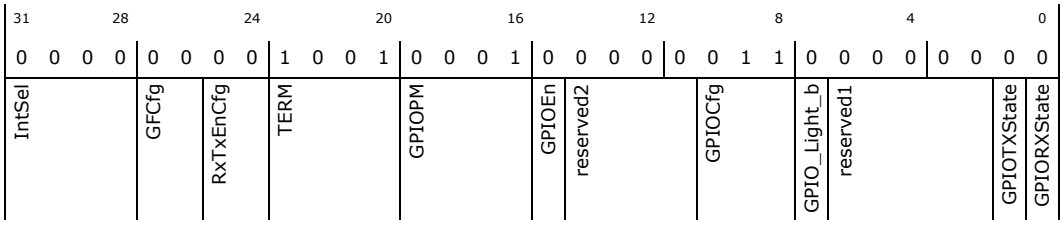
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4C28h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.130 Pad Control Register 1 (SDMMC3_D0_PAD_CFG1)—Offset 4C2Ch

Pad Control Register 1

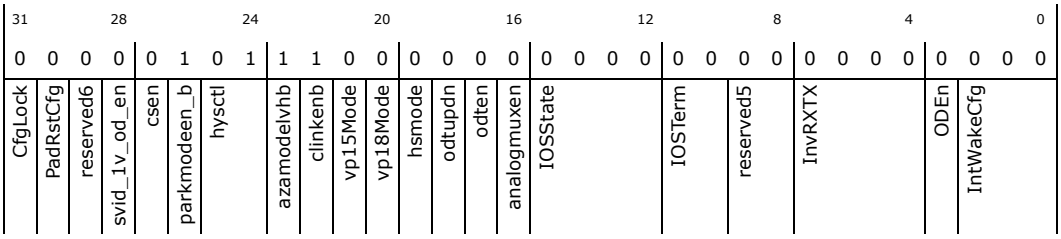
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 4C2Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.131 Pad Control Register 0 (MF_LPC_AD2_PAD_CFG0)—Offset 5000h

Pad Control Register 0

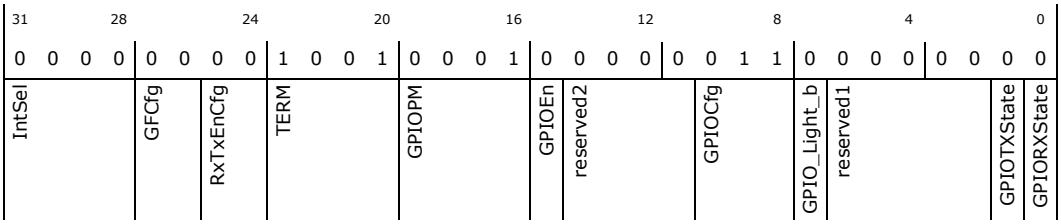
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5000h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.132 Pad Control Register 1 (MF_LPC_AD2_PAD_CFG1)—Offset 5004h

Pad Control Register 1

Access Method

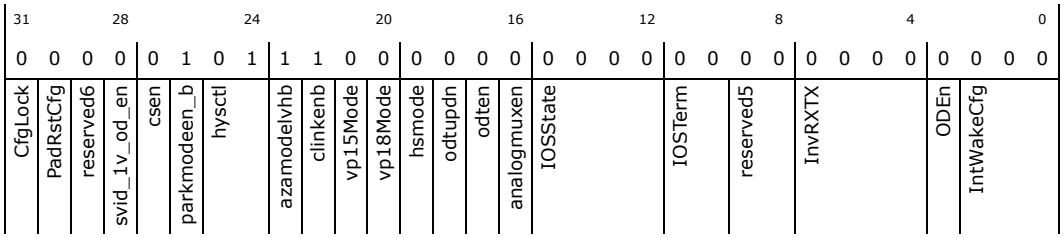
Type: Message Bus Register (Size: 32 bits)

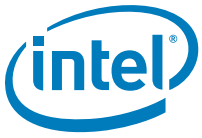
Offset: [Port: 0x48] + 5004h

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.133 Pad Control Register 0 (LPC_CLKRUNB_PAD_CFG0)—Offset 5008h

Pad Control Register 0

Access Method

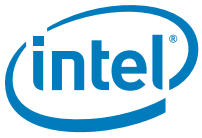
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5008h

Op Codes:
h - Read, h - Write

Default: 00910300h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
IntSel				GFCfg		RxTxEnCfg		TERM			GPIOPM				GPIOEn	reserved2			GPIOCfg				GPIO_Light_b	reserved1				GPIOTXState		GPIORXState	



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.134 Pad Control Register 1 (LPC_CLKRUNB_PAD_CFG1)—Offset 500Ch

Pad Control Register 1

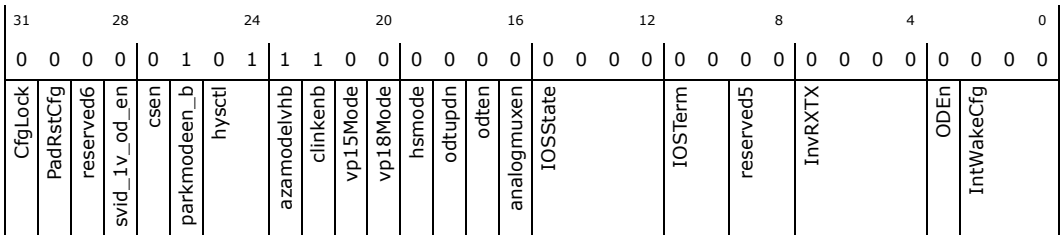
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 500Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.135 Pad Control Register 0 (MF_LPC_AD0_PAD_CFG0)—Offset 5010h

Pad Control Register 0

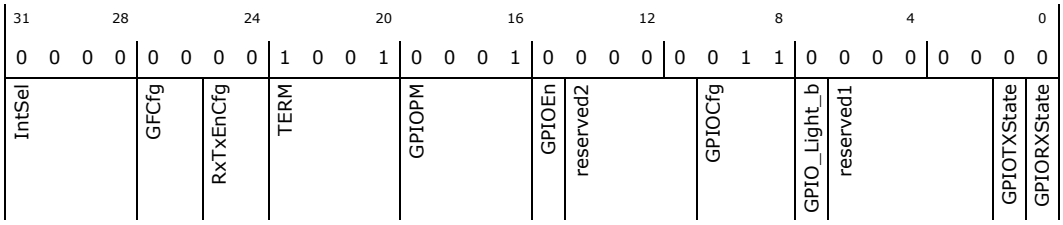
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5010h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.136 Pad Control Register 1 (MF_LPC_AD0_PAD_CFG1)—Offset 5014h

Pad Control Register 1

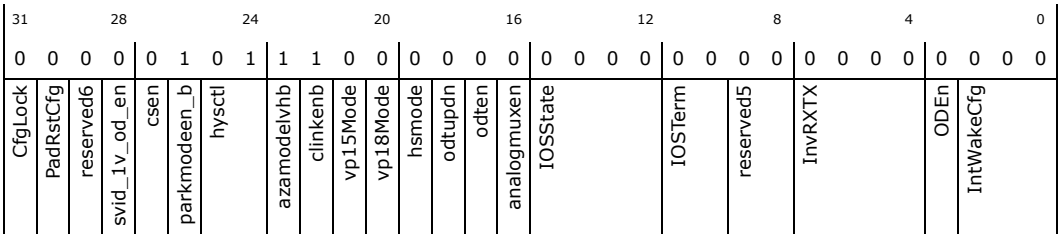
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5014h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.137 Pad Control Register 0 (LPC_FRAMEB_PAD_CFG0)—Offset 5018h

Pad Control Register 0

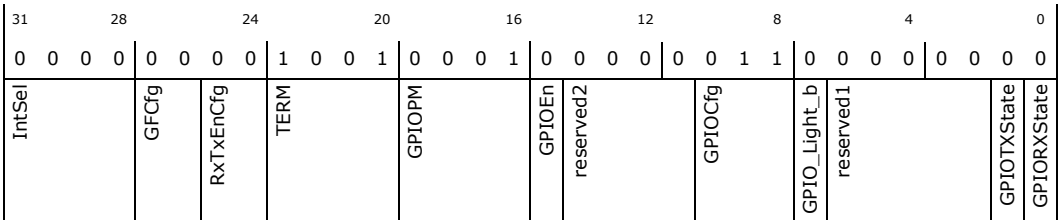
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5018h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.138 Pad Control Register 1 (LPC_FRAMEB_PAD_CFG1)—Offset 501Ch

Pad Control Register 1

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 501Ch

Op Codes:

h - Read, h - Write

Default: 05C00000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CfgLock	PadRstCfg	reserved6	svid_1v_od_en	csen	parkmodeen_b	hysctl		azamodelvhb	clinkenb	vp15Mode	vp18Mode	hsmode	odtupdn	odten	analogmuxen	IOSState				IOSTerm		reserved5		InvRXTX				ODEn	IntWakeCfg		

Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.139 Pad Control Register 0 (MF_LPC_CLKOUT1_PAD_CFG0)—Offset 5020h

Pad Control Register 0

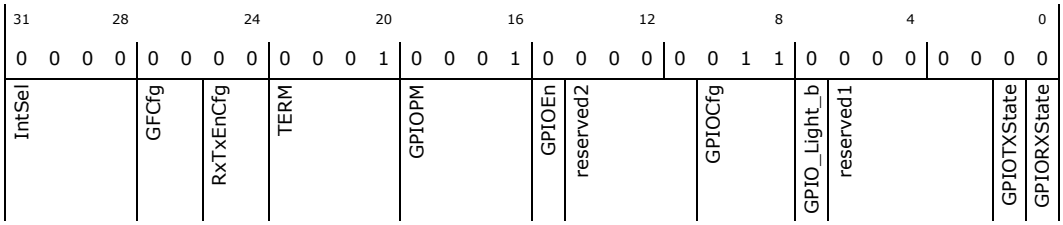
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5020h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.140 Pad Control Register 1 (MF_LPC_CLKOUT1_PAD_CFG1)—Offset 5024h

Pad Control Register 1

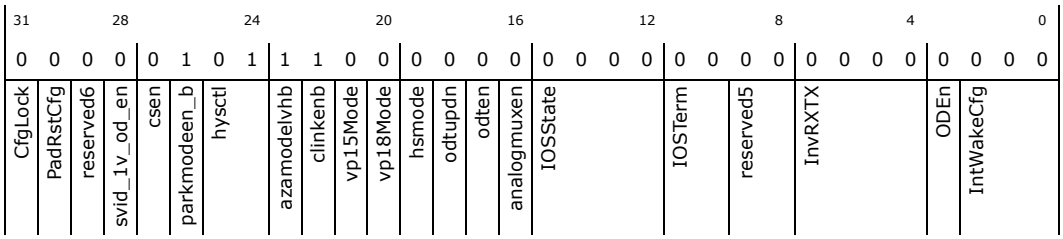
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5024h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.141 Pad Control Register 0 (MF_LPC_AD3_PAD_CFG0)—Offset 5028h

Pad Control Register 0

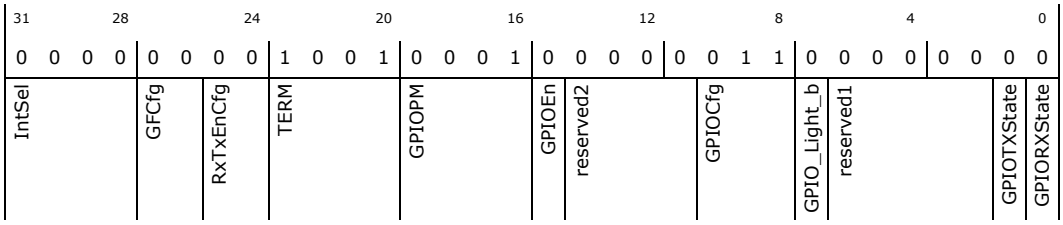
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5028h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.142 Pad Control Register 1 (MF_LPC_AD3_PAD_CFG1)—Offset 502Ch

Pad Control Register 1

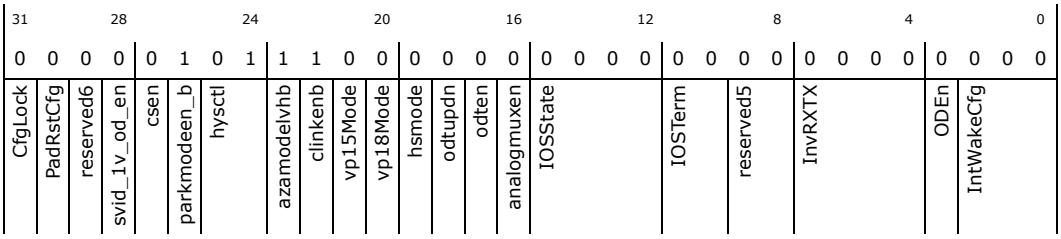
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 502Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.143 Pad Control Register 0 (MF_LPC_CLKOUT0_PAD_CFG0)—Offset 5030h

Pad Control Register 0

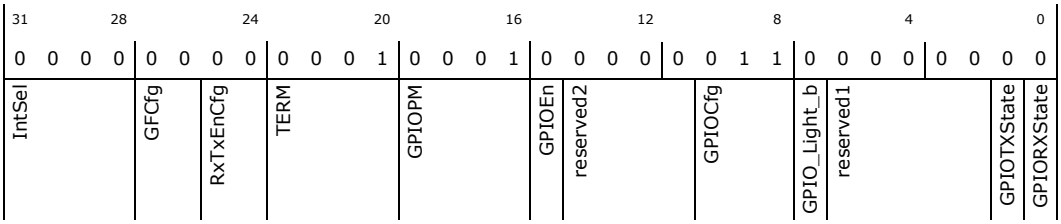
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5030h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.144 Pad Control Register 1 (MF_LPC_CLKOUT0_PAD_CFG1)—Offset 5034h

Pad Control Register 1

Access Method

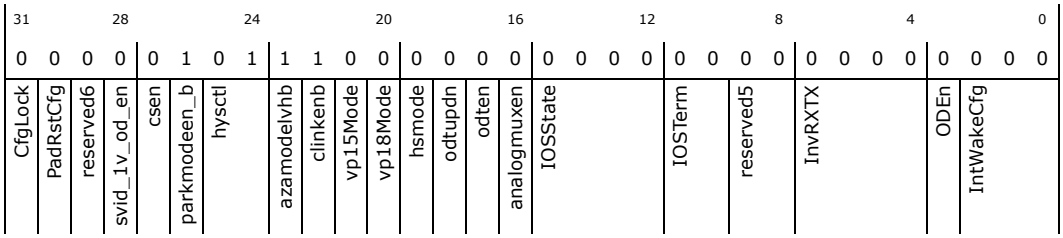
Type: Message Bus Register (Size: 32 bits)

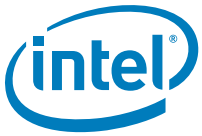
Offset: [Port: 0x48] + 5034h

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.145 Pad Control Register 0 (MF_LPC_AD1_PAD_CFG0)—Offset 5038h

Pad Control Register 0

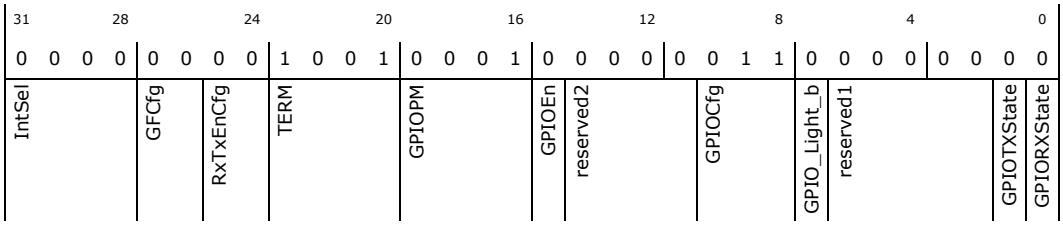
Access Method

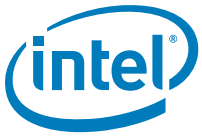
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5038h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.146 Pad Control Register 1 (MF_LPC_AD1_PAD_CFG1)—Offset 503Ch

Pad Control Register 1

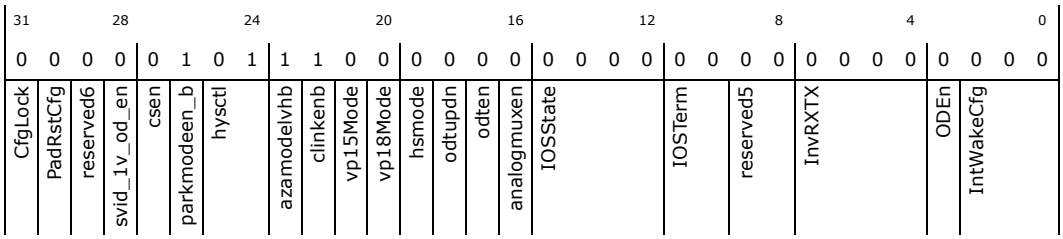
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 503Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.147 Pad Control Register 0 (SPI1_MISO_PAD_CFG0)—Offset 5400h

Pad Control Register 0

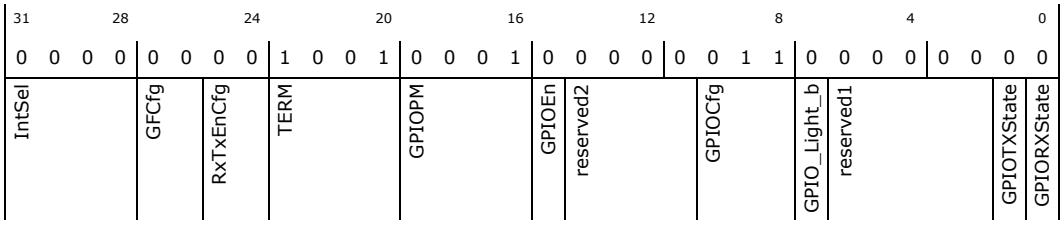
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5400h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.148 Pad Control Register 1 (SPI1_MISO_PAD_CFG1)—Offset 5404h

Pad Control Register 1

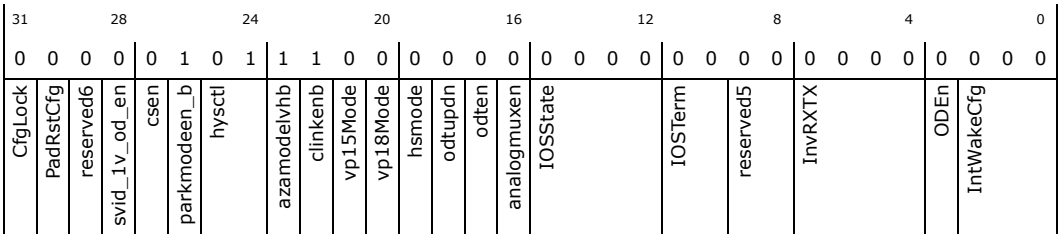
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5404h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.149 Pad Control Register 0 (SPI1_CS0_B_PAD_CFG0)—Offset 5408h

Pad Control Register 0

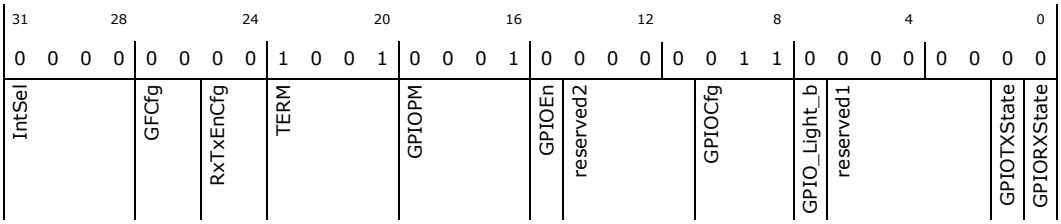
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5408h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.150 Pad Control Register 1 (SPI1_CS0_B_PAD_CFG1)—Offset 540Ch

Pad Control Register 1

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 540Ch

Op Codes:

h - Read, h - Write

Default: 05C00000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CfgLock	PadRstCfg	reserved6	svid_1v_od_en	csen	parkmodeen_b	hysctl		azamodelvhb	clinkenb	vp15Mode	vp18Mode	hsmode	odtupdn	odten	analogmuxen	IOSState				IOSTerm		reserved5		InvRXTX				ODEn	IntWakeCfg		

Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.151 Pad Control Register 0 (SPI1_CLK_PAD_CFG0)—Offset 5410h

Pad Control Register 0

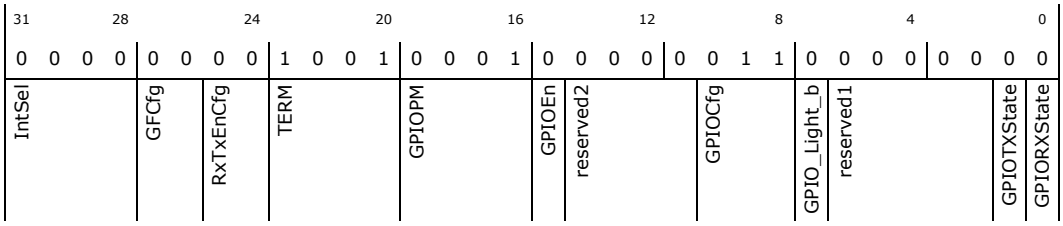
Access Method

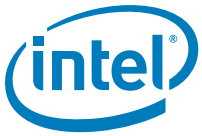
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5410h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.152 Pad Control Register 1 (SPI1_CLK_PAD_CFG1)—Offset 5414h

Pad Control Register 1

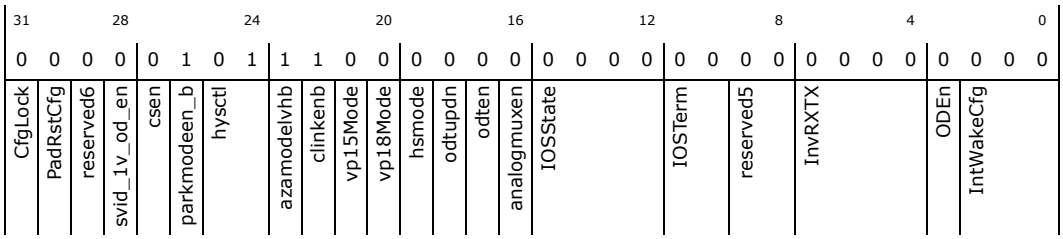
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5414h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.153 Pad Control Register 0 (MMC1_D6_PAD_CFG0)—Offset 5418h

Pad Control Register 0

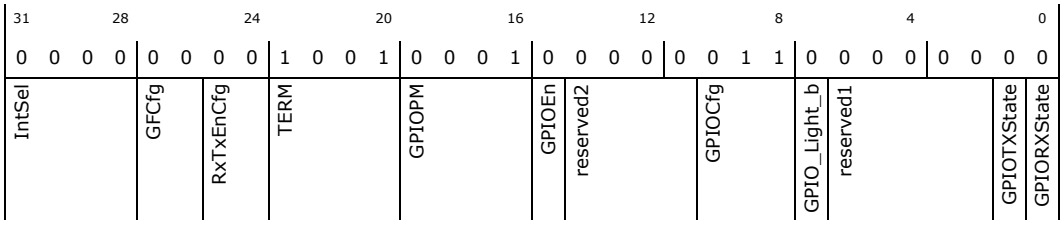
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5418h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.154 Pad Control Register 1 (MMC1_D6_PAD_CFG1)—Offset 541Ch

Pad Control Register 1

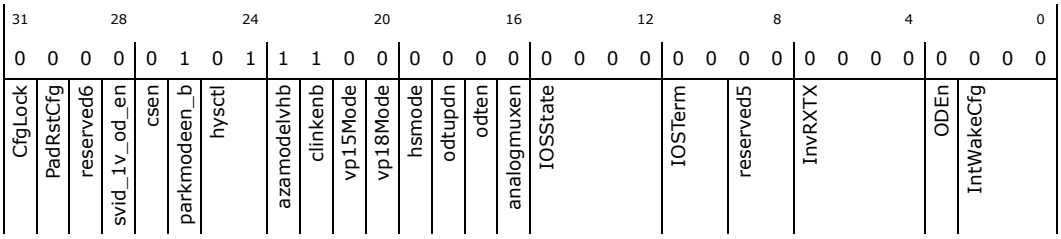
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 541Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.155 Pad Control Register 0 (SPI1_MOSI_PAD_CFG0)—Offset 5420h

Pad Control Register 0

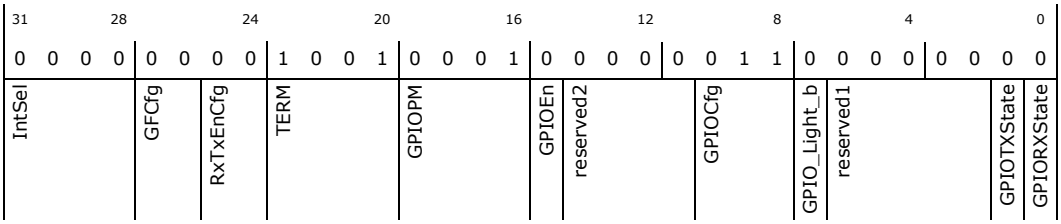
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5420h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.156 Pad Control Register 1 (SPI1_MOSI_PAD_CFG1)—Offset 5424h

Pad Control Register 1

Access Method

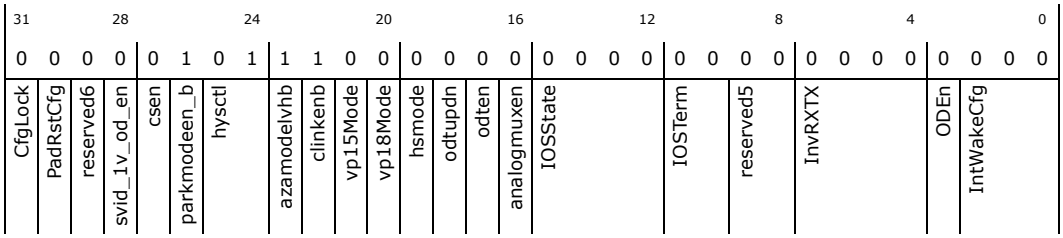
Type: Message Bus Register (Size: 32 bits)

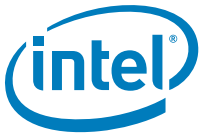
Offset: [Port: 0x48] + 5424h

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.157 Pad Control Register 0 (MMC1_D5_PAD_CFG0)—Offset 5428h

Pad Control Register 0

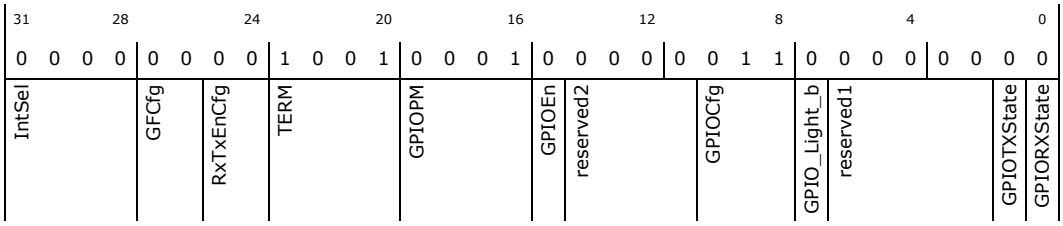
Access Method

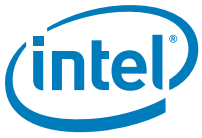
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5428h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.158 Pad Control Register 1 (MMC1_D5_PAD_CFG1)—Offset 542Ch

Pad Control Register 1

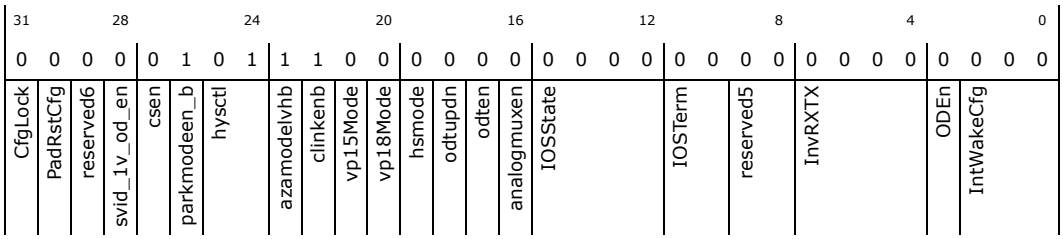
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 542Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.159 Pad Control Register 0 (SPI1_CS1_B_PAD_CFG0)—Offset 5430h

Pad Control Register 0

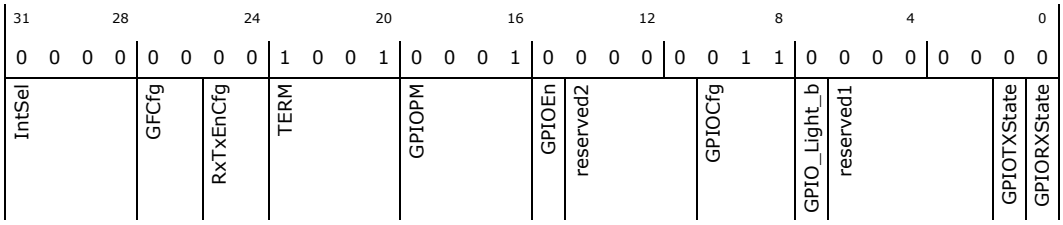
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5430h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.160 Pad Control Register 1 (SPI1_CS1_B_PAD_CFG1)—Offset 5434h

Pad Control Register 1

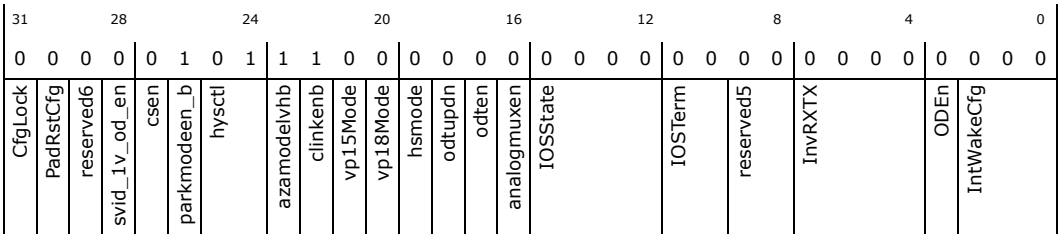
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5434h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.161 Pad Control Register 0 (MMC1_D4_SD_WE_PAD_CFG0)—Offset 5438h

Pad Control Register 0

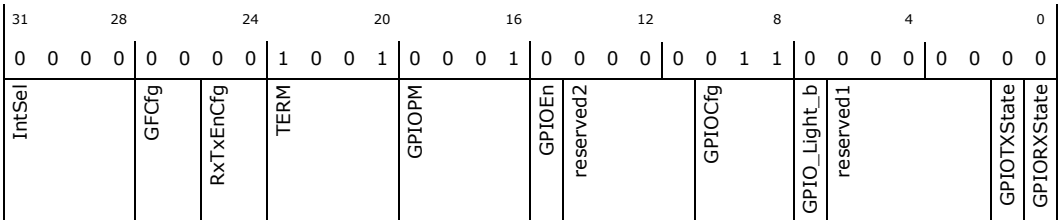
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5438h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.162 Pad Control Register 1 (MMC1_D4_SD_WE_PAD_CFG1)—Offset 543Ch

Pad Control Register 1

Access Method

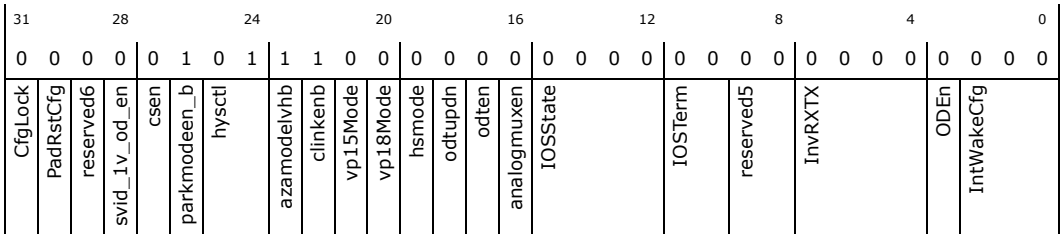
Type: Message Bus Register (Size: 32 bits)

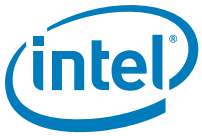
Offset: [Port: 0x48] + 543Ch

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.163 Pad Control Register 0 (MMC1_D7_PAD_CFG0)—Offset 5440h

Pad Control Register 0

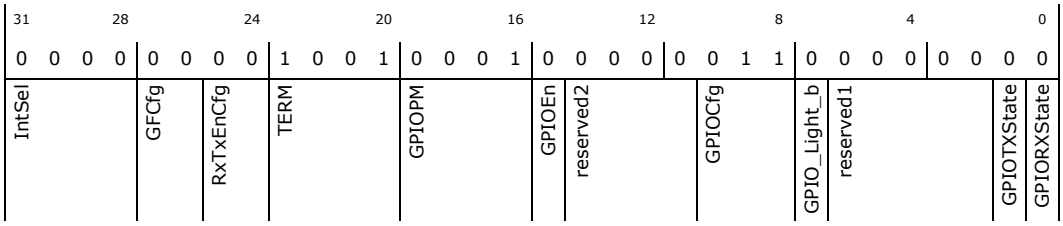
Access Method

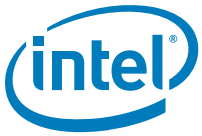
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5440h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.164 Pad Control Register 1 (MMC1_D7_PAD_CFG1)—Offset 5444h

Pad Control Register 1

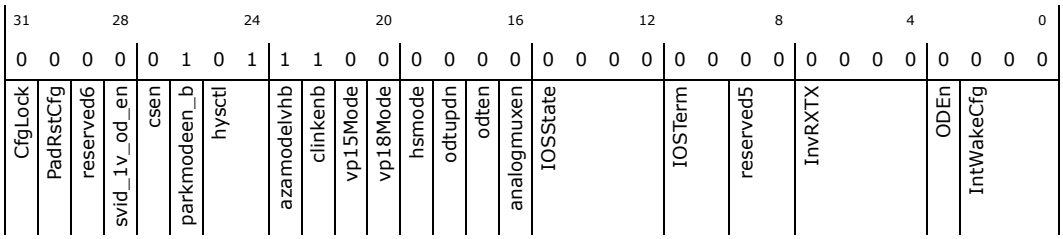
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5444h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.165 Pad Control Register 0 (MMC1_RCLK_PAD_CFG0)—Offset 5448h

Pad Control Register 0

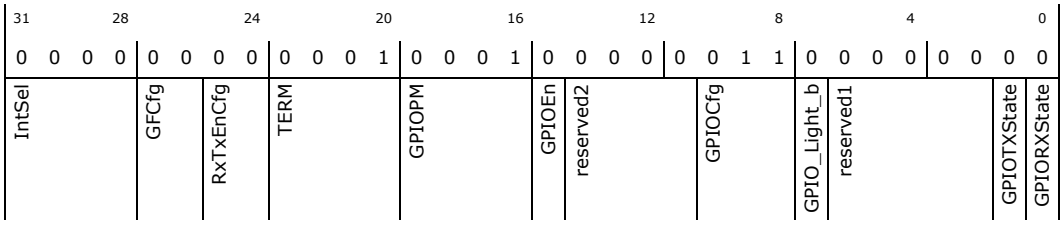
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5448h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.166 Pad Control Register 1 (MMC1_RCLK_PAD_CFG1)—Offset 544Ch

Pad Control Register 1

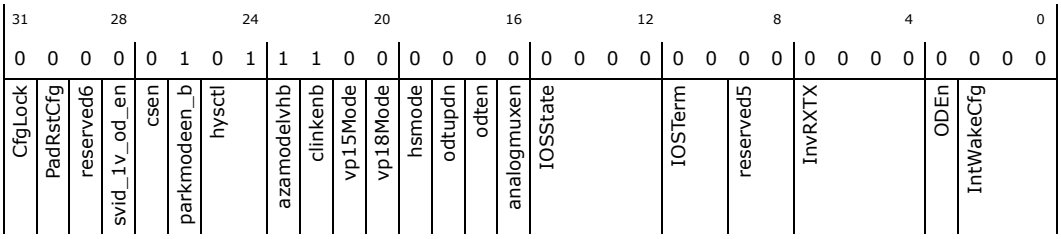
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 544Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.167 Pad Control Register 0 (USB_OC1_B_PAD_CFG0)—Offset 5800h

Pad Control Register 0

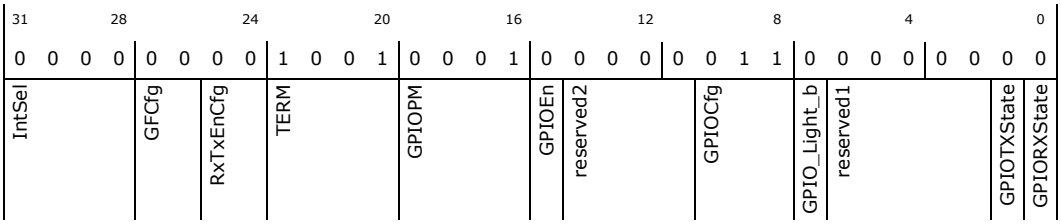
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5800h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.168 Pad Control Register 1 (USB_OC1_B_PAD_CFG1)—Offset 5804h

Pad Control Register 1

Access Method

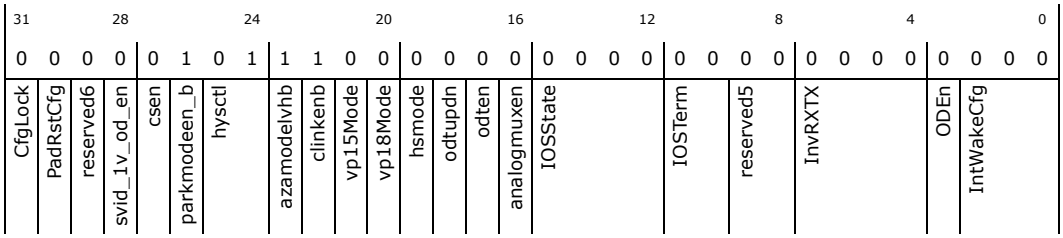
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5804h

Op Codes:

h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.169 Pad Control Register 0 (PMU_RESETBUTTON_B_PAD_CFG0)—Offset 5808h

Pad Control Register 0

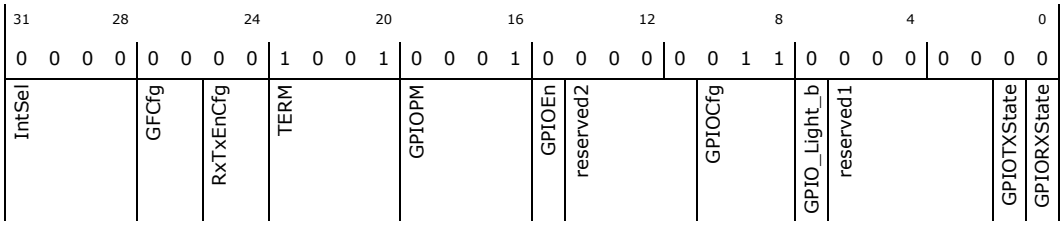
Access Method

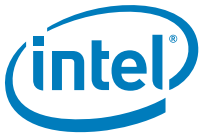
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5808h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.170 Pad Control Register 1 (PMU_RESETBUTTON_B_PAD_CFG1)—Offset 580Ch

Pad Control Register 1

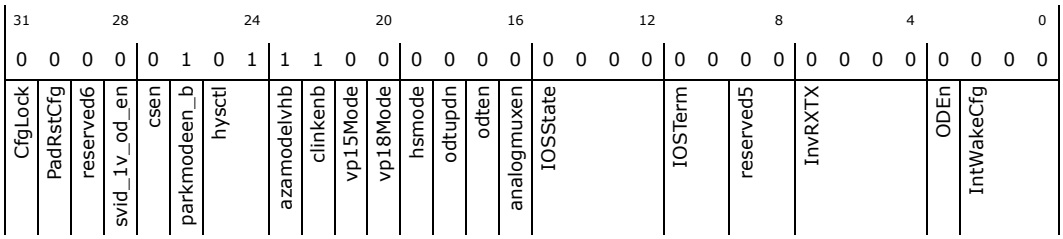
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 580Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.171 Pad Control Register 0 (GPIO_ALERT_PAD_CFG0)—Offset 5810h

Pad Control Register 0

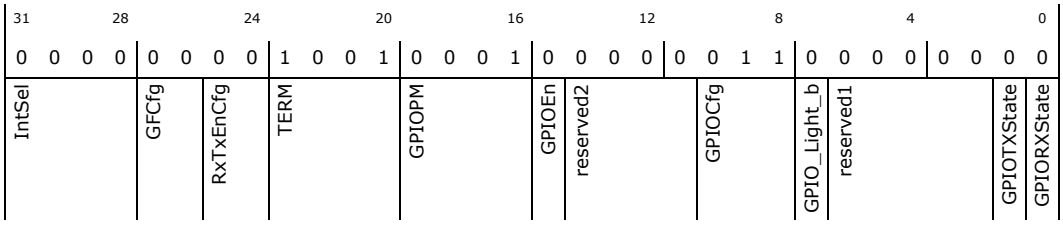
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5810h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.172 Pad Control Register 1 (GPIO_ALERT_PAD_CFG1)—Offset 5814h

Pad Control Register 1

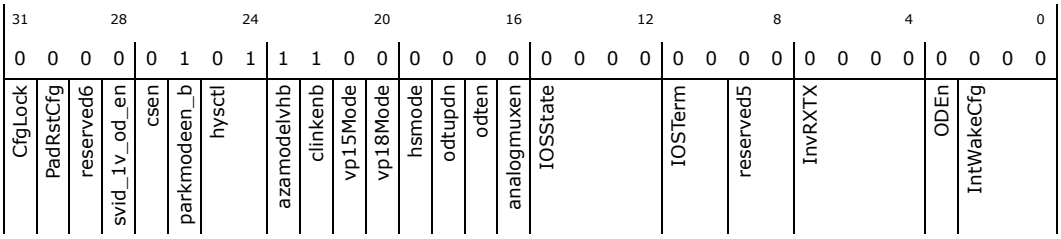
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5814h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.173 Pad Control Register 0 (SDMMC3_PWR_EN_B_PAD_CFG0)—Offset 5818h

Pad Control Register 0

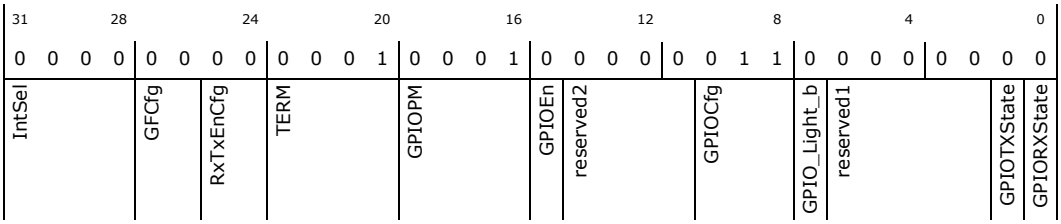
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5818h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.174 Pad Control Register 1 (SDMMC3_PWR_EN_B_PAD_CFG1)—Offset 581Ch

Pad Control Register 1

Access Method

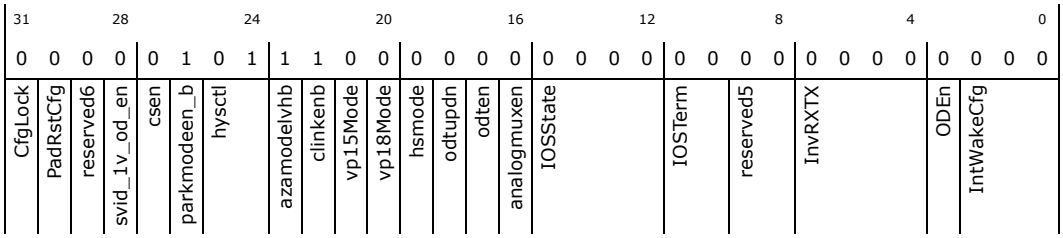
Type: Message Bus Register (Size: 32 bits)

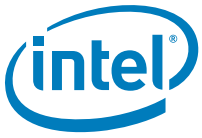
Offset: [Port: 0x48] + 581Ch

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.175 Pad Control Register 0 (ILB_SERIRQ_PAD_CFG0)—Offset 5820h

Pad Control Register 0

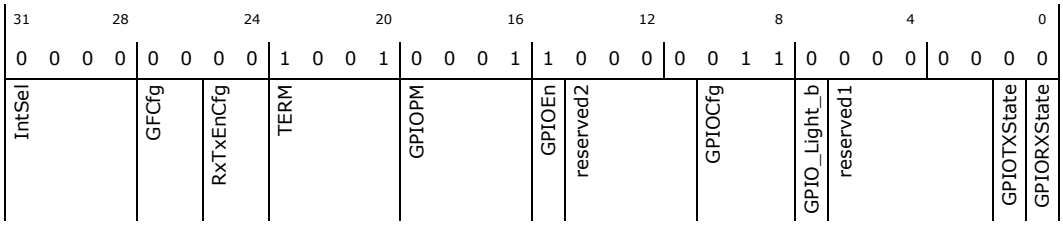
Access Method

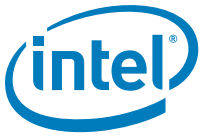
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5820h

Op Codes:
h - Read, h - Write

Default: 00918300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x1 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.176 Pad Control Register 1 (ILB_SERIRQ_PAD_CFG1)—Offset 5824h

Pad Control Register 1

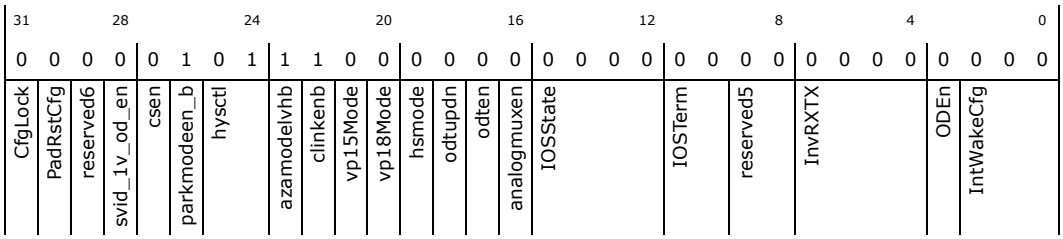
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5824h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.177 Pad Control Register 0 (USB_OC0_B_PAD_CFG0)—Offset 5828h

Pad Control Register 0

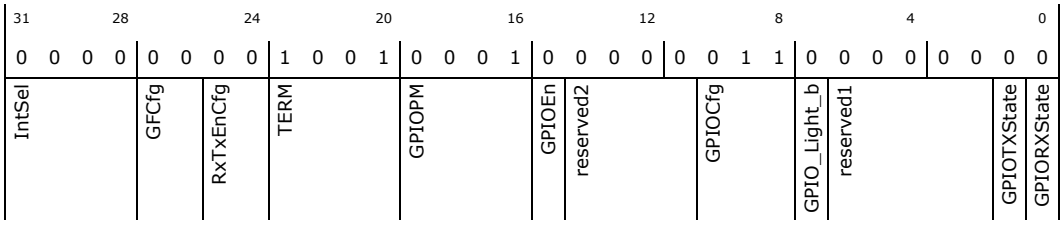
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5828h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.178 Pad Control Register 1 (USB_OC0_B_PAD_CFG1)—Offset 582Ch

Pad Control Register 1

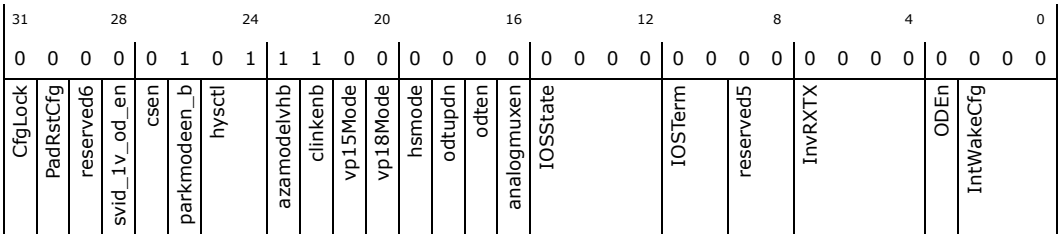
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 582Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.179 Pad Control Register 0 (SDMMC3_CD_B_PAD_CFG0)—Offset 5830h

Pad Control Register 0

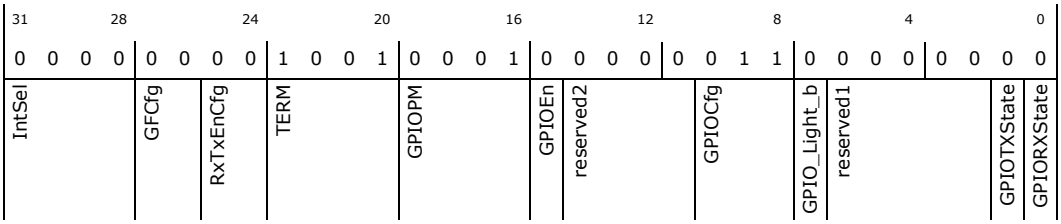
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5830h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.180 Pad Control Register 1 (SDMMC3_CD_B_PAD_CFG1)—Offset 5834h

Pad Control Register 1

Access Method

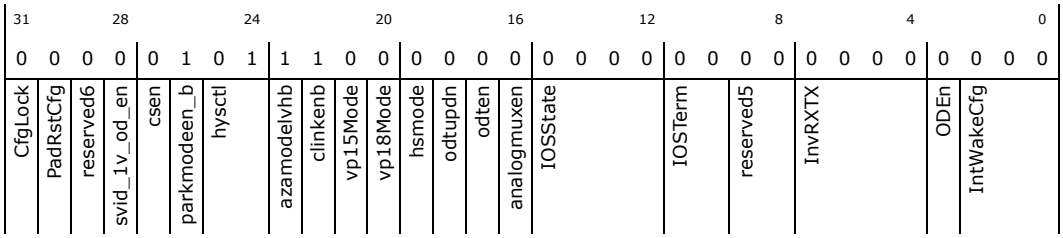
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5834h

Op Codes:

h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.181 Pad Control Register 0 (SPKR_PAD_CFG0)—Offset 5838h

Pad Control Register 0

Access Method

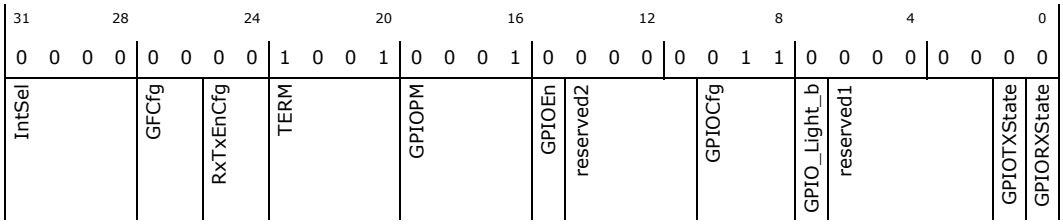
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5838h

Op Codes:

h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.182 Pad Control Register 1 (SPKR_PAD_CFG1)—Offset 583Ch

Pad Control Register 1

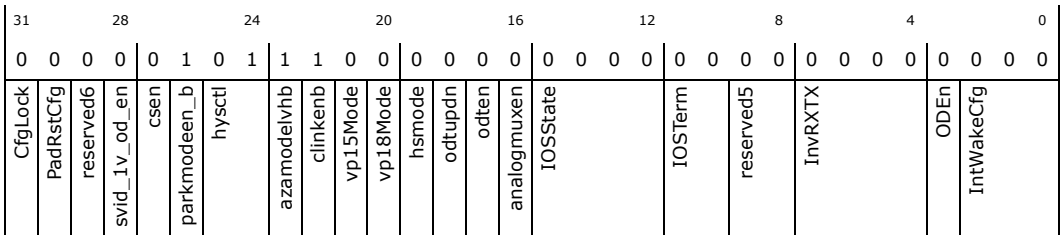
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 583Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.183 Pad Control Register 0 (SUSPWRDNACK_PAD_CFG0)—Offset 5840h

Pad Control Register 0

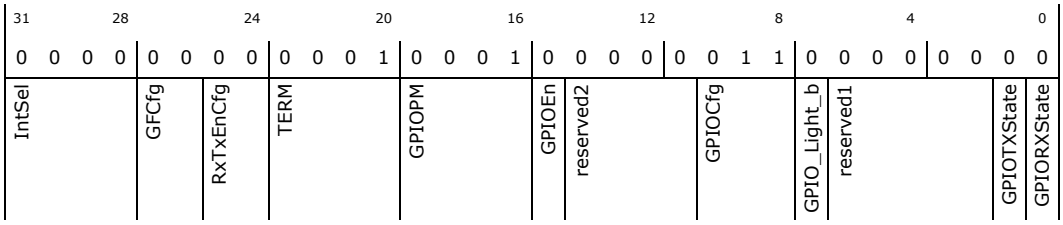
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5840h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.184 Pad Control Register 1 (SUSPWRDNACK_PAD_CFG1)—Offset 5844h

Pad Control Register 1

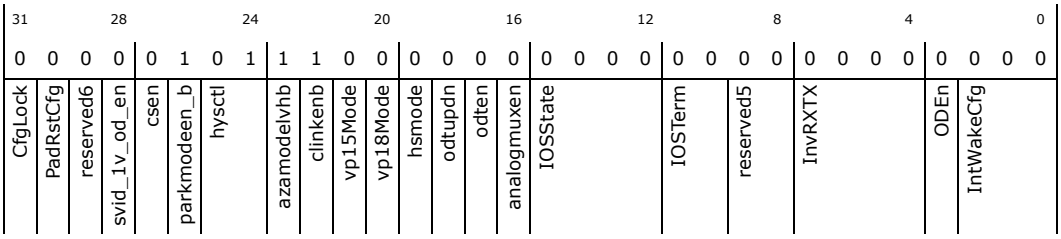
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5844h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.185 Pad Control Register 0 (SPARE_PIN_PAD_CFG0)—Offset 5848h

Pad Control Register 0

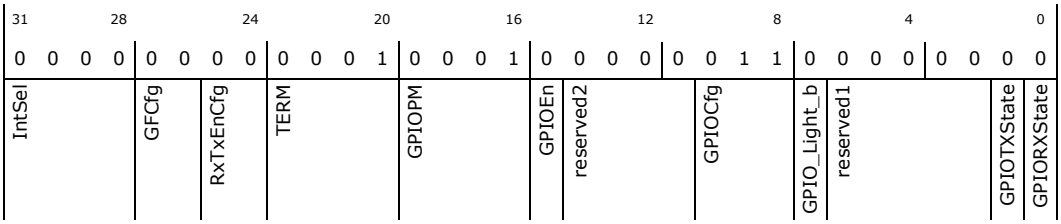
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5848h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.186 Pad Control Register 1 (SPARE_PIN_PAD_CFG1)—Offset 584Ch

Pad Control Register 1

Access Method

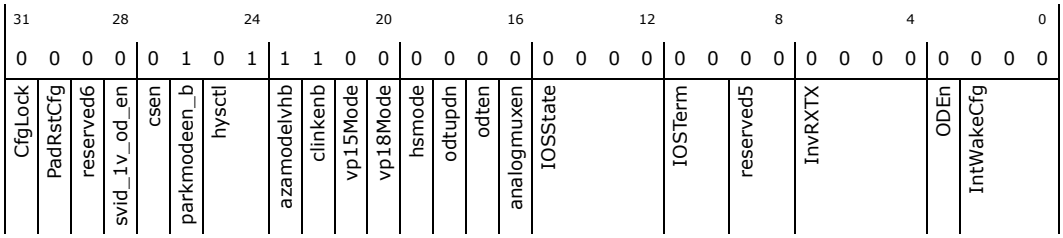
Type: Message Bus Register (Size: 32 bits)

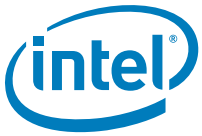
Offset: [Port: 0x48] + 584Ch

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.6.187 Pad Control Register 0 (SDMMC3_1P8_EN_PAD_CFG0)—Offset 5850h

Pad Control Register 0

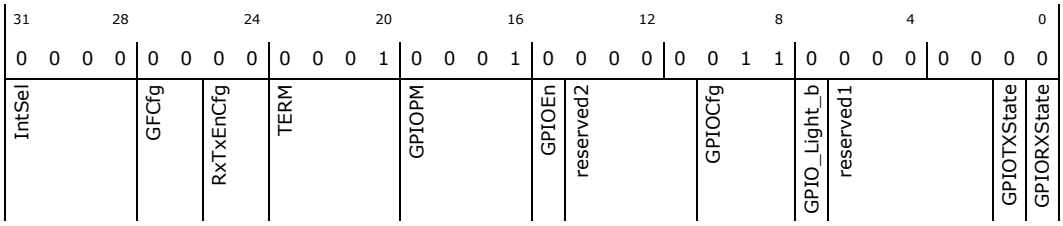
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5850h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.6.188 Pad Control Register 1 (SDMMC3_1P8_EN_PAD_CFG1)—Offset 5854h

Pad Control Register 1

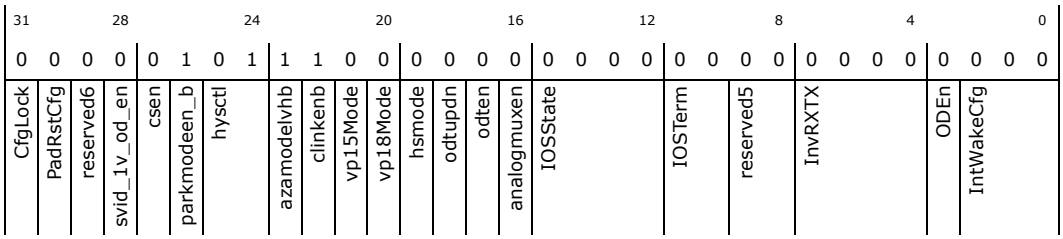
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x48] + 5854h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7 Summary of GPIO SOUTHWEST Message Bus Registers

Table 10-102.Summary of GPIO SouthWest Message Bus Registers—0xB2

Offset	Register Name (Register Symbol)	Default Value
0–3h	"GPIO Read Access Control (gpio_read_access_policy_access_reg)—Offset 0h" on page 5419	FFFFFFFFh
4–7h	"GPIO Read Access Control (gpio_read_access_policy_wake_reg)—Offset 4h" on page 5419	FFFFFFFFh
8–Bh	"GPIO Read Access Control (gpio_read_access_policy_interrupt_reg)—Offset 8h" on page 5420	FFFFFFFFh
C–Fh	"GPIO Read Access Control (gpio_read_access_policy_community_reg)—Offset Ch" on page 5420	FFFFFFFFh
10–13h	"GPIO Read Access Control (gpio_read_access_policy_family_broadcast_reg)—Offset 10h" on page 5421	FFFFFFFFh
14–17h	"GPIO Read Access Control (gpio_read_access_policy_family_reg)—Offset 14h" on page 5421	FFFFFFFFh
18–1Bh	"GPIO Read Access Control (gpio_read_access_policy_pad_broadcast_reg)—Offset 18h" on page 5422	FFFFFFFFh
1C–1Fh	"GPIO Read Access Control (gpio_read_access_policy_ulphsmvfamily_2x3_8_1_regs)—Offset 1Ch" on page 5423	FFFFFFFFh
20–23h	"GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_2x3_8_6_regs)—Offset 20h" on page 5423	FFFFFFFFh
24–27h	"GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_2x3_8_5_regs)—Offset 24h" on page 5424	FFFFFFFFh
28–2Bh	"GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_2x3_8_4_regs)—Offset 28h" on page 5424	FFFFFFFFh
2C–2Fh	"GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_2x3_8_3_regs)—Offset 2Ch" on page 5425	FFFFFFFFh
30–33h	"GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_2x3_8_1_regs)—Offset 30h" on page 5425	FFFFFFFFh
34–37h	"GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_2x3_8_0_regs)—Offset 34h" on page 5426	FFFFFFFFh
100–103h	"GPIO Write Access Control (gpio_write_access_policy_access_reg)—Offset 100h" on page 5427	FFFFFFFFh
104–107h	"GPIO Write Access Control (gpio_write_access_policy_wake_reg)—Offset 104h" on page 5427	FFFFFFFFh
108–10Bh	"GPIO Write Access Control (gpio_write_access_policy_interrupt_reg)—Offset 108h" on page 5428	FFFFFFFFh
10C–10Fh	"GPIO Write Access Control (gpio_write_access_policy_community_reg)—Offset 10Ch" on page 5428	FFFFFFFFh
110–113h	"GPIO Write Access Control (gpio_write_access_policy_family_broadcast_reg)—Offset 110h" on page 5429	FFFFFFFFh
114–117h	"GPIO Write Access Control (gpio_write_access_policy_family_reg)—Offset 114h" on page 5429	FFFFFFFFh
118–11Bh	"GPIO Write Access Control (gpio_write_access_policy_pad_broadcast_reg)—Offset 118h" on page 5430	FFFFFFFFh
11C–11Fh	"GPIO Write Access Control (gpio_write_access_policy_ulphsmvfamily_2x3_8_1_regs)—Offset 11Ch" on page 5431	FFFFFFFFh
120–123h	"GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_2x3_8_6_regs)—Offset 120h" on page 5431	FFFFFFFFh
124–127h	"GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_2x3_8_5_regs)—Offset 124h" on page 5432	FFFFFFFFh
128–12Bh	"GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_2x3_8_4_regs)—Offset 128h" on page 5432	FFFFFFFFh
12C–12Fh	"GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_2x3_8_3_regs)—Offset 12Ch" on page 5433	FFFFFFFFh

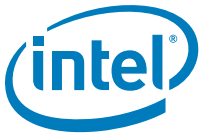


Table 10-102.Summary of GPIO SouthWest Message Bus Registers—0xB2 (Continued)

Offset	Register Name (Register Symbol)	Default Value
130–133h	"GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_2x3_8_1_regs)—Offset 130h" on page 5433	FFFFFFFFh
134–137h	"GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_2x3_8_0_regs)—Offset 134h" on page 5434	FFFFFFFFh
200–203h	"GPIO_WAKE_STATUS_REG #0 (gpio_wake_status_reg_0)—Offset 200h" on page 5434	00000000h
204–207h	"GPIO_WAKE_STATUS_REG #1 (gpio_wake_status_reg_1)—Offset 204h" on page 5436	00000000h
280–283h	"GPIO_WAKE_MASK_REG #0 (gpio_wake_mask_reg_0)—Offset 280h" on page 5438	00000000h
284–287h	"GPIO_WAKE_MASK_REG #1 (gpio_wake_mask_reg_1)—Offset 284h" on page 5439	00000000h
300–303h	"GPIO Interrupt Status (gpio_interrupt_status)—Offset 300h" on page 5441	00000000h
380–383h	"GPIO Interrupt Status (gpio_interrupt_mask)—Offset 380h" on page 5441	00000000h
1000–1003h	"GPIO Broadcast Data Mask bit Register (gpio_family_bw_mask_31_0)—Offset 1000h" on page 5442	00000000h
1004–1007h	"GPIO Broadcast Data Register (gpio_family_bw_data_31_0)—Offset 1004h" on page 5442	00000000h
1008–100Bh	"gpio_family_broadcast_reg_mask #0 (gpio_family_broadcast_reg_mask_0)—Offset 1008h" on page 5443	00000000h
100C–100Fh	"gpio_family_broadcast_reg_mask #1 (gpio_family_broadcast_reg_mask_1)—Offset 100Ch" on page 5446	00000000h
1090–1093h	"family_config_rcomp_reg (ulphsmvfamily_2x3_8_1_family_config_rcomp_reg)—Offset 1090h" on page 5447	41410300h
1094–1097h	"gpio_family_configuration_register (ulphsmvfamily_2x3_8_1_family_config_reg)—Offset 1094h" on page 5448	05C00000h
1110–1113h	"family_config_rcomp_reg (ulpmsmvfamily_2x3_8_6_family_config_rcomp_reg)—Offset 1110h" on page 5449	02020311h
1114–1117h	"gpio_family_configuration_register (ulpmsmvfamily_2x3_8_6_family_config_reg)—Offset 1114h" on page 5450	05C00000h
1190–1193h	"family_config_rcomp_reg (ulpmsmvfamily_2x3_8_5_family_config_rcomp_reg)—Offset 1190h" on page 5451	02020311h
1194–1197h	"gpio_family_configuration_register (ulpmsmvfamily_2x3_8_5_family_config_reg)—Offset 1194h" on page 5452	05C00000h
1210–1213h	"family_config_rcomp_reg (ulpmsmvfamily_2x3_8_4_family_config_rcomp_reg)—Offset 1210h" on page 5453	02020311h
1214–1217h	"gpio_family_configuration_register (ulpmsmvfamily_2x3_8_4_family_config_reg)—Offset 1214h" on page 5454	05C00000h
1290–1293h	"family_config_rcomp_reg (ulpmsmvfamily_2x3_8_3_family_config_rcomp_reg)—Offset 1290h" on page 5455	02020311h
1294–1297h	"gpio_family_configuration_register (ulpmsmvfamily_2x3_8_3_family_config_reg)—Offset 1294h" on page 5456	05C00000h
1310–1313h	"family_config_rcomp_reg (ulpmsmvfamily_2x3_8_1_family_config_rcomp_reg)—Offset 1310h" on page 5457	02020311h
1314–1317h	"gpio_family_configuration_register (ulpmsmvfamily_2x3_8_1_family_config_reg)—Offset 1314h" on page 5458	05C00000h
1390–1393h	"family_config_rcomp_reg (ulpmsmvfamily_2x3_8_0_family_config_rcomp_reg)—Offset 1390h" on page 5459	02020311h
1394–1397h	"gpio_family_configuration_register (ulpmsmvfamily_2x3_8_0_family_config_reg)—Offset 1394h" on page 5460	05C00000h
4000–4003h	"GPIO Broadcast Data Mask bit Register (gpio_pad_bw_mask_31_0)—Offset 4000h" on page 5461	00000000h

Table 10-102.Summary of GPIO SouthWest Message Bus Registers—0xB2 (Continued)

Offset	Register Name (Register Symbol)	Default Value
4004–4007h	"GPIO Broadcast Data Register (gpio_pad_bw_data_31_0)—Offset 4004h" on page 5462	00000000h
4008–400Bh	"gpio_pad_broadcast_reg_mask #0 (gpio_pad_broadcast_reg_mask_0)—Offset 4008h" on page 5462	00000000h
400C–400Fh	"gpio_pad_broadcast_reg_mask #1 (gpio_pad_broadcast_reg_mask_1)—Offset 400Ch" on page 5464	00000000h
4010–4013h	"gpio_pad_broadcast_reg_mask #2 (gpio_pad_broadcast_reg_mask_2)—Offset 4010h" on page 5466	00000000h
4014–4017h	"gpio_pad_broadcast_reg_mask #3 (gpio_pad_broadcast_reg_mask_3)—Offset 4014h" on page 5467	00000000h
4400–4403h	"Pad Control Register 0 (FST_SPI_D2_PAD_CFG0)—Offset 4400h" on page 5469	00910300h
4404–4407h	"Pad Control Register 1 (FST_SPI_D2_PAD_CFG1)—Offset 4404h" on page 5470	05C00000h
4408–440Bh	"Pad Control Register 0 (FST_SPI_D0_PAD_CFG0)—Offset 4408h" on page 5472	00910300h
440C–440Fh	"Pad Control Register 1 (FST_SPI_D0_PAD_CFG1)—Offset 440Ch" on page 5473	05C00000h
4410–4413h	"Pad Control Register 0 (FST_SPI_CLK_PAD_CFG0)—Offset 4410h" on page 5475	00910300h
4414–4417h	"Pad Control Register 1 (FST_SPI_CLK_PAD_CFG1)—Offset 4414h" on page 5477	05C00000h
4418–441Bh	"Pad Control Register 0 (FST_SPI_D3_PAD_CFG0)—Offset 4418h" on page 5479	00910300h
441C–441Fh	"Pad Control Register 1 (FST_SPI_D3_PAD_CFG1)—Offset 441Ch" on page 5480	05C00000h
4420–4423h	"Pad Control Register 0 (FST_SPI_CS1_B_PAD_CFG0)—Offset 4420h" on page 5482	00910300h
4424–4427h	"Pad Control Register 1 (FST_SPI_CS1_B_PAD_CFG1)—Offset 4424h" on page 5483	05C00000h
4428–442Bh	"Pad Control Register 0 (FST_SPI_D1_PAD_CFG0)—Offset 4428h" on page 5486	00910300h
442C–442Fh	"Pad Control Register 1 (FST_SPI_D1_PAD_CFG1)—Offset 442Ch" on page 5488	05C00000h
4430–4433h	"Pad Control Register 0 (FST_SPI_CS0_B_PAD_CFG0)—Offset 4430h" on page 5490	00910300h
4434–4437h	"Pad Control Register 1 (FST_SPI_CS0_B_PAD_CFG1)—Offset 4434h" on page 5491	05C00000h
4438–443Bh	"Pad Control Register 0 (FST_SPI_CS2_B_PAD_CFG0)—Offset 4438h" on page 5493	00910300h
443C–443Fh	"Pad Control Register 1 (FST_SPI_CS2_B_PAD_CFG1)—Offset 443Ch" on page 5495	05C00000h
4800–4803h	"Pad Control Register 0 (UART1_RTS_B_PAD_CFG0)—Offset 4800h" on page 5497	00910300h
4804–4807h	"Pad Control Register 1 (UART1_RTS_B_PAD_CFG1)—Offset 4804h" on page 5498	05C00000h
4808–480Bh	"Pad Control Register 0 (UART1_RXD_PAD_CFG0)—Offset 4808h" on page 5500	00910300h

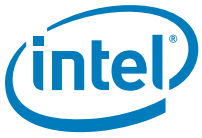


Table 10-102.Summary of GPIO SouthWest Message Bus Registers—0xB2 (Continued)

Offset	Register Name (Register Symbol)	Default Value
480C–480Fh	"Pad Control Register 1 (UART1_RXD_PAD_CFG1)—Offset 480Ch" on page 5501	05C00000h
4810–4813h	"Pad Control Register 0 (UART2_RXD_PAD_CFG0)—Offset 4810h" on page 5503	00910300h
4814–4817h	"Pad Control Register 1 (UART2_RXD_PAD_CFG1)—Offset 4814h" on page 5505	05C00000h
4818–481Bh	"Pad Control Register 0 (UART1_CTS_B_PAD_CFG0)—Offset 4818h" on page 5507	00910300h
481C–481Fh	"Pad Control Register 1 (UART1_CTS_B_PAD_CFG1)—Offset 481Ch" on page 5508	05C00000h
4820–4823h	"Pad Control Register 0 (UART2_RTS_B_PAD_CFG0)—Offset 4820h" on page 5510	00910300h
4824–4827h	"Pad Control Register 1 (UART2_RTS_B_PAD_CFG1)—Offset 4824h" on page 5511	05C00000h
4828–482Bh	"Pad Control Register 0 (UART1_TXD_PAD_CFG0)—Offset 4828h" on page 5513	00910300h
482C–482Fh	"Pad Control Register 1 (UART1_TXD_PAD_CFG1)—Offset 482Ch" on page 5515	05C00000h
4830–4833h	"Pad Control Register 0 (UART2_TXD_PAD_CFG0)—Offset 4830h" on page 5517	00910300h
4834–4837h	"Pad Control Register 1 (UART2_TXD_PAD_CFG1)—Offset 4834h" on page 5518	05C00000h
4838–483Bh	"Pad Control Register 0 (UART2_CTS_B_PAD_CFG0)—Offset 4838h" on page 5520	00910300h
483C–483Fh	"Pad Control Register 1 (UART2_CTS_B_PAD_CFG1)—Offset 483Ch" on page 5521	05C00000h
5000–5003h	"Pad Control Register 0 (I2C5_SDA_PAD_CFG0)—Offset 5000h" on page 5523	00910300h
5004–5007h	"Pad Control Register 1 (I2C5_SDA_PAD_CFG1)—Offset 5004h" on page 5525	05C00020h
5008–500Bh	"Pad Control Register 0 (I2C4_SDA_PAD_CFG0)—Offset 5008h" on page 5527	00910300h
500C–500Fh	"Pad Control Register 1 (I2C4_SDA_PAD_CFG1)—Offset 500Ch" on page 5528	05C00020h
5010–5013h	"Pad Control Register 0 (I2C6_SDA_PAD_CFG0)—Offset 5010h" on page 5530	00910300h
5014–5017h	"Pad Control Register 1 (I2C6_SDA_PAD_CFG1)—Offset 5014h" on page 5531	05C00020h
5018–501Bh	"Pad Control Register 0 (I2C5_SCL_PAD_CFG0)—Offset 5018h" on page 5533	00910300h
501C–501Fh	"Pad Control Register 1 (I2C5_SCL_PAD_CFG1)—Offset 501Ch" on page 5535	05C00020h
5020–5023h	"Pad Control Register 0 (I2C_NFC_SDA_PAD_CFG0)—Offset 5020h" on page 5537	00910300h
5024–5027h	"Pad Control Register 1 (I2C_NFC_SDA_PAD_CFG1)—Offset 5024h" on page 5538	05C00020h
5028–502Bh	"Pad Control Register 0 (I2C4_SCL_PAD_CFG0)—Offset 5028h" on page 5540	00910300h

Table 10-102.Summary of GPIO SouthWest Message Bus Registers—0xB2 (Continued)

Offset	Register Name (Register Symbol)	Default Value
502C–502Fh	"Pad Control Register 1 (I2C4_SCL_PAD_CFG1)—Offset 502Ch" on page 5541	05C00020h
5030–5033h	"Pad Control Register 0 (I2C6_SCL_PAD_CFG0)—Offset 5030h" on page 5543	00910300h
5034–5037h	"Pad Control Register 1 (I2C6_SCL_PAD_CFG1)—Offset 5034h" on page 5545	05C00020h
5038–503Bh	"Pad Control Register 0 (I2C_NFC_SCL_PAD_CFG0)—Offset 5038h" on page 5547	00910300h
503C–503Fh	"Pad Control Register 1 (I2C_NFC_SCL_PAD_CFG1)—Offset 503Ch" on page 5548	05C00020h
5400–5403h	"Pad Control Register 0 (I2C1_SDA_PAD_CFG0)—Offset 5400h" on page 5550	00910300h
5404–5407h	"Pad Control Register 1 (I2C1_SDA_PAD_CFG1)—Offset 5404h" on page 5551	05C00020h
5408–540Bh	"Pad Control Register 0 (I2C0_SDA_PAD_CFG0)—Offset 5408h" on page 5553	00C10300h
540C–540Fh	"Pad Control Register 1 (I2C0_SDA_PAD_CFG1)—Offset 540Ch" on page 5555	05C00020h
5410–5413h	"Pad Control Register 0 (I2C2_SDA_PAD_CFG0)—Offset 5410h" on page 5557	00910300h
5414–5417h	"Pad Control Register 1 (I2C2_SDA_PAD_CFG1)—Offset 5414h" on page 5558	05C00020h
5418–541Bh	"Pad Control Register 0 (I2C1_SCL_PAD_CFG0)—Offset 5418h" on page 5560	00910300h
541C–541Fh	"Pad Control Register 1 (I2C1_SCL_PAD_CFG1)—Offset 541Ch" on page 5561	05C00020h
5420–5423h	"Pad Control Register 0 (I2C3_SDA_PAD_CFG0)—Offset 5420h" on page 5563	00910300h
5424–5427h	"Pad Control Register 1 (I2C3_SDA_PAD_CFG1)—Offset 5424h" on page 5565	05C00020h
5428–542Bh	"Pad Control Register 0 (I2C0_SCL_PAD_CFG0)—Offset 5428h" on page 5567	00C10300h
542C–542Fh	"Pad Control Register 1 (I2C0_SCL_PAD_CFG1)—Offset 542Ch" on page 5568	05C00020h
5430–5433h	"Pad Control Register 0 (I2C2_SCL_PAD_CFG0)—Offset 5430h" on page 5570	00910300h
5434–5437h	"Pad Control Register 1 (I2C2_SCL_PAD_CFG1)—Offset 5434h" on page 5571	05C00020h
5438–543Bh	"Pad Control Register 0 (I2C3_SCL_PAD_CFG0)—Offset 5438h" on page 5573	00910300h
543C–543Fh	"Pad Control Register 1 (I2C3_SCL_PAD_CFG1)—Offset 543Ch" on page 5575	05C00020h
5800–5803h	"Pad Control Register 0 (PCIE_CLKREQ0B_PAD_CFG0)—Offset 5C00h" on page 5577	00110300h
5804–5807h	"Pad Control Register 0 (PCIE_CLKREQ0B_PAD_CFG0)—Offset 5C00h" on page 5577	05C00000h
5808–580Bh	"Pad Control Register 0 (PCIE_CLKREQ0B_PAD_CFG0)—Offset 5C00h" on page 5577	00110300h

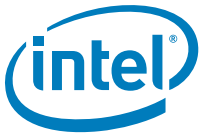


Table 10-102.Summary of GPIO SouthWest Message Bus Registers—0xB2 (Continued)

Offset	Register Name (Register Symbol)	Default Value
5810–5813h	"Pad Control Register 0 (PCIE_CLKREQ0B_PAD_CFG0)—Offset 5C00h" on page 5577	00110300h
5814–5817h	"Pad Control Register 0 (PCIE_CLKREQ0B_PAD_CFG0)—Offset 5C00h" on page 5577	05C00000h
5818–581Bh	"Pad Control Register 0 (PCIE_CLKREQ0B_PAD_CFG0)—Offset 5C00h" on page 5577	00110300h
5820–5823h	"Pad Control Register 0 (PCIE_CLKREQ0B_PAD_CFG0)—Offset 5C00h" on page 5577	00910300h
5824–5827h	"Pad Control Register 0 (PCIE_CLKREQ0B_PAD_CFG0)—Offset 5C00h" on page 5577	05C00000h
5828–582Bh	"Pad Control Register 0 (PCIE_CLKREQ0B_PAD_CFG0)—Offset 5C00h" on page 5577	00110300h
582C–582Fh	"Pad Control Register 0 (PCIE_CLKREQ0B_PAD_CFG0)—Offset 5C00h" on page 5577	05C00000h
5830–5833h	"Pad Control Register 0 (PCIE_CLKREQ0B_PAD_CFG0)—Offset 5C00h" on page 5577	00910300h
5834–5837h	"Pad Control Register 0 (PCIE_CLKREQ0B_PAD_CFG0)—Offset 5C00h" on page 5577	05C00000h
5838–583Bh	"Pad Control Register 0 (PCIE_CLKREQ0B_PAD_CFG0)—Offset 5C00h" on page 5577	00910300h
583C–583Fh	"Pad Control Register 0 (PCIE_CLKREQ0B_PAD_CFG0)—Offset 5C00h" on page 5577	05C00000h
5C00–5C03h	"Pad Control Register 0 (PCIE_CLKREQ0B_PAD_CFG0)—Offset 5C00h" on page 5577	00910300h
5C04–5C07h	"Pad Control Register 1 (PCIE_CLKREQ0B_PAD_CFG1)—Offset 5C04h" on page 5578	05C00000h
5C08–5C0Bh	"Pad Control Register 0 (PCIE_CLKREQ1B_PAD_CFG0)—Offset 5C08h" on page 5580	00910300h
5C0C–5C0Fh	"Pad Control Register 1 (PCIE_CLKREQ1B_PAD_CFG1)—Offset 5C0Ch" on page 5581	05C00000h
5C10–5C13h	"Pad Control Register 0 (GP_SSP_2_CLK_PAD_CFG0)—Offset 5C10h" on page 5584	00110300h
5C14–5C17h	"Pad Control Register 1 (GP_SSP_2_CLK_PAD_CFG1)—Offset 5C14h" on page 5585	05C00000h
5C18–5C1Bh	"Pad Control Register 0 (PCIE_CLKREQ2B_PAD_CFG0)—Offset 5C18h" on page 5587	00910300h
5C1C–5C1Fh	"Pad Control Register 1 (PCIE_CLKREQ2B_PAD_CFG1)—Offset 5C1Ch" on page 5588	05C00000h
5C20–5C23h	"Pad Control Register 0 (GP_SSP_2_RXD_PAD_CFG0)—Offset 5C20h" on page 5590	00110300h
5C24–5C27h	"Pad Control Register 1 (GP_SSP_2_RXD_PAD_CFG1)—Offset 5C24h" on page 5592	05C00000h
5C28–5C2Bh	"Pad Control Register 0 (PCIE_CLKREQ3B_PAD_CFG0)—Offset 5C28h" on page 5594	00910300h
5C2C–5C2Fh	"Pad Control Register 1 (PCIE_CLKREQ3B_PAD_CFG1)—Offset 5C2Ch" on page 5595	05C00000h
5C30–5C33h	"Pad Control Register 0 (GP_SSP_2_FS_PAD_CFG0)—Offset 5C30h" on page 5597	00110300h

Table 10-102.Summary of GPIO SouthWest Message Bus Registers—0xB2 (Continued)

Offset	Register Name (Register Symbol)	Default Value
5C34–5C37h	"Pad Control Register 1 (GP_SSP_2_FS_PAD_CFG1)—Offset 5C34h" on page 5598	05C00000h
5C38–5C3Bh	"Pad Control Register 0 (GP_SSP_2_TXD_PAD_CFG0)—Offset 5C38h" on page 5600	00110300h
5C3C–5C3Fh	"Pad Control Register 1 (GP_SSP_2_TXD_PAD_CFG1)—Offset 5C3Ch" on page 5602	05C00020h

10.7.1 GPIO Read Access Control (gpio_read_access_policy_access_reg)—Offset 0h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

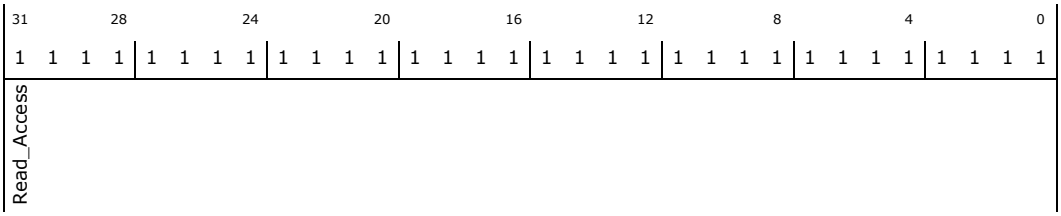
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 0h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.7.2 GPIO Read Access Control (gpio_read_access_policy_wake_reg)—Offset 4h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

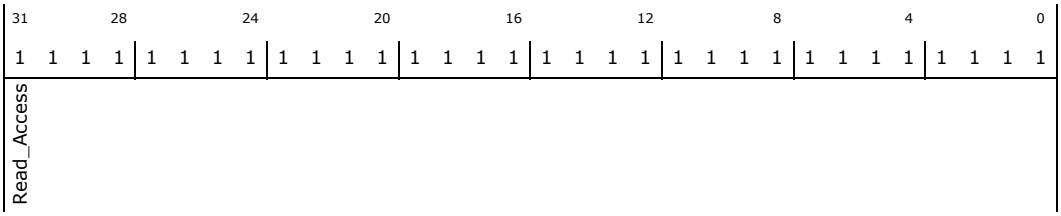
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.7.3 GPIO Read Access Control (gpio_read_access_policy_interrupt_reg)—Offset 8h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

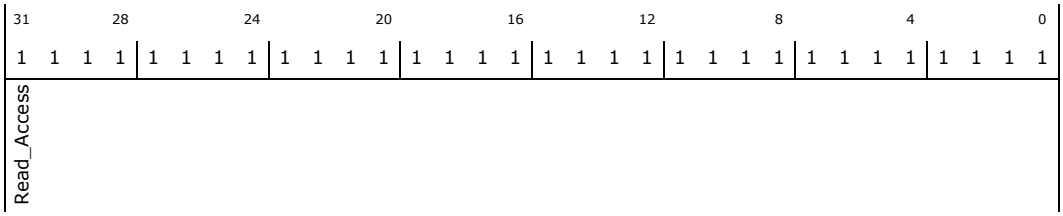
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 8h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.7.4 GPIO Read Access Control (gpio_read_access_policy_community_reg)—Offset Ch

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

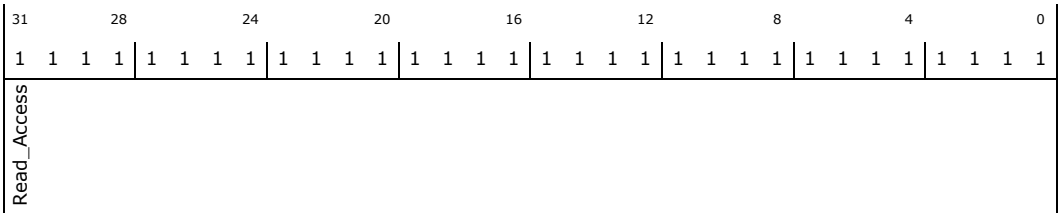
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.7.5 GPIO Read Access Control (gpio_read_access_policy_family_broadcast_reg)—Offset 10h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

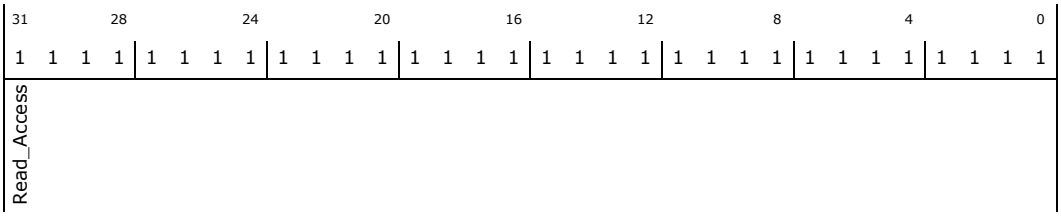
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 10h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.7.6 GPIO Read Access Control (gpio_read_access_policy_family_reg)—Offset 14h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

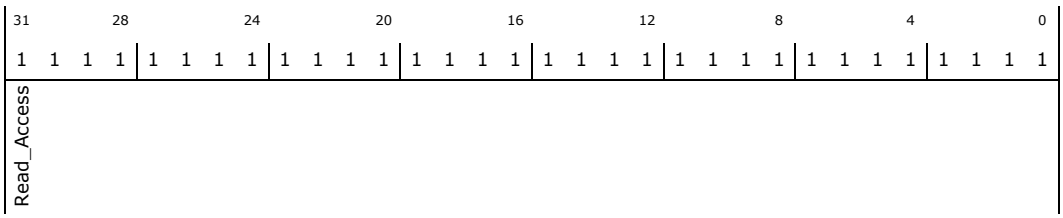
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 14h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.7.7 GPIO Read Access Control (gpio_read_access_policy_pad_broadcast_reg)—Offset 18h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

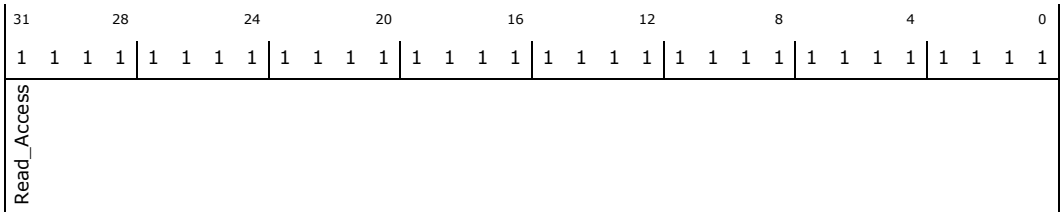
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 18h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.7.8 GPIO Read Access Control (gpio_read_access_policy_ulphsmvfamily_2x3_8_1_regs)—Offset 1Ch

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

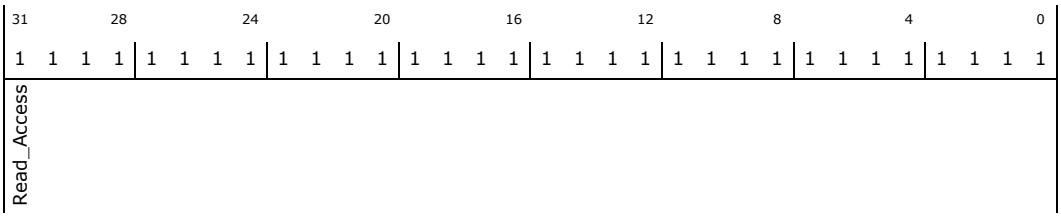
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 1Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.7.9 GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_2x3_8_6_regs)—Offset 20h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

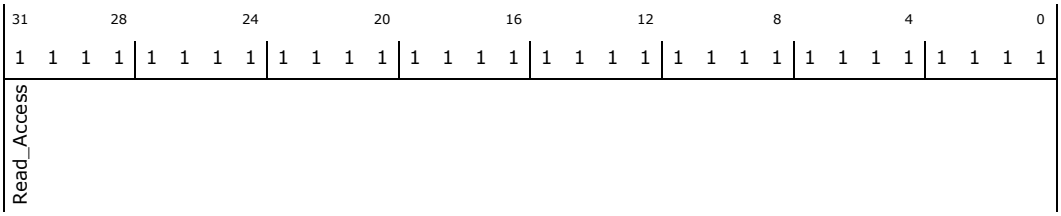
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 20h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.7.10 GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_2x3_8_5_regs)—Offset 24h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

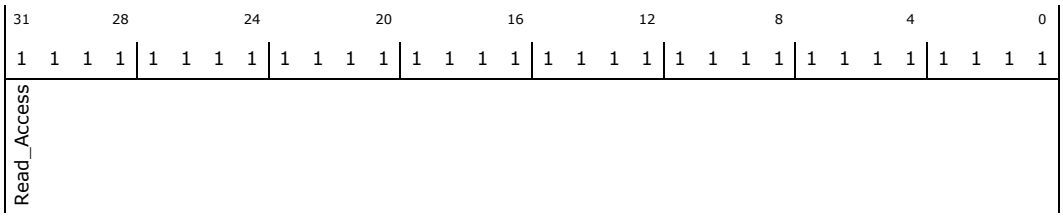
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 24h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.7.11 GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_2x3_8_4_regs)—Offset 28h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

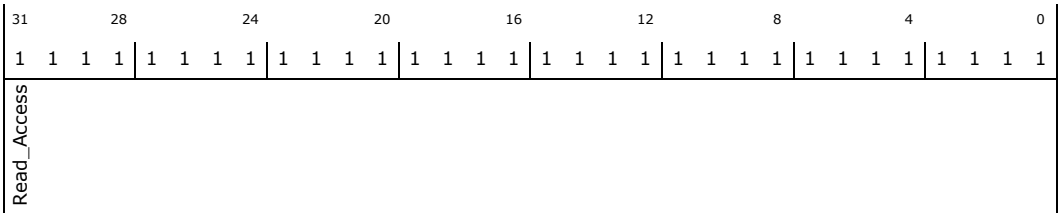
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 28h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.7.12 GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_2x3_8_3_regs)—Offset 2Ch

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

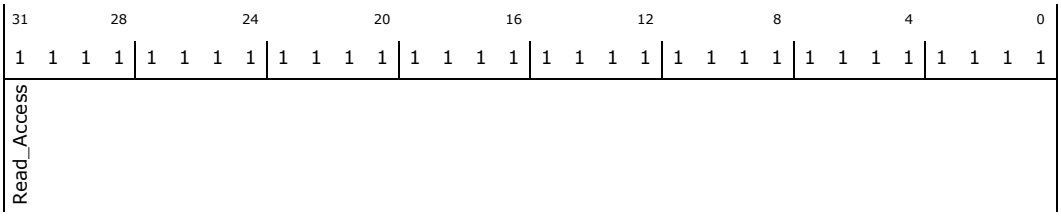
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 2Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.7.13 GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_2x3_8_1_regs)—Offset 30h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

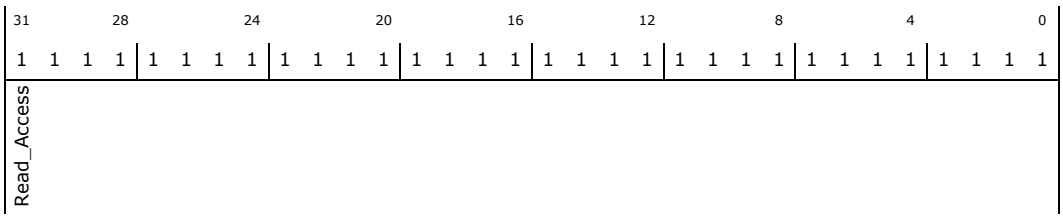
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 30h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.7.14 GPIO Read Access Control (gpio_read_access_policy_ulpmsmvfamily_2x3_8_0_regs)—Offset 34h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

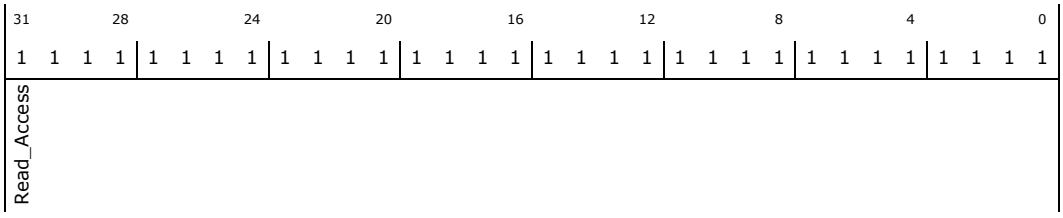
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 34h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.7.15 GPIO Write Access Control (gpio_write_access_policy_access_reg)—Offset 100h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

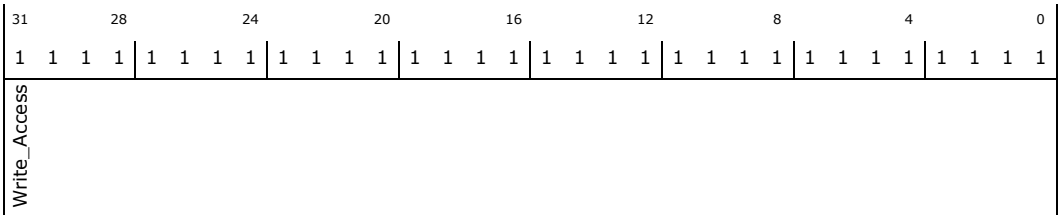
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 100h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.7.16 GPIO Write Access Control (gpio_write_access_policy_wake_reg)—Offset 104h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

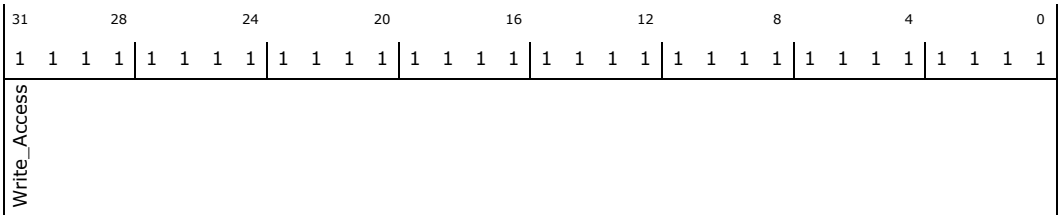
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 104h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.7.17 GPIO Write Access Control (gpio_write_access_policy_interrupt_reg)—Offset 108h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

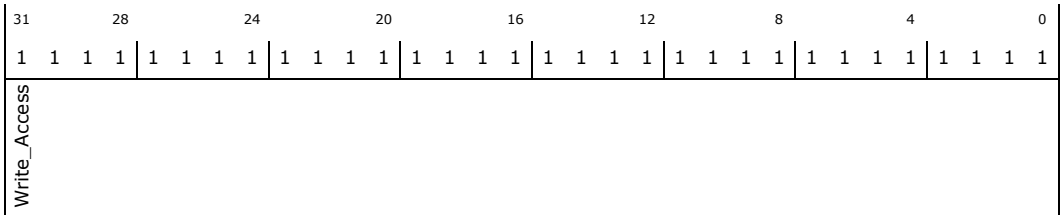
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 108h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.7.18 GPIO Write Access Control (gpio_write_access_policy_community_reg)—Offset 10Ch

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

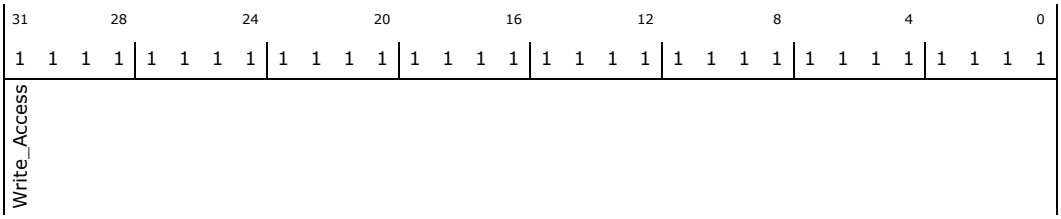
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 10Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.7.19 GPIO Write Access Control (gpio_write_access_policy_family_broadcast_reg)—Offset 110h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

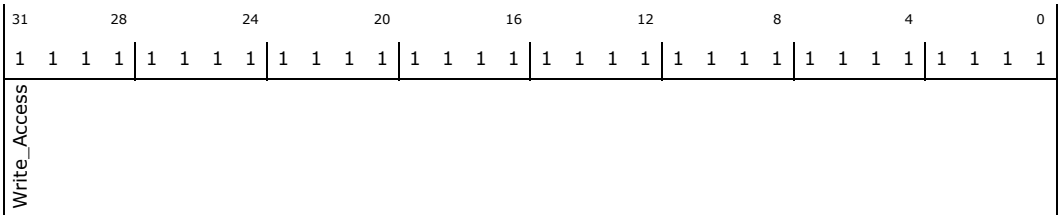
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 110h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.7.20 GPIO Write Access Control (gpio_write_access_policy_family_reg)—Offset 114h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

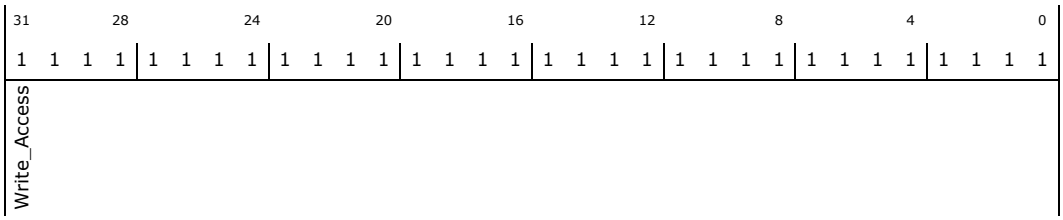
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 114h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.7.21 GPIO Write Access Control (gpio_write_access_policy_pad_broadcast_reg)—Offset 118h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

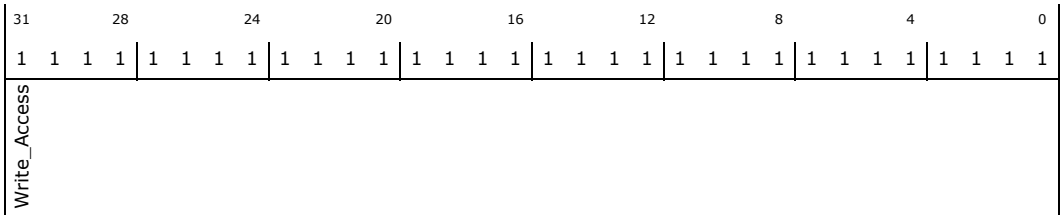
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 118h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.7.22 GPIO Write Access Control (gpio_write_access_policy_ulphsmvfamily_2x3_8_1_regs)—Offset 11Ch

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

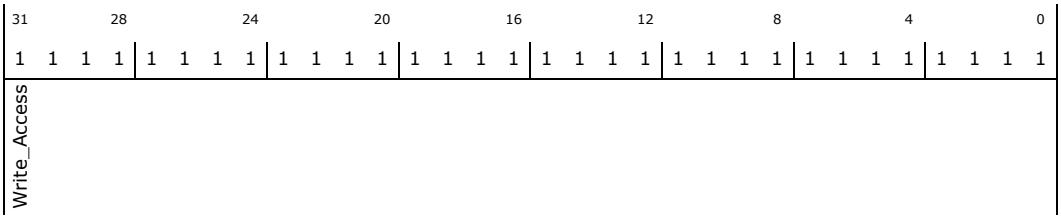
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 11Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.7.23 GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_2x3_8_6_regs)—Offset 120h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

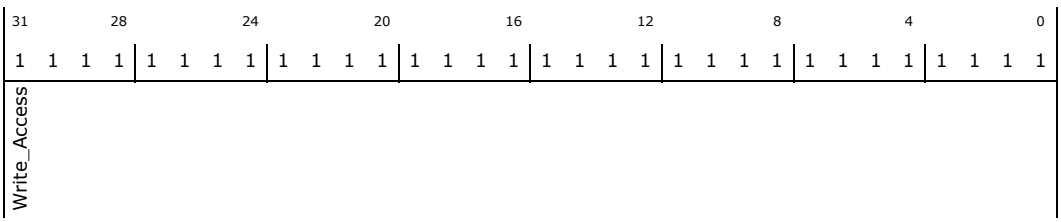
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 120h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.7.24 GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_2x3_8_5_regs)—Offset 124h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

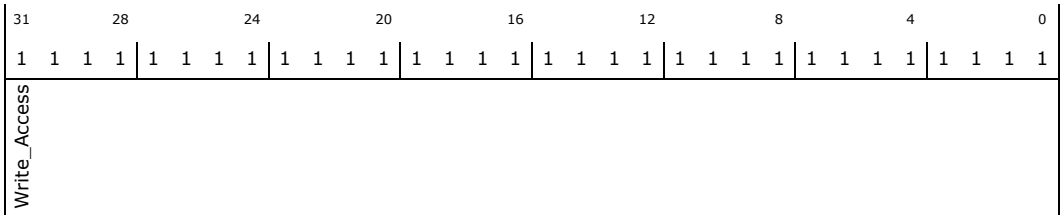
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 124h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.7.25 GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_2x3_8_4_regs)—Offset 128h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

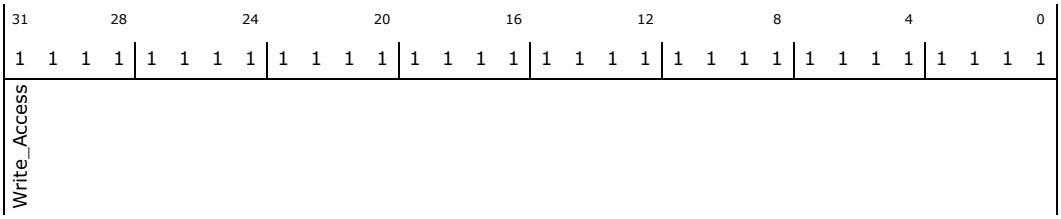
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 128h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.7.26 GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_2x3_8_3_regs)—Offset 12Ch

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

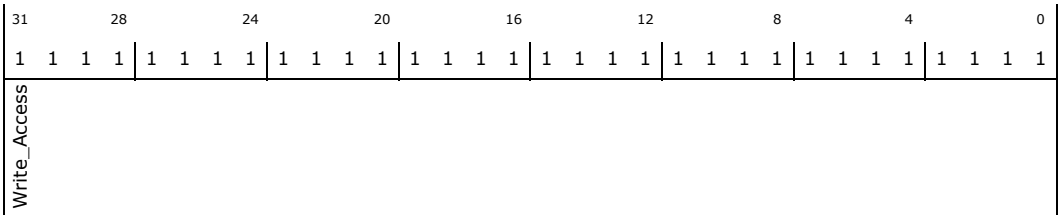
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 12Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.7.27 GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_2x3_8_1_regs)—Offset 130h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

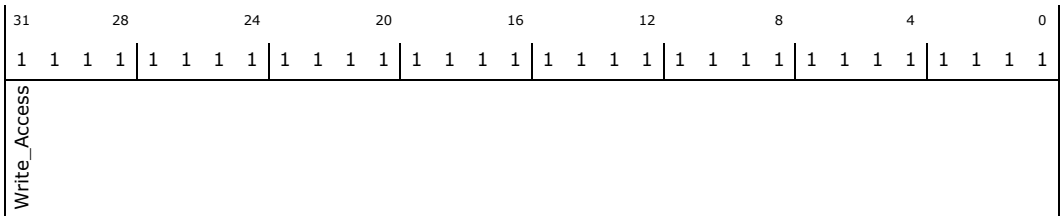
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 130h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.7.28 GPIO Write Access Control (gpio_write_access_policy_ulpmsmvfamily_2x3_8_0_regs)—Offset 134h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

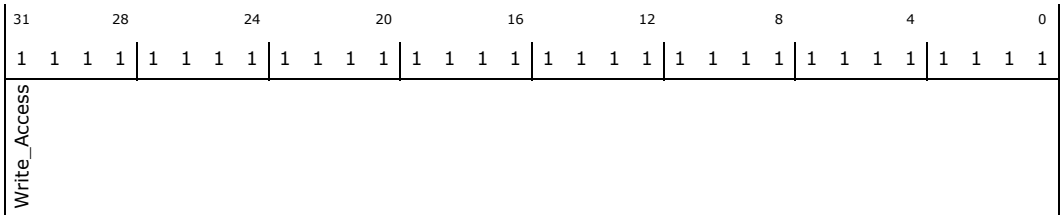
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 134h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.7.29 GPIO_WAKE_STATUS_REG #0 (gpio_wake_status_reg_0)—Offset 200h

GPIO Wake Status Register write 1 to clear.

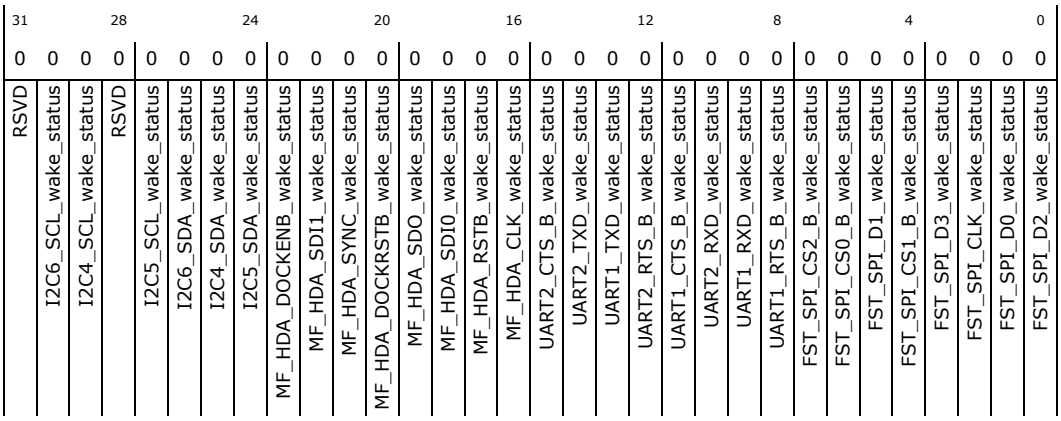
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 200h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1C	Reserved.
30	0x0 RW/1C	**I2C6_SCL_wake_status:** Reserved.
29	0x0 RW/1C	**I2C4_SCL_wake_status:** Reserved.
28	0x0 RW/1C	Reserved.
27	0x0 RW/1C	**I2C5_SCL_wake_status:** Reserved.
26	0x0 RW/1C	**I2C6_SDA_wake_status:** Reserved.
25	0x0 RW/1C	**I2C4_SDA_wake_status:** Reserved.
24	0x0 RW/1C	**I2C5_SDA_wake_status:** Reserved.
15	0x0 RW/1C	**UART2_CTS_B_wake_status:** Reserved.
14	0x0 RW/1C	**UART2_TXD_wake_status:** Reserved.
13	0x0 RW/1C	**UART1_TXD_wake_status:** Reserved.
12	0x0 RW/1C	**UART2_RTS_B_wake_status:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
11	0x0 RW/1C	**UART1_CTS_B_wake_status:** Reserved.
10	0x0 RW/1C	**UART2_RXD_wake_status:** Reserved.
9	0x0 RW/1C	**UART1_RXD_wake_status:** Reserved.
8	0x0 RW/1C	**UART1_RTS_B_wake_status:** Reserved.
7	0x0 RW/1C	**FST_SPI_CS2_B_wake_status:** Reserved.
6	0x0 RW/1C	**FST_SPI_CS0_B_wake_status:** Reserved.
5	0x0 RW/1C	**FST_SPI_D1_wake_status:** Reserved.
4	0x0 RW/1C	**FST_SPI_CS1_B_wake_status:** Reserved.
3	0x0 RW/1C	**FST_SPI_D3_wake_status:** Reserved.
2	0x0 RW/1C	**FST_SPI_CLK_wake_status:** Reserved.
1	0x0 RW/1C	**FST_SPI_D0_wake_status:** Reserved.
0	0x0 RW/1C	**FST_SPI_D2_wake_status:** Reserved.

10.7.30 GPIO_WAKE_STATUS_REG #1 (gpio_wake_status_reg_1)—Offset 204h

GPIO Wake Status Register write 1 to clear.

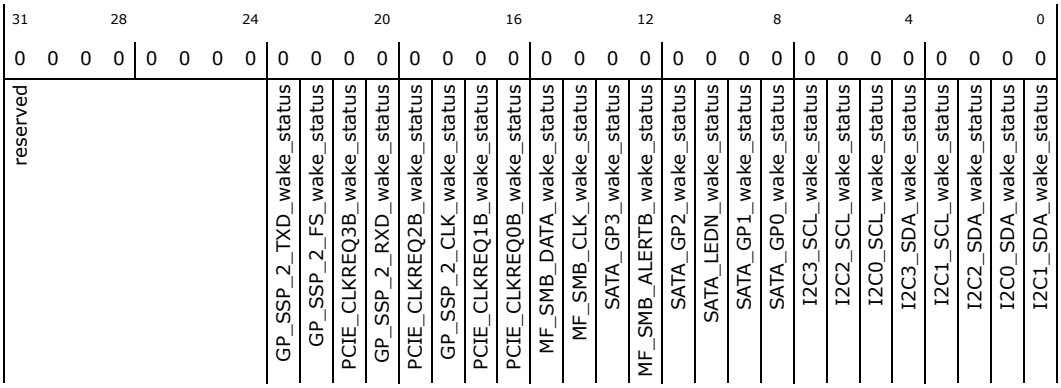
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 204h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RW/1C	**reserved:** Reserved.
23	0x0 RW/1C	**GP_SSP_2_TXD_wake_status:** Reserved.
22	0x0 RW/1C	**GP_SSP_2_FS_wake_status:** Reserved.
21	0x0 RW/1C	**PCIE_CLKREQ3B_wake_status:** Reserved.
20	0x0 RW/1C	**GP_SSP_2_RXD_wake_status:** Reserved.
19	0x0 RW/1C	**PCIE_CLKREQ2B_wake_status:** Reserved.
18	0x0 RW/1C	**GP_SSP_2_CLK_wake_status:** Reserved.
17	0x0 RW/1C	**PCIE_CLKREQ1B_wake_status:** Reserved.
16	0x0 RW/1C	**PCIE_CLKREQ0B_wake_status:** Reserved.
7	0x0 RW/1C	**I2C3_SCL_wake_status:** Reserved.
6	0x0 RW/1C	**I2C2_SCL_wake_status:** Reserved.
5	0x0 RW/1C	**I2C0_SCL_wake_status:** Reserved.
4	0x0 RW/1C	**I2C3_SDA_wake_status:** Reserved.
3	0x0 RW/1C	**I2C1_SCL_wake_status:** Reserved.
2	0x0 RW/1C	**I2C2_SDA_wake_status:** Reserved.
1	0x0 RW/1C	**I2C0_SDA_wake_status:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
0	0x0 RW/1C	**I2C1_SDA_wake_status:** Reserved.

10.7.31 GPIO_WAKE_MASK_REG #0 (gpio_wake_mask_reg_0)—Offset 280h

GPIO Wake Register 0 Masks Wake.

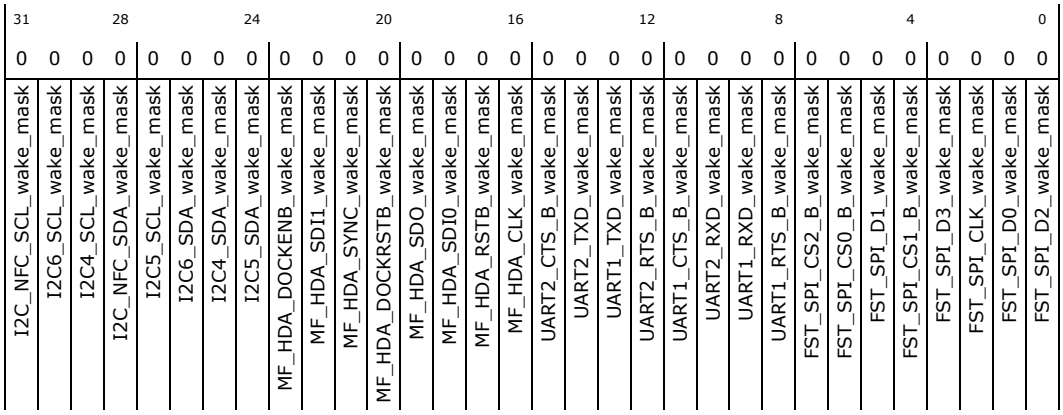
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 280h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**I2C_NFC_SCL_wake_mask:** Reserved.
30	0x0 RW	**I2C6_SCL_wake_mask:** Reserved.
29	0x0 RW	**I2C4_SCL_wake_mask:** Reserved.
28	0x0 RW	**I2C_NFC_SDA_wake_mask:** Reserved.
27	0x0 RW	**I2C5_SCL_wake_mask:** Reserved.
26	0x0 RW	**I2C6_SDA_wake_mask:** Reserved.
25	0x0 RW	**I2C4_SDA_wake_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
24	0x0 RW	**I2C5_SDA_wake_mask:** Reserved.
15	0x0 RW	**UART2_CTS_B_wake_mask:** Reserved.
14	0x0 RW	**UART2_TXD_wake_mask:** Reserved.
13	0x0 RW	**UART1_TXD_wake_mask:** Reserved.
12	0x0 RW	**UART2_RTS_B_wake_mask:** Reserved.
11	0x0 RW	**UART1_CTS_B_wake_mask:** Reserved.
10	0x0 RW	**UART2_RXD_wake_mask:** Reserved.
9	0x0 RW	**UART1_RXD_wake_mask:** Reserved.
8	0x0 RW	**UART1_RTS_B_wake_mask:** Reserved.
7	0x0 RW	**FST_SPI_CS2_B_wake_mask:** Reserved.
6	0x0 RW	**FST_SPI_CS0_B_wake_mask:** Reserved.
5	0x0 RW	**FST_SPI_D1_wake_mask:** Reserved.
4	0x0 RW	**FST_SPI_CS1_B_wake_mask:** Reserved.
3	0x0 RW	**FST_SPI_D3_wake_mask:** Reserved.
2	0x0 RW	**FST_SPI_CLK_wake_mask:** Reserved.
1	0x0 RW	**FST_SPI_D0_wake_mask:** Reserved.
0	0x0 RW	**FST_SPI_D2_wake_mask:** Reserved.

10.7.32 GPIO_WAKE_MASK_REG #1 (gpio_wake_mask_reg_1)—Offset 284h

GPIO Wake Register 0 Masks Wake.

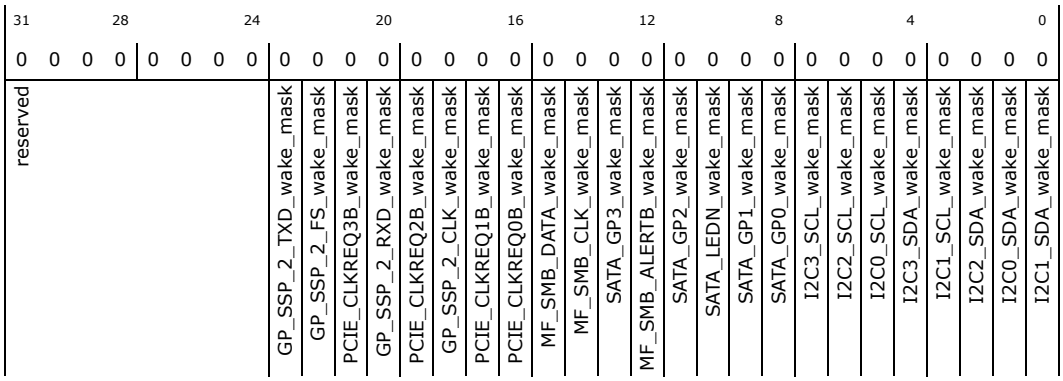
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 284h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RW	**reserved:** Reserved.
23	0x0 RW	**GP_SSP_2_TXD_wake_mask:** Reserved.
22	0x0 RW	**GP_SSP_2_FS_wake_mask:** Reserved.
21	0x0 RW	**PCIE_CLKREQ3B_wake_mask:** Reserved.
20	0x0 RW	**GP_SSP_2_RXD_wake_mask:** Reserved.
19	0x0 RW	**PCIE_CLKREQ2B_wake_mask:** Reserved.
18	0x0 RW	**GP_SSP_2_CLK_wake_mask:** Reserved.
17	0x0 RW	**PCIE_CLKREQ1B_wake_mask:** Reserved.
16	0x0 RW	**PCIE_CLKREQ0B_wake_mask:** Reserved.
7	0x0 RW	**I2C3_SCL_wake_mask:** Reserved.
6	0x0 RW	**I2C2_SCL_wake_mask:** Reserved.
5	0x0 RW	**I2C0_SCL_wake_mask:** Reserved.
4	0x0 RW	**I2C3_SDA_wake_mask:** Reserved.
3	0x0 RW	**I2C1_SCL_wake_mask:** Reserved.
2	0x0 RW	**I2C2_SDA_wake_mask:** Reserved.
1	0x0 RW	**I2C0_SDA_wake_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
0	0x0 RW	**I2C1_SDA_wake_mask:** Reserved.

10.7.33 GPIO Interrupt Status (gpio_interrupt_status)—Offset 300h

Status bits for the 16 interrupts.

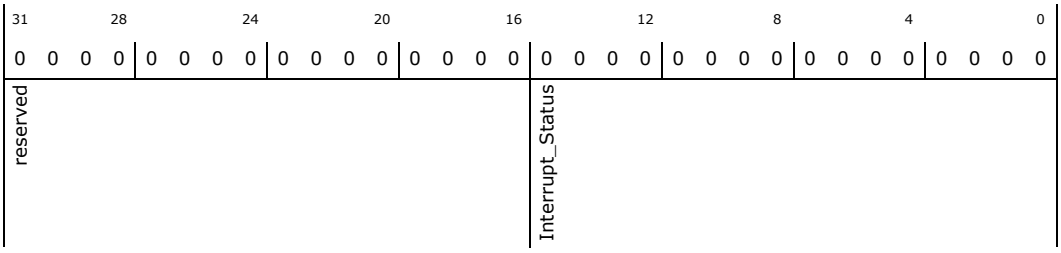
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 300h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW/1C	**reserved:** reserved
15:0	0x0 RW/1C	**Interrupt Status (Interrupt_Status):** Status bits for the 16 interrupts. Write 1 to Clear

10.7.34 GPIO Interrupt Status (gpio_interrupt_mask)—Offset 380h

Mask bits for the 16 interrupts.

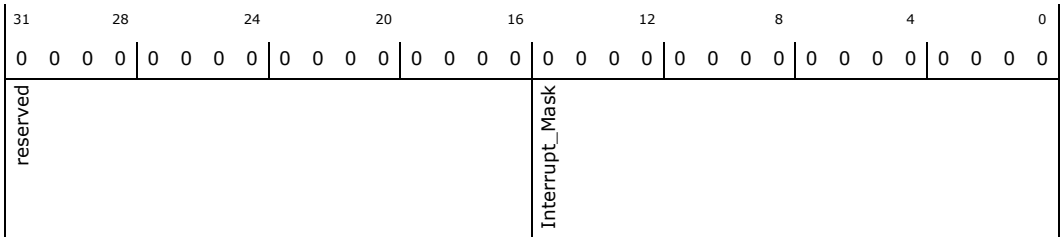
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 380h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**reserved:** reserved
15:0	0x0 RW	**Interrupt Mask (Interrupt_Mask):** Mask bits for the 16 interrupts. Interrupt masked when 0.

10.7.35 GPIO Broadcast Data Mask bit Register (gpio_family_bw_mask_31_0)—Offset 1000h

Write Mask that masks bit by bit the data written to BWData

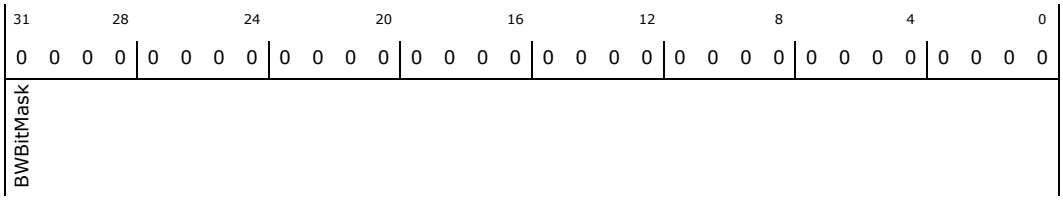
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 1000h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**BWBitMask:** Reserved.

10.7.36 GPIO Broadcast Data Register (gpio_family_bw_data_31_0)—Offset 1004h

Broadcast Write Data

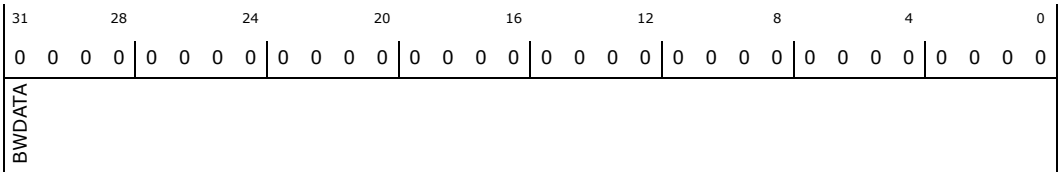
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 1004h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 WO	**BWDATA:** Reserved.

10.7.37 gpio_family_broadcast_reg_mask #0 (gpio_family_broadcast_reg_mask_0)—Offset 1008h

Family Broadcast Register Masking

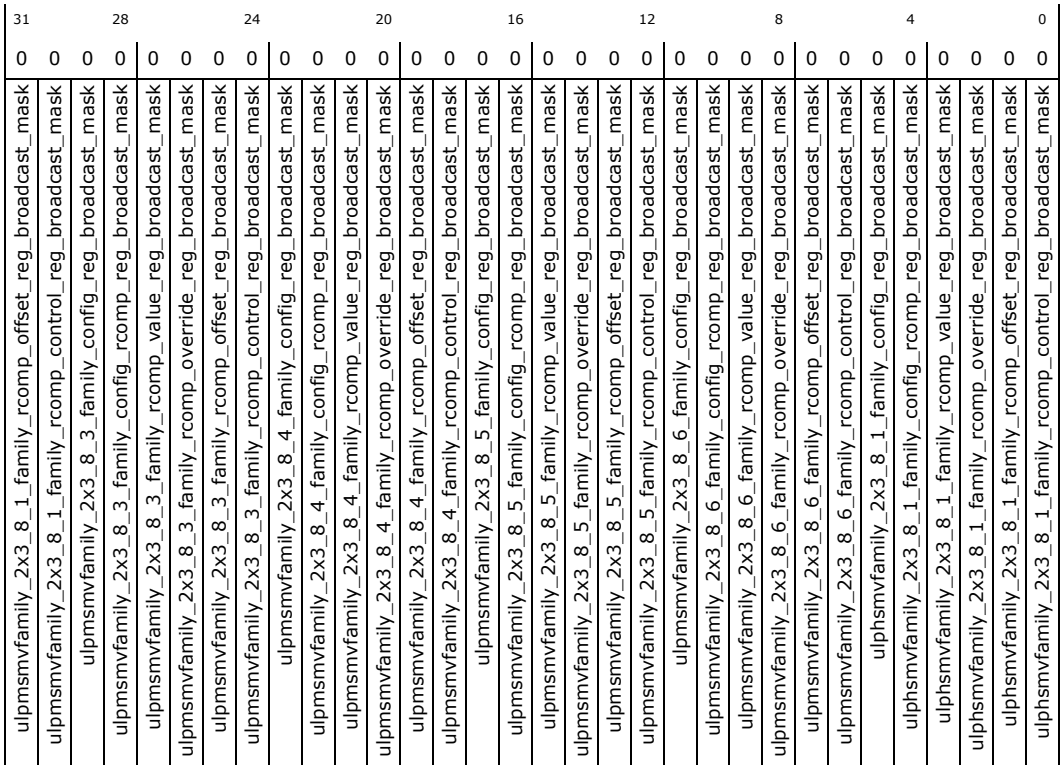
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 1008h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**ulpmsmvfamily_2x3_8_1_family_rcomp_offset_reg_broadcast_mask:** Reserved.
30	0x0 RW	**ulpmsmvfamily_2x3_8_1_family_rcomp_control_reg_broadcast_mask:** Reserved.
29	0x0 RW	**ulpmsmvfamily_2x3_8_3_family_config_reg_broadcast_mask:** Reserved.
28	0x0 RW	**ulpmsmvfamily_2x3_8_3_family_config_rcomp_reg_broadcast_mask:** Reserved.
27	0x0 RW	**ulpmsmvfamily_2x3_8_3_family_rcomp_value_reg_broadcast_mask:** Reserved.
26	0x0 RW	**ulpmsmvfamily_2x3_8_3_family_rcomp_override_reg_broadcast_mask:** Reserved.
25	0x0 RW	**ulpmsmvfamily_2x3_8_3_family_rcomp_offset_reg_broadcast_mask:** Reserved.
24	0x0 RW	**ulpmsmvfamily_2x3_8_3_family_rcomp_control_reg_broadcast_mask:** Reserved.
23	0x0 RW	**ulpmsmvfamily_2x3_8_4_family_config_reg_broadcast_mask:** Reserved.
22	0x0 RW	**ulpmsmvfamily_2x3_8_4_family_config_rcomp_reg_broadcast_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
21	0x0 RW	**ulpmsmvfamily_2x3_8_4_family_rcomp_value_reg_broadcast_mask:** Reserved.
20	0x0 RW	**ulpmsmvfamily_2x3_8_4_family_rcomp_override_reg_broadcast_mask:** Reserved.
19	0x0 RW	**ulpmsmvfamily_2x3_8_4_family_rcomp_offset_reg_broadcast_mask:** Reserved.
18	0x0 RW	**ulpmsmvfamily_2x3_8_4_family_rcomp_control_reg_broadcast_mask:** Reserved.
17	0x0 RW	**ulpmsmvfamily_2x3_8_5_family_config_reg_broadcast_mask:** Reserved.
16	0x0 RW	**ulpmsmvfamily_2x3_8_5_family_config_rcomp_reg_broadcast_mask:** Reserved.
15	0x0 RW	**ulpmsmvfamily_2x3_8_5_family_rcomp_value_reg_broadcast_mask:** Reserved.
14	0x0 RW	**ulpmsmvfamily_2x3_8_5_family_rcomp_override_reg_broadcast_mask:** Reserved.
13	0x0 RW	**ulpmsmvfamily_2x3_8_5_family_rcomp_offset_reg_broadcast_mask:** Reserved.
12	0x0 RW	**ulpmsmvfamily_2x3_8_5_family_rcomp_control_reg_broadcast_mask:** Reserved.
11	0x0 RW	**ulpmsmvfamily_2x3_8_6_family_config_reg_broadcast_mask:** Reserved.
10	0x0 RW	**ulpmsmvfamily_2x3_8_6_family_config_rcomp_reg_broadcast_mask:** Reserved.
9	0x0 RW	**ulpmsmvfamily_2x3_8_6_family_rcomp_value_reg_broadcast_mask:** Reserved.
8	0x0 RW	**ulpmsmvfamily_2x3_8_6_family_rcomp_override_reg_broadcast_mask:** Reserved.
7	0x0 RW	**ulpmsmvfamily_2x3_8_6_family_rcomp_offset_reg_broadcast_mask:** Reserved.
6	0x0 RW	**ulpmsmvfamily_2x3_8_6_family_rcomp_control_reg_broadcast_mask:** Reserved.
5	0x0 RW	**ulphsmvfamily_2x3_8_1_family_config_reg_broadcast_mask:** Reserved.
4	0x0 RW	**ulphsmvfamily_2x3_8_1_family_config_rcomp_reg_broadcast_mask:** Reserved.
3	0x0 RW	**ulphsmvfamily_2x3_8_1_family_rcomp_value_reg_broadcast_mask:** Reserved.
2	0x0 RW	**ulphsmvfamily_2x3_8_1_family_rcomp_override_reg_broadcast_mask:** Reserved.
1	0x0 RW	**ulphsmvfamily_2x3_8_1_family_rcomp_offset_reg_broadcast_mask:** Reserved.
0	0x0 RW	**ulphsmvfamily_2x3_8_1_family_rcomp_control_reg_broadcast_mask:** Reserved.

10.7.38 gpio_family_broadcast_reg_mask #1 (gpio_family_broadcast_reg_mask_1)—Offset 100Ch

Family Broadcast Register Masking

Access Method

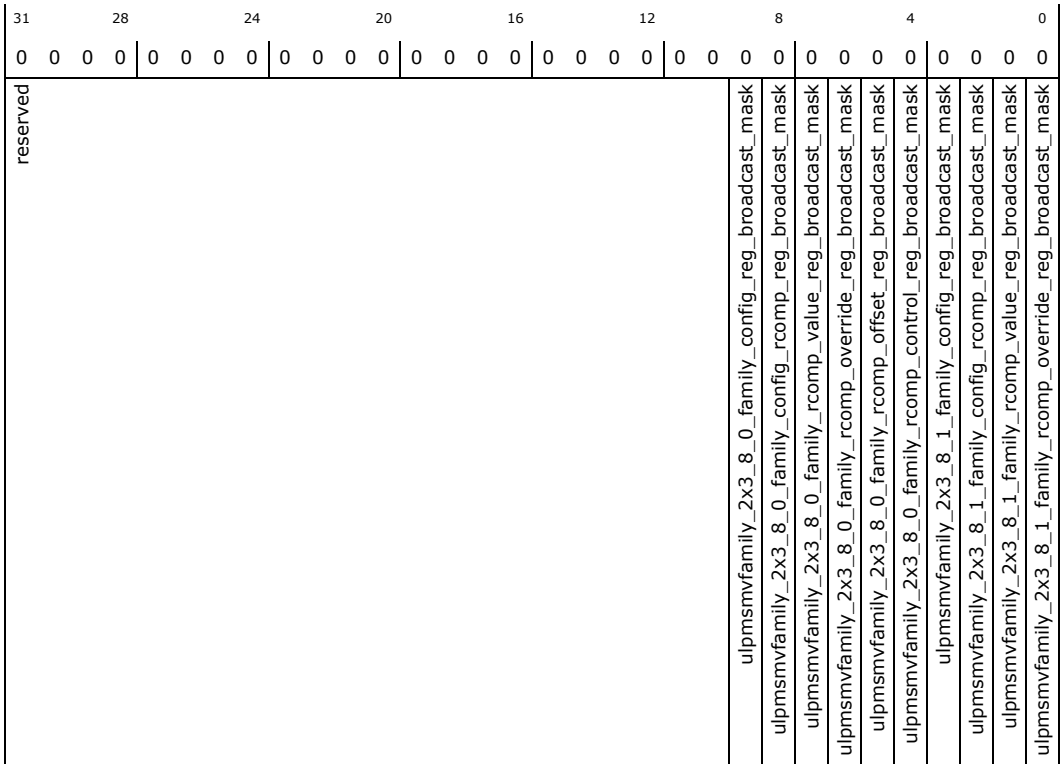
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 100Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:10	0x0 RW	**reserved:** Reserved.
9	0x0 RW	**ulpmsmvfamily_2x3_8_0_family_config_reg_broadcast_mask:** Reserved.
8	0x0 RW	**ulpmsmvfamily_2x3_8_0_family_config_rcomp_reg_broadcast_mask:** Reserved.
7	0x0 RW	**ulpmsmvfamily_2x3_8_0_family_rcomp_value_reg_broadcast_mask:** Reserved.
6	0x0 RW	**ulpmsmvfamily_2x3_8_0_family_rcomp_override_reg_broadcast_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
5	0x0 RW	**ulpmsmvfamily_2x3_8_0_family_rcomp_offset_reg_broadcast_mask:** Reserved.
4	0x0 RW	**ulpmsmvfamily_2x3_8_0_family_rcomp_control_reg_broadcast_mask:** Reserved.
3	0x0 RW	**ulpmsmvfamily_2x3_8_1_family_config_reg_broadcast_mask:** Reserved.
2	0x0 RW	**ulpmsmvfamily_2x3_8_1_family_config_rcomp_reg_broadcast_mask:** Reserved.
1	0x0 RW	**ulpmsmvfamily_2x3_8_1_family_rcomp_value_reg_broadcast_mask:** Reserved.
0	0x0 RW	**ulpmsmvfamily_2x3_8_1_family_rcomp_override_reg_broadcast_mask:** Reserved.

10.7.39 family_config_rcomp_reg (ulphsmvfamily_2x3_8_1_family_config_rcomp_reg)—Offset 1090h

GPIO Family RCOMP Register

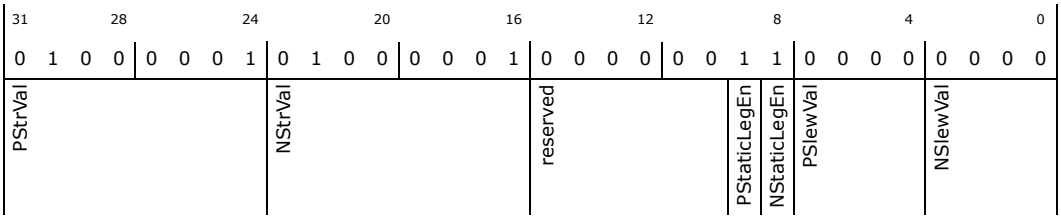
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 1090h

Op Codes:
h - Read, h - Write

Default: 41410300h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x41 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x41 RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable

Bit Range	Default and Access	Field Name (ID): Description
7:4	0x0 RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.
3:0	0x0 RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.7.40 gpio_family_configuration_register (ulphsmvfamily_2x3_8_1_family_config_reg)—Offset 1094h

GPIO Family CFIO Configuration Register

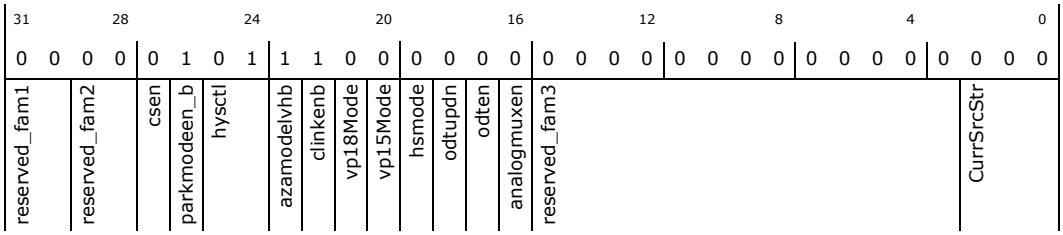
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 1094h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x1 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.

Bit Range	Default and Access	Field Name (ID): Description
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.7.41 family_config_rcomp_reg (ulpmsmvfamily_2x3_8_6_family_config_rcomp_reg)—Offset 1110h

GPIO Family RCOMP Register

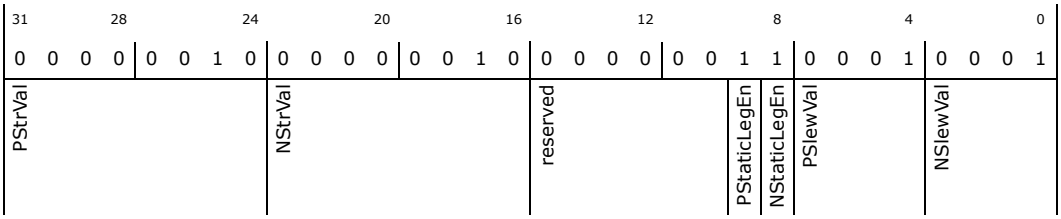
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 1110h

Op Codes:
h - Read, h - Write

Default: 02020311h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x2 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x2 RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable

Bit Range	Default and Access	Field Name (ID): Description
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable
7:4	0x1 RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.
3:0	0x1 RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.7.42 gpio_family_configuration_register (ulpmsmvfamily_2x3_8_6_family_config_reg)—Offset 1114h

GPIO Family CFIO Configuration Register

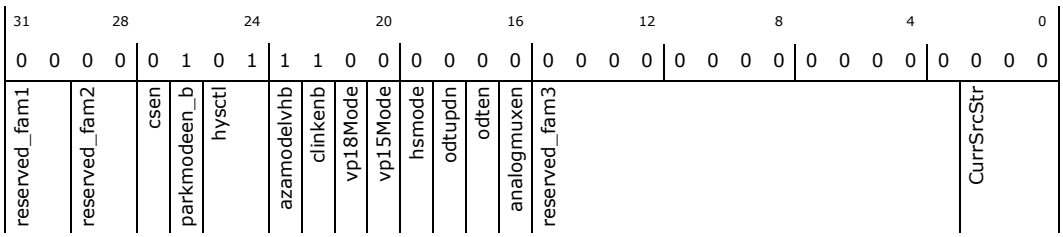
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 1114h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x1 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC

Bit Range	Default and Access	Field Name (ID): Description
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.7.43 family_config_rcomp_reg (ulpmsmvfamily_2x3_8_5_family_config_rcomp_reg)—Offset 1190h

GPIO Family RCOMP Register

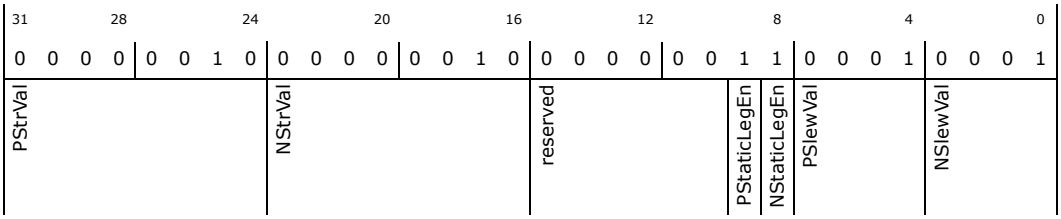
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 1190h

Op Codes:
h - Read, h - Write

Default: 02020311h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x2 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x2 RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.

Bit Range	Default and Access	Field Name (ID): Description
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable
7:4	0x1 RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.
3:0	0x1 RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.7.44 gpio_family_configuration_register (ulpmsmvfamily_2x3_8_5_family_config_reg)—Offset 1194h

GPIO Family CFIO Configuration Register

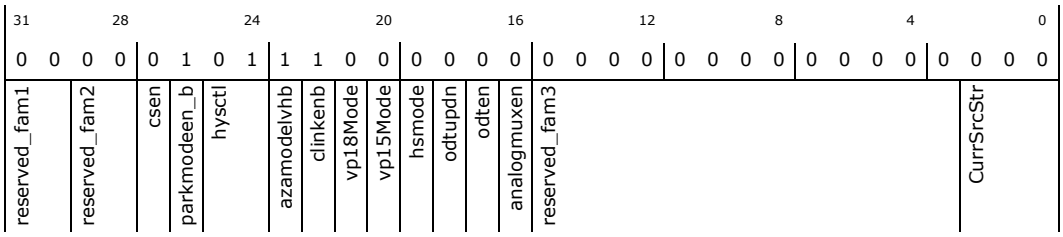
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 1194h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x1 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.

Bit Range	Default and Access	Field Name (ID): Description
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.7.45 family_config_rcomp_reg (ulpmsmvfamily_2x3_8_4_family_config_rcomp_reg)—Offset 1210h

GPIO Family RCOMP Register

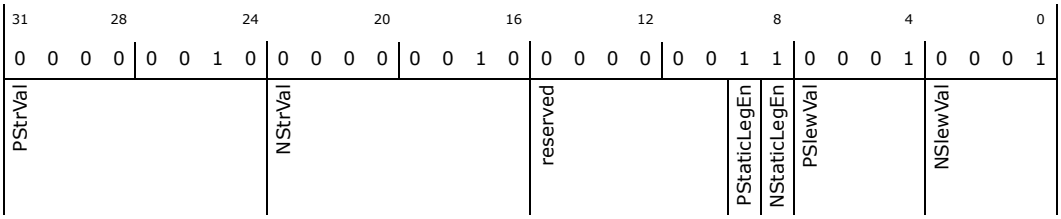
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 1210h

Op Codes:
h - Read, h - Write

Default: 02020311h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x2 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x2 RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable
7:4	0x1 RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.
3:0	0x1 RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.7.46 gpio_family_configuration_register (ulpmsmvfamily_2x3_8_4_family_config_reg)—Offset 1214h

GPIO Family CFIO Configuration Register

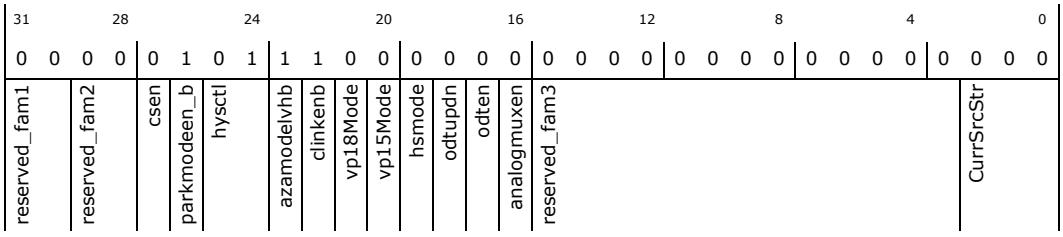
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 1214h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers

Bit Range	Default and Access	Field Name (ID): Description
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x1 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.7.47 family_config_rcomp_reg (ulpmsmvfamily_2x3_8_3_family_config_rcomp_reg)—Offset 1290h

GPIO Family RCOMP Register

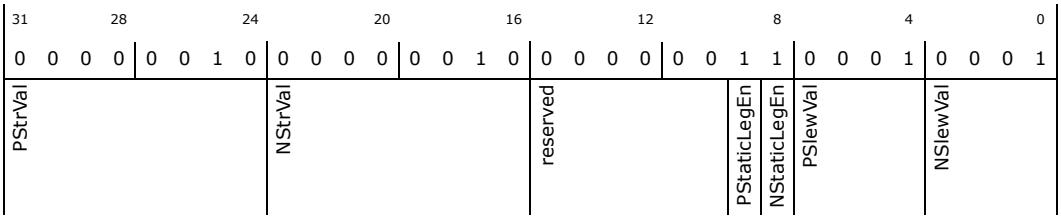
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 1290h

Op Codes:
h - Read, h - Write

Default: 02020311h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x2 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x2 RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable
7:4	0x1 RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.
3:0	0x1 RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.7.48 gpio_family_configuration_register (ulpmsmvfamily_2x3_8_3_family_config_reg)—Offset 1294h

GPIO Family CFIO Configuration Register

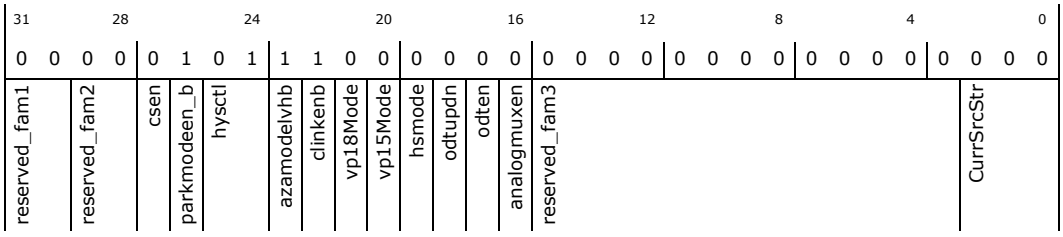
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 1294h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers

Bit Range	Default and Access	Field Name (ID): Description
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x1 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.7.49 family_config_rcomp_reg (ulpmsmvfamily_2x3_8_1_family_config_rcomp_reg)—Offset 1310h

GPIO Family RCOMP Register

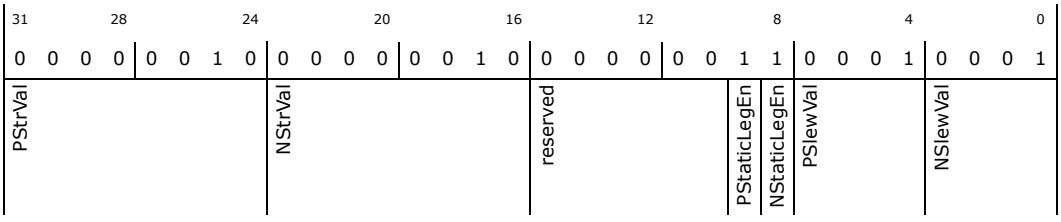
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 1310h

Op Codes:
h - Read, h - Write

Default: 02020311h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x2 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x2 RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable
7:4	0x1 RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.
3:0	0x1 RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.7.50 gpio_family_configuration_register (ulpmsmvfamily_2x3_8_1_family_config_reg)—Offset 1314h

GPIO Family CFIO Configuration Register

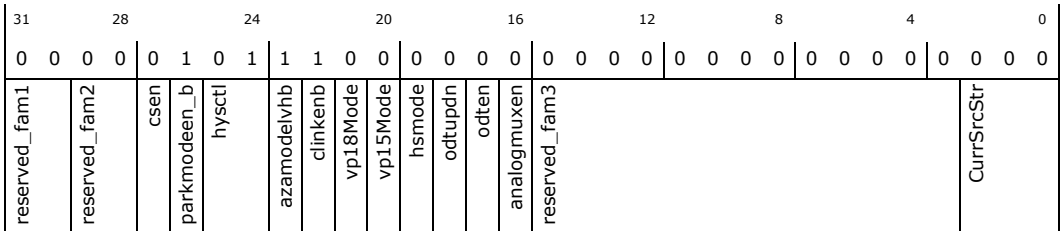
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 1314h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers

Bit Range	Default and Access	Field Name (ID): Description
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x1 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.7.51 family_config_rcomp_reg (ulpmsmvfamily_2x3_8_0_family_config_rcomp_reg)—Offset 1390h

GPIO Family RCOMP Register

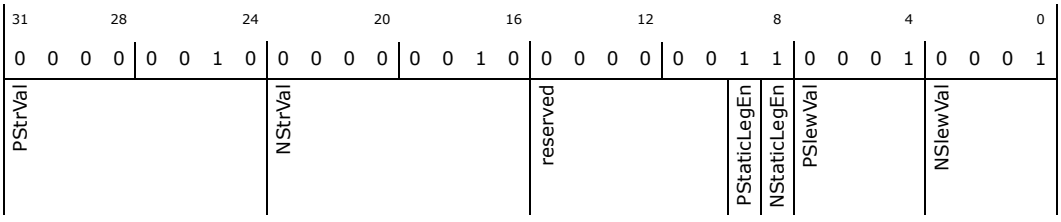
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 1390h

Op Codes:
h - Read, h - Write

Default: 02020311h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x2 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x2 RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable
7:4	0x1 RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.
3:0	0x1 RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.7.52 gpio_family_configuration_register (ulpmsmvfamily_2x3_8_0_family_config_reg)—Offset 1394h

GPIO Family CFIO Configuration Register

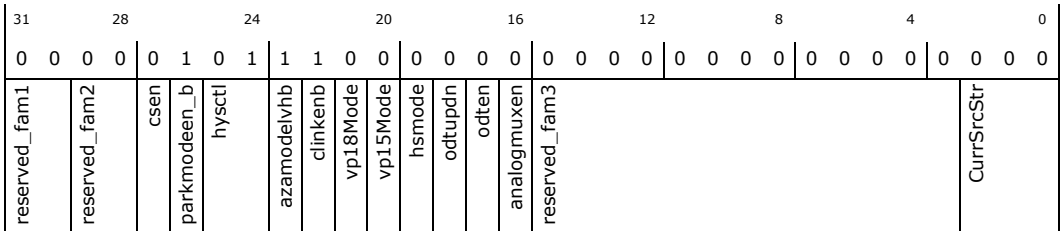
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 1394h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers

Bit Range	Default and Access	Field Name (ID): Description
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x1 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.7.53 GPIO Broadcast Data Mask bit Register (gpio_pad_bw_mask_31_0)—Offset 4000h

Write Mask that masks bit by bit the data written to BWData

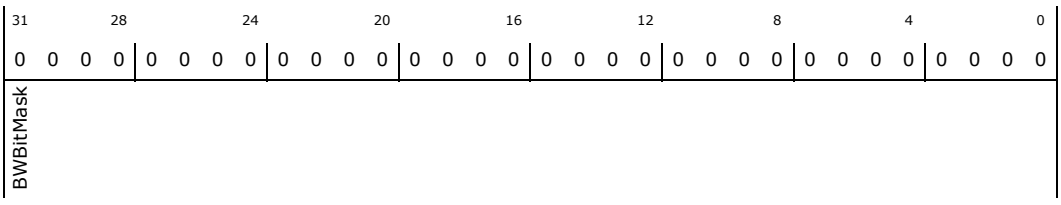
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4000h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**BWBitMask:** Reserved.

10.7.54 GPIO Broadcast Data Register (gpio_pad_bw_data_31_0)—Offset 4004h

Broadcast Write Data

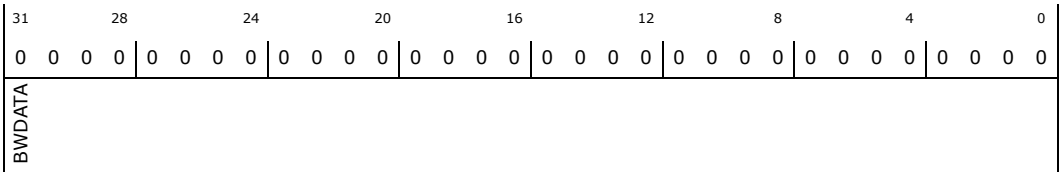
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4004h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 WO	**BWDATA:** Reserved.

10.7.55 gpio_pad_broadcast_reg_mask #0 (gpio_pad_broadcast_reg_mask_0)—Offset 4008h

Pad Broadcast Register Masking

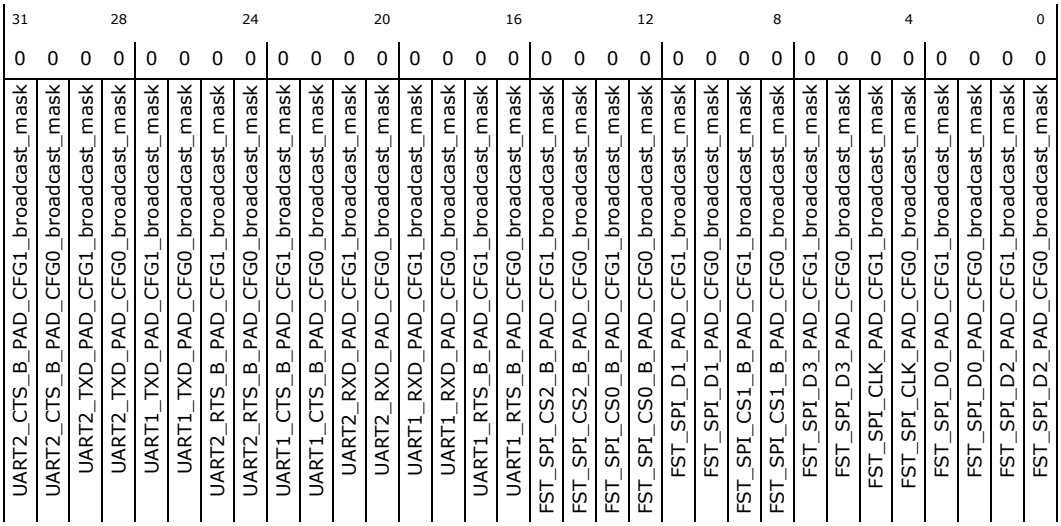
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4008h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**UART2_CTS_B_PAD_CFG1_broadcast_mask:** Reserved.
30	0x0 RW	**UART2_CTS_B_PAD_CFG0_broadcast_mask:** Reserved.
29	0x0 RW	**UART2_TXD_PAD_CFG1_broadcast_mask:** Reserved.
28	0x0 RW	**UART2_TXD_PAD_CFG0_broadcast_mask:** Reserved.
27	0x0 RW	**UART1_TXD_PAD_CFG1_broadcast_mask:** Reserved.
26	0x0 RW	**UART1_TXD_PAD_CFG0_broadcast_mask:** Reserved.
25	0x0 RW	**UART2_RTS_B_PAD_CFG1_broadcast_mask:** Reserved.
24	0x0 RW	**UART2_RTS_B_PAD_CFG0_broadcast_mask:** Reserved.
23	0x0 RW	**UART1_CTS_B_PAD_CFG1_broadcast_mask:** Reserved.
22	0x0 RW	**UART1_CTS_B_PAD_CFG0_broadcast_mask:** Reserved.
21	0x0 RW	**UART2_RXD_PAD_CFG1_broadcast_mask:** Reserved.
20	0x0 RW	**UART2_RXD_PAD_CFG0_broadcast_mask:** Reserved.
19	0x0 RW	**UART1_RXD_PAD_CFG1_broadcast_mask:** Reserved.
18	0x0 RW	**UART1_RXD_PAD_CFG0_broadcast_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
17	0x0 RW	**UART1_RTS_B_PAD_CFG1_broadcast_mask:** Reserved.
16	0x0 RW	**UART1_RTS_B_PAD_CFG0_broadcast_mask:** Reserved.
15	0x0 RW	**FST_SPI_CS2_B_PAD_CFG1_broadcast_mask:** Reserved.
14	0x0 RW	**FST_SPI_CS2_B_PAD_CFG0_broadcast_mask:** Reserved.
13	0x0 RW	**FST_SPI_CS0_B_PAD_CFG1_broadcast_mask:** Reserved.
12	0x0 RW	**FST_SPI_CS0_B_PAD_CFG0_broadcast_mask:** Reserved.
11	0x0 RW	**FST_SPI_D1_PAD_CFG1_broadcast_mask:** Reserved.
10	0x0 RW	**FST_SPI_D1_PAD_CFG0_broadcast_mask:** Reserved.
9	0x0 RW	**FST_SPI_CS1_B_PAD_CFG1_broadcast_mask:** Reserved.
8	0x0 RW	**FST_SPI_CS1_B_PAD_CFG0_broadcast_mask:** Reserved.
7	0x0 RW	**FST_SPI_D3_PAD_CFG1_broadcast_mask:** Reserved.
6	0x0 RW	**FST_SPI_D3_PAD_CFG0_broadcast_mask:** Reserved.
5	0x0 RW	**FST_SPI_CLK_PAD_CFG1_broadcast_mask:** Reserved.
4	0x0 RW	**FST_SPI_CLK_PAD_CFG0_broadcast_mask:** Reserved.
3	0x0 RW	**FST_SPI_D0_PAD_CFG1_broadcast_mask:** Reserved.
2	0x0 RW	**FST_SPI_D0_PAD_CFG0_broadcast_mask:** Reserved.
1	0x0 RW	**FST_SPI_D2_PAD_CFG1_broadcast_mask:** Reserved.
0	0x0 RW	**FST_SPI_D2_PAD_CFG0_broadcast_mask:** Reserved.

10.7.56 gpio_pad_broadcast_reg_mask #1 (gpio_pad_broadcast_reg_mask_1)—Offset 400Ch

Pad Broadcast Register Masking

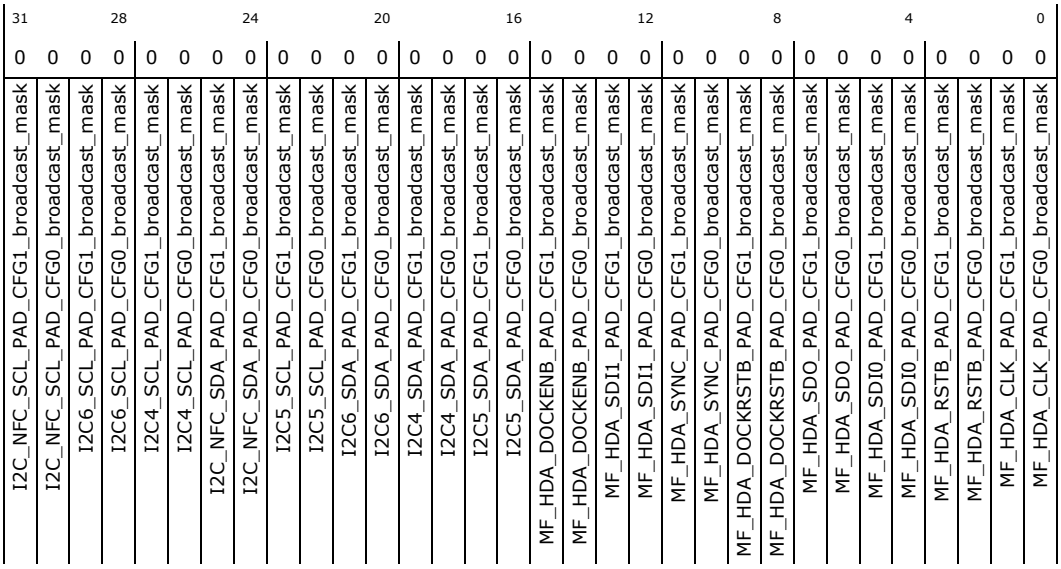
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 400Ch

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**I2C_NFC_SCL_PAD_CFG1_broadcast_mask:** Reserved.
30	0x0 RW	**I2C_NFC_SCL_PAD_CFG0_broadcast_mask:** Reserved.
29	0x0 RW	**I2C6_SCL_PAD_CFG1_broadcast_mask:** Reserved.
28	0x0 RW	**I2C6_SCL_PAD_CFG0_broadcast_mask:** Reserved.
27	0x0 RW	**I2C4_SCL_PAD_CFG1_broadcast_mask:** Reserved.
26	0x0 RW	**I2C4_SCL_PAD_CFG0_broadcast_mask:** Reserved.
25	0x0 RW	**I2C_NFC_SDA_PAD_CFG1_broadcast_mask:** Reserved.
24	0x0 RW	**I2C_NFC_SDA_PAD_CFG0_broadcast_mask:** Reserved.
23	0x0 RW	**I2C5_SCL_PAD_CFG1_broadcast_mask:** Reserved.
22	0x0 RW	**I2C5_SCL_PAD_CFG0_broadcast_mask:** Reserved.
21	0x0 RW	**I2C6_SDA_PAD_CFG1_broadcast_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
20	0x0 RW	**I2C6_SDA_PAD_CFG0_broadcast_mask:** Reserved.
19	0x0 RW	**I2C4_SDA_PAD_CFG1_broadcast_mask:** Reserved.
18	0x0 RW	**I2C4_SDA_PAD_CFG0_broadcast_mask:** Reserved.
17	0x0 RW	**I2C5_SDA_PAD_CFG1_broadcast_mask:** Reserved.
16	0x0 RW	**I2C5_SDA_PAD_CFG0_broadcast_mask:** Reserved.

10.7.57 gpio_pad_broadcast_reg_mask #2 (gpio_pad_broadcast_reg_mask_2)—Offset 4010h

Pad Broadcast Register Masking

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4010h

Op Codes:

h - Read, h - Write

Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MF_SMB_DATA_PAD_CFG1_broadcast_mask	MF_SMB_DATA_PAD_CFG0_broadcast_mask	MF_SMB_CLK_PAD_CFG1_broadcast_mask	MF_SMB_CLK_PAD_CFG0_broadcast_mask	SATA_GP3_PAD_CFG1_broadcast_mask	SATA_GP3_PAD_CFG0_broadcast_mask	MF_SMB_ALERTB_PAD_CFG1_broadcast_mask	MF_SMB_ALERTB_PAD_CFG0_broadcast_mask	SATA_GP2_PAD_CFG1_broadcast_mask	SATA_GP2_PAD_CFG0_broadcast_mask	SATA_LEDN_PAD_CFG1_broadcast_mask	SATA_LEDN_PAD_CFG0_broadcast_mask	SATA_GP1_PAD_CFG1_broadcast_mask	SATA_GP1_PAD_CFG0_broadcast_mask	SATA_GP0_PAD_CFG1_broadcast_mask	SATA_GP0_PAD_CFG0_broadcast_mask	I2C3_SCL_PAD_CFG1_broadcast_mask	I2C3_SCL_PAD_CFG0_broadcast_mask	I2C2_SCL_PAD_CFG1_broadcast_mask	I2C2_SCL_PAD_CFG0_broadcast_mask	I2C0_SCL_PAD_CFG1_broadcast_mask	I2C0_SCL_PAD_CFG0_broadcast_mask	I2C3_SDA_PAD_CFG1_broadcast_mask	I2C3_SDA_PAD_CFG0_broadcast_mask	I2C1_SCL_PAD_CFG1_broadcast_mask	I2C1_SCL_PAD_CFG0_broadcast_mask	I2C2_SDA_PAD_CFG1_broadcast_mask	I2C2_SDA_PAD_CFG0_broadcast_mask	I2C0_SDA_PAD_CFG1_broadcast_mask	I2C0_SDA_PAD_CFG0_broadcast_mask	I2C1_SDA_PAD_CFG1_broadcast_mask	I2C1_SDA_PAD_CFG0_broadcast_mask

Bit Range	Default and Access	Field Name (ID): Description
15	0x0 RW	**I2C3_SCL_PAD_CFG1_broadcast_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
14	0x0 RW	**I2C3_SCL_PAD_CFG0_broadcast_mask:** Reserved.
13	0x0 RW	**I2C2_SCL_PAD_CFG1_broadcast_mask:** Reserved.
12	0x0 RW	**I2C2_SCL_PAD_CFG0_broadcast_mask:** Reserved.
11	0x0 RW	**I2C0_SCL_PAD_CFG1_broadcast_mask:** Reserved.
10	0x0 RW	**I2C0_SCL_PAD_CFG0_broadcast_mask:** Reserved.
9	0x0 RW	**I2C3_SDA_PAD_CFG1_broadcast_mask:** Reserved.
8	0x0 RW	**I2C3_SDA_PAD_CFG0_broadcast_mask:** Reserved.
7	0x0 RW	**I2C1_SCL_PAD_CFG1_broadcast_mask:** Reserved.
6	0x0 RW	**I2C1_SCL_PAD_CFG0_broadcast_mask:** Reserved.
5	0x0 RW	**I2C2_SDA_PAD_CFG1_broadcast_mask:** Reserved.
4	0x0 RW	**I2C2_SDA_PAD_CFG0_broadcast_mask:** Reserved.
3	0x0 RW	**I2C0_SDA_PAD_CFG1_broadcast_mask:** Reserved.
2	0x0 RW	**I2C0_SDA_PAD_CFG0_broadcast_mask:** Reserved.
1	0x0 RW	**I2C1_SDA_PAD_CFG1_broadcast_mask:** Reserved.
0	0x0 RW	**I2C1_SDA_PAD_CFG0_broadcast_mask:** Reserved.

10.7.58 gpio_pad_broadcast_reg_mask #3 (gpio_pad_broadcast_reg_mask_3)—Offset 4014h

Pad Broadcast Register Masking

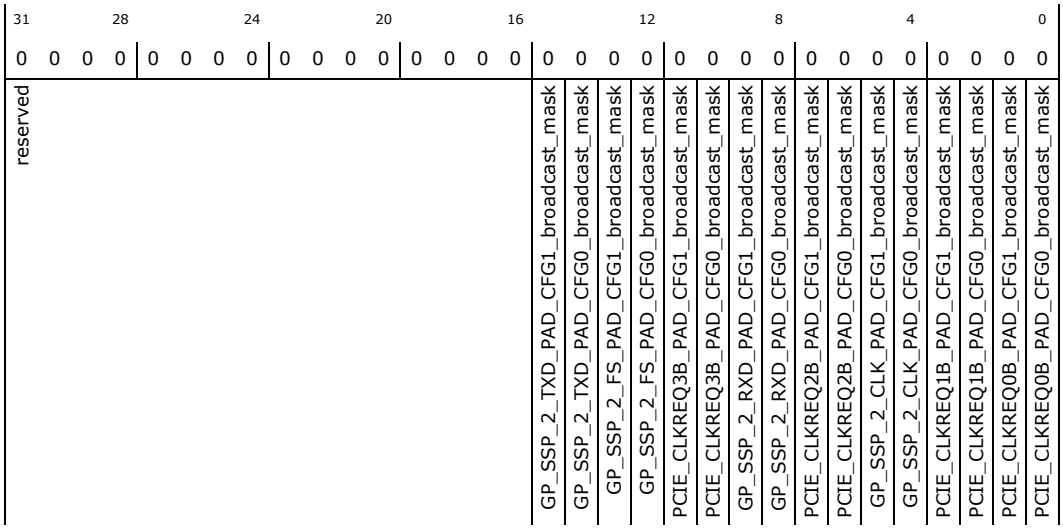
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4014h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**reserved:** Reserved.
15	0x0 RW	**GP_SSP_2_TXD_PAD_CFG1_broadcast_mask:** Reserved.
14	0x0 RW	**GP_SSP_2_TXD_PAD_CFG0_broadcast_mask:** Reserved.
13	0x0 RW	**GP_SSP_2_FS_PAD_CFG1_broadcast_mask:** Reserved.
12	0x0 RW	**GP_SSP_2_FS_PAD_CFG0_broadcast_mask:** Reserved.
11	0x0 RW	**PCIE_CLKREQ3B_PAD_CFG1_broadcast_mask:** Reserved.
10	0x0 RW	**PCIE_CLKREQ3B_PAD_CFG0_broadcast_mask:** Reserved.
9	0x0 RW	**GP_SSP_2_RXD_PAD_CFG1_broadcast_mask:** Reserved.
8	0x0 RW	**GP_SSP_2_RXD_PAD_CFG0_broadcast_mask:** Reserved.
7	0x0 RW	**PCIE_CLKREQ2B_PAD_CFG1_broadcast_mask:** Reserved.
6	0x0 RW	**PCIE_CLKREQ2B_PAD_CFG0_broadcast_mask:** Reserved.
5	0x0 RW	**GP_SSP_2_CLK_PAD_CFG1_broadcast_mask:** Reserved.
4	0x0 RW	**GP_SSP_2_CLK_PAD_CFG0_broadcast_mask:** Reserved.
3	0x0 RW	**PCIE_CLKREQ1B_PAD_CFG1_broadcast_mask:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
2	0x0 RW	**PCIE_CLKREQ1B_PAD_CFG0_broadcast_mask:** Reserved.
1	0x0 RW	**PCIE_CLKREQ0B_PAD_CFG1_broadcast_mask:** Reserved.
0	0x0 RW	**PCIE_CLKREQ0B_PAD_CFG0_broadcast_mask:** Reserved.

10.7.59 Pad Control Register 0 (FST_SPI_D2_PAD_CFG0)—Offset 4400h

Pad Control Register 0

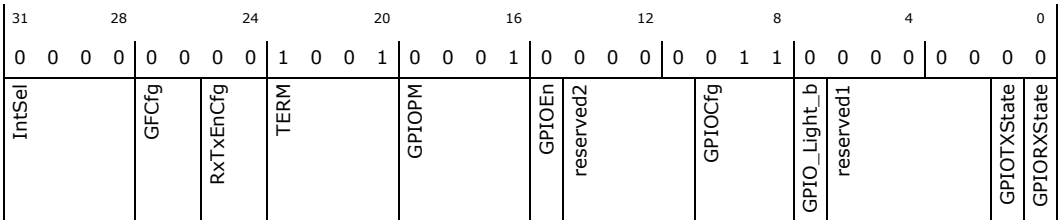
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4400h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.60 Pad Control Register 1 (FST_SPI_D2_PAD_CFG1)—Offset 4404h

Pad Control Register 1

Access Method

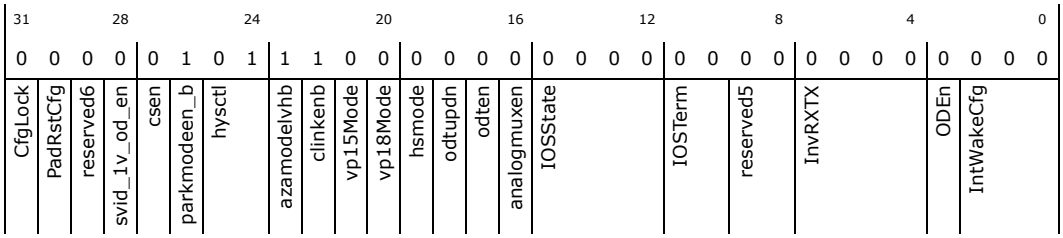
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4404h

Op Codes:

h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.61 Pad Control Register 0 (FST_SPI_D0_PAD_CFG0)—Offset 4408h

Pad Control Register 0

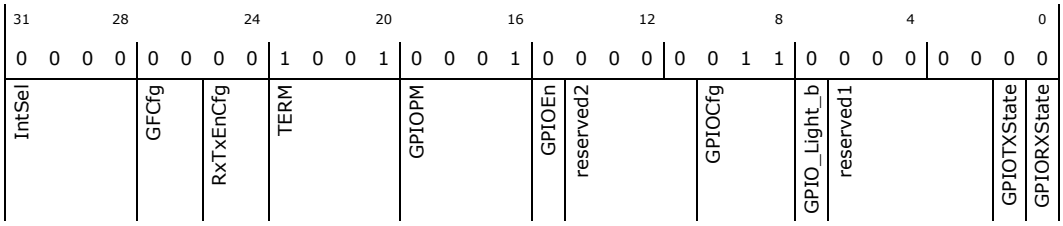
Access Method

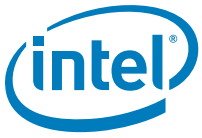
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4408h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.62 Pad Control Register 1 (FST_SPI_D0_PAD_CFG1)—Offset 440Ch

Pad Control Register 1

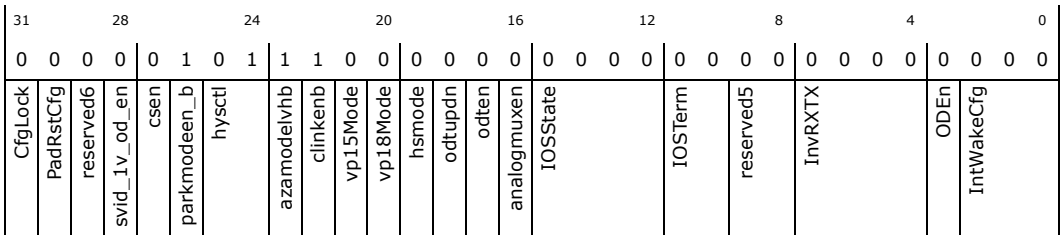
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 440Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.63 Pad Control Register 0 (FST_SPI_CLK_PAD_CFG0)—Offset 4410h

Pad Control Register 0

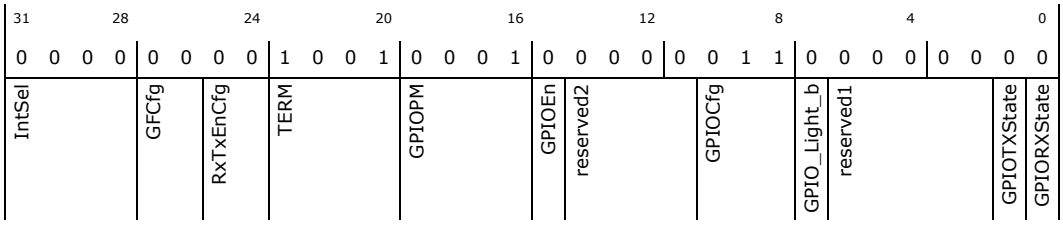
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4410h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.64 Pad Control Register 1 (FST_SPI_CLK_PAD_CFG1)—Offset 4414h

Pad Control Register 1

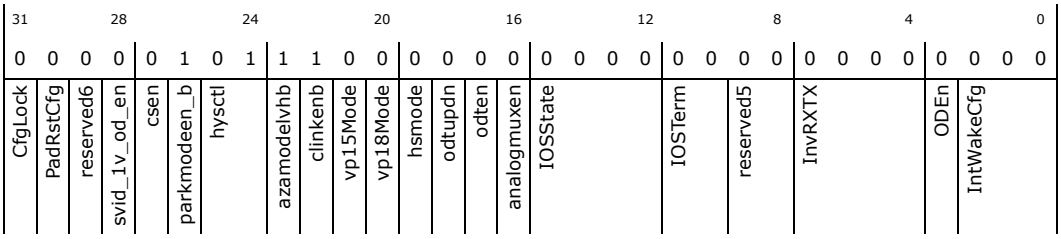
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4414h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.65 Pad Control Register 0 (FST_SPI_D3_PAD_CFG0)—Offset 4418h

Pad Control Register 0

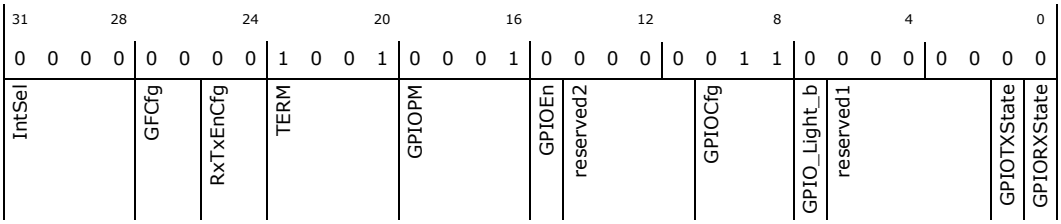
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4418h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.66 Pad Control Register 1 (FST_SPI_D3_PAD_CFG1)—Offset 441Ch

Pad Control Register 1

Access Method

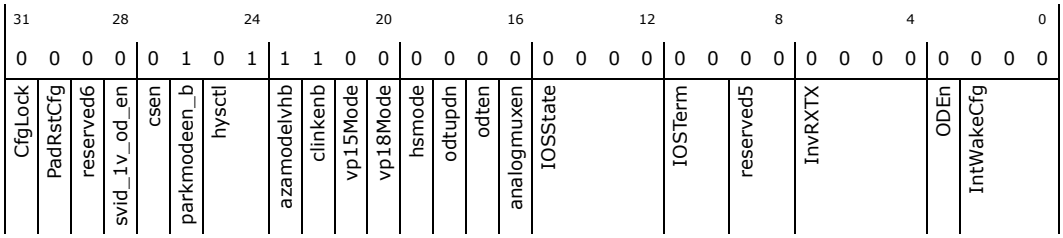
Type: Message Bus Register (Size: 32 bits)

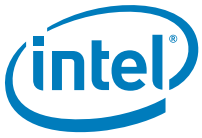
Offset: [Port: 0xB2] + 441Ch

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.67 Pad Control Register 0 (FST_SPI_CS1_B_PAD_CFG0)—Offset 4420h

Pad Control Register 0

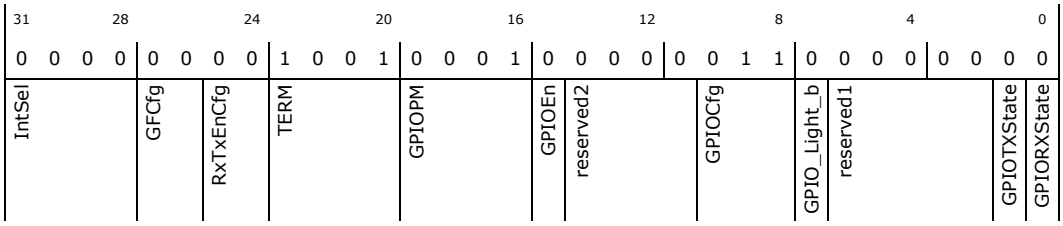
Access Method

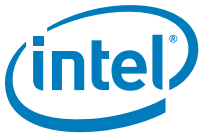
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4420h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.68 Pad Control Register 1 (FST_SPI_CS1_B_PAD_CFG1)—Offset 4424h

Pad Control Register 1

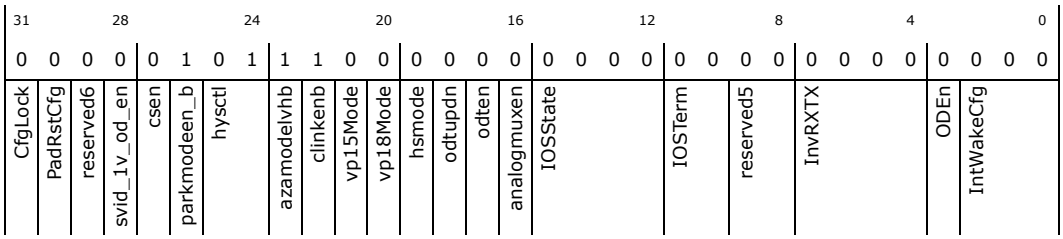
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4424h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.69 Pad Control Register 0 (FST_SPI_D1_PAD_CFG0)—Offset 4428h

Pad Control Register 0

Access Method

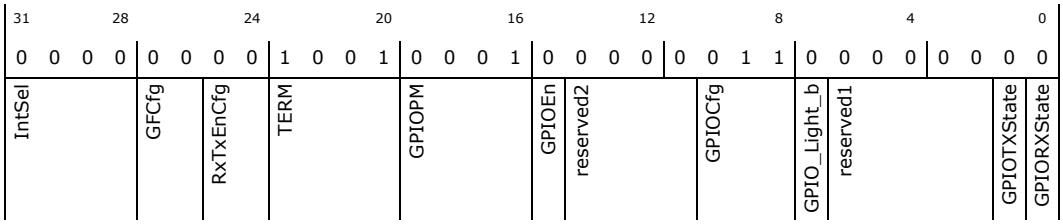
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4428h

Op Codes:

h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.70 Pad Control Register 1 (FST_SPI_D1_PAD_CFG1)—Offset 442Ch

Pad Control Register 1

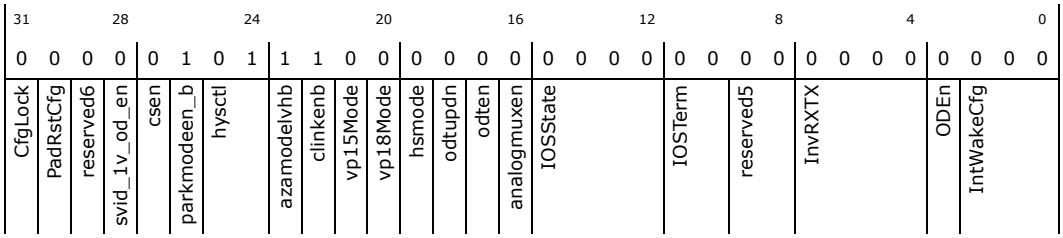
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 442Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.71 Pad Control Register 0 (FST_SPI_CS0_B_PAD_CFG0)—Offset 4430h

Pad Control Register 0

Access Method

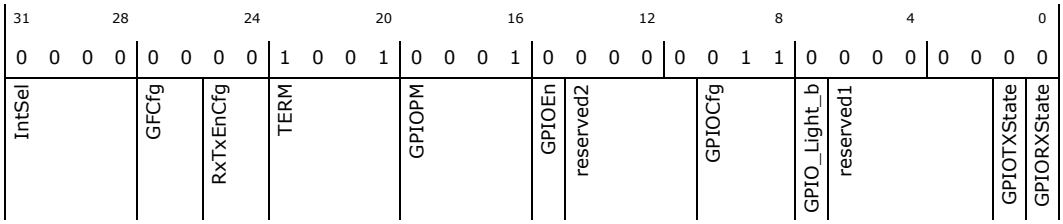
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4430h

Op Codes:

h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.72 Pad Control Register 1 (FST_SPI_CS0_B_PAD_CFG1)—Offset 4434h

Pad Control Register 1

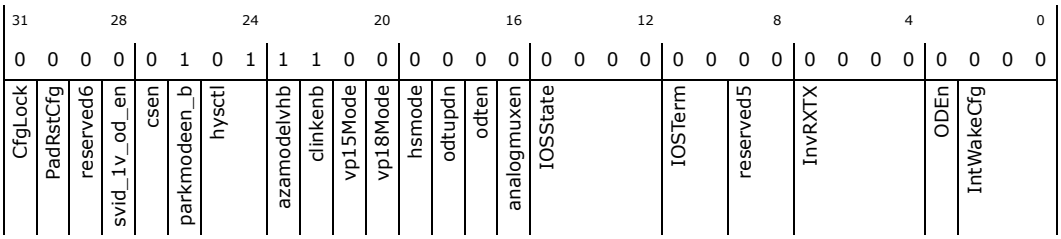
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4434h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6

Bit Range	Default and Access	Field Name (ID): Description
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.73 Pad Control Register 0 (FST_SPI_CS2_B_PAD_CFG0)—Offset 4438h

Pad Control Register 0

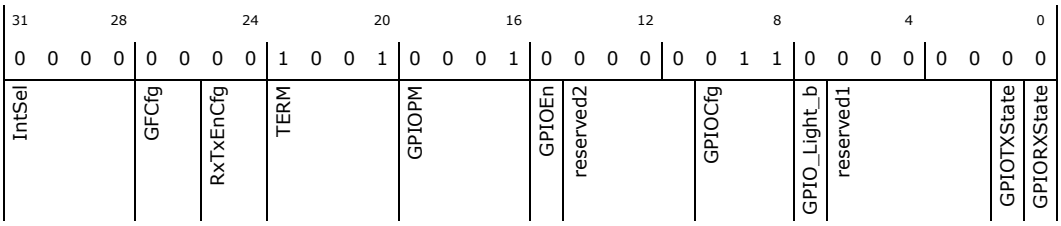
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4438h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.74 Pad Control Register 1 (FST_SPI_CS2_B_PAD_CFG1)—Offset 443Ch

Pad Control Register 1

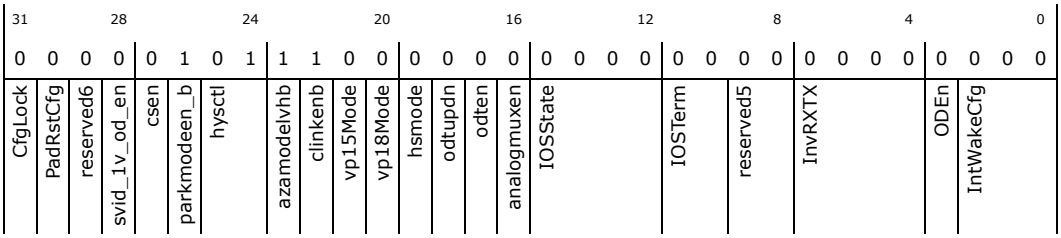
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 443Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.75 Pad Control Register 0 (UART1_RTS_B_PAD_CFG0)—Offset 4800h

Pad Control Register 0

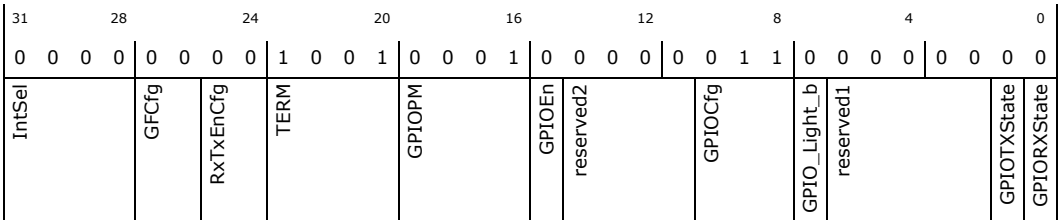
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4800h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.76 Pad Control Register 1 (UART1_RTS_B_PAD_CFG1)—Offset 4804h

Pad Control Register 1

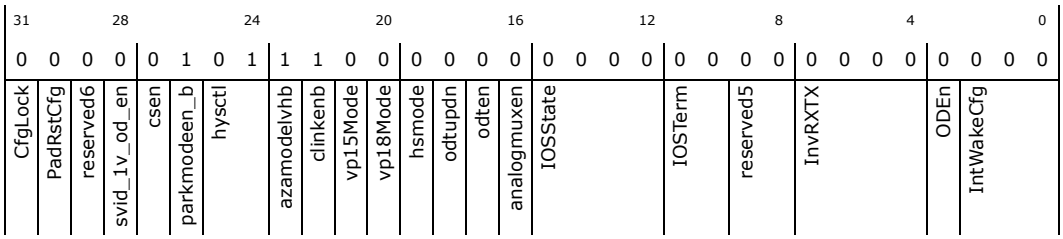
Access Method

Type: Message Bus Register (Size: 32 bits)

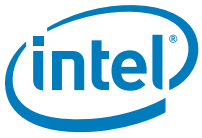
Offset: [Port: 0xB2] + 4804h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6



Bit Range	Default and Access	Field Name (ID): Description
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.77 Pad Control Register 0 (UART1_RXD_PAD_CFG0)—Offset 4808h

Pad Control Register 0

Access Method

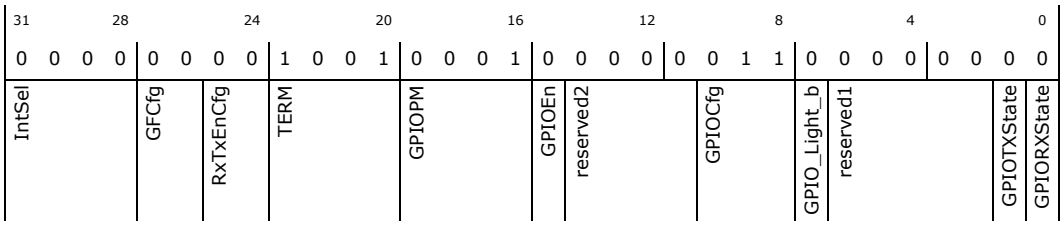
Type: Message Bus Register (Size: 32 bits)

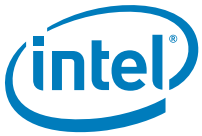
Offset: [Port: 0xB2] + 4808h

Op Codes:

h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.78 Pad Control Register 1 (UART1_RXD_PAD_CFG1)—Offset 480Ch

Pad Control Register 1

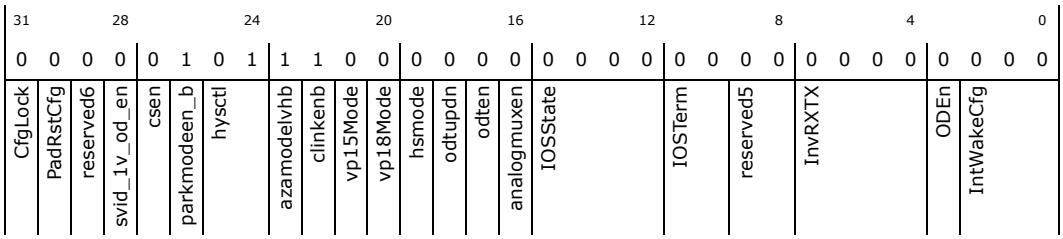
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 480Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.79 Pad Control Register 0 (UART2_RXD_PAD_CFG0)—Offset 4810h

Pad Control Register 0

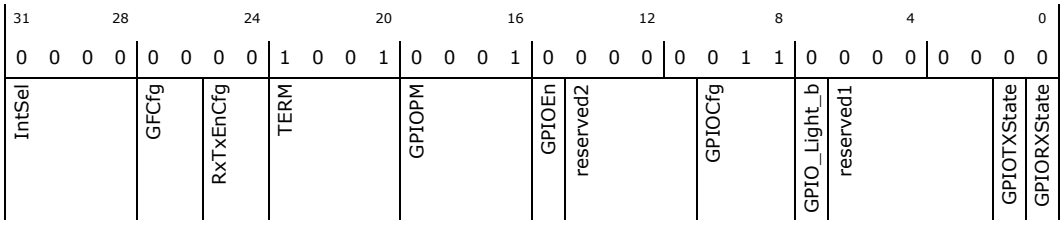
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4810h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.80 Pad Control Register 1 (UART2_RXD_PAD_CFG1)—Offset 4814h

Pad Control Register 1

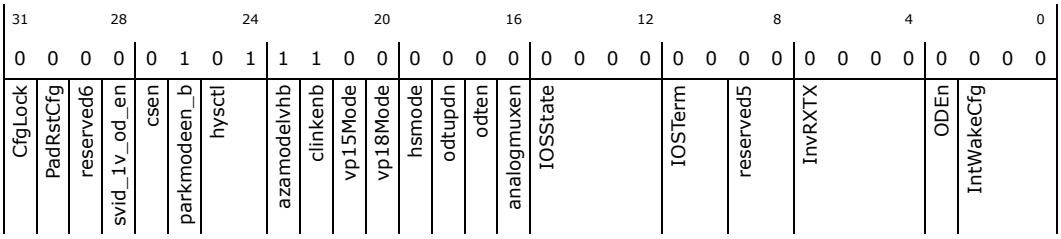
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4814h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.81 Pad Control Register 0 (UART1_CTS_B_PAD_CFG0)—Offset 4818h

Pad Control Register 0

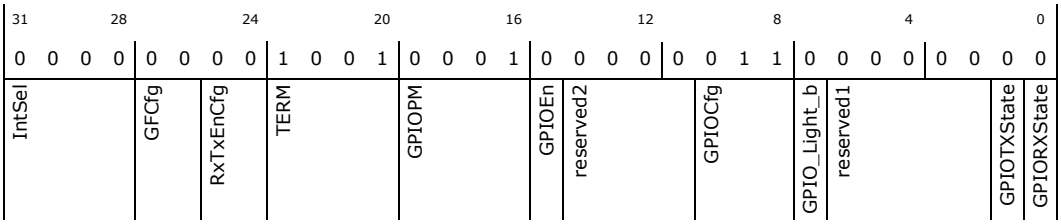
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4818h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.82 Pad Control Register 1 (UART1_CTS_B_PAD_CFG1)—Offset 481Ch

Pad Control Register 1

Access Method

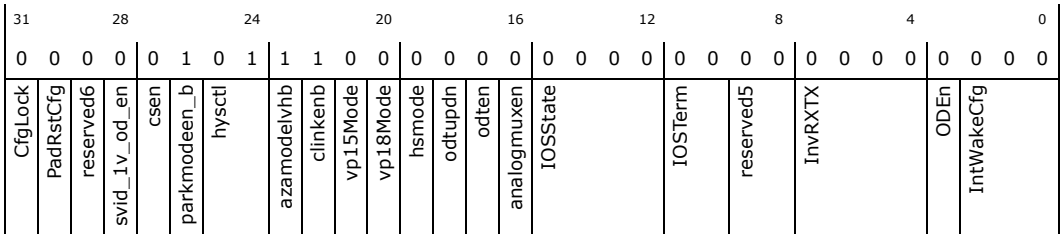
Type: Message Bus Register (Size: 32 bits)

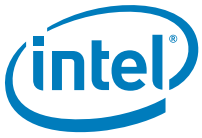
Offset: [Port: 0xB2] + 481Ch

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.83 Pad Control Register 0 (UART2_RTS_B_PAD_CFG0)—Offset 4820h

Pad Control Register 0

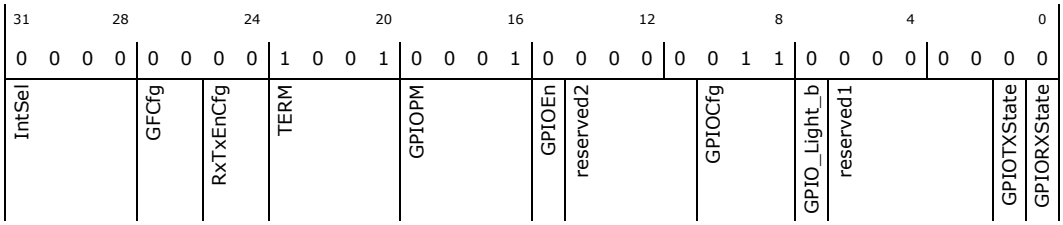
Access Method

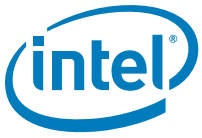
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4820h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.84 Pad Control Register 1 (UART2_RTS_B_PAD_CFG1)—Offset 4824h

Pad Control Register 1

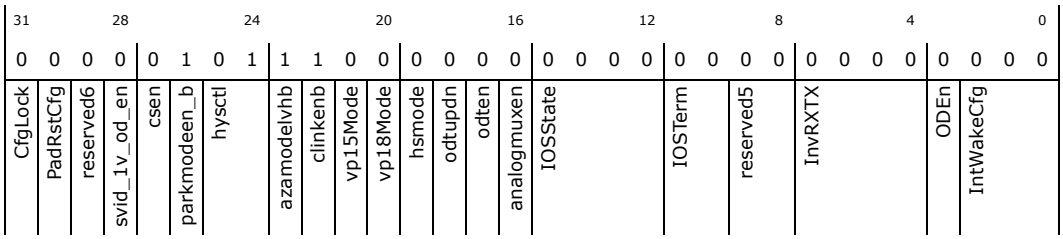
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4824h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.85 Pad Control Register 0 (UART1_TXD_PAD_CFG0)—Offset 4828h

Pad Control Register 0

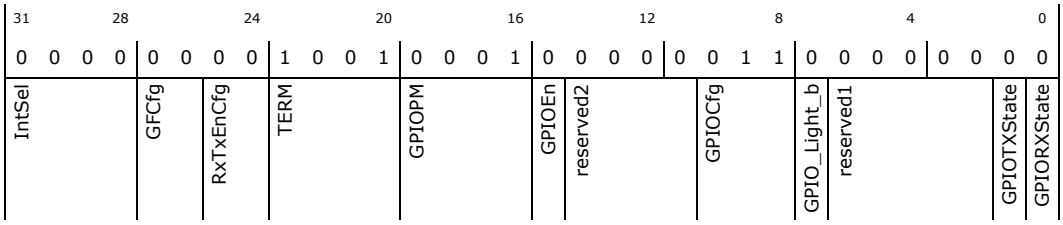
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4828h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.86 Pad Control Register 1 (UART1_TXD_PAD_CFG1)—Offset 482Ch

Pad Control Register 1

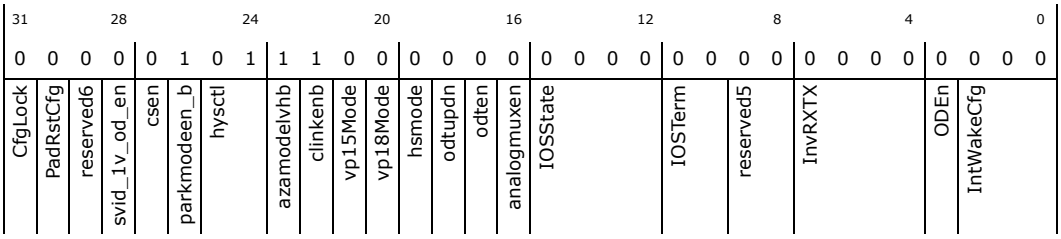
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 482Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.87 Pad Control Register 0 (UART2_TXD_PAD_CFG0)—Offset 4830h

Pad Control Register 0

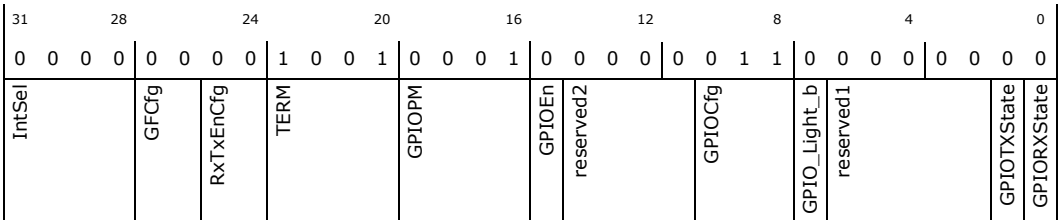
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4830h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.88 Pad Control Register 1 (UART2_TXD_PAD_CFG1)—Offset 4834h

Pad Control Register 1

Access Method

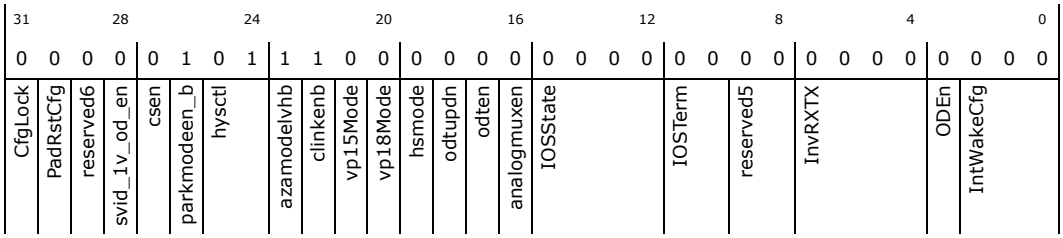
Type: Message Bus Register (Size: 32 bits)

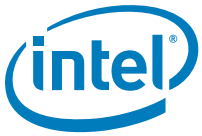
Offset: [Port: 0xB2] + 4834h

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.89 Pad Control Register 0 (UART2_CTS_B_PAD_CFG0)—Offset 4838h

Pad Control Register 0

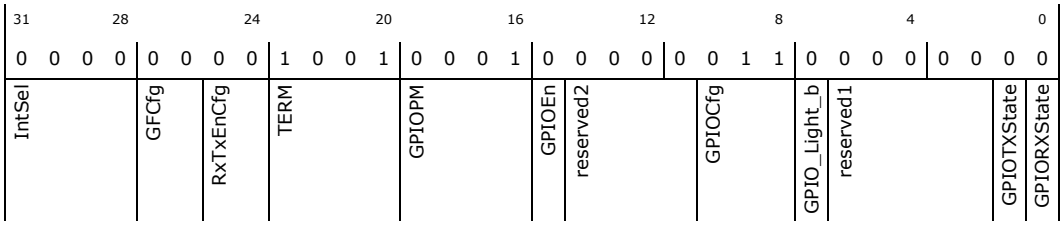
Access Method

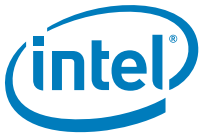
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 4838h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.90 Pad Control Register 1 (UART2_CTS_B_PAD_CFG1)—Offset 483Ch

Pad Control Register 1

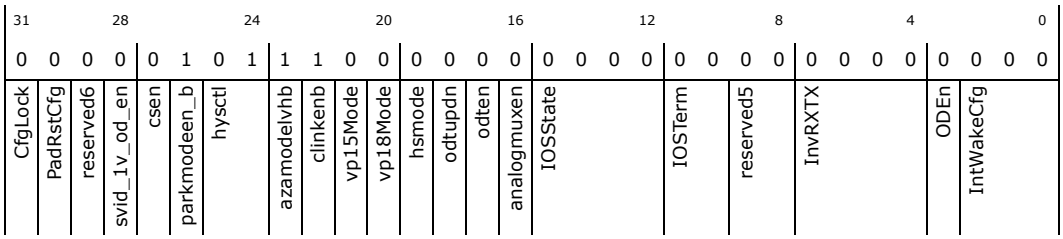
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 483Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.91 Pad Control Register 0 (I2C5_SDA_PAD_CFG0)—Offset 5000h

Pad Control Register 0

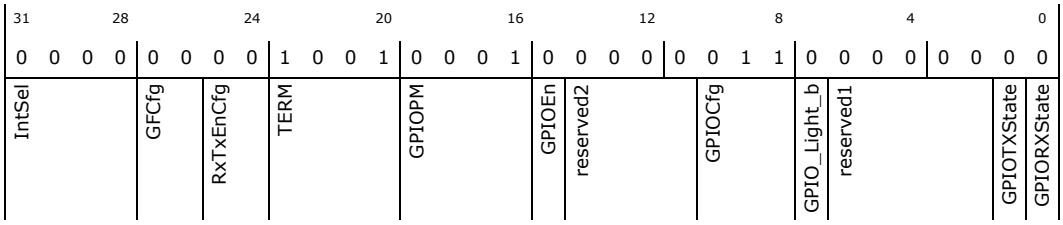
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5000h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.92 Pad Control Register 1 (I2C5_SDA_PAD_CFG1)—Offset 5004h

Pad Control Register 1

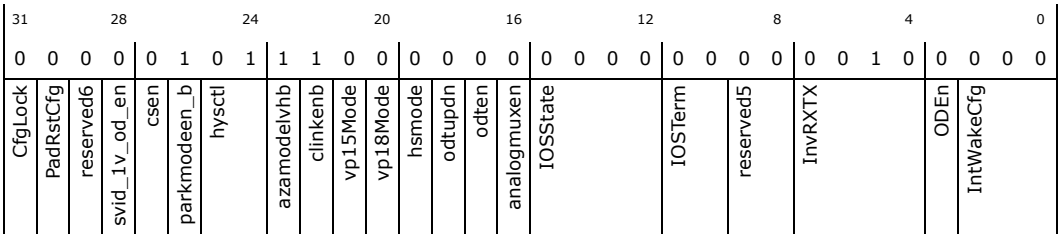
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5004h

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.93 Pad Control Register 0 (I2C4_SDA_PAD_CFG0)—Offset 5008h

Pad Control Register 0

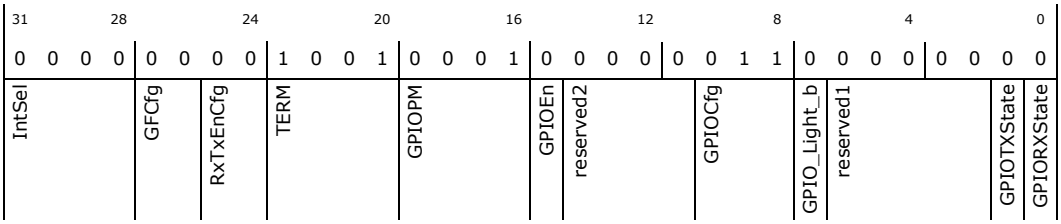
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5008h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.94 Pad Control Register 1 (I2C4_SDA_PAD_CFG1)—Offset 500Ch

Pad Control Register 1

Access Method

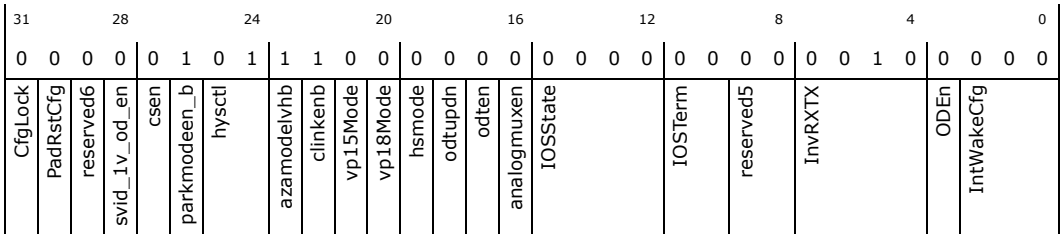
Type: Message Bus Register (Size: 32 bits)

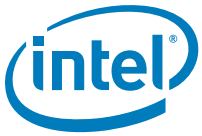
Offset: [Port: 0xB2] + 500Ch

Op Codes:

h - Read, h - Write

Default: 05C00020h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.95 Pad Control Register 0 (I2C6_SDA_PAD_CFG0)—Offset 5010h

Pad Control Register 0

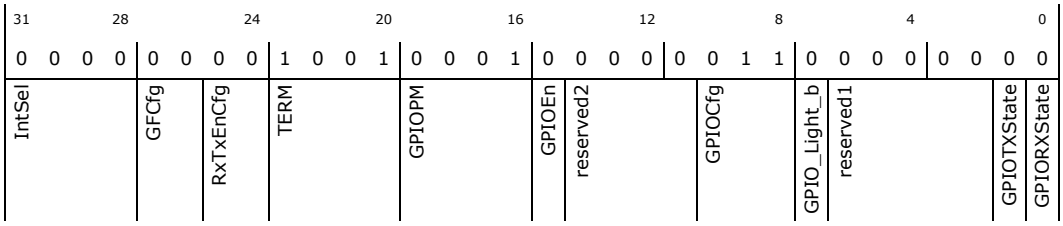
Access Method

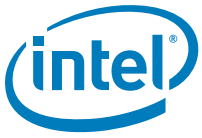
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5010h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.96 Pad Control Register 1 (I2C6_SDA_PAD_CFG1)—Offset 5014h

Pad Control Register 1

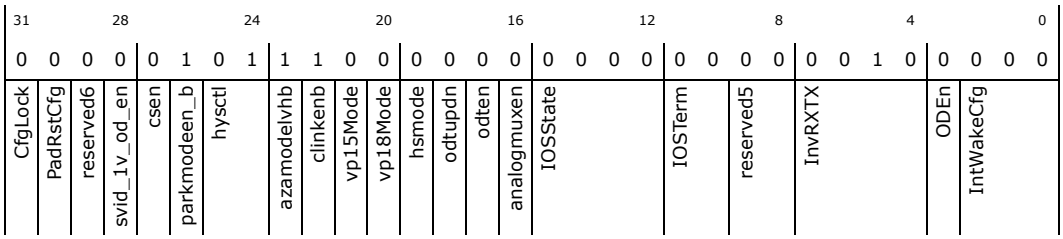
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5014h

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.97 Pad Control Register 0 (I2C5_SCL_PAD_CFG0)—Offset 5018h

Pad Control Register 0

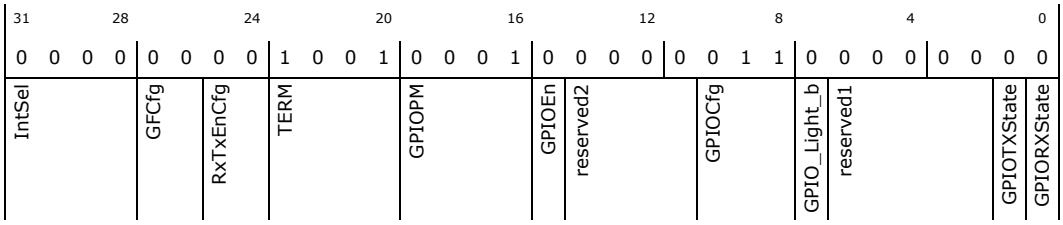
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5018h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.98 Pad Control Register 1 (I2C5_SCL_PAD_CFG1)—Offset 501Ch

Pad Control Register 1

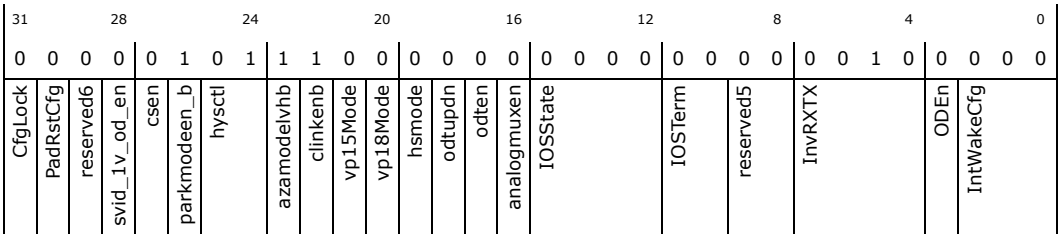
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 501Ch

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.99 Pad Control Register 0 (I2C_NFC_SDA_PAD_CFG0)—Offset 5020h

Pad Control Register 0

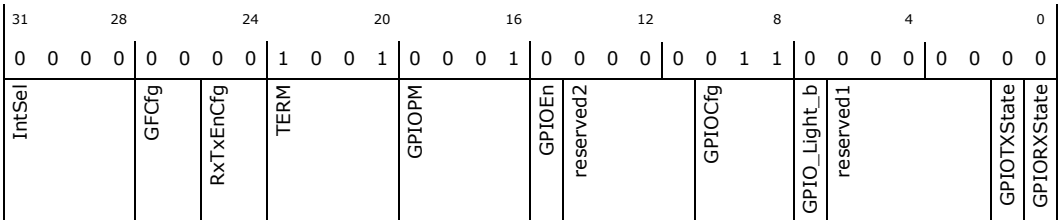
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5020h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.100 Pad Control Register 1 (I2C_NFC_SDA_PAD_CFG1)—Offset 5024h

Pad Control Register 1

Access Method

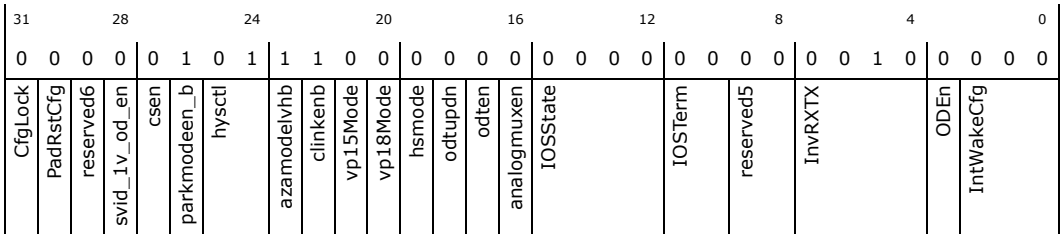
Type: Message Bus Register (Size: 32 bits)

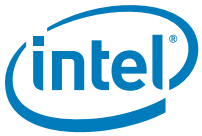
Offset: [Port: 0xB2] + 5024h

Op Codes:

h - Read, h - Write

Default: 05C00020h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.101 Pad Control Register 0 (I2C4_SCL_PAD_CFG0)—Offset 5028h

Pad Control Register 0

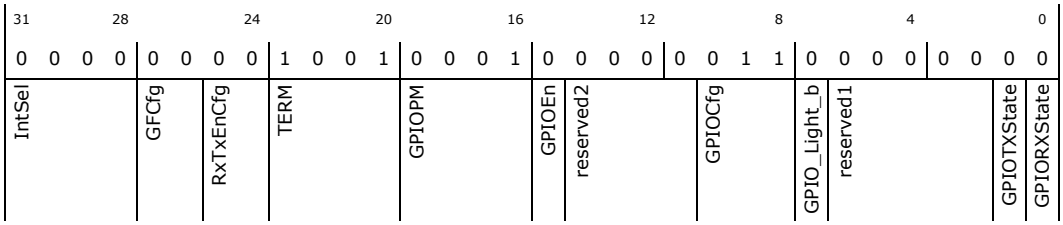
Access Method

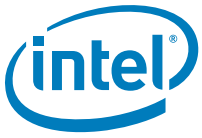
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5028h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.102 Pad Control Register 1 (I2C4_SCL_PAD_CFG1)—Offset 502Ch

Pad Control Register 1

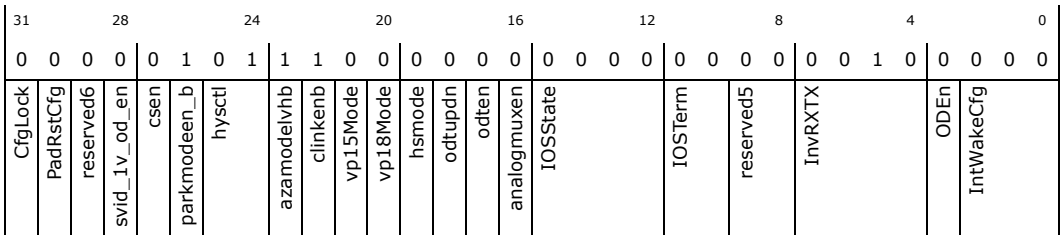
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 502Ch

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.103 Pad Control Register 0 (I2C6_SCL_PAD_CFG0)—Offset 5030h

Pad Control Register 0

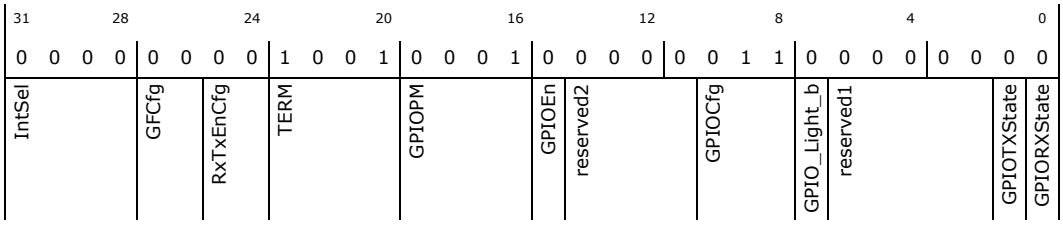
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5030h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.104 Pad Control Register 1 (I2C6_SCL_PAD_CFG1)—Offset 5034h

Pad Control Register 1

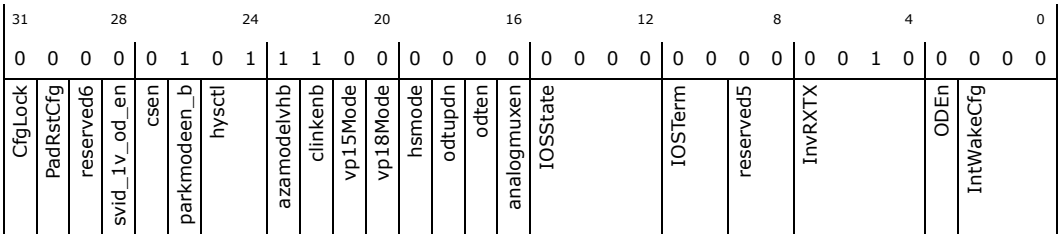
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5034h

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.105 Pad Control Register 0 (I2C_NFC_SCL_PAD_CFG0)—Offset 5038h

Pad Control Register 0

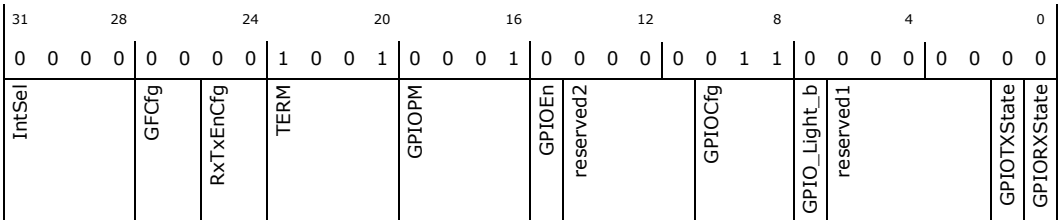
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5038h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.106 Pad Control Register 1 (I2C_NFC_SCL_PAD_CFG1)—Offset 503Ch

Pad Control Register 1

Access Method

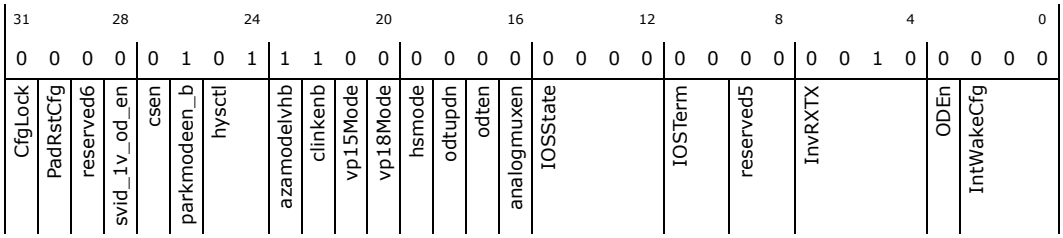
Type: Message Bus Register (Size: 32 bits)

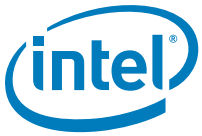
Offset: [Port: 0xB2] + 503Ch

Op Codes:

h - Read, h - Write

Default: 05C00020h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.107 Pad Control Register 0 (I2C1_SDA_PAD_CFG0)—Offset 5400h

Pad Control Register 0

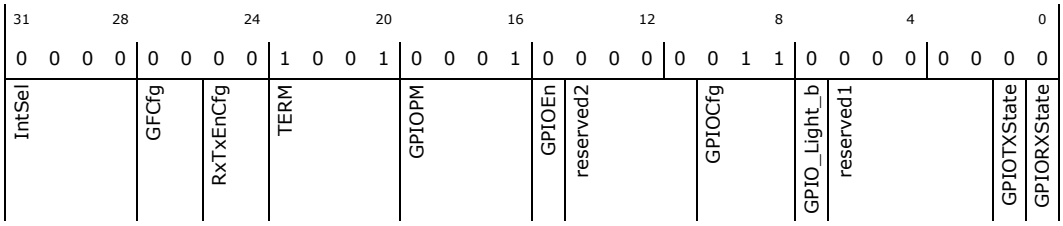
Access Method

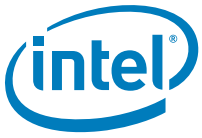
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5400h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.108 Pad Control Register 1 (I2C1_SDA_PAD_CFG1)—Offset 5404h

Pad Control Register 1

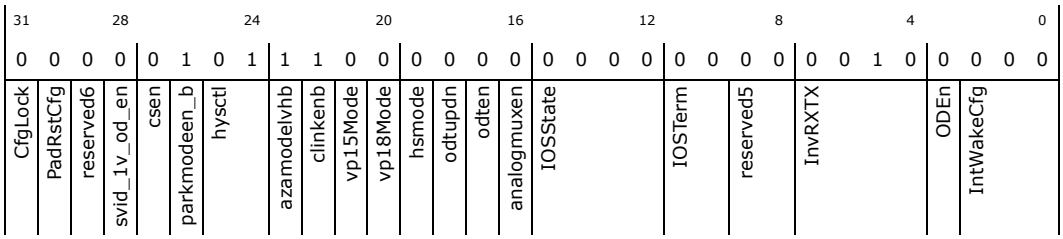
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5404h

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.109 Pad Control Register 0 (I2C0_SDA_PAD_CFG0)—Offset 5408h

Pad Control Register 0

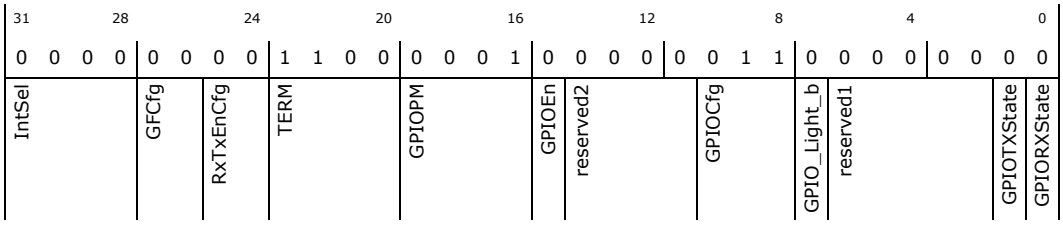
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5408h

Op Codes:
h - Read, h - Write

Default: 00C10300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0xc RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.110 Pad Control Register 1 (I2C0_SDA_PAD_CFG1)—Offset 540Ch

Pad Control Register 1

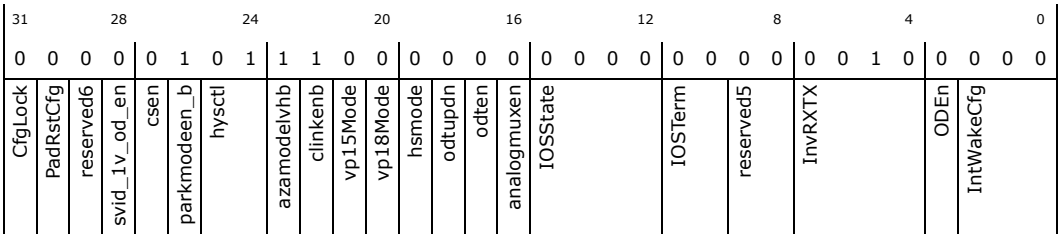
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 540Ch

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.111 Pad Control Register 0 (I2C2_SDA_PAD_CFG0)—Offset 5410h

Pad Control Register 0

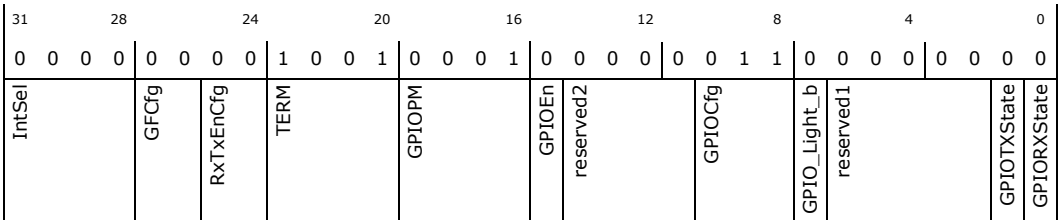
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5410h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.112 Pad Control Register 1 (I2C2_SDA_PAD_CFG1)—Offset 5414h

Pad Control Register 1

Access Method

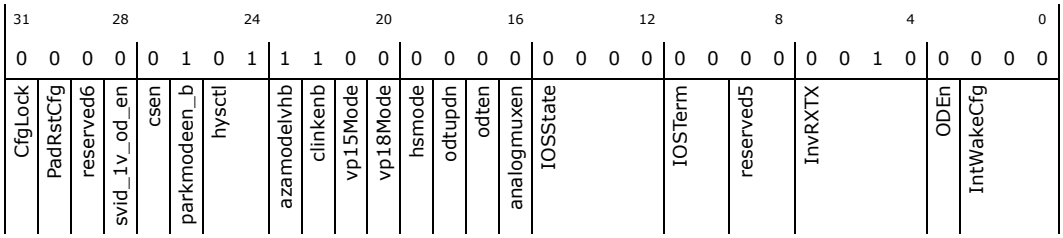
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5414h

Op Codes:

h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.113 Pad Control Register 0 (I2C1_SCL_PAD_CFG0)—Offset 5418h

Pad Control Register 0

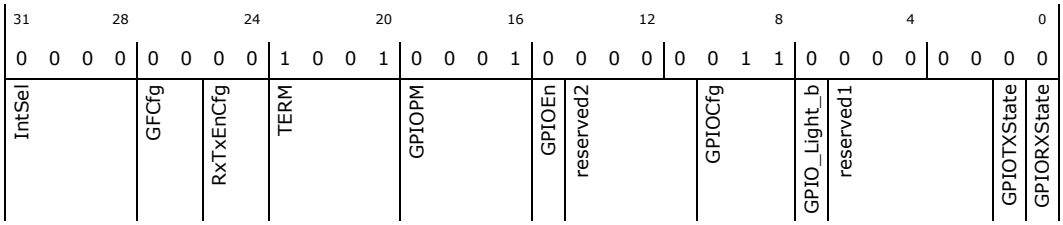
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5418h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.114 Pad Control Register 1 (I2C1_SCL_PAD_CFG1)—Offset 541Ch

Pad Control Register 1

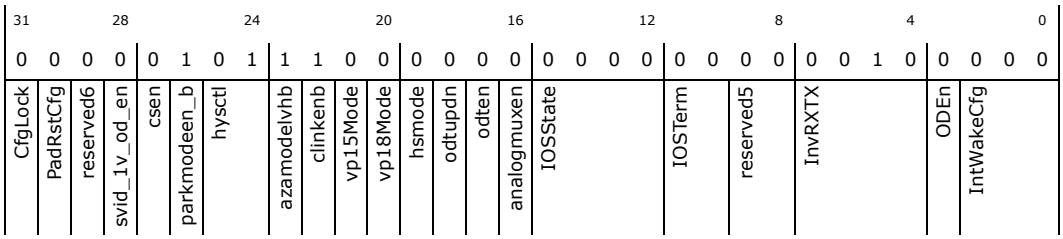
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 541Ch

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.115 Pad Control Register 0 (I2C3_SDA_PAD_CFG0)—Offset 5420h

Pad Control Register 0

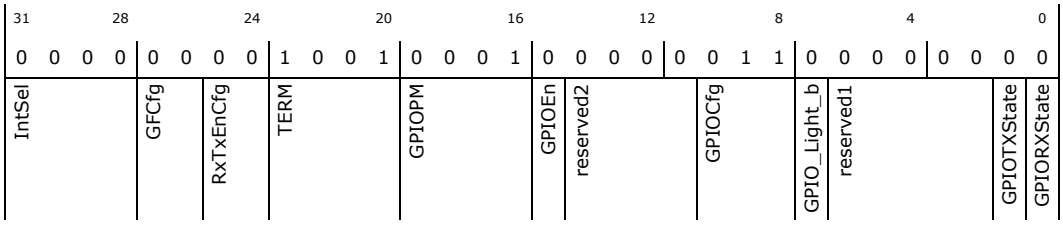
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5420h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.116 Pad Control Register 1 (I2C3_SDA_PAD_CFG1)—Offset 5424h

Pad Control Register 1

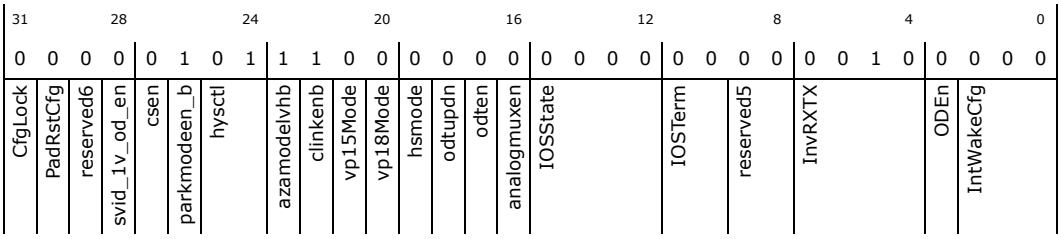
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5424h

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.117 Pad Control Register 0 (I2C0_SCL_PAD_CFG0)—Offset 5428h

Pad Control Register 0

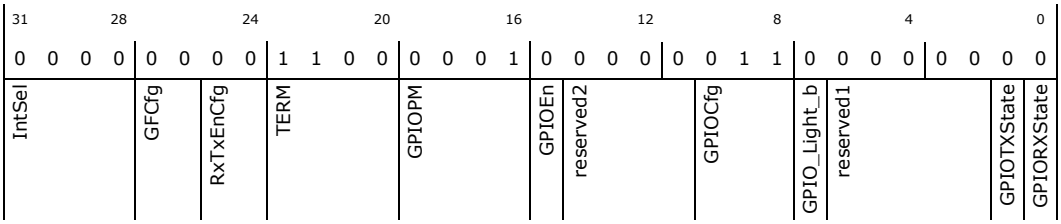
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5428h

Op Codes:
h - Read, h - Write

Default: 00C10300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0xc RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.118 Pad Control Register 1 (I2C0_SCL_PAD_CFG1)—Offset 542Ch

Pad Control Register 1

Access Method

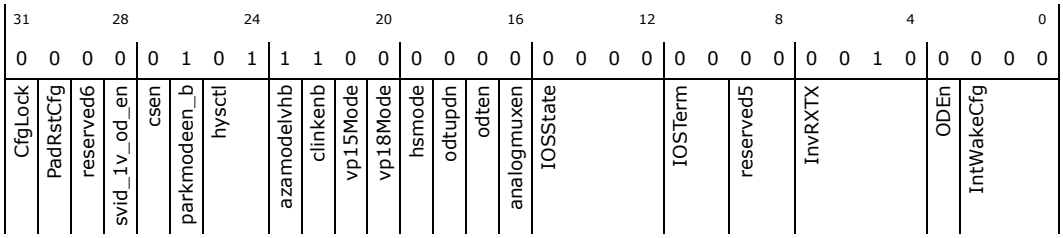
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 542Ch

Op Codes:

h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.119 Pad Control Register 0 (I2C2_SCL_PAD_CFG0)—Offset 5430h

Pad Control Register 0

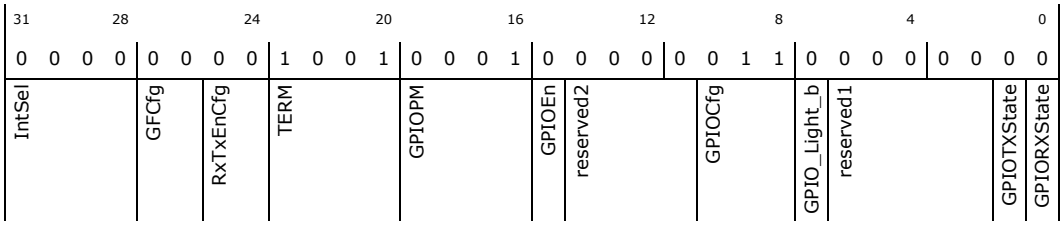
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5430h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.120 Pad Control Register 1 (I2C2_SCL_PAD_CFG1)—Offset 5434h

Pad Control Register 1

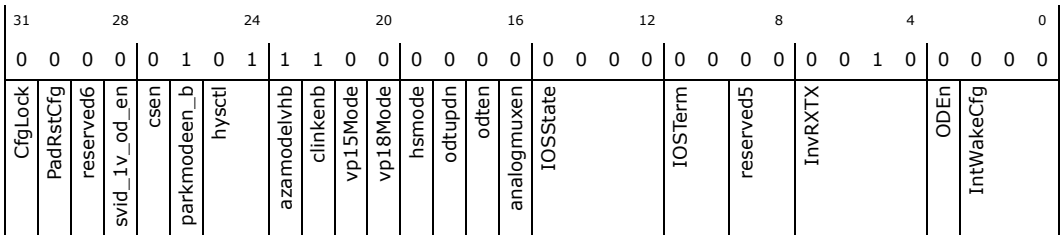
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5434h

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.121 Pad Control Register 0 (I2C3_SCL_PAD_CFG0)—Offset 5438h

Pad Control Register 0

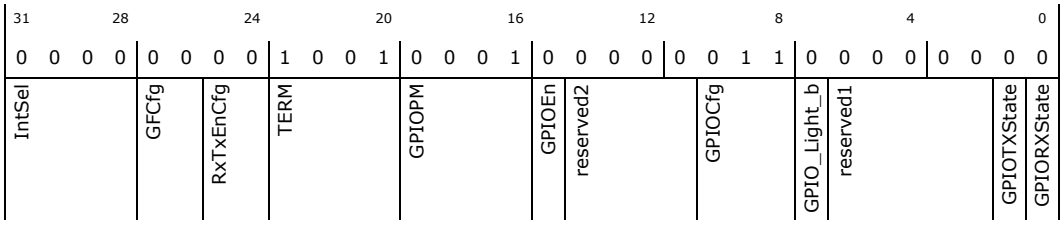
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5438h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.122 Pad Control Register 1 (I2C3_SCL_PAD_CFG1)—Offset 543Ch

Pad Control Register 1

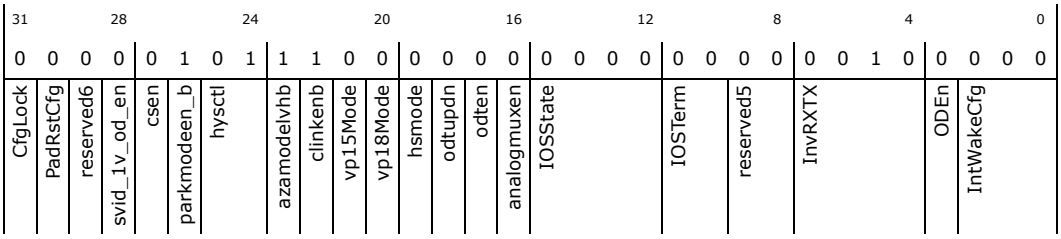
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 543Ch

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.123 Pad Control Register 0 (PCIE_CLKREQ0B_PAD_CFG0)—Offset 5C00h

Pad Control Register 0

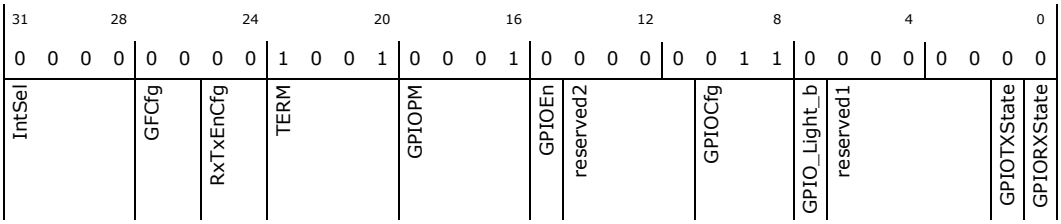
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5C00h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.124 Pad Control Register 1 (PCIE_CLKREQ0B_PAD_CFG1)—Offset 5C04h

Pad Control Register 1

Access Method

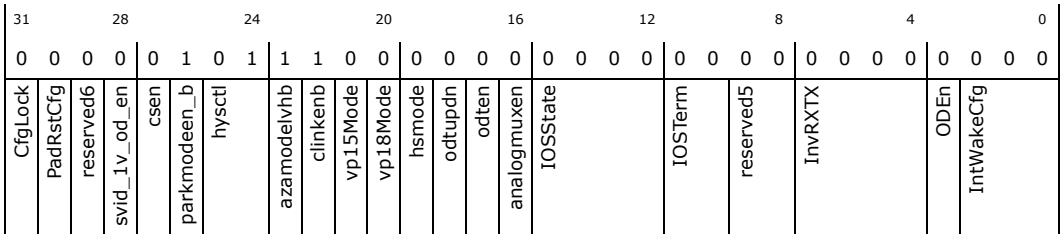
Type: Message Bus Register (Size: 32 bits)

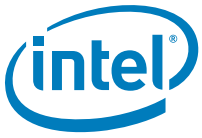
Offset: [Port: 0xB2] + 5C04h

Op Codes:

h - Read, h - Write

Default: 05C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.125 Pad Control Register 0 (PCIE_CLKREQ1B_PAD_CFG0)—Offset 5C08h

Pad Control Register 0

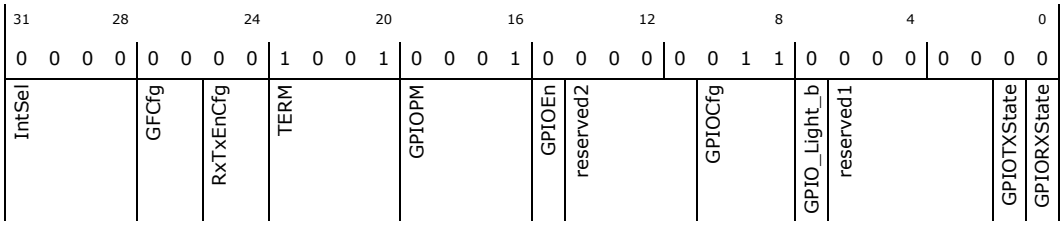
Access Method

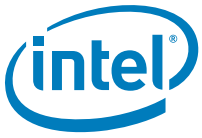
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5C08h

Op Codes:
h - Read, h - Write

Default: 00910300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.126 Pad Control Register 1 (PCIE_CLKREQ1B_PAD_CFG1)—Offset 5C0Ch

Pad Control Register 1

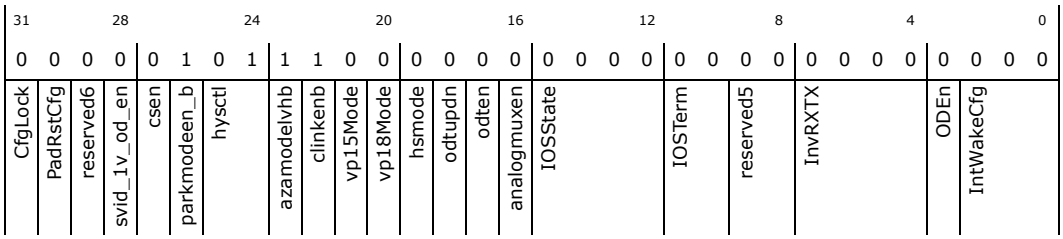
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5C0Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.127 Pad Control Register 0 (GP_SSP_2_CLK_PAD_CFG0)—Offset 5C10h

Pad Control Register 0

Access Method

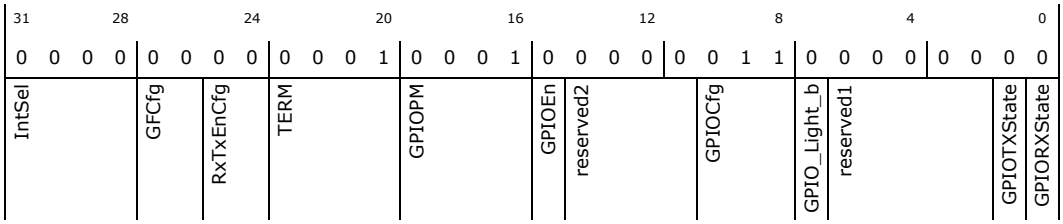
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5C10h

Op Codes:

h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.128 Pad Control Register 1 (GP_SSP_2_CLK_PAD_CFG1)—Offset 5C14h

Pad Control Register 1

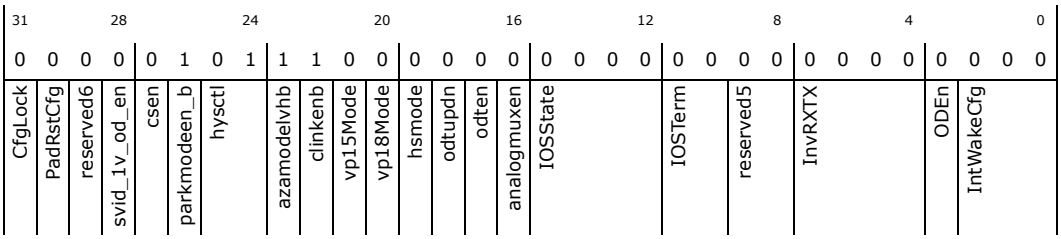
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5C14h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6

Bit Range	Default and Access	Field Name (ID): Description
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.

Bit Range	Default and Access	Field Name (ID): Description
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.129 Pad Control Register 0 (PCIE_CLKREQ2B_PAD_CFG0)—Offset 5C18h

Pad Control Register 0

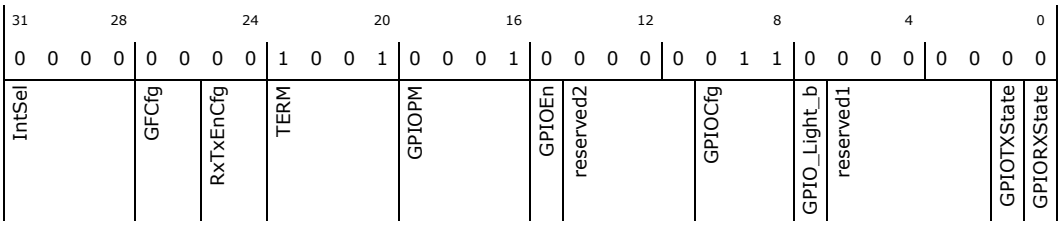
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5C18h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.130 Pad Control Register 1 (PCIE_CLKREQ2B_PAD_CFG1)—Offset 5C1Ch

Pad Control Register 1

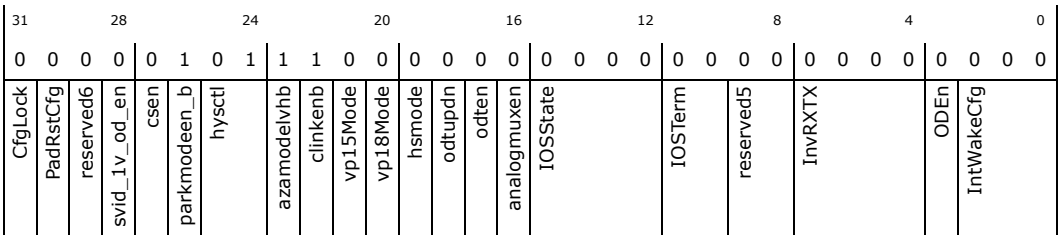
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5C1Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.131 Pad Control Register 0 (GP_SSP_2_RXD_PAD_CFG0)—Offset 5C20h

Pad Control Register 0

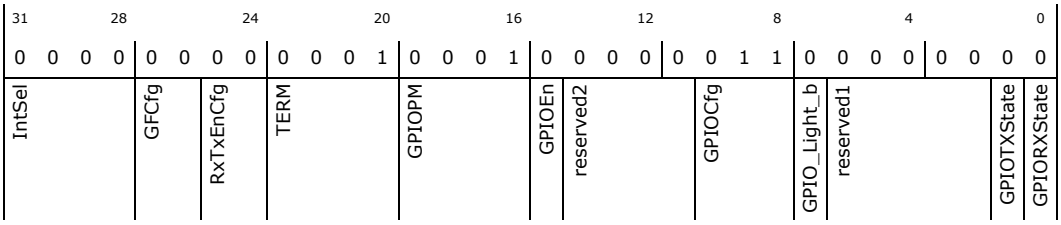
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5C20h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.132 Pad Control Register 1 (GP_SSP_2_RXD_PAD_CFG1)—Offset 5C24h

Pad Control Register 1

Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5C24h

Op Codes:
h - Read, h - Write

Default: 05C00000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CfgLock	PadRstCfg	reserved6	svid_1v_od_en	csen	parkmodeen_b	hysctl		azamodelvhb	clinkenb	vp15Mode	vp18Mode	hsmode	odtupdn	odten	analogmuxen	IOSState				IOSTerm		reserved5		InvRXTX				ODEn	IntWakeCfg		

Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.133 Pad Control Register 0 (PCIE_CLKREQ3B_PAD_CFG0)—Offset 5C28h

Pad Control Register 0

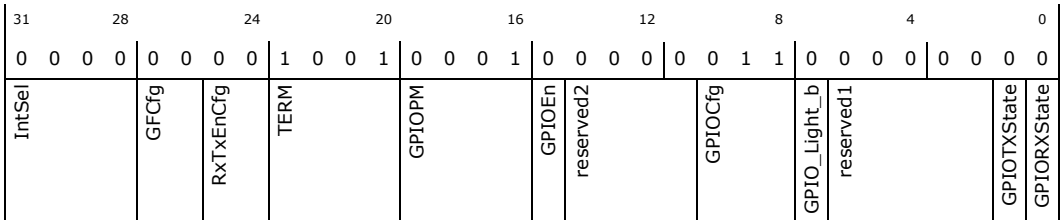
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5C28h

Op Codes:
h - Read, h - Write

Default: 00910300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x9 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.134 Pad Control Register 1 (PCIE_CLKREQ3B_PAD_CFG1)—Offset 5C2Ch

Pad Control Register 1

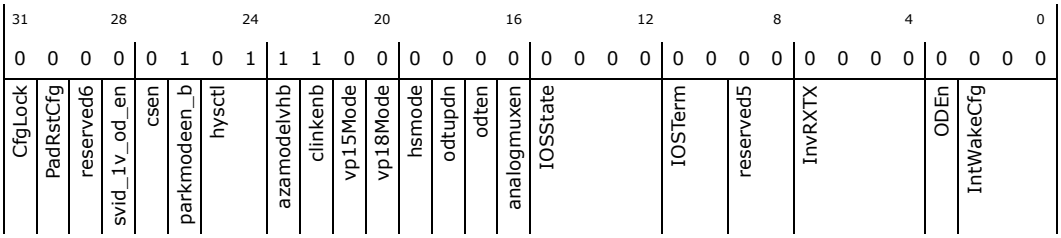
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5C2Ch

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.135 Pad Control Register 0 (GP_SSP_2_FS_PAD_CFG0)—Offset 5C30h

Pad Control Register 0

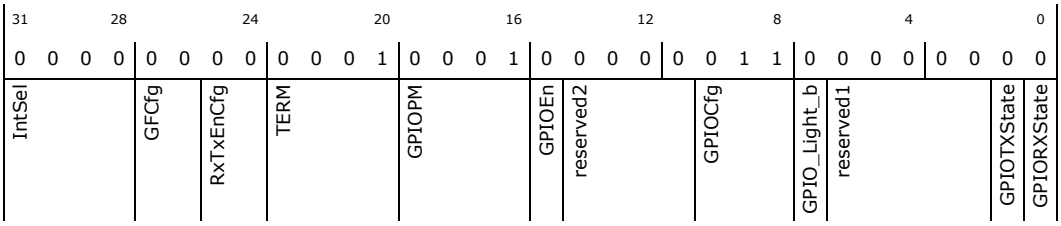
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5C30h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.136 Pad Control Register 1 (GP_SSP_2_FS_PAD_CFG1)—Offset 5C34h

Pad Control Register 1

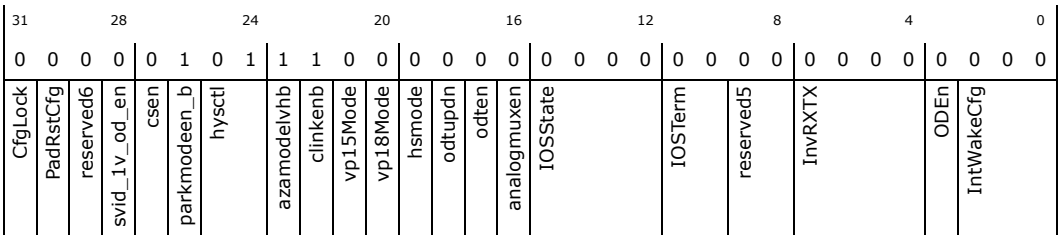
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5C34h

Op Codes:
h - Read, h - Write

Default: 05C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.7.137 Pad Control Register 0 (GP_SSP_2_TXD_PAD_CFG0)—Offset 5C38h

Pad Control Register 0

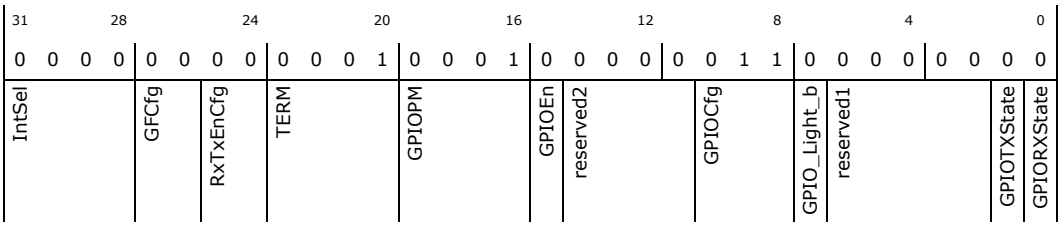
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5C38h

Op Codes:
h - Read, h - Write

Default: 00110300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x1 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.

Bit Range	Default and Access	Field Name (ID): Description
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.7.138 Pad Control Register 1 (GP_SSP_2_TXD_PAD_CFG1)—Offset 5C3Ch

Pad Control Register 1

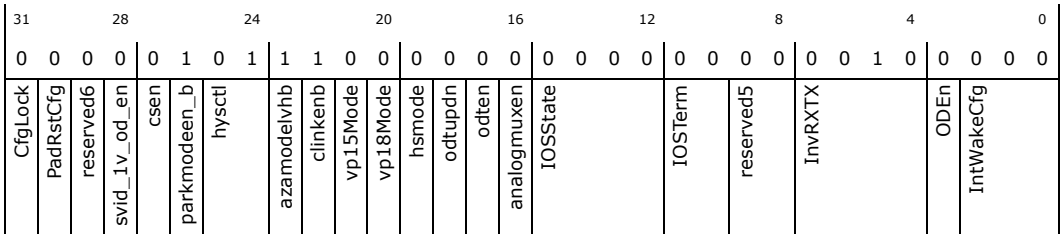
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB2] + 5C3Ch

Op Codes:
h - Read, h - Write

Default: 05C00020h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x1 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC

Bit Range	Default and Access	Field Name (ID): Description
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.8 Summary of GPIO Virtual Registers

Table 10-103.Summary of GPIO Virtual Message Bus Registers—0xB6

Offset	Register Name (Register Symbol)	Default Value
0–3h	"GPIO Read Access Control (gpio_read_access_policy_access_reg)—Offset 0h" on page 5607	FFFFFFFFh
4–7h	"GPIO Read Access Control (gpio_read_access_policy_wake_reg)—Offset 4h" on page 5607	FFFFFFFFh
8–Bh	"GPIO Read Access Control (gpio_read_access_policy_interrupt_reg)—Offset 8h" on page 5608	FFFFFFFFh
C–Fh	"GPIO Read Access Control (gpio_read_access_policy_community_reg)—Offset Ch" on page 5608	FFFFFFFFh
10–13h	"GPIO Read Access Control (gpio_read_access_policy_family_broadcast_reg)—Offset 10h" on page 5609	FFFFFFFFh
14–17h	"GPIO Read Access Control (gpio_read_access_policy_family_reg)—Offset 14h" on page 5609	FFFFFFFFh
18–1Bh	"GPIO Read Access Control (gpio_read_access_policy_pad_broadcast_reg)—Offset 18h" on page 5610	FFFFFFFFh
1C–1Fh	"GPIO Read Access Control (gpio_read_access_policy_virtual_fam_regs)—Offset 1Ch" on page 5611	FFFFFFFFh
100–103h	"GPIO Write Access Control (gpio_write_access_policy_access_reg)—Offset 100h" on page 5611	FFFFFFFFh
104–107h	"GPIO Write Access Control (gpio_write_access_policy_wake_reg)—Offset 104h" on page 5612	FFFFFFFFh
108–10Bh	"GPIO Write Access Control (gpio_write_access_policy_interrupt_reg)—Offset 108h" on page 5612	FFFFFFFFh
10C–10Fh	"GPIO Write Access Control (gpio_write_access_policy_community_reg)—Offset 10Ch" on page 5613	FFFFFFFFh
110–113h	"GPIO Write Access Control (gpio_write_access_policy_family_broadcast_reg)—Offset 110h" on page 5613	FFFFFFFFh
114–117h	"GPIO Write Access Control (gpio_write_access_policy_family_reg)—Offset 114h" on page 5614	FFFFFFFFh
118–11Bh	"GPIO Write Access Control (gpio_write_access_policy_pad_broadcast_reg)—Offset 118h" on page 5615	FFFFFFFFh
11C–11Fh	"GPIO Write Access Control (gpio_write_access_policy_virtual_fam_regs)—Offset 11Ch" on page 5615	FFFFFFFFh
200–203h	"GPIO_WAKE_STATUS_REG #0 (gpio_wake_status_reg_0)—Offset 200h" on page 5616	00000000h
280–283h	"GPIO_WAKE_MASK_REG #0 (gpio_wake_mask_reg_0)—Offset 280h" on page 5617	00000000h
300–303h	"GPIO Interrupt Status (gpio_interrupt_status)—Offset 300h" on page 5617	00000000h
380–383h	"GPIO Interrupt Status (gpio_interrupt_mask)—Offset 380h" on page 5618	00000000h
1000–1003h	"GPIO Broadcast Data Mask bit Register (gpio_family_bw_mask_31_0)—Offset 1000h" on page 5619	00000000h

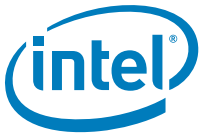


Table 10-103.Summary of GPIO Virtual Message Bus Registers—0xB6 (Continued)

Offset	Register Name (Register Symbol)	Default Value
1004–1007h	"GPIO Broadcast Data Register (gpio_family_bw_data_31_0)—Offset 1004h" on page 5619	00000000h
1008–100Bh	"gpio_family_broadcast_reg_mask #0 (gpio_family_broadcast_reg_mask_0)—Offset 1008h" on page 5620	00000000h
1080–1083h	"RCOMP Control Register (virtual_fam_family_rcomp_control_reg)—Offset 1080h" on page 5621	00941D1Dh
1084–1087h	"RCOMP Offset Register (virtual_fam_family_rcomp_offset_reg)—Offset 1084h" on page 5622	00000000h
1088–108Bh	"RCOMP Override Register (virtual_fam_family_rcomp_override_reg)—Offset 1088h" on page 5623	00110202h
108C–108Fh	"RCOMP Value Register (virtual_fam_family_rcomp_value_reg)—Offset 108Ch" on page 5624	00110202h
1090–1093h	"family_config_rcomp_reg (virtual_fam_family_config_rcomp_reg)—Offset 1090h" on page 5625	02020311h
1094–1097h	"gpio_family_configuration_register (virtual_fam_family_config_reg)—Offset 1094h" on page 5625	04C00000h
4000–4003h	"GPIO Broadcast Data Mask bit Register (gpio_pad_bw_mask_31_0)—Offset 4000h" on page 5627	00000000h
4004–4007h	"GPIO Broadcast Data Register (gpio_pad_bw_data_31_0)—Offset 4004h" on page 5627	00000000h
4008–400Bh	"GPIO Broadcast Write Enable Register (gpio_pad_bw_ctrl_31_0)—Offset 4008h" on page 5628	00000000h
4400–4403h	"Pad Control Register 0 (VIRTUAL0_PAD_CFG0)—Offset 4400h" on page 5628	00010300h
4404–4407h	"Pad Control Register 1 (VIRTUAL0_PAD_CFG1)—Offset 4404h" on page 5629	04C00000h
4408–440Bh	"Pad Control Register 0 (VIRTUAL1_PAD_CFG0)—Offset 4408h" on page 5631	00010300h
440C–440Fh	"Pad Control Register 1 (VIRTUAL1_PAD_CFG1)—Offset 440Ch" on page 5633	04C00000h
4410–4413h	"Pad Control Register 0 (VIRTUAL2_PAD_CFG0)—Offset 4410h" on page 5635	00010300h
4414–4417h	"Pad Control Register 1 (VIRTUAL2_PAD_CFG1)—Offset 4414h" on page 5636	04C00000h
4418–441Bh	"Pad Control Register 0 (VIRTUAL3_PAD_CFG0)—Offset 4418h" on page 5638	00010300h
441C–441Fh	"Pad Control Register 1 (VIRTUAL3_PAD_CFG1)—Offset 441Ch" on page 5639	04C00000h
4420–4423h	"Pad Control Register 0 (VIRTUAL4_PAD_CFG0)—Offset 4420h" on page 5641	00010300h
4424–4427h	"Pad Control Register 1 (VIRTUAL4_PAD_CFG1)—Offset 4424h" on page 5643	04C00000h
4428–442Bh	"Pad Control Register 0 (VIRTUAL5_PAD_CFG0)—Offset 4428h" on page 5645	00010300h
442C–442Fh	"Pad Control Register 1 (VIRTUAL5_PAD_CFG1)—Offset 442Ch" on page 5646	04C00000h
4430–4433h	"Pad Control Register 0 (VIRTUAL6_PAD_CFG0)—Offset 4430h" on page 5648	00010300h

Table 10-103.Summary of GPIO Virtual Message Bus Registers—0xB6 (Continued)

Offset	Register Name (Register Symbol)	Default Value
4434–4437h	"Pad Control Register 1 (VIRTUAL6_PAD_CFG1)—Offset 4434h" on page 5649	04C00000h
4438–443Bh	"Pad Control Register 0 (VIRTUAL7_PAD_CFG0)—Offset 4438h" on page 5651	00010300h
443C–443Fh	"Pad Control Register 1 (VIRTUAL7_PAD_CFG1)—Offset 443Ch" on page 5653	04C00000h

10.8.1 GPIO Read Access Control (gpio_read_access_policy_access_reg)—Offset 0h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

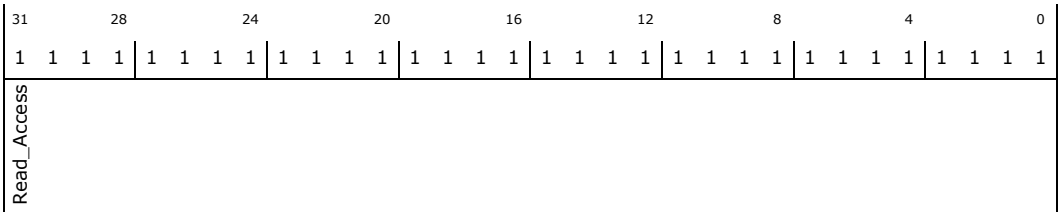
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 0h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.8.2 GPIO Read Access Control (gpio_read_access_policy_wake_reg)—Offset 4h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

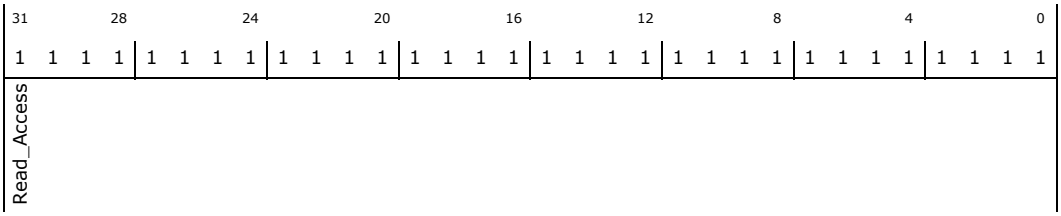
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 4h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.8.3 GPIO Read Access Control (gpio_read_access_policy_interrupt_reg)—Offset 8h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

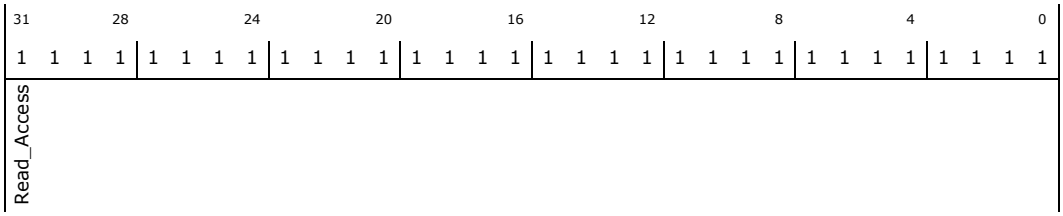
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 8h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.8.4 GPIO Read Access Control (gpio_read_access_policy_community_reg)—Offset Ch

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

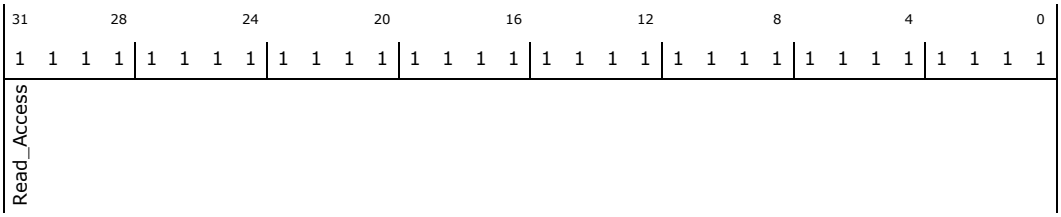
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.8.5 GPIO Read Access Control (gpio_read_access_policy_family_broadcast_reg)—Offset 10h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

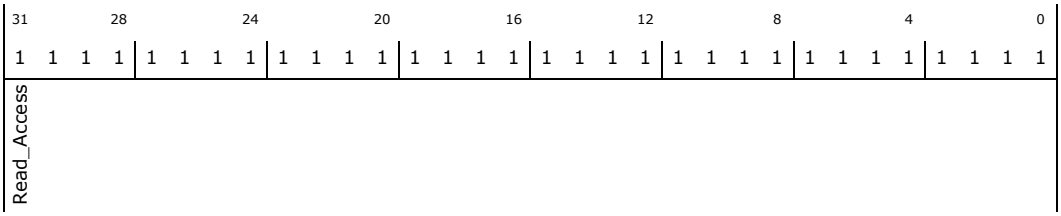
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 10h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.8.6 GPIO Read Access Control (gpio_read_access_policy_family_reg)—Offset 14h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

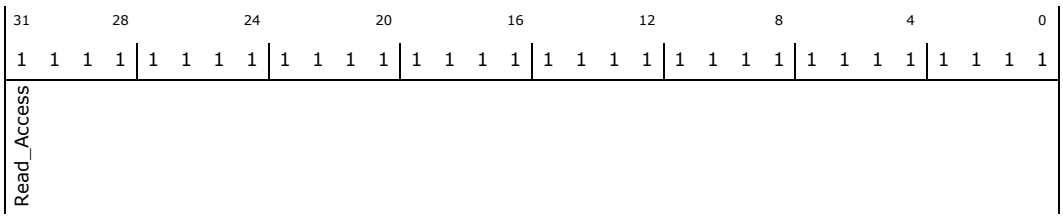
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 14h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.8.7 GPIO Read Access Control (gpio_read_access_policy_pad_broadcast_reg)—Offset 18h

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

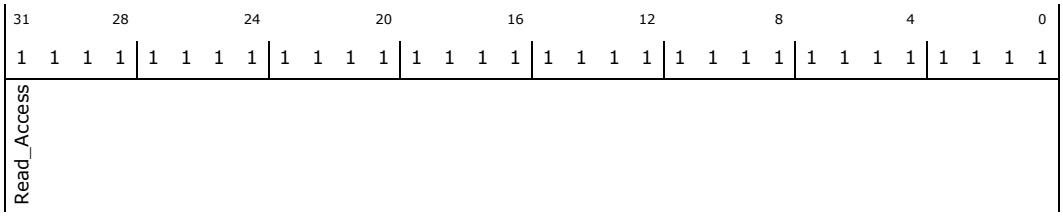
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 18h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.8.8 GPIO Read Access Control (gpio_read_access_policy_virtual_fam_regs)—Offset 1Ch

Each bit represents allows access to an initiator. On read the 1 hot decoded SAI value is compared to grant access.

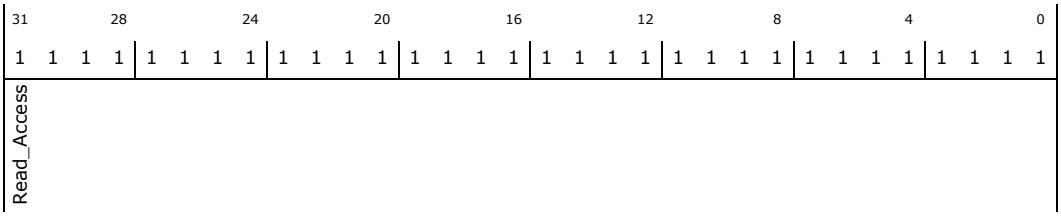
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 1Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Read_Access:** Reserved.

10.8.9 GPIO Write Access Control (gpio_write_access_policy_access_reg)—Offset 100h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

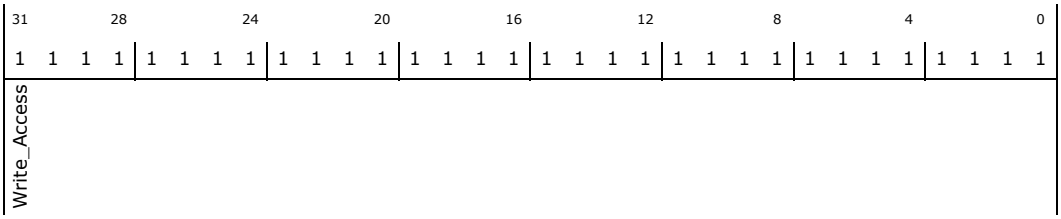
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 100h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.8.10 GPIO Write Access Control (gpio_write_access_policy_wake_reg)—Offset 104h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

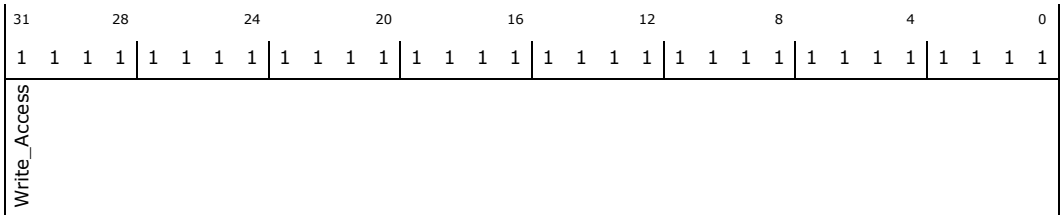
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 104h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.8.11 GPIO Write Access Control (gpio_write_access_policy_interrupt_reg)—Offset 108h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

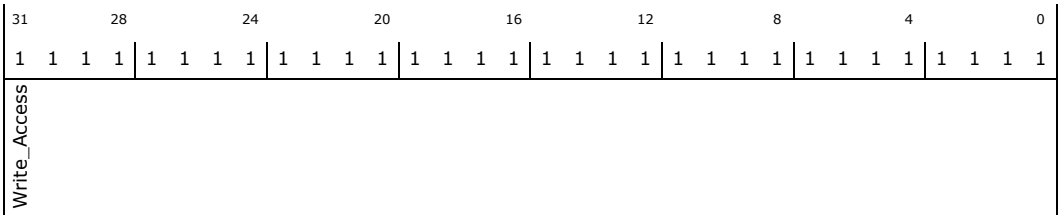
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 108h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.8.12 GPIO Write Access Control (gpio_write_access_policy_community_reg)—Offset 10Ch

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

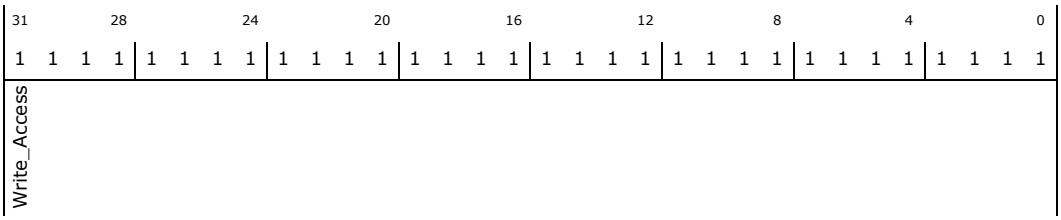
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 10Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.8.13 GPIO Write Access Control (gpio_write_access_policy_family_broadcast_reg)—Offset 110h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

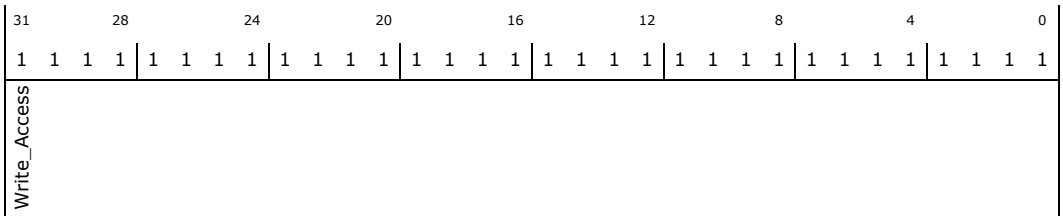
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 110h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.8.14 GPIO Write Access Control (gpio_write_access_policy_family_reg)—Offset 114h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

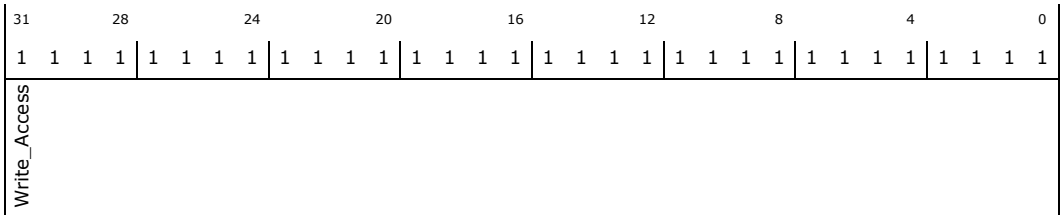
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 114h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.8.15 GPIO Write Access Control (gpio_write_access_policy_pad_broadcast_reg)—Offset 118h

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

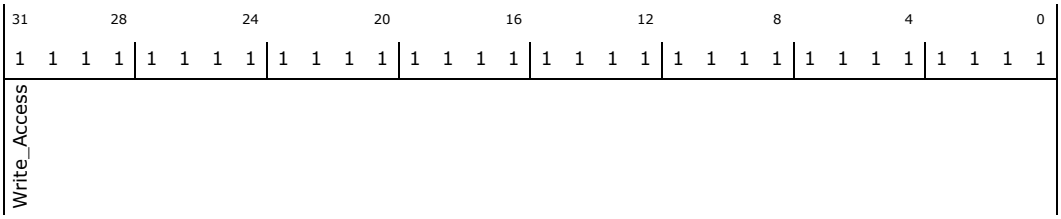
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 118h

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.8.16 GPIO Write Access Control (gpio_write_access_policy_virtual_fam_regs)—Offset 11Ch

Each bit represents allows access to an initiator. On write the 1 hot decoded SAI value is compared to grant access.

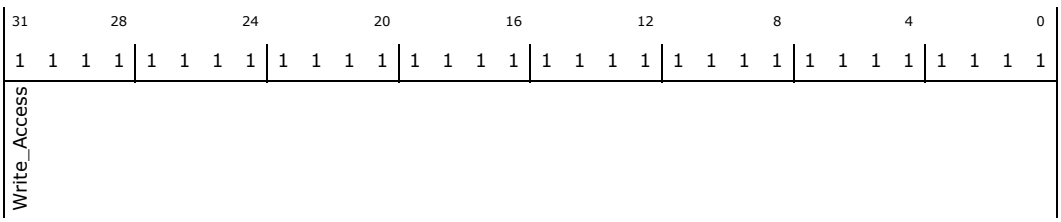
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 11Ch

Op Codes:
h - Read, h - Write

Default: FFFFFFFFh



Bit Range	Default and Access	Field Name (ID): Description
31:0	0xffffffff RW	**Write_Access:** Reserved.

10.8.17 GPIO_WAKE_STATUS_REG #0 (gpio_wake_status_reg_0)—Offset 200h

GPIO Wake Status Register write 1 to clear.

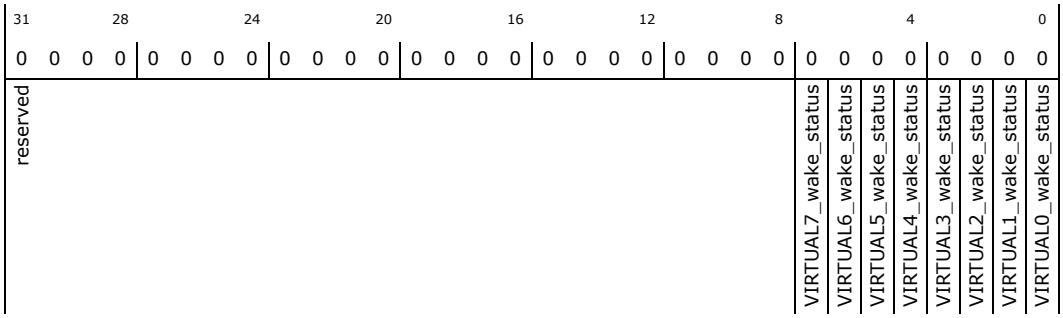
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 200h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RW	**reserved:** Reserved.
7	0x0 RW/1C	**VIRTUAL7_wake_status:** Reserved.
6	0x0 RW/1C	**VIRTUAL6_wake_status:** Reserved.
5	0x0 RW/1C	**VIRTUAL5_wake_status:** Reserved.
4	0x0 RW/1C	**VIRTUAL4_wake_status:** Reserved.
3	0x0 RW/1C	**VIRTUAL3_wake_status:** Reserved.
2	0x0 RW/1C	**VIRTUAL2_wake_status:** Reserved.
1	0x0 RW/1C	**VIRTUAL1_wake_status:** Reserved.
0	0x0 RW/1C	**VIRTUAL0_wake_status:** Reserved.

10.8.18 GPIO_WAKE_MASK_REG #0 (gpio_wake_mask_reg_0)—Offset 280h

GPIO Wake Register 0 Masks Wake.

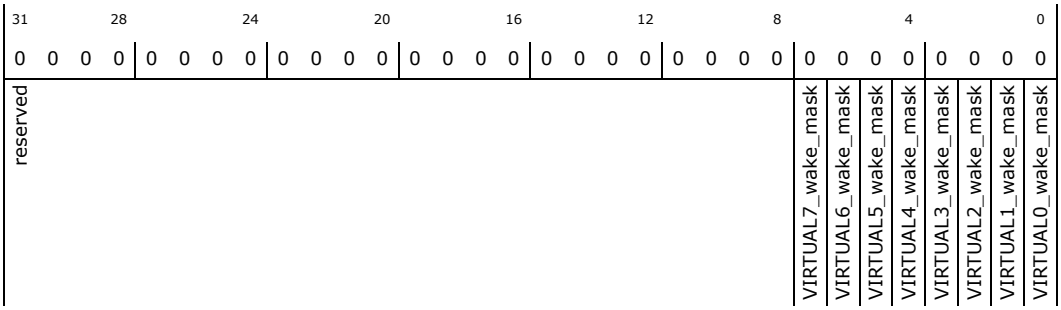
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 280h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:8	0x0 RW	**reserved:** Reserved.
7	0x0 RW	**VIRTUAL7_wake_mask:** Reserved.
6	0x0 RW	**VIRTUAL6_wake_mask:** Reserved.
5	0x0 RW	**VIRTUAL5_wake_mask:** Reserved.
4	0x0 RW	**VIRTUAL4_wake_mask:** Reserved.
3	0x0 RW	**VIRTUAL3_wake_mask:** Reserved.
2	0x0 RW	**VIRTUAL2_wake_mask:** Reserved.
1	0x0 RW	**VIRTUAL1_wake_mask:** Reserved.
0	0x0 RW	**VIRTUAL0_wake_mask:** Reserved.

10.8.19 GPIO Interrupt Status (gpio_interrupt_status)—Offset 300h

Status bits for the 16 interrupts.

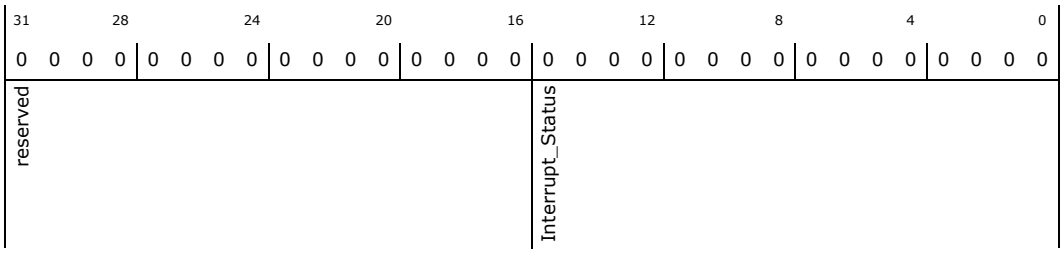
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 300h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW/1C	**reserved:** reserved
15:0	0x0 RW/1C	**Interrupt Status (Interrupt_Status):** Status bits for the 16 interrupts. Write 1 to Clear

10.8.20 GPIO Interrupt Status (gpio_interrupt_mask)—Offset 380h

Mask bits for the 16 interrupts.

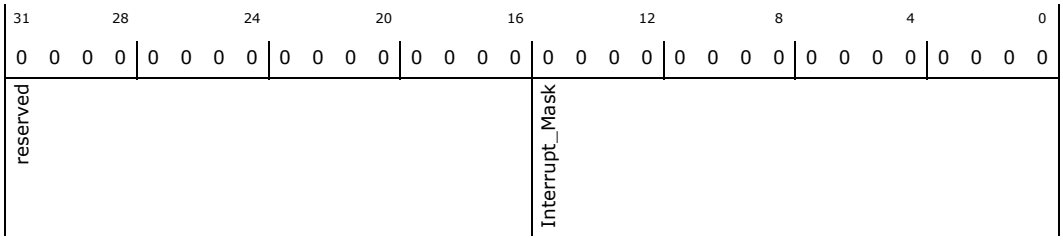
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 380h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:16	0x0 RW	**reserved:** reserved
15:0	0x0 RW	**Interrupt Mask (Interrupt_Mask):** Mask bits for the 16 interrupts. Interrupt masked when 0.

10.8.21 GPIO Broadcast Data Mask bit Register (gpio_family_bw_mask_31_0)—Offset 1000h

Write Mask that masks bit by bit the data written to BWData

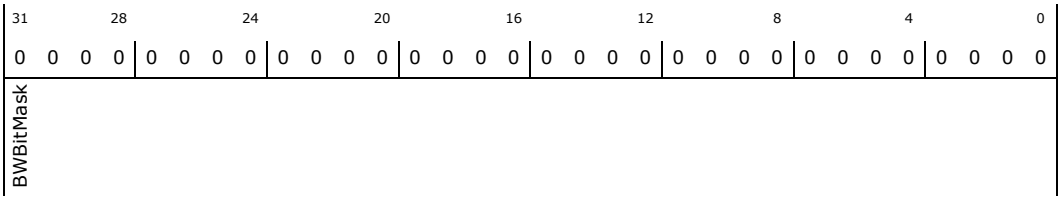
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 1000h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**BWBitMask:** Reserved.

10.8.22 GPIO Broadcast Data Register (gpio_family_bw_data_31_0)—Offset 1004h

Broadcast Write Data

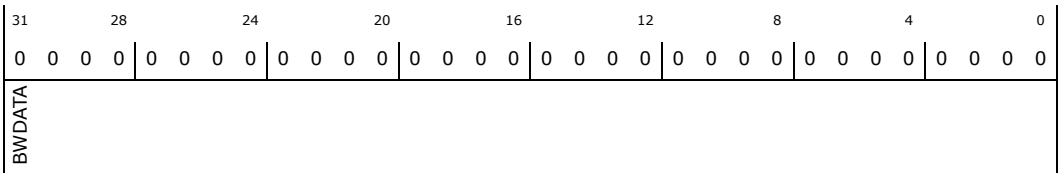
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 1004h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 WO	**BWDATA:** Reserved.

10.8.23 gpio_family_broadcast_reg_mask #0 (gpio_family_broadcast_reg_mask_0)—Offset 1008h

Family Broadcast Register Masking

Access Method

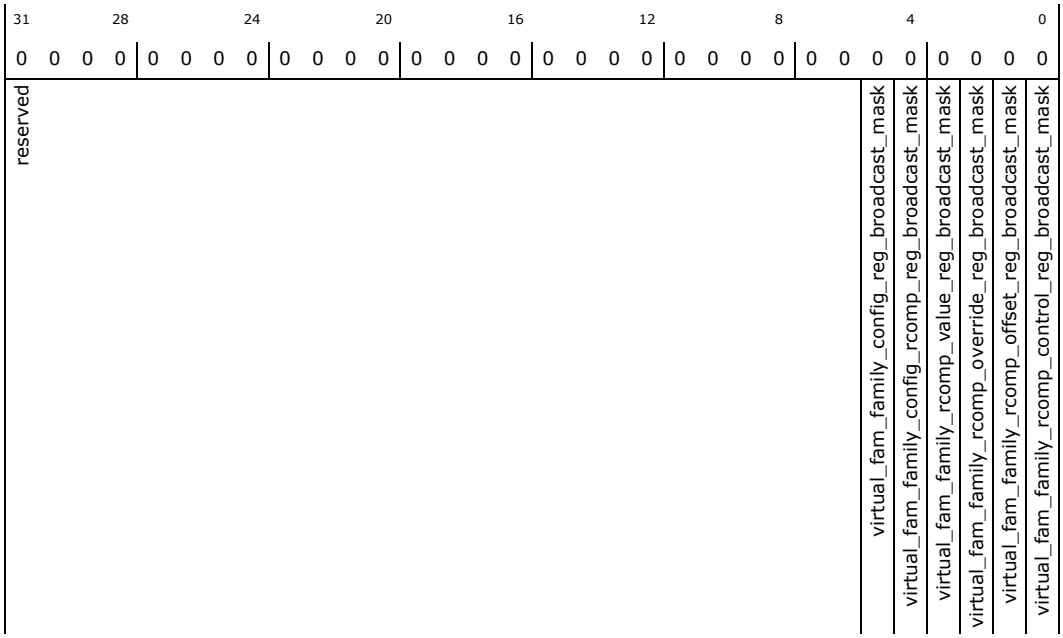
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 1008h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:6	0x0 RW	**reserved:** Reserved.
5	0x0 RW	**virtual_fam_family_config_reg_broadcast_mask:** Reserved.
4	0x0 RW	**virtual_fam_family_config_rcomp_reg_broadcast_mask:** Reserved.
3	0x0 RW	**virtual_fam_family_rcomp_value_reg_broadcast_mask:** Reserved.
2	0x0 RW	**virtual_fam_family_rcomp_override_reg_broadcast_mask:** Reserved.
1	0x0 RW	**virtual_fam_family_rcomp_offset_reg_broadcast_mask:** Reserved.
0	0x0 RW	**virtual_fam_family_rcomp_control_reg_broadcast_mask:** Reserved.

10.8.24 RCOMP Control Register (virtual_fam_family_rcomp_control_reg)—Offset 1080h

RCOMP Control Register

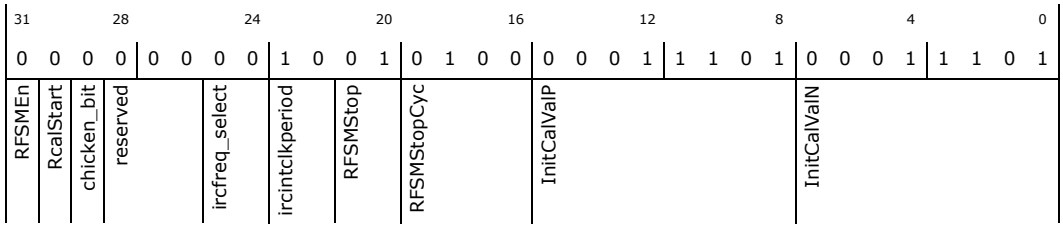
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 1080h

Op Codes:
h - Read, h - Write

Default: 00941D1Dh



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**RCOMP FSM Enable (RFSMEn):** 0 = state machine disabled (clock gated) 1 = state machine enabled It is important to have this bit enabled in order for all internal clocks inside the RCOMP FSM to run.
30	0x0 RW	**RCOMP Calibration Start (RcalStart):** When set to 1 this bit triggers the RCOMP FSM to start hunting for the correct values for strength and slew. This bit should be cleared after calibration has finished. Before setting the RcalStart bit RFSMEn must have been asserted for at least 5 clock cycles. The first calibration takes 10us to complete and subsequent calibrations take 3us. Details of this process are in the CFIP RCOMP A Specification
29	0x0 RW	**RCOMP FSM Binary Chicken Bit (chicken_bit):** Toggling this bit Simulates a V1P8 Mode change. This will allow Binary re-calibration
28:26	0x0 RW	**reserved:** reserved
25:24	0x0 RW	**IRCCLK Frequency Select (ircfreq_select):** Clock ircclk frequency. This signals indicate what frequency ircclk is. This is used for 1 ms and 10 ms counters. 00 if clk input is 25 MHz (default, and SoC Clock) 01 if 50 MHz 10 if 100 MHz 11 if 125 MHz
23:22	0x2 RW	**IRC Internal Clock Period (ircintclkperiod):** To select rcomp clock period. This is the compensation clock frequency/period. Clock is derived from ircclk (which can be 25 MHz, 50 MHz, 100 MHz or 125 MHz user must set ircfreq_select[1:0] accordingly) 00 40 ns (64 ns for ircclk=125 MHz) 01 80 ns (96 ns for ircclk=125 MHz) 10 120 ns (128 ns for ircclk=125 MHz) (default) 11 160 ns (192 ns for ircclk=125 MHz)

Bit Range	Default and Access	Field Name (ID): Description
21:20	0x1 RW	**RCOMP FSM Stop Condition (RFSMStop):** RCOMP FSM Stop calibration condition. RCOMP FSM (Pull-up and Pull-down) will finish calibrating once orcpupen/orcpdnen toggles. The toggling indicates the compensation value has been reached. This option is programmable for toggle once (single edge), toggle twice (double edge), toggle thrice (triple edge) or forcing it to finish after a certain cycle (defined by RFSMStopCyc). 00b = single edge detect (10 or 01) 01b = double edge detect (101 or 010) (default) 10b = triple edge detect (1010 or 0101) 11b = stop after x cycles (depending on ircstpcyc[3:0] value—This is meant for debug)
19:16	0x4 RW	**RCOMP FSM Stop Cycles (RFSMStopCyc):** Number of cycles to stop RCOMP FSM from searching for strength and slew settings. RFSMStop must be set to 11b for this option to take affect. 0000b = 0 cycle (illegal option) 0001b = 1 cycle (illegal option) 0010b = 2 cycles (illegal option) 0011b = 3 cycles (illegal option) 0100b = 4 cycles ... 1110b = 14 cycles 1111b = 15 cycles (maximum allowed) This is meant for debug.
15:8	0x1d RW	**Initial Pull-up Value (InitCalValP):** Initial pleg calibration value. RCOMP FSM will always start with this values for Pull-up calibration.
7:0	0x1d RW	**Initial Pull-down Value (InitCalValN):** Initial nleg calibration value. RCOMP FSM will always start with this values for Pull-down calibration.

10.8.25 RCOMP Offset Register (virtual_fam_family_rcomp_offset_reg)—Offset 1084h

RCOMP Offset Register

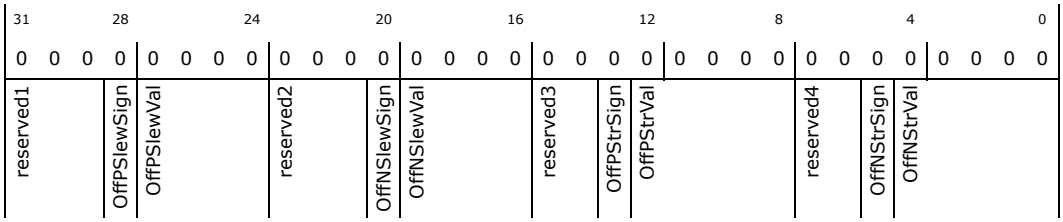
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 1084h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:29	0x0 RW	**Reserved (reserved1):** Reserved
28	0x0 RW	**Pull-up Offset Slew Sign (OffPSlewSign):** Sign Bit for PSlew Offset strength value.

Bit Range	Default and Access	Field Name (ID): Description
27:24	0x0 RW	**Pull-up Slew Offset (OffPSlewVal):** Offset slew value for pleg.
23:21	0x0 RW	**Reserved (reserved2):** Reserved
20	0x0 RW	**Pull-down Offset Slew Sign (OffNSlewSign):** Sign Bit for NSlew Offset strength value.
19:16	0x0 RW	**Pull-down Slew Offset (OffNSlewVal):** Offset slew value for nleg.
15:14	0x0 RW	**Reserved (reserved3):** Reserved
13	0x0 RW	**Pull-up Offset Strength Sign (OffPStrSign):** Sign Bit for PStrength Offset value.
12:8	0x0 RW	**Pull-up Offset Strength Value (OffPStrVal):** PStrength Offset Value.
7:6	0x0 RW	**Reserved (reserved4):** Reserved
5	0x0 RW	**Pull-down Offset Strength Sign (OffNStrSign):** Sign Bit for NStrength Offset value.
4:0	0x0 RW	**Pull-down Offset Strength Value (OffNStrVal):** NStrength Offset Value.

10.8.26 RCOMP Override Register (virtual_fam_family_rcomp_override_reg)—Offset 1088h

RCOMP Override Register

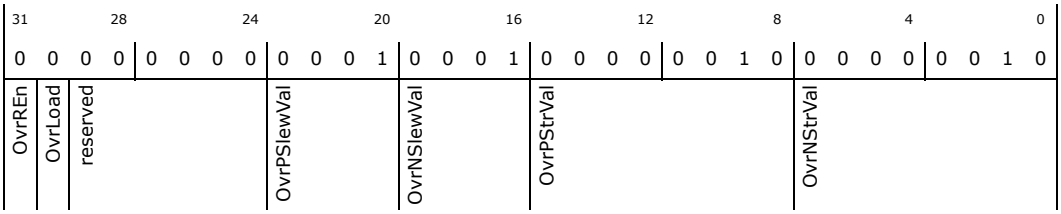
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 1088h

Op Codes:
h - Read, h - Write

Default: 00110202h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW	**Override RCOMP Enable (OvrREn):** Override enable bit to override the strength and slew values driven by the RCOMP FSM. The override values are driven through config registers. 0 = Override Disable 1 = Override Enable
30	0x0 RW	**Override Load (OvrLoad):** Load the override values into the RCOMP FSM and drive these values to the CFIO buffer. This is only valid when OvrRen = 1. 0 = Unload Values 1 = Load Values to CFIO
29:24	0x0 RW	**reserved:** reserved
23:20	0x1 RW	**Override P Slew Value (OvrPSlewVal):** Override slew values for Pull-up settings.
19:16	0x1 RW	**Override N Slew Value (OvrNSlewVal):** Override slew values for Pull-down settings.
15:8	0x2 RW	**Override Pull-up Strength Value (OvrPStrVal):** Override strength value for Pull-up settings. Should be 50ohm typical corner.
7:0	0x2 RW	**Override Pull-down Strength Value (OvrNStrVal):** Override strength value for Pull-down settings. Should be 50ohm typical corner.

10.8.27 RCOMP Value Register (virtual_fam_family_rcomp_value_reg)—Offset 108Ch

RCOMP Value Register

Access Method

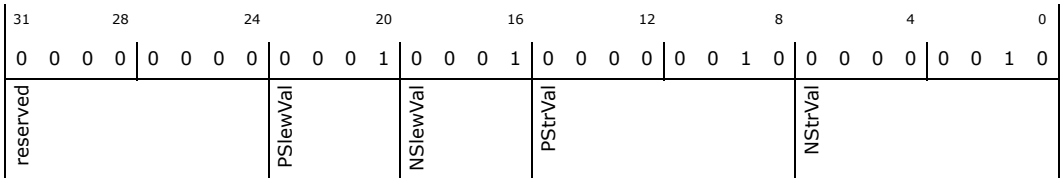
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 108Ch

Op Codes:

h - Read, h - Write

Default: 00110202h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x0 RO	**reserved_fam1 (reserved):** reserved
23:20	0x1 RO	**P Slew Value (PSlewVal):** P Slew values. Valid only after calibration is done.
19:16	0x1 RO	**N Slew Value (NSlewVal):** N Slew values. Valid only after calibration is done.

Bit Range	Default and Access	Field Name (ID): Description
15:8	0x2 RO	**Pull-up Strength Value (PStrVal):** Compensation strength for pleg. This is valid only after calibration is done.
7:0	0x2 RO	**Pull-down Strength Value (NStrVal):** Compensation strength for nleg. This is valid only after calibration is done.

10.8.28 family_config_rcomp_reg (virtual_fam_family_config_rcomp_reg)—Offset 1090h

GPIO Family RCOMP Register

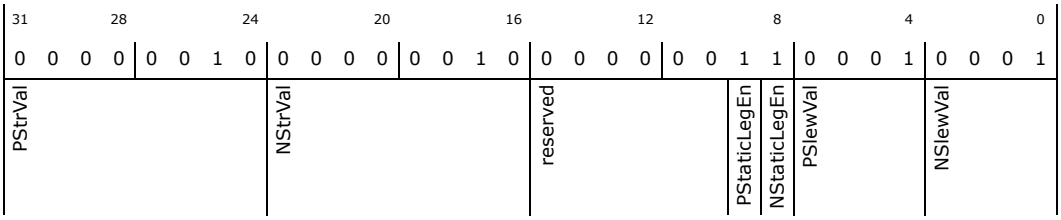
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 1090h

Op Codes:
h - Read, h - Write

Default: 02020311h



Bit Range	Default and Access	Field Name (ID): Description
31:24	0x2 RW	**Pull-up Strength Value (PStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
23:16	0x2 RW	**Pull-down Strength Value (NStrVal):** Termination strength setting for the CFIO buffer Family. Termination strength is allocated 8 bits per Pull-down and Pull-up.
15:10	0x0 RW	**reserved:** reserved
9	0x1 RW	**P Static Leg Enable (PStaticLegEn):** CFIO P Static Leg Enable
8	0x1 RW	**N Static Leg Enable (NStaticLegEn):** CFIO N Static Leg Enable
7:4	0x1 RW	**P Slew Value (PSlewVal):** Slew values for Pull-up settings.
3:0	0x1 RW	**N Slew Value (NSlewVal):** Slew values for Pull-down settings.

10.8.29 gpio_family_configuration_register (virtual_fam_family_config_reg)—Offset 1094h

GPIO Family CFIO Configuration Register

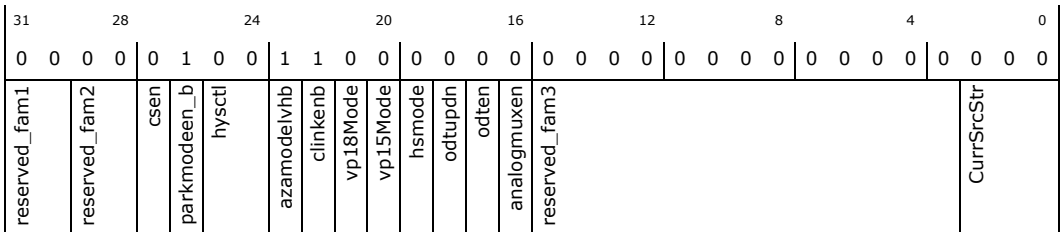
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 1094h

Op Codes:
h - Read, h - Write

Default: 04C00000h



Bit Range	Default and Access	Field Name (ID): Description
31:30	0x0 RW	**reserved_fam2 (reserved_fam1):** reserved
29:28	0x0 RW	**reserved6 (reserved_fam2):** reserved6
27	0x0 RW	**Reserved for Current Source Enable (csen):** Controlled by Pad Registers
26	0x1 RW	**Park Mode Enable Bar (parkmodeen_b):** When 0 GPIO park mode is enabled. This reduces I/O leakage a tiny amount. It should only be enabled when buffer is static value.
25:24	0x0 RW	**Hysteresis Control (hysctl):** Controls VIH to VIL hysteresis. Refer Description in CFIO HIP for values.
23	0x1 RW	**Reserved for AZAMODE active low (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLINKENB (clinkenb):** Not used on SoC
21	0x0 RW	**1.8V buffer mode (vp18Mode):** HSHV Buffers only. This should be set to 1, only when I/O is operating at 1.8V This ***must*** be 0 when I/Os are powered with the 3.3V supply to avoid EOS.
20	0x0 RW	**Reserved for V1P5MODE (vp15Mode):** Not used on SoC
19	0x0 RW	**High Speed Mode (hsmode):** For HSMV and HSHV buffers only. Enables faster operation for DFX only.
18	0x0 RW	**On Die Termination Up/Down (odtupdn):** 0 = Pull-up 1 = Pull-down.
17	0x0 RW	**On Die Termination Enable (odten):** HSMV buffers only. Enables on die termination typically 50ohm when set.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** CFIO FAMCFG Analog Mux Enable
15:3	0x0 RW	**reserved_fam3:** reserved
2:0	0x0 RW	**CurrSrcStr:** Current Source Strength configuration bits for I2C High Speed Mode. Only supported on ULPMSMV CFIO Type. Connected to crtstr[2:0] CFIO signal.

10.8.30 GPIO Broadcast Data Mask bit Register (gpio_pad_bw_mask_31_0)—Offset 4000h

Write Mask that masks bit by bit the data written to BWData

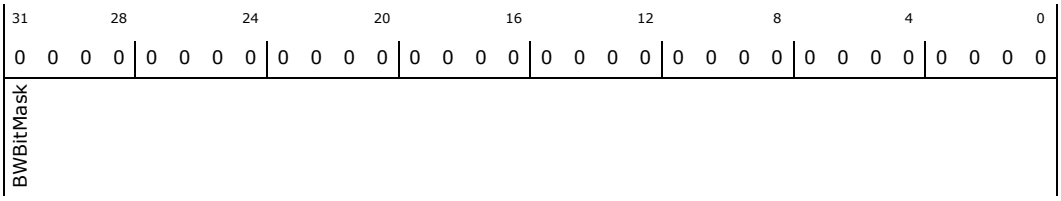
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 4000h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**BWBitMask:** Reserved.

10.8.31 GPIO Broadcast Data Register (gpio_pad_bw_data_31_0)—Offset 4004h

Broadcast Write Data

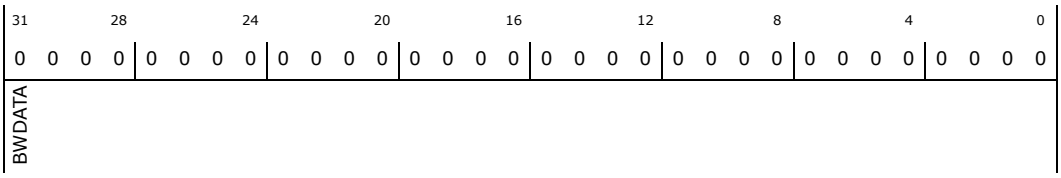
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 4004h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 WO	**BWDATA:** Reserved.

10.8.32 GPIO Broadcast Write Enable Register (gpio_pad_bw_ctrl_31_0)—Offset 4008h

32 bit Broadcast Write Enable Register

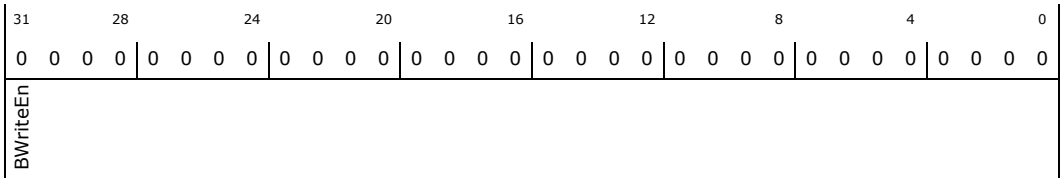
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 4008h

Op Codes:
h - Read, h - Write

Default: 00000000h



Bit Range	Default and Access	Field Name (ID): Description
31:0	0x0 RW	**BWriteEn:** Reserved.

10.8.33 Pad Control Register 0 (VIRTUAL0_PAD_CFG0)—Offset 4400h

Pad Control Register 0

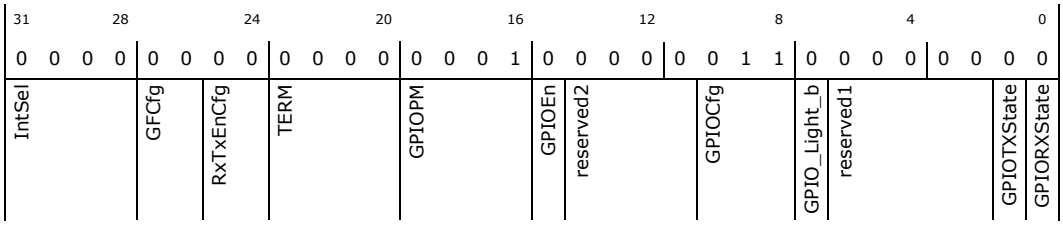
Access Method

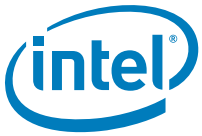
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 4400h

Op Codes:
h - Read, h - Write

Default: 00010300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.8.34 Pad Control Register 1 (VIRTUAL0_PAD_CFG1)—Offset 4404h

Pad Control Register 1

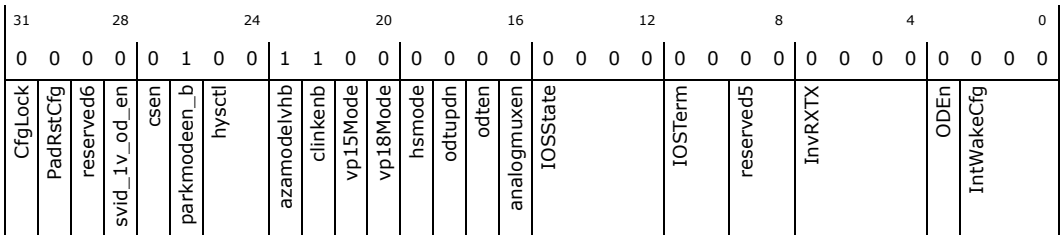
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 4404h

Op Codes:
h - Read, h - Write

Default: 04C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x0 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.8.35 Pad Control Register 0 (VIRTUAL1_PAD_CFG0)—Offset 4408h

Pad Control Register 0

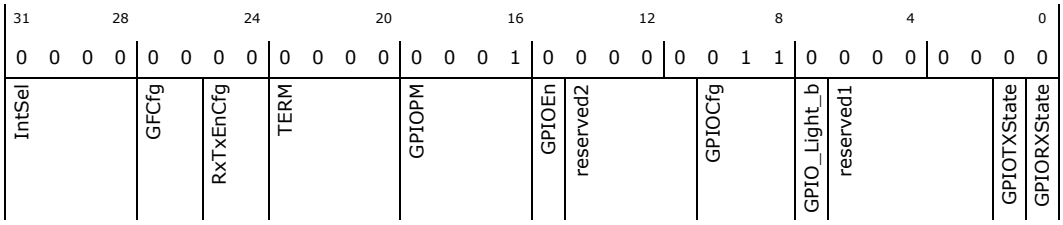
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 4408h

Op Codes:
h - Read, h - Write

Default: 00010300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.8.36 Pad Control Register 1 (VIRTUAL1_PAD_CFG1)—Offset 440Ch

Pad Control Register 1

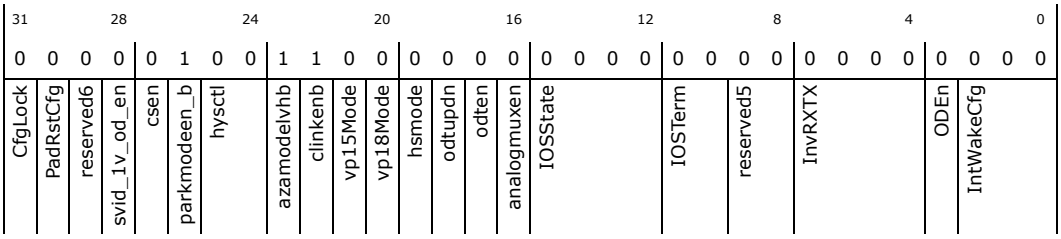
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 440Ch

Op Codes:
h - Read, h - Write

Default: 04C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x0 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.8.37 Pad Control Register 0 (VIRTUAL2_PAD_CFG0)—Offset 4410h

Pad Control Register 0

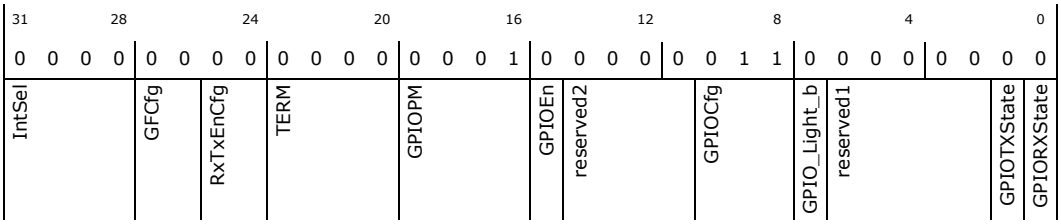
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 4410h

Op Codes:
h - Read, h - Write

Default: 00010300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.8.38 Pad Control Register 1 (VIRTUAL2_PAD_CFG1)—Offset 4414h

Pad Control Register 1

Access Method

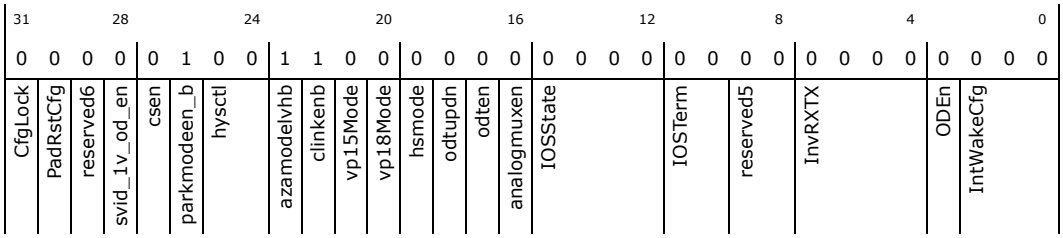
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 4414h

Op Codes:

h - Read, h - Write

Default: 04C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x0 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.8.39 Pad Control Register 0 (VIRTUAL3_PAD_CFG0)—Offset 4418h

Pad Control Register 0

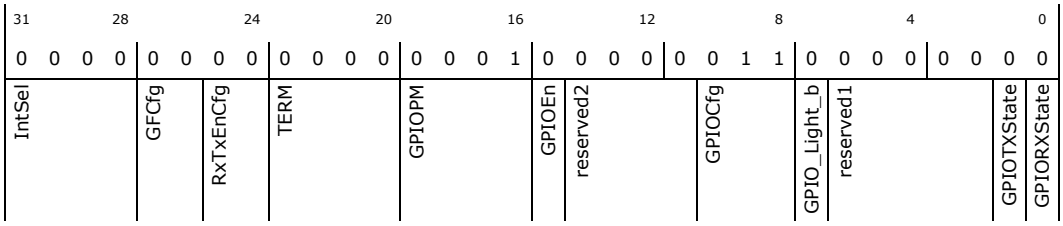
Access Method

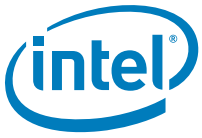
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 4418h

Op Codes:
h - Read, h - Write

Default: 00010300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.8.40 Pad Control Register 1 (VIRTUAL3_PAD_CFG1)—Offset 441Ch

Pad Control Register 1

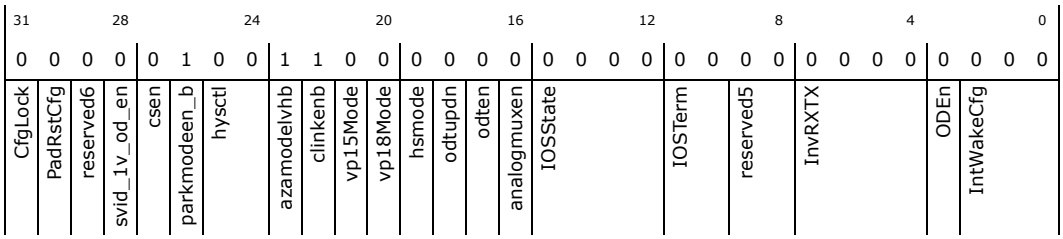
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 441Ch

Op Codes:
h - Read, h - Write

Default: 04C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x0 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.8.41 Pad Control Register 0 (VIRTUAL4_PAD_CFG0)—Offset 4420h

Pad Control Register 0

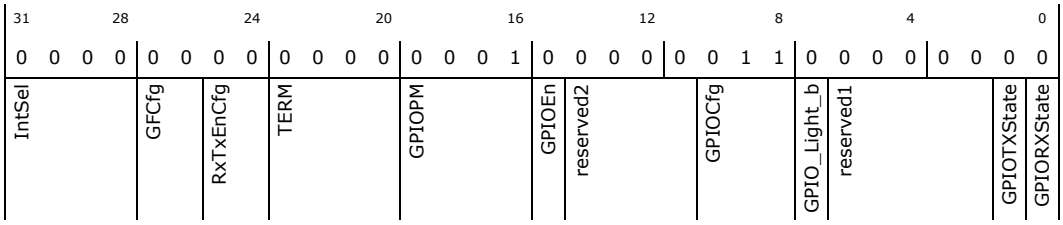
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 4420h

Op Codes:
h - Read, h - Write

Default: 00010300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.8.42 Pad Control Register 1 (VIRTUAL4_PAD_CFG1)—Offset 4424h

Pad Control Register 1

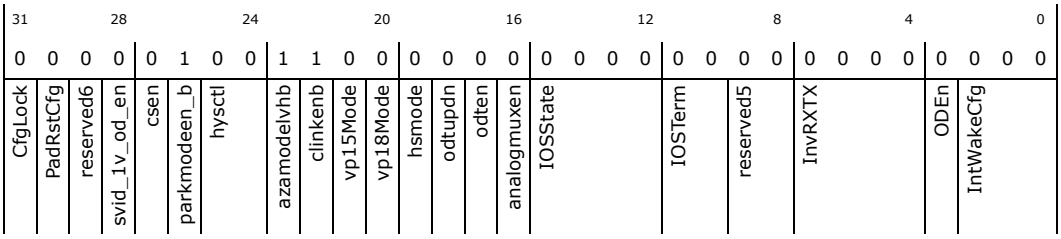
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 4424h

Op Codes:
h - Read, h - Write

Default: 04C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x0 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.8.43 Pad Control Register 0 (VIRTUAL5_PAD_CFG0)—Offset 4428h

Pad Control Register 0

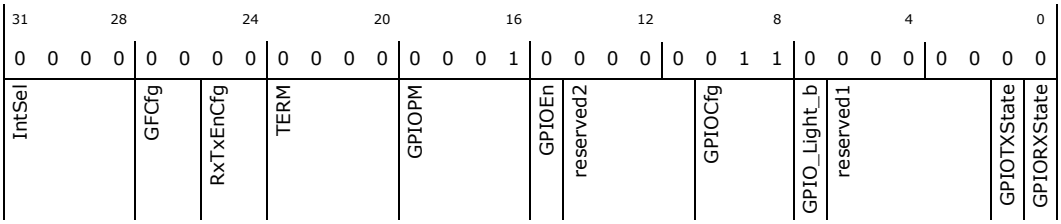
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 4428h

Op Codes:
h - Read, h - Write

Default: 00010300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled

Bit Range	Default and Access	Field Name (ID): Description
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.8.44 Pad Control Register 1 (VIRTUAL5_PAD_CFG1)—Offset 442Ch

Pad Control Register 1

Access Method

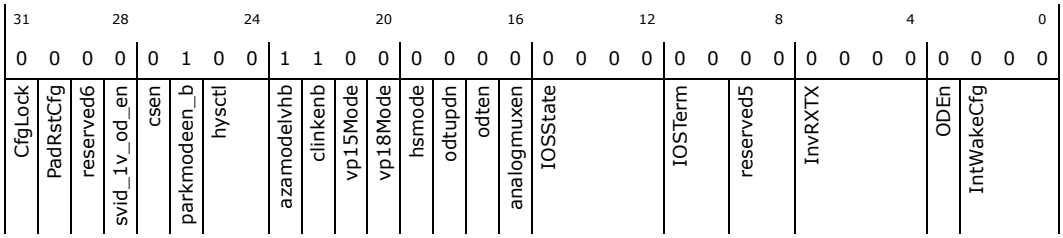
Type: Message Bus Register (Size: 32 bits)

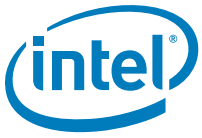
Offset: [Port: 0xB6] + 442Ch

Op Codes:

h - Read, h - Write

Default: 04C00000h





Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x0 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved

Bit Range	Default and Access	Field Name (ID): Description
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.8.45 Pad Control Register 0 (VIRTUAL6_PAD_CFG0)—Offset 4430h

Pad Control Register 0

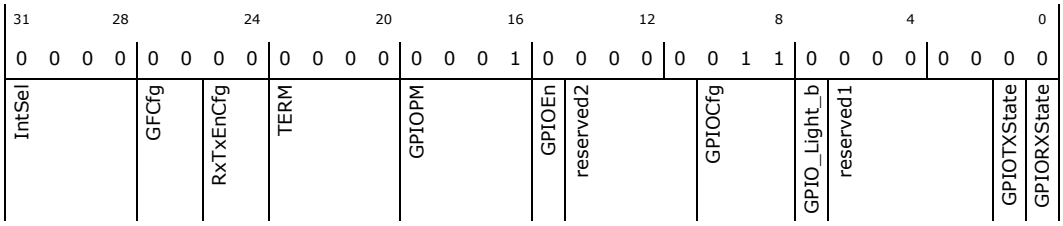
Access Method

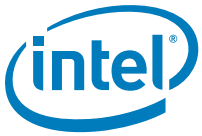
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 4430h

Op Codes:
h - Read, h - Write

Default: 00010300h





Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.8.46 Pad Control Register 1 (VIRTUAL6_PAD_CFG1)—Offset 4434h

Pad Control Register 1

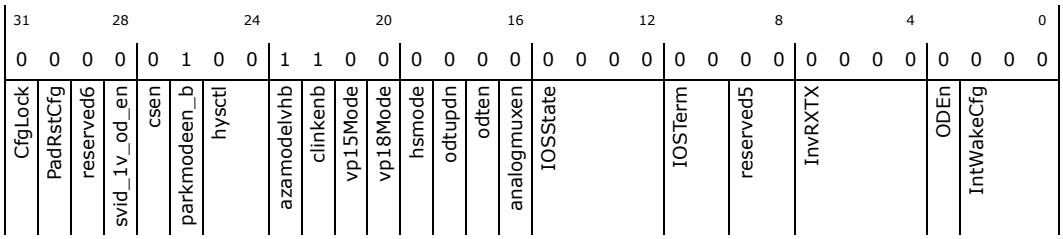
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 4434h

Op Codes:
h - Read, h - Write

Default: 04C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.
25:24	0x0 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved

10.8.47 Pad Control Register 0 (VIRTUAL7_PAD_CFG0)—Offset 4438h

Pad Control Register 0

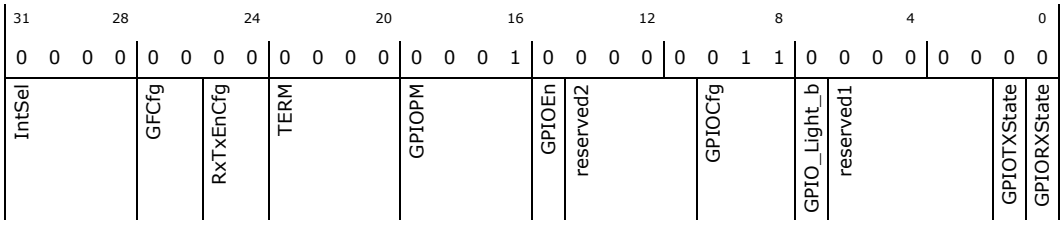
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 4438h

Op Codes:
h - Read, h - Write

Default: 00010300h



Bit Range	Default and Access	Field Name (ID): Description
31:28	0x0 RW	**Interrupt Select (IntSel):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. Only applicable when parallel wires are used for Interrupt Wire Logic with the Interrupt Steering Logic. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 15 = Interrupt Line 15
27:26	0x0 RW	**Glitch Filter Config (GFCfg):** Enable the Glitch Filter on the RX path to deglitch the incoming signal. This only makes sense when the buffer is configured as an input. 0 = Disable (Bypass the glitch filter) 1 = Enable for Edge Detect Only 2 = Enable for RX Data Only 3 = Enable for Edge Detect and RX Data
25:24	0x0 RW	**RX/TX Enable Config (RxTxEnCfg):** This field controls the Rx and Tx Buffer enables when GPIO mode is disabled 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Always Disabled 2 = Function controls TX Enable and RX Always Enabled 3 = Both TX and RX Always Enabled
23:20	0x0 RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. [3] 0=Pull-down, 1=Pull-up [2] =1K Pull-up only. MSMV only. [1] = 5K [0] = 20K
19:16	0x1 RW	**PAD Mode (GPIOPM):** This controls which function controls this particular Pad when GPIO Enable = 0.
15	0x0 RW	**GPIO Enable (GPIOEn):** This enables GPIO mode and function in Pad Mode no longer controls the Pad and the GPIO* fields control the Pad. 0 = GPIO disabled and function defined in Pad Mode controls the pad 1 = GPIO enabled and Pad Register controls the pad
14:11	0x0 RW	**reserved2:** Reserved.
10:8	0x3 RW	**GPIO Config (GPIOCfg):** 0 = GPIO (TX Enabled and RX Enabled) 1 = GPO (TX Enabled and RX Disabled) 2 = GPI (TX Disabled and RX Enabled) 3 = Hi-Z (TX Disabled and RX Disabled) Others = Reserved
7	0x0 RW	**GPIO Light Mode Bar (GPIO_Light_b):** A0 ECO - Only Enabled for PLT_CLK* pins: This mode disables the following fields and muxes function 1 directly out of the pad. (Pmode, GPIOCfg, GPIOEn, RXTXEnCfg, GFCfg, IOSState, InvRXTX, ODEn)

Bit Range	Default and Access	Field Name (ID): Description
6:2	0x0 RW	**reserved1:** Reserved.
1	0x0 RW	**GPIO TX State (GPIOTXState):** GPIO TX State is register that controls the output driven by the pad. This only applies when GPIO Config is set to enable the TX buffer.
0	0x0 RO	**GPIO Rx State (GPIORXState):** GPIO RX State, this is the current state of the PAD

10.8.48 Pad Control Register 1 (VIRTUAL7_PAD_CFG1)—Offset 443Ch

Pad Control Register 1

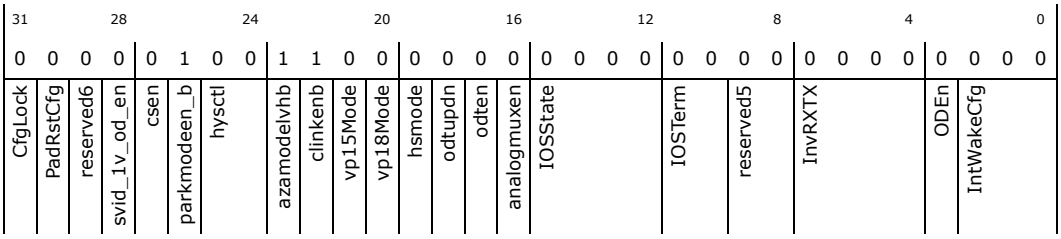
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB6] + 443Ch

Op Codes:
h - Read, h - Write

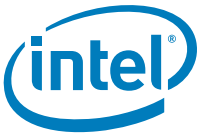
Default: 04C00000h



Bit Range	Default and Access	Field Name (ID): Description
31	0x0 RW/1L	**Configuration Lock (CfgLock):** CfgLock locks the pad from being configured for the specified fields. The following register fields will be RO when this bit is set. 0 = Unlocked 1 = Lock the following fields as RO PadRstCfg, CFIOPadCfg, IOState, IOSTerm, InvRXTX, ODEn, IntWakeCfg, IntSel, GFCfg, RXTXEnCfg, Term, Pmode, GPIOEn, GPIOCfg
30	0x0 RW	**PAD Reset Config (PadRstCfg):** This register controls which reset is used to reset the specified Pad Register fields. 0 = Powergood (that is, sticky reset) 1 = GPIO Reset (that is, warm reset)
29	0x0 RW	**reserved6:** reserved6
28	0x0 RW	**SVID 1V Open Drain Mode (svid_1v_od_en):** MSMV Buffers Only Changes VIH level to support 1V open drain mode for SVID.
27	0x0 RW	**Current Source Enable (csen):** MSMV Buffers Only Enables the Current Source for I2C HS Mode.
26	0x1 RW	**Reserved for Parkmode Enable Bar (parkmodeen_b):** Controlled by Family Register.

Bit Range	Default and Access	Field Name (ID): Description
25:24	0x0 RW	**Reserved for Hysteresis Control (hysctl):** Controlled by Family Register.
23	0x1 RW	**Reserved for AZAMODE (azamodelvhb):** Not used on SoC
22	0x1 RW	**Reserved for CLKNENB (clinkenb):** Not used on SoC
21	0x0 RW	**Reserved for 1.5V Mode (vp15Mode):** Not used on SoC
20	0x0 RW	**Reserved for 1.8V Mode (vp18Mode):** Controlled by Family Register.
19	0x0 RW	**Reserved for High Speed mode (hsmode):** Controlled by Family Register.
18	0x0 RW	**Reserved for On Die Termination Up/Down (odtupdn):** Controlled by Family Register.
17	0x0 RW	**Reserved for On Die Termination Enable (odten):** Controlled by Family Register.
16	0x0 RW	**Analog Mux Enable (analogmuxen):** Enables the analog mux at the Pad SIP
15:12	0x0 RW	**I/O Standby State (IOSState):** The I/O Standby State defines which state the pin should be parked in when the I/O is in a standby state. 0 = Latch last value driven on TX, TX Enable and RX Enable 1 = Drive 0 with RX disabled 2 = Drive 1 with RX disabled 3 = Drive 0 with RX enabled 4 = Drive 1 with RX enabled 5 = Hi-Z 6 = TX Disabled and RX Enabled (that is, wake or interrupt) Others = Reserved
11:10	0x0 RW	**I/O Standby Termination (IOSTerm):** IOSTerm defines the behavior of the termination logic when the I/O Standby state has been triggered. The value of the termination is determined in Term[2:0]. 0 = Same as state specified in Term. 1 = Disable Pull-up and Pull-down 2 = Enable Pull-down 3 = Enable Pull-up
9:8	0x0 RW	**reserved5:** Reserved.
7:4	0x0 RW	**Invert Rx Tx (InvRXTX):** These bits invert the RX/TX Data and RX/TX Enables to the CFIO buffer. Typically this is used to indicate an active high or low signal. This setting affects all modes. 0 = No Inversion 1 = Inversion Enabled [0] RX Enable [1] TX Enable [2] RX Data [3] TX Data **Note:** If GPIOEn=1, InvRxTx must be 0x0, and while GPIOEn=0 InvRxTX can either be 0x0 or 0x2 depending on function selected.
3	0x0 RW	**Open Drain Enable (ODEn):** Open Drain Enable muxes TX Data to output 0 and TX Enable is connected to TX Data. This allows only zero to be driven on the output buffer and ones are pulled up with either an external or internal Pull-up. 0 = Disabled 1 = Enabled

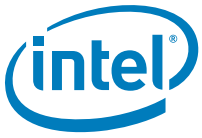
Bit Range	Default and Access	Field Name (ID): Description
2:0	0x0 RW	**Interrupt and Wake Configuration (IntWakeCfg):** Configure the edge detection logic that is used to trigger interrupts and wakes. Pad must be configured as an input. For active low level interrupts then invert the RX Data (that is, InvRXTX). 0 = Interrupt/Wake Disable (Disabled and no Pad State toggles trigger the Wake/ Interrupt logic) 1 = Falling Edge Detect Interrupt/Wake 2 = Rising Edge Detect Interrupt/Wake 3 = Falling or Rising Edge Detect Interrupt/Wake 4 = Level Interrupt/Wake (Bypass edge detect logic and Pad state is directly toggling the Wake/Interrupt logic) Others = Reserved



10.9 PCU SPI for Firmware 1 Memory Mapped I/O

Table 104. Summary of PCU SPI for Firmware 1 Memory Mapped I/O Registers—SPI_BASE_ADDRESS

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"BFPREG (BIOS_Flash_Primary_Region_bios)—Offset 0h" on page 5658	00007FFFh
4–5h	2	"HSFSTS (Hardware_Sequencing_Flash_Status_bios)—Offset 4h" on page 5658	0000h
6–7h	2	"HSFCTL (Hardware_Sequencing_Flash_Control_bios)—Offset 6h" on page 5660	0000h
8–Bh	4	"FADDR (Flash_Address_bios)—Offset 8h" on page 5661	00000000h
10–13h	4	"FDATA0 (Flash_Data_0_bios)—Offset 10h" on page 5662	00000000h
14–17h	4	"FDATA1 (Flash_Data_1_bios)—Offset 14h" on page 5662	00000000h
18–1Bh	4	"FDATA2 (Flash_Data_2_bios)—Offset 18h" on page 5663	00000000h
1C–1Fh	4	"FDATA3 (Flash_Data_3_bios)—Offset 1Ch" on page 5663	00000000h
20–23h	4	"FDATA4 (Flash_Data_4_bios)—Offset 20h" on page 5664	00000000h
24–27h	4	"FDATA5 (Flash_Data_5_bios)—Offset 24h" on page 5664	00000000h
28–2Bh	4	"FDATA6 (Flash_Data_6_bios)—Offset 28h" on page 5665	00000000h
2C–2Fh	4	"FDATA7 (Flash_Data_7_bios)—Offset 2Ch" on page 5665	00000000h
30–33h	4	"FDATA8 (Flash_Data_8_bios)—Offset 30h" on page 5666	00000000h
34–37h	4	"FDATA9 (Flash_Data_9_bios)—Offset 34h" on page 5666	00000000h
38–3Bh	4	"FDATA10 (Flash_Data_10_bios)—Offset 38h" on page 5666	00000000h
3C–3Fh	4	"FDATA11 (Flash_Data_11_bios)—Offset 3Ch" on page 5667	00000000h
40–43h	4	"FDATA12 (Flash_Data_12_bios)—Offset 40h" on page 5667	00000000h
44–47h	4	"FDATA13 (Flash_Data_13_bios)—Offset 44h" on page 5668	00000000h
48–4Bh	4	"FDATA14 (Flash_Data_14_bios)—Offset 48h" on page 5668	00000000h
4C–4Fh	4	"FDATA15 (Flash_Data_15_bios)—Offset 4Ch" on page 5669	00000000h
50–53h	4	"FRACC (Flash_Region_Access_Permissions_bios)—Offset 50h" on page 5669	00000202h
54–57h	4	"FREG0 (Flash_Region_0_bios)—Offset 54h" on page 5670	00007FFFh
58–5Bh	4	"FREG1 (Flash_Region_1_bios)—Offset 58h" on page 5671	00007FFFh
5C–5Fh	4	"FREG2 (Flash_Region_2_bios)—Offset 5Ch" on page 5672	00007FFFh
60–63h	4	"FREG3 (Flash_Region_3_bios)—Offset 60h" on page 5672	00007FFFh
64–67h	4	"FREG4 (Flash_Region_4_bios)—Offset 64h" on page 5673	00007FFFh
74–77h	4	"PR0 (Protected_Range_0_bios)—Offset 74h" on page 5674	00000000h
78–7Bh	4	"PR1 (Protected_Range_1_bios)—Offset 78h" on page 5675	00000000h
7C–7Fh	4	"PR2 (Protected_Range_2_bios)—Offset 7Ch" on page 5676	00000000h
80–83h	4	"PR3 (Protected_Range_3_bios)—Offset 80h" on page 5677	00000000h
84–87h	4	"PR4 (Protected_Range_4_bios)—Offset 84h" on page 5678	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
90–93h	4	"SSFCTLSTS (Software_Sequencing_Flash_Control_Status_bios)—Offset 90h" on page 5679	F8000000h
94–95h	2	"PREOP (Prefix_Opcode_Configuration_bios)—Offset 94h" on page 5682	0000h
96–97h	2	"OPTYPE (Opcode_Type_Configuration_bios)—Offset 96h" on page 5683	0000h
98–9Bh	4	"OPMENU0 (Opcode_Menu_Configuration_0_bios)—Offset 98h" on page 5684	00000000h
9C–9Fh	4	"OPMENU1 (Opcode_Menu_Configuration_1_bios)—Offset 9Ch" on page 5685	00000000h
A0–A3h	4	"BIOS_SCRATCHPAD (Bios_Scratchpad_Register)—Offset A0h" on page 5686	00000000h
A4–A7h	4	"LOCK (Individual_Lock_Register)—Offset A4h" on page 5687	00000000h
B0–B3h	4	"FDOC (Flash_Descriptor_Observability_Control_bios)—Offset B0h" on page 5689	00000000h
B4–B7h	4	"FDOD (Flash_Descriptor_Observability_Data_bios)—Offset B4h" on page 5690	00000000h
C0–C3h	4	"AFC (Additional_Flash_Control_bios)—Offset C0h" on page 5690	00000000h
C4–C7h	4	"VSCC0 (Lower_Vendor_Specific_Component_Capabilities_bios)—Offset C4h" on page 5691	00000000h
C8–CBh	4	"VSCC1 (Upper_Vendor_Specific_Component_Capabilities_bios)—Offset C8h" on page 5693	00000000h
CC–CFh	4	"PTINX (Parameter_Table_Index_bios)—Offset CCh" on page 5695	00000000h
D0–D3h	4	"PTDATA (Parameter_Table_Data_bios)—Offset D0h" on page 5696	00000000h
D4–D7h	4	"FPB (Flash_Partition_Boundary_bios)—Offset D4h" on page 5696	00000000h
F8–FBh	4	"SCS (SMI_Control_Status_Register_bios)—Offset F8h" on page 5697	00000080h
FC–FFh	4	"BCR (BIOS_Control_Register_bios)—Offset FCh" on page 5698	00000020h
100–103h	4	"TCGC (Trunk_Clock_Gating_Control_bios)—Offset 100h" on page 5699	00000510h

10.9.1 BFPREG (BIOS_Flash_Primary_Region_bios)—Offset 0h

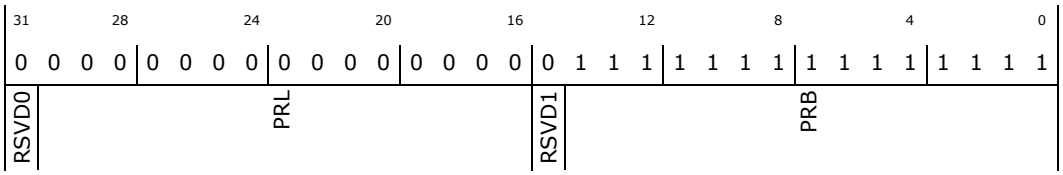
BIOS flash primary region addresses

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 0h

Default: 00007FFFh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RSVD0:** Reserved
30:16	0x0 RO	**BIOS Flash Primary Region Limit (PRL):** This specifies address bits 26:12 for the Primary Region Limit. The value in this register loaded from the contents in the Flash Descriptor.FLREG1.Region Limit **Power Well:** EPW
15	0x0 RO	**RSVD1:** Reserved
14:0	0x7fff RO	**BIOS Flash Primary Region Base (PRB):** This specifies address bits 26:12 for the Primary Region Base The value in this register iloaded from the contents in the Flash Descriptor.FLREG1.Region Base **Power Well:** EPW

10.9.2 HSFSTS (Hardware_Sequencing_Flash_Status_bios)—Offset 4h

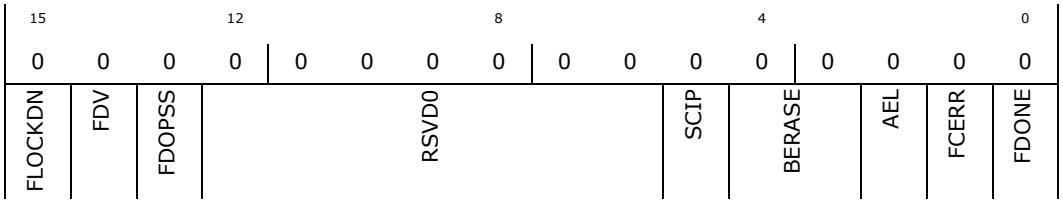
Hardware sequencing flash status Note: If operating in Non-Descriptor mode, the Software Sequencing Flash Status register must be used.

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [SPI_BASE_ADDRESS] + 4h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW/L	**Flash Configuration Lock-Down (FLOCKDN):** When set to 1, those Flash Program Registers that are locked down by this FLOCKDN bit cannot be written. Once set to 1, this bit can only be cleared by a hardware reset. **Power Well:** EPW
14	0x0 RO	**Flash Descriptor Valid (FDV):** This bit is set to a 1 if the Flash Controller read the correct Flash Descriptor Signature. If the Flash Descriptor Valid bit is not 1 , software cannot use the Hardware Sequencing registers, but must use the software sequencing registers. Any attempt to use the Hardware Sequencing registers will result in the FCERR bit being set. **Power Well:** EPW
13	0x0 RO	**Flash Descriptor Override Pin-Strap Status (FDOPSS):** This register reflects the value the Flash Descriptor Override Pin-Strap. '1': No override '0': The Flash Descriptor Overide strap is set **Power Well:** EPW
12:6	0x0 RO	**RSVD0:** Reserved
5	0x0 RO	**SPI Cycle In Progress (SCIP):** Hardware sets this bit when software sets the Flash Cycle Go (FGO) bit in the Hardware Sequencing Flash Control register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0. **Power Well:** EPW
4:3	0x0 RO	**Block/Sector Erase Size (BERASE):** This field identifies the erasable sector size for all Flash components. Valid Bit Settings: 00 : 256 Byte 01 : 4K Byte 10 : 8K Byte 11 : 64K Byte If the FLA (FPBA then this field reflects the value in the VSCC0.LBES register. If the FLA)= FPBA then this field reflects the value in the VSCC1.UBES register. **Power Well:** EPW
2	0x0 RW/1C	**Access Error Log (AEL):** Hardware sets this bit to a 1 when a direct read was made by BIOS that violated the security restrictions. Or , when a SB transaction to read/write one of the BIOS registers was accepted with bad SAI - see security table. This bit has no affect on indirect accesses. This bit is cleared by software writing a 1. **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW/1C	**Flash Cycle Error (FCERR):** Hardware sets this bit to 1 when an program register access is blocked to the FLASH due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or until hardware reset occures. Software must clear this bit before setting the FLASH Cycle GO bit in this register. **Power Well:** EPW
0	0x0 RW/1C	**Flash Cycle Done (FDONE):** The SPI controller sets this bit to 1 when the SPI Cycle completes after software previously set the FGO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access. **Power Well:** EPW

10.9.3 HSFCTL (Hardware_Sequencing_Flash_Control_bios)—Offset 6h

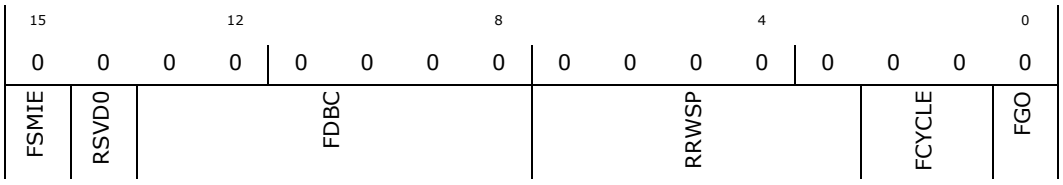
Hardware sequencing flash control.

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [SPI_BASE_ADDRESS] + 6h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Flash SPI SMI# Enable (FSMIE):** When set to 1, the SPI asserts an SMI# request whenever the Flash Cycle Done bit is 1. **Power Well:** EPW
14	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:8	0x0 RW	**Flash Data Byte Count (FDBC):** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The contents of this register are 0s based with 0b reprenting 1 byte and 111111b representing 64 bytes. The number of bytes transferred is the value of this field plus 1. This field is ignored for the Block Erase command. **Power Well:** EPW
7:3	0x0 RW	**Reserved RW Scratch Pad (RRWSP):** Reserved: Scratch Pad bits that are R/W to be used during ECO **Power Well:** EPW
2:1	0x0 RW	**FLASH Cycle (FCYCLE):** This field defines the Flash SPI cycle type generated to the FLASH when the FGO bit is set as defined below: 00 Read (1 up to 64 bytes by setting FDBC) 01 Reserved 10 Write (1 up to 64 bytes by setting FDBC) 11 Block Erase Implementation Note: if reserved 2'b01 is programmed to this field, flash controller will handle it as if it is 00 (Read) **Power Well:** EPW
0	0x0 RW/SE	**Flash Cycle Go (FGO):** A write to this register with a 1 in this bit initiates a request to the Flash SPI Arbiter to start a cycle. This register is cleared by hardware when the cycle is granted by the SPI arbiter to run the cycle on the SPI bus. When the cycle is complete, the FDONE bit is set. Software is forbidden to write to any register in the HSFLCTL register between the FGO bit getting set and the FDONE bit being cleared. Any attempt to violate this rule will be ignored by hardware. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write. This bit always returns 0 on reads. **Power Well:** EPW

10.9.4 FADDR (Flash_Address_bios)—Offset 8h

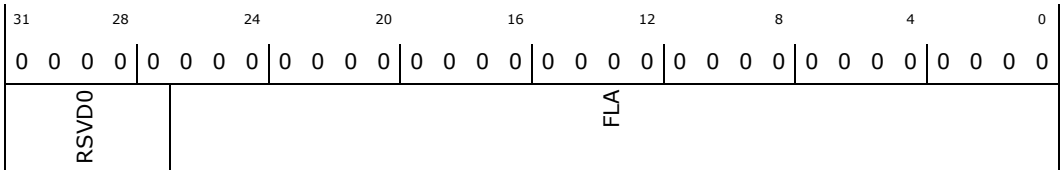
Flash address

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RSVD0:** Reserved
26:0	0x0 RW	**Flash Linear Address (FLA):** The FLA is the starting byte linear address of a SPI Read or Write cycle or an address within a Block for the Block Erase command. The Flash Linear Address must fall within a region for which BIOS has access permissions. Hardware must convert the FLA into a Flash Physical Address (FPA) before running this cycle on the SPI bus. Only 24 bits are used for the SPI address (3 Byte address mode only). **Power Well:** EPW

10.9.5 FDATA0 (Flash_Data_0_bios)—Offset 10h

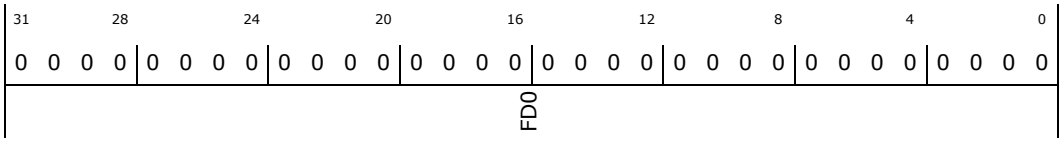
Flash data #0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 0 (FD0):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- 8-23-22- 16-31 24 Bit 24 is the last bit shifted out/in. There are no alignment assumptions, byte 0 always represents the value specified by the cycle address. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register. **Power Well:** EPW

10.9.6 FDATA1 (Flash_Data_1_bios)—Offset 14h

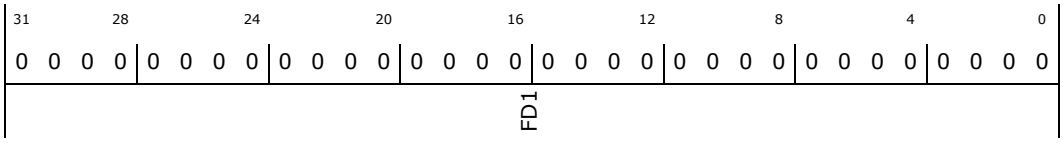
Flash data #1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 1 (FD1):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD0 has completely shifted in/out. **Power Well:** EPW

10.9.7 FDATA2 (Flash_Data_2_bios)—Offset 18h

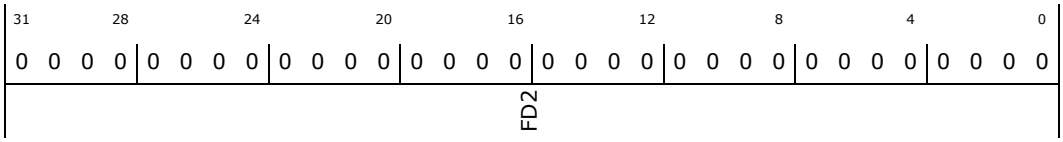
Flash data #2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 18h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 2 (FD2):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD1 has completely shifted in/out. **Power Well:** EPW

10.9.8 FDATA3 (Flash_Data_3_bios)—Offset 1Ch

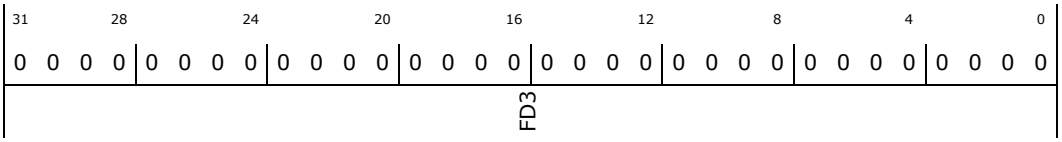
Flash data #3

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 1Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 3 (FD3):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD2 has completely shifted in/out. **Power Well:** EPW

10.9.9 FDATA4 (Flash_Data_4_bios)—Offset 20h

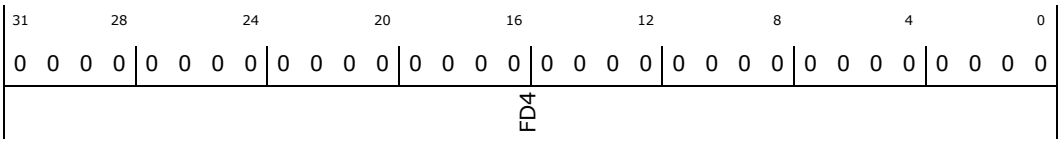
Flash data #4

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 20h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 4 (FD4):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD3 has completely shifted in/out. **Power Well:** EPW

10.9.10 FDATA5 (Flash_Data_5_bios)—Offset 24h

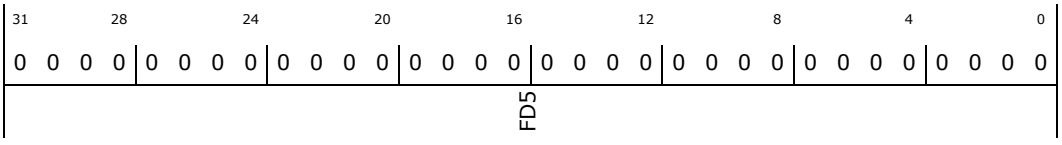
Flash data #5

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 24h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 5 (FD5):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD4 has completely shifted in/out. **Power Well:** EPW

10.9.11 FDATA6 (Flash_Data_6_bios)—Offset 28h

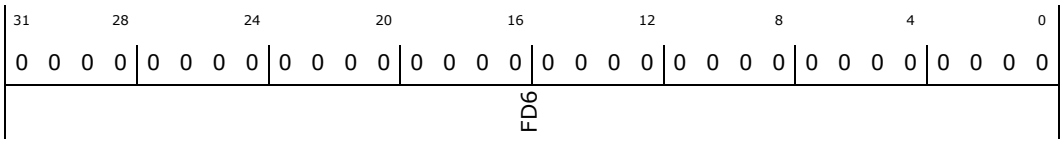
Flash data #6

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 28h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 6 (FD6):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD5 has completely shifted in/out. **Power Well:** EPW

10.9.12 FDATA7 (Flash_Data_7_bios)—Offset 2Ch

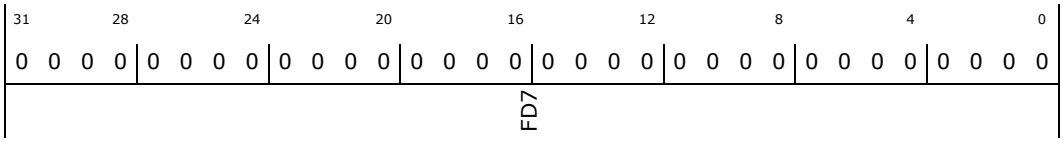
Flash data #7

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 7 (FD7):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD6 has completely shifted in/out. **Power Well:** EPW

10.9.13 FDATA8 (Flash_Data_8_bios)—Offset 30h

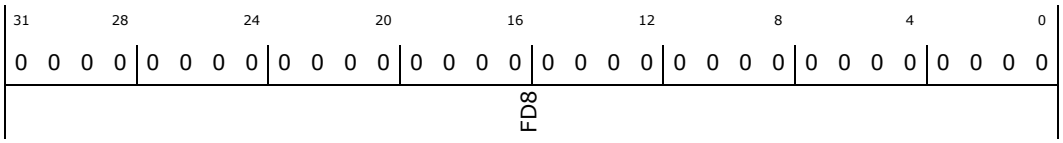
Flash data #8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 8 (FD8):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD7 has completely shifted in/out. **Power Well:** EPW

10.9.14 FDATA9 (Flash_Data_9_bios)—Offset 34h

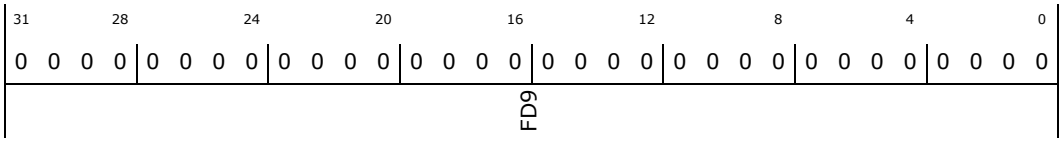
Flash data #9

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 9 (FD9):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD8 has completely shifted in/out. **Power Well:** EPW

10.9.15 FDATA10 (Flash_Data_10_bios)—Offset 38h

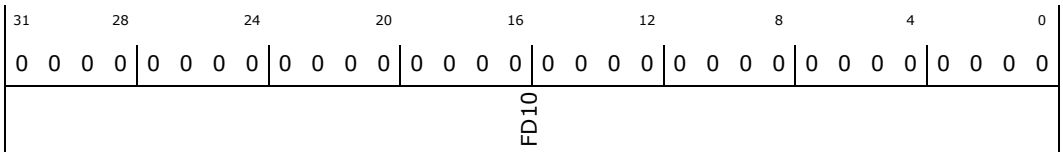
Flash data #10

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 38h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 10 (FD10):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD9 has completely shifted in/out. **Power Well:** EPW

10.9.16 FDATA11 (Flash_Data_11_bios)—Offset 3Ch

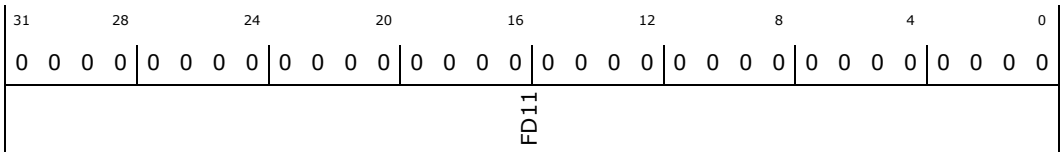
Flash data #11

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 3Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 11 (FD11):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD10 has completely shifted in/out. **Power Well:** EPW

10.9.17 FDATA12 (Flash_Data_12_bios)—Offset 40h

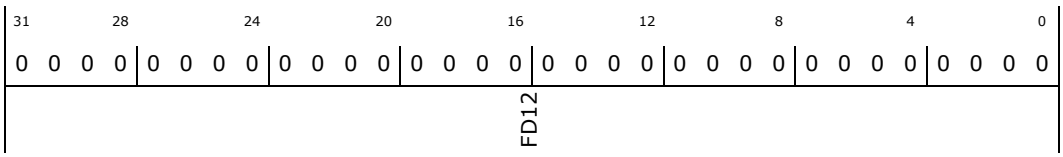
Flash data #12

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 40h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 12 (FD12):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD11 has completely shifted in/out. **Power Well:** EPW

10.9.18 FDATA13 (Flash_Data_13_bios)—Offset 44h

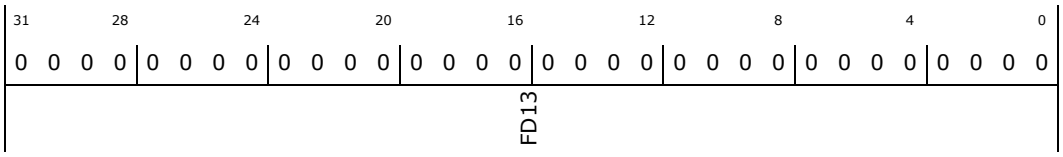
Flash data #13

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 44h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 13 (FD13):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD12 has completely shifted in/out. **Power Well:** EPW

10.9.19 FDATA14 (Flash_Data_14_bios)—Offset 48h

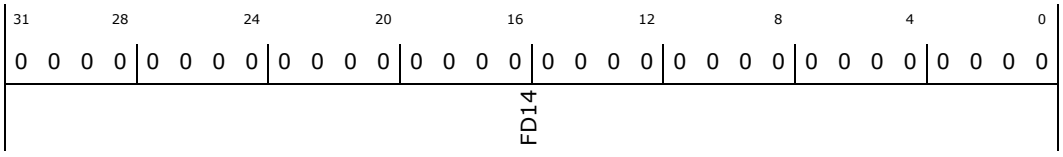
Flash data #14

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 48h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 14 (FD14):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD13 has completely shifted in/out. **Power Well:** EPW

10.9.20 FDATA15 (Flash_Data_15_bios)—Offset 4Ch

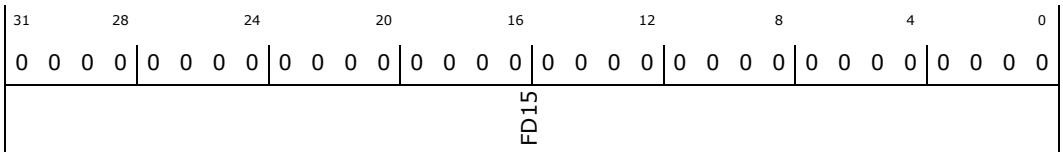
Flash data #15

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 15 (FD15):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD14 has completely shifted in/out. **Power Well:** EPW

10.9.21 FRACC (Flash_Region_Access_Permissions_bios)—Offset 50h

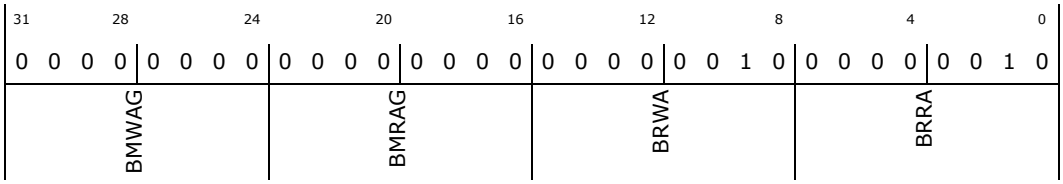
Flash region access permissions

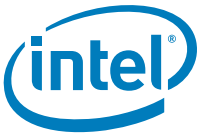
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 50h

Default: 00000202h





Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW/L	**BIOS Master Write Access Grant (BMWAG):** Each bit [lb]31:24[rb] corresponds to Master[lb]7:0[rb]. BIOS can grant one or more masters write access to the BIOS region 1 overriding the permissions in the Flash Descriptor. Master[lb]1[rb] is Host CPU/BIOS, Master[lb]2[rb] is SEC, Master[lb]0[rb] and Master[lb]7:4[rb] are reserved. The contents of this register are locked by the FLOCKDN or BMWAGLOCKDN bits. **Power Well:** EPW
23:16	0x0 RW/L	**BIOS Master Read Access Grant (BMRAG):** Each bit [lb]23:16[rb] corresponds to Master[lb]7:0[rb]. BIOS can grant one or more masters read access to the BIOS region 1 overriding the read permissions in the Flash Descriptor. Master[lb]1[rb] is Host CPU/BIOS, Master[lb]2[rb] is SEC, Master[lb]0[rb] and Master[lb]7:4[rb] are reserved. The contents of this register are locked by the FLOCKDN or BMRAGLOCKDN bit. **Power Well:** EPW
15:8	0x2 RO	**BIOS Region Write Access (BRWA):** Each bit [lb]15:8[rb] corresponds to Regions [lb]7:0[rb]. If the bit is set, this master can erase and write that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Write Access OR a particular master has granted BIOS write permissions in their Master Write Access Grant register OR the Flash Descriptor Security Override strap is set. BIOS always have the write access to its own Region 1 by default. Thus, the reset default of this field will be read as 8'h02 regardless of descriptor or non-descriptor mode. **Power Well:** EPW
7:0	0x2 RO	**BIOS Region Read Access (BRRA):** Each bit [lb]7:0[rb] corresponds to Regions [lb]7:0[rb]. If the bit is set, this master can read that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Write Access OR a particular master has granted BIOS read permissions in their Master Read Access Grant register OR the Flash Descriptor Security Override strap is set. BIOS always have the read access to its own Region 1 by default. Thus, the reset default of this field will be read as 8'h02 regardless of descriptor or non-descriptor mode. **Power Well:** EPW

10.9.22 FREG0 (Flash_Region_0_bios)—Offset 54h

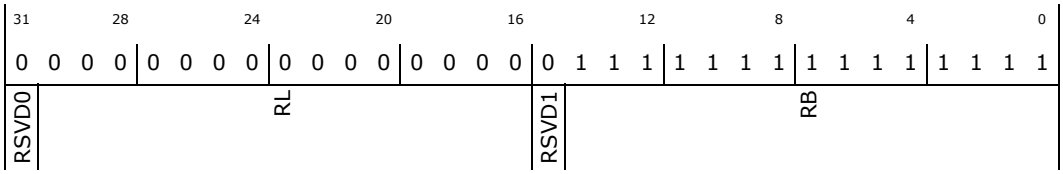
Flash region 0 (flash descriptor)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 54h

Default: 00007FFFh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RSVD0:** Reserved
30:16	0x0 RO	**Region Limit (RL):** This specifies address bits 26:12 for the Region 0 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Limit **Power Well:** EPW
15	0x0 RO	**RSVD1:** Reserved
14:0	0x7fff RO	**Region Base (RB):** This specifies address bits 26:12 for the Region 0 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Base **Power Well:** EPW

10.9.23 FREG1 (Flash_Region_1_bios)—Offset 58h

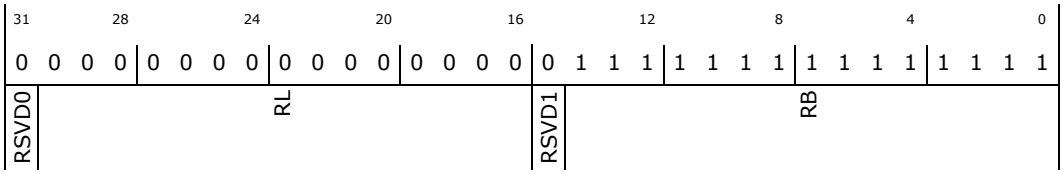
Flash region 1 (BIOS)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 58h

Default: 00007FFFh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RSVD0:** Reserved
30:16	0x0 RO	**Region Limit (RL):** This specifies address bits 26:12 for the Region 1 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**RSVD1:** Reserved
14:0	0x7fff RO	**Region Base (RB):** This specifies address bits 26:12 for the Region 1 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base **Power Well:** EPW

10.9.24 FREG2 (Flash_Region_2_bios)—Offset 5Ch

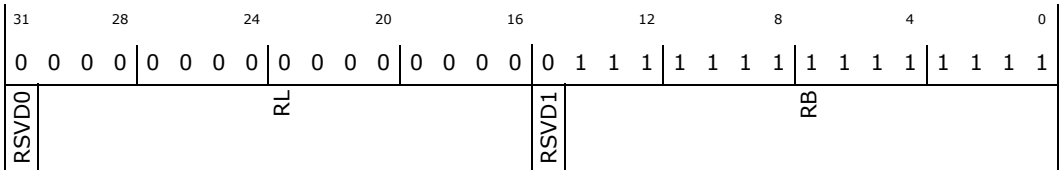
Flash region 2 (SEC)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 5Ch

Default: 00007FFFh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RSVD0:** Reserved
30:16	0x0 RO	**Region Limit (RL):** This specifies address bits 26:12 for the Region 2 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Limit **Power Well:** EPW
15	0x0 RO	**RSVD1:** Reserved
14:0	0x7fff RO	**Region Base (RB):** This specifies address bits 26:12 for the Region 2 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Base **Power Well:** EPW

10.9.25 FREG3 (Flash_Region_3_bios)—Offset 60h

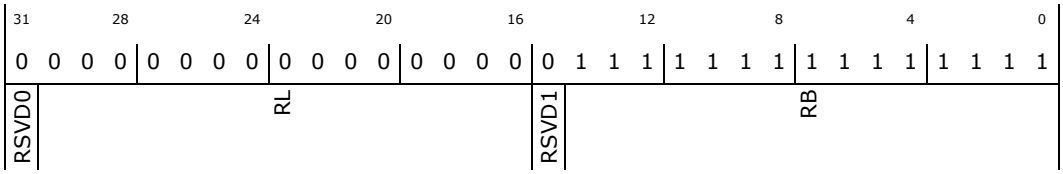
Flash region 3

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 60h

Default: 00007FFFh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RSVD0:** Reserved
30:16	0x0 RO	**Region Limit (RL):** This specifies address bits 26:12 for the Region 3 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Limit **Power Well:** EPW
15	0x0 RO	**RSVD1:** Reserved
14:0	0x7fff RO	**Region Base (RB):** This specifies address bits 26:12 for the Region 3 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Base **Power Well:** EPW

10.9.26 FREG4 (Flash_Region_4_bios)—Offset 64h

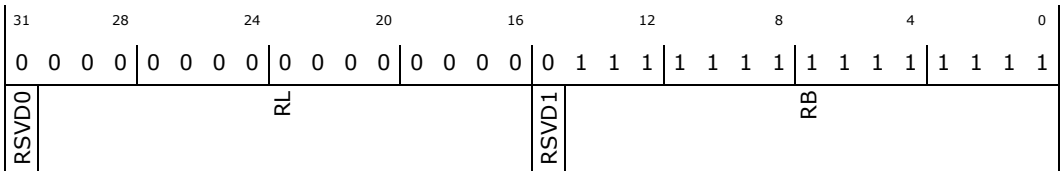
Flash region 4 (platform data)

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 64h

Default: 00007FFFh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
30:16	0x0 RO	**Region Limit (RL):** This specifies address bits 26:12 for the Region 4 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Limit **Power Well:** EPW
15	0x0 RO	**RSVD1:** Reserved
14:0	0x7fff RO	**Region Base (RB):** This specifies address bits 26:12 for the Region 4 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Base **Power Well:** EPW

10.9.27 PR0 (Protected_Range_0_bios)—Offset 74h

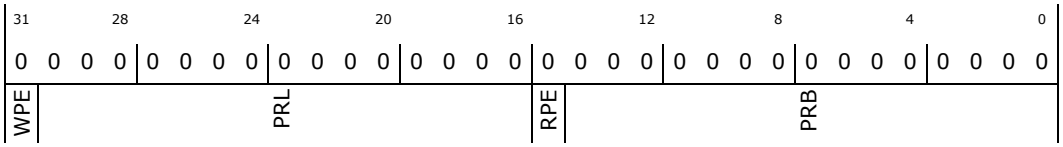
Protected range #0. This register can not be written when the FLOCKDN bit is set to 1.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 74h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the PR0LOCKDN bit of the LOCK register. **Power Well:** EPW
30:16	0x0 RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the PR0LOCKDN bit of the LOCK register. **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the PR0LOCKDN bit of the LOCK register. **Power Well:** EPW
14:0	0x0 RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the PR0LOCKDN bit of the LOCK register. **Power Well:** EPW

10.9.28 PR1 (Protected_Range_1_bios)—Offset 78h

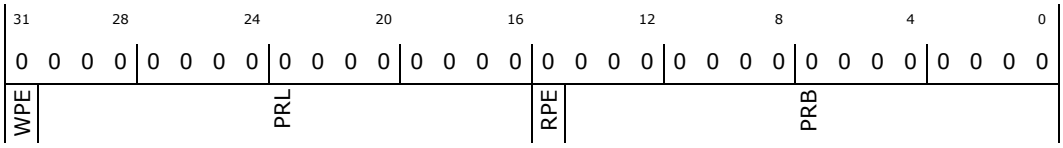
Protected range #1. This register can not be written when the FLOCKDN bit is set to 1.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 78h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the PR1LOCKDN bit of the LOCK register. **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
30:16	0x0 RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the PR1LOCKDN bit of the LOCK register. **Power Well:** EPW
15	0x0 RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the PR1LOCKDN bit of the LOCK register. **Power Well:** EPW
14:0	0x0 RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the PR1LOCKDN bit of the LOCK register. **Power Well:** EPW

10.9.29 PR2 (Protected_Range_2_bios)—Offset 7Ch

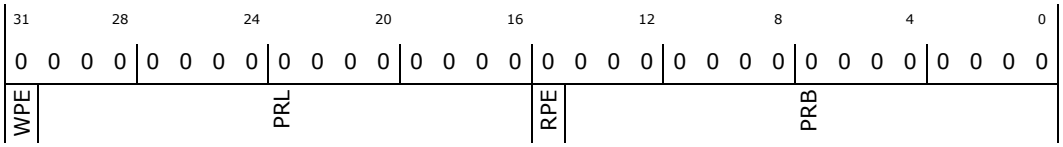
Protected range #2. This register can not be written when the FLOCKDN bit is set to 1.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 7Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the PR2LOCKDN bit of the LOCK register. **Power Well:** EPW
30:16	0x0 RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the PR2LOCKDN bit of the LOCK register. **Power Well:** EPW
15	0x0 RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the PR2LOCKDN bit of the LOCK register. **Power Well:** EPW
14:0	0x0 RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the PR2LOCKDN bit of the LOCK register. **Power Well:** EPW

10.9.30 PR3 (Protected_Range_3_bios)—Offset 80h

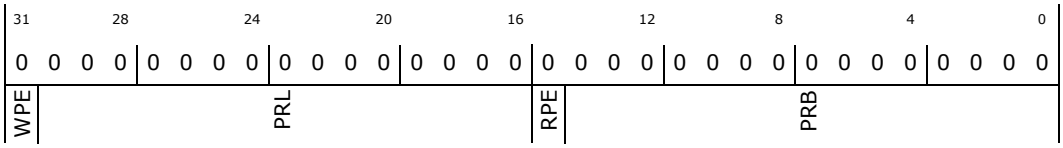
Protected range #3. This register can not be written when the FLOCKDN bit is set to 1.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 80h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the PR3LOCKDN bit of the LOCK register. **Power Well:** EPW
30:16	0x0 RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the PR3LOCKDN bit of the LOCK register. **Power Well:** EPW
15	0x0 RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the PR3LOCKDN bit of the LOCK register. **Power Well:** EPW
14:0	0x0 RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the PR3LOCKDN bit of the LOCK register. **Power Well:** EPW

10.9.31 PR4 (Protected_Range_4_bios)—Offset 84h

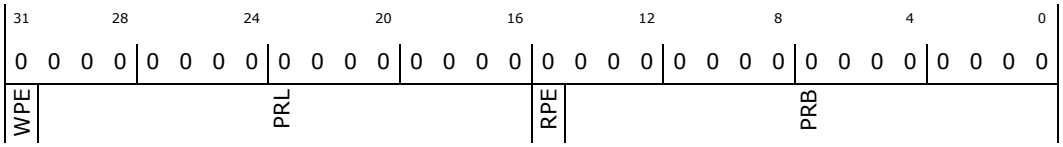
Protected range #4. This register use for H/W range protection. All register values are coming from soft-straps, and the Write Protection Enable is controlled also by the Flash Security Override Pin Strap

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 84h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	X RO	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. This field value should be an or between soft-strap and the ~Flash Security Override Pin Strap. Such, H/W range protection is active aonly if write protection is enabled by soft-strap and Flash Security Override Pin Strap is deasserted. **Power Well:** EPW
30:16	X RO	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. This field value should be taken from soft-straps. **Power Well:** EPW
15	0x0 RO	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. This field should be always 1'b0 **Power Well:** EPW
14:0	X RO	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. This field value should be taken from soft-straps. **Power Well:** EPW

10.9.32 SSFCTLSTS (Software_Sequencing_Flash_Control_Status_bios)—Offset 90h

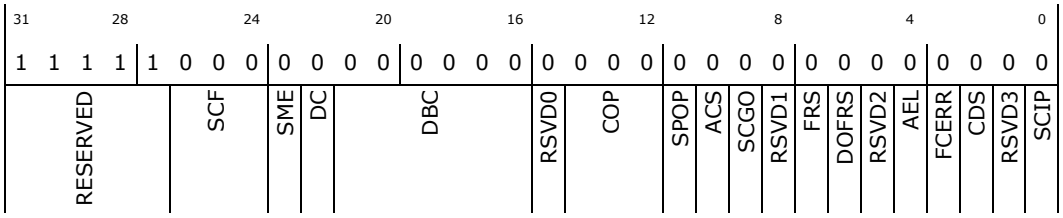
The software sequencing flash control and Status register is a combination of two registers the software sequencing flash status register (bits 7:0) and the software sequencing flash control register (bits 31:8). This register is intended to be used only as a back-up mode to the hardware sequencing control and status registers.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 90h

Default: F8000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x1f RO	**RESERVED:** reserved, should be with default 1 **Power Well:** EPW
26:24	0x0 RW/L	**SPI Cycle Frequency (SCF):** 000 : 20MHz 001 : 33MHz 010 : 66MHz 011 : 25MHz 100 : 50MHz All Others: Reserved This register sets frequency to use for all SPI Software Sequencing cycles (write, erase, fast read, read status, .etc) except for the Read cycle which always run at 20MHz. This register is locked when the SPI Configuration Lock-Down bit is set or when FREQLOCKDN bit is set. **Power Well:** EPW
23	0x0 RW	**SPI SMI# Enable (SME):** When set to 1, the SPI asserts an SMI# request whenever the Cycle Done Status bit is 1. **Power Well:** EPW
22	0x0 RW	**Data Cycle (DC):** When set to 1, there is data that corresponds to this transaction. When 0, no data is dleivered for this cycle, and the DBC and data fields themselves are don t cares. **Power Well:** EPW
21:16	0x0 RW	**Data Byte Count (DBC):** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The valid settings (in decimal) are any value from 0 to 63. The number of bytes transferred is the value of this field plus 1. Note that when this field is 00_0000b, then there is 1 byte to transfer and that 11_1111b means there are 64 bytes to transfer. **Power Well:** EPW
15	0x0 RO	**RSVD0:** Reserved
14:12	0x0 RW	**Cycle Opcode Pointer (COP):** This field selects one of the programmed opcodes in the Opcode Menu to be used as the SPI Command/Opcode. In the case of an Atomic Cycle Sequence, this determines the second command. **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
11	0x0 RW	**Sequence Prefix Opcode Pointer (SPOP):** This field selects one of the two programmed prefix opcodes for use when performing an Atomic Cycle Sequence. A value of 0 points to the opcode in the least significant byte of the Prefix Opcodes register. By making this programmable, the SPI controller supports flash devices that have different opcodes for enabling writes to the data space vs. status register. **Power Well:** EPW
10	0x0 RW	**Atomic Cycle Sequence (ACS):** When set to 1 along with the SCGO assertion, the SPI controller will execute a sequence of commands on the SPI interface without allowing the LAN component to arbitrate and interleave cycles. The sequence is composed of:) Atomic Sequence Prefix Command (8-bit opcode only)) Primary Command specified below by software (can include address and data)) Polling the Flash Status Register (opcode 8'h05) until bit 0 becomes 1'b0. The SPI Cycle in Progress bit remains set and the Cycle Done Status bit remains unset until the Busy bit in the Flash Status Register returns 0. **Power Well:** EPW
9	0x0 RW/SE	**SPI Cycle Go (SCGO):** This bit always returns 1'b0 on reads. However, a write to this register with a 1'b1 in this bit starts the SPI cycle defined by the other bits of this register. The SPI Cycle in Progress (SCIP) bit gets set by this action. Hardware must ignore writes to this bit while the Cycle In Progress bit is set. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1'b1. This saves an additional memory write. **Power Well:** EPW
8	0x0 RO	**RSVD1:** Reserved
7	0x0 RO/U	**Fast Read Supported (FRS):** This bit reflects the value of the Fast Read Support bit in the Flash Descriptor Component Section. **Power Well:** EPW
6	0x0 RO/U	**Dual Output Fast Read Supported (DOFRS):** This bit reflects the value of the Dual Output Fast Read Support bit in the Flash Descriptor Component Section. **Power Well:** EPW
5	0x0 RO	**RSVD2:** Reserved
4	0x0 RO	**Access Error Log (AEL):** This bit reflects the value of the Hardware Sequencing Status.AEL register. **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW/1C	**Flash Cycle Error (FCERR):** Hardware sets this bit to 1'b1 when a programmed access is blocked from running on the SPI interface due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1'b1 or hardware reset. **Power Well:** EPW
2	0x0 RW/1C	**Cycle Done Status (CDS):** The SPI controller sets this bit to 1'b1 when the SPI Cycle completes i.e., SCIP bit is 1'b0) after software sets the GO bit. This bit remains asserted until cleared by software writing a 1'b1 or hardware reset. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access. **Power Well:** EPW
1	0x0 RO	**RSVD3:** Reserved
0	0x0 RO	**SPI Cycle In Progress (SCIP):** Hardware sets this bit when software sets the SPI Cycle Go bit in the Command register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 1'b0. **Power Well:** EPW

10.9.33 PREOP (Prefix_Opcode_Configuration_bios)—Offset 94h

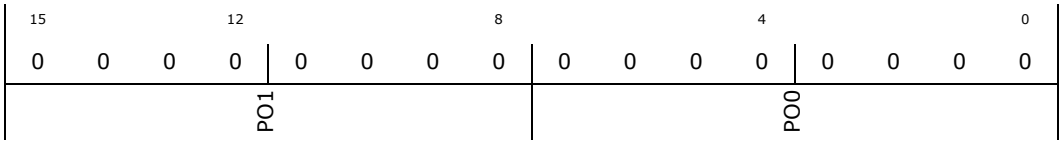
Prefix opcode configuration. This register is not writable when the SPI Configuration Lock-Down bit is set.

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [SPI_BASE_ADDRESS] + 94h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RW/L	**Prefix Opcode 1 (PO1):** Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the PREOPLOCKDN bit of the LOCK register. **Power Well:** EPW
7:0	0x0 RW/L	**Prefix Opcode 0 (PO0):** Prefix Opcode 0: Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the PREOPLOCKDN bit of the LOCK register. **Power Well:** EPW

10.9.34 OPTYPE (Opcode_Type_Configuration_bios)—Offset 96h

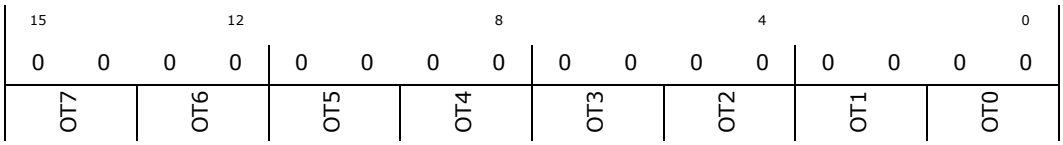
Opcode type configuration. This register is not writable when the Flash Configuration Lock-Down bit is set. Entries in this register correspond to the entries in the Opcode Menu Configuration register. Note that the definition below only provides write protection for opcodes that have addresses associated with them. Therefore, any erase or write opcodes that do not use an address should be avoided (for example, Chip Erase and Auto-Address Increment Byte Program).

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [SPI_BASE_ADDRESS] + 96h

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RW/L	**Opcode Type 7 (OT7):** Refer the description for bits 1:0. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the OPTYPELOCKDN bit of the LOCK register. **Power Well:** EPW
13:12	0x0 RW/L	**Opcode Type 6 (OT6):** Refer the description for bits 1:0. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the OPTYPELOCKDN bit of the LOCK register. **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
11:10	0x0 RW/L	**Opcode Type 5 (OT5):** Refer the description for bits 1:0. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the OPTYPELOCKDN bit of the LOCK register. **Power Well:** EPW
9:8	0x0 RW/L	**Opcode Type 4 (OT4):** Refer the description for bits 1:0. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the OPTYPELOCKDN bit of the LOCK register. **Power Well:** EPW
7:6	0x0 RW/L	**Opcode Type 3 (OT3):** Refer the description for bits 1:0. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the OPTYPELOCKDN bit of the LOCK register. **Power Well:** EPW
5:4	0x0 RW/L	**Opcode Type 2 (OT2):** Refer the description for bits 1:0. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the OPTYPELOCKDN bit of the LOCK register. **Power Well:** EPW
3:2	0x0 RW/L	**Opcode Type 1 (OT1):** Refer the description for bits 1:0. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the OPTYPELOCKDN bit of the LOCK register. **Power Well:** EPW
1:0	0x0 RW/L	**Opcode Type 0 (OT0):** This field specifies information about the corresponding Opcode 0. This information allows the hardware to 1) know whether to use the address field and 2) provide BIOS and Shared Flash protection capabilities. The hardware implementation also uses the read vs. write information for modifying the behavior of the SPI interface logic. The encoding of the two bits is: 00 = No Address associated with this Opcode and Read Cycle type 01 = No Address associated with this Opcode and Write Cycle type 10 = Address required, Read cycle type 11 = Address required, Write cycle type Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the OPTYPELOCKDN bit of the LOCK register. **Power Well:** EPW

10.9.35 OPMENU0 (Opcode_Menu_Configuration_0_bios)—Offset 98h

Opcode (0-3) Menu Configuration. This register is not writable when the SPI Configuration Lock-Down bit is set. Four entries are available in this register and four are available in OPMENU1 register to give BIOS a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI

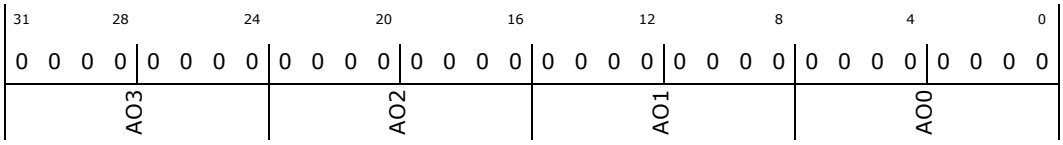
devices. It is recommended that BIOS avoid programming Write Enable opcodes in this menu. Malicious software could then perform writes and erases to the SPI flash without using the atomic cycle mechanism. This could cause functional failures in a shared flash environment. Write Enable opcodes should only be programmed in the Prefix Opcodes.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 98h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW/L	**Allowable Opcode 3 (AO3):** Refer the description for bits 7:0. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the OPMENULOCKDN bit of the LOCK register. **Power Well:** EPW
23:16	0x0 RW/L	**Allowable Opcode 2 (AO2):** Refer the description for bits 7:0. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the OPMENULOCKDN bit of the LOCK register. **Power Well:** EPW
15:8	0x0 RW/L	**Allowable Opcode 1 (AO1):** Refer the description for bits 7:0. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the OPMENULOCKDN bit of the LOCK register. **Power Well:** EPW
7:0	0x0 RW/L	**Allowable Opcode 0 (AO0):** Software programs an SPI opcode into this field for use when initiating SPI commands through the Control Register. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the OPMENULOCKDN bit of the LOCK register. **Power Well:** EPW

10.9.36 OPMENU1 (Opcode_Menu_Configuration_1_bios)—Offset 9Ch

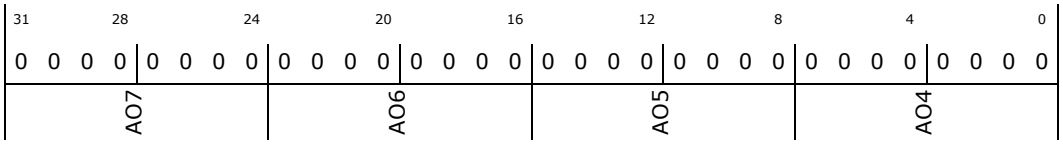
Opcode (7-4) Menu Configuration. This register is not writable when the SPI Configuration Lock-Down bit is set. Four entries are available in this register and four are available in OPMENU0 register to give BIOS a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices. It is recommended that BIOS avoid programming Write Enable opcodes in this

menu. Malicious software could then perform writes and erases to the SPI flash without using the atomic cycle mechanism. This could cause functional failures in a shared flash environment. Write Enable opcodes should only be programmed in the Prefix Opcodes.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** [SPI_BASE_ADDRESS] + 9Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW/L	**Allowable Opcode 7 (AO7):** Refer the description for bits 7:0 in OPMENU0. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the OPMENULOCKDN bit of the LOCK register. **Power Well:** EPW
23:16	0x0 RW/L	**Allowable Opcode 6 (AO6):** Refer the description for bits 7:0 in OPMENU0. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the OPMENULOCKDN bit of the LOCK register. **Power Well:** EPW
15:8	0x0 RW/L	**Allowable Opcode 5 (AO5):** Refer the description for bits 7:0 in OPMENU0. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the OPMENULOCKDN bit of the LOCK register. **Power Well:** EPW
7:0	0x0 RW/L	**Allowable Opcode 4 (AO4):** Refer the description for bits 7:0 in OPMENU0. Locked by the OR of the Flash Configuration Lock-Down bit in the HSFSTS register and the OPMENULOCKDN bit of the LOCK register. **Power Well:** EPW

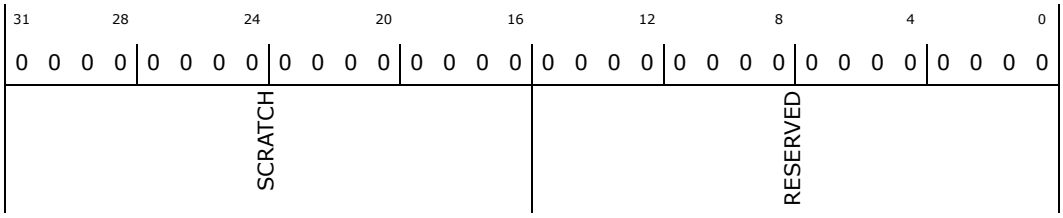
10.9.37 BIOS_SCRATCHPAD (Bios_Scratchpad_Register)—Offset A0h

Extra bits, can be used by BIOS as a scratchpad, these bits have no effect on the design.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** [SPI_BASE_ADDRESS] + A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**SCRATCH:** Scratch pad bits that are RW **Power Well:** EPW
15:0	0x0 RO	**RESERVED:** reserved, should be with default 0 **Power Well:** EPW

10.9.38 LOCK (Individual_Lock_Register)—Offset A4h

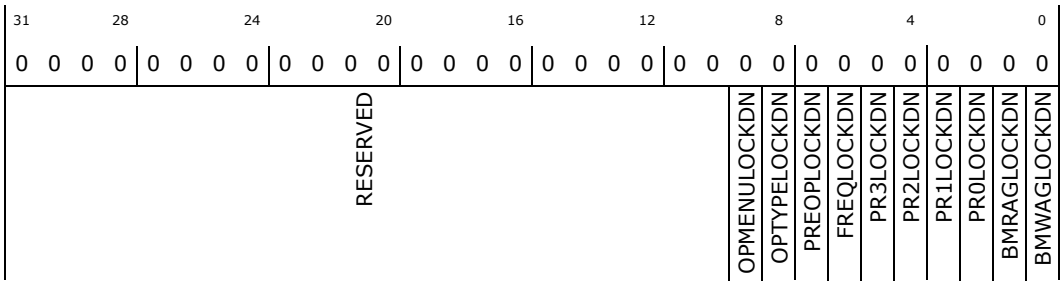
Used to individually lock each one of the registers formaly locked only by FLOCKDN bit. This register doesn't exclude FLOCKDN. It adds an individual option to lock each register in above to FLOCKDN.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RO	**RESERVED:** reserved, should be with default 0 **Power Well:** EPW
9	0x0 RW/L	**OPMENU Lock-Down (OPMENULOCKDN):** When set to 1, OPMENU0 and OPMENU1 registers cannot be written. Once set to 1, this bit can only be cleared by a hardware reset. This field is locked by the OR of itself with the Flash Configuration Lock-Down bit in the HSFSTS register. **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW/L	**OPTYPE Lock-Down (OPTYPELOCKDN):** When set to 1, OPTYPE register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset. This field is locked by the OR of itself with the Flash Configuration Lock-Down bit in the HSFSTS register. **Power Well:** EPW
7	0x0 RW/L	**PREOP Lock-Down (PREOPLOCKDN):** When set to 1, PREOP register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset. This field is locked by the OR of itself with the Flash Configuration Lock-Down bit in the HSFSTS register. **Power Well:** EPW
6	0x0 RW/L	**SCF Lock-Down (FREQLOCKDN):** When set to 1, SCF field cannot be written. Once set to 1, this bit can only be cleared by a hardware reset. This field is locked by the OR of itself with the Flash Configuration Lock-Down bit in the HSFSTS register. **Power Well:** EPW
5	0x0 RW/L	**PR3 Lock-Down (PR3LOCKDN):** When set to 1, PR3 register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset. This field is locked by the OR of itself with the Flash Configuration Lock-Down bit in the HSFSTS register. **Power Well:** EPW
4	0x0 RW/L	**PR2 Lock-Down (PR2LOCKDN):** When set to 1, PR2 register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset. This field is locked by the OR of itself with the Flash Configuration Lock-Down bit in the HSFSTS register. **Power Well:** EPW
3	0x0 RW/L	**PR1 Lock-Down (PR1LOCKDN):** When set to 1, PR1 register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset. This field is locked by the OR of itself with the Flash Configuration Lock-Down bit in the HSFSTS register. **Power Well:** EPW
2	0x0 RW/L	**PR0 Lock-Down (PR0LOCKDN):** When set to 1, PR0 register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset. This field is locked by the OR of itself with the Flash Configuration Lock-Down bit in the HSFSTS register. **Power Well:** EPW
1	0x0 RW/L	**BMRAG Lock-Down (BMRAGLOCKDN):** When set to 1, BMRAG field cannot be written. Once set to 1, this bit can only be cleared by a hardware reset. This field is locked by the OR of itself with the Flash Configuration Lock-Down bit in the HSFSTS register. **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW/L	**BMWAG Lock-Down (BMWAGLOCKDN):** When set to 1, BMWAG field cannot be written. Once set to 1, this bit can only be cleared by a hardware reset. This field is locked by the OR of itself with the Flash Configuration Lock-Down bit in the HSFSTS register. **Power Well:** EPW

10.9.39 FDOC (Flash_Descriptor_Observability_Control_bios)—Offset B0h

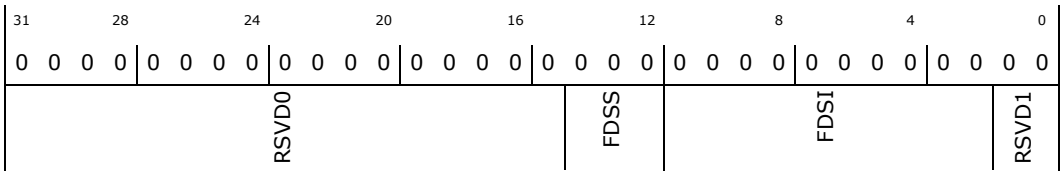
Flash Descriptor Observability Control. This is a test mode only register that can be used to observe the contents of the Flash Descriptor that is stored internally in the SPI Controller.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0x0 RO	**RSVD0:** Reserved
14:12	0x0 RW	**Flash Descriptor Section Select (FDSS):** Selects which section within the loaded Flash Descriptor to observe. 000 : Flash Signature and Descriptor Map 001 : Component 010 : Region 011 : Master 100 : Soft Straps 101 : Reserved 110 : Reserved 111 : Reserved **Power Well:** EPW
11:2	0x0 RW	**Flash Descriptor Section Index (FDSI):** Selects the DW offset within the Flash Descriptor Section to observe. **Power Well:** EPW
1:0	0x0 RO	**RSVD1:** Reserved

10.9.40 FDOD (Flash_Descriptor_Observability_Data_bios)—Offset B4h

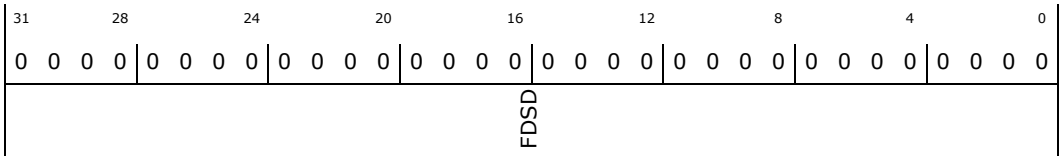
Flash descriptor observability data

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + B4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Flash Descriptor Section Data (FDSD):** Contains the DW of data to observe as selected in the Flash Descriptor Observability Control. at default the FDSS==3'b000 hence this register contans the data of Flash Signature and Descriptor Map. **Power Well:** EPW

10.9.41 AFC (Additional_Flash_Control_bios)—Offset C0h

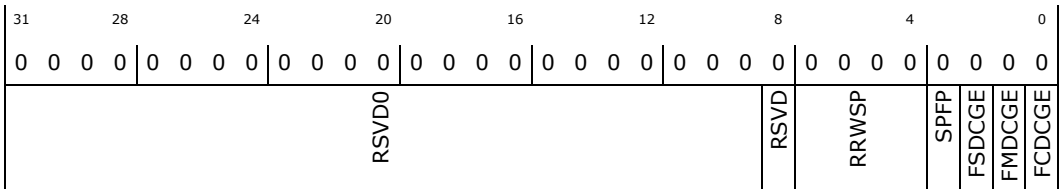
Additional flash control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
8	0x0 RW/L	**Reserved (RSVD):** Used to select whether the data coming from external SPI device is sampled using the looped back SPI clock or the internal clock. For SoC B0 and BX, this is not used anymore as only internal clock is used for sampling. **Power Well:** EPW
7:4	0x0 RW	**Reserved RW Scratch Pad (RRWSP):** Scratch Pad bits that are R/W to be used during ECO **Power Well:** EPW
3	0x0 RW	**Stop Prefetch on Flush Pending (SPFP):** When set to 1'b1, the in progress of a prefetch will be ended if subsequence access from the same master is detected to be a cache-miss and read cache will be flushed. When set to 1'b0, the prefetch will be allowed to complete prior to flushing. **Power Well:** EPW
2	0x0 RW	**Flash IOSF PRI Dynamic Clock Gating Enable (FSDCGE):** When set to 1'b1, the SPI controller IOSF-PRI interface logic can be dynamically clock gated. This register is only clear on a reset. **Power Well:** EPW
1	0x0 RW	**Flash IOSF SB Dynamic Clock Gating Enable (FMDCGE):** When set to 1'b1, the SPI controller IOSF-SB interface logic can be dynamically clock gated. This register is only clear on a reset. **Power Well:** EPW
0	0x0 RW	**Flash Core Dynamic Clock Gating Enable (FCDCGE):** When set to 1'b1, the SPI controller core logic can be dynamically clock gated. This register is only clear on a reset. **Power Well:** EPW

10.9.42 VSCC0 (Lower_Vendor_Specific_Component_Capabilities_bios)—Offset C4h

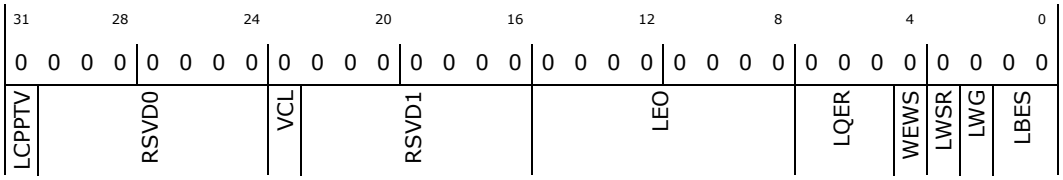
Lower vendor specific component capabilities

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + C4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO/U	**Lower Component Property Parameter Table Valid (LCPPTV):** This bit is set to a 1 if the Flash Controller detects a valid SFDP Component Property Parameter Table in Component 0. **Power Well:** EPW
30:24	0x0 RO	**RSVD0:** Reserved
23	0x0 RW/L	**Vendor Component Lock (VCL):** '0': The lock bit is not set '1': The Vendor Component Lock bit is set. This register locks itself when set. If this register is not set and the Flash is operating in Flash Mode (as opposed to EEPROM mode), then software cannot use hardware sequencing. This requirement is not enforced by hardware, but is a requirement of the the power-on usage model. **Power Well:** EPW
22:16	0x0 RO	**RSVD1:** Reserved
15:8	0x0 RW/L	**Lower Erase Opcode (LEO):** This register is programed with the Flash erase instruction opcode required by this vendors Flash component. This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses below the Flash Partition Address. **Power Well:** EPW
7:5	0x0 RW/L	**Lower QUAD Enable Requirements (LQER) (LQER):** These bits are not used. They are reserved bits. 000 Part does not require a Quad Enable bit to be set, either because Quad is not supported or because the manufacturer somehow permanently enables Quad capability. 001 Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to status register clears all bits in register 2, therefore status register writes MUST be two bytes. (If the status register is unlocked and SFDP bits WSR or VSCC WSR is 1 then SoC cannot use the quad output, quad IO features of this part because the hardware will automatically write one byte of zeros to status register with every write/erase.) 010 Part requires bit 6 of status register 1 to be set to enable quad IO. If the status register is unlocked and SFDP WSR bit or VSCC WSR is 1 then SoC cannot use the quad output, quad IO features of this part because the hardware will automatically write one byte of zeros to status register with every write/erase. 011 Part requires bit 7 of the configuration register to be set to enable Quad. 100 Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to the status register does not clear the second byte. **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW/L	**Write Enable on Write Status (WEWS):** Write Enable Opcode Select for Writing to Volatile Status Register 0: 0x50 is the Opcode to enable a status register write when bit 3 is set to 1. 1: 0x06 is the Opcode to enable a status register write when bit 3 is set to 1. **Power Well:** EPW
3	0x0 RW/L	**Lower Write Status Required (LWSR):** '0' : No requirement to to write to the Write Status Register prior to a write '1' : A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses below the Flash Partition Address. **Power Well:** EPW
2	0x0 RW/L	**Lower Write Granularity (LWG):** '0' : 1 Byte '1' : 64 Byte This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses below the Flash Partition Address. **Power Well:** EPW
1:0	0x0 RW/L	**Lower Block/Sector Erase Size (LBES):** This field identifies the erasable sector size for all Flash components. Valid Bit Settings: '00' : 256 Byte '01' : 4K Byte '10' : 8K Byte '11' : 64K Byte This register is locked by the Vendor Component Lock (VCL) bit. Hardware takes no action based on the value of this register. The contents of this register are to be used only by software and can be read in the HSFSTS. This field is used for cycles targeting addresses below the Flash Partition Address. **Power Well:** EPW

10.9.43 VSCC1 (Upper_Vendor_Specific_Component_Capabilities_bios)—Offset C8h

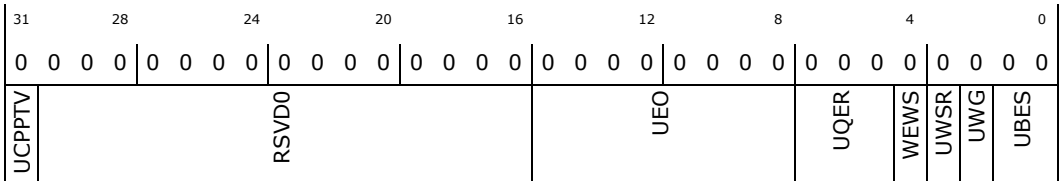
Upper vendor specific component capabilities

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + C8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO/U	**Upeer Component Property Parameter Table Valid (UCPPTV):** This bit is set to a 1 if the Flash Controller detects a valid SFDP Component Property Parameter Table in Component 0. **Power Well:** EPW
30:16	0x0 RO	**RSVD0:** Reserved
15:8	0x0 RW/L	**Upper Erase Opcode (UEO):** This register is programed with the Flash erase instruction opcode required by this vendors Flash component. This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses above the Flash Partition Address. **Power Well:** EPW
7:5	0x0 RW/L	**Upper QUAD Enable Requirements (UQER):** These bits are not used. They are reserved bits. 000 Part does not require a Quad Enable bit to be set, either because Quad is not supported or because the manufacturer somehow permanently enables Quad capability. 001 Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to status register clears all bits in register 2, therefore status register writes MUST be two bytes. (If the status register is unlocked and SFDP bits WSR or VSCC WSR is 1 then SoC cannot use the quad output, quad IO features of this part because the hardware will automatically write one byte of zeros to status register with every write/erase.) 010 Part requires bit 6 of status register 1 to be set to enable quad IO. If the status register is unlocked and SFDP WSR bit or VSCC WSR is 1 then SoC cannot use the quad output, quad IO features of this part because the hardware will automatically write one byte of zeros to status register with every write/erase. 011 Part requires bit 7 of the configuration register to be set to enable Quad. 100 Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to the status register does not clear the second byte. **Power Well:** EPW
4	0x0 RW/L	**Write Enable on Write Status (WEWS):** Write Enable Opcode Select for Writing to Volatile Status Register 0: 0x50 is the Opcode to enable a status register write when bit 3 is set to 1. 1: 0x06 is the Opcode to enable a status register write when bit 3 is set to 1. **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW/L	**Upper Write Status Required (UWSR):** '0': No requirement to to write to the Write Status Register prior to a write '1': A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses above the Flash Partition Address. **Power Well:** EPW
2	0x0 RW/L	**Upper Write Granularity (UWG):** '0' : 1 Byte '1' : 64 Byte This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses above the Flash Partition Address. **Power Well:** EPW
1:0	0x0 RW/L	**Upper Block/Sector Erase Size (UBES):** This field identifies the erasable sector size for all Flash components. Valid Bit Settings: '00' : 256 Byte '01' : 4K Byte '10' : 8K Byte '11' : 64K Byte Note: If supporting more than one Flash component, all flash components must have identical Block/ Sector erase sizes. This register is locked by the Vendor Component Lock (VCL) bit. Hardware takes no action based on the value of this register. The contents of this register are to be used only by software and can be read in the HSFSTS. This field is used for cycles targeting addresses above the Flash Partition Address. **Power Well:** EPW

10.9.44 PTINX (Parameter_Table_Index_bios)—Offset CCh

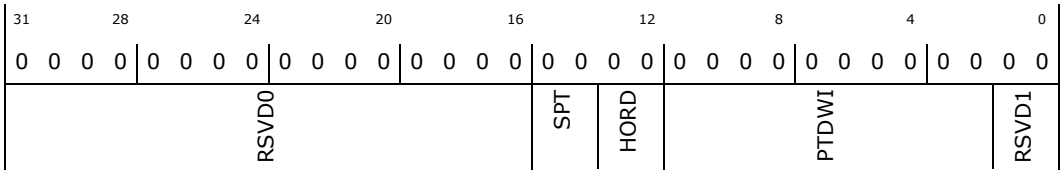
Parameter table index

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + CCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RW	**Supported parameter table (SPT):** 00 : Component 0 Property Parameter Table 01 : Component 1 Property Parameter Table 10 ? 11 : Reserved **Power Well:** EPW
13:12	0x0 RW	**Header or Data (HORD):** 00 : SFDP Header 01 : Parameter Table Header 10 : Data 11 : Reserved **Power Well:** EPW
11:2	0x0 RW	**Parameter Table DW Index (PTDWI):** Selects the DW offset within the parameter table to observe **Power Well:** EPW
1:0	0x0 RO	**RSVD1:** Reserved

10.9.45 PTDATA (Parameter_Table_Data_bios)—Offset D0h

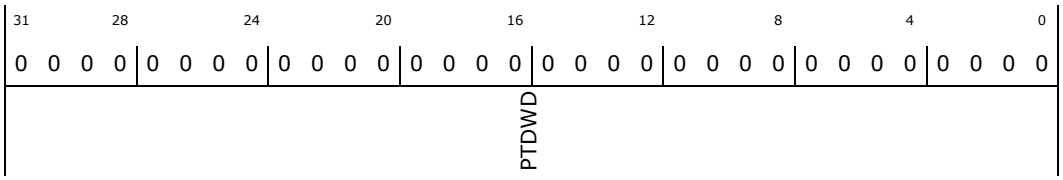
Parameter table data

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO/U	**Supported parameter table (PTDWD):** Returns the DW of data to observe as selected in the Parameter Table Index register. **Power Well:** EPW

10.9.46 FPB (Flash_Partition_Boundary_bios)—Offset D4h

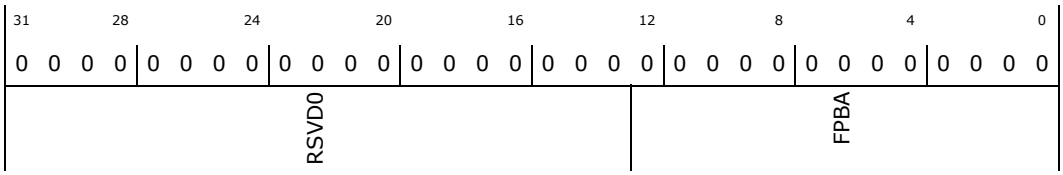
Flash partition boundary

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + D4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RSVD0:** Reserved
12:0	0x0 RO/U	**Flash Partition Boundary Address (FPBA):** This register reflects the value of the Flash Descriptor Component FPBA field **Power Well:** EPW

10.9.47 SCS (SMI_Control_Status_Register_bios)—Offset F8h

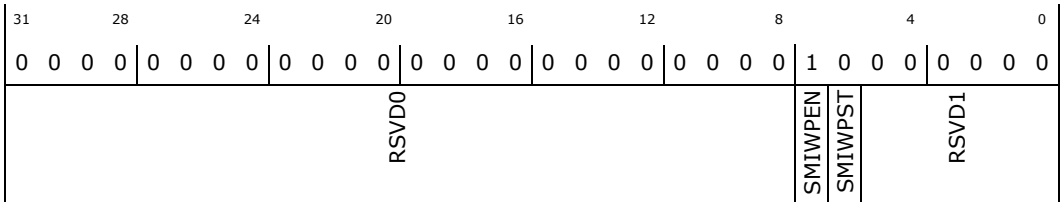
SMI Control and Status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + F8h

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7	0x1 RW	**SMI WPD Enable (SMIWPEN):** When this bit is set to a 1'b1, it enables the SPI controller to generate SMI upon not SMM code is trying to set WPD from a 1'b0 to a 1'b1 while LE is set. **Power Well:** EPW
6	0x0 RW/1C	**SMI WPD Status (SMIWPST):** Set when SMI is generated upon trying to set WPD from a 1'b0 to a 1'b1 by not SMM code (while LE and SMIWPEN are set). Write a 1'b1 to this bit should clear it and clear the SMI (send DEASSERT_SMI) **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
5:0	0x0 RO	**RSVD1:** Reserved

10.9.48 BCR (BIOS_Control_Register_bios)—Offset FCh

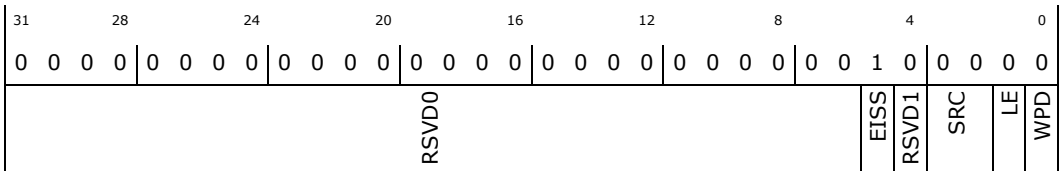
BIOS control register. This register formerly was in the 0:31:0 config space

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + FCh

Default: 00000020h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**RSVD0:** Reserved
5	0x1 RW/L	**Enable InSMM_STS (EISS):** When this bit is set, the BIOS region is writable only to SMM code. Today BIOS Flash is writable if WPD is a '1'. If this bit [lb]5[rb] is set, then WPD must be a 1'b1 and iosfep_xxx_hprot[lb]1[rb] signal be 1'b1 also. If this bit [lb]5[rb] is clear, then BIOS is writable based only on WPD = 1'b1 and the iosfep_xxx_hprot[lb]1[rb] signal is a don't care. **Power Well:** EPW
4	0x0 RO	**RSVD1:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
3:2	0x0 RW	**SPI Read Configuration (SRC):** This 2-bit field controls two policies related to BIOS reads on the SPI interface: Bit 3 - Prefetch Enable, Bit 2 - Cache Disable. Settings are summarized below: '00' : No prefetching, but caching enabled. Direct Memory reads load the read buffer cache with 'valid' data, allowing repeated reads to the same range to complete quickly. '01' : No prefetching and no caching. One-to-one correspondence of host BIOS reads to SPI cycles. This value can be used to invalidate the cache. '10' : Prefetching and Caching enabled. This mode is used for long sequences of short reads to consecutive addresses (i.e. shadowing) '11' : Illegal. Caching must be enabled when Prefetching is enabled. This eliminates the need for a complex prefetch-flushing mechanism. Note that if BIOS direct read caching is disabled while data has already been cached internally, subsequent BIOS direct reads will continue to return data from the cache until the cache is invalidated. **Power Well:** EPW
1	0x0 RW/L	**Lock Enable (LE):** When set, WPD bit could be set from a 1'b0 to a 1'b1 only by SMM code. When cleared, setting the WP bit is allowed in all modes and SMI is not generated. Once set, this bit can only be cleared by a PLTRST#. When this bit is set, EISS - bit [lb]5[rb] of this register is locked down. **Power Well:** EPW
0	0x0 RW	**Write Protect Disable (WPD):** When set, access to the BIOS space is enabled for both read and write cycles. When cleared, only read cycles are permitted to the flash. When LE bit is set this bit could be written from a 1'b0 to a 1'b1 only by SMM code. When not SMM code tries to writes this bit from a 1'b0 to a 1'b1, bit remain in its 1'b0 value. An Async-SMI is generated (Send ASSERT_SMI) if SMIWPEN is set. This ensures that only SMM code can update BIOS. **Power Well:** EPW

10.9.49 TCGC (Trunk_Clock_Gating_Control_bios)—Offset 100h

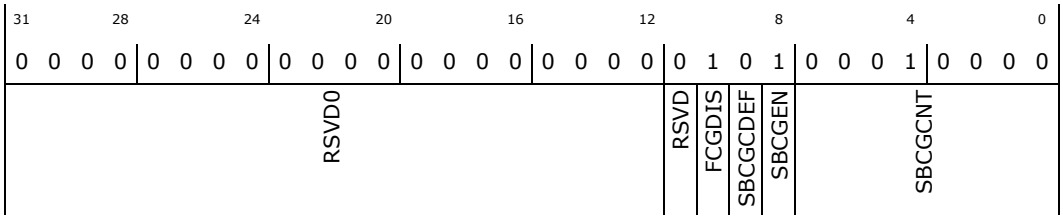
Trunk_Clock_Gating_Control

Access Method

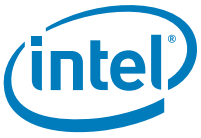
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [SPI_BASE_ADDRESS] + 100h

Default: 00000510h



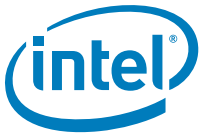
Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RSVD0:** Reserved
11	0x0 RO	**Reserved (RSVD):** Reserved.
10	0x1 RW	**FCGDIS:** Functional clock gating disable, chicken bit for the func_clk_gating FSM **Power Well:** EPW
9	0x0 RW	**SBCGCDEF:** SideBanb Control Gating Clock Defeature .Clock gate defeature bit which allows the ISM to transition to idle, but prevents the final clock masking from occurring. The value of this bit goes to the 'cgctrl_clkgatedef' port of the SideBand EndPoint **Power Well:** EPW
8	0x1 RW	**SBCGEN:** SideBanb Control Gating Clock Enable. Clock gate enable which prevents ISM from leaving ACTIVE. Also prevents the clocks from being gated. The value of this bit goes to the 'cgctrl_clkgaten' port of the SideBand EndPoint **Power Well:** EPW
7:0	0x10 RW	**SBCGCNT:** SideBanb Control Gating Clock Counter. Idle count limit for ISM which is used to determine the block is idle.Recommended value 8'd16 . The value of those bits goes to the 'cgctrl_idlecnt' ports of the SideBand EndPoint **Power Well:** EPW



10.10 PCU SPI for Firmware 2 Memory Mapped I/O

Table 105. Summary of PCU SPI for Firmware 2 Message Bus Registers—0x51

Offset	Register Name (Register Symbol)	Default Value
1000–1003h	"SECFPREG (SEC_Flash_Primary_Region_sec)—Offset 1000h" on page 5705	00007FFFh
1004–1005h	"HSFSTS (Hardware_Sequencing_Flash_Status_sec)—Offset 1004h" on page 5705	0000h
1006–1007h	"HSFCTL (Hardware_Sequencing_Flash_Control_sec)—Offset 1006h" on page 5707	0000h
1008–100Bh	"FADDR (Flash_Address_sec)—Offset 1008h" on page 5708	00000000h
1010–1013h	"FDATA0 (Flash_Data_0_sec)—Offset 1010h" on page 5709	00000000h
1014–1017h	"FDATA1 (Flash_Data_1_sec)—Offset 1014h" on page 5710	00000000h
1018–101Bh	"FDATA2 (Flash_Data_2_sec)—Offset 1018h" on page 5710	00000000h
101C–101Fh	"FDATA3 (Flash_Data_3_sec)—Offset 101Ch" on page 5711	00000000h
1020–1023h	"FDATA4 (Flash_Data_4_sec)—Offset 1020h" on page 5711	00000000h
1024–1027h	"FDATA5 (Flash_Data_5_sec)—Offset 1024h" on page 5712	00000000h
1028–102Bh	"FDATA6 (Flash_Data_6_sec)—Offset 1028h" on page 5712	00000000h
102C–102Fh	"FDATA7 (Flash_Data_7_sec)—Offset 102Ch" on page 5713	00000000h
1030–1033h	"FDATA8 (Flash_Data_8_sec)—Offset 1030h" on page 5713	00000000h
1034–1037h	"FDATA9 (Flash_Data_9_sec)—Offset 1034h" on page 5714	00000000h
1038–103Bh	"FDATA10 (Flash_Data_10_sec)—Offset 1038h" on page 5714	00000000h
103C–103Fh	"FDATA11 (Flash_Data_11_sec)—Offset 103Ch" on page 5715	00000000h
1040–1043h	"FDATA12 (Flash_Data_12_sec)—Offset 1040h" on page 5715	00000000h
1044–1047h	"FDATA13 (Flash_Data_13_sec)—Offset 1044h" on page 5716	00000000h
1048–104Bh	"FDATA14 (Flash_Data_14_sec)—Offset 1048h" on page 5716	00000000h
104C–104Fh	"FDATA15 (Flash_Data_15_sec)—Offset 104Ch" on page 5717	00000000h



Offset	Register Name (Register Symbol)	Default Value
1050–1053h	"FRACC (Flash_Region_Access_Permissions_sec)—Offset 1050h" on page 5717	00000404h
1054–1057h	"FREG0 (Flash_Region_0_sec)—Offset 1054h" on page 5719	00007FFFh
1058–105Bh	"FREG1 (Flash_Region_1_sec)—Offset 1058h" on page 5719	00007FFFh
105C–105Fh	"FREG2 (Flash_Region_2_sec)—Offset 105Ch" on page 5720	00007FFFh
1060–1063h	"FREG3 (Flash_Region_3_sec)—Offset 1060h" on page 5721	00007FFFh
1064–1067h	"FREG4 (Flash_Region_4_sec)—Offset 1064h" on page 5722	00007FFFh
1074–1077h	"PR0 (Protected_Range_0_sec)—Offset 1074h" on page 5722	00000000h
1078–107Bh	"PR1 (Protected_Range_1_sec)—Offset 1078h" on page 5723	00000000h
107C–107Fh	"PR2 (Protected_Range_2_sec)—Offset 107Ch" on page 5724	00000000h
1080–1083h	"PR3 (Protected_Range_3_sec)—Offset 1080h" on page 5725	00000000h
1084–1087h	"PR4 (Protected_Range_4_sec)—Offset 1084h" on page 5726	00000000h
1090–1093h	"SSFCTLSTS (Software_Sequencing_Flash_Control_Status_sec)—Offset 1090h" on page 5727	F8000000h
1094–1095h	"PREOP (Prefix_Opcode_Configuration_sec)—Offset 1094h" on page 5730	0000h
1096–1097h	"OPTYPE (Opcode_Type_Configuration_sec)—Offset 1096h" on page 5731	0000h
1098–109Bh	"OPMENU0 (Opcode_Menu_Configuration_0_sec)—Offset 1098h" on page 5732	00000000h
109C–109Fh	"OPMENU1 (Opcode_Menu_Configuration_1_sec)—Offset 109Ch" on page 5733	00000000h
10A0–10A3h	"SCRATCH0 (Scratch0_sec)—Offset 10A0h" on page 5734	00000007h
10A4–10A7h	"SCRATCH1 (Scratch1_sec)—Offset 10A4h" on page 5734	D810DC10h
10A8–10ABh	"SCRATCH2 (Scratch2_sec)—Offset 10A8h" on page 5735	0000520Fh
10AC–10AFh	"SCRATCH3 (Scratch3_sec)—Offset 10ACh" on page 5736	00000000h
10C4–10C7h	"VSCC0 (Lower_Vendor_Specific_Component_Capabilities_sec)—Offset 10C4h" on page 5736	00000000h
10C8–10CBh	"VSCC1 (Upper_Vendor_Specific_Component_Capabilities_sec)—Offset 10C8h" on page 5738	00000000h

Offset	Register Name (Register Symbol)	Default Value
10CC–10CFh	"PTINX (Parameter_Table_Index_sec)—Offset 10CCh" on page 5740	00000000h
10D0–10D3h	"PTDATA (Parameter_Table_Data_sec)—Offset 10D0h" on page 5741	00000000h
10D4–10D7h	"FPB (Flash_Partition_Boundary_sec)—Offset 10D4h" on page 5741	00000000h
10F0–10F3h	"ICE (Interrupt_Cause_Enable_sec)—Offset 10F0h" on page 5742	00000000h
10F4–10F7h	"ICS (Interrupt_Cause_Status_sec)—Offset 10F4h" on page 5743	00000000h
10F8–10FBh	"IADD (Interrupt_Address_sec)—Offset 10F8h" on page 5744	0085C044h
10FC–10FFh	"SECCTRL (SEC_Flash_Control_sec)—Offset 10FCh" on page 5744	00000003h
1100–1103h	"ERE (Erase_range_enable)—Offset 1100h" on page 5745	00000007h

10.10.1 SECFPREG (SEC_Flash_Primary_Region_sec)—Offset 1000h

SEC flash primary region

Access Method

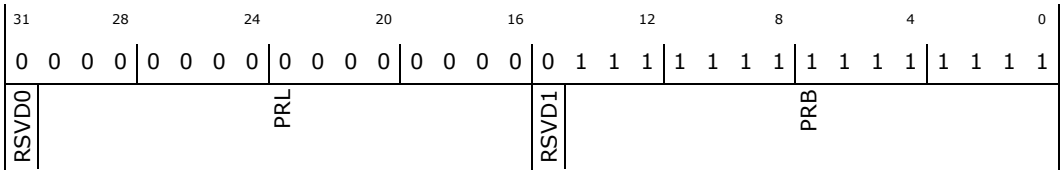
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1000h

Op Codes:

h - Read, h - Write

Default: 00007FFFh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RSVD0:** Reserved
30:16	0x0 RO	**SEC Flash Primary Region Limit (PRL):** This specifies address bits 26:12 for the Primary Region Limit. The value in this register loaded from the contents in the Flash Descriptor.FLREG2.Region Limit **Power Well:** EPW
15	0x0 RO	**RSVD1:** Reserved
14:0	0x7fff RO	**SEC Flash Primary Region Base (PRB):** This specifies address bits 24:12 for the Primary Region Base. The value in this register iloaded from the contents in the Flash Descriptor.FLREG2.Region Base **Power Well:** EPW

10.10.2 HSFSTS (Hardware_Sequencing_Flash_Status_sec)—Offset 1004h

Hardware sequencing flash status

Access Method

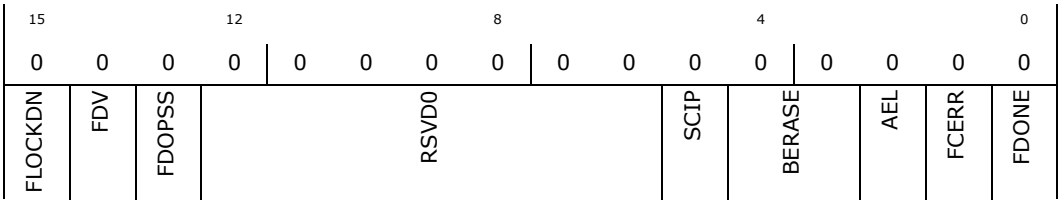
Type: Message Bus Register (Size: 16 bits)

Offset: [Port: 0x51] + 1004h

Op Codes:

h - Read, h - Write

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW/L	**Flash Configuration Lockdown (FLOCKDN):** When set to 1'b1, those Flash Program Registers that are locked down by this FLOCKDN bit cannot be written. Once set to 1'b1, this bit can only be cleared by a hardware reset. **Power Well:** EPW
14	0x0 RO	**Flash Descriptor Valid (FDV):** This bit is set to a 1'b1 if the Flash Controller read the correct Flash Descriptor Signature. If the Flash Descriptor Valid bit is not 1'b1, software cannot use the Hardware Sequencing registers, but must use the software sequencing registers. Any attempt to use the Hardware Sequencing registers will result in the FCERR bit being set. **Power Well:** EPW
13	0x0 RO	**Flash Descriptor Override Pin-Strap Status (FDOPSS):** This register reflects the value the Flash Descriptor Override Pin-Strap. '1' : No override '0' : The Flash Descriptor Overide strap is set **Power Well:** EPW
12:6	0x0 RO	**RSVD0:** Reserved
5	0x0 RO	**SPI Cycle In Progress (SCIP):** Hardware sets this bit when software sets the Flash Cycle Go (FGO) bit in the Hardware Sequencing Flash Control register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 1'b0. **Power Well:** EPW
4:3	0x0 RO	**Block/Sector Erase Size (BERASE):** This field identifies the erasable sector size for all Flash components. Valid Bit Settings: '00' : 256 Byte '01' : 4K Byte '10' : 8K Byte '11' : 64K Byte If the FLA (FPBA then this field reflects the value in the VSCC0.LBES register. If the FLA)= FPBA then this field reflects the value in the VSCC1.UBES register. **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW/1C	**Access Error Log (AEL):** Hardware sets this bit to a 1 when a direct read was made by SEC that violated the security restrictions. Or , when a SB transaction to read/write one of the SEC registers was accepted with bad SAI - see security table. This bit has no affect on indirect accesses. This bit is cleared by software writing a 1. **Power Well:** EPW
1	0x0 RW/1C	**Flash Cycle Error (FCERR):** Hardware sets this bit to 1'b1 when an program register access is blocked to the FLASH due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1'b1 or until hardware reset occures. Software must clear this bit before setting the FLASH Cycle GO bit in this register. **Power Well:** EPW
0	0x0 RW/1C	**Flash Cycle Done (FDONE):** The SPI controller sets this bit to 1'b1 when the SPI Cycle completes after software previously set the FGO bit. This bit remains asserted until cleared by software writing a 1'b1 or hardware reset. **Power Well:** EPW

10.10.3 HSFCTL (Hardware_Sequencing_Flash_Control_sec)—Offset 1006h

Hardware sequencing flash control

Access Method

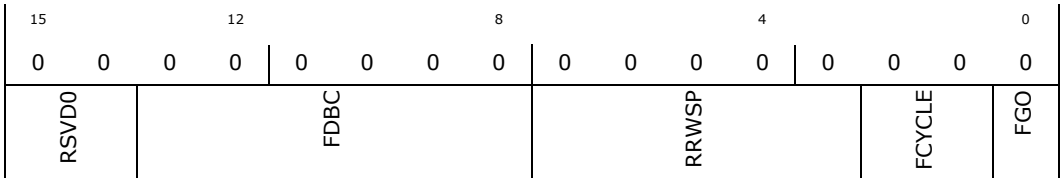
Type: Message Bus Register (Size: 16 bits)

Offset: [Port: 0x51] + 1006h

Op Codes:

h - Read, h - Write

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
13:8	0x0 RW	**Flash Data Byte Count (FDBC):** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The contents of this register are 0s based with 6'b000000 representing 1 byte and 6'b111111 representing 64 bytes. The number of bytes transferred is the value of this field plus 1. This field is ignored for the Block Erase command. **Power Well:** EPW
7:3	0x0 RW	**Reserved RW Scratch Pad (RRWSP):** Scratch Pad bits that are R/W to be used during ECO **Power Well:** EPW
2:1	0x0 RW	**Flash Cycle (FCYCLE):** This field defines the Flash SPI cycle type generated to the FLASH when the FGO bit is set as defined below: 00 Read (1 up to 64 bytes by setting FDBC) 01 Reserved 10 Write (1 up to 64 bytes by setting FDBC) 11 Block Erase Implementation Note: if reserved 2'b01 is programmed to this field, flash controller will handle it as if it is 2'b00 (Read) **Power Well:** EPW
0	0x0 RW/SE	**Flash Cycle Go (FGO):** A write to this register with a 1'b1 in this bit initiates a request to the Flash SPI Arbiter to start a cycle. This register is cleared by hardware when the cycle is granted by the SPI arbiter to run the cycle on the SPI bus. When the cycle is complete, the FDONE bit is set. Software is forbidden to write to any register in the HSFLCTL register between the FGO bit getting set and the FDONE bit being cleared. Any attempt to violate this rule will be ignored by hardware. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1'b1. This saves an additional memory write. This bit always returns 0 on reads. **Power Well:** EPW

10.10.4 FADDR (Flash_Address_sec)—Offset 1008h

Flash address

Access Method

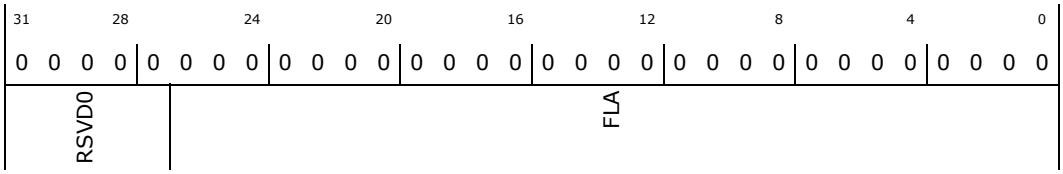
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1008h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**RSVD0:** Reserved
26:0	0x0 RW	**Flash Linear Address (FLA):** The FLA is the starting byte linear address of a SPI Read or Write cycle or an address within a Block for the Block Erase command. The Flash Linear Address must fall within a region for which SEC has access permissions. Hardware must convert the FLA into a Flash Physical Address (FPA) before running this cycle on the SPI bus. Only 24 bits are used for the SPI address (3 Byte address mode only). **Power Well:** EPW

10.10.5 FDATA0 (Flash_Data_0_sec)—Offset 1010h

Flash data #0

Access Method

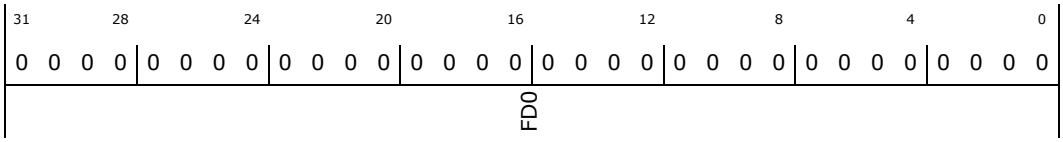
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1010h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 0 (FD0):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- 8-23-22- 16-31 24 Bit 24 is the last bit shifted out/in. There are no alignment assumptions, byte 0 always represents the value specified by the cycle address. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register. **Power Well:** EPW

10.10.6 FDATA1 (Flash_Data_1_sec)—Offset 1014h

Flash data #1

Access Method

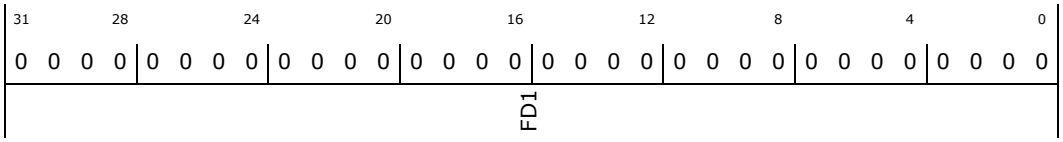
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1014h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 1 (FD1):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD[lb]0[rb] has completely shifted in/out. **Power Well:** EPW

10.10.7 FDATA2 (Flash_Data_2_sec)—Offset 1018h

Flash data #2

Access Method

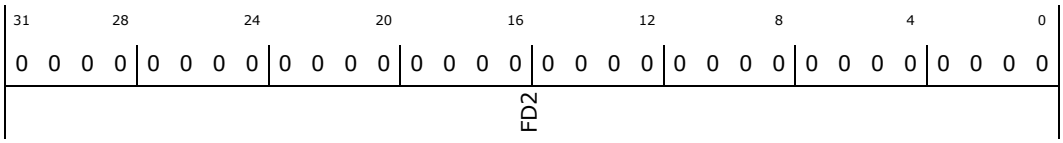
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1018h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 2 (FD2):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD[lb]1[rb] has completely shifted in/out. **Power Well:** EPW

10.10.8 FDATA3 (Flash_Data_3_sec)—Offset 101Ch

Flash data #3

Access Method

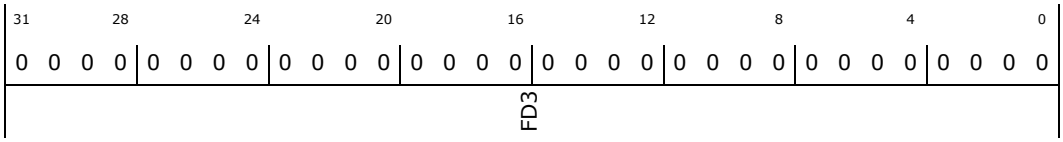
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 101Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 3 (FD3):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD[lb]2[rb] has completely shifted in/out. **Power Well:** EPW

10.10.9 FDATA4 (Flash_Data_4_sec)—Offset 1020h

Flash data #4

Access Method

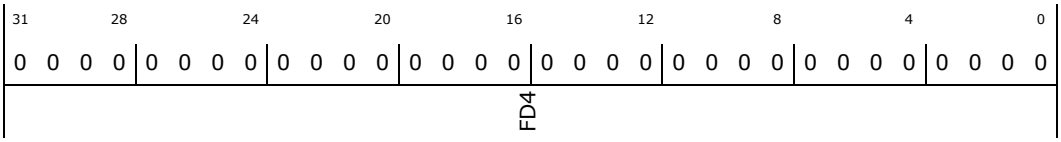
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1020h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 4 (FD4):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD[lb]3[rb] has completely shifted in/out. **Power Well:** EPW

10.10.10 FDATA5 (Flash_Data_5_sec)—Offset 1024h

Flash data #5

Access Method

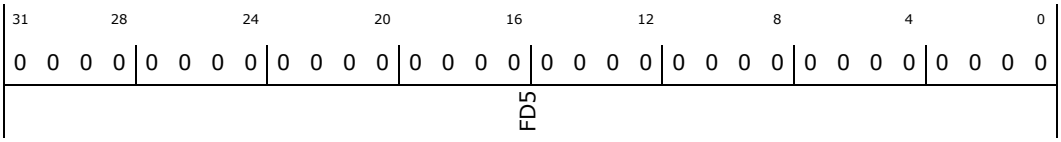
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1024h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 5 (FD5):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD[lb]4[rb] has completely shifted in/out. **Power Well:** EPW

10.10.11 FDATA6 (Flash_Data_6_sec)—Offset 1028h

Flash data #6

Access Method

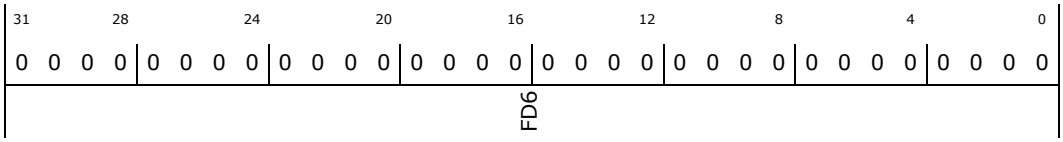
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1028h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 6 (FD6):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD[lb]5[rb] has completely shifted in/out. **Power Well:** EPW

10.10.12 FDATA7 (Flash_Data_7_sec)—Offset 102Ch

Flash data #7

Access Method

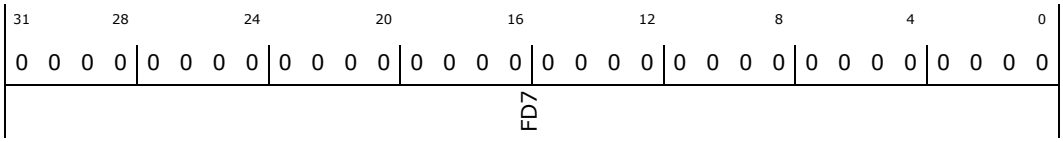
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 102Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 7 (FD7):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD[lb]6[rb] has completely shifted in/out. **Power Well:** EPW

10.10.13 FDATA8 (Flash_Data_8_sec)—Offset 1030h

Flash data #8

Access Method

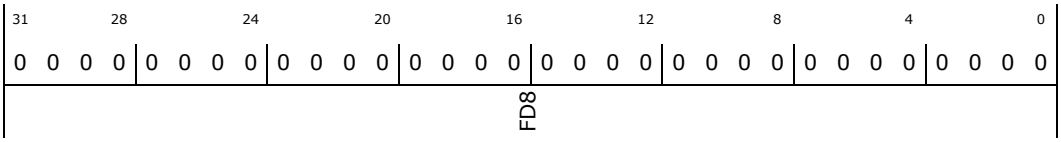
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1030h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 8 (FD8):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD[lb]7[rb] has completely shifted in/out. **Power Well:** EPW

10.10.14 FDATA9 (Flash_Data_9_sec)—Offset 1034h

Flash data #9

Access Method

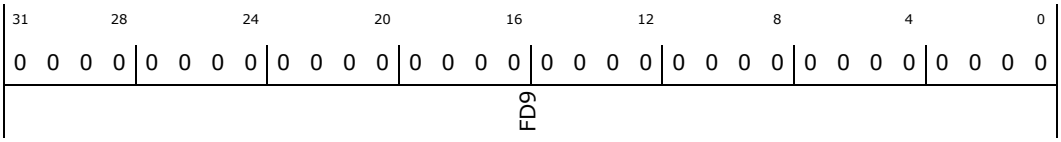
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1034h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 9 (FD9):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD[lb]8[rb] has completely shifted in/out. **Power Well:** EPW

10.10.15 FDATA10 (Flash_Data_10_sec)—Offset 1038h

Flash data #10

Access Method

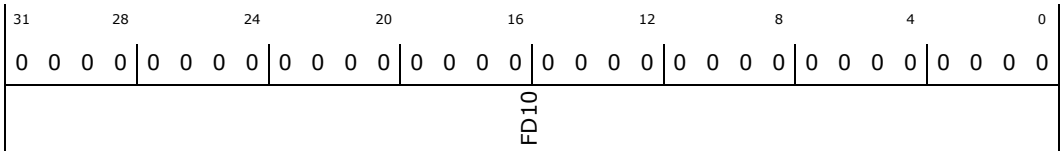
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1038h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 10 (FD10):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD[lb]9[rb] has completely shifted in/out. **Power Well:** EPW

10.10.16 FDATA11 (Flash_Data_11_sec)—Offset 103Ch

Flash data #11

Access Method

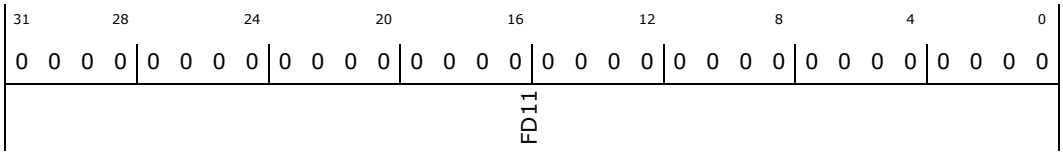
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 103Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 11 (FD11):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD[lb]10[rb] has completely shifted in/out. **Power Well:** EPW

10.10.17 FDATA12 (Flash_Data_12_sec)—Offset 1040h

Flash data #12

Access Method

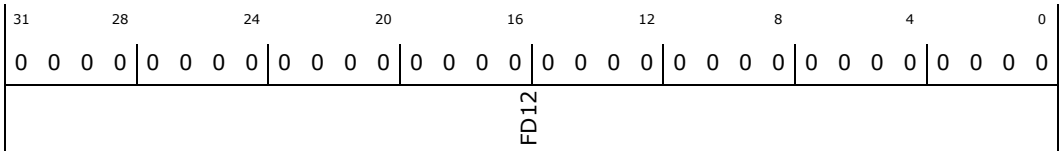
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1040h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 12 (FD12):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD[lb]11[rb] has completely shifted in/out. **Power Well:** EPW

10.10.18 FDATA13 (Flash_Data_13_sec)—Offset 1044h

Flash data #13

Access Method

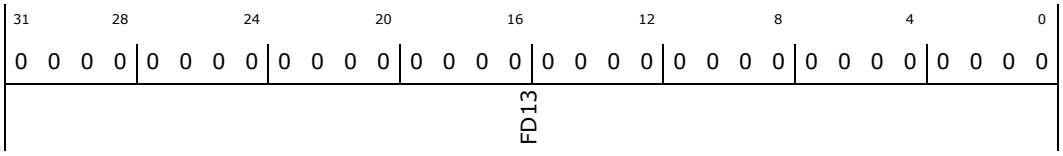
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1044h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 13 (FD13):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD[lb]12[rb] has completely shifted in/out. **Power Well:** EPW

10.10.19 FDATA14 (Flash_Data_14_sec)—Offset 1048h

Flash data #14

Access Method

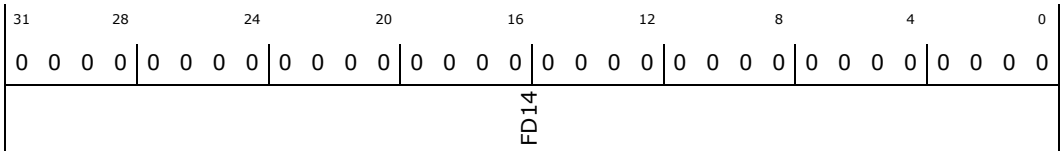
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1048h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 14 (FD14):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD[lb]13[rb] has completely shifted in/out. **Power Well:** EPW

10.10.20 FDATA15 (Flash_Data_15_sec)—Offset 104Ch

Flash data #15

Access Method

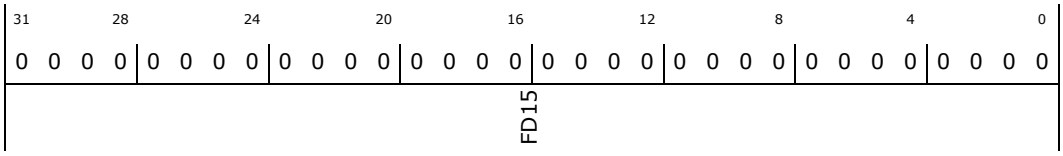
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 104Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Flash Data 15 (FD15):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD[lb]14[rb] has completely shifted in/out. **Power Well:** EPW

10.10.21 FRACC (Flash_Region_Access_Permissions_sec)—Offset 1050h

Flash region access permissions

Access Method

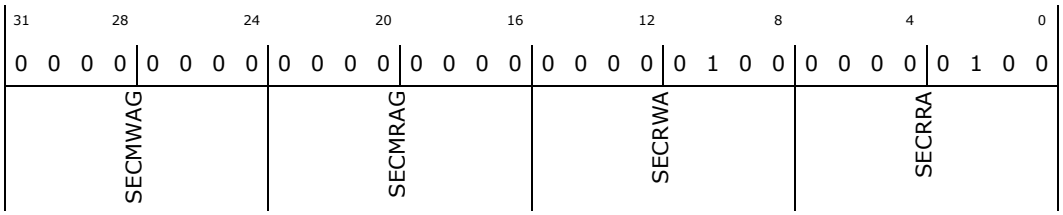
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1050h

Op Codes:

h - Read, h - Write

Default: 00000404h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW/L	**SEC Master Write Access Grant (SECMWAG):** Each bit [lb]31:29[rb] corresponds to Master[lb]7:0[rb]. SEC can grant one or more masters write access to the SEC region 2 overriding the permissions in the Flash Descriptor. Master[lb]1[rb] is Host CPU/BIOS, Master[lb]2[rb] is SEC, Master[lb]0[rb] and Master[lb]7:4[rb] are reserved. The contents of this register are locked by the FLOCKDN bit. **Power Well:** EPW
23:16	0x0 RW/L	**SEC Master Read Access Grant (SECMRAG):** Each bit [lb]28:16[rb] corresponds to Master[lb]7:0[rb]. SEC can grant one or more masters read access to the SEC region 2 overriding the read permissions in the Flash Descriptor. Master[lb]1[rb] is Host CPU/BIOS, Master[lb]2[rb] is SEC, Master[lb]0[rb] and Master[lb]7:4[rb] are reserved. The contents of this register are locked by the FLOCKDN bit. **Power Well:** EPW
15:8	0x4 RO	**SEC Region Write Access (SECRWA):** Each bit [lb]15:8[rb] corresponds to Regions [lb]7:0[rb]. If the bit is set, this master can erase and write that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 2.Master Region Write Access OR a particular master has granted SEC write permissions in their Master Write Access Grant register OR the Flash Descriptor Security Override strap is set. SEC always have the write access to its own Region 2 by default. Thus, the reset default of this field will be read as 8'h04 regardless of descriptor or non-descriptor mode. **Power Well:** EPW
7:0	0x4 RO	**SEC Region Read Access (SECRRA):** Each bit [lb]7:0[rb] corresponds to Regions [lb]7:0[rb]. If the bit is set, this master can read that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 2.Master Region Write Access OR a particular master has granted SEC read permissions in their Master Read Access Grant register OR the Flash Descriptor Security Override strap is set. SEC always have the read access to its own Region 2 by default. Thus, the reset default of this field will be read as 8'h04 regardless of descriptor or non-descriptor mode. **Power Well:** EPW

10.10.22 FREG0 (Flash_Region_0_sec)—Offset 1054h

Flash region 0 (flash descriptor)

Access Method

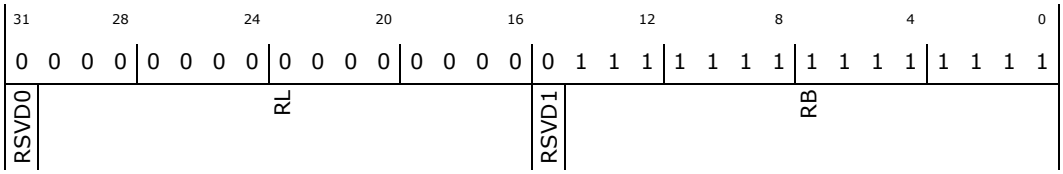
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1054h

Op Codes:

h - Read, h - Write

Default: 00007FFFh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RSVD0:** Reserved
30:16	0x0 RO	**Region Limit (RL):** This specifies address bits 26:12 for the Region 0 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Limit **Power Well:** EPW
15	0x0 RO	**RSVD1:** Reserved
14:0	0x7fff RO	**Region Base (RB):** This specifies address bits 26:12 for the Region 0 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Base **Power Well:** EPW

10.10.23 FREG1 (Flash_Region_1_sec)—Offset 1058h

Flash region 1 (BIOS)

Access Method

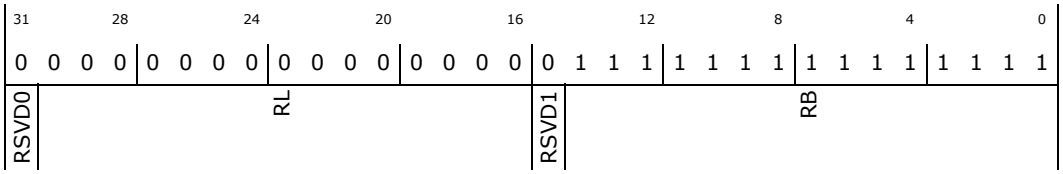
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1058h

Op Codes:

h - Read, h - Write

Default: 00007FFFh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RSVD0:** Reserved
30:16	0x0 RO	**Region Limit (RL):** This specifies address bits 26:12 for the Region 1 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit **Power Well:** EPW
15	0x0 RO	**RSVD1:** Reserved
14:0	0x7fff RO	**Region Base (RB):** This specifies address bits 26:12 for the Region 1 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base **Power Well:** EPW

10.10.24 FREG2 (Flash_Region_2_sec)—Offset 105Ch

Flash region 2 (SEC)

Access Method

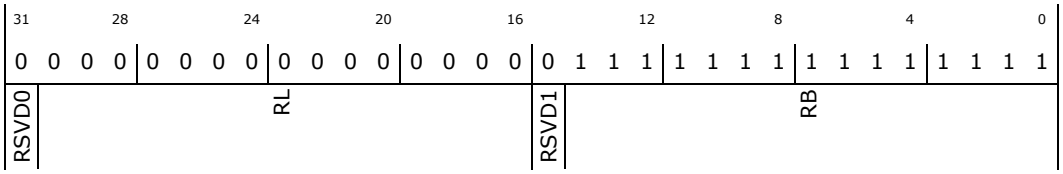
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 105Ch

Op Codes:

h - Read, h - Write

Default: 00007FFFh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
30:16	0x0 RO	**Region Limit (RL):** This specifies address bits 26:12 for the Region 2 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Limit **Power Well:** EPW
15	0x0 RO	**RSVD1:** Reserved
14:0	0x7fff RO	**Region Base (RB):** This specifies address bits 26:12 for the Region 2 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Base **Power Well:** EPW

10.10.25 FREG3 (Flash_Region_3_sec)—Offset 1060h

Flash region 3

Access Method

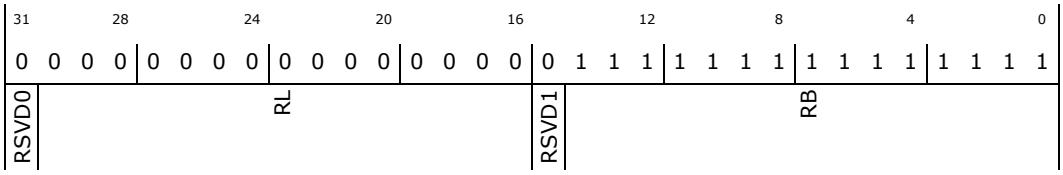
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1060h

Op Codes:

h - Read, h - Write

Default: 00007FFFh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RSVD0:** Reserved
30:16	0x0 RO	**Region Limit (RL):** This specifies address bits 26:12 for the Region 3 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Limit **Power Well:** EPW
15	0x0 RO	**RSVD1:** Reserved
14:0	0x7fff RO	**Region Base (RB):** This specifies address bits 26:12 for the Region 3 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Base **Power Well:** EPW

10.10.26 FREG4 (Flash_Region_4_sec)—Offset 1064h

Flash region 4 (platform data)

Access Method

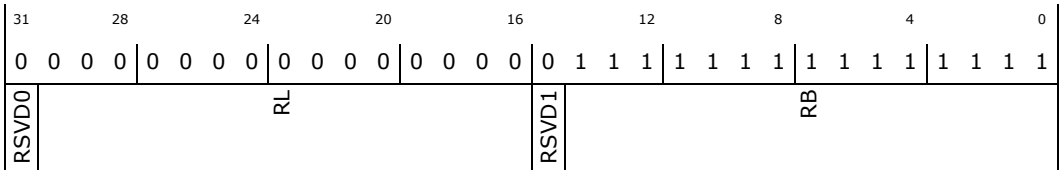
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1064h

Op Codes:

h - Read, h - Write

Default: 00007FFFh



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RSVD0:** Reserved
30:16	0x0 RO	**Region Limit (RL):** This specifies address bits 26:12 for the Region 4 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Limit **Power Well:** EPW
15	0x0 RO	**RSVD1:** Reserved
14:0	0x7fff RO	**Region Base (RB):** This specifies address bits 26:12 for the Region 4 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Base **Power Well:** EPW

10.10.27 PR0 (Protected_Range_0_sec)—Offset 1074h

Protected range #0. This register can not be written when the FLOCKDN bit is set to 1.

Access Method

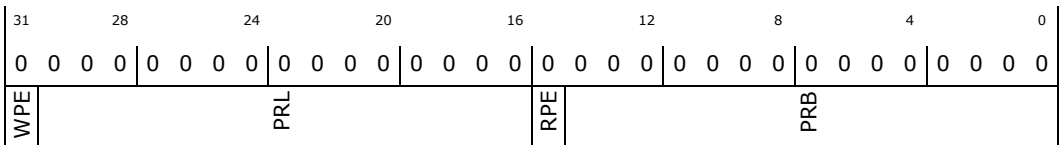
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1074h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Power Well:** EPW
30:16	0x0 RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. **Power Well:** EPW
15	0x0 RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Power Well:** EPW
14:0	0x0 RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. **Power Well:** EPW

10.10.28 PR1 (Protected_Range_1_sec)—Offset 1078h

Protected range #1. This register can not be written when the FLOCKDN bit is set to 1.

Access Method

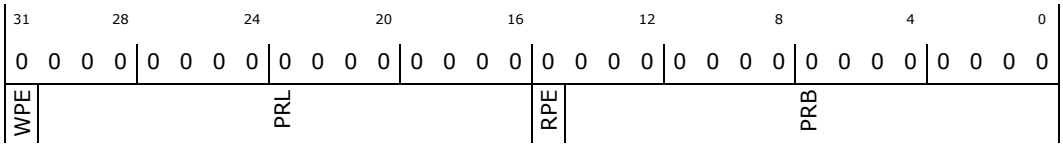
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1078h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Power Well:** EPW
30:16	0x0 RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. **Power Well:** EPW
15	0x0 RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Power Well:** EPW
14:0	0x0 RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. **Power Well:** EPW

10.10.29 PR2 (Protected_Range_2_sec)—Offset 107Ch

Protected range #2. This register can not be written when the FLOCKDN bit is set to 1.

Access Method

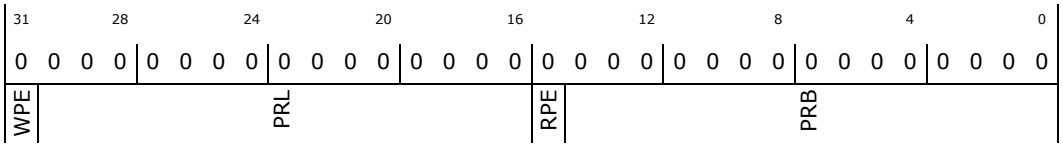
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 107Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Power Well:** EPW
30:16	0x0 RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. **Power Well:** EPW
15	0x0 RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Power Well:** EPW
14:0	0x0 RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. **Power Well:** EPW

10.10.30 PR3 (Protected_Range_3_sec)—Offset 1080h

Protected range #3. This register can not be written when the FLOCKDN bit is set to 1.

Access Method

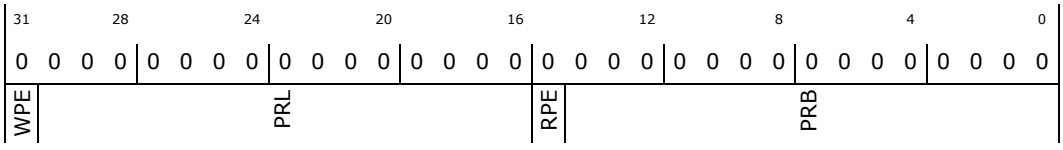
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1080h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Power Well:** EPW
30:16	0x0 RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. **Power Well:** EPW
15	0x0 RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Power Well:** EPW
14:0	0x0 RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. **Power Well:** EPW

10.10.31 PR4 (Protected_Range_4_sec)—Offset 1084h

Protected range #4. This register can not be written when the FLOCKDN bit is set to 1.

Access Method

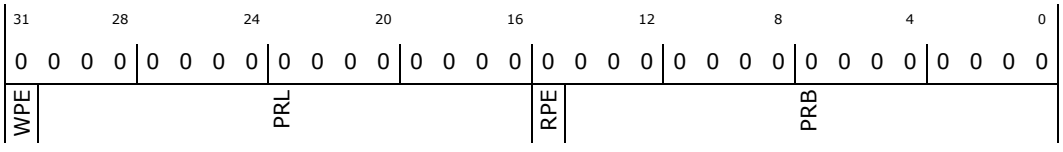
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1084h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Power Well:** EPW
30:16	0x0 RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. **Power Well:** EPW
15	0x0 RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. **Power Well:** EPW
14:0	0x0 RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. **Power Well:** EPW

10.10.32 SSFCTLSTS (Software_Sequencing_Flash_Control_Status_sec)—Offset 1090h

The software sequencing flash control and Status register is a combination of two registers the software sequencing flash status register (bits 7:0) and the software sequencing flash control register (bits 31:8). This register is intended to be used only as a back-up mode to the hardware sequencing control and status registers.

Access Method

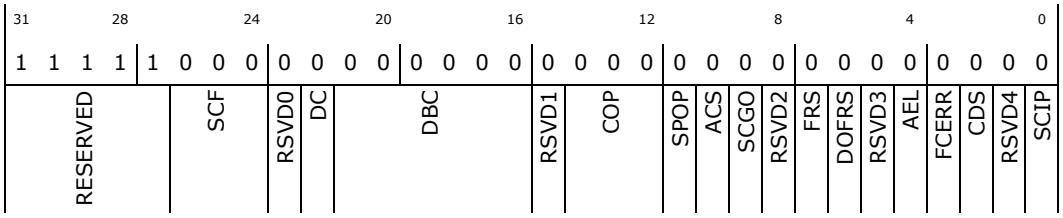
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1090h

Op Codes:

h - Read, h - Write

Default: F8000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x1f RO	**RESERVED:** reserved, should be with default 1 **Power Well:** EPW
26:24	0x0 RW/L	**SPI Cycle Frequency (SCF):** 000 : 20MHz 001 : 33MHz 010 : 66MHz 011 : 25MHz 100 : 50MHz All Others: Reserved This register sets frequency to use for all SPI Software Sequencing cycles (write, erase, fast read, read status, .etc) except for the Read cycle which always run at 20MHz. This register is locked when the SPI Configuration Lock-Down bit is set. **Power Well:** EPW
23	0x0 RO	**RSVD0:** Reserved
22	0x0 RW	**Data Cycle (DC):** When set to 1, there is data that corresponds to this transaction. When 0, no data is dleivered for this cycle, and the DBC and data fields themselves are don t cares. **Power Well:** EPW
21:16	0x0 RW	**Data Byte Count (DBC):** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The valid settings (in decimal) are any value from 0 to 63. The number of bytes transferred is the value of this field plus 1. Note that when this field is 00_0000b, then there is 1 byte to transfer and that 11_1111b means there are 64 bytes to transfer. **Power Well:** EPW
15	0x0 RO	**RSVD1:** Reserved
14:12	0x0 RW	**Cycle Opcode Pointer (COP):** This field selects one of the programmed opcodes in the Opcode Menu to be used as the SPI Command/Opcode. In the case of an Atomic Cycle Sequence, this determines the second command. **Power Well:** EPW
11	0x0 RW	**Sequence Prefix Opcode Pointer (SPOP):** This field selects one of the two programmed prefix opcodes for use when performing an Atomic Cycle Sequence. A value of 0 points to the opcode in the least significant byte of the Prefix Opcodes register. By making this programmable, the SPI controller supports flash devices that have different opcodes for enabling writes to the data space vs. status register. **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RW	**Atomic Cycle Sequence (ACS):** When set to 1 along with the SCGO assertion, the SPI controller will execute a sequence of commands on the SPI interface without allowing the LAN component to arbitrate and interleave cycles. The sequence is composed of:) Atomic Sequence Prefix Command (8-bit opcode only)) Primary Command specified below by software (can include address and data)) Polling the Flash Status Register (opcode 8'h05) until bit 0 becomes 1'b0. The SPI Cycle in Progress bit remains set and the Cycle Done Status bit remains unset until the Busy bit in the Flash Status Register returns 0. **Power Well:** EPW
9	0x0 RW/SE	**SPI Cycle Go (SCGO):** This bit always returns 1'b0 on reads. However, a write to this register with a 1'b1 in this bit starts the SPI cycle defined by the other bits of this register. The SPI Cycle in Progress (SCIP) bit gets set by this action. Hardware must ignore writes to this bit while the Cycle In Progress bit is set. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1'b1. This saves an additional memory write. **Power Well:** EPW
8	0x0 RO	**RSVD2:** Reserved
7	0x0 RO/U	**Fast Read Supported (FRS):** This bit reflects the value of the Fast Read Support bit in the Flash Descriptor Component Section. **Power Well:** EPW
6	0x0 RO/U	**Dual Output Fast Read Supported (DOFRS):** This bit reflects the value of the Dual Output Fast Read Support bit in the Flash Descriptor Component Section. **Power Well:** EPW
5	0x0 RO	**RSVD3:** Reserved
4	0x0 RO	**Access Error Log (AEL):** This bit reflects the value of the Hardware Sequencing Status.AEL register. **Power Well:** EPW
3	0x0 RW/1C	**Flash Cycle Error (FCERR):** Hardware sets this bit to 1'b1 when a programmed access is blocked from running on the SPI interface due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1'b1 or hardware reset. **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW/1C	**Cycle Done Status (CDS):** The SPI controller sets this bit to 1'b1 when the SPI Cycle completes i.e., SCIP bit is 1'b0) after software sets the GO bit. This bit remains asserted until cleared by software writing a 1'b1 or hardware reset. **Power Well:** EPW
1	0x0 RO	**RSVD4:** Reserved
0	0x0 RO	**SPI Cycle In Progress (SCIP):** Hardware sets this bit when software sets the SPI Cycle Go bit in the Command register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 1'b0. **Power Well:** EPW

10.10.33 PREOP (Prefix_Opcode_Configuration_sec)—Offset 1094h

Prefix opcode configuration. This register is not writable when the SPI Configuration Lock-Down bit is set.

Access Method

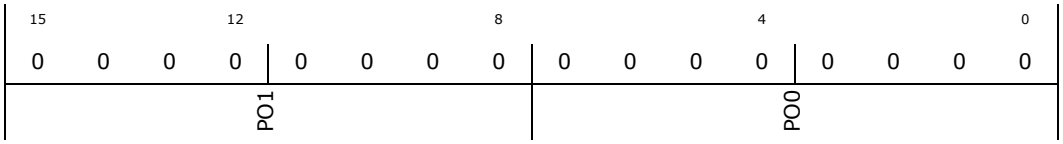
Type: Message Bus Register (Size: 16 bits)

Offset: [Port: 0x51] + 1094h

Op Codes:

h - Read, h - Write

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RW/L	**Prefix Opcode 1 (PO1):** Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence. **Power Well:** EPW
7:0	0x0 RW/L	**Prefix Opcode 0 (PO0):** Prefix Opcode 0: Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence. **Power Well:** EPW

10.10.34 OPTYPE (Opcode_Type_Configuration_sec)—Offset 1096h

Opcode type configuration. This register is not writable when the Flash Configuration Lock-Down bit is set. Entries in this register correspond to the entries in the Opcode Menu Configuration register. Note that the definition below only provides write protection for opcodes that have addresses associated with them. Therefore, any erase or write opcodes that do not use an address should be avoided (for example, Chip Erase and Auto-Address Increment Byte Program).

Access Method

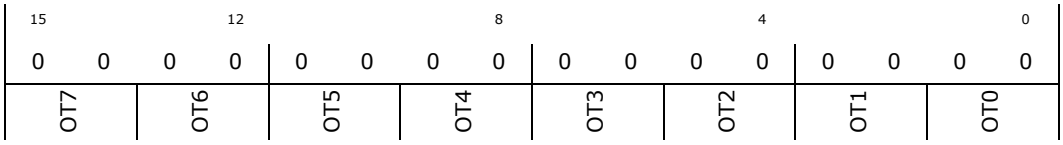
Type: Message Bus Register (Size: 16 bits)

Offset: [Port: 0x51] + 1096h

Op Codes:

h - Read, h - Write

Default: 0000h



Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RW/L	**Opcode Type 7 (OT7):** Refer the description for bits 1:0 **Power Well:** EPW
13:12	0x0 RW/L	**Opcode Type 6 (OT6):** Refer the description for bits 1:0 **Power Well:** EPW
11:10	0x0 RW/L	**Opcode Type 5 (OT5):** Refer the description for bits 1:0 **Power Well:** EPW
9:8	0x0 RW/L	**Opcode Type 4 (OT4):** Refer the description for bits 1:0 **Power Well:** EPW
7:6	0x0 RW/L	**Opcode Type 3 (OT3):** Refer the description for bits 1:0 **Power Well:** EPW
5:4	0x0 RW/L	**Opcode Type 2 (OT2):** Refer the description for bits 1:0 **Power Well:** EPW
3:2	0x0 RW/L	**Opcode Type 1 (OT1):** Refer the description for bits 1:0 **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
1:0	0x0 RW/L	**Opcode Type 0 (OT0):** This field specifies information about the corresponding Opcode 0. This information allows the hardware to 1) know whether to use the address field and 2) provide BIOS and Shared Flash protection capabilities. The hardware implementation also uses the read vs. write information for modifying the behavior of the SPI interface logic. The encoding of the two bits is: 00 = No Address associated with this Opcode and Read Cycle type 01 = No Address associated with this Opcode and Write Cycle type 10 = Address required, Read cycle type 11 = Address required, Write cycle type **Power Well:** EPW

10.10.35 OPMENU0 (Opcode_Menu_Configuration_0_sec)—Offset 1098h

Opcode (0-3) Menu Configuration. This register is not writable when the SPI Configuration Lock-Down bit is set. Four entries are available in this register and four are available in OPMENU1 register to give BIOS a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices. It is recommended that BIOS avoid programming Write Enable opcodes in this menu. Malicious software could then perform writes and erases to the SPI flash without using the atomic cycle mechanism. This could cause functional failures in a shared flash environment. Write Enable opcodes should only be programmed in the Prefix Opcodes.

Access Method

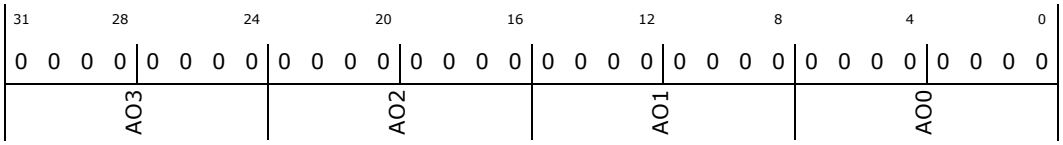
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1098h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW/L	**Allowable Opcode 3 (AO3):** Refer the description for bits 7:0 **Power Well:** EPW
23:16	0x0 RW/L	**Allowable Opcode 2 (AO2):** Refer the description for bits 7:0 **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RW/L	**Allowable Opcode 1 (AO1):** Refer the description for bits 7:0 **Power Well:** EPW
7:0	0x0 RW/L	**Allowable Opcode 0 (AO0):** Software programs an SPI opcode into this field for use when initiating SPI commands through the Control Register. **Power Well:** EPW

10.10.36 OPMENU1 (Opcode_Menu_Configuration_1_sec)—Offset 109Ch

Opcode (7-4) Menu Configuration. This register is not writable when the SPI Configuration Lock-Down bit is set. Four entries are available in this register and four are available in OPMENU0 register to give BIOS a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices. It is recommended that BIOS avoid programming Write Enable opcodes in this menu. Malicious software could then perform writes and erases to the SPI flash without using the atomic cycle mechanism. This could cause functional failures in a shared flash environment. Write Enable opcodes should only be programmed in the Prefix Opcodes.

Access Method

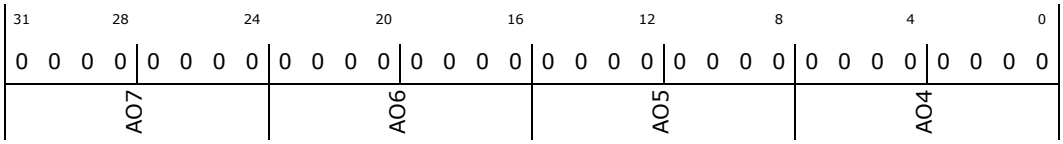
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 109Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW/L	**Allowable Opcode 7 (AO7):** Refer the description for bits 7:0 in OPMENU0 **Power Well:** EPW
23:16	0x0 RW/L	**Allowable Opcode 6 (AO6):** Refer the description for bits 7:0 in OPMENU0 **Power Well:** EPW
15:8	0x0 RW/L	**Allowable Opcode 5 (AO5):** Refer the description for bits 7:0 in OPMENU0 **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW/L	**Allowable Opcode 4 (AO4):** Refer the description for bits 7:0 in OPMENU0 **Power Well:** EPW

10.10.37 SCRATCH0 (Scratch0_sec)—Offset 10A0h

Scratch0 register

Access Method

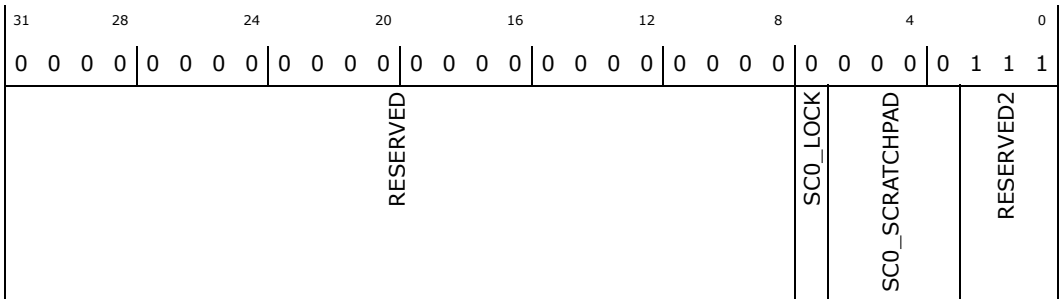
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 10A0h

Op Codes:

h - Read, h - Write

Default: 00000007h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (RESERVED):** Reserved **Power Well:** EPW
7	0x0 RW/L	**SC0_LOCK:** Scratch registers LOCK: When set to 1 it locks the SEC Scratch registers. This bit is write 1 once. Once set to 1, this bit can only be cleared by a hardware reset. **Power Well:** EPW
6:3	0x0 RW/L	**SC0_SCRATCHPAD:** Scratch register 0 Scratchpad, no effect on design **Power Well:** EPW
2:0	0x7 RO	**Reserved2 (RESERVED2):** Reserved **Power Well:** EPW

10.10.38 SCRATCH1 (Scratch1_sec)—Offset 10A4h

Scratch1 register

Access Method

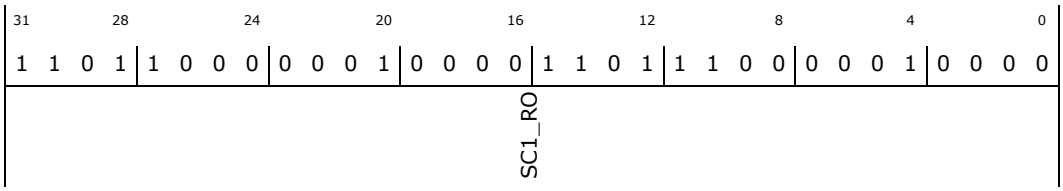
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 10A4h

Op Codes:

h - Read, h - Write

Default: D810DC10h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xd810dc10 RO	**Scratch1RO (SC1_RO):** Scratch1 read only bits **Power Well:** EPW

10.10.39 SCRATCH2 (Scratch2_sec)—Offset 10A8h

Scratch2 register

Access Method

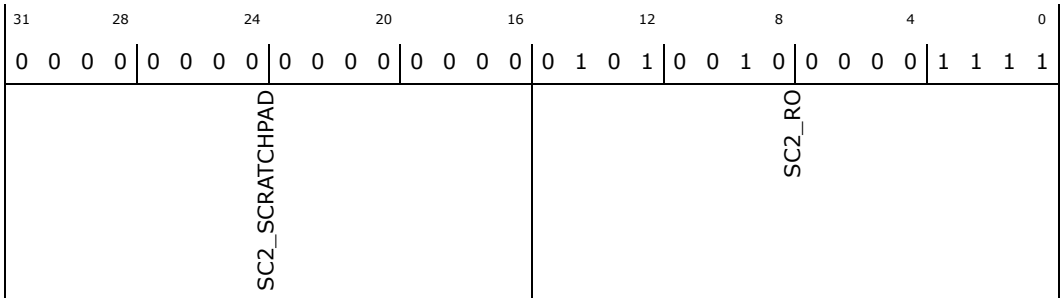
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 10A8h

Op Codes:

h - Read, h - Write

Default: 0000520Fh



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/L	**SC2_SCRATCHPAD:** Scratch register 2 Scratchpad, no effect on design **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
15:0	0x520f RO	**Scratch2RO (SC2_RO):** Scratch2 read only bits **Power Well:** EPW

10.10.40 SCRATCH3 (Scratch3_sec)—Offset 10ACh

Scratch2 register

Access Method

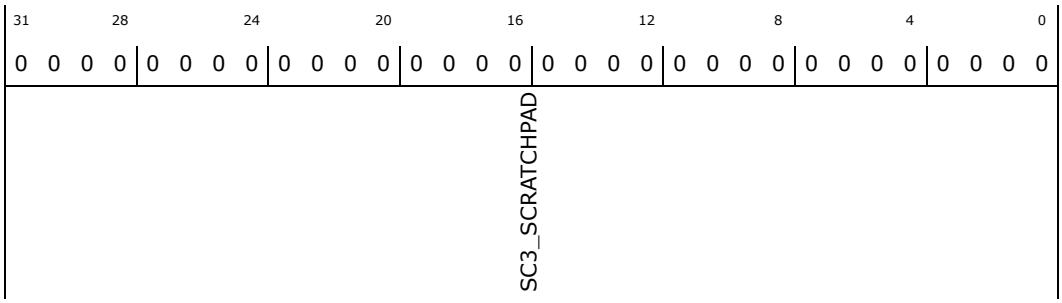
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 10ACh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/L	**SC3_SCRATCHPAD:** Scratch register 3 Scratchpad, no effect on design **Power Well:** EPW

10.10.41 VSCC0 (Lower_Vendor_Specific_Component_Capabilities_sec)—Offset 10C4h

Lower vendor specific component capabilities

Access Method

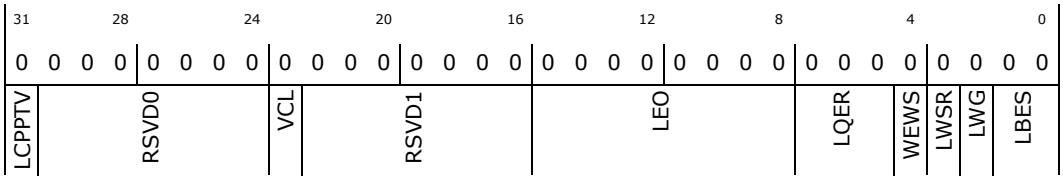
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 10C4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO/U	**Lower Component Property Parameter Table Valid (LCPPTV):** This bit is set to a 1 if the Flash Controller detects a valid SFDP Component Property Parameter Table in Component 0. **Power Well:** EPW
30:24	0x0 RO	**RSVD0:** Reserved
23	0x0 RW/L	**Vendor Component Lock (VCL):** '0': The lock bit is not set '1': The Vendor Component Lock bit is set. This register locks itself when set. If this register is not set and the Flash is operating in Flash Mode (as opposed to EEPROM mode), then software cannot use hardware sequencing. This requirement is not enforced by hardware, but is a requirement of the the power-on usage model. **Power Well:** EPW
22:16	0x0 RO	**RSVD1:** Reserved
15:8	0x0 RW/L	**Lower Erase Opcode (LEO):** This register is programed with the Flash erase instruction opcode required by this vendors Flash component. This field is used for cycles targeting addresses below the Flash Partition Address. **Power Well:** EPW
7:5	0x0 RW/L	**Lower QUAD Enable Requirements (LQER) (LQER):** 000 Part does not require a Quad Enable bit to be set, either because Quad is not supported or because the manufacturer somehow permanently enables Quad capability. 001 Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to status register clears all bits in register 2, therefore status register writes MUST be two bytes. (If the status register is unlocked and SFDP bits WSR or VSCC WSR is 1 then SoC cannot use the quad output, quad IO features of this part because the hardware will automatically write one byte of zeros to status register with every write/erase.) 010 Part requires bit 6 of status register 1 to be set to enable quad IO. If the status register is unlocked and SFDP WSR bit or VSCC WSR is 1 then SoC cannot use the quad output, quad IO features of this part because the hardware will automatically write one byte of zeros to status register with every write/erase. 011 Part requires bit 7 of the configuration register to be set to enable Quad. 100 Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to the status register does not clear the second byte. **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW/L	**Write Enable on Write Status (WEWS):** Write Enable Opcode Select for Writing to Volatile Status Register 0: 0x50 is the Opcode to enable a status register write when bit 3 is set to 1. 1: 0x06 is the Opcode to enable a status register write when bit 3 is set to 1. **Power Well:** EPW
3	0x0 RW/L	**Lower Write Status Required (LWSR):** '0' : No requirement to to write to the Write Status Register prior to a write '1' : A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This field is used for cycles targeting addresses below the Flash Partition Address. **Power Well:** EPW
2	0x0 RW/L	**Lower Write Granularity (LWG):** '0' : 1 Byte '1' : 64 Byte This field is used for cycles targeting addresses below the Flash Partition Address. **Power Well:** EPW
1:0	0x0 RW/L	**Lower Block/Sector Erase Size (LBES):** This field identifies the erasable sector size for all Flash components. Valid Bit Settings: '00' : 256 Byte '01' : 4K Byte '10' : 8K Byte '11' : 64K Byte This field is used for cycles targeting addresses below the Flash Partition Address. **Power Well:** EPW

10.10.42 VSCC1 (Upper_Vendor_Specific_Component_Capabilities_sec)—Offset 10C8h

Upper vendor specific component capabilities

Access Method

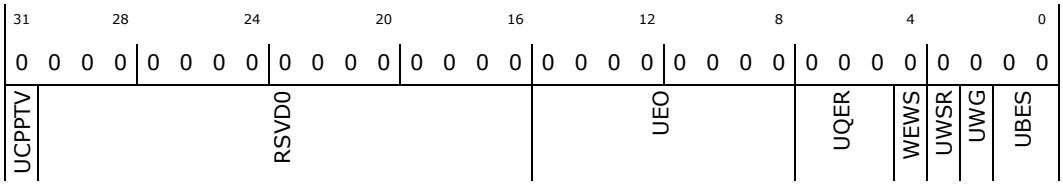
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 10C8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO/U	**Upeer Component Property Parameter Table Valid (UCPPTV):** This bit is set to a 1 if the Flash Controller detects a valid SFDP Component Property Parameter Table in Component 0. **Power Well:** EPW
30:16	0x0 RO	**RSVD0:** Reserved
15:8	0x0 RW/L	**Upper Erase Opcode (UEO):** This register is programed with the Flash erase instruction opcode required by this vendors Flash component. This field is used for cycles targeting addresses above the Flash Partition Address. **Power Well:** EPW
7:5	0x0 RW/L	**Upper QUAD Enable Requirements (UQER):** 000 Part does not require a Quad Enable bit to be set, either because Quad is not supported or because the manufacturer somehow permanently enables Quad capability. 001 Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to status register clears all bits in register 2, therefore status register writes MUST be two bytes. (If the status register is unlocked and SFDP bits WSR or VSCC WSR is 1 then SoC cannot use the quad output, quad IO features of this part because the hardware will automatically write one byte of zeros to status register with every write/erase.) 010 Part requires bit 6 of status register 1 to be set to enable quad IO. If the status register is unlocked and SFDP WSR bit or VSCC WSR is 1 then SoC cannot use the quad output, quad IO features of this part because the hardware will automatically write one byte of zeros to status register with every write/erase. 011 Part requires bit 7 of the configuration register to be set to enable Quad. 100 Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to the status register does not clear the second byte. **Power Well:** EPW
4	0x0 RW/L	**Write Enable on Write Status (WEWS):** Write Enable Opcode Select for Writing to Volatile Status Register 0: 0x50 is the Opcode to enable a status register write when bit 3 is set to 1. 1: 0x06 is the Opcode to enable a status register write when bit 3 is set to 1. **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW/L	**Upper Write Status Required (UWSR):** '0': No requirement to to write to the Write Status Register prior to a write '1': A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This field is used for cycles targeting addresses above the Flash Partition Address. **Power Well:** EPW
2	0x0 RW/L	**Upper Write Granularity (UWG):** '0' : 1 Byte '1' : 64 Byte This field is used for cycles targeting addresses above the Flash Partition Address. **Power Well:** EPW
1:0	0x0 RW/L	**Upper Block/Sector Erase Size (UBES):** This field identifies the erasable sector size for all Flash components. Valid Bit Settings: '00' : 256 Byte '01' : 4K Byte '10' : 8K Byte '11' : 64K Byte This field is used for cycles targeting addresses above the Flash Partition Address. **Power Well:** EPW

10.10.43 PTINX (Parameter_Table_Index_sec)—Offset 10CCh

Parameter table index

Access Method

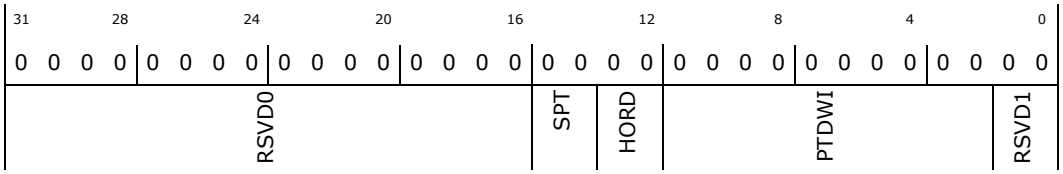
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 10CCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:14	0x0 RW	**Supported parameter table (SPT):** 00 : Component 0 Property Parameter Table 01 : Component 1 Property Parameter Table 10 ? 11 : Reserved **Power Well:** EPW
13:12	0x0 RW	**Header or Data (HORD):** 00 : SFDP Header 01 : Parameter Table Header 10 : Data 11 : Reserved **Power Well:** EPW
11:2	0x0 RW	**Parameter Table DW Index (PTDWI):** Selects the DW offset within the parameter table to observe **Power Well:** EPW
1:0	0x0 RO	**RSVD1:** Reserved

10.10.44 PTDATA (Parameter_Table_Data_sec)—Offset 10D0h

Parameter table data

Access Method

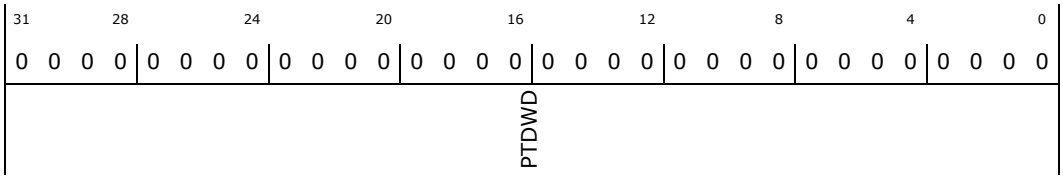
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 10D0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO/U	**Supported parameter table (PTDWD):** Returns the DW of data to observe as selected in the Parameter Table Index register. **Power Well:** EPW

10.10.45 FPB (Flash_Partition_Boundary_sec)—Offset 10D4h

Flash partition boundary

Access Method

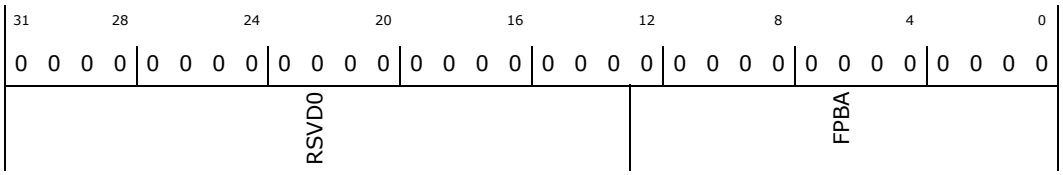
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 10D4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RSVD0:** Reserved
12:0	0x0 RO/U	**Flash Partition Boundary Address (FPBA):** This register reflects the value of the Flash Descriptor Component FPBA field **Power Well:** EPW

10.10.46 ICE (Interrupt_Cause_Enable_sec)—Offset 10F0h

Interrupt cause enable

Access Method

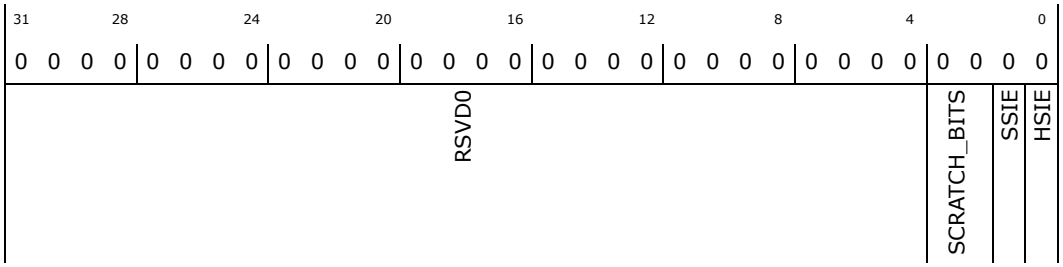
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 10F0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RSVD0:** Reserved
3:2	0x0 RW	**Scratchpad (SCRATCH_BITS):** Scratchpad bits **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**Software Sequencing Interrupt Enable (SSIE):** When 1'b1, an interrupt will be sent with cause value set to 0x00 whenever the Software Sequencing Interrupt Status register is set to 1'b1. **Power Well:** EPW
0	0x0 RW	**Hardware Sequencing Interrupt Enable (HSIE):** When 1'b1, an interrupt will be sent with cause value set to 0x01 whenever the Hardware Sequencing Interrupt Status register is set to 1'b1. **Power Well:** EPW

10.10.47 ICS (Interrupt_Cause_Status_sec)—Offset 10F4h

Interrupt cause status

Access Method

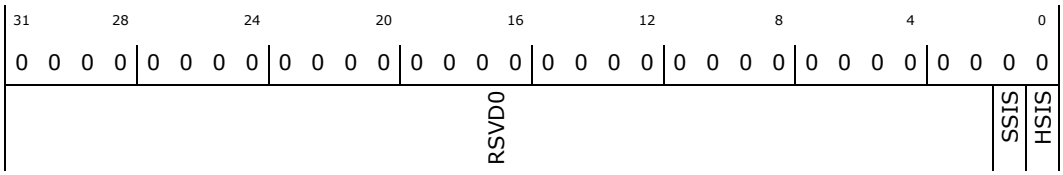
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 10F4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**RSVD0:** Reserved
1	0x0 RW/1C	**Software Sequencing Interrupt Status (SSIS):** This register is set to 1'b1 whenever the Software Sequencing.Cycle Done status register is set to a 1'b1. This register is cleared by hardware when interrupt is enabled and the interrupt is sent. If interrupt is not enabled, then firmware will clear this register. **Power Well:** EPW
0	0x0 RW/1C	**Hardware Sequencing Interrupt Status (HSIS):** This register is set to 1'b1 whenever the Hardware Sequencing.Flash Cycle Done status register is set to a 1'b1. This register is cleared by hardware when interrupt is enabled and the interrupt is sent. If interrupt is not enabled, then firmware will clear this register. **Power Well:** EPW

10.10.48 IADD (Interrupt_Address_sec)—Offset 10F8h

Interrupt Address. Controls the destination ID and the address should be use by SEC interrupt SB message

Access Method

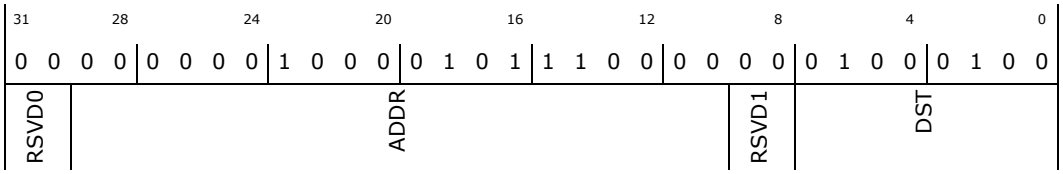
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 10F8h

Op Codes:

h - Read, h - Write

Default: 0085C044h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**RSVD0:** Reserved
29:10	0x2170 RW	**Address (ADDR):** Address should be used in the SEC interrupt message. **Power Well:** EPW
9:8	0x0 RO	**RSVD1:** Reserved
7:0	0x44 RW	**Destination ID (DST):** Address should be used in the SEC interrupt message. **Power Well:** EPW

10.10.49 SECCTRL (SEC_Flash_Control_sec)—Offset 10FCh

SEC flash control

Access Method

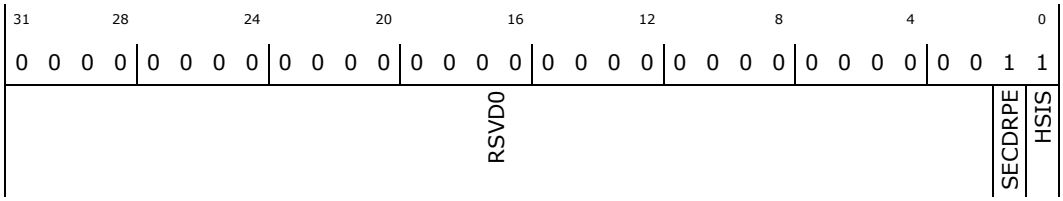
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 10FCh

Op Codes:

h - Read, h - Write

Default: 00000003h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**RSVD0:** Reserved
1	0x1 RW	**SEC Direct Read Prefetch Enable (SECDRPE):** When set to a 1'b1, SEC direct read are prefetched in the flash controller. This bit has no meaning if SEC cache is disable. **Power Well:** EPW
0	0x1 RW	**SEC Direct Read Cache Enable (HSIS):** When set to a 1'b1, SEC direct read are cached in the flash controller .Note that if SEC direct read caching is disabled while data has already been cached internally, subsequent SEC direct reads will continue to return data from the cache until the cache is invalidated. **Power Well:** EPW

10.10.50 ERE (Erase_range_enable)—Offset 1100h

Erase range enable. Enable the security check of the matched opcode. security usage.

Access Method

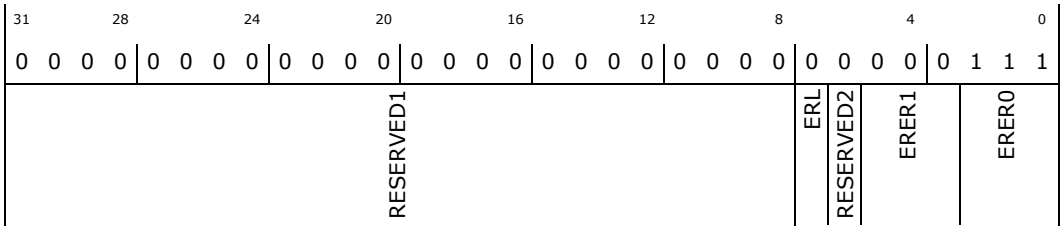
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x51] + 1100h

Op Codes:

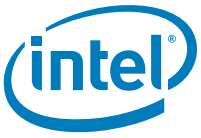
h - Read, h - Write

Default: 00000007h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (RESERVED1):** Reserved **Power Well:** EPW

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW/L	**ERL:** Erase Range LOCK: When set to 1 it locks the Erase Range registers. This bit is write 1 once. Once set to 1, this bit can only be cleared by a hardware reset. **Power Well:** EPW
6	0x0 RW/L	**Reserved (RESERVED2):** Reserved. NOTE: This bit is locked when Erase Range LOCK is set to 1 **Power Well:** EPW
5:3	0x0 RW/L	**ERER1:** Erase Range Enable Register: Defines whether erase ranges 5 to 3 are active. Both the softstrap (Erase Range check Enable) AND this register must be enabled to enable the erase range check. NOTE: These bits are locked when Erase Range LOCK is set to 1 **Power Well:** EPW
2:0	0x7 RO	**ERER0:** EraErase Range Enable Register: Defines whether erase ranges 2 to 0 are active NOTE: Erase Ranges 2:0 can only be disabled by SPI Flash Erase Range Disable 2:0 softstraps. **Power Well:** EPW



10.11 PCU iLB UART I/O Registers

Table 106. Summary of PCU iLB UART I/O Registers—

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3F8–3F8h	1	"Receiver Buffer / Transmitter Holding Register (COM1_Rx_Tx_Buffer)—Offset 3F8h" on page 5749	00h
3F9–3F9h	1	"Interrupt Enable Register (COM1_IER)—Offset 3F9h" on page 5750	00h
3FA–3FAh	1	"Interrupt Identification / FIFO Control Register (COM1_IIR)—Offset 3FAh" on page 5751	01h
3FB–3FBh	1	"Line Control Register (COM1_LCR)—Offset 3FBh" on page 5753	00h
3FC–3FCh	1	"Modem Control Register (COM1_MCR)—Offset 3FCh" on page 5754	00h
3FD–3FDh	1	"Line Status Register (COM1_LSR)—Offset 3FDh" on page 5756	60h
3FE–3FEh	1	"Modem Status Register (COM1_MSR)—Offset 3FEh" on page 5757	00h
3FF–3FFh	1	"Scratchpad Register (COM1_SCR)—Offset 3FFh" on page 5759	00h

10.11.1 Receiver Buffer / Transmitter Holding Register (COM1_Rx_Tx_Buffer)—Offset 3F8h

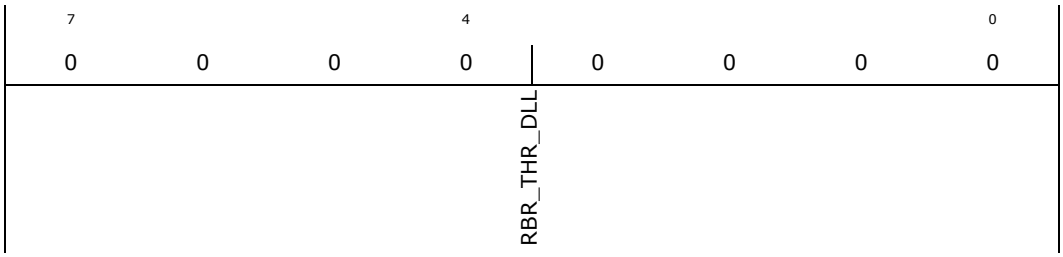
This register is a combination of three registers: the receiver buffer register (RBR) that is a read-only register when DLAB=0, the transmitter holding register (THR) that is a write-only register when DLAB=0 and the divisor latch LSB (DLL) register when DLAB=1.

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 3F8h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**Receiver buffer / transmitter holding (RBR_THR_DLL): When reading from this register and DLAB=1'b0**, it contains the byte received if no FIFO is used, or the oldest unread byte with FIFO's. If FIFO buffering is used, each new read action of the register will return the next byte, until no more bytes are present. Bit 0 in the LSR line status register can be used to check if all received bytes have been read. This bit will change to zero if no more bytes are present. **When writing to this register and DLAB=1'b0**, it is used to buffer outgoing characters. If no FIFO buffering is used, only one character can be stored. Otherwise the amount of characters depends on the type of UART. Bit 5 in the LSR, line status register can be used to check if new information must be written to this register. The value 1'b1 indicates that the register is empty. If FIFO buffering is used, more than one character can be written to the transmitter holding register when the bit signals an empty state. There is no indication of the amount of bytes currently present in the transmitter FIFO. This register is not used to transfer the data directly. The byte is first transferred to a shift register where the information is broken in single bits which are sent one by one. **If DLAB=1'b1**, this register is used as DLL (Divisor Latch LSB). For generating its timing information, each UART uses an oscillator generating a frequency of about 1.8432 MHz. This frequency is divided by 16 to generate the time base for communication. Because of this division, the maximum allowed communication speed is 115200 bps. Modern UARTS like the 16550 are capable of handling higher input frequencies up to 24 MHz which makes it possible to communicate with a maximum speed of 1.5 Mbps. On PC's higher frequencies than the 1.8432 MHz are rarely seen because this would be software incompatible with the original XT configuration. This 115200 bps communication speed is not suitable for all applications. To change the communication speed, the frequency can be further decreased by dividing it by a programmable value. For very slow communications, this value can go beyond 255. Therefore, the divisor is stored in two separate bytes, the divisor latch registers DLL and DLM which contain the least, and most significant byte. For error free communication, it is necessary that both the transmitting and receiving UART use the same time base. Default values have been defined which are commonly used. The table shows the most common values with the appropriate settings of the divisor latch bytes. Note that these values only hold for a PC compatible system where a clock frequency of 1.8432 MHz is used. Speed(bps) Divisor DLL DLM 50 2,304 0x00 0x09 300 384 0x80 0x01 1,200 96 0x60 0x00 2,400 48 0x30 0x00 4,800 24 0x18 0x00 9,600 12 0x0C 0x00 19,200 6 0x06 0x00 38,400 3 0x03 0x00 57,600 2 0x02 0x00 115,200 1 0x01 0x00

10.11.2 Interrupt Enable Register (COM1_IER)—Offset 3F9h

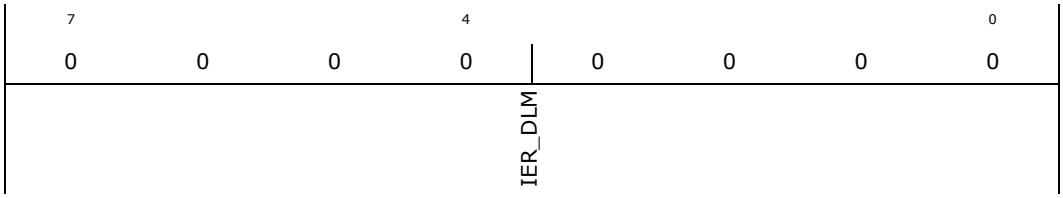
This register is a combination of two registers: the interrupt enable register (IER) when DLAB=0 and the divisor latch MSB (DLM) register when DLAB=1.

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 3F9h

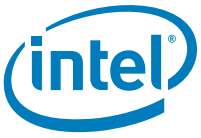
Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**Interrupt Enable (IER_DLM): If DLAB=1'b0**, This field is used as interrupt enable register. The smartest way to perform serial communications on a PC is using interrupt driven routines. In that configuration, it is not necessary to poll the registers of the UART periodically for state changes. The UART will signal each change by generating a processor interrupt. A software routine must be present to handle the interrupt and to check what state change was responsible for it. Interrupts are not generated, unless the UART is told to do so. This is done by setting bits in the IER, interrupt enable register. A bit value 1 indicates, that an interrupt may take place. Bit Description 0 ERBFI - Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 1 ETBEI - Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 2 ELSI - Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 3 EDSSI - Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 4 Reserved and read as zero 5 Reserved and read as zero 6 Reserved and read as zero 7 PTIME - Programmable THRE Interrupt Mode Enable that can be written to only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt. **If DLAB=1'b1**, this register is used as DLM (Divisor Latch MSB). Refer DLL field description in the Rx_Tx_Buffer register.

10.11.3 Interrupt Identification / FIFO Control Register (COM1_IIR)—Offset 3FAh

This register is a combination of two registers: the interrupt identification register (IIR) that is a read-only register and the FIFO control register (FCR) that is a write-only register. If FIFOs are not implemented, the FIFO control register does not exist and writing to this register address has no effect.



Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 3FAh

Default: 01h

7			4				0
0	0	0	0	0	0	0	1
FERT			TET	IIR			

Bit Range	Default & Access	Field Name (ID): Description
7:6	0x0 RO	**FIFOs Enabled / RCVR Trigger (FERT): Read** from this field is used to indicate whether the FIFOs are enabled or disabled. '00' - disabled '11' - enabled **Write** to this field is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. The following trigger levels are supported: '00' - 1 character in the FIFO '01' - FIFO 1/4 full '10' - FIFO 1/2 full '11' - FIFO 2 less than full
5:4	0x0 RO	**TX Empty Trigger (TET): Read** from this field is reserved and should return zero **Write** to this field is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: '00' - FIFO empty '01' - 2 characters in the FIFO '10' - FIFO 1/4 full '11' - FIFO 1/2 full
3:0	0x1 RO	**Interrupt ID (IIR): Read** from this field indicates the highest priority pending interrupt which can be one of the following types: '0000' - modem status '0001' - no interrupt pending '0010' - THR empty '0100' - received data available '0110' - receiver line status '0111' - busy detect '1100' - character timeout **Write** to this field is split to four bits: Bit Description 3 DMA Mode, determines the DMA signalling mode used: '0'- mode 0, '1' - mode 1 2 XMIT FIFO Reset, resets the control portion of the transmit FIFO and treats the FIFO as empty. 1 RCVR FIFO Reset, resets the control portion of the receive FIFO and treats the FIFO as empty. 0 FIFO Enable. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

10.11.4 Line Control Register (COM1_LCR)—Offset 3FBh

The LCR, line control register is used at initialization to set the communication parameters. Parity and number of data bits can be changed for example. The register also controls the accessibility of the DLL and DLM registers. These registers are mapped to the same I/O port as the RBR, THR and IER registers. Because they are only accessed at initialization when no communication occurs this register swapping has no influence on performance.

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 3FBh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
DLAB	BC	SP	EPS	PEN	STOP	DLS	

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW	**Divisor Latch Access Bit (DLAB):** This field is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. '0' - RBR, THR and IER accessible '1' - DLL and DLM accessible Refer Rx_Tx_Buffer and IER registers description for more details.
6	0x0 RW	**Break Control (BC):** This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	0x0 RO	**Stick Parity (SP):** Reserved and read as zero
4	0x0 RW	**Even Parity Select (EPS):** This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked.
3	0x0 RW	**Parity Enable (PEN):** This is used to enable and disable parity generation and detection in transmitted and received serial character respectively. '0' - parity disabled '1' - parity enabled

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**Number ofStop bits (STOP):** This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. '0' - 1 stop bit '1' - 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	0x0 RW	**Data Length Select (DLS):** This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: '00' - 5 bits '01' - 6 bits '10' - 7 bits '11' - 8 bits

10.11.5 Modem Control Register (COM1_MCR)—Offset 3FCh

The MCR, modem control register is used to perform handshaking actions with the attached device. In the original UART series including the 16550, setting and resetting of the control signals must be done by software. The new 16750 is capable of handling flow control automatically, thereby reducing the load on the processor.

Access Method

Type: I/O Register
(Size: 8 bits)

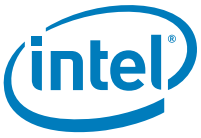
Offset: 3FCh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSVD0	SIRE	AFCE	LB	OUT2	OUT1	RTS	DTR

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**RSVD0:** Reserved
6	0x0 RW	**SIR Mode Enable (SIRE):** Writeable only when SIR_MODE == Enabled, always readable. This is used to enable/disable the IrDA SIR Mode features as described in 'IrDA 1.0 SIR Protocol' on Synopsys UART specification. '0' - IrDA SIR Mode disabled '1' - IrDA SIR Mode enabled
5	0x0 RW	**Auto Flow Control Enable (AFCE):** Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled as described in 'Auto Flow Control' on Synopsys UART specification. '0' - Auto Flow Control Mode disabled '1' - Auto Flow Control Mode enabled

Bit Range	Default & Access	Field Name (ID): Description
4	0x0 RW	**LoopBack (LB):** This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	0x0 RW	**Auxiliary output 2 (OUT2):** This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: '0' - out2_n de-asserted (logic 1) '1' - out2_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.
2	0x0 RW	**Auxiliary output 1 (OUT1):** This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n, that is: '0' - out1_n de-asserted (logic 1) '1' - out1_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input.
1	0x0 RW	**Request to Send (RTS):** This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input. Note that PCU-UART does not implement the Request to Send (rts_n) output.
0	0x0 RW	**Data Terminal Ready (DTR):** This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is: '0' - dtr_n de-asserted (logic 1) '1' - dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input. Note that PCU-UART does not implement the Data Terminal Ready (dtr_n) output.



10.11.6 Line Status Register (COM1_LSR)—Offset 3FDh

The LSR, line status register shows the current state of communication. Errors are reflected in this register. The state of the receive and transmit buffers is also available.

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 3FDh

Default: 60h

7			4				0
0	1	1	0	0	0	0	0
RFE	TEMT	THRE	BI	FE	PE	OE	DR

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**Receiver FIFO Error (RFE):** This bit is only relevant when FIFO_MODE != NONE AND FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. '0' - no error in RX FIFO '1' - error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.
6	0x1 RO	**Transmitter Empty (TEMT):** If in FIFO mode (FIFO_MODE != NONE) and FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	0x1 RO	**Transmit Holding Register Empty (THRE):** If THRE_MODE_USER == Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.
4	0x0 RO	**Break Interrupt (BI):** This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RO	**Framing Error (FE):** This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). '0' - no framing error '1' - framing error Reading the LSR clears the FE bit.
2	0x0 RO	**Parity Error (PE):** This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). '0' - no parity error '1' - parity error Reading the LSR clears the PE bit.
1	0x0 RO	**Overrun Error (OE):** This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. '0' - no overrun error '1' - overrun error Reading the LSR clears the OE bit.
0	0x0 RO	**Data Ready (DR):** This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. '0' - no data ready '1' - data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

10.11.7 Modem Status Register (COM1_MSR)—Offset 3FEh

The MSR, modem status register contains information about the four incoming modem control lines on the device. The information is split in two nibbles. The four most significant bits contain information about the current state of the inputs where the least significant bits are used to indicate state changes. The four LSB's are reset, each time the register is read. Whenever bits 0, 1, 2 or 3 are set to logic one, to indicate a change on the modem control inputs, a modem status interrupt is generated if enabled through the IER, regardless of when the change occurred. Since the delta bits (bits 0, 1, 3) can

get set after a reset if their respective modem signals are active (see individual bits for details), a read of the MSR after reset can be performed to prevent unwanted interrupts.

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 3FEh

Default: 00h

7				4			0
0	0	0	0	0	0	0	0
DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**Data Carrier Detect (DCD):** This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. '0' - dcd_n input is de-asserted (logic 1) '1' - dcd_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2). Note that PCU-UART does not implement the Data Carrier Detect (dcd_n) input.
6	0x0 RO	**Ring Indicator (RI):** This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. '0' - ri_n input is de-asserted (logic 1) '1' - ri_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1). Note that PCU-UART does not implement the Ring Indicator (ri_n) input.
5	0x0 RO	**Data Set Ready (DSR):** This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. '0' - dsr_n input is de-asserted (logic 1) '1' - dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR). Note that PCU-UART does not implement the Data Set Ready (dsr_n) input.
4	0x0 RO	**Clear to Send (CTS):** This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. '0' - cts_n input is de-asserted (logic 1) '1' - cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS). Note that PCU-UART does not implement the Clear to Send (cts_n) input.

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RO	**Delta Data Carrier Detect (DDCD):** This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. '0' - no change on dcd_n since last read of MSR '1' - change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] = 1), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted. Note that PCU-UART does not implement the Data Carrier Detect (dcd_n) input.
2	0x0 RO	**Trailing Edge of Ring Indicator (TERI):** This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. '0' - no change on ri_n since last read of MSR '1' - change on ri_n since last read of MSR Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] = 1), TERI reflects when MCR[2] (Out1) has changed state from a high to a low. Note that PCU-UART does not implement the Ring Indicator (ri_n) input.
1	0x0 RO	**Delta Data Set Ready (DDSR):** This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. '0' - no change on dsr_n since last read of MSR '1' - change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted. Note that PCU-UART does not implement the Data Set Ready (dsr_n) input.
0	0x0 RO	**Delta Clear to Send (DCTS):** This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. '0' - no change on cts_n since last read of MSR '1' - change on cts_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted. Note that PCU-UART does not implement the Clear to Send (cts_n) input.

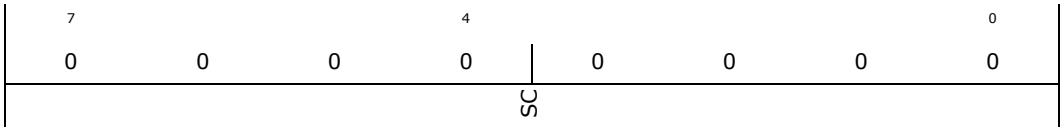
10.11.8 Scratchpad Register (COM1_SCR)—Offset 3FFh

Access Method

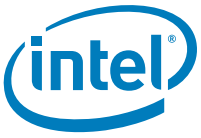
Type: I/O Register
(Size: 8 bits)

Offset: 3FFh

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**Scratchpad (SC):** This register is for programmers to use as a temporary storage space.



10.12 PCU—iLB LPC BIOS Control Memory Mapped I/O Registers

Table 107. Summary of PCU—iLB LPC BIOS Control Memory Mapped I/O Registers—RCRB_BASE_ADDRESS

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	GCS (RCRB_GENERAL_CONTROL)—Offset 0h	00000000h

10.12.1 GCS (RCRB_GENERAL_CONTROL)—Offset 0h

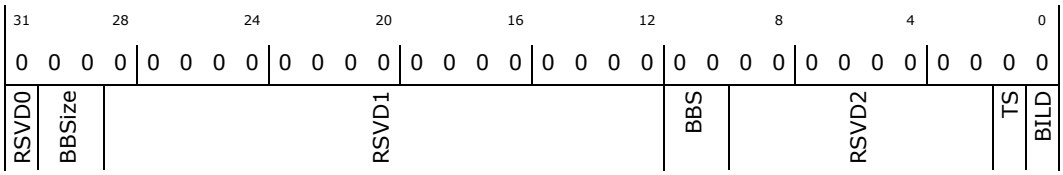
General Control and Status - contains BIOS configuration and status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [RCRB_BASE_ADDRESS] + 0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**RSVD0:** Reserved
30:29	X RO	**Boot Block Size (BBSize):** This field determines the size of the BIOS boot block. Default is controlled by 'Boot Block Size' soft strap. 00 : 64KB (Default) : Invert A16 if Top Swap is enabled 01 : 128KB : Invert A17 if Top Swap is enabled 10 : 256KB : Invert A18 if Top Swap is enabled 11 : Reserved This soft strap only applies when booting from SPI. Boot from LPC (FWH) only supports a 64KB boot block size (Invert A16) and this soft strap value is a don't care.
28:12	0x0 RO	**RSVD1:** Reserved
11:10	X RW	**Boot BIOS Straps (BBS):** This field determines the destination of accesses to the BIOS memory range. Default is controlled by 'Boot BIOS Straps' pin strap. 00 LPC 01 Reserved 10 Reserved 11 SPI The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down (bit 0) is not set.
9:2	0x0 RO	**RSVD2:** Reserved
1	X RW	**Top Swap (TS):** When set, PCU EP will invert either A16, A17, or A18 for cycles going to the BIOS space (but not the feature space) in the FWH. When cleared, PCU EP will not invert A16. If booting from LPC (FWH), then the Boot Blook size is 64KB and A16 is inverted if Top Swap is enabled. If booting from SPI, then the BOOT_BLOCK_SIZE soft strap determines if A16, A17, or A18 should be inverted if Top Swap is enabled. If Top-Swap pin-strap is active, then this bit cannot be cleared by software. This bit should be kept in RTC well and should be reset only by SRTCRST_b
0	0x0 RW	**BIOS Interface Lock-Down (BILD):** When set, prevents GCS.TS and GCS.BBS from being changed. This bit can only be written from 0 to 1 once.

10.13 PCU—iLB Real Time Clock (RTC) Memory Mapped I/O Registers

Table 108. Summary of PCU—iLB RTC I/O Registers—

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
70–70h	1	"IR (reg_RTC_IR_type)—Offset 70h" on page 5765	00h
71–71h	1	"TR (reg_RTC_TR_type)—Offset 71h" on page 5765	00h
72–72h	1	"RIR (reg_RTC_RIR_type)—Offset 72h" on page 5765	00h
73–73h	1	"RTR (reg_RTC_RTR_type)—Offset 73h" on page 5766	00h

10.13.1 IR (reg_RTC_IR_type)—Offset 70h

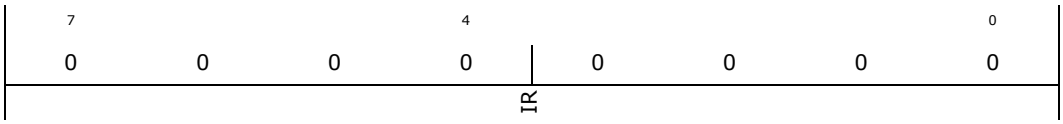
Indexed Registers

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 70h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	X RW	**IR:** Real-Time Clock (Standard RAM) Index Register Note: Writes to 72h, 74h, and 76h do not affect the NMI enable (bit 7 of 70h)

10.13.2 TR (reg_RTC_TR_type)—Offset 71h

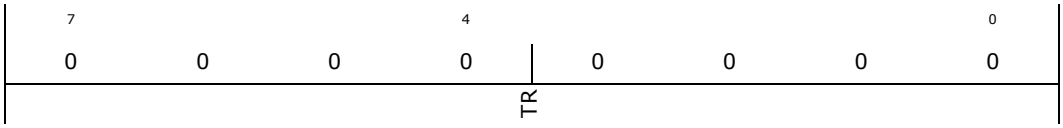
Target Registers

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 71h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	X RW	**TR:** Real-Time Clock (Standard RAM) Target Register

10.13.3 RIR (reg_RTC_RIR_type)—Offset 72h

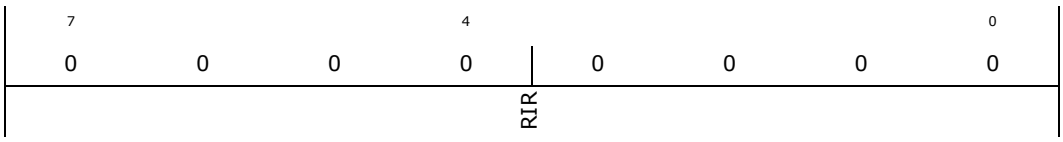
Extended RAM Index Register

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 72h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	X RW	**RIR:** Extended RAM Index Register

10.13.4 RTR (reg_RTC_RTR_type)—Offset 73h

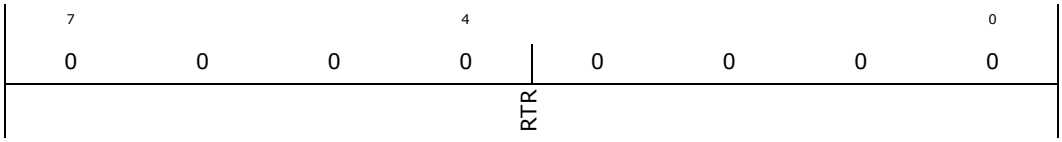
Extended RAM Target Register

Access Method

Type: I/O Register (Size: 8 bits)

Offset: 73h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	X RW	**RTR:** Extended RAM Target Register

10.14 PCU—iLB 8254 Timers Memory Mapped I/O Registers

Table 109. Summary of PCU-iLB 8254 Timers Memory Mapped I/O Registers—

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40–40h	1	"C0TS—Offset 40h" on page 5769	00h
41–41h	1	"C1TS—Offset 41h" on page 5769	00h
42–42h	1	"C2TS—Offset 42h" on page 5770	00h
43–43h	1	"TCW—Offset 43h" on page 5771	00h
50–50h	1	"C0AP—Offset 50h" on page 5772	00h
51–51h	1	"C1AP—Offset 51h" on page 5772	00h
52–52h	1	"C2AP—Offset 52h" on page 5773	00h
61–61h	1	"NSC—Offset 61h" on page 5773	20h

10.14.1 C0TS—Offset 40h

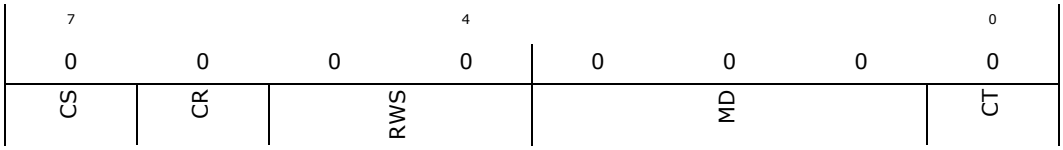
Counter 0 Interval Time Status Byte Format.Status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for counter 0, the next read from this register returns the status byte.

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 40h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**CS:** Counter State (CS): When set, OUT of the counter is set. When cleared, OUT of the counter is 0.
6	X RO	**CR:** Count Register: When cleared, indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE) and is available for reading. The time this happens depends on the counter mode.
5:4	X RO	**RWS:** Read/Write Selection: These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	X RO	**MD:** Mode: Returns the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. Bits Mode Description 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	X RO	**CT:** Countdown Type: 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

10.14.2 C1TS—Offset 41h

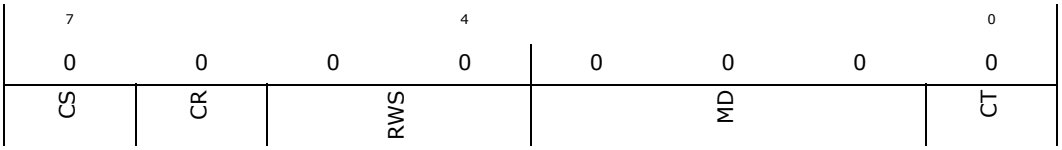
Counter 1 Interval Time Status Byte Format. Counter 1 Interval Time Status Byte Format. Status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for counter 1, the next read from this register returns the status byte.

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 41h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**CS:** Counter State (CS): When set, OUT of the counter is set. When cleared, OUT of the counter is 0.
6	X RO	**CR:** Count Register: When cleared, indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE) and is available for reading. The time this happens depends on the counter mode.
5:4	X RO	**RWS:** Read/Write Selection: These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	X RO	**MD:** Mode: Returns the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. Bits Mode Description 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	X RO	**CT:** Countdown Type: 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

10.14.3 C2TS—Offset 42h

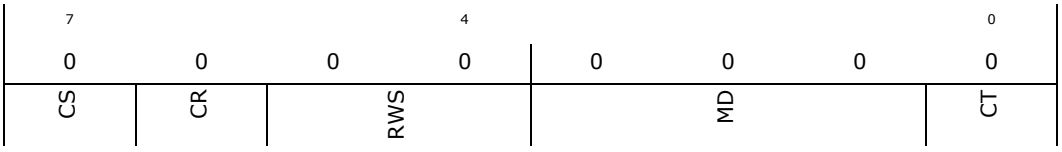
Counter 2 Interval Time Status Byte Format. Counter 2 Interval Time Status Byte Format. Status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for counter 2, the next read from this register returns the status byte.

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 42h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**CS:** Counter State (CS): When set, OUT of the counter is set. When cleared, OUT of the counter is 0.

Bit Range	Default & Access	Field Name (ID): Description
6	X RO	**CR:** Count Register: When cleared, indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE) and is available for reading. The time this happens depends on the counter mode.
5:4	X RO	**RWS:** Read/Write Selection: These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	X RO	**MD:** Mode: Returns the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. Bits Mode Description 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	X RO	**CT:** Countdown Type: 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

10.14.4 TCW—Offset 43h

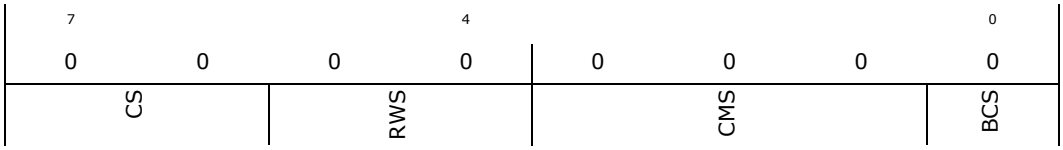
Timer Control Word Register. This register is programmed prior to any counter being accessed to specify counter modes. Following reset, the control words for each register are undefined and each counter output is 0. Each timer must be programmed to bring it into a known state.

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 43h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:6	X WO	**CS:** Counter Select (CS): The Counter Selection bits select the counter the control word acts upon as shown below. The Read Back Command is selected when bits[7:6] are both 1 00 Counter 0 select 01 Counter 1 select 10 Counter 2 select 11 Read Back Command
5:4	X WO	**RWS:** Read/Write Select RWS): The counter programming is done through the counter port (40h for counter 0, 41h for counter 1, and 42h for counter 2) 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB

Bit Range	Default & Access	Field Name (ID): Description
3:1	X WO	**CMS:** Counter Mode Selection (CMS): Selects one of six modes of operation for the selected counter. 000 = Out signal on end of count (=0) 001 = Hardware retriggerable one-shot x10 = Rate generator (divide by n counter) x11 = Square wave output 100 = Software triggered strobe 101 = Hardware triggered strobe
0	X WO	**BCS:** Binary/BCD Countdown Select (BCS): 0 Binary countdown is used. The largest possible binary count is 216 1 Binary coded decimal (BCD) count is used. The largest possible BCD count is 104

10.14.5 C0AP—Offset 50h

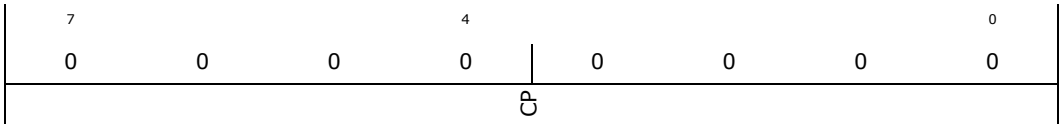
Counter 0 Counter Access Port Register

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 50h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	X RW	**CP:** Counter Port: Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

10.14.6 C1AP—Offset 51h

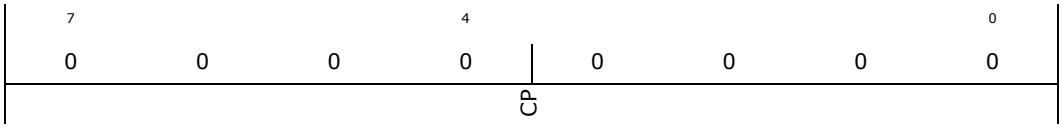
Counter 1 Counter Access Port Register

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 51h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	X RW	**CP:** Counter Port: Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

10.14.7 C2AP—Offset 52h

Counter 2 Counter Access Port Register

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 52h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CP							

Bit Range	Default & Access	Field Name (ID): Description
7:0	X RW	**CP:** Counter Port: Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

10.14.8 NSC—Offset 61h

NMI Status and Control

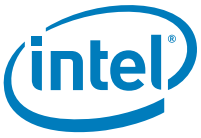
Access Method

Type: I/O Register
(Size: 8 bits)

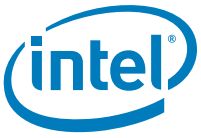
Offset: 61h

Default: 20h

7			4				0
0	0	1	0	0	0	0	0
SNS	INS	T2S	RTS	INE	SNE	SDE	TC2E



Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**SNS:** SERR# NMI Status (SNS): Set on errors from a PCIe port or internal functions that generate SERR#. SNE in this register must be cleared in order for this bit to be set. To reset the interrupt, set bit 2 to 1 and then set it to 0.
6	0x0 RO	**INS:** IOCHK NMI Status (INS): Set when SERIRQ asserts IOCHK# and INE in this register is cleared. To reset the interrupt, set bit 3 to 1 and then set it to 0.
5	0x1 RO	**RTS (T2S):** Timer Counter 2 Status (T2S): Reflects the current state of the 8254 counter 2 outputs. Counter 2 must be programmed for this bit to have a determinate value.
4	0x0 RO	**RTS:** Refresh Cycle Toggle Status (RTS): Reflects the current state of 8254 counter 1
3	X RW	**INE:** IOCHK NMI Enable (INE): When set, IOCHK# NMIs are disabled. When cleared, IOCHK# NMIs are enabled.
2	0x0 RW	**SNE:** SERR# NMI Enable (SNE): When set, SERR# NMIs are disabled. When cleared, SERR# NMIs are enabled.
1	0x0 RW	**SDE:** Speaker Data Enable (SDE): When this bit is a 0, the SPKR output is a 0. When this bit is a 1, the SPKR output is equivalent to the Counter 2 OUT signal value.
0	0x0 RW	**TC2E:** Timer Counter 2 Enable (TC2E): When cleared, counter 2 counting is disabled. When set, counting is enabled.



10.15 PCU—iLB High Performance Event Timer (HPET) Memory Mapped I/O Registers

Table 110. Summary of PCU—iLB HPET Memory Mapped I/O Registers—

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
FED00000–FED00007h	8	"GCID (HPET_GCID)—Offset FED00000h" on page 5777	0429B17F8086A201h
FED00010–FED00017h	8	"GCFG (HPET_GCFG)—Offset FED00010h" on page 5777	0000000000000000h
FED00020–FED00027h	8	"GIS (HPET_GIS)—Offset FED00020h" on page 5778	0000000000000000h
FED000F0–FED000F7h	8	"MCV (HPET_MCV)—Offset FED000F0h" on page 5778	0000000000000000h
FED00100–FED00107h	8	"T0C (HPET_T0C)—Offset FED00100h" on page 5779	00F0000000000030h
FED00108–FED0010Bh	4	"T0CV_L (HPET_T0CV_L)—Offset FED00108h" on page 5780	FFFFFFFFh
FED0010C–FED0010Fh	4	"T0CV_U (HPET_T0CV_U)—Offset FED0010Ch" on page 5780	FFFFFFFFh
FED00120–FED00127h	8	"T1C (HPET_T1C)—Offset FED00120h" on page 5781	00F0000000000000h
FED00128–FED0012Fh	8	"T1CV (HPET_T1CV)—Offset FED00128h" on page 5782	00000000FFFFFFFFh
FED00140–FED00147h	8	"T2C (HPET_T2C)—Offset FED00140h" on page 5783	00F0080000000000h
FED00148–FED0014Fh	8	"T2CV (HPET_T2CV)—Offset FED00148h" on page 5784	00000000FFFFFFFFh

10.15.1 GCID (HPET_GCID)—Offset FED00000h

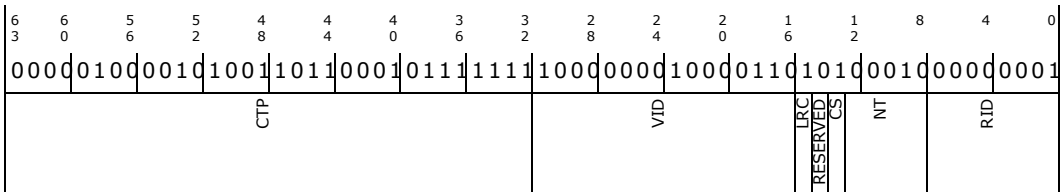
General Capabilities and ID

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: FED00000h

Default: 0429B17F8086A201h



Bit Range	Default & Access	Field Name (ID): Description
63:32	0x429b17f RO	**CTP:** Counter Tick Period (CTP): Indicates a period of 69.841279ns, (14.1318 MHz clock period)
31:16	0x8086 RO	**VID:** Vendor ID (VID): Value of 8086h indicates Intel.
15	0x1 RO	**LRC:** Legacy Rout Capable (LRC): Indicates support for Legacy Interrupt Rout.
14	0x0 RO	**RESERVED:** Reserved.
13	0x1 RO	**CS:** Counter Size (CS): This bit is set to indicate that the main counter is 64 bits wide.
12:8	0x2 RO	**NT:** Number of Timers (NT): Indicates that 3 timers are supported.
7:0	0x1 RO	**RID:** Revision ID (RID): Indicates that revision 1.0 of the specification is implemented.

10.15.2 GCFG (HPET_GCFG)—Offset FED00010h

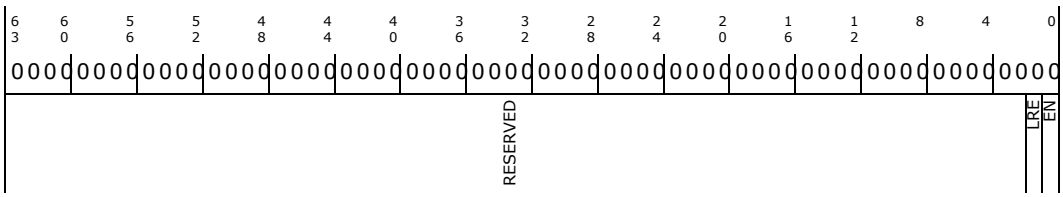
General Configuration

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: FED00010h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:2	0x0 RO	**RESERVED:** Reserved.
1	0x0 RW	**LRE:** Legacy Rout Enable (LRE): When set, interrupts will be routed as follows: Timer 0 will be routed to IRQ0 in 8259 or IRQ2 in the I/O APIC Timer 1 will be routed to IRQ8 in 8259 and I/O APIC Timer 2 will be routed as per the routing in T2C When set, the T[1:0]C.IR will have no impact for timers 0 and 1.
0	0x0 RW	**EN:** Overall Enable (EN): When set, the timers can generate interrupts. When cleared, the main counter will halt and no interrupts will be caused by any timer. For level-triggered interrupts, if an interrupt is pending when this bit is cleared, the GIS.Tx will not be cleared.

10.15.3 GIS (HPET_GIS)—Offset FED00020h

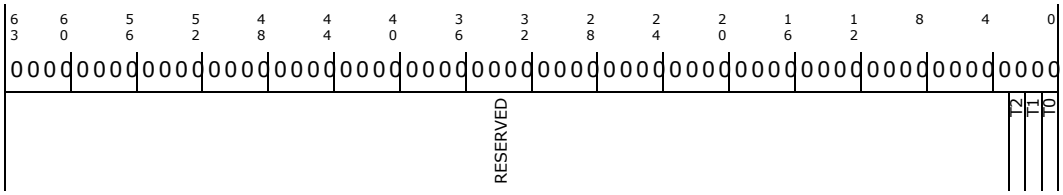
General Interrupt Status

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: FED00020h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:3	0x0 RO	**RESERVED:** Reserved.
2	0x0 RW	**T2:** Timer 2 Status (T2): Same functionality as T0, for timer 2.
1	0x0 RW	**T1:** Timer 1 Status (T1): Same functionality as T0, for timer 1.
0	0x0 RW	**T0:** Timer 0 Status (T0): In edge triggered mode, this bit always reads as 0. In level triggered mode, this bit is set when an interrupt is active.

10.15.4 MCV (HPET_MCV)—Offset FED000F0h

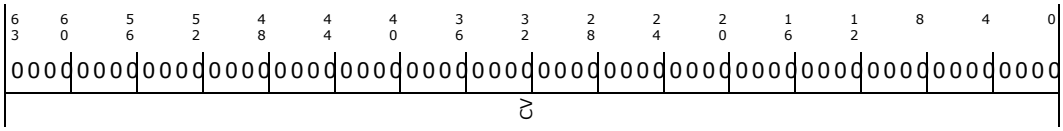
Main Counter Value

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: FED000F0h

Default: 0000000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:0	0x0 RW	**CV:** Counter Value (CV): Reads return the current value of the counter. Writes load the new value to the counter. Timers 1 and 2 return 0 for the upper 32-bits of this register.

10.15.5 T0C (HPET_T0C)—Offset FED00100h

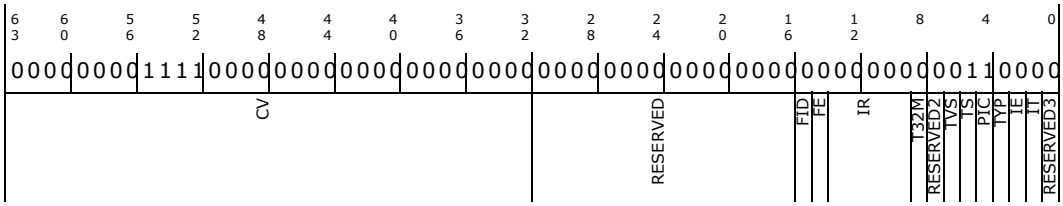
Timer 0 Config and Capabilities

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: FED00100h

Default: 00F0000000000030h



Bit Range	Default & Access	Field Name (ID): Description
63:32	0xf00000 RO	**IRC (CV):** Interrupt Rout Capability (IRC): Indicates I/OxAPIC interrupts the timer can use: Timer 0,1: 00f00000h. Indicates support for IRQ20, 21, 22, 23 Timer 2: 00f00800h. Indicates support for IRQ11, 20, 21, 22, and 23
31:16	0x0 RO	**RESERVED:** Reserved.
15	0x0 RO	**FID:** FSB Interrupt Delivery (FID): Not supported
14	0x0 RO	**FE:** FSB Enable (FE): Not supported, since FID is not supported.
13:9	0x0 RW	**IR:** Interrupt Rout (IR): Indicates the routing for the interrupt to the IOxAPIC. If the value is not supported by this prarticular timer, the value read back will not match what is written. If GCFG.LRE is set, then Timers 0 and 1 have a fixed routing, and this field has no effect.
8	0x0 RW	**T32M:** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
7	0x0 RO	**RESERVED (RESERVED2):** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.

Bit Range	Default & Access	Field Name (ID): Description
6	0x0 RW	**TVS:** Timer Value Set (TVS): This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1 and 2.
5	0x1 RO	**TS:** Timer Size (TS): 1 = 64-bits, 0 = 32-bits. Set for timer 0. Cleared for timers 1 and 2.
4	0x1 RO	**PIC:** Periodic Interrupt Capable (PIC): When set, hardware supports a periodic mode for this timer's interrupt. This bit is set for timer 0, and cleared for timers 1 and 2.
3	0x0 RW	**TYP:** Timer Type (TYP): If PIC is set, this bit is read/write, and can be used to enable the timer to generate a periodic interrupt. This bit is RW for timer 0, and RO for timers 1 and 2.
2	0x0 RW	**IE:** Interrupt Enable (IE): When set, enables the timer to cause an interrupt when it times out. When cleared, the timer count and generates status bits, but will not cause an interrupt.
1	0x0 RW	**IT:** Timer Interrupt Type (IT): When cleared, interrupt is edge triggered. When set, interrupt is level triggered and will be held active until it is cleared by writing 1 to GIS.Tn. If another interrupt occurs before the interrupt is cleared, the interrupt remains active.
0	0x0 RO	**RESERVED (RESERVED3):** Reserved.

10.15.6 T0CV_L (HPET_T0CV_L)—Offset FED00108h

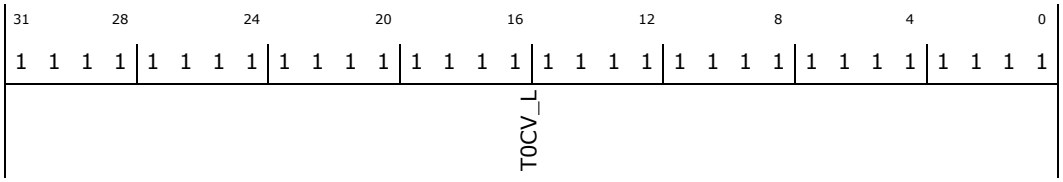
Lower Timer 0 Comperator Value

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: FED00108h

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**T0CV_L:** Lower Timer 0 Comperator Value

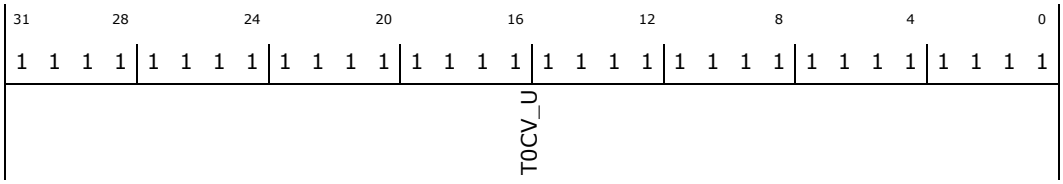
10.15.7 T0CV_U (HPET_T0CV_U)—Offset FED0010Ch

Upper Timer 0 Comperator Value

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits) **Offset:** FED0010Ch

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	0xffffffff RW	**T0CV_U:** Upper Timer 0 Comperator Value

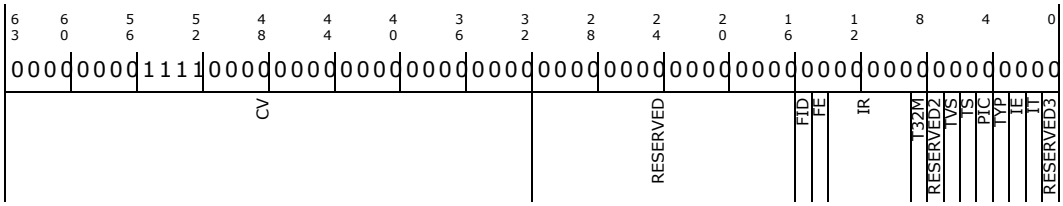
10.15.8 T1C (HPET_T1C)—Offset FED00120h

Timer 1 Config and Capabilities

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits) **Offset:** FED00120h

Default: 00F0000000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:32	0xf00000 RO	**IRC (CV):** Interrupt Rout Capability (IRC): Indicates I/OxAPIC interrupts the timer can use: Timer 0,1: 00f00000h. Indicates support for IRQ20, 21, 22, 23 Timer 2: 00f00800h. Indicates support for IRQ11, 20, 21, 22, and 23
31:16	0x0 RO	**RESERVED:** Reserved.
15	0x0 RO	**FID:** FSB Interrupt Delivery (FID): Not supported
14	0x0 RO	**FE:** FSB Enable (FE): Not supported, since FID is not supported.
13:9	0x0 RW	**IR:** Interrupt Rout (IR): Indicates the routing for the interrupt to the IOxAPIC. If the value is not supported by this prarticular timer, the value read back will not match what is written. If GCFG.LRE is set, then Timers 0 and 1 have a fixed routing, and this field has no effect.
8	0x0 RO	**T32M:** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**RESERVED (RESERVED2):** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
6	0x0 RO	**TVS:** Timer Value Set (TVS): This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1 and 2.
5	0x0 RO	**TS:** Timer Size (TS): 1 = 64-bits, 0 = 32-bits. Set for timer 0. Cleared for timers 1 and 2.
4	0x0 RO	**PIC:** Periodic Interrupt Capable (PIC): When set, hardware supports a periodic mode for this timer's interrupt. This bit is set for timer 0, and cleared for timers 1 and 2.
3	0x0 RO	**TYP:** Timer Type (TYP): If PIC is set, this bit is read/write, and can be used to enable the timer to generate a periodic interrupt. This bit is RW for timer 0, and RO for timers 1 and 2.
2	0x0 RW	**IE:** Interrupt Enable (IE): When set, enables the timer to cause an interrupt when it times out. When cleared, the timer count and generates status bits, but will not cause an interrupt.
1	0x0 RW	**IT:** Timer Interrupt Type (IT): When cleared, interrupt is edge triggered. When set, interrupt is level triggered and will be held active until it is cleared by writing 1 to GIS.Tn. If another interrupt occurs before the interrupt is cleared, the interrupt remains active.
0	0x0 RO	**RESERVED (RESERVED3):** Reserved.

10.15.9 T1CV (HPET_T1CV)—Offset FED00128h

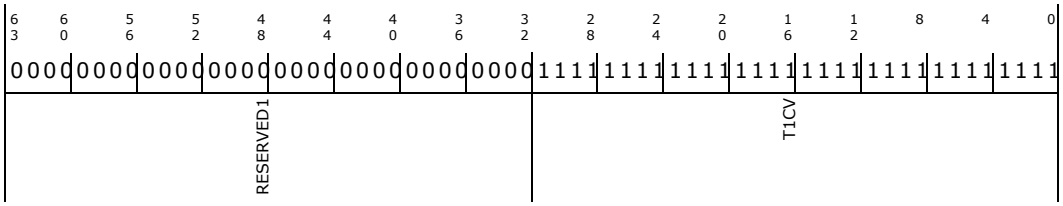
Timer 1 Comperator Value

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: FED00128h

Default: 00000000FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
63:32	0x0 RO	**RESERVED (RESERVED1):** Reserved.
31:0	0xffffffff RO	**T1CV:** Timer 1 Comperator Value

10.15.10 T2C (HPET_T2C)—Offset FED00140h

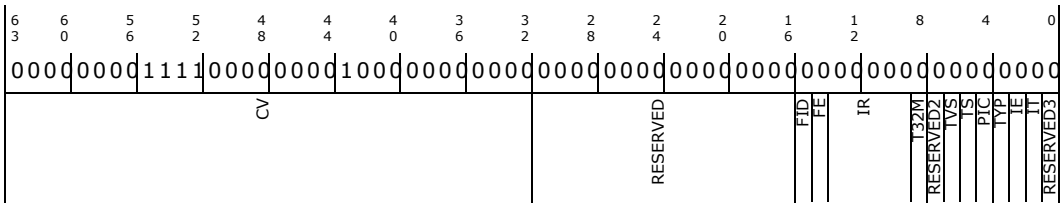
Timer 2 Config and Capabilities

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: FED00140h

Default: 00F0080000000000h



Bit Range	Default & Access	Field Name (ID): Description
63:32	0xf00800 RO	**IRC (CV):** Interrupt Rout Capability (IRC): Indicates I/OxAPIC interrupts the timer can use: Timer 0,1: 00f00000h. Indicates support for IRQ20, 21, 22, 23 Timer 2: 00f00800h. Indicates support for IRQ11, 20, 21, 22, and 23
31:16	0x0 RO	**RESERVED:** Reserved.
15	0x0 RO	**FID:** FSB Interrupt Delivery (FID): Not supported
14	0x0 RO	**FE:** FSB Enable (FE): Not supported, since FID is not supported.
13:9	0x0 RW	**IR:** Interrupt Rout (IR): Indicates the routing for the interrupt to the IOxAPIC. If the value is not supported by this prarticular timer, the value read back will not match what is written. If GCFG.LRE is set, then Timers 0 and 1 have a fixed routing, and this field has no effect.
8	0x0 RO	**T32M:** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
7	0x0 RO	**RESERVED (RESERVED2):** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
6	0x0 RO	**TVS:** Timer Value Set (TVS): This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1 and 2.
5	0x0 RO	**TS:** Timer Size (TS): 1 = 64-bits, 0 = 32-bits. Set for timer 0. Cleared for timers 1 and 2.
4	0x0 RO	**PIC:** Periodic Interrupt Capable (PIC): When set, hardware supports a periodic mode for this timer's interrupt. This bit is set for timer 0, and cleared for timers 1 and 2.
3	0x0 RO	**TYP:** Timer Type (TYP): If PIC is set, this bit is read/write, and can be used to enable the timer to generate a periodic interrupt. This bit is RW for timer 0, and RO for timers 1 and 2.

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**IE:** Interrupt Enable (IE): When set, enables the timer to cause an interrupt when it times out. When cleared, the timer count and generates status bits, but will not cause an interrupt.
1	0x0 RW	**IT:** Timer Interrupt Type (IT): When cleared, interrupt is edge triggered. When set, interrupt is level triggered and will be held active until it is cleared by writing 1 to GIS.Tn. If another interrupt occurs before the interrupt is cleared, the interrupt remains active.
0	0x0 RO	**RESERVED (RESERVED3):** Reserved.

10.15.11 T2CV (HPET_T2CV)—Offset FED00148h

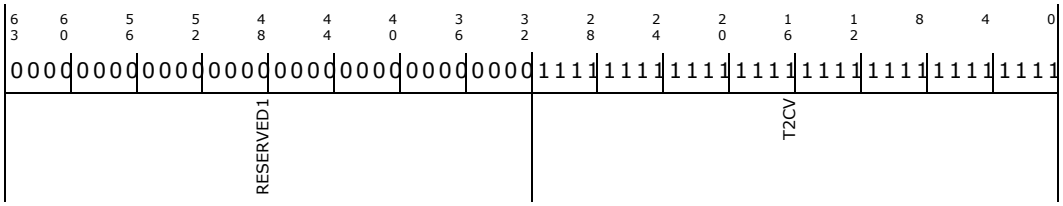
Timer 2 Comperator Value

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

Offset: FED00148h

Default: 00000000FFFFFFFFh

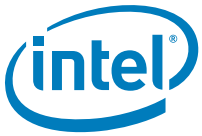


Bit Range	Default & Access	Field Name (ID): Description
63:32	0x0 RO	**RESERVED (RESERVED1):** Reserved.
31:0	0xffffffff RO	**T2CV:** Timer 2 Comperator Value

10.16 PCU-iLB Interrupt Decode and Route Memory Mapped I/O Registers

Table 111. Summary of PCU-iLB Interrupt Decode and Route Memory Mapped I/O Registers—ILB_BASE_ADDRESS

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"ACTL—Offset 0h" on page 5788	00000003h
4–7h	4	"MC—Offset 4h" on page 5788	00000000h
8–8h	1	"PIRQA—Offset 8h" on page 5789	80h
9–9h	1	"PIRQB—Offset 9h" on page 5789	80h
A–Ah	1	"PIRQC—Offset Ah" on page 5790	80h
B–Bh	1	"PIRQD—Offset Bh" on page 5790	80h
C–Ch	1	"PIRQE—Offset Ch" on page 5791	80h
D–Dh	1	"PIRQF—Offset Dh" on page 5791	80h
E–Eh	1	"PIRQG—Offset Eh" on page 5792	80h
F–Fh	1	"PIRQH—Offset Fh" on page 5793	80h
10–13h	4	"SCNT—Offset 10h" on page 5793	00000000h
14–17h	4	"KMC—Offset 14h" on page 5794	00000000h
18–1Bh	4	"FS—Offset 18h" on page 5795	00112233h
1C–1Fh	4	"BC—Offset 1Ch" on page 5796	00000100h
20–21h	2	"IR0—Offset 20h" on page 5796	3210h
22–23h	2	"IR1—Offset 22h" on page 5797	3210h
24–25h	2	"IR2—Offset 24h" on page 5797	3210h
26–27h	2	"IR3—Offset 26h" on page 5798	3210h
28–29h	2	"IR4—Offset 28h" on page 5798	3210h
2A–2Bh	2	"IR5—Offset 2Ah" on page 5799	3210h
2C–2Dh	2	"IR6—Offset 2Ch" on page 5799	3210h
2E–2Fh	2	"IR7—Offset 2Eh" on page 5800	3210h
30–31h	2	"IR8—Offset 30h" on page 5800	3210h
32–33h	2	"IR9—Offset 32h" on page 5801	3210h
34–35h	2	"IR10—Offset 34h" on page 5801	3210h
36–37h	2	"IR11—Offset 36h" on page 5802	3210h
38–39h	2	"IR12—Offset 38h" on page 5802	3210h
3A–3Bh	2	"IR13—Offset 3Ah" on page 5803	3210h
3C–3Dh	2	"IR14—Offset 3Ch" on page 5803	3210h
3E–3Fh	2	"IR15—Offset 3Eh" on page 5804	3210h
40–41h	2	"IR16—Offset 40h" on page 5804	3210h
42–43h	2	"IR17—Offset 42h" on page 5805	3210h
44–45h	2	"IR18—Offset 44h" on page 5805	3210h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
46–47h	2	"IR19—Offset 46h" on page 5806	3210h
48–49h	2	"IR20—Offset 48h" on page 5806	3210h
4A–4Bh	2	"IR21—Offset 4Ah" on page 5807	3210h
4C–4Dh	2	"IR22—Offset 4Ch" on page 5807	3210h
4E–4Fh	2	"IR23—Offset 4Eh" on page 5808	3210h
50–51h	2	"IR24—Offset 50h" on page 5808	3210h
52–53h	2	"IR25—Offset 52h" on page 5809	3210h
54–55h	2	"IR26—Offset 54h" on page 5809	3210h
56–57h	2	"IR27—Offset 56h" on page 5810	3210h
58–59h	2	"IR28—Offset 58h" on page 5810	3210h
5A–5Bh	2	"IR29—Offset 5Ah" on page 5811	3210h
5C–5Dh	2	"IR30—Offset 5Ch" on page 5811	3210h
5E–5Fh	2	"IR31—Offset 5Eh" on page 5812	3210h
60–63h	4	"OIC—Offset 60h" on page 5812	00001100h
64–67h	4	"RC—Offset 64h" on page 5813	00000000h
6C–6Fh	4	"BCS - BIOS Control Status (BCS)—Offset 6Ch" on page 5814	00000002h
70–73h	4	"LE—Offset 70h" on page 5814	00000003h
80–83h	4	"NMI (GNMI)—Offset 80h" on page 5815	00000004h
84–87h	4	"LPCC—Offset 84h" on page 5816	00000001h
88–8Bh	4	"IRQEN (IRQE)—Offset 88h" on page 5816	00000000h

10.16.1 ACTL—Offset 0h

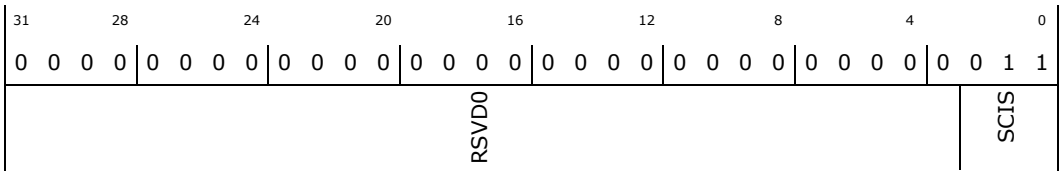
ACPI Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ILB_BASE_ADDRESS] + 0h

Default: 00000003h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**RSVD0:** Reserved
2:0	0x3 RW	**SCIS:** SCI IRQ Select (SCIS): Specifies on which IRQ the SCI will internally appear. If not using the APIC, the SCI must be routed to IRQ9-11 , and that interrupt is not sharable with the SERIRQ stream, but is shareable with other PCI interrupts. If using the APIC, the SCI can also be mapped to IRQ20-23, and can be shared with other interrupts. Bits SCI Map 000 IRQ9 001 IRQ10 010 IRQ11 011 Reserved 100 IRQ20 (only if APIC enabled) 101 IRQ21 (only if APIC enabled) 110 IRQ22 (only if APIC enabled) 111 IRQ23 (only if APIC enabled) When the interrupt is mapped to APIC interrupts 9, 10 or 11, the APIC should be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, the APIC should be programmed for active-low

10.16.2 MC—Offset 4h

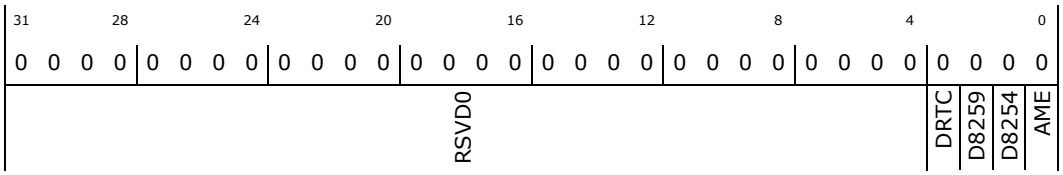
Miscellaneous Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ILB_BASE_ADDRESS] + 4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**AME:** Alt Access Mode is a mode that enables host reading some WO registers . 1. Read 8254 (legacy timers) indirect WO registers 2. Read 8259 (legacy interrupt controller) indirect WO registers 3. Read port 0x70 - port 0x70 includes the RTC memory address [6:0] and the NMI enable bit [7]

10.16.3 PIRQA—Offset 8h

PIRQA Routing Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [ILB_BASE_ADDRESS] + 8h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD0			IR			

Bit Range	Default & Access	Field Name (ID): Description
7	0x1 RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0x0 RO	**RSVD0:** Reserved
3:0	0x0 RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

10.16.4 PIRQB—Offset 9h

PIRQB Routing Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [ILB_BASE_ADDRESS] + 9h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD0			IR			

Bit Range	Default & Access	Field Name (ID): Description
7	0x1 RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0x0 RO	**RSVD0:** Reserved
3:0	0x0 RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

10.16.5 PIRQC—Offset Ah

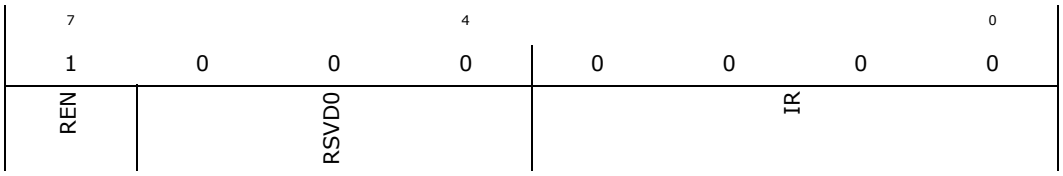
PIRQC Routing Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [ILB_BASE_ADDRESS] + Ah

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7	0x1 RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0x0 RO	**RSVD0:** Reserved
3:0	0x0 RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

10.16.6 PIRQD—Offset Bh

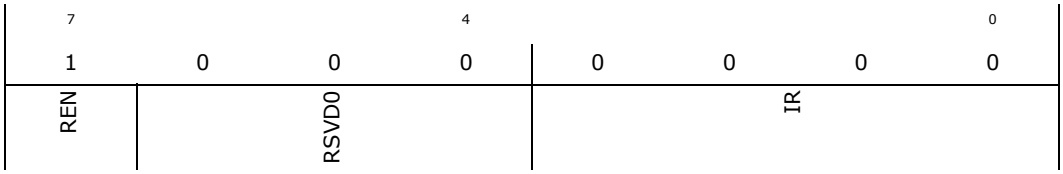
PIRQD Routing Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [ILB_BASE_ADDRESS] + Bh

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7	0x1 RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0x0 RO	**RSVD0:** Reserved
3:0	0x0 RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

10.16.7 PIRQE—Offset Ch

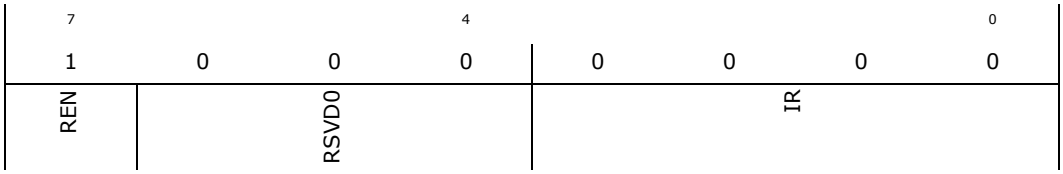
PIRQE Routing Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [ILB_BASE_ADDRESS] + Ch

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7	0x1 RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0x0 RO	**RSVD0:** Reserved
3:0	0x0 RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

10.16.8 PIRQF—Offset Dh

PIRQF Routing Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [ILB_BASE_ADDRESS] + Dh

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD0			IR			

Bit Range	Default & Access	Field Name (ID): Description
7	0x1 RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0x0 RO	**RSVD0:** Reserved
3:0	0x0 RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

10.16.9 PIRQG—Offset Eh

PIRQG Routing Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [ILB_BASE_ADDRESS] + Eh

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD0			IR			

Bit Range	Default & Access	Field Name (ID): Description
7	0x1 RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0x0 RO	**RSVD0:** Reserved
3:0	0x0 RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

10.16.10 PIRQH—Offset Fh

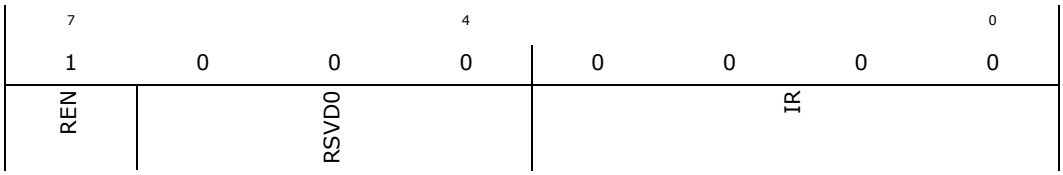
PIRQH Routing Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: [ILB_BASE_ADDRESS] + Fh

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7	0x1 RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0x0 RO	**RSVD0:** Reserved
3:0	0x0 RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

10.16.11 SCNT—Offset 10h

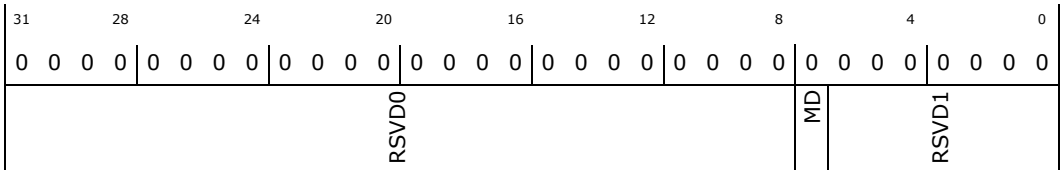
SCNT - Serial IRQ Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ILB_BASE_ADDRESS] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7	0x0 RW	**MD:** Mode (MD): When set, the SERIRQ is in continuous mode. When cleared, SERIRQ is in quiet mode. This bit must be set to guarantee that the first action of SERIRQ is a start frame.

Bit Range	Default & Access	Field Name (ID): Description
6:0	0x0 RO	**RSVD1:** Reserved

10.16.12 KMC—Offset 14h

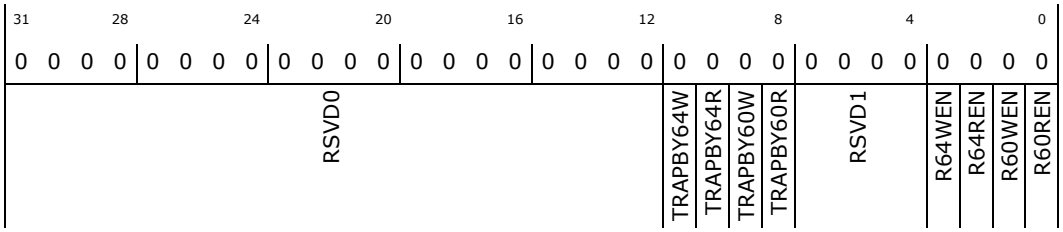
USB Legacy Keyboard/Mouse Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ILB_BASE_ADDRESS] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**RSVD0:** Reserved
11	0x0 RW/1C	**TRAPBY64W:** TRAPBY64W - SMI Caused by Port 64 Write: Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 3, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
10	0x0 RW/1C	**TRAPBY64R:** TRAPBY64R - SMI Caused by Port 64 Read: Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 2, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
9	0x0 RW/1C	**TRAPBY60W:** TRAPBY60W - SMI Caused by Port 60 Write: Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 1, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
8	0x0 RW/1C	**TRAPBY60R:** TRAPBY60R - SMI Caused by Port 60 Read: Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 0, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
7:4	0x0 RO	**RSVD1:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW	**R64WEN:** R64WEN - SMI on Port 64 Writes Enable: When set, a 1 in bit 11 will cause an SMI event.
2	0x0 RW	**R64REN:** R64REN - SMI on Port 64 Reads Enable: When set, a 1 in bit 10 will cause an SMI event.
1	0x0 RW	**R60WEN:** R60WEN - SMI on Port 60 Writes Enable: When set, a 1 in bit 9 will cause an SMI event.
0	0x0 RW	**R60REN:** R60REN - SMI on Port 60 Reads Enable: When set, a 1 in bit 8 will cause an SMI event.

10.16.13 FS—Offset 18h

FS - FWH ID Select

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ILB_BASE_ADDRESS] + 18h

Default: 00112233h

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 1	0 0 1 0	0 0 1 0	0 0 1 1	0 0 1 1
IF8	IF0	IE8	IE0	ID8	ID0	IC8	IC0

Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**IF8:** F8-FF IDSEL (IF8): IDSEL to use in FWH cycle for range enabled by BDE.EF8. The Address ranges are: FFF80000h - FFFFFFFFh, FFB80000h - FFBFFFFFh and 000E0000h - 000FFFFFh
27:24	0x0 RW	**IF0:** F0-F7 IDSEL (IF0): IDSEL to use in FWH cycle for range enabled by BDE.EF0. The Address ranges are: FFF00000h - FFF7FFFFh, FFB00000h - FFB7FFFFh
23:20	0x1 RW	**IE8:** E8-EF IDSEL (IE8): IDSEL to use in FWH cycle for range enabled by BDE.EE8. The Address ranges are: FFE80000h - FFEFFFFFh, FFA80000h - FFAFFFFFh
19:16	0x1 RW	**IE0:** E0-E7 IDSEL (IE0): IDSEL to use in FWH cycle for range enabled by BDE.EE0. The Address ranges are: FFE00000h - FFE7FFFFh, FFA00000h - FFA7FFFFh
15:12	0x2 RW	**ID8:** D8-DF IDSEL (ID8): IDSEL to use in FWH cycle for range enabled by BDE.ED8. The Address ranges are: FFD80000h - FFDFFFFFh, FF980000h - FF9FFFFFh
11:8	0x2 RW	**ID0:** D0-D7 IDSEL (ID0): IDSEL to use in FWH cycle for range enabled by BDE.ED0. The Address ranges are: FFD00000h - FFD7FFFFh, FF900000h - FF97FFFFh
7:4	0x3 RW	**IC8:** C8-CF IDSEL (IC8): IDSEL to use in FWH cycle for range enabled by BDE.EC8. The Address ranges are: FFC80000h - FFCFFFFFh, FF880000h - FF8FFFFFh

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x3 RW	**IC0:** C0-C7 IDSEL (IC0): IDSEL to use in FWH cycle for range enabled by BDE.EC0. The Address ranges are: FFC00000h - FFC7FFFFh, FF800000h - FF87FFFFh

10.16.14 BC—Offset 1Ch

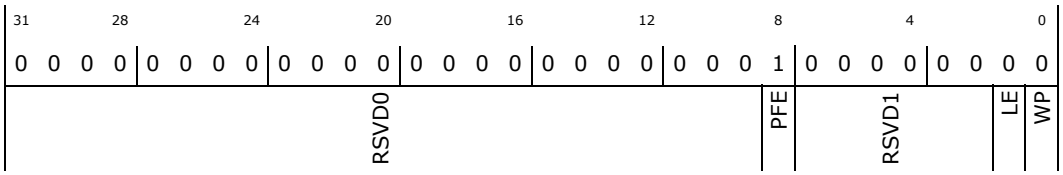
BC - BIOS Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ILB_BASE_ADDRESS] + 1Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**RSVD0:** Reserved
8	0x1 RW	**PFE:** Prefetch Enable (PFE): When set, BIOS prefetching is enabled. An access to BIOS causes a 64-byte fetch of the line starting at that region. Subsequent accesses within that region result in data being returned from the prefetch buffer. The prefetch buffer is invalidated when this bit is cleared, or a BIOS access occurs to a different line than what is currently in the buffer.
7:2	0x0 RO	**RSVD1:** Reserved
1	0x0 RW	**LE:** Lock Enable (LE): When set, setting the WP bit will cause SMIs. When cleared, setting the WP bit will not cause SMIs. Once set, this bit can only be cleared by a PMU_PLTRST_B#.
0	0x0 RW	**WP:** Write Protect (WP): When set, access to BIOS is enabled for both read and write cycles. When cleared, only read cycles are permitted to BIOS. When written from a 0 to a 1 and LE is also set, an SMI# is generated. This ensures that only SMM code can update BIOS.

10.16.15 IR0—Offset 20h

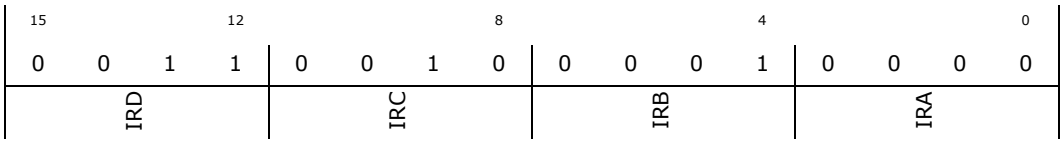
IR0 - Interrupt Routing Device 0

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 20h

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.16 IR1—Offset 22h

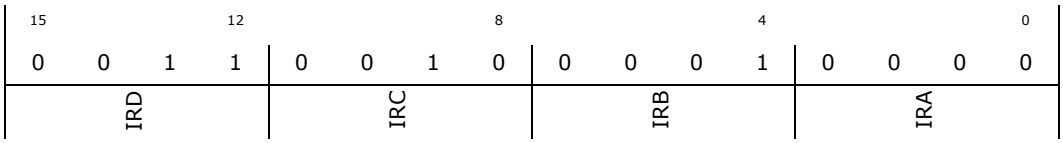
IR1 - Interrupt Routing Device 1

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 22h

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.17 IR2—Offset 24h

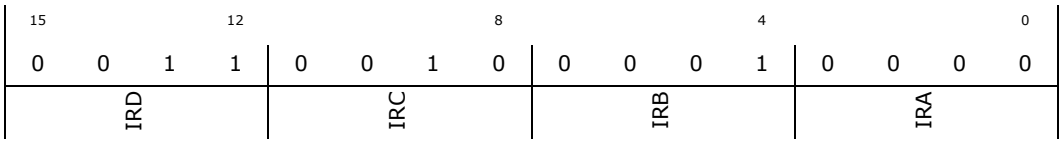
IR2 - Interrupt Routing Device 2

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 24h

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.18 IR3—Offset 26h

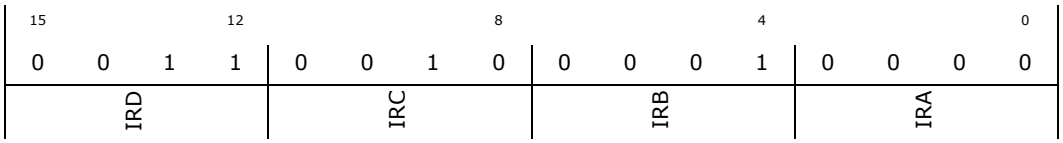
IR3 - Interrupt Routing Device 3

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 26h

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.19 IR4—Offset 28h

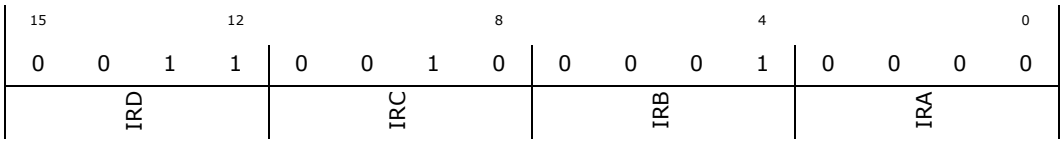
IR4 - Interrupt Routing Device 4

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 28h

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.20 IR5—Offset 2Ah

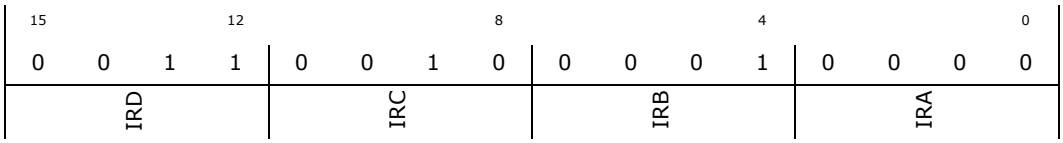
IR5 - Interrupt Routing Device 5

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 2Ah

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.21 IR6—Offset 2Ch

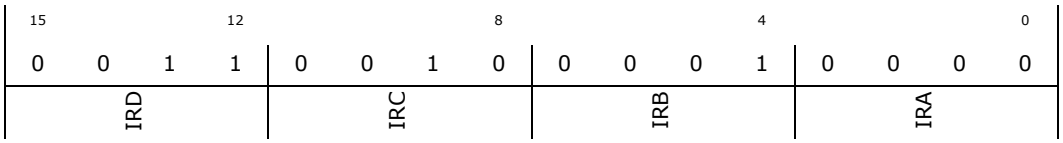
IR6 - Interrupt Routing Device 6

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 2Ch

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.22 IR7—Offset 2Eh

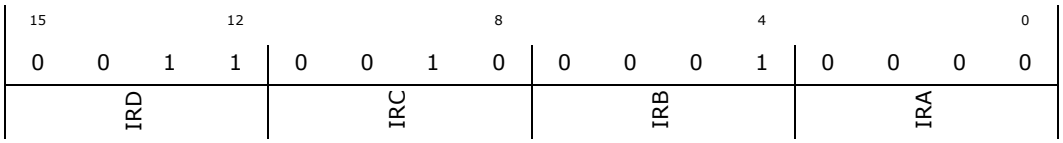
IR7 - Interrupt Routing Device 7

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 2Eh

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.23 IR8—Offset 30h

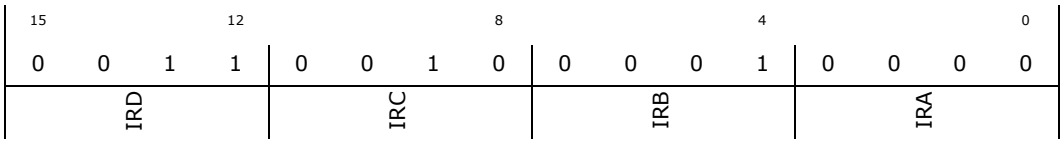
IR8 - Interrupt Routing Device 8

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 30h

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.24 IR9—Offset 32h

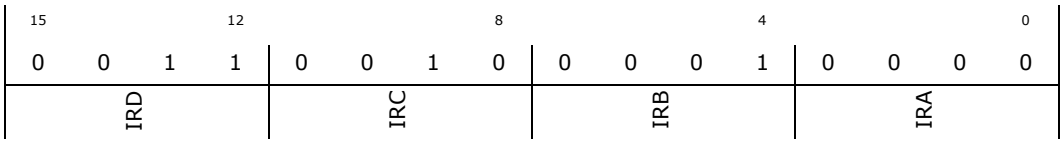
IR9 - Interrupt Routing Device 9

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 32h

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.25 IR10—Offset 34h

IR10 - Interrupt Routing Device 10

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 34h

Default: 3210h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.26 IR11—Offset 36h

IR11 - Interrupt Routing Device 11

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 36h

Default: 3210h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.27 IR12—Offset 38h

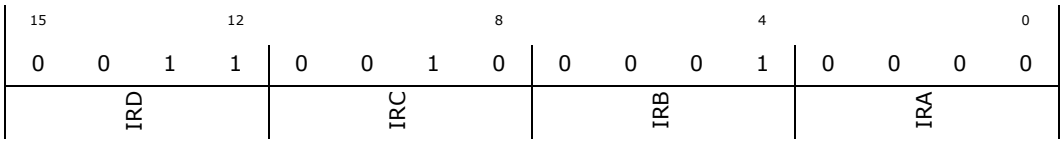
IR12 - Interrupt Routing Device 12

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 38h

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.28 IR13—Offset 3Ah

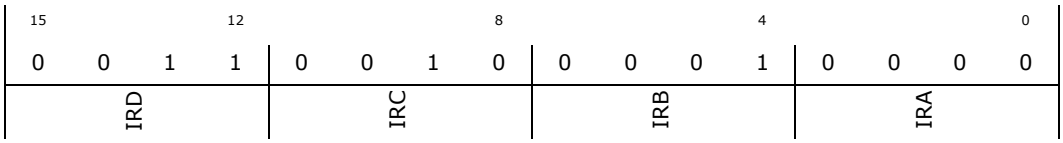
IR13 - Interrupt Routing Device 13

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 3Ah

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.29 IR14—Offset 3Ch

IR14 - Interrupt Routing Device 14

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 3Ch

Default: 3210h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.30 IR15—Offset 3Eh

IR15 - Interrupt Routing Device 15

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 3Eh

Default: 3210h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.31 IR16—Offset 40h

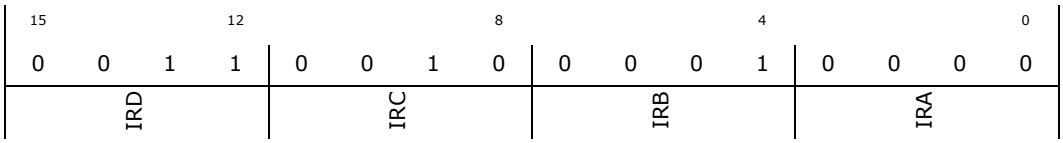
IR16 - Interrupt Routing Device 16

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 40h

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.32 IR17—Offset 42h

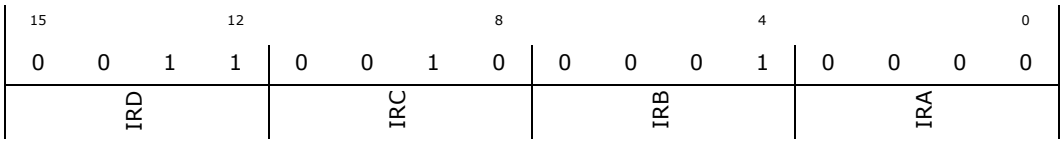
IR17 - Interrupt Routing Device 17

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 42h

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.33 IR18—Offset 44h

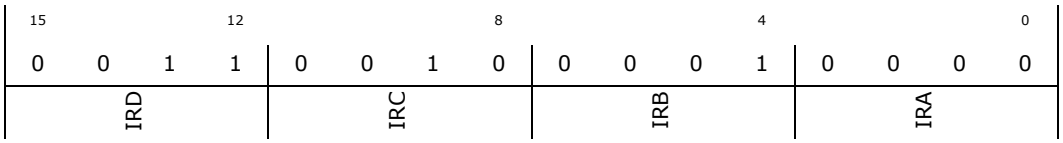
IR18 - Interrupt Routing Device 18

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 44h

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.34 IR19—Offset 46h

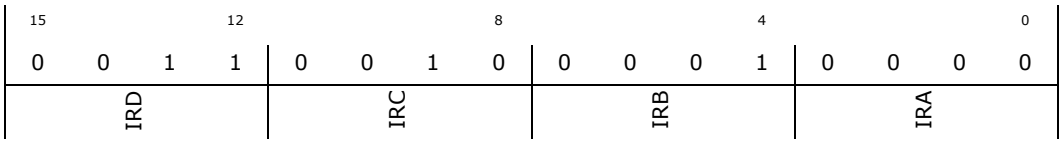
IR19 - Interrupt Routing Device 19

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 46h

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.35 IR20—Offset 48h

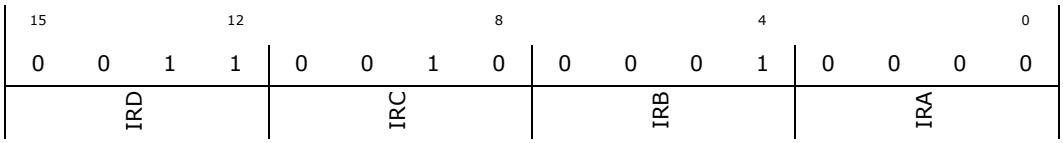
IR20 - Interrupt Routing Device 20

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 48h

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.36 IR21—Offset 4Ah

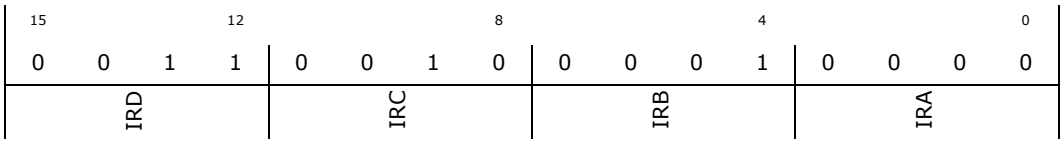
IR21 - Interrupt Routing Device 21

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 4Ah

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.37 IR22—Offset 4Ch

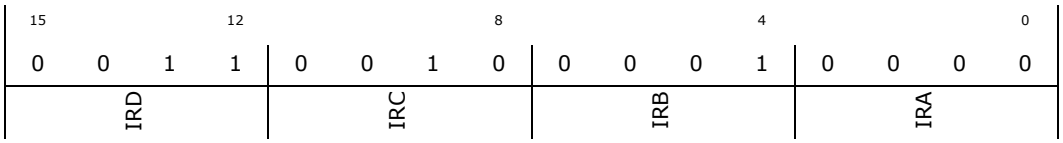
IR22 - Interrupt Routing Device 22

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 4Ch

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.38 IR23—Offset 4Eh

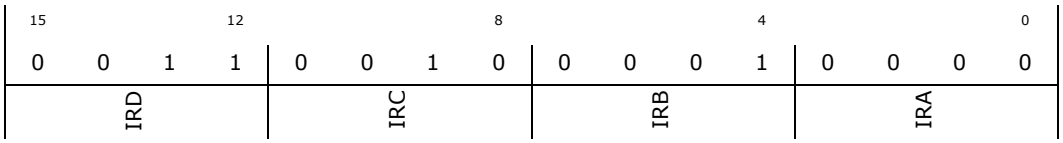
IR23 - Interrupt Routing Device 23

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 4Eh

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.39 IR24—Offset 50h

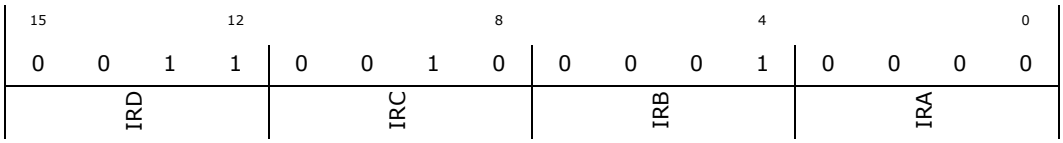
IR24 - Interrupt Routing Device 24

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 50h

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.40 IR25—Offset 52h

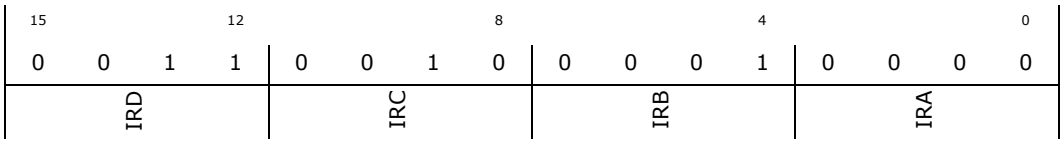
IR25 - Interrupt Routing Device 25

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 52h

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.41 IR26—Offset 54h

IR26 - Interrupt Routing Device 26

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 54h

Default: 3210h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.42 IR27—Offset 56h

IR27 - Interrupt Routing Device 27

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 56h

Default: 3210h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.43 IR28—Offset 58h

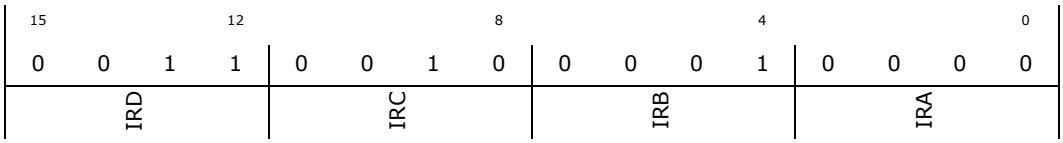
IR28 - Interrupt Routing Device 28

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 58h

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.44 IR29—Offset 5Ah

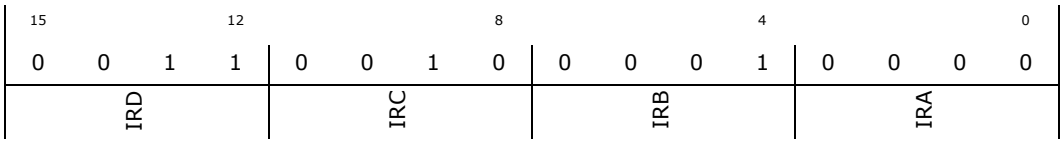
IR29 - Interrupt Routing Device 29

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 5Ah

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.45 IR30—Offset 5Ch

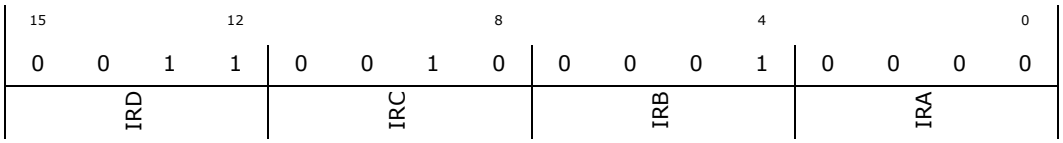
IR30 - Interrupt Routing Device 30

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 5Ch

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.46 IR31—Offset 5Eh

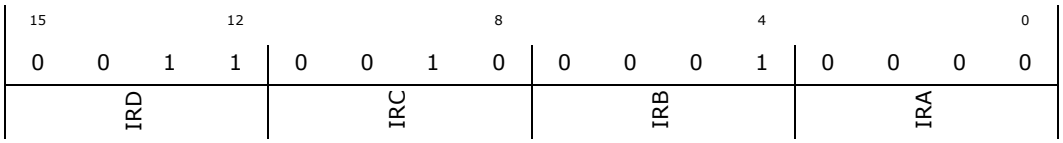
IR31 - Interrupt Routing Device 31

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

Offset: [ILB_BASE_ADDRESS] + 5Eh

Default: 3210h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0x3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	0x2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	0x1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	0x0 RW	**IRA:** INTA mapping to IRQ A-H

10.16.47 OIC—Offset 60h

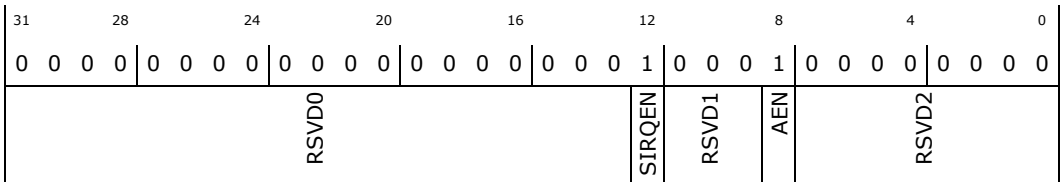
Other Interrupt Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ILB_BASE_ADDRESS] + 60h

Default: 00001100h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RO	**RSVD0:** Reserved
12	0x1 RW	**SIRQEN:** When set, enables the internal SIRQ . when cleared the internal sIRQ is disabled
11:9	0x0 RO	**RSVD1:** Reserved
8	0x1 RW	**AEN:** When set, enables the internal IOAPIC and its address decode, when cleared the internal IOxAPIC is disabled. software should read this register after modifying the APIC enable prior to acces to IOxAPIC addresss range. comment: en Couger Point the default value is 0
7:0	0x0 RO	**RSVD2:** Reserved

10.16.48 RC—Offset 64h

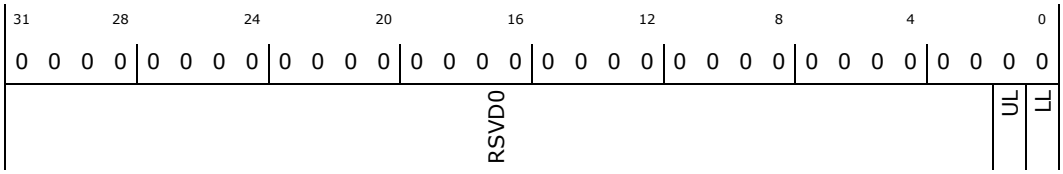
RC - RTC Configuration

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ILB_BASE_ADDRESS] + 64h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**RSVD0:** Reserved
1	0x0 RW/L	**UL:** Upper 128 Byte Lock (UL): When set, bytes 38h-3Fh in the upper 128 byte bank of RTC RAM are locked. Writes will be dropped and reads will not return any guaranteed data.
0	0x0 RW/L	**LL:** Lower 128 Byte Lock (LL): When set, bytes 38h-3Fh in the lower 128 byte bank of RTC RAM are locked. Writes will be dropped and reads will not return any guaranteed data.

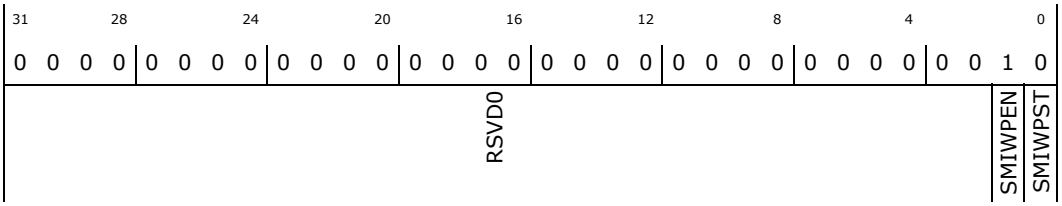
10.16.49 BCS - BIOS Control Status (BCS)—Offset 6Ch

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ILB_BASE_ADDRESS] + 6Ch

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**RSVD0:** Reserved
1	0x1 RW	**SMIWPEN:** SMI WPD Enable (SMIWPEN): When this bit is set to a 1, it enables the LPC to generate SMI upon not SMM code is trying to set BCR.WPD from a 0 to a 1 while BCR.LE is set.
0	0x0 RW/1C	**SMIWPST:** SMI WPD Status (SMIWPST): Set when SMI is generated upon trying to set BCR.WPD from a 0 to a 1 by not SMM code (while BCR.LE and SMIWPEN are set). Write a 1 to this bit should clear it and clear the SMI (send DEASSERT_SMI)

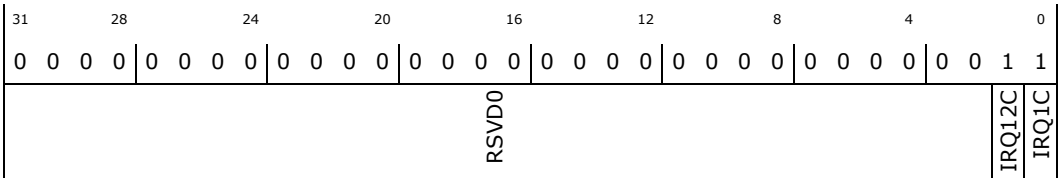
10.16.50 LE—Offset 70h

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ILB_BASE_ADDRESS] + 70h

Default: 00000003h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**RSVD0:** Reserved
1	0x1 RW	**IRQ12_CAUSE (IRQ12C):** When software sets the bit to 1, IRQ12 will be high (asserted), When software set bit to 0,IRQ12 will be low (deasserted). default for this bit is 1

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**IRQ1_CAUSE (IRQ1C):** When software sets the bit to 1, IRQ11 will be high (asserted), When software set bit to 0,IRQ1 will be low (deasserted). default for this bit is 1

10.16.51 NMI (GNMI)—Offset 80h

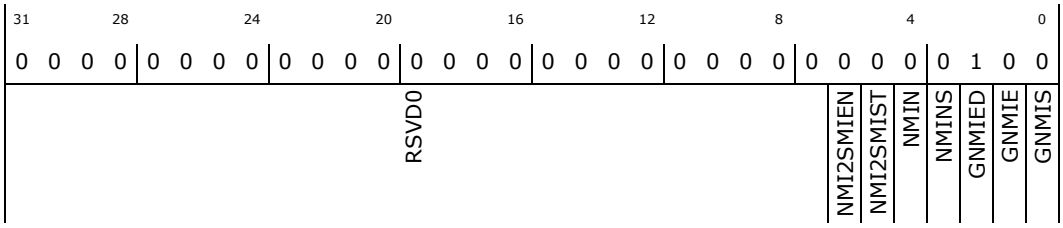
NMI register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ILB_BASE_ADDRESS] + 80h

Default: 00000004h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0x0 RO	**RSVD0:** Reserved
6	0x0 RW	**NMI2SMIEN:** NMI to SMI Enable (NMI2SMIEN): When set, instead of NMI messgae SMI message will be sent.
5	0x0 RO	**NMI2SMIST:** NMI to SMI bit Status (NMI2SMIST)
4	0x0 RW/1C	**NMIN:** NMI NOW (NMIN): When set, NMI messgae will be sent. Writing 1'b1 to NMI_NOW inverts NMI_MOW and NMI_NOW_STS value
3	0x0 RO	**NMINS:** NMI_NOW_STS is a result of the NMI_NOW configuration bit. Writing 1'b1 to NMI_NOW inverts NMI_NOW_STS value. Resulting that the first time NMI_NOW is written sets the NMI_NOW_STS and initiates NMI. Next writing clears the NMI_NOW_STS and allows initiating NMI by the next writing to NMI_NOW
2	0x1 RW	**GNMIED:** GPIO NMI Edge Detction (GNMIED): When set, NMI messgae will be sent on NMI GPIO posedge. when cleared the NMI message will be sent on negedge
1	0x0 RW	**GNMIE:** GPIO NMI Enable (GNMIE): When set, NMI messgae will be sent when NMI GPIO occurred. when cleared the message will not be sent
0	0x0 RW/1C	**GNMS (GNMIS):** GPIO NMI Status (GNMIS), when NMI is recieved from GPIO this bit is set. write '1' to this register to clear the status bit

10.16.52 LPCC—Offset 84h

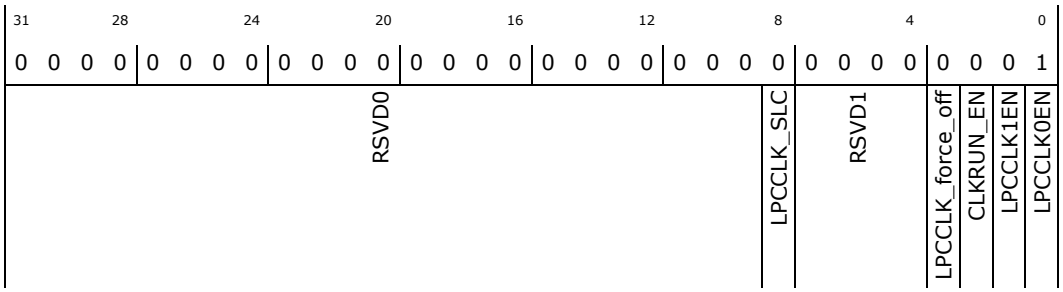
LPC Control register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ILB_BASE_ADDRESS] + 84h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**RSVD0:** Reserved
8	0x0 RO	**LPCCLK_SLC:** iLPCCLK mux select (0 - ilpcclk0, 1 ilpcclk1)This bit get value from soft strap.
7:4	0x0 RO	**RSVD1:** Reserved
3	0x0 RW	**LPCCLK_force_off:** when asserted,oLPCCLK shut off similarly to CLKRUN protocol while ignoring iCLKRUN (LPC device reactions)
2	0x0 RW	**CLKRUN_EN:** LPC CLKRUN protocol enable (when not asserted, oLPCCLK toggles)
1	0x0 RO	**LPCCLK1EN:** Clock 1 Enable (EN): This bit get value from soft strap. When set, LPC clock 1 is enabled. When cleared, it is disabled.
0	0x1 RO	**LPCCLK0EN:** Clock 0 Enable (EN): When set, LPC clock 0 is enabled. When cleared, it is disabled.

10.16.53 IRQEN (IRQE)—Offset 88h

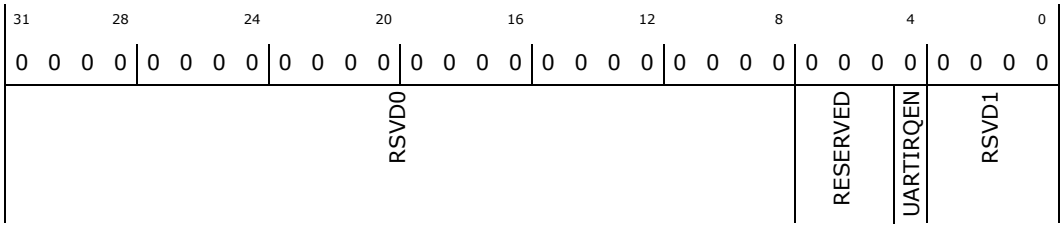
IRQ Enable Control

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [ILB_BASE_ADDRESS] + 88h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7:5	0x0 RO	**RESERVED:**
4	0x0 RO	**UARTIRQEN:** UART IRQ4 Enable
3:0	0x0 RO	**RSVD1:** Reserved

10.17 PCU PMC ACPI I/O Registers

Table 112. Summary of PMC ACPI I/O Registers—ACPI_BASE_ADDRESS

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"PM1_STS_EN - Power Management 1 Status and enable (PM1_STS_EN)—Offset 0h" on page 5819	00000000h
4–7h	4	"PM1_CNT - Power Management 1 Control (PM1_CNT)—Offset 4h" on page 5822	00000000h
8–Bh	4	"PM1_TMR - Power Management 1 Timer (PM1_TMR)—Offset 8h" on page 5822	00000000h
20–23h	4	"GPE0a_STS - General Purpose Event 0 Status (GPE0a_STS)—Offset 20h" on page 5823	00000000h
28–2Bh	4	"GPE0a_EN - General Purpose Event 0 Enables (GPE0a_EN)—Offset 28h" on page 5826	00000000h
30–33h	4	"SMI_EN - SMI Control and Enable (SMI_EN)—Offset 30h" on page 5828	00000002h
34–37h	4	"SMI_STS - SMI Status Register (SMI_STS)—Offset 34h" on page 5829	00000000h
38–3Bh	4	"ALT_GPIO_SMI - Alternate GPIO SMI Status and Enable Register. (ALT_GPIO_SMI)—Offset 38h" on page 5831	00000000h
3C–3Fh	4	"UPRWC - USB Per-Port Registers Write Control (UPRWC)—Offset 3Ch" on page 5832	00000000h
40–43h	4	"GPE_CTRL - General Purpose Event Control (GPE_CTRL)—Offset 40h" on page 5833	00000000h
50–53h	4	"PM2A_CNT_BLK - PM2a Control Block (PM2A_CNT_BLK)—Offset 50h" on page 5834	00000000h
60–63h	4	"TCO_RLD: TCO Reload Register (TCO_RLD)—Offset 60h" on page 5834	00000000h
64–67h	4	"TCO_STS: TCO Timer Status (TCO_STS)—Offset 64h" on page 5835	00000000h
68–6Bh	4	"TCO1_CNT: TCO Timer Control (TCO1_CNT)—Offset 68h" on page 5836	00000000h
70–73h	4	"TCO_TMR: TCO Timer Register (TCO_TMR)—Offset 70h" on page 5837	00040000h

10.17.1 PM1_STS_EN - Power Management 1 Status and enable (PM1_STS_EN)—Offset 0h

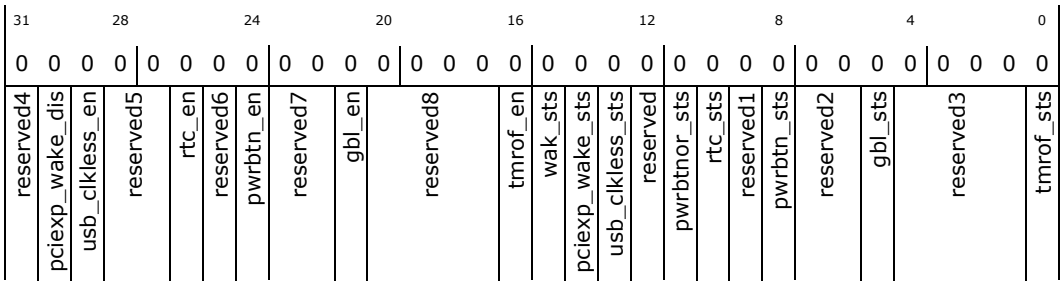
Power Management 1 Status and Enable

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [ACPI_BASE_ADDRESS] + 0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**reserved4:** Reserved.
30	0x0 RW	**PCI Express Wake Disable (PCIEXP_WAKE_DIS) (pciexp_wake_dis):** This bit disables the inputs to the PCIEXP_WAKE_STS bit in the PM1 Status register from waking the system. Modification of this bit has no impact on the value of the PCIEXP_WAKE_STS bit. reset_type=Resume Well Reset#
29	0x0 RW	**USB clockless Wake Enable (USB_CLKLESS_EN) (usb_clkless_en):** This bit enables the inputs to the USB_CLKLESS_STS bit in the PM1 Status register to wake the system. Modification of this bit has no impact on the value of the USB_CLKLESS_STS bit. reset_type=Resume Well Reset#
28:27	0x0 RO	**reserved5:** Reserved.
26	0x0 RW	**RTC Alarm Enable (RTC_EN) (rtc_en):** This is the RTC alarm enable bit. It works in conjunction with the SCI_EN bit: RTC_EN SCI_EN Effect when RTC_STS is set 0 x No SMI# or SCI. If system was in S1-S5, no wake even occurs. 1 0 SMI#. If system was in S1-S5, then a wake event occurs before the SMI#. 1 1 SCI. If system was in S1-S5, then a wake event occurs before the SCI. Note: This bit needs to be backed by the RTC well to allow an RTC event to wake after a power failure. In addition to being reset by SRTCRST_B assertion, PMC also clears this bit due to certain events: - Power button override - CPU thermal trip reset_type=SRTCRST_B
25	0x0 RO	**reserved6:** Reserved.
24	0x0 RW	**Power Button Enable (PWRBTN_EN) (pwrbtn_en):** This bit is the power button enable. It works in conjunction with the SCI_EN bit: PWRBTN_EN SCI_EN Effect when PWRBTN_STS is set 0 x No SMI# or SCI. 1 0 SMI#. 1 1 SCI. reset_type=Resume Well Reset#
23:22	0x0 RO	**reserved7:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21	0x0 RW	**Global Enable (GBL_EN) (gbl_en):** The global enable bit. When both the GBL_EN and the GBL_STS are set, PMC generates an SCI. reset_type=PMU_PLTRST_B
20:17	0x0 RO	**reserved8:** Reserved.
16	0x0 RW	**Timer Overflow Interrupt Enable (TMROF_EN) (tmrof_en):** This is the timer overflow interrupt enable bit. It works in conjunction with the SCI_EN bit: TMROF_EN SCI_EN Effect when TMROF_STS is set 0 x No SMI# or SCI. . 1 0 SMI#. 1 1 SCI. reset_type=PMU_PLTRST_B
15	0x0 RW/1C	**Wake Status (WAK_STS) (wak_sts):** This bit is set when the system is in one of the Sleep states (via the SLP_EN bit) and an enabled Wake event occurs. Upon setting this bit, the PMC will transition the system to the ON state. This bit can only be set by hardware and can only be cleared by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST_B. If a power failure occurs (such as removed batteries) without the SLP_EN bit set, the WAK_STS bit will not be set when the power returns if the AFTER_G3 bit is 0. If the AFTER_G3 bit is 1, then the WAK_STS bit will be set after waking from a power failure. If necessary, the BIOS can clear the WAK_STS bit in this case This is based on discussions with Microsoft. That behavior is not in the ACPI spec. reset_type=RSMRST_B
14	0x0 RW/1C	**PCI Express Wake Status (PCIEXP_WAKE_STS) (pciexp_wake_sts):** This bit is set by hardware to indicate that the system woke due to a PCI Express wakeup event. This event can be caused by the PCI Express WAKE# pins (PCI_WAKE0_B, PCI_WAKE1_B, PCI_WAKE2_B, PCI_WAKE3_B) being active, or one or more of the PCI Express ports being in beacon state, or recept of a PCI Express PME message at root port. This bit should only be set when one of these events causes the system to transition from a non-S0 system power state to the S0 system power state. This bit is set independent of the PCIEXP_WAKE_DIS bit. Software writes a 1 to clear this bit. If one of the WAKE# pins is still active during the write or one or more PCI Express ports is in the beacon state or PME message received indication is not cleared in the root port, then the bit will remain Power Management active (i.e. all inputs to this bit are level sensitive) Note: This bit does not itself cause a wake event or prevent entry to a sleeping state. Thus if the bit is 1 and the system is put into a sleeping state, the system will not automatically wake. PMC FW chicken bit is available to route PMU_WAKE_B to this logic, enabling semi-backwards compatibility (NOT SCI) PMC FW cfg register with chicken bit is PLTFRM_CFG[0] reset_type=pmc_global_rst_b
13	0x0 RW/1C	**USB clockless Wake Status (USB_CLKLESS_STS) (usb_clkless_sts):** This bit is set by hardware to indicate that the system woke due to change in USB serial lines. This bit is set independant of the USB_CLKLESS_EN bit. Software writes a 1 to clear this bit. reset_type=pmc_global_rst_b
12	0x0 RO	**reserved:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	0x0 RW/1C	**Power Button Override (PWRBTNOR_STS) (pwrbtnor_sts):** This bit is set any time a Power Button Override Event occurs (i.e. the power button is pressed for at least 4 consecutive seconds), or due to an internal thermal sensor catastrophic condition. These events cause an unconditional transition to the S5 state. The BIOS or SCI handler clears this bit by writing a 1 to it. This bit is not affected by hard resets via CF9h writes, and is not reset by RSMRST_B. Thus, this bit is preserved through power failures. Note that this bit is still asserted when the global SCI_EN is set to '1' then an SCI will be generated. reset_type=SRTCRST_B
10	0x0 RW/1C	**RTC Status (RTC_STS) (rtc_sts):** This bit is set when the RTC generates an alarm (assertion of the IRQ8# signal), and is not affected by any other enable bit. Refer RTC_EN for the effect when RTC_STS goes active. This bit is only set by hardware and can only be reset by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST_B. reset_type=RSMRST_B
9	0x0 RO	**reserved1:** Reserved.
8	0x0 RW/1C	**Power Button Status (PWRBTN_STS) (pwrbtn_sts):** This bit is set when the PMU_PWRBTN_B signal is asserted (low), independent of any other enable bit. Refer PWRBTN_EN for the effect when PWRBTN_STS goes active. PWRBTN_STS is always a wake event when PWRBTN_EN is 1'b1. This bit is only set by hardware and can be cleared by software writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST_B. If the PMU_PWRBTN_B signal is held low for more than 4 seconds, the PMC clears the PWRBTN_STS bit, sets the PWRBTNOR_STS bit, the system transitions to the S5 state, and only PMU_PWRBTN_B is enabled as a wake event. If PWRBTN_STS bit is cleared by software while the PMU_PWRBTN_B pin is still held low, this will not cause the PWRBTN_STS bit to be set. The PMU_PWRBTN_B signal must go inactive and active again to set the PWRBTN_STS bit. Note that the CPU Thermal Trip and the Internal Thermal Sensors' Catastrophic Condition result in behavior matching the Powerbutton Override, which includes clearing this bit. reset_type=RSMRST_B
7:6	0x0 RO	**reserved2:** Reserved.
5	0x0 RW/1C	**GBL Status (GBL_STS) (gbl_sts):** This bit is set when an SCI is generated due to the BIOS wanting the attention of the SCI handler. BIOS has a corresponding bit, BIOS_RLS, which will cause an SCI and set this bit. The SCI handler should then clear this bit by writing a 1 to it. This bit will not cause wake events or SMI#. This bit is not effected by SCI_EN. Note: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place. reset_type=PMU_PLTRST_B
4:1	0x0 RO	**RESERVED (reserved3):** Reserved.
0	0x0 RW/1C	**Timer Overflow Status (TMROF_STS) (tmrof_sts):** This is the timer overflow status bit. This bit gets set anytime bit 22 of the 24 bit timer goes low (bits are counted from 0 to 23). This will occur every 2.3435 seconds. Refer TMROF_EN for the effect when TMROF_STS goes active. Software clears this bit by writing a 1 to it. reset_type=PMU_PLTRST_B

10.17.2 PM1_CNT - Power Management 1 Control (PM1_CNT)—Offset 4h

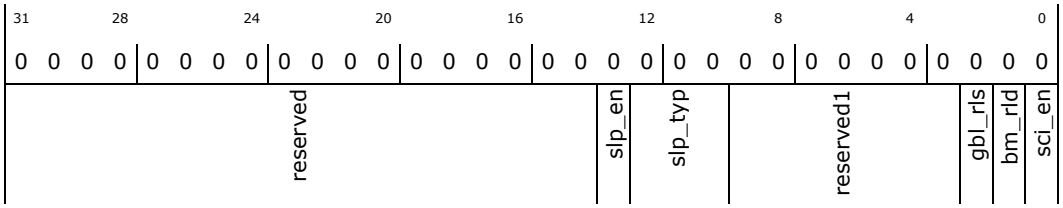
Power Management Control register

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [ACPI_BASE_ADDRESS] + 4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**reserved:** Reserved.
13	0x0 WO	**Sleep Enable (SLP_EN) (slp_en):** This is a write-only bit and reads to it always return a zero. Setting this bit causes the system to sequence into the Sleep state defined by the SLP_TYP field.
12:10	0x0 RW	**Sleep Type (SLP_TYP) (slp_typ):** This 3-bit field defines the type of Sleep the system should enter when the SLP_EN bit is set to 1. These bits are reset by SRTCRST_B only. Bits Mode Typical Mapping 000 ON S0 001 Puts CPU in S1 state. S1 010 Reserved 011 Reserved 100 Reserved 101 Suspend-To-RAM S3 110 Suspend-To-Disk S4 111 Soft Off S5
9:3	0x0 RO	**reserved1:** Reserved.
2	0x0 RO	**GBL_RLS (GBL_RLS) (gbl_rls):** This bit is used by the ACPI software to raise an event to the BIOS software. BIOS software has a corresponding enable and status bits to control its ability to receive ACPI events. This bit always reads as 0.
1	0x0 RW	**BM_RLD (BM_RLD) (bm_rld):** This bit is treated as a scratchpad bit
0	0x0 RW	**SCI Enable (SCI_EN) (sci_en):** SCI Enable (SCI_EN): Selects the SCI interrupt or the SMI# for various events. When this bit is 1, then the events will generate an SCI interrupt. When this bit is 0, these events will generate an SMI#.

10.17.3 PM1_TMR - Power Management 1 Timer (PM1_TMR)—Offset 8h

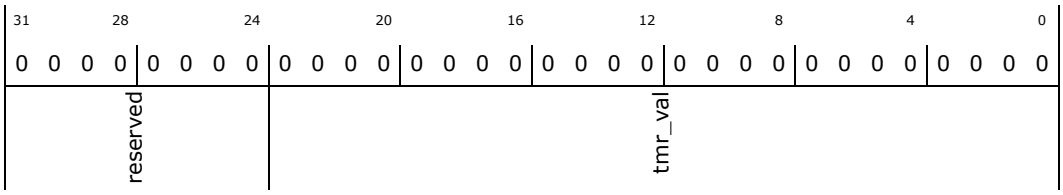
Power Management 1 Timer

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [ACPI_BASE_ADDRESS] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**reserved:** Reserved.
23:0	0x0 RO	**Timer Value (TMR_VAL) (tmr_val):** This read-only field returns the running count of the PM timer. This counter runs off a 3.579545 MHz clock (derived from 14.31818 MHz divided by 4). It is reset (to 0) during a Platform reset, and then continues counting as long as the system is in the S0 state. Anytime bit 22 of the timer goes HIGH to LOW (bits referenced from 0 to 23), the TMROF_STS bit is set. The High-to-Low transition will occur every 2.3435 seconds. Writes to this register have no effect.

10.17.4 GPE0a_STS - General Purpose Event 0 Status (GPE0a_STS)—Offset 20h

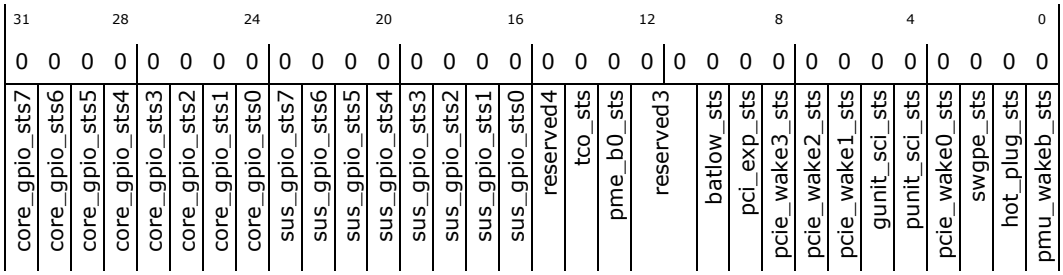
Note: This register is symmetrical to the General Purpose Event 0a Enable Register. Unless indicated otherwise below, if the corresponding _EN bit is set, then when the STS bit get set, the PMC will generate a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the PMC will also generate an SCI if the SCI_EN bit is set, or an SMI# if the SCI_EN bit is not set. CLARIFICATION: Bits 15:0 should not be reset by CF9 write. Bits 31:16 are reset by CF9h full resets. reset_type=RSMRST_B

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [ACPI_BASE_ADDRESS] + 20h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts7):** These bits are set any time the corresponding Core GPIO is set up as an input and the corresponding GPIO signal is asserted. CORE GPIO pins are GPIO_SOUTHWEST0-7. PCIE_CLKREQ0B (GPIO SW 3) PCIE_CLKREQ1B (GPIO SW 4) PCIE_CLKREQ2B (GPIO SW 5) PCIE_CLKREQ3B (GPIO SW 6) PCIE_CLKREQ4B (GPIO SW 7) If the corresponding enable bit is set in the GPE0a_EN register, then when the CORE_GPIO_STS[n] bit is set, an SCI will be caused, depending on the GPIO_ROUT bits for the corresponding GPIO. These bits are sticky bits and are cleared by writing a 1 back to this bit position. reset_type=Resume Well Reset#
30	0x0 RW/1C	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts6):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
29	0x0 RW/1C	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts5):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
28	0x0 RW/1C	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts4):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
27	0x0 RW/1C	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts3):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
26	0x0 RW/1C	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts2):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
25	0x0 RW/1C	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts1):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
24	0x0 RW/1C	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts0):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
23	0x0 RW/1C	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts7):** These bits are set any time the corresponding Sus GPIO is set up as an input and the corresponding GPIO signal is asserted. Sus GPIO pins are GPIO_NORTH0-7. If the corresponding enable bit is set in the GPE0a_EN register, then when the SUS_GPIO_STS[n] bit is set: * If the system is in an S3-S5 state, the event will also wake the system. * If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIO_ROUT bits for the corresponding GPI. These bits are sticky bits and are cleared by writing a 1 back to this bit position. reset_type=Resume Well Reset#
22	0x0 RW/1C	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts6):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
21	0x0 RW/1C	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts5):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
20	0x0 RW/1C	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts4):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
19	0x0 RW/1C	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts3):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
18	0x0 RW/1C	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts2):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
17	0x0 RW/1C	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts1):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)

Bit Range	Default & Access	Field Name (ID): Description
16	0x0 RW/1C	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts0):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
15	0x0 RO	**reserved (reserved4):** Reserved.
14	0x0 RW/1C	**TCO Status (TCO_STS): (tco_sts):** Indicates an SCI or SMI was caused by the TCO logic. This bit is cleared by writing a 1 to this bit position.
13	0x0 RW/1C	**Power Management Event Bus 0 Status (PME_B0_STS) (pme_b0_sts):** This bit will be set to 1 by the PMC when any internal device with PCI Power Management capabilities on bus 0 asserts the equivalent of the PME# signal. Additionally, if the PME_B0_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the PME_B0_STS bit will generate an SCI (or SMI# if SCI_EN is not set). This bit is cleared by a software write of '1'. Internal devices which can set this bit: - Integrated LAN - USB
12:11	0x0 RO	**reserved (reserved3):** Reserved.
10	0x0 RW/1C	**Battery Low Status (BATLOW_STS) (batlow_sts):** This bit will be set to 1 by hardware when the PMU_BATLOW_B signal goes low. Software clears the bit by writing a 1 to the bit position. In Desktop Mode, this bit will be treated as Reserved.
9	0x0 RW/1C	**PCI Express Status (PCI_EXP_STS) (pci_exp_sts):** This bit will be set to 1 by hardware to indicate that: - The PME event message was received on one or more of the PCI-Express Ports Note: The PCI PMU_WAKE_B pin and the PCI-Express Beacons have no impact on this bit. Software attempts to clear this bit by writing a 1 to this bit position. If the bit is not cleared and the corresponding PCI_EXP_EN bit is set, the leveltriggered SCI will remain active. Note that a race condition exists where the PCI Express device sends another PME message because the PCI Express device was not serviced within the time when it must resend the message. This may result in a spurious interrupt, and this is comprehended and approved by the PCI Express specification. The window for this race condition is approximately 95-105 milliseconds.
8	0x0 RW/1C	**PCI Express Wake3 Status (PCIE_WAKE3_STS) (pcie_wake3_sts):** This bit is set by hardware to indicate that the PCI_WAKE3_B pin was asserted. Software writes a 1 to clear this bit. If PCI_WAKE3_B pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). reset_type=pmc_global_rst_b
7	0x0 RW/1C	**PCI Express Wake2 Status (PCIE_WAKE2_STS) (pcie_wake2_sts):** This bit is set by hardware to indicate that the PCI_WAKE2_B pin was asserted. Software writes a 1 to clear this bit. If PCI_WAKE2_B pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). reset_type=pmc_global_rst_b
6	0x0 RW/1C	**PCI Express Wake1 Status (PCIE_WAKE1_STS) (pcie_wake1_sts):** This bit is set by hardware to indicate that the PCI_WAKE1_B pin was asserted. Software writes a 1 to clear this bit. If PCI_WAKE1_B pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). reset_type=pmc_global_rst_b

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RW/1C	**GUNIT SCI status (GUNIT_SCI_STS) (gunit_sci_sts):** This bit will be set if the Graphics Unit requests SCI
4	0x0 RW/1C	**PUNIT SCI status (PUNIT_SCI_STS) (punit_sci_sts):** This bit will be set if the Power Management Unit requests SCI
3	0x0 RW/1C	**PCI Express Wake0 Status (PCIE_WAKE0_STS) (pcie_wake0_sts):** This bit is set by hardware to indicate that the PCIE_WAKE0_B pin was asserted. Software writes a 1 to clear this bit. If PCIE_WAKE0_B pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). reset_type=pmc_global_rst_b
2	0x0 RW/1C	**Software GPE Status (SWGPE_STS) (swgpe_sts):** The SWGPE_CTRL bit (bit 1 of GPE_CTRL reg) acts as a level input to this bit.
1	0x0 RO	**Hot Plug Status (HOT_PLUG_STS) (hot_plug_sts):** This bit is set to 1 by hardware when a PCI-Express hotplug event occurs. This will cause an SCI if the HOT_PLUG_EN and SCI_EN bits are set. This bit is cleared by writing a 1 to this bit position. The following events cause this bit to set - Assert_GPE message received from any of the PCI_E ports in the SOC - Assert_HPGPE message received from any of the PCI_E ports in the SOC
0	0x0 RW/1C	**PMU_WAKE_B Wake Status (PMU_WAKE_B_STS) (pmu_wakeb_sts):** This bit is set by hardware to indicate that the system woke due to a PMU_WAKE_B wakeup event. This bit is set independently of the GPIO_WAKE_DIS bit. Software writes a 1 to clear this bit. reset_type=pmc_global_rst_b

10.17.5 GPE0a_EN - General Purpose Event 0 Enables (GPE0a_EN)—Offset 28h

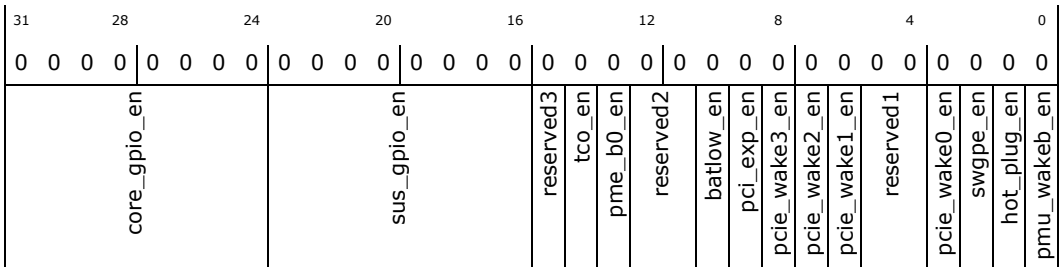
Note: This register is symmetrical to the General Purpose Event 0a Status Register.
reset_type=Resume Well Reset#

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [ACPI_BASE_ADDRESS] + 28h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW	**CORE GPIO Enable (CORE_GPIO_EN) (core_gpio_en):** These bits enable the corresponding CORE_GPIO_STS[n] bits being set to cause an SCI and/or wake event.
23:16	0x0 RW	**SUS GPIO Enable (SUS_GPIO_EN) (sus_gpio_en):** These bits enable the corresponding SUS_GPIO_STS[n] bits being set to cause an SCI and/or wake event.
15	0x0 RO	**reserved (reserved3):** Reserved.
14	0x0 RW	**TCO Enable (TCO_EN): (tco_en):** when set Enables the TCO logic to generate an SCI or SMI#. when cleared disables TCO logic generating an SMI#. NOTE: This bit can not be written once the TCO_LOCK bit is set. This prevents unauthorized software from disabling the generation of TCO-based SMI's
13	0x0 RW	**PME_B0 Enable (PME_B0_EN) (pme_b0_en):** Enables the setting of the PME_B0_STS bit to generate a wake event and/or an SCI or SMI#. In addition to being reset by SRTCRST_B assertion, the PMC also clears this bit due to certain events: - Power button override - CPU thermal trip reset_type=SRTCRST_B
12:11	0x0 RO	**reserved (reserved2):** Reserved.
10	0x0 RW	**Low Battery Enable (BATLOW_EN) (batlow_en):** This bit enables the PMU_BATLOW_B signal to cause an SMI# or SCI (depending on the SCI_EN bit) when it goes low.This bit does not prevent the PMU_BATLOW_B signal from inhibiting the wake event. In Desktop Mode this bit will be treated as Reserved. In addition to being reset by SRTCRST_B assertion, the PMC also clears this bit due to certain events: - Power button override - CPU thermal trip reset_type=SRTCRST_B
9	0x0 RW	**PCI Express Enable (PCI_EXP_EN) (pci_exp_en):** Enables the PMC to cause an SCI when PCI_EXP_STS bit is set. This is used to allow the PCI Express ports, to cause an SCI due to wake/PME events
8	0x0 RW	**PCI Express Wake3 Enable (PCIE_WAKE3_EN) (pcie_wake3_en):** This bit, when set to 1, enables the PCIE_WAKE3_STS to to cause an SCI
7	0x0 RW	**PCI Express Wake2 Enable (PCIE_WAKE2_EN) (pcie_wake2_en):** This bit, when set to 1, enables the PCIE_WAKE2_STS to to cause an SCI
6	0x0 RW	**PCI Express Wake1 Enable (PCIE_WAKE1_EN) (pcie_wake1_en):** This bit, when set to 1, enables the PCIE_WAKE1_STS to to cause an SCI
5:4	0x0 RO	**reserved (reserved1):** Reserved.
3	0x0 RW	**PCI Express Wake0 Enable (PCIE_WAKE0_EN) (pcie_wake0_en):** This bit, when set to 1, enables the PCIE_WAKE0_STS to to cause an SCI
2	0x0 RW	**Software GPE Enable (SWGPE_EN) (swgpe_en):** This bit, when set to 1, enables the SW GPE function. If SWGPE_CTRL is written to a 1, hardware will set SWGPE_STS (acts as a level input) If SWGPE_STS, SWGPE_EN, and SCI_EN are all 1's, an SCI will be generated If SWGPE_STS = 1, SWGPE_EN = 1, SCI_EN = 0, and GBL_SMI_EN = 1 then an SMI# will be generated
1	0x0 RW	**Hot Plug Enable (HOT_PLUG_EN) (hot_plug_en):** Enables the PMC to cause an SCI when the HOT_PLUG_STS bit is set. This is used to allow the PCI Express ports to cause an SCI due to hot-plug events.

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**PMU_WAKEB Enable (PMU_WAKEB_EN) (pmu_wakeb_en):** Enables the PMC to cause an SCI when the PMU_WAKEB_STS bit is set. This is used to allow the PMU_WAKEB to cause an SCI due to GPIO PMU_WAKEB events

10.17.6 SMI_EN - SMI Control and Enable (SMI_EN)—Offset 30h

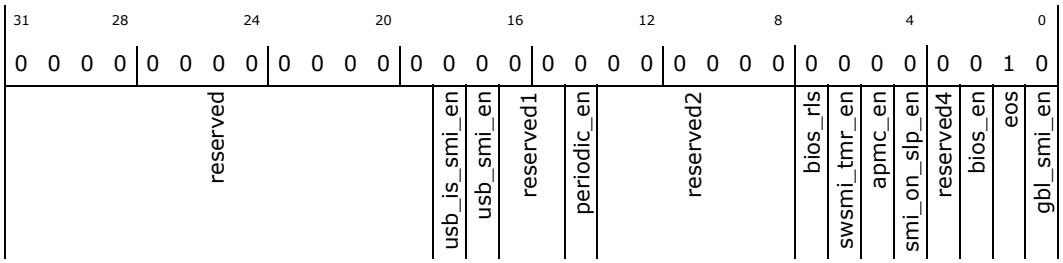
SMI Control and Enable Register

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [ACPI_BASE_ADDRESS] + 30h

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0x0 RO	**reserved:** Reserved.
18	0x0 RW	**Intel USB 2 Enable (USB_IS_SMI_EN): (usb_is_smi_en):** Enables Intel-Specific USB2 SMI logic to cause SMI#.
17	0x0 RW	**USB SMI Enable (USB_SMI_EN): (usb_smi_en):** Enables SMI from USB
16:15	0x0 RO	**reserved1:** Reserved.
14	0x0 RW	**Periodic Enable (PERIODIC_EN) (periodic_en):** Setting this bit will cause the PMC to generate an SMI# when the PERIODIC_STS bit is set in the SMI_STS register.
13:8	0x0 RO	**reserved2:** Reserved.
7	0x0 RO	**BIOS_RLS (BIOS_RLS): (bios_rls):** Enables the generation of an SCI interrupt for ACPI software when a one is written to this bit position by BIOS software. This bit always reads a zero. NOTE: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place.

Bit Range	Default & Access	Field Name (ID): Description
6	0x0 RW	**Software SMI Timer Enable (SWSMI_TMR_EN): (swsmi_tmr_en):** Software sets this bit to a 1 to start the Software SMI# Timer. When the timer expires (depending on the SWSMI_RATE_SEL bits), it will generate an SMI# and set the SWSMI_TMR_STS bit. The SWSMI_TMR_EN bit will remain at 1 until software sets it back to 0. Clearing the SWSMI_TMR_EN bit before the timer expires will reset the timer and the SMI# will not be generated. The default for this bit is 0.
5	0x0 RW	**APMC_EN (apmc_en):** APMC Enable - If set, this enables writes to the APM register to cause an SMI#
4	0x0 RW	**SMI On Sleep Enable (SMI_ON_SLP_EN): (smi_on_slp_en):** If this bit is set, the PMC will generate an SMI# when a write access attempts to set the SLP_EN bit (in the PM1_CNT register). Furthermore, the PMC will not put the system to a sleep state. This allows the SMI# handler work around chip-level bugs. It is expected that the SMI# handler will turn off the SMI_ON_SLP_EN bit before actually setting the SLP_EN bit.
3	0x0 RO	**reserved4:** Reserved.
2	0x0 RW	**BIOS Enable (BIOS_EN): (bios_en):** Enables the generation of SMI# when ACPI software writes a 1 to the GBL_RLS bit. Note that if the BIOS_STS bit, which gets set when software writes a 1 to GBL_RLS bit, is already a 1 at the time that BIOS_EN becomes 1, an SMI# will be generated when BIOS_EN gets set.
1	0x1 WO	**End of SMI (EOS): (eos):** SMI handler sets this bit when it finishes handling the SMI. Setting this bit will force the PMC internal SMI request to zero for 1 clock.Thus if the internal SMI request is still asserted due to new SMI trigger a new rising edge will happen, setting the interrupt to the PMC controller.
0	0x0 RW	**Global SMI Enable (GBL_SMI_EN): (gbl_smi_en):** When set, this bit enables the generation of SMIs in the system upon any enabled SMI event. This bit is reset by a PMU_PLTRST_B reset event. If this bit is not set, no SMI# will be generated. NOTE: When the SMI_LOCK bit is set, this bit cannot be changed.

10.17.7 SMI_STS - SMI Status Register (SMI_STS)—Offset 34h

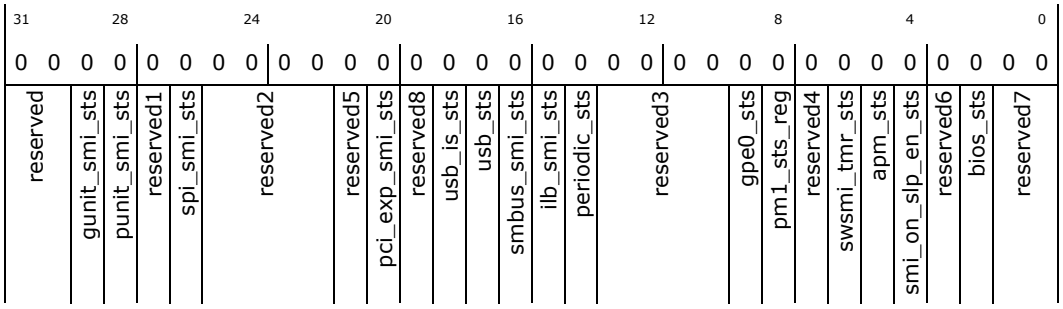
SMI Status Register

Access Method

Type: I/O Register (Size: 32 bits)

Offset: [ACPI_BASE_ADDRESS] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**reserved:** Reserved.
29	0x0 RW/1C	**GUNIT SMI Status (GUNIT_SMI_STS): (gunit_smi_sts):** This bit will be set if Graphics unit is requesting an SMI#. Writing a '1' to this bit position clears this bit to '0'
28	0x0 RW/1C	**PUNIT SMI Status (PUNIT_SMI_STS): (punit_smi_sts):** This bit will be set if Power Management is requesting an SMI#. Writing a '1' to this bit position clears this bit to '0'
27	0x0 RO	**reserved (reserved1):** Reserved.
26	0x0 RO	**SPI_SMI Status (SPI_SMI_STS): (spi_smi_sts):** This bit will be set when the SPI logic is requesting an SMI#
25:22	0x0 RO	**reserved (reserved2):** Reserved.
21	0x0 RW/1C	**reserved (reserved5):** This bit is reserved for future use
20	0x0 RO	**PCI_EXP_SMI Status (PCI_EXP_SMI_STS): (pci_exp_smi_sts):** 1-PCI Express SMI event occurred. This could be due to a PCI Express PME event.
19	0x0 RO	**reserved (reserved8):** Reserved.
18	0x0 RO	**Intel USB2 Status (USB_IS_STS): (usb_is_sts):** This non-sticky read-only bit is a logical OR of each of the SMI status bits in the Intel-Specific USB2 SMI Status Register ANDed with the corresponding enable bits. Additionally, the Port Disable Write Enable SMI is reported in this bit; the specific status bit for this event is contained in the USB Per-Port Registers Write Control Register in this I/O space. This bit will not be active if the enable bits are not set. Writes to this bit will have no effect. All integrated USB2 Host Controllers are represented with this bit.
17	0x0 RO	**USB Status (USB_STS): (usb_sts):** This bit will be set when the USB logic is requesting an SMI#
16	0x0 RO	**SMBUS_SMI Status (SMBUS_SMI_STS): (smbus_smi_sts):** This bit will be set when the SMBUS logic is requesting an SMI#
15	0x0 RO	**ILB_SMI Status (ILB_SMI_STS): (ilb_smi_sts):** This bit will be set when the ILB logic is requesting an SMI#

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW/1C	**Periodic Status (PERIODIC_STS): (periodic_sts):** This bit will be set at the rate determined by the PER_SMI_SEL bits. If the PERIODIC_EN bit is also set, the PMC will generate an SMI#. This bit is cleared by writing a 1 to this bit position.
13:10	0x0 RO	**reserved (reserved3):** Reserved.
9	0x0 RO	**GPE0a Status (GPE0a_STS): (gpe0_sts):** There are several status/ enable bit pairs in GPE0a_STS/EN that are capable of triggering SMI. This bit is a logical OR of all of those pairs (i.e. this bit is asserted whenever at least one of those pairs has both the status and enable bit asserted). This bit is NOT sticky. Writes to this bit will have no effect. Note: The setting of this bit does not cause the SMI#.
8	0x0 RO	**PM1 Status Register (PM1_STS_REG): (pm1_sts_reg):** This is an OR of the bits (except for bits 5 and 4) in the ACPI PM1_STS_EN Status Reg. Not sticky. Writes to this bit have no effect. Note: The setting of this bit does not cause the SMI#.
7	0x0 RO	**reserved (reserved4):** Reserved.
6	0x0 RW/1C	**Software SMI Timer Status (SWSMI_TMR_STS): (swsmi_tmr_sts):** This bit will be set to 1 by the hardware when the Software SMI# Timer expires. This bit will remain 1 until the software writes a 1 to this bit.
5	0x0 RW/1C	**APM_STS (apm_sts):** APM Status - SMI# was generated by a write access to the APM control register and if the APMC_EN bit is set. This bit is cleared by writing a one to its bit position.
4	0x0 RW/1C	**SMI_ON_SLP_EN Status (SMI_ON_SLP_EN_STS): (smi_on_slp_en_sts):** This bit will be set by the PMC when a write access attempts to set the SLP_EN bit. This bit is cleared by writing a 1 to this bit position
3	0x0 RO	**reserved (reserved6):** Reserved.
2	0x0 RW/1C	**BIOS Status (BIOS_STS): (bios_sts):** This bit gets set by hardware when a 1 is written by software to the GBL_RLS bit. When both BIOS_EN and the BIOS_STS bit are set, an SMI# will be generated. The BIOS_STS bit is cleared when software writes a 1 to this bit position.
1:0	0x0 RO	**reserved (reserved7):** Reserved.

10.17.8 ALT_GPIO_SMI - Alternate GPIO SMI Status and Enable Register. (ALT_GPIO_SMI)—Offset 38h

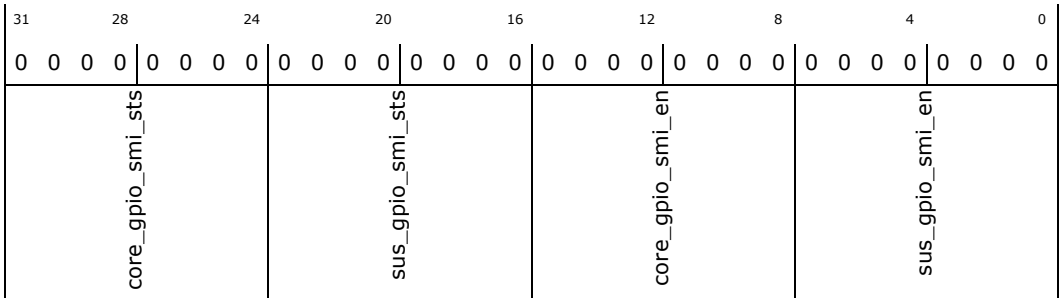
reset_type=Resume Well Reset#

Access Method

Type: I/O Register (Size: 32 bits)

Offset: [ACPI_BASE_ADDRESS] + 38h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW/1C	**CORE GPIO SMI Status Setting (CORE_GPIO_SMI_STS): (core_gpio_smi_sts):** These bits report the status of the corresponding GPIO's. 1 = active, -0 = inactive. These bits are sticky. If the following conditions are true, then an SMI# will be generated: 1. The corresponding enable bit in this register is set 2. The corresponding GPIO must be routed in the GPIO_ROUT register to cause an SMI. 3. The corresponding GPIO must be implemented. Core GPIO pins are: PCIE_CLKREQ0B (GPIO SW 3) PCIE_CLKREQ1B (GPIO SW 4) PCIE_CLKREQ2B (GPIO SW 5) PCIE_CLKREQ3B (GPIO SW 6) PCIE_CLKREQ4B (GPIO SW 7) All bits are in the resume well. Default for these bits are dependent on the state of the GPIO pins.
23:16	0x0 RW/1C	**SUS GPIO SMI Status Setting (SUS_GPIO_SMI_STS): (sus_gpio_smi_sts):** These bits report the status of the corresponding GPIO's. 1 = active, -0 = inactive. These bits are sticky. If the following conditions are true, then an SMI# will be generated: 1. The corresponding enable bit in this register is set 2. The corresponding GPIO must be routed in the GPIO_ROUT register to cause an SMI. 3. The corresponding GPIO must be implemented. Sus GPIO pins are GPIO_NORTH0-7. All bits are in the resume well. Default for these bits are dependent on the state of the GPIO pins.
15:8	0x0 RW	**CORE GPIO SMI Enable Setting (CORE_GPIO_SMI_EN): (core_gpio_smi_en):** These bits are used to enable the corresponding SOUTHWEST GPIO to cause an SMI#.
7:0	0x0 RW	**SUS GPIO SMI Enable Setting (SUS_GPIO_SMI_EN): (sus_gpio_smi_en):** These bits are used to enable the corresponding NORTH GPIO to cause an SMI#.

10.17.9 UPRWC - USB Per-Port Registers Write Control (UPRWC)—Offset 3Ch

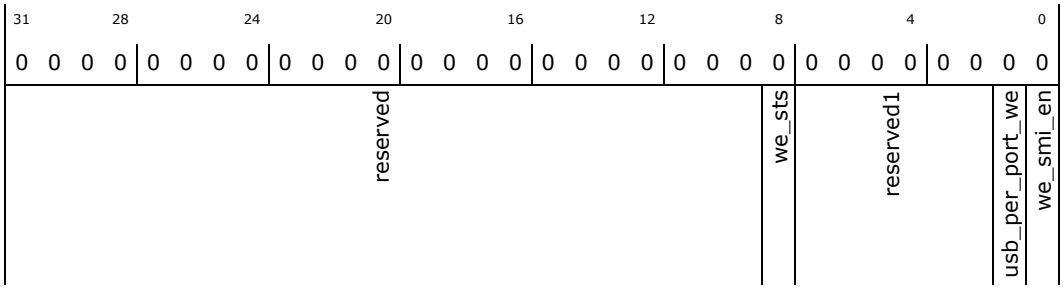
USB Per-Port Registers Write Control

Access Method

Type: I/O Register (Size: 32 bits)

Offset: [ACPI_BASE_ADDRESS] + 3Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**reserved:** Reserved.
8	0x0 RW/1C	**Write Enable Status (WE_STS) (we_sts):** This bit gets set by hardware when the Per-Port Registers Write Enable bit is written from 0 to 1. This bit is cleared by software writing a 1b to this bit location. The setting condition takes precedence over the clearing condition in the event that both occur at once. When this bit is 1b and bit 0 is 1b, the INTEL_USB2_STS bit is set in the SMI_STS register.
7:2	0x0 RO	**reserved (reserved1):** Reserved.
1	0x0 RW	**USB Per-Port Registers Write Enable (USB_PER_PORT_WE) (usb_per_port_we):** This bit controls whether writes are enabled to the USB Port Power Off and Port Disable Override registers
0	0x0 RW	**Write Enable SMI Enable (WE_SMI_EN) (we_smi_en):** This bit enables the generation of SMI when the Per-Port Registers Write Enable (bit 1) is written from 0 to 1. Once written to 1b, this bit can not be cleared by software.

10.17.10 GPE_CTRL - General Purpose Event Control (GPE_CTRL)—Offset 40h

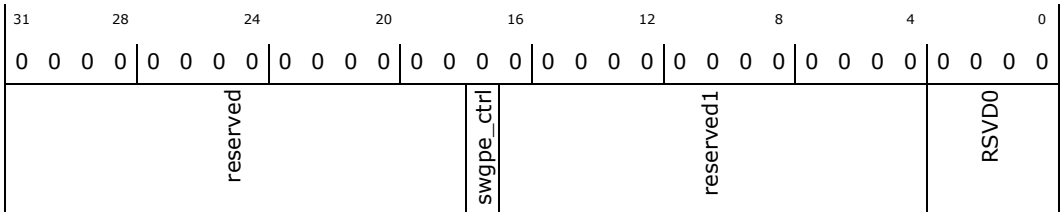
General Purpose Event Control

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [ACPI_BASE_ADDRESS] + 40h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0x0 RO	**reserved:** Reserved.
17	0x0 RW	**Software GPE Control (SWGPE_CTRL) (swgpe_ctrl):** This bit allows software to control the assertion of SWGPE_STS bit. This bit is used by hardware as the level input signal for the SWGPE_STS bit in the GPE0a_STS register. When SWGPE_CTRL is 1, SWGPE_STS will be set to 1, and writes to SWGPE_STS with a value of 1 to clear SWGPE_STS will result in SWGPE_STS being set back to 1 by hardware. When SWGPE_CTRL is 0, writes to SWGPE_STS with a value of 1 will clear SWGPE_STS to 0. In addition to being reset by RSMRST_B assertion, the PMC also clears this bit due to certain events: - Power button override - CPU thermal trip
16:4	0x0 RO	**reserved1:** Reserved.
3:0	0x0 RO	**RSVD0:** Reserved

10.17.11 PM2A_CNT_BLK - PM2a Control Block (PM2A_CNT_BLK)—Offset 50h

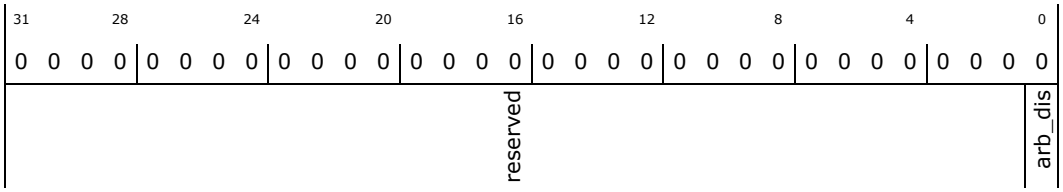
Power Management Control Block - 2a

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [ACPI_BASE_ADDRESS] + 50h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**reserved:** Reserved.
0	0x0 RW	**ARB_DIS (ARB_DIS) (arb_dis):** This bit is essentially just a scratchpad bit for legacy software compatibility.

10.17.12 TCO_RLD: TCO Reload Register (TCO_RLD)—Offset 60h

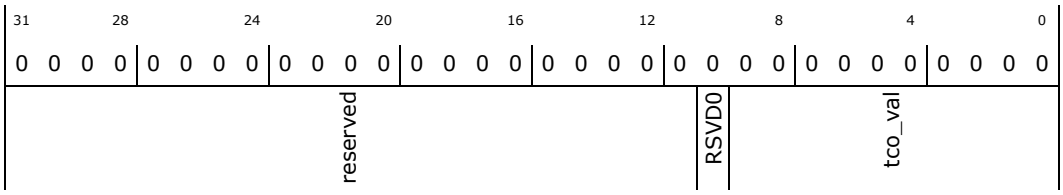
TCO Timer Reload Register

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [ACPI_BASE_ADDRESS] + 60h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:11	0x0 RO	**reserved:** Reserved.
10	0x0 RO	**RSVD0:** Reserved
9:0	0x0 RO	**TCO Timer Value (TCO_TVAL) (tco_val):** Reading this register will return the current count of the TCO timer. Writing any value to this register will reload the timer to prevent the timeout.

10.17.13 TCO_STS: TCO Timer Status (TCO_STS)—Offset 64h

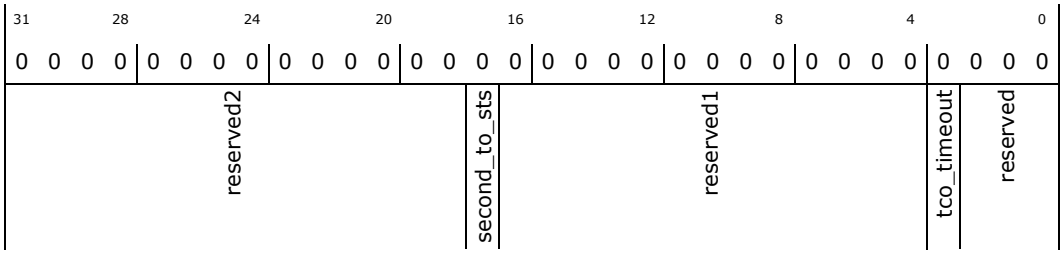
TCO Timer Status Register

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [ACPI_BASE_ADDRESS] + 64h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0x0 RO	**reserved (reserved2):** Reserved.
17	0x0 RW/1C	**Second Timeout Status(SECOND_TO_STS) (second_to_sts):** PMC sets this bit to 1 to indicate that the TIMEOUT bit had been (or is currently) set and a second timeout occurred before the TCO_RLD register was written. If this bit is set and the NO_REBOOT config bit is 0, then the PMC will reboot the system after the second timeout. The reboot is done by asserting PMU_PLTRST_B. This bit is only cleared by writing a 1 to this bit or by a RSMRST_B.
16:4	0x0 RO	**reserved (reserved1):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RW/1C	**TCO Timeout (TCO_TIMEOUT) (tco_timeout):** Bit set to 1 by PMC to indicate that the SMI was caused by TCO timer reaching 0.
2:0	0x0 RO	**reserved:** Reserved.

10.17.14 TCO1_CNT: TCO Timer Control (TCO1_CNT)—Offset 68h

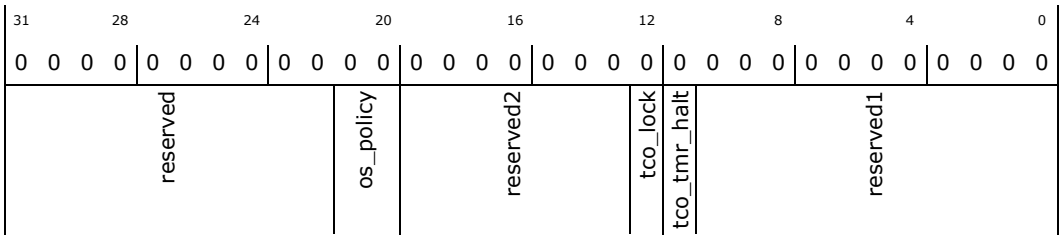
TCO1 Timer Control Register

Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [ACPI_BASE_ADDRESS] + 68h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**reserved:** Reserved.
21:20	0x0 RW	**OS_POLICY (os_policy):** OS-based software writes to these bits to select the policy that the BIOS will use after the platform resets due the WDT. The following convention is recommended for the BIOS and OS: 00 Boot normally 01 Shut down 10 Dont load OS. Hold in pre-boot state and use LAN to determine next step 11 Reserved
19:13	0x0 RO	**reserved (reserved2):** Reserved.
12	0x0 RW	**TCO Lock (TCO_LOCK) (tco_lock):** When set to 1, this bit prevents writes from changing the TCO_EN bit (in offset 30h of Power Management I/O space). Once this bit is set to 1, it can not be cleared by software writing a 0 to this bit location. A core-well reset is required to change this bit from 1 to 0. This bit defaults to 0.
11	0x0 RW	**TCO Timer Halt (TCO_TMR_HALT) (tco_tmr_halt):** 1 = The TCO timer will halt. It will not count, and thus cannot reach a value that would cause an SMI# or to cause the SECOND_TO_STS bit to be set. This will also prevent rebooting. 0 = The TCO timer is enabled to count. This is the default.
10:0	0x0 RO	**reserved1:** Reserved.

10.17.15 TCO_TMR: TCO Timer Register (TCO_TMR)—Offset 70h

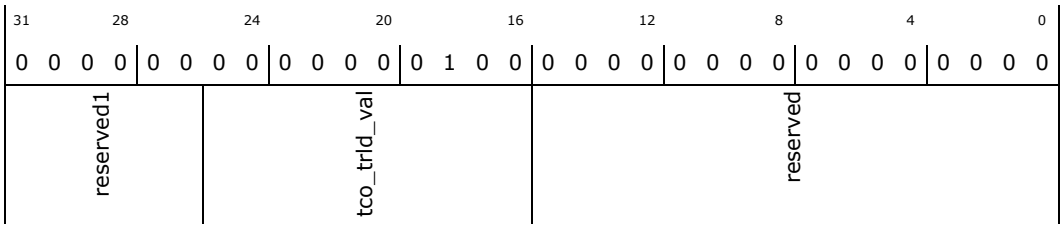
TCO Timer Register

Access Method

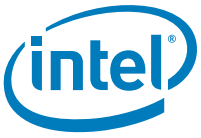
Type: I/O Register
(Size: 32 bits)

Offset: [ACPI_BASE_ADDRESS] + 70h

Default: 00040000h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0x0 RO	**reserved (reserved1):** Reserved.
25:16	0x4 RW	**TCO Timer reload value (TCO_TRLD_VAL) (tco_trld_val):** Value that is loaded into the timer each time the TCO_RLD register is written. Values of 0000h or 0001h will be ignored and should not be attempted. The timer is clocked at approximately 0.6 seconds, and thus allows timeouts ranging from 1.2 second to 613.8 seconds. Note: The timer has an error of +/- 1 tick (0.6s). The TCO Timer will only count down in the S0 state.
15:0	0x0 RO	**reserved:** Reserved.



10.18 PCU—iLB APIC Memory Mapped I/O Registers

Table 113. Summary of PCU—iLB APIC Memory Mapped I/O Registers—

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
FEC00000–FEC00000h	1	"IDX (IOAPIC_IDX)—Offset FEC00000h" on page 5839	00h
FEC00010–FEC00013h	4	"WDW (IOAPIC_WDW)—Offset FEC00010h" on page 5839	00000000h
FEC00040–FEC00043h	4	"EOI (IOAPIC_EOI)—Offset FEC00040h" on page 5839	00000000h

10.18.1 IDX (IOAPIC_IDX)—Offset FEC00000h

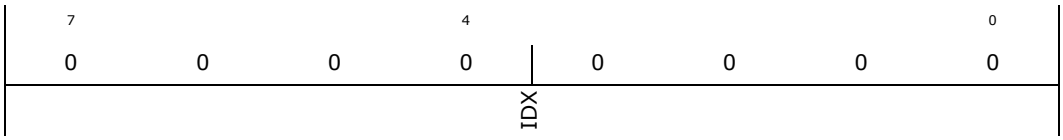
Index Register

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

Offset: FEC00000h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**IDX:** This 8-bit register selects which indirect register appears in the window register to be manipulated by software. Software will program this register to select the desired APIC internal register.

10.18.2 WDW (IOAPIC_WDW)—Offset FEC00010h

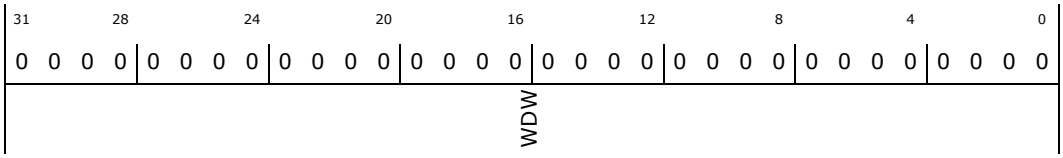
Window Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: FEC00010h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**WDW:** This 32-bit register specifies the data to be read or written to the register pointed to by the IDX register. This register can be accessed only in DW quantities.

10.18.3 EOI (IOAPIC_EOI)—Offset FEC00040h

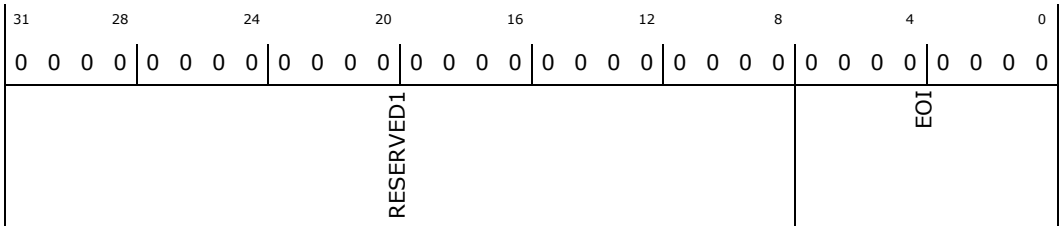
EOI Register

Access Method

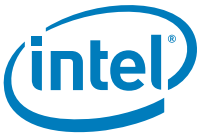
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: FEC00040h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 WO	**RESERVED (RESERVED1):** Reserved.
7:0	0x0 WO	**EOI:** When a write is issued to this register, the IOxAPIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, RTE.RIRR for that entry will be cleared. If multiple entries have the same vector, each of those entries will have RTE.RIRR cleared.



10.19 PCU—iLB 8259 Interrupt Controller (PIC) Memory Mapped I/O Registers

Table 114. Summary of PCU—iLB 8259 Interrupt Controller (PIC) Memory Mapped I/O Registers—

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
20–20h	1	"MICW1—Offset 20h" on page 5843	00h
21–23h	3	"MICW2—Offset 21h" on page 5843	00h
24–24h	1	"MOCW2—Offset 24h" on page 5844	20h
25–27h	3	"MICW3—Offset 25h" on page 5845	00h
28–28h	1	"MOCW3—Offset 28h" on page 5845	22h
29–29h	1	"MICW4—Offset 29h" on page 5846	01h
2D–2Dh	1	"MOCW1—Offset 2Dh" on page 5847	00h
A0–A0h	1	"SICW1—Offset A0h" on page 5847	00h
A1–A3h	3	"SICW2—Offset A1h" on page 5848	00h
A4–A4h	1	"SOCW2—Offset A4h" on page 5849	20h
A5–A7h	3	"SICW3—Offset A5h" on page 5850	00h
A8–A8h	1	"SOCW3—Offset A8h" on page 5850	22h
A9–A9h	1	"SICW4—Offset A9h" on page 5851	01h
AD–ADh	1	"SOCW1—Offset ADh" on page 5852	00h
4D0–4D0h	1	"ELCR1—Offset 4D0h" on page 5852	00h
4D1–4D1h	1	"ELCR2—Offset 4D1h" on page 5853	00h

10.19.1 MICW1—Offset 20h

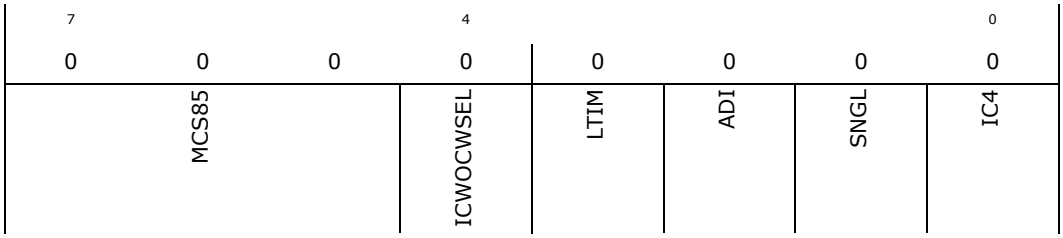
Master Initialization Command Word 1.A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs: * The Interrupt Mask register is cleared. * IRQ7 input is assigned priority 7. * The slave mode address is set to 7. * Special Mask Mode is cleared and Status Read is set to IRR. Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 20h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:5	X WO	**MCS85:** These bits are MCS-85 specific, and not needed. Should be programmed to 000
4	X WO	**ICWOCWSEL:** ICW/OCW select: This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	X WO	**LTIM:** Edge/Level Bank Select (LTIM): Disabled. Replaced by ELCR1 and ELCR2.
2	X WO	**ADI:** ADI. Should be programmed to 0.
1	X WO	**SNGL:** Single or Cascade (SNGL): Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	X WO	**IC4:** wICW4 Write Required (IC4): This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

10.19.2 MICW2—Offset 21h

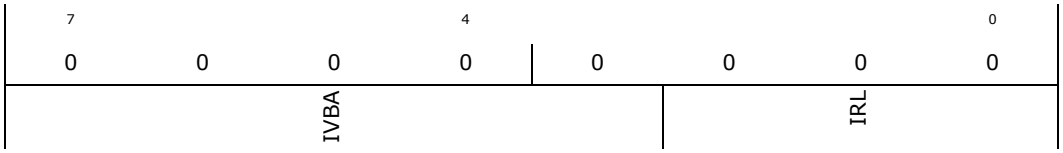
Master ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 21h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:3	X WO	**IVBA:** Interrupt Vector Base Address: Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.
2:0	X WO	**IRL:** Interrupt Request Level: When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Master Interrupt Slave Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

10.19.3 MOCW2—Offset 24h

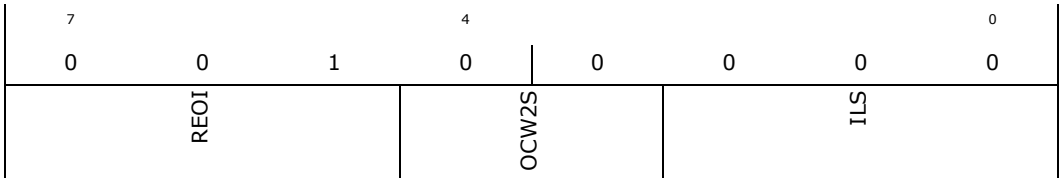
Master Operational Control Word 2 (Interrupt Mask).Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 24h

Default: 20h



Bit Range	Default & Access	Field Name (ID): Description
7:5	0x1 WO	**REOI:** Rotate and EOI Codes: R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 - Rotate in Auto EOI Mode (Clear) 001 - Non-specific EOI command 010 - No Operation 011 - *Specific EOI Command 100 - Rotate in Auto EOI Mode (Set) 101 - Rotate on Non-Specific EOI Command 110 - *Set Priority Command 111 - *Rotate on Specific EOI Command *L0 - L2 Are Used
4:3	X WO	**OCW2S:** OCW2 Select: When selecting OCW2, bits 4:3 = 00

Bit Range	Default & Access	Field Name (ID): Description
2:0	X WO	**ILS:** Interrupt Level Select (L2, L1, L0): L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function; programming L2, L1 and L0 to 0 is sufficient in this case. Bits Interrupt Level Bits Interrupt Level 000 IRQ0/8 100 IRQ4/12 001 IRQ1/9 101 IRQ5/13 010 IRQ2/10 110 IRQ6/14 011 IRQ3/11 111 IRQ7/15

10.19.4 MICW3—Offset 25h

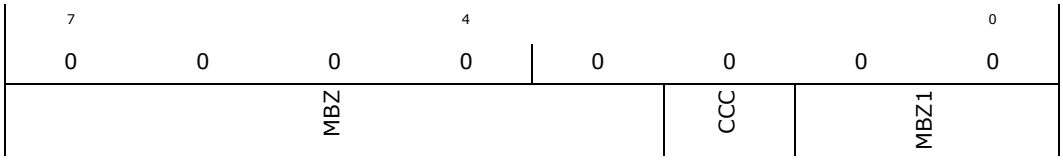
Master Initialization Command Word 3

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 25h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:3	X WO	**MBZ:** These bits must be programmed to zero.
2	X WO	**CCC:** Cascaded Controller Connection (CCC): This bit must always be programmed to a 1 to indicate the slave controller for interrupts 8 15 is cascaded on IRQ2.
1:0	X WO	**MBZ (MBZ1):** These bits must be programmed to zero.

10.19.5 MOCW3—Offset 28h

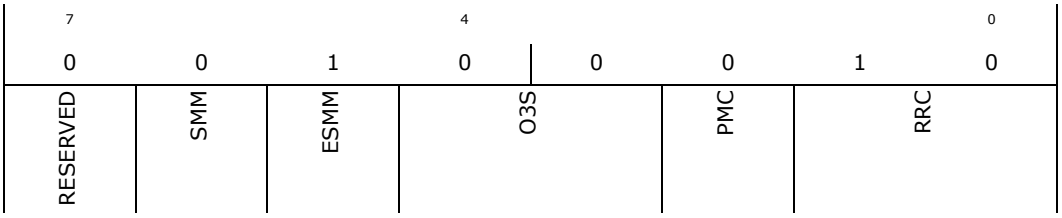
Master Operational Control Word 3

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 28h

Default: 22h



Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**RESERVED:** Reserved. Must be 0.
6	0x0 WO	**SMM:** Special Mask Mode (SMM): If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.
5	0x1 WO	**ESMM:** Enable Special Mask Mode (ESMM): When set, the SMM bit is enabled to set or reset the Special Mask Mode. When cleared, the SMM bit becomes a don't care.
4:3	X WO	**O3S:** OCW3 Select (O3S): When selecting OCW3, bits 4:3 = 01
2	X WO	**PMC:** Poll Mode Command (PMC): When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	0x2 WO	**RRC:** Register Read Command (RRC): These bits provide control for reading the ISR and Interrupt IRR. When bit 1=0, bit 0 will not affect the register read selection. Following ICW initialization, the default OCW3 port address read will be read IRR. To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

10.19.6 MICW4—Offset 29h

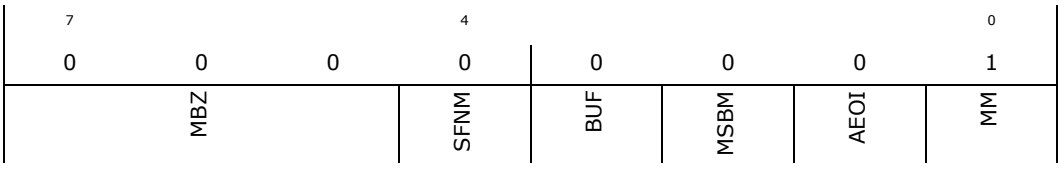
Master Initialization Command Word 4

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 29h

Default: 01h



Bit Range	Default & Access	Field Name (ID): Description
7:5	X WO	**MBZ:** These bits must be programmed to zero.
4	0x0 WO	**SFNM:** Special Fully Nested Mode (SFNM): Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
3	0x0 WO	**BUF:** Buffered Mode (BUF): Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.
2	0x0 WO	**MSBM:** Master/Slave in Buffered Mode (MSBM): Not used. Should always be programmed to 0.
1	0x0 WO	**AEOI:** Automatic End of Interrupt (AEOI): This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed.
0	0x1 WO	**MM:** Microprocessor Mode (MM): This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.

10.19.7 MOCW1—Offset 2Dh

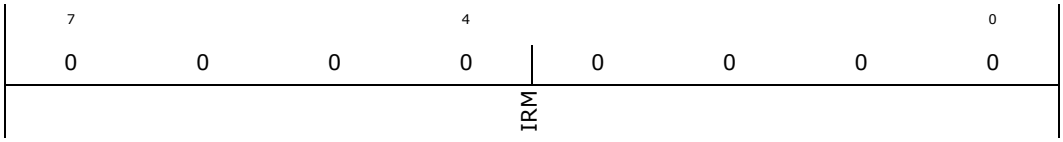
Master Operational Control Word 1 (Interrupt Mask)

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 2Dh

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**IRM:** Interrupt Request Mask (IRM): When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

10.19.8 SICW1—Offset A0h

Slave Initialization Command Word 1.A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs: * The Interrupt Mask register is cleared. * IRQ7 input is assigned priority 7. * The slave mode address is set to 7. * Special Mask Mode is cleared and Status Read is set to IRR. Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: A0h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
MCS85			ICWOCWSEL	LTIM	ADI	SNGL	IC4

Bit Range	Default & Access	Field Name (ID): Description
7:5	X WO	**MCS85:** These bits are MCS-85 specific, and not needed. Should be programmed to 000
4	X WO	**ICWOCWSEL:** ICW/OCW select: This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	X WO	**LTIM:** Edge/Level Bank Select (LTIM): Disabled. Replaced by ELCR1 and ELCR2.
2	X WO	**ADI:** ADI. Should be programmed to 0.
1	X WO	**SNGL:** Single or Cascade (SNGL): Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	X WO	**IC4:** wICW4 Write Required (IC4): This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

10.19.9 SICW2—Offset A1h

Slave ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: A1h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
IVBA				IRL			

Bit Range	Default & Access	Field Name (ID): Description
7:3	X WO	**IVBA:** Interrupt Vector Base Address: Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.
2:0	X WO	**IRL:** Interrupt Request Level: When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Master Interrupt Slave Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

10.19.10 SOCW2—Offset A4h

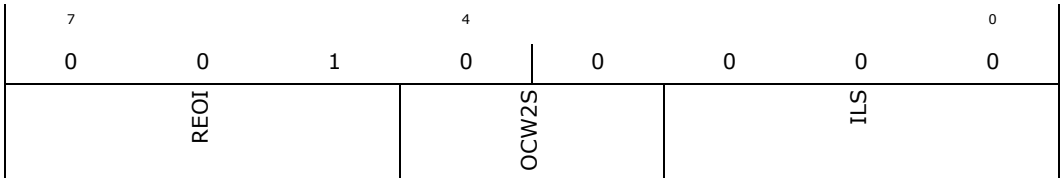
Slave Operational Control Word 2 (Interrupt Mask).Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: A4h

Default: 20h



Bit Range	Default & Access	Field Name (ID): Description
7:5	0x1 WO	**REOI:** Rotate and EOI Codes: R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 - Rotate in Auto EOI Mode (Clear) 001 - Non-specific EOI command 010 - No Operation 011 - *Specific EOI Command 100 - Rotate in Auto EOI Mode (Set) 101 - Rotate on Non-Specific EOI Command 110 - *Set Priority Command 111 - *Rotate on Specific EOI Command *L0 - L2 Are Used
4:3	X WO	**OCW2S:** OCW2 Select: When selecting OCW2, bits 4:3 = 00
2:0	X WO	**ILS:** Interrupt Level Select (L2, L1, L0): L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function; programming L2, L1 and L0 to 0 is sufficient in this case. Bits Interrupt Level Bits Interrupt Level 000 IRQ0/8 100 IRQ4/12 001 IRQ1/9 101 IRQ5/13 010 IRQ2/10 110 IRQ6/14 011 IRQ3/11 111 IRQ7/15

10.19.11 SICW3—Offset A5h

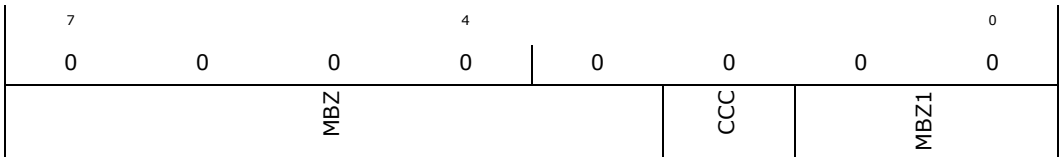
Slave Initialization Command Word 3

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: A5h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:3	X WO	**MBZ:** These bits must be programmed to zero.
2	X WO	**CCC:** Cascaded Controller Connection (CCC): This bit must always be programmed to a 1 to indicate the slave controller for interrupts 8 15 is cascaded on IRQ2.
1:0	X WO	**MBZ (MBZ1):** These bits must be programmed to zero.

10.19.12 SOCW3—Offset A8h

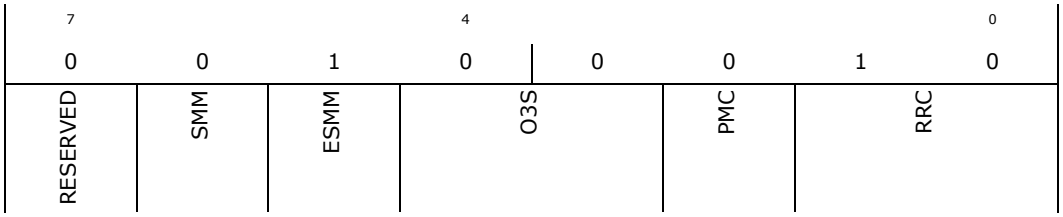
Slave Operational Control Word 3

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: A8h

Default: 22h



Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RO	**RESERVED:** Reserved. Must be 0.
6	0x0 WO	**SMM:** Special Mask Mode (SMM): If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.

Bit Range	Default & Access	Field Name (ID): Description
5	0x1 WO	**ESMM:** Enable Special Mask Mode (ESMM): When set, the SMM bit is enabled to set or reset the Special Mask Mode. When cleared, the SMM bit becomes a don't care.
4:3	X WO	**O3S:** OCW3 Select (O3S): When selecting OCW3, bits 4:3 = 01
2	X WO	**PMC:** Poll Mode Command (PMC): When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	0x2 WO	**RRC:** Register Read Command (RRC): These bits provide control for reading the ISR and Interrupt IRR. When bit 1=0, bit 0 will not affect the register read selection. Following ICW initialization, the default OCW3 port address read will be read IRR. To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

10.19.13 SICW4—Offset A9h

Slave Initialization Command Word 4

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: A9h

Default: 01h

7			4				0
0	0	0	0	0	0	0	1
MBZ			SFNM	BUF	MSBM	AEOI	MM

Bit Range	Default & Access	Field Name (ID): Description
7:5	X WO	**MBZ:** These bits must be programmed to zero.
4	0x0 WO	**SFNM:** Special Fully Nested Mode (SFNM): Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
3	0x0 WO	**BUF:** Buffered Mode (BUF): Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.
2	0x0 WO	**MSBM:** Master/Slave in Buffered Mode (MSBM): Not used. Should always be programmed to 0.
1	0x0 WO	**AEOI:** Automatic End of Interrupt (AEOI): This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed.

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 WO	**MM:** Microprocessor Mode (MM): This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.

10.19.14 SOCW1—Offset ADh

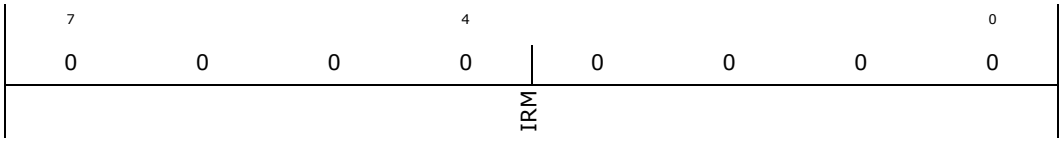
Slave Operational Control Word 1 (Interrupt Mask)

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: ADh

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**IRM:** Interrupt Request Mask (IRM): When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

10.19.15 ELCR1—Offset 4D0h

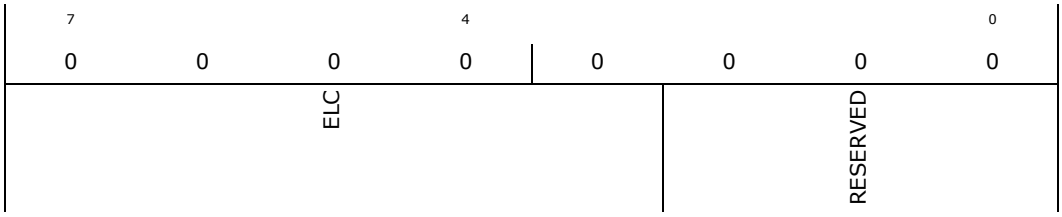
Master Edge/Level Control

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 4D0h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:3	X RW	**ELC:** Edge Level Control (ECL[7:3]): In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level.
2:0	0x0 RO	**RESERVED:** Reserved.

10.19.16 ELCR2—Offset 4D1h

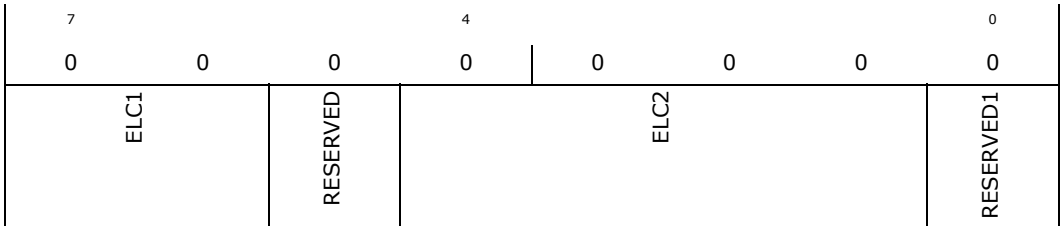
Slave Edge/Level Control

Access Method

Type: I/O Register
(Size: 8 bits)

Offset: 4D1h

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:6	X RW	**ELC1:** Edge Level Control (ECL[15:14]): In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 7 applies to IRQ15, and bit 6 to IRQ14.
5	0x0 RO	**RESERVED:** Reserved.
4:1	X RW	**ELC2:** Edge Level Control (ECL[12:9]: In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 4 applies to IRQ12, bit 3 to IRQ11, bit 2 to IRQ10, and bit 1 to IRQ9.
0	0x0 RO	**RESERVED (RESERVED1):** Reserved.

10.20 PCU—iLB Low Pin Count (LPC) Bridge PCI Configuration Registers

Table 115. Summary of PCI Configuration Registers—0/31/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Identifiers Register (PCIE_REG_Identifiers)—Offset 0h" on page 5855	00008086h
4–5h	2	"Command (PCIE_REG_COMMAND)—Offset 4h" on page 5855	0007h
6–7h	2	"Status (PCIE_REG_STATUS)—Offset 6h" on page 5856	0210h
8–Bh	4	"Revision ID and Class Code (PCIE_REG_REVISION_ID_CLASS_CODE)—Offset 8h" on page 5858	06010000h
D–Dh	1	"Master Latency Timer (PCIE_REG_MASTER_LAT_TIMER)—Offset Dh" on page 5859	00h
E–Eh	1	"Header Type (PCIE_REG_HEADER_TYPE)—Offset Eh" on page 5859	80h
2C–2Fh	4	"Subsystem ID and Vendor ID (PCIE_REG_SUBSYS_VENDOR_ID)—Offset 2Ch" on page 5860	00000000h
34–37h	4	"Capability List Pointer (PCIE_REG_CAP_POINTER)—Offset 34h" on page 5861	000000E0h
40–43h	4	"ABASE (ACPI_BASE_ADDRESS)—Offset 40h" on page 5861	00000001h
44–47h	4	"PBASE (PMC_BASE_ADDRESS)—Offset 44h" on page 5862	00000000h
4C–4Fh	4	"IOBASE (IO_CONTROLLER_BASE_ADDRESS)—Offset 4Ch" on page 5863	00000000h
50–53h	4	"IBASE (ILB_BASE_ADDRESS)—Offset 50h" on page 5863	00000000h
54–57h	4	"SBASE (SPI_BASE_ADDRESS)—Offset 54h" on page 5864	00000000h
58–5Bh	4	"MPBASE (MPHY_BASE_ADDRESS)—Offset 58h" on page 5865	00000000h
5C–5Fh	4	"PUBASE (PUNIT_BASE_ADDRESS)—Offset 5Ch" on page 5866	00000000h
80–83h	4	"UART Control (UART_CONT)—Offset 80h" on page 5867	00000000h
D8–D9h	2	"BIOS Decode Enable (PCIE_REG_BIOS_DECODE_EN)—Offset D8h" on page 5867	FFCFh
E0–E1h	2	"FDCAP (Feature_Detection_Capability_ID)—Offset E0h" on page 5869	0009h
E2–E2h	1	"FDLEN (Feature_Detection_Capability_Length)—Offset E2h" on page 5869	0Ch
E3–E3h	1	"FDVER (Feature_Detection_Version_Register)—Offset E3h" on page 5870	10h
E4–E7h	4	"FVECTIDX (Feature_Vector_Index)—Offset E4h" on page 5870	00000000h
E8–EBh	4	"FVECTD (Feature_Vector_Data)—Offset E8h" on page 5870	00000000h
F0–F3h	4	"RCBA (RCRB_BASE_ADDRESS)—Offset F0h" on page 5871	00000000h

10.20.1 Identifiers Register (PCIE_REG_Identifiers)—Offset 0h

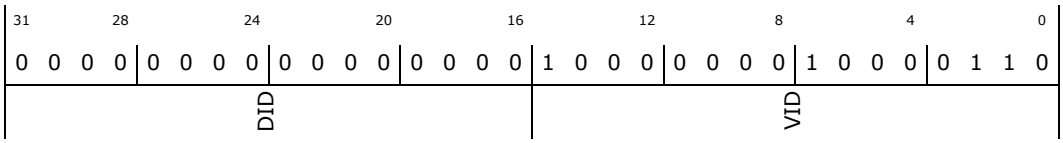
PCIE device/vendor ID register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:31, F:0] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	X RO	**Device Identification (DID):** This field identifies the particular device. This identifier is allocated by the vendor. This field is controlled by the LPC DID fuses Bits [31:23] are coming from the SETIDVALUE message Device ID[15:7] bits. Bits [22:21] are set constantly to 2'b00. Bits [20:16] are set constantly by pcu_did fuses.
15:0	0x8086 RO	**Vendor Identification (VID):** This field identifies the manufacturer of the device. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. 0 FFFFh is an invalid value for Vendor ID.

10.20.2 Command (PCIE_REG_COMMAND)—Offset 4h

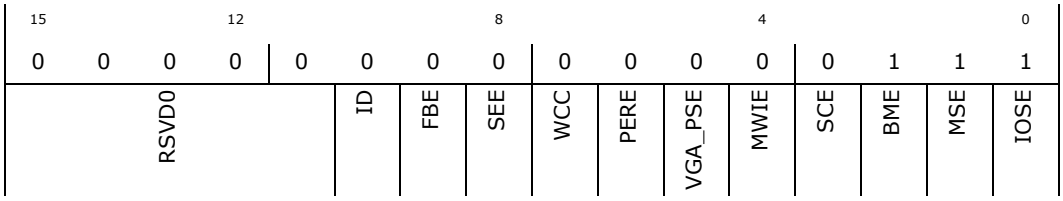
The Command register provides coarse control over a device's ability to generate and respond to PCI cycles. When a 0 is written to this register, the device is logically disconnected from the PCI bus for all accesses except configuration accesses. All devices are required to support this base level of functionality. Individual bits in the Command register may or may not be implemented depending on a device's functionality

Access Method

Type: PCI Configuration Register (Size: 16 bits)

Offset: [B:0, D:31, F:0] + 4h

Default: 0007h



Bit Range	Default & Access	Field Name (ID): Description
15:11	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
10	0x0 RO	**Interrupt Disable (ID):** This bit disables the device/function from asserting INTx#. A value of 0 enables the assertion of its INTx# signal. A value of 1 disables the assertion of its INTx# signal. The LPC bridge has no interrupts to disable
9	0x0 RO	**Fast Back to Back Enable (FBE):** This optional read/write bit controls whether or not a master can do fast back-to-back transactions to different devices. A value of 0 means fast back-to-back transactions are only allowed to the same agent
8	0x0 RW	**SERR# Enable (SEE):** This bit is an enable bit for the SERR# driver. A value of 0 disables the SERR# driver. A value of 1 enables the SERR# driver.
7	0x0 RO	**Wait Cycle Control (WCC):** Reserved as '0' per PCI-Express spec
6	0x0 RW	**Parity Error Response Enable (PERE):** This bit controls the device's response to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is 0, the device sets its Detected Parity Error status bit (bit 15 in the Status register) when an error is detected, but does not assert PERR# and continues normal operation.
4	0x0 RO	**Memory Write and Invalidate Enable (MWIE):** This is an enable bit for using the Memory Write and Invalidate command. When this bit is 1, masters may generate the command. When it is 0, Memory Write must be used instead. Reserved as '0' per PCI-Express spec
3	0x0 RO	**Special Cycle Enable (SCE):** Controls a device's action on Special Cycle operations. A value of 0 causes the device to ignore all Special Cycle operations. A value of 1 allows the device to monitor Special Cycle operations. Reserved as '0' per PCI-Express spec
2	0x1 RO	**Bus Master Enable (BME):** Controls a device's ability to act as a master on the PCI bus. A value of 0 disables the device from generating PCI accesses. A value of 1 allows the device to behave as a bus master. Bus master cannot be disabled on LPC
1	0x1 RO	**Memory Space Enable (MSE):** Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. Memory space cannot be disable on LPC
0	0x1 RO	**I/O Space Enable (IOSE):** Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. I/O space cannot be disable on LPC

10.20.3 Status (PCIE_REG_STATUS)—Offset 6h

The Status register is used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A one bit is reset (if it is not read-only) whenever the register is written, and the write data in the corresponding bit location is a 1. For instance, to clear bit 14 and not affect any other bits, write the value 0100_0000_0000_0000b to the register.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

Offset: [B:0, D:31, F:0] + 6h

Default: 0210h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0
DPE	SSE	RMA	RTA	STA	DTS		DPD	FBC	RSVD0	C66	CLIST	IS	RSVD1		

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RW	**Detected Parity Error (DPE):** This bit must be set by the device whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit 6 in the Command register).
14	0x0 RW	**Signaled System Error (SSE):** This bit must be set whenever the device asserts SERR#. Set when the LPC bridge signals a system error to the internal SERR# logic.
13	0x0 RW	**Received Master Abort (RMA):** This bit must be set by a master device whenever its transaction (except for Special Cycle) is terminated with Master-Abort. All master devices must implement this bit.
12	0x0 RW	**Received Target Abort: (RTA):** This bit must be set by a master device whenever its transaction is terminated with Target-Abort. All master devices must implement this bit.
11	0x0 RW	**Signaled Target Abort (STA):** This bit must be set by a target device whenever it terminates a transaction with Target-Abort. Devices that will never signal Target- Abort do not need to implement this bit.
10:9	0x1 RO	**DEVSEL# Timing Status (DTS):** These bits encode the timing of DEVSEL#. These are encoded as 00b for fast, 01b for medium, and 10b for slow (11b is reserved). These bits Indicate medium timing, although this has no meaning on the backbone
8	0x0 RW	**Data Parity Error Detected (DPD):** This bit is only implemented by bus masters. It is set when three conditions are met: 1) the bus agent asserted PERR# itself (on a read) or observed PERR# asserted (on a write); 2) the agent setting the bit acted as the bus master for the operation in which the error occurred; and 3) the Parity Error Response bit (Command register) is set.
7	0x0 RO	**Fast Back to Back Capable (FBC):** This optional read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. This bit can be set to 1 if the device can accept these transactions and must be set to 0 otherwise. This bit has no meaning on internal backbone.
6	0x0 RO	**RSVD0:** Reserved
5	0x0 RO	**66 MHz Capable (C66):** This optional read-only bit indicates whether or not this device is capable of running at 66 MHz. A value of zero indicates 33 MHz. A value of 1 indicates that the device is 66 MHz capable. This bit has no meaning on internal backbone

Bit Range	Default & Access	Field Name (ID): Description
4	0x1 RO	**Capabilities List (CLIST):** This optional read-only bit indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. A value of zero indicates that no New Capabilities linked list is available. A value of one indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities. There is a capabilities list in the LPC bridge.
3	0x0 RO	**Interrupt Status (IS):** This read-only bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. The LPC bridge does not generate interrupts
2:0	0x0 RO	**RSVD1:** Reserved

10.20.4 Revision ID and Class Code (PCIE_REG_REVISION_ID_CLASS_CODE)—Offset 8h

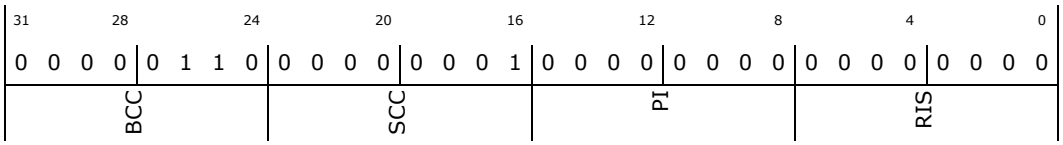
This register is a combination of two registers the Revision ID register and the Class Code register. The revision ID register specifies a device specific revision identifier. The value is chosen by the vendor. Zero is an acceptable value. The Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific registerlevel programming interface.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:31, F:0] + 8h

Default: 06010000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x6 RO	**Base Class Code (BCC):** This field is a base class code which broadly classifies the type of function the device performs. Indicates the device is a bridge device.
23:16	0x1 RO	**Sub-Class Code (SCC):** This field is a sub-class code which identifies more specifically the function of the device. Indicates the device a PCI to ISA bridge
15:8	0x0 RO	**Programming Interface (PI):** This field identifies a specific register-level programming interface if any) so that device independent software can interact with the device. The LPC bridge has no programming interface.

Bit Range	Default & Access	Field Name (ID): Description
7:0	X RO	**Revision ID (RIS):** This register specifies a device specific revision identifier. The value is chosen by the vendor. Zero is an acceptable value. This field should be viewed as a vendor defined extension to the Device ID. This field is controlled by the LPC RID fuses. Coming from the SETIDVALUE message Revision ID field

10.20.5 Master Latency Timer (PCIE_REG_MASTER_LAT_TIMER)—Offset Dh

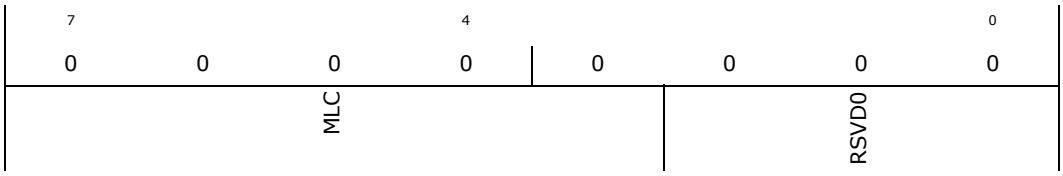
This register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. This register is implemented as read-only, the register must be initialized to 0.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:31, F:0] + Dh

Default: 00h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0x0 RO	**Master Latency Count (MLC):** Reserved per PCIe spec.
2:0	0x0 RO	**RSVD0:** Reserved

10.20.6 Header Type (PCIE_REG_HEADER_TYPE)—Offset Eh

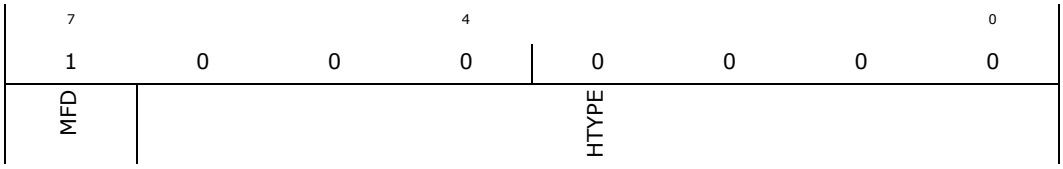
This byte identifies the layout of the second part of the predefined header (beginning at byte 10h in Configuration Space) and also whether or not the device contains multiple functions.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:31, F:0] + Eh

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7	0x1 RO	**Multi-function Device (MFD):** This field is used to identify a multi-function device. If the bit is 0, then the device is single function. If the bit is 1, then the device has multiple functions.
6:0	0x0 RO	**Header Type (HTYPE):** This field identifies the layout of the second part of the predefined header. The encoding 00h specifies the standard layout.

10.20.7 Subsystem ID and Vendor ID (PCIE_REG_SUBSYS_VENDOR_ID)—Offset 2Ch

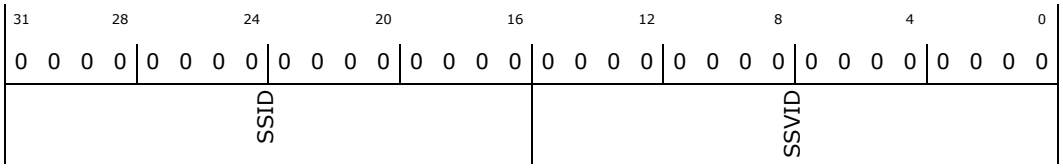
This register is used to uniquely identify the add-in card or subsystem where the PCI device resides. It provides a mechanism for add-in card vendors to distinguish their add- in cards from one another even though the add-in cards may have the same PCI controller on them (and, therefore, the same Vendor ID and Device ID).
Implementation of this register is required for all PCI devices except those that have a base class 6 with sub class 0-4 (0, 1, 2, 3, 4), or a base class 8 with sub class 0-3 (0, 1, 2, 3). Subsystem Vendor IDs can be obtained from the PCI SIG and are used to identify the vendor of the add-in card or subsystem. Values for the Subsystem ID are vendor specific. Values in these registers must be loaded and valid prior to the system firmware or any system software accessing the PCI Configuration Space. How these values are loaded is not specified but could be done during the manufacturing process or loaded from external logic (e.g., strapping options, serial ROMs, etc.). These values must not be loaded using expansion ROM software because expansion ROM software is not guaranteed to be run during POST in all systems. Devices are responsible for guaranteeing the data is valid before allowing reads to these registers to complete. This can be done by responding to any accesses with Retry until the data is valid. If a device is designed to be used exclusively on the system board, the system vendor may use system specific software to initialize these registers after each power-on. This register can be written only once after PMU_PLTRST_B de-assertion.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:31, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value. This field could be written only once.
15:0	0x0 RW	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value. This field could be written only once.

10.20.8 Capability List Pointer (PCIE_REG_CAP_POINTER)—Offset 34h

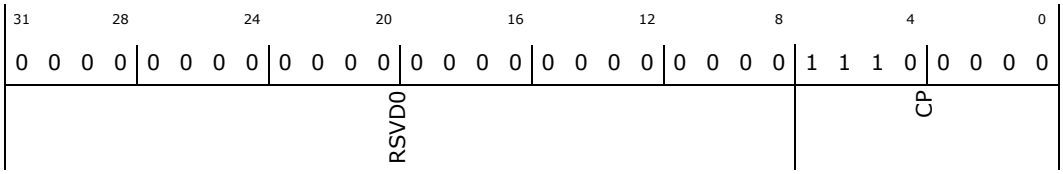
This optional register is used to point to a linked list of new capabilities implemented by this device. This register is only valid if the Capabilities List bit in the Status Register is set. If implemented, the bottom two bits are reserved and should be set to 00b. Software should mask these bits off before using this register as a pointer in Configuration Space to the first entry of a linked list of new capabilities.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:31, F:0] + 34h

Default: 000000E0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**RSVD0:** Reserved
7:0	0xe0 RO	**Capability Pointer (CP):** Indicates the offset of the first Capability Item.

10.20.9 ABASE (ACPI_BASE_ADDRESS)—Offset 40h

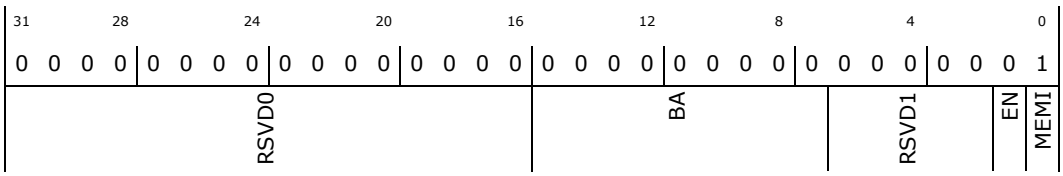
ACPI is mapped into I/O space. It is used by the PMC. Base Address registers that map into I/O Space are always 32 bits wide with bit 0 hardwired to a 1. Bit 1 is used to enable IO range pointed by this base address. Bits 31:16 are reserved and must return 0 on reads and the other bits could be used to map the device into I/O Space.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:31, F:0] + 40h

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:7	0x0 RW	**Base Address (BA):** Provides the 128 bytes of I/O space for ACPI and TCO logic
6:2	0x0 RO	**RSVD1:** Reserved
1	0x0 RW	**Enable (EN):** When set, decode of the IO range pointed to by the ABASE is enabled.
0	0x1 RO	**Memory Space Indication (MEMI):** This read-only bit always is 1, indicating that this BAR is IO mapped

10.20.10 PBASE (PMC_BASE_ADDRESS)—Offset 44h

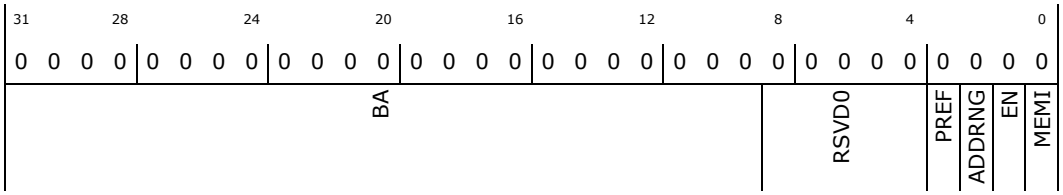
PMC registers are mapped into memory space. It is used by the PMC. Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RW	**Base Address (BA):** Provides 512 byte system memory base address for the PMC logic
8:4	0x0 RO	**RSVD0:** Reserved
3	0x0 RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0x0 RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0x0 RW	**Enable (EN):** When set, decode of the memory range pointed to by the PBASE is enabled.
0	0x0 RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

10.20.11 IOBASE (IO_CONTROLLER_BASE_ADDRESS)—Offset 4Ch

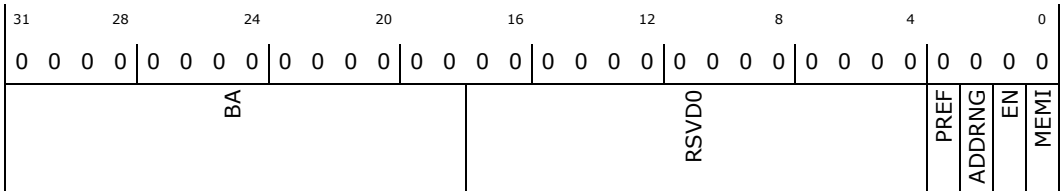
IO Controllers registers are mapped into memory space. It is used by the Proxy agent (to IO controllers). Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0x0 RW	**Base Address (BA):** Provides 8K byte system memory base address for the IO controllers logic
17:4	0x0 RO	**RSVD0:** Reserved
3	0x0 RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0x0 RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0x0 RW	**Enable (EN):** When set, decode of the memory range pointed to by the IOBASE is enabled.
0	0x0 RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

10.20.12 IBASE (ILB_BASE_ADDRESS)—Offset 50h

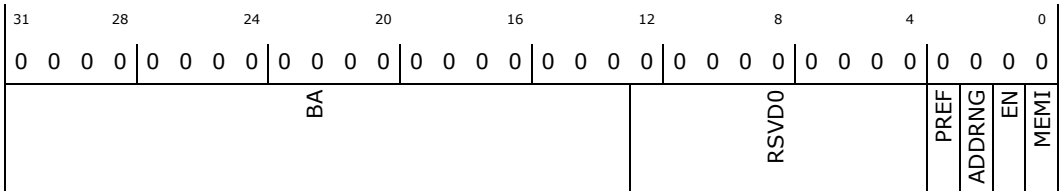
iLB registers are mapped into memory space. It is used by the iLB. Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:31, F:0] + 50h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0x0 RW	**Base Address (BA):** Provides 8K byte system memory base address for the iLB logic
12:4	0x0 RO	**RSVD0:** Reserved
3	0x0 RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0x0 RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0x0 RW	**Enable (EN):** When set, decode of the memory range pointed to by the IBASE is enabled.
0	0x0 RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

10.20.13 SBASE (SPI_BASE_ADDRESS)—Offset 54h

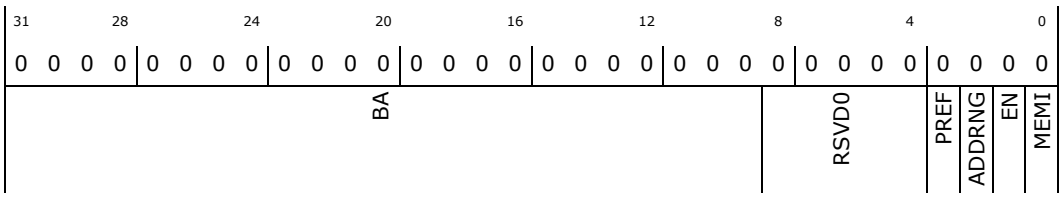
SPI registers are mapped into memory space. It is used by the SPI. Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RW	**Base Address (BA):** Provides 512 byte system memory base address for the SPI logic
8:4	0x0 RO	**RSVD0:** Reserved
3	0x0 RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0x0 RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0x0 RW	**Enable (EN):** When set, decode of the memory range pointed to by the SBASE is enabled.
0	0x0 RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

10.20.14 MPBASE (MPHY_BASE_ADDRESS)—Offset 58h

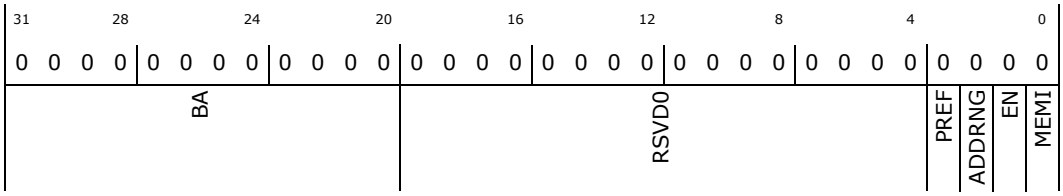
M-phys registers are mapped into memory space. It is used by the Proxy agent (to M-phys). Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:31, F:0] + 58h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**Base Address (BA):** Provides 1M byte system memory base address for the M phys logic
19:4	0x0 RO	**RSVD0:** Reserved

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0x0 RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0x0 RW	**Enable (EN):** When set, decode of the memory range pointed to by the MPBASE is enabled.
0	0x0 RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

10.20.15 PUBASE (PUNIT_BASE_ADDRESS)—Offset 5Ch

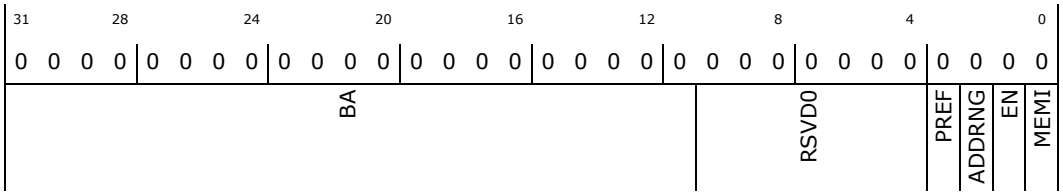
P-Unit registers are mapped into memory space. It is used by the Proxy agent (to P-Unit). Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:31, F:0] + 5Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:11	0x0 RW	**Base Address (BA):** Provides 2K byte system memory base address for the P-Unit registers
10:4	0x0 RO	**RSVD0:** Reserved
3	0x0 RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0x0 RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**Enable (EN):** When set, decode of the memory range pointed to by the PUBASE is enabled.
0	0x0 RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

10.20.16 UART Control (UART_CONT)—Offset 80h

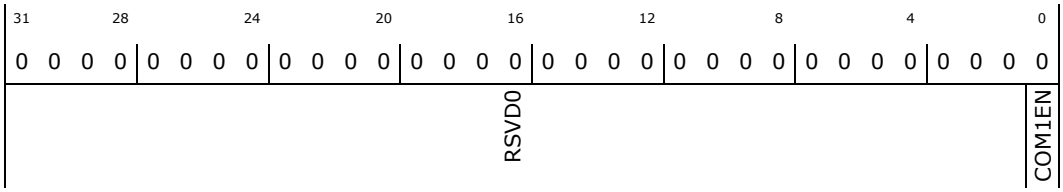
Controls the internal PCU UART ports

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:31, F:0] + 80h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RW	**COM1 Enable (COM1EN):** When set, enables the internal PCU COM1 UART port.

10.20.17 BIOS Decode Enable (PCIE_REG_BIOS_DECODE_EN)—Offset D8h

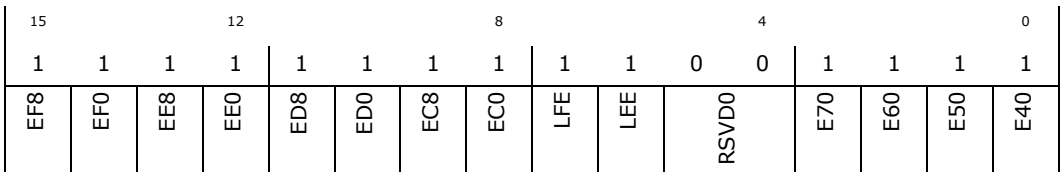
This register enables ranges in the BIOS for decoding purposes. Note that this register affects the BIOS decode regardless of whether the BIOS is resident on LPC or SPI. The concept of Feature Space does not apply to SPI-based flash. PCU EP simply decodes these ranges as memory accesses when enabled for the SPI/LPC flash interface.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

Offset: [B:0, D:31, F:0] + D8h

Default: FFCFh



Bit Range	Default & Access	Field Name (ID): Description
15	0x1 RW	**F8-FF Enable (EF8):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFF80000 - 0xFFFFFFFF - Feature space: 0xFFB80000 - 0xFFBFFFFF
14	0x1 RW	**F0-F8 Enable (EF0):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFF00000 - 0xFFF7FFFF - Feature space: 0xFFB00000 - 0xFFB7FFFF
13	0x1 RW	**E8-EF Enable (EE8):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFE80000 - 0xFFEFFFFF - Feature space: 0xFFA80000 - 0xFFAFFFFF
12	0x1 RW	**E0-E8 Enable (EE0):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFE00000 - 0xFFE7FFFF - Feature space: 0xFFA00000 - 0xFFA7FFFF
11	0x1 RW	**D8-DF Enable (ED8):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFD80000 - 0xFFDFFFFF - Feature space: 0XFF980000 - 0xFF9FFFFF
10	0x1 RW	**D0-D8 Enable (ED0):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFD00000 - 0xFFD7FFFF - Feature space: 0XFF900000 - 0xFF97FFFF
9	0x1 RW	**C8-CF Enable (EC8):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFC80000h - 0xFFCFFFFF - Feature space: 0xFF880000h - 0xFF8FFFFF
8	0x1 RW	**C0-C8 Enable (EC0):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFC00000 - 0xFFC7FFFF - Feature space: 0xFF800000 - 0xFF87FFFF
7	0x1 RW	**Legacy F Segment Enable (LFE):** This enables the decoding of the legacy 64KB range at 0xF0000 - 0xFFFFF
6	0x1 RW	**Legacy E Segment Enable (LEE):** This enables the decoding of the legacy 64KB range at 0xE0000 - 0xEFFFF
5:4	0x0 RO	**RSVD0:** Reserved
3	0x1 RW	**70-7F Enable (E70):** Enables decoding of 1MB of the following BIOS range: - Data space: 0xFF700000 - 0xFF7FFFFF - Feature space: 0xFF300000 - 0xFF3FFFFF
2	0x1 RW	**60-6F Enable (E60):** Enables decoding of 1MB of the following BIOS range: - Data space: 0xFF600000 - 0xFF6FFFFF - Feature Space: 0xFF200000 - 0xFF2FFFFF
1	0x1 RW	**50-5F Enable (E50):** Enables decoding of 1MB of the following BIOS range: - Data space: 0xFF500000 - 0xFF5FFFFF - Feature space: 0xFF100000 - 0xFF1FFFFF

Bit Range	Default & Access	Field Name (ID): Description
0	0x1 RW	**40-4F Enable (E40):** Enables decoding of 1MB of the following BIOS range: - Data space: 0xFF400000 - 0xFF4FFFFF - Feature Space: 0xFF000000 - 0xFF0FFFFF

10.20.18 FDCAP (Feature_Detection_Capability_ID)—Offset E0h

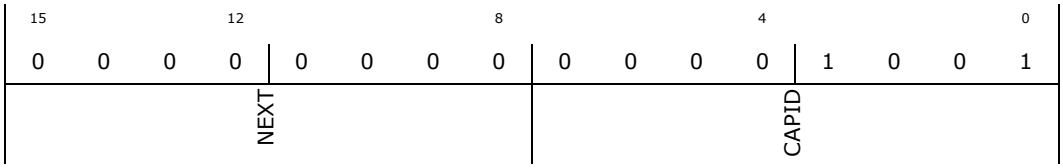
Feature detection capability ID.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

Offset: [B:0, D:31, F:0] + E0h

Default: 0009h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Next Item Pointer (NEXT):** Configuration offset of the next Capability Item. 0x00 indicates the last item in the Capability List.
7:0	0x9 RO	**Capability ID (CAPID):** Value of 0x09 indicates a Vendor Specific Capability

10.20.19 FDLEN (Feature_Detection_Capability_Length)—Offset E2h

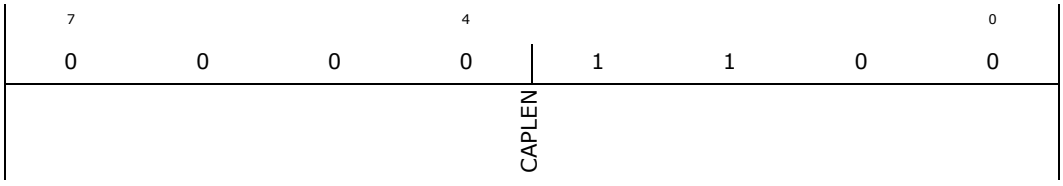
Feature detection capability length.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:31, F:0] + E2h

Default: 0Ch



Bit Range	Default & Access	Field Name (ID): Description
7:0	0xc RO	**Capability Length (CAPLEN):** Indicates the length of this Vendor Specific capability, as required by PCI Spec

10.20.20 FDVER (Feature_Detection_Version_Register)—Offset E3h

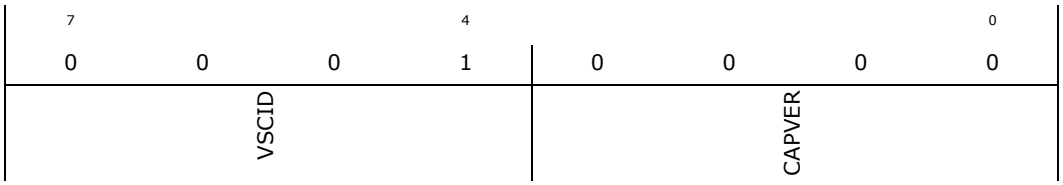
Feature detection version register.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Offset: [B:0, D:31, F:0] + E3h

Default: 10h



Bit Range	Default & Access	Field Name (ID): Description
7:4	0x1 RO	**Vendor-Specific Capability ID (VSCID):** A value of 0x1 in this 4-bit field identifies this Capability as Feature Detection Type. This field allows software to differentiate the Feature Detection Capability from other Vendor-Specific capabilities.
3:0	0x0 RO	**Capability Version (CAPVER):** This field indicates the version of the Feature Detection capability

10.20.21 FVECTIDX (Feature_Vector_Index)—Offset E4h

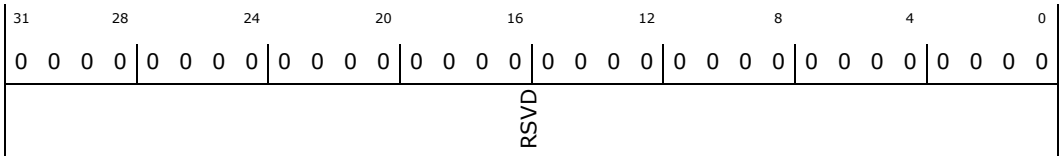
Feature vector index - Reserved

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:31, F:0] + E4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**RSVD:** RSVD

10.20.22 FVECTD (Feature_Vector_Data)—Offset E8h

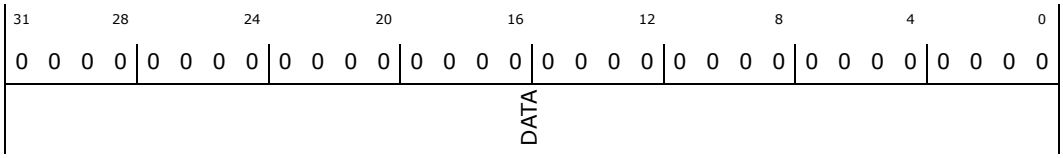
Feature vector data

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:31, F:0] + E8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Data (DATA):** 32-bit data value that is taken from capability feature fuses

10.20.23 RCBA (RCRB_BASE_ADDRESS)—Offset F0h

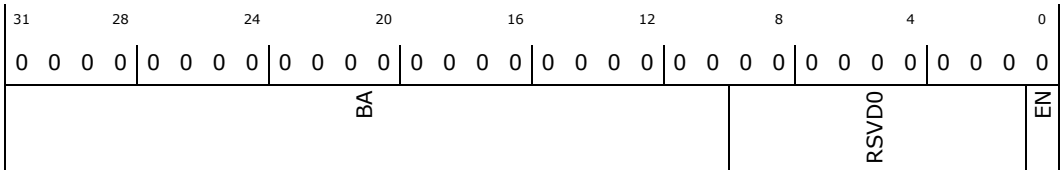
Root Complex registers are mapped into memory space. It is used by the PCU EP and Proxy engine.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:31, F:0] + F0h

Default: 00000000h



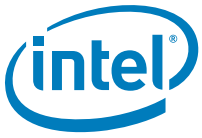
Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**Base Address (BA):** Base Address for the root complex register block decode range. This address is aligned on a 1KB boundary.
9:1	0x0 RO	**RSVD0:** Reserved
0	0x0 RW	**Enable (EN):** When set, enables the range specified in BA to be claimed as the RCRB.

11 PCI Express* 2.0 Registers

11.1 PCI Express* Lane 0 PCI Configuration Registers

Table 116. Summary of PCI Express Lane 0 PCI Configuration Registers—0/28/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Identifiers (ID)—Offset 0h" on page 5875	00008086h
4–7h	4	"Device Command; Primary Status (CMD_PSTS)—Offset 4h" on page 5875	00100000h
8–Bh	4	"Revision ID;Class Code (RID_CC)—Offset 8h" on page 5878	06040000h
C–Fh	4	"Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch" on page 5879	00810000h
18–1Bh	4	"Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h" on page 5880	00000000h
1C–1Fh	4	"I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch" on page 5880	00000000h
20–23h	4	"Memory Base and Limit (MBL)—Offset 20h" on page 5882	00000000h
24–27h	4	"Prefetchable Memory Base and Limit (PMBL)—Offset 24h" on page 5883	00010001h
28–2Bh	4	"Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h" on page 5884	00000000h
2C–2Fh	4	"Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch" on page 5884	00000000h
34–37h	4	"Capabilities List Pointer (CAPP)—Offset 34h" on page 5885	00000040h
3C–3Fh	4	"Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch" on page 5885	00000000h
40–43h	4	"Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h" on page 5887	00428010h
44–47h	4	"Device Capabilities (DCAP)—Offset 44h" on page 5888	00008000h
48–4Bh	4	"Device Control; Device Status (DCTL_DSTS)—Offset 48h" on page 5890	00100000h
4C–4Fh	4	"Link Capabilities (LCAP)—Offset 4Ch" on page 5893	00310C02h
50–53h	4	"Link Control; Link Status (LCTL_LSTS)—Offset 50h" on page 5895	00010000h
54–57h	4	"Slot Capabilities (SLCAP)—Offset 54h" on page 5898	00040060h
58–5Bh	4	"Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h" on page 5900	00000000h
5C–5Fh	4	"Root Control (RCTL)—Offset 5Ch" on page 5903	00000000h
60–63h	4	"Root Status (RSTS)—Offset 60h" on page 5904	00000000h
64–67h	4	"Device Capabilities 2 (DCAP2)—Offset 64h" on page 5904	00080817h
68–6Bh	4	"Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h" on page 5906	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
6C–6Fh	4	"Link Capabilities 2 (LCAP2)—Offset 6Ch" on page 5908	00000000h
70–73h	4	"Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h" on page 5909	00000000h
74–77h	4	"Slot Capabilities 2 (SLCAP2)—Offset 74h" on page 5911	00000000h
78–7Bh	4	"Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h" on page 5912	00000000h
80–83h	4	"Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h" on page 5912	00009005h
84–87h	4	"Message Signaled Interrupt Message Address (MA)—Offset 84h" on page 5913	00000000h
88–8Bh	4	"Message Signaled Interrupt Message Data (MD)—Offset 88h" on page 5914	00000000h
90–93h	4	"Subsystem Vendor Capability (SVCAP)—Offset 90h" on page 5914	0000A00Dh
94–97h	4	"Subsystem Vendor IDs (SVID)—Offset 94h" on page 5915	00000000h
A0–A3h	4	"Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h" on page 5916	C8030001h
A4–A7h	4	"PCI Power Management Control And Status (PMCS)—Offset A4h" on page 5917	00000008h
F8–FBh	4	"Manufacturer's ID (MANID)—Offset F8h" on page 5919	00000F00h
100–103h	4	"Advanced Error Reporting Capability Header (AECH)—Offset 100h" on page 5920	00000000h
104–107h	4	"Uncorrectable Error Status (UES)—Offset 104h" on page 5920	00000000h
108–10Bh	4	"Uncorrectable Error Mask (UEM)—Offset 108h" on page 5922	00000000h
10C–10Fh	4	"Uncorrectable Error Severity (UEV)—Offset 10Ch" on page 5924	00060011h
110–113h	4	"Correctable Error Status (CES)—Offset 110h" on page 5925	00000000h
114–117h	4	"Correctable Error Mask (CEM)—Offset 114h" on page 5926	00002000h
118–11Bh	4	"Advanced Error Capabilities and Control (AECC)—Offset 118h" on page 5927	00000000h
11C–11Fh	4	"Header Log DW1 (HL_DW1)—Offset 11Ch" on page 5928	00000000h
120–123h	4	"Header Log DW2 (HL_DW2)—Offset 120h" on page 5929	00000000h
124–127h	4	"Header Log DW3 (HL_DW3)—Offset 124h" on page 5929	00000000h
128–12Bh	4	"Header Log DW4 (HL_DW4)—Offset 128h" on page 5930	00000000h
12C–12Fh	4	"Root Error Command (REC)—Offset 12Ch" on page 5930	00000000h
130–133h	4	"Root Error Status (RES)—Offset 130h" on page 5931	00000000h
134–137h	4	"Error Source Identification (ESID)—Offset 134h" on page 5932	00000000h
200–203h	4	"L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h" on page 5933	00010000h
204–207h	4	"L1 Sub-States Capabilities (L1SCAP)—Offset 204h" on page 5934	0028281Fh
208–20Bh	4	"L1 Sub-States Control 1 (L1SCTL1)—Offset 208h" on page 5936	00000010h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
20C–20Fh	4	"L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch" on page 5938	00000028h
328–32Bh	4	"PCI Express Status 1 (PCIESTS1)—Offset 328h" on page 5939	00000000h
32C–32Fh	4	"PCI Express Status 2 (PCIESTS2)—Offset 32Ch" on page 5942	00000000h
330–333h	4	"PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h" on page 5944	28000016h
334–337h	4	"PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h" on page 5946	4ABCB5BCh
414–417h	4	"Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h" on page 5947	00000000h

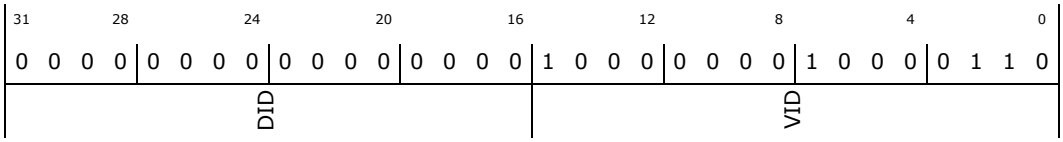
11.1.1 Identifiers (ID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO/V	**Device Identification (DID):** The value of this ID is product specific. **Power Well:** Core
15:0	0x8086 RO	**Vendor Identification (VID):** Indicates Intel **Power Well:** Core

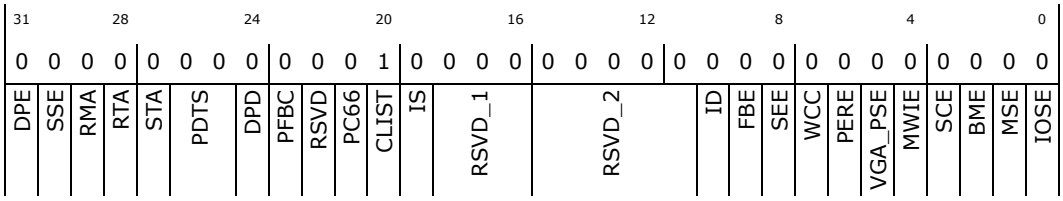
11.1.2 Device Command; Primary Status (CMD_PSTS)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

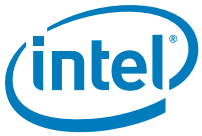
Offset: [B:0, D:28, F:0] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C/V	**DPE - Detected Parity Error (DPE):** Set when the root port receives a command or data from the backbone with a parity error. This is set even if CMD.PERE is not set. **Power Well:** Core
30	0x0 RW/1C/V	**Signaled System Error (SSE):** Set when the root port signals a system error to the internal SERR# logic. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
29	0x0 RW/1C/V	**Received Master Abort (RMA):** Set when the root port receives a completion with unsupported request status from the backbone. **Power Well:** Core
28	0x0 RW/1C/V	**Received Target Abort (RTA):** Set when the root port receives a completion with completer abort from the backbone. **Power Well:** Core
27	0x0 RW/1C/V	**Signaled Target Abort (STA):** Set whenever the root port forwards a target abort received from the downstream device onto the backbone. **Power Well:** Core
26:25	0x0 RO	**Primary DEVSEL# Timing Status (PDTS):** Reserved per PCI-Express spec **Power Well:** Core
24	0x0 RW/1C/V	**Master Data Parity Error Detected (DPD):** Set when the root port receives a completion with a data parity error on the backbone and CMD.PERE is set. **Power Well:** Core
23	0x0 RO	**Primary Fast Back to Back Capable (PFBC):** Reserved per PCI-Express spec. **Power Well:** Core
22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**Primary 66 MHz Capable (PC66):** Reserved per PCI-Express spec. **Power Well:** Core
20	0x1 RO	**Capabilities List (CLIST):** Indicates the presence of a capabilities list. **Power Well:** Core
19	0x0 RO/V	**Interrupt Status (IS):** Indicates status of hot plug and power management interrupts on the root port that result in INTx# message generation. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of CMD.ID. **Power Well:** Core
18:16	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
15:11	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
10	0x0 RW/V2	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above. **Power Well:** Core
9	0x0 RO	**Fast Back to Back Enable (FBE):** Reserved per PCI-Express spec. **Power Well:** Core
8	0x0 RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set. **Power Well:** Core
7	0x0 RO	**Wait Cycle Control (WCC):** Reserved per PCI-Express spec. **Power Well:** Core
6	0x0 RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a master on the backbone. **Power Well:** Core
4	0x0 RO	**Memory Write and Invalidate Enable (MWIE):** Reserved per PCI-Express spec. **Power Well:** Core
3	0x0 RO	**Special Cycle Enable (SCE):** Reserved per PCI-Express and PCI bridge spec. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**Bus Master Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit. **Power Well:** Core
1	0x0 RW	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone. **Power Well:** Core
0	0x0 RW	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone. **Power Well:** Core

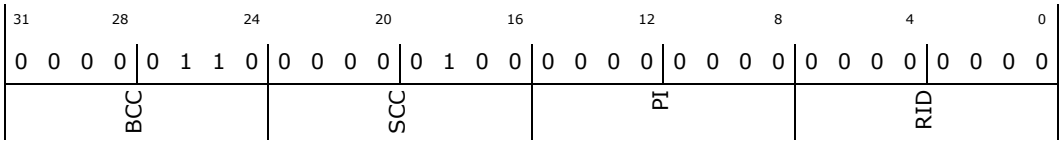
11.1.3 Revision ID;Class Code (RID_CC)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 8h

Default: 06040000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x6 RO	**Base Class Code (BCC):** Indicates the device is a bridge device. **Power Well:** Core
23:16	0x4 RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO/V	**Programming Interface (PI):** The value reported in this register is a function of the Decode Control.Subtractive Decode Enable (SDE) register. SDE Value reported in this register 0: 00h 1: 01h **Power Well:** Core
7:0	0x0 RO/V	**Revision ID (RID):** Indicates the revision of the bridge. **Power Well:** Core

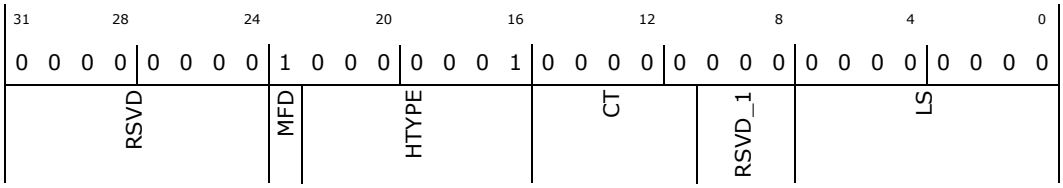
11.1.4 Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + Ch

Default: 00810000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
23	0x1 RO	**Multi-function Device (MFD):** This bit is '1' to indicate a multi-function device. **Power Well:** Core
22:16	0x1 RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h. **Power Well:** Core
15:11	0x0 RO	**Latency Count (CT):** Reserved per PCI-Express spec **Power Well:** Core
10:8	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**Line Size (LS):** This is read/write but contains no functionality, per PCI-Express spec **Power Well:** Core

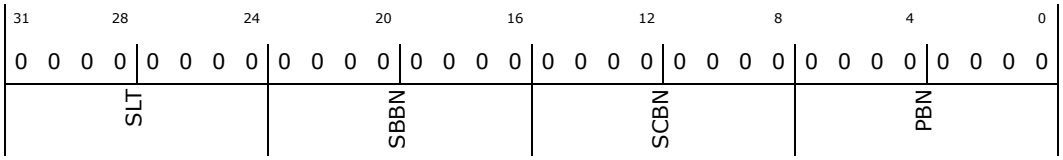
11.1.5 Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 18h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW/V2	**Secondary Latency Timer (SLT):** For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is a RW register; else this register is RO and returns 0. This register does not affect the behavior of any HW logic. **Power Well:** Core
23:16	0x0 RW	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge. **Power Well:** Core
15:8	0x0 RW	**Secondary Bus Number (SCBN):** Indicates the bus number the port. **Power Well:** Core
7:0	0x0 RW	**Primary Bus Number (PBN):** Indicates the bus number of the backbone. **Power Well:** Core

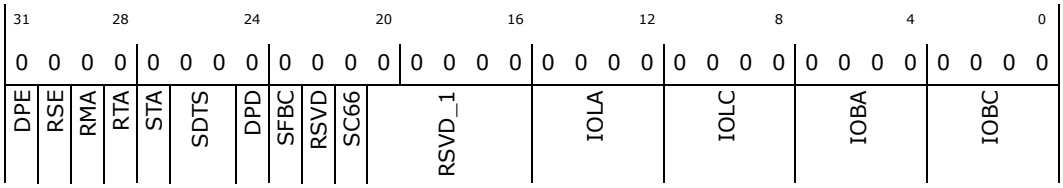
11.1.6 I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 1Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C/V	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP. **Power Well:** Core
30	0x0 RW/1C/V	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device. **Power Well:** Core
29	0x0 RW/1C/V	**Received Master Abort (RMA):** Set when the port receives a completion with [quote]Unsupported Request[/quote] status from the device. **Power Well:** Core
28	0x0 RW/1C/V	**Received Target Abort (RTA):** Set when the port receives a completion with [quote]Completion Abort[/quote] status from the device. **Power Well:** Core
27	0x0 RW/1C/V	**Signaled Target Abort (STA):** Set when the port generates a completion with [quote]Completion Abort[/quote] status to the device. **Power Well:** Core
26:25	0x0 RO/V	**Secondary DEVSEL# Timing Status (SDTS):** Reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b. **Power Well:** Core
24	0x0 RW/1C/V	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side. **Power Well:** Core
23	0x0 RO/V	**Secondary Fast Back to Back Capable (SFBC):** Reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**Secondary 66 MHz Capable (SC66):** Reserved per PCI Express spec **Power Well:** Core
20:16	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
15:12	0x0 RW	**I/O Address Limit (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh. **Power Well:** Core
11:8	0x0 RO	**I/O Limit Address Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing. **Power Well:** Core
7:4	0x0 RW	**I/O Base Address (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h. **Power Well:** Core
3:0	0x0 RO	**I/O Base Address Capability (IOBC):** Indicates that the bridge does not support 32-bit I/O addressing. **Power Well:** Core

11.1.7 Memory Base and Limit (MBL)—Offset 20h

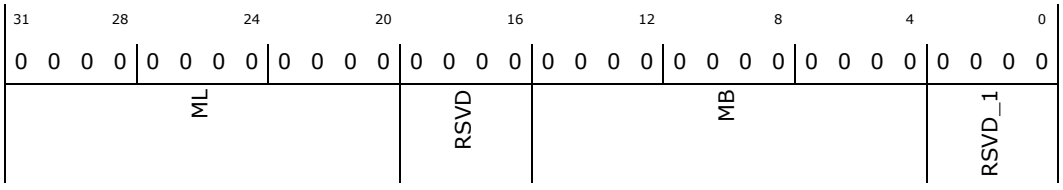
Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is MB [gt]= AD[lb]31:20[rb] [lt]= ML.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 20h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range. **Power Well:** Core
19:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:4	0x0 RW	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range. **Power Well:** Core
3:0	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

11.1.8 Prefetchable Memory Base and Limit (PMBL)—Offset 24h

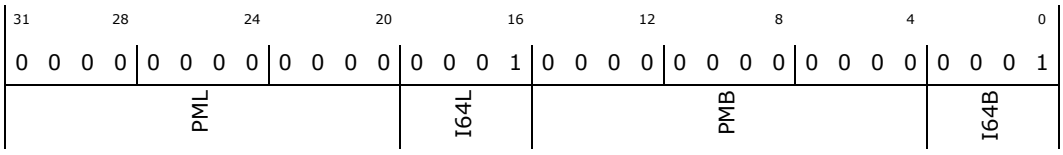
Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is PMBU32:PMB [gt]= AD[lb]63:32[rb]:AD[lb]31:20[rb] [lt]= PMLU32:PML.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 24h

Default: 00010001h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range. **Power Well:** Core
19:16	0x1 RO	**64-bit Indicator (I64L):** Indicates support for 64-bit addressing. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:4	0x0 RW	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range. **Power Well:** Core
3:0	0x1 RO	**64-bit Indicator (I64B):** Indicates support for 64-bit addressing. **Power Well:** Core

11.1.9 Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h

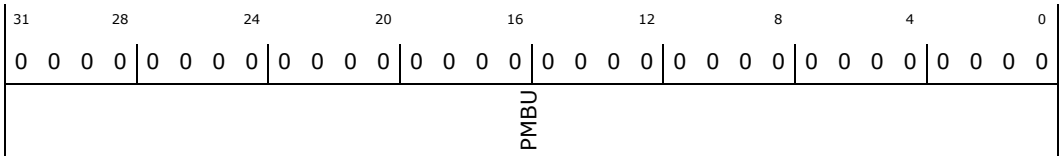
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 28h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base. **Power Well:** Core

11.1.10 Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch

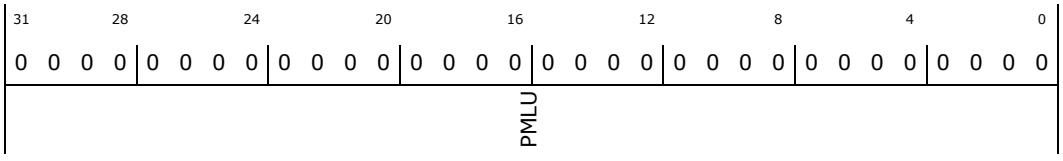
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit. **Power Well:** Core

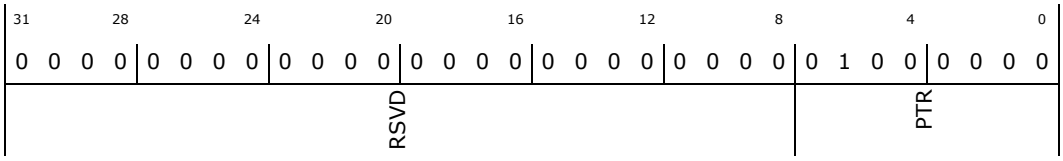
11.1.11 Capabilities List Pointer (CAPP)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 34h

Default: 00000040h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
7:0	0x40 RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. Capability Linked List (Default Settings) Offset Capability Next Pointer 40h PCI Express 80h 80h Message Signaled Interrupt (MSI) 90h 90h Subsystem Vendor A0h A0h PCI Power Management 00h Extended PCIe Capability Linked List Offset Capability Next Pointer 100h Advanced Error Reporting 000h **Power Well:** Core

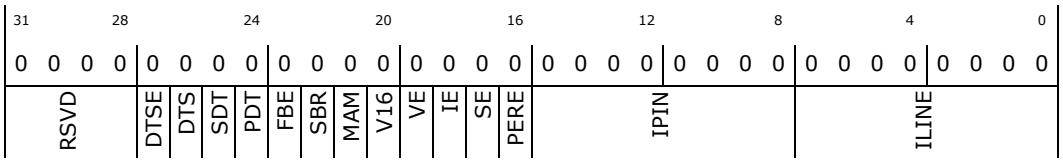
11.1.12 Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch

Access Method

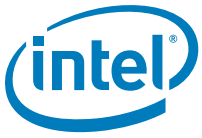
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 3Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
27	0x0 RW/V2	**Discard Timer SERR# Enable (DTSE):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port. **Power Well:** Core
26	0x0 RO	**Discard Timer Status (DTS):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, this register can remain RO as no secondary discard timer exists that will ever cause it to be set. **Power Well:** Core
25	0x0 RW/V2	**Secondary Discard Timer (SDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port. **Power Well:** Core
24	0x0 RW/V2	**Primary Discard Timer (PDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port. **Power Well:** Core
23	0x0 RO	**Fast Back to Back Enable (FBE):** Reserved per Express spec. **Power Well:** Core
22	0x0 RW	**Secondary Bus Reset (SBR):** Triggers a Hot Reset on the PCI-Express port. **Power Well:** Core
21	0x0 RW/V2	**Master Abort Mode (MAM):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port. **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
18	0x0 RW	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh). **Power Well:** Core
17	0x0 RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not. **Power Well:** Core
16	0x0 RW	**Parity Error Response Enable (PERE):** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD. **Power Well:** Core
15:8	0x0 RO/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the STRPFUSECFG register in chipset config space: Port Bits[lb]15:12[rb] Bits[lb]11:08[rb] 1 0h STRPFUSECFG.P1IP 2 0h STRPFUSECFG.P2IP 3 0h STRPFUSECFG.P3IP 4 0h STRPFUSECFG.P4IP 5 0h STRPFUSECFG.P5IP 6 0h STRPFUSECFG.P6IP 7 0h STRPFUSECFG.P7IP 8 0h STRPFUSECFG.P8IP The value that is programmed into STRPFUSECFG is always reflected in this register. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register returns a value of 00h when read, else this register returns the value from the table above. **Power Well:** Core
7:0	0x0 RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. **Power Well:** Core

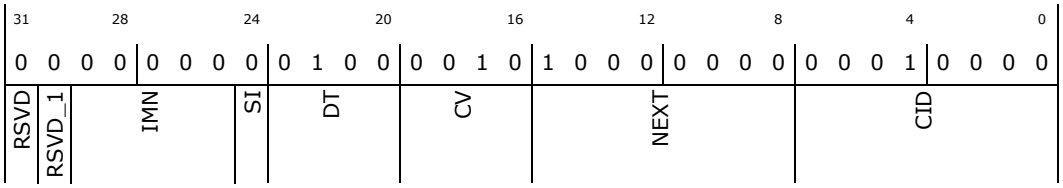
11.1.13 Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 40h

Default: 00428010h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
30	0x0 RO	**Reserved (RSVD_1):** Reserved. This register at one time was for TCS Routing but that was later removed from the PCIe 2.0 spec **Power Well:** Core
29:25	0x0 RO	**Interrupt Message Number (IMN):** The PCIE SIP does not have multiple MSI interrupt numbers. **Power Well:** Core
24	0x0 RW/O	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset. **Power Well:** Core
23:20	0x4 RO	**Device / Port Type (DT):** Indicates this is a PCI-Express root port **Power Well:** Core
19:16	0x2 RO	**Capability Version (CV):** Version 2.0 indicates devices compliant to the PCI Express 2.0 specification which incorporates the Register Expansion ECN. **Power Well:** Core
15:8	0x80 RW/O	**Next Capability (NEXT):** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. **Power Well:** Core
7:0	0x10 RO	**Capability ID (CID):** Indicates this is a PCI Express capability **Power Well:** Core

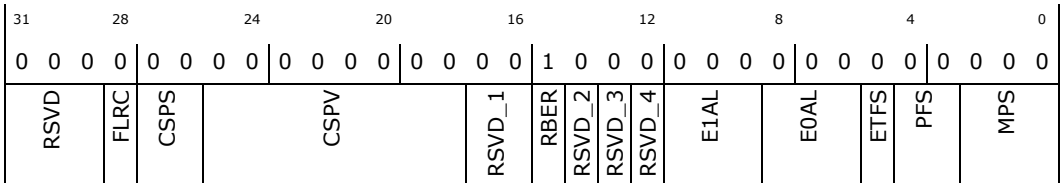
11.1.14 Device Capabilities (DCAP)—Offset 44h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 44h

Default: 00008000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
28	0x0 RO	**Function Level Reset Capable (FLRC):** Not supported in Root Ports **Power Well:** Core
27:26	0x0 RO	**Captured Slot Power Limit Scale (CSPS):** Not supported **Power Well:** Core
25:18	0x0 RO	**Captured Slot Power Limit Value (CSPV):** Not supported **Power Well:** Core
17:16	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
15	0x1 RO	**Role Based Error Reporting (RBER):** When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions. **Power Well:** Core
14	0x0 RO	**Reserved (RSVD_2):** Reserved. On previous version of the specification this was Power Indicator Present (PIP) **Power Well:** Core
13	0x0 RO	**Reserved (RSVD_3):** Reserved. On previous version of the specification this was Attention Indicator Present (AIP) **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12	0x0 RO	**Reserved (RSVD_4):** Reserved. On previous version of the specification this was Attention Button Present (ABP) **Power Well:** Core
11:9	0x0 RO	**Endpoint L1 Acceptable Latency (E1AL):** Reserved for root ports. **Power Well:** Core
8:6	0x0 RO	**Endpoint L0 Acceptable Latency (E0AL):** Reserved for Root port. **Power Well:** Core
5	0x0 RO	**Extended Tag Field Supported (ETFS):** The PCIE SIP never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags. **Power Well:** Core
4:3	0x0 RO	**Phantom Functions Supported (PFS):** No phantom functions supported **Power Well:** Core
2:0	0x0 RW/O	**Max Payload Size Supported (MPS):** BIOS should write to this field during system initialization. Only Max Payload Size of 128B is supported. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. **Power Well:** Core

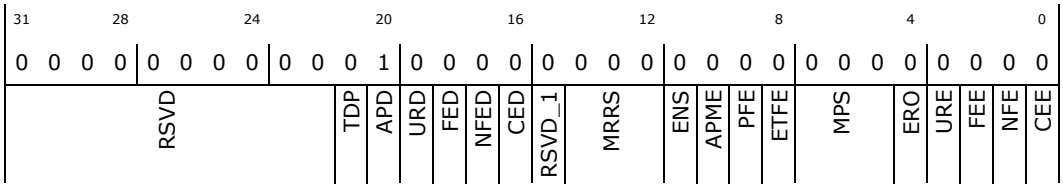
11.1.15 Device Control; Device Status (DCTL_DSTS)—Offset 48h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 48h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID. **Power Well:** Core
20	0x1 RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup **Power Well:** Core
19	0x0 RW/1C/V	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected. **Power Well:** Core
18	0x0 RW/1C/V	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed tlp **Power Well:** Core
17	0x0 RW/1C/V	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned tlp, unexpected completions, unsupported requests, completor abort, or completer timeout **Power Well:** Core
16	0x0 RW/1C/V	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, tlp crc error, dllp crc error, replay num rollover, replay timeout. **Power Well:** Core
15	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
14:12	0x0 RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11	0x0 RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests. **Power Well:** Core
10	0x0 RW/P	**Aux Power PM Enable (APME):** The OS will set this bit to '1' if the device connected has detected aux power. **Power Well:** Core
9	0x0 RO	**Phantom Functions Enable (PFE):** Not supported **Power Well:** Core
8	0x0 RO	**Extended Tag Field Enable (ETFE):** Not supported **Power Well:** Core
7:5	0x0 RW	**Max Payload Size (MPS):** The root port only supports 128B max payload. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. If the DCAP.MPS indicates 128B max payload size support, programming this field to any values other than 128B will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME. **Power Well:** Core
4	0x0 RO	**Enable Relaxed Ordering (ERO):** Not supported **Power Well:** Core
3	0x0 RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**Fatal Error Reporting Enable (FEE):** enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting. **Power Well:** Core
1	0x0 RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting. **Power Well:** Core
0	0x0 RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting. **Power Well:** Core

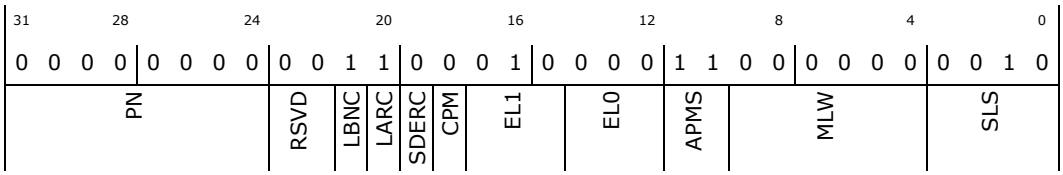
11.1.16 Link Capabilities (LCAP)—Offset 4Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 4Ch

Default: 00310C02h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port # Value of PN field 1 01h 2 02h 3 03h 4 04h **Power Well:** Core
23:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
21	0x1 RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms. **Power Well:** Core
20	0x1 RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. **Power Well:** Core
19	0x0 RO	**Surprise Down Error Reporting Capable (SDERC):** Set to '0' to indicate the root port does not support Surprise Down Error Reporting **Power Well:** Core
18	0x0 RO	**Clock Power Management (CPM):** '0' Indicates that root ports do not support the CLKREQ# mechanism. **Power Well:** Core
17:15	0x2 RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b Less than 1 us 001b 1 us to less than 2 us 010b 2 us to less than 4 us 011b 4 us to less than 8 us 100b 8 us to less than 16 us 101b 16 us to less than 32 us 110b 32 us to 64 us 111b More than 64 us Note: If PXP PLL shutdown is enabled, BIOS should program this latency to comprehend PLL lock latency. **Power Well:** Core
14:12	0x0 RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration: LCTL.CCC Value 0 MPC.UCEL 1 MPC.CCEL **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11:10	0x3 RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00 (Reserved) 01 L0s Entry supported 10 Reserved 11 Both L0s and L1 supported Note: If STRPFUSECFG.ASPMDIS is 1, the default of this field is [quote]01[/quote]. Otherwise, the default of this field is [quote]11[/quote]. If STRPFUSECFG.ASPMDIS is 1, BIOS writing [quote]11[/quote] to this field will have the same effect as [quote]01[/quote]. [quote]01[/quote] will be reflected on this register when read and the register will turn to Read-Only once written once. **Power Well:** Core
9:4	0x0 RO/V	**Maximum Link Width (MLW):** For the root ports, several values can be taken, based upon the value of the chipset configuration register field RPC.PC1 for ports 1-4: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h **Power Well:** Core
3:0	0x2 RO/V	**Supported Link Speeds (SLS):** Indicates the supported link speeds of the Root Port. 0001b 2.5 GT/s Link speed supported 0010b 5.0 GT/s and 2.5GT/s Link speeds supported This register reports a value of 0001b if the Root Port Gen2 Disable Fuse is set or the MPC.PCIEGEN2DIS bit is set, else this register reports a value of 0010b. **Power Well:** Core

11.1.17 Link Control; Link Status (LCTL_LSTS)—Offset 50h

Access Method

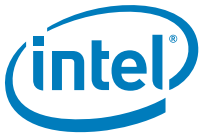
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 50h

Default: 00010000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LABS	LBMS	LA	SCC	LT	RSVD	NLW						CLS				RSVD_1				LABIE	LBMIE	HAWD	ECPM	ES	CCC	RL	LD	RCBC	RSVD_2	ASPM	

Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C/V	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b. **Power Well:** Core
30	0x0 RW/1C/V	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b. **Power Well:** Core
29	0x0 RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise. **Power Well:** Core
28	0x0 RO/V	**Slot Clock Configuration (SCC):** In normal mode, PCIE SIP uses the same reference clock as on the platform and does not generate its own clock. Note: The default of this register bit is dependent on the [quote]PCIe Non-Common Clock With SSC Mode Enable Strap[/quote]. If the strap enables non-common clock with SSC support, this bit shall default to '0'. Otherwise, this bit shall default to '1'. **Power Well:** Core
27	0x0 RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training. **Power Well:** Core
26	0x0 RO	**Reserved (RSVD):** Reserved. Previously this was defined as Link Training Error (LTE) but support for this bit was removed from subsequent versions of the PCI Express specification. **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
25:20	0x0 RO/V	**Negotiated Link Width (NLW):** For the root ports, this register could take on several values: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h The value of this register is undefined if the link has not successfully trained. **Power Well:** Core
19:16	0x1 RO/V	**Current Link Speed (CLS):** 0001b Link is 2.5Gb/s Link 0010b 5.0 GT/s Link The value of this field is undefined if the link is not up. **Power Well:** Core
15:12	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
11	0x0 RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set. **Power Well:** Core
10	0x0 RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b. **Power Well:** Core
9	0x0 RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Default value of this bit is 0b. **Power Well:** Core
8	0x0 RO	**Enable Clock Power Management (ECPM):** Reserved. Not supported on PCIE SIP Root Ports. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW	**Extended Synch (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0. **Power Well:** Core
6	0x0 RW	**Common Clock Configuration (CCC):** When set, indicates that the PCIE SIP and device are operating with a distributed common reference clock. **Power Well:** Core
5	0x0 WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns '0' when read. Software uses LSTS.LT to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress. **Power Well:** Core
4	0x0 RW	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state. **Power Well:** Core
3	0x0 RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes. **Power Well:** Core
2	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
1:0	0x0 RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used. Note: If STRPFUSECFG.ASPMDIS is '1', hardware will always see [quote]00[/quote] as an output from this register. BIOS reading this register should always return the correct value. **Power Well:** Core

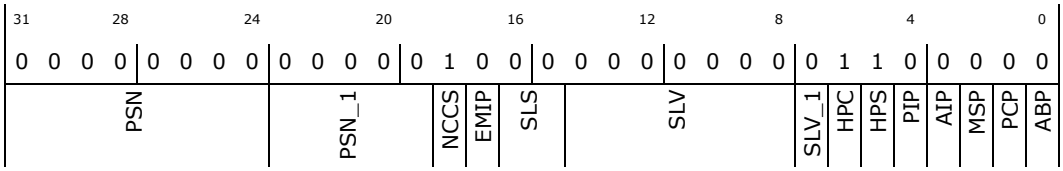
11.1.18 Slot Capabilities (SLCAP)—Offset 54h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 54h

Default: 00040060h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW/O	**Physical Slot Number (PSN):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
23:19	0x0 RW/O	**Physical Slot Number (PSN_1):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
18	0x1 RO	**No Command Completed Support (NCCS):** Set to '1' as this port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes. **Power Well:** Core
17	0x0 RO	**Electromechanical Interlock Present (EMIP):** Set to 0 to indicate that no electro-mechanical interlock is implemented. **Power Well:** Core
16:15	0x0 RW/O	**Slot Power Limit Scale (SLS):** specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
14:8	0x0 RW/O	**Slot Power Limit Value (SLV):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
7	0x0 RW/O	**Slot Power Limit Value (SLV_1):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
6	0x1 RW/O	**Hot Plug Capable (HPC):** When set, Indicates that hot plug is supported. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5	0x1 RW/O	**Hot Plug Surprise (HPS):** When set, indicates the device may be removed from the slot without prior notification. **Power Well:** Core
4	0x0 RO	**Power Indicator Present (PIP):** Indicates that a power indicator LED is not present for this slot. **Power Well:** Core
3	0x0 RO	**Attention Indicator Present (AIP):** Indicates that an attention indicator LED is not present for this slot. **Power Well:** Core
2	0x0 RO	**MRL Sensor Present (MSP):** Indicates that an MRL sensor is not present **Power Well:** Core
1	0x0 RO	**Power Controller Present (PCP):** Indicates that a power controller is not implemented for this slot **Power Well:** Core
0	0x0 RO	**Attention Button Present (ABP):** Indicates that an attention button is not implemented for this slot. **Power Well:** Core

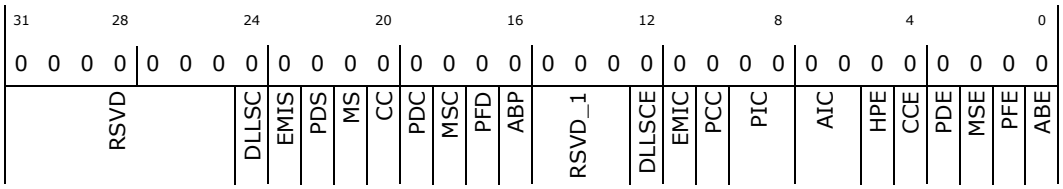
11.1.19 Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h

Access Method

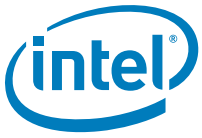
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 58h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
24	0x0 RW/1C/V	**Data Link Layer State Changed (DLLSC):** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device. **Power Well:** Core
23	0x0 RO	**Electromechanical Interlock Status (EMIS):** Reserved as this port does not support and electromechanical interlock. **Power Well:** Core
22	0x0 RO/V	**Presence Detect State (PDS):** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected ('1') or empty ('0'). If XCAP.SI is cleared, this bit is a '1'. **Power Well:** Core
21	0x0 RO	**MRL Sensor State (MS):** Reserved as the MRL sensor is not implemented. **Power Well:** Core
20	0x0 RO	**Command Completed (CC):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
19	0x0 RW/1C/V	**Presence Detect Changed (PDC):** This bit is set by the root port when the SLSTS.PDS bit changes state. **Power Well:** Core
18	0x0 RO	**MRL Sensor Changed (MSC):** Reserved as the MRL sensor is not implemented. **Power Well:** Core
17	0x0 RO	**Power Fault Detected (PFD):** Reserved as a power controller is not implemented. **Power Well:** Core
16	0x0 RO	**Attention Button Pressed (ABP):** This register is RO as this port does not implement an attention button **Power Well:** Core
15:13	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12	0x0 RW	**Data Link Layer State Changed Enable (DLLSCE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed **Power Well:** Core
11	0x0 RO	**Electromechanical Interlock Control (EMIC):** Reserved as this port does not support an Electromechanical Interlock. **Power Well:** Core
10	0x0 RO	**Power Controller Control (PCC):** This bit has no meaning for module based hot plug. **Power Well:** Core
9:8	0x0 RO	**Power Indicator Control (PIC):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
7:6	0x0 RO	**Attention Indicator Control (AIC):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
5	0x0 RW	**Hot Plug Interrupt Enable (HPE):** When set, enables generation of a hot plug interrupt on enabled hot plug events. **Power Well:** Core
4	0x0 RO	**Command Completed Interrupt Enable (CCE):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
3	0x0 RW	**Presence Detect Changed Enable (PDE):** When set, enables the generation of a hot plug interrupt or wake message when the presence detect logic changes state. **Power Well:** Core
2	0x0 RO	**MRL Sensor Changed Enable (MSE):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
1	0x0 RO	**Power Fault Detected Enable (PFE):** This register is RO as this port does not implement a Hot Plug Controller... **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RO	**Attention Button Pressed Enable (ABE):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core

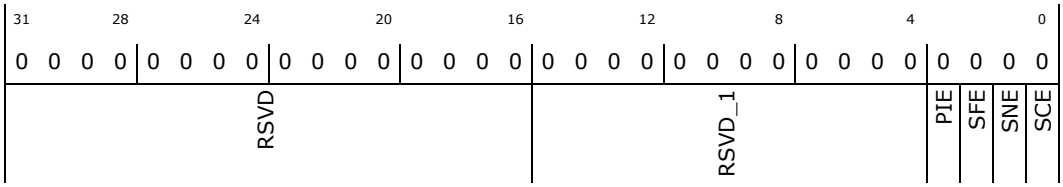
11.1.20 Root Control (RCTL)—Offset 5Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 5Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:4	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
3	0x0 RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a '0' to '1' transition, or due to this bit being set with RSTS.PS already set). **Power Well:** Core
2	0x0 RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set. **Power Well:** Core
1	0x0 RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set. **Power Well:** Core

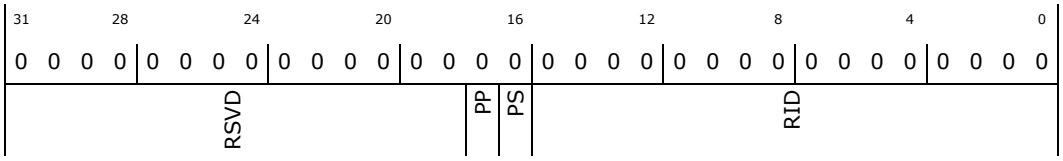
11.1.21 Root Status (RSTS)—Offset 60h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 60h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
17	0x0 RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. PCIE SIP root ports have a one deep PME pending queue. **Power Well:** Core
16	0x0 RW/1C/V	**PME Status (PS):** Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared. **Power Well:** Core
15:0	0x0 RO/V	**PME Requestor ID (RID):** Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set. PCIE SIP root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped. **Power Well:** Core

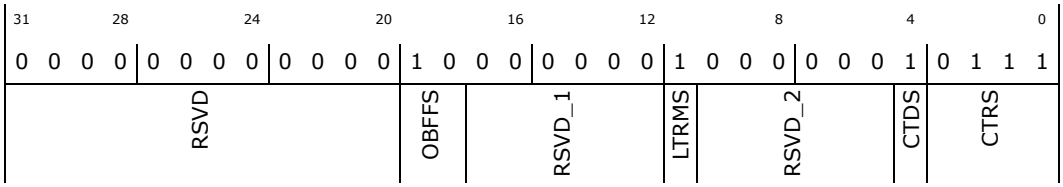
11.1.22 Device Capabilities 2 (DCAP2)—Offset 64h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 64h

Default: 00080817h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
19:18	0x2 RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b - OBFF is not supported. 01b - OBFF is supported using Message signaling only. 10b - OBFF is supported using WAKE# signaling only. 11b - OBFF is supported using WAKE# and Message signaling. BIOS should program this field to 00b or 10b during system initialization to advertise the level of hardware OBFF support to software. BIOS should never program this field to 01b or 11b since OBFF messaging is not supported. **Power Well:** Core
17:12	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
11	0x1 RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a '1' or a '0' to enable/disable the root port from declaring support for the LTR capability. **Power Well:** Core
10:5	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
4	0x1 RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x7 RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A [amp] B 0110b Ranges B [amp] C 0111b Ranges A, B [amp] C [lt]-- This is what IP supports 1110b Ranges B, C [amp] D 1111b Ranges A, B, C [amp] D All other values are reserved. **Power Well:** Core

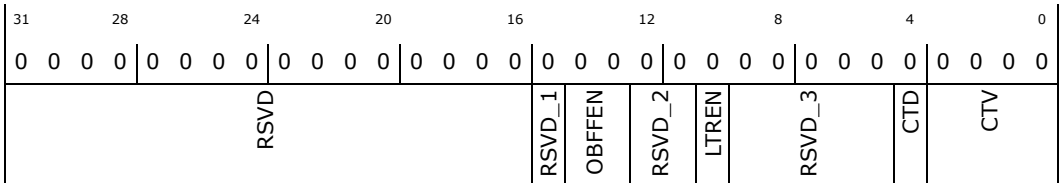
11.1.23 Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h

Access Method

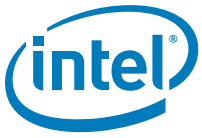
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 68h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
14:13	0x0 RW	**Optimized Buffer Flush/Fill Enable (OBFFEN):** 00b Disable OBFF mechanism. 01b Enable OBFF mechanism using Message signaling (Variation A). 10b Enable OBFF mechanism using Message signaling (Variation B). 11b Enable OBFF using WAKE# signaling. Note: Only encoding 00b and 11b are supported. The encoding of 01b or 10b would be aliased to 00b. If DCAP2.OBFFS is clear, programming this field to any non-zero values will have no effect. **Power Well:** Core
12:11	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
10	0x0 RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect. **Power Well:** Core
9:5	0x0 RO	**Reserved (RSVD_3):** Reserved **Power Well:** Core
4	0x0 RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x0 RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. ThePCIE SIP targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range A (50us to 10 ms) programmability range is supported: 0001b 90-100us (spec range is 50 us to 100 us) 0010b 9-10ms (spec range is 1ms to 10 ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either when this value was changed or when each request was issued. **Power Well:** Core

11.1.24 Link Capabilities 2 (LCAP2)—Offset 6Ch

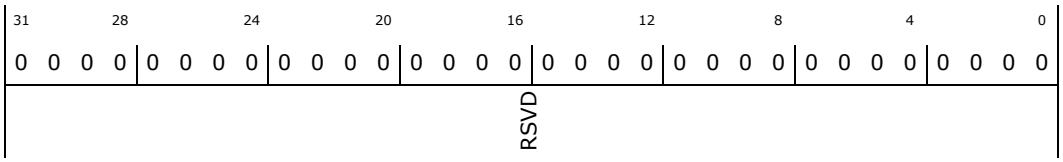
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 6Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

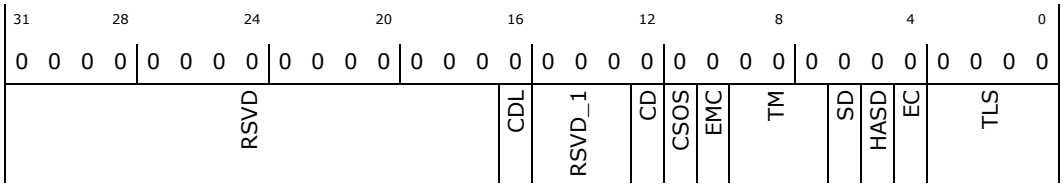
11.1.25 Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 70h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
16	0x0 RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is operating at 2.5 GT/s speed. **Power Well:** Core
15:13	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
12	0x0 RW/P	**Compliance De-emphasis (CD):** This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s, the setting of this bit has no effect. The default value of this bit is 0b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11	0x0 RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b. **Power Well:** Core
10	0x0 RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value. **Power Well:** Core
9:7	0x0 RW/P	**Transmit Margin (TM):** This field controls the value of the nondeemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see PCI Express Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value. **Power Well:** Core
6	0x0 RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RO	**Hardware Autonomous Speed Disable (HASD):** Reserved. This port cannot autonomously change speeds. **Power Well:** Core
4	0x0 RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. **Power Well:** Core
3:0	0x0 RW/V/P	**Target Link Speed (TLS):** This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. For PCIE SIP, the allowed value is: 0001b 2.5 GT/s Target Link Speed 0010b 5.0 GT/s and 2.5GT/s Link speeds supported If a value is written to this field that does not correspond to a speed included in the Supported Link Speeds field, the result is undefined. The default value of this field is the highest Link speed supported by the component (as reported in the Supported Link Speeds field of the Link Capabilities register). **Power Well:** Core

11.1.26 Slot Capabilities 2 (SLCAP2)—Offset 74h

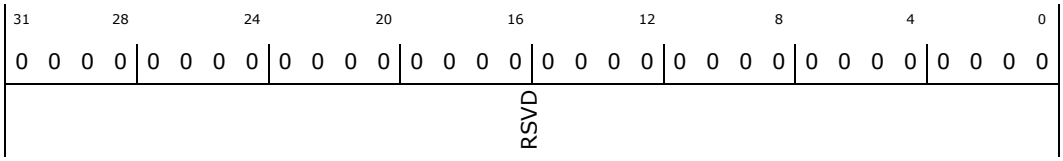
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 74h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

11.1.27 Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h

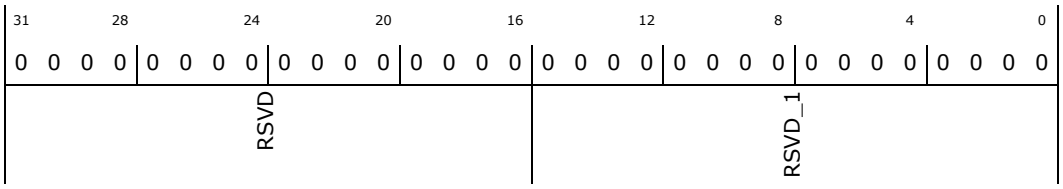
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 78h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:0	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

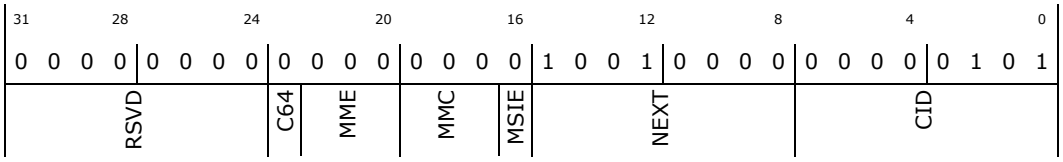
11.1.28 Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 80h

Default: 00009005h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
23	0x0 RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
22:20	0x0 RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port. **Power Well:** Core
19:17	0x0 RO	**Multiple Message Capable (MMC):** Only one message is required. **Power Well:** Core
16	0x0 RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated. **Power Well:** Core
15:8	0x90 RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. **Power Well:** Core
7:0	0x5 RO	**Capability ID (CID):** Capabilities ID indicates MSI. **Power Well:** Core

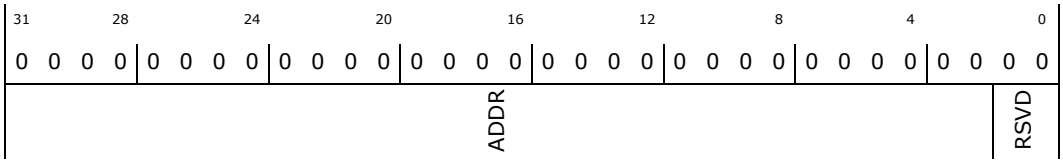
11.1.29 Message Signaled Interrupt Message Address (MA)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 84h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Address (ADDR):** Lower 32 bits of the system specified message address, always DW aligned. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1:0	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

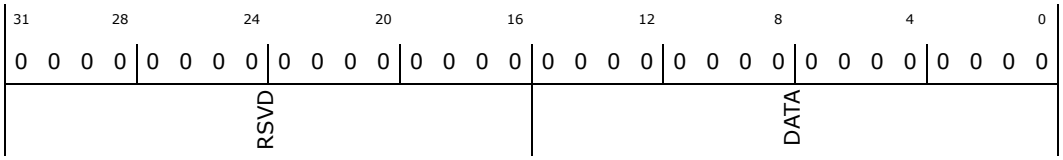
11.1.30 Message Signaled Interrupt Message Data (MD)—Offset 88h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 88h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:0	0x0 RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[lb]15:0[rb]) during the data phase of the MSI memory write transaction. **Power Well:** Core

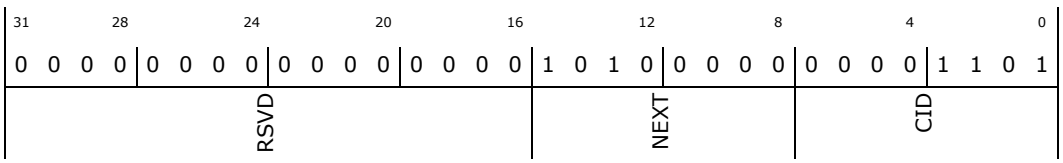
11.1.31 Subsystem Vendor Capability (SVCAP)—Offset 90h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 90h

Default: 0000A00Dh



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:8	0xa0 RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. **Power Well:** Core
7:0	0xd RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability. **Power Well:** Core

11.1.32 Subsystem Vendor IDs (SVID)—Offset 94h

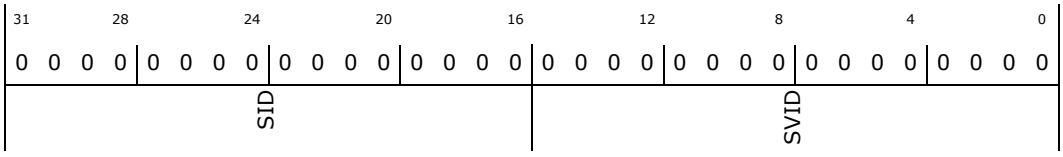
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 94h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset). **Power Well:** Core
15:0	0x0 RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset). **Power Well:** Core

11.1.33 Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h

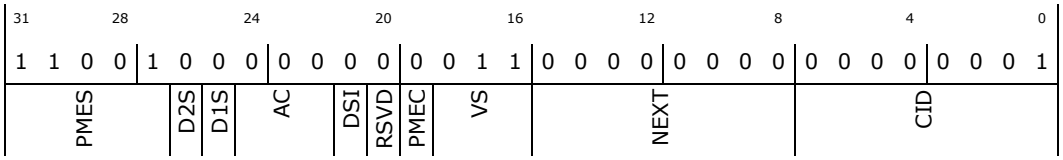
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + A0h

Default: C8030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x19 RO	**PME Support (PMES):** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy Microsoft operating systems to enable PME# in devices connected behind this root port. **Power Well:** Core
26	0x0 RO	**D2_Support (D2S):** The D2 state is not supported. **Power Well:** Core
25	0x0 RO	**D1_Support (D1S):** The D1 state is not supported. **Power Well:** Core
24:22	0x0 RO	**Aux_Current (AC):** Reports 0mA (self-powered), as use of this controller does not add to suspend well power consumption. **Power Well:** Core
21	0x0 RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required. **Power Well:** Core
20	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
19	0x0 RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#. **Power Well:** Core
18:16	0x3 RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Next Capability (NEXT):** Indicates this is the last item in the list. **Power Well:** Core
7:0	0x1 RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability. **Power Well:** Core

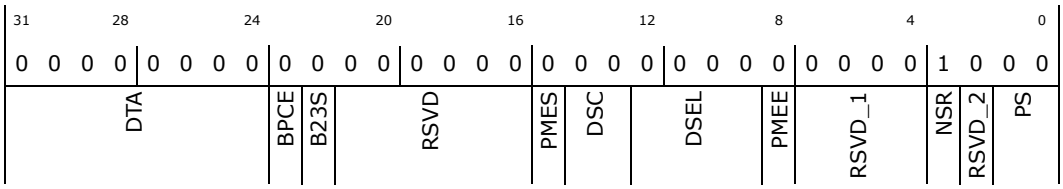
11.1.34 PCI Power Management Control And Status (PMCS)—Offset A4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + A4h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Data (DTA):** Reserved **Power Well:** Core
23	0x0 RO	**Bus Power / Clock Control Enable (BPCE):** Reserved per PCI Express specification **Power Well:** Core
22	0x0 RO	**B2/B3 Support (B23S):** Reserved per PCI Express specification. **Power Well:** Core
21:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15	0x0 RO	**PME Status (PMES):** Indicates a PME was received on the downstream link. **Power Well:** Core
14:13	0x0 RO	**Data Scale (DSC):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12:9	0x0 RO	**Data Select (DSEL):** Reserved **Power Well:** Core
8	0x0 RW/P	**PME Enable (PMEE):** Indicates PME is enabled. The root port takes no action on this bit, but it must be RW for legacy Microsoft operating systems to enable PME# on devices connected to this root port. This register resides in the resume well and is not reset on a resume from S3/S4/S5. The reset for this register is RSMRST# which is not asserted during a Warm Reset. **Power Well:** Core
7:4	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
3	0x1 RW/O	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. **Power Well:** Core
2	0x0 RO	**Reserved (RSVD_2):** Reserved. **Power Well:** Core
1:0	0x0 RW	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 - D0 state 11 - D3HOT state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a '10' or '01' to these bits, the write will be ignored. **Power Well:** Core

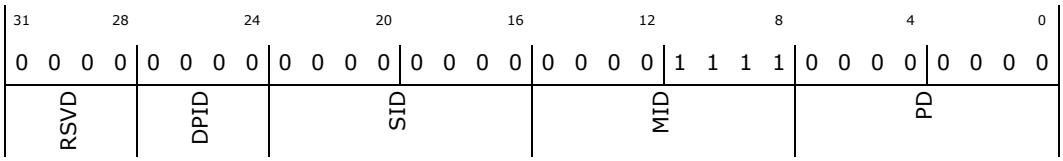
11.1.35 Manufacturer's ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + F8h

Default: 00000F00h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
27:24	0x0 RO/V	**Dot portion of Process ID (DPID):** The value of this field is SoC specific. Example: Process/Dot (PD) is 1265.8. Indicates the dot as .8. **Power Well:** Core
23:16	0x0 RO/V	**Stepping Identifier (SID):** This field is incremented for each stepping of the part. Note that this field can be used by software to differentiate steppings when the Revision ID may not change. A single Manufacturing Stepping ID can be implemented that is readable from all functions in the chip because all of them are incremented in lock-step. **Power Well:** Core
15:8	0xf RO	**Manufacturing Identifier (MID):** 0Fh = Intel **Power Well:** Core
7:0	0x0 RO/V	**Process/Dot (PD):** Indicates the current process. The value of this field is SoC specific. Example: Process/Dot (PD) is 1265.8. Indicates the Process (1265). **Power Well:** Core

11.1.36 Advanced Error Reporting Capability Header (AECH)—Offset 100h

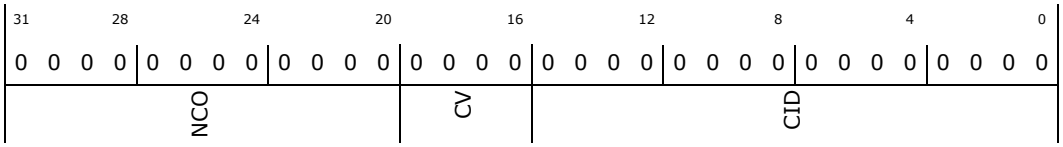
Size:32 bits The AER capability can optionally be included or excluded from the capabilities list. The full AER is supported.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 100h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW/O	**Next Capability Offset (NCO):** Set to 000h as this is the last capability in the list. **Power Well:** Core
19:16	0x0 RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0 **Power Well:** Core
15:0	0x0 RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0 **Power Well:** Core

11.1.37 Uncorrectable Error Status (UES)—Offset 104h

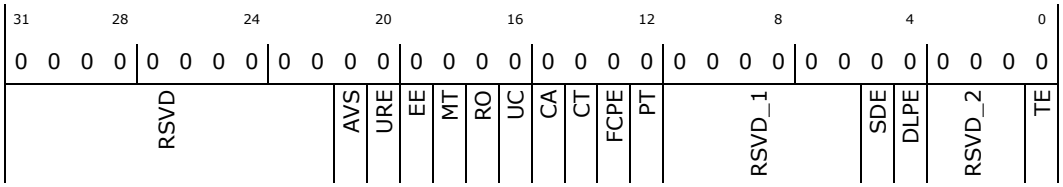
This register must maintain its state through a platform reset. It loses its state upon loss of core power.

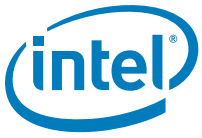
Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 104h

Default: 00000000h





Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported **Power Well:** Core
20	0x0 RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received. **Power Well:** Core
19	0x0 RO	**ECRC Error Status (EE):** ECRC is not supported. **Power Well:** Core
18	0x0 RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received. **Power Well:** Core
17	0x0 RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred. **Power Well:** Core
16	0x0 RW/1C/V/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received. **Power Well:** Core
15	0x0 RW/1C/V/P	**Completor Abort Status (CA):** Indicates a completer abort was received **Power Well:** Core
14	0x0 RW/1C/V/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value **Power Well:** Core
13	0x0 RO	**Flow Control Protocol Error Status (FCPE):** Not supported. **Power Well:** Core
12	0x0 RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received. **Power Well:** Core
11:6	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RO	**Surprise Down Error Status (SDE):** Surprise Down is not supported. **Power Well:** Core
4	0x0 RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred. **Power Well:** Core
3:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x0 RO	**Training Error Status (TE):** Not supported. **Power Well:** Core

11.1.38 Uncorrectable Error Mask (UEM)—Offset 108h

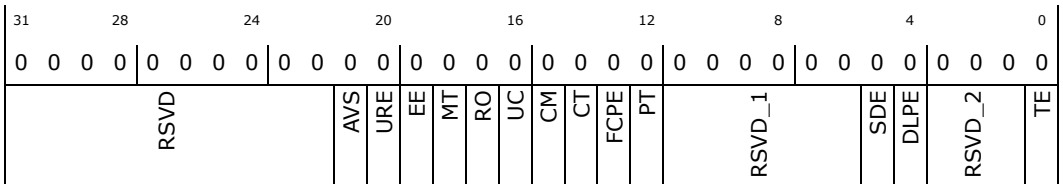
When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

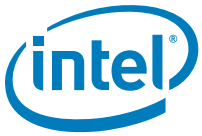
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 108h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported **Power Well:** Core
20	0x0 RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors. **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RO	**ECRC Error Mask (EE):** ECRC is not supported. **Power Well:** Core
18	0x0 RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs **Power Well:** Core
17	0x0 RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows. **Power Well:** Core
16	0x0 RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions. **Power Well:** Core
15	0x0 RW/P	**Completor Abort Mask (CM):** Mask for completer abort. **Power Well:** Core
14	0x0 RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts. **Power Well:** Core
13	0x0 RO	**Flow Control Protocol Error Mask (FCPE):** Not supported. **Power Well:** Core
12	0x0 RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs. **Power Well:** Core
11:6	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
5	0x0 RO	**Surprise Down Error Mask (SDE):** Surprise Down is not supported. **Power Well:** Core
4	0x0 RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors. **Power Well:** Core
3:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x0 RO	**Training Error Mask (TE):** Not supported. **Power Well:** Core

11.1.39 Uncorrectable Error Severity (UEV)—Offset 10Ch

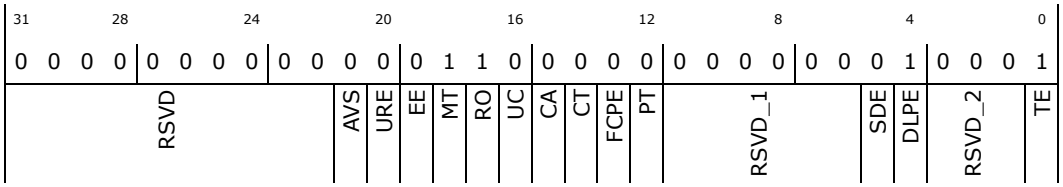
This register gives the option to make an uncorrectable error fatal or non-fatal. An error is fatal if the bit is set. An error is non-fatal if the bit is cleared. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 10Ch

Default: 00060011h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**ACS Violation Severity (AVS):** Reserved. Access Control Services are not supported **Power Well:** Core
20	0x0 RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception. **Power Well:** Core
19	0x0 RO	**ECRC Error Severity (EE):** ECRC is not supported. **Power Well:** Core
18	0x1 RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception. **Power Well:** Core
17	0x1 RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences. **Power Well:** Core
16	0x0 RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception. **Power Well:** Core
15	0x0 RW/P	**Completor Abort Severity (CA):** Severity for completer abort. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout. **Power Well:** Core
13	0x0 RO	**Flow Control Protocol Error Severity (FCPE):** Not supported. **Power Well:** Core
12	0x0 RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception. **Power Well:** Core
11:6	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
5	0x0 RO	**Surprise Down Error Severity (SDE):** Surprise Down is not supported. **Power Well:** Core
4	0x1 RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors. **Power Well:** Core
3:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x1 RO	**Training Error Severity (TE):** TE not supported. This bit is left as RO='1' for ease of implementation.. **Power Well:** Core

11.1.40 Correctable Error Status (CES)—Offset 110h

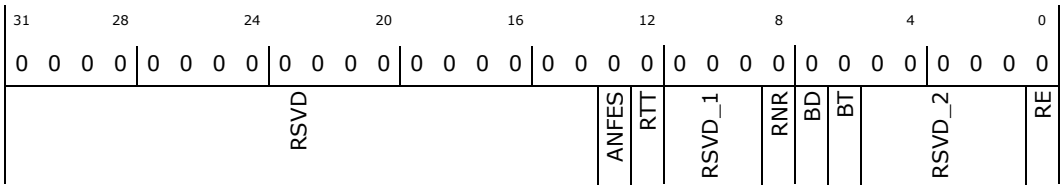
This register is only reset by a loss of core power

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 110h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
13	0x0 RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that a Advisory Non-Fatal Error occurred. **Power Well:** Core
12	0x0 RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out. **Power Well:** Core
11:9	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
8	0x0 RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over. **Power Well:** Core
7	0x0 RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received. **Power Well:** Core
6	0x0 RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received. **Power Well:** Core
5:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x0 RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred. **Power Well:** Core

11.1.41 Correctable Error Mask (CEM)—Offset 114h

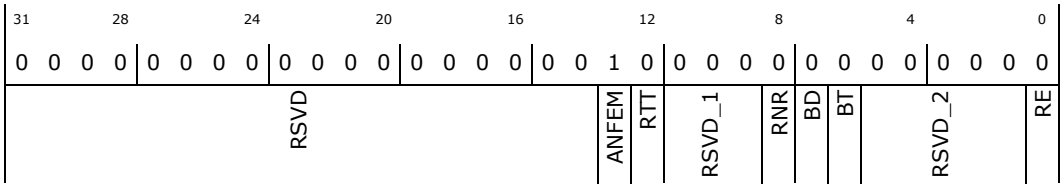
When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 114h

Default: 00002000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
13	0x1 RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting. **Power Well:** Core
12	0x0 RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout. **Power Well:** Core
11:9	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
8	0x0 RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover. **Power Well:** Core
7	0x0 RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception. **Power Well:** Core
6	0x0 RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception. **Power Well:** Core
5:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x0 RW/P	**Receiver Error Mask (RE):** Mask for receiver errors. **Power Well:** Core

11.1.42 Advanced Error Capabilities and Control (AECC)—Offset 118h

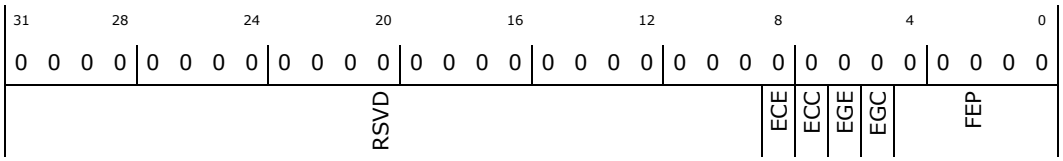
This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 118h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
8	0x0 RO	**ECRC Check Enable (ECE):** ECRC is not supported. **Power Well:** Core
7	0x0 RO	**ECRC Check Capable (ECC):** ECRC is not supported. **Power Well:** Core
6	0x0 RO	**ECRC Generation Enable (EGE):** ECRC is not supported. **Power Well:** Core
5	0x0 RO	**ECRC Generation Capable (EGC):** ECRC is not supported. **Power Well:** Core
4:0	0x0 RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register. **Power Well:** Core

11.1.43 Header Log DW1 (HL_DW1)—Offset 11Ch

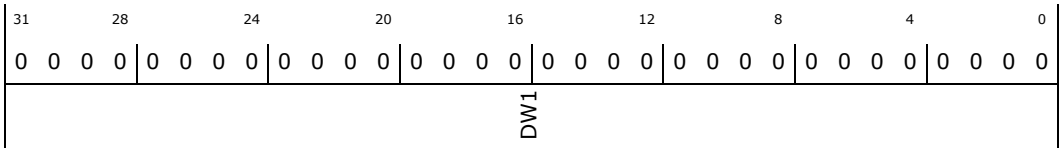
Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 11Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO/V/P	**1st dWord of TLP (DW1):** Byte0 [amp][amp] Byte1 [amp][amp] Byte2 [amp][amp] Byte3 **Power Well:** Core

11.1.44 Header Log DW2 (HL_DW2)—Offset 120h

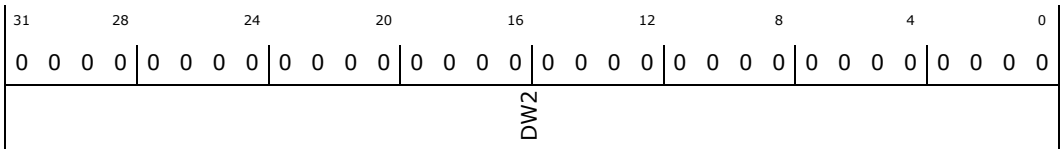
Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 120h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO/V/P	**2nd dWord of TLP (DW2):** Byte4 [amp][amp] Byte5 [amp][amp] Byte6 [amp][amp] Byte7 **Power Well:** Core

11.1.45 Header Log DW3 (HL_DW3)—Offset 124h

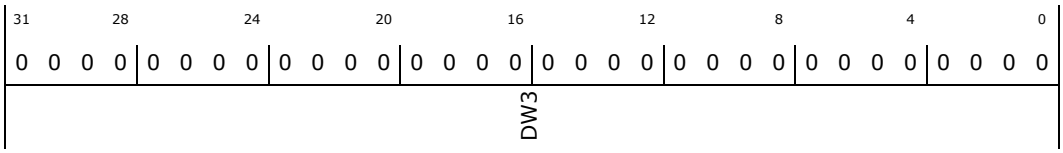
Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 124h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO/V/P	**3rd dWord of TLP (DW3):** Byte8 [amp][amp] Byte9 [amp][amp] Byte10 [amp][amp] Byte11 **Power Well:** Core

11.1.46 Header Log DW4 (HL_DW4)—Offset 128h

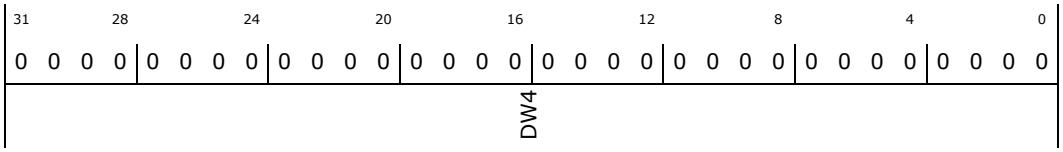
Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 128h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO/V/P	**4th dWord of TLP (DW4):** Byte12 [amp][amp] Byte13 [amp][amp] Byte14 [amp][amp] Byte15 **Power Well:** Core

11.1.47 Root Error Command (REC)—Offset 12Ch

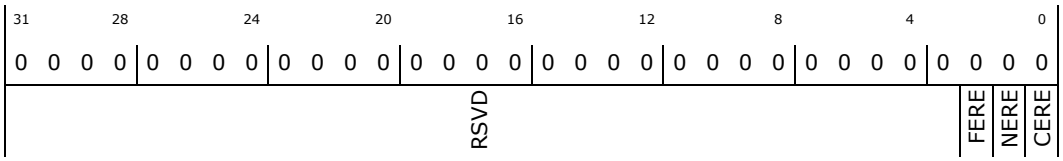
This register allows errors to generate interrupts.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 12Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
2	0x0 RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device. **Power Well:** Core
1	0x0 RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device. **Power Well:** Core
0	0x0 RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device. **Power Well:** Core

11.1.48 Root Error Status (RES)—Offset 130h

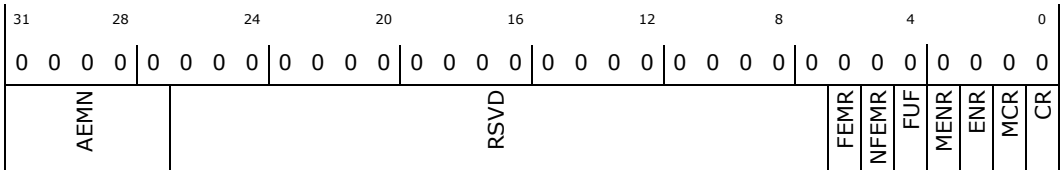
This register can track more than one error and set the [quote]multiple[/quote] bits if a second or subsequent error occurs and the first has not been serviced. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 130h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**Advanced Error Interrupt Message Number (AEMN):** Reserved. There is only one error interrupt allocated. **Power Well:** Core
26:7	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
6	0x0 RW/1C/V/P	**Fatal Error Message Received (FEMR):** Set when one or more Fatal Uncorrectable Error Messages have been received. **Power Well:** Core
5	0x0 RW/1C/V/P	**Non-Fatal Error Messages Received (NFEMR):** Set when one or more Non-Fatal Uncorrectable error messages have been received **Power Well:** Core
4	0x0 RW/1C/V/P	**First Uncorrectable Fatal (FUF):** Set when the first Uncorrectable Error message received is for a fatal error. **Power Well:** Core
3	0x0 RW/1C/V/P	**Multiple ERR_FATAL/NONFATAL Received (MENR):** Set when either a fatal or a non-fatal error is received and the ENR bit is already set. **Power Well:** Core
2	0x0 RW/1C/V/P	**ERR_FATAL/NONFATAL Received (ENR):** Set when either a fatal or a non-fatal error message is received. **Power Well:** Core
1	0x0 RW/1C/V/P	**Multiple ERR_COR Received (MCR):** Set when a correctable error message is received and the CR bit is already set. **Power Well:** Core
0	0x0 RW/1C/V/P	**ERR_COR Received (CR):** Set when a correctable error message is received. **Power Well:** Core

11.1.49 Error Source Identification (ESID)—Offset 134h

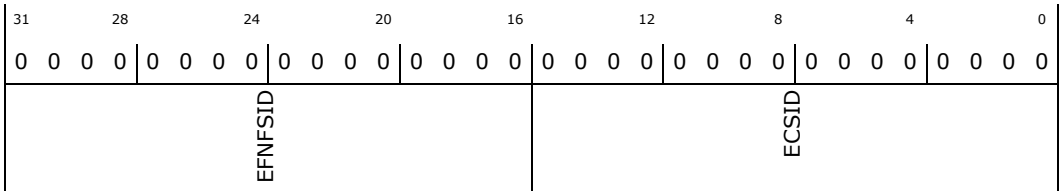
Size:32 bits Identifies the source (Requester ID) of the first correctable and uncorrectable (Non-Fatal / Fatal) errors reported in the Root Error Status register. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 134h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message with the ERR_FATAL/NONFATAL Received register is not already set. **Power Well:** Core
15:0	0x0 RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the Requester ID indicated in the received ERR_COR Message with the ERR_COR Received register is not already set. **Power Well:** Core

11.1.50 L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h

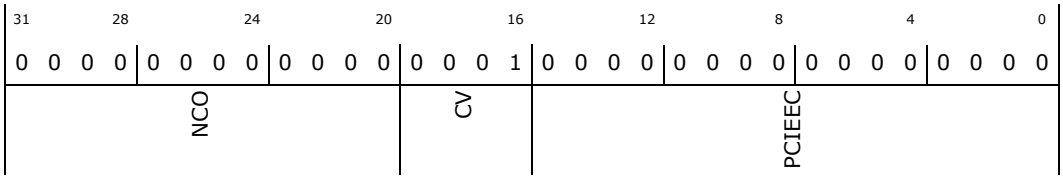
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 200h

Default: 00010000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits. **Power Well:** Core
19:16	0x1 RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW/O	**PCI Express Extended Capability ID (PCIEEC):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for L1 Substates is [lt]TBD[gt]. **Power Well:** Core

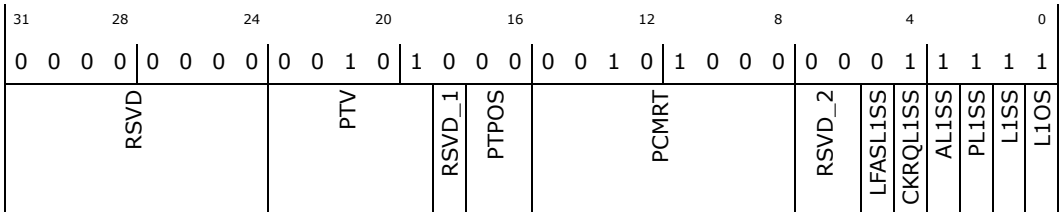
11.1.51 L1 Sub-States Capabilities (L1SCAP)—Offset 204h

Access Method

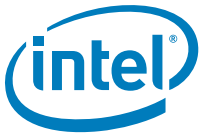
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 204h

Default: 0028281Fh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
23:19	0x5 RW/O	**Port Tpower_on Value (PTV):** Along with the Port T_POWER_ON Scale Field in the L1 Substates Capabilities register sets theTime (in us) that this Port requires the port on the opposite side of Link to wait in L1.OFF_EXIT after sampling CLKREQ# asserted before actively driving the interface. Port Tpower_on is calculated by multiplying the value in this field by the value in the Port Tpower_on scale field in the L1 Sub-States Capabilities 2 register. Required for all Ports that support L1.OFF. **Power Well:** Core
18	0x0 RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
17:16	0x0 RW/O	**Port Tpower_on Scale (PTPOS):** Specifies the scale used for Tpower_on value field in the L1 Substates Capabilities register. [quote]00b[/quote]: 2 us [quote]01b[/quote]: 10 us [quote]10b[/quote]: 100 us [quote]11b[/quote]: Reserved Required for all Ports that support L1.OFF. **Power Well:** Core
15:8	0x28 RW/O	**Port Common Mode Restore Time (PCMRT):** This is the time (in us) required for this Port to re-establish common mode. Required for all ports that support L1.OFF. **Power Well:** Core
7:6	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
5	0x0 RO	**LFAS L1 Substates Supported (LFASL1SS):** When Set this bit indicates that this Port supports the LFAS mechanism. Required for both Upstream and Downstream Ports. **Power Well:** Core
4	0x1 RO	**CLKREQ# L1 Substates Supported (CKRQL1SS):** When Set this bit indicates that this Port supports the CLKREQ# out-of-band wake mechanism. Required for both Upstream and Downstream Ports. **Power Well:** Core
3	0x1 RW/O	**ASPM L1 Substates Supported (AL1SS):** When set, this bit indicates that this port supports L1 substates for ASPM L1. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static **Power Well:** Core
2	0x1 RW/O	**PCI-PM L1 Substates Supported (PL1SS):** When set, this bit indicates that this port supports L1 substates for PCI-PM. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1	0x1 RW/O	**L1.SNOOZ Supported (L1SS):** When set, this bit indicates that L1.SNOOZ sub-state is supported and this bit must be set by all ports implementing L1 Sub-States. A port that supports L1.OFF must support L1.SNOOZ. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static **Power Well:** Core
0	0x1 RW/O	**L1.OFF Supported (L1OS):** When set, this bit indicates that L1.OFF power management feature is supported. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static **Power Well:** Core

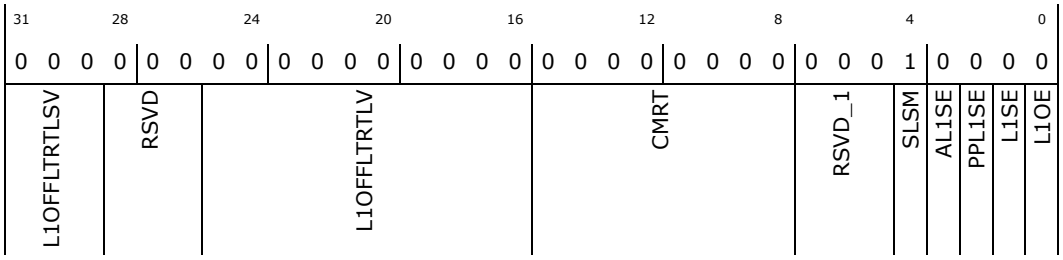
11.1.52 L1 Sub-States Control 1 (L1SCTL1)—Offset 208h

Access Method

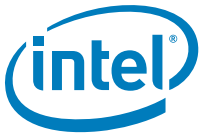
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 208h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**L1.OFF LTR Threshold Latency ScaleValue (L1OFFLTRTLSV):** This field contains the L1.OFF LTR Threshold Latency Scale Value for this particular PCIe root port. The value in this field, together with L1OFFLTRTLV is compared against both the snoop and non-snoop LTR values of the device. 000: L1OFFLTRSTLV times 1 ns 001: L1OFFLTRSTLV times 32 ns 010: L1OFFLTRSTLV times 1024 ns 011: L1OFFLTRSTLV times 32768 ns 100: L1OFFLTRSTLV times 1048576 ns 101: L1OFFLTRSTLV times 33554432 ns Others: Not Permitted. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
28:26	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
25:16	0x0 RW	**L1.OFF LTR Threshold Latency Value (L1OFFLTRTLV):** This field contains the L1.OFF LTR Threshold Latency Value for this particular PCIe root port. The value in this field, together with L1OFFLTRTLSV is compared against both the snoop and non-snoop LTR values of the device. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static **Power Well:** Core
15:8	0x0 RW	**Common Mode Restore Time (CMRT):** This is the Tcommon_mode time the PCIe root port needs to continue sending TS1 and refrain from sending TS2 in Recovery state to allow the TX common mode to be established prior to sending TS2. The timer starts from the time when the first TS1 has been sent and the receiver has detected un-squelch. The value in this field defines the time in micro-seconds. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static **Power Well:** Core
7:5	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
4	0x1 RO	**Select L1 Substates Mechanism (SLSM):** When Set this bit indicates that this Port must use the CLKREQ#-based mechanism, when Clear the LFAS mechanism must be used. Ports that support only one mechanism for L1 Substates are permitted to implement this bit as RO/HwInit, and the value of this bit must reflect the supported mechanism. Default value is implementation-specific. **Power Well:** Core
3	0x0 RW	**ASPM L1 Substates Enabled (AL1SE):** When set, this bit indicates that L1 substates are enabled for ASPM. Required for both upstream and downstream ports. Register Attribute: Dynamic **Power Well:** Core
2	0x0 RW	**PCI-PM L1 Substates Enabled (PPL1SE):** When set, this bit indicates that L1 substates are enabled for PCI-PM. Required for both upstream and downstream ports. Register Attribute: Dynamic **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**L1.SNOOZ Enable (L1SE):** When set, this bit indicates that L1.SNOOZ power management feature is enabled. If L1.OFF is enabled, L1.SNOOZ must also be enabled. This field must be programmed prior to enabling ASPM L1. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. **Power Well:** Core
0	0x0 RW	**L1.OFF Enable (L1OE):** When set, this bit indicates that L1.OFF power management feature is enabled. L1.OFF can only be enabled if the platform supports bi-directional CLKREQPLUS#. This field must be programmed prior to enabling ASPM L1. Ports that support L1.OFF shall support Latency Tolerance Reporting. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. **Power Well:** Core

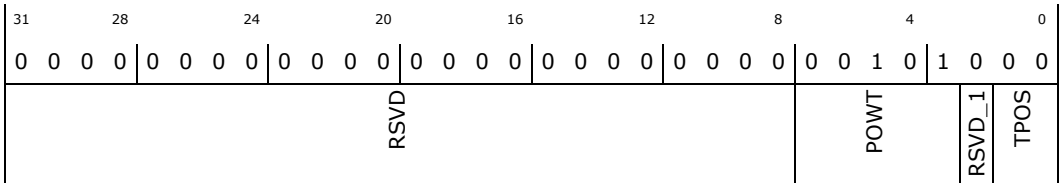
11.1.53 L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 20Ch

Default: 00000028h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
7:3	0x5 RW	**Power On Wait Time (POWT):** Along with the Tpower_on Scale sets the minimum amount of time (in us) that the Port must wait in L1.OFF EXIT after sampling CLKREQPLUS# asserted before actively driving the interface. The timer starts counting when CLKREQPLUS# asserts in L1.OFF state. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
1:0	0x0 RW	**Tpower_on Scale (TPOS):** Specifies the scale used for Tpower_on value. '00b': 2 us '01b': 10 us '10b': 100us '11b': Reserved. Required for all Ports that support L1.OFF. Register Attribute: Static **Power Well:** Core

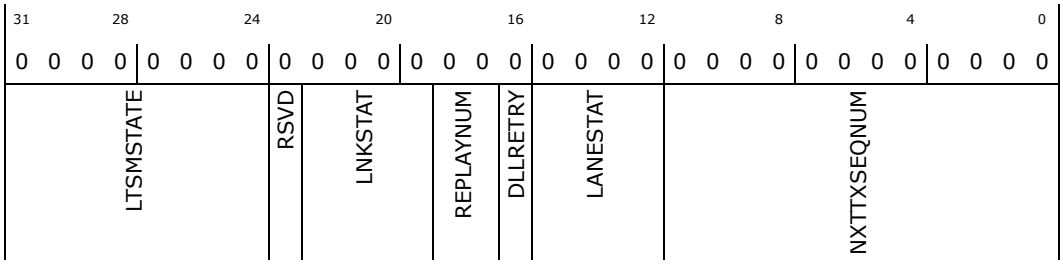
11.1.54 PCI Express Status 1 (PCIESTS1)—Offset 328h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

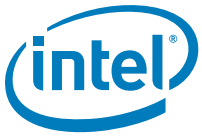
Offset: [B:0, D:28, F:0] + 328h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO/V	**LTSM State (LTSMSTATE):** Indicates the LTSM present state. Hex LTSSM States 00DETIDLE 01DETRDY 02DETIDLEP1TOP2 03DETRDYP2TOP1 04DETRDYINP1 05DETRDYINP1EXE 06DETP2POLLSTART 07DETP1POLLSTART 08DETP2TOP0 09DETP1TOP0 0AECPCMPRETRAIN 0BECPCMFAILP0TOP2 0C DETP0TOP2 0D PMODECHANGE 0EECPCMPCIE 0FECPCMUSB3

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO/V	10DET2POLLINP0 11POLLINGACTIVE 12POLLINGCOMPLIANCEMARGINCNT 13POLLINGCOMPLIANCE 14POLLINGCOMPLIANCESPEEDUP 15POLLINGCOMPLIANCESPEEDDN 16POLLINGCOMPLIANCESPEEDTXEIDLE 17POLLINGCOMPLIANCESPEEDRXEIDLE 18POLLINGCOMPLIANCESPEED 19POLLINGCOMPLIANCESPEEDDONE 1APOLLINGCOMPLIANCEEXIT 1BPOLLINGCONFIGURATION 1C POLLINGTXEIDLE 1D POLLINGEND 1EPOLLINGENDWAIT 1FLINKWIDTHSTART 20LINKWIDTHACCEPT 21LANENUMWAIT 22LANENUMACCEPT 23LANEDESKEW 24CONFIGCOMPLETE 25CONFIGIDLE 26LWNEXITRECOVERY 27CONFIGLPBKENTRY 28CONFIGLPBKLWSTART 29CONFIGLPBKSPEEDTXEIDLE 2ACONFIGLPBKSPEEDSTART 2BCONFIGLPBKSPEEDRXEIDLE 2C CONFIGLPBKSPEED 2D CONFIGLPBKREUTSKIP 2ECONFIGLPBKREUT 2FCONFIGLPBKEXITM 30CONFIGLPBKTXEIDLE 31LWNEXIT 32LWNLNK2DETECT 33L0 34TXL0SRXL0 35RXL0STXL0 36TXL0SRXL0S 37L1TXEIDLE 38L1RCVEIDLE 39L1PREENTRY 3AL1ENTRY 3BL1IDLE 3C L1IDLEGEN2WAIT 3D L1EXIT 3EL2TXEIDLE 3FL2RCVEIDLE 40L2IDLEWAIT 41L2IDLERDY 42L2IDLE 43LOOPBACKENTRY 44LPBKACTIVEMTXSKP 45LPBKACTIVEMSKPDSKW



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO/V	46LOOPBACKACTIVEM 47LPBKSLAVESPEEDTXEIDLE 48LPBKSLAVESPEEDRXEIDLE 49LPBKSLAVESPEED 4ALOOPBACKACTIVES 4BLOOPBACKCMMSKP 4C LOOPBACKCMM 4D LOOPBACKEXITM 4ELOOPBACKEXITS 4FLOOPBACKEXITL0 50LOOPBACKLNK2DETECT 51LOOPBACK2DETECT 52DISTX16TS1DIS 53DISTXEIDLE 54DISWAITSTART 55DISWAITGNT 56DISWAIT4TXMARGIN 57DISWAIT 58DIS2DETECT 59HOTRESETTS1 5AHOTRESETDONE 5BHOTRESETEIDLE 5C RECOVERYRCVRWAIT 5D RECOVERYRCVRMARGINCNT 5ERECOVERYRCVRLOCK 5FRECOVERYDESKEW 60RECOVERYRCVRCFG 61RECOVERYSPEED 62RECOVERYSPEEDTXEIDLE 63RECOVERYSPEEDRXEIDLE 64RECOVERYSPEEDREADY 65RECOVERYIDLE 66RECOVERYEXITDETECT 67RECOVERYLNK2DETECT 68RECOVERYEXITLPBK 69RECOVERYEXITL0 6ARECOVERYEXITDIS 6BRECOVERYEXITRST Note: This register field could be used by REUT software to monitor the link LTSSM substates. **Power Well:** Core
23	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
22:19	0x0 RO/V	**Link Status (LNKSTAT):** During Link initialization the Link will always traverse this list of state from the top (0000) to the bottom of the list (0111). One or more power management states may be skipped, but the direction of list traversal will remain the same. 0000 Link Down 0001 : Link Retrain 0011 : L1 0100 : L2 0101 : L3 0111 : L0 (Link Up) 1000 : L0s (Transmit [amp] Receive) 1001 : L0s (Transmit only) 1010 : L0s (Receive only) All others reserved **Power Well:** Core
18:17	0x0 RO/V	**Replay Number (REPLAYNUM):** Number of times the Retry Buffer has been replayed since the last Link initialization / re-training. When the Data Link Layer has replayed the contents of the Retry Buffer four times a Link re-training will be initiated which will reset this value back to zero. **Power Well:** Core
16	0x0 RO/V	**Data Link Layer Retry (DLLRETRY):** Indicates when the Data Link Layer has received a corrupted TLP or has detected a dropped packet and is currently waiting for the remote agent to re-transmit the corrupted/dropped packet. The value of Next Receive Sequence Number will be the sequence number associated with the corrupted packet. **Power Well:** Core
15:12	0x0 RO/V	**Lane Status (LANESTAT):** Indicates which lanes are trained. A '1' indicates that the corresponding lane is trained (i.e. bit 0 = '1' means lane 0 is trained). **Power Well:** Core
11:0	0x0 RO/V	**Next Transmitted Sequence Number (NXTTXSEQNUM):** This is the sequence number to be applied to and pre-pended to the next outgoing TLP. **Power Well:** Core

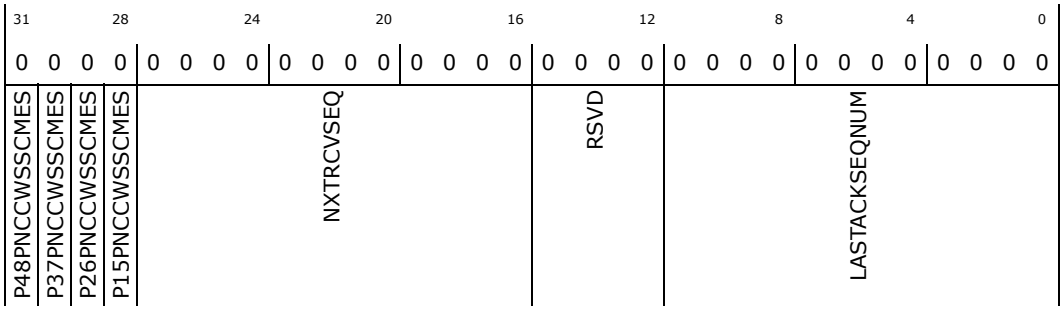
11.1.55 PCI Express Status 2 (PCIESTS2)—Offset 32Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 32Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO/V	**PCIe Port 4 Non-Common Clock With SSC Mode Enable Strap (P48PNCCWSSCMES):** '0': PCIe port 4 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 4 is enabled to operate in non-common clock mode with SSC enabled. **Power Well:** Core
30	0x0 RO/V	**PCIe Port 3 Non-Common Clock With SSC Mode Enable Strap (P37PNCCWSSCMES):** '0': PCIe port 3 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 3 is enabled to operate in non-common clock mode with SSC enabled. **Power Well:** Core
29	0x0 RO/V	**PCIe Port 2 Non-Common Clock With SSC Mode Enable Strap (P26PNCCWSSCMES):** '0': PCIe port 2 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 2 is enabled to operate in non-common clock mode with SSC enabled. **Power Well:** Core
28	0x0 RO/V	**PCIe Port 1 Non-Common Clock With SSC Mode Enable Strap (P15PNCCWSSCMES):** '0': PCIe port 1 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 1 is enabled to operate in non-common clock mode with SSC enabled. **Power Well:** Core
27:16	0x0 RO/V	**Next Receive Sequence Number (NXTRCVSEQ):** This is the sequence number associated with the TLP that is expected to be received next. **Power Well:** Core
15:12	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11:0	0x0 RO/V	**Last Acknowledged Sequence Number (LASTACKSEQNUM):** This is the sequence number associated with the last acknowledged TLP. **Power Well:** Core

11.1.56 PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h

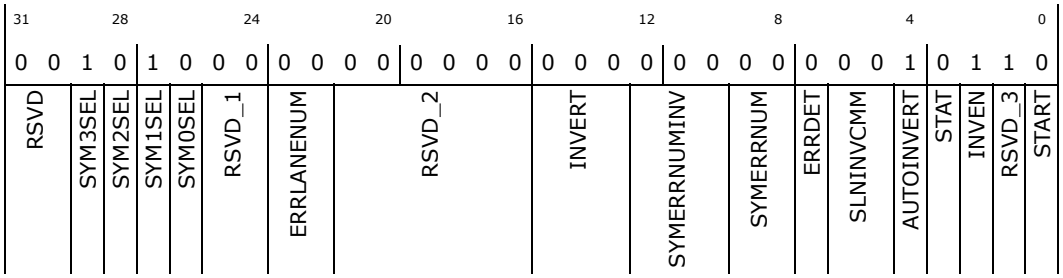
Note that selecting a lane number that does not exist for a port may result in undefined behavior.

Access Method

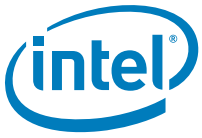
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 330h

Default: 28000016h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
29	0x1 RW	**CMM Symbol[3] Select (SYM3SEL):** 0: selects CMM Symbol [lb]3[rb] to a control character 1: selects CMM Symbol [lb]3[rb] as a data character **Power Well:** Core
28	0x0 RW	**CMM Symbol[2] Select (SYM2SEL):** 0: selects CMM Symbol [lb]2[rb] to a control character 1: selects CMM Symbol [lb]2[rb] as a data character **Power Well:** Core
27	0x1 RW	**CMM Symbol[1] Select (SYM1SEL):** 0: selects CMM Symbol [lb]1[rb] to a control character 1: selects CMM Symbol [lb]1[rb] as a data character **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
26	0x0 RW	**CMM Symbol[0] Select (SYM0SEL):** 0: selects CMM Symbol [lb]0[rb] to a control character 1: selects CMM Symbol [lb]0[rb] as a data character **Power Well:** Core
25:24	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
23:22	0x0 RO/V	**CMM Error Lane Number (ERRLANENUM):** This field contains the lane number of the failing lane. Only valid when CMM Error Detected is 1. **Power Well:** Core
21:16	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
15:13	0x0 RO/V	**CMM Invert (INVERT):** Indicates which lanes are inverted 000: No inversion 001: Lanes 0 010: Lanes 1 011: Lanes 2 100: Lanes 3 This field is only valid when CMM Error Detected (bit 7) is asserted. Additionally, when CMM Error Detected is asserted this field is locked (will not be updated) **Power Well:** Core
12:10	0x0 RO/V	**CMM Symbol Error Number Invert (SYMERRNUMINV):** Indicates which register number miscompared on the failing lane, if the failing lane was an inverted lane. Only valid when CMM Error Detected is 1. 000: CMM Data D0 001: CMM Data D0 010: CMM Data D0 011: CMM Data D1 100: CMM Data D2 101: CMM Data D3 110: CMM Data D0 111: CMM Data D0 **Power Well:** Core
9:8	0x0 RO/V	**CMM Symbol Error Number (SYMERRNUM):** Indicates which register number miscompared on the failing lane, if the failing lane was not inverted. Only valid when CMM Error Detected is 1. 00: CMM Data 0 01: CMM Data 1 10: CMM Data 2 11: CMM Data 3 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW/1C/V	**CMM Error Detected (ERRDET):** 1: An error was detected 0: No error detected Note: This bit will be shadowed to an observability pin that can be used for IRQ generation. **Power Well:** Core
6:5	0x0 RW	**Select Lane Number to be inverted for CMM (SLNINVCMM):** Select Lane Number to be inverted for CMM **Power Well:** Core
4	0x1 RW	**CMM AutoInvert (AUTOINVERT):** 1: CMM autosequences through the inversion 0: CMM does not sequence inversion **Power Well:** Core
3	0x0 RO/V	**CMM Status (STAT):** This bit is set when the CMM Start bit is set and cleared when the CMM mode has been entered successfully. 0: Compliance Measurement Mode is not active or CMM mode has been entered successfully. 1: Set as a result of CMM Start bit being set. **Power Well:** Core
2	0x1 RW	**CMM Invert Enable (INVEN):** 1: Enables the Inversion of the lane 0: Lane not inverted **Power Well:** Core
1	0x1 RW	**Reserved (RSVD_3):** Reserved. **Power Well:** Core
0	0x0 RW/L	**CMM Start (START):** 1: Start CMM 0: Stop CMM This register bit is Read-Only when the MPC.SRL bit is set. **Power Well:** Core

11.1.57 PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h

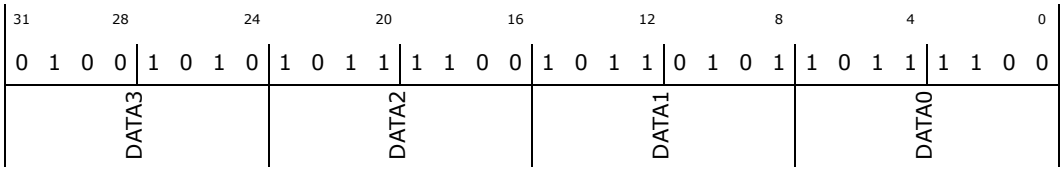
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 334h

Default: 4ABCB5BCh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x4a RW	**CMM Data [3] (DATA3):** This character contains CMM Data [lb]3[rb] that will be transmitted on the link. **Power Well:** Core
23:16	0xbc RW	**CMM Data [2] (DATA2):** This character contains CMM Data [lb]2[rb] that will be transmitted on the link. **Power Well:** Core
15:8	0xb5 RW	**CMM Data [1] (DATA1):** This character contains CMM Data [lb]1[rb] that will be transmitted on the link. **Power Well:** Core
7:0	0xbc RW	**CMM Data [0] (DATA0):** This character contains CMM Data [lb]0[rb] that will be transmitted on the link. **Power Well:** Core

11.1.58 Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h

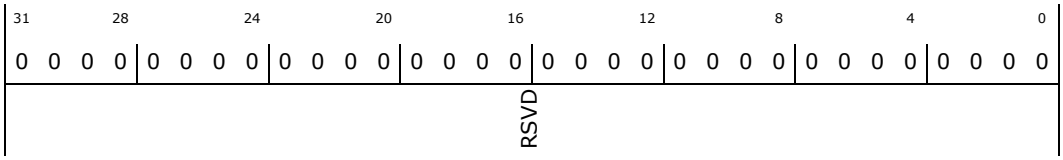
Size:32 bits

Access Method

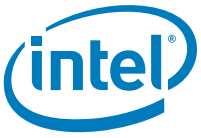
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:0] + 414h

Default: 00000000h



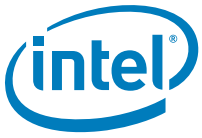
Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core



11.2 PCI Express* Lane 1 PCI Configuration Registers

Table 117. Summary of PCI Express* Lane 1 PCI Configuration Registers—0/28/1

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Identifiers (ID)—Offset 0h" on page 5951	00008086h
4–7h	4	"Device Command; Primary Status (CMD_PSTS)—Offset 4h" on page 5951	00100000h
8–Bh	4	"Revision ID;Class Code (RID_CC)—Offset 8h" on page 5954	06040000h
C–Fh	4	"Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch" on page 5955	00810000h
18–1Bh	4	"Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h" on page 5956	00000000h
1C–1Fh	4	"I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch" on page 5956	00000000h
20–23h	4	"Memory Base and Limit (MBL)—Offset 20h" on page 5958	00000000h
24–27h	4	"Prefetchable Memory Base and Limit (PMBL)—Offset 24h" on page 5959	00010001h
28–2Bh	4	"Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h" on page 5960	00000000h
2C–2Fh	4	"Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch" on page 5960	00000000h
34–37h	4	"Capabilities List Pointer (CAPP)—Offset 34h" on page 5961	00000040h
3C–3Fh	4	"Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch" on page 5961	00000000h
40–43h	4	"Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h" on page 5963	00428010h
44–47h	4	"Device Capabilities (DCAP)—Offset 44h" on page 5964	00008000h
48–4Bh	4	"Device Control; Device Status (DCTL_DSTS)—Offset 48h" on page 5966	00100000h
4C–4Fh	4	"Link Capabilities (LCAP)—Offset 4Ch" on page 5969	00310C02h
50–53h	4	"Link Control; Link Status (LCTL_LSTS)—Offset 50h" on page 5971	00010000h
54–57h	4	"Slot Capabilities (SLCAP)—Offset 54h" on page 5974	00040060h
58–5Bh	4	"Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h" on page 5976	00000000h
5C–5Fh	4	"Root Control (RCTL)—Offset 5Ch" on page 5979	00000000h
60–63h	4	"Root Status (RSTS)—Offset 60h" on page 5980	00000000h
64–67h	4	"Device Capabilities 2 (DCAP2)—Offset 64h" on page 5980	00080817h
68–6Bh	4	"Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h" on page 5982	00000000h
6C–6Fh	4	"Link Capabilities 2 (LCAP2)—Offset 6Ch" on page 5984	00000000h
70–73h	4	"Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h" on page 5985	00000000h
74–77h	4	"Slot Capabilities 2 (SLCAP2)—Offset 74h" on page 5987	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
78–7Bh	4	"Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h" on page 5988	00000000h
80–83h	4	"Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h" on page 5988	00009005h
84–87h	4	"Message Signaled Interrupt Message Address (MA)—Offset 84h" on page 5989	00000000h
88–8Bh	4	"Message Signaled Interrupt Message Data (MD)—Offset 88h" on page 5990	00000000h
90–93h	4	"Subsystem Vendor Capability (SVCAP)—Offset 90h" on page 5990	0000A00Dh
94–97h	4	"Subsystem Vendor IDs (SVID)—Offset 94h" on page 5991	00000000h
A0–A3h	4	"Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h" on page 5992	C8030001h
A4–A7h	4	"PCI Power Management Control And Status (PMCS)—Offset A4h" on page 5993	00000008h
F8–FBh	4	"Manufacturer's ID (MANID)—Offset F8h" on page 5995	00000F00h
100–103h	4	"Advanced Error Reporting Capability Header (AECH)—Offset 100h" on page 5996	00000000h
104–107h	4	"Uncorrectable Error Status (UES)—Offset 104h" on page 5996	00000000h
108–10Bh	4	"Uncorrectable Error Mask (UEM)—Offset 108h" on page 5998	00000000h
10C–10Fh	4	"Uncorrectable Error Severity (UEV)—Offset 10Ch" on page 6000	00060011h
110–113h	4	"Correctable Error Status (CES)—Offset 110h" on page 6001	00000000h
114–117h	4	"Correctable Error Mask (CEM)—Offset 114h" on page 6002	00002000h
118–11Bh	4	"Advanced Error Capabilities and Control (AECC)—Offset 118h" on page 6003	00000000h
11C–11Fh	4	"Header Log DW1 (HL_DW1)—Offset 11Ch" on page 6004	00000000h
120–123h	4	"Header Log DW2 (HL_DW2)—Offset 120h" on page 6005	00000000h
124–127h	4	"Header Log DW3 (HL_DW3)—Offset 124h" on page 6005	00000000h
128–12Bh	4	"Header Log DW4 (HL_DW4)—Offset 128h" on page 6006	00000000h
12C–12Fh	4	"Root Error Command (REC)—Offset 12Ch" on page 6006	00000000h
130–133h	4	"Root Error Status (RES)—Offset 130h" on page 6007	00000000h
134–137h	4	"Error Source Identification (ESID)—Offset 134h" on page 6008	00000000h
200–203h	4	"L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h" on page 6009	00010000h
204–207h	4	"L1 Sub-States Capabilities (L1SCAP)—Offset 204h" on page 6010	0028281Fh
208–20Bh	4	"L1 Sub-States Control 1 (L1SCTL1)—Offset 208h" on page 6012	00000010h
20C–20Fh	4	"L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch" on page 6014	00000028h
328–32Bh	4	"PCI Express Status 1 (PCIESTS1)—Offset 328h" on page 6015	00000000h
32C–32Fh	4	"PCI Express Status 2 (PCIESTS2)—Offset 32Ch" on page 6018	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
330–333h	4	"PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h" on page 6019	28000016h
334–337h	4	"PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h" on page 6022	4ABCB5BCh
414–417h	4	"Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h" on page 6023	00000000h

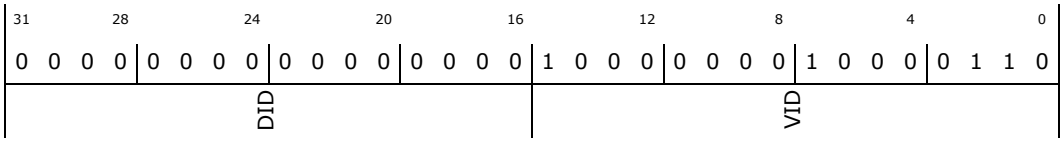
11.2.1 Identifiers (ID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO/V	**Device Identification (DID):** The value of this ID is product specific. **Power Well:** Core
15:0	0x8086 RO	**Vendor Identification (VID):** Indicates Intel **Power Well:** Core

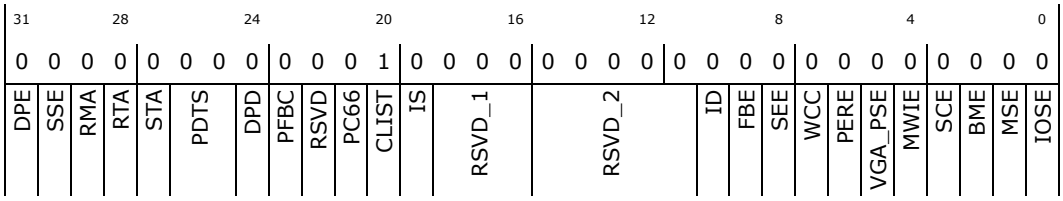
11.2.2 Device Command; Primary Status (CMD_PSTS)—Offset 4h

Access Method

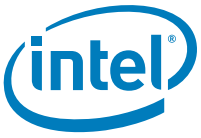
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C/V	**DPE - Detected Parity Error (DPE):** Set when the root port receives a command or data from the backbone with a parity error. This is set even if CMD.PERE is not set. **Power Well:** Core
30	0x0 RW/1C/V	**Signaled System Error (SSE):** Set when the root port signals a system error to the internal SERR# logic. **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
29	0x0 RW/1C/V	**Received Master Abort (RMA):** Set when the root port receives a completion with unsupported request status from the backbone. **Power Well:** Core
28	0x0 RW/1C/V	**Received Target Abort (RTA):** Set when the root port receives a completion with completer abort from the backbone. **Power Well:** Core
27	0x0 RW/1C/V	**Signaled Target Abort (STA):** Set whenever the root port forwards a target abort received from the downstream device onto the backbone. **Power Well:** Core
26:25	0x0 RO	**Primary DEVSEL# Timing Status (PDTS):** Reserved per PCI-Express spec **Power Well:** Core
24	0x0 RW/1C/V	**Master Data Parity Error Detected (DPD):** Set when the root port receives a completion with a data parity error on the backbone and CMD.PERE is set. **Power Well:** Core
23	0x0 RO	**Primary Fast Back to Back Capable (PFBC):** Reserved per PCI-Express spec. **Power Well:** Core
22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**Primary 66 MHz Capable (PC66):** Reserved per PCI-Express spec. **Power Well:** Core
20	0x1 RO	**Capabilities List (CLIST):** Indicates the presence of a capabilities list. **Power Well:** Core
19	0x0 RO/V	**Interrupt Status (IS):** Indicates status of hot plug and power management interrupts on the root port that result in INTx# message generation. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of CMD.ID. **Power Well:** Core
18:16	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:11	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
10	0x0 RW/V2	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above. **Power Well:** Core
9	0x0 RO	**Fast Back to Back Enable (FBE):** Reserved per PCI-Express spec. **Power Well:** Core
8	0x0 RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set. **Power Well:** Core
7	0x0 RO	**Wait Cycle Control (WCC):** Reserved per PCI-Express spec. **Power Well:** Core
6	0x0 RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a master on the backbone. **Power Well:** Core
4	0x0 RO	**Memory Write and Invalidate Enable (MWIE):** Reserved per PCI-Express spec. **Power Well:** Core
3	0x0 RO	**Special Cycle Enable (SCE):** Reserved per PCI-Express and PCI bridge spec. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**Bus Master Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit. **Power Well:** Core
1	0x0 RW	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone. **Power Well:** Core
0	0x0 RW	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone. **Power Well:** Core

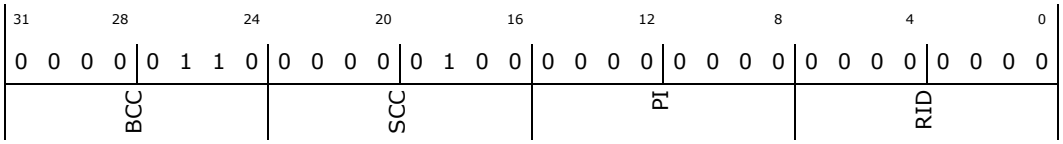
11.2.3 Revision ID;Class Code (RID_CC)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 8h

Default: 06040000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x6 RO	**Base Class Code (BCC):** Indicates the device is a bridge device. **Power Well:** Core
23:16	0x4 RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO/V	**Programming Interface (PI):** The value reported in this register is a function of the Decode Control.Subtractive Decode Enable (SDE) register. SDE Value reported in this register 0: 00h 1: 01h **Power Well:** Core
7:0	0x0 RO/V	**Revision ID (RID):** Indicates the revision of the bridge. **Power Well:** Core

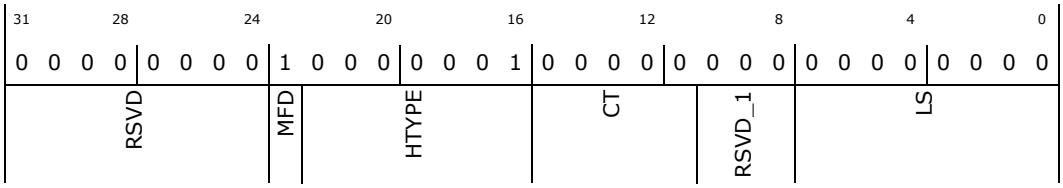
11.2.4 Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + Ch

Default: 00810000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
23	0x1 RO	**Multi-function Device (MFD):** This bit is '1' to indicate a multi-function device. **Power Well:** Core
22:16	0x1 RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h. **Power Well:** Core
15:11	0x0 RO	**Latency Count (CT):** Reserved per PCI-Express spec **Power Well:** Core
10:8	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**Line Size (LS):** This is read/write but contains no functionality, per PCI-Express spec **Power Well:** Core

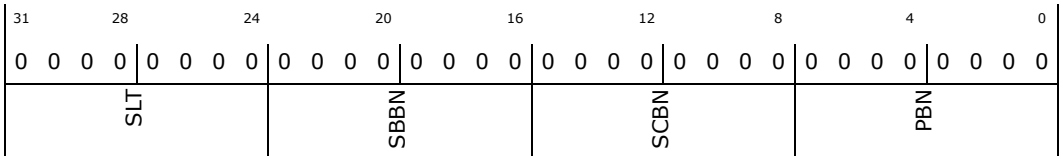
11.2.5 Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 18h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW/V2	**Secondary Latency Timer (SLT):** For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is a RW register; else this register is RO and returns 0. This register does not affect the behavior of any HW logic. **Power Well:** Core
23:16	0x0 RW	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge. **Power Well:** Core
15:8	0x0 RW	**Secondary Bus Number (SCBN):** Indicates the bus number the port. **Power Well:** Core
7:0	0x0 RW	**Primary Bus Number (PBN):** Indicates the bus number of the backbone. **Power Well:** Core

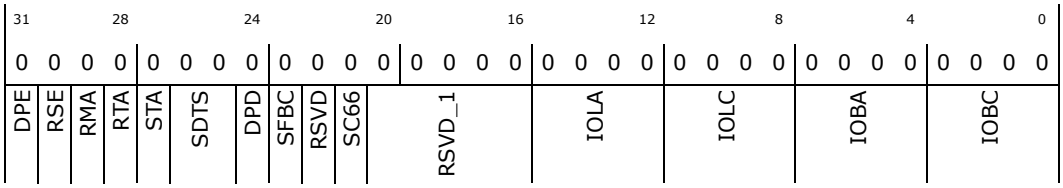
11.2.6 I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 1Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C/V	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP. **Power Well:** Core
30	0x0 RW/1C/V	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device. **Power Well:** Core
29	0x0 RW/1C/V	**Received Master Abort (RMA):** Set when the port receives a completion with [quote]Unsupported Request[/quote] status from the device. **Power Well:** Core
28	0x0 RW/1C/V	**Received Target Abort (RTA):** Set when the port receives a completion with [quote]Completion Abort[/quote] status from the device. **Power Well:** Core
27	0x0 RW/1C/V	**Signaled Target Abort (STA):** Set when the port generates a completion with [quote]Completion Abort[/quote] status to the device. **Power Well:** Core
26:25	0x0 RO/V	**Secondary DEVSEL# Timing Status (SDTS):** Reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b. **Power Well:** Core
24	0x0 RW/1C/V	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side. **Power Well:** Core
23	0x0 RO/V	**Secondary Fast Back to Back Capable (SFBC):** Reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**Secondary 66 MHz Capable (SC66):** Reserved per PCI Express spec **Power Well:** Core
20:16	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
15:12	0x0 RW	**I/O Address Limit (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh. **Power Well:** Core
11:8	0x0 RO	**I/O Limit Address Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing. **Power Well:** Core
7:4	0x0 RW	**I/O Base Address (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h. **Power Well:** Core
3:0	0x0 RO	**I/O Base Address Capability (IOBC):** Indicates that the bridge does not support 32-bit I/O addressing. **Power Well:** Core

11.2.7 Memory Base and Limit (MBL)—Offset 20h

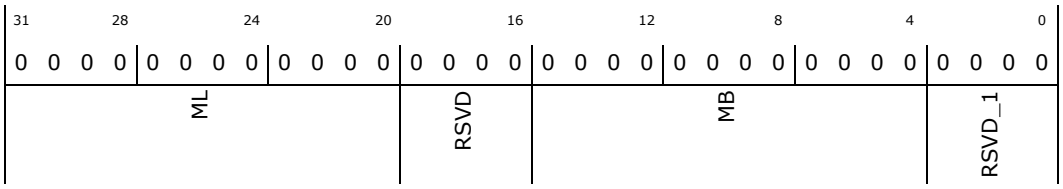
Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is MB [gt]= AD[lb]31:20[rb] [lt]= ML.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 20h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range. **Power Well:** Core
19:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:4	0x0 RW	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range. **Power Well:** Core
3:0	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

11.2.8 Prefetchable Memory Base and Limit (PMBL)—Offset 24h

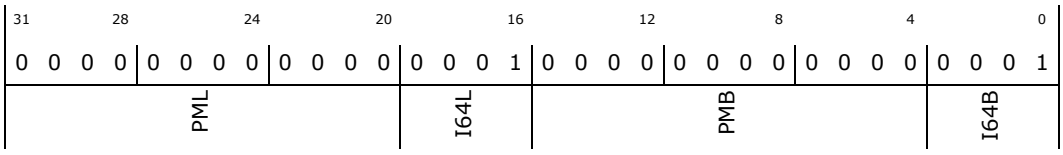
Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is PMBU32:PMB [gt]= AD[lb]63:32[rb]:AD[lb]31:20[rb] [lt]= PMLU32:PML.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 24h

Default: 00010001h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range. **Power Well:** Core
19:16	0x1 RO	**64-bit Indicator (I64L):** Indicates support for 64-bit addressing. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:4	0x0 RW	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range. **Power Well:** Core
3:0	0x1 RO	**64-bit Indicator (I64B):** Indicates support for 64-bit addressing. **Power Well:** Core

11.2.9 Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h

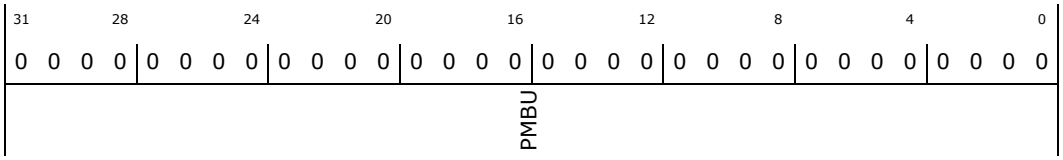
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 28h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base. **Power Well:** Core

11.2.10 Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch

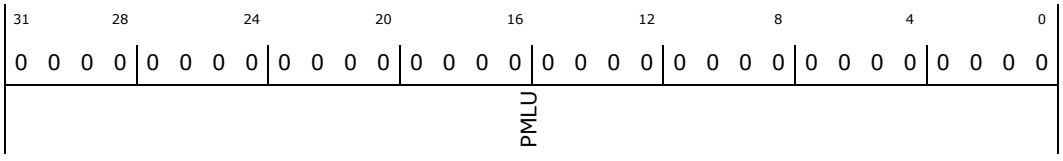
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit. **Power Well:** Core

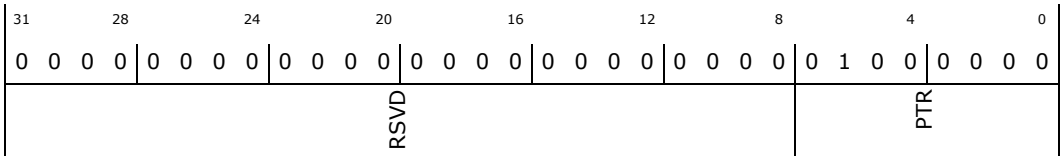
11.2.11 Capabilities List Pointer (CAPP)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 34h

Default: 00000040h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
7:0	0x40 RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. Capability Linked List (Default Settings) Offset Capability Next Pointer 40h PCI Express 80h 80h Message Signaled Interrupt (MSI) 90h 90h Subsystem Vendor A0h A0h PCI Power Management 00h Extended PCIe Capability Linked List Offset Capability Next Pointer 100h Advanced Error Reporting 000h **Power Well:** Core

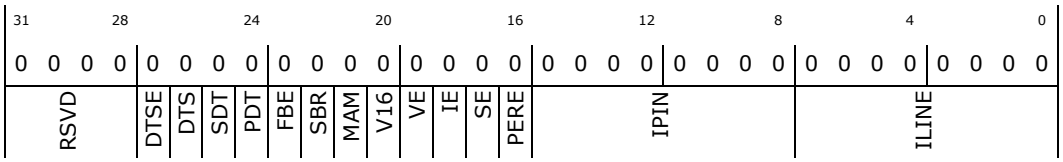
11.2.12 Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 3Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
27	0x0 RW/V2	**Discard Timer SERR# Enable (DTSE):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port. **Power Well:** Core
26	0x0 RO	**Discard Timer Status (DTS):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, this register can remain RO as no secondary discard timer exists that will ever cause it to be set. **Power Well:** Core
25	0x0 RW/V2	**Secondary Discard Timer (SDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port. **Power Well:** Core
24	0x0 RW/V2	**Primary Discard Timer (PDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port. **Power Well:** Core
23	0x0 RO	**Fast Back to Back Enable (FBE):** Reserved per Express spec. **Power Well:** Core
22	0x0 RW	**Secondary Bus Reset (SBR):** Triggers a Hot Reset on the PCI-Express port. **Power Well:** Core
21	0x0 RW/V2	**Master Abort Mode (MAM):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
18	0x0 RW	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh). **Power Well:** Core
17	0x0 RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not. **Power Well:** Core
16	0x0 RW	**Parity Error Response Enable (PERE):** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD. **Power Well:** Core
15:8	0x0 RO/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the STRPFUSECFG register in chipset config space: Port Bits[lb]15:12[rb] Bits[lb]11:08[rb] 1 0h STRPFUSECFG.P1IP 2 0h STRPFUSECFG.P2IP 3 0h STRPFUSECFG.P3IP 4 0h STRPFUSECFG.P4IP 5 0h STRPFUSECFG.P5IP 6 0h STRPFUSECFG.P6IP 7 0h STRPFUSECFG.P7IP 8 0h STRPFUSECFG.P8IP The value that is programmed into STRPFUSECFG is always reflected in this register. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register returns a value of 00h when read, else this register returns the value from the table above. **Power Well:** Core
7:0	0x0 RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. **Power Well:** Core

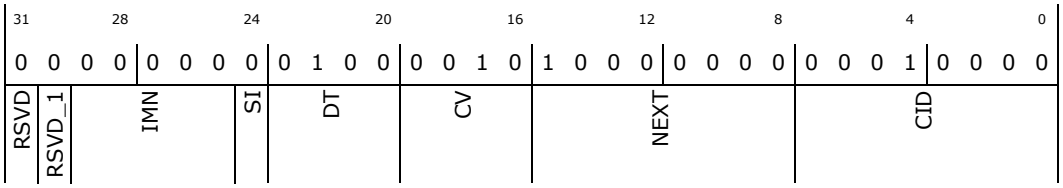
11.2.13 Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 40h

Default: 00428010h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
30	0x0 RO	**Reserved (RSVD_1):** Reserved. This register at one time was for TCS Routing but that was later removed from the PCIe 2.0 spec **Power Well:** Core
29:25	0x0 RO	**Interrupt Message Number (IMN):** The PCIE SIP does not have multiple MSI interrupt numbers. **Power Well:** Core
24	0x0 RW/O	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset. **Power Well:** Core
23:20	0x4 RO	**Device / Port Type (DT):** Indicates this is a PCI-Express root port **Power Well:** Core
19:16	0x2 RO	**Capability Version (CV):** Version 2.0 indicates devices compliant to the PCI Express 2.0 specification which incorporates the Register Expansion ECN. **Power Well:** Core
15:8	0x80 RW/O	**Next Capability (NEXT):** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. **Power Well:** Core
7:0	0x10 RO	**Capability ID (CID):** Indicates this is a PCI Express capability **Power Well:** Core

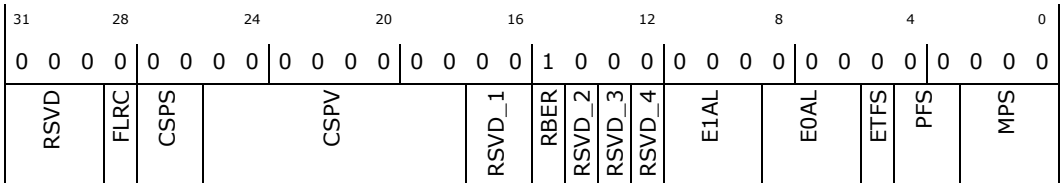
11.2.14 Device Capabilities (DCAP)—Offset 44h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 44h

Default: 00008000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
28	0x0 RO	**Function Level Reset Capable (FLRC):** Not supported in Root Ports **Power Well:** Core
27:26	0x0 RO	**Captured Slot Power Limit Scale (CSPS):** Not supported **Power Well:** Core
25:18	0x0 RO	**Captured Slot Power Limit Value (CSPV):** Not supported **Power Well:** Core
17:16	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
15	0x1 RO	**Role Based Error Reporting (RBER):** When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions. **Power Well:** Core
14	0x0 RO	**Reserved (RSVD_2):** Reserved. On previous version of the specification this was Power Indicator Present (PIP) **Power Well:** Core
13	0x0 RO	**Reserved (RSVD_3):** Reserved. On previous version of the specification this was Attention Indicator Present (AIP) **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12	0x0 RO	**Reserved (RSVD_4):** Reserved. On previous version of the specification this was Attention Button Present (ABP) **Power Well:** Core
11:9	0x0 RO	**Endpoint L1 Acceptable Latency (E1AL):** Reserved for root ports. **Power Well:** Core
8:6	0x0 RO	**Endpoint L0 Acceptable Latency (E0AL):** Reserved for Root port. **Power Well:** Core
5	0x0 RO	**Extended Tag Field Supported (ETFS):** The PCIE SIP never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags. **Power Well:** Core
4:3	0x0 RO	**Phantom Functions Supported (PFS):** No phantom functions supported **Power Well:** Core
2:0	0x0 RW/O	**Max Payload Size Supported (MPS):** BIOS should write to this field during system initialization. Only Max Payload Size of 128B is supported. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. **Power Well:** Core

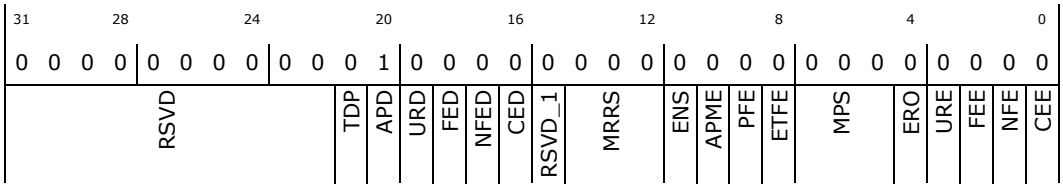
11.2.15 Device Control; Device Status (DCTL_DSTS)—Offset 48h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 48h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID. **Power Well:** Core
20	0x1 RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup **Power Well:** Core
19	0x0 RW/1C/V	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected. **Power Well:** Core
18	0x0 RW/1C/V	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed tlp **Power Well:** Core
17	0x0 RW/1C/V	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned tlp, unexpected completions, unsupported requests, completor abort, or completer timeout **Power Well:** Core
16	0x0 RW/1C/V	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, tlp crc error, dllp crc error, replay num rollover, replay timeout. **Power Well:** Core
15	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
14:12	0x0 RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11	0x0 RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests. **Power Well:** Core
10	0x0 RW/P	**Aux Power PM Enable (APME):** The OS will set this bit to '1' if the device connected has detected aux power. **Power Well:** Core
9	0x0 RO	**Phantom Functions Enable (PFE):** Not supported **Power Well:** Core
8	0x0 RO	**Extended Tag Field Enable (ETFE):** Not supported **Power Well:** Core
7:5	0x0 RW	**Max Payload Size (MPS):** The root port only supports 128B max payload. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. If the DCAP.MPS indicates 128B max payload size support, programming this field to any values other than 128B will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME. **Power Well:** Core
4	0x0 RO	**Enable Relaxed Ordering (ERO):** Not supported **Power Well:** Core
3	0x0 RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**Fatal Error Reporting Enable (FEE):** enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting. **Power Well:** Core
1	0x0 RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting. **Power Well:** Core
0	0x0 RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting. **Power Well:** Core

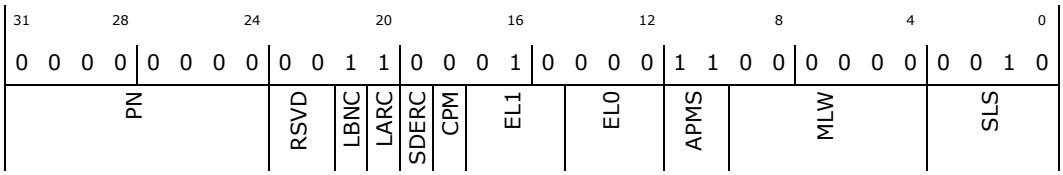
11.2.16 Link Capabilities (LCAP)—Offset 4Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 4Ch

Default: 00310C02h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port # Value of PN field 1 01h 2 02h 3 03h 4 04h **Power Well:** Core
23:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
21	0x1 RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms. **Power Well:** Core
20	0x1 RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. **Power Well:** Core
19	0x0 RO	**Surprise Down Error Reporting Capable (SDERC):** Set to '0' to indicate the root port does not support Surprise Down Error Reporting **Power Well:** Core
18	0x0 RO	**Clock Power Management (CPM):** '0' Indicates that root ports do not support the CLKREQ# mechanism. **Power Well:** Core
17:15	0x2 RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b Less than 1 us 001b 1 us to less than 2 us 010b 2 us to less than 4 us 011b 4 us to less than 8 us 100b 8 us to less than 16 us 101b 16 us to less than 32 us 110b 32 us to 64 us 111b More than 64 us Note: If PXP PLL shutdown is enabled, BIOS should program this latency to comprehend PLL lock latency. **Power Well:** Core
14:12	0x0 RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration: LCTL.CCC Value 0 MPC.UCEL 1 MPC.CCEL **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11:10	0x3 RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00 (Reserved) 01 L0s Entry supported 10 Reserved 11 Both L0s and L1 supported Note: If STRPFUSECFG.ASPMDIS is 1, the default of this field is [quote]01[/quote]. Otherwise, the default of this field is [quote]11[/quote]. If STRPFUSECFG.ASPMDIS is 1, BIOS writing [quote]11[/quote] to this field will have the same effect as [quote]01[/quote]. [quote]01[/quote] will be reflected on this register when read and the register will turn to Read-Only once written once. **Power Well:** Core
9:4	0x0 RO/V	**Maximum Link Width (MLW):** For the root ports, several values can be taken, based upon the value of the chipset configuration register field RPC.PC1 for ports 1-4: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h **Power Well:** Core
3:0	0x2 RO/V	**Supported Link Speeds (SLS):** Indicates the supported link speeds of the Root Port. 0001b 2.5 GT/s Link speed supported 0010b 5.0 GT/s and 2.5GT/s Link speeds supported This register reports a value of 0001b if the Root Port Gen2 Disable Fuse is set or the MPC.PCIEGEN2DIS bit is set, else this register reports a value of 0010b. **Power Well:** Core

11.2.17 Link Control; Link Status (LCTL_LSTS)—Offset 50h

Access Method

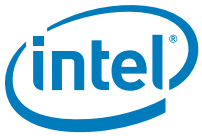
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 50h

Default: 00010000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LABS	LBMS	LA	SCC	LT	RSVD	NLW					CLS					RSVD_1				LABIE	LBMIE	HAWD	ECPM	ES	CCC	RL	LD	RCBC	RSVD_2	ASPM	

Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C/V	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b. **Power Well:** Core
30	0x0 RW/1C/V	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b. **Power Well:** Core
29	0x0 RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise. **Power Well:** Core
28	0x0 RO/V	**Slot Clock Configuration (SCC):** In normal mode, PCIE SIP uses the same reference clock as on the platform and does not generate its own clock. Note: The default of this register bit is dependent on the [quote]PCIe Non-Common Clock With SSC Mode Enable Strap[/quote]. If the strap enables non-common clock with SSC support, this bit shall default to '0'. Otherwise, this bit shall default to '1'. **Power Well:** Core
27	0x0 RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training. **Power Well:** Core
26	0x0 RO	**Reserved (RSVD):** Reserved. Previously this was defined as Link Training Error (LTE) but support for this bit was removed from subsequent versions of the PCI Express specification. **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
25:20	0x0 RO/V	**Negotiated Link Width (NLW):** For the root ports, this register could take on several values: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h The value of this register is undefined if the link has not successfully trained. **Power Well:** Core
19:16	0x1 RO/V	**Current Link Speed (CLS):** 0001b Link is 2.5Gb/s Link 0010b 5.0 GT/s Link The value of this field is undefined if the link is not up. **Power Well:** Core
15:12	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
11	0x0 RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set. **Power Well:** Core
10	0x0 RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/ PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b. **Power Well:** Core
9	0x0 RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Default value of this bit is 0b. **Power Well:** Core
8	0x0 RO	**Enable Clock Power Management (ECPM):** Reserved. Not supported on PCIE SIP Root Ports. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW	**Extended Synch (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0. **Power Well:** Core
6	0x0 RW	**Common Clock Configuration (CCC):** When set, indicates that the PCIE SIP and device are operating with a distributed common reference clock. **Power Well:** Core
5	0x0 WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns '0' when read. Software uses LSTS.LT to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress. **Power Well:** Core
4	0x0 RW	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state. **Power Well:** Core
3	0x0 RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes. **Power Well:** Core
2	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
1:0	0x0 RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used. Note: If STRPFUSECFG.ASPMDIS is '1', hardware will always see [quote]00[/quote] as an output from this register. BIOS reading this register should always return the correct value. **Power Well:** Core

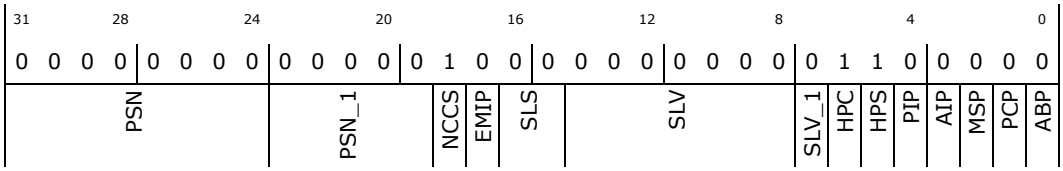
11.2.18 Slot Capabilities (SLCAP)—Offset 54h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 54h

Default: 00040060h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW/O	**Physical Slot Number (PSN):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
23:19	0x0 RW/O	**Physical Slot Number (PSN_1):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
18	0x1 RO	**No Command Completed Support (NCCS):** Set to '1' as this port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes. **Power Well:** Core
17	0x0 RO	**Electromechanical Interlock Present (EMIP):** Set to 0 to indicate that no electro-mechanical interlock is implemented. **Power Well:** Core
16:15	0x0 RW/O	**Slot Power Limit Scale (SLS):** specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
14:8	0x0 RW/O	**Slot Power Limit Value (SLV):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
7	0x0 RW/O	**Slot Power Limit Value (SLV_1):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
6	0x1 RW/O	**Hot Plug Capable (HPC):** When set, Indicates that hot plug is supported. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5	0x1 RW/O	**Hot Plug Surprise (HPS):** When set, indicates the device may be removed from the slot without prior notification. **Power Well:** Core
4	0x0 RO	**Power Indicator Present (PIP):** Indicates that a power indicator LED is not present for this slot. **Power Well:** Core
3	0x0 RO	**Attention Indicator Present (AIP):** Indicates that an attention indicator LED is not present for this slot. **Power Well:** Core
2	0x0 RO	**MRL Sensor Present (MSP):** Indicates that an MRL sensor is not present **Power Well:** Core
1	0x0 RO	**Power Controller Present (PCP):** Indicates that a power controller is not implemented for this slot **Power Well:** Core
0	0x0 RO	**Attention Button Present (ABP):** Indicates that an attention button is not implemented for this slot. **Power Well:** Core

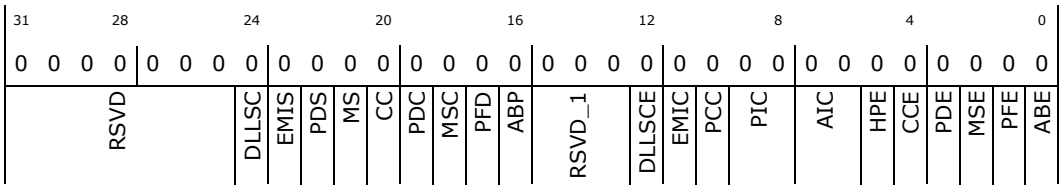
11.2.19 Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 58h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
24	0x0 RW/1C/V	**Data Link Layer State Changed (DLLSC):** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device. **Power Well:** Core
23	0x0 RO	**Electromechanical Interlock Status (EMIS):** Reserved as this port does not support and electromechanical interlock. **Power Well:** Core
22	0x0 RO/V	**Presence Detect State (PDS):** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected ('1') or empty ('0'). If XCAP.SI is cleared, this bit is a '1'. **Power Well:** Core
21	0x0 RO	**MRL Sensor State (MS):** Reserved as the MRL sensor is not implemented. **Power Well:** Core
20	0x0 RO	**Command Completed (CC):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
19	0x0 RW/1C/V	**Presence Detect Changed (PDC):** This bit is set by the root port when the SLSTS.PDS bit changes state. **Power Well:** Core
18	0x0 RO	**MRL Sensor Changed (MSC):** Reserved as the MRL sensor is not implemented. **Power Well:** Core
17	0x0 RO	**Power Fault Detected (PFD):** Reserved as a power controller is not implemented. **Power Well:** Core
16	0x0 RO	**Attention Button Pressed (ABP):** This register is RO as this port does not implement an attention button **Power Well:** Core
15:13	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12	0x0 RW	**Data Link Layer State Changed Enable (DLLSCE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed **Power Well:** Core
11	0x0 RO	**Electromechanical Interlock Control (EMIC):** Reserved as this port does not support an Electromechanical Interlock. **Power Well:** Core
10	0x0 RO	**Power Controller Control (PCC):** This bit has no meaning for module based hot plug. **Power Well:** Core
9:8	0x0 RO	**Power Indicator Control (PIC):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
7:6	0x0 RO	**Attention Indicator Control (AIC):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
5	0x0 RW	**Hot Plug Interrupt Enable (HPE):** When set, enables generation of a hot plug interrupt on enabled hot plug events. **Power Well:** Core
4	0x0 RO	**Command Completed Interrupt Enable (CCE):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
3	0x0 RW	**Presence Detect Changed Enable (PDE):** When set, enables the generation of a hot plug interrupt or wake message when the presence detect logic changes state. **Power Well:** Core
2	0x0 RO	**MRL Sensor Changed Enable (MSE):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
1	0x0 RO	**Power Fault Detected Enable (PFE):** This register is RO as this port does not implement a Hot Plug Controller... **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RO	**Attention Button Pressed Enable (ABE):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core

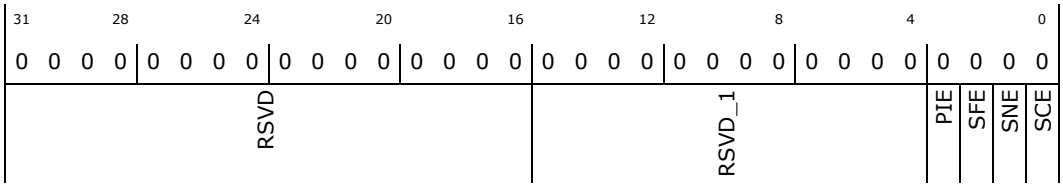
11.2.20 Root Control (RCTL)—Offset 5Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 5Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:4	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
3	0x0 RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a '0' to '1' transition, or due to this bit being set with RSTS.PS already set). **Power Well:** Core
2	0x0 RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set. **Power Well:** Core
1	0x0 RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set. **Power Well:** Core

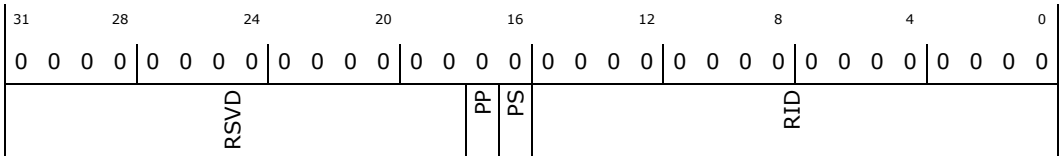
11.2.21 Root Status (RSTS)—Offset 60h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 60h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
17	0x0 RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. PCIE SIP root ports have a one deep PME pending queue. **Power Well:** Core
16	0x0 RW/1C/V	**PME Status (PS):** Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared. **Power Well:** Core
15:0	0x0 RO/V	**PME Requestor ID (RID):** Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set. PCIE SIP root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped. **Power Well:** Core

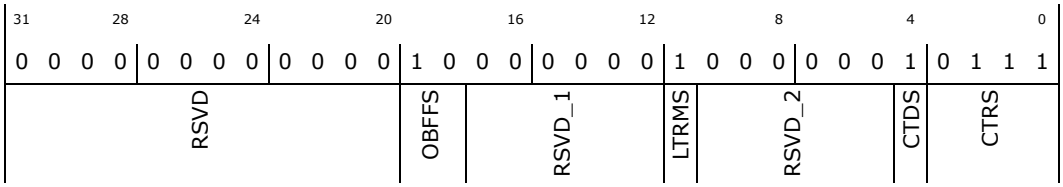
11.2.22 Device Capabilities 2 (DCAP2)—Offset 64h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 64h

Default: 00080817h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
19:18	0x2 RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b - OBFF is not supported. 01b - OBFF is supported using Message signaling only. 10b - OBFF is supported using WAKE# signaling only. 11b - OBFF is supported using WAKE# and Message signaling. BIOS should program this field to 00b or 10b during system initialization to advertise the level of hardware OBFF support to software. BIOS should never program this field to 01b or 11b since OBFF messaging is not supported. **Power Well:** Core
17:12	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
11	0x1 RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a '1' or a '0' to enable/disable the root port from declaring support for the LTR capability. **Power Well:** Core
10:5	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
4	0x1 RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x7 RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A [amp] B 0110b Ranges B [amp] C 0111b Ranges A, B [amp] C [lt]-- This is what IP supports 1110b Ranges B, C [amp] D 1111b Ranges A, B, C [amp] D All other values are reserved. **Power Well:** Core

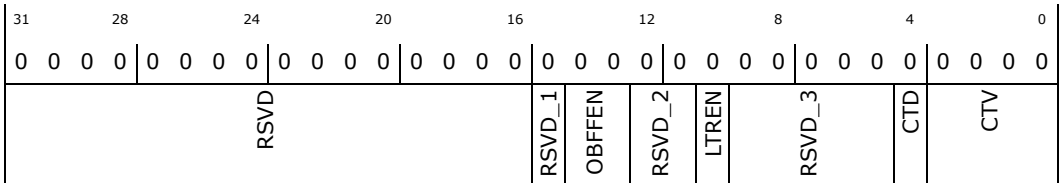
11.2.23 Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 68h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
14:13	0x0 RW	**Optimized Buffer Flush/Fill Enable (OBFFEN):** 00b Disable OBFF mechanism. 01b Enable OBFF mechanism using Message signaling (Variation A). 10b Enable OBFF mechanism using Message signaling (Variation B). 11b Enable OBFF using WAKE# signaling. Note: Only encoding 00b and 11b are supported. The encoding of 01b or 10b would be aliased to 00b. If DCAP2.OBFFS is clear, programming this field to any non-zero values will have no effect. **Power Well:** Core
12:11	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
10	0x0 RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect. **Power Well:** Core
9:5	0x0 RO	**Reserved (RSVD_3):** Reserved **Power Well:** Core
4	0x0 RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x0 RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. ThePCIE SIP targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range A (50us to 10 ms) programmability range is supported: 0001b 90-100us (spec range is 50 us to 100 us) 0010b 9-10ms (spec range is 1ms to 10 ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either when this value was changed or when each request was issued. **Power Well:** Core

11.2.24 Link Capabilities 2 (LCAP2)—Offset 6Ch

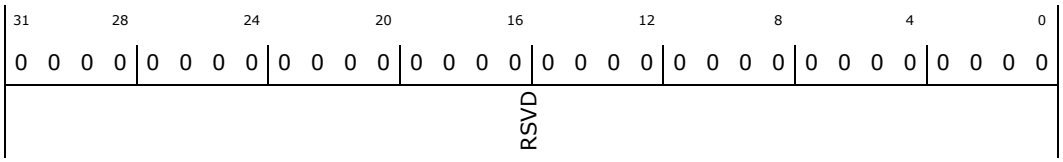
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 6Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

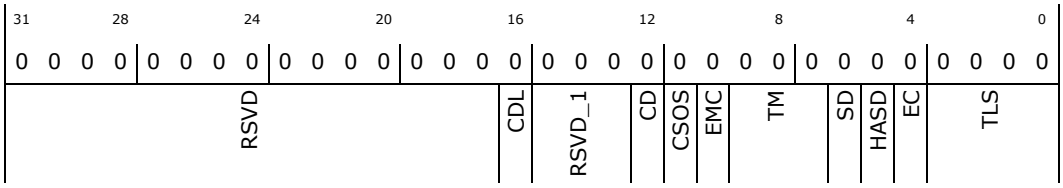
11.2.25 Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 70h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
16	0x0 RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is operating at 2.5 GT/s speed. **Power Well:** Core
15:13	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
12	0x0 RW/P	**Compliance De-emphasis (CD):** This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s, the setting of this bit has no effect. The default value of this bit is 0b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11	0x0 RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b. **Power Well:** Core
10	0x0 RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value. **Power Well:** Core
9:7	0x0 RW/P	**Transmit Margin (TM):** This field controls the value of the nondeemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see PCI Express Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value. **Power Well:** Core
6	0x0 RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RO	**Hardware Autonomous Speed Disable (HASD):** Reserved. This port cannot autonomously change speeds. **Power Well:** Core
4	0x0 RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. **Power Well:** Core
3:0	0x0 RW/V/P	**Target Link Speed (TLS):** This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. For PCIE SIP, the allowed value is: 0001b 2.5 GT/s Target Link Speed 0010b 5.0 GT/s and 2.5GT/s Link speeds supported If a value is written to this field that does not correspond to a speed included in the Supported Link Speeds field, the result is undefined. The default value of this field is the highest Link speed supported by the component (as reported in the Supported Link Speeds field of the Link Capabilities register). **Power Well:** Core

11.2.26 Slot Capabilities 2 (SLCAP2)—Offset 74h

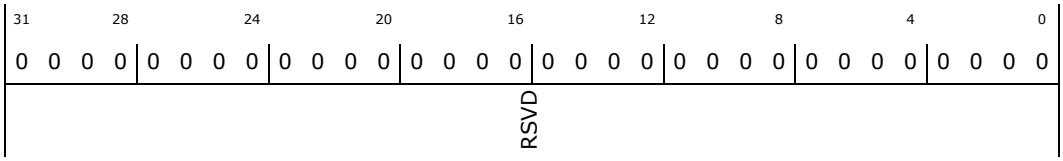
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 74h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

11.2.27 Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h

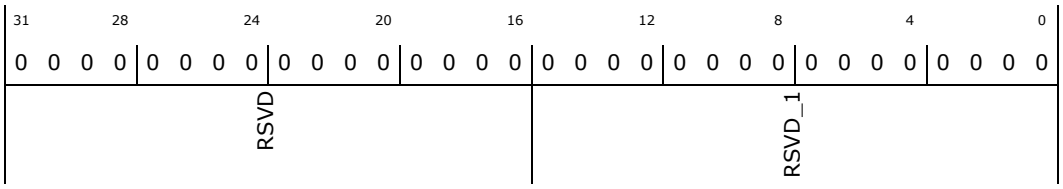
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 78h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:0	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

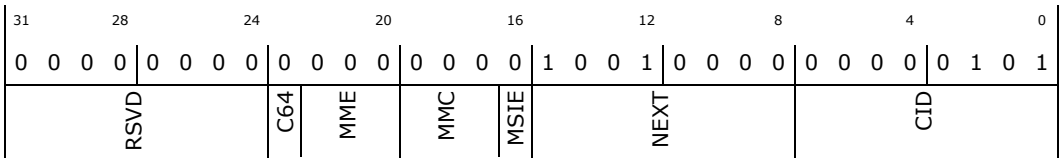
11.2.28 Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 80h

Default: 00009005h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
23	0x0 RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
22:20	0x0 RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port. **Power Well:** Core
19:17	0x0 RO	**Multiple Message Capable (MMC):** Only one message is required. **Power Well:** Core
16	0x0 RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated. **Power Well:** Core
15:8	0x90 RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. **Power Well:** Core
7:0	0x5 RO	**Capability ID (CID):** Capabilities ID indicates MSI. **Power Well:** Core

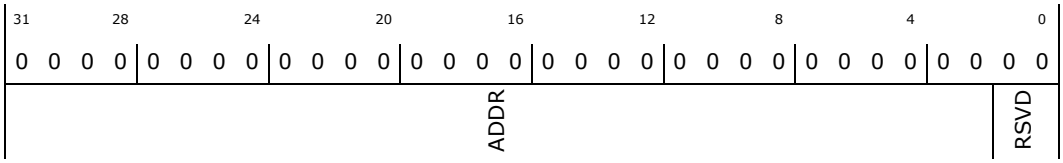
11.2.29 Message Signaled Interrupt Message Address (MA)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 84h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Address (ADDR):** Lower 32 bits of the system specified message address, always DW aligned. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1:0	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

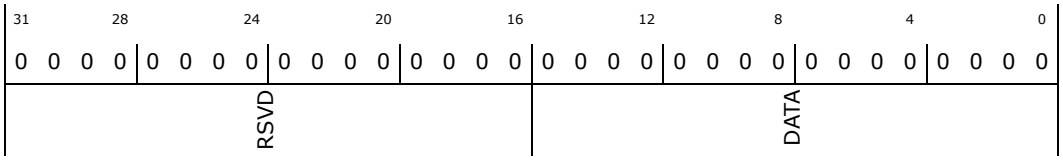
11.2.30 Message Signaled Interrupt Message Data (MD)—Offset 88h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 88h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:0	0x0 RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[lb]15:0[rb]) during the data phase of the MSI memory write transaction. **Power Well:** Core

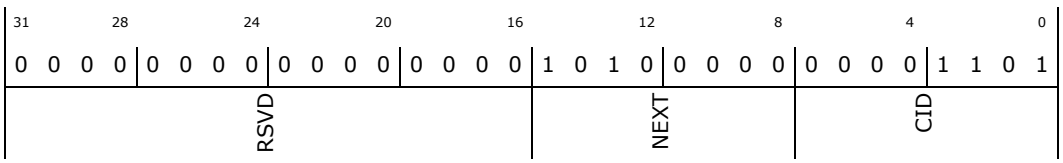
11.2.31 Subsystem Vendor Capability (SVCAP)—Offset 90h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 90h

Default: 0000A00Dh



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:8	0xa0 RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. **Power Well:** Core
7:0	0xd RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability. **Power Well:** Core

11.2.32 Subsystem Vendor IDs (SVID)—Offset 94h

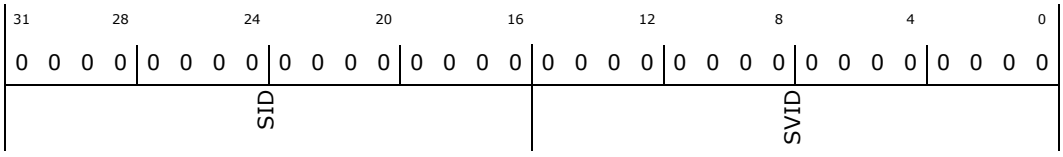
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 94h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset). **Power Well:** Core
15:0	0x0 RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset). **Power Well:** Core

11.2.33 Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h

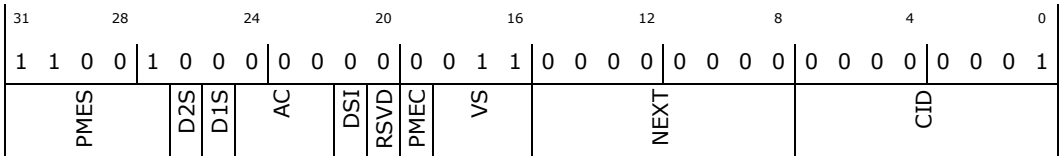
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + A0h

Default: C8030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x19 RO	**PME Support (PMES):** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy Microsoft operating systems to enable PME# in devices connected behind this root port. **Power Well:** Core
26	0x0 RO	**D2_Support (D2S):** The D2 state is not supported. **Power Well:** Core
25	0x0 RO	**D1_Support (D1S):** The D1 state is not supported. **Power Well:** Core
24:22	0x0 RO	**Aux_Current (AC):** Reports 0mA (self-powered), as use of this controller does not add to suspend well power consumption. **Power Well:** Core
21	0x0 RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required. **Power Well:** Core
20	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
19	0x0 RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#. **Power Well:** Core
18:16	0x3 RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Next Capability (NEXT):** Indicates this is the last item in the list. **Power Well:** Core
7:0	0x1 RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability. **Power Well:** Core

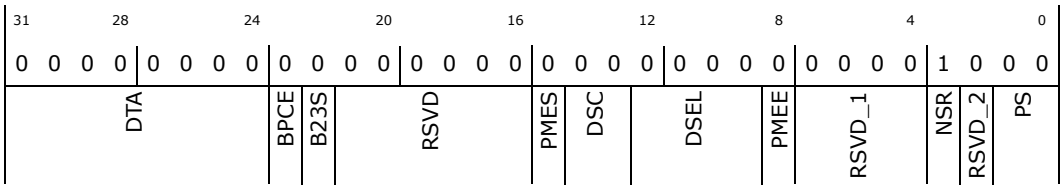
11.2.34 PCI Power Management Control And Status (PMCS)—Offset A4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + A4h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Data (DTA):** Reserved **Power Well:** Core
23	0x0 RO	**Bus Power / Clock Control Enable (BPCE):** Reserved per PCI Express specification **Power Well:** Core
22	0x0 RO	**B2/B3 Support (B23S):** Reserved per PCI Express specification. **Power Well:** Core
21:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15	0x0 RO	**PME Status (PMES):** Indicates a PME was received on the downstream link. **Power Well:** Core
14:13	0x0 RO	**Data Scale (DSC):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12:9	0x0 RO	**Data Select (DSEL):** Reserved **Power Well:** Core
8	0x0 RW/P	**PME Enable (PMEE):** Indicates PME is enabled. The root port takes no action on this bit, but it must be RW for legacy Microsoft operating systems to enable PME# on devices connected to this root port. This register resides in the resume well and is not reset on a resume from S3/S4/S5. The reset for this register is RSMRST# which is not asserted during a Warm Reset. **Power Well:** Core
7:4	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
3	0x1 RW/O	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. **Power Well:** Core
2	0x0 RO	**Reserved (RSVD_2):** Reserved. **Power Well:** Core
1:0	0x0 RW	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 - D0 state 11 - D3HOT state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a '10' or '01' to these bits, the write will be ignored. **Power Well:** Core

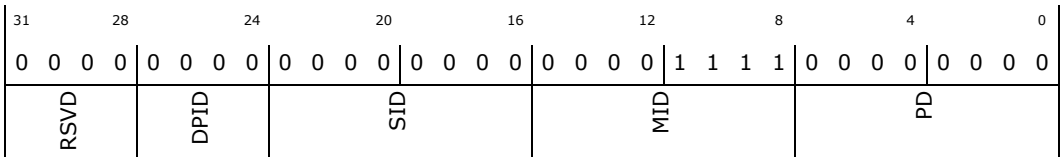
11.2.35 Manufacturer's ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + F8h

Default: 00000F00h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
27:24	0x0 RO/V	**Dot portion of Process ID (DPID):** The value of this field is SoC specific. Example: Process/Dot (PD) is 1265.8. Indicates the dot as .8. **Power Well:** Core
23:16	0x0 RO/V	**Stepping Identifier (SID):** This field is incremented for each stepping of the part. Note that this field can be used by software to differentiate steppings when the Revision ID may not change. A single Manufacturing Stepping ID can be implemented that is readable from all functions in the chip because all of them are incremented in lock-step. **Power Well:** Core
15:8	0xf RO	**Manufacturing Identifier (MID):** 0Fh = Intel **Power Well:** Core
7:0	0x0 RO/V	**Process/Dot (PD):** Indicates the current process. The value of this field is SoC specific. Example: Process/Dot (PD) is 1265.8. Indicates the Process (1265). **Power Well:** Core

11.2.36 Advanced Error Reporting Capability Header (AECH)—Offset 100h

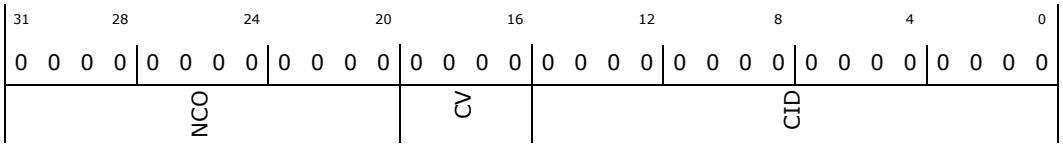
Size:32 bits The AER capability can optionally be included or excluded from the capabilities list. The full AER is supported.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 100h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW/O	**Next Capability Offset (NCO):** Set to 000h as this is the last capability in the list. **Power Well:** Core
19:16	0x0 RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0 **Power Well:** Core
15:0	0x0 RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0 **Power Well:** Core

11.2.37 Uncorrectable Error Status (UES)—Offset 104h

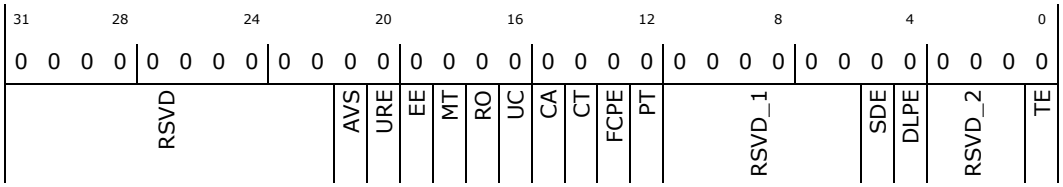
This register must maintain its state through a platform reset. It loses its state upon loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 104h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported **Power Well:** Core
20	0x0 RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received. **Power Well:** Core
19	0x0 RO	**ECRC Error Status (EE):** ECRC is not supported. **Power Well:** Core
18	0x0 RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received. **Power Well:** Core
17	0x0 RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred. **Power Well:** Core
16	0x0 RW/1C/V/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received. **Power Well:** Core
15	0x0 RW/1C/V/P	**Completor Abort Status (CA):** Indicates a completer abort was received **Power Well:** Core
14	0x0 RW/1C/V/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value **Power Well:** Core
13	0x0 RO	**Flow Control Protocol Error Status (FCPE):** Not supported. **Power Well:** Core
12	0x0 RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received. **Power Well:** Core
11:6	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RO	**Surprise Down Error Status (SDE):** Surprise Down is not supported. **Power Well:** Core
4	0x0 RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred. **Power Well:** Core
3:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x0 RO	**Training Error Status (TE):** Not supported. **Power Well:** Core

11.2.38 Uncorrectable Error Mask (UEM)—Offset 108h

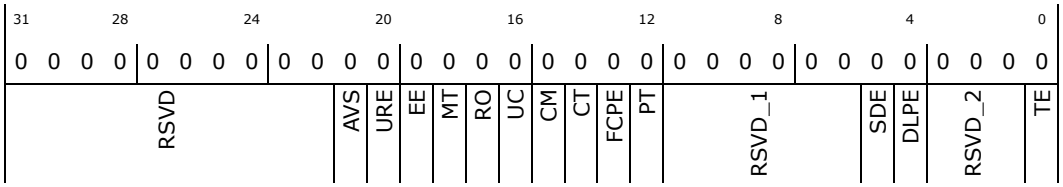
When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 108h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported **Power Well:** Core
20	0x0 RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RO	**ECRC Error Mask (EE):** ECRC is not supported. **Power Well:** Core
18	0x0 RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs **Power Well:** Core
17	0x0 RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows. **Power Well:** Core
16	0x0 RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions. **Power Well:** Core
15	0x0 RW/P	**Completor Abort Mask (CM):** Mask for completer abort. **Power Well:** Core
14	0x0 RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts. **Power Well:** Core
13	0x0 RO	**Flow Control Protocol Error Mask (FCPE):** Not supported. **Power Well:** Core
12	0x0 RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs. **Power Well:** Core
11:6	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
5	0x0 RO	**Surprise Down Error Mask (SDE):** Surprise Down is not supported. **Power Well:** Core
4	0x0 RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors. **Power Well:** Core
3:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x0 RO	**Training Error Mask (TE):** Not supported. **Power Well:** Core

11.2.39 Uncorrectable Error Severity (UEV)—Offset 10Ch

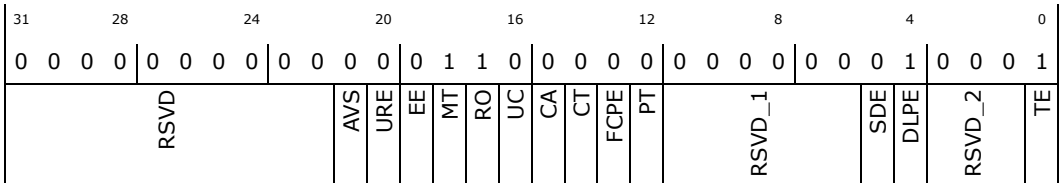
This register gives the option to make an uncorrectable error fatal or non-fatal. An error is fatal if the bit is set. An error is non-fatal if the bit is cleared. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 10Ch

Default: 00060011h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**ACS Violation Severity (AVS):** Reserved. Access Control Services are not supported **Power Well:** Core
20	0x0 RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception. **Power Well:** Core
19	0x0 RO	**ECRC Error Severity (EE):** ECRC is not supported. **Power Well:** Core
18	0x1 RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception. **Power Well:** Core
17	0x1 RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences. **Power Well:** Core
16	0x0 RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception. **Power Well:** Core
15	0x0 RW/P	**Completor Abort Severity (CA):** Severity for completer abort. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout. **Power Well:** Core
13	0x0 RO	**Flow Control Protocol Error Severity (FCPE):** Not supported. **Power Well:** Core
12	0x0 RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception. **Power Well:** Core
11:6	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
5	0x0 RO	**Surprise Down Error Severity (SDE):** Surprise Down is not supported. **Power Well:** Core
4	0x1 RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors. **Power Well:** Core
3:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x1 RO	**Training Error Severity (TE):** TE not supported. This bit is left as RO='1' for ease of implementation.. **Power Well:** Core

11.2.40 Correctable Error Status (CES)—Offset 110h

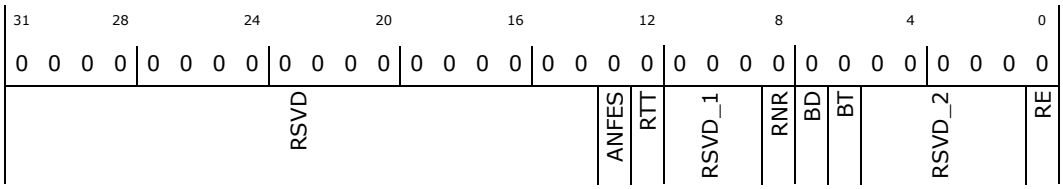
This register is only reset by a loss of core power

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 110h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
13	0x0 RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that a Advisory Non-Fatal Error occurred. **Power Well:** Core
12	0x0 RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out. **Power Well:** Core
11:9	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
8	0x0 RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over. **Power Well:** Core
7	0x0 RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received. **Power Well:** Core
6	0x0 RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received. **Power Well:** Core
5:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x0 RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred. **Power Well:** Core

11.2.41 Correctable Error Mask (CEM)—Offset 114h

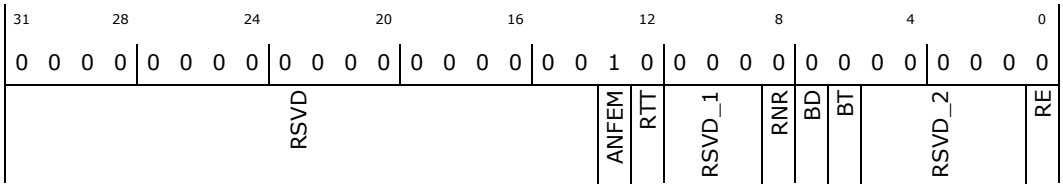
When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 114h

Default: 00002000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
13	0x1 RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting. **Power Well:** Core
12	0x0 RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout. **Power Well:** Core
11:9	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
8	0x0 RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover. **Power Well:** Core
7	0x0 RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception. **Power Well:** Core
6	0x0 RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception. **Power Well:** Core
5:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x0 RW/P	**Receiver Error Mask (RE):** Mask for receiver errors. **Power Well:** Core

11.2.42 Advanced Error Capabilities and Control (AECC)—Offset 118h

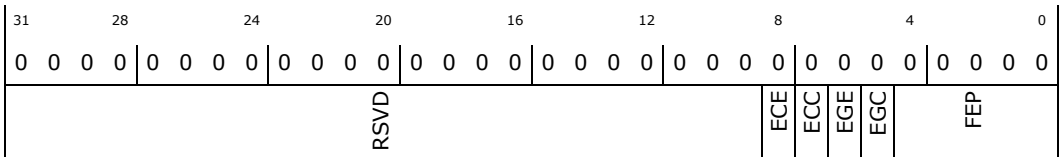
This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 118h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
8	0x0 RO	**ECRC Check Enable (ECE):** ECRC is not supported. **Power Well:** Core
7	0x0 RO	**ECRC Check Capable (ECC):** ECRC is not supported. **Power Well:** Core
6	0x0 RO	**ECRC Generation Enable (EGE):** ECRC is not supported. **Power Well:** Core
5	0x0 RO	**ECRC Generation Capable (EGC):** ECRC is not supported. **Power Well:** Core
4:0	0x0 RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register. **Power Well:** Core

11.2.43 Header Log DW1 (HL_DW1)—Offset 11Ch

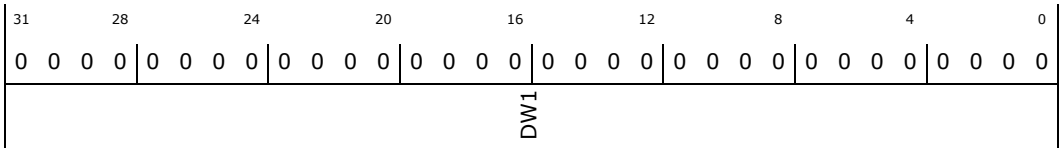
Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 11Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO/V/P	**1st dWord of TLP (DW1):** Byte0 [amp][amp] Byte1 [amp][amp] Byte2 [amp][amp] Byte3 **Power Well:** Core

11.2.44 Header Log DW2 (HL_DW2)—Offset 120h

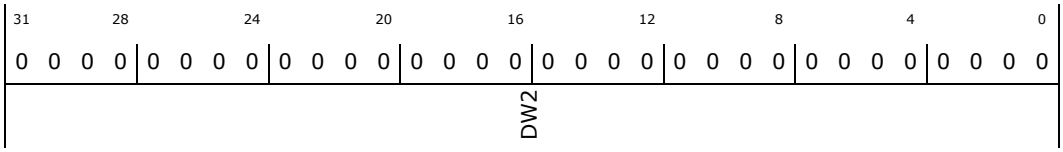
Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 120h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO/V/P	**2nd dWord of TLP (DW2):** Byte4 [amp][amp] Byte5 [amp][amp] Byte6 [amp][amp] Byte7 **Power Well:** Core

11.2.45 Header Log DW3 (HL_DW3)—Offset 124h

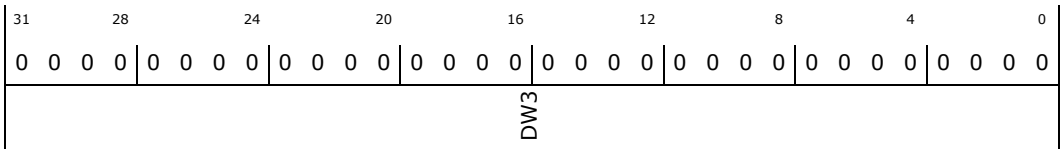
Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 124h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO/V/P	**3rd dWord of TLP (DW3):** Byte8 [amp][amp] Byte9 [amp][amp] Byte10 [amp][amp] Byte11 **Power Well:** Core

11.2.46 Header Log DW4 (HL_DW4)—Offset 128h

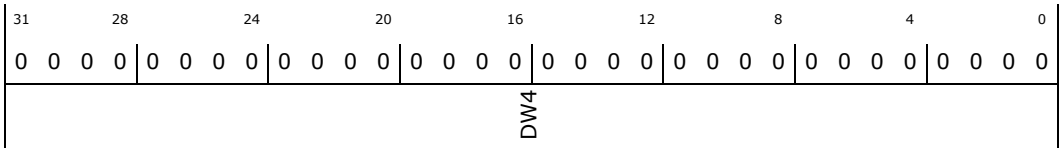
Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 128h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO/V/P	**4th dWord of TLP (DW4):** Byte12 [amp][amp] Byte13 [amp][amp] Byte14 [amp][amp] Byte15 **Power Well:** Core

11.2.47 Root Error Command (REC)—Offset 12Ch

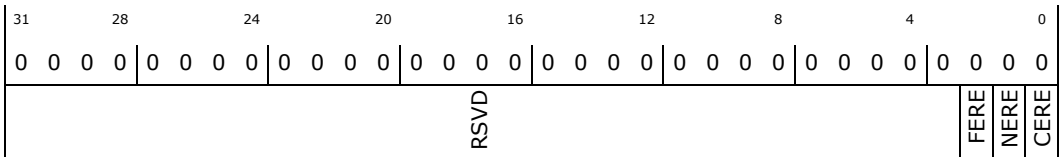
This register allows errors to generate interrupts.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 12Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
2	0x0 RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device. **Power Well:** Core
1	0x0 RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device. **Power Well:** Core
0	0x0 RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device. **Power Well:** Core

11.2.48 Root Error Status (RES)—Offset 130h

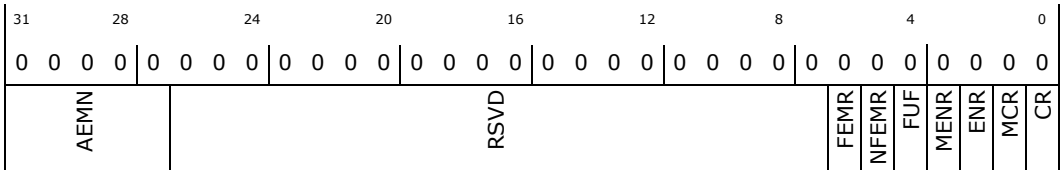
This register can track more than one error and set the [quote]multiple[/quote] bits if a second or subsequent error occurs and the first has not been serviced. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 130h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**Advanced Error Interrupt Message Number (AEMN):** Reserved. There is only one error interrupt allocated. **Power Well:** Core
26:7	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
6	0x0 RW/1C/V/P	**Fatal Error Message Received (FEMR):** Set when one or more Fatal Uncorrectable Error Messages have been received. **Power Well:** Core
5	0x0 RW/1C/V/P	**Non-Fatal Error Messages Received (NFEMR):** Set when one or more Non-Fatal Uncorrectable error messages have been received **Power Well:** Core
4	0x0 RW/1C/V/P	**First Uncorrectable Fatal (FUF):** Set when the first Uncorrectable Error message received is for a fatal error. **Power Well:** Core
3	0x0 RW/1C/V/P	**Multiple ERR_FATAL/NONFATAL Received (MENR):** Set when either a fatal or a non-fatal error is received and the ENR bit is already set. **Power Well:** Core
2	0x0 RW/1C/V/P	**ERR_FATAL/NONFATAL Received (ENR):** Set when either a fatal or a non-fatal error message is received. **Power Well:** Core
1	0x0 RW/1C/V/P	**Multiple ERR_COR Received (MCR):** Set when a correctable error message is received and the CR bit is already set. **Power Well:** Core
0	0x0 RW/1C/V/P	**ERR_COR Received (CR):** Set when a correctable error message is received. **Power Well:** Core

11.2.49 Error Source Identification (ESID)—Offset 134h

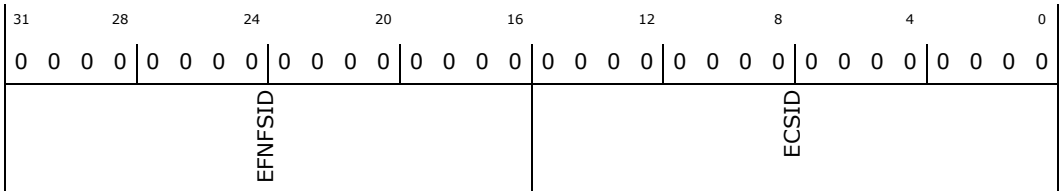
Size:32 bits Identifies the source (Requester ID) of the first correctable and uncorrectable (Non-Fatal / Fatal) errors reported in the Root Error Status register. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 134h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message with the ERR_FATAL/NONFATAL Received register is not already set. **Power Well:** Core
15:0	0x0 RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the Requester ID indicated in the received ERR_COR Message with the ERR_COR Received register is not already set. **Power Well:** Core

11.2.50 L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h

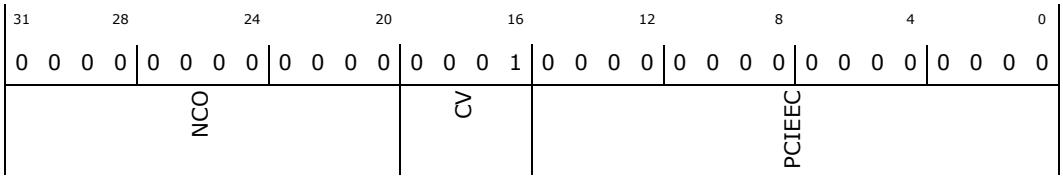
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 200h

Default: 00010000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits. **Power Well:** Core
19:16	0x1 RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW/O	**PCI Express Extended Capability ID (PCIEEC):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for L1 Substates is [lt]TBD[gt]. **Power Well:** Core

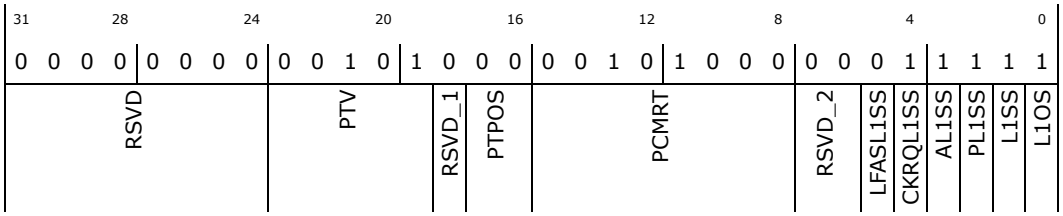
11.2.51 L1 Sub-States Capabilities (L1SCAP)—Offset 204h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 204h

Default: 0028281Fh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
23:19	0x5 RW/O	**Port Tpower_on Value (PTV):** Along with the Port T_POWER_ON Scale Field in the L1 Substates Capabilities register sets theTime (in us) that this Port requires the port on the opposite side of Link to wait in L1.OFF_EXIT after sampling CLKREQ# asserted before actively driving the interface. Port Tpower_on is calculated by multiplying the value in this field by the value in the Port Tpower_on scale field in the L1 Sub-States Capabilities 2 register. Required for all Ports that support L1.OFF. **Power Well:** Core
18	0x0 RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
17:16	0x0 RW/O	**Port Tpower_on Scale (PTPOS):** Specifies the scale used for Tpower_on value field in the L1 Substates Capabilities register. [quote]00b[/quote]: 2 us [quote]01b[/quote]: 10 us [quote]10b[/quote]: 100 us [quote]11b[/quote]: Reserved Required for all Ports that support L1.OFF. **Power Well:** Core
15:8	0x28 RW/O	**Port Common Mode Restore Time (PCMRT):** This is the time (in us) required for this Port to re-establish common mode. Required for all ports that support L1.OFF. **Power Well:** Core
7:6	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
5	0x0 RO	**LFAS L1 Substates Supported (LFASL1SS):** When Set this bit indicates that this Port supports the LFAS mechanism. Required for both Upstream and Downstream Ports. **Power Well:** Core
4	0x1 RO	**CLKREQ# L1 Substates Supported (CKRQL1SS):** When Set this bit indicates that this Port supports the CLKREQ# out-of-band wake mechanism. Required for both Upstream and Downstream Ports. **Power Well:** Core
3	0x1 RW/O	**ASPM L1 Substates Supported (AL1SS):** When set, this bit indicates that this port supports L1 substates for ASPM L1. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static **Power Well:** Core
2	0x1 RW/O	**PCI-PM L1 Substates Supported (PL1SS):** When set, this bit indicates that this port supports L1 substates for PCI-PM. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1	0x1 RW/O	**L1.SNOOZ Supported (L1SS):** When set, this bit indicates that L1.SNOOZ sub-state is supported and this bit must be set by all ports implementing L1 Sub-States. A port that supports L1.OFF must support L1.SNOOZ. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static **Power Well:** Core
0	0x1 RW/O	**L1.OFF Supported (L1OS):** When set, this bit indicates that L1.OFF power management feature is supported. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static **Power Well:** Core

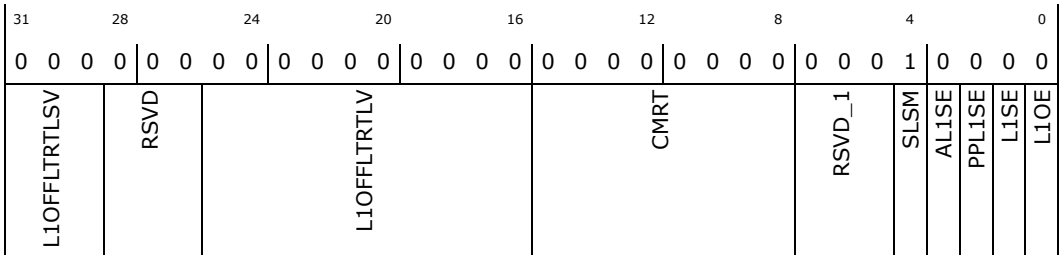
11.2.52 L1 Sub-States Control 1 (L1SCTL1)—Offset 208h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 208h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**L1.OFF LTR Threshold Latency ScaleValue (L1OFFLTRTLSV):** This field contains the L1.OFF LTR Threshold Latency Scale Value for this particular PCIe root port. The value in this field, together with L1OFFLTRTLV is compared against both the snoop and non-snoop LTR values of the device. 000: L1OFFLTRSTLV times 1 ns 001: L1OFFLTRSTLV times 32 ns 010: L1OFFLTRSTLV times 1024 ns 011: L1OFFLTRSTLV times 32768 ns 100: L1OFFLTRSTLV times 1048576 ns 101: L1OFFLTRSTLV times 33554432 ns Others: Not Permitted. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
28:26	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
25:16	0x0 RW	**L1.OFF LTR Threshold Latency Value (L1OFFLTRTLV):** This field contains the L1.OFF LTR Threshold Latency Value for this particular PCIe root port. The value in this field, together with L1OFFLTRTLSV is compared against both the snoop and non-snoop LTR values of the device. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static **Power Well:** Core
15:8	0x0 RW	**Common Mode Restore Time (CMRT):** This is the Tcommon_mode time the PCIe root port needs to continue sending TS1 and refrain from sending TS2 in Recovery state to allow the TX common mode to be established prior to sending TS2. The timer starts from the time when the first TS1 has been sent and the receiver has detected un-squelch. The value in this field defines the time in micro-seconds. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static **Power Well:** Core
7:5	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
4	0x1 RO	**Select L1 Substates Mechanism (SLSM):** When Set this bit indicates that this Port must use the CLKREQ#-based mechanism, when Clear the LFAS mechanism must be used. Ports that support only one mechanism for L1 Substates are permitted to implement this bit as RO/HwInit, and the value of this bit must reflect the supported mechanism. Default value is implementation-specific. **Power Well:** Core
3	0x0 RW	**ASPM L1 Substates Enabled (AL1SE):** When set, this bit indicates that L1 substates are enabled for ASPM. Required for both upstream and downstream ports. Register Attribute: Dynamic **Power Well:** Core
2	0x0 RW	**PCI-PM L1 Substates Enabled (PPL1SE):** When set, this bit indicates that L1 substates are enabled for PCI-PM. Required for both upstream and downstream ports. Register Attribute: Dynamic **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**L1.SNOOZ Enable (L1SE):** When set, this bit indicates that L1.SNOOZ power management feature is enabled. If L1.OFF is enabled, L1.SNOOZ must also be enabled. This field must be programmed prior to enabling ASPM L1. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. **Power Well:** Core
0	0x0 RW	**L1.OFF Enable (L1OE):** When set, this bit indicates that L1.OFF power management feature is enabled. L1.OFF can only be enabled if the platform supports bi-directional CLKREQPLUS#. This field must be programmed prior to enabling ASPM L1. Ports that support L1.OFF shall support Latency Tolerance Reporting. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. **Power Well:** Core

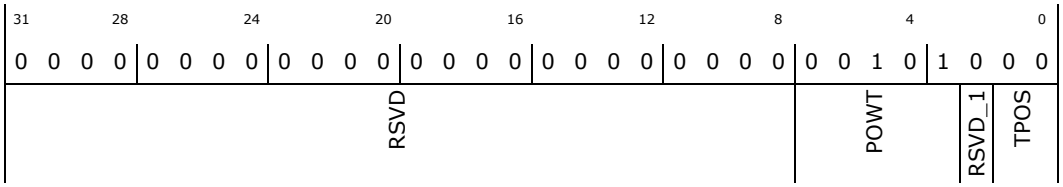
11.2.53 L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 20Ch

Default: 00000028h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
7:3	0x5 RW	**Power On Wait Time (POWT):** Along with the Tpower_on Scale sets the minimum amount of time (in us) that the Port must wait in L1.OFF EXIT after sampling CLKREQPLUS# asserted before actively driving the interface. The timer starts counting when CLKREQPLUS# asserts in L1.OFF state. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
1:0	0x0 RW	**Tpower_on Scale (TPOS):** Specifies the scale used for Tpower_on value. '00b': 2 us '01b': 10 us '10b': 100us '11b': Reserved. Required for all Ports that support L1.OFF. Register Attribute: Static **Power Well:** Core

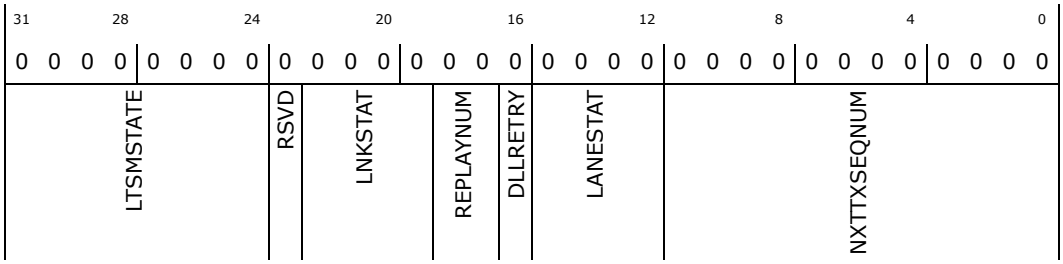
11.2.54 PCI Express Status 1 (PCIESTS1)—Offset 328h

Access Method

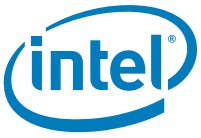
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 328h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO/V	0AECPCMPRETRAIN 0BECPCMFAILP0TOP2 0C DETP0TOP2 0D PMODECHANGE 0EECPCMPCIE 0FECPCMUSB3 10DET2POLLINP0 11POLLINGACTIVE 12POLLINGCOMPLIANCEMARGINCNT 13POLLINGCOMPLIANCE 14POLLINGCOMPLIANCESPEEDUP 15POLLINGCOMPLIANCESPEEDDN 16POLLINGCOMPLIANCESPEEDTXEIDLE 17POLLINGCOMPLIANCESPEEDRXEIDLE 18POLLINGCOMPLIANCESPEED 19POLLINGCOMPLIANCESPEEDDONE 1APOLLINGCOMPLIANCEEXIT



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO/V	1BPOLLINGCONFIGURATION 1C POLLINGTXEIDLE 1D POLLINGEND 1EPOLLINGENDWAIT 1FLINKWIDTHSTART 20LINKWIDTHACCEPT 21LANENUMWAIT 22LANENUMACCEPT 23LANEDESKEW 24CONFIGCOMPLETE 25CONFIGIDLE 26LWNEXITRECOVERY 27CONFIGLPBKENTRY 28CONFIGLPBKLWSTART 29CONFIGLPBKSPEEDTXEIDLE 2ACONFIGLPBKSPEEDSTART 2BCONFIGLPBKSPEEDRXEIDLE 2C CONFIGLPBKSPEED 2D CONFIGLPBKREUTSKIP 2ECONFIGLPBKREUT 2FCONFIGLPBKEXITM 30CONFIGLPBKTXEIDLE 31LWNEXIT 32LWNLNK2DETECT 33L0 34TXL0SRXL0 35RXL0STXL0 36TXL0SRXL0S 37L1TXEIDLE 38L1RCVEIDLE 39L1PREENTRY 3AL1ENTRY 3BL1IDLE 3C L1IDLEGEN2WAIT 3D L1EXIT 3EL2TXEIDLE 3FL2RCVEIDLE 40L2IDLEWAIT 41L2IDLERDY 42L2IDLE 43LOOPBACKENTRY 44LPBKACTIVEMTXSKP 45LPBKACTIVEMSKPDSKW 46LOOPBACKACTIVEM 47LPBKSLAVESPEEDTXEIDLE 48LPBKSLAVESPEEDRXEIDLE 49LPBKSLAVESPEED 4ALOOPBACKACTIVES 4BLOOPBACKCMMSKP 4C LOOPBACKCMM 4D LOOPBACKEXITM 4ELOOPBACKEXITS 4FLOOPBACKEXITL0 50LOOPBACKLNK2DETECT

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO/V	51LOOPBACK2DETECT 52DISTX16TS1DIS 53DISTXEIDLE 54DISWAITSTART 55DISWAITGNT 56DISWAIT4TXMARGIN 57DISWAIT 58DIS2DETECT 59HOTRESETTS1 5AHOTRESETDONE 5BHOTRESETEIDLE 5C RECOVERYRCVRWAIT 5D RECOVERYRCVRMARGINCNT 5ERECOVERYRCVRLOCK 5FRECOVERYDESKEW 60RECOVERYRCVRCFG 61RECOVERYSPEED 62RECOVERYSPEEDTXEIDLE 63RECOVERYSPEEDRXEIDLE 64RECOVERYSPEEDREADY 65RECOVERYIDLE 66RECOVERYEXITDETECT 67RECOVERYLNK2DETECT 68RECOVERYEXITLPBK 69RECOVERYEXITL0 6ARECOVERYEXITDIS 6BRECOVERYEXITRST Note: This register field could be used by REUT software to monitor the link LTSSM substates. **Power Well:** Core
23	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core
22:19	0x0 RO/V	**Link Status (LNKSTAT):** During Link initialization the Link will always traverse this list of state from the top (0000) to the bottom of the list (0111). One or more power management states may be skipped, but the direction of list traversal will remain the same. 0000 Link Down 0001 : Link Retrain 0011 : L1 0100 : L2 0101 : L3 0111 : L0 (Link Up) 1000 : L0s (Transmit [amp] Receive) 1001 : L0s (Transmit only) 1010 : L0s (Receive only) All others reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
18:17	0x0 RO/V	**Replay Number (REPLAYNUM):** Number of times the Retry Buffer has been replayed since the last Link initialization / re-training. When the Data Link Layer has replayed the contents of the Retry Buffer four times a Link re-training will be initiated which will reset this value back to zero. **Power Well:** Core
16	0x0 RO/V	**Data Link Layer Retry (DLLRETRY):** Indicates when the Data Link Layer has received a corrupted TLP or has detected a dropped packet and is currently waiting for the remote agent to re-transmit the corrupted/dropped packet. The value of Next Receive Sequence Number will be the sequence number associated with the corrupted packet. **Power Well:** Core
15:12	0x0 RO/V	**Lane Status (LANESTAT):** Indicates which lanes are trained. A '1' indicates that the corresponding lane is trained (i.e. bit 0 = '1' means lane 0 is trained). **Power Well:** Core
11:0	0x0 RO/V	**Next Transmitted Sequence Number (NXTTXSEQNUM):** This is the sequence number to be applied to and pre-pended to the next outgoing TLP. **Power Well:** Core

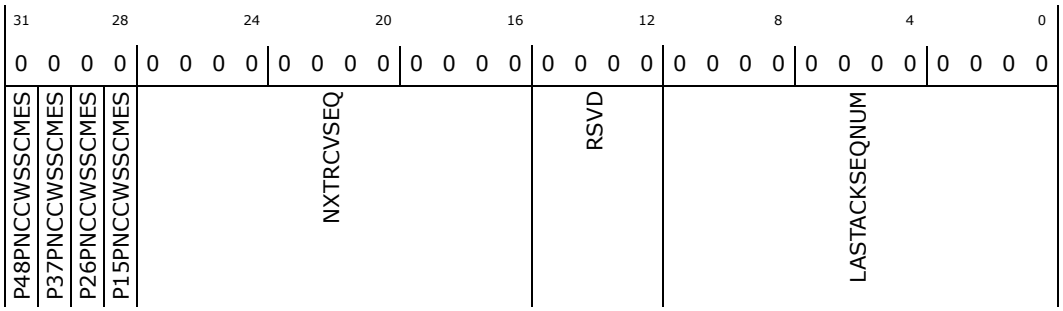
11.2.55 PCI Express Status 2 (PCIESTS2)—Offset 32Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 32Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO/V	**PCIe Port 4 Non-Common Clock With SSC Mode Enable Strap (P48PNCCWSSCMES):** '0': PCIe port 4 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 4 is enabled to operate in non-common clock mode with SSC enabled. **Power Well:** Core
30	0x0 RO/V	**PCIe Port 3 Non-Common Clock With SSC Mode Enable Strap (P37PNCCWSSCMES):** '0': PCIe port 3 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 3 is enabled to operate in non-common clock mode with SSC enabled. **Power Well:** Core
29	0x0 RO/V	**PCIe Port 2 Non-Common Clock With SSC Mode Enable Strap (P26PNCCWSSCMES):** '0': PCIe port 2 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 2 is enabled to operate in non-common clock mode with SSC enabled. **Power Well:** Core
28	0x0 RO/V	**PCIe Port 1 Non-Common Clock With SSC Mode Enable Strap (P15PNCCWSSCMES):** '0': PCIe port 1 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 1 is enabled to operate in non-common clock mode with SSC enabled. **Power Well:** Core
27:16	0x0 RO/V	**Next Receive Sequence Number (NXTRCVSEQ):** This is the sequence number associated with the TLP that is expected to be received next. **Power Well:** Core
15:12	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
11:0	0x0 RO/V	**Last Acknowledged Sequence Number (LASTACKSEQNUM):** This is the sequence number associated with the last acknowledged TLP. **Power Well:** Core

11.2.56 PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h

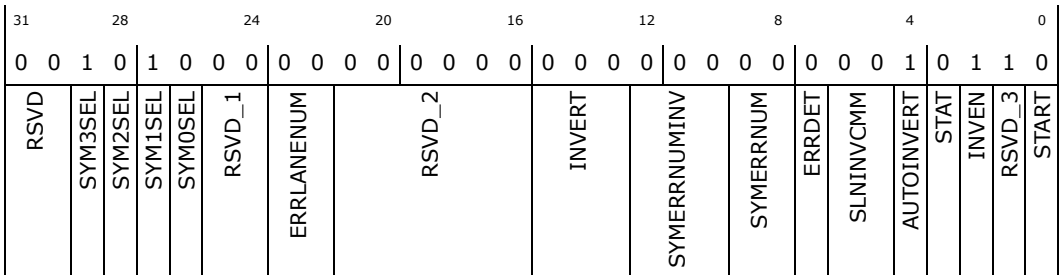
Note that selecting a lane number that does not exist for a port may result in undefined behavior.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 330h

Default: 28000016h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
29	0x1 RW	**CMM Symbol[3] Select (SYM3SEL):** 0: selects CMM Symbol [lb]3[rb] to a control character 1: selects CMM Symbol [lb]3[rb] as a data character **Power Well:** Core
28	0x0 RW	**CMM Symbol[2] Select (SYM2SEL):** 0: selects CMM Symbol [lb]2[rb] to a control character 1: selects CMM Symbol [lb]2[rb] as a data character **Power Well:** Core
27	0x1 RW	**CMM Symbol[1] Select (SYM1SEL):** 0: selects CMM Symbol [lb]1[rb] to a control character 1: selects CMM Symbol [lb]1[rb] as a data character **Power Well:** Core
26	0x0 RW	**CMM Symbol[0] Select (SYM0SEL):** 0: selects CMM Symbol [lb]0[rb] to a control character 1: selects CMM Symbol [lb]0[rb] as a data character **Power Well:** Core
25:24	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
23:22	0x0 RO/V	**CMM Error Lane Number (ERRLANENUM):** This field contains the lane number of the failing lane. Only valid when CMM Error Detected is 1. **Power Well:** Core
21:16	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:13	0x0 RO/V	**CMM Invert (INVERT):** Indicates which lanes are inverted 000: No inversion 001: Lanes 0 010: Lanes 1 011: Lanes 2 100: Lanes 3 This field is only valid when CMM Error Detected (bit 7) is asserted. Additionally, when CMM Error Detected is asserted this field is locked (will not be updated) **Power Well:** Core
12:10	0x0 RO/V	**CMM Symbol Error Number Invert (SYMERRNUMINV):** Indicates which register number miscompared on the failing lane, if the failing lane was an inverted lane. Only valid when CMM Error Detected is 1. 000: CMM Data D0 001: CMM Data D0 010: CMM Data D0 011: CMM Data D1 100: CMM Data D2 101: CMM Data D3 110: CMM Data D0 111: CMM Data D0 **Power Well:** Core
9:8	0x0 RO/V	**CMM Symbol Error Number (SYMERRNUM):** Indicates which register number miscompared on the failing lane, if the failing lane was not inverted. Only valid when CMM Error Detected is 1. 00: CMM Data 0 01: CMM Data 1 10: CMM Data 2 11: CMM Data 3 **Power Well:** Core
7	0x0 RW/1C/V	**CMM Error Detected (ERRDET):** 1: An error was detected 0: No error detected Note: This bit will be shadowed to an observability pin that can be used for IRQ generation. **Power Well:** Core
6:5	0x0 RW	**Select Lane Number to be inverted for CMM (SLNINVCMM):** Select Lane Number to be inverted for CMM **Power Well:** Core
4	0x1 RW	**CMM AutoInvert (AUTOINVERT):** 1: CMM autosequences through the inversion 0: CMM does not sequence inversion **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3	0x0 RO/V	**CMM Status (STAT):** This bit is set when the CMM Start bit is set and cleared when the CMM mode has been entered successfully. 0: Compliance Measurement Mode is not active or CMM mode has been entered successfully. 1: Set as a result of CMM Start bit being set. **Power Well:** Core
2	0x1 RW	**CMM Invert Enable (INVEN):** 1: Enables the Inversion of the lane 0: Lane not inverted **Power Well:** Core
1	0x1 RW	**Reserved (RSVD_3):** Reserved. **Power Well:** Core
0	0x0 RW/L	**CMM Start (START):** 1: Start CMM 0: Stop CMM This register bit is Read-Only when the MPC.SRL bit is set. **Power Well:** Core

11.2.57 PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h

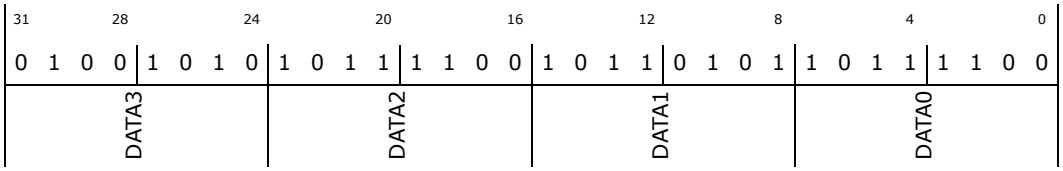
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 334h

Default: 4ABCB5BCh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x4a RW	**CMM Data [3] (DATA3):** This character contains CMM Data [lb]3[rb] that will be transmitted on the link. **Power Well:** Core
23:16	0xbc RW	**CMM Data [2] (DATA2):** This character contains CMM Data [lb]2[rb] that will be transmitted on the link. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0xb5 RW	**CMM Data [1] (DATA1):** This character contains CMM Data [lb]1[rb] that will be transmitted on the link. **Power Well:** Core
7:0	0xbc RW	**CMM Data [0] (DATA0):** This character contains CMM Data [lb]0[rb] that will be transmitted on the link. **Power Well:** Core

11.2.58 Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h

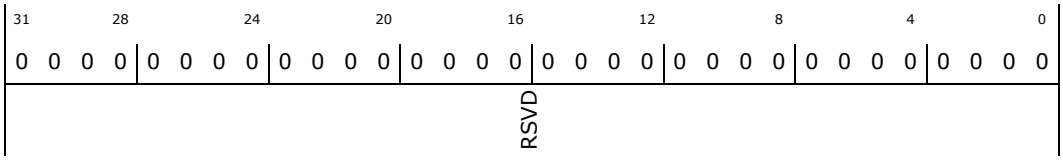
Size:32 bits

Access Method

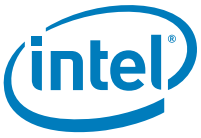
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:1] + 414h

Default: 00000000h



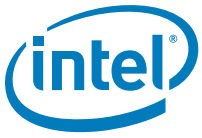
Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core



11.3 PCI Express* Lane 2 PCI Configuration Registers

Table 118. Summary of PCI Express* Lane 2 PCI Configuration Registers—0/28/2

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Identifiers (ID)—Offset 0h" on page 6027	00008086h
4–7h	4	"Device Command; Primary Status (CMD_PSTS)—Offset 4h" on page 6027	00100000h
8–Bh	4	"Revision ID;Class Code (RID_CC)—Offset 8h" on page 6030	06040000h
C–Fh	4	"Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch" on page 6031	00810000h
18–1Bh	4	"Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h" on page 6032	00000000h
1C–1Fh	4	"I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch" on page 6032	00000000h
20–23h	4	"Memory Base and Limit (MBL)—Offset 20h" on page 6034	00000000h
24–27h	4	"Prefetchable Memory Base and Limit (PMBL)—Offset 24h" on page 6035	00010001h
28–2Bh	4	"Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h" on page 6036	00000000h
2C–2Fh	4	"Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch" on page 6036	00000000h
34–37h	4	"Capabilities List Pointer (CAPP)—Offset 34h" on page 6037	00000040h
3C–3Fh	4	"Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch" on page 6037	00000000h
40–43h	4	"Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h" on page 6039	00428010h
44–47h	4	"Device Capabilities (DCAP)—Offset 44h" on page 6040	00008000h
48–4Bh	4	"Device Control; Device Status (DCTL_DSTS)—Offset 48h" on page 6042	00100000h
4C–4Fh	4	"Link Capabilities (LCAP)—Offset 4Ch" on page 6045	00310C02h
50–53h	4	"Link Control; Link Status (LCTL_LSTS)—Offset 50h" on page 6047	00010000h
54–57h	4	"Slot Capabilities (SLCAP)—Offset 54h" on page 6050	00040060h
58–5Bh	4	"Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h" on page 6052	00000000h
5C–5Fh	4	"Root Control (RCTL)—Offset 5Ch" on page 6055	00000000h
60–63h	4	"Root Status (RSTS)—Offset 60h" on page 6056	00000000h
64–67h	4	"Device Capabilities 2 (DCAP2)—Offset 64h" on page 6056	00080817h
68–6Bh	4	"Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h" on page 6058	00000000h
6C–6Fh	4	"Link Capabilities 2 (LCAP2)—Offset 6Ch" on page 6060	00000000h
70–73h	4	"Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h" on page 6061	00000000h
74–77h	4	"Slot Capabilities 2 (SLCAP2)—Offset 74h" on page 6063	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
78–7Bh	4	"Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h" on page 6064	00000000h
80–83h	4	"Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h" on page 6064	00009005h
84–87h	4	"Message Signaled Interrupt Message Address (MA)—Offset 84h" on page 6065	00000000h
88–8Bh	4	"Message Signaled Interrupt Message Data (MD)—Offset 88h" on page 6066	00000000h
90–93h	4	"Subsystem Vendor Capability (SVCAP)—Offset 90h" on page 6066	0000A00Dh
94–97h	4	"Subsystem Vendor IDs (SVID)—Offset 94h" on page 6067	00000000h
A0–A3h	4	"Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h" on page 6068	C8030001h
A4–A7h	4	"PCI Power Management Control And Status (PMCS)—Offset A4h" on page 6069	00000008h
F8–FBh	4	"Manufacturer's ID (MANID)—Offset F8h" on page 6071	00000F00h
100–103h	4	"Advanced Error Reporting Capability Header (AECH)—Offset 100h" on page 6072	00000000h
104–107h	4	"Uncorrectable Error Status (UES)—Offset 104h" on page 6072	00000000h
108–10Bh	4	"Uncorrectable Error Mask (UEM)—Offset 108h" on page 6074	00000000h
10C–10Fh	4	"Uncorrectable Error Severity (UEV)—Offset 10Ch" on page 6076	00060011h
110–113h	4	"Correctable Error Status (CES)—Offset 110h" on page 6077	00000000h
114–117h	4	"Correctable Error Mask (CEM)—Offset 114h" on page 6078	00002000h
118–11Bh	4	"Advanced Error Capabilities and Control (AECC)—Offset 118h" on page 6079	00000000h
11C–11Fh	4	"Header Log DW1 (HL_DW1)—Offset 11Ch" on page 6080	00000000h
120–123h	4	"Header Log DW2 (HL_DW2)—Offset 120h" on page 6081	00000000h
124–127h	4	"Header Log DW3 (HL_DW3)—Offset 124h" on page 6081	00000000h
128–12Bh	4	"Header Log DW4 (HL_DW4)—Offset 128h" on page 6082	00000000h
12C–12Fh	4	"Root Error Command (REC)—Offset 12Ch" on page 6082	00000000h
130–133h	4	"Root Error Status (RES)—Offset 130h" on page 6083	00000000h
134–137h	4	"Error Source Identification (ESID)—Offset 134h" on page 6084	00000000h
200–203h	4	"L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h" on page 6085	00010000h
204–207h	4	"L1 Sub-States Capabilities (L1SCAP)—Offset 204h" on page 6086	0028281Fh
208–20Bh	4	"L1 Sub-States Control 1 (L1SCTL1)—Offset 208h" on page 6088	00000010h
20C–20Fh	4	"L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch" on page 6090	00000028h
328–32Bh	4	"PCI Express Status 1 (PCIESTS1)—Offset 328h" on page 6091	00000000h
32C–32Fh	4	"PCI Express Status 2 (PCIESTS2)—Offset 32Ch" on page 6094	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
330–333h	4	"PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h" on page 6096	28000016h
334–337h	4	"PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h" on page 6098	4ABCB5BCh
414–417h	4	"Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h" on page 6099	00000000h

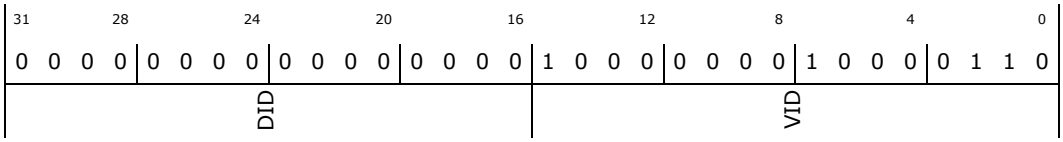
11.3.1 Identifiers (ID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO/V	**Device Identification (DID):** The value of this ID is product specific. **Power Well:** Core
15:0	0x8086 RO	**Vendor Identification (VID):** Indicates Intel **Power Well:** Core

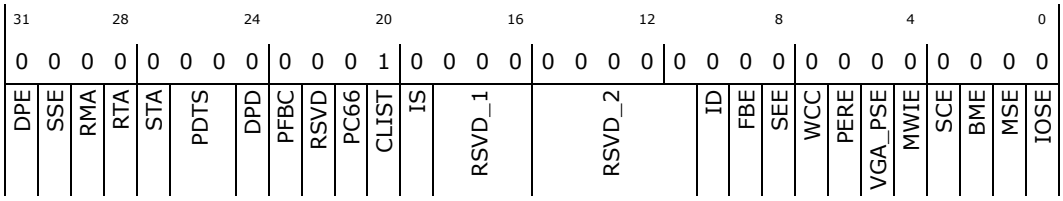
11.3.2 Device Command; Primary Status (CMD_PSTS)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C/V	**DPE - Detected Parity Error (DPE):** Set when the root port receives a command or data from the backbone with a parity error. This is set even if CMD.PERE is not set. **Power Well:** Core
30	0x0 RW/1C/V	**Signaled System Error (SSE):** Set when the root port signals a system error to the internal SERR# logic. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
29	0x0 RW/1C/V	**Received Master Abort (RMA):** Set when the root port receives a completion with unsupported request status from the backbone. **Power Well:** Core
28	0x0 RW/1C/V	**Received Target Abort (RTA):** Set when the root port receives a completion with completer abort from the backbone. **Power Well:** Core
27	0x0 RW/1C/V	**Signaled Target Abort (STA):** Set whenever the root port forwards a target abort received from the downstream device onto the backbone. **Power Well:** Core
26:25	0x0 RO	**Primary DEVSEL# Timing Status (PDTS):** Reserved per PCI-Express spec **Power Well:** Core
24	0x0 RW/1C/V	**Master Data Parity Error Detected (DPD):** Set when the root port receives a completion with a data parity error on the backbone and CMD.PERE is set. **Power Well:** Core
23	0x0 RO	**Primary Fast Back to Back Capable (PFBC):** Reserved per PCI-Express spec. **Power Well:** Core
22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**Primary 66 MHz Capable (PC66):** Reserved per PCI-Express spec. **Power Well:** Core
20	0x1 RO	**Capabilities List (CLIST):** Indicates the presence of a capabilities list. **Power Well:** Core
19	0x0 RO/V	**Interrupt Status (IS):** Indicates status of hot plug and power management interrupts on the root port that result in INTx# message generation. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of CMD.ID. **Power Well:** Core
18:16	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:11	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
10	0x0 RW/V2	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above. **Power Well:** Core
9	0x0 RO	**Fast Back to Back Enable (FBE):** Reserved per PCI-Express spec. **Power Well:** Core
8	0x0 RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set. **Power Well:** Core
7	0x0 RO	**Wait Cycle Control (WCC):** Reserved per PCI-Express spec. **Power Well:** Core
6	0x0 RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a master on the backbone. **Power Well:** Core
4	0x0 RO	**Memory Write and Invalidate Enable (MWIE):** Reserved per PCI-Express spec. **Power Well:** Core
3	0x0 RO	**Special Cycle Enable (SCE):** Reserved per PCI-Express and PCI bridge spec. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**Bus Master Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit. **Power Well:** Core
1	0x0 RW	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone. **Power Well:** Core
0	0x0 RW	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone. **Power Well:** Core

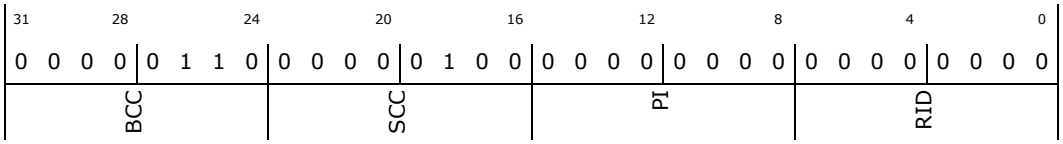
11.3.3 Revision ID;Class Code (RID_CC)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 8h

Default: 06040000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x6 RO	**Base Class Code (BCC):** Indicates the device is a bridge device. **Power Well:** Core
23:16	0x4 RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO/V	**Programming Interface (PI):** The value reported in this register is a function of the Decode Control.Subtractive Decode Enable (SDE) register. SDE Value reported in this register 0: 00h 1: 01h **Power Well:** Core
7:0	0x0 RO/V	**Revision ID (RID):** Indicates the revision of the bridge. **Power Well:** Core

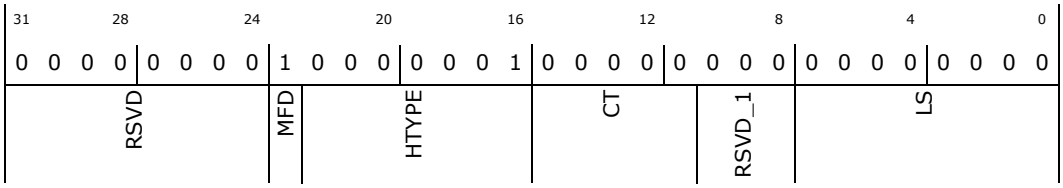
11.3.4 Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + Ch

Default: 00810000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
23	0x1 RO	**Multi-function Device (MFD):** This bit is '1' to indicate a multi-function device. **Power Well:** Core
22:16	0x1 RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h. **Power Well:** Core
15:11	0x0 RO	**Latency Count (CT):** Reserved per PCI-Express spec **Power Well:** Core
10:8	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**Line Size (LS):** This is read/write but contains no functionality, per PCI-Express spec **Power Well:** Core

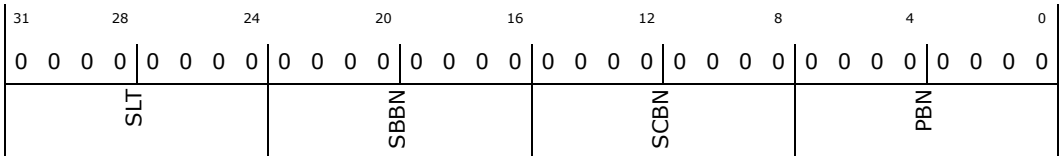
11.3.5 Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 18h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW/V2	**Secondary Latency Timer (SLT):** For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is a RW register; else this register is RO and returns 0. This register does not affect the behavior of any HW logic. **Power Well:** Core
23:16	0x0 RW	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge. **Power Well:** Core
15:8	0x0 RW	**Secondary Bus Number (SCBN):** Indicates the bus number the port. **Power Well:** Core
7:0	0x0 RW	**Primary Bus Number (PBN):** Indicates the bus number of the backbone. **Power Well:** Core

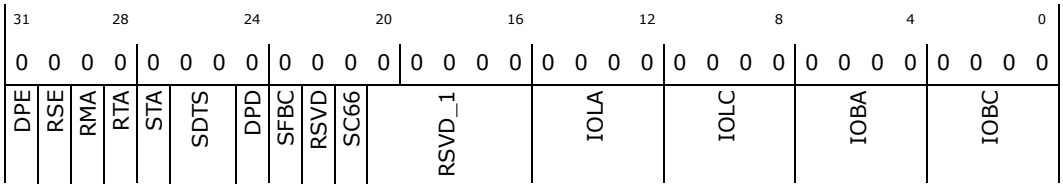
11.3.6 I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 1Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C/V	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP. **Power Well:** Core
30	0x0 RW/1C/V	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device. **Power Well:** Core
29	0x0 RW/1C/V	**Received Master Abort (RMA):** Set when the port receives a completion with [quote]Unsupported Request[/quote] status from the device. **Power Well:** Core
28	0x0 RW/1C/V	**Received Target Abort (RTA):** Set when the port receives a completion with [quote]Completion Abort[/quote] status from the device. **Power Well:** Core
27	0x0 RW/1C/V	**Signaled Target Abort (STA):** Set when the port generates a completion with [quote]Completion Abort[/quote] status to the device. **Power Well:** Core
26:25	0x0 RO/V	**Secondary DEVSEL# Timing Status (SDTS):** Reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b. **Power Well:** Core
24	0x0 RW/1C/V	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side. **Power Well:** Core
23	0x0 RO/V	**Secondary Fast Back to Back Capable (SFBC):** Reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**Secondary 66 MHz Capable (SC66):** Reserved per PCI Express spec **Power Well:** Core
20:16	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
15:12	0x0 RW	**I/O Address Limit (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh. **Power Well:** Core
11:8	0x0 RO	**I/O Limit Address Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing. **Power Well:** Core
7:4	0x0 RW	**I/O Base Address (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h. **Power Well:** Core
3:0	0x0 RO	**I/O Base Address Capability (IOBC):** Indicates that the bridge does not support 32-bit I/O addressing. **Power Well:** Core

11.3.7 Memory Base and Limit (MBL)—Offset 20h

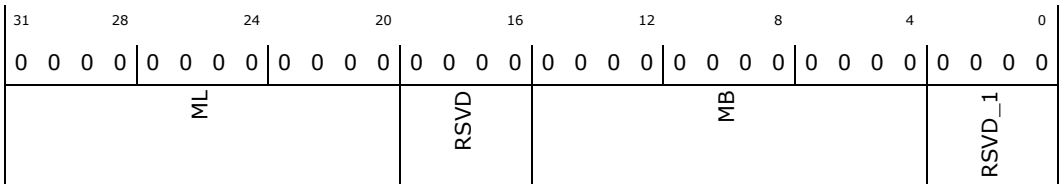
Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is MB [gt]= AD[lb]31:20[rb] [lt]= ML.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 20h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range. **Power Well:** Core
19:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:4	0x0 RW	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range. **Power Well:** Core
3:0	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

11.3.8 Prefetchable Memory Base and Limit (PMBL)—Offset 24h

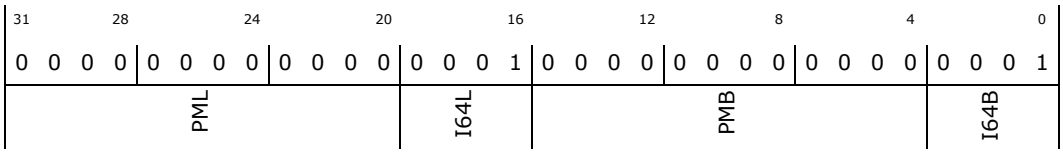
Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is PMBU32:PMB [gt]= AD[lb]63:32[rb]:AD[lb]31:20[rb] [lt]= PMLU32:PML.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 24h

Default: 00010001h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range. **Power Well:** Core
19:16	0x1 RO	**64-bit Indicator (I64L):** Indicates support for 64-bit addressing. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:4	0x0 RW	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range. **Power Well:** Core
3:0	0x1 RO	**64-bit Indicator (I64B):** Indicates support for 64-bit addressing. **Power Well:** Core

11.3.9 Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h

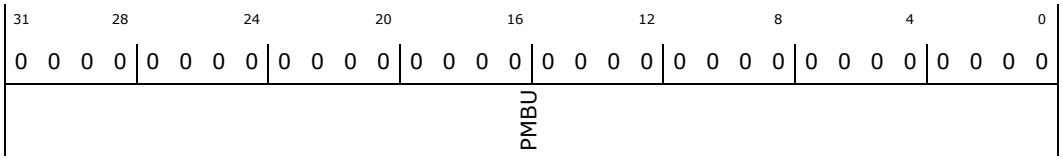
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 28h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base. **Power Well:** Core

11.3.10 Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch

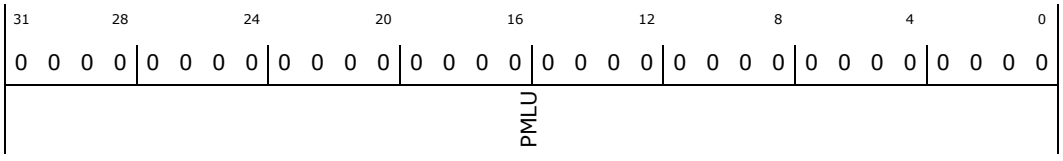
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit. **Power Well:** Core

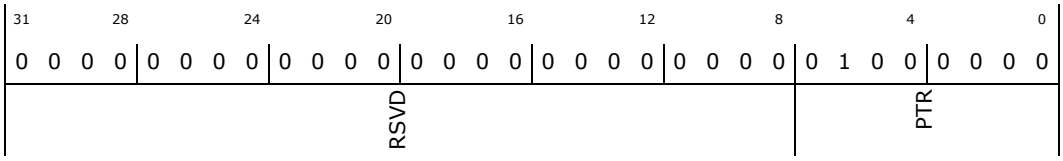
11.3.11 Capabilities List Pointer (CAPP)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 34h

Default: 00000040h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
7:0	0x40 RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. Capability Linked List (Default Settings) Offset Capability Next Pointer 40h PCI Express 80h 80h Message Signaled Interrupt (MSI) 90h 90h Subsystem Vendor A0h A0h PCI Power Management 00h Extended PCIe Capability Linked List Offset Capability Next Pointer 100h Advanced Error Reporting 000h **Power Well:** Core

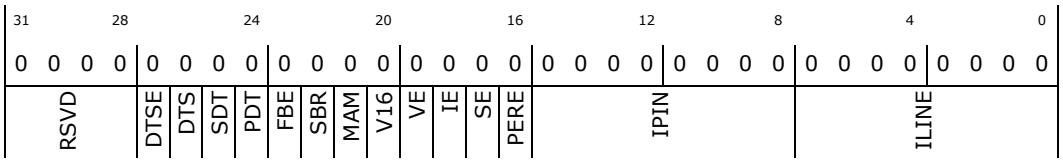
11.3.12 Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 3Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
27	0x0 RW/V2	**Discard Timer SERR# Enable (DTSE):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port. **Power Well:** Core
26	0x0 RO	**Discard Timer Status (DTS):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, this register can remain RO as no secondary discard timer exists that will ever cause it to be set. **Power Well:** Core
25	0x0 RW/V2	**Secondary Discard Timer (SDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port. **Power Well:** Core
24	0x0 RW/V2	**Primary Discard Timer (PDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port. **Power Well:** Core
23	0x0 RO	**Fast Back to Back Enable (FBE):** Reserved per Express spec. **Power Well:** Core
22	0x0 RW	**Secondary Bus Reset (SBR):** Triggers a Hot Reset on the PCI-Express port. **Power Well:** Core
21	0x0 RW/V2	**Master Abort Mode (MAM):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
18	0x0 RW	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh). **Power Well:** Core
17	0x0 RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not. **Power Well:** Core
16	0x0 RW	**Parity Error Response Enable (PERE):** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD. **Power Well:** Core
15:8	0x0 RO/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the STRPFUSECFG register in chipset config space: Port Bits[lb]15:12[rb] Bits[lb]11:08[rb] 1 0h STRPFUSECFG.P1IP 2 0h STRPFUSECFG.P2IP 3 0h STRPFUSECFG.P3IP 4 0h STRPFUSECFG.P4IP 5 0h STRPFUSECFG.P5IP 6 0h STRPFUSECFG.P6IP 7 0h STRPFUSECFG.P7IP 8 0h STRPFUSECFG.P8IP The value that is programmed into STRPFUSECFG is always reflected in this register. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register returns a value of 00h when read, else this register returns the value from the table above. **Power Well:** Core
7:0	0x0 RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. **Power Well:** Core

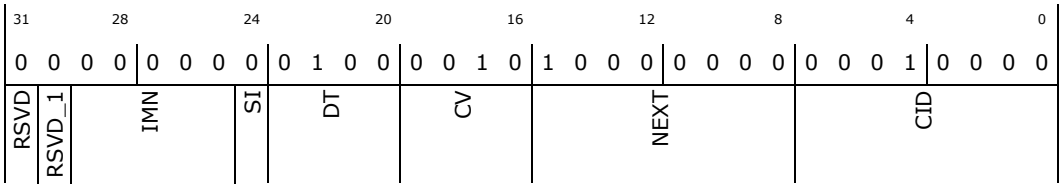
11.3.13 Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 40h

Default: 00428010h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
30	0x0 RO	**Reserved (RSVD_1):** Reserved. This register at one time was for TCS Routing but that was later removed from the PCIe 2.0 spec **Power Well:** Core
29:25	0x0 RO	**Interrupt Message Number (IMN):** The PCIE SIP does not have multiple MSI interrupt numbers. **Power Well:** Core
24	0x0 RW/O	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset. **Power Well:** Core
23:20	0x4 RO	**Device / Port Type (DT):** Indicates this is a PCI-Express root port **Power Well:** Core
19:16	0x2 RO	**Capability Version (CV):** Version 2.0 indicates devices compliant to the PCI Express 2.0 specification which incorporates the Register Expansion ECN. **Power Well:** Core
15:8	0x80 RW/O	**Next Capability (NEXT):** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. **Power Well:** Core
7:0	0x10 RO	**Capability ID (CID):** Indicates this is a PCI Express capability **Power Well:** Core

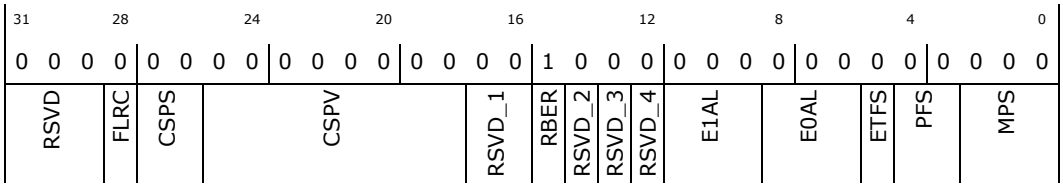
11.3.14 Device Capabilities (DCAP)—Offset 44h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 44h

Default: 00008000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
28	0x0 RO	**Function Level Reset Capable (FLRC):** Not supported in Root Ports **Power Well:** Core
27:26	0x0 RO	**Captured Slot Power Limit Scale (CSPS):** Not supported **Power Well:** Core
25:18	0x0 RO	**Captured Slot Power Limit Value (CSPV):** Not supported **Power Well:** Core
17:16	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
15	0x1 RO	**Role Based Error Reporting (RBER):** When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions. **Power Well:** Core
14	0x0 RO	**Reserved (RSVD_2):** Reserved. On previous version of the specification this was Power Indicator Present (PIP) **Power Well:** Core
13	0x0 RO	**Reserved (RSVD_3):** Reserved. On previous version of the specification this was Attention Indicator Present (AIP) **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12	0x0 RO	**Reserved (RSVD_4):** Reserved. On previous version of the specification this was Attention Button Present (ABP) **Power Well:** Core
11:9	0x0 RO	**Endpoint L1 Acceptable Latency (E1AL):** Reserved for root ports. **Power Well:** Core
8:6	0x0 RO	**Endpoint L0 Acceptable Latency (E0AL):** Reserved for Root port. **Power Well:** Core
5	0x0 RO	**Extended Tag Field Supported (ETFS):** The PCIE SIP never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags. **Power Well:** Core
4:3	0x0 RO	**Phantom Functions Supported (PFS):** No phantom functions supported **Power Well:** Core
2:0	0x0 RW/O	**Max Payload Size Supported (MPS):** BIOS should write to this field during system initialization. Only Max Payload Size of 128B is supported. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. **Power Well:** Core

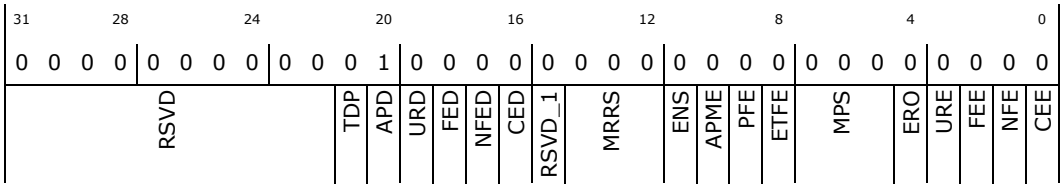
11.3.15 Device Control; Device Status (DCTL_DSTS)—Offset 48h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 48h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID. **Power Well:** Core
20	0x1 RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup **Power Well:** Core
19	0x0 RW/1C/V	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected. **Power Well:** Core
18	0x0 RW/1C/V	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed tlp **Power Well:** Core
17	0x0 RW/1C/V	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned tlp, unexpected completions, unsupported requests, completor abort, or completer timeout **Power Well:** Core
16	0x0 RW/1C/V	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, tlp crc error, dllp crc error, replay num rollover, replay timeout. **Power Well:** Core
15	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
14:12	0x0 RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11	0x0 RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests. **Power Well:** Core
10	0x0 RW/P	**Aux Power PM Enable (APME):** The OS will set this bit to '1' if the device connected has detected aux power. **Power Well:** Core
9	0x0 RO	**Phantom Functions Enable (PFE):** Not supported **Power Well:** Core
8	0x0 RO	**Extended Tag Field Enable (ETFE):** Not supported **Power Well:** Core
7:5	0x0 RW	**Max Payload Size (MPS):** The root port only supports 128B max payload. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. If the DCAP.MPS indicates 128B max payload size support, programming this field to any values other than 128B will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME. **Power Well:** Core
4	0x0 RO	**Enable Relaxed Ordering (ERO):** Not supported **Power Well:** Core
3	0x0 RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**Fatal Error Reporting Enable (FEE):** enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting. **Power Well:** Core
1	0x0 RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting. **Power Well:** Core
0	0x0 RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting. **Power Well:** Core

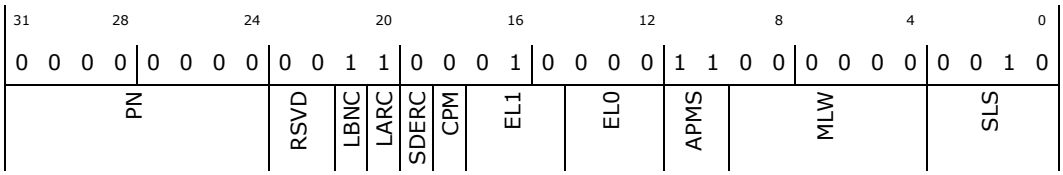
11.3.16 Link Capabilities (LCAP)—Offset 4Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 4Ch

Default: 00310C02h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port # Value of PN field 1 01h 2 02h 3 03h 4 04h **Power Well:** Core
23:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
21	0x1 RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms. **Power Well:** Core
20	0x1 RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. **Power Well:** Core
19	0x0 RO	**Surprise Down Error Reporting Capable (SDERC):** Set to '0' to indicate the root port does not support Surprise Down Error Reporting **Power Well:** Core
18	0x0 RO	**Clock Power Management (CPM):** '0' Indicates that root ports do not support the CLKREQ# mechanism. **Power Well:** Core
17:15	0x2 RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b Less than 1 us 001b 1 us to less than 2 us 010b 2 us to less than 4 us 011b 4 us to less than 8 us 100b 8 us to less than 16 us 101b 16 us to less than 32 us 110b 32 us to 64 us 111b More than 64 us Note: If PXP PLL shutdown is enabled, BIOS should program this latency to comprehend PLL lock latency. **Power Well:** Core
14:12	0x0 RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration: LCTL.CCC Value 0 MPC.UCEL 1 MPC.CCEL **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11:10	0x3 RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00 (Reserved) 01 L0s Entry supported 10 Reserved 11 Both L0s and L1 supported Note: If STRPFUSECFG.ASPMDIS is 1, the default of this field is [quote]01[/quote]. Otherwise, the default of this field is [quote]11[/quote]. If STRPFUSECFG.ASPMDIS is 1, BIOS writing [quote]11[/quote] to this field will have the same effect as [quote]01[/quote]. [quote]01[/quote] will be reflected on this register when read and the register will turn to Read-Only once written once. **Power Well:** Core
9:4	0x0 RO/V	**Maximum Link Width (MLW):** For the root ports, several values can be taken, based upon the value of the chipset configuration register field RPC.PC1 for ports 1-4: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h **Power Well:** Core
3:0	0x2 RO/V	**Supported Link Speeds (SLS):** Indicates the supported link speeds of the Root Port. 0001b 2.5 GT/s Link speed supported 0010b 5.0 GT/s and 2.5GT/s Link speeds supported This register reports a value of 0001b if the Root Port Gen2 Disable Fuse is set or the MPC.PCIEGEN2DIS bit is set, else this register reports a value of 0010b. **Power Well:** Core

11.3.17 Link Control; Link Status (LCTL_LSTS)—Offset 50h

Access Method

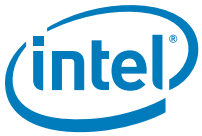
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 50h

Default: 00010000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LABS	LBMS	LA	SCC	LT	RSVD	NLW						CLS				RSVD_1				LABIE	LBMIE	HAWD	ECPM	ES	CCC	RL	LD	RCBC	RSVD_2	ASPM	

Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C/V	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b. **Power Well:** Core
30	0x0 RW/1C/V	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b. **Power Well:** Core
29	0x0 RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise. **Power Well:** Core
28	0x0 RO/V	**Slot Clock Configuration (SCC):** In normal mode, PCIE SIP uses the same reference clock as on the platform and does not generate its own clock. Note: The default of this register bit is dependent on the [quote]PCIe Non-Common Clock With SSC Mode Enable Strap[/quote]. If the strap enables non-common clock with SSC support, this bit shall default to '0'. Otherwise, this bit shall default to '1'. **Power Well:** Core
27	0x0 RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training. **Power Well:** Core
26	0x0 RO	**Reserved (RSVD):** Reserved. Previously this was defined as Link Training Error (LTE) but support for this bit was removed from subsequent versions of the PCI Express specification. **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
25:20	0x0 RO/V	**Negotiated Link Width (NLW):** For the root ports, this register could take on several values: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h The value of this register is undefined if the link has not successfully trained. **Power Well:** Core
19:16	0x1 RO/V	**Current Link Speed (CLS):** 0001b Link is 2.5Gb/s Link 0010b 5.0 GT/s Link The value of this field is undefined if the link is not up. **Power Well:** Core
15:12	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
11	0x0 RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set. **Power Well:** Core
10	0x0 RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/ PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b. **Power Well:** Core
9	0x0 RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Default value of this bit is 0b. **Power Well:** Core
8	0x0 RO	**Enable Clock Power Management (ECPM):** Reserved. Not supported on PCIE SIP Root Ports. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW	**Extended Synch (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0. **Power Well:** Core
6	0x0 RW	**Common Clock Configuration (CCC):** When set, indicates that the PCIE SIP and device are operating with a distributed common reference clock. **Power Well:** Core
5	0x0 WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns '0' when read. Software uses LSTS.LT to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress. **Power Well:** Core
4	0x0 RW	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state. **Power Well:** Core
3	0x0 RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes. **Power Well:** Core
2	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
1:0	0x0 RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used. Note: If STRPFUSECFG.ASPMDIS is '1', hardware will always see [quote]00[/quote] as an output from this register. BIOS reading this register should always return the correct value. **Power Well:** Core

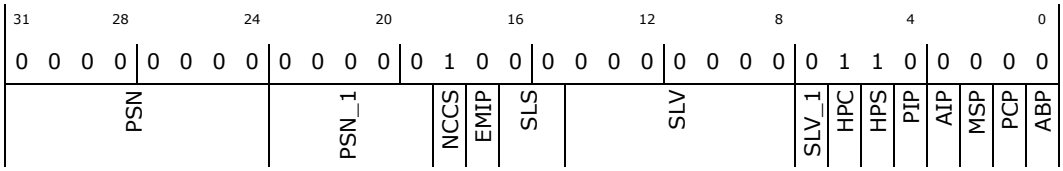
11.3.18 Slot Capabilities (SLCAP)—Offset 54h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 54h

Default: 00040060h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW/O	**Physical Slot Number (PSN):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
23:19	0x0 RW/O	**Physical Slot Number (PSN_1):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
18	0x1 RO	**No Command Completed Support (NCCS):** Set to '1' as this port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes. **Power Well:** Core
17	0x0 RO	**Electromechanical Interlock Present (EMIP):** Set to 0 to indicate that no electro-mechanical interlock is implemented. **Power Well:** Core
16:15	0x0 RW/O	**Slot Power Limit Scale (SLS):** specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
14:8	0x0 RW/O	**Slot Power Limit Value (SLV):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
7	0x0 RW/O	**Slot Power Limit Value (SLV_1):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
6	0x1 RW/O	**Hot Plug Capable (HPC):** When set, Indicates that hot plug is supported. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5	0x1 RW/O	**Hot Plug Surprise (HPS):** When set, indicates the device may be removed from the slot without prior notification. **Power Well:** Core
4	0x0 RO	**Power Indicator Present (PIP):** Indicates that a power indicator LED is not present for this slot. **Power Well:** Core
3	0x0 RO	**Attention Indicator Present (AIP):** Indicates that an attention indicator LED is not present for this slot. **Power Well:** Core
2	0x0 RO	**MRL Sensor Present (MSP):** Indicates that an MRL sensor is not present **Power Well:** Core
1	0x0 RO	**Power Controller Present (PCP):** Indicates that a power controller is not implemented for this slot **Power Well:** Core
0	0x0 RO	**Attention Button Present (ABP):** Indicates that an attention button is not implemented for this slot. **Power Well:** Core

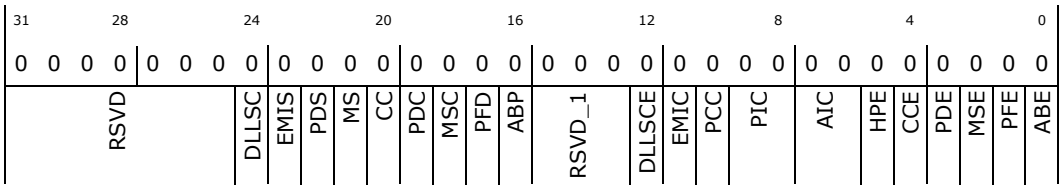
11.3.19 Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 58h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
24	0x0 RW/1C/V	**Data Link Layer State Changed (DLLSC):** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device. **Power Well:** Core
23	0x0 RO	**Electromechanical Interlock Status (EMIS):** Reserved as this port does not support and electromechanical interlock. **Power Well:** Core
22	0x0 RO/V	**Presence Detect State (PDS):** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected ('1') or empty ('0'). If XCAP.SI is cleared, this bit is a '1'. **Power Well:** Core
21	0x0 RO	**MRL Sensor State (MS):** Reserved as the MRL sensor is not implemented. **Power Well:** Core
20	0x0 RO	**Command Completed (CC):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
19	0x0 RW/1C/V	**Presence Detect Changed (PDC):** This bit is set by the root port when the SLSTS.PDS bit changes state. **Power Well:** Core
18	0x0 RO	**MRL Sensor Changed (MSC):** Reserved as the MRL sensor is not implemented. **Power Well:** Core
17	0x0 RO	**Power Fault Detected (PFD):** Reserved as a power controller is not implemented. **Power Well:** Core
16	0x0 RO	**Attention Button Pressed (ABP):** This register is RO as this port does not implement an attention button **Power Well:** Core
15:13	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12	0x0 RW	**Data Link Layer State Changed Enable (DLLSCE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed **Power Well:** Core
11	0x0 RO	**Electromechanical Interlock Control (EMIC):** Reserved as this port does not support an Electromechanical Interlock. **Power Well:** Core
10	0x0 RO	**Power Controller Control (PCC):** This bit has no meaning for module based hot plug. **Power Well:** Core
9:8	0x0 RO	**Power Indicator Control (PIC):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
7:6	0x0 RO	**Attention Indicator Control (AIC):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
5	0x0 RW	**Hot Plug Interrupt Enable (HPE):** When set, enables generation of a hot plug interrupt on enabled hot plug events. **Power Well:** Core
4	0x0 RO	**Command Completed Interrupt Enable (CCE):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
3	0x0 RW	**Presence Detect Changed Enable (PDE):** When set, enables the generation of a hot plug interrupt or wake message when the presence detect logic changes state. **Power Well:** Core
2	0x0 RO	**MRL Sensor Changed Enable (MSE):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
1	0x0 RO	**Power Fault Detected Enable (PFE):** This register is RO as this port does not implement a Hot Plug Controller... **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RO	**Attention Button Pressed Enable (ABE):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core

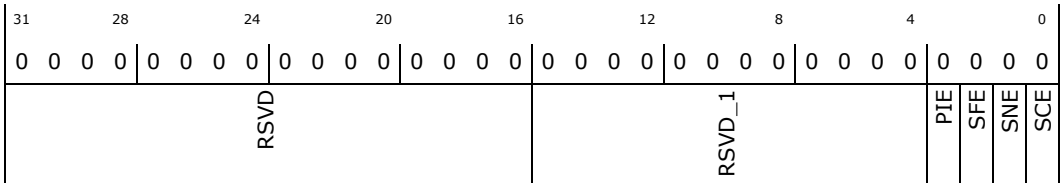
11.3.20 Root Control (RCTL)—Offset 5Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 5Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:4	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
3	0x0 RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a '0' to '1' transition, or due to this bit being set with RSTS.PS already set). **Power Well:** Core
2	0x0 RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set. **Power Well:** Core
1	0x0 RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set. **Power Well:** Core

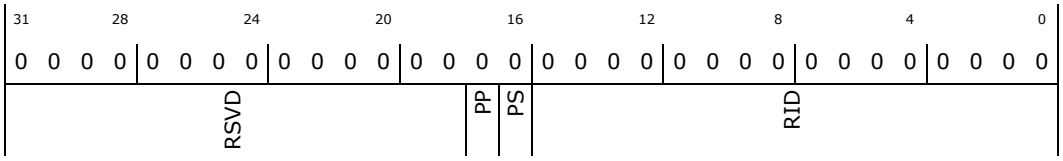
11.3.21 Root Status (RSTS)—Offset 60h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 60h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
17	0x0 RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. PCIE SIP root ports have a one deep PME pending queue. **Power Well:** Core
16	0x0 RW/1C/V	**PME Status (PS):** Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared. **Power Well:** Core
15:0	0x0 RO/V	**PME Requestor ID (RID):** Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set. PCIE SIP root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped. **Power Well:** Core

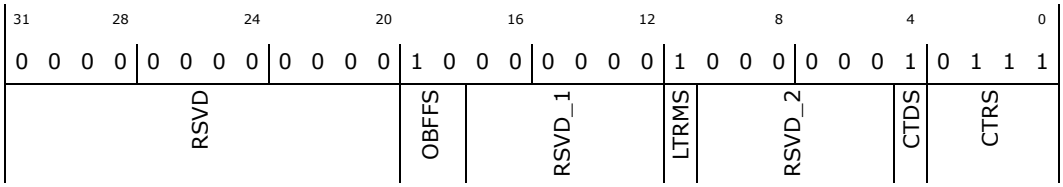
11.3.22 Device Capabilities 2 (DCAP2)—Offset 64h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 64h

Default: 00080817h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
19:18	0x2 RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b - OBFF is not supported. 01b - OBFF is supported using Message signaling only. 10b - OBFF is supported using WAKE# signaling only. 11b - OBFF is supported using WAKE# and Message signaling. BIOS should program this field to 00b or 10b during system initialization to advertise the level of hardware OBFF support to software. BIOS should never program this field to 01b or 11b since OBFF messaging is not supported. **Power Well:** Core
17:12	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
11	0x1 RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a '1' or a '0' to enable/disable the root port from declaring support for the LTR capability. **Power Well:** Core
10:5	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
4	0x1 RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x7 RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A [amp] B 0110b Ranges B [amp] C 0111b Ranges A, B [amp] C [lt]-- This is what IP supports 1110b Ranges B, C [amp] D 1111b Ranges A, B, C [amp] D All other values are reserved. **Power Well:** Core

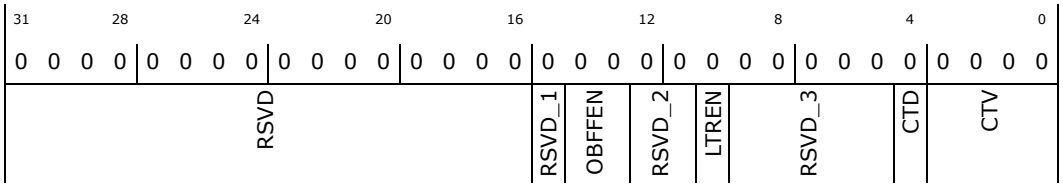
11.3.23 Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 68h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
14:13	0x0 RW	**Optimized Buffer Flush/Fill Enable (OBFFEN):** 00b Disable OBFF mechanism. 01b Enable OBFF mechanism using Message signaling (Variation A). 10b Enable OBFF mechanism using Message signaling (Variation B). 11b Enable OBFF using WAKE# signaling. Note: Only encoding 00b and 11b are supported. The encoding of 01b or 10b would be aliased to 00b. If DCAP2.OBFFS is clear, programming this field to any non-zero values will have no effect. **Power Well:** Core
12:11	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
10	0x0 RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect. **Power Well:** Core
9:5	0x0 RO	**Reserved (RSVD_3):** Reserved **Power Well:** Core
4	0x0 RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x0 RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. ThePCIE SIP targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range A (50us to 10 ms) programmability range is supported: 0001b 90-100us (spec range is 50 us to 100 us) 0010b 9-10ms (spec range is 1ms to 10 ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either when this value was changed or when each request was issued. **Power Well:** Core

11.3.24 Link Capabilities 2 (LCAP2)—Offset 6Ch

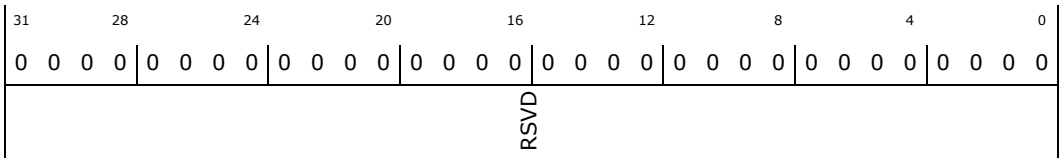
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 6Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

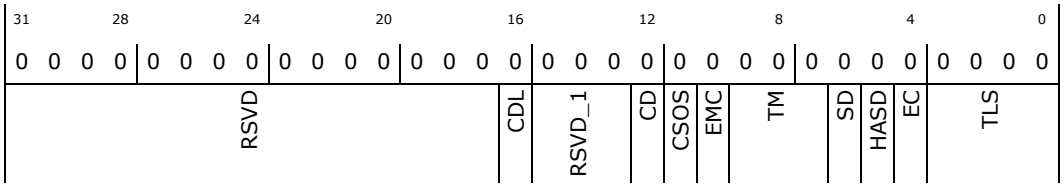
11.3.25 Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 70h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
16	0x0 RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is operating at 2.5 GT/s speed. **Power Well:** Core
15:13	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
12	0x0 RW/P	**Compliance De-emphasis (CD):** This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s, the setting of this bit has no effect. The default value of this bit is 0b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11	0x0 RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b. **Power Well:** Core
10	0x0 RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value. **Power Well:** Core
9:7	0x0 RW/P	**Transmit Margin (TM):** This field controls the value of the nondeemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see PCI Express Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value. **Power Well:** Core
6	0x0 RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RO	**Hardware Autonomous Speed Disable (HASD):** Reserved. This port cannot autonomously change speeds. **Power Well:** Core
4	0x0 RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. **Power Well:** Core
3:0	0x0 RW/V/P	**Target Link Speed (TLS):** This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. For PCIE SIP, the allowed value is: 0001b 2.5 GT/s Target Link Speed 0010b 5.0 GT/s and 2.5GT/s Link speeds supported If a value is written to this field that does not correspond to a speed included in the Supported Link Speeds field, the result is undefined. The default value of this field is the highest Link speed supported by the component (as reported in the Supported Link Speeds field of the Link Capabilities register). **Power Well:** Core

11.3.26 Slot Capabilities 2 (SLCAP2)—Offset 74h

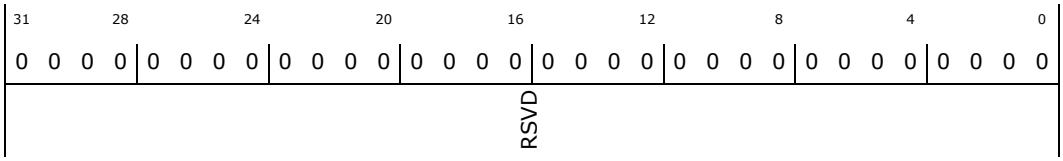
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 74h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

11.3.27 Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h

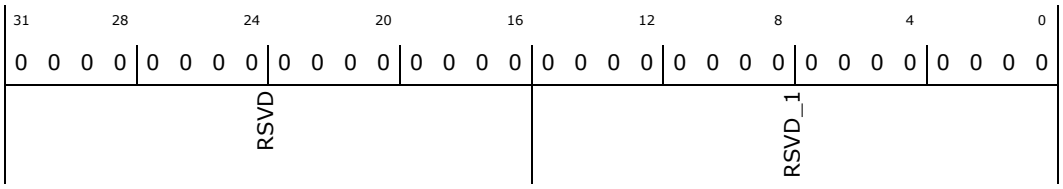
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 78h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:0	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

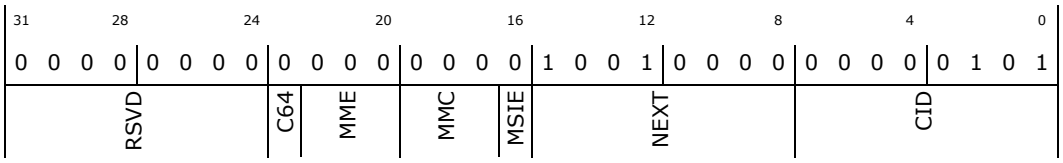
11.3.28 Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 80h

Default: 00009005h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
23	0x0 RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
22:20	0x0 RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port. **Power Well:** Core
19:17	0x0 RO	**Multiple Message Capable (MMC):** Only one message is required. **Power Well:** Core
16	0x0 RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated. **Power Well:** Core
15:8	0x90 RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. **Power Well:** Core
7:0	0x5 RO	**Capability ID (CID):** Capabilities ID indicates MSI. **Power Well:** Core

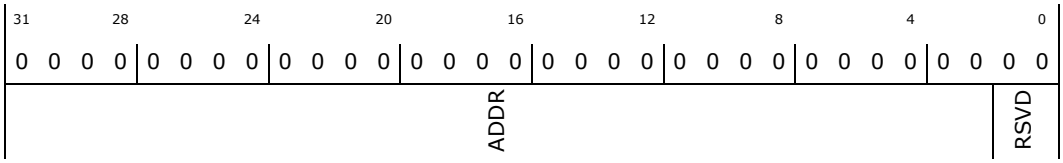
11.3.29 Message Signaled Interrupt Message Address (MA)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 84h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Address (ADDR):** Lower 32 bits of the system specified message address, always DW aligned. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1:0	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

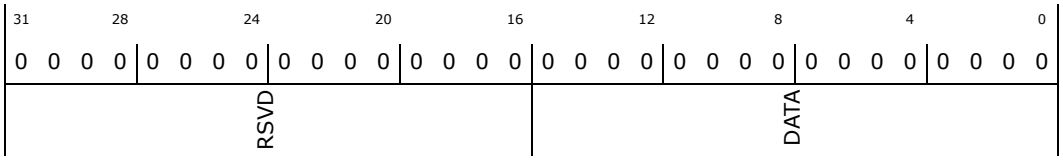
11.3.30 Message Signaled Interrupt Message Data (MD)—Offset 88h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 88h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:0	0x0 RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[lb]15:0[rb]) during the data phase of the MSI memory write transaction. **Power Well:** Core

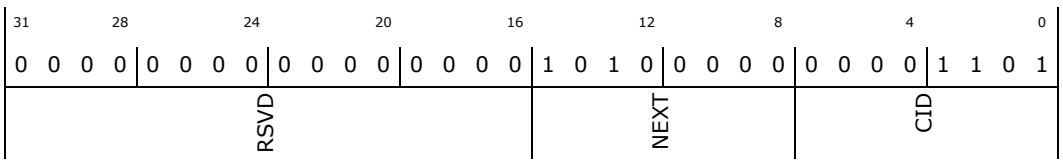
11.3.31 Subsystem Vendor Capability (SVCAP)—Offset 90h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 90h

Default: 0000A00Dh



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:8	0xa0 RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. **Power Well:** Core
7:0	0xd RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability. **Power Well:** Core

11.3.32 Subsystem Vendor IDs (SVID)—Offset 94h

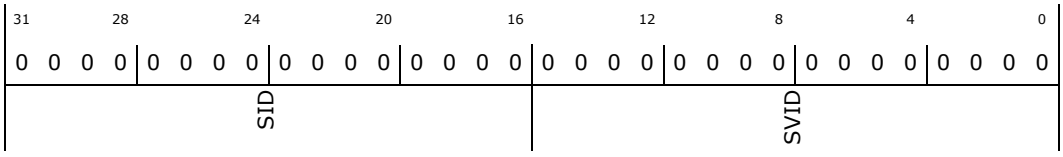
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 94h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset). **Power Well:** Core
15:0	0x0 RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset). **Power Well:** Core

11.3.33 Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h

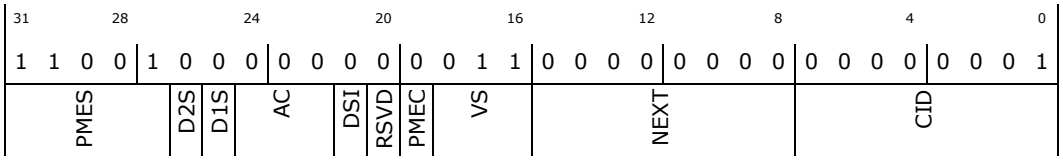
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + A0h

Default: C8030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x19 RO	**PME Support (PMES):** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy Microsoft operating systems to enable PME# in devices connected behind this root port. **Power Well:** Core
26	0x0 RO	**D2_Support (D2S):** The D2 state is not supported. **Power Well:** Core
25	0x0 RO	**D1_Support (D1S):** The D1 state is not supported. **Power Well:** Core
24:22	0x0 RO	**Aux_Current (AC):** Reports 0mA (self-powered), as use of this controller does not add to suspend well power consumption. **Power Well:** Core
21	0x0 RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required. **Power Well:** Core
20	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
19	0x0 RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#. **Power Well:** Core
18:16	0x3 RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Next Capability (NEXT):** Indicates this is the last item in the list. **Power Well:** Core
7:0	0x1 RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability. **Power Well:** Core

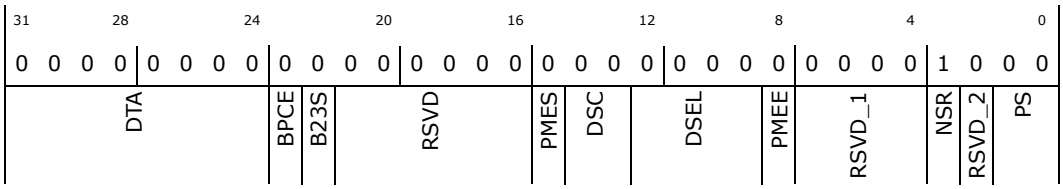
11.3.34 PCI Power Management Control And Status (PMCS)—Offset A4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + A4h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Data (DTA):** Reserved **Power Well:** Core
23	0x0 RO	**Bus Power / Clock Control Enable (BPCE):** Reserved per PCI Express specification **Power Well:** Core
22	0x0 RO	**B2/B3 Support (B23S):** Reserved per PCI Express specification. **Power Well:** Core
21:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15	0x0 RO	**PME Status (PMES):** Indicates a PME was received on the downstream link. **Power Well:** Core
14:13	0x0 RO	**Data Scale (DSC):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12:9	0x0 RO	**Data Select (DSEL):** Reserved **Power Well:** Core
8	0x0 RW/P	**PME Enable (PMEE):** Indicates PME is enabled. The root port takes no action on this bit, but it must be RW for legacy Microsoft operating systems to enable PME# on devices connected to this root port. This register resides in the resume well and is not reset on a resume from S3/S4/S5. The reset for this register is RSMRST# which is not asserted during a Warm Reset. **Power Well:** Core
7:4	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
3	0x1 RW/O	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. **Power Well:** Core
2	0x0 RO	**Reserved (RSVD_2):** Reserved. **Power Well:** Core
1:0	0x0 RW	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 - D0 state 11 - D3HOT state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a '10' or '01' to these bits, the write will be ignored. **Power Well:** Core

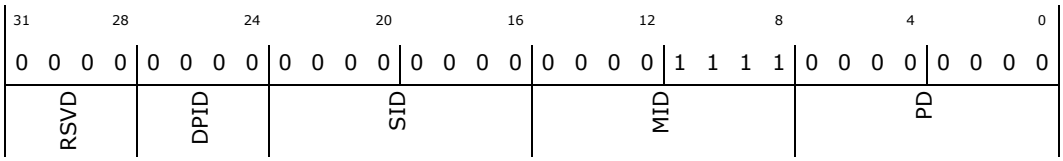
11.3.35 Manufacturer's ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + F8h

Default: 00000F00h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
27:24	0x0 RO/V	**Dot portion of Process ID (DPID):** The value of this field is SoC specific. Example: Process/Dot (PD) is 1265.8. Indicates the dot as .8. **Power Well:** Core
23:16	0x0 RO/V	**Stepping Identifier (SID):** This field is incremented for each stepping of the part. Note that this field can be used by software to differentiate steppings when the Revision ID may not change. A single Manufacturing Stepping ID can be implemented that is readable from all functions in the chip because all of them are incremented in lock-step. **Power Well:** Core
15:8	0xf RO	**Manufacturing Identifier (MID):** 0Fh = Intel **Power Well:** Core
7:0	0x0 RO/V	**Process/Dot (PD):** Indicates the current process. The value of this field is SoC specific. Example: Process/Dot (PD) is 1265.8. Indicates the Process (1265). **Power Well:** Core

11.3.36 Advanced Error Reporting Capability Header (AECH)—Offset 100h

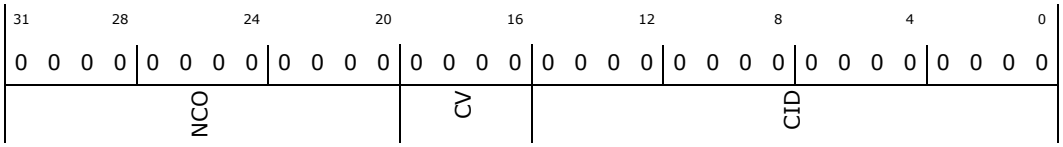
Size:32 bits The AER capability can optionally be included or excluded from the capabilities list. The full AER is supported.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 100h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW/O	**Next Capability Offset (NCO):** Set to 000h as this is the last capability in the list. **Power Well:** Core
19:16	0x0 RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0 **Power Well:** Core
15:0	0x0 RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0 **Power Well:** Core

11.3.37 Uncorrectable Error Status (UES)—Offset 104h

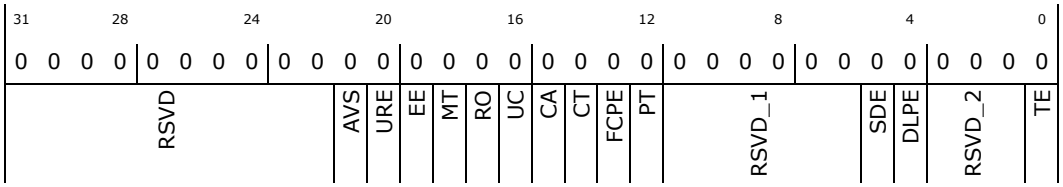
This register must maintain its state through a platform reset. It loses its state upon loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 104h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported **Power Well:** Core
20	0x0 RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received. **Power Well:** Core
19	0x0 RO	**ECRC Error Status (EE):** ECRC is not supported. **Power Well:** Core
18	0x0 RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received. **Power Well:** Core
17	0x0 RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred. **Power Well:** Core
16	0x0 RW/1C/V/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received. **Power Well:** Core
15	0x0 RW/1C/V/P	**Completor Abort Status (CA):** Indicates a completer abort was received **Power Well:** Core
14	0x0 RW/1C/V/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value **Power Well:** Core
13	0x0 RO	**Flow Control Protocol Error Status (FCPE):** Not supported. **Power Well:** Core
12	0x0 RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received. **Power Well:** Core
11:6	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RO	**Surprise Down Error Status (SDE):** Surprise Down is not supported. **Power Well:** Core
4	0x0 RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred. **Power Well:** Core
3:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x0 RO	**Training Error Status (TE):** Not supported. **Power Well:** Core

11.3.38 Uncorrectable Error Mask (UEM)—Offset 108h

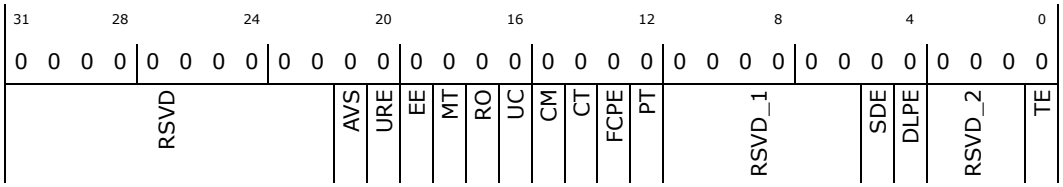
When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 108h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported **Power Well:** Core
20	0x0 RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RO	**ECRC Error Mask (EE):** ECRC is not supported. **Power Well:** Core
18	0x0 RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs **Power Well:** Core
17	0x0 RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows. **Power Well:** Core
16	0x0 RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions. **Power Well:** Core
15	0x0 RW/P	**Completor Abort Mask (CM):** Mask for completer abort. **Power Well:** Core
14	0x0 RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts. **Power Well:** Core
13	0x0 RO	**Flow Control Protocol Error Mask (FCPE):** Not supported. **Power Well:** Core
12	0x0 RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs. **Power Well:** Core
11:6	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
5	0x0 RO	**Surprise Down Error Mask (SDE):** Surprise Down is not supported. **Power Well:** Core
4	0x0 RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors. **Power Well:** Core
3:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x0 RO	**Training Error Mask (TE):** Not supported. **Power Well:** Core

11.3.39 Uncorrectable Error Severity (UEV)—Offset 10Ch

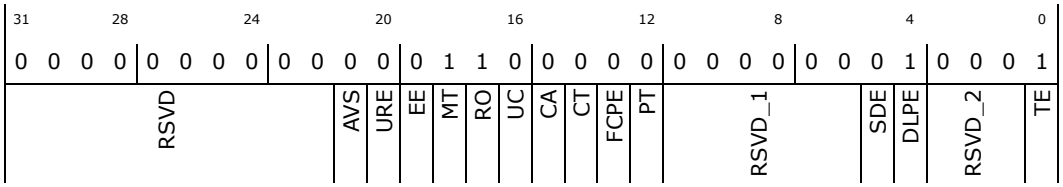
This register gives the option to make an uncorrectable error fatal or non-fatal. An error is fatal if the bit is set. An error is non-fatal if the bit is cleared. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 10Ch

Default: 00060011h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**ACS Violation Severity (AVS):** Reserved. Access Control Services are not supported **Power Well:** Core
20	0x0 RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception. **Power Well:** Core
19	0x0 RO	**ECRC Error Severity (EE):** ECRC is not supported. **Power Well:** Core
18	0x1 RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception. **Power Well:** Core
17	0x1 RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences. **Power Well:** Core
16	0x0 RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception. **Power Well:** Core
15	0x0 RW/P	**Completor Abort Severity (CA):** Severity for completer abort. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout. **Power Well:** Core
13	0x0 RO	**Flow Control Protocol Error Severity (FCPE):** Not supported. **Power Well:** Core
12	0x0 RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception. **Power Well:** Core
11:6	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
5	0x0 RO	**Surprise Down Error Severity (SDE):** Surprise Down is not supported. **Power Well:** Core
4	0x1 RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors. **Power Well:** Core
3:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x1 RO	**Training Error Severity (TE):** TE not supported. This bit is left as RO='1' for ease of implementation.. **Power Well:** Core

11.3.40 Correctable Error Status (CES)—Offset 110h

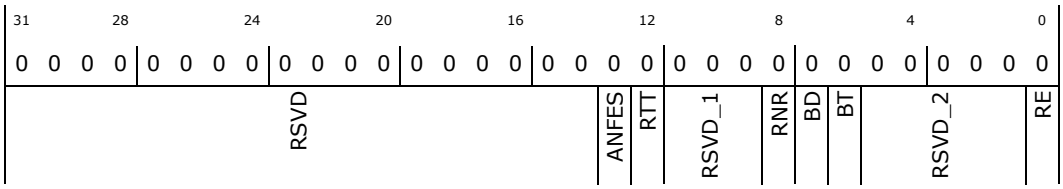
This register is only reset by a loss of core power

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 110h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
13	0x0 RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that a Advisory Non-Fatal Error occurred. **Power Well:** Core
12	0x0 RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out. **Power Well:** Core
11:9	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
8	0x0 RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over. **Power Well:** Core
7	0x0 RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received. **Power Well:** Core
6	0x0 RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received. **Power Well:** Core
5:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x0 RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred. **Power Well:** Core

11.3.41 Correctable Error Mask (CEM)—Offset 114h

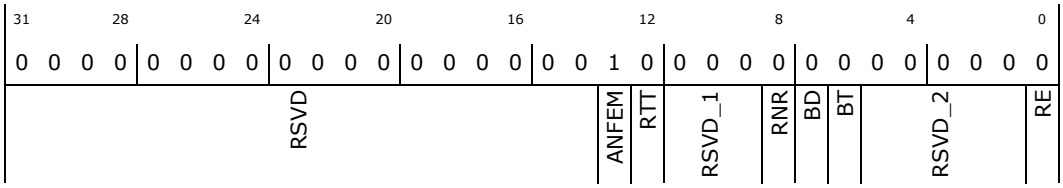
When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 114h

Default: 00002000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
13	0x1 RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting. **Power Well:** Core
12	0x0 RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout. **Power Well:** Core
11:9	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
8	0x0 RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover. **Power Well:** Core
7	0x0 RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception. **Power Well:** Core
6	0x0 RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception. **Power Well:** Core
5:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x0 RW/P	**Receiver Error Mask (RE):** Mask for receiver errors. **Power Well:** Core

11.3.42 Advanced Error Capabilities and Control (AECC)—Offset 118h

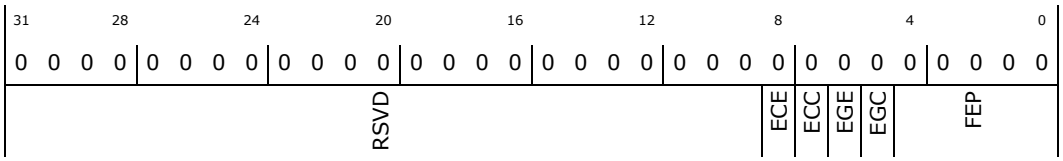
This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 118h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
8	0x0 RO	**ECRC Check Enable (ECE):** ECRC is not supported. **Power Well:** Core
7	0x0 RO	**ECRC Check Capable (ECC):** ECRC is not supported. **Power Well:** Core
6	0x0 RO	**ECRC Generation Enable (EGE):** ECRC is not supported. **Power Well:** Core
5	0x0 RO	**ECRC Generation Capable (EGC):** ECRC is not supported. **Power Well:** Core
4:0	0x0 RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register. **Power Well:** Core

11.3.43 Header Log DW1 (HL_DW1)—Offset 11Ch

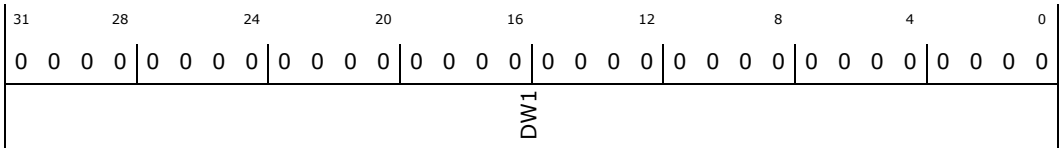
Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 11Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO/V/P	**1st dWord of TLP (DW1):** Byte0 [amp][amp] Byte1 [amp][amp] Byte2 [amp][amp] Byte3 **Power Well:** Core

11.3.44 Header Log DW2 (HL_DW2)—Offset 120h

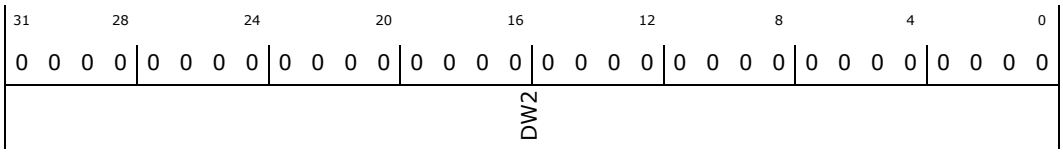
Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 120h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO/V/P	**2nd dWord of TLP (DW2):** Byte4 [amp][amp] Byte5 [amp][amp] Byte6 [amp][amp] Byte7 **Power Well:** Core

11.3.45 Header Log DW3 (HL_DW3)—Offset 124h

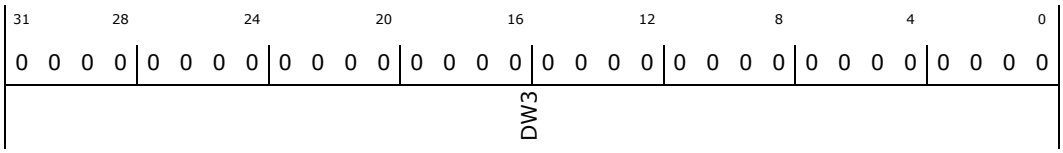
Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 124h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO/V/P	**3rd dWord of TLP (DW3):** Byte8 [amp][amp] Byte9 [amp][amp] Byte10 [amp][amp] Byte11 **Power Well:** Core

11.3.46 Header Log DW4 (HL_DW4)—Offset 128h

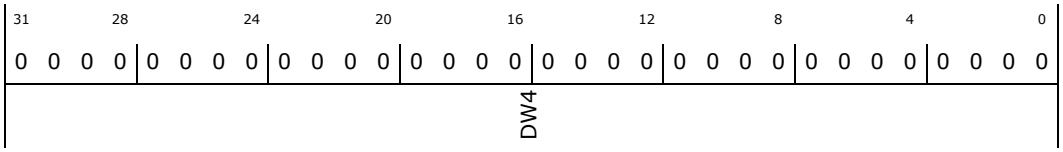
Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 128h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO/V/P	**4th dWord of TLP (DW4):** Byte12 [amp][amp] Byte13 [amp][amp] Byte14 [amp][amp] Byte15 **Power Well:** Core

11.3.47 Root Error Command (REC)—Offset 12Ch

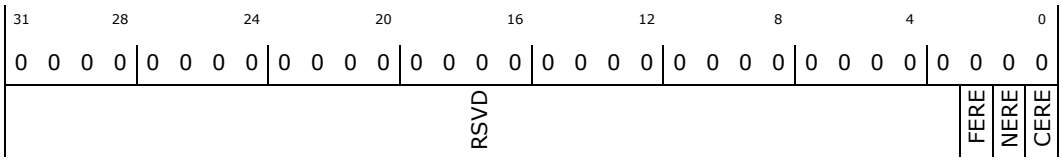
This register allows errors to generate interrupts.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 12Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
2	0x0 RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device. **Power Well:** Core
1	0x0 RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device. **Power Well:** Core
0	0x0 RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device. **Power Well:** Core

11.3.48 Root Error Status (RES)—Offset 130h

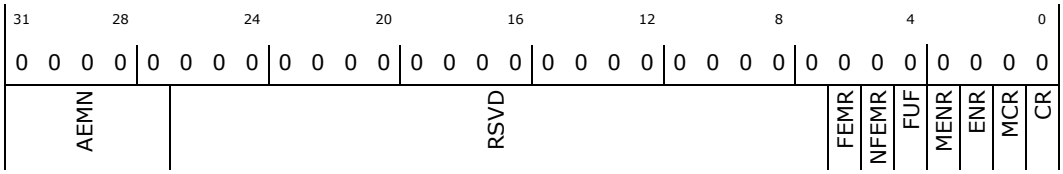
This register can track more than one error and set the [quote]multiple[/quote] bits if a second or subsequent error occurs and the first has not been serviced. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 130h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**Advanced Error Interrupt Message Number (AEMN):** Reserved. There is only one error interrupt allocated. **Power Well:** Core
26:7	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
6	0x0 RW/1C/V/P	**Fatal Error Message Received (FEMR):** Set when one or more Fatal Uncorrectable Error Messages have been received. **Power Well:** Core
5	0x0 RW/1C/V/P	**Non-Fatal Error Messages Received (NFEMR):** Set when one or more Non-Fatal Uncorrectable error messages have been received **Power Well:** Core
4	0x0 RW/1C/V/P	**First Uncorrectable Fatal (FUF):** Set when the first Uncorrectable Error message received is for a fatal error. **Power Well:** Core
3	0x0 RW/1C/V/P	**Multiple ERR_FATAL/NONFATAL Received (MENR):** Set when either a fatal or a non-fatal error is received and the ENR bit is already set. **Power Well:** Core
2	0x0 RW/1C/V/P	**ERR_FATAL/NONFATAL Received (ENR):** Set when either a fatal or a non-fatal error message is received. **Power Well:** Core
1	0x0 RW/1C/V/P	**Multiple ERR_COR Received (MCR):** Set when a correctable error message is received and the CR bit is already set. **Power Well:** Core
0	0x0 RW/1C/V/P	**ERR_COR Received (CR):** Set when a correctable error message is received. **Power Well:** Core

11.3.49 Error Source Identification (ESID)—Offset 134h

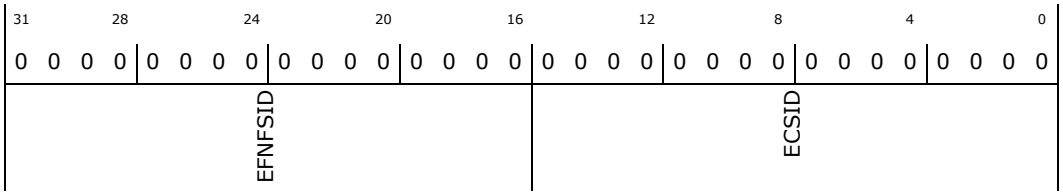
Size:32 bits Identifies the source (Requester ID) of the first correctable and uncorrectable (Non-Fatal / Fatal) errors reported in the Root Error Status register. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 134h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message with the ERR_FATAL/NONFATAL Received register is not already set. **Power Well:** Core
15:0	0x0 RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the Requester ID indicated in the received ERR_COR Message with the ERR_COR Received register is not already set. **Power Well:** Core

11.3.50 L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h

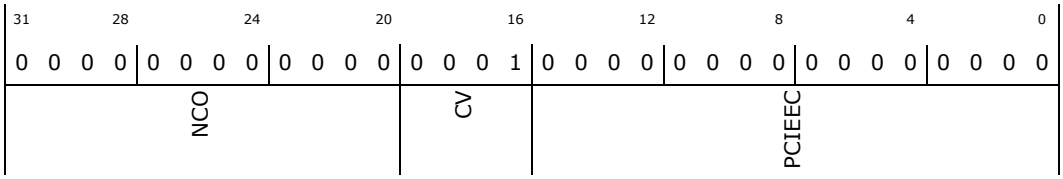
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 200h

Default: 00010000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits. **Power Well:** Core
19:16	0x1 RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW/O	**PCI Express Extended Capability ID (PCIEEC):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for L1 Substates is [lt]TBD[gt]. **Power Well:** Core

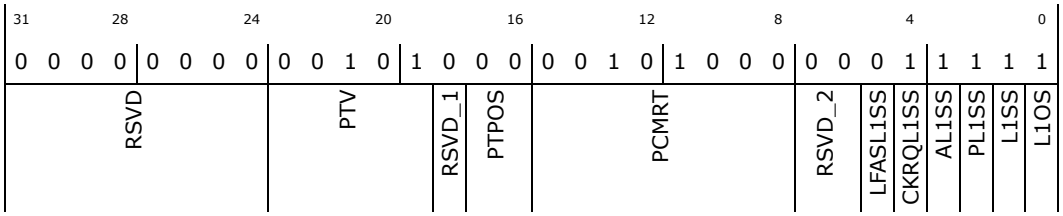
11.3.51 L1 Sub-States Capabilities (L1SCAP)—Offset 204h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 204h

Default: 0028281Fh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
23:19	0x5 RW/O	**Port Tpower_on Value (PTV):** Along with the Port T_POWER_ON Scale Field in the L1 Substates Capabilities register sets theTime (in us) that this Port requires the port on the opposite side of Link to wait in L1.OFF_EXIT after sampling CLKREQ# asserted before actively driving the interface. Port Tpower_on is calculated by multiplying the value in this field by the value in the Port Tpower_on scale field in the L1 Sub-States Capabilities 2 register. Required for all Ports that support L1.OFF. **Power Well:** Core
18	0x0 RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
17:16	0x0 RW/O	**Port Tpower_on Scale (PTPOS):** Specifies the scale used for Tpower_on value field in the L1 Substates Capabilities register. [quote]00b[/quote]: 2 us [quote]01b[/quote]: 10 us [quote]10b[/quote]: 100 us [quote]11b[/quote]: Reserved Required for all Ports that support L1.OFF. **Power Well:** Core
15:8	0x28 RW/O	**Port Common Mode Restore Time (PCMRT):** This is the time (in us) required for this Port to re-establish common mode. Required for all ports that support L1.OFF. **Power Well:** Core
7:6	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
5	0x0 RO	**LFAS L1 Substates Supported (LFASL1SS):** When Set this bit indicates that this Port supports the LFAS mechanism. Required for both Upstream and Downstream Ports. **Power Well:** Core
4	0x1 RO	**CLKREQ# L1 Substates Supported (CKRQL1SS):** When Set this bit indicates that this Port supports the CLKREQ# out-of-band wake mechanism. Required for both Upstream and Downstream Ports. **Power Well:** Core
3	0x1 RW/O	**ASPM L1 Substates Supported (AL1SS):** When set, this bit indicates that this port supports L1 substates for ASPM L1. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static **Power Well:** Core
2	0x1 RW/O	**PCI-PM L1 Substates Supported (PL1SS):** When set, this bit indicates that this port supports L1 substates for PCI-PM. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1	0x1 RW/O	**L1.SNOOZ Supported (L1SS):** When set, this bit indicates that L1.SNOOZ sub-state is supported and this bit must be set by all ports implementing L1 Sub-States. A port that supports L1.OFF must support L1.SNOOZ. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static **Power Well:** Core
0	0x1 RW/O	**L1.OFF Supported (L1OS):** When set, this bit indicates that L1.OFF power management feature is supported. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static **Power Well:** Core

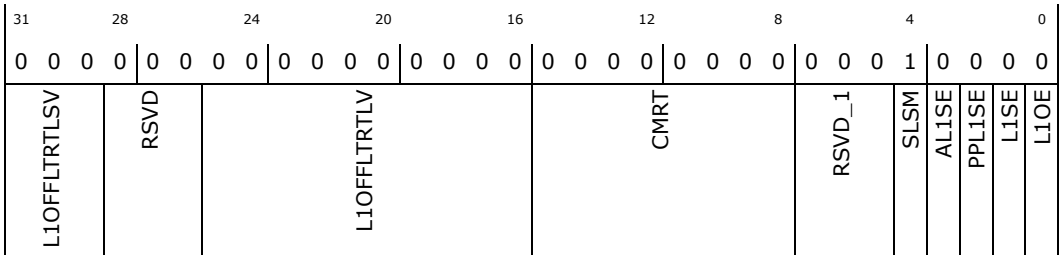
11.3.52 L1 Sub-States Control 1 (L1SCTL1)—Offset 208h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 208h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**L1.OFF LTR Threshold Latency ScaleValue (L1OFFLTRTLSV):** This field contains the L1.OFF LTR Threshold Latency Scale Value for this particular PCIe root port. The value in this field, together with L1OFFLTRTLV is compared against both the snoop and non-snoop LTR values of the device. 000: L1OFFLTRSTLV times 1 ns 001: L1OFFLTRSTLV times 32 ns 010: L1OFFLTRSTLV times 1024 ns 011: L1OFFLTRSTLV times 32768 ns 100: L1OFFLTRSTLV times 1048576 ns 101: L1OFFLTRSTLV times 33554432 ns Others: Not Permitted. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
28:26	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
25:16	0x0 RW	**L1.OFF LTR Threshold Latency Value (L1OFFLTRTLV):** This field contains the L1.OFF LTR Threshold Latency Value for this particular PCIe root port. The value in this field, together with L1OFFLTRTLSV is compared against both the snoop and non-snoop LTR values of the device. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static **Power Well:** Core
15:8	0x0 RW	**Common Mode Restore Time (CMRT):** This is the Tcommon_mode time the PCIe root port needs to continue sending TS1 and refrain from sending TS2 in Recovery state to allow the TX common mode to be established prior to sending TS2. The timer starts from the time when the first TS1 has been sent and the receiver has detected un-squelch. The value in this field defines the time in micro-seconds. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static **Power Well:** Core
7:5	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
4	0x1 RO	**Select L1 Substates Mechanism (SLSM):** When Set this bit indicates that this Port must use the CLKREQ#-based mechanism, when Clear the LFAS mechanism must be used. Ports that support only one mechanism for L1 Substates are permitted to implement this bit as RO/HwInit, and the value of this bit must reflect the supported mechanism. Default value is implementation-specific. **Power Well:** Core
3	0x0 RW	**ASPM L1 Substates Enabled (AL1SE):** When set, this bit indicates that L1 substates are enabled for ASPM. Required for both upstream and downstream ports. Register Attribute: Dynamic **Power Well:** Core
2	0x0 RW	**PCI-PM L1 Substates Enabled (PPL1SE):** When set, this bit indicates that L1 substates are enabled for PCI-PM. Required for both upstream and downstream ports. Register Attribute: Dynamic **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**L1.SNOOZ Enable (L1SE):** When set, this bit indicates that L1.SNOOZ power management feature is enabled. If L1.OFF is enabled, L1.SNOOZ must also be enabled. This field must be programmed prior to enabling ASPM L1. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. **Power Well:** Core
0	0x0 RW	**L1.OFF Enable (L1OE):** When set, this bit indicates that L1.OFF power management feature is enabled. L1.OFF can only be enabled if the platform supports bi-directional CLKREQPLUS#. This field must be programmed prior to enabling ASPM L1. Ports that support L1.OFF shall support Latency Tolerance Reporting. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. **Power Well:** Core

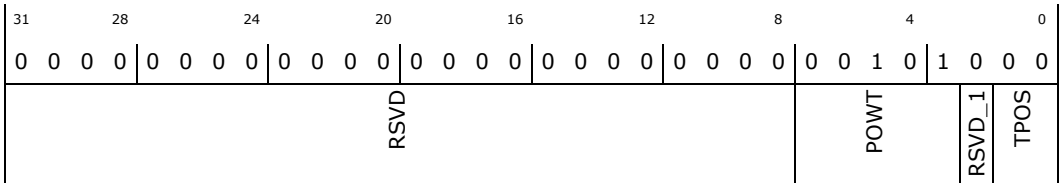
11.3.53 L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 20Ch

Default: 00000028h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
7:3	0x5 RW	**Power On Wait Time (POWT):** Along with the Tpower_on Scale sets the minimum amount of time (in us) that the Port must wait in L1.OFF EXIT after sampling CLKREQPLUS# asserted before actively driving the interface. The timer starts counting when CLKREQPLUS# asserts in L1.OFF state. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
1:0	0x0 RW	**Tpower_on Scale (TPOS):** Specifies the scale used for Tpower_on value. '00b': 2 us '01b': 10 us '10b': 100us '11b': Reserved. Required for all Ports that support L1.OFF. Register Attribute: Static **Power Well:** Core

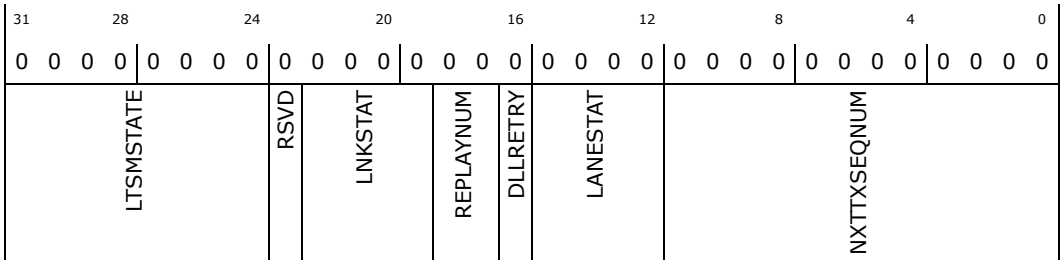
11.3.54 PCI Express Status 1 (PCIESTS1)—Offset 328h

Access Method

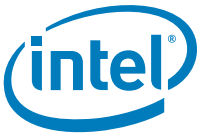
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 328h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO/V	**LTSM State (LTSMSTATE):** Indicates the LTSM present state. Hex LTSSM States 00DETIDLE 01DETRDY 02DETIDLEP1TOP2 03DETRDYP2TOP1 04DETRDYINP1 05DETRDYINP1EXE 06DETP2POLLSTART 07DETP1POLLSTART 08DETP2TOP0 09DETP1TOP0 0AECPCMPRETRAIN 0BECPCMFAILP0TOP2 0C DETP0TOP2 0D PMODECHANGE 0EECPCMPCIE 0FECPCMUSB3



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO/V	10DET2POLLINP0 11POLLINGACTIVE 12POLLINGCOMPLIANCEMARGINCNT 13POLLINGCOMPLIANCE 14POLLINGCOMPLIANCESPEEDUP 15POLLINGCOMPLIANCESPEEDDN 16POLLINGCOMPLIANCESPEEDTXEIDLE 17POLLINGCOMPLIANCESPEEDRXEIDLE 18POLLINGCOMPLIANCESPEED 19POLLINGCOMPLIANCESPEEDDONE 1APOLLINGCOMPLIANCEEXIT 1BPOLLINGCONFIGURATION 1C POLLINGTXEIDLE 1D POLLINGEND 1EPOLLINGENDWAIT 1FLINKWIDTHSTART 20LINKWIDTHACCEPT 21LANENUMWAIT 22LANENUMACCEPT 23LANEDESKEW 24CONFIGCOMPLETE 25CONFIGIDLE 26LWNEXITRECOVERY 27CONFIGLPBKENTRY 28CONFIGLPBKLWSTART 29CONFIGLPBKSPEEDTXEIDLE 2ACONFIGLPBKSPEEDSTART 2BCONFIGLPBKSPEEDRXEIDLE 2C CONFIGLPBKSPEED 2D CONFIGLPBKREUTSKIP 2ECONFIGLPBKREUT 2FCONFIGLPBKEXITM 30CONFIGLPBKTXEIDLE 31LWNEXIT 32LWNLNK2DETECT 33L0 34TXL0SRXL0 35RXL0STXL0 36TXL0SRXL0S 37L1TXEIDLE 38L1RCVEIDLE 39L1PREENTRY 3AL1ENTRY 3BL1IDLE 3C L1IDLEGEN2WAIT 3D L1EXIT 3EL2TXEIDLE 3FL2RCVEIDLE 40L2IDLEWAIT 41L2IDLERDY 42L2IDLE 43LOOPBACKENTRY 44LPBKACTIVEMTXSKP 45LPBKACTIVEMSKPDSKW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO/V	46LOOPBACKACTIVEM 47LPBKSLAVESPEEDTXEIDLE 48LPBKSLAVESPEEDRXEIDLE 49LPBKSLAVESPEED 4ALOOPBACKACTIVES 4BLOOPBACKCMMSKP 4C LOOPBACKCMM 4D LOOPBACKEXITM 4ELOOPBACKEXITS 4FLOOPBACKEXITL0 50LOOPBACKLNK2DETECT 51LOOPBACK2DETECT 52DISTX16TS1DIS 53DISTXEIDLE 54DISWAITSTART 55DISWAITGNT 56DISWAIT4TXMARGIN 57DISWAIT 58DIS2DETECT 59HOTRESETTS1 5AHOTRESETDONE 5BHOTRESETEIDLE 5C RECOVERYRCVRWAIT 5D RECOVERYRCVRMARGINCNT 5ERECOVERYRCVRLOCK 5FRECOVERYDESKEW 60RECOVERYRCVRCFG 61RECOVERYSPEED 62RECOVERYSPEEDTXEIDLE 63RECOVERYSPEEDRXEIDLE 64RECOVERYSPEEDREADY 65RECOVERYIDLE 66RECOVERYEXITDETECT 67RECOVERYLNK2DETECT 68RECOVERYEXITLPBK 69RECOVERYEXITL0 6ARECOVERYEXITDIS 6BRECOVERYEXITRST Note: This register field could be used by REUT software to monitor the link LTSSM substates. **Power Well:** Core
23	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
22:19	0x0 RO/V	**Link Status (LNKSTAT):** During Link initialization the Link will always traverse this list of state from the top (0000) to the bottom of the list (0111). One or more power management states may be skipped, but the direction of list traversal will remain the same. 0000 Link Down 0001 : Link Retrain 0011 : L1 0100 : L2 0101 : L3 0111 : L0 (Link Up) 1000 : L0s (Transmit [amp] Receive) 1001 : L0s (Transmit only) 1010 : L0s (Receive only) All others reserved **Power Well:** Core
18:17	0x0 RO/V	**Replay Number (REPLAYNUM):** Number of times the Retry Buffer has been replayed since the last Link initialization / re-training. When the Data Link Layer has replayed the contents of the Retry Buffer four times a Link re-training will be initiated which will reset this value back to zero. **Power Well:** Core
16	0x0 RO/V	**Data Link Layer Retry (DLLRETRY):** Indicates when the Data Link Layer has received a corrupted TLP or has detected a dropped packet and is currently waiting for the remote agent to re-transmit the corrupted/dropped packet. The value of Next Receive Sequence Number will be the sequence number associated with the corrupted packet. **Power Well:** Core
15:12	0x0 RO/V	**Lane Status (LANESTAT):** Indicates which lanes are trained. A '1' indicates that the corresponding lane is trained (i.e. bit 0 = '1' means lane 0 is trained). **Power Well:** Core
11:0	0x0 RO/V	**Next Transmitted Sequence Number (NXTTXSEQNUM):** This is the sequence number to be applied to and pre-pended to the next outgoing TLP. **Power Well:** Core

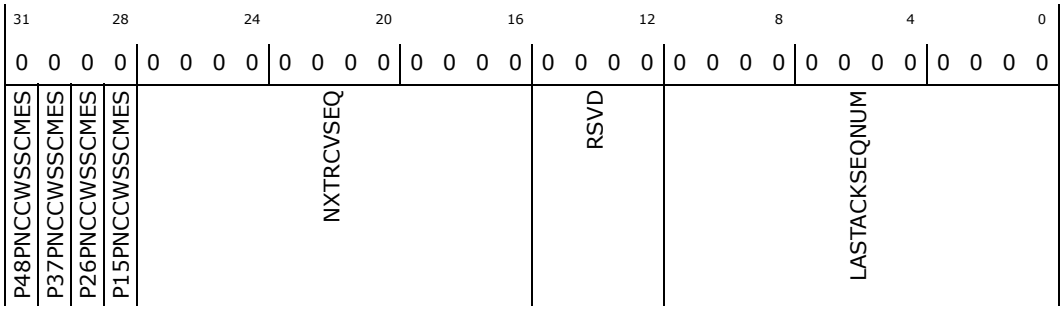
11.3.55 PCI Express Status 2 (PCIESTS2)—Offset 32Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 32Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO/V	**PCIe Port 4 Non-Common Clock With SSC Mode Enable Strap (P48PNCCWSSCMES):** '0': PCIe port 4 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 4 is enabled to operate in non-common clock mode with SSC enabled. **Power Well:** Core
30	0x0 RO/V	**PCIe Port 3 Non-Common Clock With SSC Mode Enable Strap (P37PNCCWSSCMES):** '0': PCIe port 3 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 3 is enabled to operate in non-common clock mode with SSC enabled. **Power Well:** Core
29	0x0 RO/V	**PCIe Port 2 Non-Common Clock With SSC Mode Enable Strap (P26PNCCWSSCMES):** '0': PCIe port 2 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 2 is enabled to operate in non-common clock mode with SSC enabled. **Power Well:** Core
28	0x0 RO/V	**PCIe Port 1 Non-Common Clock With SSC Mode Enable Strap (P15PNCCWSSCMES):** '0': PCIe port 1 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 1 is enabled to operate in non-common clock mode with SSC enabled. **Power Well:** Core
27:16	0x0 RO/V	**Next Receive Sequence Number (NXTRCVSEQ):** This is the sequence number associated with the TLP that is expected to be received next. **Power Well:** Core
15:12	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11:0	0x0 RO/V	**Last Acknowledged Sequence Number (LASTACKSEQNUM):** This is the sequence number associated with the last acknowledged TLP. **Power Well:** Core

11.3.56 PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h

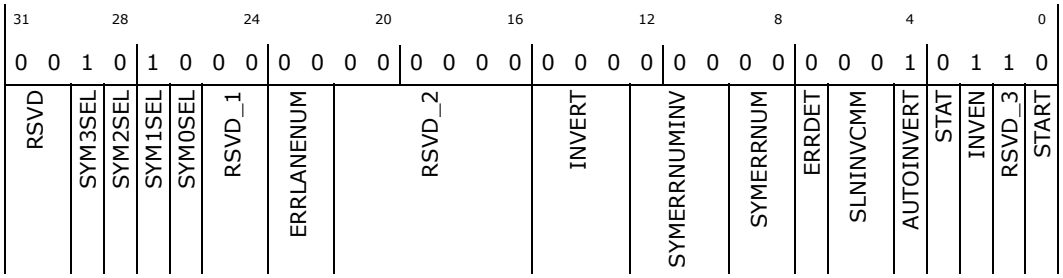
Note that selecting a lane number that does not exist for a port may result in undefined behavior.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 330h

Default: 28000016h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
29	0x1 RW	**CMM Symbol[3] Select (SYM3SEL):** 0: selects CMM Symbol [lb]3[rb] to a control character 1: selects CMM Symbol [lb]3[rb] as a data character **Power Well:** Core
28	0x0 RW	**CMM Symbol[2] Select (SYM2SEL):** 0: selects CMM Symbol [lb]2[rb] to a control character 1: selects CMM Symbol [lb]2[rb] as a data character **Power Well:** Core
27	0x1 RW	**CMM Symbol[1] Select (SYM1SEL):** 0: selects CMM Symbol [lb]1[rb] to a control character 1: selects CMM Symbol [lb]1[rb] as a data character **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
26	0x0 RW	**CMM Symbol[0] Select (SYM0SEL):** 0: selects CMM Symbol [lb]0[rb] to a control character 1: selects CMM Symbol [lb]0[rb] as a data character **Power Well:** Core
25:24	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
23:22	0x0 RO/V	**CMM Error Lane Number (ERRLANENUM):** This field contains the lane number of the failing lane. Only valid when CMM Error Detected is 1. **Power Well:** Core
21:16	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
15:13	0x0 RO/V	**CMM Invert (INVERT):** Indicates which lanes are inverted 000: No inversion 001: Lanes 0 010: Lanes 1 011: Lanes 2 100: Lanes 3 This field is only valid when CMM Error Detected (bit 7) is asserted. Additionally, when CMM Error Detected is asserted this field is locked (will not be updated) **Power Well:** Core
12:10	0x0 RO/V	**CMM Symbol Error Number Invert (SYMERRNUMINV):** Indicates which register number miscompared on the failing lane, if the failing lane was an inverted lane. Only valid when CMM Error Detected is 1. 000: CMM Data D0 001: CMM Data D0 010: CMM Data D0 011: CMM Data D1 100: CMM Data D2 101: CMM Data D3 110: CMM Data D0 111: CMM Data D0 **Power Well:** Core
9:8	0x0 RO/V	**CMM Symbol Error Number (SYMERRNUM):** Indicates which register number miscompared on the failing lane, if the failing lane was not inverted. Only valid when CMM Error Detected is 1. 00: CMM Data 0 01: CMM Data 1 10: CMM Data 2 11: CMM Data 3 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW/1C/V	**CMM Error Detected (ERRDET):** 1: An error was detected 0: No error detected Note: This bit will be shadowed to an observability pin that can be used for IRQ generation. **Power Well:** Core
6:5	0x0 RW	**Select Lane Number to be inverted for CMM (SLNINVCMM):** Select Lane Number to be inverted for CMM **Power Well:** Core
4	0x1 RW	**CMM AutoInvert (AUTOINVERT):** 1: CMM auto sequences through the inversion 0: CMM does not sequence inversion **Power Well:** Core
3	0x0 RO/V	**CMM Status (STAT):** This bit is set when the CMM Start bit is set and cleared when the CMM mode has been entered successfully. 0: Compliance Measurement Mode is not active or CMM mode has been entered successfully. 1: Set as a result of CMM Start bit being set. **Power Well:** Core
2	0x1 RW	**CMM Invert Enable (INVEN):** 1: Enables the Inversion of the lane 0: Lane not inverted **Power Well:** Core
1	0x1 RW	**Reserved (RSVD_3):** Reserved. **Power Well:** Core
0	0x0 RW/L	**CMM Start (START):** 1: Start CMM 0: Stop CMM This register bit is Read-Only when the MPC.SRL bit is set. **Power Well:** Core

11.3.57 PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h

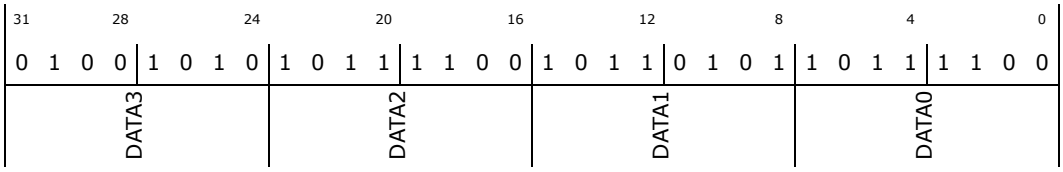
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 334h

Default: 4ABCB5BCh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x4a RW	**CMM Data [3] (DATA3):** This character contains CMM Data [lb]3[rb] that will be transmitted on the link. **Power Well:** Core
23:16	0xbc RW	**CMM Data [2] (DATA2):** This character contains CMM Data [lb]2[rb] that will be transmitted on the link. **Power Well:** Core
15:8	0xb5 RW	**CMM Data [1] (DATA1):** This character contains CMM Data [lb]1[rb] that will be transmitted on the link. **Power Well:** Core
7:0	0xbc RW	**CMM Data [0] (DATA0):** This character contains CMM Data [lb]0[rb] that will be transmitted on the link. **Power Well:** Core

11.3.58 Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h

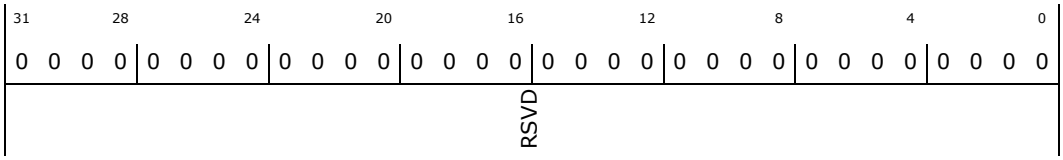
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:2] + 414h

Default: 00000000h

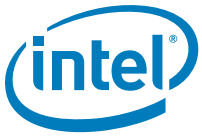


Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

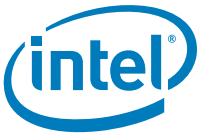
11.4 PCI Express* Lane 3 PCI Configuration Registers

Table 119. Summary of PCI Express* Lane 3 PCI Configuration Registers—0/28/3

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"Identifiers (ID)—Offset 0h" on page 6103	00008086h
4–7h	4	"Device Command; Primary Status (CMD_PSTS)—Offset 4h" on page 6103	00100000h
8–Bh	4	"Revision ID;Class Code (RID_CC)—Offset 8h" on page 6106	06040000h
C–Fh	4	"Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch" on page 6107	00810000h
18–1Bh	4	"Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h" on page 6108	00000000h
1C–1Fh	4	"I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch" on page 6108	00000000h
20–23h	4	"Memory Base and Limit (MBL)—Offset 20h" on page 6110	00000000h
24–27h	4	"Prefetchable Memory Base and Limit (PMBL)—Offset 24h" on page 6111	00010001h
28–2Bh	4	"Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h" on page 6112	00000000h
2C–2Fh	4	"Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch" on page 6112	00000000h
34–37h	4	"Capabilities List Pointer (CAPP)—Offset 34h" on page 6113	00000040h
3C–3Fh	4	"Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch" on page 6113	00000000h
40–43h	4	"Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h" on page 6115	00428010h
44–47h	4	"Device Capabilities (DCAP)—Offset 44h" on page 6116	00008000h
48–4Bh	4	"Device Control; Device Status (DCTL_DSTS)—Offset 48h" on page 6118	00100000h
4C–4Fh	4	"Link Capabilities (LCAP)—Offset 4Ch" on page 6121	00310C02h
50–53h	4	"Link Control; Link Status (LCTL_LSTS)—Offset 50h" on page 6123	00010000h
54–57h	4	"Slot Capabilities (SLCAP)—Offset 54h" on page 6126	00040060h
58–5Bh	4	"Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h" on page 6128	00000000h
5C–5Fh	4	"Root Control (RCTL)—Offset 5Ch" on page 6131	00000000h
60–63h	4	"Root Status (RSTS)—Offset 60h" on page 6132	00000000h
64–67h	4	"Device Capabilities 2 (DCAP2)—Offset 64h" on page 6132	00080817h
68–6Bh	4	"Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h" on page 6134	00000000h
6C–6Fh	4	"Link Capabilities 2 (LCAP2)—Offset 6Ch" on page 6136	00000000h
70–73h	4	"Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h" on page 6137	00000000h
74–77h	4	"Slot Capabilities 2 (SLCAP2)—Offset 74h" on page 6139	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
78–7Bh	4	"Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h" on page 6140	00000000h
80–83h	4	"Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h" on page 6140	00009005h
84–87h	4	"Message Signaled Interrupt Message Address (MA)—Offset 84h" on page 6141	00000000h
88–8Bh	4	"Message Signaled Interrupt Message Data (MD)—Offset 88h" on page 6142	00000000h
90–93h	4	"Subsystem Vendor Capability (SVCAP)—Offset 90h" on page 6142	0000A00Dh
94–97h	4	"Subsystem Vendor IDs (SVID)—Offset 94h" on page 6143	00000000h
A0–A3h	4	"Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h" on page 6144	C8030001h
A4–A7h	4	"PCI Power Management Control And Status (PMCS)—Offset A4h" on page 6145	00000008h
F8–FBh	4	"Manufacturer's ID (MANID)—Offset F8h" on page 6147	00000F00h
100–103h	4	"Advanced Error Reporting Capability Header (AECH)—Offset 100h" on page 6148	00000000h
104–107h	4	"Uncorrectable Error Status (UES)—Offset 104h" on page 6148	00000000h
108–10Bh	4	"Uncorrectable Error Mask (UEM)—Offset 108h" on page 6150	00000000h
10C–10Fh	4	"Uncorrectable Error Severity (UEV)—Offset 10Ch" on page 6152	00060011h
110–113h	4	"Correctable Error Status (CES)—Offset 110h" on page 6153	00000000h
114–117h	4	"Correctable Error Mask (CEM)—Offset 114h" on page 6154	00002000h
118–11Bh	4	"Advanced Error Capabilities and Control (AECC)—Offset 118h" on page 6155	00000000h
11C–11Fh	4	"Header Log DW1 (HL_DW1)—Offset 11Ch" on page 6156	00000000h
120–123h	4	"Header Log DW2 (HL_DW2)—Offset 120h" on page 6157	00000000h
124–127h	4	"Header Log DW3 (HL_DW3)—Offset 124h" on page 6157	00000000h
128–12Bh	4	"Header Log DW4 (HL_DW4)—Offset 128h" on page 6158	00000000h
12C–12Fh	4	"Root Error Command (REC)—Offset 12Ch" on page 6158	00000000h
130–133h	4	"Root Error Status (RES)—Offset 130h" on page 6159	00000000h
134–137h	4	"Error Source Identification (ESID)—Offset 134h" on page 6160	00000000h
200–203h	4	"L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h" on page 6161	00010000h
204–207h	4	"L1 Sub-States Capabilities (L1SCAP)—Offset 204h" on page 6162	0028281Fh
208–20Bh	4	"L1 Sub-States Control 1 (L1SCTL1)—Offset 208h" on page 6164	00000010h
20C–20Fh	4	"L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch" on page 6166	00000028h
328–32Bh	4	"PCI Express Status 1 (PCIESTS1)—Offset 328h" on page 6167	00000000h
32C–32Fh	4	"PCI Express Status 2 (PCIESTS2)—Offset 32Ch" on page 6170	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
330–333h	4	"PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h" on page 6172	28000016h
334–337h	4	"PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h" on page 6174	4ABCB5BCh
414–417h	4	"Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h" on page 6175	00000000h

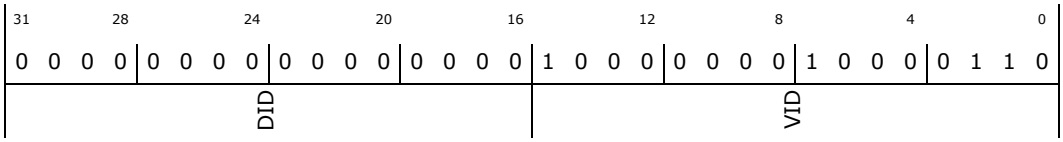
11.4.1 Identifiers (ID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 0h

Default: 00008086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO/V	**Device Identification (DID):** The value of this ID is product specific. **Power Well:** Core
15:0	0x8086 RO	**Vendor Identification (VID):** Indicates Intel **Power Well:** Core

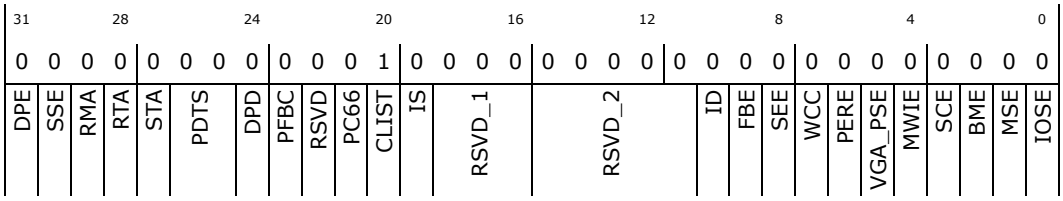
11.4.2 Device Command; Primary Status (CMD_PSTS)—Offset 4h

Access Method

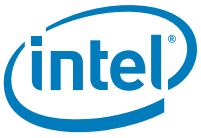
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C/V	**DPE - Detected Parity Error (DPE):** Set when the root port receives a command or data from the backbone with a parity error. This is set even if CMD.PERE is not set. **Power Well:** Core
30	0x0 RW/1C/V	**Signaled System Error (SSE):** Set when the root port signals a system error to the internal SERR# logic. **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
29	0x0 RW/1C/V	**Received Master Abort (RMA):** Set when the root port receives a completion with unsupported request status from the backbone. **Power Well:** Core
28	0x0 RW/1C/V	**Received Target Abort (RTA):** Set when the root port receives a completion with completer abort from the backbone. **Power Well:** Core
27	0x0 RW/1C/V	**Signaled Target Abort (STA):** Set whenever the root port forwards a target abort received from the downstream device onto the backbone. **Power Well:** Core
26:25	0x0 RO	**Primary DEVSEL# Timing Status (PDTS):** Reserved per PCI-Express spec **Power Well:** Core
24	0x0 RW/1C/V	**Master Data Parity Error Detected (DPD):** Set when the root port receives a completion with a data parity error on the backbone and CMD.PERE is set. **Power Well:** Core
23	0x0 RO	**Primary Fast Back to Back Capable (PFBC):** Reserved per PCI-Express spec. **Power Well:** Core
22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**Primary 66 MHz Capable (PC66):** Reserved per PCI-Express spec. **Power Well:** Core
20	0x1 RO	**Capabilities List (CLIST):** Indicates the presence of a capabilities list. **Power Well:** Core
19	0x0 RO/V	**Interrupt Status (IS):** Indicates status of hot plug and power management interrupts on the root port that result in INTx# message generation. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of CMD.ID. **Power Well:** Core
18:16	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:11	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
10	0x0 RW/V2	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above. **Power Well:** Core
9	0x0 RO	**Fast Back to Back Enable (FBE):** Reserved per PCI-Express spec. **Power Well:** Core
8	0x0 RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set. **Power Well:** Core
7	0x0 RO	**Wait Cycle Control (WCC):** Reserved per PCI-Express spec. **Power Well:** Core
6	0x0 RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a master on the backbone. **Power Well:** Core
4	0x0 RO	**Memory Write and Invalidate Enable (MWIE):** Reserved per PCI-Express spec. **Power Well:** Core
3	0x0 RO	**Special Cycle Enable (SCE):** Reserved per PCI-Express and PCI bridge spec. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**Bus Master Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit. **Power Well:** Core
1	0x0 RW	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone. **Power Well:** Core
0	0x0 RW	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone. **Power Well:** Core

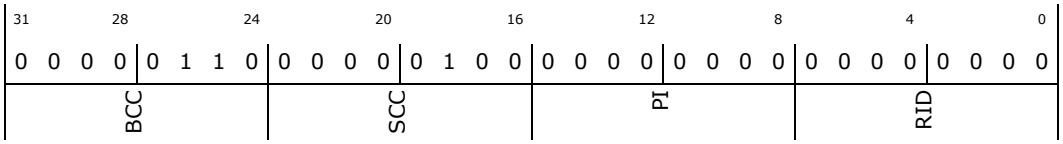
11.4.3 Revision ID;Class Code (RID_CC)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 8h

Default: 06040000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x6 RO	**Base Class Code (BCC):** Indicates the device is a bridge device. **Power Well:** Core
23:16	0x4 RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO/V	**Programming Interface (PI):** The value reported in this register is a function of the Decode Control.Subtractive Decode Enable (SDE) register. SDE Value reported in this register 0: 00h 1: 01h **Power Well:** Core
7:0	0x0 RO/V	**Revision ID (RID):** Indicates the revision of the bridge. **Power Well:** Core

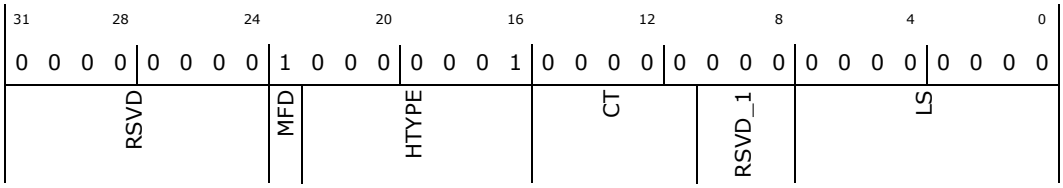
11.4.4 Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + Ch

Default: 00810000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
23	0x1 RO	**Multi-function Device (MFD):** This bit is '1' to indicate a multi-function device. **Power Well:** Core
22:16	0x1 RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' for a Host Bridge, this register reads 00h. **Power Well:** Core
15:11	0x0 RO	**Latency Count (CT):** Reserved per PCI-Express spec **Power Well:** Core
10:8	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**Line Size (LS):** This is read/write but contains no functionality, per PCI-Express spec **Power Well:** Core

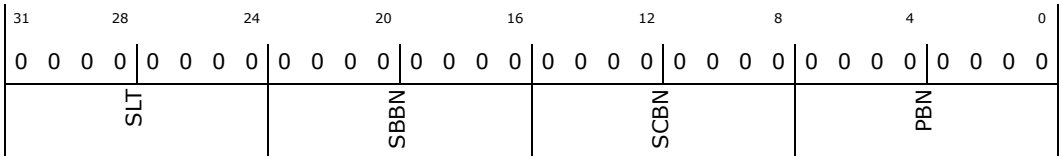
11.4.5 Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 18h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW/V2	**Secodary Latency Timer (SLT):** For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is a RW register; else this register is RO and returns 0. This register does not affect the behavior of any HW logic. **Power Well:** Core
23:16	0x0 RW	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge. **Power Well:** Core
15:8	0x0 RW	**Secondary Bus Number (SCBN):** Indicates the bus number the port. **Power Well:** Core
7:0	0x0 RW	**Primary Bus Number (PBN):** Indicates the bus number of the backbone. **Power Well:** Core

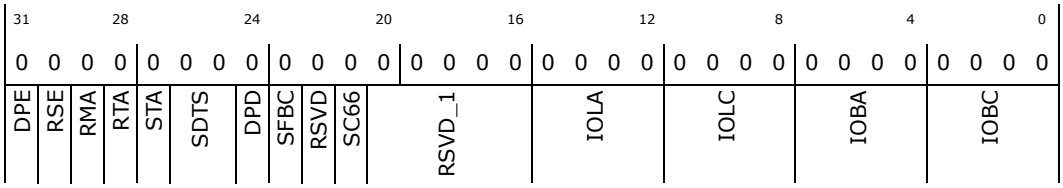
11.4.6 I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 1Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C/V	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP. **Power Well:** Core
30	0x0 RW/1C/V	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device. **Power Well:** Core
29	0x0 RW/1C/V	**Received Master Abort (RMA):** Set when the port receives a completion with [quote]Unsupported Request[/quote] status from the device. **Power Well:** Core
28	0x0 RW/1C/V	**Received Target Abort (RTA):** Set when the port receives a completion with [quote]Completion Abort[/quote] status from the device. **Power Well:** Core
27	0x0 RW/1C/V	**Signaled Target Abort (STA):** Set when the port generates a completion with [quote]Completion Abort[/quote] status to the device. **Power Well:** Core
26:25	0x0 RO/V	**Secondary DEVSEL# Timing Status (SDTS):** Reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b. **Power Well:** Core
24	0x0 RW/1C/V	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side. **Power Well:** Core
23	0x0 RO/V	**Secondary Fast Back to Back Capable (SFBC):** Reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**Secondary 66 MHz Capable (SC66):** Reserved per PCI Express spec **Power Well:** Core
20:16	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
15:12	0x0 RW	**I/O Address Limit (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh. **Power Well:** Core
11:8	0x0 RO	**I/O Limit Address Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing. **Power Well:** Core
7:4	0x0 RW	**I/O Base Address (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h. **Power Well:** Core
3:0	0x0 RO	**I/O Base Address Capability (IOBC):** Indicates that the bridge does not support 32-bit I/O addressing. **Power Well:** Core

11.4.7 Memory Base and Limit (MBL)—Offset 20h

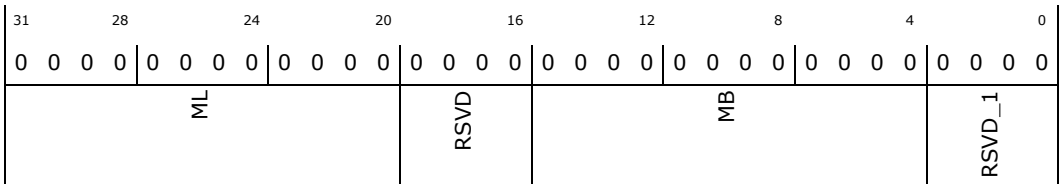
Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is MB [gt]= AD[lb]31:20[rb] [lt]= ML.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 20h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range. **Power Well:** Core
19:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:4	0x0 RW	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range. **Power Well:** Core
3:0	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

11.4.8 Prefetchable Memory Base and Limit (PMBL)—Offset 24h

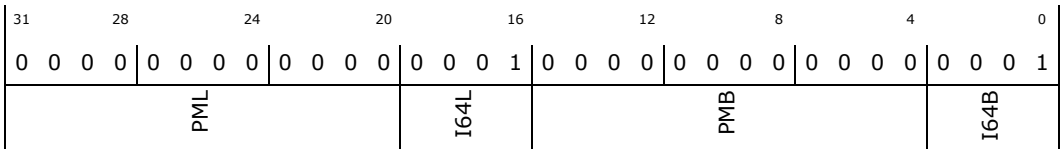
Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is PMBU32:PMB [gt]= AD[lb]63:32[rb]:AD[lb]31:20[rb] [lt]= PMLU32:PML.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 24h

Default: 00010001h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range. **Power Well:** Core
19:16	0x1 RO	**64-bit Indicator (I64L):** Indicates support for 64-bit addressing. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:4	0x0 RW	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range. **Power Well:** Core
3:0	0x1 RO	**64-bit Indicator (I64B):** Indicates support for 64-bit addressing. **Power Well:** Core

11.4.9 Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h

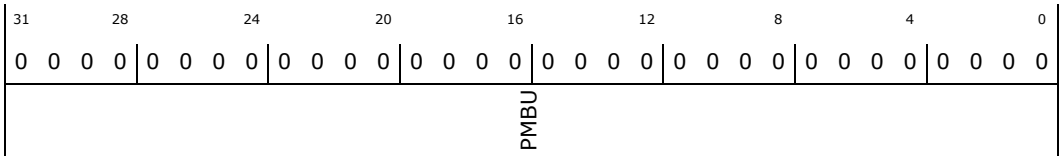
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 28h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base. **Power Well:** Core

11.4.10 Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch

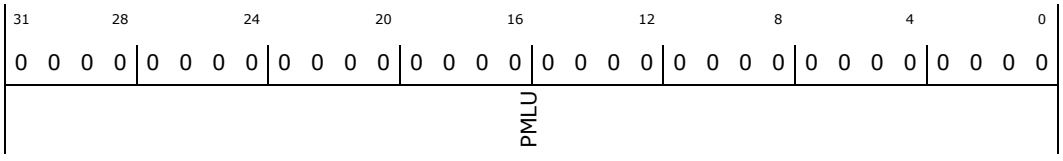
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit. **Power Well:** Core

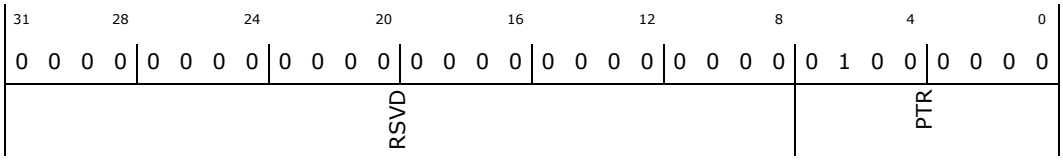
11.4.11 Capabilities List Pointer (CAPP)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 34h

Default: 00000040h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
7:0	0x40 RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. Capability Linked List (Default Settings) Offset Capability Next Pointer 40h PCI Express 80h 80h Message Signaled Interrupt (MSI) 90h 90h Subsystem Vendor A0h A0h PCI Power Management 00h Extended PCIe Capability Linked List Offset Capability Next Pointer 100h Advanced Error Reporting 000h **Power Well:** Core

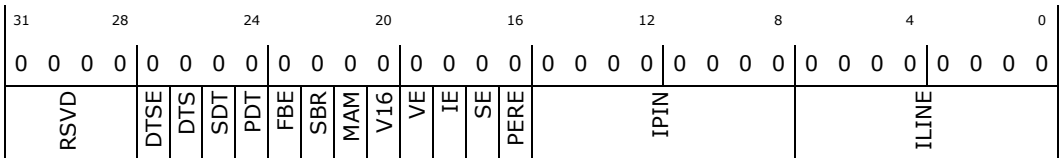
11.4.12 Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch

Access Method

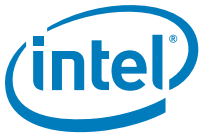
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 3Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
27	0x0 RW/V2	**Discard Timer SERR# Enable (DTSE):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port. **Power Well:** Core
26	0x0 RO	**Discard Timer Status (DTS):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, this register can remain RO as no secondary discard timer exists that will ever cause it to be set. **Power Well:** Core
25	0x0 RW/V2	**Secondary Discard Timer (SDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port. **Power Well:** Core
24	0x0 RW/V2	**Primary Discard Timer (PDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port. **Power Well:** Core
23	0x0 RO	**Fast Back to Back Enable (FBE):** Reserved per Express spec. **Power Well:** Core
22	0x0 RW	**Secondary Bus Reset (SBR):** Triggers a Hot Reset on the PCI-Express port. **Power Well:** Core
21	0x0 RW/V2	**Master Abort Mode (MAM):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port. **Power Well:** Core



Bit Range	Default & Access	Field Name (ID): Description
18	0x0 RW	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh). **Power Well:** Core
17	0x0 RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not. **Power Well:** Core
16	0x0 RW	**Parity Error Response Enable (PERE):** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD. **Power Well:** Core
15:8	0x0 RO/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the STRPFUSECFG register in chipset config space: Port Bits[lb]15:12[rb] Bits[lb]11:08[rb] 1 0h STRPFUSECFG.P1IP 2 0h STRPFUSECFG.P2IP 3 0h STRPFUSECFG.P3IP 4 0h STRPFUSECFG.P4IP 5 0h STRPFUSECFG.P5IP 6 0h STRPFUSECFG.P6IP 7 0h STRPFUSECFG.P7IP 8 0h STRPFUSECFG.P8IP The value that is programmed into STRPFUSECFG is always reflected in this register. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register returns a value of 00h when read, else this register returns the value from the table above. **Power Well:** Core
7:0	0x0 RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. **Power Well:** Core

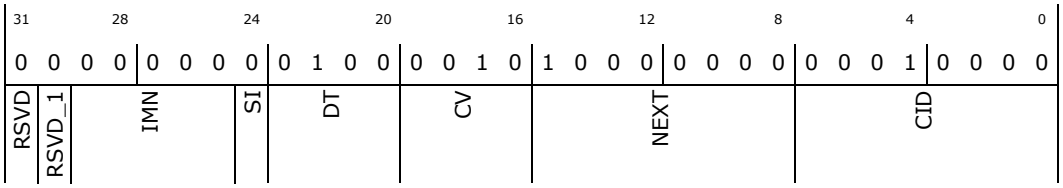
11.4.13 Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 40h

Default: 00428010h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
30	0x0 RO	**Reserved (RSVD_1):** Reserved. This register at one time was for TCS Routing but that was later removed from the PCIe 2.0 spec **Power Well:** Core
29:25	0x0 RO	**Interrupt Message Number (IMN):** The PCIE SIP does not have multiple MSI interrupt numbers. **Power Well:** Core
24	0x0 RW/O	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset. **Power Well:** Core
23:20	0x4 RO	**Device / Port Type (DT):** Indicates this is a PCI-Express root port **Power Well:** Core
19:16	0x2 RO	**Capability Version (CV):** Version 2.0 indicates devices compliant to the PCI Express 2.0 specification which incorporates the Register Expansion ECN. **Power Well:** Core
15:8	0x80 RW/O	**Next Capability (NEXT):** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. **Power Well:** Core
7:0	0x10 RO	**Capability ID (CID):** Indicates this is a PCI Express capability **Power Well:** Core

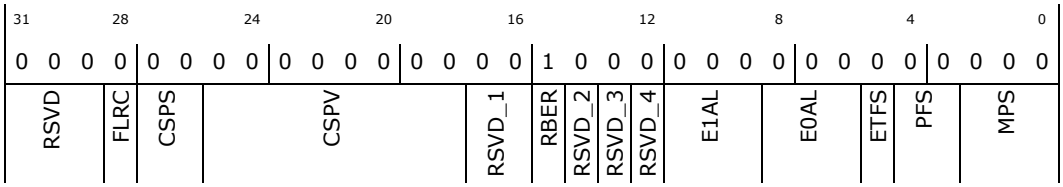
11.4.14 Device Capabilities (DCAP)—Offset 44h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 44h

Default: 00008000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
28	0x0 RO	**Function Level Reset Capable (FLRC):** Not supported in Root Ports **Power Well:** Core
27:26	0x0 RO	**Captured Slot Power Limit Scale (CSPS):** Not supported **Power Well:** Core
25:18	0x0 RO	**Captured Slot Power Limit Value (CSPV):** Not supported **Power Well:** Core
17:16	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
15	0x1 RO	**Role Based Error Reporting (RBER):** When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions. **Power Well:** Core
14	0x0 RO	**Reserved (RSVD_2):** Reserved. On previous version of the specification this was Power Indicator Present (PIP) **Power Well:** Core
13	0x0 RO	**Reserved (RSVD_3):** Reserved. On previous version of the specification this was Attention Indicator Present (AIP) **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12	0x0 RO	**Reserved (RSVD_4):** Reserved. On previous version of the specification this was Attention Button Present (ABP) **Power Well:** Core
11:9	0x0 RO	**Endpoint L1 Acceptable Latency (E1AL):** Reserved for root ports. **Power Well:** Core
8:6	0x0 RO	**Endpoint L0 Acceptable Latency (E0AL):** Reserved for Root port. **Power Well:** Core
5	0x0 RO	**Extended Tag Field Supported (ETFS):** The PCIE SIP never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags. **Power Well:** Core
4:3	0x0 RO	**Phantom Functions Supported (PFS):** No phantom functions supported **Power Well:** Core
2:0	0x0 RW/O	**Max Payload Size Supported (MPS):** BIOS should write to this field during system initialization. Only Max Payload Size of 128B is supported. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. **Power Well:** Core

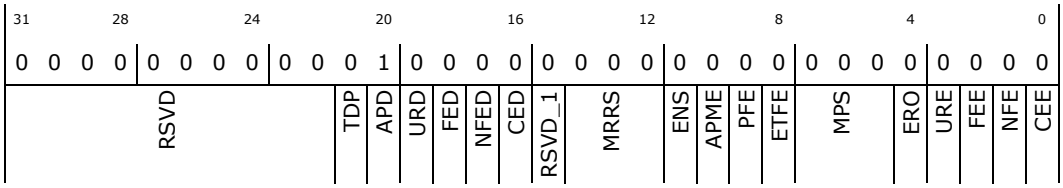
11.4.15 Device Control; Device Status (DCTL_DSTS)—Offset 48h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 48h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID. **Power Well:** Core
20	0x1 RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup **Power Well:** Core
19	0x0 RW/1C/V	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected. **Power Well:** Core
18	0x0 RW/1C/V	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed tlp **Power Well:** Core
17	0x0 RW/1C/V	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned tlp, unexpected completions, unsupported requests, completor abort, or completer timeout **Power Well:** Core
16	0x0 RW/1C/V	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, tlp crc error, dllp crc error, replay num rollover, replay timeout. **Power Well:** Core
15	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
14:12	0x0 RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11	0x0 RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests. **Power Well:** Core
10	0x0 RW/P	**Aux Power PM Enable (APME):** The OS will set this bit to '1' if the device connected has detected aux power. **Power Well:** Core
9	0x0 RO	**Phantom Functions Enable (PFE):** Not supported **Power Well:** Core
8	0x0 RO	**Extended Tag Field Enable (ETFE):** Not supported **Power Well:** Core
7:5	0x0 RW	**Max Payload Size (MPS):** The root port only supports 128B max payload. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. If the DCAP.MPS indicates 128B max payload size support, programming this field to any values other than 128B will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME. **Power Well:** Core
4	0x0 RO	**Enable Relaxed Ordering (ERO):** Not supported **Power Well:** Core
3	0x0 RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RW	**Fatal Error Reporting Enable (FEE):** enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting. **Power Well:** Core
1	0x0 RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting. **Power Well:** Core
0	0x0 RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting. **Power Well:** Core

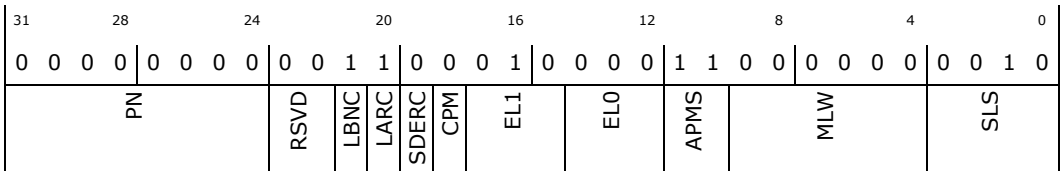
11.4.16 Link Capabilities (LCAP)—Offset 4Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 4Ch

Default: 00310C02h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port # Value of PN field 1 01h 2 02h 3 03h 4 04h **Power Well:** Core
23:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
21	0x1 RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms. **Power Well:** Core
20	0x1 RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. **Power Well:** Core
19	0x0 RO	**Surprise Down Error Reporting Capable (SDERC):** Set to '0' to indicate the root port does not support Surprise Down Error Reporting **Power Well:** Core
18	0x0 RO	**Clock Power Management (CPM):** '0' Indicates that root ports do not support the CLKREQ# mechanism. **Power Well:** Core
17:15	0x2 RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b Less than 1 us 001b 1 us to less than 2 us 010b 2 us to less than 4 us 011b 4 us to less than 8 us 100b 8 us to less than 16 us 101b 16 us to less than 32 us 110b 32 us to 64 us 111b More than 64 us Note: If PXP PLL shutdown is enabled, BIOS should program this latency to comprehend PLL lock latency. **Power Well:** Core
14:12	0x0 RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration: LCTL.CCC Value 0 MPC.UCEL 1 MPC.CCEL **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11:10	0x3 RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00 (Reserved) 01 L0s Entry supported 10 Reserved 11 Both L0s and L1 supported Note: If STRPFUSECFG.ASPMDIS is 1, the default of this field is [quote]01[/quote]. Otherwise, the default of this field is [quote]11[/quote]. If STRPFUSECFG.ASPMDIS is 1, BIOS writing [quote]11[/quote] to this field will have the same effect as [quote]01[/quote]. [quote]01[/quote] will be reflected on this register when read and the register will turn to Read-Only once written once. **Power Well:** Core
9:4	0x0 RO/V	**Maximum Link Width (MLW):** For the root ports, several values can be taken, based upon the value of the chipset configuration register field RPC.PC1 for ports 1-4: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h **Power Well:** Core
3:0	0x2 RO/V	**Supported Link Speeds (SLS):** Indicates the supported link speeds of the Root Port. 0001b 2.5 GT/s Link speed supported 0010b 5.0 GT/s and 2.5GT/s Link speeds supported This register reports a value of 0001b if the Root Port Gen2 Disable Fuse is set or the MPC.PCIEGEN2DIS bit is set, else this register reports a value of 0010b. **Power Well:** Core

11.4.17 Link Control; Link Status (LCTL_LSTS)—Offset 50h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 50h

Default: 00010000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LABS	LBMS	LA	SCC	LT	RSVD	NLW						CLS				RSVD_1				LABIE	LBMIE	HAWD	ECPM	ES	CCC	RL	LD	RCBC	RSVD_2	ASPM	

Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW/1C/V	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b. **Power Well:** Core
30	0x0 RW/1C/V	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b. **Power Well:** Core
29	0x0 RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise. **Power Well:** Core
28	0x0 RO/V	**Slot Clock Configuration (SCC):** In normal mode, PCIE SIP uses the same reference clock as on the platform and does not generate its own clock. Note: The default of this register bit is dependent on the [quote]PCIe Non-Common Clock With SSC Mode Enable Strap[/quote]. If the strap enables non-common clock with SSC support, this bit shall default to '0'. Otherwise, this bit shall default to '1'. **Power Well:** Core
27	0x0 RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training. **Power Well:** Core
26	0x0 RO	**Reserved (RSVD):** Reserved. Previously this was defined as Link Training Error (LTE) but support for this bit was removed from subsequent versions of the PCI Express specification. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
25:20	0x0 RO/V	**Negotiated Link Width (NLW):** For the root ports, this register could take on several values: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h The value of this register is undefined if the link has not successfully trained. **Power Well:** Core
19:16	0x1 RO/V	**Current Link Speed (CLS):** 0001b Link is 2.5Gb/s Link 0010b 5.0 GT/s Link The value of this field is undefined if the link is not up. **Power Well:** Core
15:12	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
11	0x0 RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set. **Power Well:** Core
10	0x0 RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/ PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b. **Power Well:** Core
9	0x0 RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Default value of this bit is 0b. **Power Well:** Core
8	0x0 RO	**Enable Clock Power Management (ECPM):** Reserved. Not supported on PCIE SIP Root Ports. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW	**Extended Synch (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0. **Power Well:** Core
6	0x0 RW	**Common Clock Configuration (CCC):** When set, indicates that the PCIE SIP and device are operating with a distributed common reference clock. **Power Well:** Core
5	0x0 WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns '0' when read. Software uses LSTS.LT to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress. **Power Well:** Core
4	0x0 RW	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state. **Power Well:** Core
3	0x0 RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes. **Power Well:** Core
2	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
1:0	0x0 RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used. Note: If STRPFUSECFG.ASPMDIS is '1', hardware will always see [quote]00[/quote] as an output from this register. BIOS reading this register should always return the correct value. **Power Well:** Core

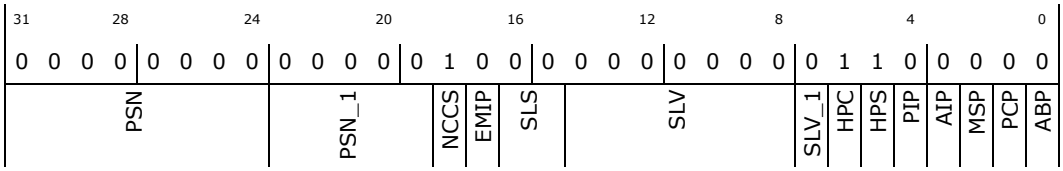
11.4.18 Slot Capabilities (SLCAP)—Offset 54h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 54h

Default: 00040060h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RW/O	**Physical Slot Number (PSN):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
23:19	0x0 RW/O	**Physical Slot Number (PSN_1):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
18	0x1 RO	**No Command Completed Support (NCCS):** Set to '1' as this port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes. **Power Well:** Core
17	0x0 RO	**Electromechanical Interlock Present (EMIP):** Set to 0 to indicate that no electro-mechanical interlock is implemented. **Power Well:** Core
16:15	0x0 RW/O	**Slot Power Limit Scale (SLS):** specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
14:8	0x0 RW/O	**Slot Power Limit Value (SLV):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
7	0x0 RW/O	**Slot Power Limit Value (SLV_1):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset. **Power Well:** Core
6	0x1 RW/O	**Hot Plug Capable (HPC):** When set, Indicates that hot plug is supported. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5	0x1 RW/O	**Hot Plug Surprise (HPS):** When set, indicates the device may be removed from the slot without prior notification. **Power Well:** Core
4	0x0 RO	**Power Indicator Present (PIP):** Indicates that a power indicator LED is not present for this slot. **Power Well:** Core
3	0x0 RO	**Attention Indicator Present (AIP):** Indicates that an attention indicator LED is not present for this slot. **Power Well:** Core
2	0x0 RO	**MRL Sensor Present (MSP):** Indicates that an MRL sensor is not present **Power Well:** Core
1	0x0 RO	**Power Controller Present (PCP):** Indicates that a power controller is not implemented for this slot **Power Well:** Core
0	0x0 RO	**Attention Button Present (ABP):** Indicates that an attention button is not implemented for this slot. **Power Well:** Core

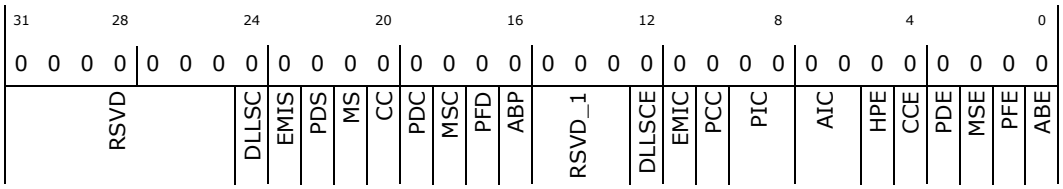
11.4.19 Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 58h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
24	0x0 RW/1C/V	**Data Link Layer State Changed (DLLSC):** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device. **Power Well:** Core
23	0x0 RO	**Electromechanical Interlock Status (EMIS):** Reserved as this port does not support and electromechanical interlock. **Power Well:** Core
22	0x0 RO/V	**Presence Detect State (PDS):** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected ('1') or empty ('0'). If XCAP.SI is cleared, this bit is a '1'. **Power Well:** Core
21	0x0 RO	**MRL Sensor State (MS):** Reserved as the MRL sensor is not implemented. **Power Well:** Core
20	0x0 RO	**Command Completed (CC):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
19	0x0 RW/1C/V	**Presence Detect Changed (PDC):** This bit is set by the root port when the SLSTS.PDS bit changes state. **Power Well:** Core
18	0x0 RO	**MRL Sensor Changed (MSC):** Reserved as the MRL sensor is not implemented. **Power Well:** Core
17	0x0 RO	**Power Fault Detected (PFD):** Reserved as a power controller is not implemented. **Power Well:** Core
16	0x0 RO	**Attention Button Pressed (ABP):** This register is RO as this port does not implement an attention button **Power Well:** Core
15:13	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12	0x0 RW	**Data Link Layer State Changed Enable (DLLSCE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed **Power Well:** Core
11	0x0 RO	**Electromechanical Interlock Control (EMIC):** Reserved as this port does not support an Electromechanical Interlock. **Power Well:** Core
10	0x0 RO	**Power Controller Control (PCC):** This bit has no meaning for module based hot plug. **Power Well:** Core
9:8	0x0 RO	**Power Indicator Control (PIC):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
7:6	0x0 RO	**Attention Indicator Control (AIC):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
5	0x0 RW	**Hot Plug Interrupt Enable (HPE):** When set, enables generation of a hot plug interrupt on enabled hot plug events. **Power Well:** Core
4	0x0 RO	**Command Completed Interrupt Enable (CCE):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
3	0x0 RW	**Presence Detect Changed Enable (PDE):** When set, enables the generation of a hot plug interrupt or wake message when the presence detect logic changes state. **Power Well:** Core
2	0x0 RO	**MRL Sensor Changed Enable (MSE):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core
1	0x0 RO	**Power Fault Detected Enable (PFE):** This register is RO as this port does not implement a Hot Plug Controller... **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RO	**Attention Button Pressed Enable (ABE):** This register is RO as this port does not implement a Hot Plug Controller.. **Power Well:** Core

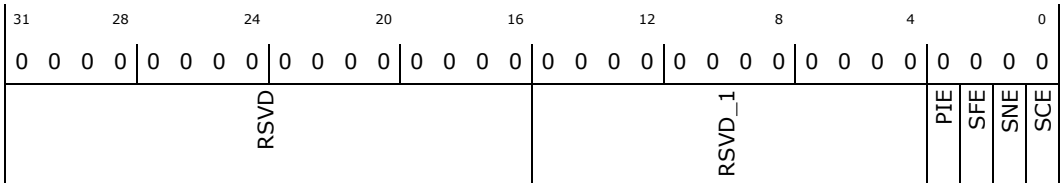
11.4.20 Root Control (RCTL)—Offset 5Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 5Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:4	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
3	0x0 RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a '0' to '1' transition, or due to this bit being set with RSTS.PS already set). **Power Well:** Core
2	0x0 RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set. **Power Well:** Core
1	0x0 RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set. **Power Well:** Core

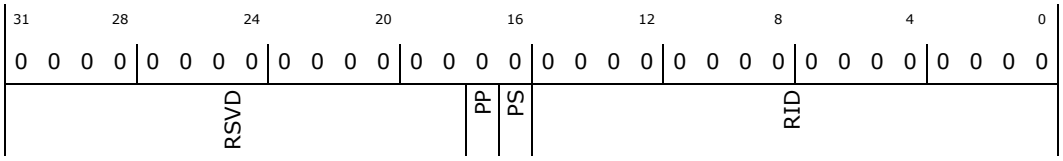
11.4.21 Root Status (RSTS)—Offset 60h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 60h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
17	0x0 RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. PCIE SIP root ports have a one deep PME pending queue. **Power Well:** Core
16	0x0 RW/1C/V	**PME Status (PS):** Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared. **Power Well:** Core
15:0	0x0 RO/V	**PME Requestor ID (RID):** Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set. PCIE SIP root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped. **Power Well:** Core

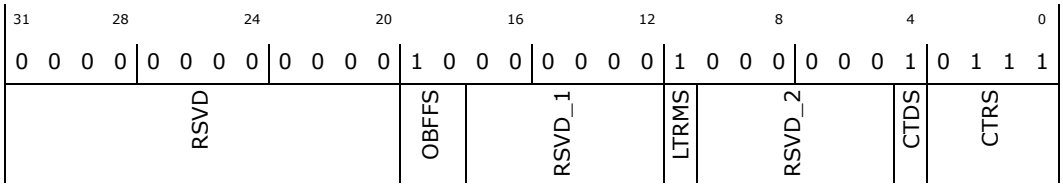
11.4.22 Device Capabilities 2 (DCAP2)—Offset 64h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 64h

Default: 00080817h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
19:18	0x2 RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b - OBFF is not supported. 01b - OBFF is supported using Message signaling only. 10b - OBFF is supported using WAKE# signaling only. 11b - OBFF is supported using WAKE# and Message signaling. BIOS should program this field to 00b or 10b during system initialization to advertise the level of hardware OBFF support to software. BIOS should never program this field to 01b or 11b since OBFF messaging is not supported. **Power Well:** Core
17:12	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
11	0x1 RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a '1' or a '0' to enable/disable the root port from declaring support for the LTR capability. **Power Well:** Core
10:5	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
4	0x1 RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x7 RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A [amp] B 0110b Ranges B [amp] C 0111b Ranges A, B [amp] C [lt]-- This is what IP supports 1110b Ranges B, C [amp] D 1111b Ranges A, B, C [amp] D All other values are reserved. **Power Well:** Core

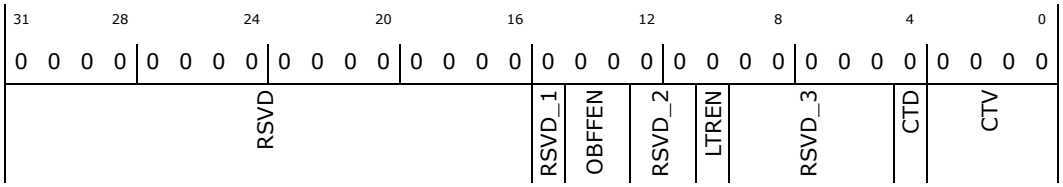
11.4.23 Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 68h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
14:13	0x0 RW	**Optimized Buffer Flush/Fill Enable (OBFFEN):** 00b Disable OBFF mechanism. 01b Enable OBFF mechanism using Message signaling (Variation A). 10b Enable OBFF mechanism using Message signaling (Variation B). 11b Enable OBFF using WAKE# signaling. Note: Only encoding 00b and 11b are supported. The encoding of 01b or 10b would be aliased to 00b. If DCAP2.OBFFS is clear, programming this field to any non-zero values will have no effect. **Power Well:** Core
12:11	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
10	0x0 RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect. **Power Well:** Core
9:5	0x0 RO	**Reserved (RSVD_3):** Reserved **Power Well:** Core
4	0x0 RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x0 RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. ThePCIE SIP targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range A (50us to 10 ms) programmability range is supported: 0001b 90-100us (spec range is 50 us to 100 us) 0010b 9-10ms (spec range is 1ms to 10 ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either when this value was changed or when each request was issued. **Power Well:** Core

11.4.24 Link Capabilities 2 (LCAP2)—Offset 6Ch

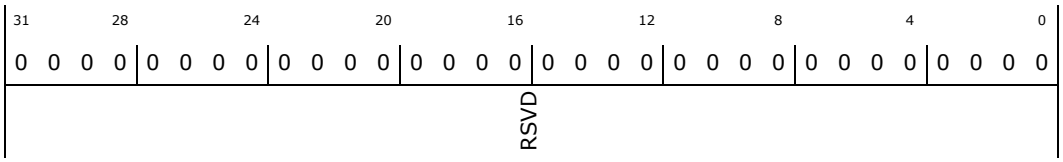
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 6Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

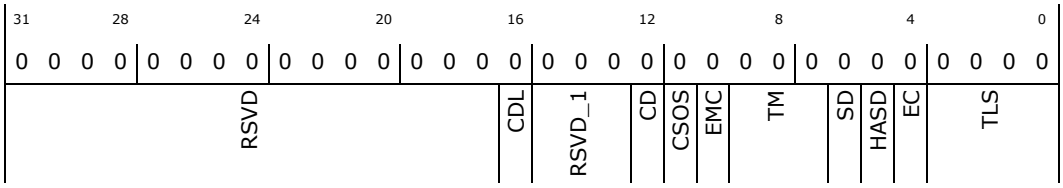
11.4.25 Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 70h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
16	0x0 RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is operating at 2.5 GT/s speed. **Power Well:** Core
15:13	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
12	0x0 RW/P	**Compliance De-emphasis (CD):** This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s, the setting of this bit has no effect. The default value of this bit is 0b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11	0x0 RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b. **Power Well:** Core
10	0x0 RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value. **Power Well:** Core
9:7	0x0 RW/P	**Transmit Margin (TM):** This field controls the value of the nondeemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see PCI Express Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value. **Power Well:** Core
6	0x0 RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RO	**Hardware Autonomous Speed Disable (HASD):** Reserved. This port cannot autonomously change speeds. **Power Well:** Core
4	0x0 RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. **Power Well:** Core
3:0	0x0 RW/V/P	**Target Link Speed (TLS):** This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. For PCIE SIP, the allowed value is: 0001b 2.5 GT/s Target Link Speed 0010b 5.0 GT/s and 2.5GT/s Link speeds supported If a value is written to this field that does not correspond to a speed included in the Supported Link Speeds field, the result is undefined. The default value of this field is the highest Link speed supported by the component (as reported in the Supported Link Speeds field of the Link Capabilities register). **Power Well:** Core

11.4.26 Slot Capabilities 2 (SLCAP2)—Offset 74h

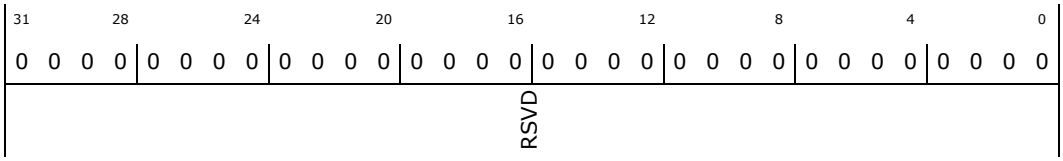
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 74h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

11.4.27 Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h

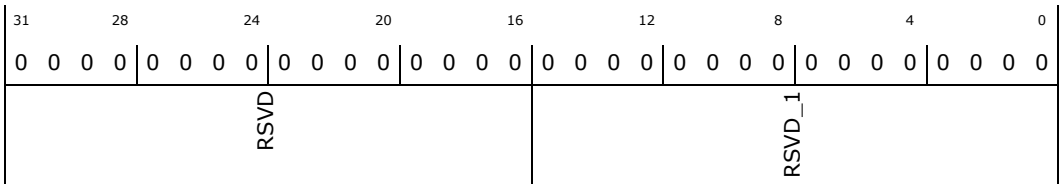
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 78h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:0	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

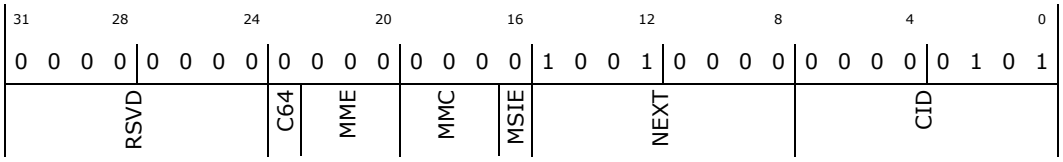
11.4.28 Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 80h

Default: 00009005h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
23	0x0 RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
22:20	0x0 RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port. **Power Well:** Core
19:17	0x0 RO	**Multiple Message Capable (MMC):** Only one message is required. **Power Well:** Core
16	0x0 RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated. **Power Well:** Core
15:8	0x90 RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. **Power Well:** Core
7:0	0x5 RO	**Capability ID (CID):** Capabilities ID indicates MSI. **Power Well:** Core

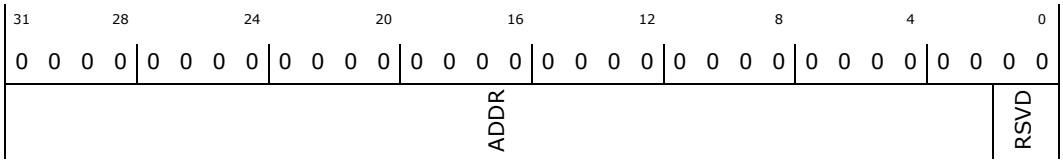
11.4.29 Message Signaled Interrupt Message Address (MA)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 84h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RW	**Address (ADDR):** Lower 32 bits of the system specified message address, always DW aligned. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1:0	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

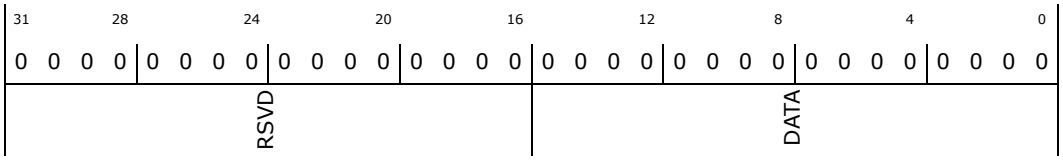
11.4.30 Message Signaled Interrupt Message Data (MD)—Offset 88h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 88h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:0	0x0 RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[lb]15:0[rb]) during the data phase of the MSI memory write transaction. **Power Well:** Core

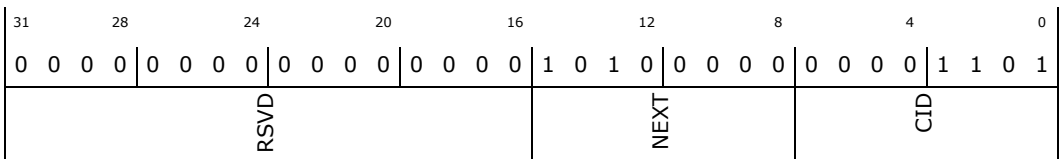
11.4.31 Subsystem Vendor Capability (SVCAP)—Offset 90h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 90h

Default: 0000A00Dh



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15:8	0xa0 RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. **Power Well:** Core
7:0	0xd RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability. **Power Well:** Core

11.4.32 Subsystem Vendor IDs (SVID)—Offset 94h

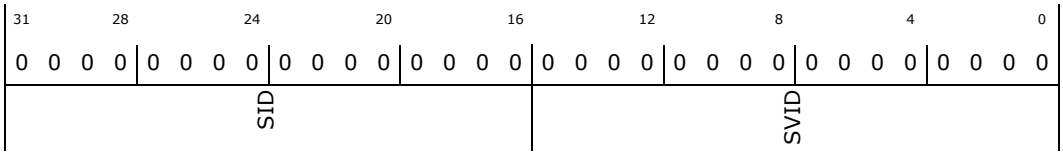
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 94h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset). **Power Well:** Core
15:0	0x0 RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset). **Power Well:** Core

11.4.33 Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h

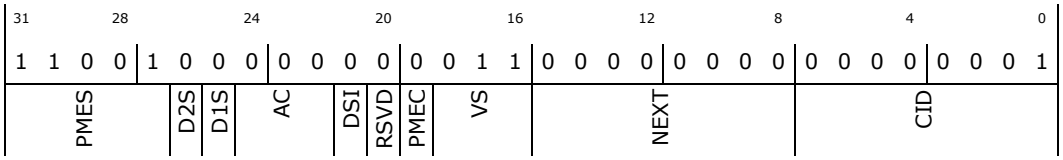
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + A0h

Default: C8030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x19 RO	**PME Support (PMES):** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy Microsoft operating systems to enable PME# in devices connected behind this root port. **Power Well:** Core
26	0x0 RO	**D2_Support (D2S):** The D2 state is not supported. **Power Well:** Core
25	0x0 RO	**D1_Support (D1S):** The D1 state is not supported. **Power Well:** Core
24:22	0x0 RO	**Aux_Current (AC):** Reports 0mA (self-powered), as use of this controller does not add to suspend well power consumption. **Power Well:** Core
21	0x0 RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required. **Power Well:** Core
20	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
19	0x0 RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#. **Power Well:** Core
18:16	0x3 RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:8	0x0 RO	**Next Capability (NEXT):** Indicates this is the last item in the list. **Power Well:** Core
7:0	0x1 RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability. **Power Well:** Core

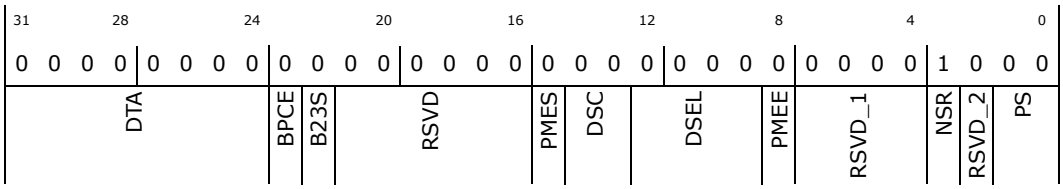
11.4.34 PCI Power Management Control And Status (PMCS)—Offset A4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + A4h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Data (DTA):** Reserved **Power Well:** Core
23	0x0 RO	**Bus Power / Clock Control Enable (BPCE):** Reserved per PCI Express specification **Power Well:** Core
22	0x0 RO	**B2/B3 Support (B23S):** Reserved per PCI Express specification. **Power Well:** Core
21:16	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
15	0x0 RO	**PME Status (PMES):** Indicates a PME was received on the downstream link. **Power Well:** Core
14:13	0x0 RO	**Data Scale (DSC):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
12:9	0x0 RO	**Data Select (DSEL):** Reserved **Power Well:** Core
8	0x0 RW/P	**PME Enable (PMEE):** Indicates PME is enabled. The root port takes no action on this bit, but it must be RW for legacy Microsoft operating systems to enable PME# on devices connected to this root port. This register resides in the resume well and is not reset on a resume from S3/S4/S5. The reset for this register is RSMRST# which is not asserted during a Warm Reset. **Power Well:** Core
7:4	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
3	0x1 RW/O	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. **Power Well:** Core
2	0x0 RO	**Reserved (RSVD_2):** Reserved. **Power Well:** Core
1:0	0x0 RW	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 - D0 state 11 - D3HOT state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a '10' or '01' to these bits, the write will be ignored. **Power Well:** Core

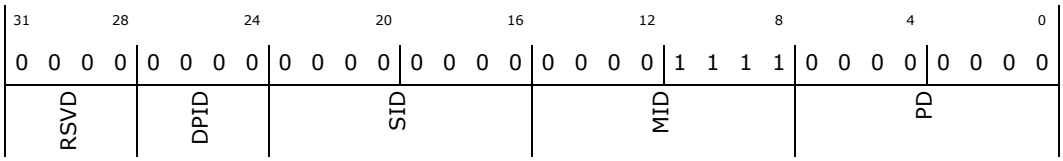
11.4.35 Manufacturer's ID (MANID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + F8h

Default: 00000F00h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
27:24	0x0 RO/V	**Dot portion of Process ID (DPID):** The value of this field is SoC specific. Example: Process/Dot (PD) is 1265.8. Indicates the dot as .8. **Power Well:** Core
23:16	0x0 RO/V	**Stepping Identifier (SID):** This field is incremented for each stepping of the part. Note that this field can be used by software to differentiate steppings when the Revision ID may not change. A single Manufacturing Stepping ID can be implemented that is readable from all functions in the chip because all of them are incremented in lock-step. **Power Well:** Core
15:8	0xf RO	**Manufacturing Identifier (MID):** 0Fh = Intel **Power Well:** Core
7:0	0x0 RO/V	**Process/Dot (PD):** Indicates the current process. The value of this field is SoC specific. Example: Process/Dot (PD) is 1265.8. Indicates the Process (1265). **Power Well:** Core

11.4.36 Advanced Error Reporting Capability Header (AECH)—Offset 100h

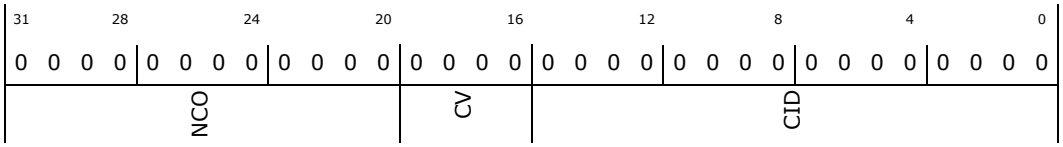
Size:32 bits The AER capability can optionally be included or excluded from the capabilities list. The full AER is supported.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 100h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW/O	**Next Capability Offset (NCO):** Set to 000h as this is the last capability in the list. **Power Well:** Core
19:16	0x0 RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0 **Power Well:** Core
15:0	0x0 RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0 **Power Well:** Core

11.4.37 Uncorrectable Error Status (UES)—Offset 104h

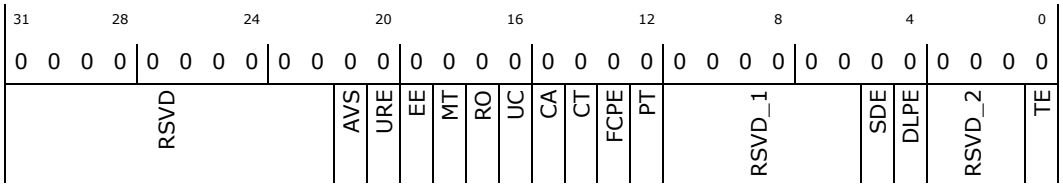
This register must maintain its state through a platform reset. It loses its state upon loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 104h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported **Power Well:** Core
20	0x0 RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received. **Power Well:** Core
19	0x0 RO	**ECRC Error Status (EE):** ECRC is not supported. **Power Well:** Core
18	0x0 RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received. **Power Well:** Core
17	0x0 RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred. **Power Well:** Core
16	0x0 RW/1C/V/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received. **Power Well:** Core
15	0x0 RW/1C/V/P	**Completor Abort Status (CA):** Indicates a completer abort was received **Power Well:** Core
14	0x0 RW/1C/V/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value **Power Well:** Core
13	0x0 RO	**Flow Control Protocol Error Status (FCPE):** Not supported. **Power Well:** Core
12	0x0 RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received. **Power Well:** Core
11:6	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
5	0x0 RO	**Surprise Down Error Status (SDE):** Surprise Down is not supported. **Power Well:** Core
4	0x0 RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred. **Power Well:** Core
3:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x0 RO	**Training Error Status (TE):** Not supported. **Power Well:** Core

11.4.38 Uncorrectable Error Mask (UEM)—Offset 108h

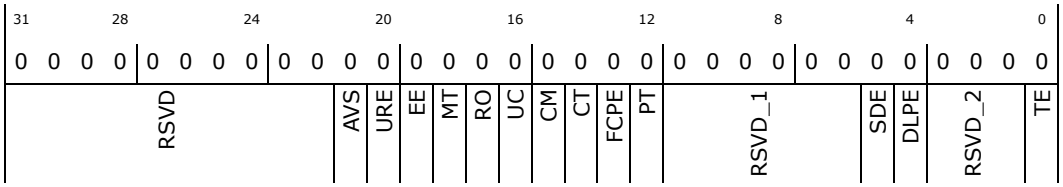
When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 108h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported **Power Well:** Core
20	0x0 RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
19	0x0 RO	**ECRC Error Mask (EE):** ECRC is not supported. **Power Well:** Core
18	0x0 RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs **Power Well:** Core
17	0x0 RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows. **Power Well:** Core
16	0x0 RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions. **Power Well:** Core
15	0x0 RW/P	**Completor Abort Mask (CM):** Mask for completer abort. **Power Well:** Core
14	0x0 RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts. **Power Well:** Core
13	0x0 RO	**Flow Control Protocol Error Mask (FCPE):** Not supported. **Power Well:** Core
12	0x0 RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs. **Power Well:** Core
11:6	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
5	0x0 RO	**Surprise Down Error Mask (SDE):** Surprise Down is not supported. **Power Well:** Core
4	0x0 RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors. **Power Well:** Core
3:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x0 RO	**Training Error Mask (TE):** Not supported. **Power Well:** Core

11.4.39 Uncorrectable Error Severity (UEV)—Offset 10Ch

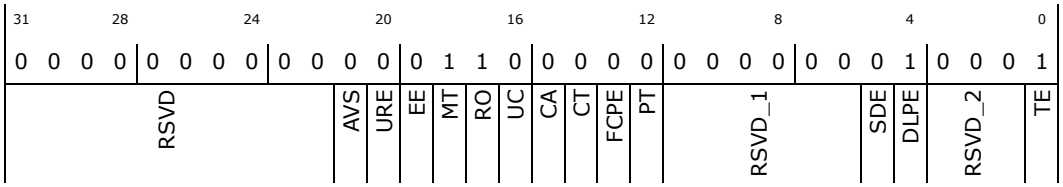
This register gives the option to make an uncorrectable error fatal or non-fatal. An error is fatal if the bit is set. An error is non-fatal if the bit is cleared. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 10Ch

Default: 00060011h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
21	0x0 RO	**ACS Violation Severity (AVS):** Reserved. Access Control Services are not supported **Power Well:** Core
20	0x0 RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception. **Power Well:** Core
19	0x0 RO	**ECRC Error Severity (EE):** ECRC is not supported. **Power Well:** Core
18	0x1 RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception. **Power Well:** Core
17	0x1 RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences. **Power Well:** Core
16	0x0 RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception. **Power Well:** Core
15	0x0 RW/P	**Completor Abort Severity (CA):** Severity for completer abort. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
14	0x0 RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout. **Power Well:** Core
13	0x0 RO	**Flow Control Protocol Error Severity (FCPE):** Not supported. **Power Well:** Core
12	0x0 RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception. **Power Well:** Core
11:6	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
5	0x0 RO	**Surprise Down Error Severity (SDE):** Surprise Down is not supported. **Power Well:** Core
4	0x1 RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors. **Power Well:** Core
3:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x1 RO	**Training Error Severity (TE):** TE not supported. This bit is left as RO='1' for ease of implementation.. **Power Well:** Core

11.4.40 Correctable Error Status (CES)—Offset 110h

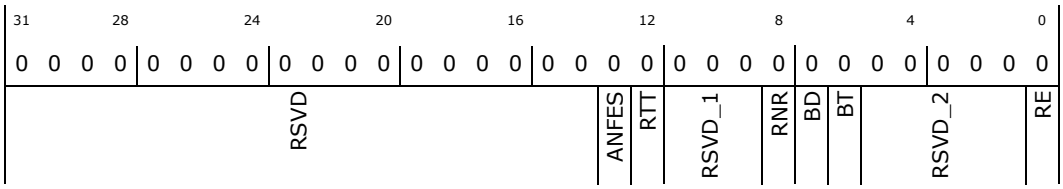
This register is only reset by a loss of core power

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 110h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
13	0x0 RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that a Advisory Non-Fatal Error occured. **Power Well:** Core
12	0x0 RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out. **Power Well:** Core
11:9	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
8	0x0 RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over. **Power Well:** Core
7	0x0 RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received. **Power Well:** Core
6	0x0 RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received. **Power Well:** Core
5:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x0 RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred. **Power Well:** Core

11.4.41 Correctable Error Mask (CEM)—Offset 114h

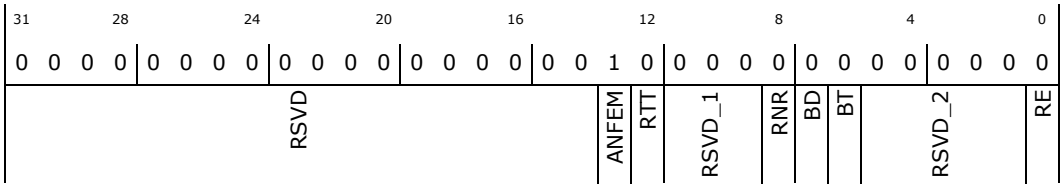
When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 114h

Default: 00002000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
13	0x1 RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting. **Power Well:** Core
12	0x0 RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout. **Power Well:** Core
11:9	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
8	0x0 RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover. **Power Well:** Core
7	0x0 RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception. **Power Well:** Core
6	0x0 RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception. **Power Well:** Core
5:1	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
0	0x0 RW/P	**Receiver Error Mask (RE):** Mask for receiver errors. **Power Well:** Core

11.4.42 Advanced Error Capabilities and Control (AECC)—Offset 118h

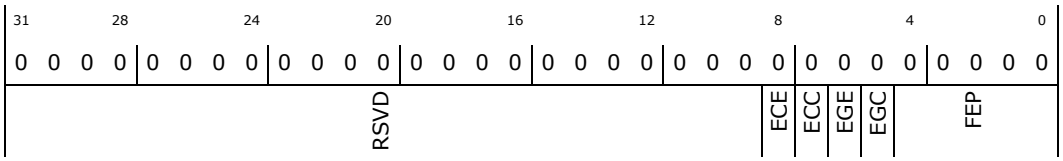
This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 118h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
8	0x0 RO	**ECRC Check Enable (ECE):** ECRC is not supported. **Power Well:** Core
7	0x0 RO	**ECRC Check Capable (ECC):** ECRC is not supported. **Power Well:** Core
6	0x0 RO	**ECRC Generation Enable (EGE):** ECRC is not supported. **Power Well:** Core
5	0x0 RO	**ECRC Generation Capabile (EGC):** ECRC is not supported. **Power Well:** Core
4:0	0x0 RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register. **Power Well:** Core

11.4.43 Header Log DW1 (HL_DW1)—Offset 11Ch

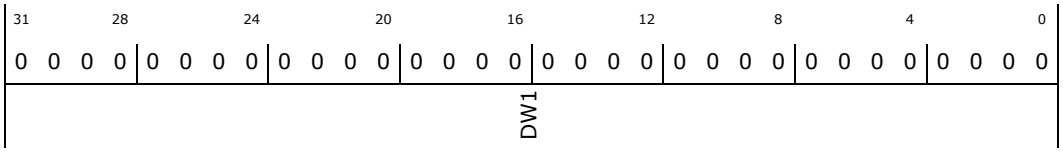
Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 11Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO/V/P	**1st dWord of TLP (DW1):** Byte0 [amp][amp] Byte1 [amp][amp] Byte2 [amp][amp] Byte3 **Power Well:** Core

11.4.44 Header Log DW2 (HL_DW2)—Offset 120h

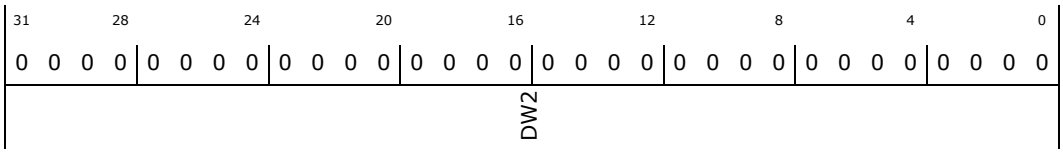
Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 120h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO/V/P	**2nd dWord of TLP (DW2):** Byte4 [amp][amp] Byte5 [amp][amp] Byte6 [amp][amp] Byte7 **Power Well:** Core

11.4.45 Header Log DW3 (HL_DW3)—Offset 124h

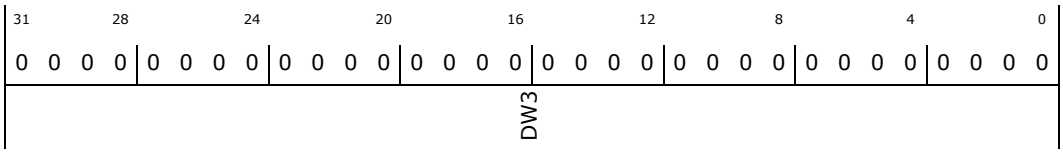
Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 124h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO/V/P	**3rd dWord of TLP (DW3):** Byte8 [amp][amp] Byte9 [amp][amp] Byte10 [amp][amp] Byte11 **Power Well:** Core

11.4.46 Header Log DW4 (HL_DW4)—Offset 128h

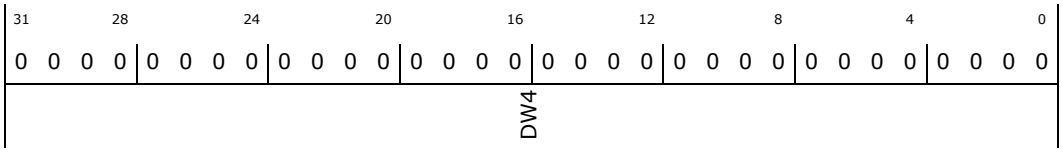
Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 128h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO/V/P	**4th dWord of TLP (DW4):** Byte12 [amp][amp] Byte13 [amp][amp] Byte14 [amp][amp] Byte15 **Power Well:** Core

11.4.47 Root Error Command (REC)—Offset 12Ch

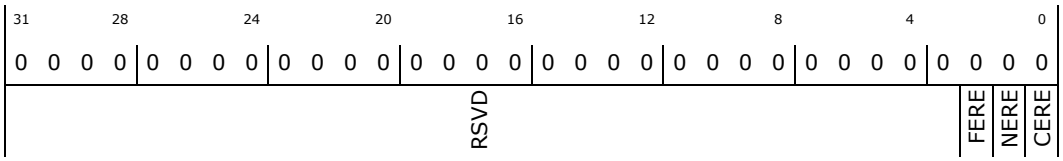
This register allows errors to generate interrupts.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 12Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
2	0x0 RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device. **Power Well:** Core
1	0x0 RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device. **Power Well:** Core
0	0x0 RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device. **Power Well:** Core

11.4.48 Root Error Status (RES)—Offset 130h

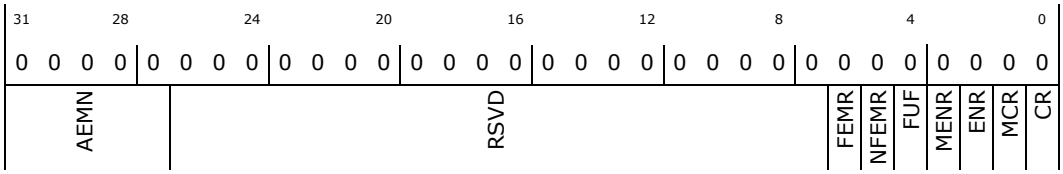
This register can track more than one error and set the [quote]multiple[/quote] bits if a second or subsequent error occurs and the first has not been serviced. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 130h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**Advanced Error Interrupt Message Number (AEMN):** Reserved. There is only one error interrupt allocated. **Power Well:** Core
26:7	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
6	0x0 RW/1C/V/P	**Fatal Error Message Received (FEMR):** Set when one or more Fatal Uncorrectable Error Messages have been received. **Power Well:** Core
5	0x0 RW/1C/V/P	**Non-Fatal Error Messages Received (NFEMR):** Set when one or more Non-Fatal Uncorrectable error messages have been received **Power Well:** Core
4	0x0 RW/1C/V/P	**First Uncorrectable Fatal (FUF):** Set when the first Uncorrectable Error message received is for a fatal error. **Power Well:** Core
3	0x0 RW/1C/V/P	**Multiple ERR_FATAL/NONFATAL Received (MENR):** Set when either a fatal or a non-fatal error is received and the ENR bit is already set. **Power Well:** Core
2	0x0 RW/1C/V/P	**ERR_FATAL/NONFATAL Received (ENR):** Set when either a fatal or a non-fatal error message is received. **Power Well:** Core
1	0x0 RW/1C/V/P	**Multiple ERR_COR Received (MCR):** Set when a correctable error message is received and the CR bit is already set. **Power Well:** Core
0	0x0 RW/1C/V/P	**ERR_COR Received (CR):** Set when a correctable error message is received. **Power Well:** Core

11.4.49 Error Source Identification (ESID)—Offset 134h

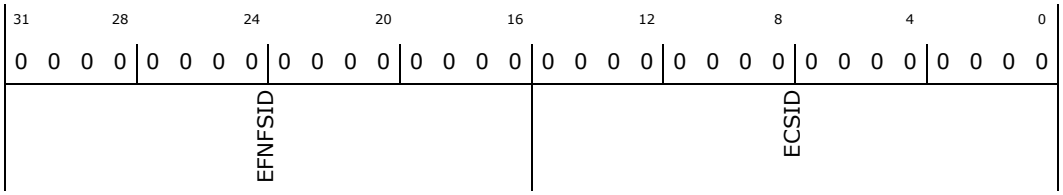
Size:32 bits Identifies the source (Requester ID) of the first correctable and uncorrectable (Non-Fatal / Fatal) errors reported in the Root Error Status register. This register is only reset by a loss of core power.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 134h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message with the ERR_FATAL/NONFATAL Received register is not already set. **Power Well:** Core
15:0	0x0 RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the Requester ID indicated in the received ERR_COR Message with the ERR_COR Received register is not already set. **Power Well:** Core

11.4.50 L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h

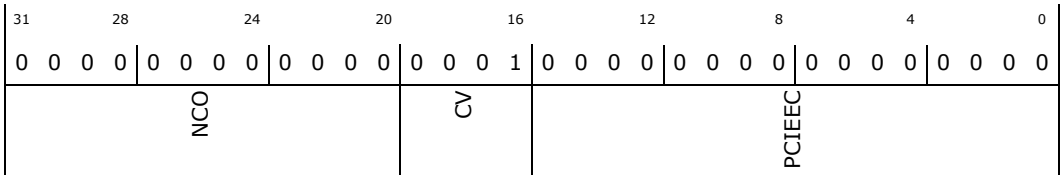
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 200h

Default: 00010000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits. **Power Well:** Core
19:16	0x1 RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
15:0	0x0 RW/O	**PCI Express Extended Capability ID (PCIEEC):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for L1 Substates is [lt]TBD[gt]. **Power Well:** Core

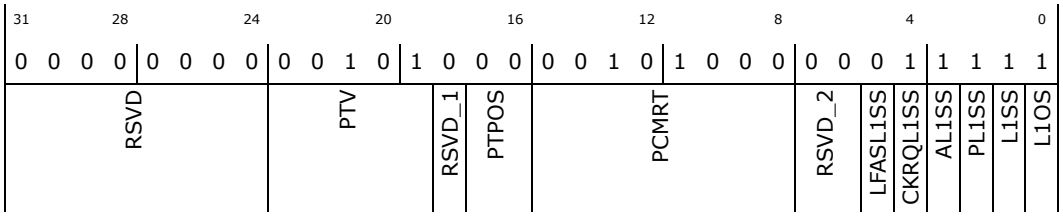
11.4.51 L1 Sub-States Capabilities (L1SCAP)—Offset 204h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 204h

Default: 0028281Fh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
23:19	0x5 RW/O	**Port Tpower_on Value (PTV):** Along with the Port T_POWER_ON Scale Field in the L1 Substates Capabilities register sets theTime (in us) that this Port requires the port on the opposite side of Link to wait in L1.OFF_EXIT after sampling CLKREQ# asserted before actively driving the interface. Port Tpower_on is calculated by multiplying the value in this field by the value in the Port Tpower_on scale field in the L1 Sub-States Capabilities 2 register. Required for all Ports that support L1.OFF. **Power Well:** Core
18	0x0 RO	**Reserved (RSVD_1):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
17:16	0x0 RW/O	**Port Tpower_on Scale (PTPOS):** Specifies the scale used for Tpower_on value field in the L1 Substates Capabilities register. [quote]00b[/quote]: 2 us [quote]01b[/quote]: 10 us [quote]10b[/quote]: 100 us [quote]11b[/quote]: Reserved Required for all Ports that support L1.OFF. **Power Well:** Core
15:8	0x28 RW/O	**Port Common Mode Restore Time (PCMRT):** This is the time (in us) required for this Port to re-establish common mode. Required for all ports that support L1.OFF. **Power Well:** Core
7:6	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
5	0x0 RO	**LFAS L1 Substates Supported (LFASL1SS):** When Set this bit indicates that this Port supports the LFAS mechanism. Required for both Upstream and Downstream Ports. **Power Well:** Core
4	0x1 RO	**CLKREQ# L1 Substates Supported (CKRQL1SS):** When Set this bit indicates that this Port supports the CLKREQ# out-of-band wake mechanism. Required for both Upstream and Downstream Ports. **Power Well:** Core
3	0x1 RW/O	**ASPM L1 Substates Supported (AL1SS):** When set, this bit indicates that this port supports L1 substates for ASPM L1. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static **Power Well:** Core
2	0x1 RW/O	**PCI-PM L1 Substates Supported (PL1SS):** When set, this bit indicates that this port supports L1 substates for PCI-PM. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1	0x1 RW/O	**L1.SNOOZ Supported (L1SS):** When set, this bit indicates that L1.SNOOZ sub-state is supported and this bit must be set by all ports implementing L1 Sub-States. A port that supports L1.OFF must support L1.SNOOZ. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static **Power Well:** Core
0	0x1 RW/O	**L1.OFF Supported (L1OS):** When set, this bit indicates that L1.OFF power management feature is supported. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static **Power Well:** Core

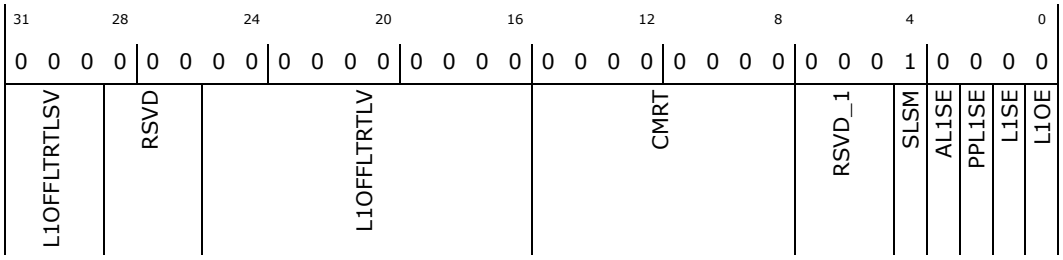
11.4.52 L1 Sub-States Control 1 (L1SCTL1)—Offset 208h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 208h

Default: 00000010h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0x0 RW	**L1.OFF LTR Threshold Latency ScaleValue (L1OFFLTRTLSV):** This field contains the L1.OFF LTR Threshold Latency Scale Value for this particular PCIe root port. The value in this field, together with L1OFFLTRTLV is compared against both the snoop and non-snoop LTR values of the device. 000: L1OFFLTRSTLV times 1 ns 001: L1OFFLTRSTLV times 32 ns 010: L1OFFLTRSTLV times 1024 ns 011: L1OFFLTRSTLV times 32768 ns 100: L1OFFLTRSTLV times 1048576 ns 101: L1OFFLTRSTLV times 33554432 ns Others: Not Permitted. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
28:26	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
25:16	0x0 RW	**L1.OFF LTR Threshold Latency Value (L1OFFLTRTLV):** This field contains the L1.OFF LTR Threshold Latency Value for this particular PCIe root port. The value in this field, together with L1OFFLTRTLSV is compared against both the snoop and non-snoop LTR values of the device. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static **Power Well:** Core
15:8	0x0 RW	**Common Mode Restore Time (CMRT):** This is the Tcommon_mode time the PCIe root port needs to continue sending TS1 and refrain from sending TS2 in Recovery state to allow the TX common mode to be established prior to sending TS2. The timer starts from the time when the first TS1 has been sent and the receiver has detected un-squelch. The value in this field defines the time in micro-seconds. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static **Power Well:** Core
7:5	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
4	0x1 RO	**Select L1 Substates Mechanism (SLSM):** When Set this bit indicates that this Port must use the CLKREQ#-based mechanism, when Clear the LFAS mechanism must be used. Ports that support only one mechanism for L1 Substates are permitted to implement this bit as RO/HwInit, and the value of this bit must reflect the supported mechanism. Default value is implementation-specific. **Power Well:** Core
3	0x0 RW	**ASPM L1 Substates Enabled (AL1SE):** When set, this bit indicates that L1 substates are enabled for ASPM. Required for both upstream and downstream ports. Register Attribute: Dynamic **Power Well:** Core
2	0x0 RW	**PCI-PM L1 Substates Enabled (PPL1SE):** When set, this bit indicates that L1 substates are enabled for PCI-PM. Required for both upstream and downstream ports. Register Attribute: Dynamic **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
1	0x0 RW	**L1.SNOOZ Enable (L1SE):** When set, this bit indicates that L1.SNOOZ power management feature is enabled. If L1.OFF is enabled, L1.SNOOZ must also be enabled. This field must be programmed prior to enabling ASPM L1. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. **Power Well:** Core
0	0x0 RW	**L1.OFF Enable (L1OE):** When set, this bit indicates that L1.OFF power management feature is enabled. L1.OFF can only be enabled if the platform supports bi-directional CLKREQPLUS#. This field must be programmed prior to enabling ASPM L1. Ports that support L1.OFF shall support Latency Tolerance Reporting. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. **Power Well:** Core

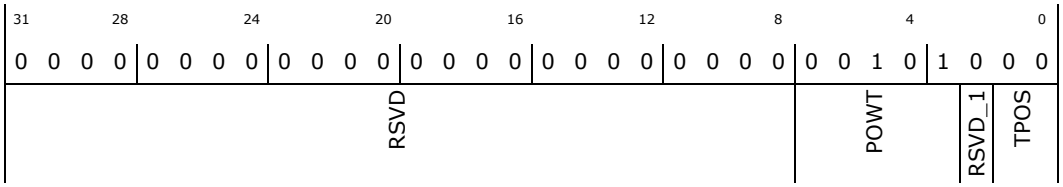
11.4.53 L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 20Ch

Default: 00000028h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
7:3	0x5 RW	**Power On Wait Time (POWT):** Along with the Tpower_on Scale sets the minimum amount of time (in us) that the Port must wait in L1.OFF EXIT after sampling CLKREQPLUS# asserted before actively driving the interface. The timer starts counting when CLKREQPLUS# asserts in L1.OFF state. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
2	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
1:0	0x0 RW	**Tpower_on Scale (TPOS):** Specifies the scale used for Tpower_on value. '00b': 2 us '01b': 10 us '10b': 100us '11b': Reserved. Required for all Ports that support L1.OFF. Register Attribute: Static **Power Well:** Core

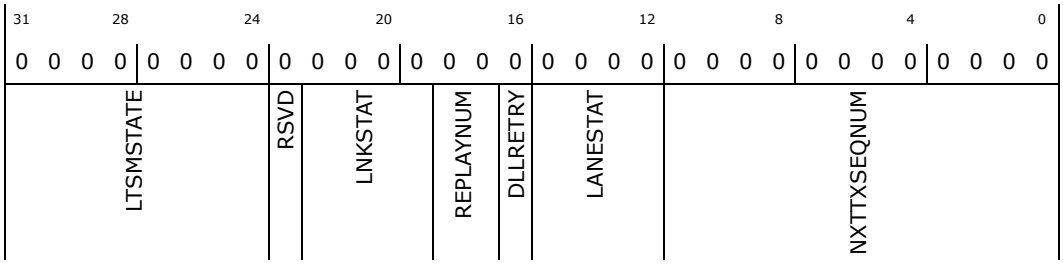
11.4.54 PCI Express Status 1 (PCIESTS1)—Offset 328h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 328h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO/V	**LTSM State (LTSMSTATE):** Indicates the LTSM present state. Hex LTSSM States 00DETIDLE 01DETRDY 02DETIDLEP1TOP2 03DETRDYP2TOP1 04DETRDYINP1 05DETRDYINP1EXE 06DETP2POLLSTART 07DETP1POLLSTART 08DETP2TOP0 09DETP1TOP0 0AECPCMPRETRAIN 0BECPCMFAILP0TOP2 0C DETP0TOP2 0D PMODECHANGE 0EECPCMPCIE 0FECPCMUSB3

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO/V	10DET2POLLINP0 11POLLINGACTIVE 12POLLINGCOMPLIANCEMARGINCNT 13POLLINGCOMPLIANCE 14POLLINGCOMPLIANCESPEEDUP 15POLLINGCOMPLIANCESPEEDDN 16POLLINGCOMPLIANCESPEEDTXEIDLE 17POLLINGCOMPLIANCESPEEDRXEIDLE 18POLLINGCOMPLIANCESPEED 19POLLINGCOMPLIANCESPEEDDONE 1APOLLINGCOMPLIANCEEXIT 1BPOLLINGCONFIGURATION 1C POLLINGTXEIDLE 1D POLLINGEND 1EPOLLINGENDWAIT 1FLINKWIDTHSTART 20LINKWIDTHACCEPT 21LANENUMWAIT 22LANENUMACCEPT 23LANEDESKEW 24CONFIGCOMPLETE 25CONFIGIDLE 26LWNEXITRECOVERY 27CONFIGLPBKENTRY 28CONFIGLPBKLWSTART 29CONFIGLPBKSPEEDTXEIDLE 2ACONFIGLPBKSPEEDSTART 2BCONFIGLPBKSPEEDRXEIDLE 2C CONFIGLPBKSPEED 2D CONFIGLPBKREUTSKIP 2ECONFIGLPBKREUT 2FCONFIGLPBKEXITM 30CONFIGLPBKTXEIDLE 31LWNEXIT 32LWNLNK2DETECT 33L0 34TXL0SRXL0 35RXL0STXL0 36TXL0SRXL0S 37L1TXEIDLE 38L1RCVEIDLE 39L1PREENTRY 3AL1ENTRY 3BL1IDLE 3C L1IDLEGEN2WAIT 3D L1EXIT 3EL2TXEIDLE 3FL2RCVEIDLE 40L2IDLEWAIT 41L2IDLERDY 42L2IDLE 43LOOPBACKENTRY 44LPBKACTIVEMTXSKP 45LPBKACTIVEMSKPDSKW

Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO/V	46LOOPBACKACTIVEM 47LPBKSLAVESPEEDTXEIDLE 48LPBKSLAVESPEEDRXEIDLE 49LPBKSLAVESPEED 4ALOOPBACKACTIVES 4BLOOPBACKCMMSKP 4C LOOPBACKCMM 4D LOOPBACKEXITM 4ELOOPBACKEXITS 4FLOOPBACKEXITL0 50LOOPBACKLNK2DETECT 51LOOPBACK2DETECT 52DISTX16TS1DIS 53DISTXEIDLE 54DISWAITSTART 55DISWAITGNT 56DISWAIT4TXMARGIN 57DISWAIT 58DIS2DETECT 59HOTRESETTS1 5AHOTRESETDONE 5BHOTRESETEIDLE 5C RECOVERYRCVRWAIT 5D RECOVERYRCVRMARGINCNT 5ERECOVERYRCVRLOCK 5FRECOVERYDESKEW 60RECOVERYRCVRCFG 61RECOVERYSPEED 62RECOVERYSPEEDTXEIDLE 63RECOVERYSPEEDRXEIDLE 64RECOVERYSPEEDREADY 65RECOVERYIDLE 66RECOVERYEXITDETECT 67RECOVERYLNK2DETECT 68RECOVERYEXITLPBK 69RECOVERYEXITL0 6ARECOVERYEXITDIS 6BRECOVERYEXITRST Note: This register field could be used by REUT software to monitor the link LTSSM substates. **Power Well:** Core
23	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
22:19	0x0 RO/V	**Link Status (LNKSTAT):** During Link initialization the Link will always traverse this list of state from the top (0000) to the bottom of the list (0111). One or more power management states may be skipped, but the direction of list traversal will remain the same. 0000 Link Down 0001 : Link Retrain 0011 : L1 0100 : L2 0101 : L3 0111 : L0 (Link Up) 1000 : L0s (Transmit [amp] Receive) 1001 : L0s (Transmit only) 1010 : L0s (Receive only) All others reserved **Power Well:** Core
18:17	0x0 RO/V	**Replay Number (REPLAYNUM):** Number of times the Retry Buffer has been replayed since the last Link initialization / re-training. When the Data Link Layer has replayed the contents of the Retry Buffer four times a Link re-training will be initiated which will reset this value back to zero. **Power Well:** Core
16	0x0 RO/V	**Data Link Layer Retry (DLLRETRY):** Indicates when the Data Link Layer has received a corrupted TLP or has detected a dropped packet and is currently waiting for the remote agent to re-transmit the corrupted/dropped packet. The value of Next Receive Sequence Number will be the sequence number associated with the corrupted packet. **Power Well:** Core
15:12	0x0 RO/V	**Lane Status (LANESTAT):** Indicates which lanes are trained. A '1' indicates that the corresponding lane is trained (i.e. bit 0 = '1' means lane 0 is trained). **Power Well:** Core
11:0	0x0 RO/V	**Next Transmitted Sequence Number (NXTTXSEQNUM):** This is the sequence number to be applied to and pre-pended to the next outgoing TLP. **Power Well:** Core

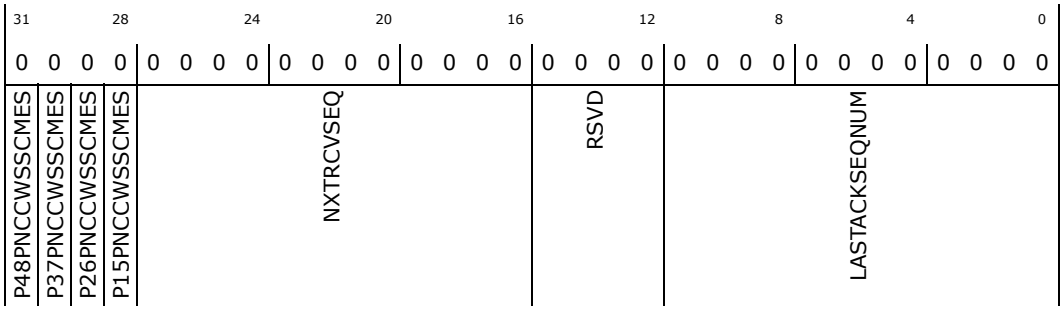
11.4.55 PCI Express Status 2 (PCIESTS2)—Offset 32Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 32Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RO/V	**PCIe Port 4 Non-Common Clock With SSC Mode Enable Strap (P48PNCCWSSCMES):** '0': PCIe port 4 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 4 is enabled to operate in non-common clock mode with SSC enabled. **Power Well:** Core
30	0x0 RO/V	**PCIe Port 3 Non-Common Clock With SSC Mode Enable Strap (P37PNCCWSSCMES):** '0': PCIe port 3 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 3 is enabled to operate in non-common clock mode with SSC enabled. **Power Well:** Core
29	0x0 RO/V	**PCIe Port 2 Non-Common Clock With SSC Mode Enable Strap (P26PNCCWSSCMES):** '0': PCIe port 2 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 2 is enabled to operate in non-common clock mode with SSC enabled. **Power Well:** Core
28	0x0 RO/V	**PCIe Port 1 Non-Common Clock With SSC Mode Enable Strap (P15PNCCWSSCMES):** '0': PCIe port 1 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 1 is enabled to operate in non-common clock mode with SSC enabled. **Power Well:** Core
27:16	0x0 RO/V	**Next Receive Sequence Number (NXTRCVSEQ):** This is the sequence number associated with the TLP that is expected to be received next. **Power Well:** Core
15:12	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
11:0	0x0 RO/V	**Last Acknowledged Sequence Number (LASTACKSEQNUM):** This is the sequence number associated with the last acknowledged TLP. **Power Well:** Core

11.4.56 PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h

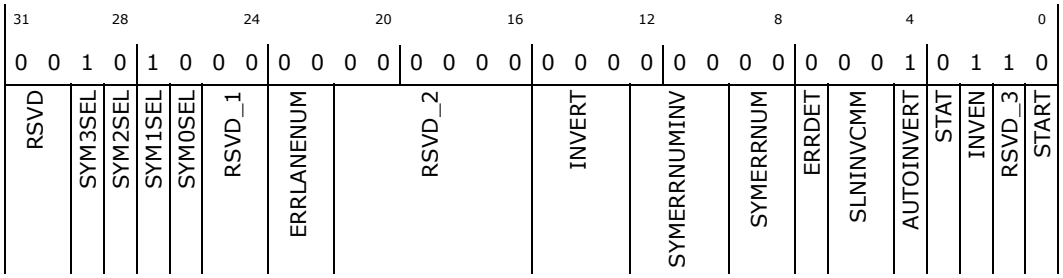
Note that selecting a lane number that does not exist for a port may result in undefined behavior.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 330h

Default: 28000016h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved (RSVD):** Reserved **Power Well:** Core
29	0x1 RW	**CMM Symbol[3] Select (SYM3SEL):** 0: selects CMM Symbol [lb]3[rb] to a control character 1: selects CMM Symbol [lb]3[rb] as a data character **Power Well:** Core
28	0x0 RW	**CMM Symbol[2] Select (SYM2SEL):** 0: selects CMM Symbol [lb]2[rb] to a control character 1: selects CMM Symbol [lb]2[rb] as a data character **Power Well:** Core
27	0x1 RW	**CMM Symbol[1] Select (SYM1SEL):** 0: selects CMM Symbol [lb]1[rb] to a control character 1: selects CMM Symbol [lb]1[rb] as a data character **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
26	0x0 RW	**CMM Symbol[0] Select (SYM0SEL):** 0: selects CMM Symbol [lb]0[rb] to a control character 1: selects CMM Symbol [lb]0[rb] as a data character **Power Well:** Core
25:24	0x0 RO	**Reserved (RSVD_1):** Reserved **Power Well:** Core
23:22	0x0 RO/V	**CMM Error Lane Number (ERRLANENUM):** This field contains the lane number of the failing lane. Only valid when CMM Error Detected is 1. **Power Well:** Core
21:16	0x0 RO	**Reserved (RSVD_2):** Reserved **Power Well:** Core
15:13	0x0 RO/V	**CMM Invert (INVERT):** Indicates which lanes are inverted 000: No inversion 001: Lanes 0 010: Lanes 1 011: Lanes 2 100: Lanes 3 This field is only valid when CMM Error Detected (bit 7) is asserted. Additionally, when CMM Error Detected is asserted this field is locked (will not be updated) **Power Well:** Core
12:10	0x0 RO/V	**CMM Symbol Error Number Invert (SYMERRNUMINV):** Indicates which register number miscompared on the failing lane, if the failing lane was an inverted lane. Only valid when CMM Error Detected is 1. 000: CMM Data D0 001: CMM Data D0 010: CMM Data D0 011: CMM Data D1 100: CMM Data D2 101: CMM Data D3 110: CMM Data D0 111: CMM Data D0 **Power Well:** Core
9:8	0x0 RO/V	**CMM Symbol Error Number (SYMERRNUM):** Indicates which register number miscompared on the failing lane, if the failing lane was not inverted. Only valid when CMM Error Detected is 1. 00: CMM Data 0 01: CMM Data 1 10: CMM Data 2 11: CMM Data 3 **Power Well:** Core

Bit Range	Default & Access	Field Name (ID): Description
7	0x0 RW/1C/V	**CMM Error Detected (ERRDET):** 1: An error was detected 0: No error detected Note: This bit will be shadowed to an observability pin that can be used for IRQ generation. **Power Well:** Core
6:5	0x0 RW	**Select Lane Number to be inverted for CMM (SLNINVCMM):** Select Lane Number to be inverted for CMM **Power Well:** Core
4	0x1 RW	**CMM AutoInvert (AUTOINVERT):** 1: CMM autosequences through the inversion 0: CMM does not sequence inversion **Power Well:** Core
3	0x0 RO/V	**CMM Status (STAT):** This bit is set when the CMM Start bit is set and cleared when the CMM mode has been entered successfully. 0: Compliance Measurement Mode is not active or CMM mode has been entered successfully. 1: Set as a result of CMM Start bit being set. **Power Well:** Core
2	0x1 RW	**CMM Invert Enable (INVEN):** 1: Enables the Inversion of the lane 0: Lane not inverted **Power Well:** Core
1	0x1 RW	**Reserved (RSVD_3):** Reserved. **Power Well:** Core
0	0x0 RW/L	**CMM Start (START):** 1: Start CMM 0: Stop CMM This register bit is Read-Only when the MPC.SRL bit is set. **Power Well:** Core

11.4.57 PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h

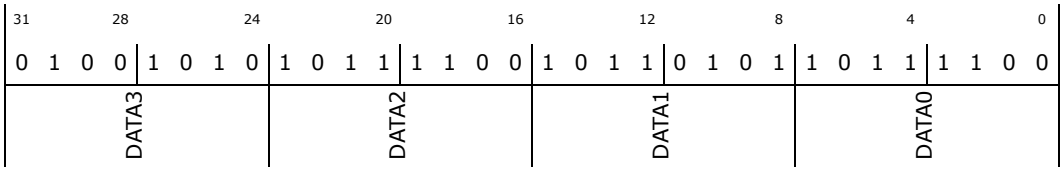
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 334h

Default: 4ABCB5BCh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x4a RW	**CMM Data [3] (DATA3):** This character contains CMM Data [lb]3[rb] that will be transmitted on the link. **Power Well:** Core
23:16	0xbc RW	**CMM Data [2] (DATA2):** This character contains CMM Data [lb]2[rb] that will be transmitted on the link. **Power Well:** Core
15:8	0xb5 RW	**CMM Data [1] (DATA1):** This character contains CMM Data [lb]1[rb] that will be transmitted on the link. **Power Well:** Core
7:0	0xbc RW	**CMM Data [0] (DATA0):** This character contains CMM Data [lb]0[rb] that will be transmitted on the link. **Power Well:** Core

11.4.58 Strap and Fuse Configuration 2 (STRPFUSECFG2)—Offset 414h

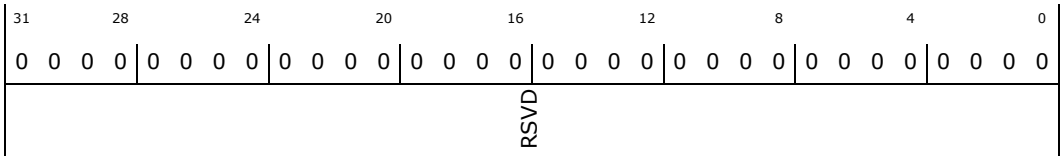
Size:32 bits

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:28, F:3] + 414h

Default: 00000000h



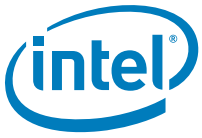
Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved (RSVD):** Reserved. **Power Well:** Core

12 Intel Sensor Hub

12.1 ISH IPC Configuration Registers

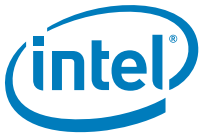
Table 120. Summary of ISH IPC Configuration Registers—0xB1

Offset	Register Name (Register Symbol)	Default Value
0–3h	"reg_PISR_type (PISR)—Offset 0h" on page 6186	00000000h
4–7h	"reg_PIMR_type (PIMR)—Offset 4h" on page 6186	00000000h
8–Bh	"reg_RESERVED0_type (RESERVED0)—Offset 8h" on page 6187	00000000h
C–Fh	"reg_RESERVED1_type (RESERVED1)—Offset Ch" on page 6188	00000000h
10–13h	"reg_RESERVED2_type (RESERVED2)—Offset 10h" on page 6188	00000000h
14–17h	"reg_RESERVED3_type (RESERVED3)—Offset 14h" on page 6189	00000000h
18–1Bh	"reg_RESERVED4_type (RESERVED4)—Offset 18h" on page 6189	00000000h
1C–1Fh	"reg_RESERVED5_type (RESERVED5)—Offset 1Ch" on page 6190	00000000h
20–23h	"reg_RESERVED6_type (RESERVED6)—Offset 20h" on page 6190	00000000h
24–27h	"reg_RESERVED7_type (RESERVED7)—Offset 24h" on page 6191	00000000h
28–2Bh	"reg_RESERVED8_type (RESERVED8)—Offset 28h" on page 6191	00000000h
2C–2Fh	"reg_RESERVED9_type (RESERVED9)—Offset 2Ch" on page 6192	00000000h
30–33h	"reg_RESERVED10_type (RESERVED10)—Offset 30h" on page 6192	00000000h
34–37h	"reg_ISH_HOST_FWSTS_type (ISH_HOST_FWSTS)—Offset 34h" on page 6193	00000000h
38–3Bh	"reg_HOST_COMM_type (HOST_COMM)—Offset 38h" on page 6193	00000000h
3C–3Fh	"reg_ISH_SEC_FWSTS_type (ISH_SEC_FWSTS)—Offset 3Ch" on page 6194	00000000h
40–43h	"reg_SEC_COMM_type (SEC_COMM)—Offset 40h" on page 6194	00000000h
44–47h	"reg_ISH_RST_type (ISH_RST)—Offset 44h" on page 6195	00000000h
48–4Bh	"reg_HOST2ISH_DOORBELL_type (HOST2ISH_DOORBELL)—Offset 48h" on page 6195	00000000h
4C–4Fh	"reg_PMC2ISH_DOORBELL_type (PMC2ISH_DOORBELL)—Offset 4Ch" on page 6196	00000000h
50–53h	"reg_SEC2ISH_DOORBELL_type (SEC2ISH_DOORBELL)—Offset 50h" on page 6197	00000000h
54–57h	"reg_ISH2HOST_DOORBELL_type (ISH2HOST_DOORBELL)—Offset 54h" on page 6197	00000000h
58–5Bh	"reg_ISH2PMC_DOORBELL_type (ISH2PMC_DOORBELL)—Offset 58h" on page 6198	00000000h
5C–5Fh	"reg_ISH2SEC_DOORBELL_type (ISH2SEC_DOORBELL)—Offset 5Ch" on page 6198	00000000h
60–63h	"reg_ISH2HOST_MSG1_type (ISH2HOST_MSG1)—Offset 60h" on page 6199	00000000h
64–67h	"reg_ISH2HOST_MSG2_type (ISH2HOST_MSG2)—Offset 64h" on page 6200	00000000h
68–6Bh	"reg_ISH2HOST_MSG3_type (ISH2HOST_MSG3)—Offset 68h" on page 6200	00000000h
6C–6Fh	"reg_ISH2HOST_MSG4_type (ISH2HOST_MSG4)—Offset 6Ch" on page 6200	00000000h
70–73h	"reg_ISH2HOST_MSG5_type (ISH2HOST_MSG5)—Offset 70h" on page 6201	00000000h
74–77h	"reg_ISH2HOST_MSG6_type (ISH2HOST_MSG6)—Offset 74h" on page 6201	00000000h
78–7Bh	"reg_ISH2HOST_MSG7_type (ISH2HOST_MSG7)—Offset 78h" on page 6202	00000000h



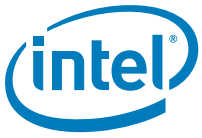
Offset	Register Name (Register Symbol)	Default Value
7C–7Fh	"reg_ISH2HOST_MSG8_type (ISH2HOST_MSG8)—Offset 7Ch" on page 6202	00000000h
80–83h	"reg_ISH2HOST_MSG9_type (ISH2HOST_MSG9)—Offset 80h" on page 6203	00000000h
84–87h	"reg_ISH2HOST_MSG10_type (ISH2HOST_MSG10)—Offset 84h" on page 6203	00000000h
88–8Bh	"reg_ISH2HOST_MSG11_type (ISH2HOST_MSG11)—Offset 88h" on page 6204	00000000h
8C–8Fh	"reg_ISH2HOST_MSG12_type (ISH2HOST_MSG12)—Offset 8Ch" on page 6204	00000000h
90–93h	"reg_ISH2HOST_MSG13_type (ISH2HOST_MSG13)—Offset 90h" on page 6205	00000000h
94–97h	"reg_ISH2HOST_MSG14_type (ISH2HOST_MSG14)—Offset 94h" on page 6205	00000000h
98–9Bh	"reg_ISH2HOST_MSG15_type (ISH2HOST_MSG15)—Offset 98h" on page 6206	00000000h
9C–9Fh	"reg_ISH2HOST_MSG16_type (ISH2HOST_MSG16)—Offset 9Ch" on page 6206	00000000h
A0–A3h	"reg_ISH2HOST_MSG17_type (ISH2HOST_MSG17)—Offset A0h" on page 6207	00000000h
A4–A7h	"reg_ISH2HOST_MSG18_type (ISH2HOST_MSG18)—Offset A4h" on page 6207	00000000h
A8–ABh	"reg_ISH2HOST_MSG19_type (ISH2HOST_MSG19)—Offset A8h" on page 6208	00000000h
AC–AFh	"reg_ISH2HOST_MSG20_type (ISH2HOST_MSG20)—Offset ACh" on page 6208	00000000h
B0–B3h	"reg_ISH2HOST_MSG21_type (ISH2HOST_MSG21)—Offset B0h" on page 6209	00000000h
B4–B7h	"reg_ISH2HOST_MSG22_type (ISH2HOST_MSG22)—Offset B4h" on page 6209	00000000h
B8–BBh	"reg_ISH2HOST_MSG23_type (ISH2HOST_MSG23)—Offset B8h" on page 6210	00000000h
BC–BFh	"reg_ISH2HOST_MSG24_type (ISH2HOST_MSG24)—Offset BCh" on page 6210	00000000h
C0–C3h	"reg_ISH2HOST_MSG25_type (ISH2HOST_MSG25)—Offset C0h" on page 6211	00000000h
C4–C7h	"reg_ISH2HOST_MSG26_type (ISH2HOST_MSG26)—Offset C4h" on page 6211	00000000h
C8–CBh	"reg_ISH2HOST_MSG27_type (ISH2HOST_MSG27)—Offset C8h" on page 6212	00000000h
CC–CFh	"reg_ISH2HOST_MSG28_type (ISH2HOST_MSG28)—Offset CCh" on page 6212	00000000h
D0–D3h	"reg_ISH2HOST_MSG29_type (ISH2HOST_MSG29)—Offset D0h" on page 6213	00000000h
D4–D7h	"reg_ISH2HOST_MSG30_type (ISH2HOST_MSG30)—Offset D4h" on page 6213	00000000h
D8–DBh	"reg_ISH2HOST_MSG31_type (ISH2HOST_MSG31)—Offset D8h" on page 6214	00000000h
DC–DFh	"reg_ISH2HOST_MSG32_type (ISH2HOST_MSG32)—Offset DCh" on page 6214	00000000h
E0–E3h	"reg_HOST2ISH_MSG1_type (HOST2ISH_MSG1)—Offset E0h" on page 6215	00000000h
E4–E7h	"reg_HOST2ISH_MSG2_type (HOST2ISH_MSG2)—Offset E4h" on page 6215	00000000h
E8–EBh	"reg_HOST2ISH_MSG3_type (HOST2ISH_MSG3)—Offset E8h" on page 6216	00000000h
EC–EFh	"reg_HOST2ISH_MSG4_type (HOST2ISH_MSG4)—Offset ECh" on page 6216	00000000h
F0–F3h	"reg_HOST2ISH_MSG5_type (HOST2ISH_MSG5)—Offset F0h" on page 6217	00000000h
F4–F7h	"reg_HOST2ISH_MSG6_type (HOST2ISH_MSG6)—Offset F4h" on page 6217	00000000h
F8–FBh	"reg_HOST2ISH_MSG7_type (HOST2ISH_MSG7)—Offset F8h" on page 6218	00000000h
FC–FFh	"reg_HOST2ISH_MSG8_type (HOST2ISH_MSG8)—Offset FCh" on page 6218	00000000h
100–103h	"reg_HOST2ISH_MSG9_type (HOST2ISH_MSG9)—Offset 100h" on page 6219	00000000h
104–107h	"reg_HOST2ISH_MSG10_type (HOST2ISH_MSG10)—Offset 104h" on page 6219	00000000h

Offset	Register Name (Register Symbol)	Default Value
108–10Bh	"reg_HOST2ISH_MSG11_type (HOST2ISH_MSG11)—Offset 108h" on page 6220	00000000h
10C–10Fh	"reg_HOST2ISH_MSG12_type (HOST2ISH_MSG12)—Offset 10Ch" on page 6220	00000000h
110–113h	"reg_HOST2ISH_MSG13_type (HOST2ISH_MSG13)—Offset 110h" on page 6221	00000000h
114–117h	"reg_HOST2ISH_MSG14_type (HOST2ISH_MSG14)—Offset 114h" on page 6221	00000000h
118–11Bh	"reg_HOST2ISH_MSG15_type (HOST2ISH_MSG15)—Offset 118h" on page 6222	00000000h
11C–11Fh	"reg_HOST2ISH_MSG16_type (HOST2ISH_MSG16)—Offset 11Ch" on page 6222	00000000h
120–123h	"reg_HOST2ISH_MSG17_type (HOST2ISH_MSG17)—Offset 120h" on page 6223	00000000h
124–127h	"reg_HOST2ISH_MSG18_type (HOST2ISH_MSG18)—Offset 124h" on page 6223	00000000h
128–12Bh	"reg_HOST2ISH_MSG19_type (HOST2ISH_MSG19)—Offset 128h" on page 6224	00000000h
12C–12Fh	"reg_HOST2ISH_MSG20_type (HOST2ISH_MSG20)—Offset 12Ch" on page 6224	00000000h
130–133h	"reg_HOST2ISH_MSG21_type (HOST2ISH_MSG21)—Offset 130h" on page 6225	00000000h
134–137h	"reg_HOST2ISH_MSG22_type (HOST2ISH_MSG22)—Offset 134h" on page 6225	00000000h
138–13Bh	"reg_HOST2ISH_MSG23_type (HOST2ISH_MSG23)—Offset 138h" on page 6226	00000000h
13C–13Fh	"reg_HOST2ISH_MSG24_type (HOST2ISH_MSG24)—Offset 13Ch" on page 6226	00000000h
140–143h	"reg_HOST2ISH_MSG25_type (HOST2ISH_MSG25)—Offset 140h" on page 6227	00000000h
144–147h	"reg_HOST2ISH_MSG26_type (HOST2ISH_MSG26)—Offset 144h" on page 6227	00000000h
148–14Bh	"reg_HOST2ISH_MSG27_type (HOST2ISH_MSG27)—Offset 148h" on page 6228	00000000h
14C–14Fh	"reg_HOST2ISH_MSG28_type (HOST2ISH_MSG28)—Offset 14Ch" on page 6228	00000000h
150–153h	"reg_HOST2ISH_MSG29_type (HOST2ISH_MSG29)—Offset 150h" on page 6229	00000000h
154–157h	"reg_HOST2ISH_MSG30_type (HOST2ISH_MSG30)—Offset 154h" on page 6229	00000000h
158–15Bh	"reg_HOST2ISH_MSG31_type (HOST2ISH_MSG31)—Offset 158h" on page 6230	00000000h
15C–15Fh	"reg_HOST2ISH_MSG32_type (HOST2ISH_MSG32)—Offset 15Ch" on page 6230	00000000h



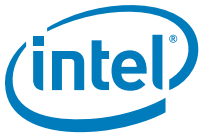
Offset	Register Name (Register Symbol)	Default Value
160–163h	"reg_ISH2SEC_MSG1_type (ISH2SEC_MSG1)—Offset 160h" on page 6231	00000000h
164–167h	"reg_ISH2SEC_MSG2_type (ISH2SEC_MSG2)—Offset 164h" on page 6231	00000000h
168–16Bh	"reg_ISH2SEC_MSG3_type (ISH2SEC_MSG3)—Offset 168h" on page 6232	00000000h
16C–16Fh	"reg_ISH2SEC_MSG4_type (ISH2SEC_MSG4)—Offset 16Ch" on page 6232	00000000h
170–173h	"reg_ISH2SEC_MSG5_type (ISH2SEC_MSG5)—Offset 170h" on page 6233	00000000h
174–177h	"reg_ISH2SEC_MSG6_type (ISH2SEC_MSG6)—Offset 174h" on page 6233	00000000h
178–17Bh	"reg_ISH2SEC_MSG7_type (ISH2SEC_MSG7)—Offset 178h" on page 6233	00000000h
17C–17Fh	"reg_ISH2SEC_MSG8_type (ISH2SEC_MSG8)—Offset 17Ch" on page 6234	00000000h
180–183h	"reg_ISH2SEC_MSG9_type (ISH2SEC_MSG9)—Offset 180h" on page 6234	00000000h
184–187h	"reg_ISH2SEC_MSG10_type (ISH2SEC_MSG10)—Offset 184h" on page 6235	00000000h
188–18Bh	"reg_ISH2SEC_MSG11_type (ISH2SEC_MSG11)—Offset 188h" on page 6235	00000000h
18C–18Fh	"reg_ISH2SEC_MSG12_type (ISH2SEC_MSG12)—Offset 18Ch" on page 6236	00000000h
190–193h	"reg_ISH2SEC_MSG13_type (ISH2SEC_MSG13)—Offset 190h" on page 6236	00000000h
194–197h	"reg_ISH2SEC_MSG14_type (ISH2SEC_MSG14)—Offset 194h" on page 6237	00000000h
198–19Bh	"reg_ISH2SEC_MSG15_type (ISH2SEC_MSG15)—Offset 198h" on page 6237	00000000h
19C–19Fh	"reg_ISH2SEC_MSG16_type (ISH2SEC_MSG16)—Offset 19Ch" on page 6238	00000000h
1A0–1A3h	"reg_ISH2SEC_MSG17_type (ISH2SEC_MSG17)—Offset 1A0h" on page 6238	00000000h
1A4–1A7h	"reg_ISH2SEC_MSG18_type (ISH2SEC_MSG18)—Offset 1A4h" on page 6239	00000000h
1A8–1ABh	"reg_ISH2SEC_MSG19_type (ISH2SEC_MSG19)—Offset 1A8h" on page 6239	00000000h
1AC–1AFh	"reg_ISH2SEC_MSG20_type (ISH2SEC_MSG20)—Offset 1ACh" on page 6240	00000000h
1B0–1B3h	"reg_ISH2SEC_MSG21_type (ISH2SEC_MSG21)—Offset 1B0h" on page 6240	00000000h
1B4–1B7h	"reg_ISH2SEC_MSG22_type (ISH2SEC_MSG22)—Offset 1B4h" on page 6241	00000000h

Offset	Register Name (Register Symbol)	Default Value
1B8–1BBh	"reg_ISH2SEC_MSG23_type (ISH2SEC_MSG23)—Offset 1B8h" on page 6241	00000000h
1BC–1BFh	"reg_ISH2SEC_MSG24_type (ISH2SEC_MSG24)—Offset 1BCh" on page 6242	00000000h
1C0–1C3h	"reg_ISH2SEC_MSG25_type (ISH2SEC_MSG25)—Offset 1C0h" on page 6242	00000000h
1C4–1C7h	"reg_ISH2SEC_MSG26_type (ISH2SEC_MSG26)—Offset 1C4h" on page 6243	00000000h
1C8–1CBh	"reg_ISH2SEC_MSG27_type (ISH2SEC_MSG27)—Offset 1C8h" on page 6243	00000000h
1CC–1CFh	"reg_ISH2SEC_MSG28_type (ISH2SEC_MSG28)—Offset 1CCh" on page 6244	00000000h
1D0–1D3h	"reg_ISH2SEC_MSG29_type (ISH2SEC_MSG29)—Offset 1D0h" on page 6244	00000000h
1D4–1D7h	"reg_ISH2SEC_MSG30_type (ISH2SEC_MSG30)—Offset 1D4h" on page 6245	00000000h
1D8–1DBh	"reg_ISH2SEC_MSG31_type (ISH2SEC_MSG31)—Offset 1D8h" on page 6245	00000000h
1DC–1DFh	"reg_ISH2SEC_MSG32_type (ISH2SEC_MSG32)—Offset 1DCh" on page 6246	00000000h
1E0–1E3h	"reg_SEC2ISH_MSG1_type (SEC2ISH_MSG1)—Offset 1E0h" on page 6246	00000000h
1E4–1E7h	"reg_SEC2ISH_MSG2_type (SEC2ISH_MSG2)—Offset 1E4h" on page 6247	00000000h
1E8–1EBh	"reg_SEC2ISH_MSG3_type (SEC2ISH_MSG3)—Offset 1E8h" on page 6247	00000000h
1EC–1EFh	"reg_SEC2ISH_MSG4_type (SEC2ISH_MSG4)—Offset 1ECh" on page 6248	00000000h
1F0–1F3h	"reg_SEC2ISH_MSG5_type (SEC2ISH_MSG5)—Offset 1F0h" on page 6248	00000000h
1F4–1F7h	"reg_SEC2ISH_MSG6_type (SEC2ISH_MSG6)—Offset 1F4h" on page 6248	00000000h
1F8–1FBh	"reg_SEC2ISH_MSG7_type (SEC2ISH_MSG7)—Offset 1F8h" on page 6249	00000000h
1FC–1FFh	"reg_SEC2ISH_MSG8_type (SEC2ISH_MSG8)—Offset 1FCh" on page 6249	00000000h
200–203h	"reg_SEC2ISH_MSG9_type (SEC2ISH_MSG9)—Offset 200h" on page 6250	00000000h
204–207h	"reg_SEC2ISH_MSG10_type (SEC2ISH_MSG10)—Offset 204h" on page 6250	00000000h
208–20Bh	"reg_SEC2ISH_MSG11_type (SEC2ISH_MSG11)—Offset 208h" on page 6251	00000000h
20C–20Fh	"reg_SEC2ISH_MSG12_type (SEC2ISH_MSG12)—Offset 20Ch" on page 6251	00000000h



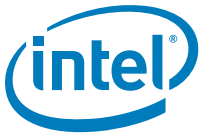
Offset	Register Name (Register Symbol)	Default Value
210–213h	"reg_SEC2ISH_MSG13_type (SEC2ISH_MSG13)—Offset 210h" on page 6252	00000000h
214–217h	"reg_SEC2ISH_MSG14_type (SEC2ISH_MSG14)—Offset 214h" on page 6252	00000000h
218–21Bh	"reg_SEC2ISH_MSG15_type (SEC2ISH_MSG15)—Offset 218h" on page 6253	00000000h
21C–21Fh	"reg_SEC2ISH_MSG16_type (SEC2ISH_MSG16)—Offset 21Ch" on page 6253	00000000h
220–223h	"reg_SEC2ISH_MSG17_type (SEC2ISH_MSG17)—Offset 220h" on page 6254	00000000h
224–227h	"reg_SEC2ISH_MSG18_type (SEC2ISH_MSG18)—Offset 224h" on page 6254	00000000h
228–22Bh	"reg_SEC2ISH_MSG19_type (SEC2ISH_MSG19)—Offset 228h" on page 6255	00000000h
22C–22Fh	"reg_SEC2ISH_MSG20_type (SEC2ISH_MSG20)—Offset 22Ch" on page 6255	00000000h
230–233h	"reg_SEC2ISH_MSG21_type (SEC2ISH_MSG21)—Offset 230h" on page 6256	00000000h
234–237h	"reg_SEC2ISH_MSG22_type (SEC2ISH_MSG22)—Offset 234h" on page 6256	00000000h
238–23Bh	"reg_SEC2ISH_MSG23_type (SEC2ISH_MSG23)—Offset 238h" on page 6257	00000000h
23C–23Fh	"reg_SEC2ISH_MSG24_type (SEC2ISH_MSG24)—Offset 23Ch" on page 6257	00000000h
240–243h	"reg_SEC2ISH_MSG25_type (SEC2ISH_MSG25)—Offset 240h" on page 6258	00000000h
244–247h	"reg_SEC2ISH_MSG26_type (SEC2ISH_MSG26)—Offset 244h" on page 6258	00000000h
248–24Bh	"reg_SEC2ISH_MSG27_type (SEC2ISH_MSG27)—Offset 248h" on page 6259	00000000h
24C–24Fh	"reg_SEC2ISH_MSG28_type (SEC2ISH_MSG28)—Offset 24Ch" on page 6259	00000000h
250–253h	"reg_SEC2ISH_MSG29_type (SEC2ISH_MSG29)—Offset 250h" on page 6260	00000000h
254–257h	"reg_SEC2ISH_MSG30_type (SEC2ISH_MSG30)—Offset 254h" on page 6260	00000000h
258–25Bh	"reg_SEC2ISH_MSG31_type (SEC2ISH_MSG31)—Offset 258h" on page 6261	00000000h
25C–25Fh	"reg_SEC2ISH_MSG32_type (SEC2ISH_MSG32)—Offset 25Ch" on page 6261	00000000h
260–263h	"reg_ISH2PMC_MSG1_type (ISH2PMC_MSG1)—Offset 260h" on page 6262	00000000h
264–267h	"reg_ISH2PMC_MSG2_type (ISH2PMC_MSG2)—Offset 264h" on page 6262	00000000h

Offset	Register Name (Register Symbol)	Default Value
268–26Bh	"reg_ISH2PMC_MSG3_type (ISH2PMC_MSG3)—Offset 268h" on page 6263	00000000h
26C–26Fh	"reg_ISH2PMC_MSG4_type (ISH2PMC_MSG4)—Offset 26Ch" on page 6263	00000000h
270–273h	"reg_ISH2PMC_MSG5_type (ISH2PMC_MSG5)—Offset 270h" on page 6263	00000000h
274–277h	"reg_ISH2PMC_MSG6_type (ISH2PMC_MSG6)—Offset 274h" on page 6264	00000000h
278–27Bh	"reg_ISH2PMC_MSG7_type (ISH2PMC_MSG7)—Offset 278h" on page 6264	00000000h
27C–27Fh	"reg_ISH2PMC_MSG8_type (ISH2PMC_MSG8)—Offset 27Ch" on page 6265	00000000h
280–283h	"reg_ISH2PMC_MSG9_type (ISH2PMC_MSG9)—Offset 280h" on page 6265	00000000h
284–287h	"reg_ISH2PMC_MSG10_type (ISH2PMC_MSG10)—Offset 284h" on page 6266	00000000h
288–28Bh	"reg_ISH2PMC_MSG11_type (ISH2PMC_MSG11)—Offset 288h" on page 6266	00000000h
28C–28Fh	"reg_ISH2PMC_MSG12_type (ISH2PMC_MSG12)—Offset 28Ch" on page 6267	00000000h
290–293h	"reg_ISH2PMC_MSG13_type (ISH2PMC_MSG13)—Offset 290h" on page 6267	00000000h
294–297h	"reg_ISH2PMC_MSG14_type (ISH2PMC_MSG14)—Offset 294h" on page 6268	00000000h
298–29Bh	"reg_ISH2PMC_MSG15_type (ISH2PMC_MSG15)—Offset 298h" on page 6268	00000000h
29C–29Fh	"reg_ISH2PMC_MSG16_type (ISH2PMC_MSG16)—Offset 29Ch" on page 6269	00000000h
2A0–2A3h	"reg_ISH2PMC_MSG17_type (ISH2PMC_MSG17)—Offset 2A0h" on page 6269	00000000h
2A4–2A7h	"reg_ISH2PMC_MSG18_type (ISH2PMC_MSG18)—Offset 2A4h" on page 6270	00000000h
2A8–2ABh	"reg_ISH2PMC_MSG19_type (ISH2PMC_MSG19)—Offset 2A8h" on page 6270	00000000h
2AC–2AFh	"reg_ISH2PMC_MSG20_type (ISH2PMC_MSG20)—Offset 2ACh" on page 6271	00000000h
2B0–2B3h	"reg_ISH2PMC_MSG21_type (ISH2PMC_MSG21)—Offset 2B0h" on page 6271	00000000h
2B4–2B7h	"reg_ISH2PMC_MSG22_type (ISH2PMC_MSG22)—Offset 2B4h" on page 6272	00000000h
2B8–2BBh	"reg_ISH2PMC_MSG23_type (ISH2PMC_MSG23)—Offset 2B8h" on page 6272	00000000h
2BC–2BFh	"reg_ISH2PMC_MSG24_type (ISH2PMC_MSG24)—Offset 2BCh" on page 6273	00000000h



Offset	Register Name (Register Symbol)	Default Value
2C0–2C3h	"reg_ISH2PMC_MSG25_type (ISH2PMC_MSG25)—Offset 2C0h" on page 6273	00000000h
2C4–2C7h	"reg_ISH2PMC_MSG26_type (ISH2PMC_MSG26)—Offset 2C4h" on page 6274	00000000h
2C8–2CBh	"reg_ISH2PMC_MSG27_type (ISH2PMC_MSG27)—Offset 2C8h" on page 6274	00000000h
2CC–2CFh	"reg_ISH2PMC_MSG28_type (ISH2PMC_MSG28)—Offset 2CCh" on page 6275	00000000h
2D0–2D3h	"reg_ISH2PMC_MSG29_type (ISH2PMC_MSG29)—Offset 2D0h" on page 6275	00000000h
2D4–2D7h	"reg_ISH2PMC_MSG30_type (ISH2PMC_MSG30)—Offset 2D4h" on page 6276	00000000h
2D8–2DBh	"reg_ISH2PMC_MSG31_type (ISH2PMC_MSG31)—Offset 2D8h" on page 6276	00000000h
2DC–2DFh	"reg_ISH2PMC_MSG32_type (ISH2PMC_MSG32)—Offset 2DCh" on page 6277	00000000h
2E0–2E3h	"reg_PMC2ISH_MSG1_type (PMC2ISH_MSG1)—Offset 2E0h" on page 6277	00000000h
2E4–2E7h	"reg_PMC2ISH_MSG2_type (PMC2ISH_MSG2)—Offset 2E4h" on page 6278	00000000h
2E8–2EBh	"reg_PMC2ISH_MSG3_type (PMC2ISH_MSG3)—Offset 2E8h" on page 6278	00000000h
2EC–2EFh	"reg_PMC2ISH_MSG4_type (PMC2ISH_MSG4)—Offset 2ECh" on page 6278	00000000h
2F0–2F3h	"reg_PMC2ISH_MSG5_type (PMC2ISH_MSG5)—Offset 2F0h" on page 6279	00000000h
2F4–2F7h	"reg_PMC2ISH_MSG6_type (PMC2ISH_MSG6)—Offset 2F4h" on page 6279	00000000h
2F8–2FBh	"reg_PMC2ISH_MSG7_type (PMC2ISH_MSG7)—Offset 2F8h" on page 6280	00000000h
2FC–2FFh	"reg_PMC2ISH_MSG8_type (PMC2ISH_MSG8)—Offset 2FCh" on page 6280	00000000h
300–303h	"reg_PMC2ISH_MSG9_type (PMC2ISH_MSG9)—Offset 300h" on page 6281	00000000h
304–307h	"reg_PMC2ISH_MSG10_type (PMC2ISH_MSG10)—Offset 304h" on page 6281	00000000h
308–30Bh	"reg_PMC2ISH_MSG11_type (PMC2ISH_MSG11)—Offset 308h" on page 6282	00000000h
30C–30Fh	"reg_PMC2ISH_MSG12_type (PMC2ISH_MSG12)—Offset 30Ch" on page 6282	00000000h
310–313h	"reg_PMC2ISH_MSG13_type (PMC2ISH_MSG13)—Offset 310h" on page 6282	00000000h
314–317h	"reg_PMC2ISH_MSG14_type (PMC2ISH_MSG14)—Offset 314h" on page 6283	00000000h

Offset	Register Name (Register Symbol)	Default Value
318–31Bh	"reg_PMC2ISH_MSG15_type (PMC2ISH_MSG15)—Offset 318h" on page 6283	00000000h
31C–31Fh	"reg_PMC2ISH_MSG16_type (PMC2ISH_MSG16)—Offset 31Ch" on page 6284	00000000h
320–323h	"reg_PMC2ISH_MSG17_type (PMC2ISH_MSG17)—Offset 320h" on page 6284	00000000h
324–327h	"reg_PMC2ISH_MSG18_type (PMC2ISH_MSG18)—Offset 324h" on page 6285	00000000h
328–32Bh	"reg_PMC2ISH_MSG19_type (PMC2ISH_MSG19)—Offset 328h" on page 6285	00000000h
32C–32Fh	"reg_PMC2ISH_MSG20_type (PMC2ISH_MSG20)—Offset 32Ch" on page 6286	00000000h
330–333h	"reg_PMC2ISH_MSG21_type (PMC2ISH_MSG21)—Offset 330h" on page 6286	00000000h
334–337h	"reg_PMC2ISH_MSG22_type (PMC2ISH_MSG22)—Offset 334h" on page 6287	00000000h
338–33Bh	"reg_PMC2ISH_MSG23_type (PMC2ISH_MSG23)—Offset 338h" on page 6287	00000000h
33C–33Fh	"reg_PMC2ISH_MSG24_type (PMC2ISH_MSG24)—Offset 33Ch" on page 6288	00000000h
340–343h	"reg_PMC2ISH_MSG25_type (PMC2ISH_MSG25)—Offset 340h" on page 6288	00000000h
344–347h	"reg_PMC2ISH_MSG26_type (PMC2ISH_MSG26)—Offset 344h" on page 6289	00000000h
348–34Bh	"reg_PMC2ISH_MSG27_type (PMC2ISH_MSG27)—Offset 348h" on page 6289	00000000h
34C–34Fh	"reg_PMC2ISH_MSG28_type (PMC2ISH_MSG28)—Offset 34Ch" on page 6290	00000000h
350–353h	"reg_PMC2ISH_MSG29_type (PMC2ISH_MSG29)—Offset 350h" on page 6290	00000000h
354–357h	"reg_PMC2ISH_MSG30_type (PMC2ISH_MSG30)—Offset 354h" on page 6291	00000000h
358–35Bh	"reg_PMC2ISH_MSG31_type (PMC2ISH_MSG31)—Offset 358h" on page 6291	00000000h
35C–35Fh	"reg_PMC2ISH_MSG32_type (PMC2ISH_MSG32)—Offset 35Ch" on page 6292	00000000h
360–363h	"reg_REMAP0_type (REMAP0)—Offset 360h" on page 6292	00000000h
364–367h	"reg_REMAP1_type (REMAP1)—Offset 364h" on page 6293	00000000h
368–36Bh	"reg_REMAP2_type (REMAP2)—Offset 368h" on page 6293	00000000h
36C–36Fh	"reg_REMAP3_type (REMAP3)—Offset 36Ch" on page 6294	00000000h



Offset	Register Name (Register Symbol)	Default Value
370–373h	"reg_REMAP4_type (REMAP4)—Offset 370h" on page 6294	00000000h
374–377h	"reg_REMAP5_type (REMAP5)—Offset 374h" on page 6295	00000000h
378–37Bh	"reg_ISH_IPC_BUSY_CLEAR_type (ISH_IPC_BUSY_CLEAR)—Offset 378h" on page 6295	00000000h
37C–37Fh	"reg_ISH_FUSE_type (ISH_FUSE)—Offset 37Ch" on page 6296	00000000h
380–383h	"reg_UMA_RANGE_LOWER_0_type (UMA_RANGE_LOWER_0)—Offset 380h" on page 6297	FFFFF000h
384–387h	"reg_UMA_RANGE_LOWER_1_type (UMA_RANGE_LOWER_1)—Offset 384h" on page 6297	00000000h
388–38Bh	"reg_UMA_RANGE_UPPER_0_type (UMA_RANGE_UPPER_0)—Offset 388h" on page 6298	FFFFF000h
38C–38Fh	"reg_UMA_RANGE_UPPER_1_type (UMA_RANGE_UPPER_1)—Offset 38Ch" on page 6299	00000000h

12.1.1 reg_PISR_type (PISR)—Offset 0h

Reserved

Access Method

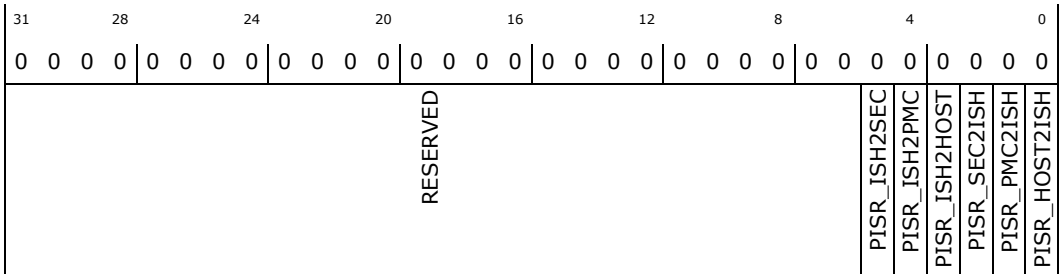
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**RESERVED:** ish_clk
5	0x0 RO	**PISR_ISH2SEC:** ish_clk
4	0x0 RO	**PISR_ISH2PMC:** ish_clk
3	0x0 RO	**PISR_ISH2HOST:** ish_clk
2	0x0 RO	**PISR_SEC2ISH:** ish_clk
1	0x0 RO	**PISR_PMC2ISH:** ish_clk
0	0x0 RO	**PISR_HOST2ISH:** ish_clk

12.1.2 reg_PIMR_type (PIMR)—Offset 4h

Reserved

Access Method

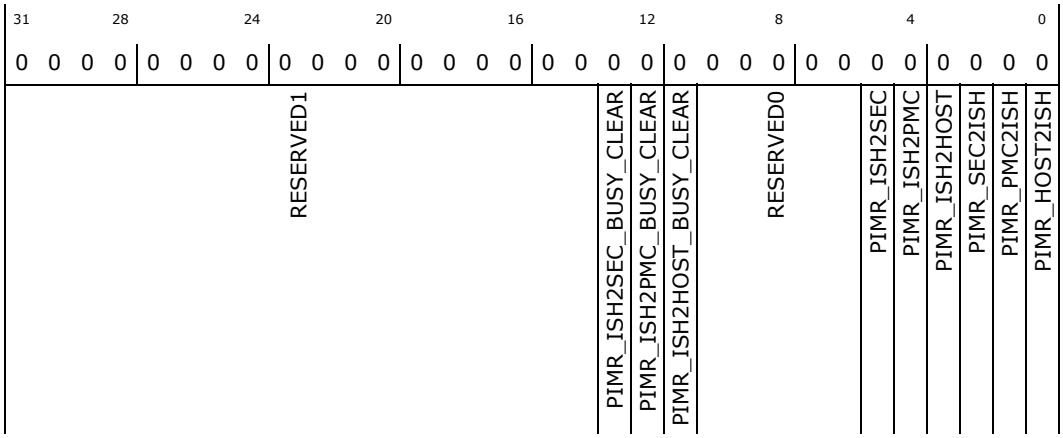
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**RESERVED1:** ish_clk
13	0x0 RW	**PIMR_ISH2SEC_BUSY_CLEAR:** ish_clk
12	0x0 RW	**PIMR_ISH2PMC_BUSY_CLEAR:** ish_clk
11	0x0 RW	**PIMR_ISH2HOST_BUSY_CLEAR:** ish_clk
10:6	0x0 RO	**RESERVED0:** ish_clk
5	0x0 RW	**PIMR_ISH2SEC:** ish_clk
4	0x0 RW	**PIMR_ISH2PMC:** ish_clk
3	0x0 RW	**PIMR_ISH2HOST:** ish_clk
2	0x0 RW	**PIMR_SEC2ISH:** ish_clk
1	0x0 RW	**PIMR_PMC2ISH:** ish_clk
0	0x0 RW	**PIMR_HOST2ISH:** ish_clk

12.1.3 reg_RESERVED0_type (RESERVED0)—Offset 8h

Reserved

Access Method

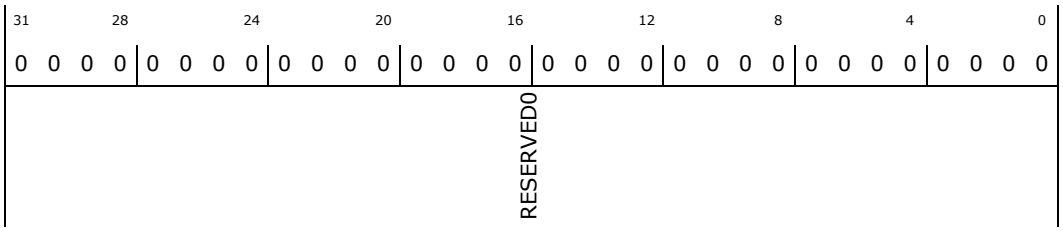
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED0:** ish_clk

12.1.4 reg_RESERVED1_type (RESERVED1)—Offset Ch

Reserved

Access Method

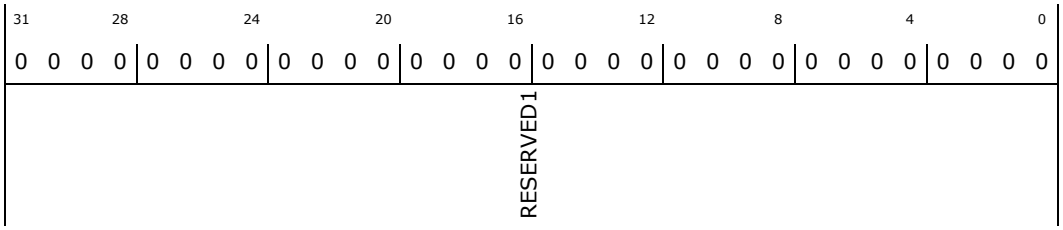
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED1:** ish_clk

12.1.5 reg_RESERVED2_type (RESERVED2)—Offset 10h

Reserved

Access Method

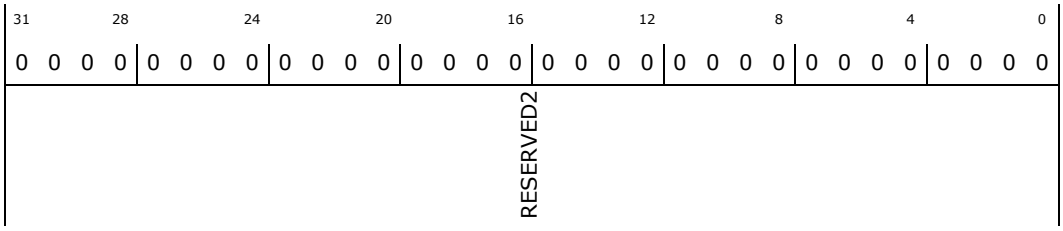
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED2:** ish_clk

12.1.6 reg_RESERVED3_type (RESERVED3)—Offset 14h

Reserved

Access Method

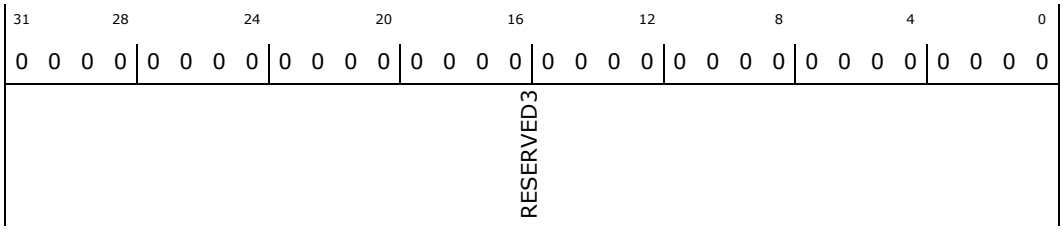
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 14h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED3:** ish_clk

12.1.7 reg_RESERVED4_type (RESERVED4)—Offset 18h

Reserved

Access Method

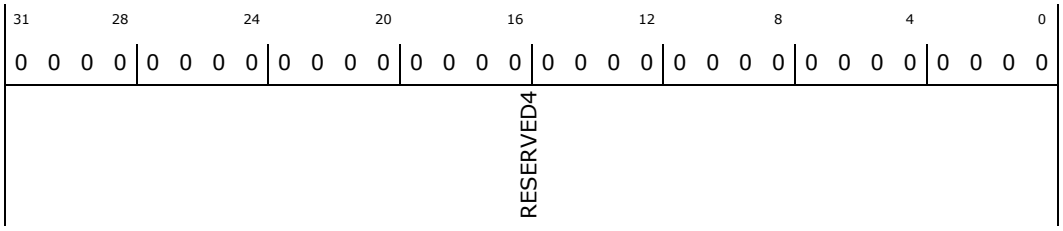
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 18h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED4:** ish_clk

12.1.8 reg_RESERVED5_type (RESERVED5)—Offset 1Ch

Reserved

Access Method

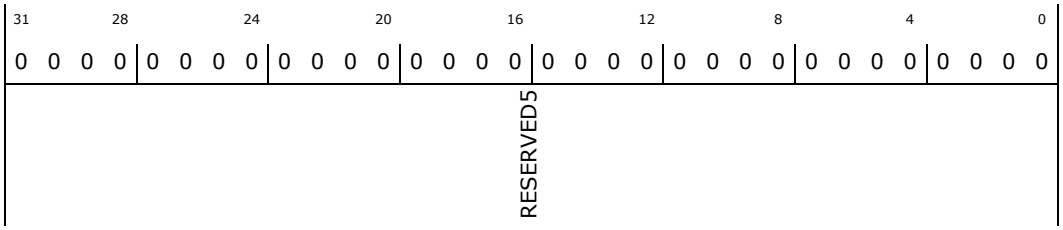
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED5:** ish_clk

12.1.9 reg_RESERVED6_type (RESERVED6)—Offset 20h

Reserved

Access Method

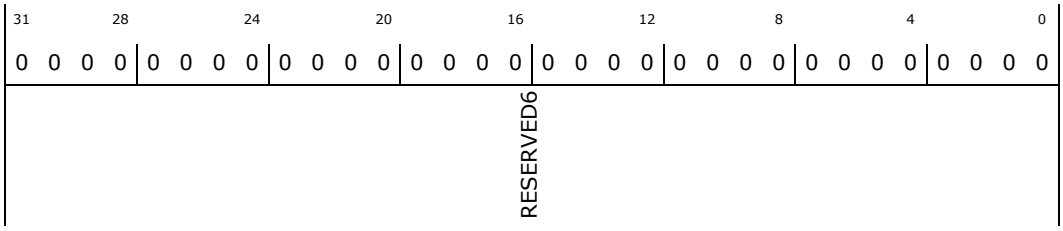
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 20h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED6:** ish_clk

12.1.10 reg_RESERVED7_type (RESERVED7)—Offset 24h

Reserved

Access Method

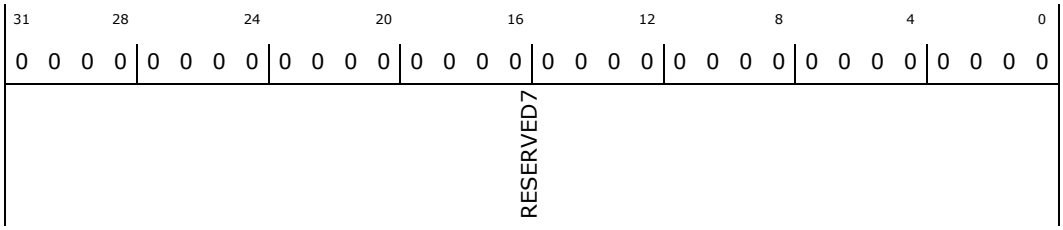
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 24h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED7:** ish_clk

12.1.11 reg_RESERVED8_type (RESERVED8)—Offset 28h

Reserved

Access Method

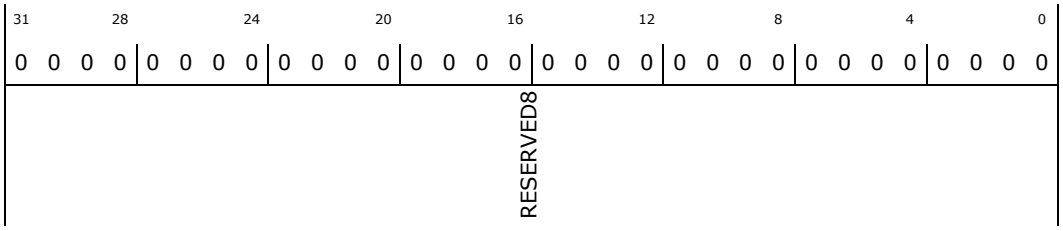
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 28h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED8:** ish_clk

12.1.12 reg_RESERVED9_type (RESERVED9)—Offset 2Ch

Reserved

Access Method

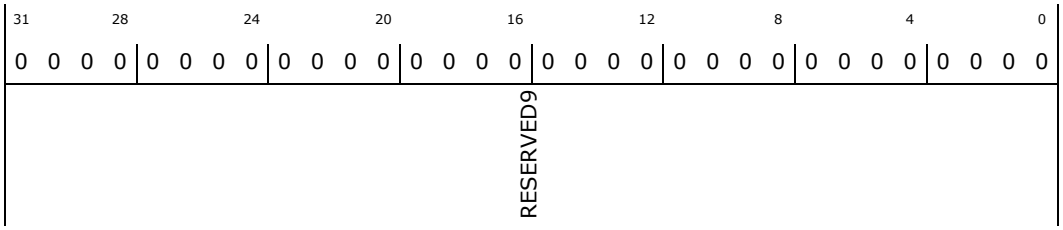
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED9:** ish_clk

12.1.13 reg_RESERVED10_type (RESERVED10)—Offset 30h

Reserved

Access Method

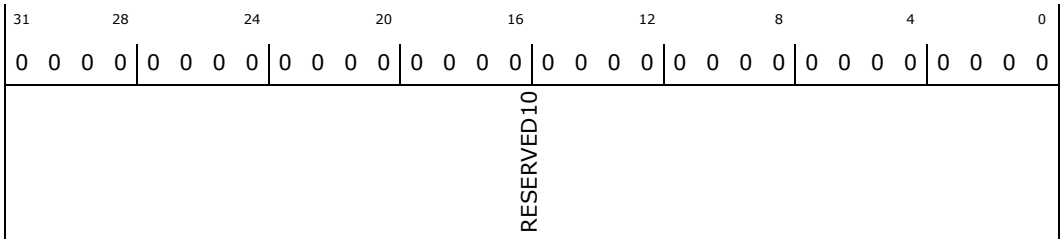
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 30h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED10:** ish_clk

12.1.14 reg_ISH_HOST_FWSTS_type (ISH_HOST_FWSTS)—Offset 34h

ISH Host firmware status

Access Method

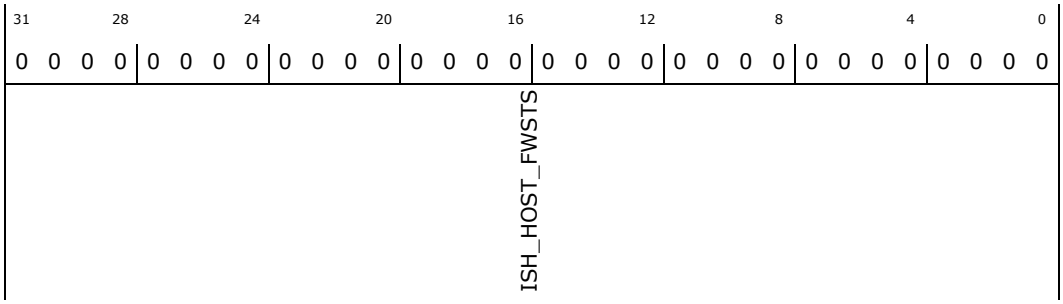
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 34h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**ISH_HOST_FWSTS:** ish_clk

12.1.15 reg_HOST_COMM_type (HOST_COMM)—Offset 38h

Host communication register

Access Method

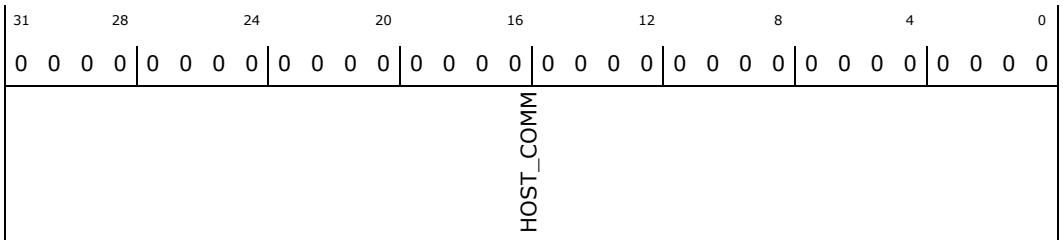
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 38h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**HOST_COMM:** ish_clk

12.1.16 reg_ISH_SEC_FWSTS_type (ISH_SEC_FWSTS)—Offset 3Ch

ISH SEC firmware status

Access Method

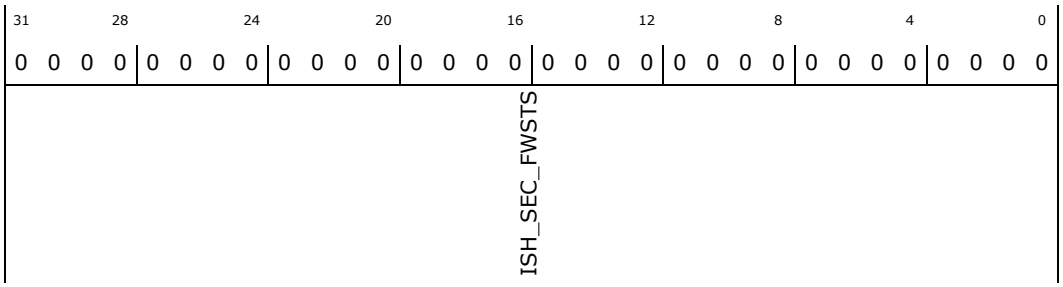
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 3Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**ISH_SEC_FWSTS:** ish_clk

12.1.17 reg_SEC_COMM_type (SEC_COMM)—Offset 40h

SEC communication register

Access Method

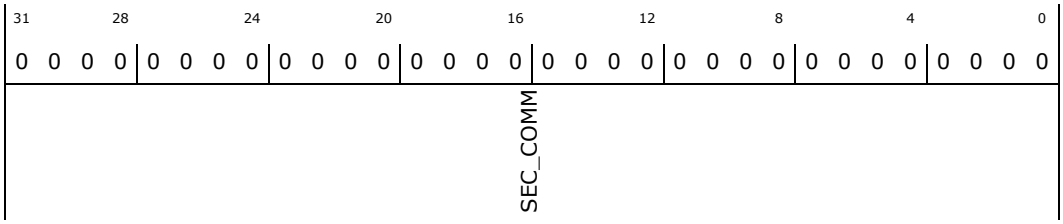
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 40h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SEC_COMM:** ish_clk

12.1.18 reg_ISH_RST_type (ISH_RST)—Offset 44h

Reset register used to reset minuteIA

Access Method

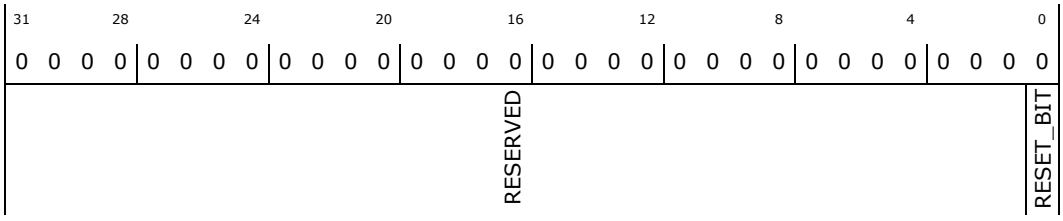
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 44h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RESERVED:** ish_clk
0	0x0 RW	**RESET_BIT:** ish_clk

12.1.19 reg_HOST2ISH_DOORBELL_type (HOST2ISH_DOORBELL)—Offset 48h

When this bit is cleared, the ISH CPU is Ready to accept a new message

Access Method

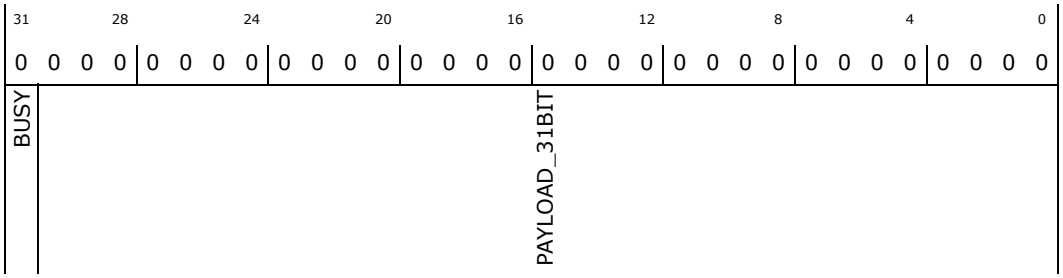
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 48h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**BUSY:** ish_clk
30:0	0x0 RW	**PAYLOAD_31BIT:** ish_clk

12.1.20 reg_PMC2ISH_DOORBELL_type (PMC2ISH_DOORBELL)—Offset 4Ch

When this bit is cleared, the ISH CPU is Ready to accept a new message

Access Method

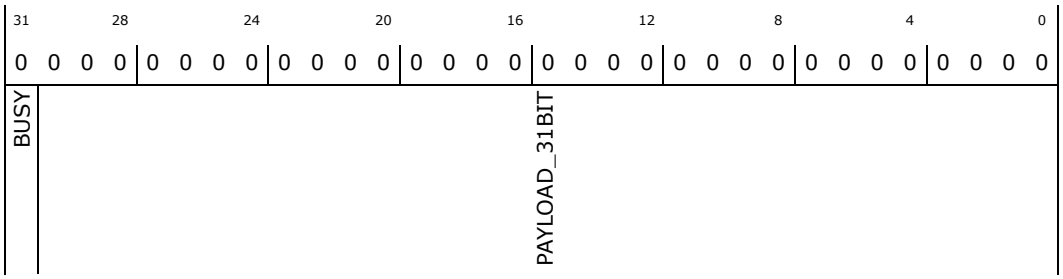
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 4Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**BUSY:** ish_clk

Bit Range	Default & Access	Field Name (ID): Description
30:0	0x0 RW	**PAYLOAD_31BIT:** ish_clk

12.1.21 reg_SEC2ISH_DOORBELL_type (SEC2ISH_DOORBELL)—Offset 50h

When this bit is cleared, the ISH CPU is Ready to accept a new message

Access Method

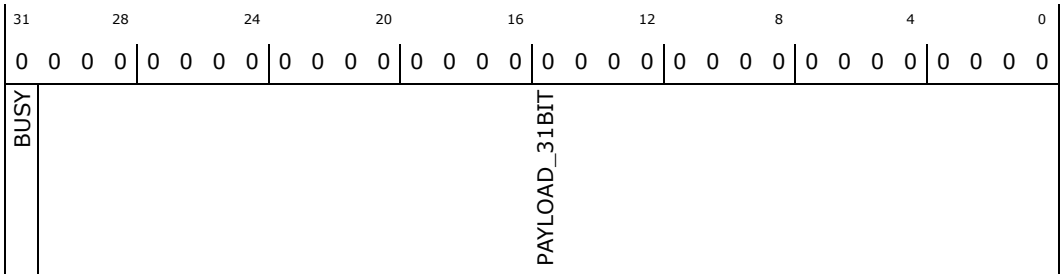
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 50h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**BUSY:** ish_clk
30:0	0x0 RW	**PAYLOAD_31BIT:** ish_clk

12.1.22 reg_ISH2HOST_DOORBELL_type (ISH2HOST_DOORBELL)—Offset 54h

When this bit is cleared, the HOST CPU is Ready to accept a new message

Access Method

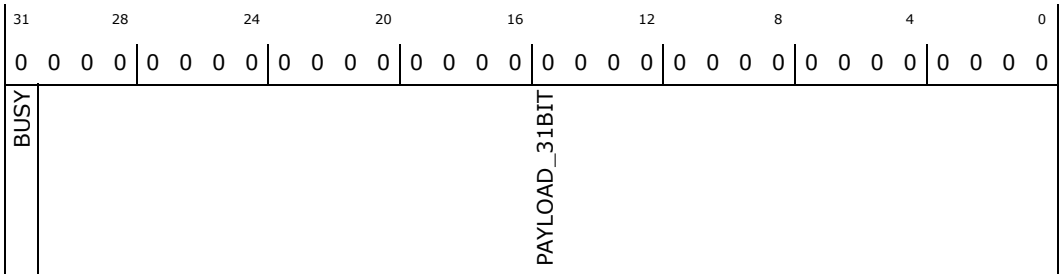
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 54h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**BUSY:** ish_clk
30:0	0x0 RW	**PAYLOAD_31BIT:** ish_clk

12.1.23 reg_ISH2PMC_DOORBELL_type (ISH2PMC_DOORBELL)—Offset 58h

When this bit is cleared, the PMC CPU is Ready to accept a new message

Access Method

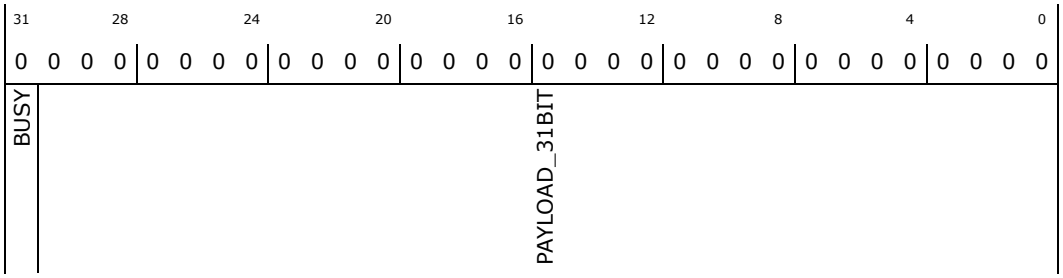
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 58h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**BUSY:** ish_clk
30:0	0x0 RW	**PAYLOAD_31BIT:** ish_clk

12.1.24 reg_ISH2SEC_DOORBELL_type (ISH2SEC_DOORBELL)—Offset 5Ch

When this bit is cleared, the SEC CPU is Ready to accept a new message

Access Method

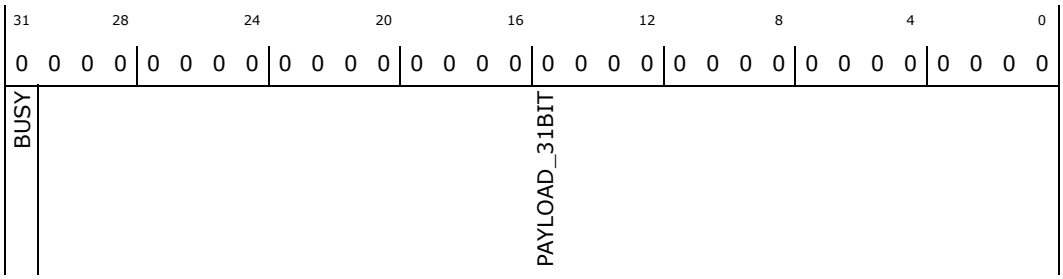
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 5Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**BUSY:** ish_clk
30:0	0x0 RW	**PAYLOAD_31BIT:** ish_clk

12.1.25 reg_ISH2HOST_MSG1_type (ISH2HOST_MSG1)—Offset 60h

Message from ISH to HOST

Access Method

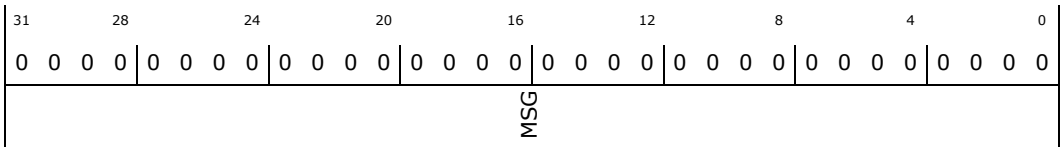
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 60h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.26 reg_ISH2HOST_MSG2_type (ISH2HOST_MSG2)—Offset 64h

Message from ISH to HOST

Access Method

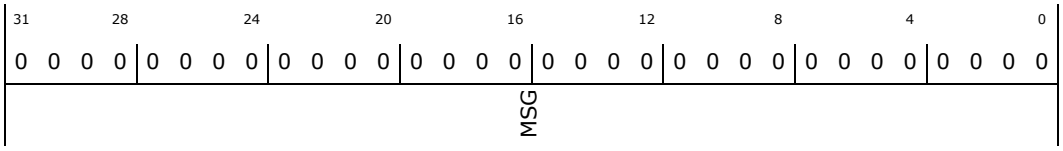
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 64h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.27 reg_ISH2HOST_MSG3_type (ISH2HOST_MSG3)—Offset 68h

Message from ISH to HOST

Access Method

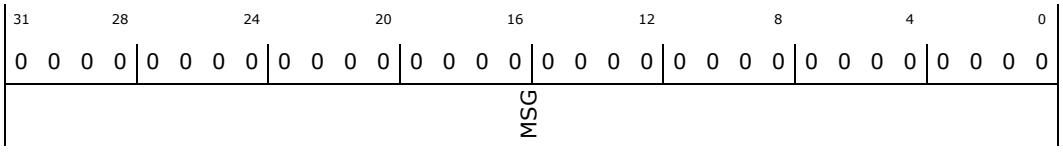
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 68h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.28 reg_ISH2HOST_MSG4_type (ISH2HOST_MSG4)—Offset 6Ch

Message from ISH to HOST

Access Method

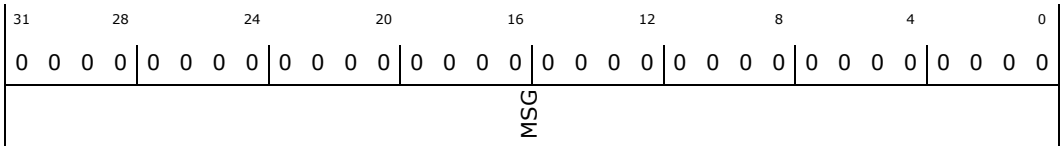
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 6Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.29 reg_ISH2HOST_MSG5_type (ISH2HOST_MSG5)—Offset 70h

Message from ISH to HOST

Access Method

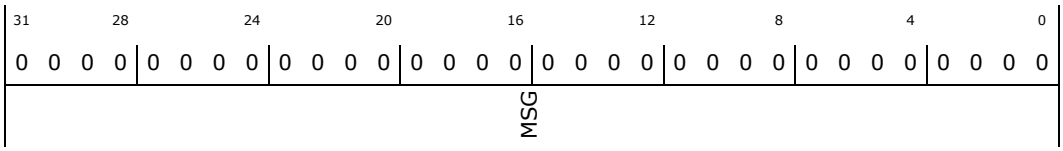
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 70h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.30 reg_ISH2HOST_MSG6_type (ISH2HOST_MSG6)—Offset 74h

Message from ISH to HOST

Access Method

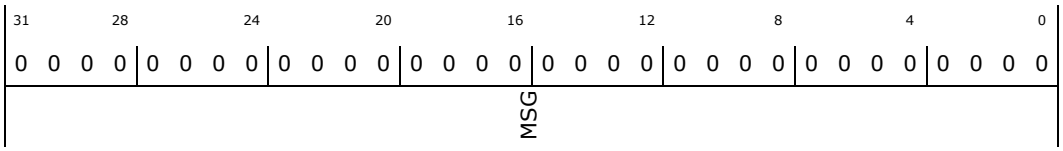
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 74h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.31 reg_ISH2HOST_MSG7_type (ISH2HOST_MSG7)—Offset 78h

Message from ISH to HOST

Access Method

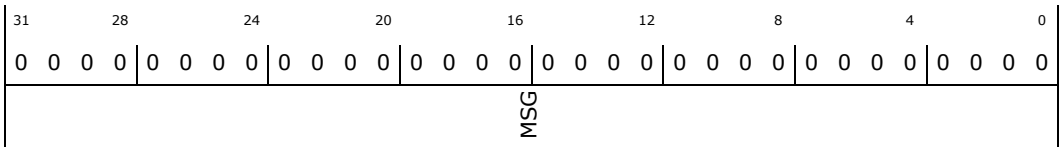
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 78h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.32 reg_ISH2HOST_MSG8_type (ISH2HOST_MSG8)—Offset 7Ch

Message from ISH to HOST

Access Method

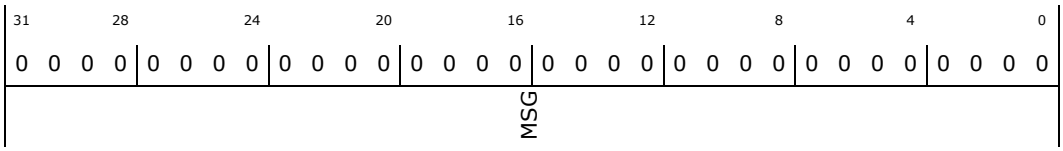
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 7Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.33 reg_ISH2HOST_MSG9_type (ISH2HOST_MSG9)—Offset 80h

Message from ISH to HOST

Access Method

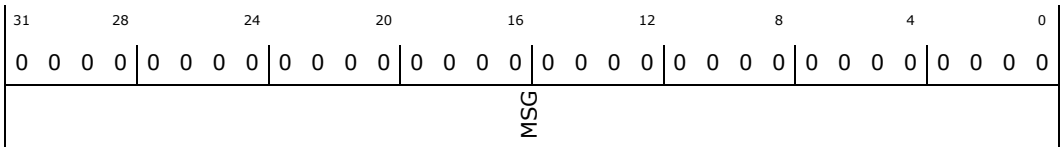
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 80h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.34 reg_ISH2HOST_MSG10_type (ISH2HOST_MSG10)—Offset 84h

Message from ISH to HOST

Access Method

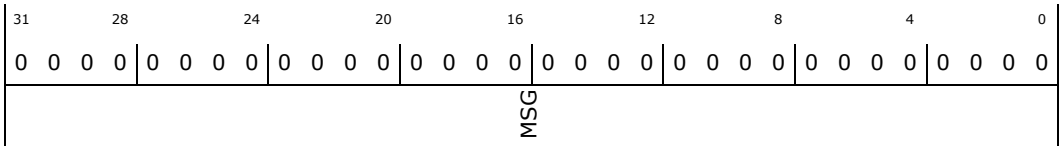
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 84h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.35 reg_ISH2HOST_MSG11_type (ISH2HOST_MSG11)—Offset 88h

Message from ISH to HOST

Access Method

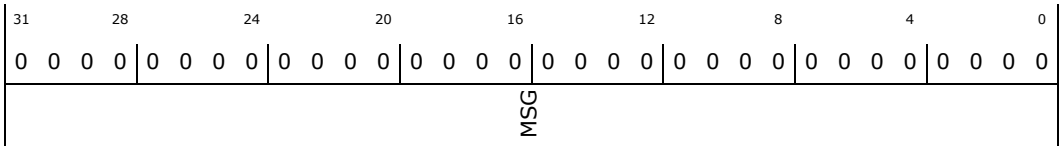
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 88h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.36 reg_ISH2HOST_MSG12_type (ISH2HOST_MSG12)—Offset 8Ch

Message from ISH to HOST

Access Method

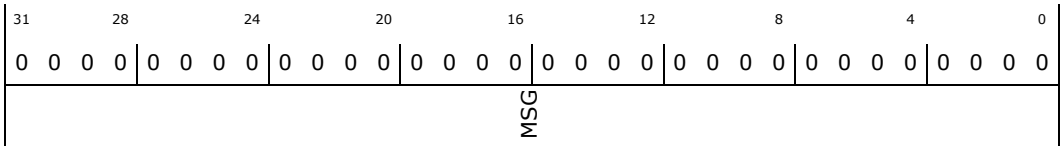
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 8Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.37 reg_ISH2HOST_MSG13_type (ISH2HOST_MSG13)—Offset 90h

Message from ISH to HOST

Access Method

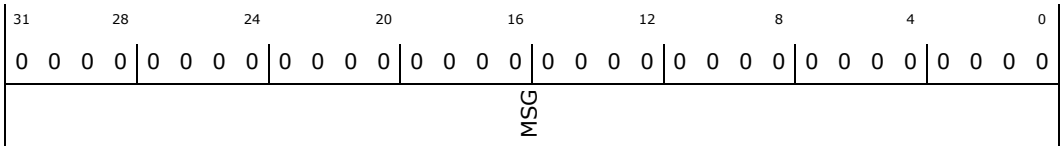
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 90h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.38 reg_ISH2HOST_MSG14_type (ISH2HOST_MSG14)—Offset 94h

Message from ISH to HOST

Access Method

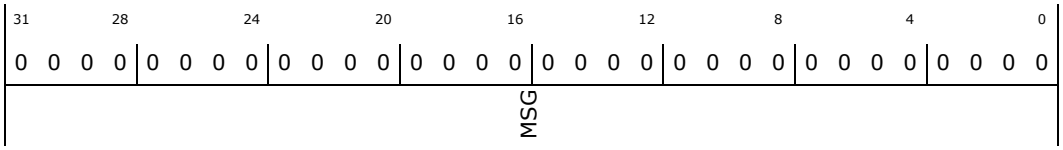
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 94h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.39 reg_ISH2HOST_MSG15_type (ISH2HOST_MSG15)—Offset 98h

Message from ISH to HOST

Access Method

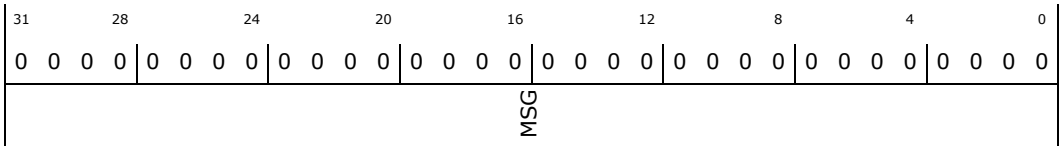
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 98h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.40 reg_ISH2HOST_MSG16_type (ISH2HOST_MSG16)—Offset 9Ch

Message from ISH to HOST

Access Method

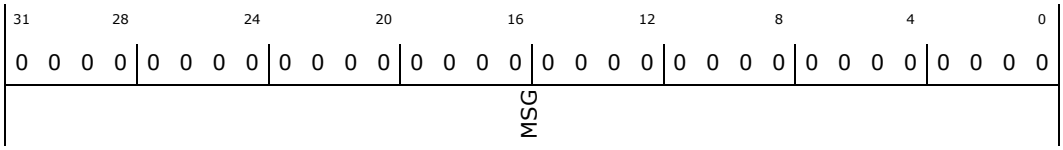
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 9Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.41 reg_ISH2HOST_MSG17_type (ISH2HOST_MSG17)—Offset A0h

Message from ISH to HOST

Access Method

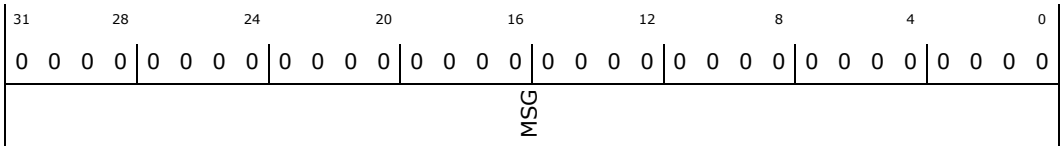
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + A0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.42 reg_ISH2HOST_MSG18_type (ISH2HOST_MSG18)—Offset A4h

Message from ISH to HOST

Access Method

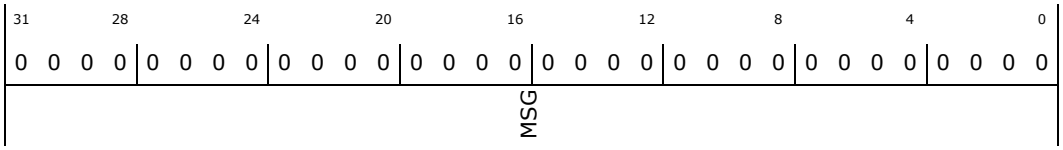
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + A4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.43 reg_ISH2HOST_MSG19_type (ISH2HOST_MSG19)—Offset A8h

Message from ISH to HOST

Access Method

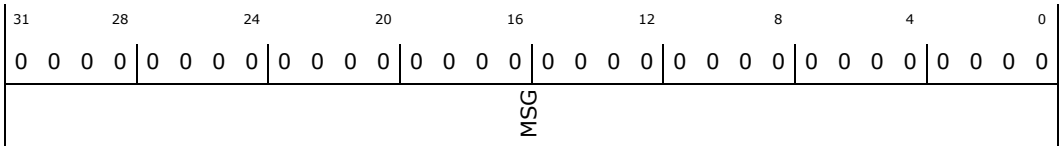
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + A8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.44 reg_ISH2HOST_MSG20_type (ISH2HOST_MSG20)—Offset ACh

Message from ISH to HOST

Access Method

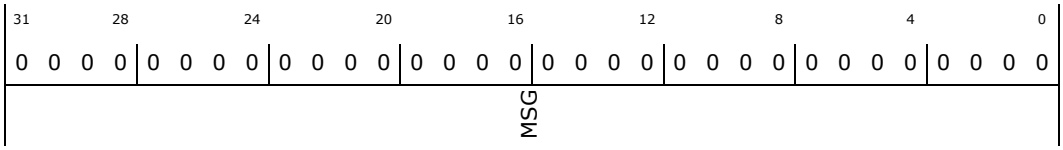
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + ACh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.45 reg_ISH2HOST_MSG21_type (ISH2HOST_MSG21)—Offset B0h

Message from ISH to HOST

Access Method

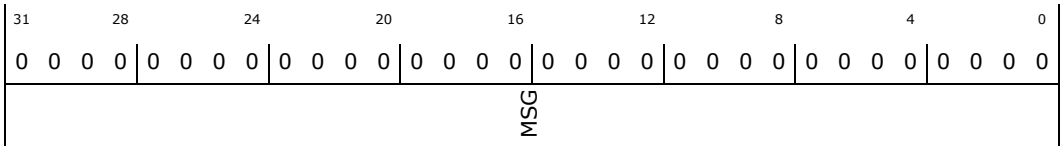
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + B0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.46 reg_ISH2HOST_MSG22_type (ISH2HOST_MSG22)—Offset B4h

Message from ISH to HOST

Access Method

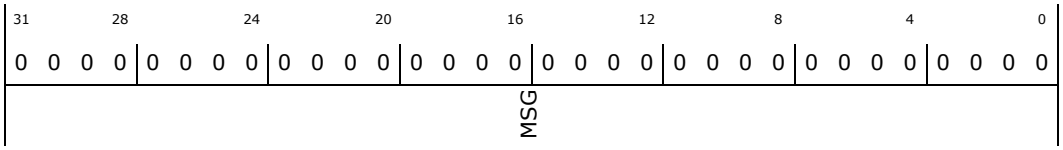
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + B4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.47 reg_ISH2HOST_MSG23_type (ISH2HOST_MSG23)—Offset B8h

Message from ISH to HOST

Access Method

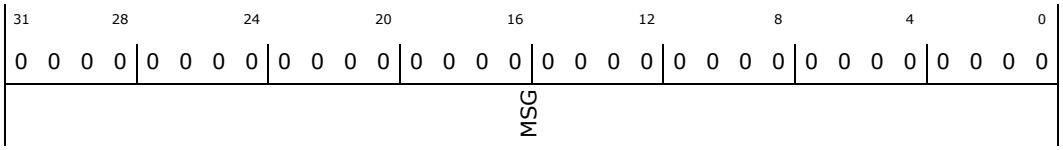
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + B8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.48 reg_ISH2HOST_MSG24_type (ISH2HOST_MSG24)—Offset BCh

Message from ISH to HOST

Access Method

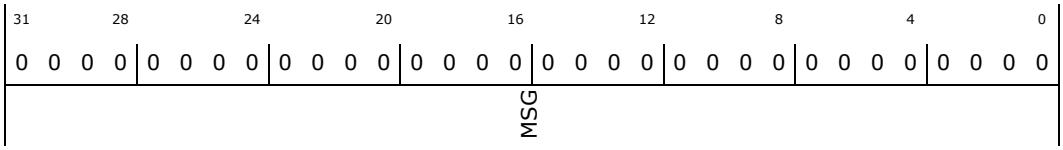
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + BCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.49 reg_ISH2HOST_MSG25_type (ISH2HOST_MSG25)—Offset C0h

Message from ISH to HOST

Access Method

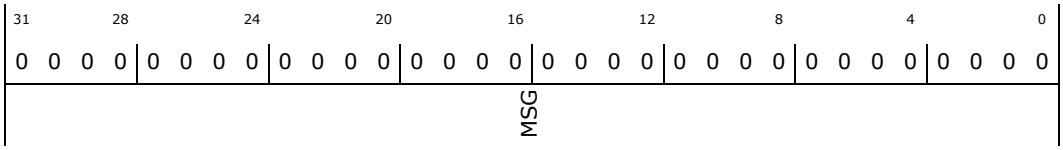
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + C0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.50 reg_ISH2HOST_MSG26_type (ISH2HOST_MSG26)—Offset C4h

Message from ISH to HOST

Access Method

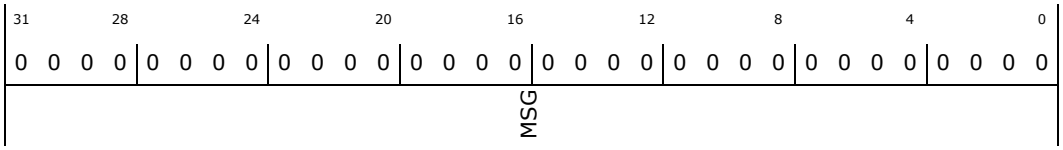
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + C4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.51 reg_ISH2HOST_MSG27_type (ISH2HOST_MSG27)—Offset C8h

Message from ISH to HOST

Access Method

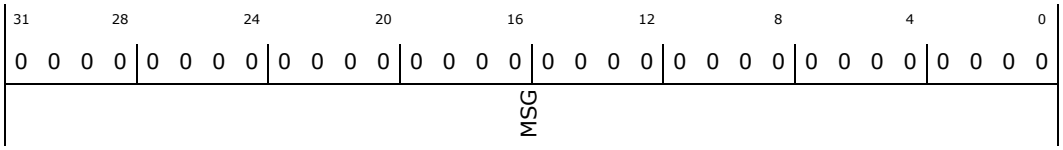
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + C8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.52 reg_ISH2HOST_MSG28_type (ISH2HOST_MSG28)—Offset CCh

Message from ISH to HOST

Access Method

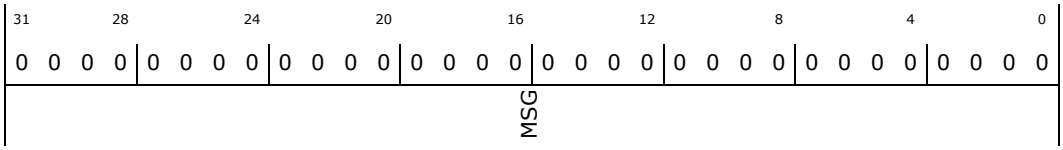
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + CCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.53 reg_ISH2HOST_MSG29_type (ISH2HOST_MSG29)—Offset D0h

Message from ISH to HOST

Access Method

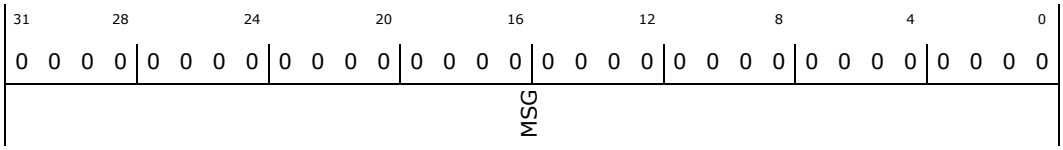
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + D0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.54 reg_ISH2HOST_MSG30_type (ISH2HOST_MSG30)—Offset D4h

Message from ISH to HOST

Access Method

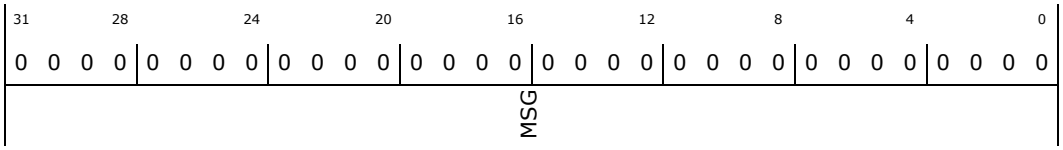
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + D4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.55 reg_ISH2HOST_MSG31_type (ISH2HOST_MSG31)—Offset D8h

Message from ISH to HOST

Access Method

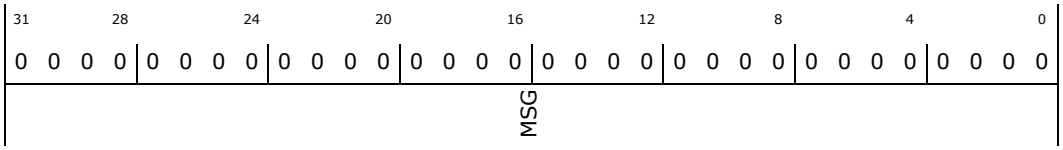
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + D8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.56 reg_ISH2HOST_MSG32_type (ISH2HOST_MSG32)—Offset DCh

Message from ISH to HOST

Access Method

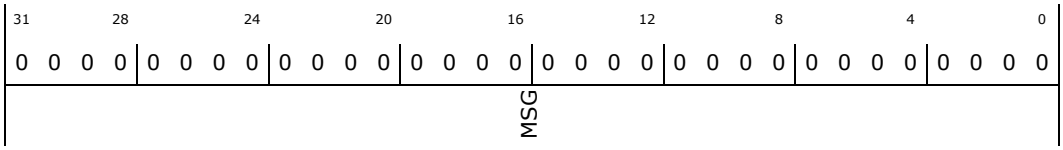
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + DCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.57 reg_HOST2ISH_MSG1_type (HOST2ISH_MSG1)—Offset E0h

Message from HOST to ISH

Access Method

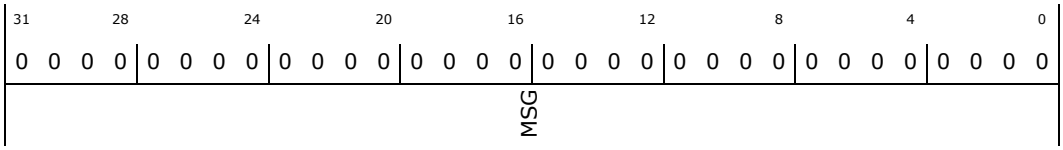
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + E0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.58 reg_HOST2ISH_MSG2_type (HOST2ISH_MSG2)—Offset E4h

Message from HOST to ISH

Access Method

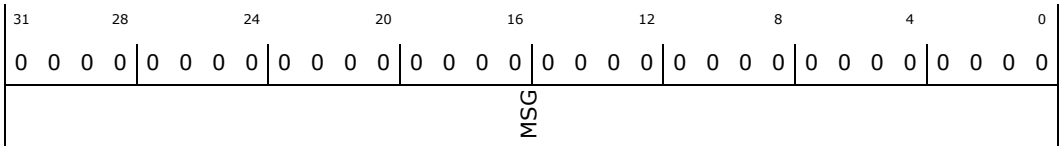
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + E4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.59 reg_HOST2ISH_MSG3_type (HOST2ISH_MSG3)—Offset E8h

Message from HOST to ISH

Access Method

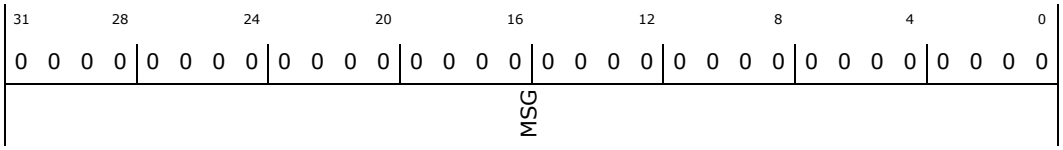
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + E8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.60 reg_HOST2ISH_MSG4_type (HOST2ISH_MSG4)—Offset ECh

Message from HOST to ISH

Access Method

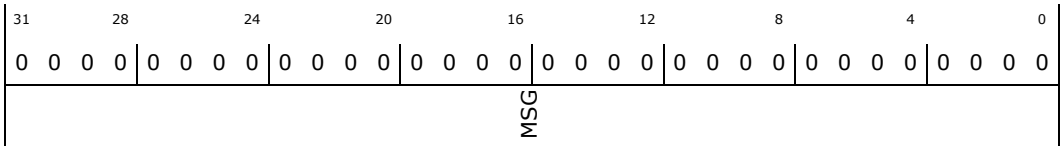
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + ECh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.61 reg_HOST2ISH_MSG5_type (HOST2ISH_MSG5)—Offset F0h

Message from HOST to ISH

Access Method

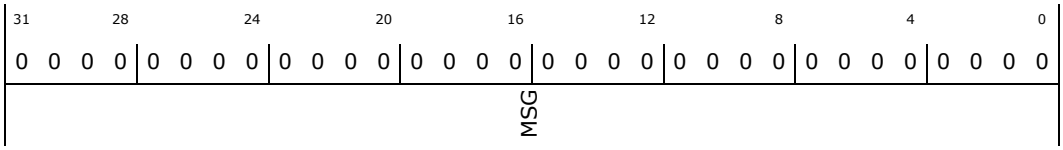
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + F0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.62 reg_HOST2ISH_MSG6_type (HOST2ISH_MSG6)—Offset F4h

Message from HOST to ISH

Access Method

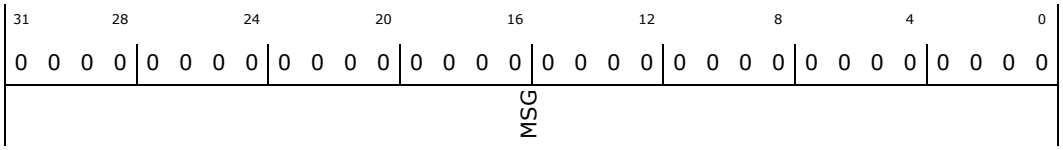
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + F4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.63 reg_HOST2ISH_MSG7_type (HOST2ISH_MSG7)—Offset F8h

Message from HOST to ISH

Access Method

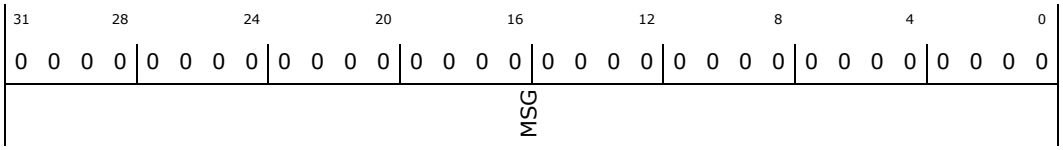
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + F8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.64 reg_HOST2ISH_MSG8_type (HOST2ISH_MSG8)—Offset FCh

Message from HOST to ISH

Access Method

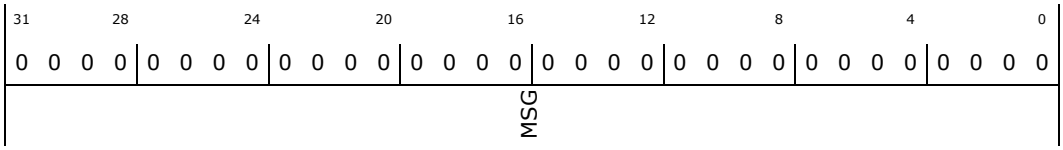
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + FCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.65 reg_HOST2ISH_MSG9_type (HOST2ISH_MSG9)—Offset 100h

Message from HOST to ISH

Access Method

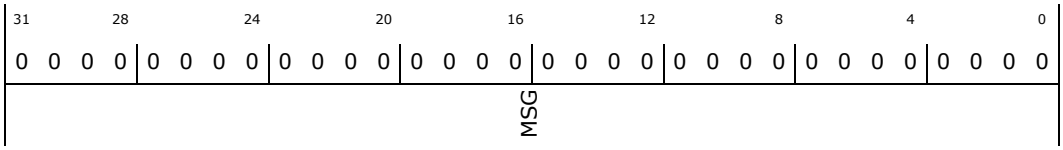
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 100h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.66 reg_HOST2ISH_MSG10_type (HOST2ISH_MSG10)—Offset 104h

Message from HOST to ISH

Access Method

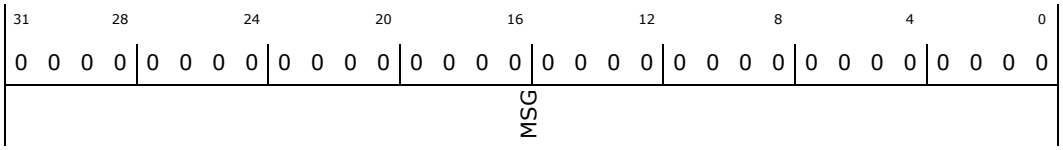
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 104h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.67 reg_HOST2ISH_MSG11_type (HOST2ISH_MSG11)—Offset 108h

Message from HOST to ISH

Access Method

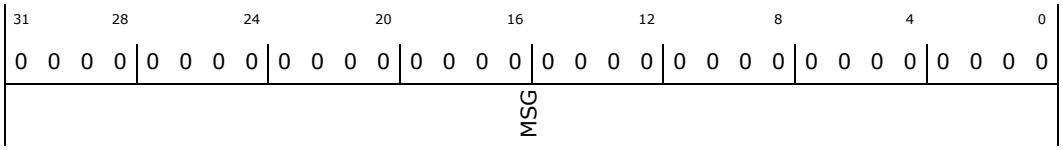
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 108h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.68 reg_HOST2ISH_MSG12_type (HOST2ISH_MSG12)—Offset 10Ch

Message from HOST to ISH

Access Method

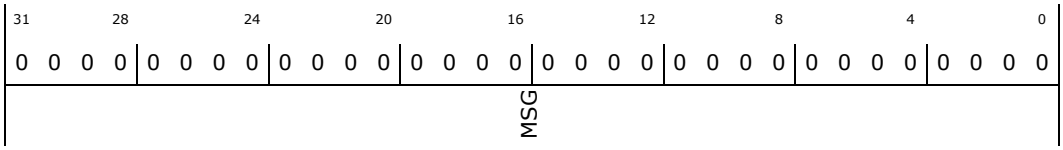
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.69 reg_HOST2ISH_MSG13_type (HOST2ISH_MSG13)—Offset 110h

Message from HOST to ISH

Access Method

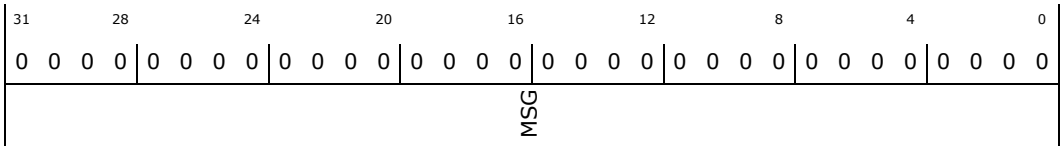
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 110h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.70 reg_HOST2ISH_MSG14_type (HOST2ISH_MSG14)—Offset 114h

Message from HOST to ISH

Access Method

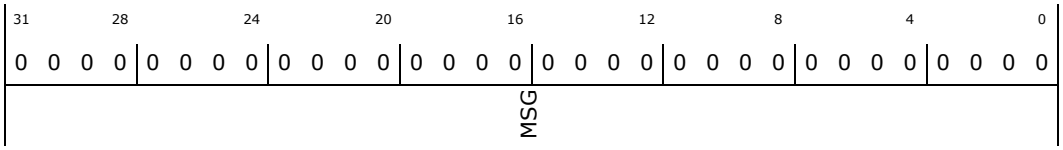
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 114h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.71 reg_HOST2ISH_MSG15_type (HOST2ISH_MSG15)—Offset 118h

Message from HOST to ISH

Access Method

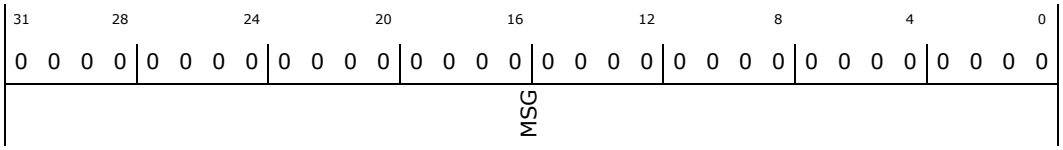
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 118h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.72 reg_HOST2ISH_MSG16_type (HOST2ISH_MSG16)—Offset 11Ch

Message from HOST to ISH

Access Method

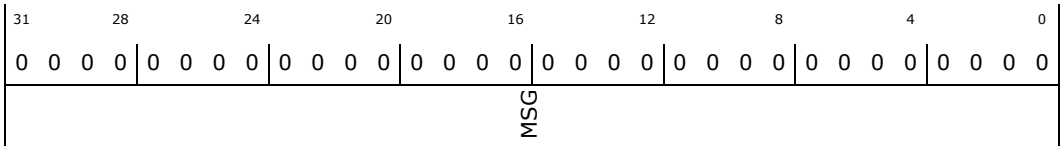
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.73 reg_HOST2ISH_MSG17_type (HOST2ISH_MSG17)—Offset 120h

Message from HOST to ISH

Access Method

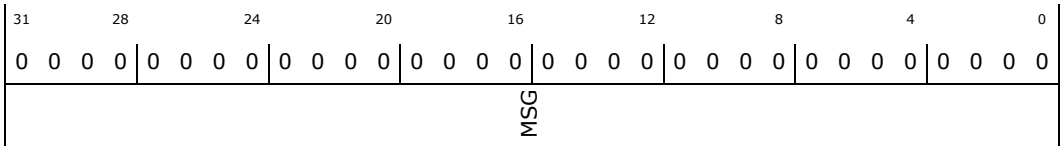
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 120h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.74 reg_HOST2ISH_MSG18_type (HOST2ISH_MSG18)—Offset 124h

Message from HOST to ISH

Access Method

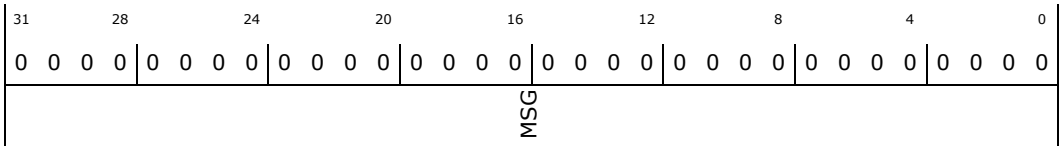
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 124h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.75 reg_HOST2ISH_MSG19_type (HOST2ISH_MSG19)—Offset 128h

Message from HOST to ISH

Access Method

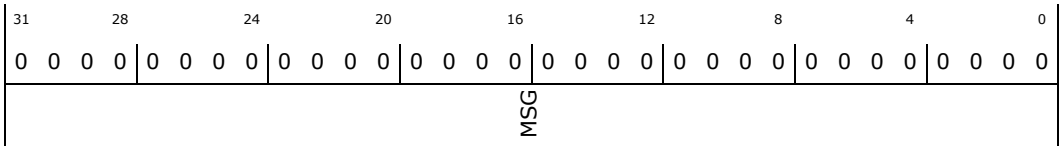
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 128h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.76 reg_HOST2ISH_MSG20_type (HOST2ISH_MSG20)—Offset 12Ch

Message from HOST to ISH

Access Method

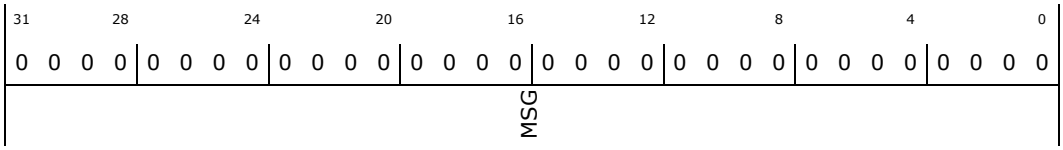
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.77 reg_HOST2ISH_MSG21_type (HOST2ISH_MSG21)—Offset 130h

Message from HOST to ISH

Access Method

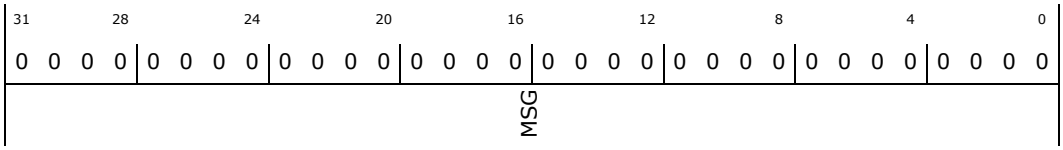
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 130h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.78 reg_HOST2ISH_MSG22_type (HOST2ISH_MSG22)—Offset 134h

Message from HOST to ISH

Access Method

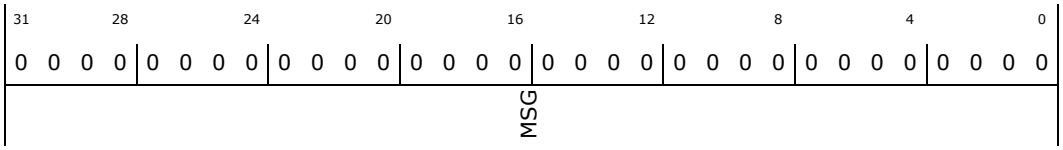
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 134h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.79 reg_HOST2ISH_MSG23_type (HOST2ISH_MSG23)—Offset 138h

Message from HOST to ISH

Access Method

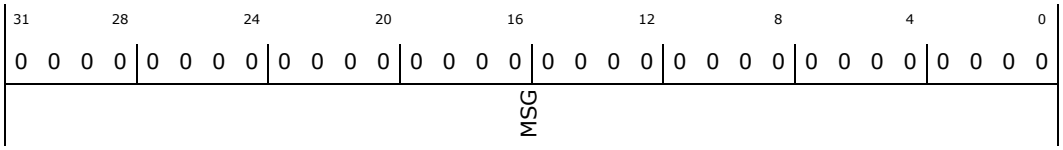
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 138h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.80 reg_HOST2ISH_MSG24_type (HOST2ISH_MSG24)—Offset 13Ch

Message from HOST to ISH

Access Method

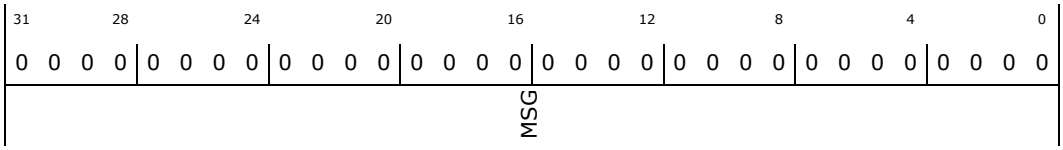
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 13Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.81 reg_HOST2ISH_MSG25_type (HOST2ISH_MSG25)—Offset 140h

Message from HOST to ISH

Access Method

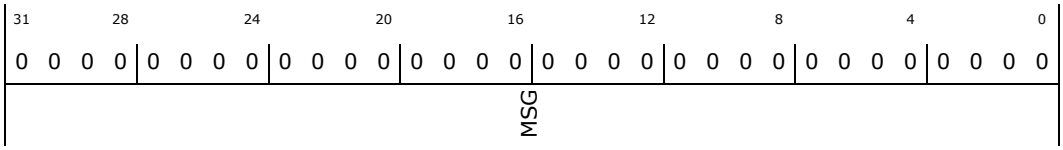
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 140h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.82 reg_HOST2ISH_MSG26_type (HOST2ISH_MSG26)—Offset 144h

Message from HOST to ISH

Access Method

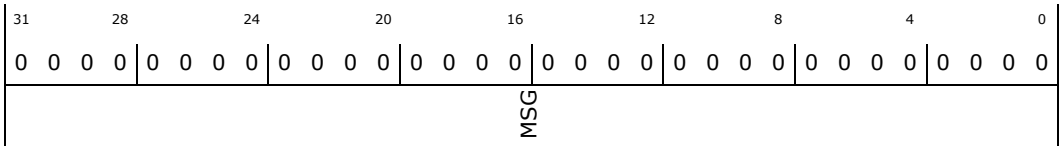
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 144h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.83 reg_HOST2ISH_MSG27_type (HOST2ISH_MSG27)—Offset 148h

Message from HOST to ISH

Access Method

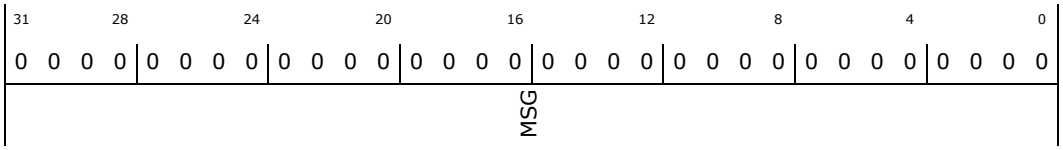
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 148h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.84 reg_HOST2ISH_MSG28_type (HOST2ISH_MSG28)—Offset 14Ch

Message from HOST to ISH

Access Method

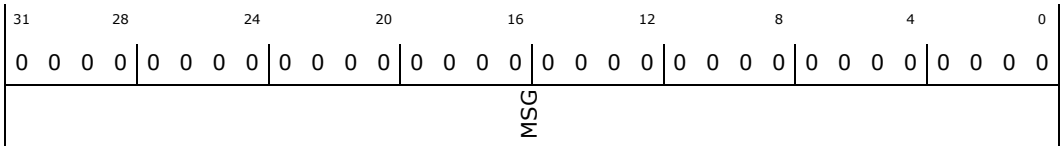
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 14Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.85 reg_HOST2ISH_MSG29_type (HOST2ISH_MSG29)—Offset 150h

Message from HOST to ISH

Access Method

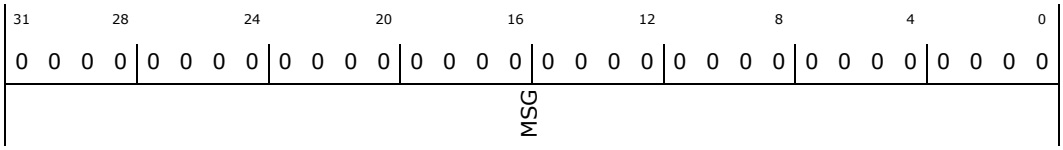
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 150h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.86 reg_HOST2ISH_MSG30_type (HOST2ISH_MSG30)—Offset 154h

Message from HOST to ISH

Access Method

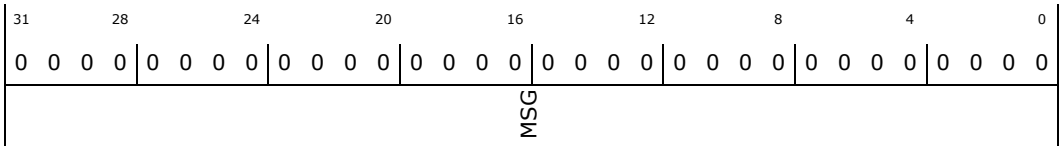
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 154h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.87 reg_HOST2ISH_MSG31_type (HOST2ISH_MSG31)—Offset 158h

Message from HOST to ISH

Access Method

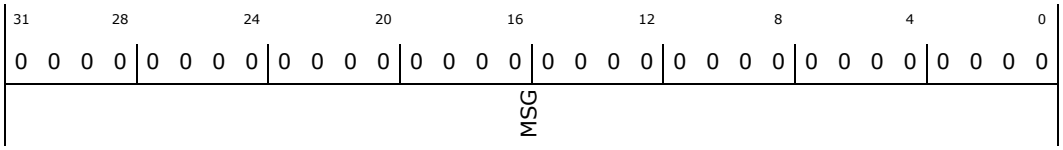
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 158h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.88 reg_HOST2ISH_MSG32_type (HOST2ISH_MSG32)—Offset 15Ch

Message from HOST to ISH

Access Method

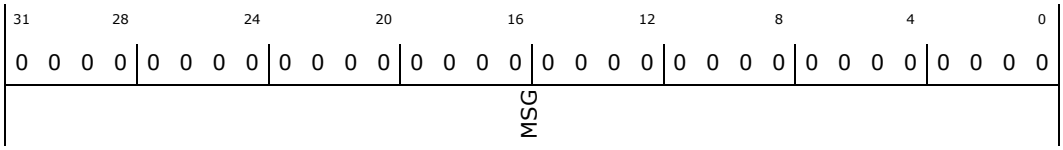
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 15Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.89 reg_ISH2SEC_MSG1_type (ISH2SEC_MSG1)—Offset 160h

Message from ISH to SEC

Access Method

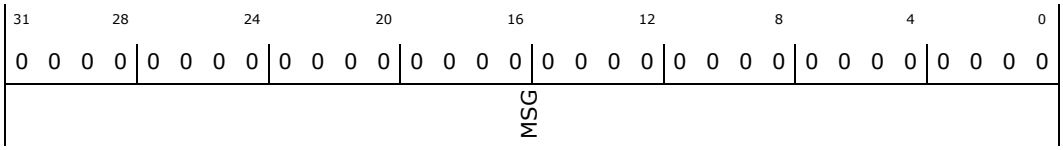
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 160h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.90 reg_ISH2SEC_MSG2_type (ISH2SEC_MSG2)—Offset 164h

Message from ISH to SEC

Access Method

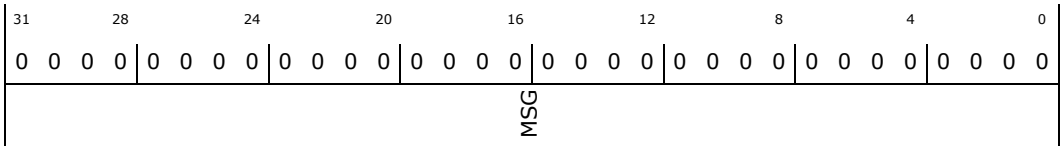
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 164h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.91 reg_ISH2SEC_MSG3_type (ISH2SEC_MSG3)—Offset 168h

Message from ISH to SEC

Access Method

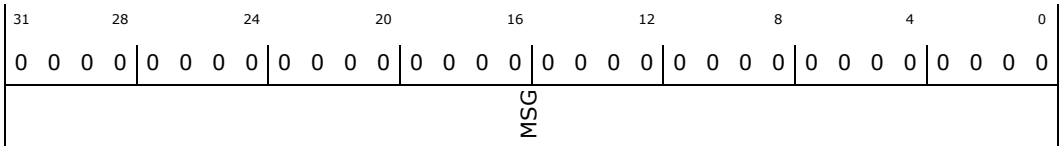
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 168h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.92 reg_ISH2SEC_MSG4_type (ISH2SEC_MSG4)—Offset 16Ch

Message from ISH to SEC

Access Method

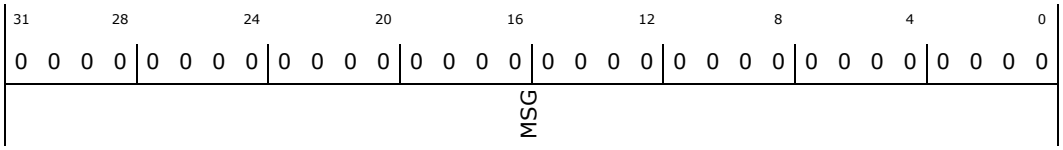
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 16Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.93 reg_ISH2SEC_MSG5_type (ISH2SEC_MSG5)—Offset 170h

Message from ISH to SEC

Access Method

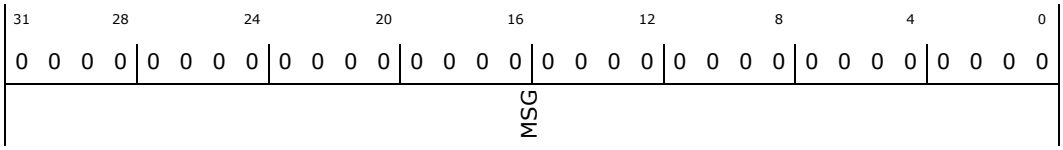
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 170h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.94 reg_ISH2SEC_MSG6_type (ISH2SEC_MSG6)—Offset 174h

Message from ISH to SEC

Access Method

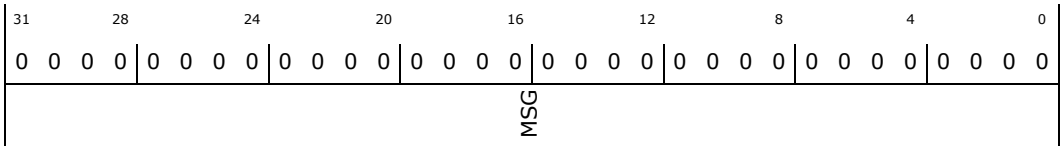
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 174h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.95 reg_ISH2SEC_MSG7_type (ISH2SEC_MSG7)—Offset 178h

Message from ISH to SEC

Access Method

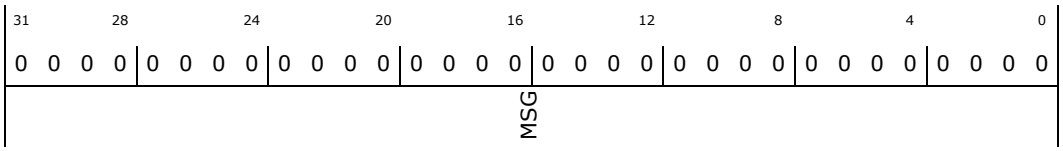
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 178h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.96 reg_ISH2SEC_MSG8_type (ISH2SEC_MSG8)—Offset 17Ch

Message from ISH to SEC

Access Method

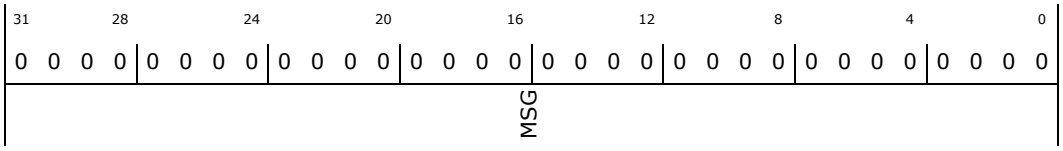
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 17Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.97 reg_ISH2SEC_MSG9_type (ISH2SEC_MSG9)—Offset 180h

Message from ISH to SEC

Access Method

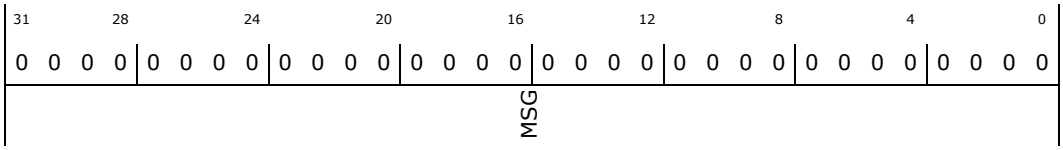
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 180h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.98 reg_ISH2SEC_MSG10_type (ISH2SEC_MSG10)—Offset 184h

Message from ISH to SEC

Access Method

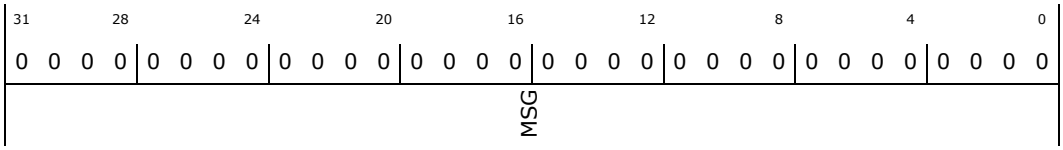
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 184h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.99 reg_ISH2SEC_MSG11_type (ISH2SEC_MSG11)—Offset 188h

Message from ISH to SEC

Access Method

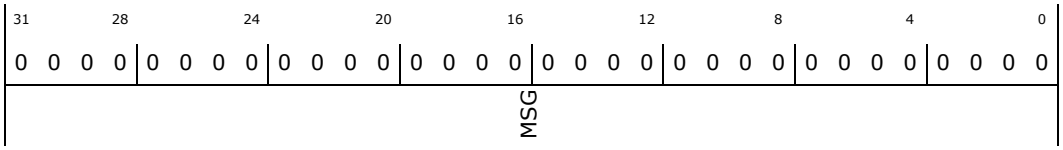
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 188h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.100 reg_ISH2SEC_MSG12_type (ISH2SEC_MSG12)—Offset 18Ch

Message from ISH to SEC

Access Method

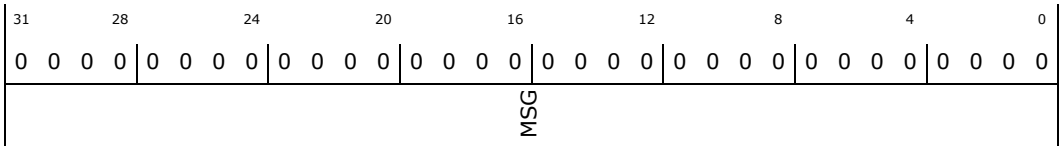
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 18Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.101 reg_ISH2SEC_MSG13_type (ISH2SEC_MSG13)—Offset 190h

Message from ISH to SEC

Access Method

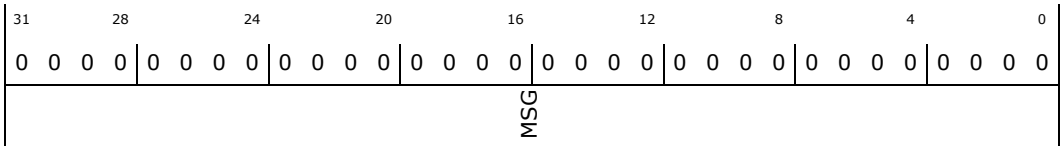
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 190h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.102 reg_ISH2SEC_MSG14_type (ISH2SEC_MSG14)—Offset 194h

Message from ISH to SEC

Access Method

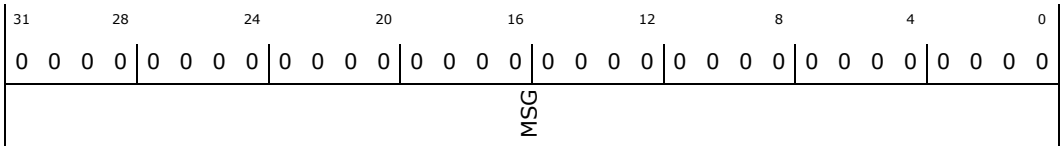
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 194h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.103 reg_ISH2SEC_MSG15_type (ISH2SEC_MSG15)—Offset 198h

Message from ISH to SEC

Access Method

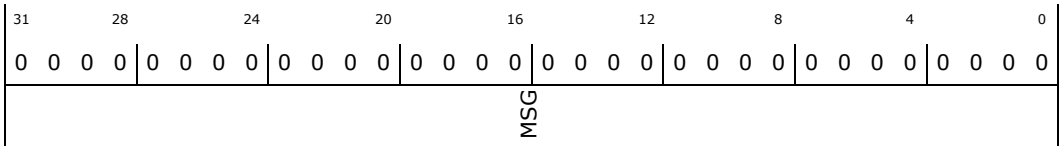
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 198h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.104 reg_ISH2SEC_MSG16_type (ISH2SEC_MSG16)—Offset 19Ch

Message from ISH to SEC

Access Method

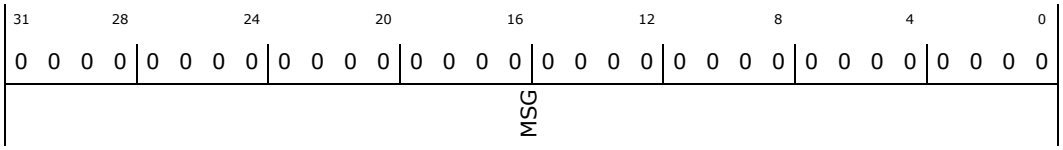
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 19Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.105 reg_ISH2SEC_MSG17_type (ISH2SEC_MSG17)—Offset 1A0h

Message from ISH to SEC

Access Method

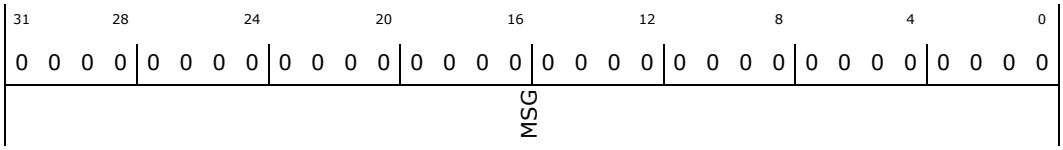
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1A0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.106 reg_ISH2SEC_MSG18_type (ISH2SEC_MSG18)—Offset 1A4h

Message from ISH to SEC

Access Method

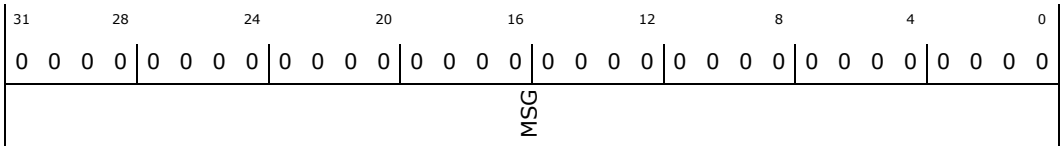
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1A4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.107 reg_ISH2SEC_MSG19_type (ISH2SEC_MSG19)—Offset 1A8h

Message from ISH to SEC

Access Method

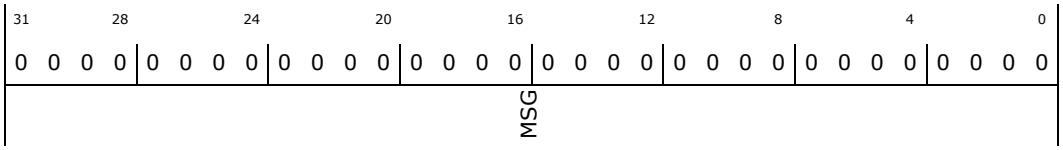
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1A8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.108 reg_ISH2SEC_MSG20_type (ISH2SEC_MSG20)—Offset 1ACh

Message from ISH to SEC

Access Method

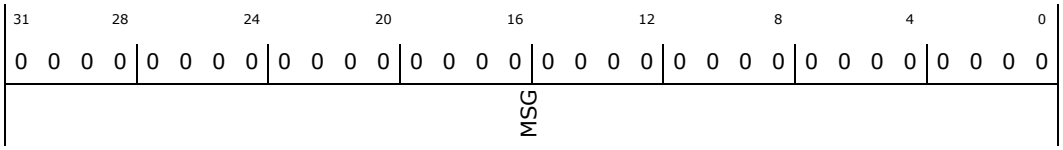
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1ACh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.109 reg_ISH2SEC_MSG21_type (ISH2SEC_MSG21)—Offset 1B0h

Message from ISH to SEC

Access Method

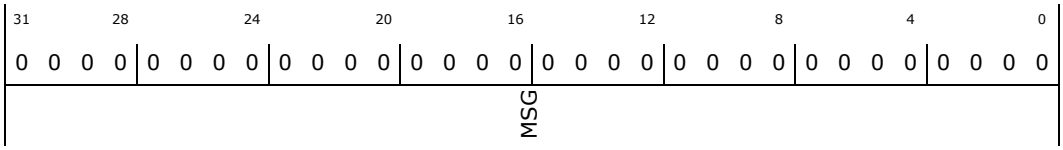
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1B0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.110 reg_ISH2SEC_MSG22_type (ISH2SEC_MSG22)—Offset 1B4h

Message from ISH to SEC

Access Method

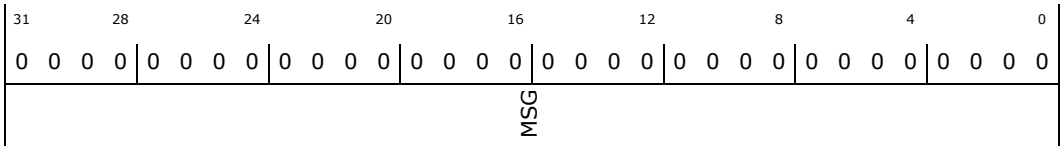
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1B4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.111 reg_ISH2SEC_MSG23_type (ISH2SEC_MSG23)—Offset 1B8h

Message from ISH to SEC

Access Method

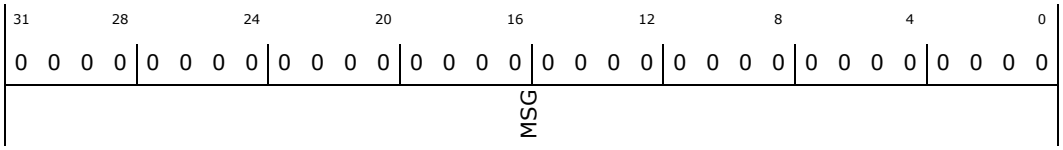
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1B8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.112 reg_ISH2SEC_MSG24_type (ISH2SEC_MSG24)—Offset 1BCh

Message from ISH to SEC

Access Method

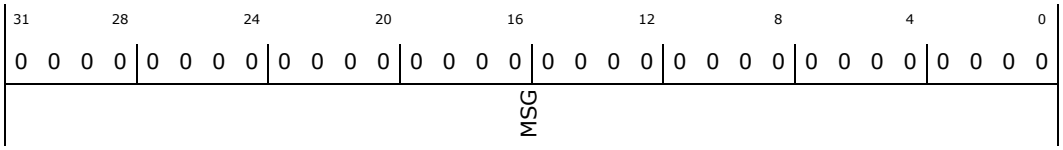
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1BCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.113 reg_ISH2SEC_MSG25_type (ISH2SEC_MSG25)—Offset 1C0h

Message from ISH to SEC

Access Method

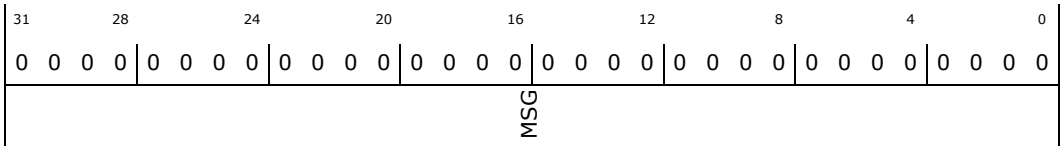
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1C0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.114 reg_ISH2SEC_MSG26_type (ISH2SEC_MSG26)—Offset 1C4h

Message from ISH to SEC

Access Method

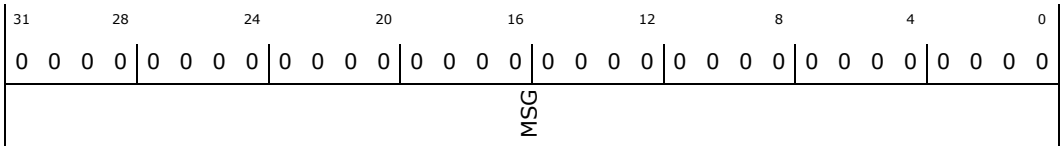
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1C4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.115 reg_ISH2SEC_MSG27_type (ISH2SEC_MSG27)—Offset 1C8h

Message from ISH to SEC

Access Method

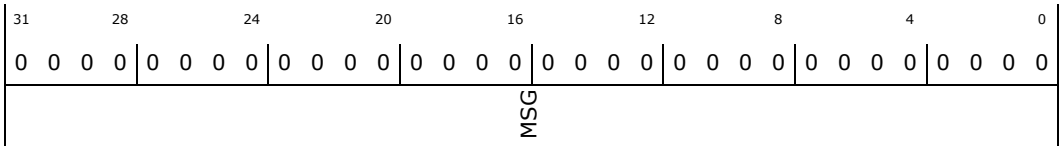
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1C8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.116 reg_ISH2SEC_MSG28_type (ISH2SEC_MSG28)—Offset 1CCh

Message from ISH to SEC

Access Method

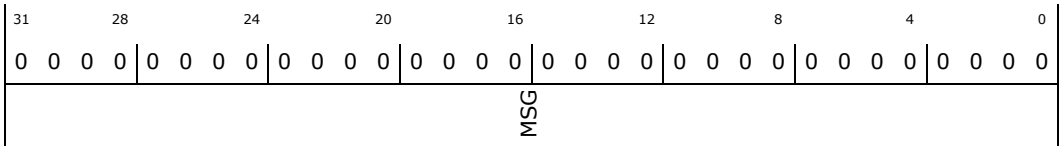
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1CCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.117 reg_ISH2SEC_MSG29_type (ISH2SEC_MSG29)—Offset 1D0h

Message from ISH to SEC

Access Method

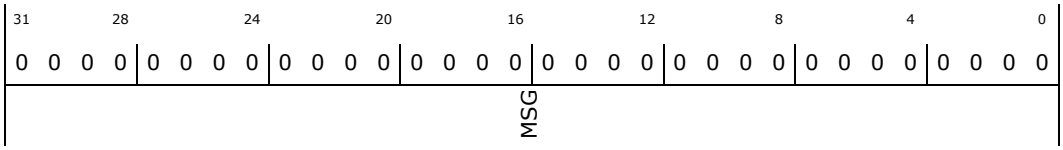
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1D0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.118 reg_ISH2SEC_MSG30_type (ISH2SEC_MSG30)—Offset 1D4h

Message from ISH to SEC

Access Method

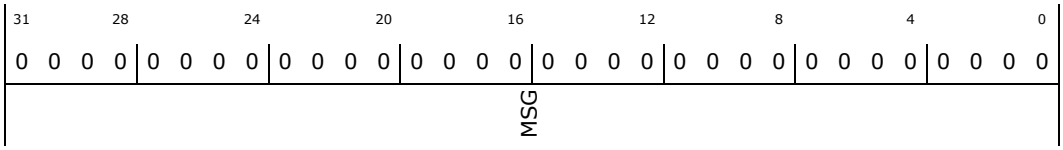
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1D4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.119 reg_ISH2SEC_MSG31_type (ISH2SEC_MSG31)—Offset 1D8h

Message from ISH to SEC

Access Method

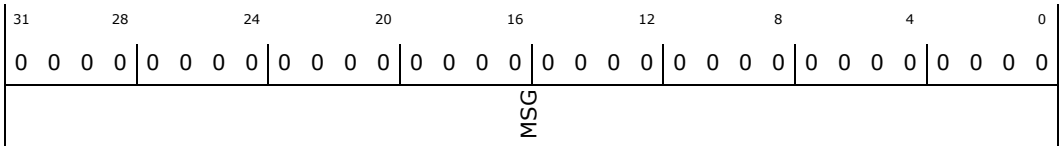
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1D8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.120 reg_ISH2SEC_MSG32_type (ISH2SEC_MSG32)—Offset 1DCh

Message from ISH to SEC

Access Method

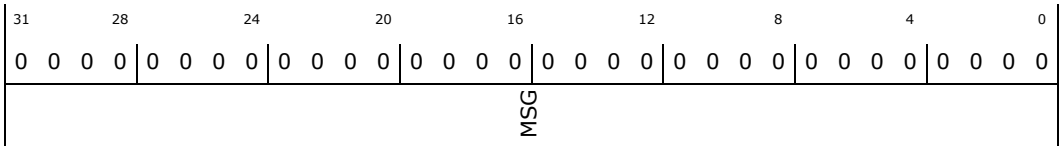
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1DCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.121 reg_SEC2ISH_MSG1_type (SEC2ISH_MSG1)—Offset 1E0h

Message from SEC to ISH

Access Method

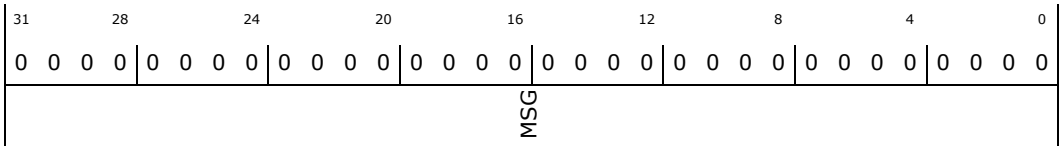
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1E0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.122 reg_SEC2ISH_MSG2_type (SEC2ISH_MSG2)—Offset 1E4h

Message from SEC to ISH

Access Method

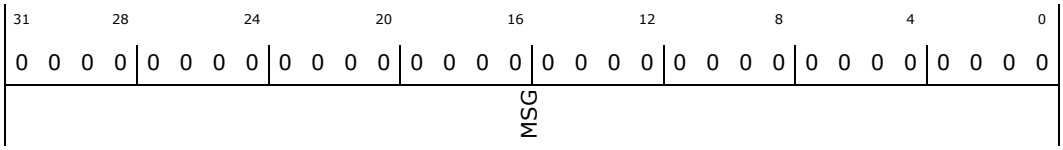
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1E4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.123 reg_SEC2ISH_MSG3_type (SEC2ISH_MSG3)—Offset 1E8h

Message from SEC to ISH

Access Method

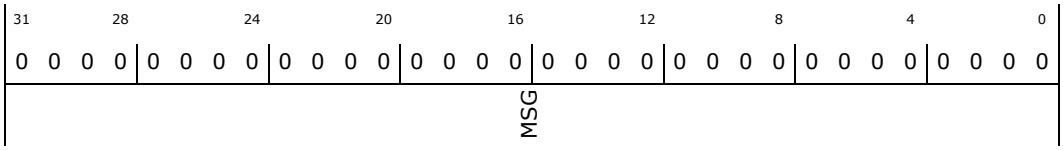
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1E8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.124 reg_SEC2ISH_MSG4_type (SEC2ISH_MSG4)—Offset 1ECh

Message from SEC to ISH

Access Method

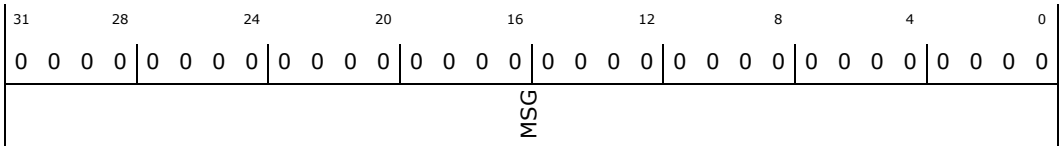
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1ECh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.125 reg_SEC2ISH_MSG5_type (SEC2ISH_MSG5)—Offset 1F0h

Message from SEC to ISH

Access Method

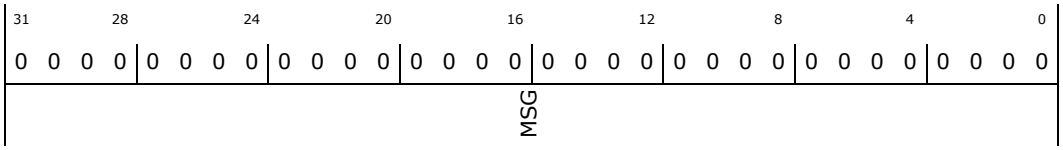
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1F0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.126 reg_SEC2ISH_MSG6_type (SEC2ISH_MSG6)—Offset 1F4h

Message from SEC to ISH

Access Method

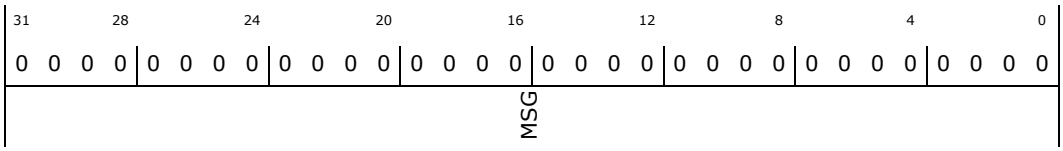
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1F4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.127 reg_SEC2ISH_MSG7_type (SEC2ISH_MSG7)—Offset 1F8h

Message from SEC to ISH

Access Method

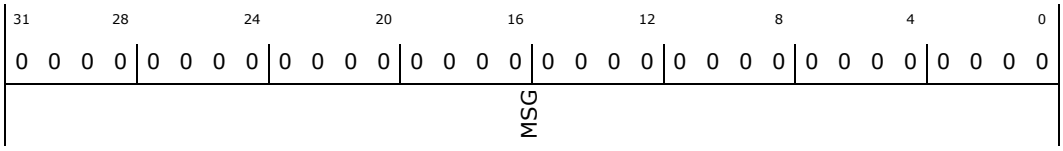
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1F8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.128 reg_SEC2ISH_MSG8_type (SEC2ISH_MSG8)—Offset 1FCh

Message from SEC to ISH

Access Method

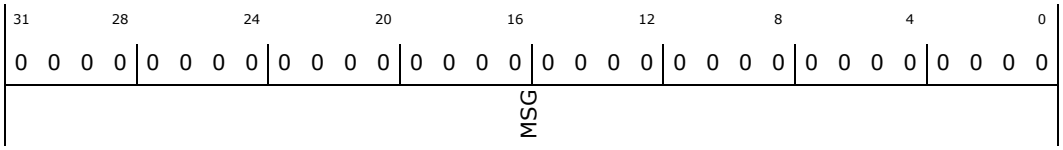
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1FCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.129 reg_SEC2ISH_MSG9_type (SEC2ISH_MSG9)—Offset 200h

Message from SEC to ISH

Access Method

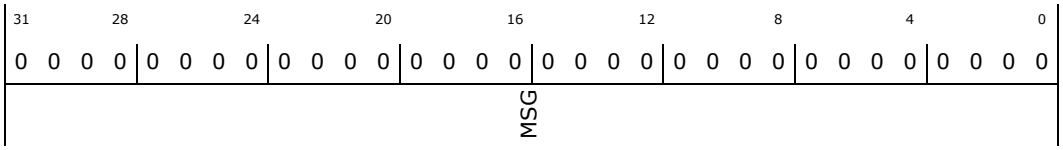
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 200h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.130 reg_SEC2ISH_MSG10_type (SEC2ISH_MSG10)—Offset 204h

Message from SEC to ISH

Access Method

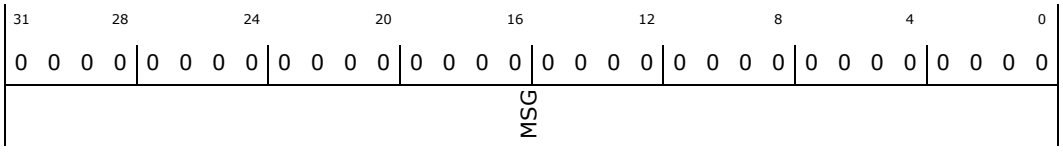
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 204h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.131 reg_SEC2ISH_MSG11_type (SEC2ISH_MSG11)—Offset 208h

Message from SEC to ISH

Access Method

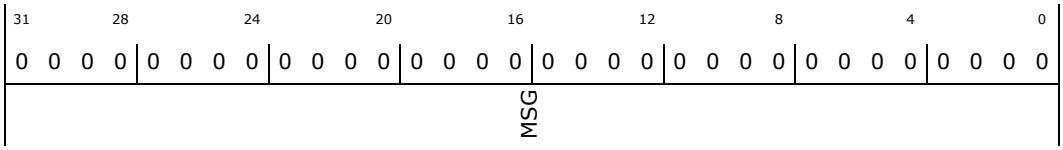
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 208h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.132 reg_SEC2ISH_MSG12_type (SEC2ISH_MSG12)—Offset 20Ch

Message from SEC to ISH

Access Method

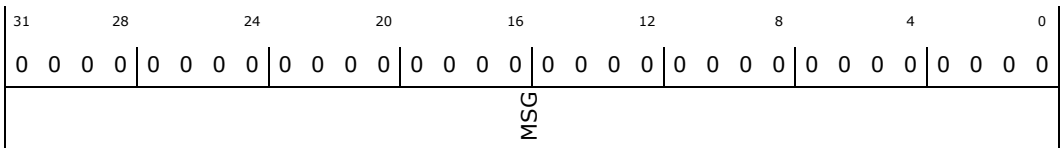
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 20Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.133 reg_SEC2ISH_MSG13_type (SEC2ISH_MSG13)—Offset 210h

Message from SEC to ISH

Access Method

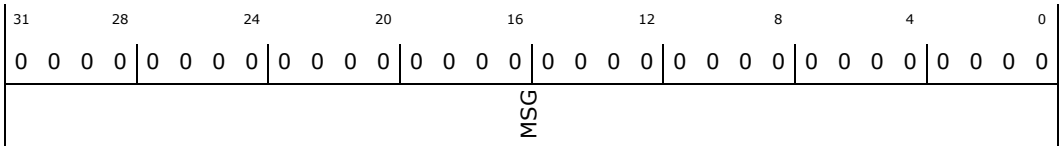
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 210h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.134 reg_SEC2ISH_MSG14_type (SEC2ISH_MSG14)—Offset 214h

Message from SEC to ISH

Access Method

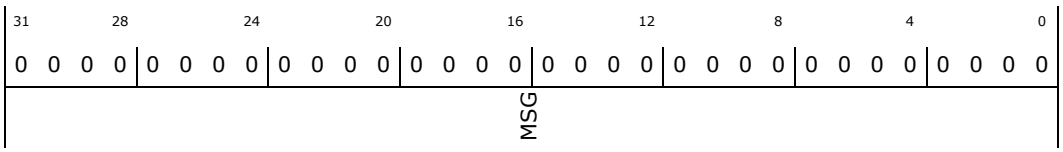
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 214h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.135 reg_SEC2ISH_MSG15_type (SEC2ISH_MSG15)—Offset 218h

Message from SEC to ISH

Access Method

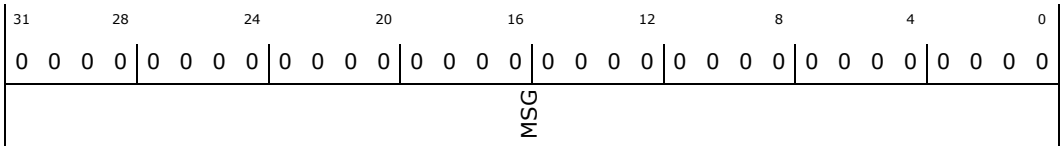
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 218h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.136 reg_SEC2ISH_MSG16_type (SEC2ISH_MSG16)—Offset 21Ch

Message from SEC to ISH

Access Method

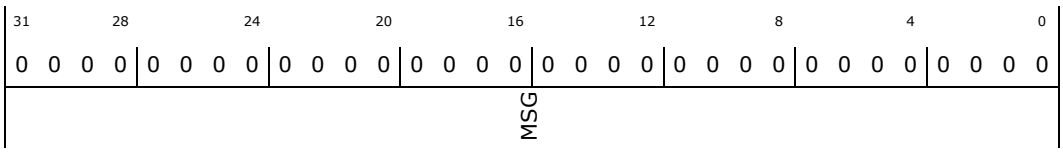
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 21Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.137 reg_SEC2ISH_MSG17_type (SEC2ISH_MSG17)—Offset 220h

Message from SEC to ISH

Access Method

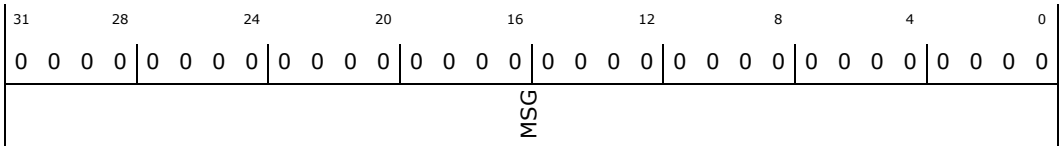
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 220h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.138 reg_SEC2ISH_MSG18_type (SEC2ISH_MSG18)—Offset 224h

Message from SEC to ISH

Access Method

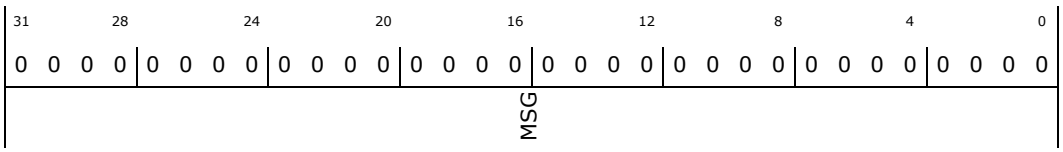
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 224h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.139 reg_SEC2ISH_MSG19_type (SEC2ISH_MSG19)—Offset 228h

Message from SEC to ISH

Access Method

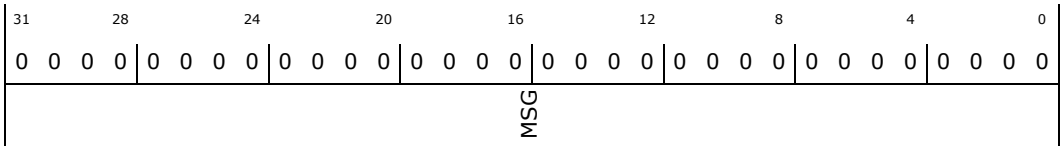
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 228h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.140 reg_SEC2ISH_MSG20_type (SEC2ISH_MSG20)—Offset 22Ch

Message from SEC to ISH

Access Method

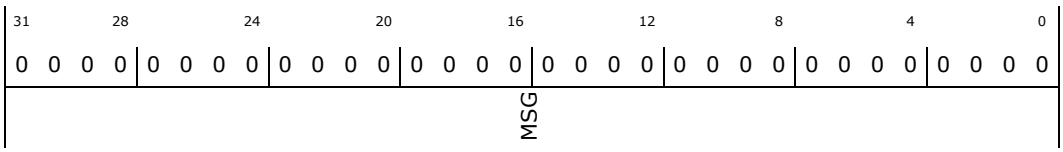
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 22Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.141 reg_SEC2ISH_MSG21_type (SEC2ISH_MSG21)—Offset 230h

Message from SEC to ISH

Access Method

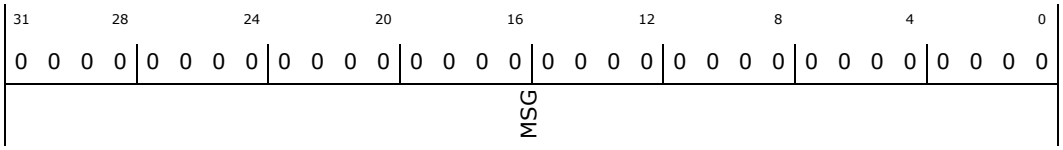
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 230h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.142 reg_SEC2ISH_MSG22_type (SEC2ISH_MSG22)—Offset 234h

Message from SEC to ISH

Access Method

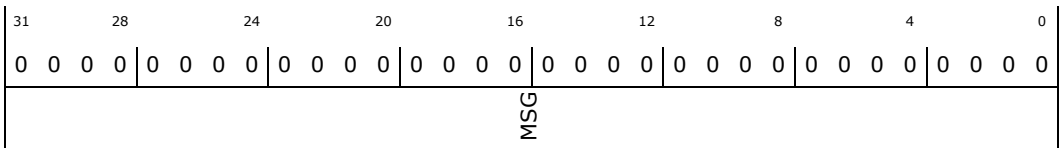
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 234h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.143 reg_SEC2ISH_MSG23_type (SEC2ISH_MSG23)—Offset 238h

Message from SEC to ISH

Access Method

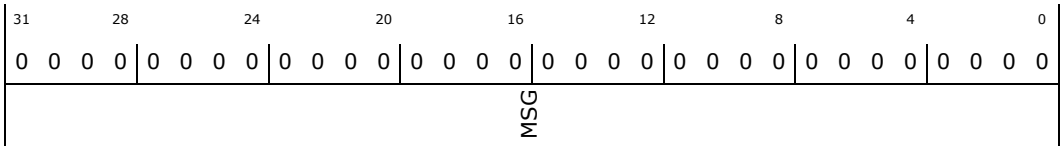
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 238h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.144 reg_SEC2ISH_MSG24_type (SEC2ISH_MSG24)—Offset 23Ch

Message from SEC to ISH

Access Method

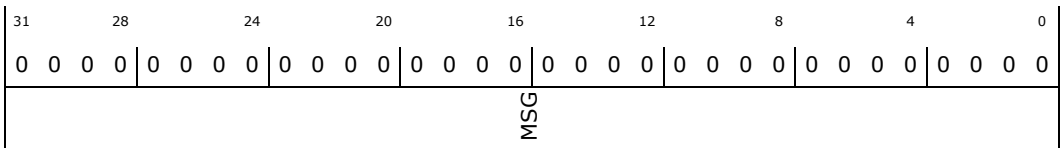
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 23Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.145 reg_SEC2ISH_MSG25_type (SEC2ISH_MSG25)—Offset 240h

Message from SEC to ISH

Access Method

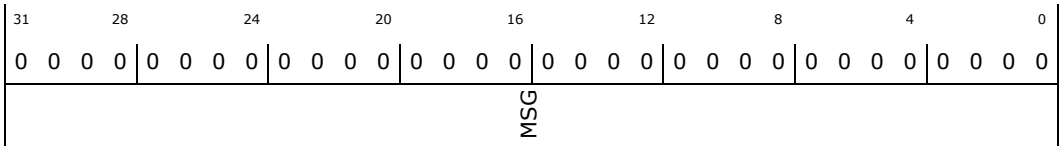
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 240h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.146 reg_SEC2ISH_MSG26_type (SEC2ISH_MSG26)—Offset 244h

Message from SEC to ISH

Access Method

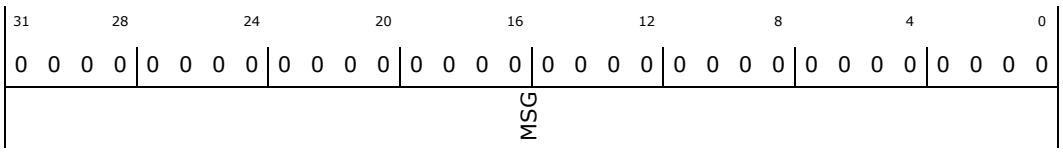
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 244h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.147 reg_SEC2ISH_MSG27_type (SEC2ISH_MSG27)—Offset 248h

Message from SEC to ISH

Access Method

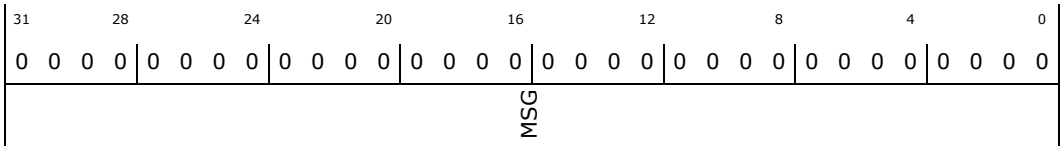
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 248h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.148 reg_SEC2ISH_MSG28_type (SEC2ISH_MSG28)—Offset 24Ch

Message from SEC to ISH

Access Method

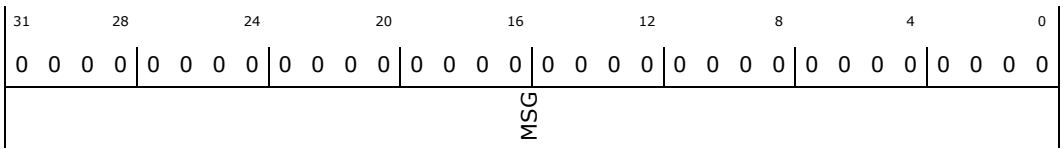
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 24Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.149 reg_SEC2ISH_MSG29_type (SEC2ISH_MSG29)—Offset 250h

Message from SEC to ISH

Access Method

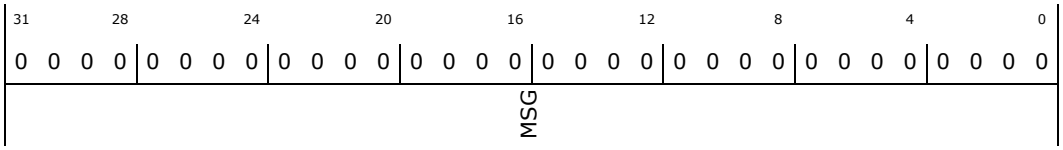
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 250h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.150 reg_SEC2ISH_MSG30_type (SEC2ISH_MSG30)—Offset 254h

Message from SEC to ISH

Access Method

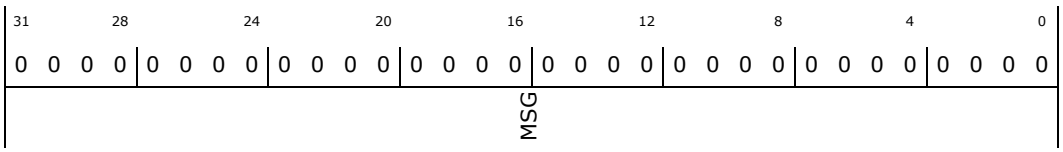
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 254h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.151 reg_SEC2ISH_MSG31_type (SEC2ISH_MSG31)—Offset 258h

Message from SEC to ISH

Access Method

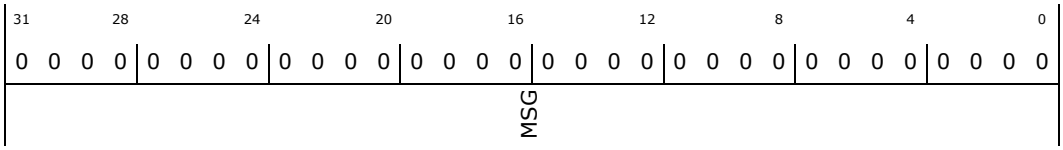
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 258h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.152 reg_SEC2ISH_MSG32_type (SEC2ISH_MSG32)—Offset 25Ch

Message from SEC to ISH

Access Method

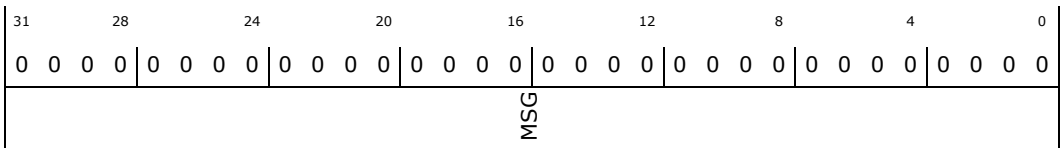
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 25Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.153 reg_ISH2PMC_MSG1_type (ISH2PMC_MSG1)—Offset 260h

Message from ISH to PMC

Access Method

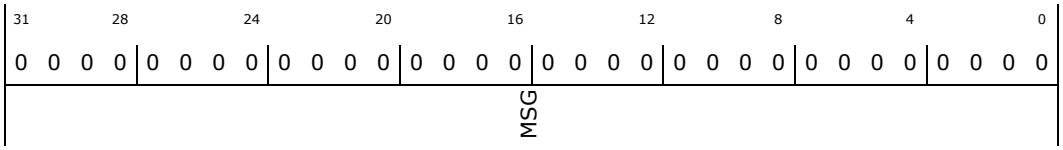
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 260h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.154 reg_ISH2PMC_MSG2_type (ISH2PMC_MSG2)—Offset 264h

Message from ISH to PMC

Access Method

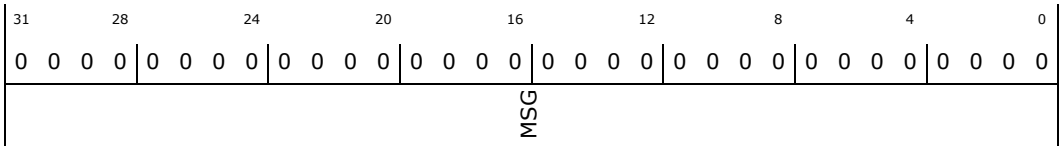
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 264h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.155 reg_ISH2PMC_MSG3_type (ISH2PMC_MSG3)—Offset 268h

Message from ISH to PMC

Access Method

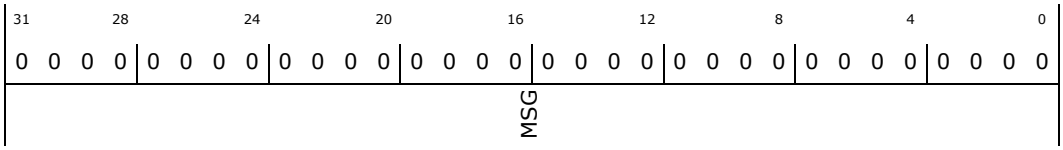
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 268h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.156 reg_ISH2PMC_MSG4_type (ISH2PMC_MSG4)—Offset 26Ch

Message from ISH to PMC

Access Method

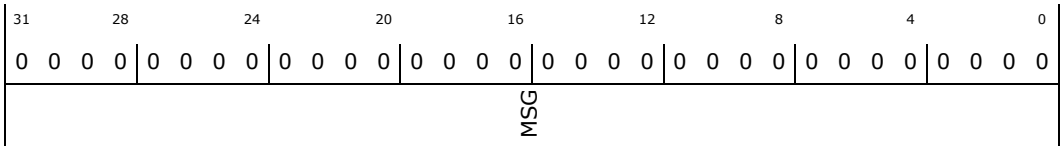
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 26Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.157 reg_ISH2PMC_MSG5_type (ISH2PMC_MSG5)—Offset 270h

Message from ISH to PMC

Access Method

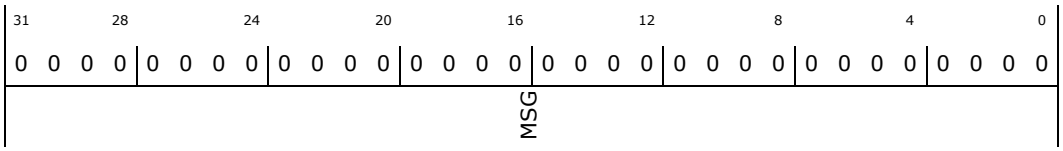
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 270h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.158 reg_ISH2PMC_MSG6_type (ISH2PMC_MSG6)—Offset 274h

Message from ISH to PMC

Access Method

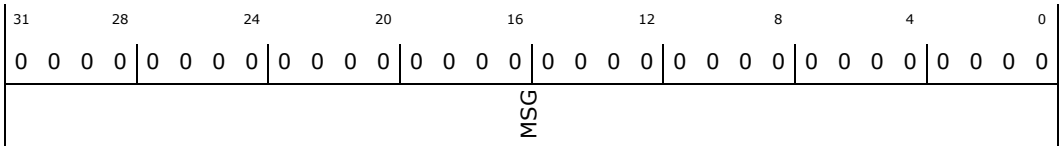
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 274h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.159 reg_ISH2PMC_MSG7_type (ISH2PMC_MSG7)—Offset 278h

Message from ISH to PMC

Access Method

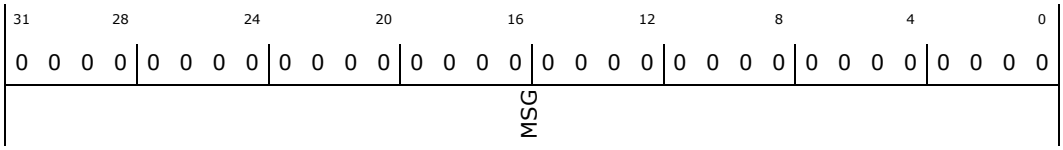
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 278h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.160 reg_ISH2PMC_MSG8_type (ISH2PMC_MSG8)—Offset 27Ch

Message from ISH to PMC

Access Method

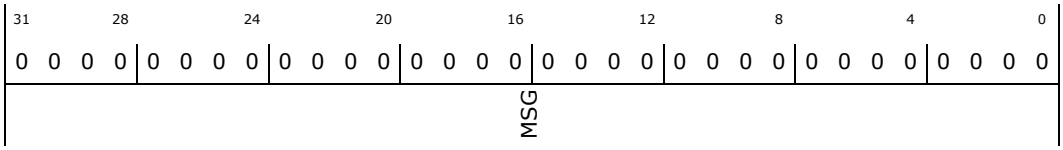
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 27Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.161 reg_ISH2PMC_MSG9_type (ISH2PMC_MSG9)—Offset 280h

Message from ISH to PMC

Access Method

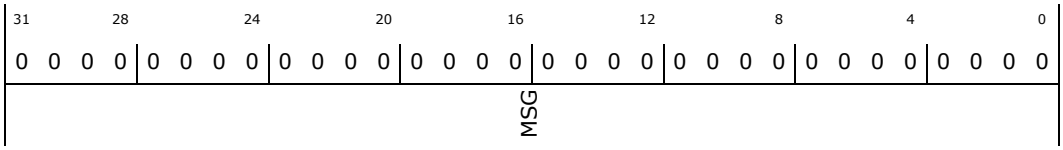
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 280h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.162 reg_ISH2PMC_MSG10_type (ISH2PMC_MSG10)—Offset 284h

Message from ISH to PMC

Access Method

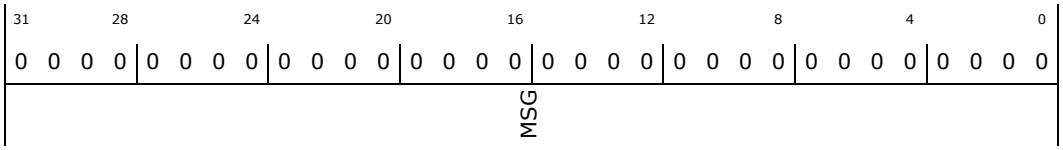
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 284h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.163 reg_ISH2PMC_MSG11_type (ISH2PMC_MSG11)—Offset 288h

Message from ISH to PMC

Access Method

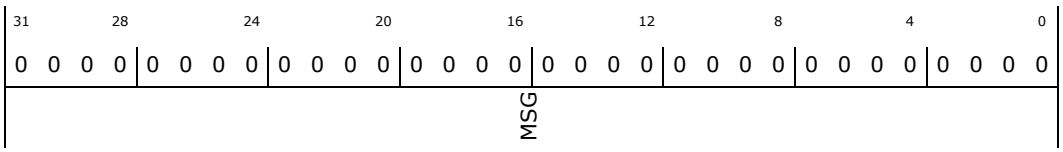
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 288h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.164 reg_ISH2PMC_MSG12_type (ISH2PMC_MSG12)—Offset 28Ch

Message from ISH to PMC

Access Method

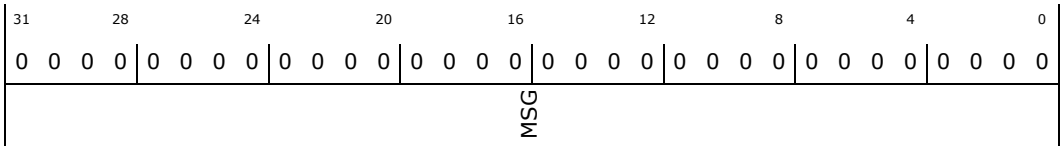
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 28Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.165 reg_ISH2PMC_MSG13_type (ISH2PMC_MSG13)—Offset 290h

Message from ISH to PMC

Access Method

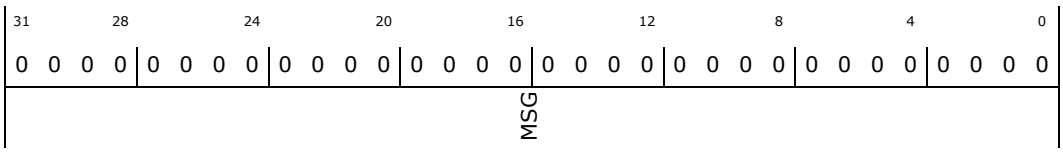
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 290h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.166 reg_ISH2PMC_MSG14_type (ISH2PMC_MSG14)—Offset 294h

Message from ISH to PMC

Access Method

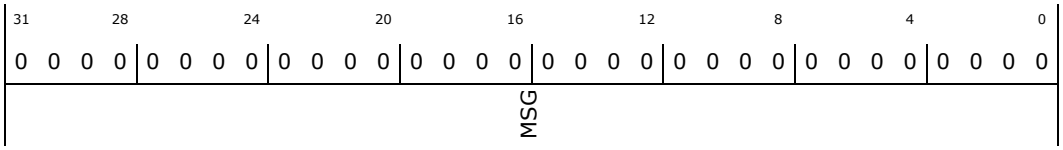
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 294h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.167 reg_ISH2PMC_MSG15_type (ISH2PMC_MSG15)—Offset 298h

Message from ISH to PMC

Access Method

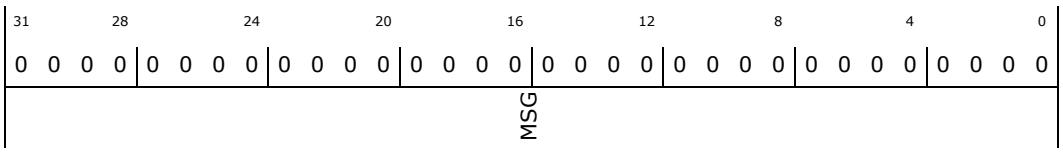
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 298h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.168 reg_ISH2PMC_MSG16_type (ISH2PMC_MSG16)—Offset 29Ch

Message from ISH to PMC

Access Method

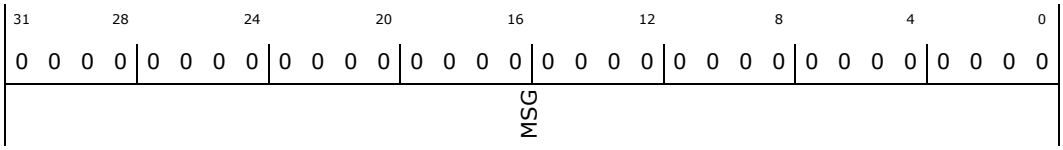
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 29Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.169 reg_ISH2PMC_MSG17_type (ISH2PMC_MSG17)—Offset 2A0h

Message from ISH to PMC

Access Method

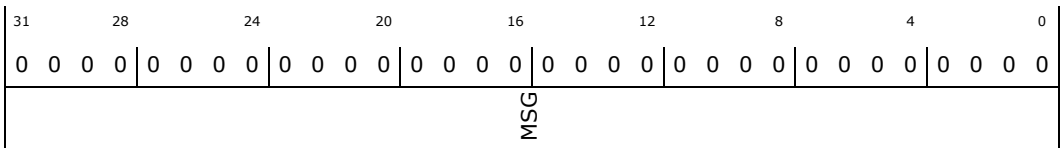
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2A0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.170 reg_ISH2PMC_MSG18_type (ISH2PMC_MSG18)—Offset 2A4h

Message from ISH to PMC

Access Method

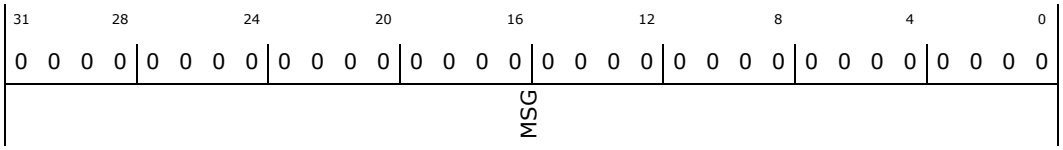
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2A4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.171 reg_ISH2PMC_MSG19_type (ISH2PMC_MSG19)—Offset 2A8h

Message from ISH to PMC

Access Method

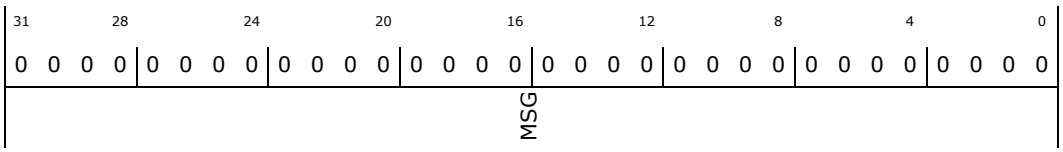
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2A8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.172 reg_ISH2PMC_MSG20_type (ISH2PMC_MSG20)—Offset 2ACh

Message from ISH to PMC

Access Method

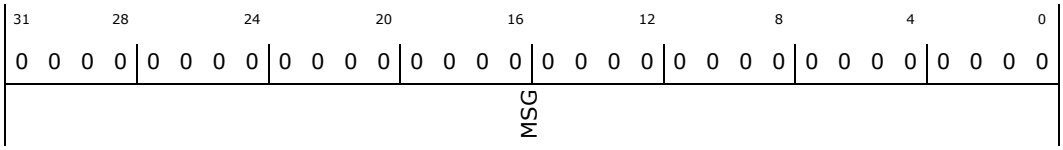
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2ACh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.173 reg_ISH2PMC_MSG21_type (ISH2PMC_MSG21)—Offset 2B0h

Message from ISH to PMC

Access Method

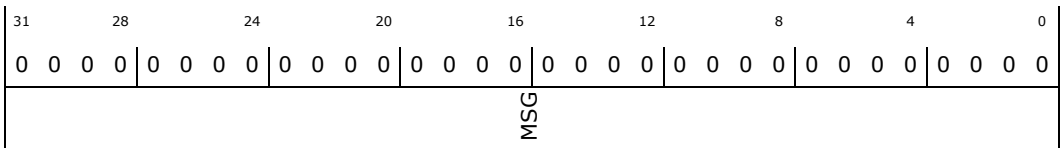
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2B0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.174 reg_ISH2PMC_MSG22_type (ISH2PMC_MSG22)—Offset 2B4h

Message from ISH to PMC

Access Method

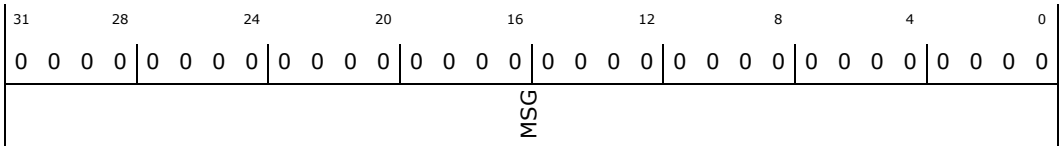
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2B4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.175 reg_ISH2PMC_MSG23_type (ISH2PMC_MSG23)—Offset 2B8h

Message from ISH to PMC

Access Method

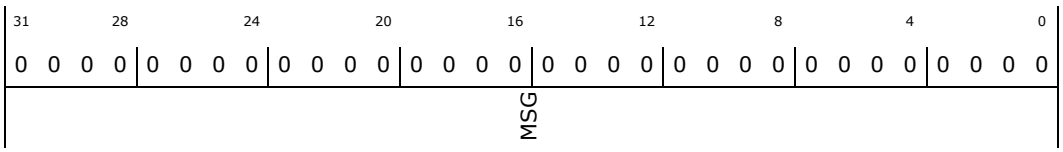
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2B8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.176 reg_ISH2PMC_MSG24_type (ISH2PMC_MSG24)—Offset 2BCh

Message from ISH to PMC

Access Method

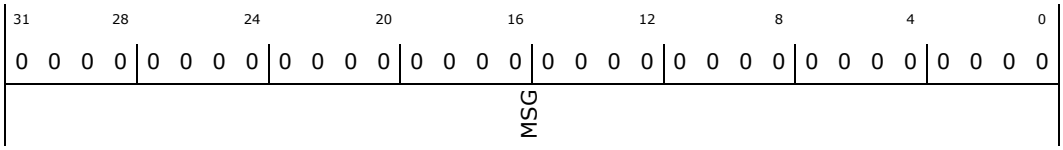
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2BCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.177 reg_ISH2PMC_MSG25_type (ISH2PMC_MSG25)—Offset 2C0h

Message from ISH to PMC

Access Method

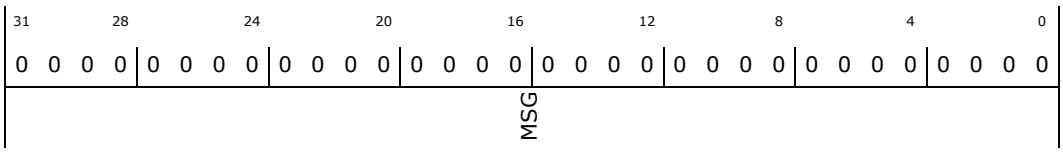
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2C0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.178 reg_ISH2PMC_MSG26_type (ISH2PMC_MSG26)—Offset 2C4h

Message from ISH to PMC

Access Method

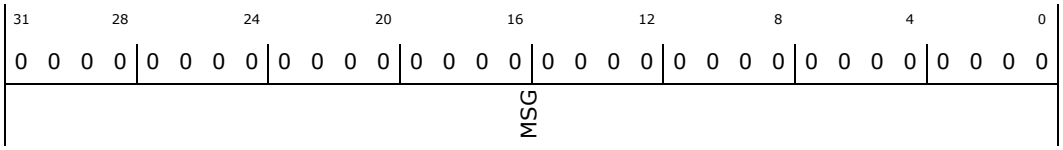
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2C4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.179 reg_ISH2PMC_MSG27_type (ISH2PMC_MSG27)—Offset 2C8h

Message from ISH to PMC

Access Method

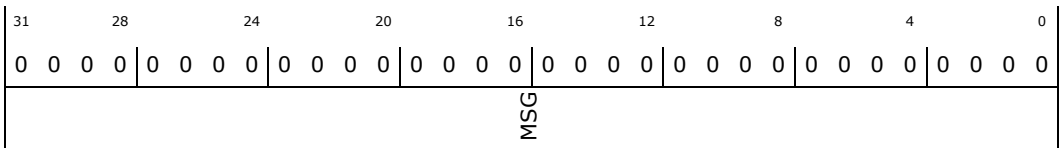
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2C8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.180 reg_ISH2PMC_MSG28_type (ISH2PMC_MSG28)—Offset 2CCh

Message from ISH to PMC

Access Method

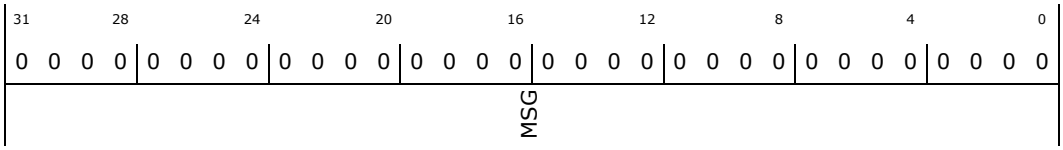
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2CCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.181 reg_ISH2PMC_MSG29_type (ISH2PMC_MSG29)—Offset 2D0h

Message from ISH to PMC

Access Method

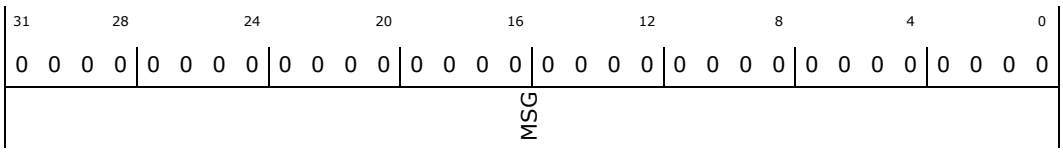
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2D0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.182 reg_ISH2PMC_MSG30_type (ISH2PMC_MSG30)—Offset 2D4h

Message from ISH to PMC

Access Method

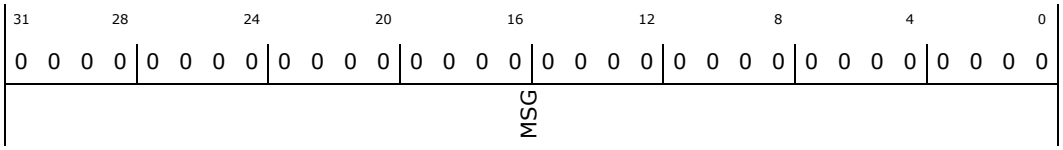
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2D4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.183 reg_ISH2PMC_MSG31_type (ISH2PMC_MSG31)—Offset 2D8h

Message from ISH to PMC

Access Method

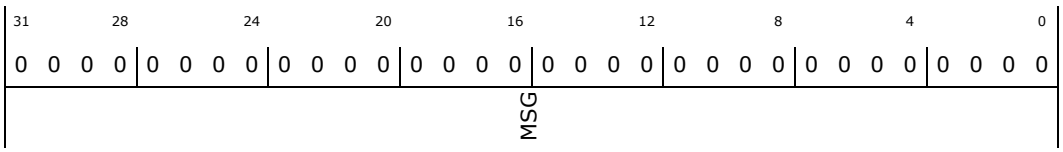
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2D8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.184 reg_ISH2PMC_MSG32_type (ISH2PMC_MSG32)—Offset 2DCh

Message from ISH to PMC

Access Method

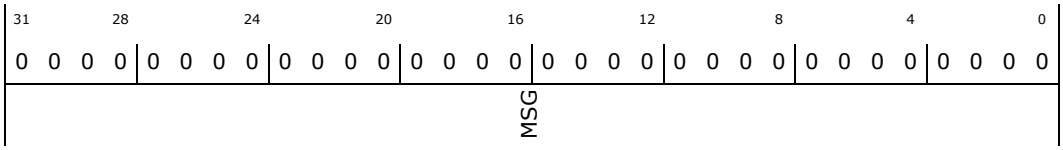
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2DCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.185 reg_PMC2ISH_MSG1_type (PMC2ISH_MSG1)—Offset 2E0h

Message from PMC to ISH

Access Method

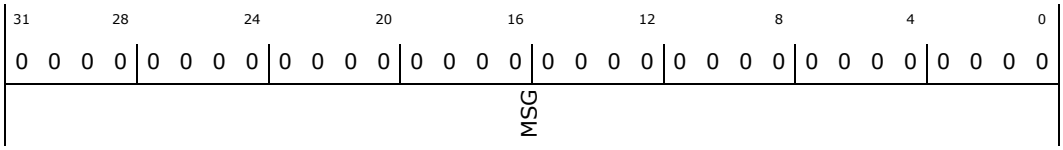
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2E0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.186 reg_PMC2ISH_MSG2_type (PMC2ISH_MSG2)—Offset 2E4h

Message from PMC to ISH

Access Method

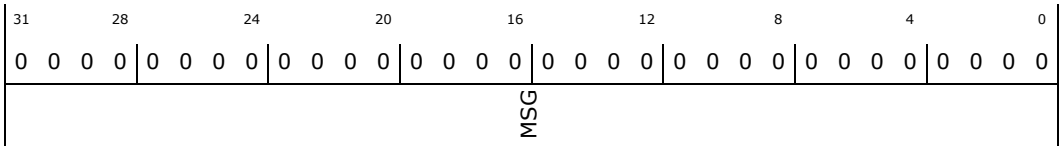
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2E4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.187 reg_PMC2ISH_MSG3_type (PMC2ISH_MSG3)—Offset 2E8h

Message from PMC to ISH

Access Method

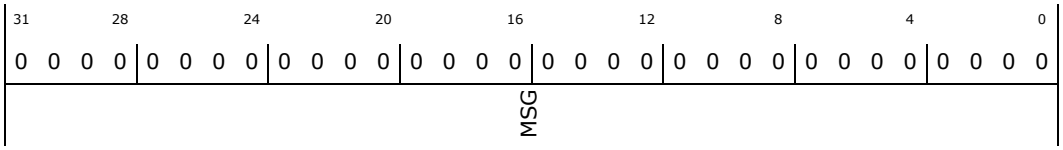
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2E8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.188 reg_PMC2ISH_MSG4_type (PMC2ISH_MSG4)—Offset 2ECh

Message from PMC to ISH

Access Method

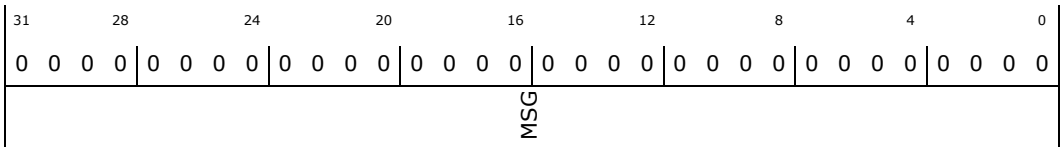
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2ECh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.189 reg_PMC2ISH_MSG5_type (PMC2ISH_MSG5)—Offset 2F0h

Message from PMC to ISH

Access Method

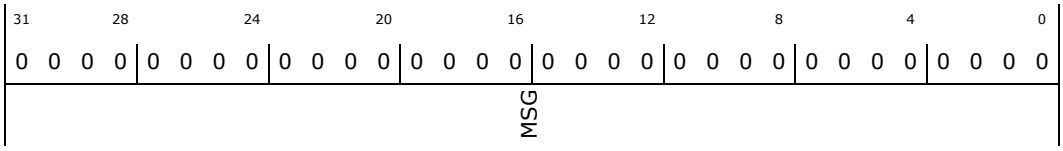
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2F0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.190 reg_PMC2ISH_MSG6_type (PMC2ISH_MSG6)—Offset 2F4h

Message from PMC to ISH

Access Method

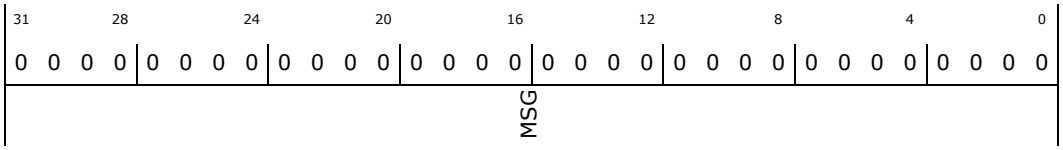
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2F4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.191 reg_PMC2ISH_MSG7_type (PMC2ISH_MSG7)—Offset 2F8h

Message from PMC to ISH

Access Method

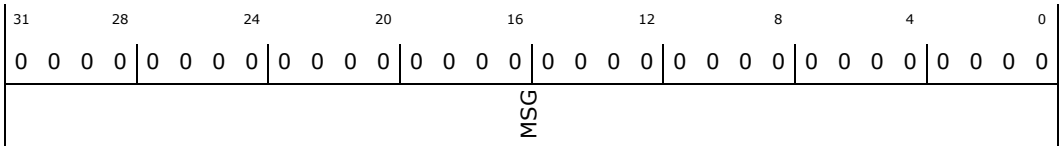
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2F8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.192 reg_PMC2ISH_MSG8_type (PMC2ISH_MSG8)—Offset 2FCh

Message from PMC to ISH

Access Method

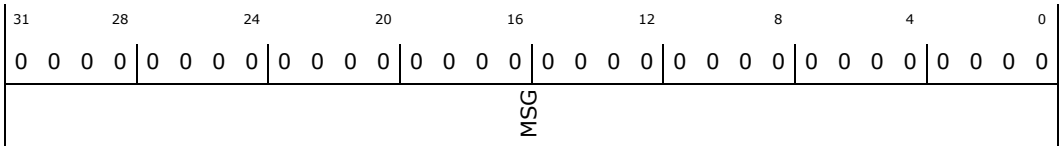
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2FCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.193 reg_PMC2ISH_MSG9_type (PMC2ISH_MSG9)—Offset 300h

Message from PMC to ISH

Access Method

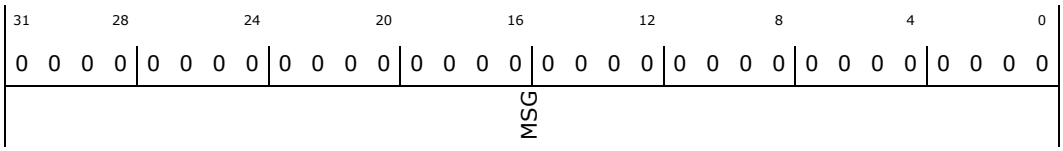
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 300h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.194 reg_PMC2ISH_MSG10_type (PMC2ISH_MSG10)—Offset 304h

Message from PMC to ISH

Access Method

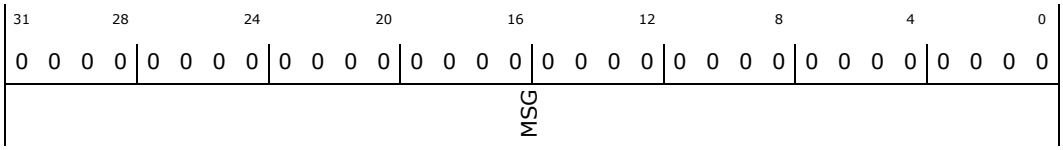
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 304h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.195 reg_PMC2ISH_MSG11_type (PMC2ISH_MSG11)—Offset 308h

Message from PMC to ISH

Access Method

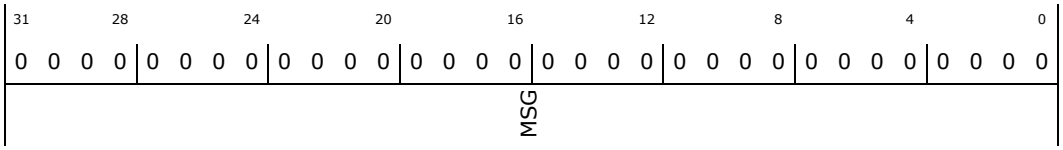
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 308h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.196 reg_PMC2ISH_MSG12_type (PMC2ISH_MSG12)—Offset 30Ch

Message from PMC to ISH

Access Method

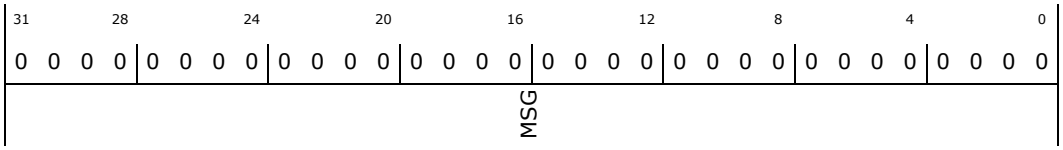
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 30Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.197 reg_PMC2ISH_MSG13_type (PMC2ISH_MSG13)—Offset 310h

Message from PMC to ISH

Access Method

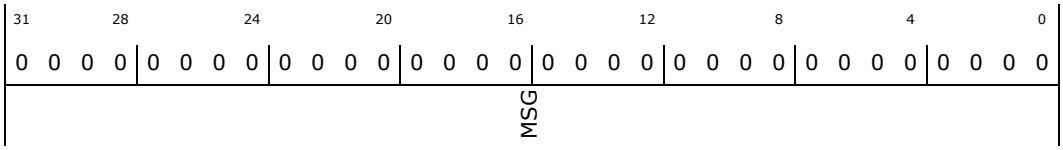
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 310h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.198 reg_PMC2ISH_MSG14_type (PMC2ISH_MSG14)—Offset 314h

Message from PMC to ISH

Access Method

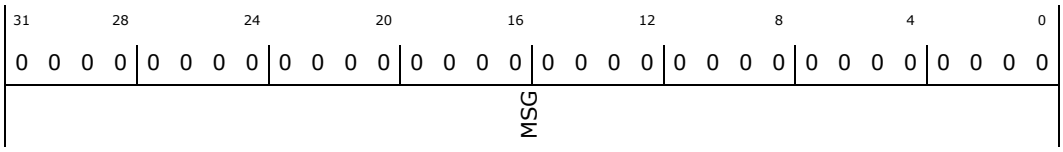
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 314h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.199 reg_PMC2ISH_MSG15_type (PMC2ISH_MSG15)—Offset 318h

Message from PMC to ISH

Access Method

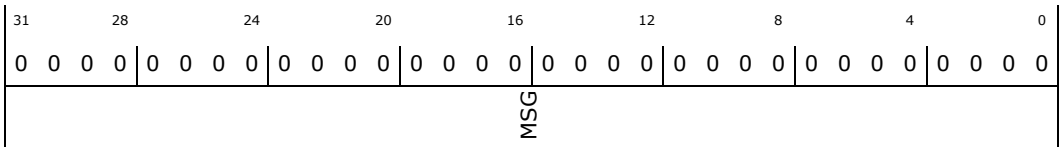
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 318h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.200 reg_PMC2ISH_MSG16_type (PMC2ISH_MSG16)—Offset 31Ch

Message from PMC to ISH

Access Method

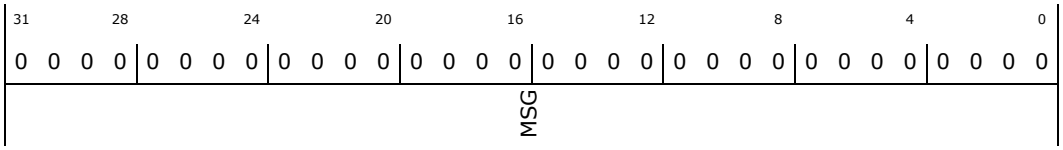
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 31Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.201 reg_PMC2ISH_MSG17_type (PMC2ISH_MSG17)—Offset 320h

Message from PMC to ISH

Access Method

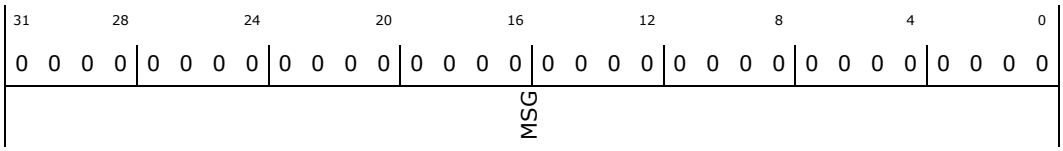
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 320h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.202 reg_PMC2ISH_MSG18_type (PMC2ISH_MSG18)—Offset 324h

Message from PMC to ISH

Access Method

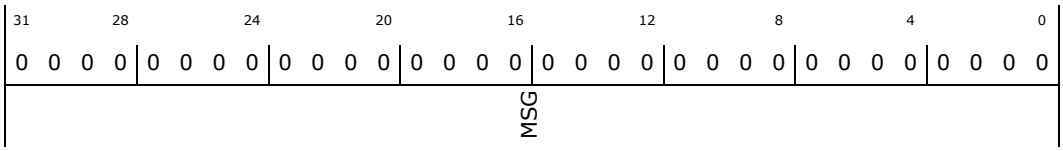
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 324h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.203 reg_PMC2ISH_MSG19_type (PMC2ISH_MSG19)—Offset 328h

Message from PMC to ISH

Access Method

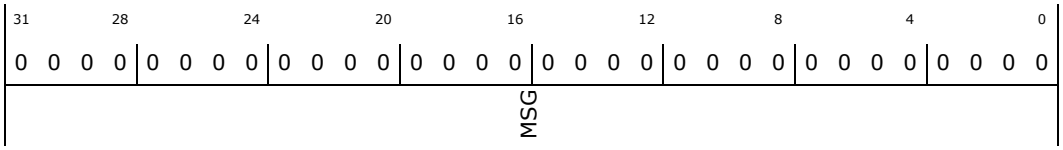
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 328h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.204 reg_PMC2ISH_MSG20_type (PMC2ISH_MSG20)—Offset 32Ch

Message from PMC to ISH

Access Method

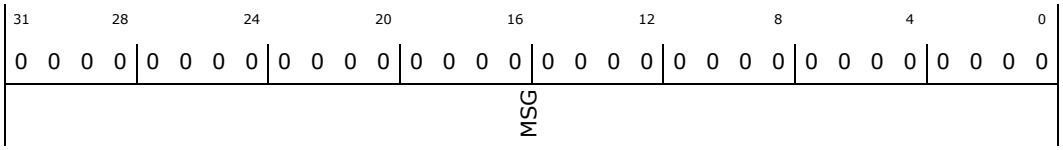
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 32Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.205 reg_PMC2ISH_MSG21_type (PMC2ISH_MSG21)—Offset 330h

Message from PMC to ISH

Access Method

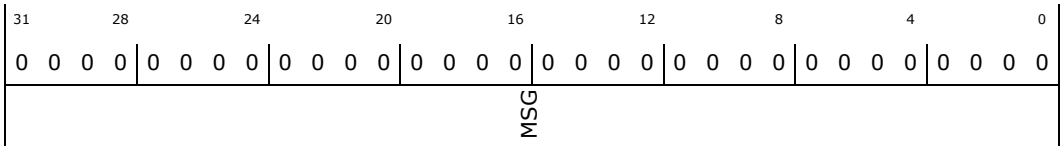
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 330h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.206 reg_PMC2ISH_MSG22_type (PMC2ISH_MSG22)—Offset 334h

Message from PMC to ISH

Access Method

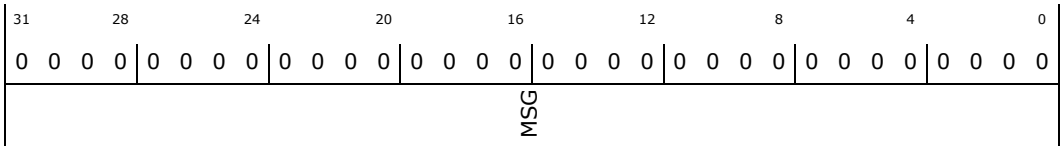
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 334h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.207 reg_PMC2ISH_MSG23_type (PMC2ISH_MSG23)—Offset 338h

Message from PMC to ISH

Access Method

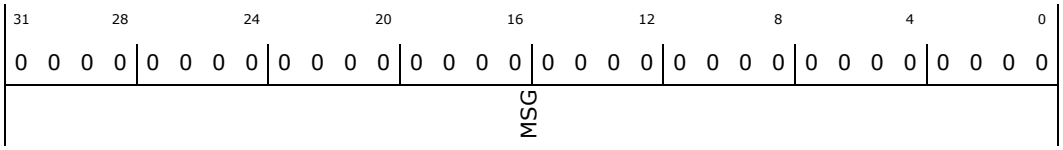
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 338h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.208 reg_PMC2ISH_MSG24_type (PMC2ISH_MSG24)—Offset 33Ch

Message from PMC to ISH

Access Method

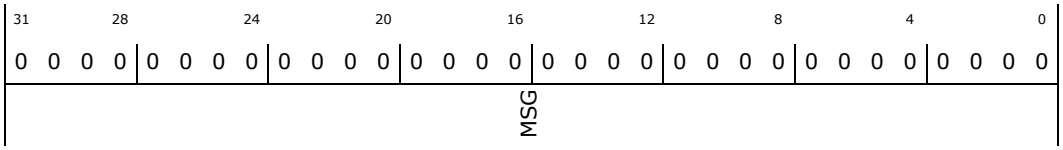
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 33Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.209 reg_PMC2ISH_MSG25_type (PMC2ISH_MSG25)—Offset 340h

Message from PMC to ISH

Access Method

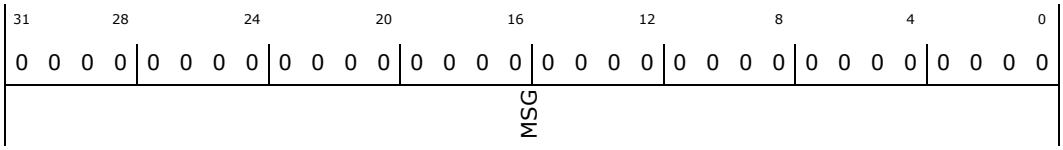
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 340h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.210 reg_PMC2ISH_MSG26_type (PMC2ISH_MSG26)—Offset 344h

Message from PMC to ISH

Access Method

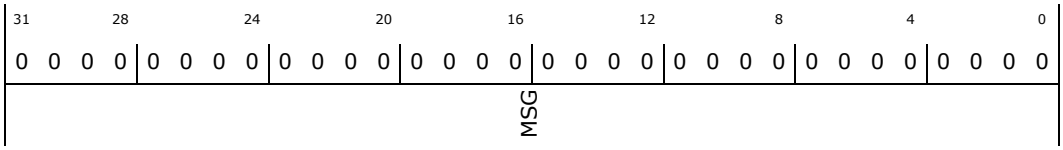
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 344h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.211 reg_PMC2ISH_MSG27_type (PMC2ISH_MSG27)—Offset 348h

Message from PMC to ISH

Access Method

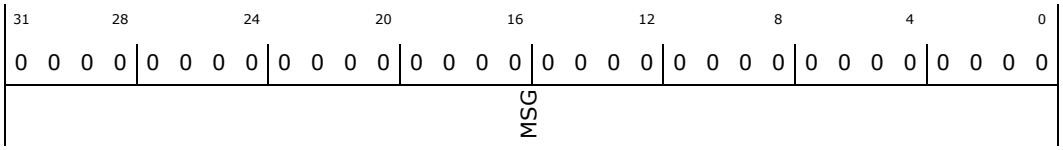
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 348h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.212 reg_PMC2ISH_MSG28_type (PMC2ISH_MSG28)—Offset 34Ch

Message from PMC to ISH

Access Method

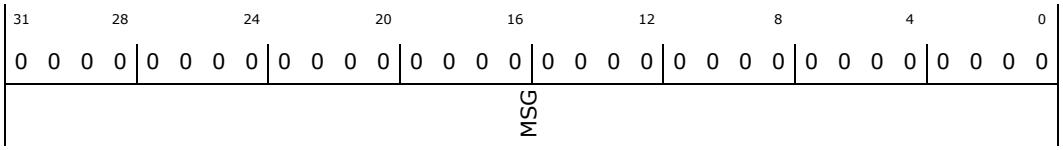
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 34Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.213 reg_PMC2ISH_MSG29_type (PMC2ISH_MSG29)—Offset 350h

Message from PMC to ISH

Access Method

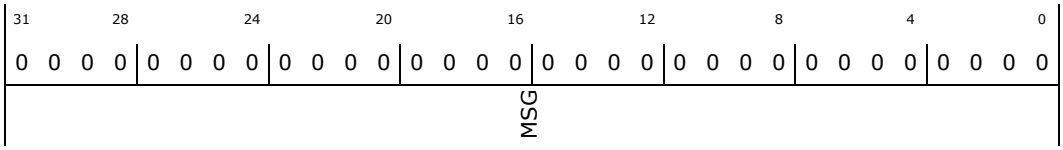
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 350h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.214 reg_PMC2ISH_MSG30_type (PMC2ISH_MSG30)—Offset 354h

Message from PMC to ISH

Access Method

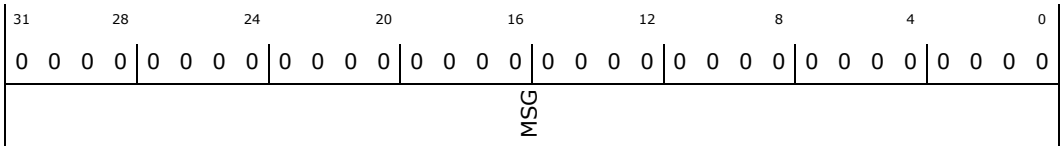
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 354h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.215 reg_PMC2ISH_MSG31_type (PMC2ISH_MSG31)—Offset 358h

Message from PMC to ISH

Access Method

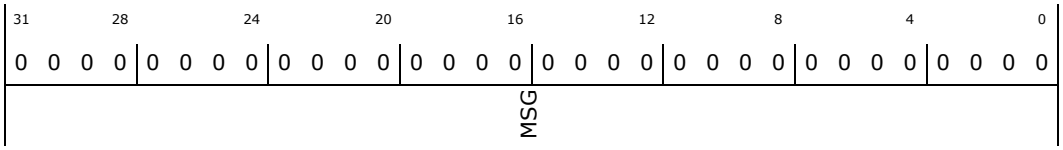
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 358h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.216 reg_PMC2ISH_MSG32_type (PMC2ISH_MSG32)—Offset 35Ch

Message from PMC to ISH

Access Method

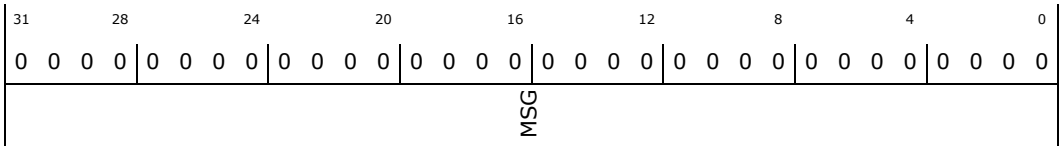
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 35Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.1.217 reg_REMAP0_type (REMAP0)—Offset 360h

REMAP0

Access Method

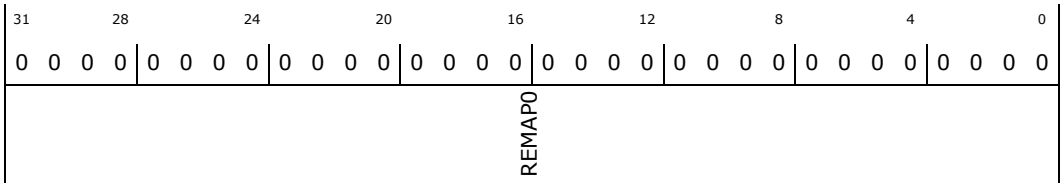
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 360h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**REMAP0:** ish_clk

12.1.218 reg_REMAP1_type (REMAP1)—Offset 364h

REMAP1

Access Method

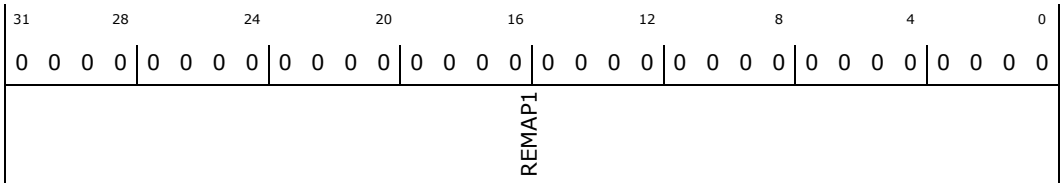
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 364h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**REMAP1:** ish_clk

12.1.219 reg_REMAP2_type (REMAP2)—Offset 368h

REMAP2

Access Method

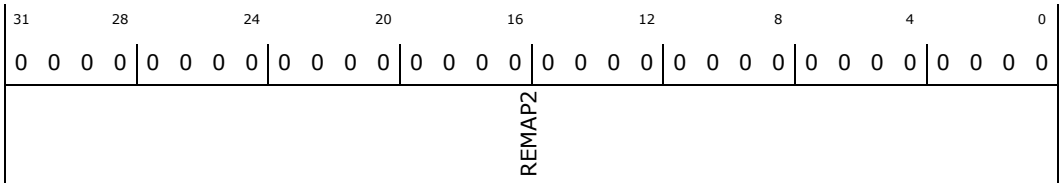
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 368h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**REMAP2:** ish_clk

12.1.220 reg_REMAP3_type (REMAP3)—Offset 36Ch

REMAP3

Access Method

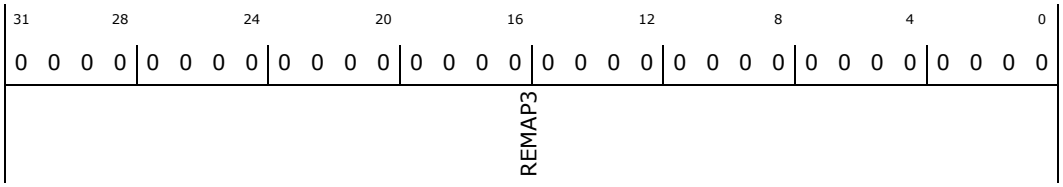
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 36Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**REMAP3:** ish_clk

12.1.221 reg_REMAP4_type (REMAP4)—Offset 370h

REMAP4

Access Method

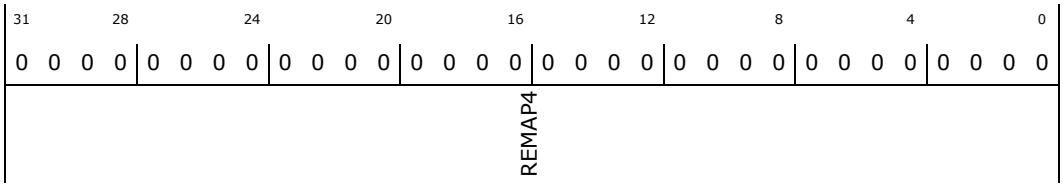
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 370h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**REMAP4:** ish_clk

12.1.222 reg_REMAP5_type (REMAP5)—Offset 374h

REMAP5

Access Method

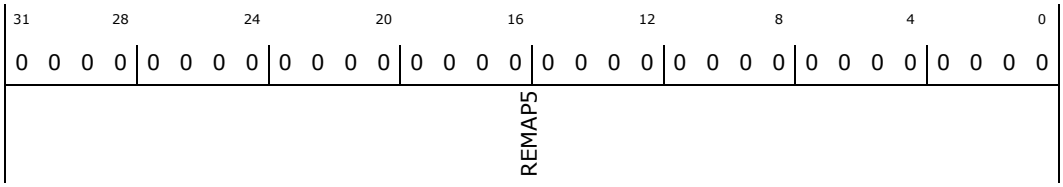
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 374h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**REMAP5:** ish_clk

12.1.223 reg_ISH_IPC_BUSY_CLEAR_type (ISH_IPC_BUSY_CLEAR)—Offset 378h

Reserved

Access Method

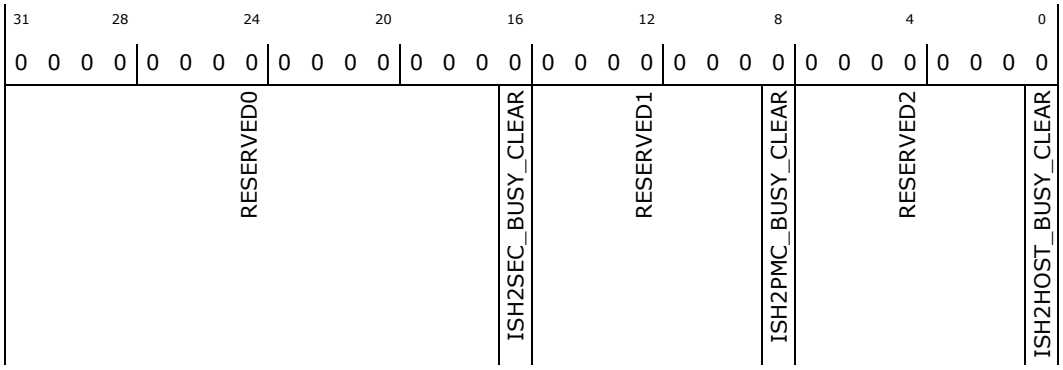
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 378h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RESERVED0:** ish_clk
16	0x0 RW/1C	**ISH2SEC_BUSY_CLEAR:** ish_clk
15:9	0x0 RO	**RESERVED1:** ish_clk
8	0x0 RW/1C	**ISH2PMC_BUSY_CLEAR:** ish_clk
7:1	0x0 RO	**RESERVED2:** ish_clk
0	0x0 RW/1C	**ISH2HOST_BUSY_CLEAR:** ish_clk

12.1.224 reg_ISH_FUSE_type (ISH_FUSE)—Offset 37Ch

Reserved

Access Method

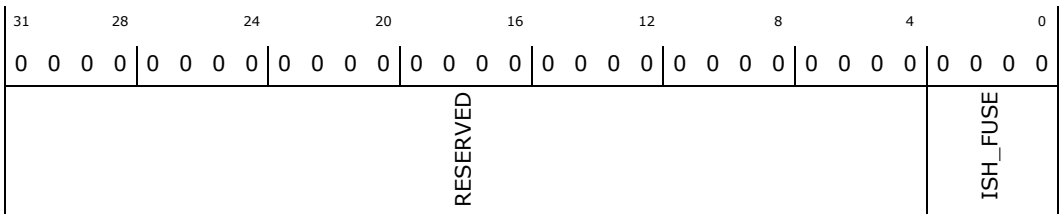
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 37Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RESERVED:** ish_clk
3:0	0x0 RO	**ISH_FUSE:** ish_clk

12.1.225 reg_UMA_RANGE_LOWER_0_type (UMA_RANGE_LOWER_0)—Offset 380h

UMA base address LSB register

Access Method

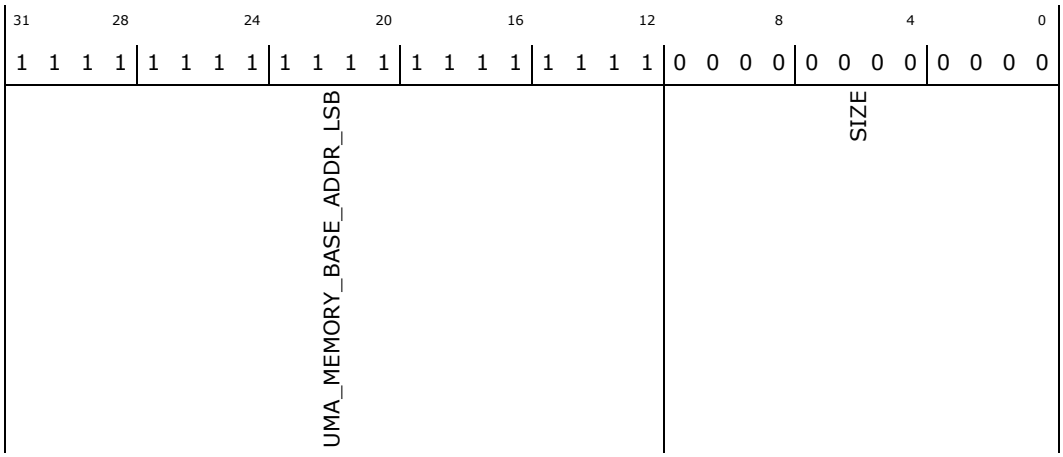
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 380h

Op Codes:

h - Read, h - Write

Default: FFFFF000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0xfffff RW	**UMA_MEMORY_BASE_ADDR_LSB:** ish_clk
11:0	0x0 RO	**SIZE:** ish_clk

12.1.226 reg_UMA_RANGE_LOWER_1_type (UMA_RANGE_LOWER_1)—Offset 384h

UMA base address MSB register

Access Method

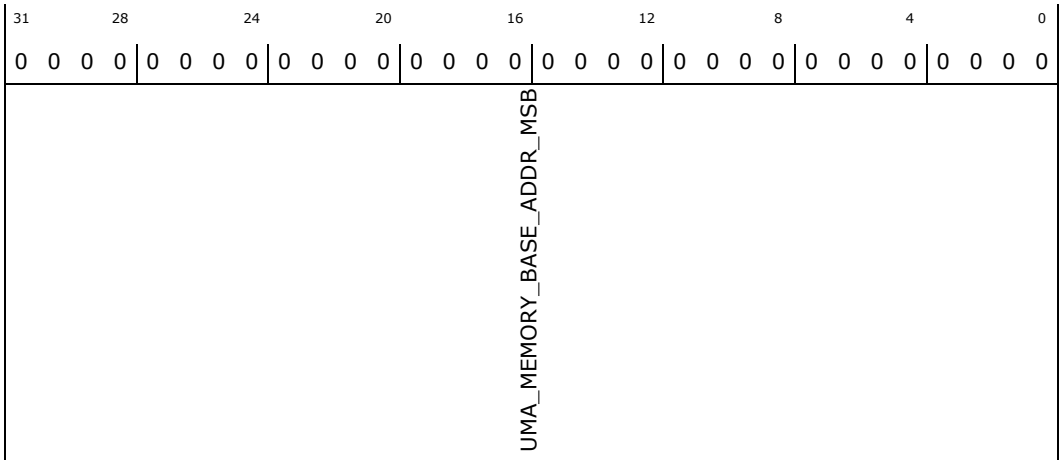
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 384h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**UMA_MEMORY_BASE_ADDR_MSB:** ish_clk

12.1.227 reg_UMA_RANGE_UPPER_0_type (UMA_RANGE_UPPER_0)—Offset 388h

UMA limit address LSB register

Access Method

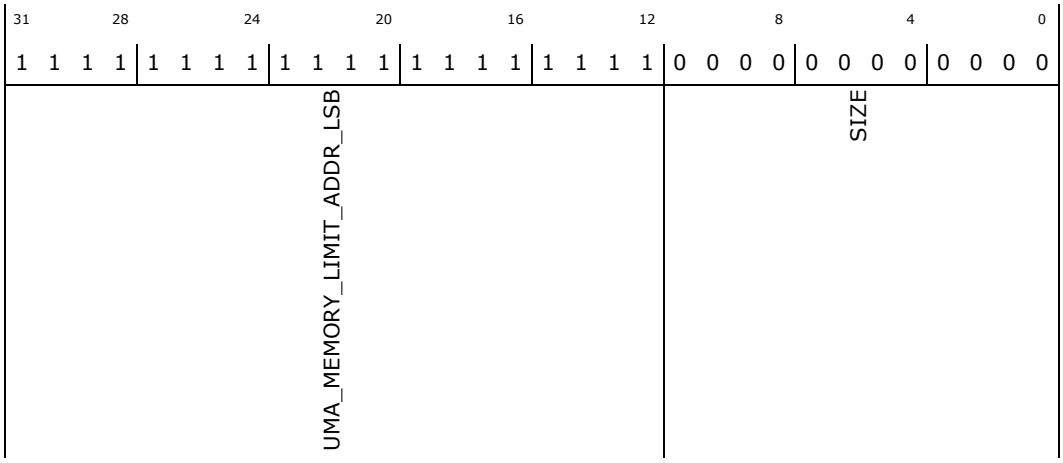
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 388h

Op Codes:

h - Read, h - Write

Default: FFFFF000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0xfffff RW	**UMA_MEMORY_LIMIT_ADDR_LSB:** ish_clk
11:0	0x0 RO	**SIZE:** ish_clk

12.1.228 reg_UMA_RANGE_UPPER_1_type (UMA_RANGE_UPPER_1)—Offset 38Ch

UMA limit address MSB register

Access Method

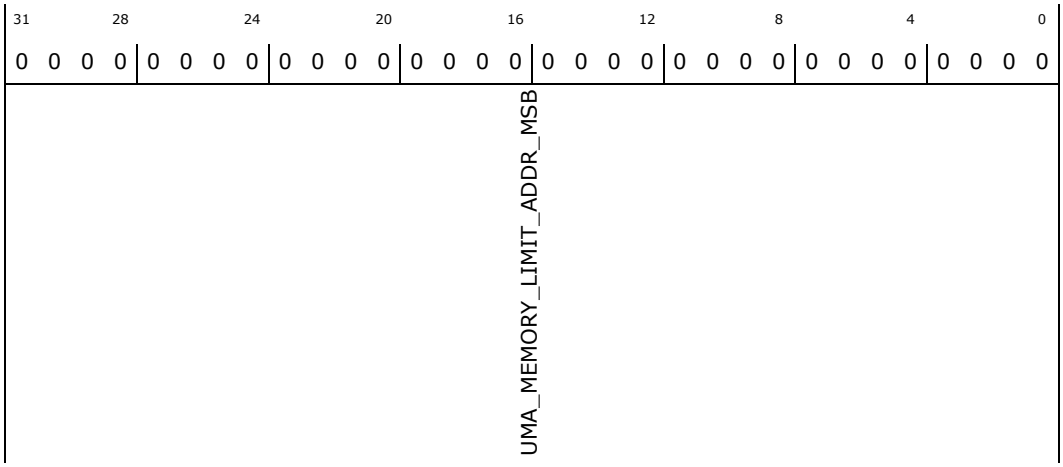
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 38Ch

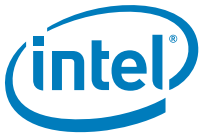
Op Codes:

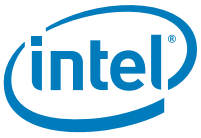
h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**UMA_MEMORY_LIMIT_ADDR_MSB:** ish_clk

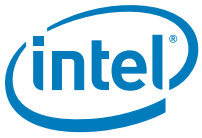




12.2 ISH IPC Memory Mapped I/O Registers

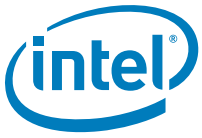
Table 121. Summary of ISH IPC Memory Mapped I/O Registers—IOSF2OCP_PCI_cfg.BAR

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"reg_PISR_type (PISR)—Offset 0h" on page 6312	00000000h
4–7h	4	"reg_PIMR_type (PIMR)—Offset 4h" on page 6312	00000000h
8–Bh	4	"reg_RESERVED0_type (RESERVED0)—Offset 8h" on page 6313	00000000h
C–Fh	4	"reg_RESERVED1_type (RESERVED1)—Offset Ch" on page 6314	00000000h
10–13h	4	"reg_RESERVED2_type (RESERVED2)—Offset 10h" on page 6314	00000000h
14–17h	4	"reg_RESERVED3_type (RESERVED3)—Offset 14h" on page 6315	00000000h
18–1Bh	4	"reg_RESERVED4_type (RESERVED4)—Offset 18h" on page 6315	00000000h
1C–1Fh	4	"reg_RESERVED5_type (RESERVED5)—Offset 1Ch" on page 6316	00000000h
20–23h	4	"reg_RESERVED6_type (RESERVED6)—Offset 20h" on page 6316	00000000h
24–27h	4	"reg_RESERVED7_type (RESERVED7)—Offset 24h" on page 6317	00000000h
28–2Bh	4	"reg_RESERVED8_type (RESERVED8)—Offset 28h" on page 6317	00000000h
2C–2Fh	4	"reg_RESERVED9_type (RESERVED9)—Offset 2Ch" on page 6318	00000000h
30–33h	4	"reg_RESERVED10_type (RESERVED10)—Offset 30h" on page 6318	00000000h
34–37h	4	"reg_ISH_HOST_FWSTS_type (ISH_HOST_FWSTS)—Offset 34h" on page 6319	00000000h
38–3Bh	4	"reg_HOST_COMM_type (HOST_COMM)—Offset 38h" on page 6319	00000000h
3C–3Fh	4	"reg_ISH_SEC_FWSTS_type (ISH_SEC_FWSTS)—Offset 3Ch" on page 6320	00000000h
40–43h	4	"reg_SEC_COMM_type (SEC_COMM)—Offset 40h" on page 6320	00000000h
44–47h	4	"reg_ISH_RST_type (ISH_RST)—Offset 44h" on page 6321	00000000h
48–4Bh	4	"reg_HOST2ISH_DOORBELL_type (HOST2ISH_DOORBELL)—Offset 48h" on page 6321	00000000h
4C–4Fh	4	"reg_PMC2ISH_DOORBELL_type (PMC2ISH_DOORBELL)—Offset 4Ch" on page 6322	00000000h
50–53h	4	"reg_SEC2ISH_DOORBELL_type (SEC2ISH_DOORBELL)—Offset 50h" on page 6322	00000000h
54–57h	4	"reg_ISH2HOST_DOORBELL_type (ISH2HOST_DOORBELL)—Offset 54h" on page 6323	00000000h
58–5Bh	4	"reg_ISH2PMC_DOORBELL_type (ISH2PMC_DOORBELL)—Offset 58h" on page 6324	00000000h
5C–5Fh	4	"reg_ISH2SEC_DOORBELL_type (ISH2SEC_DOORBELL)—Offset 5Ch" on page 6324	00000000h
60–63h	4	"reg_ISH2HOST_MSG1_type (ISH2HOST_MSG1)—Offset 60h" on page 6325	00000000h
64–67h	4	"reg_ISH2HOST_MSG2_type (ISH2HOST_MSG2)—Offset 64h" on page 6325	00000000h
68–6Bh	4	"reg_ISH2HOST_MSG3_type (ISH2HOST_MSG3)—Offset 68h" on page 6326	00000000h



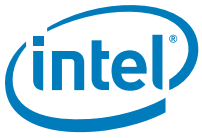
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
6C–6Fh	4	"reg_ISH2HOST_MSG4_type (ISH2HOST_MSG4)—Offset 6Ch" on page 6326	00000000h
70–73h	4	"reg_ISH2HOST_MSG5_type (ISH2HOST_MSG5)—Offset 70h" on page 6326	00000000h
74–77h	4	"reg_ISH2HOST_MSG6_type (ISH2HOST_MSG6)—Offset 74h" on page 6327	00000000h
78–7Bh	4	"reg_ISH2HOST_MSG7_type (ISH2HOST_MSG7)—Offset 78h" on page 6327	00000000h
7C–7Fh	4	"reg_ISH2HOST_MSG8_type (ISH2HOST_MSG8)—Offset 7Ch" on page 6328	00000000h
80–83h	4	"reg_ISH2HOST_MSG9_type (ISH2HOST_MSG9)—Offset 80h" on page 6328	00000000h
84–87h	4	"reg_ISH2HOST_MSG10_type (ISH2HOST_MSG10)—Offset 84h" on page 6329	00000000h
88–8Bh	4	"reg_ISH2HOST_MSG11_type (ISH2HOST_MSG11)—Offset 88h" on page 6329	00000000h
8C–8Fh	4	"reg_ISH2HOST_MSG12_type (ISH2HOST_MSG12)—Offset 8Ch" on page 6329	00000000h
90–93h	4	"reg_ISH2HOST_MSG13_type (ISH2HOST_MSG13)—Offset 90h" on page 6330	00000000h
94–97h	4	"reg_ISH2HOST_MSG14_type (ISH2HOST_MSG14)—Offset 94h" on page 6330	00000000h
98–9Bh	4	"reg_ISH2HOST_MSG15_type (ISH2HOST_MSG15)—Offset 98h" on page 6331	00000000h
9C–9Fh	4	"reg_ISH2HOST_MSG16_type (ISH2HOST_MSG16)—Offset 9Ch" on page 6331	00000000h
A0–A3h	4	"reg_ISH2HOST_MSG17_type (ISH2HOST_MSG17)—Offset A0h" on page 6332	00000000h
A4–A7h	4	"reg_ISH2HOST_MSG18_type (ISH2HOST_MSG18)—Offset A4h" on page 6332	00000000h
A8–ABh	4	"reg_ISH2HOST_MSG19_type (ISH2HOST_MSG19)—Offset A8h" on page 6332	00000000h
AC–AFh	4	"reg_ISH2HOST_MSG20_type (ISH2HOST_MSG20)—Offset ACh" on page 6333	00000000h
B0–B3h	4	"reg_ISH2HOST_MSG21_type (ISH2HOST_MSG21)—Offset B0h" on page 6333	00000000h
B4–B7h	4	"reg_ISH2HOST_MSG22_type (ISH2HOST_MSG22)—Offset B4h" on page 6334	00000000h
B8–BBh	4	"reg_ISH2HOST_MSG23_type (ISH2HOST_MSG23)—Offset B8h" on page 6334	00000000h
BC–BFh	4	"reg_ISH2HOST_MSG24_type (ISH2HOST_MSG24)—Offset BCh" on page 6335	00000000h
C0–C3h	4	"reg_ISH2HOST_MSG25_type (ISH2HOST_MSG25)—Offset C0h" on page 6335	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
C4–C7h	4	"reg_ISH2HOST_MSG26_type (ISH2HOST_MSG26)—Offset C4h" on page 6335	00000000h
C8–CBh	4	"reg_ISH2HOST_MSG27_type (ISH2HOST_MSG27)—Offset C8h" on page 6336	00000000h
CC–CFh	4	"reg_ISH2HOST_MSG28_type (ISH2HOST_MSG28)—Offset CCh" on page 6336	00000000h
D0–D3h	4	"reg_ISH2HOST_MSG29_type (ISH2HOST_MSG29)—Offset D0h" on page 6337	00000000h
D4–D7h	4	"reg_ISH2HOST_MSG30_type (ISH2HOST_MSG30)—Offset D4h" on page 6337	00000000h
D8–DBh	4	"reg_ISH2HOST_MSG31_type (ISH2HOST_MSG31)—Offset D8h" on page 6338	00000000h
DC–DFh	4	"reg_ISH2HOST_MSG32_type (ISH2HOST_MSG32)—Offset DCh" on page 6338	00000000h
E0–E3h	4	"reg_HOST2ISH_MSG1_type (HOST2ISH_MSG1)—Offset E0h" on page 6338	00000000h
E4–E7h	4	"reg_HOST2ISH_MSG2_type (HOST2ISH_MSG2)—Offset E4h" on page 6339	00000000h
E8–EBh	4	"reg_HOST2ISH_MSG3_type (HOST2ISH_MSG3)—Offset E8h" on page 6339	00000000h
EC–EFh	4	"reg_HOST2ISH_MSG4_type (HOST2ISH_MSG4)—Offset ECh" on page 6340	00000000h
F0–F3h	4	"reg_HOST2ISH_MSG5_type (HOST2ISH_MSG5)—Offset F0h" on page 6340	00000000h
F4–F7h	4	"reg_HOST2ISH_MSG6_type (HOST2ISH_MSG6)—Offset F4h" on page 6341	00000000h
F8–FBh	4	"reg_HOST2ISH_MSG7_type (HOST2ISH_MSG7)—Offset F8h" on page 6341	00000000h
FC–FFh	4	"reg_HOST2ISH_MSG8_type (HOST2ISH_MSG8)—Offset FCh" on page 6341	00000000h
100–103h	4	"reg_HOST2ISH_MSG9_type (HOST2ISH_MSG9)—Offset 100h" on page 6342	00000000h
104–107h	4	"reg_HOST2ISH_MSG10_type (HOST2ISH_MSG10)—Offset 104h" on page 6342	00000000h
108–10Bh	4	"reg_HOST2ISH_MSG11_type (HOST2ISH_MSG11)—Offset 108h" on page 6343	00000000h
10C–10Fh	4	"reg_HOST2ISH_MSG12_type (HOST2ISH_MSG12)—Offset 10Ch" on page 6343	00000000h
110–113h	4	"reg_HOST2ISH_MSG13_type (HOST2ISH_MSG13)—Offset 110h" on page 6344	00000000h
114–117h	4	"reg_HOST2ISH_MSG14_type (HOST2ISH_MSG14)—Offset 114h" on page 6344	00000000h
118–11Bh	4	"reg_HOST2ISH_MSG15_type (HOST2ISH_MSG15)—Offset 118h" on page 6344	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
11C–11Fh	4	"reg_HOST2ISH_MSG16_type (HOST2ISH_MSG16)—Offset 11Ch" on page 6345	00000000h
120–123h	4	"reg_HOST2ISH_MSG17_type (HOST2ISH_MSG17)—Offset 120h" on page 6345	00000000h
124–127h	4	"reg_HOST2ISH_MSG18_type (HOST2ISH_MSG18)—Offset 124h" on page 6346	00000000h
128–12Bh	4	"reg_HOST2ISH_MSG19_type (HOST2ISH_MSG19)—Offset 128h" on page 6346	00000000h
12C–12Fh	4	"reg_HOST2ISH_MSG20_type (HOST2ISH_MSG20)—Offset 12Ch" on page 6347	00000000h
130–133h	4	"reg_HOST2ISH_MSG21_type (HOST2ISH_MSG21)—Offset 130h" on page 6347	00000000h
134–137h	4	"reg_HOST2ISH_MSG22_type (HOST2ISH_MSG22)—Offset 134h" on page 6347	00000000h
138–13Bh	4	"reg_HOST2ISH_MSG23_type (HOST2ISH_MSG23)—Offset 138h" on page 6348	00000000h
13C–13Fh	4	"reg_HOST2ISH_MSG24_type (HOST2ISH_MSG24)—Offset 13Ch" on page 6348	00000000h
140–143h	4	"reg_HOST2ISH_MSG25_type (HOST2ISH_MSG25)—Offset 140h" on page 6349	00000000h
144–147h	4	"reg_HOST2ISH_MSG26_type (HOST2ISH_MSG26)—Offset 144h" on page 6349	00000000h
148–14Bh	4	"reg_HOST2ISH_MSG27_type (HOST2ISH_MSG27)—Offset 148h" on page 6350	00000000h
14C–14Fh	4	"reg_HOST2ISH_MSG28_type (HOST2ISH_MSG28)—Offset 14Ch" on page 6350	00000000h
150–153h	4	"reg_HOST2ISH_MSG29_type (HOST2ISH_MSG29)—Offset 150h" on page 6350	00000000h
154–157h	4	"reg_HOST2ISH_MSG30_type (HOST2ISH_MSG30)—Offset 154h" on page 6351	00000000h
158–15Bh	4	"reg_HOST2ISH_MSG31_type (HOST2ISH_MSG31)—Offset 158h" on page 6351	00000000h
15C–15Fh	4	"reg_HOST2ISH_MSG32_type (HOST2ISH_MSG32)—Offset 15Ch" on page 6352	00000000h
160–163h	4	"reg_ISH2SEC_MSG1_type (ISH2SEC_MSG1)—Offset 160h" on page 6352	00000000h
164–167h	4	"reg_ISH2SEC_MSG2_type (ISH2SEC_MSG2)—Offset 164h" on page 6352	00000000h
168–16Bh	4	"reg_ISH2SEC_MSG3_type (ISH2SEC_MSG3)—Offset 168h" on page 6353	00000000h
16C–16Fh	4	"reg_ISH2SEC_MSG4_type (ISH2SEC_MSG4)—Offset 16Ch" on page 6353	00000000h
170–173h	4	"reg_ISH2SEC_MSG5_type (ISH2SEC_MSG5)—Offset 170h" on page 6354	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
174–177h	4	"reg_ISH2SEC_MSG6_type (ISH2SEC_MSG6)—Offset 174h" on page 6354	00000000h
178–17Bh	4	"reg_ISH2SEC_MSG7_type (ISH2SEC_MSG7)—Offset 178h" on page 6354	00000000h
17C–17Fh	4	"reg_ISH2SEC_MSG8_type (ISH2SEC_MSG8)—Offset 17Ch" on page 6355	00000000h
180–183h	4	"reg_ISH2SEC_MSG9_type (ISH2SEC_MSG9)—Offset 180h" on page 6355	00000000h
184–187h	4	"reg_ISH2SEC_MSG10_type (ISH2SEC_MSG10)—Offset 184h" on page 6356	00000000h
188–18Bh	4	"reg_ISH2SEC_MSG11_type (ISH2SEC_MSG11)—Offset 188h" on page 6356	00000000h
18C–18Fh	4	"reg_ISH2SEC_MSG12_type (ISH2SEC_MSG12)—Offset 18Ch" on page 6357	00000000h
190–193h	4	"reg_ISH2SEC_MSG13_type (ISH2SEC_MSG13)—Offset 190h" on page 6357	00000000h
194–197h	4	"reg_ISH2SEC_MSG14_type (ISH2SEC_MSG14)—Offset 194h" on page 6357	00000000h
198–19Bh	4	"reg_ISH2SEC_MSG15_type (ISH2SEC_MSG15)—Offset 198h" on page 6358	00000000h
19C–19Fh	4	"reg_ISH2SEC_MSG16_type (ISH2SEC_MSG16)—Offset 19Ch" on page 6358	00000000h
1A0–1A3h	4	"reg_ISH2SEC_MSG17_type (ISH2SEC_MSG17)—Offset 1A0h" on page 6359	00000000h
1A4–1A7h	4	"reg_ISH2SEC_MSG18_type (ISH2SEC_MSG18)—Offset 1A4h" on page 6359	00000000h
1A8–1ABh	4	"reg_ISH2SEC_MSG19_type (ISH2SEC_MSG19)—Offset 1A8h" on page 6360	00000000h
1AC–1AFh	4	"reg_ISH2SEC_MSG20_type (ISH2SEC_MSG20)—Offset 1ACh" on page 6360	00000000h
1B0–1B3h	4	"reg_ISH2SEC_MSG21_type (ISH2SEC_MSG21)—Offset 1B0h" on page 6360	00000000h
1B4–1B7h	4	"reg_ISH2SEC_MSG22_type (ISH2SEC_MSG22)—Offset 1B4h" on page 6361	00000000h
1B8–1BBh	4	"reg_ISH2SEC_MSG23_type (ISH2SEC_MSG23)—Offset 1B8h" on page 6361	00000000h
1BC–1BFh	4	"reg_ISH2SEC_MSG24_type (ISH2SEC_MSG24)—Offset 1BCh" on page 6362	00000000h
1C0–1C3h	4	"reg_ISH2SEC_MSG25_type (ISH2SEC_MSG25)—Offset 1C0h" on page 6362	00000000h
1C4–1C7h	4	"reg_ISH2SEC_MSG26_type (ISH2SEC_MSG26)—Offset 1C4h" on page 6363	00000000h
1C8–1CBh	4	"reg_ISH2SEC_MSG27_type (ISH2SEC_MSG27)—Offset 1C8h" on page 6363	00000000h

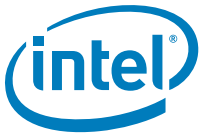


Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1CC–1CFh	4	"reg_ISH2SEC_MSG28_type (ISH2SEC_MSG28)—Offset 1CCh" on page 6363	00000000h
1D0–1D3h	4	"reg_ISH2SEC_MSG29_type (ISH2SEC_MSG29)—Offset 1D0h" on page 6364	00000000h
1D4–1D7h	4	"reg_ISH2SEC_MSG30_type (ISH2SEC_MSG30)—Offset 1D4h" on page 6364	00000000h
1D8–1DBh	4	"reg_ISH2SEC_MSG31_type (ISH2SEC_MSG31)—Offset 1D8h" on page 6365	00000000h
1DC–1DFh	4	"reg_ISH2SEC_MSG32_type (ISH2SEC_MSG32)—Offset 1DCh" on page 6365	00000000h
1E0–1E3h	4	"reg_SEC2ISH_MSG1_type (SEC2ISH_MSG1)—Offset 1E0h" on page 6365	00000000h
1E4–1E7h	4	"reg_SEC2ISH_MSG2_type (SEC2ISH_MSG2)—Offset 1E4h" on page 6366	00000000h
1E8–1EBh	4	"reg_SEC2ISH_MSG3_type (SEC2ISH_MSG3)—Offset 1E8h" on page 6366	00000000h
1EC–1EFh	4	"reg_SEC2ISH_MSG4_type (SEC2ISH_MSG4)—Offset 1ECh" on page 6367	00000000h
1F0–1F3h	4	"reg_SEC2ISH_MSG5_type (SEC2ISH_MSG5)—Offset 1F0h" on page 6367	00000000h
1F4–1F7h	4	"reg_SEC2ISH_MSG6_type (SEC2ISH_MSG6)—Offset 1F4h" on page 6367	00000000h
1F8–1FBh	4	"reg_SEC2ISH_MSG7_type (SEC2ISH_MSG7)—Offset 1F8h" on page 6368	00000000h
1FC–1FFh	4	"reg_SEC2ISH_MSG8_type (SEC2ISH_MSG8)—Offset 1FCh" on page 6368	00000000h
200–203h	4	"reg_SEC2ISH_MSG9_type (SEC2ISH_MSG9)—Offset 200h" on page 6369	00000000h
204–207h	4	"reg_SEC2ISH_MSG10_type (SEC2ISH_MSG10)—Offset 204h" on page 6369	00000000h
208–20Bh	4	"reg_SEC2ISH_MSG11_type (SEC2ISH_MSG11)—Offset 208h" on page 6369	00000000h
20C–20Fh	4	"reg_SEC2ISH_MSG12_type (SEC2ISH_MSG12)—Offset 20Ch" on page 6370	00000000h
210–213h	4	"reg_SEC2ISH_MSG13_type (SEC2ISH_MSG13)—Offset 210h" on page 6370	00000000h
214–217h	4	"reg_SEC2ISH_MSG14_type (SEC2ISH_MSG14)—Offset 214h" on page 6371	00000000h
218–21Bh	4	"reg_SEC2ISH_MSG15_type (SEC2ISH_MSG15)—Offset 218h" on page 6371	00000000h
21C–21Fh	4	"reg_SEC2ISH_MSG16_type (SEC2ISH_MSG16)—Offset 21Ch" on page 6372	00000000h
220–223h	4	"reg_SEC2ISH_MSG17_type (SEC2ISH_MSG17)—Offset 220h" on page 6372	00000000h

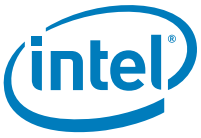
Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
224–227h	4	"reg_SEC2ISH_MSG18_type (SEC2ISH_MSG18)—Offset 224h" on page 6373	00000000h
228–22Bh	4	"reg_SEC2ISH_MSG19_type (SEC2ISH_MSG19)—Offset 228h" on page 6373	00000000h
22C–22Fh	4	"reg_SEC2ISH_MSG20_type (SEC2ISH_MSG20)—Offset 22Ch" on page 6373	00000000h
230–233h	4	"reg_SEC2ISH_MSG21_type (SEC2ISH_MSG21)—Offset 230h" on page 6374	00000000h
234–237h	4	"reg_SEC2ISH_MSG22_type (SEC2ISH_MSG22)—Offset 234h" on page 6374	00000000h
238–23Bh	4	"reg_SEC2ISH_MSG23_type (SEC2ISH_MSG23)—Offset 238h" on page 6375	00000000h
23C–23Fh	4	"reg_SEC2ISH_MSG24_type (SEC2ISH_MSG24)—Offset 23Ch" on page 6375	00000000h
240–243h	4	"reg_SEC2ISH_MSG25_type (SEC2ISH_MSG25)—Offset 240h" on page 6376	00000000h
244–247h	4	"reg_SEC2ISH_MSG26_type (SEC2ISH_MSG26)—Offset 244h" on page 6376	00000000h
248–24Bh	4	"reg_SEC2ISH_MSG27_type (SEC2ISH_MSG27)—Offset 248h" on page 6376	00000000h
24C–24Fh	4	"reg_SEC2ISH_MSG28_type (SEC2ISH_MSG28)—Offset 24Ch" on page 6377	00000000h
250–253h	4	"reg_SEC2ISH_MSG29_type (SEC2ISH_MSG29)—Offset 250h" on page 6377	00000000h
254–257h	4	"reg_SEC2ISH_MSG30_type (SEC2ISH_MSG30)—Offset 254h" on page 6378	00000000h
258–25Bh	4	"reg_SEC2ISH_MSG31_type (SEC2ISH_MSG31)—Offset 258h" on page 6378	00000000h
25C–25Fh	4	"reg_SEC2ISH_MSG32_type (SEC2ISH_MSG32)—Offset 25Ch" on page 6379	00000000h
260–263h	4	"reg_ISH2PMC_MSG1_type (ISH2PMC_MSG1)—Offset 260h" on page 6379	00000000h
264–267h	4	"reg_ISH2PMC_MSG2_type (ISH2PMC_MSG2)—Offset 264h" on page 6379	00000000h
268–26Bh	4	"reg_ISH2PMC_MSG3_type (ISH2PMC_MSG3)—Offset 268h" on page 6380	00000000h
26C–26Fh	4	"reg_ISH2PMC_MSG4_type (ISH2PMC_MSG4)—Offset 26Ch" on page 6380	00000000h
270–273h	4	"reg_ISH2PMC_MSG5_type (ISH2PMC_MSG5)—Offset 270h" on page 6381	00000000h
274–277h	4	"reg_ISH2PMC_MSG6_type (ISH2PMC_MSG6)—Offset 274h" on page 6381	00000000h
278–27Bh	4	"reg_ISH2PMC_MSG7_type (ISH2PMC_MSG7)—Offset 278h" on page 6381	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
27C–27Fh	4	"reg_ISH2PMC_MSG8_type (ISH2PMC_MSG8)—Offset 27Ch" on page 6382	00000000h
280–283h	4	"reg_ISH2PMC_MSG9_type (ISH2PMC_MSG9)—Offset 280h" on page 6382	00000000h
284–287h	4	"reg_ISH2PMC_MSG10_type (ISH2PMC_MSG10)—Offset 284h" on page 6383	00000000h
288–28Bh	4	"reg_ISH2PMC_MSG11_type (ISH2PMC_MSG11)—Offset 288h" on page 6383	00000000h
28C–28Fh	4	"reg_ISH2PMC_MSG12_type (ISH2PMC_MSG12)—Offset 28Ch" on page 6383	00000000h
290–293h	4	"reg_ISH2PMC_MSG13_type (ISH2PMC_MSG13)—Offset 290h" on page 6384	00000000h
294–297h	4	"reg_ISH2PMC_MSG14_type (ISH2PMC_MSG14)—Offset 294h" on page 6384	00000000h
298–29Bh	4	"reg_ISH2PMC_MSG15_type (ISH2PMC_MSG15)—Offset 298h" on page 6385	00000000h
29C–29Fh	4	"reg_ISH2PMC_MSG16_type (ISH2PMC_MSG16)—Offset 29Ch" on page 6385	00000000h
2A0–2A3h	4	"reg_ISH2PMC_MSG17_type (ISH2PMC_MSG17)—Offset 2A0h" on page 6386	00000000h
2A4–2A7h	4	"reg_ISH2PMC_MSG18_type (ISH2PMC_MSG18)—Offset 2A4h" on page 6386	00000000h
2A8–2ABh	4	"reg_ISH2PMC_MSG19_type (ISH2PMC_MSG19)—Offset 2A8h" on page 6386	00000000h
2AC–2AFh	4	"reg_ISH2PMC_MSG20_type (ISH2PMC_MSG20)—Offset 2ACh" on page 6387	00000000h
2B0–2B3h	4	"reg_ISH2PMC_MSG21_type (ISH2PMC_MSG21)—Offset 2B0h" on page 6387	00000000h
2B4–2B7h	4	"reg_ISH2PMC_MSG22_type (ISH2PMC_MSG22)—Offset 2B4h" on page 6388	00000000h
2B8–2BBh	4	"reg_ISH2PMC_MSG23_type (ISH2PMC_MSG23)—Offset 2B8h" on page 6388	00000000h
2BC–2BFh	4	"reg_ISH2PMC_MSG24_type (ISH2PMC_MSG24)—Offset 2BCh" on page 6389	00000000h
2C0–2C3h	4	"reg_ISH2PMC_MSG25_type (ISH2PMC_MSG25)—Offset 2C0h" on page 6389	00000000h
2C4–2C7h	4	"reg_ISH2PMC_MSG26_type (ISH2PMC_MSG26)—Offset 2C4h" on page 6389	00000000h
2C8–2CBh	4	"reg_ISH2PMC_MSG27_type (ISH2PMC_MSG27)—Offset 2C8h" on page 6390	00000000h
2CC–2CFh	4	"reg_ISH2PMC_MSG28_type (ISH2PMC_MSG28)—Offset 2CCh" on page 6390	00000000h
2D0–2D3h	4	"reg_ISH2PMC_MSG29_type (ISH2PMC_MSG29)—Offset 2D0h" on page 6391	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2D4–2D7h	4	"reg_ISH2PMC_MSG30_type (ISH2PMC_MSG30)—Offset 2D4h" on page 6391	00000000h
2D8–2DBh	4	"reg_ISH2PMC_MSG31_type (ISH2PMC_MSG31)—Offset 2D8h" on page 6392	00000000h
2DC–2DFh	4	"reg_ISH2PMC_MSG32_type (ISH2PMC_MSG32)—Offset 2DCh" on page 6392	00000000h
2E0–2E3h	4	"reg_PMC2ISH_MSG1_type (PMC2ISH_MSG1)—Offset 2E0h" on page 6392	00000000h
2E4–2E7h	4	"reg_PMC2ISH_MSG2_type (PMC2ISH_MSG2)—Offset 2E4h" on page 6393	00000000h
2E8–2EBh	4	"reg_PMC2ISH_MSG3_type (PMC2ISH_MSG3)—Offset 2E8h" on page 6393	00000000h
2EC–2EFh	4	"reg_PMC2ISH_MSG4_type (PMC2ISH_MSG4)—Offset 2ECh" on page 6394	00000000h
2F0–2F3h	4	"reg_PMC2ISH_MSG5_type (PMC2ISH_MSG5)—Offset 2F0h" on page 6394	00000000h
2F4–2F7h	4	"reg_PMC2ISH_MSG6_type (PMC2ISH_MSG6)—Offset 2F4h" on page 6394	00000000h
2F8–2FBh	4	"reg_PMC2ISH_MSG7_type (PMC2ISH_MSG7)—Offset 2F8h" on page 6395	00000000h
2FC–2FFh	4	"reg_PMC2ISH_MSG8_type (PMC2ISH_MSG8)—Offset 2FCh" on page 6395	00000000h
300–303h	4	"reg_PMC2ISH_MSG9_type (PMC2ISH_MSG9)—Offset 300h" on page 6396	00000000h
304–307h	4	"reg_PMC2ISH_MSG10_type (PMC2ISH_MSG10)—Offset 304h" on page 6396	00000000h
308–30Bh	4	"reg_PMC2ISH_MSG11_type (PMC2ISH_MSG11)—Offset 308h" on page 6396	00000000h
30C–30Fh	4	"reg_PMC2ISH_MSG12_type (PMC2ISH_MSG12)—Offset 30Ch" on page 6397	00000000h
310–313h	4	"reg_PMC2ISH_MSG13_type (PMC2ISH_MSG13)—Offset 310h" on page 6397	00000000h
314–317h	4	"reg_PMC2ISH_MSG14_type (PMC2ISH_MSG14)—Offset 314h" on page 6398	00000000h
318–31Bh	4	"reg_PMC2ISH_MSG15_type (PMC2ISH_MSG15)—Offset 318h" on page 6398	00000000h
31C–31Fh	4	"reg_PMC2ISH_MSG16_type (PMC2ISH_MSG16)—Offset 31Ch" on page 6399	00000000h
320–323h	4	"reg_PMC2ISH_MSG17_type (PMC2ISH_MSG17)—Offset 320h" on page 6399	00000000h
324–327h	4	"reg_PMC2ISH_MSG18_type (PMC2ISH_MSG18)—Offset 324h" on page 6399	00000000h
328–32Bh	4	"reg_PMC2ISH_MSG19_type (PMC2ISH_MSG19)—Offset 328h" on page 6400	00000000h



Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
32C–32Fh	4	"reg_PMC2ISH_MSG20_type (PMC2ISH_MSG20)—Offset 32Ch" on page 6400	00000000h
330–333h	4	"reg_PMC2ISH_MSG21_type (PMC2ISH_MSG21)—Offset 330h" on page 6401	00000000h
334–337h	4	"reg_PMC2ISH_MSG22_type (PMC2ISH_MSG22)—Offset 334h" on page 6401	00000000h
338–33Bh	4	"reg_PMC2ISH_MSG23_type (PMC2ISH_MSG23)—Offset 338h" on page 6402	00000000h
33C–33Fh	4	"reg_PMC2ISH_MSG24_type (PMC2ISH_MSG24)—Offset 33Ch" on page 6402	00000000h
340–343h	4	"reg_PMC2ISH_MSG25_type (PMC2ISH_MSG25)—Offset 340h" on page 6402	00000000h
344–347h	4	"reg_PMC2ISH_MSG26_type (PMC2ISH_MSG26)—Offset 344h" on page 6403	00000000h
348–34Bh	4	"reg_PMC2ISH_MSG27_type (PMC2ISH_MSG27)—Offset 348h" on page 6403	00000000h
34C–34Fh	4	"reg_PMC2ISH_MSG28_type (PMC2ISH_MSG28)—Offset 34Ch" on page 6404	00000000h
350–353h	4	"reg_PMC2ISH_MSG29_type (PMC2ISH_MSG29)—Offset 350h" on page 6404	00000000h
354–357h	4	"reg_PMC2ISH_MSG30_type (PMC2ISH_MSG30)—Offset 354h" on page 6405	00000000h
358–35Bh	4	"reg_PMC2ISH_MSG31_type (PMC2ISH_MSG31)—Offset 358h" on page 6405	00000000h
35C–35Fh	4	"reg_PMC2ISH_MSG32_type (PMC2ISH_MSG32)—Offset 35Ch" on page 6405	00000000h
360–363h	4	"reg_REMAP0_type (REMAP0)—Offset 360h" on page 6406	00000000h
364–367h	4	"reg_REMAP1_type (REMAP1)—Offset 364h" on page 6406	00000000h
368–36Bh	4	"reg_REMAP2_type (REMAP2)—Offset 368h" on page 6407	00000000h
36C–36Fh	4	"reg_REMAP3_type (REMAP3)—Offset 36Ch" on page 6407	00000000h
370–373h	4	"reg_REMAP4_type (REMAP4)—Offset 370h" on page 6407	00000000h
374–377h	4	"reg_REMAP5_type (REMAP5)—Offset 374h" on page 6408	00000000h
378–37Bh	4	"reg_ISH_IPC_BUSY_CLEAR_type (ISH_IPC_BUSY_CLEAR)—Offset 378h" on page 6408	00000000h
37C–37Fh	4	"reg_ISH_FUSE_type (ISH_FUSE)—Offset 37Ch" on page 6409	00000000h
380–383h	4	"reg_UMA_RANGE_LOWER_0_type (UMA_RANGE_LOWER_0)—Offset 380h" on page 6410	FFFFF000h
384–387h	4	"reg_UMA_RANGE_LOWER_1_type (UMA_RANGE_LOWER_1)—Offset 384h" on page 6410	00000000h
388–38Bh	4	"reg_UMA_RANGE_UPPER_0_type (UMA_RANGE_UPPER_0)—Offset 388h" on page 6411	FFFFF000h
38C–38Fh	4	"reg_UMA_RANGE_UPPER_1_type (UMA_RANGE_UPPER_1)—Offset 38Ch" on page 6412	00000000h



12.2.1 reg_PISR_type (PISR)—Offset 0h

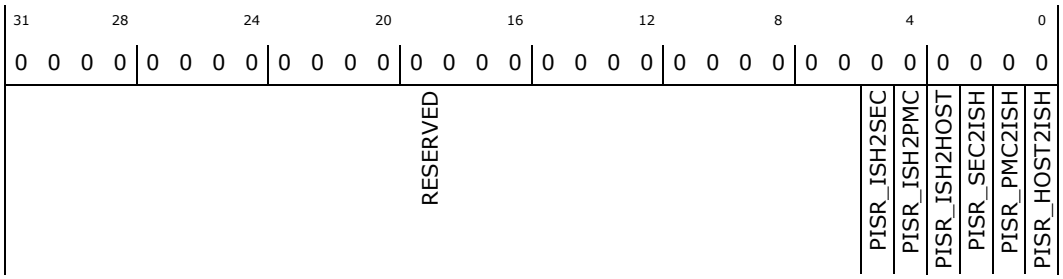
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**RESERVED:** ish_clk
5	0x0 RO	**PISR_ISH2SEC:** ish_clk
4	0x0 RO	**PISR_ISH2PMC:** ish_clk
3	0x0 RO	**PISR_ISH2HOST:** ish_clk
2	0x0 RO	**PISR_SEC2ISH:** ish_clk
1	0x0 RO	**PISR_PMC2ISH:** ish_clk
0	0x0 RO	**PISR_HOST2ISH:** ish_clk

12.2.2 reg_PIMR_type (PIMR)—Offset 4h

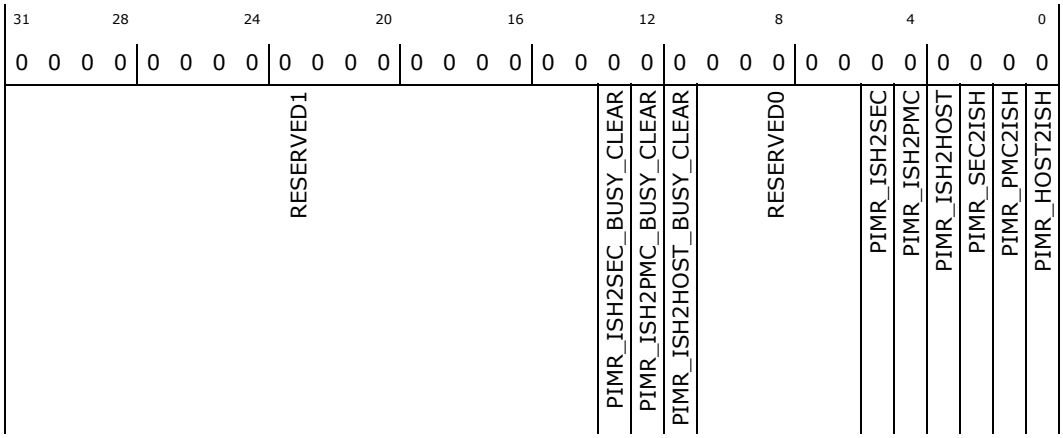
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**RESERVED1:** ish_clk
13	0x0 RW	**PIMR_ISH2SEC_BUSY_CLEAR:** ish_clk
12	0x0 RW	**PIMR_ISH2PMC_BUSY_CLEAR:** ish_clk
11	0x0 RW	**PIMR_ISH2HOST_BUSY_CLEAR:** ish_clk
10:6	0x0 RO	**RESERVED0:** ish_clk
5	0x0 RW	**PIMR_ISH2SEC:** ish_clk
4	0x0 RW	**PIMR_ISH2PMC:** ish_clk
3	0x0 RW	**PIMR_ISH2HOST:** ish_clk
2	0x0 RW	**PIMR_SEC2ISH:** ish_clk
1	0x0 RW	**PIMR_PMC2ISH:** ish_clk
0	0x0 RW	**PIMR_HOST2ISH:** ish_clk

12.2.3 reg_RESERVED0_type (RESERVED0)—Offset 8h

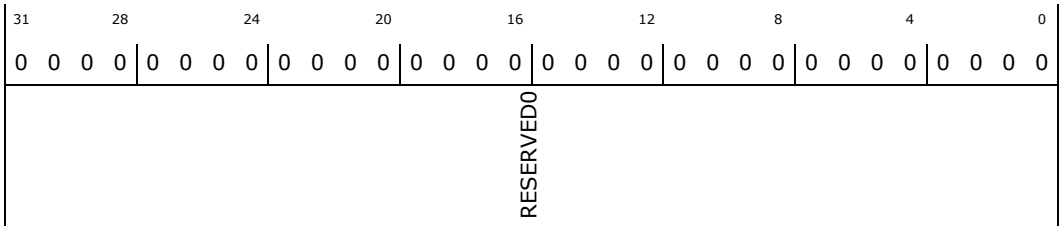
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED0:** ish_clk

12.2.4 reg_RESERVED1_type (RESERVED1)—Offset Ch

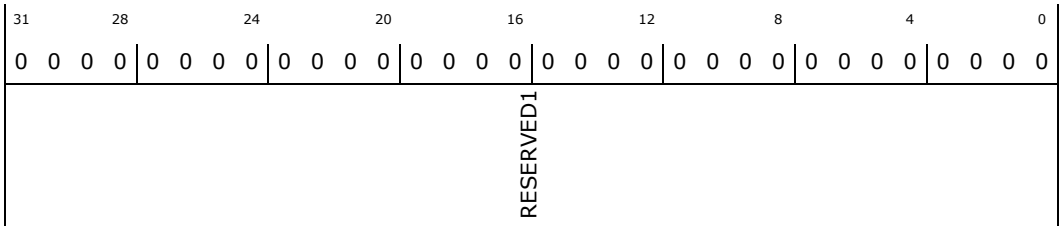
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED1:** ish_clk

12.2.5 reg_RESERVED2_type (RESERVED2)—Offset 10h

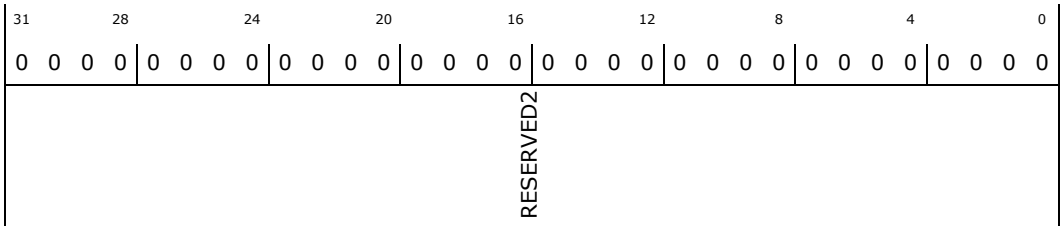
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED2:** ish_clk

12.2.6 reg_RESERVED3_type (RESERVED3)—Offset 14h

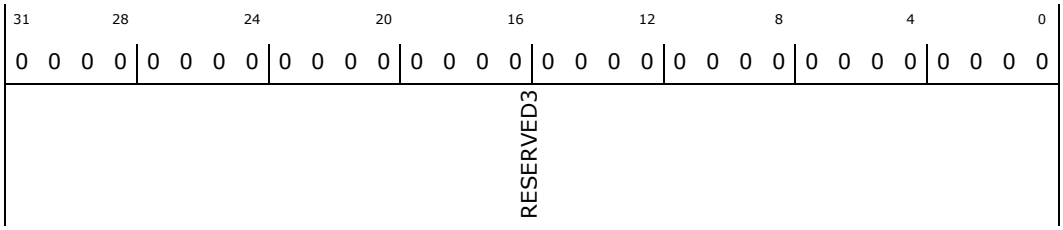
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED3:** ish_clk

12.2.7 reg_RESERVED4_type (RESERVED4)—Offset 18h

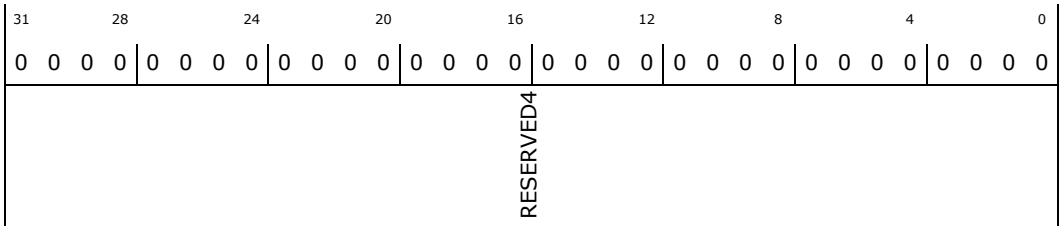
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 18h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED4:** ish_clk

12.2.8 reg_RESERVED5_type (RESERVED5)—Offset 1Ch

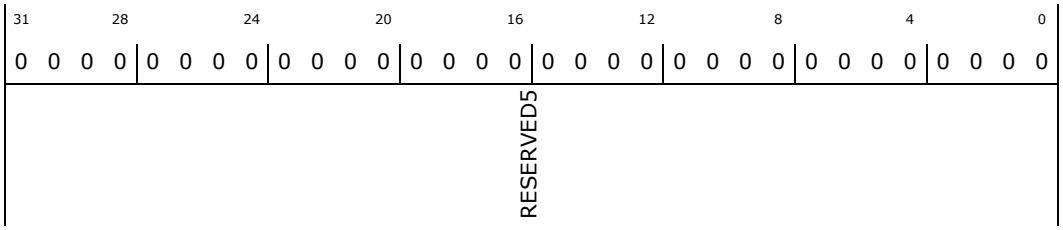
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED5:** ish_clk

12.2.9 reg_RESERVED6_type (RESERVED6)—Offset 20h

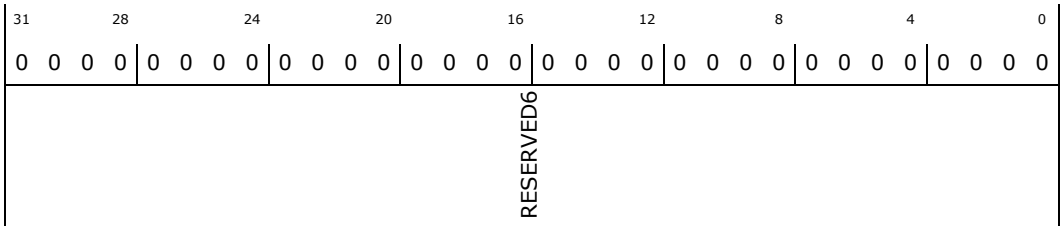
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 20h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED6:** ish_clk

12.2.10 reg_RESERVED7_type (RESERVED7)—Offset 24h

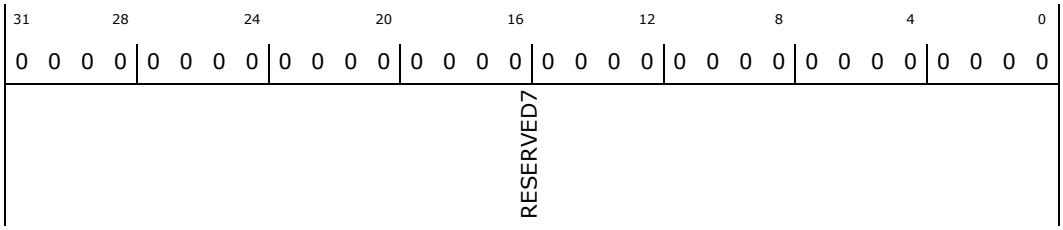
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 24h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED7:** ish_clk

12.2.11 reg_RESERVED8_type (RESERVED8)—Offset 28h

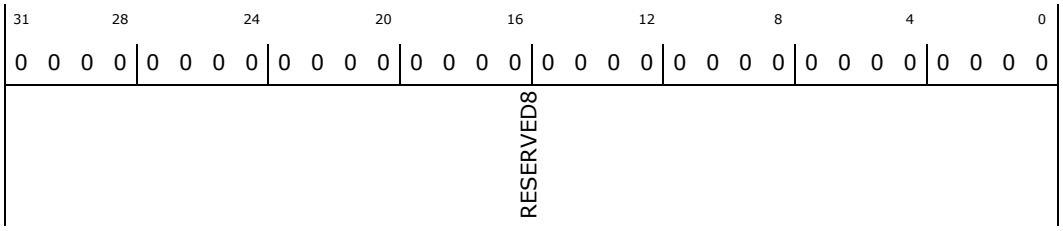
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 28h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED8:** ish_clk

12.2.12 reg_RESERVED9_type (RESERVED9)—Offset 2Ch

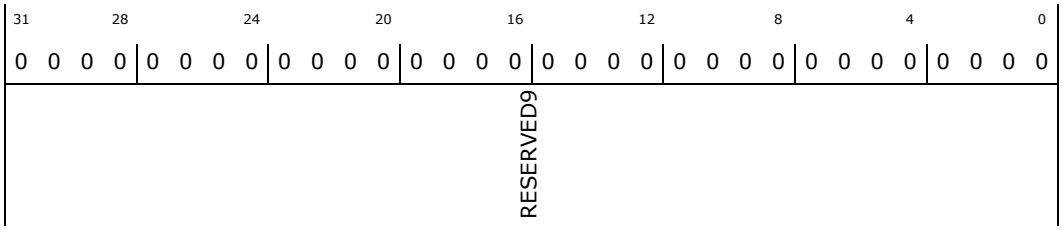
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED9:** ish_clk

12.2.13 reg_RESERVED10_type (RESERVED10)—Offset 30h

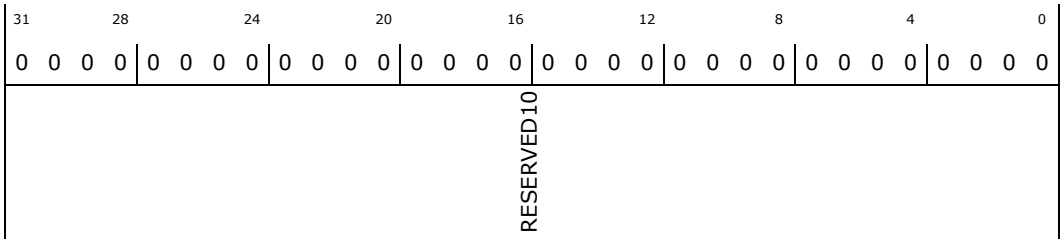
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED10:** ish_clk

12.2.14 reg_ISH_HOST_FWSTS_type (ISH_HOST_FWSTS)—Offset 34h

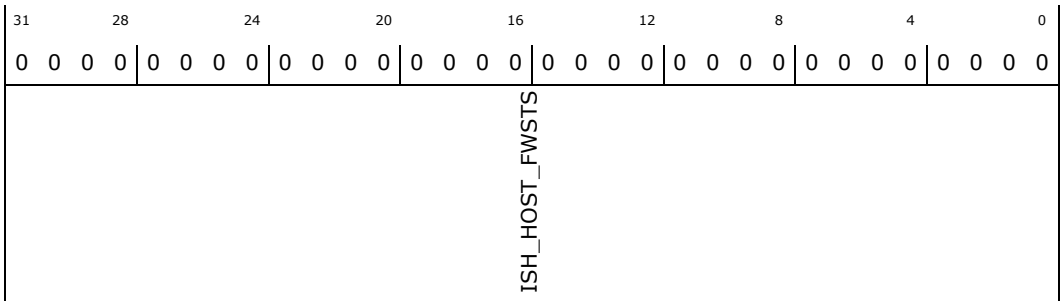
ISH Host firmware status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 34h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**ISH_HOST_FWSTS:** ish_clk

12.2.15 reg_HOST_COMM_type (HOST_COMM)—Offset 38h

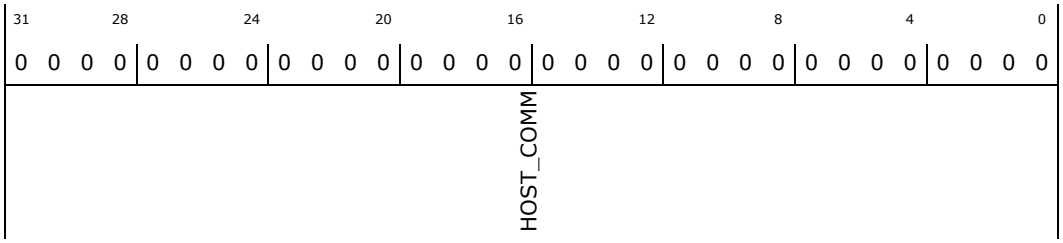
Host communication register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 38h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**HOST_COMM:** ish_clk

12.2.16 reg_ISH_SEC_FWSTS_type (ISH_SEC_FWSTS)—Offset 3Ch

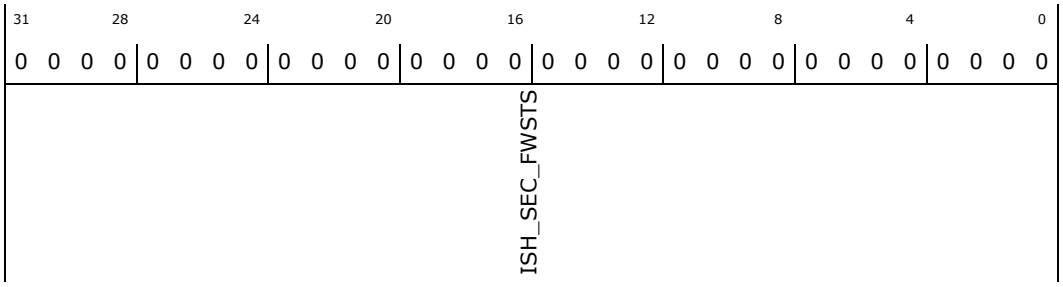
ISH SEC firmware status

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 3Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**ISH_SEC_FWSTS:** ish_clk

12.2.17 reg_SEC_COMM_type (SEC_COMM)—Offset 40h

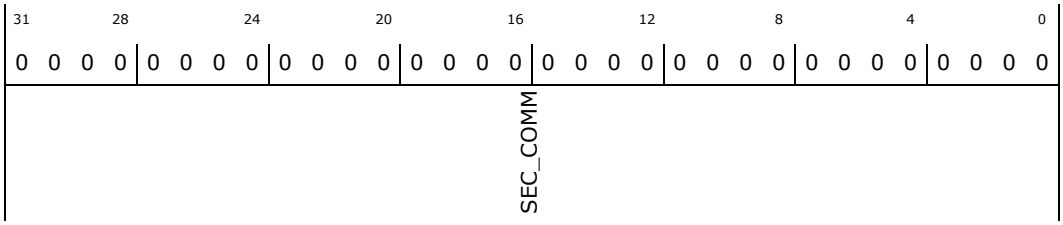
SEC communication register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 40h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SEC_COMM:** ish_clk

12.2.18 reg_ISH_RST_type (ISH_RST)—Offset 44h

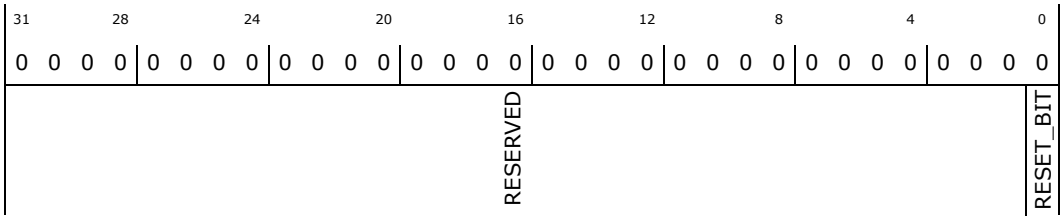
Reset register used to reset minuteIA

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 44h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RESERVED:** ish_clk
0	0x0 RW	**RESET_BIT:** ish_clk

12.2.19 reg_HOST2ISH_DOORBELL_type (HOST2ISH_DOORBELL)—Offset 48h

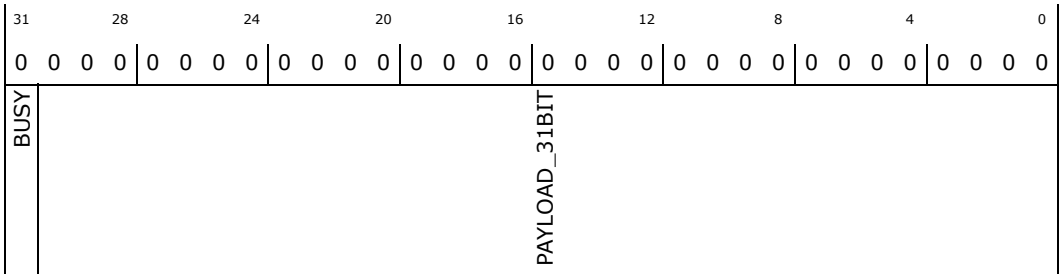
When this bit is cleared, the ISH CPU is Ready to accept a new message

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 48h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**BUSY:** ish_clk
30:0	0x0 RW	**PAYLOAD_31BIT:** ish_clk

12.2.20 reg_PMC2ISH_DOORBELL_type (PMC2ISH_DOORBELL)—Offset 4Ch

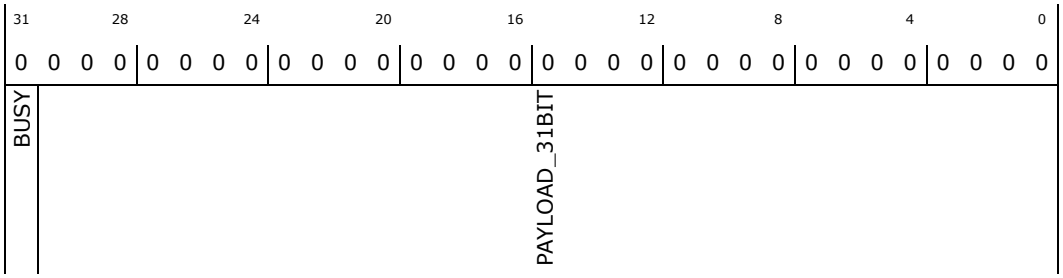
When this bit is cleared, the ISH CPU is Ready to accept a new message

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**BUSY:** ish_clk
30:0	0x0 RW	**PAYLOAD_31BIT:** ish_clk

12.2.21 reg_SEC2ISH_DOORBELL_type (SEC2ISH_DOORBELL)—Offset 50h

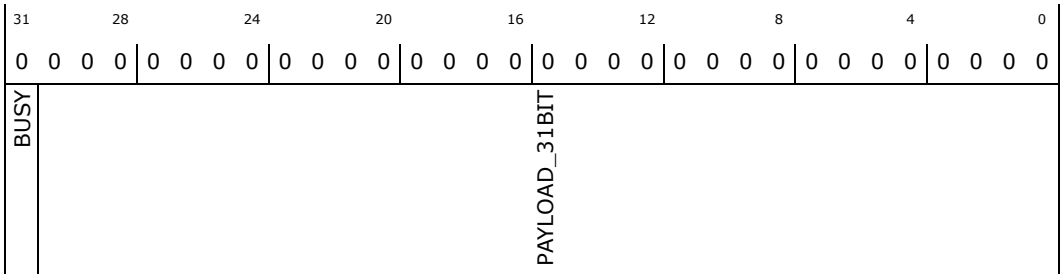
When this bit is cleared, the ISH CPU is Ready to accept a new message

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 50h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**BUSY:** ish_clk
30:0	0x0 RW	**PAYLOAD_31BIT:** ish_clk

12.2.22 reg_ISH2HOST_DOORBELL_type (ISH2HOST_DOORBELL)—Offset 54h

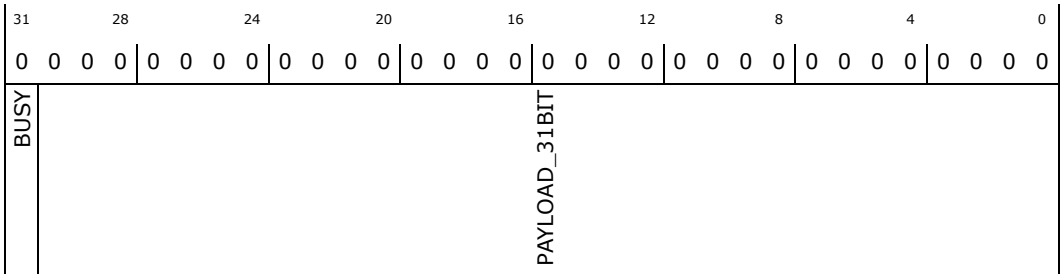
When this bit is cleared, the HOST CPU is Ready to accept a new message

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 54h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**BUSY:** ish_clk
30:0	0x0 RW	**PAYLOAD_31BIT:** ish_clk

12.2.23 reg_ISH2PMC_DOORBELL_type (ISH2PMC_DOORBELL)—Offset 58h

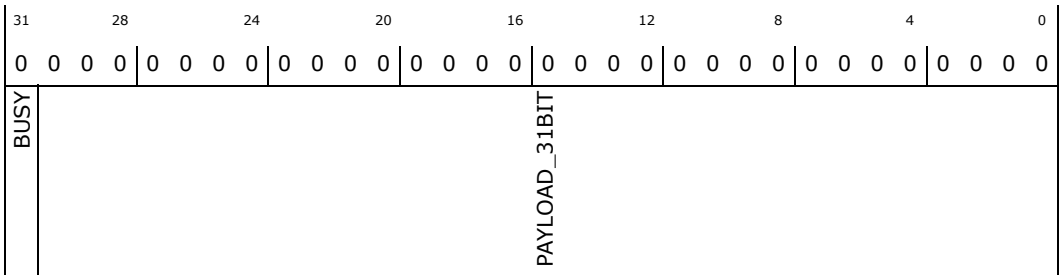
When this bit is cleared, the PMC CPU is Ready to accept a new message

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 58h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**BUSY:** ish_clk
30:0	0x0 RW	**PAYLOAD_31BIT:** ish_clk

12.2.24 reg_ISH2SEC_DOORBELL_type (ISH2SEC_DOORBELL)—Offset 5Ch

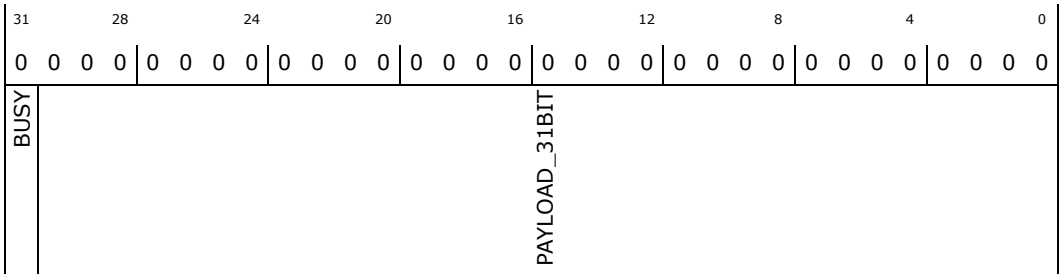
When this bit is cleared, the SEC CPU is Ready to accept a new message

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 5Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**BUSY:** ish_clk

Bit Range	Default & Access	Field Name (ID): Description
30:0	0x0 RW	**PAYLOAD_31BIT:** ish_clk

12.2.25 reg_ISH2HOST_MSG1_type (ISH2HOST_MSG1)—Offset 60h

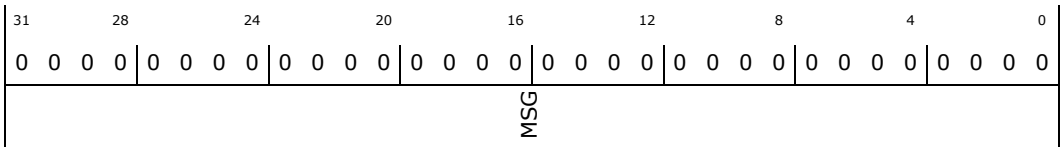
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 60h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.26 reg_ISH2HOST_MSG2_type (ISH2HOST_MSG2)—Offset 64h

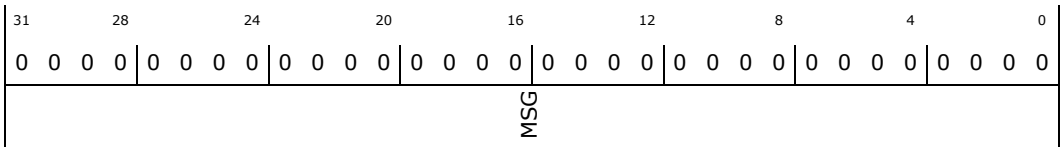
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 64h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.27 reg_ISH2HOST_MSG3_type (ISH2HOST_MSG3)—Offset 68h

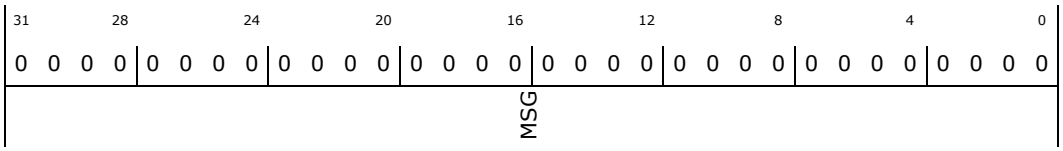
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 68h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.28 reg_ISH2HOST_MSG4_type (ISH2HOST_MSG4)—Offset 6Ch

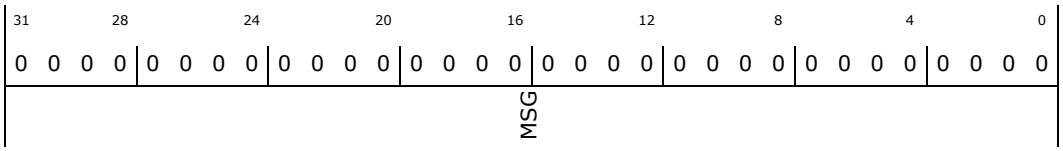
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 6Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.29 reg_ISH2HOST_MSG5_type (ISH2HOST_MSG5)—Offset 70h

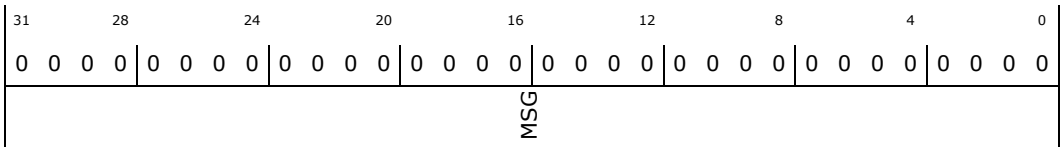
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 70h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.30 reg_ISH2HOST_MSG6_type (ISH2HOST_MSG6)—Offset 74h

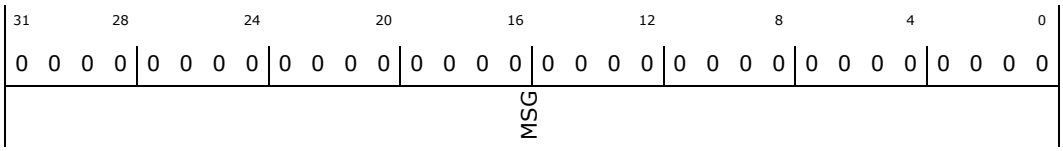
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 74h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.31 reg_ISH2HOST_MSG7_type (ISH2HOST_MSG7)—Offset 78h

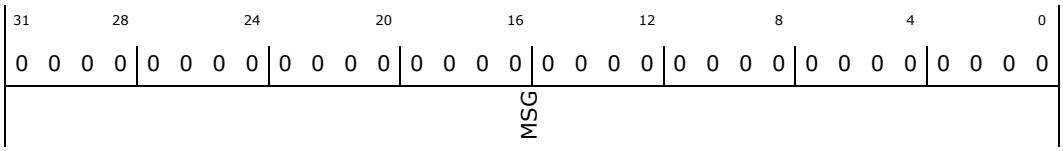
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 78h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.32 reg_ISH2HOST_MSG8_type (ISH2HOST_MSG8)—Offset 7Ch

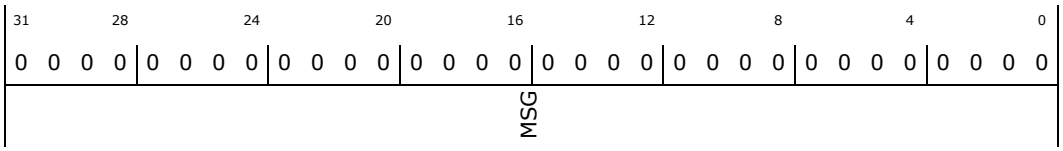
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 7Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.33 reg_ISH2HOST_MSG9_type (ISH2HOST_MSG9)—Offset 80h

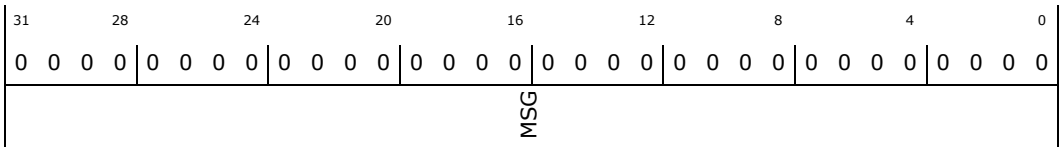
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 80h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.34 reg_ISH2HOST_MSG10_type (ISH2HOST_MSG10)—Offset 84h

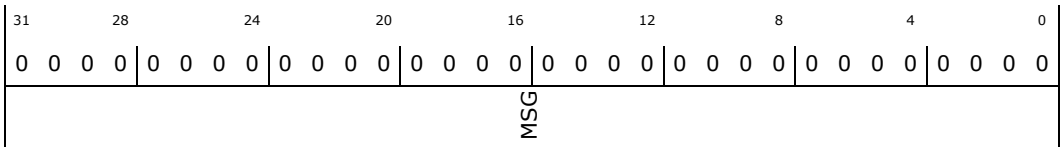
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 84h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.35 reg_ISH2HOST_MSG11_type (ISH2HOST_MSG11)—Offset 88h

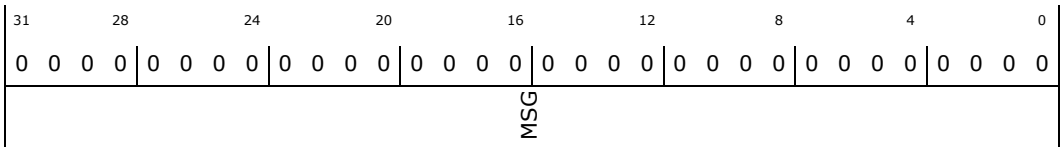
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 88h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.36 reg_ISH2HOST_MSG12_type (ISH2HOST_MSG12)—Offset 8Ch

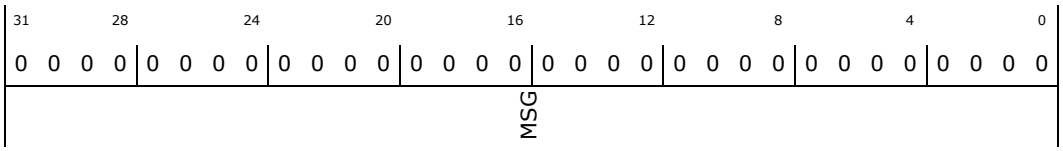
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 8Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.37 reg_ISH2HOST_MSG13_type (ISH2HOST_MSG13)—Offset 90h

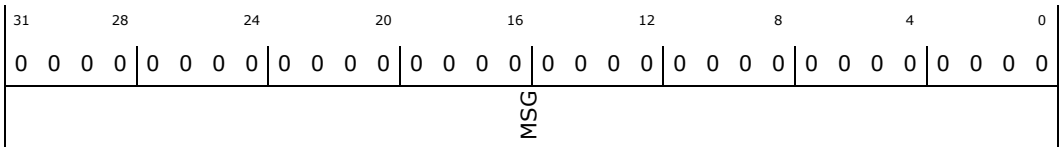
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 90h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.38 reg_ISH2HOST_MSG14_type (ISH2HOST_MSG14)—Offset 94h

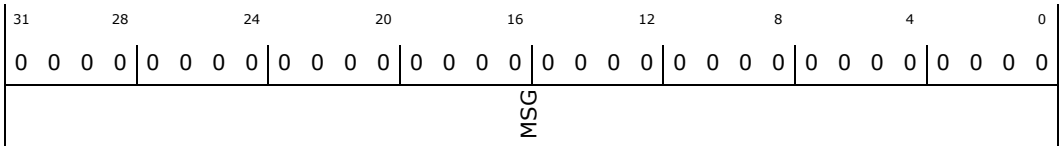
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 94h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.39 reg_ISH2HOST_MSG15_type (ISH2HOST_MSG15)—Offset 98h

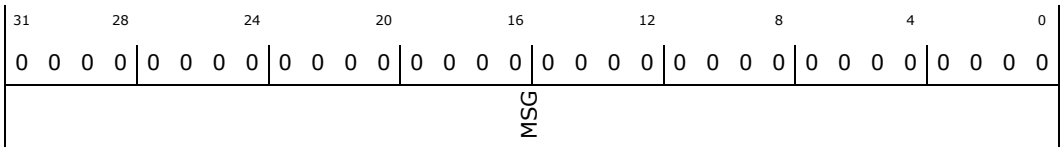
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 98h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.40 reg_ISH2HOST_MSG16_type (ISH2HOST_MSG16)—Offset 9Ch

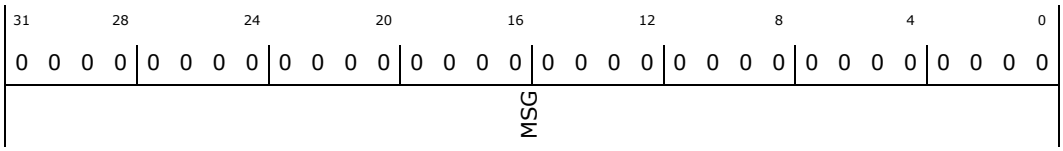
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 9Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.41 reg_ISH2HOST_MSG17_type (ISH2HOST_MSG17)—Offset A0h

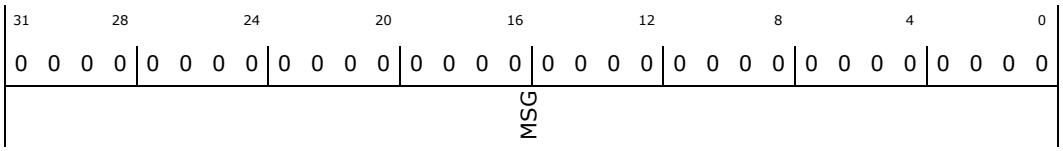
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.42 reg_ISH2HOST_MSG18_type (ISH2HOST_MSG18)—Offset A4h

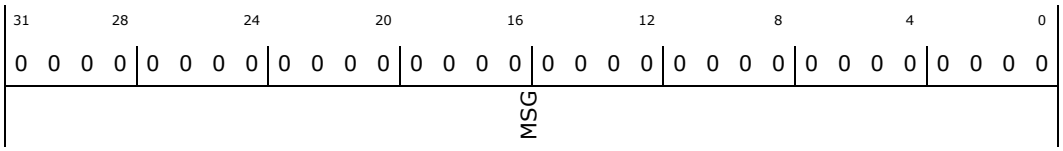
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.43 reg_ISH2HOST_MSG19_type (ISH2HOST_MSG19)—Offset A8h

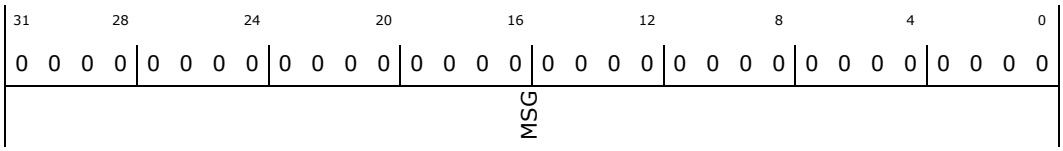
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.44 reg_ISH2HOST_MSG20_type (ISH2HOST_MSG20)—Offset ACh

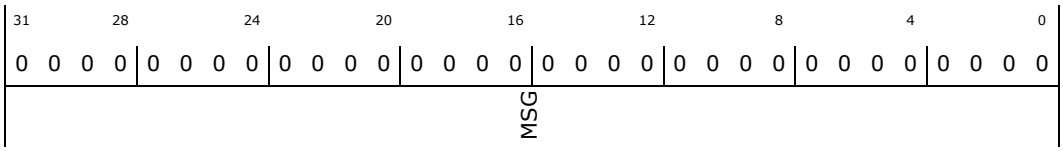
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.45 reg_ISH2HOST_MSG21_type (ISH2HOST_MSG21)—Offset B0h

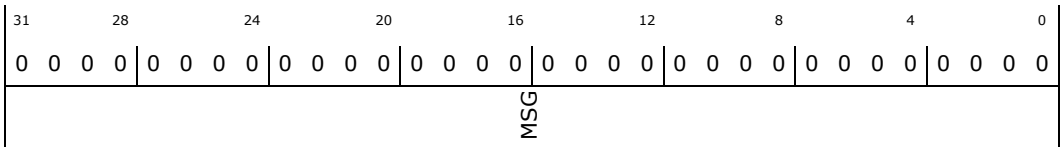
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.46 reg_ISH2HOST_MSG22_type (ISH2HOST_MSG22)—Offset B4h

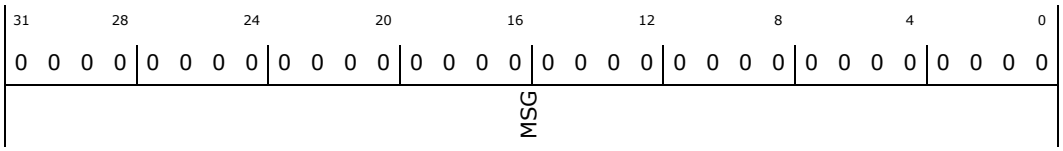
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + B4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.47 reg_ISH2HOST_MSG23_type (ISH2HOST_MSG23)—Offset B8h

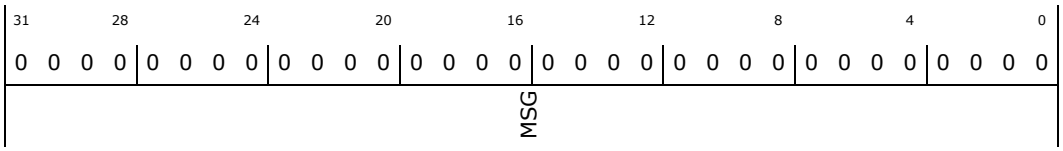
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.48 reg_ISH2HOST_MSG24_type (ISH2HOST_MSG24)—Offset BCh

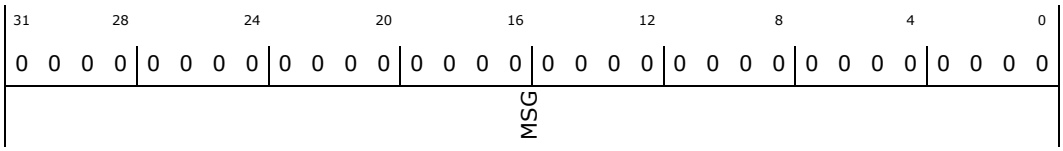
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + BCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.49 reg_ISH2HOST_MSG25_type (ISH2HOST_MSG25)—Offset C0h

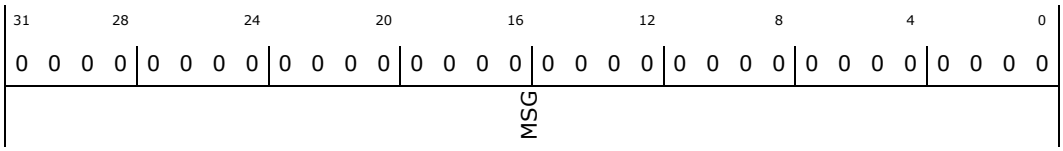
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.50 reg_ISH2HOST_MSG26_type (ISH2HOST_MSG26)—Offset C4h

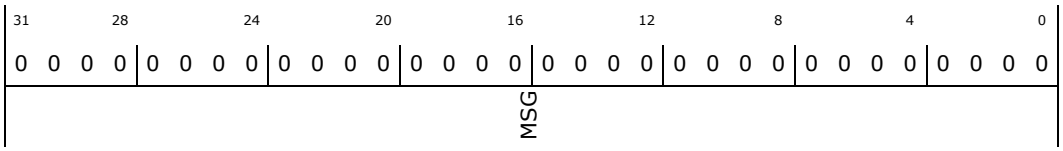
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + C4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.51 reg_ISH2HOST_MSG27_type (ISH2HOST_MSG27)—Offset C8h

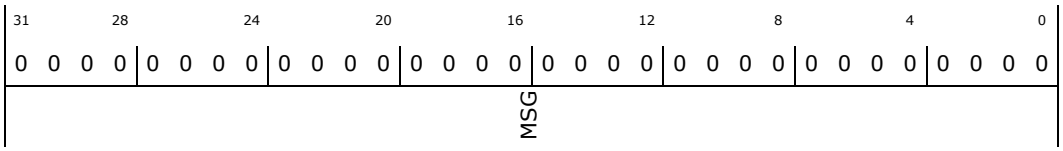
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + C8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.52 reg_ISH2HOST_MSG28_type (ISH2HOST_MSG28)—Offset CCh

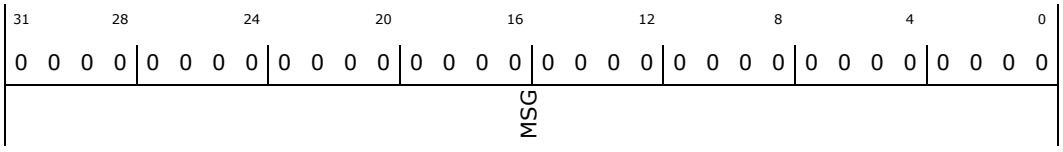
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + CCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.53 reg_ISH2HOST_MSG29_type (ISH2HOST_MSG29)—Offset D0h

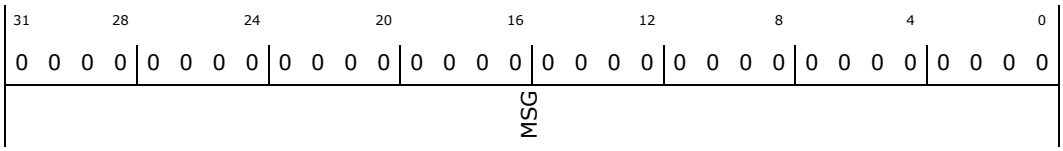
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.54 reg_ISH2HOST_MSG30_type (ISH2HOST_MSG30)—Offset D4h

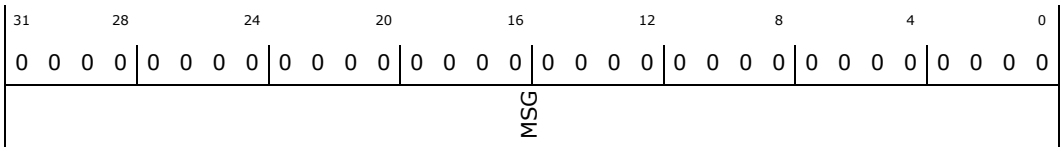
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + D4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.55 reg_ISH2HOST_MSG31_type (ISH2HOST_MSG31)—Offset D8h

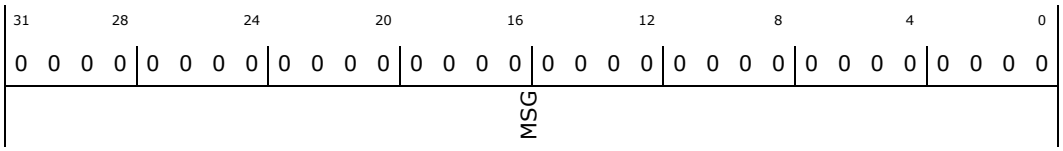
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + D8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.56 reg_ISH2HOST_MSG32_type (ISH2HOST_MSG32)—Offset DCh

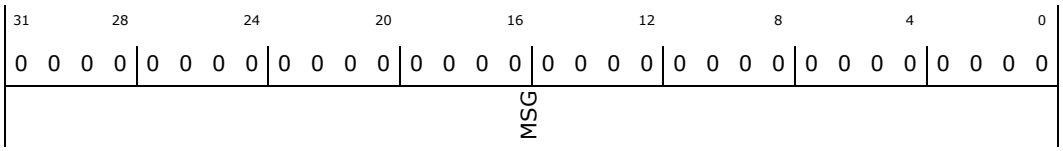
Message from ISH to HOST

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + DCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.57 reg_HOST2ISH_MSG1_type (HOST2ISH_MSG1)—Offset E0h

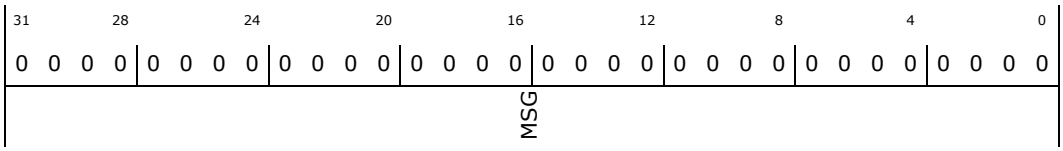
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + E0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.58 reg_HOST2ISH_MSG2_type (HOST2ISH_MSG2)—Offset E4h

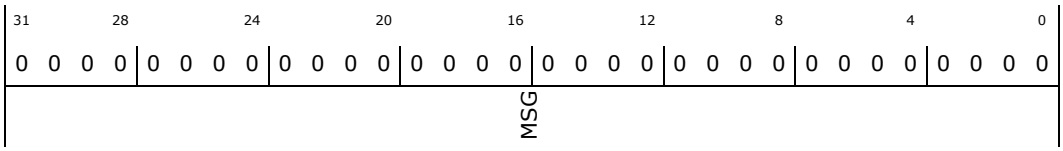
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + E4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.59 reg_HOST2ISH_MSG3_type (HOST2ISH_MSG3)—Offset E8h

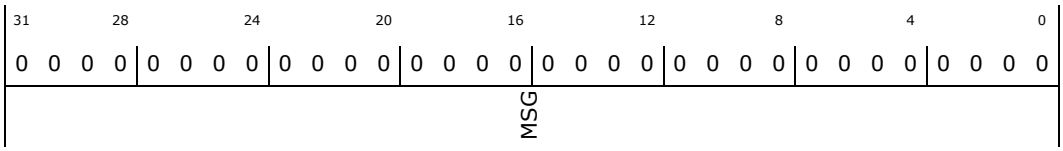
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + E8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.60 reg_HOST2ISH_MSG4_type (HOST2ISH_MSG4)—Offset ECh

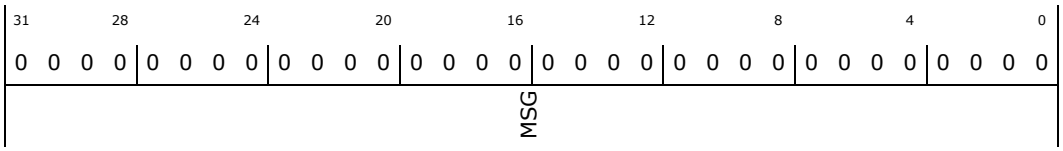
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + ECh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.61 reg_HOST2ISH_MSG5_type (HOST2ISH_MSG5)—Offset F0h

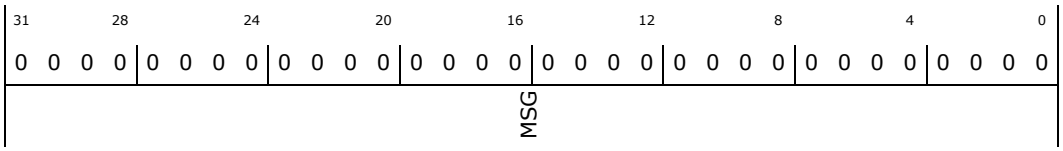
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + F0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.62 reg_HOST2ISH_MSG6_type (HOST2ISH_MSG6)—Offset F4h

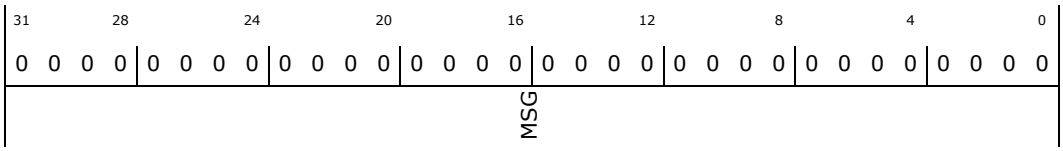
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + F4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.63 reg_HOST2ISH_MSG7_type (HOST2ISH_MSG7)—Offset F8h

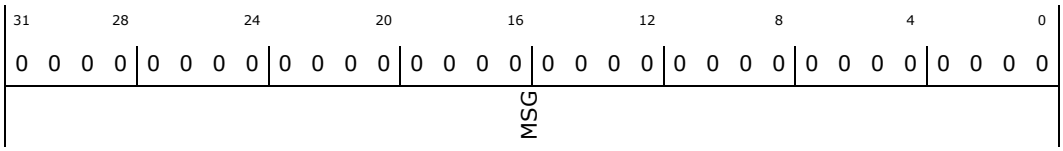
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.64 reg_HOST2ISH_MSG8_type (HOST2ISH_MSG8)—Offset FCh

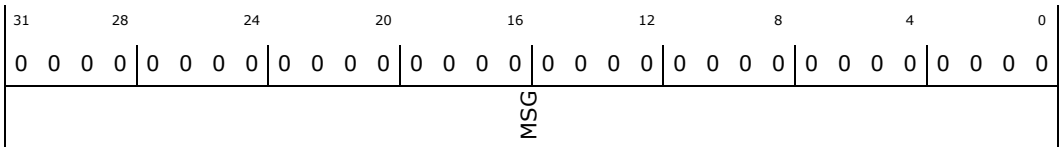
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + FCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.65 reg_HOST2ISH_MSG9_type (HOST2ISH_MSG9)—Offset 100h

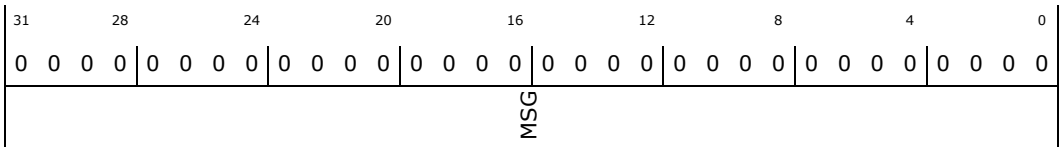
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 100h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.66 reg_HOST2ISH_MSG10_type (HOST2ISH_MSG10)—Offset 104h

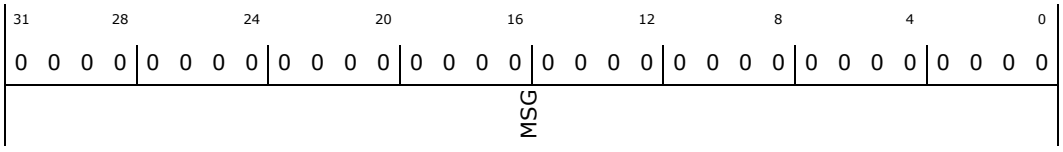
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 104h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.67 reg_HOST2ISH_MSG11_type (HOST2ISH_MSG11)—Offset 108h

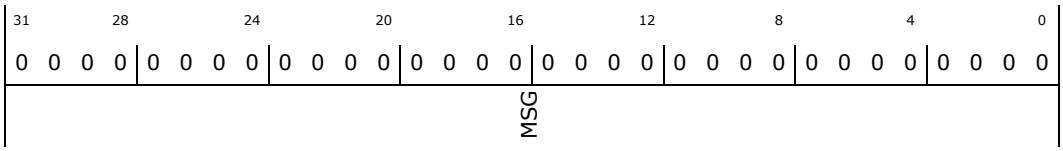
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 108h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.68 reg_HOST2ISH_MSG12_type (HOST2ISH_MSG12)—Offset 10Ch

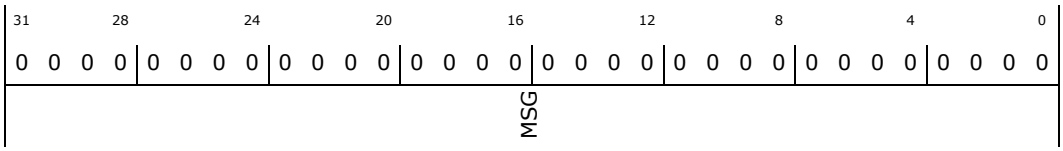
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 10Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.69 reg_HOST2ISH_MSG13_type (HOST2ISH_MSG13)—Offset 110h

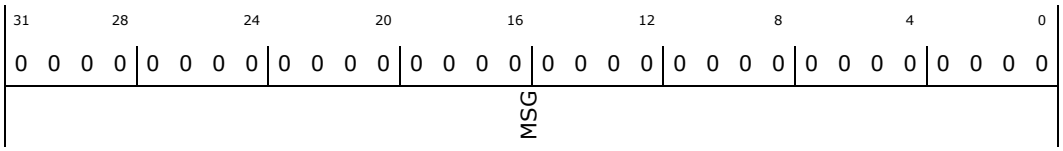
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 110h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.70 reg_HOST2ISH_MSG14_type (HOST2ISH_MSG14)—Offset 114h

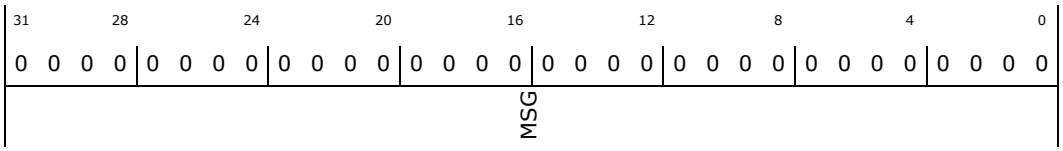
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 114h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.71 reg_HOST2ISH_MSG15_type (HOST2ISH_MSG15)—Offset 118h

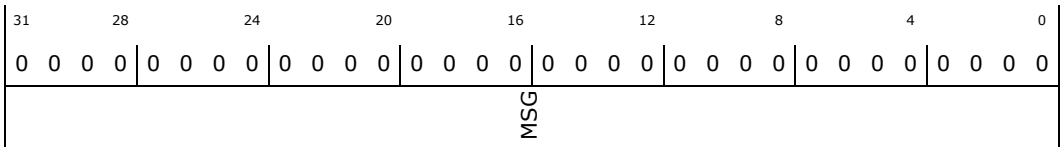
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 118h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.72 reg_HOST2ISH_MSG16_type (HOST2ISH_MSG16)—Offset 11Ch

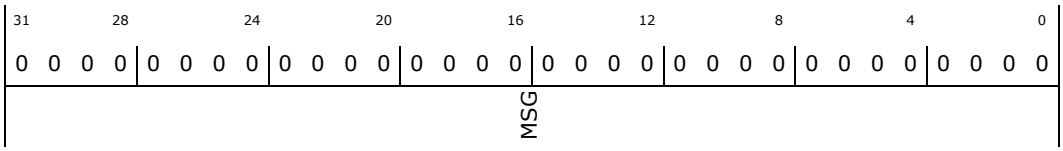
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 11Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.73 reg_HOST2ISH_MSG17_type (HOST2ISH_MSG17)—Offset 120h

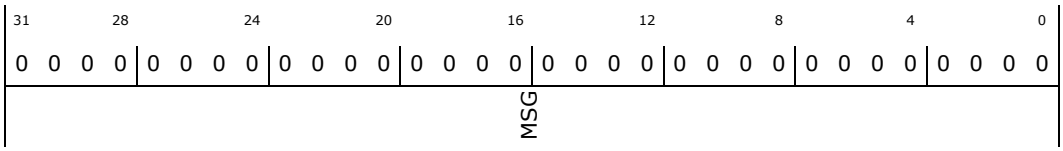
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 120h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.74 reg_HOST2ISH_MSG18_type (HOST2ISH_MSG18)—Offset 124h

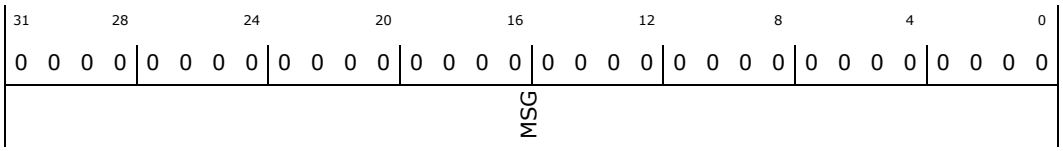
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 124h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.75 reg_HOST2ISH_MSG19_type (HOST2ISH_MSG19)—Offset 128h

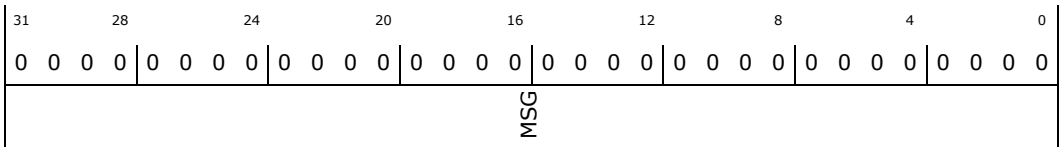
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 128h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.76 reg_HOST2ISH_MSG20_type (HOST2ISH_MSG20)—Offset 12Ch

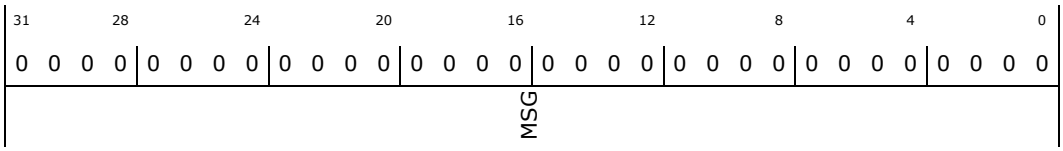
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 12Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.77 reg_HOST2ISH_MSG21_type (HOST2ISH_MSG21)—Offset 130h

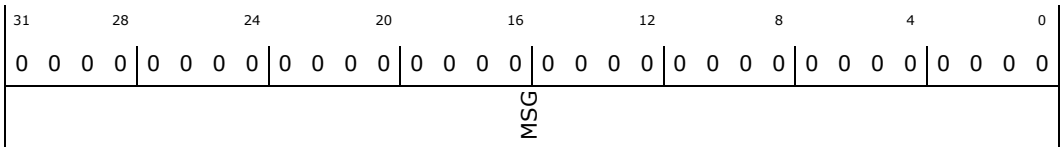
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 130h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.78 reg_HOST2ISH_MSG22_type (HOST2ISH_MSG22)—Offset 134h

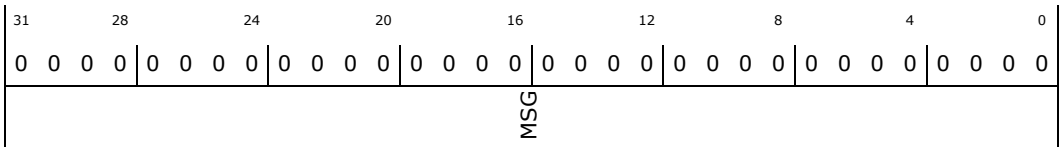
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 134h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.79 reg_HOST2ISH_MSG23_type (HOST2ISH_MSG23)—Offset 138h

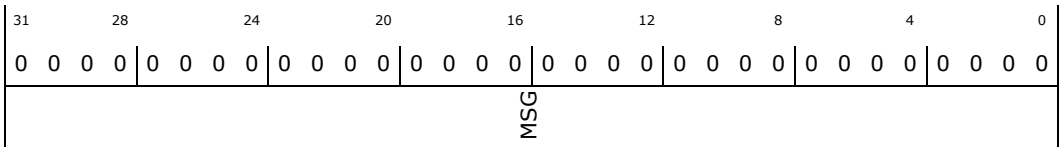
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 138h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.80 reg_HOST2ISH_MSG24_type (HOST2ISH_MSG24)—Offset 13Ch

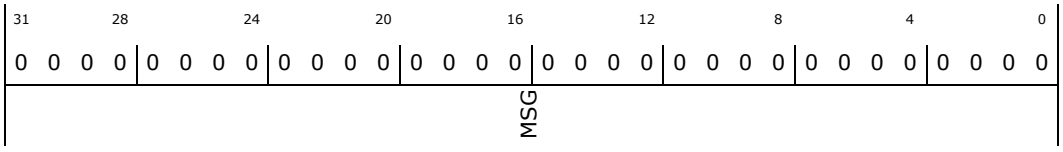
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 13Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.81 reg_HOST2ISH_MSG25_type (HOST2ISH_MSG25)—Offset 140h

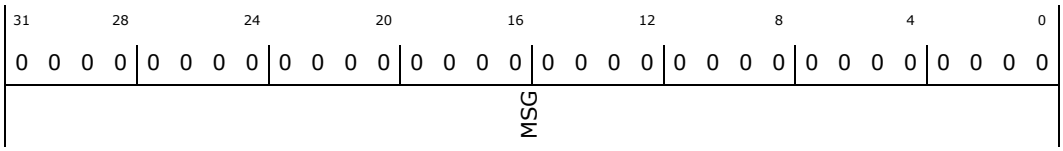
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 140h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.82 reg_HOST2ISH_MSG26_type (HOST2ISH_MSG26)—Offset 144h

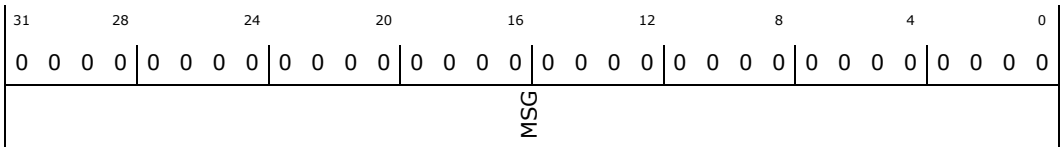
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 144h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.83 reg_HOST2ISH_MSG27_type (HOST2ISH_MSG27)—Offset 148h

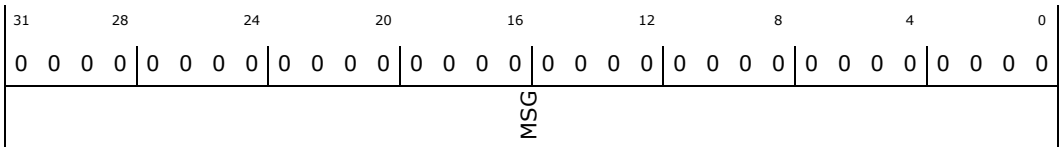
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 148h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.84 reg_HOST2ISH_MSG28_type (HOST2ISH_MSG28)—Offset 14Ch

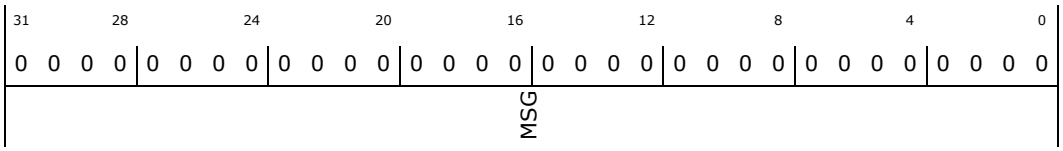
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 14Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.85 reg_HOST2ISH_MSG29_type (HOST2ISH_MSG29)—Offset 150h

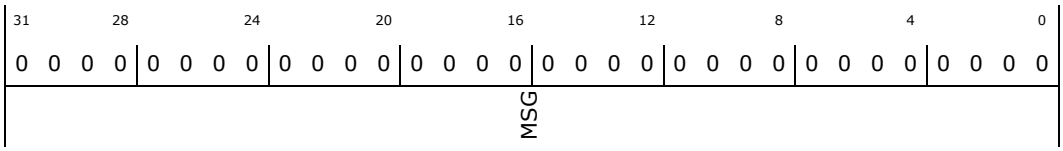
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 150h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.86 reg_HOST2ISH_MSG30_type (HOST2ISH_MSG30)—Offset 154h

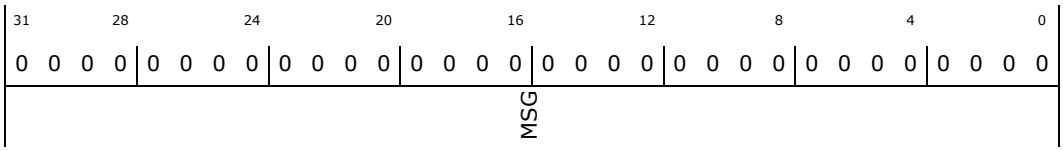
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 154h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.87 reg_HOST2ISH_MSG31_type (HOST2ISH_MSG31)—Offset 158h

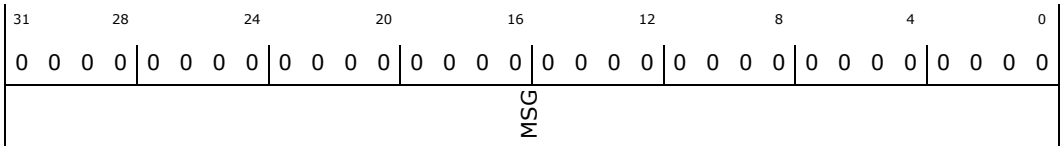
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 158h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.88 reg_HOST2ISH_MSG32_type (HOST2ISH_MSG32)—Offset 15Ch

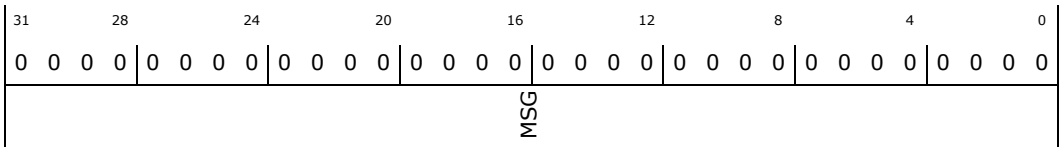
Message from HOST to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 15Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.89 reg_ISH2SEC_MSG1_type (ISH2SEC_MSG1)—Offset 160h

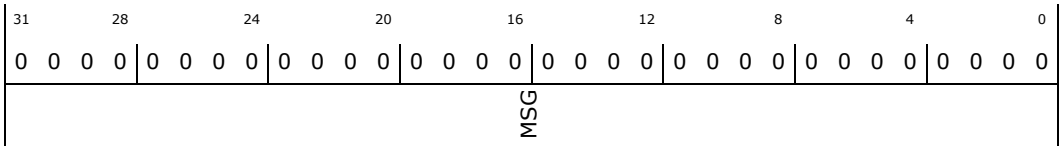
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 160h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.90 reg_ISH2SEC_MSG2_type (ISH2SEC_MSG2)—Offset 164h

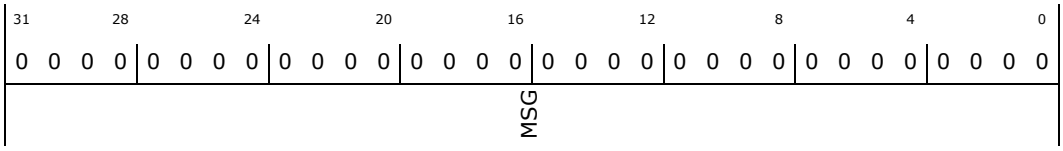
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 164h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.91 reg_ISH2SEC_MSG3_type (ISH2SEC_MSG3)—Offset 168h

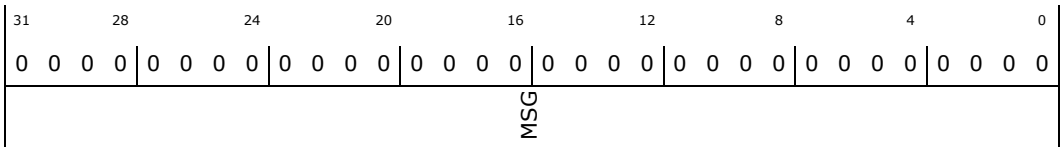
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 168h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.92 reg_ISH2SEC_MSG4_type (ISH2SEC_MSG4)—Offset 16Ch

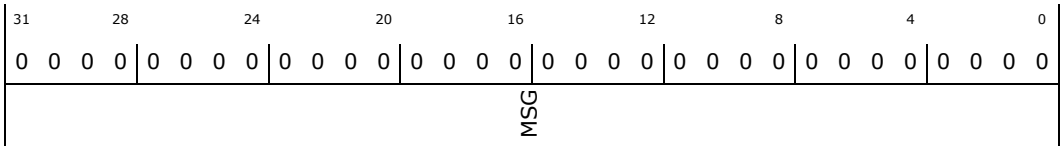
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 16Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.93 reg_ISH2SEC_MSG5_type (ISH2SEC_MSG5)—Offset 170h

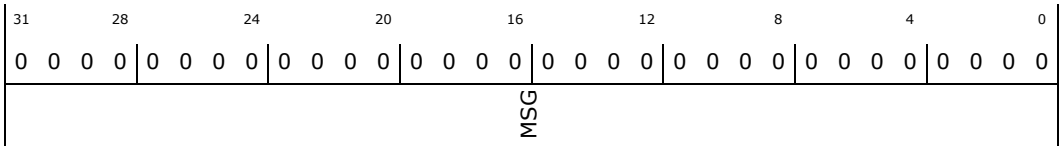
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 170h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.94 reg_ISH2SEC_MSG6_type (ISH2SEC_MSG6)—Offset 174h

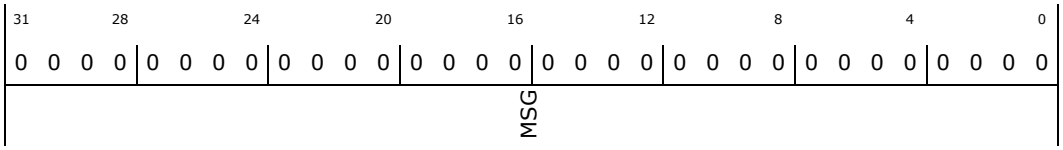
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 174h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.95 reg_ISH2SEC_MSG7_type (ISH2SEC_MSG7)—Offset 178h

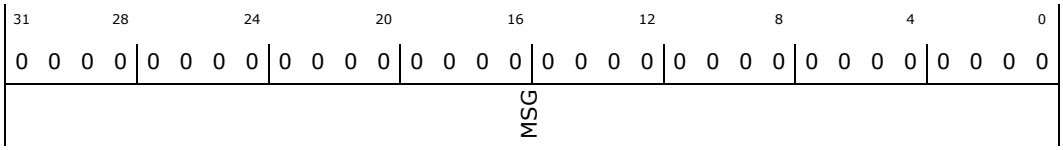
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 178h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.96 reg_ISH2SEC_MSG8_type (ISH2SEC_MSG8)—Offset 17Ch

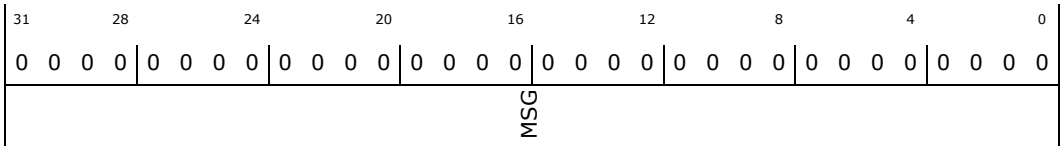
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 17Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.97 reg_ISH2SEC_MSG9_type (ISH2SEC_MSG9)—Offset 180h

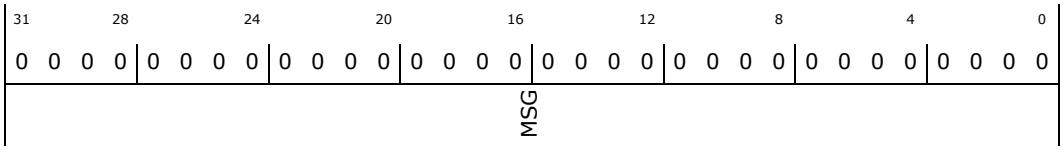
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 180h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.98 reg_ISH2SEC_MSG10_type (ISH2SEC_MSG10)—Offset 184h

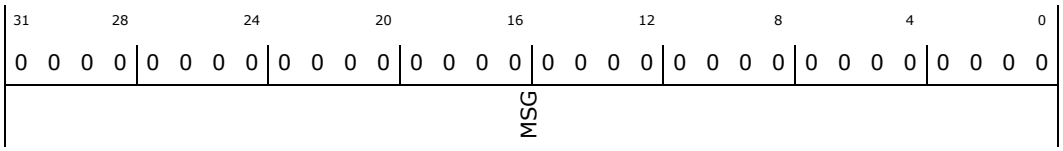
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 184h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.99 reg_ISH2SEC_MSG11_type (ISH2SEC_MSG11)—Offset 188h

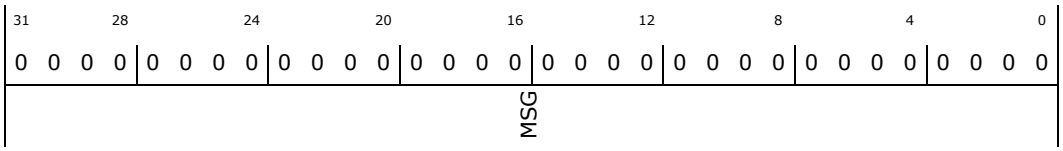
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 188h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.100 reg_ISH2SEC_MSG12_type (ISH2SEC_MSG12)—Offset 18Ch

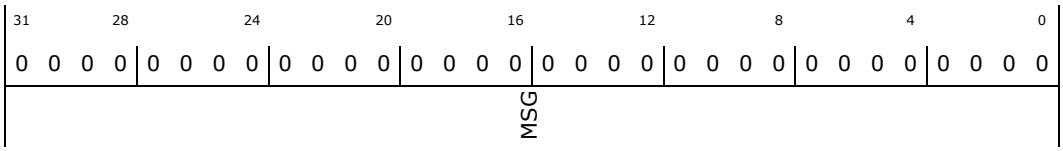
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 18Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.101 reg_ISH2SEC_MSG13_type (ISH2SEC_MSG13)—Offset 190h

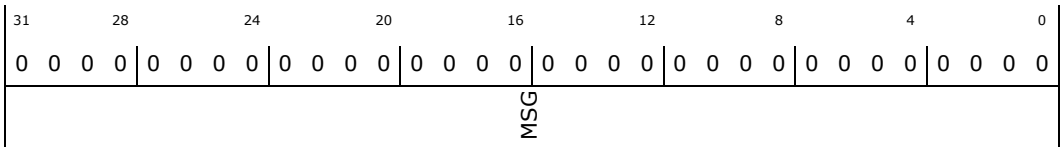
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 190h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.102 reg_ISH2SEC_MSG14_type (ISH2SEC_MSG14)—Offset 194h

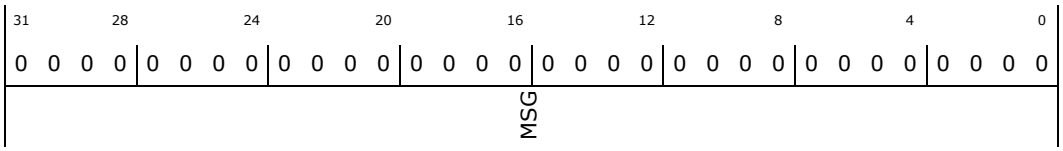
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 194h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.103 reg_ISH2SEC_MSG15_type (ISH2SEC_MSG15)—Offset 198h

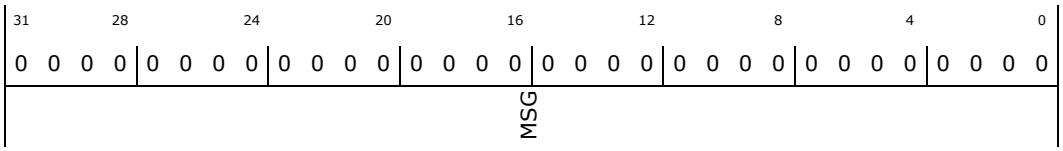
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 198h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.104 reg_ISH2SEC_MSG16_type (ISH2SEC_MSG16)—Offset 19Ch

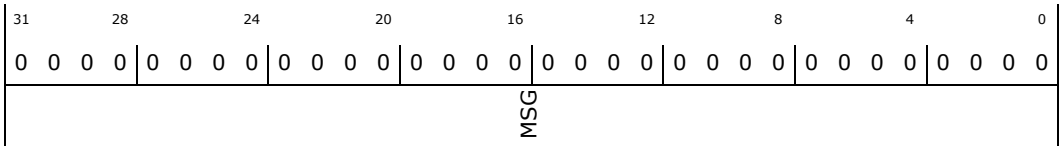
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 19Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.105 reg_ISH2SEC_MSG17_type (ISH2SEC_MSG17)—Offset 1A0h

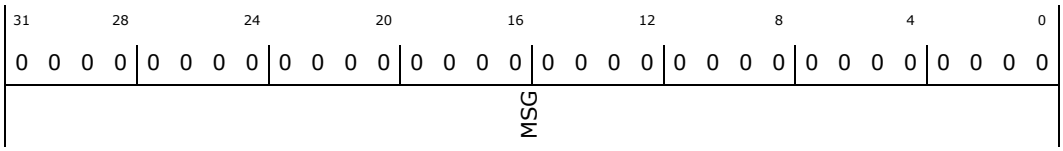
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.106 reg_ISH2SEC_MSG18_type (ISH2SEC_MSG18)—Offset 1A4h

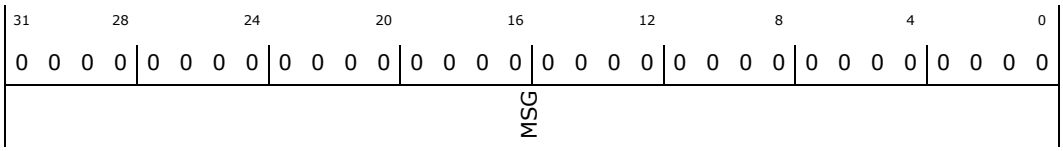
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.107 reg_ISH2SEC_MSG19_type (ISH2SEC_MSG19)—Offset 1A8h

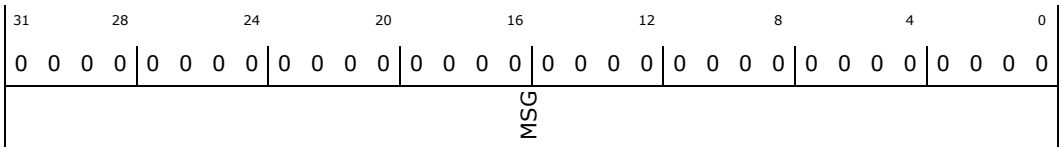
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.108 reg_ISH2SEC_MSG20_type (ISH2SEC_MSG20)—Offset 1ACh

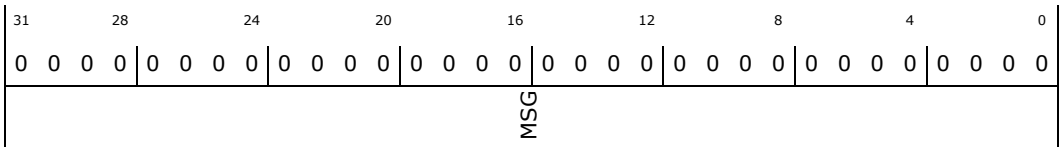
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.109 reg_ISH2SEC_MSG21_type (ISH2SEC_MSG21)—Offset 1B0h

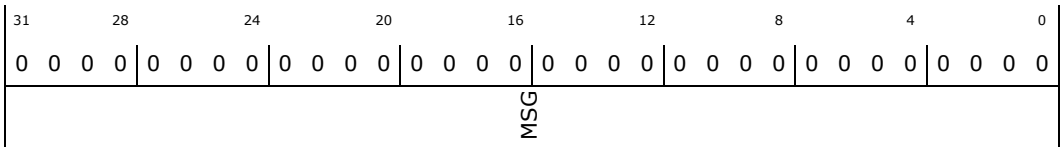
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.110 reg_ISH2SEC_MSG22_type (ISH2SEC_MSG22)—Offset 1B4h

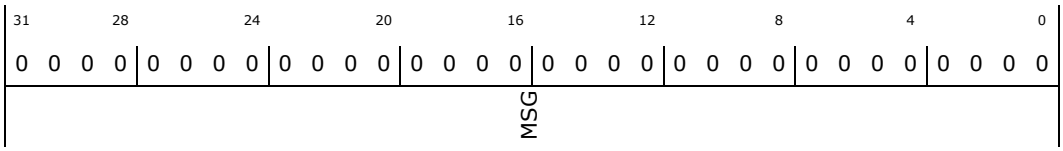
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1B4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.111 reg_ISH2SEC_MSG23_type (ISH2SEC_MSG23)—Offset 1B8h

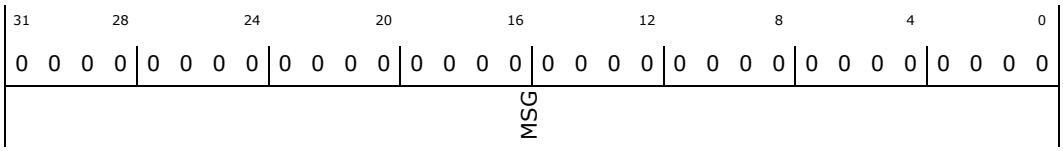
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.112 reg_ISH2SEC_MSG24_type (ISH2SEC_MSG24)—Offset 1BCh

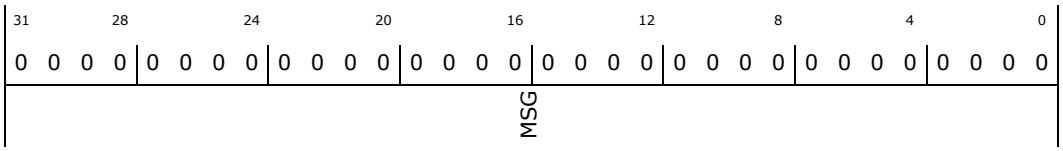
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1BCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.113 reg_ISH2SEC_MSG25_type (ISH2SEC_MSG25)—Offset 1C0h

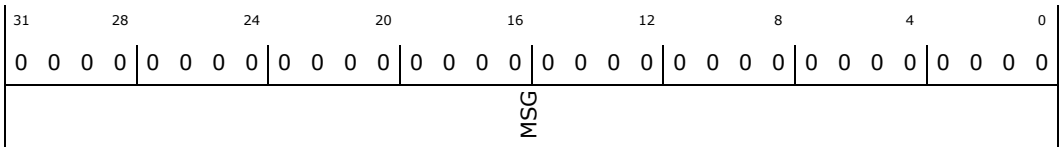
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.114 reg_ISH2SEC_MSG26_type (ISH2SEC_MSG26)—Offset 1C4h

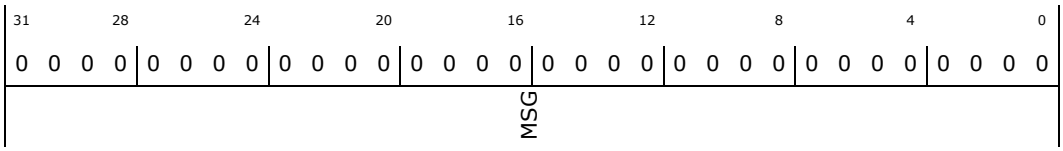
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1C4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.115 reg_ISH2SEC_MSG27_type (ISH2SEC_MSG27)—Offset 1C8h

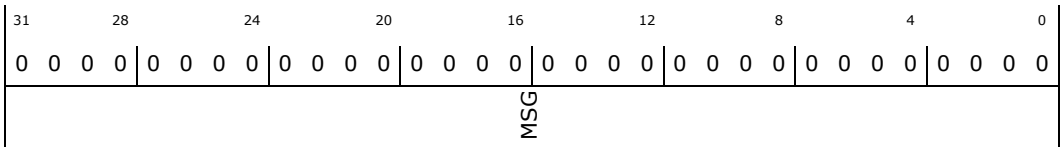
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1C8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.116 reg_ISH2SEC_MSG28_type (ISH2SEC_MSG28)—Offset 1CCh

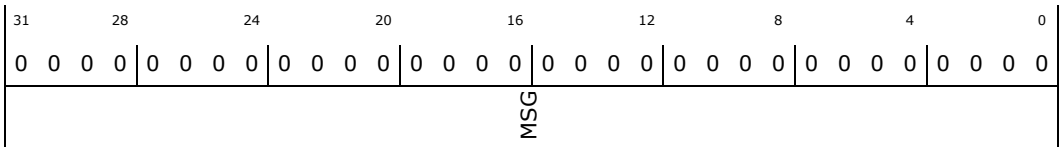
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1CCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.117 reg_ISH2SEC_MSG29_type (ISH2SEC_MSG29)—Offset 1D0h

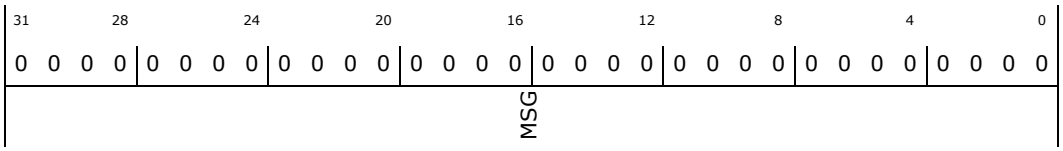
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.118 reg_ISH2SEC_MSG30_type (ISH2SEC_MSG30)—Offset 1D4h

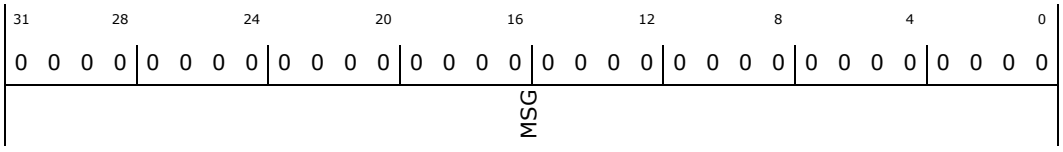
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1D4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.119 reg_ISH2SEC_MSG31_type (ISH2SEC_MSG31)—Offset 1D8h

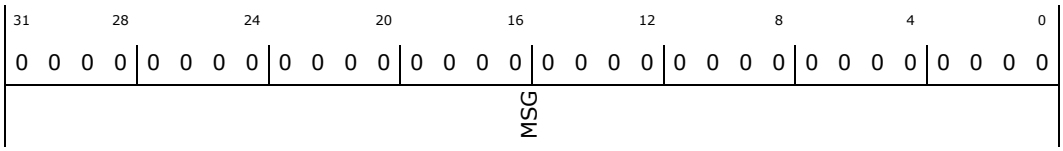
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1D8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.120 reg_ISH2SEC_MSG32_type (ISH2SEC_MSG32)—Offset 1DCh

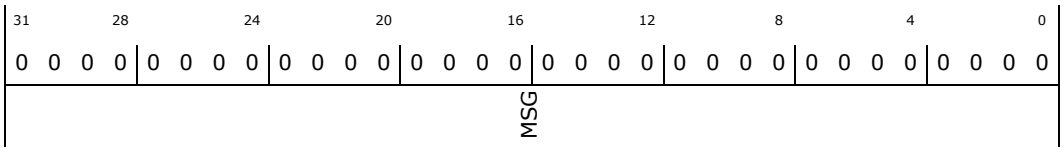
Message from ISH to SEC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1DCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.121 reg_SEC2ISH_MSG1_type (SEC2ISH_MSG1)—Offset 1E0h

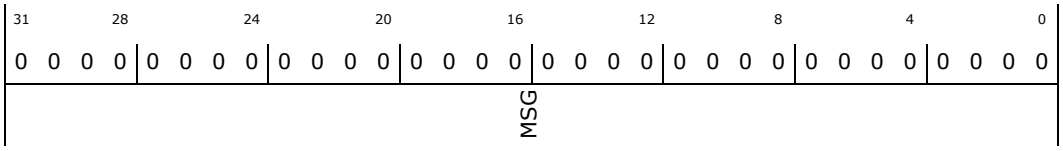
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1E0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.122 reg_SEC2ISH_MSG2_type (SEC2ISH_MSG2)—Offset 1E4h

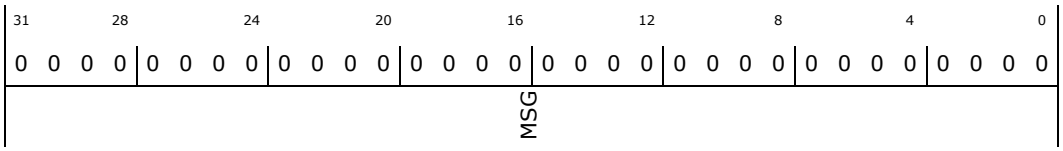
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1E4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.123 reg_SEC2ISH_MSG3_type (SEC2ISH_MSG3)—Offset 1E8h

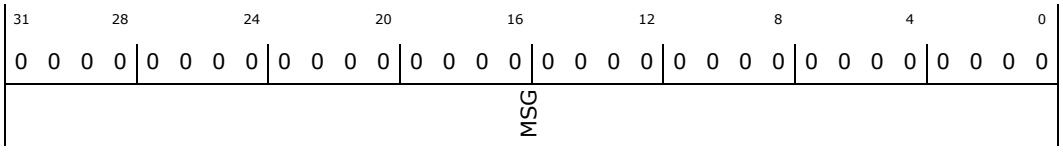
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1E8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.124 reg_SEC2ISH_MSG4_type (SEC2ISH_MSG4)—Offset 1ECh

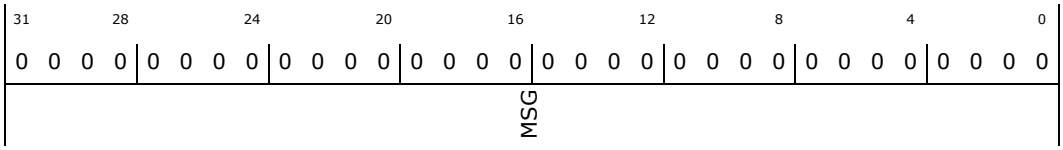
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1ECh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.125 reg_SEC2ISH_MSG5_type (SEC2ISH_MSG5)—Offset 1F0h

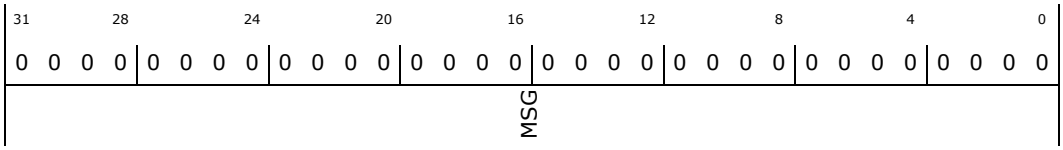
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1F0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.126 reg_SEC2ISH_MSG6_type (SEC2ISH_MSG6)—Offset 1F4h

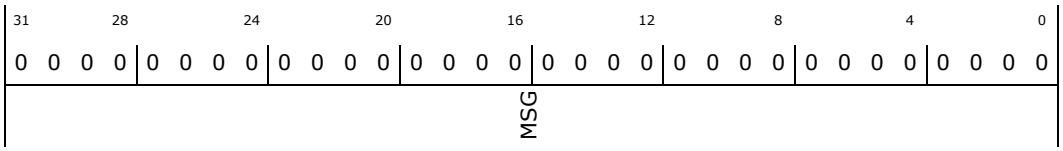
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1F4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.127 reg_SEC2ISH_MSG7_type (SEC2ISH_MSG7)—Offset 1F8h

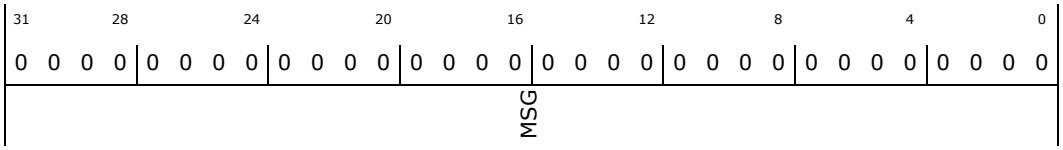
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.128 reg_SEC2ISH_MSG8_type (SEC2ISH_MSG8)—Offset 1FCh

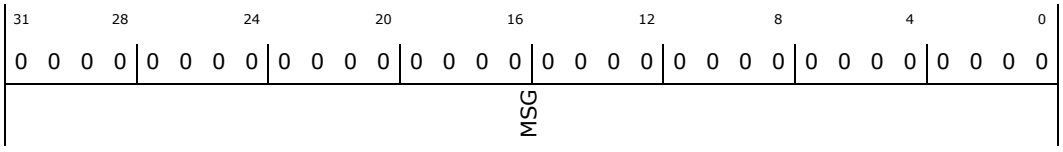
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 1FCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.129 reg_SEC2ISH_MSG9_type (SEC2ISH_MSG9)—Offset 200h

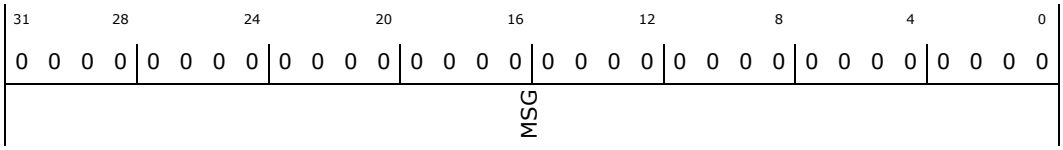
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 200h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.130 reg_SEC2ISH_MSG10_type (SEC2ISH_MSG10)—Offset 204h

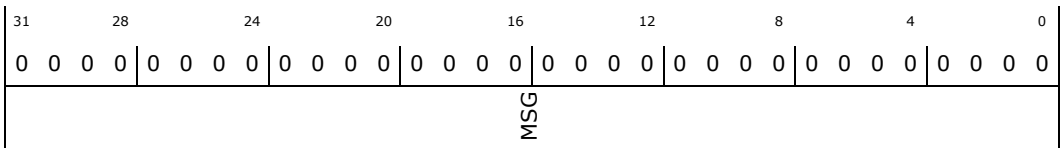
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 204h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.131 reg_SEC2ISH_MSG11_type (SEC2ISH_MSG11)—Offset 208h

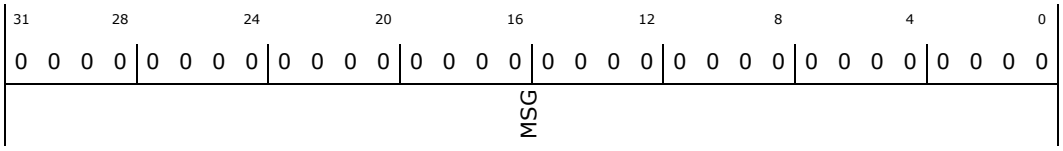
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 208h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.132 reg_SEC2ISH_MSG12_type (SEC2ISH_MSG12)—Offset 20Ch

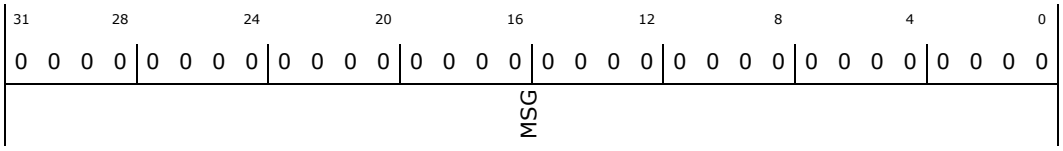
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 20Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.133 reg_SEC2ISH_MSG13_type (SEC2ISH_MSG13)—Offset 210h

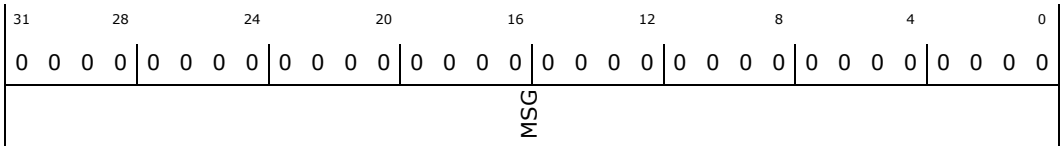
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 210h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.134 reg_SEC2ISH_MSG14_type (SEC2ISH_MSG14)—Offset 214h

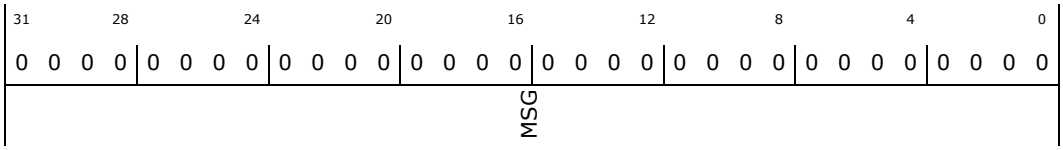
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 214h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.135 reg_SEC2ISH_MSG15_type (SEC2ISH_MSG15)—Offset 218h

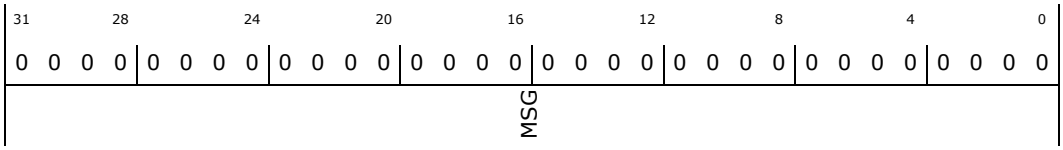
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 218h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.136 reg_SEC2ISH_MSG16_type (SEC2ISH_MSG16)—Offset 21Ch

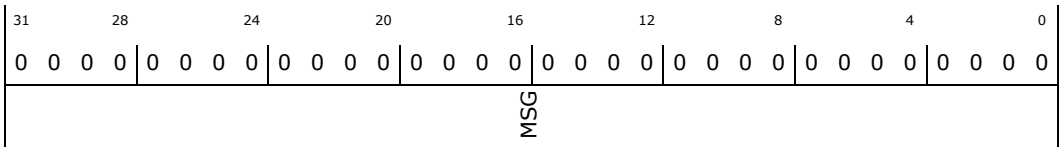
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 21Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.137 reg_SEC2ISH_MSG17_type (SEC2ISH_MSG17)—Offset 220h

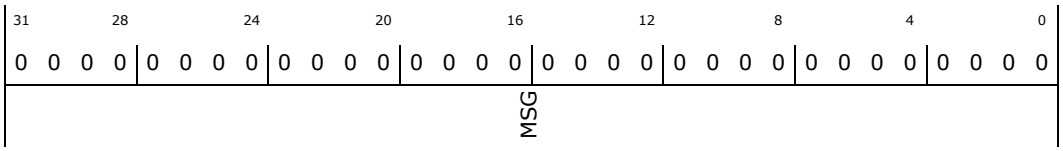
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 220h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.138 reg_SEC2ISH_MSG18_type (SEC2ISH_MSG18)—Offset 224h

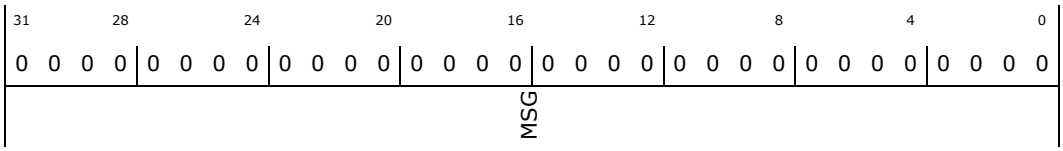
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 224h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.139 reg_SEC2ISH_MSG19_type (SEC2ISH_MSG19)—Offset 228h

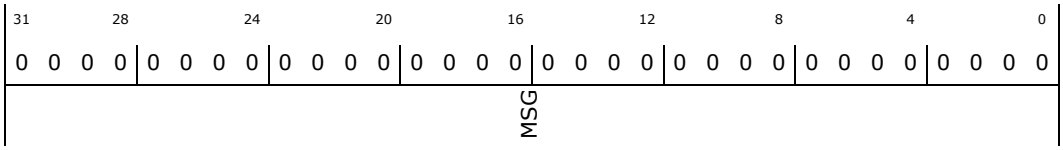
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 228h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.140 reg_SEC2ISH_MSG20_type (SEC2ISH_MSG20)—Offset 22Ch

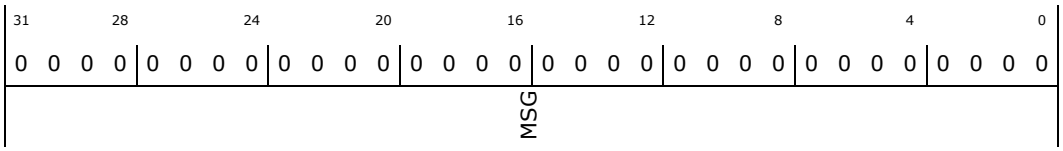
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 22Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.141 reg_SEC2ISH_MSG21_type (SEC2ISH_MSG21)—Offset 230h

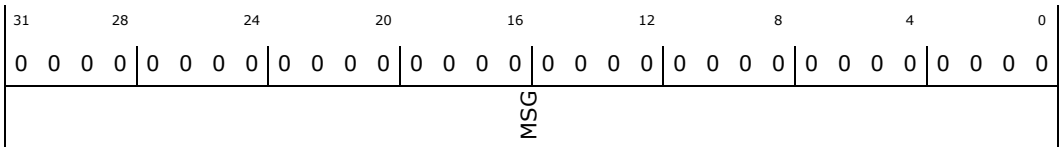
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 230h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.142 reg_SEC2ISH_MSG22_type (SEC2ISH_MSG22)—Offset 234h

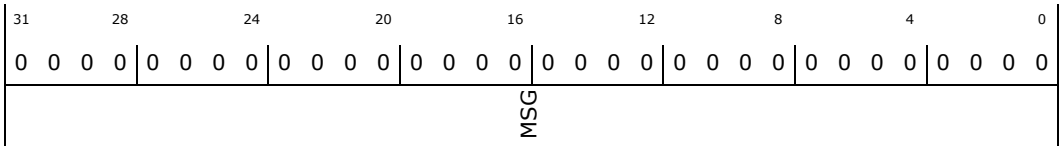
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 234h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.143 reg_SEC2ISH_MSG23_type (SEC2ISH_MSG23)—Offset 238h

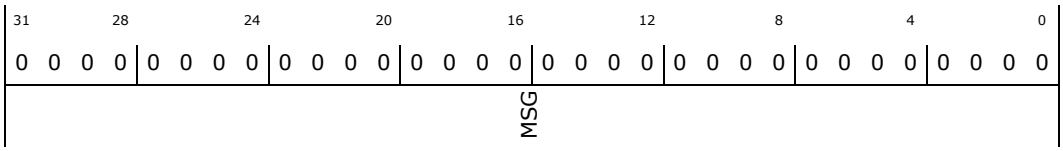
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 238h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.144 reg_SEC2ISH_MSG24_type (SEC2ISH_MSG24)—Offset 23Ch

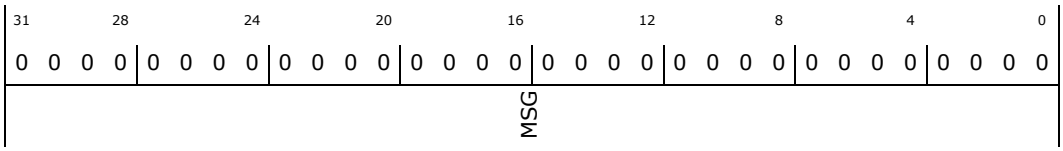
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 23Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.145 reg_SEC2ISH_MSG25_type (SEC2ISH_MSG25)—Offset 240h

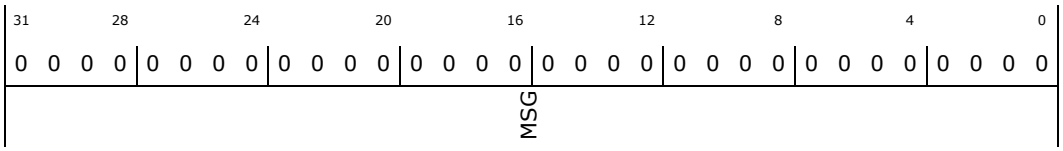
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 240h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.146 reg_SEC2ISH_MSG26_type (SEC2ISH_MSG26)—Offset 244h

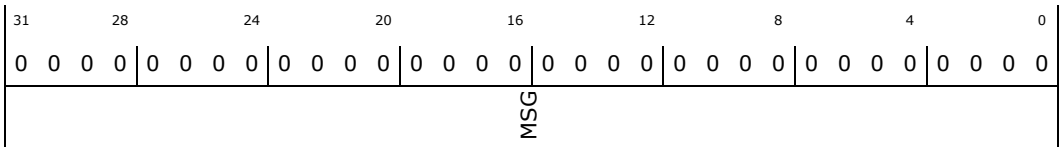
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 244h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.147 reg_SEC2ISH_MSG27_type (SEC2ISH_MSG27)—Offset 248h

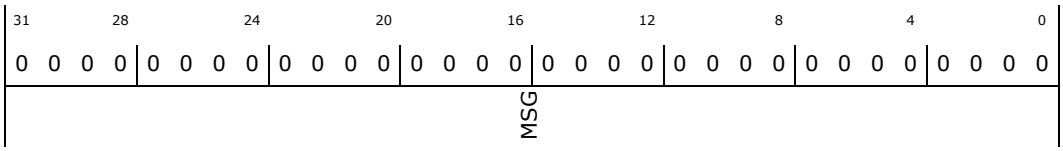
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 248h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.148 reg_SEC2ISH_MSG28_type (SEC2ISH_MSG28)—Offset 24Ch

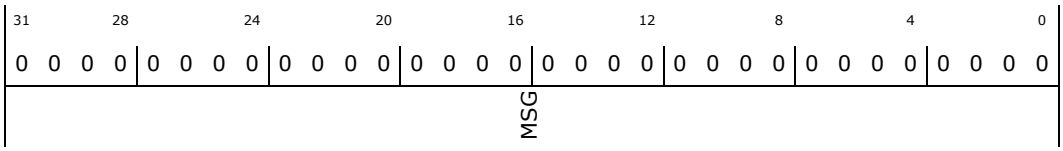
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 24Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.149 reg_SEC2ISH_MSG29_type (SEC2ISH_MSG29)—Offset 250h

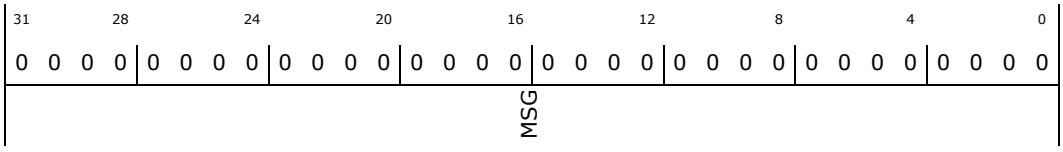
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 250h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.150 reg_SEC2ISH_MSG30_type (SEC2ISH_MSG30)—Offset 254h

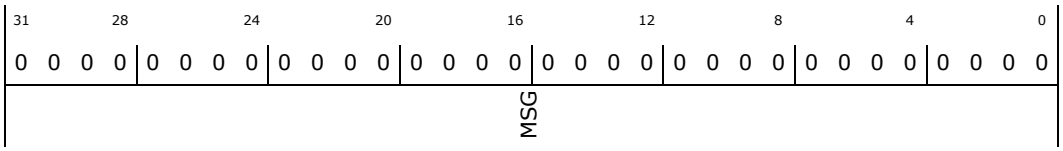
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 254h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.151 reg_SEC2ISH_MSG31_type (SEC2ISH_MSG31)—Offset 258h

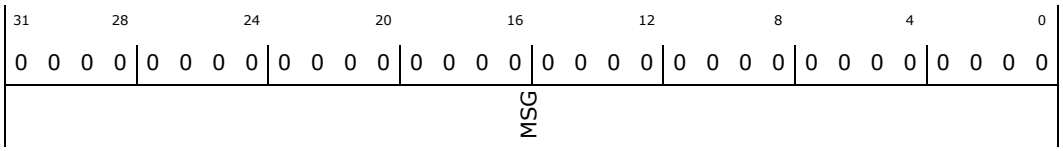
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 258h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.152 reg_SEC2ISH_MSG32_type (SEC2ISH_MSG32)—Offset 25Ch

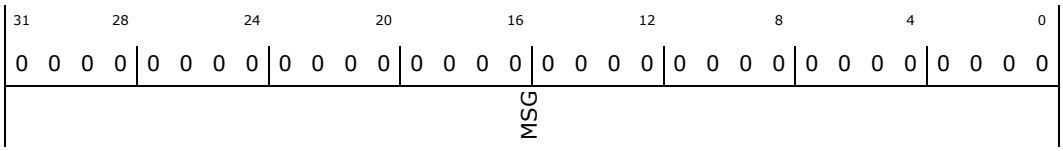
Message from SEC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 25Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.153 reg_ISH2PMC_MSG1_type (ISH2PMC_MSG1)—Offset 260h

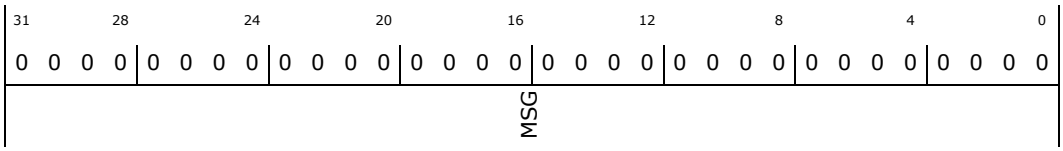
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 260h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.154 reg_ISH2PMC_MSG2_type (ISH2PMC_MSG2)—Offset 264h

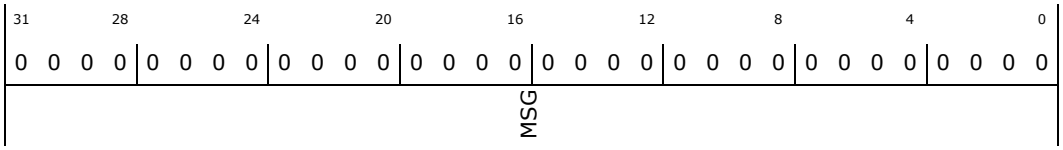
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 264h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.155 reg_ISH2PMC_MSG3_type (ISH2PMC_MSG3)—Offset 268h

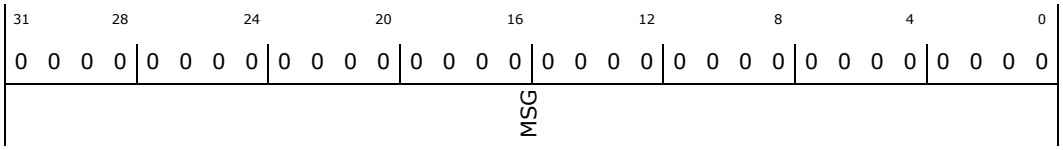
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 268h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.156 reg_ISH2PMC_MSG4_type (ISH2PMC_MSG4)—Offset 26Ch

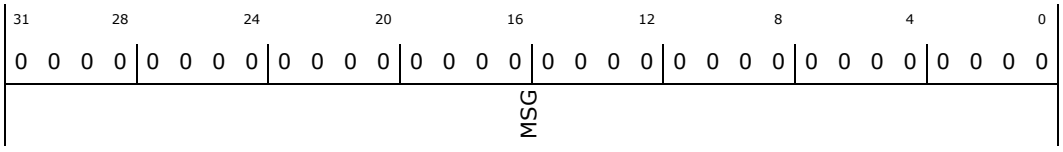
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 26Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.157 reg_ISH2PMC_MSG5_type (ISH2PMC_MSG5)—Offset 270h

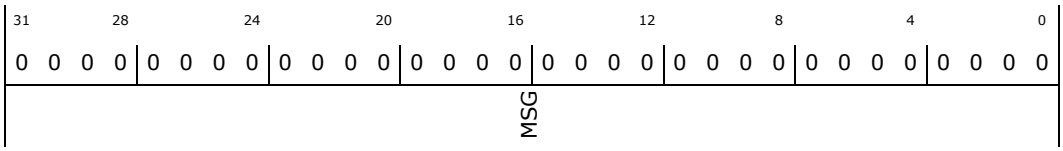
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 270h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.158 reg_ISH2PMC_MSG6_type (ISH2PMC_MSG6)—Offset 274h

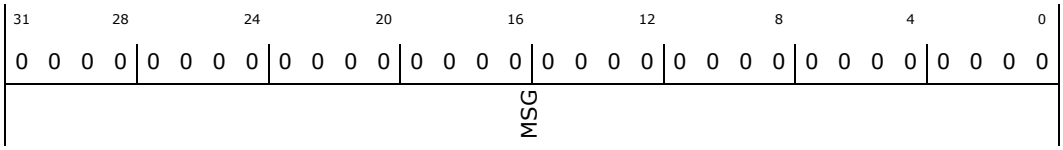
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 274h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.159 reg_ISH2PMC_MSG7_type (ISH2PMC_MSG7)—Offset 278h

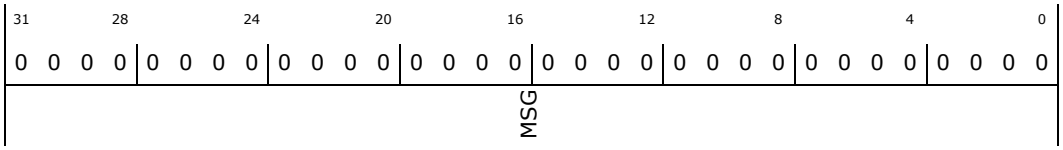
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 278h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.160 reg_ISH2PMC_MSG8_type (ISH2PMC_MSG8)—Offset 27Ch

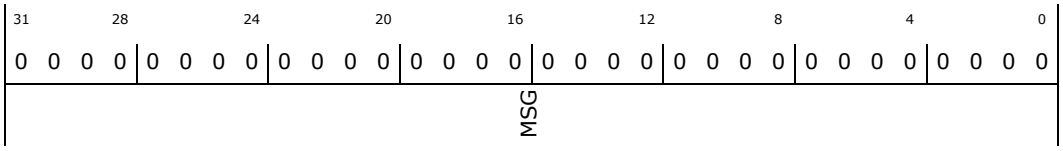
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 27Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.161 reg_ISH2PMC_MSG9_type (ISH2PMC_MSG9)—Offset 280h

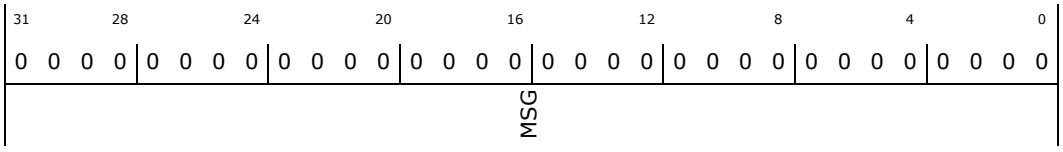
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 280h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.162 reg_ISH2PMC_MSG10_type (ISH2PMC_MSG10)—Offset 284h

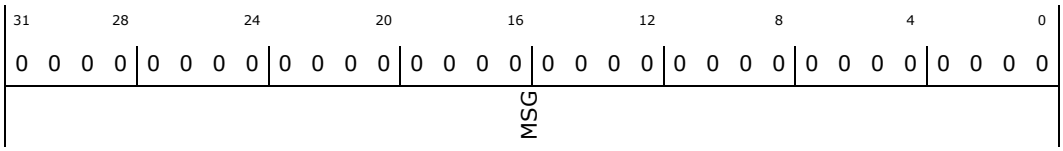
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 284h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.163 reg_ISH2PMC_MSG11_type (ISH2PMC_MSG11)—Offset 288h

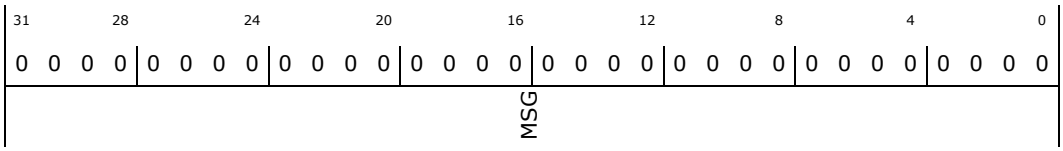
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 288h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.164 reg_ISH2PMC_MSG12_type (ISH2PMC_MSG12)—Offset 28Ch

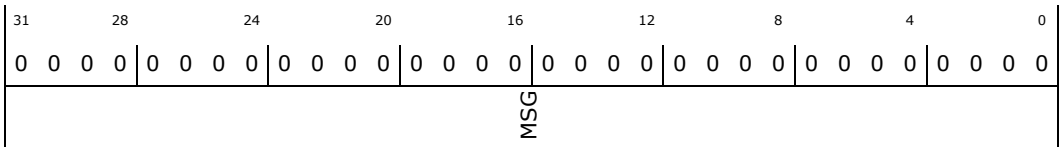
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 28Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.165 reg_ISH2PMC_MSG13_type (ISH2PMC_MSG13)—Offset 290h

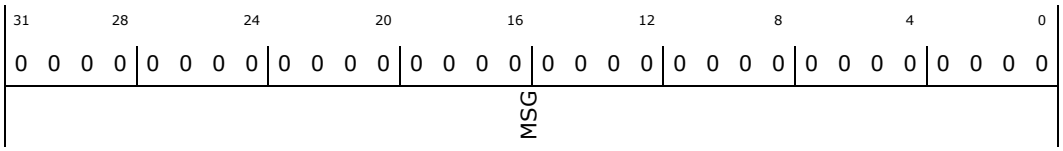
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 290h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.166 reg_ISH2PMC_MSG14_type (ISH2PMC_MSG14)—Offset 294h

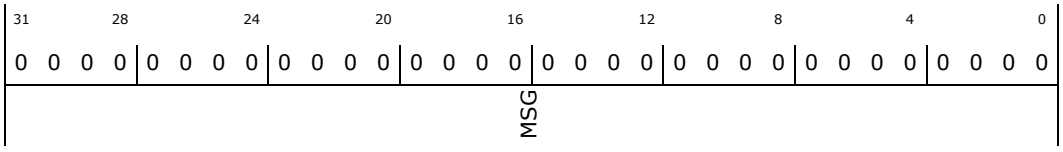
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 294h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.167 reg_ISH2PMC_MSG15_type (ISH2PMC_MSG15)—Offset 298h

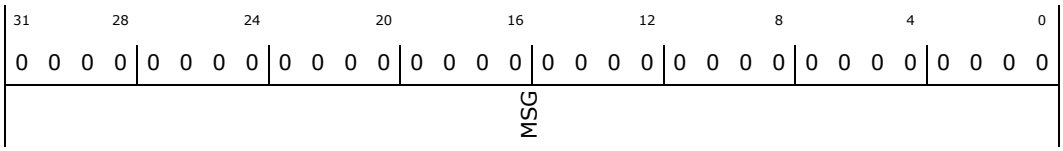
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 298h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.168 reg_ISH2PMC_MSG16_type (ISH2PMC_MSG16)—Offset 29Ch

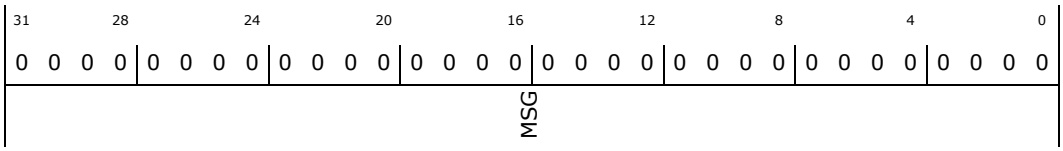
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 29Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.169 reg_ISH2PMC_MSG17_type (ISH2PMC_MSG17)—Offset 2A0h

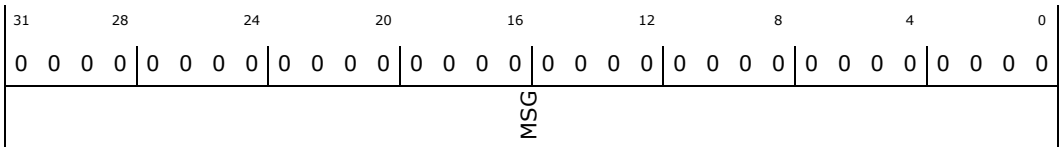
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.170 reg_ISH2PMC_MSG18_type (ISH2PMC_MSG18)—Offset 2A4h

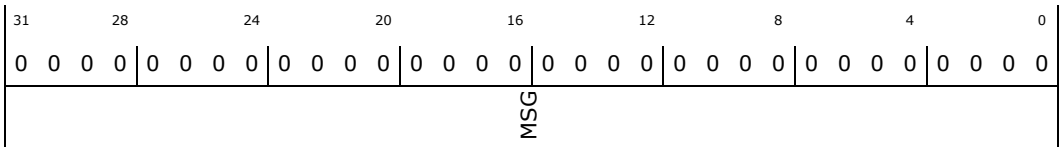
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.171 reg_ISH2PMC_MSG19_type (ISH2PMC_MSG19)—Offset 2A8h

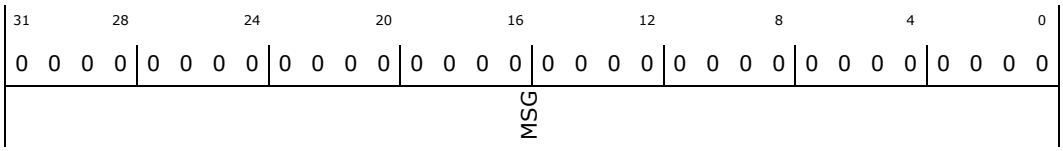
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.172 reg_ISH2PMC_MSG20_type (ISH2PMC_MSG20)—Offset 2ACh

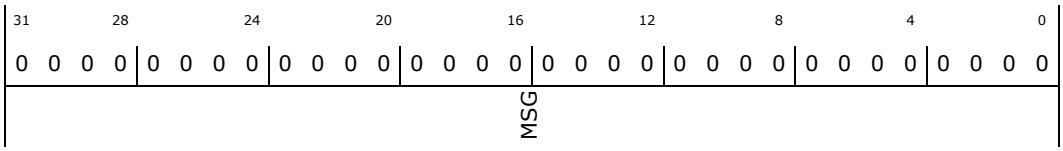
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.173 reg_ISH2PMC_MSG21_type (ISH2PMC_MSG21)—Offset 2B0h

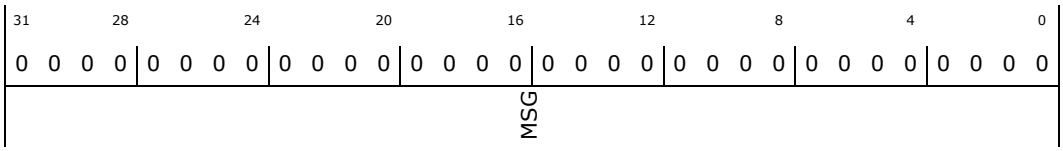
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2B0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.174 reg_ISH2PMC_MSG22_type (ISH2PMC_MSG22)—Offset 2B4h

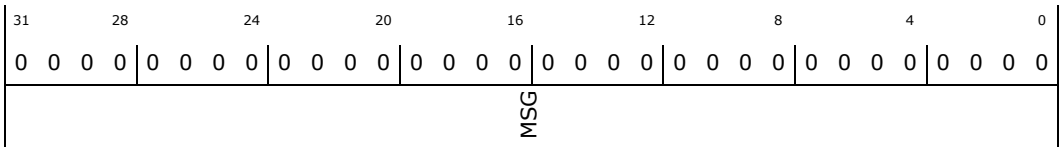
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2B4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.175 reg_ISH2PMC_MSG23_type (ISH2PMC_MSG23)—Offset 2B8h

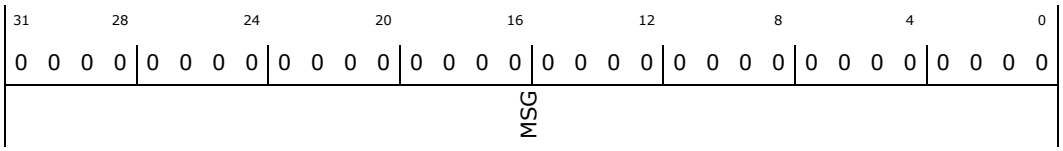
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2B8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.176 reg_ISH2PMC_MSG24_type (ISH2PMC_MSG24)—Offset 2BCh

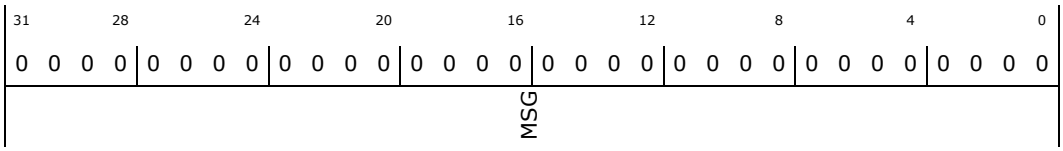
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2BCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.177 reg_ISH2PMC_MSG25_type (ISH2PMC_MSG25)—Offset 2C0h

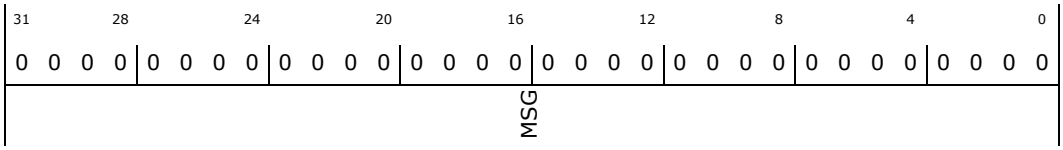
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.178 reg_ISH2PMC_MSG26_type (ISH2PMC_MSG26)—Offset 2C4h

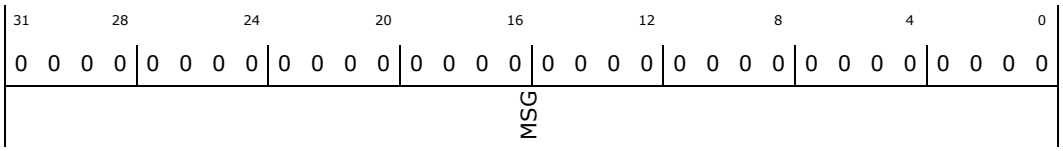
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2C4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.179 reg_ISH2PMC_MSG27_type (ISH2PMC_MSG27)—Offset 2C8h

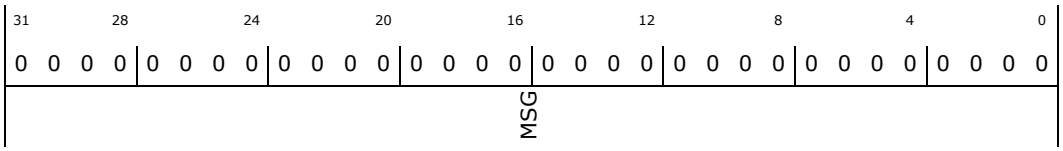
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2C8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.180 reg_ISH2PMC_MSG28_type (ISH2PMC_MSG28)—Offset 2CCh

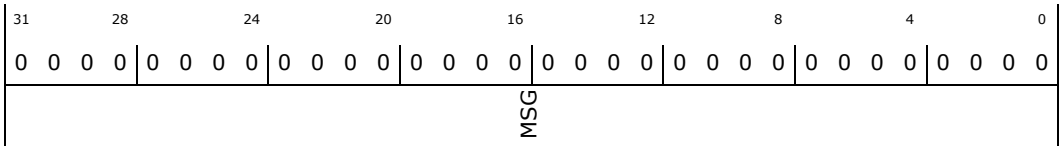
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2CCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.181 reg_ISH2PMC_MSG29_type (ISH2PMC_MSG29)—Offset 2D0h

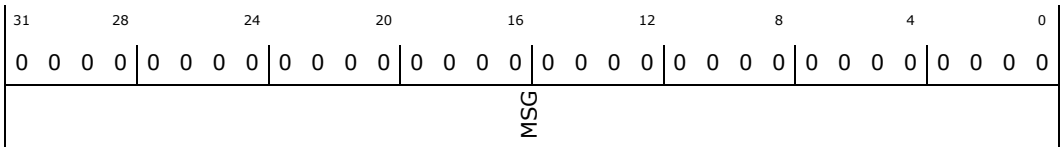
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2D0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.182 reg_ISH2PMC_MSG30_type (ISH2PMC_MSG30)—Offset 2D4h

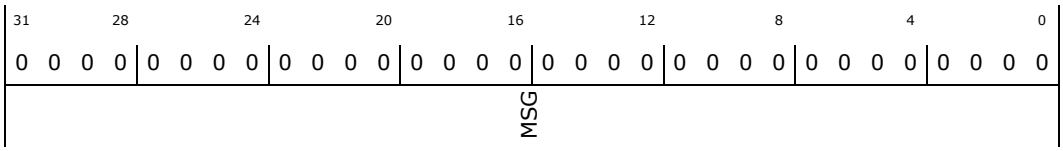
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2D4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.183 reg_ISH2PMC_MSG31_type (ISH2PMC_MSG31)—Offset 2D8h

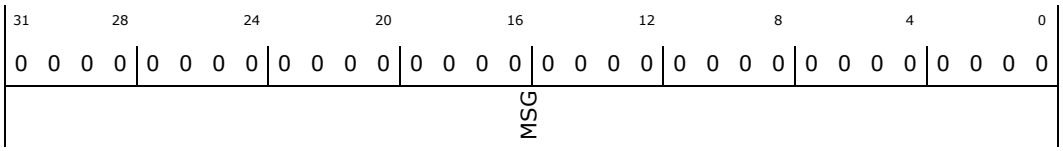
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2D8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.184 reg_ISH2PMC_MSG32_type (ISH2PMC_MSG32)—Offset 2DCh

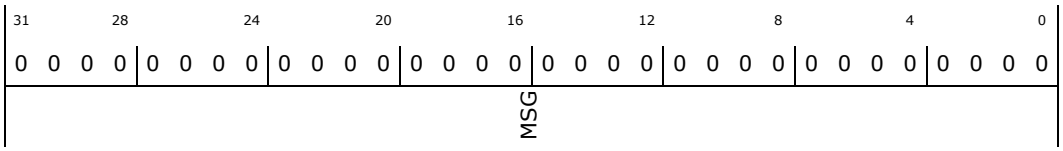
Message from ISH to PMC

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2DCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.185 reg_PMC2ISH_MSG1_type (PMC2ISH_MSG1)—Offset 2E0h

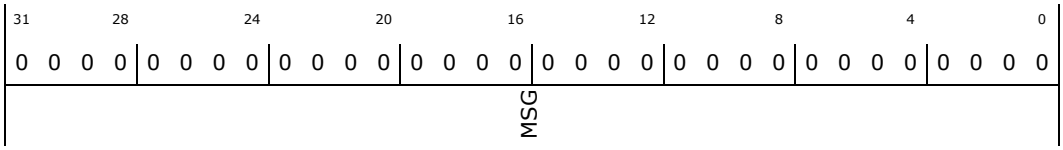
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2E0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.186 reg_PMC2ISH_MSG2_type (PMC2ISH_MSG2)—Offset 2E4h

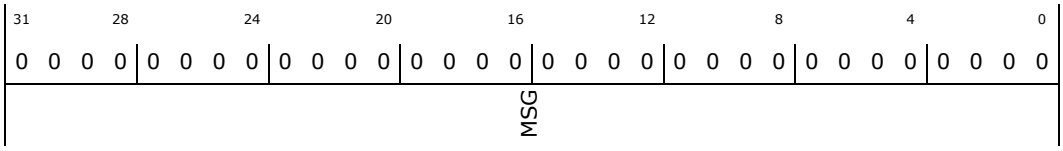
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2E4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.187 reg_PMC2ISH_MSG3_type (PMC2ISH_MSG3)—Offset 2E8h

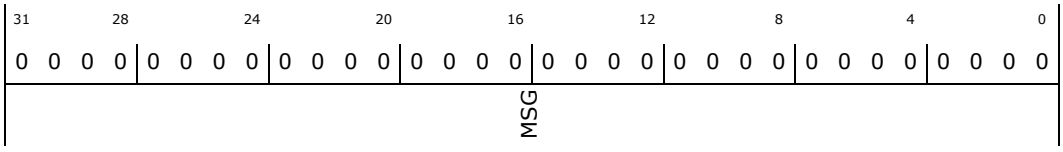
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2E8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.188 reg_PMC2ISH_MSG4_type (PMC2ISH_MSG4)—Offset 2ECh

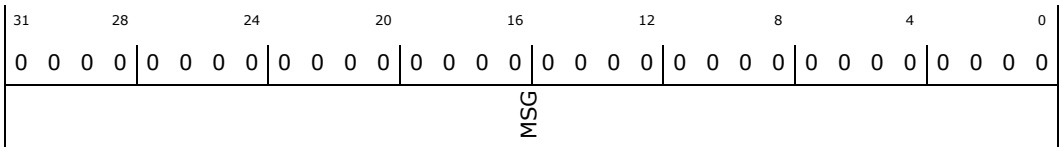
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2ECh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.189 reg_PMC2ISH_MSG5_type (PMC2ISH_MSG5)—Offset 2F0h

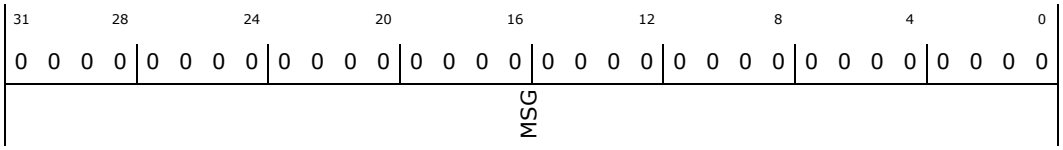
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2F0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.190 reg_PMC2ISH_MSG6_type (PMC2ISH_MSG6)—Offset 2F4h

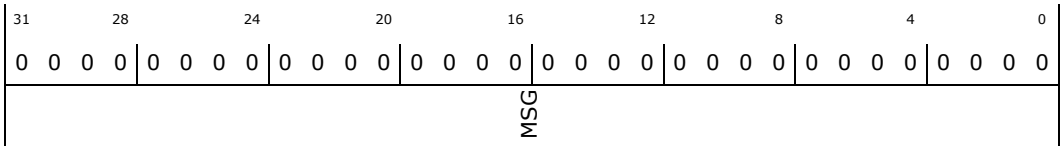
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2F4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.191 reg_PMC2ISH_MSG7_type (PMC2ISH_MSG7)—Offset 2F8h

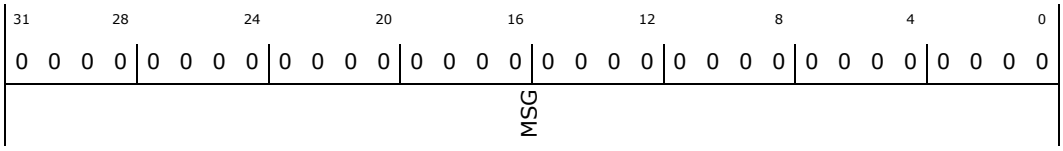
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.192 reg_PMC2ISH_MSG8_type (PMC2ISH_MSG8)—Offset 2FCh

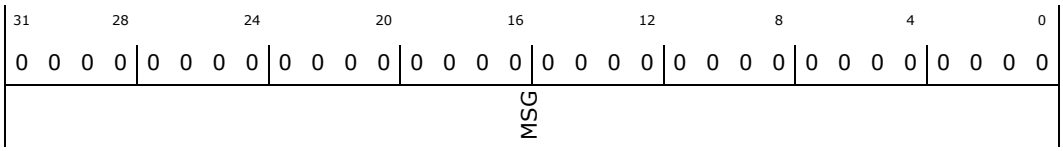
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 2FCh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.193 reg_PMC2ISH_MSG9_type (PMC2ISH_MSG9)—Offset 300h

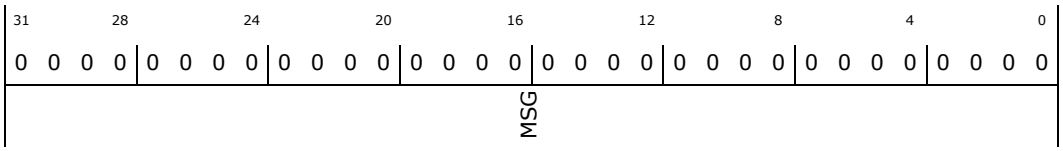
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 300h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.194 reg_PMC2ISH_MSG10_type (PMC2ISH_MSG10)—Offset 304h

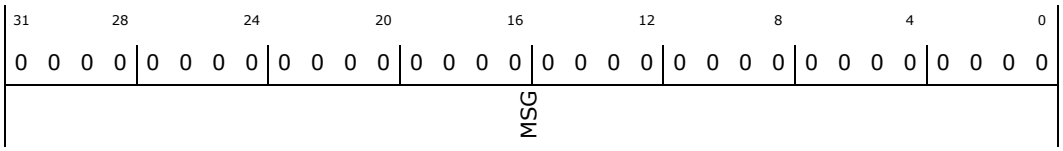
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 304h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.195 reg_PMC2ISH_MSG11_type (PMC2ISH_MSG11)—Offset 308h

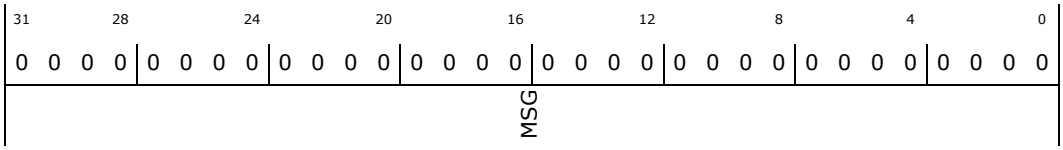
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 308h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.196 reg_PMC2ISH_MSG12_type (PMC2ISH_MSG12)—Offset 30Ch

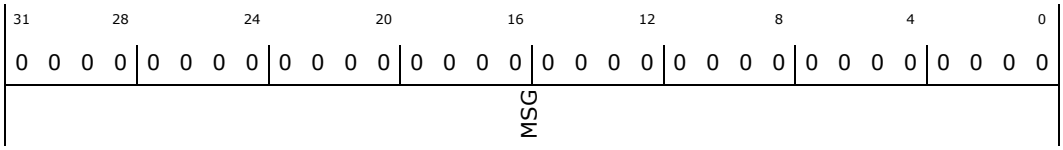
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 30Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.197 reg_PMC2ISH_MSG13_type (PMC2ISH_MSG13)—Offset 310h

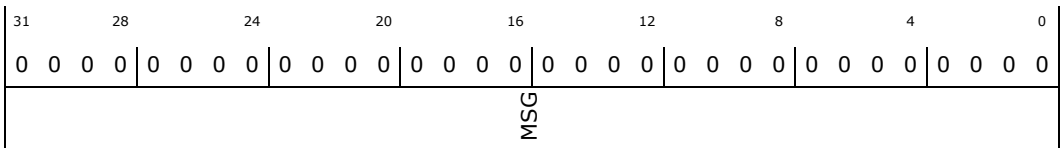
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 310h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.198 reg_PMC2ISH_MSG14_type (PMC2ISH_MSG14)—Offset 314h

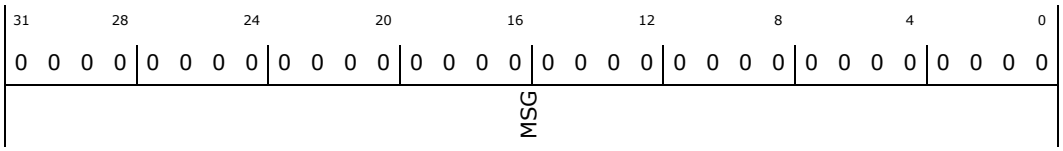
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 314h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.199 reg_PMC2ISH_MSG15_type (PMC2ISH_MSG15)—Offset 318h

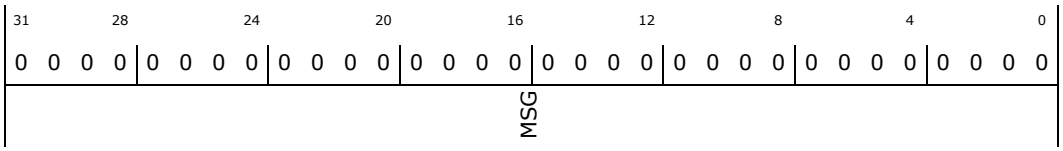
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 318h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.200 reg_PMC2ISH_MSG16_type (PMC2ISH_MSG16)—Offset 31Ch

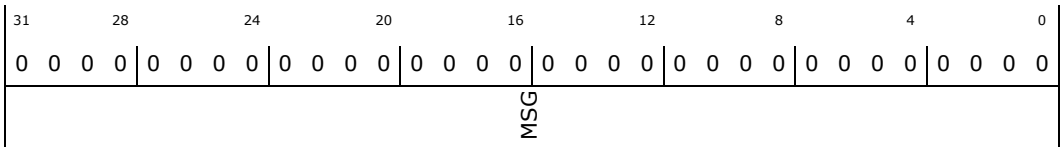
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 31Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.201 reg_PMC2ISH_MSG17_type (PMC2ISH_MSG17)—Offset 320h

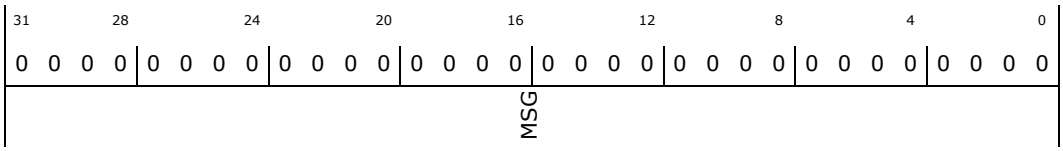
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 320h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.202 reg_PMC2ISH_MSG18_type (PMC2ISH_MSG18)—Offset 324h

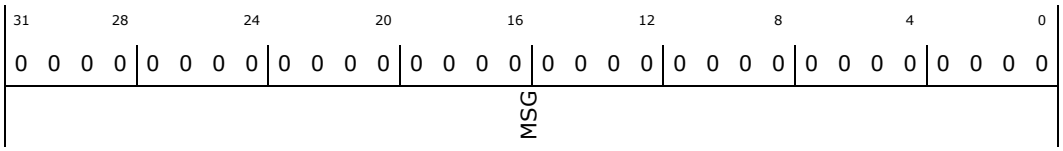
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 324h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.203 reg_PMC2ISH_MSG19_type (PMC2ISH_MSG19)—Offset 328h

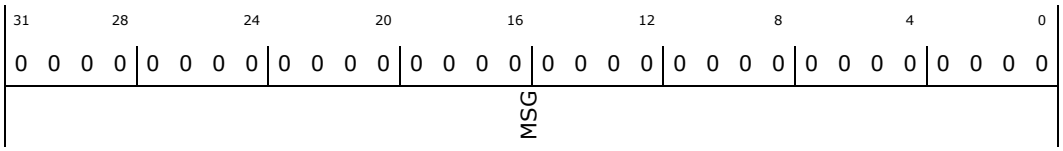
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 328h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.204 reg_PMC2ISH_MSG20_type (PMC2ISH_MSG20)—Offset 32Ch

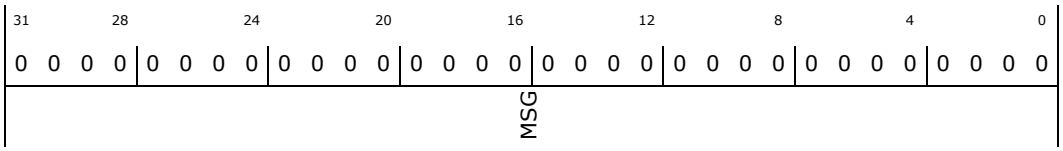
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 32Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.205 reg_PMC2ISH_MSG21_type (PMC2ISH_MSG21)—Offset 330h

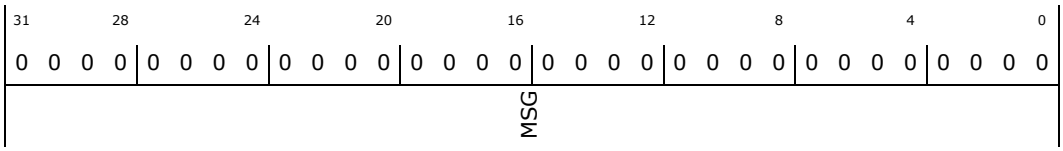
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 330h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.206 reg_PMC2ISH_MSG22_type (PMC2ISH_MSG22)—Offset 334h

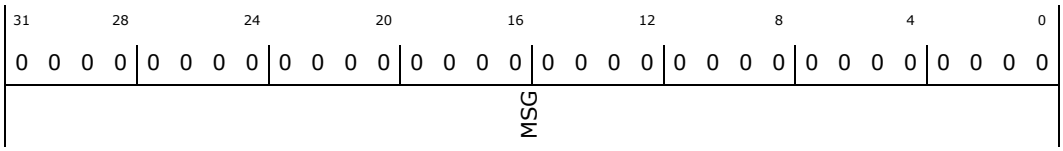
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 334h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.207 reg_PMC2ISH_MSG23_type (PMC2ISH_MSG23)—Offset 338h

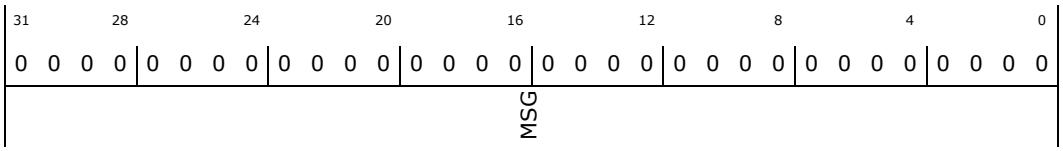
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 338h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.208 reg_PMC2ISH_MSG24_type (PMC2ISH_MSG24)—Offset 33Ch

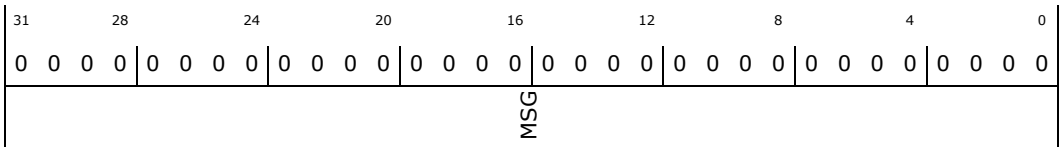
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 33Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.209 reg_PMC2ISH_MSG25_type (PMC2ISH_MSG25)—Offset 340h

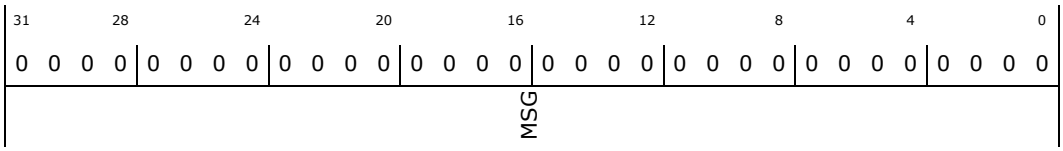
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 340h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.210 reg_PMC2ISH_MSG26_type (PMC2ISH_MSG26)—Offset 344h

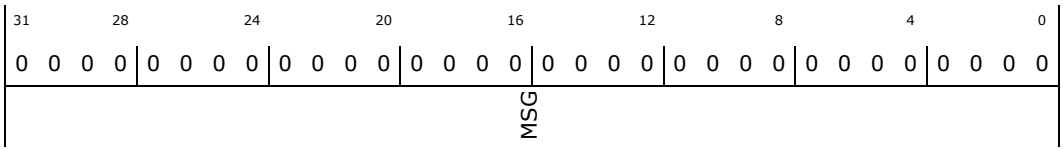
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 344h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.211 reg_PMC2ISH_MSG27_type (PMC2ISH_MSG27)—Offset 348h

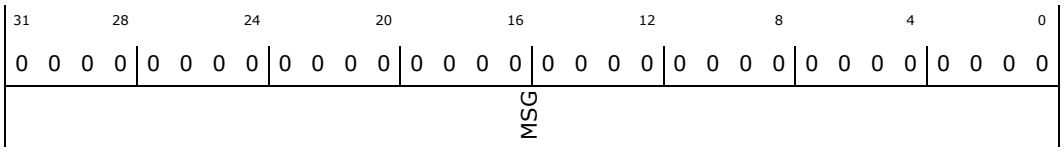
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 348h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.212 reg_PMC2ISH_MSG28_type (PMC2ISH_MSG28)—Offset 34Ch

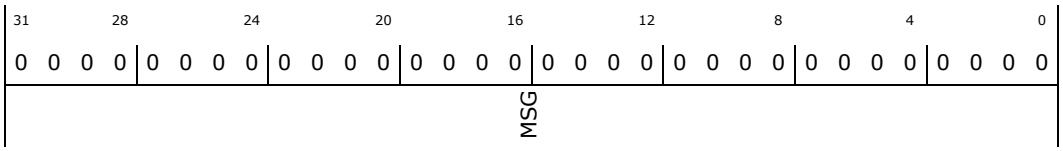
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 34Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.213 reg_PMC2ISH_MSG29_type (PMC2ISH_MSG29)—Offset 350h

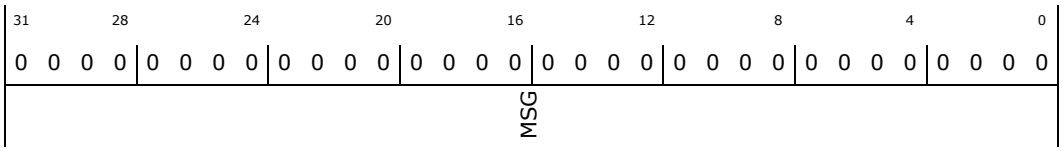
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 350h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.214 reg_PMC2ISH_MSG30_type (PMC2ISH_MSG30)—Offset 354h

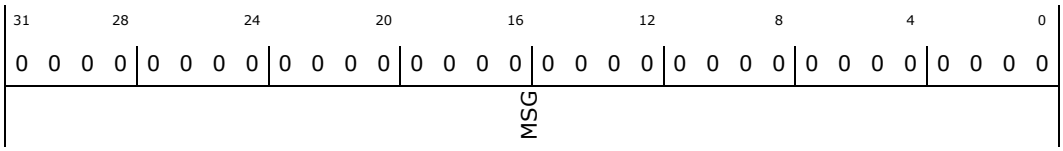
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 354h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.215 reg_PMC2ISH_MSG31_type (PMC2ISH_MSG31)—Offset 358h

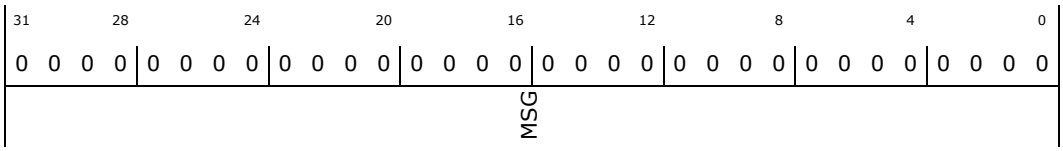
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 358h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.216 reg_PMC2ISH_MSG32_type (PMC2ISH_MSG32)—Offset 35Ch

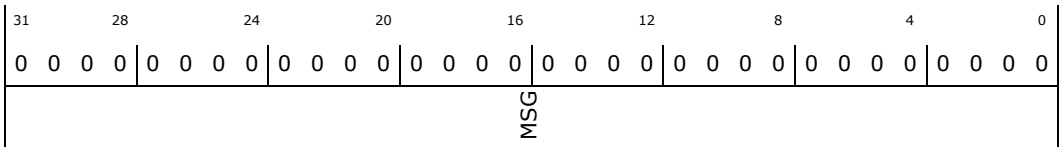
Message from PMC to ISH

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 35Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.2.217 reg_REMAP0_type (REMAP0)—Offset 360h

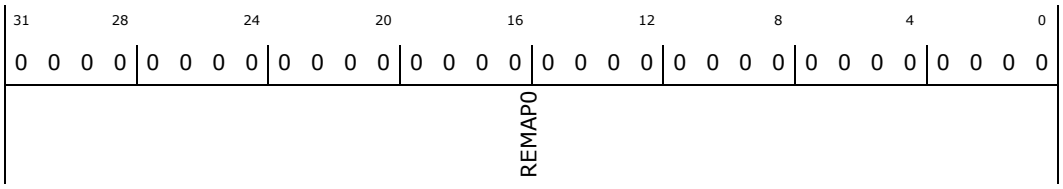
REMAP0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 360h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**REMAP0:** ish_clk

12.2.218 reg_REMAP1_type (REMAP1)—Offset 364h

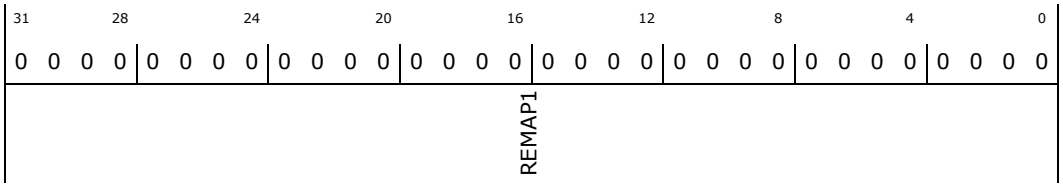
REMAP1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 364h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**REMAP1:** ish_clk

12.2.219 reg_REMAP2_type (REMAP2)—Offset 368h

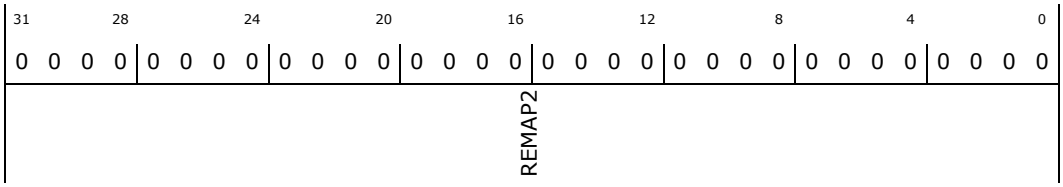
REMAP2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 368h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**REMAP2:** ish_clk

12.2.220 reg_REMAP3_type (REMAP3)—Offset 36Ch

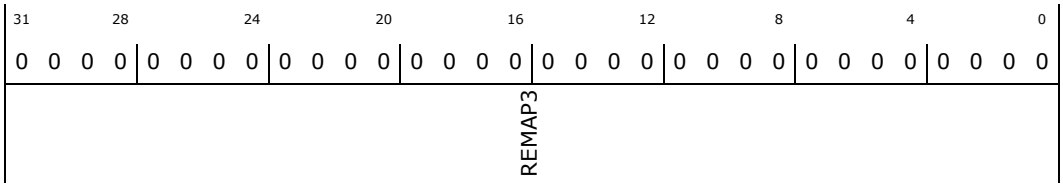
REMAP3

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 36Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**REMAP3:** ish_clk

12.2.221 reg_REMAP4_type (REMAP4)—Offset 370h

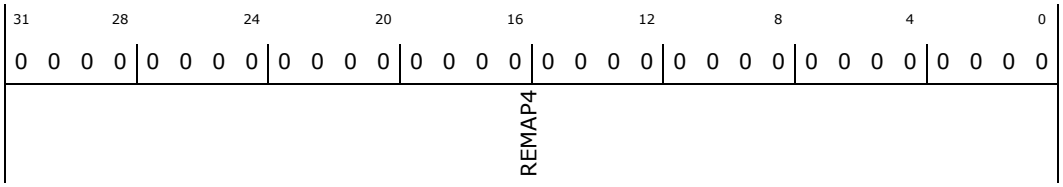
REMAP4

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 370h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**REMAP4:** ish_clk

12.2.222 reg_REMAP5_type (REMAP5)—Offset 374h

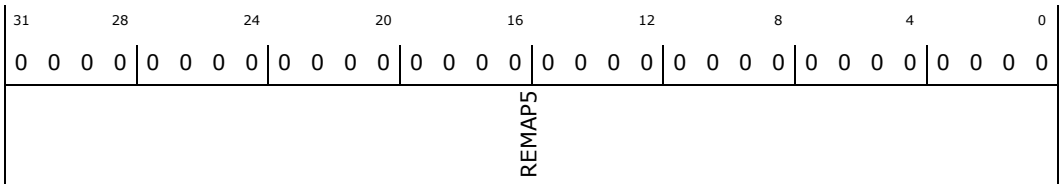
REMAP5

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 374h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**REMAP5:** ish_clk

12.2.223 reg_ISH_IPC_BUSY_CLEAR_type (ISH_IPC_BUSY_CLEAR)—Offset 378h

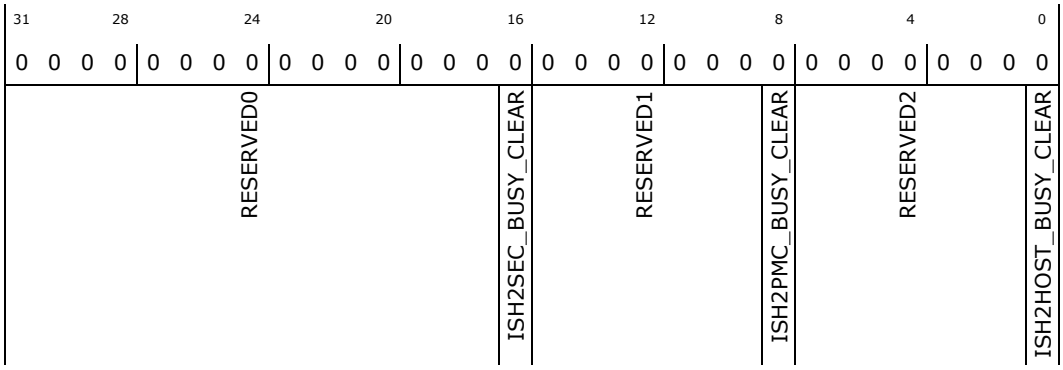
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 378h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RESERVED0:** ish_clk
16	0x0 RW/1C	**ISH2SEC_BUSY_CLEAR:** ish_clk
15:9	0x0 RO	**RESERVED1:** ish_clk
8	0x0 RW/1C	**ISH2PMC_BUSY_CLEAR:** ish_clk
7:1	0x0 RO	**RESERVED2:** ish_clk
0	0x0 RW/1C	**ISH2HOST_BUSY_CLEAR:** ish_clk

12.2.224 reg_ISH_FUSE_type (ISH_FUSE)—Offset 37Ch

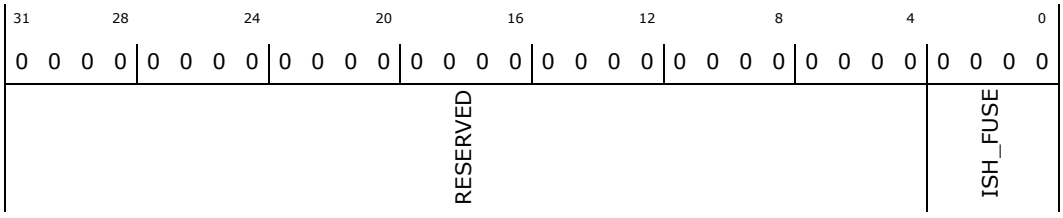
Reserved

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 37Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RESERVED:** ish_clk

Bit Range	Default & Access	Field Name (ID): Description
3:0	0x0 RO	**ISH_FUSE:** ish_clk

12.2.225 reg_UMA_RANGE_LOWER_0_type (UMA_RANGE_LOWER_0)—Offset 380h

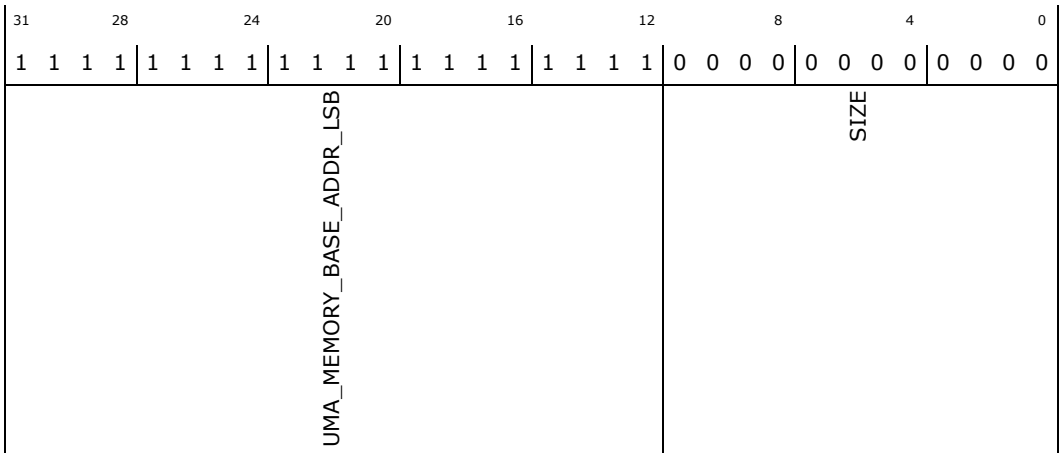
UMA base address LSB register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 380h

Default: FFFFF000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0xfffff RW	**UMA_MEMORY_BASE_ADDR_LSB:** ish_clk
11:0	0x0 RO	**SIZE:** ish_clk

12.2.226 reg_UMA_RANGE_LOWER_1_type (UMA_RANGE_LOWER_1)—Offset 384h

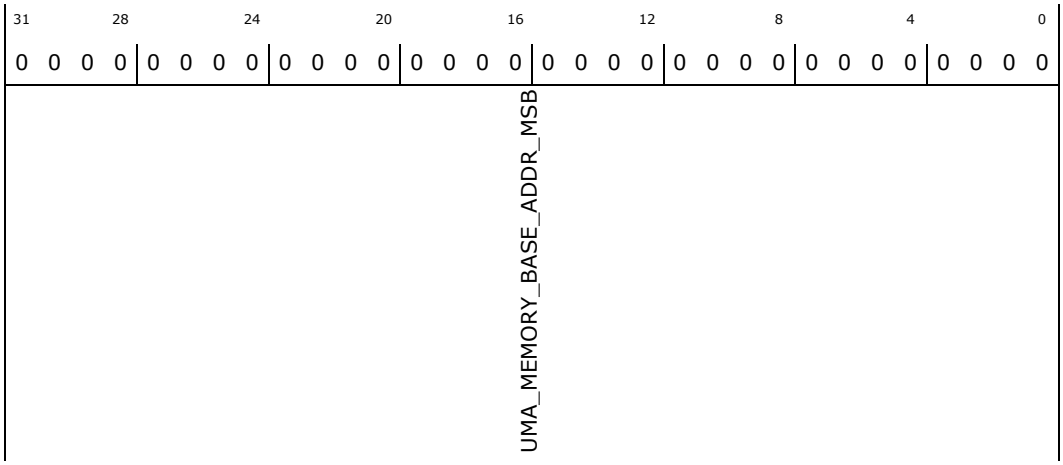
UMA base address MSB register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 384h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**UMA_MEMORY_BASE_ADDR_MSB:** ish_clk

12.2.227 reg_UMA_RANGE_UPPER_0_type (UMA_RANGE_UPPER_0)—Offset 388h

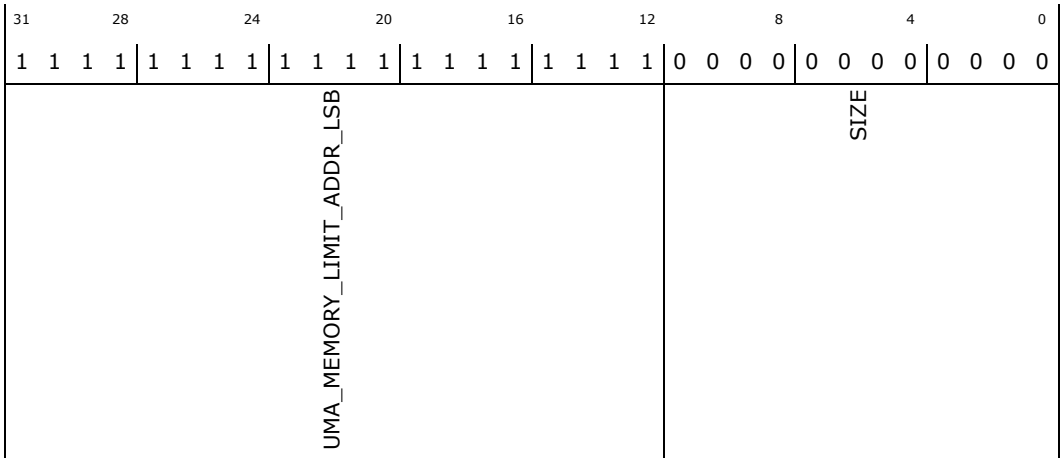
UMA limit address LSB register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 388h

Default: FFFFF000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0xfffff RW	**UMA_MEMORY_LIMIT_ADDR_LSB:** ish_clk
11:0	0x0 RO	**SIZE:** ish_clk

12.2.228 reg_UMA_RANGE_UPPER_1_type (UMA_RANGE_UPPER_1)—Offset 38Ch

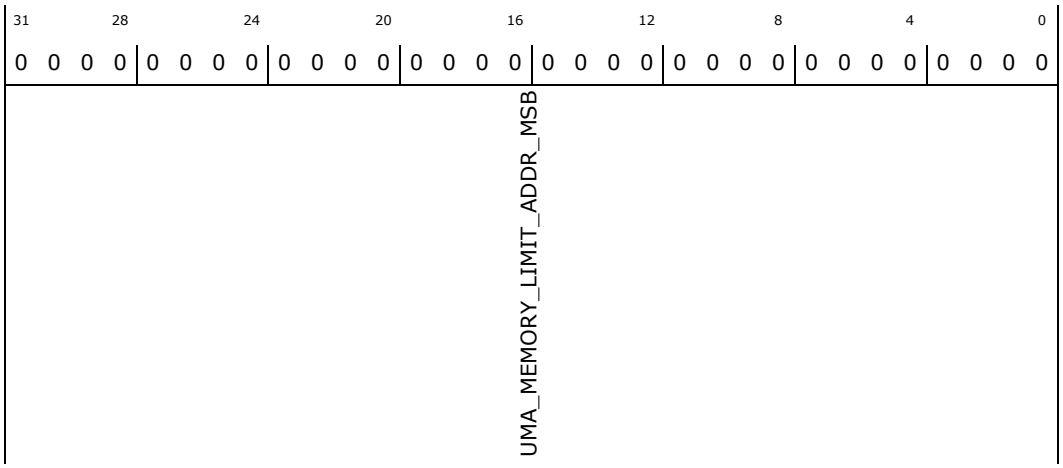
UMA limit address MSB register

Access Method

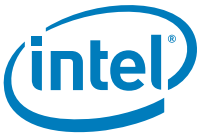
Type: Memory Mapped I/O Register (Size: 32 bits)

Offset: [IOSF2OCP_PCI_cfg.BAR] + 38Ch

Default: 00000000h



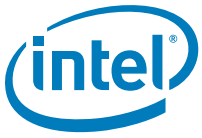
Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**UMA_MEMORY_LIMIT_ADDR_MSB:** ish_clk



12.3 ISH IPC Private Configuration Registers

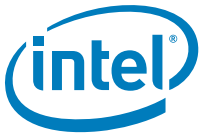
Table 122. Summary of ISH IPC Private Configuration Registers—0xB1

Offset	Register Name (Register Symbol)	Default Value
1000–1003h	"reg_PISR_type (PISR)—Offset 1000h" on page 6425	00000000h
1004–1007h	"reg_PIMR_type (PIMR)—Offset 1004h" on page 6425	00000000h
1008–100Bh	"reg_RESERVED0_type (RESERVED0)—Offset 1008h" on page 6426	00000000h
100C–100Fh	"reg_RESERVED1_type (RESERVED1)—Offset 100Ch" on page 6427	00000000h
1010–1013h	"reg_RESERVED2_type (RESERVED2)—Offset 1010h" on page 6427	00000000h
1014–1017h	"reg_RESERVED3_type (RESERVED3)—Offset 1014h" on page 6428	00000000h
1018–101Bh	"reg_RESERVED4_type (RESERVED4)—Offset 1018h" on page 6428	00000000h
101C–101Fh	"reg_RESERVED5_type (RESERVED5)—Offset 101Ch" on page 6429	00000000h
1020–1023h	"reg_RESERVED6_type (RESERVED6)—Offset 1020h" on page 6429	00000000h
1024–1027h	"reg_RESERVED7_type (RESERVED7)—Offset 1024h" on page 6430	00000000h
1028–102Bh	"reg_RESERVED8_type (RESERVED8)—Offset 1028h" on page 6430	00000000h
102C–102Fh	"reg_RESERVED9_type (RESERVED9)—Offset 102Ch" on page 6431	00000000h
1030–1033h	"reg_RESERVED10_type (RESERVED10)—Offset 1030h" on page 6431	00000000h
1034–1037h	"reg_ISH_HOST_FWSTS_type (ISH_HOST_FWSTS)—Offset 1034h" on page 6432	00000000h
1038–103Bh	"reg_HOST_COMM_type (HOST_COMM)—Offset 1038h" on page 6432	00000000h
103C–103Fh	"reg_ISH_SEC_FWSTS_type (ISH_SEC_FWSTS)—Offset 103Ch" on page 6433	00000000h
1040–1043h	"reg_SEC_COMM_type (SEC_COMM)—Offset 1040h" on page 6433	00000000h
1044–1047h	"reg_ISH_RST_type (ISH_RST)—Offset 1044h" on page 6434	00000000h
1048–104Bh	"reg_HOST2ISH_DOORBELL_type (HOST2ISH_DOORBELL)—Offset 1048h" on page 6434	00000000h
104C–104Fh	"reg_PMC2ISH_DOORBELL_type (PMC2ISH_DOORBELL)—Offset 104Ch" on page 6435	00000000h



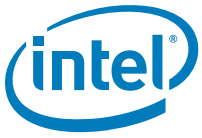
Offset	Register Name (Register Symbol)	Default Value
1050–1053h	"reg_SEC2ISH_DOORBELL_type (SEC2ISH_DOORBELL)—Offset 1050h" on page 6436	00000000h
1054–1057h	"reg_ISH2HOST_DOORBELL_type (ISH2HOST_DOORBELL)—Offset 1054h" on page 6436	00000000h
1058–105Bh	"reg_ISH2PMC_DOORBELL_type (ISH2PMC_DOORBELL)—Offset 1058h" on page 6437	00000000h
105C–105Fh	"reg_ISH2SEC_DOORBELL_type (ISH2SEC_DOORBELL)—Offset 105Ch" on page 6437	00000000h
1060–1063h	"reg_ISH2HOST_MSG1_type (ISH2HOST_MSG1)—Offset 1060h" on page 6438	00000000h
1064–1067h	"reg_ISH2HOST_MSG2_type (ISH2HOST_MSG2)—Offset 1064h" on page 6439	00000000h
1068–106Bh	"reg_ISH2HOST_MSG3_type (ISH2HOST_MSG3)—Offset 1068h" on page 6439	00000000h
106C–106Fh	"reg_ISH2HOST_MSG4_type (ISH2HOST_MSG4)—Offset 106Ch" on page 6439	00000000h
1070–1073h	"reg_ISH2HOST_MSG5_type (ISH2HOST_MSG5)—Offset 1070h" on page 6440	00000000h
1074–1077h	"reg_ISH2HOST_MSG6_type (ISH2HOST_MSG6)—Offset 1074h" on page 6440	00000000h
1078–107Bh	"reg_ISH2HOST_MSG7_type (ISH2HOST_MSG7)—Offset 1078h" on page 6441	00000000h
107C–107Fh	"reg_ISH2HOST_MSG8_type (ISH2HOST_MSG8)—Offset 107Ch" on page 6441	00000000h
1080–1083h	"reg_ISH2HOST_MSG9_type (ISH2HOST_MSG9)—Offset 1080h" on page 6442	00000000h
1084–1087h	"reg_ISH2HOST_MSG10_type (ISH2HOST_MSG10)—Offset 1084h" on page 6442	00000000h
1088–108Bh	"reg_ISH2HOST_MSG11_type (ISH2HOST_MSG11)—Offset 1088h" on page 6443	00000000h
108C–108Fh	"reg_ISH2HOST_MSG12_type (ISH2HOST_MSG12)—Offset 108Ch" on page 6443	00000000h
1090–1093h	"reg_ISH2HOST_MSG13_type (ISH2HOST_MSG13)—Offset 1090h" on page 6444	00000000h
1094–1097h	"reg_ISH2HOST_MSG14_type (ISH2HOST_MSG14)—Offset 1094h" on page 6444	00000000h
1098–109Bh	"reg_ISH2HOST_MSG15_type (ISH2HOST_MSG15)—Offset 1098h" on page 6445	00000000h
109C–109Fh	"reg_ISH2HOST_MSG16_type (ISH2HOST_MSG16)—Offset 109Ch" on page 6445	00000000h
10A0–10A3h	"reg_ISH2HOST_MSG17_type (ISH2HOST_MSG17)—Offset 10A0h" on page 6446	00000000h
10A4–10A7h	"reg_ISH2HOST_MSG18_type (ISH2HOST_MSG18)—Offset 10A4h" on page 6446	00000000h

Offset	Register Name (Register Symbol)	Default Value
10A8–10ABh	"reg_ISH2HOST_MSG19_type (ISH2HOST_MSG19)—Offset 10A8h" on page 6447	00000000h
10AC–10AFh	"reg_ISH2HOST_MSG20_type (ISH2HOST_MSG20)—Offset 10ACh" on page 6447	00000000h
10B0–10B3h	"reg_ISH2HOST_MSG21_type (ISH2HOST_MSG21)—Offset 10B0h" on page 6448	00000000h
10B4–10B7h	"reg_ISH2HOST_MSG22_type (ISH2HOST_MSG22)—Offset 10B4h" on page 6448	00000000h
10B8–10BBh	"reg_ISH2HOST_MSG23_type (ISH2HOST_MSG23)—Offset 10B8h" on page 6449	00000000h
10BC–10BFh	"reg_ISH2HOST_MSG24_type (ISH2HOST_MSG24)—Offset 10BCh" on page 6449	00000000h
10C0–10C3h	"reg_ISH2HOST_MSG25_type (ISH2HOST_MSG25)—Offset 10C0h" on page 6450	00000000h
10C4–10C7h	"reg_ISH2HOST_MSG26_type (ISH2HOST_MSG26)—Offset 10C4h" on page 6450	00000000h
10C8–10CBh	"reg_ISH2HOST_MSG27_type (ISH2HOST_MSG27)—Offset 10C8h" on page 6451	00000000h
10CC–10CFh	"reg_ISH2HOST_MSG28_type (ISH2HOST_MSG28)—Offset 10CCh" on page 6451	00000000h
10D0–10D3h	"reg_ISH2HOST_MSG29_type (ISH2HOST_MSG29)—Offset 10D0h" on page 6452	00000000h
10D4–10D7h	"reg_ISH2HOST_MSG30_type (ISH2HOST_MSG30)—Offset 10D4h" on page 6452	00000000h
10D8–10DBh	"reg_ISH2HOST_MSG31_type (ISH2HOST_MSG31)—Offset 10D8h" on page 6453	00000000h
10DC–10DFh	"reg_ISH2HOST_MSG32_type (ISH2HOST_MSG32)—Offset 10DCh" on page 6453	00000000h
10E0–10E3h	"reg_HOST2ISH_MSG1_type (HOST2ISH_MSG1)—Offset 10E0h" on page 6454	00000000h
10E4–10E7h	"reg_HOST2ISH_MSG2_type (HOST2ISH_MSG2)—Offset 10E4h" on page 6454	00000000h
10E8–10EBh	"reg_HOST2ISH_MSG3_type (HOST2ISH_MSG3)—Offset 10E8h" on page 6455	00000000h
10EC–10EFh	"reg_HOST2ISH_MSG4_type (HOST2ISH_MSG4)—Offset 10ECh" on page 6455	00000000h
10F0–10F3h	"reg_HOST2ISH_MSG5_type (HOST2ISH_MSG5)—Offset 10F0h" on page 6456	00000000h
10F4–10F7h	"reg_HOST2ISH_MSG6_type (HOST2ISH_MSG6)—Offset 10F4h" on page 6456	00000000h
10F8–10FBh	"reg_HOST2ISH_MSG7_type (HOST2ISH_MSG7)—Offset 10F8h" on page 6457	00000000h
10FC–10FFh	"reg_HOST2ISH_MSG8_type (HOST2ISH_MSG8)—Offset 10FCh" on page 6457	00000000h

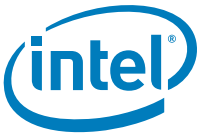


Offset	Register Name (Register Symbol)	Default Value
1100–1103h	"reg_HOST2ISH_MSG9_type (HOST2ISH_MSG9)—Offset 1100h" on page 6458	00000000h
1104–1107h	"reg_HOST2ISH_MSG10_type (HOST2ISH_MSG10)—Offset 1104h" on page 6458	00000000h
1108–110Bh	"reg_HOST2ISH_MSG11_type (HOST2ISH_MSG11)—Offset 1108h" on page 6459	00000000h
110C–110Fh	"reg_HOST2ISH_MSG12_type (HOST2ISH_MSG12)—Offset 110Ch" on page 6459	00000000h
1110–1113h	"reg_HOST2ISH_MSG13_type (HOST2ISH_MSG13)—Offset 1110h" on page 6460	00000000h
1114–1117h	"reg_HOST2ISH_MSG14_type (HOST2ISH_MSG14)—Offset 1114h" on page 6460	00000000h
1118–111Bh	"reg_HOST2ISH_MSG15_type (HOST2ISH_MSG15)—Offset 1118h" on page 6461	00000000h
111C–111Fh	"reg_HOST2ISH_MSG16_type (HOST2ISH_MSG16)—Offset 111Ch" on page 6461	00000000h
1120–1123h	"reg_HOST2ISH_MSG17_type (HOST2ISH_MSG17)—Offset 1120h" on page 6462	00000000h
1124–1127h	"reg_HOST2ISH_MSG18_type (HOST2ISH_MSG18)—Offset 1124h" on page 6462	00000000h
1128–112Bh	"reg_HOST2ISH_MSG19_type (HOST2ISH_MSG19)—Offset 1128h" on page 6463	00000000h
112C–112Fh	"reg_HOST2ISH_MSG20_type (HOST2ISH_MSG20)—Offset 112Ch" on page 6463	00000000h
1130–1133h	"reg_HOST2ISH_MSG21_type (HOST2ISH_MSG21)—Offset 1130h" on page 6464	00000000h
1134–1137h	"reg_HOST2ISH_MSG22_type (HOST2ISH_MSG22)—Offset 1134h" on page 6464	00000000h
1138–113Bh	"reg_HOST2ISH_MSG23_type (HOST2ISH_MSG23)—Offset 1138h" on page 6465	00000000h
113C–113Fh	"reg_HOST2ISH_MSG24_type (HOST2ISH_MSG24)—Offset 113Ch" on page 6465	00000000h
1140–1143h	"reg_HOST2ISH_MSG25_type (HOST2ISH_MSG25)—Offset 1140h" on page 6466	00000000h
1144–1147h	"reg_HOST2ISH_MSG26_type (HOST2ISH_MSG26)—Offset 1144h" on page 6466	00000000h
1148–114Bh	"reg_HOST2ISH_MSG27_type (HOST2ISH_MSG27)—Offset 1148h" on page 6467	00000000h
114C–114Fh	"reg_HOST2ISH_MSG28_type (HOST2ISH_MSG28)—Offset 114Ch" on page 6467	00000000h
1150–1153h	"reg_HOST2ISH_MSG29_type (HOST2ISH_MSG29)—Offset 1150h" on page 6468	00000000h
1154–1157h	"reg_HOST2ISH_MSG30_type (HOST2ISH_MSG30)—Offset 1154h" on page 6468	00000000h

Offset	Register Name (Register Symbol)	Default Value
1158–115Bh	"reg_HOST2ISH_MSG31_type (HOST2ISH_MSG31)—Offset 1158h" on page 6469	00000000h
115C–115Fh	"reg_HOST2ISH_MSG32_type (HOST2ISH_MSG32)—Offset 115Ch" on page 6469	00000000h
1160–1163h	"reg_ISH2SEC_MSG1_type (ISH2SEC_MSG1)—Offset 1160h" on page 6470	00000000h
1164–1167h	"reg_ISH2SEC_MSG2_type (ISH2SEC_MSG2)—Offset 1164h" on page 6470	00000000h
1168–116Bh	"reg_ISH2SEC_MSG3_type (ISH2SEC_MSG3)—Offset 1168h" on page 6471	00000000h
116C–116Fh	"reg_ISH2SEC_MSG4_type (ISH2SEC_MSG4)—Offset 116Ch" on page 6471	00000000h
1170–1173h	"reg_ISH2SEC_MSG5_type (ISH2SEC_MSG5)—Offset 1170h" on page 6472	00000000h
1174–1177h	"reg_ISH2SEC_MSG6_type (ISH2SEC_MSG6)—Offset 1174h" on page 6472	00000000h
1178–117Bh	"reg_ISH2SEC_MSG7_type (ISH2SEC_MSG7)—Offset 1178h" on page 6473	00000000h
117C–117Fh	"reg_ISH2SEC_MSG8_type (ISH2SEC_MSG8)—Offset 117Ch" on page 6473	00000000h
1180–1183h	"reg_ISH2SEC_MSG9_type (ISH2SEC_MSG9)—Offset 1180h" on page 6474	00000000h
1184–1187h	"reg_ISH2SEC_MSG10_type (ISH2SEC_MSG10)—Offset 1184h" on page 6474	00000000h
1188–118Bh	"reg_ISH2SEC_MSG11_type (ISH2SEC_MSG11)—Offset 1188h" on page 6475	00000000h
118C–118Fh	"reg_ISH2SEC_MSG12_type (ISH2SEC_MSG12)—Offset 118Ch" on page 6475	00000000h
1190–1193h	"reg_ISH2SEC_MSG13_type (ISH2SEC_MSG13)—Offset 1190h" on page 6476	00000000h
1194–1197h	"reg_ISH2SEC_MSG14_type (ISH2SEC_MSG14)—Offset 1194h" on page 6476	00000000h
1198–119Bh	"reg_ISH2SEC_MSG15_type (ISH2SEC_MSG15)—Offset 1198h" on page 6477	00000000h
119C–119Fh	"reg_ISH2SEC_MSG16_type (ISH2SEC_MSG16)—Offset 119Ch" on page 6477	00000000h
11A0–11A3h	"reg_ISH2SEC_MSG17_type (ISH2SEC_MSG17)—Offset 11A0h" on page 6478	00000000h
11A4–11A7h	"reg_ISH2SEC_MSG18_type (ISH2SEC_MSG18)—Offset 11A4h" on page 6478	00000000h
11A8–11ABh	"reg_ISH2SEC_MSG19_type (ISH2SEC_MSG19)—Offset 11A8h" on page 6479	00000000h
11AC–11AFh	"reg_ISH2SEC_MSG20_type (ISH2SEC_MSG20)—Offset 11ACh" on page 6479	00000000h

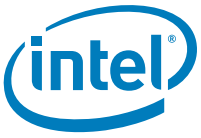


Offset	Register Name (Register Symbol)	Default Value
11B0–11B3h	"reg_ISH2SEC_MSG21_type (ISH2SEC_MSG21)—Offset 11B0h" on page 6480	00000000h
11B4–11B7h	"reg_ISH2SEC_MSG22_type (ISH2SEC_MSG22)—Offset 11B4h" on page 6480	00000000h
11B8–11BBh	"reg_ISH2SEC_MSG23_type (ISH2SEC_MSG23)—Offset 11B8h" on page 6481	00000000h
11BC–11BFh	"reg_ISH2SEC_MSG24_type (ISH2SEC_MSG24)—Offset 11BCh" on page 6481	00000000h
11C0–11C3h	"reg_ISH2SEC_MSG25_type (ISH2SEC_MSG25)—Offset 11C0h" on page 6482	00000000h
11C4–11C7h	"reg_ISH2SEC_MSG26_type (ISH2SEC_MSG26)—Offset 11C4h" on page 6482	00000000h
11C8–11CBh	"reg_ISH2SEC_MSG27_type (ISH2SEC_MSG27)—Offset 11C8h" on page 6483	00000000h
11CC–11CFh	"reg_ISH2SEC_MSG28_type (ISH2SEC_MSG28)—Offset 11CCh" on page 6483	00000000h
11D0–11D3h	"reg_ISH2SEC_MSG29_type (ISH2SEC_MSG29)—Offset 11D0h" on page 6484	00000000h
11D4–11D7h	"reg_ISH2SEC_MSG30_type (ISH2SEC_MSG30)—Offset 11D4h" on page 6484	00000000h
11D8–11DBh	"reg_ISH2SEC_MSG31_type (ISH2SEC_MSG31)—Offset 11D8h" on page 6485	00000000h
11DC–11DFh	"reg_ISH2SEC_MSG32_type (ISH2SEC_MSG32)—Offset 11DCh" on page 6485	00000000h
11E0–11E3h	"reg_SEC2ISH_MSG1_type (SEC2ISH_MSG1)—Offset 11E0h" on page 6486	00000000h
11E4–11E7h	"reg_SEC2ISH_MSG2_type (SEC2ISH_MSG2)—Offset 11E4h" on page 6486	00000000h
11E8–11EBh	"reg_SEC2ISH_MSG3_type (SEC2ISH_MSG3)—Offset 11E8h" on page 6487	00000000h
11EC–11EFh	"reg_SEC2ISH_MSG4_type (SEC2ISH_MSG4)—Offset 11ECh" on page 6487	00000000h
11F0–11F3h	"reg_SEC2ISH_MSG5_type (SEC2ISH_MSG5)—Offset 11F0h" on page 6488	00000000h
11F4–11F7h	"reg_SEC2ISH_MSG6_type (SEC2ISH_MSG6)—Offset 11F4h" on page 6488	00000000h
11F8–11FBh	"reg_SEC2ISH_MSG7_type (SEC2ISH_MSG7)—Offset 11F8h" on page 6489	00000000h
11FC–11FFh	"reg_SEC2ISH_MSG8_type (SEC2ISH_MSG8)—Offset 11FCh" on page 6489	00000000h
1200–1203h	"reg_SEC2ISH_MSG9_type (SEC2ISH_MSG9)—Offset 1200h" on page 6490	00000000h
1204–1207h	"reg_SEC2ISH_MSG10_type (SEC2ISH_MSG10)—Offset 1204h" on page 6490	00000000h

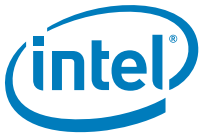


Offset	Register Name (Register Symbol)	Default Value
1208–120Bh	"reg_SEC2ISH_MSG11_type (SEC2ISH_MSG11)—Offset 1208h" on page 6491	00000000h
120C–120Fh	"reg_SEC2ISH_MSG12_type (SEC2ISH_MSG12)—Offset 120Ch" on page 6491	00000000h
1210–1213h	"reg_SEC2ISH_MSG13_type (SEC2ISH_MSG13)—Offset 1210h" on page 6492	00000000h
1214–1217h	"reg_SEC2ISH_MSG14_type (SEC2ISH_MSG14)—Offset 1214h" on page 6492	00000000h
1218–121Bh	"reg_SEC2ISH_MSG15_type (SEC2ISH_MSG15)—Offset 1218h" on page 6493	00000000h
121C–121Fh	"reg_SEC2ISH_MSG16_type (SEC2ISH_MSG16)—Offset 121Ch" on page 6493	00000000h
1220–1223h	"reg_SEC2ISH_MSG17_type (SEC2ISH_MSG17)—Offset 1220h" on page 6494	00000000h
1224–1227h	"reg_SEC2ISH_MSG18_type (SEC2ISH_MSG18)—Offset 1224h" on page 6494	00000000h
1228–122Bh	"reg_SEC2ISH_MSG19_type (SEC2ISH_MSG19)—Offset 1228h" on page 6495	00000000h
122C–122Fh	"reg_SEC2ISH_MSG20_type (SEC2ISH_MSG20)—Offset 122Ch" on page 6495	00000000h
1230–1233h	"reg_SEC2ISH_MSG21_type (SEC2ISH_MSG21)—Offset 1230h" on page 6496	00000000h
1234–1237h	"reg_SEC2ISH_MSG22_type (SEC2ISH_MSG22)—Offset 1234h" on page 6496	00000000h
1238–123Bh	"reg_SEC2ISH_MSG23_type (SEC2ISH_MSG23)—Offset 1238h" on page 6497	00000000h
123C–123Fh	"reg_SEC2ISH_MSG24_type (SEC2ISH_MSG24)—Offset 123Ch" on page 6497	00000000h
1240–1243h	"reg_SEC2ISH_MSG25_type (SEC2ISH_MSG25)—Offset 1240h" on page 6498	00000000h
1244–1247h	"reg_SEC2ISH_MSG26_type (SEC2ISH_MSG26)—Offset 1244h" on page 6498	00000000h
1248–124Bh	"reg_SEC2ISH_MSG27_type (SEC2ISH_MSG27)—Offset 1248h" on page 6499	00000000h
124C–124Fh	"reg_SEC2ISH_MSG28_type (SEC2ISH_MSG28)—Offset 124Ch" on page 6499	00000000h
1250–1253h	"reg_SEC2ISH_MSG29_type (SEC2ISH_MSG29)—Offset 1250h" on page 6500	00000000h
1254–1257h	"reg_SEC2ISH_MSG30_type (SEC2ISH_MSG30)—Offset 1254h" on page 6500	00000000h
1258–125Bh	"reg_SEC2ISH_MSG31_type (SEC2ISH_MSG31)—Offset 1258h" on page 6501	00000000h
125C–125Fh	"reg_SEC2ISH_MSG32_type (SEC2ISH_MSG32)—Offset 125Ch" on page 6501	00000000h

Offset	Register Name (Register Symbol)	Default Value
1260–1263h	"reg_ISH2PMC_MSG1_type (ISH2PMC_MSG1)—Offset 1260h" on page 6502	00000000h
1264–1267h	"reg_ISH2PMC_MSG2_type (ISH2PMC_MSG2)—Offset 1264h" on page 6502	00000000h
1268–126Bh	"reg_ISH2PMC_MSG3_type (ISH2PMC_MSG3)—Offset 1268h" on page 6503	00000000h
126C–126Fh	"reg_ISH2PMC_MSG4_type (ISH2PMC_MSG4)—Offset 126Ch" on page 6503	00000000h
1270–1273h	"reg_ISH2PMC_MSG5_type (ISH2PMC_MSG5)—Offset 1270h" on page 6504	00000000h
1274–1277h	"reg_ISH2PMC_MSG6_type (ISH2PMC_MSG6)—Offset 1274h" on page 6504	00000000h
1278–127Bh	"reg_ISH2PMC_MSG7_type (ISH2PMC_MSG7)—Offset 1278h" on page 6505	00000000h
127C–127Fh	"reg_ISH2PMC_MSG8_type (ISH2PMC_MSG8)—Offset 127Ch" on page 6505	00000000h
1280–1283h	"reg_ISH2PMC_MSG9_type (ISH2PMC_MSG9)—Offset 1280h" on page 6506	00000000h
1284–1287h	"reg_ISH2PMC_MSG10_type (ISH2PMC_MSG10)—Offset 1284h" on page 6506	00000000h
1288–128Bh	"reg_ISH2PMC_MSG11_type (ISH2PMC_MSG11)—Offset 1288h" on page 6507	00000000h
128C–128Fh	"reg_ISH2PMC_MSG12_type (ISH2PMC_MSG12)—Offset 128Ch" on page 6507	00000000h
1290–1293h	"reg_ISH2PMC_MSG13_type (ISH2PMC_MSG13)—Offset 1290h" on page 6508	00000000h
1294–1297h	"reg_ISH2PMC_MSG14_type (ISH2PMC_MSG14)—Offset 1294h" on page 6508	00000000h
1298–129Bh	"reg_ISH2PMC_MSG15_type (ISH2PMC_MSG15)—Offset 1298h" on page 6509	00000000h
129C–129Fh	"reg_ISH2PMC_MSG16_type (ISH2PMC_MSG16)—Offset 129Ch" on page 6509	00000000h
12A0–12A3h	"reg_ISH2PMC_MSG17_type (ISH2PMC_MSG17)—Offset 12A0h" on page 6510	00000000h
12A4–12A7h	"reg_ISH2PMC_MSG18_type (ISH2PMC_MSG18)—Offset 12A4h" on page 6510	00000000h
12A8–12ABh	"reg_ISH2PMC_MSG19_type (ISH2PMC_MSG19)—Offset 12A8h" on page 6511	00000000h
12AC–12AFh	"reg_ISH2PMC_MSG20_type (ISH2PMC_MSG20)—Offset 12ACh" on page 6511	00000000h
12B0–12B3h	"reg_ISH2PMC_MSG21_type (ISH2PMC_MSG21)—Offset 12B0h" on page 6512	00000000h
12B4–12B7h	"reg_ISH2PMC_MSG22_type (ISH2PMC_MSG22)—Offset 12B4h" on page 6512	00000000h



Offset	Register Name (Register Symbol)	Default Value
12B8–12BBh	"reg_ISH2PMC_MSG23_type (ISH2PMC_MSG23)—Offset 12B8h" on page 6513	00000000h
12BC–12BFh	"reg_ISH2PMC_MSG24_type (ISH2PMC_MSG24)—Offset 12BCh" on page 6513	00000000h
12C0–12C3h	"reg_ISH2PMC_MSG25_type (ISH2PMC_MSG25)—Offset 12C0h" on page 6514	00000000h
12C4–12C7h	"reg_ISH2PMC_MSG26_type (ISH2PMC_MSG26)—Offset 12C4h" on page 6514	00000000h
12C8–12CBh	"reg_ISH2PMC_MSG27_type (ISH2PMC_MSG27)—Offset 12C8h" on page 6515	00000000h
12CC–12CFh	"reg_ISH2PMC_MSG28_type (ISH2PMC_MSG28)—Offset 12CCh" on page 6515	00000000h
12D0–12D3h	"reg_ISH2PMC_MSG29_type (ISH2PMC_MSG29)—Offset 12D0h" on page 6516	00000000h
12D4–12D7h	"reg_ISH2PMC_MSG30_type (ISH2PMC_MSG30)—Offset 12D4h" on page 6516	00000000h
12D8–12DBh	"reg_ISH2PMC_MSG31_type (ISH2PMC_MSG31)—Offset 12D8h" on page 6517	00000000h
12DC–12DFh	"reg_ISH2PMC_MSG32_type (ISH2PMC_MSG32)—Offset 12DCh" on page 6517	00000000h
12E0–12E3h	"reg_PMC2ISH_MSG1_type (PMC2ISH_MSG1)—Offset 12E0h" on page 6518	00000000h
12E4–12E7h	"reg_PMC2ISH_MSG2_type (PMC2ISH_MSG2)—Offset 12E4h" on page 6518	00000000h
12E8–12EBh	"reg_PMC2ISH_MSG3_type (PMC2ISH_MSG3)—Offset 12E8h" on page 6519	00000000h
12EC–12EFh	"reg_PMC2ISH_MSG4_type (PMC2ISH_MSG4)—Offset 12ECh" on page 6519	00000000h
12F0–12F3h	"reg_PMC2ISH_MSG5_type (PMC2ISH_MSG5)—Offset 12F0h" on page 6520	00000000h
12F4–12F7h	"reg_PMC2ISH_MSG6_type (PMC2ISH_MSG6)—Offset 12F4h" on page 6520	00000000h
12F8–12FBh	"reg_PMC2ISH_MSG7_type (PMC2ISH_MSG7)—Offset 12F8h" on page 6521	00000000h
12FC–12FFh	"reg_PMC2ISH_MSG8_type (PMC2ISH_MSG8)—Offset 12FCh" on page 6521	00000000h
1300–1303h	"reg_PMC2ISH_MSG9_type (PMC2ISH_MSG9)—Offset 1300h" on page 6522	00000000h
1304–1307h	"reg_PMC2ISH_MSG10_type (PMC2ISH_MSG10)—Offset 1304h" on page 6522	00000000h
1308–130Bh	"reg_PMC2ISH_MSG11_type (PMC2ISH_MSG11)—Offset 1308h" on page 6523	00000000h
130C–130Fh	"reg_PMC2ISH_MSG12_type (PMC2ISH_MSG12)—Offset 130Ch" on page 6523	00000000h



Offset	Register Name (Register Symbol)	Default Value
1310–1313h	"reg_PMC2ISH_MSG13_type (PMC2ISH_MSG13)—Offset 1310h" on page 6524	00000000h
1314–1317h	"reg_PMC2ISH_MSG14_type (PMC2ISH_MSG14)—Offset 1314h" on page 6524	00000000h
1318–131Bh	"reg_PMC2ISH_MSG15_type (PMC2ISH_MSG15)—Offset 1318h" on page 6525	00000000h
131C–131Fh	"reg_PMC2ISH_MSG16_type (PMC2ISH_MSG16)—Offset 131Ch" on page 6525	00000000h
1320–1323h	"reg_PMC2ISH_MSG17_type (PMC2ISH_MSG17)—Offset 1320h" on page 6526	00000000h
1324–1327h	"reg_PMC2ISH_MSG18_type (PMC2ISH_MSG18)—Offset 1324h" on page 6526	00000000h
1328–132Bh	"reg_PMC2ISH_MSG19_type (PMC2ISH_MSG19)—Offset 1328h" on page 6527	00000000h
132C–132Fh	"reg_PMC2ISH_MSG20_type (PMC2ISH_MSG20)—Offset 132Ch" on page 6527	00000000h
1330–1333h	"reg_PMC2ISH_MSG21_type (PMC2ISH_MSG21)—Offset 1330h" on page 6528	00000000h
1334–1337h	"reg_PMC2ISH_MSG22_type (PMC2ISH_MSG22)—Offset 1334h" on page 6528	00000000h
1338–133Bh	"reg_PMC2ISH_MSG23_type (PMC2ISH_MSG23)—Offset 1338h" on page 6529	00000000h
133C–133Fh	"reg_PMC2ISH_MSG24_type (PMC2ISH_MSG24)—Offset 133Ch" on page 6529	00000000h
1340–1343h	"reg_PMC2ISH_MSG25_type (PMC2ISH_MSG25)—Offset 1340h" on page 6530	00000000h
1344–1347h	"reg_PMC2ISH_MSG26_type (PMC2ISH_MSG26)—Offset 1344h" on page 6530	00000000h
1348–134Bh	"reg_PMC2ISH_MSG27_type (PMC2ISH_MSG27)—Offset 1348h" on page 6531	00000000h
134C–134Fh	"reg_PMC2ISH_MSG28_type (PMC2ISH_MSG28)—Offset 134Ch" on page 6531	00000000h
1350–1353h	"reg_PMC2ISH_MSG29_type (PMC2ISH_MSG29)—Offset 1350h" on page 6532	00000000h
1354–1357h	"reg_PMC2ISH_MSG30_type (PMC2ISH_MSG30)—Offset 1354h" on page 6532	00000000h
1358–135Bh	"reg_PMC2ISH_MSG31_type (PMC2ISH_MSG31)—Offset 1358h" on page 6533	00000000h
135C–135Fh	"reg_PMC2ISH_MSG32_type (PMC2ISH_MSG32)—Offset 135Ch" on page 6533	00000000h
1360–1363h	"reg_REMAP0_type (REMAP0)—Offset 1360h" on page 6534	00000000h
1364–1367h	"reg_REMAP1_type (REMAP1)—Offset 1364h" on page 6534	00000000h

Offset	Register Name (Register Symbol)	Default Value
1368–136Bh	"reg_REMAP2_type (REMAP2)—Offset 1368h" on page 6535	00000000h
136C–136Fh	"reg_REMAP3_type (REMAP3)—Offset 136Ch" on page 6535	00000000h
1370–1373h	"reg_REMAP4_type (REMAP4)—Offset 1370h" on page 6536	00000000h
1374–1377h	"reg_REMAP5_type (REMAP5)—Offset 1374h" on page 6536	00000000h
1378–137Bh	"reg_ISH_IPC_BUSY_CLEAR_type (ISH_IPC_BUSY_CLEAR)—Offset 1378h" on page 6537	00000000h
137C–137Fh	"reg_ISH_FUSE_type (ISH_FUSE)—Offset 137Ch" on page 6538	00000000h
1380–1383h	"reg_UMA_RANGE_LOWER_0_type (UMA_RANGE_LOWER_0)—Offset 1380h" on page 6538	FFFFF000h
1384–1387h	"reg_UMA_RANGE_LOWER_1_type (UMA_RANGE_LOWER_1)—Offset 1384h" on page 6539	00000000h
1388–138Bh	"reg_UMA_RANGE_UPPER_0_type (UMA_RANGE_UPPER_0)—Offset 1388h" on page 6540	FFFFF000h
138C–138Fh	"reg_UMA_RANGE_UPPER_1_type (UMA_RANGE_UPPER_1)—Offset 138Ch" on page 6540	00000000h

12.3.1 reg_PISR_type (PISR)—Offset 1000h

Reserved

Access Method

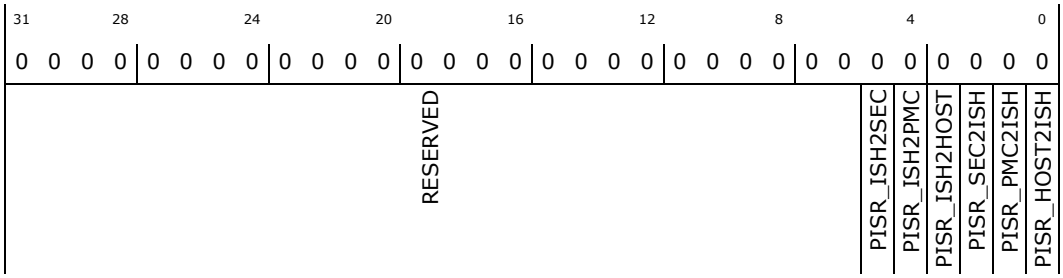
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1000h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**RESERVED:** ish_clk
5	0x0 RO	**PISR_ISH2SEC:** ish_clk
4	0x0 RO	**PISR_ISH2PMC:** ish_clk
3	0x0 RO	**PISR_ISH2HOST:** ish_clk
2	0x0 RO	**PISR_SEC2ISH:** ish_clk
1	0x0 RO	**PISR_PMC2ISH:** ish_clk
0	0x0 RO	**PISR_HOST2ISH:** ish_clk

12.3.2 reg_PIMR_type (PIMR)—Offset 1004h

Reserved

Access Method

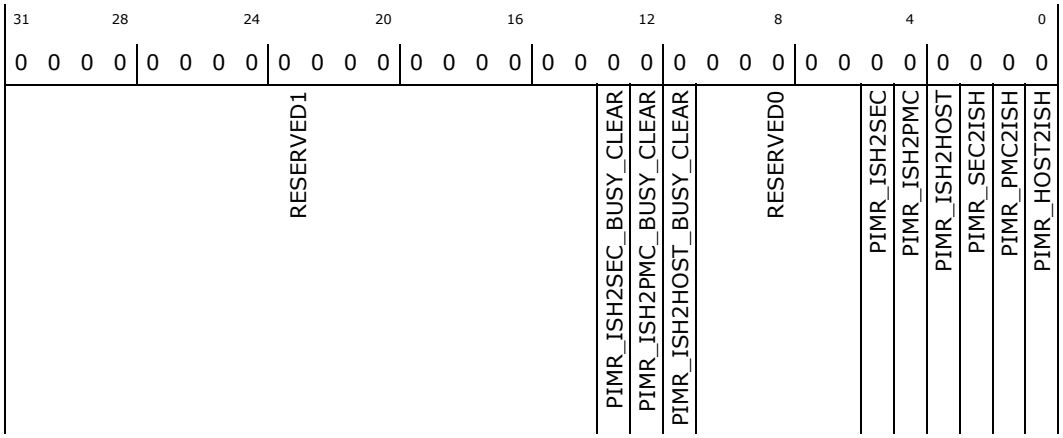
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1004h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0x0 RO	**RESERVED1:** ish_clk
13	0x0 RW	**PIMR_ISH2SEC_BUSY_CLEAR:** ish_clk
12	0x0 RW	**PIMR_ISH2PMC_BUSY_CLEAR:** ish_clk
11	0x0 RW	**PIMR_ISH2HOST_BUSY_CLEAR:** ish_clk
10:6	0x0 RO	**RESERVED0:** ish_clk
5	0x0 RW	**PIMR_ISH2SEC:** ish_clk
4	0x0 RW	**PIMR_ISH2PMC:** ish_clk
3	0x0 RW	**PIMR_ISH2HOST:** ish_clk
2	0x0 RW	**PIMR_SEC2ISH:** ish_clk
1	0x0 RW	**PIMR_PMC2ISH:** ish_clk
0	0x0 RW	**PIMR_HOST2ISH:** ish_clk

12.3.3 reg_RESERVED0_type (RESERVED0)—Offset 1008h

Reserved

Access Method

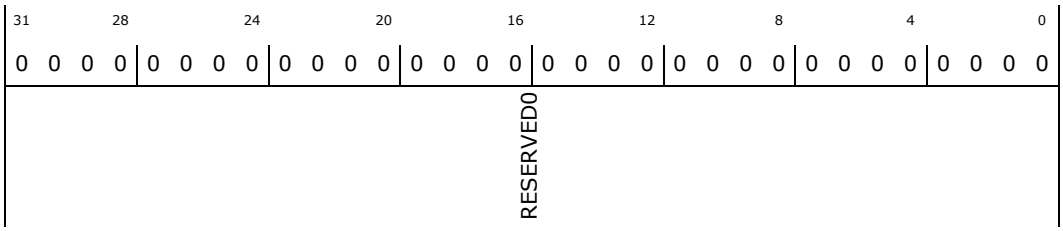
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1008h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED0:** ish_clk

12.3.4 reg_RESERVED1_type (RESERVED1)—Offset 100Ch

Reserved

Access Method

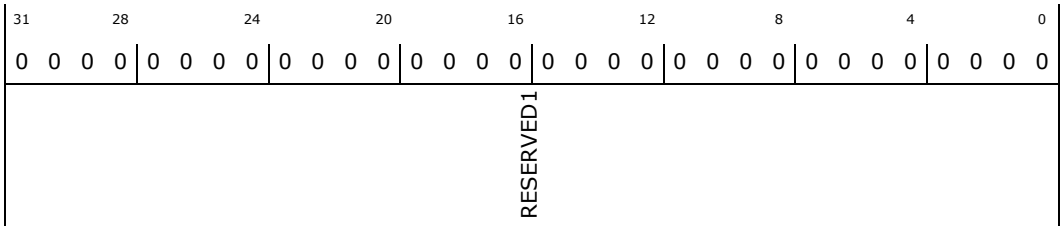
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 100Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED1:** ish_clk

12.3.5 reg_RESERVED2_type (RESERVED2)—Offset 1010h

Reserved

Access Method

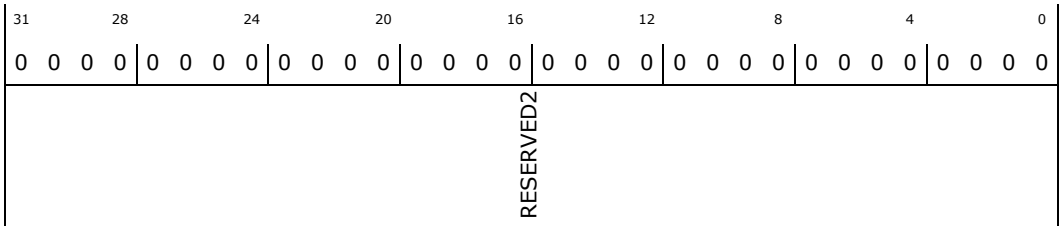
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1010h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED2:** ish_clk

12.3.6 reg_RESERVED3_type (RESERVED3)—Offset 1014h

Reserved

Access Method

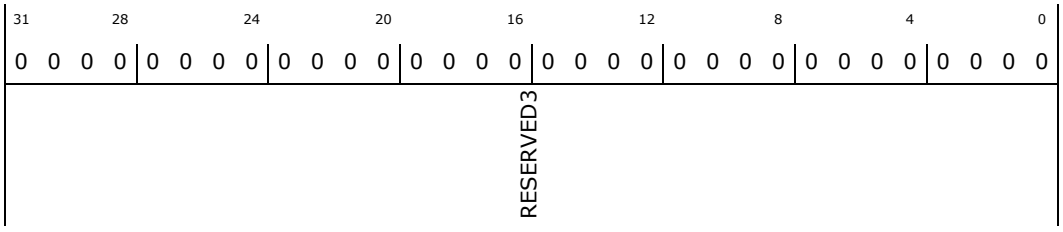
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1014h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED3:** ish_clk

12.3.7 reg_RESERVED4_type (RESERVED4)—Offset 1018h

Reserved

Access Method

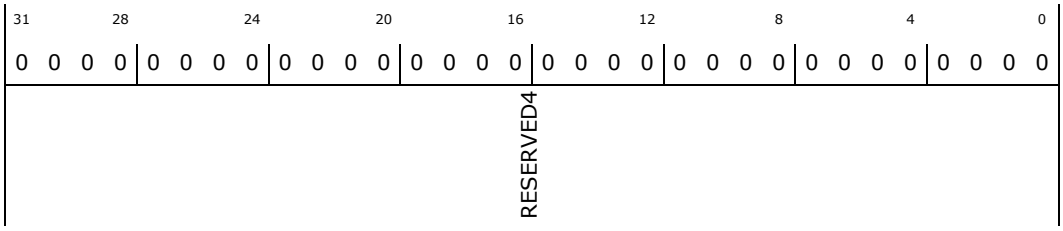
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1018h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED4:** ish_clk

12.3.8 reg_RESERVED5_type (RESERVED5)—Offset 101Ch

Reserved

Access Method

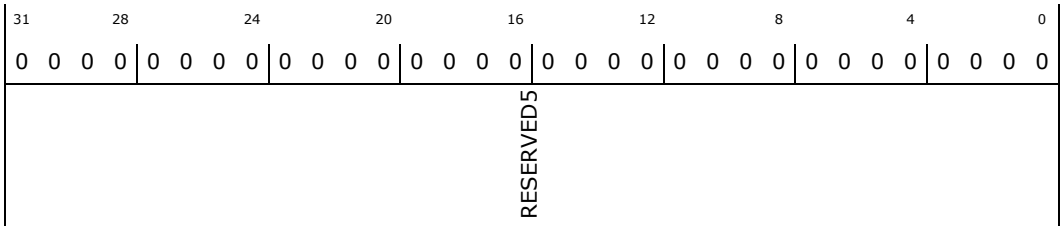
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 101Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED5:** ish_clk

12.3.9 reg_RESERVED6_type (RESERVED6)—Offset 1020h

Reserved

Access Method

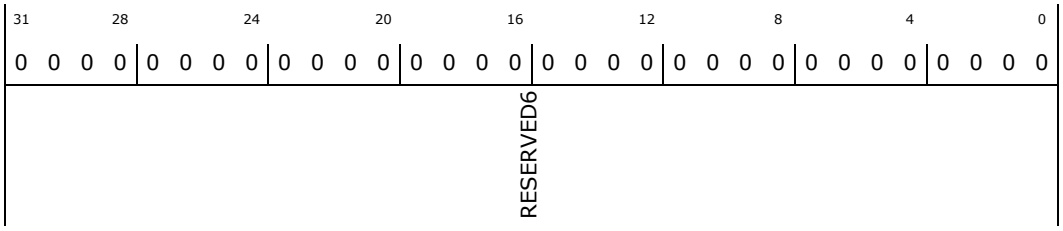
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1020h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED6:** ish_clk

12.3.10 reg_RESERVED7_type (RESERVED7)—Offset 1024h

Reserved

Access Method

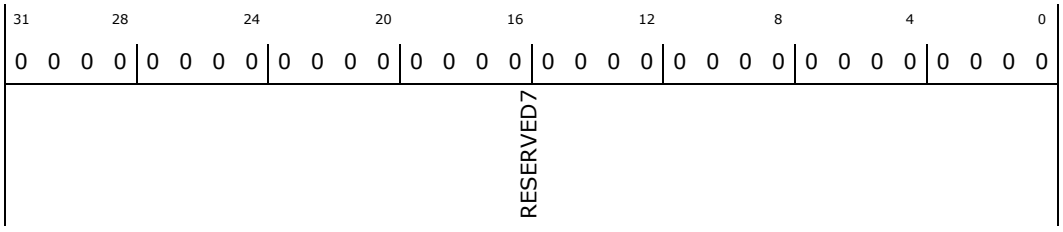
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1024h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED7:** ish_clk

12.3.11 reg_RESERVED8_type (RESERVED8)—Offset 1028h

Reserved

Access Method

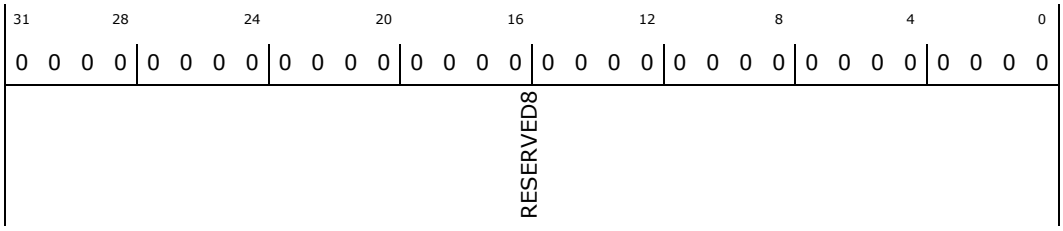
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1028h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED8:** ish_clk

12.3.12 reg_RESERVED9_type (RESERVED9)—Offset 102Ch

Reserved

Access Method

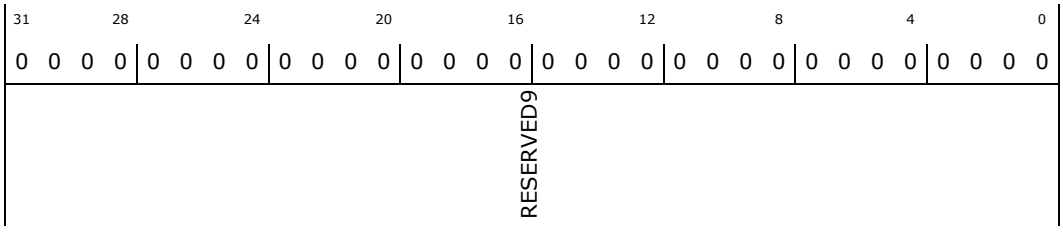
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 102Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED9:** ish_clk

12.3.13 reg_RESERVED10_type (RESERVED10)—Offset 1030h

Reserved

Access Method

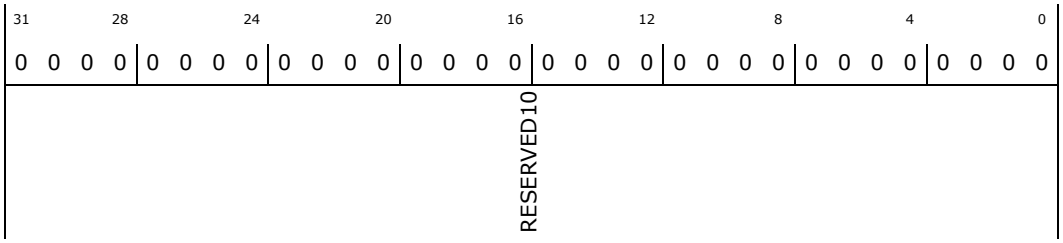
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1030h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 NA	**RESERVED10:** ish_clk

12.3.14 reg_ISH_HOST_FWSTS_type (ISH_HOST_FWSTS)—Offset 1034h

ISH Host firmware status

Access Method

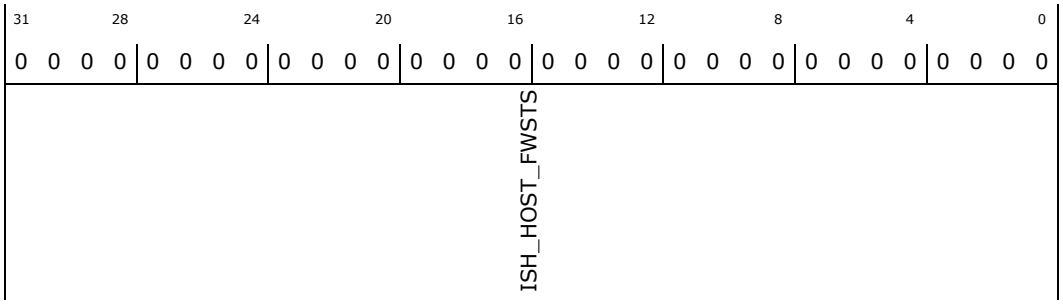
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1034h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**ISH_HOST_FWSTS:** ish_clk

12.3.15 reg_HOST_COMM_type (HOST_COMM)—Offset 1038h

Host communication register

Access Method

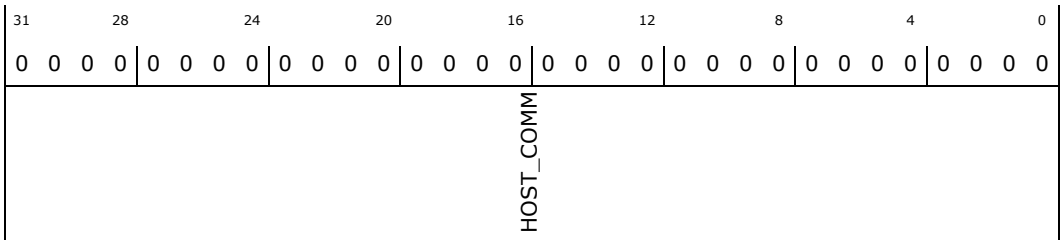
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1038h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**HOST_COMM:** ish_clk

12.3.16 reg_ISH_SEC_FWSTS_type (ISH_SEC_FWSTS)—Offset 103Ch

ISH SEC firmware status

Access Method

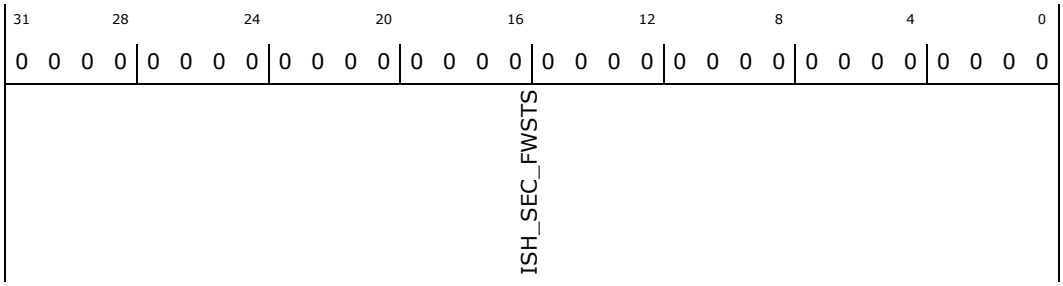
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 103Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**ISH_SEC_FWSTS:** ish_clk

12.3.17 reg_SEC_COMM_type (SEC_COMM)—Offset 1040h

SEC communication register

Access Method

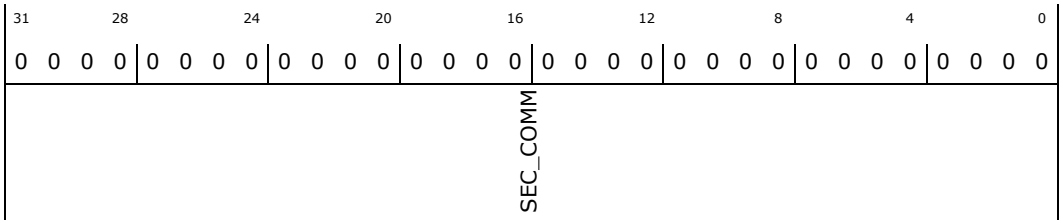
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1040h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SEC_COMM:** ish_clk

12.3.18 reg_ISH_RST_type (ISH_RST)—Offset 1044h

Reset register used to reset minuteIA

Access Method

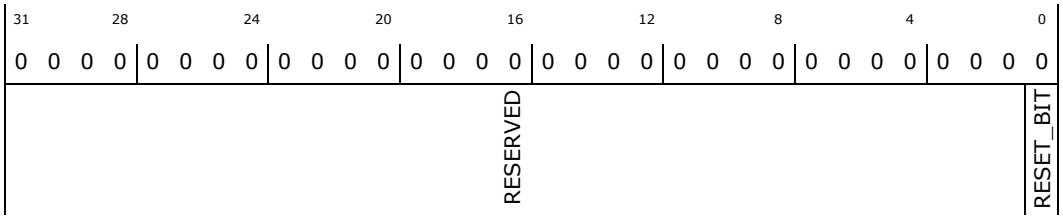
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1044h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**RESERVED:** ish_clk
0	0x0 RW	**RESET_BIT:** ish_clk

12.3.19 reg_HOST2ISH_DOORBELL_type (HOST2ISH_DOORBELL)—Offset 1048h

When this bit is cleared, the ISH CPU is Ready to accept a new message

Access Method

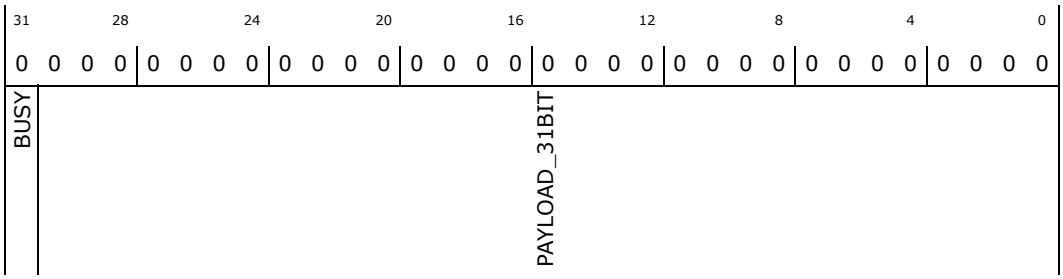
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1048h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**BUSY:** ish_clk
30:0	0x0 RW	**PAYLOAD_31BIT:** ish_clk

12.3.20 reg_PMC2ISH_DOORBELL_type (PMC2ISH_DOORBELL)—Offset 104Ch

When this bit is cleared, the ISH CPU is Ready to accept a new message

Access Method

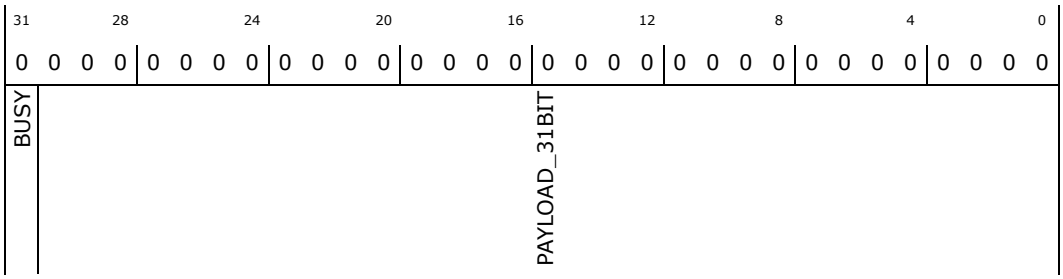
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 104Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**BUSY:** ish_clk

Bit Range	Default & Access	Field Name (ID): Description
30:0	0x0 RW	**PAYLOAD_31BIT:** ish_clk

12.3.21 reg_SEC2ISH_DOORBELL_type (SEC2ISH_DOORBELL)—Offset 1050h

When this bit is cleared, the ISH CPU is Ready to accept a new message

Access Method

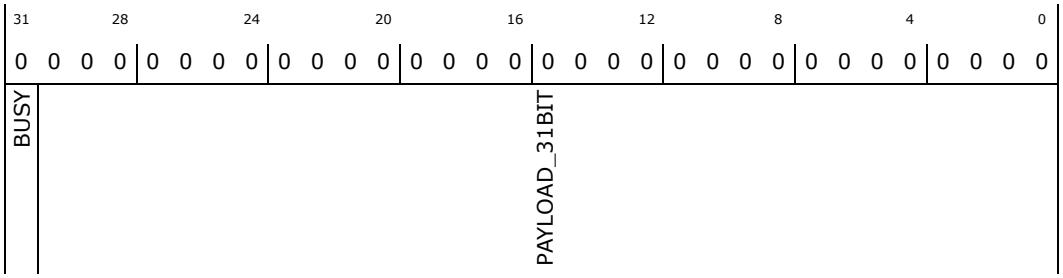
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1050h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**BUSY:** ish_clk
30:0	0x0 RW	**PAYLOAD_31BIT:** ish_clk

12.3.22 reg_ISH2HOST_DOORBELL_type (ISH2HOST_DOORBELL)—Offset 1054h

When this bit is cleared, the HOST CPU is Ready to accept a new message

Access Method

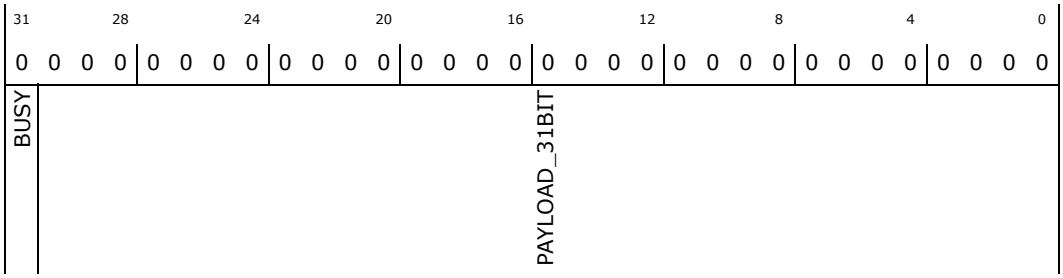
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1054h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**BUSY:** ish_clk
30:0	0x0 RW	**PAYLOAD_31BIT:** ish_clk

12.3.23 reg_ISH2PMC_DOORBELL_type (ISH2PMC_DOORBELL)—Offset 1058h

When this bit is cleared, the PMC CPU is Ready to accept a new message

Access Method

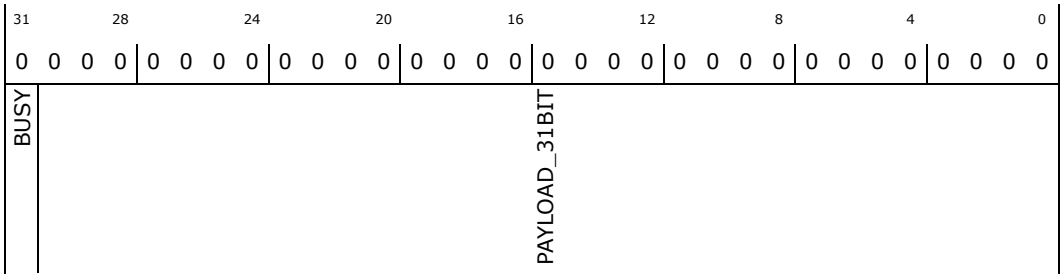
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1058h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**BUSY:** ish_clk
30:0	0x0 RW	**PAYLOAD_31BIT:** ish_clk

12.3.24 reg_ISH2SEC_DOORBELL_type (ISH2SEC_DOORBELL)—Offset 105Ch

When this bit is cleared, the SEC CPU is Ready to accept a new message

Access Method

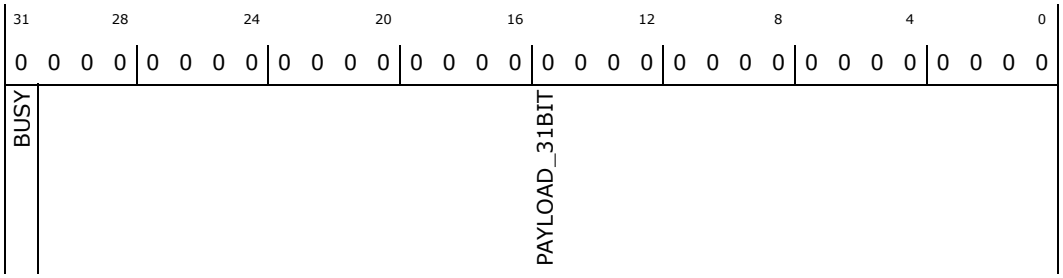
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 105Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0x0 RW	**BUSY:** ish_clk
30:0	0x0 RW	**PAYLOAD_31BIT:** ish_clk

12.3.25 reg_ISH2HOST_MSG1_type (ISH2HOST_MSG1)—Offset 1060h

Message from ISH to HOST

Access Method

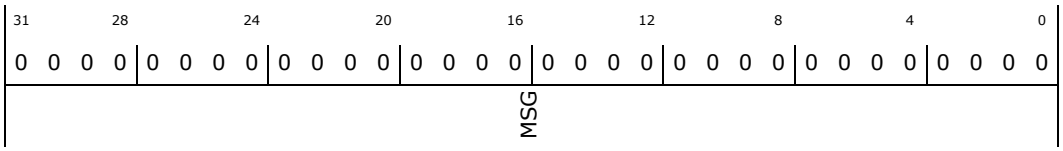
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1060h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.26 reg_ISH2HOST_MSG2_type (ISH2HOST_MSG2)—Offset 1064h

Message from ISH to HOST

Access Method

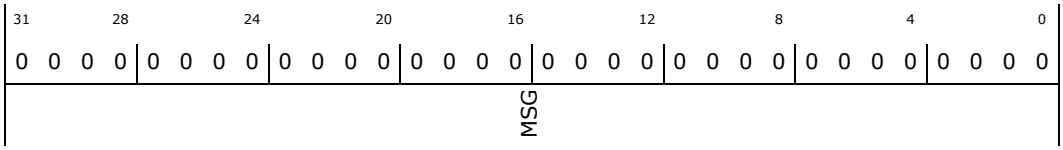
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1064h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.27 reg_ISH2HOST_MSG3_type (ISH2HOST_MSG3)—Offset 1068h

Message from ISH to HOST

Access Method

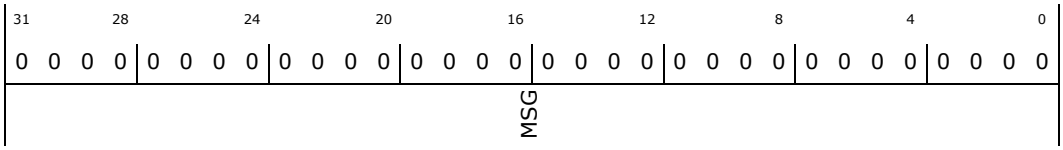
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1068h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.28 reg_ISH2HOST_MSG4_type (ISH2HOST_MSG4)—Offset 106Ch

Message from ISH to HOST

Access Method

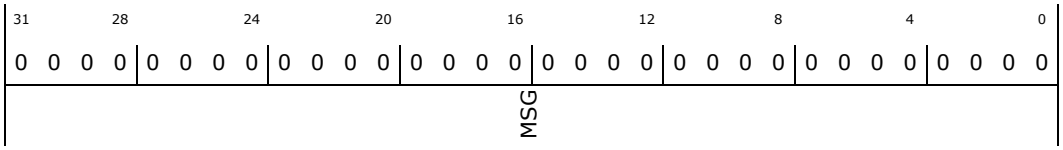
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 106Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.29 reg_ISH2HOST_MSG5_type (ISH2HOST_MSG5)—Offset 1070h

Message from ISH to HOST

Access Method

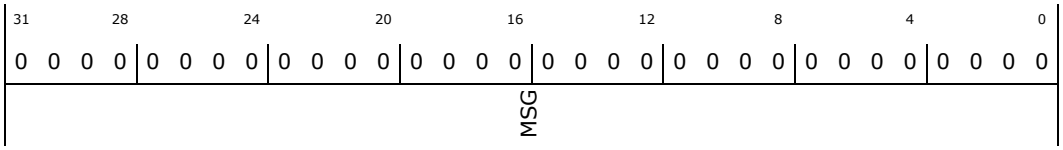
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1070h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.30 reg_ISH2HOST_MSG6_type (ISH2HOST_MSG6)—Offset 1074h

Message from ISH to HOST

Access Method

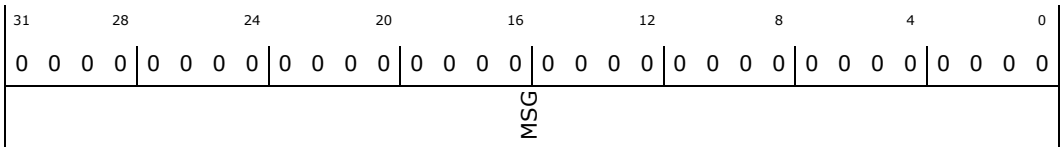
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1074h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.31 reg_ISH2HOST_MSG7_type (ISH2HOST_MSG7)—Offset 1078h

Message from ISH to HOST

Access Method

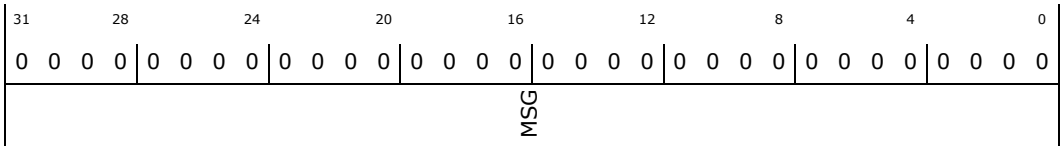
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1078h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.32 reg_ISH2HOST_MSG8_type (ISH2HOST_MSG8)—Offset 107Ch

Message from ISH to HOST

Access Method

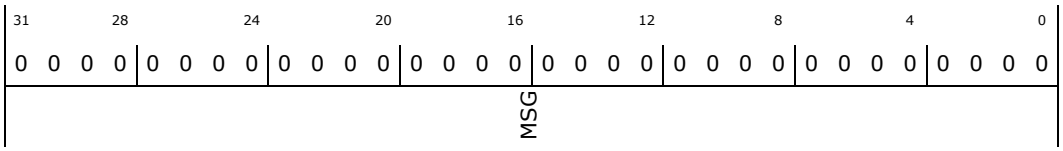
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 107Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.33 reg_ISH2HOST_MSG9_type (ISH2HOST_MSG9)—Offset 1080h

Message from ISH to HOST

Access Method

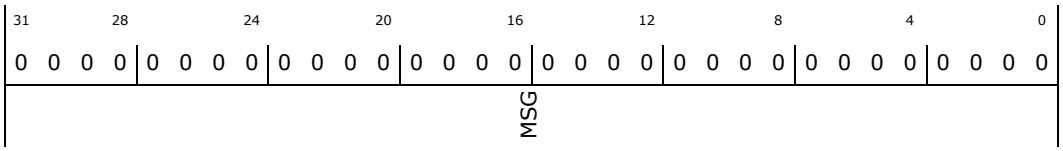
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1080h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.34 reg_ISH2HOST_MSG10_type (ISH2HOST_MSG10)—Offset 1084h

Message from ISH to HOST

Access Method

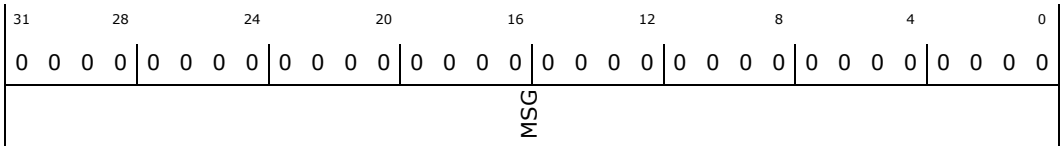
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1084h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.35 reg_ISH2HOST_MSG11_type (ISH2HOST_MSG11)—Offset 1088h

Message from ISH to HOST

Access Method

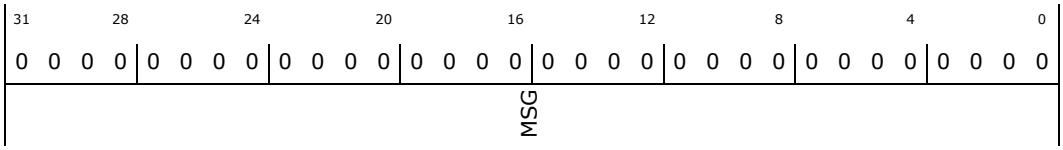
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1088h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.36 reg_ISH2HOST_MSG12_type (ISH2HOST_MSG12)—Offset 108Ch

Message from ISH to HOST

Access Method

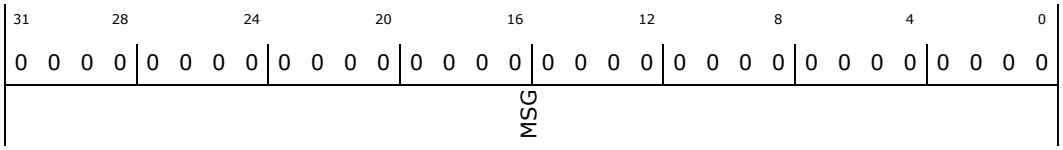
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 108Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.37 reg_ISH2HOST_MSG13_type (ISH2HOST_MSG13)—Offset 1090h

Message from ISH to HOST

Access Method

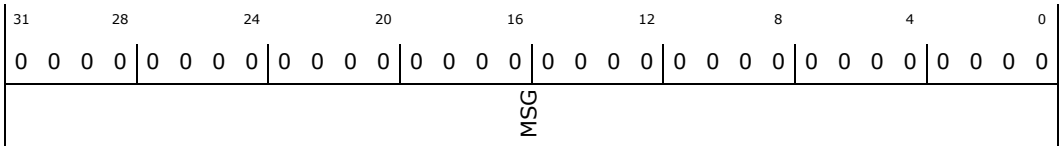
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1090h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.38 reg_ISH2HOST_MSG14_type (ISH2HOST_MSG14)—Offset 1094h

Message from ISH to HOST

Access Method

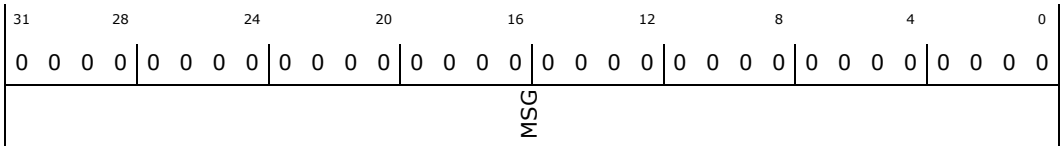
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1094h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.39 reg_ISH2HOST_MSG15_type (ISH2HOST_MSG15)—Offset 1098h

Message from ISH to HOST

Access Method

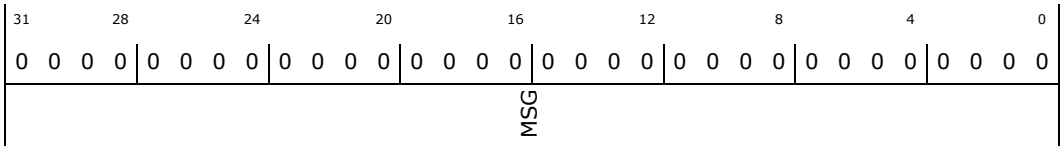
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1098h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.40 reg_ISH2HOST_MSG16_type (ISH2HOST_MSG16)—Offset 109Ch

Message from ISH to HOST

Access Method

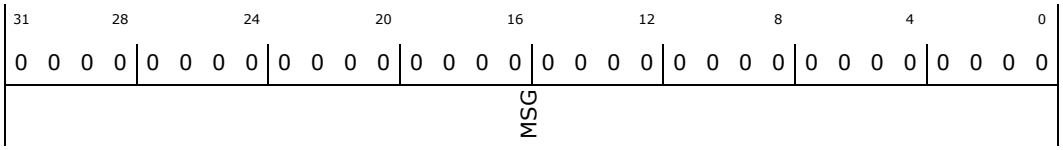
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 109Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.41 reg_ISH2HOST_MSG17_type (ISH2HOST_MSG17)—Offset 10A0h

Message from ISH to HOST

Access Method

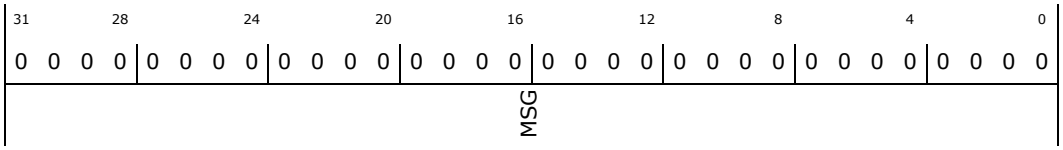
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10A0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.42 reg_ISH2HOST_MSG18_type (ISH2HOST_MSG18)—Offset 10A4h

Message from ISH to HOST

Access Method

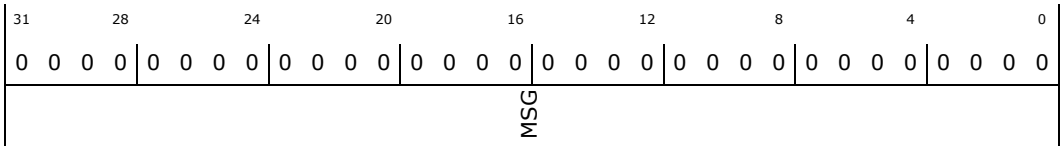
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10A4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.43 reg_ISH2HOST_MSG19_type (ISH2HOST_MSG19)—Offset 10A8h

Message from ISH to HOST

Access Method

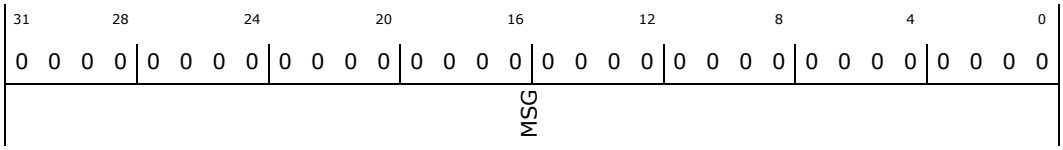
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10A8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.44 reg_ISH2HOST_MSG20_type (ISH2HOST_MSG20)—Offset 10ACh

Message from ISH to HOST

Access Method

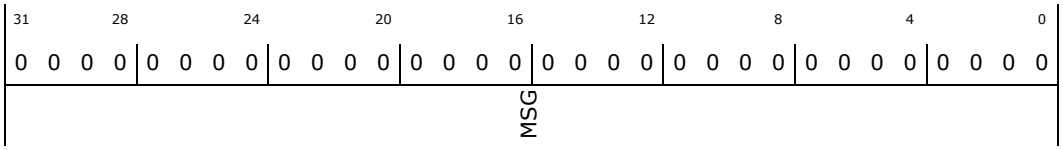
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10ACh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.45 reg_ISH2HOST_MSG21_type (ISH2HOST_MSG21)—Offset 10B0h

Message from ISH to HOST

Access Method

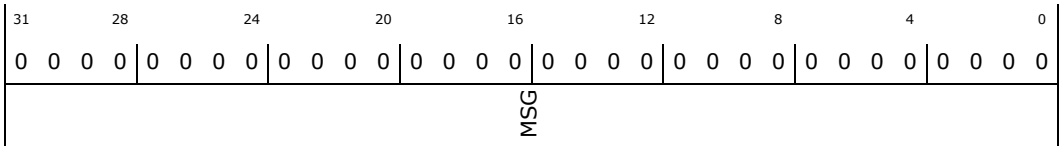
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10B0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.46 reg_ISH2HOST_MSG22_type (ISH2HOST_MSG22)—Offset 10B4h

Message from ISH to HOST

Access Method

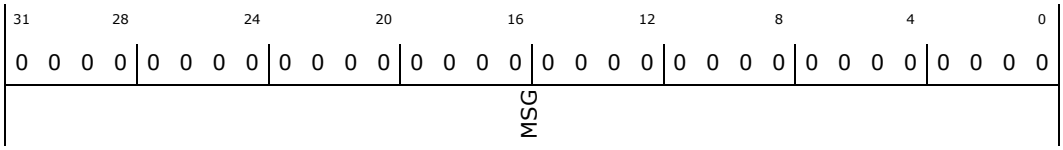
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10B4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.47 reg_ISH2HOST_MSG23_type (ISH2HOST_MSG23)—Offset 10B8h

Message from ISH to HOST

Access Method

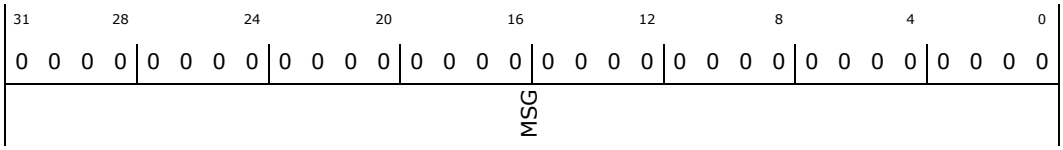
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10B8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.48 reg_ISH2HOST_MSG24_type (ISH2HOST_MSG24)—Offset 10BCh

Message from ISH to HOST

Access Method

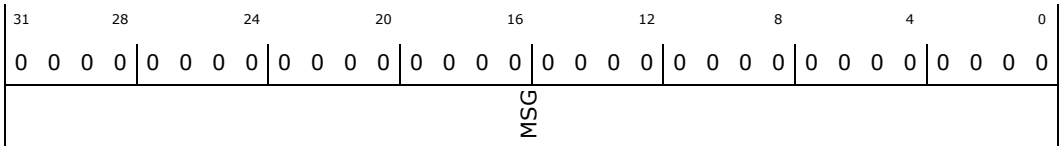
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10BCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.49 reg_ISH2HOST_MSG25_type (ISH2HOST_MSG25)—Offset 10C0h

Message from ISH to HOST

Access Method

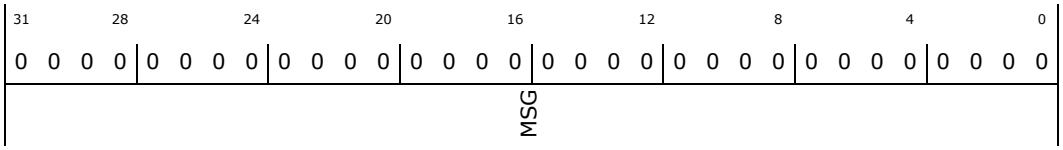
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10C0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.50 reg_ISH2HOST_MSG26_type (ISH2HOST_MSG26)—Offset 10C4h

Message from ISH to HOST

Access Method

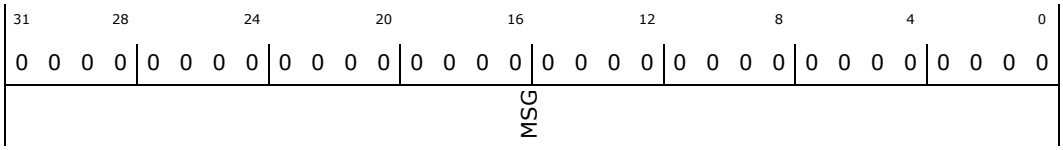
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10C4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.51 reg_ISH2HOST_MSG27_type (ISH2HOST_MSG27)—Offset 10C8h

Message from ISH to HOST

Access Method

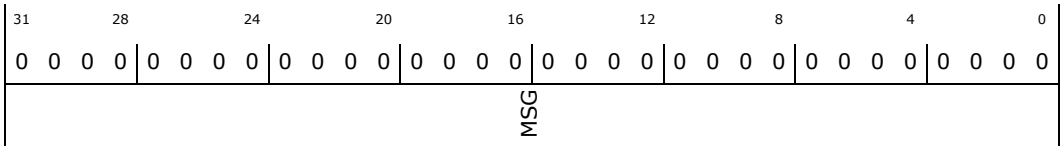
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10C8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.52 reg_ISH2HOST_MSG28_type (ISH2HOST_MSG28)—Offset 10CCh

Message from ISH to HOST

Access Method

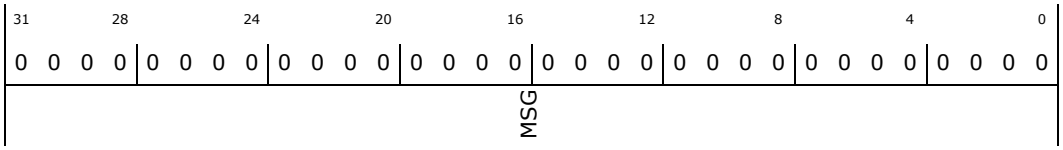
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10CCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.53 reg_ISH2HOST_MSG29_type (ISH2HOST_MSG29)—Offset 10D0h

Message from ISH to HOST

Access Method

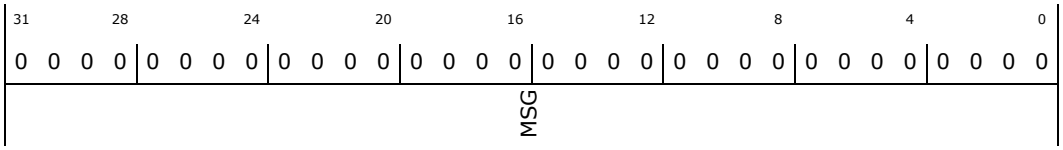
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10D0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.54 reg_ISH2HOST_MSG30_type (ISH2HOST_MSG30)—Offset 10D4h

Message from ISH to HOST

Access Method

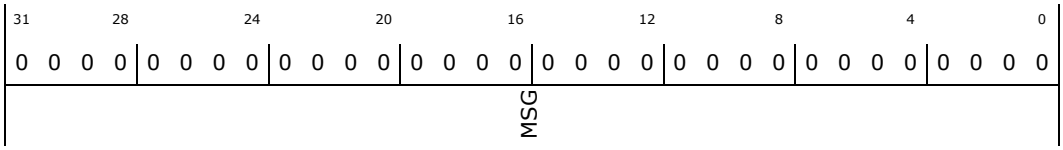
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10D4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.55 reg_ISH2HOST_MSG31_type (ISH2HOST_MSG31)—Offset 10D8h

Message from ISH to HOST

Access Method

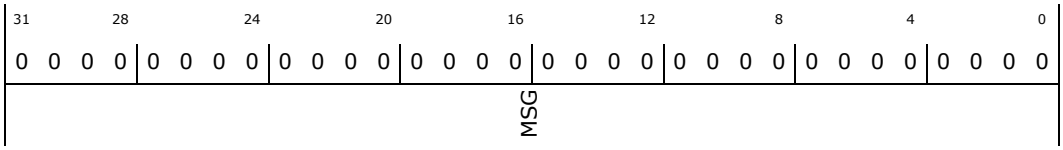
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10D8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.56 reg_ISH2HOST_MSG32_type (ISH2HOST_MSG32)—Offset 10DCh

Message from ISH to HOST

Access Method

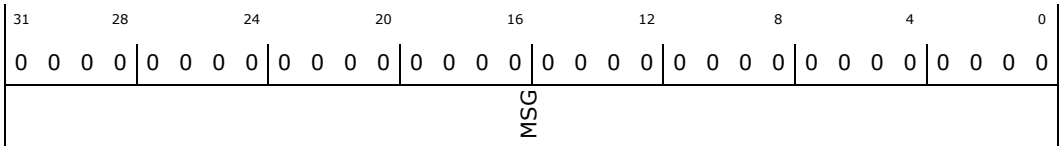
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10DCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.57 reg_HOST2ISH_MSG1_type (HOST2ISH_MSG1)—Offset 10E0h

Message from HOST to ISH

Access Method

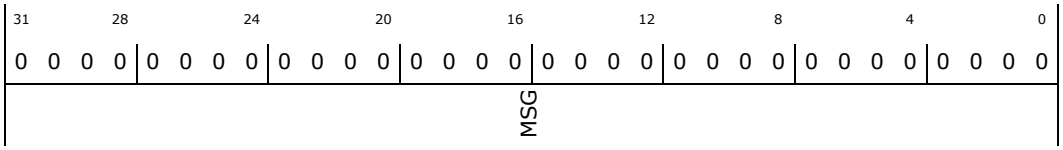
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10E0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.58 reg_HOST2ISH_MSG2_type (HOST2ISH_MSG2)—Offset 10E4h

Message from HOST to ISH

Access Method

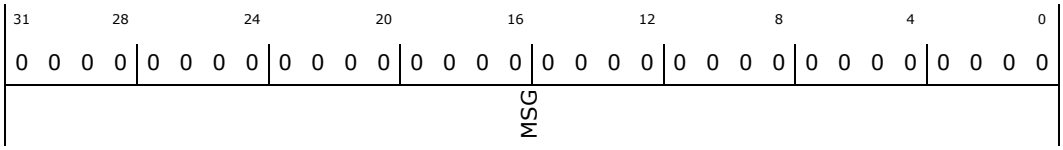
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10E4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.59 reg_HOST2ISH_MSG3_type (HOST2ISH_MSG3)—Offset 10E8h

Message from HOST to ISH

Access Method

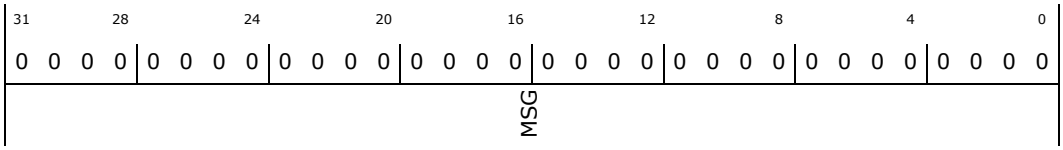
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10E8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.60 reg_HOST2ISH_MSG4_type (HOST2ISH_MSG4)—Offset 10ECh

Message from HOST to ISH

Access Method

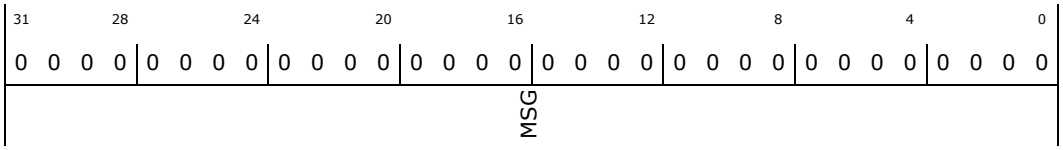
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10ECh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.61 reg_HOST2ISH_MSG5_type (HOST2ISH_MSG5)—Offset 10F0h

Message from HOST to ISH

Access Method

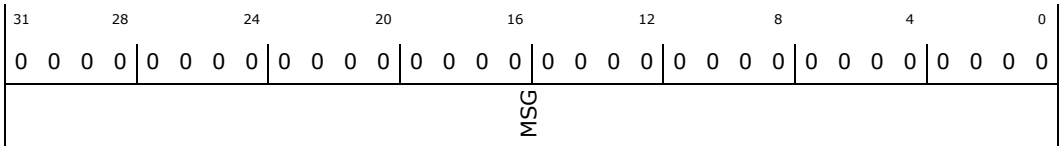
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10F0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.62 reg_HOST2ISH_MSG6_type (HOST2ISH_MSG6)—Offset 10F4h

Message from HOST to ISH

Access Method

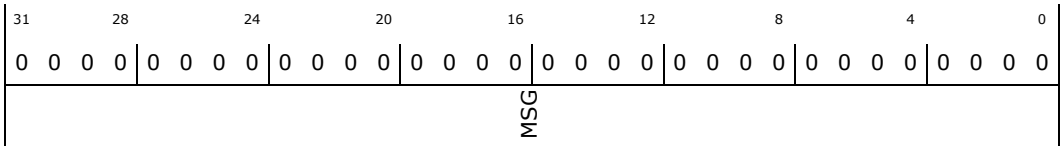
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10F4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.63 reg_HOST2ISH_MSG7_type (HOST2ISH_MSG7)—Offset 10F8h

Message from HOST to ISH

Access Method

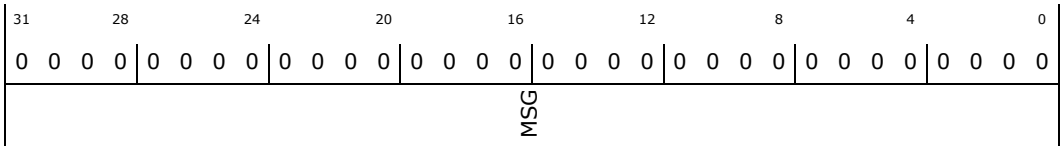
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10F8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.64 reg_HOST2ISH_MSG8_type (HOST2ISH_MSG8)—Offset 10FCh

Message from HOST to ISH

Access Method

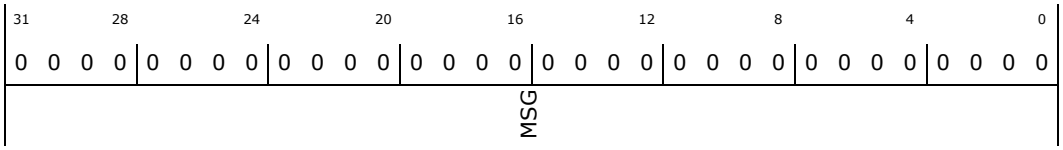
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10FCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.65 reg_HOST2ISH_MSG9_type (HOST2ISH_MSG9)—Offset 1100h

Message from HOST to ISH

Access Method

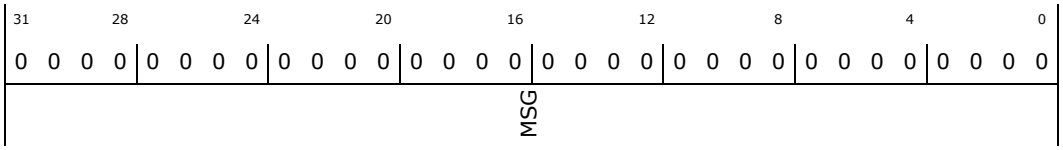
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1100h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.66 reg_HOST2ISH_MSG10_type (HOST2ISH_MSG10)—Offset 1104h

Message from HOST to ISH

Access Method

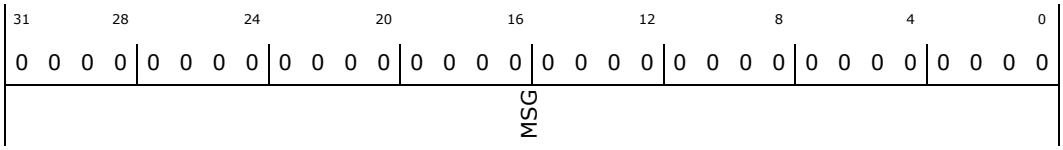
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1104h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.67 reg_HOST2ISH_MSG11_type (HOST2ISH_MSG11)—Offset 1108h

Message from HOST to ISH

Access Method

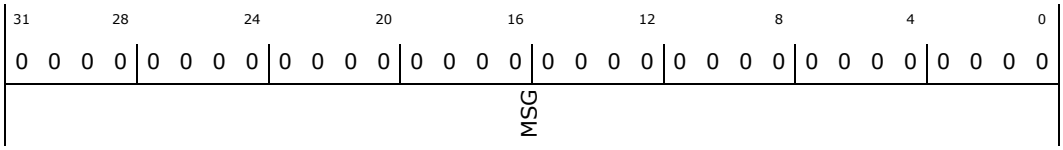
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1108h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.68 reg_HOST2ISH_MSG12_type (HOST2ISH_MSG12)—Offset 110Ch

Message from HOST to ISH

Access Method

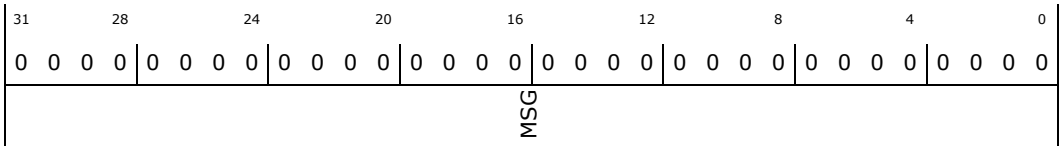
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 110Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.69 reg_HOST2ISH_MSG13_type (HOST2ISH_MSG13)—Offset 1110h

Message from HOST to ISH

Access Method

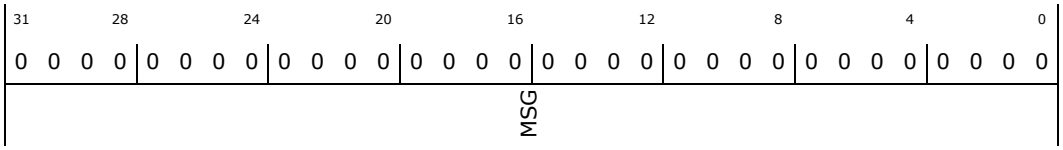
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1110h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.70 reg_HOST2ISH_MSG14_type (HOST2ISH_MSG14)—Offset 1114h

Message from HOST to ISH

Access Method

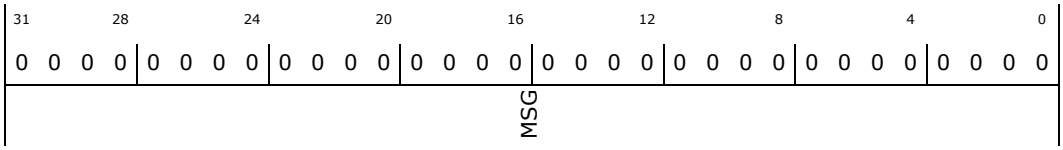
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1114h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.71 reg_HOST2ISH_MSG15_type (HOST2ISH_MSG15)—Offset 1118h

Message from HOST to ISH

Access Method

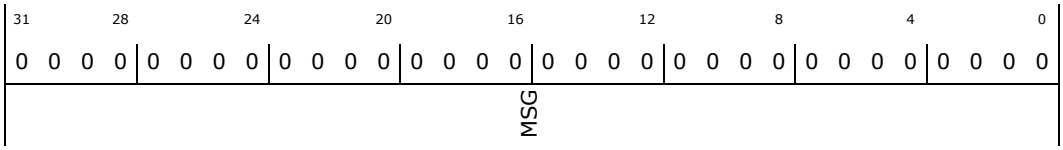
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1118h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.72 reg_HOST2ISH_MSG16_type (HOST2ISH_MSG16)—Offset 111Ch

Message from HOST to ISH

Access Method

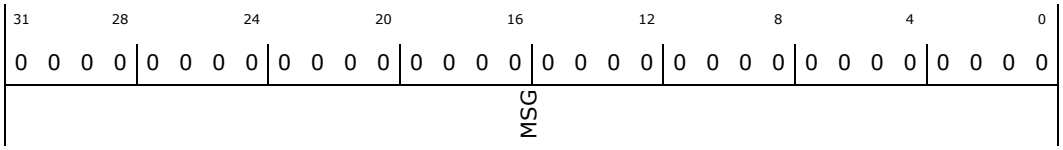
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 111Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.73 reg_HOST2ISH_MSG17_type (HOST2ISH_MSG17)—Offset 1120h

Message from HOST to ISH

Access Method

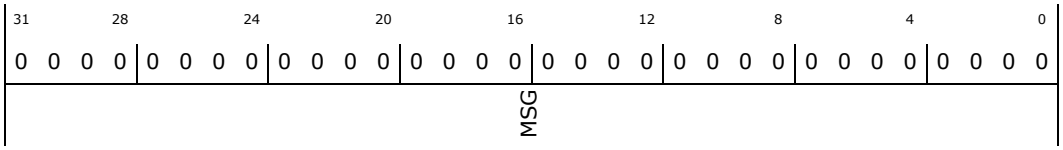
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1120h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.74 reg_HOST2ISH_MSG18_type (HOST2ISH_MSG18)—Offset 1124h

Message from HOST to ISH

Access Method

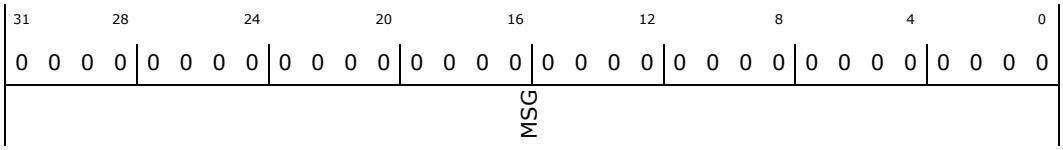
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1124h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.75 reg_HOST2ISH_MSG19_type (HOST2ISH_MSG19)—Offset 1128h

Message from HOST to ISH

Access Method

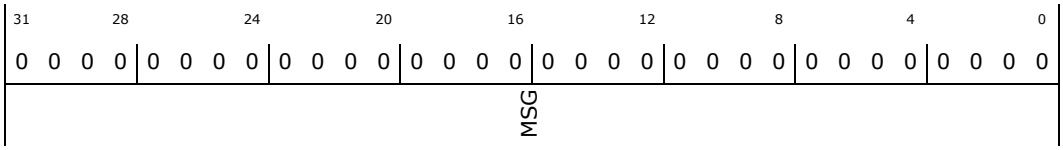
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1128h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.76 reg_HOST2ISH_MSG20_type (HOST2ISH_MSG20)—Offset 112Ch

Message from HOST to ISH

Access Method

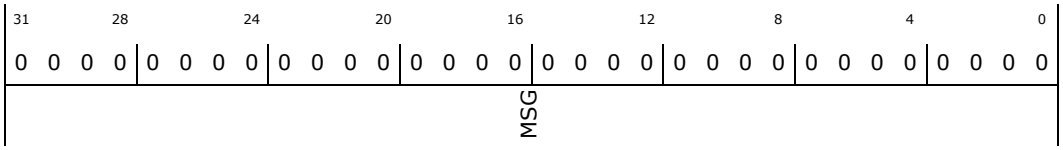
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 112Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.77 reg_HOST2ISH_MSG21_type (HOST2ISH_MSG21)—Offset 1130h

Message from HOST to ISH

Access Method

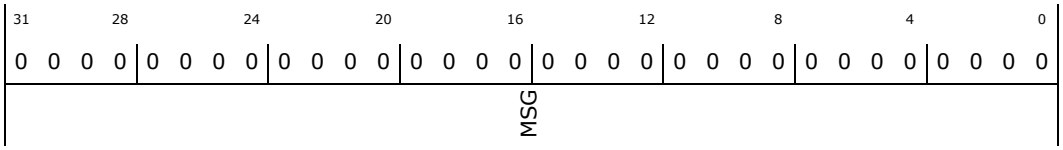
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1130h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.78 reg_HOST2ISH_MSG22_type (HOST2ISH_MSG22)—Offset 1134h

Message from HOST to ISH

Access Method

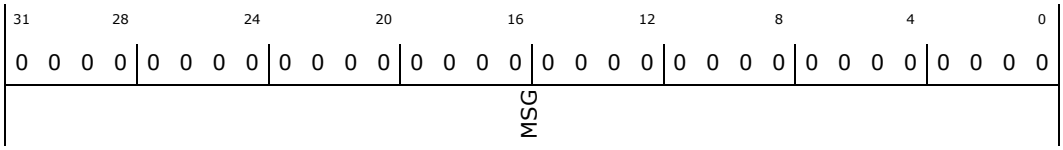
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1134h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.79 reg_HOST2ISH_MSG23_type (HOST2ISH_MSG23)—Offset 1138h

Message from HOST to ISH

Access Method

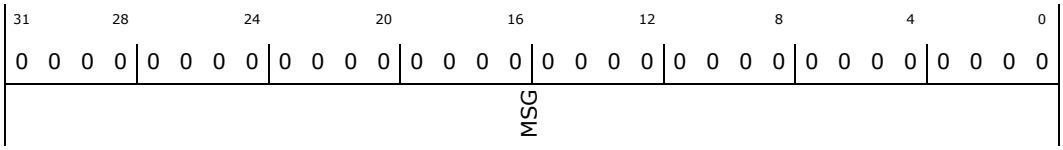
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1138h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.80 reg_HOST2ISH_MSG24_type (HOST2ISH_MSG24)—Offset 113Ch

Message from HOST to ISH

Access Method

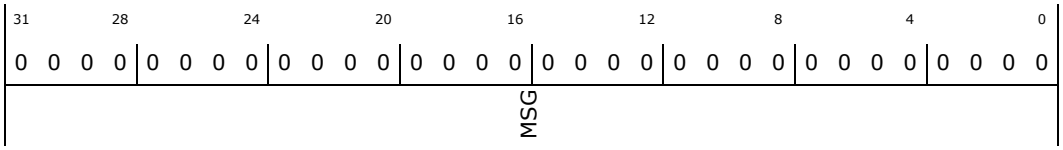
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 113Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.81 reg_HOST2ISH_MSG25_type (HOST2ISH_MSG25)—Offset 1140h

Message from HOST to ISH

Access Method

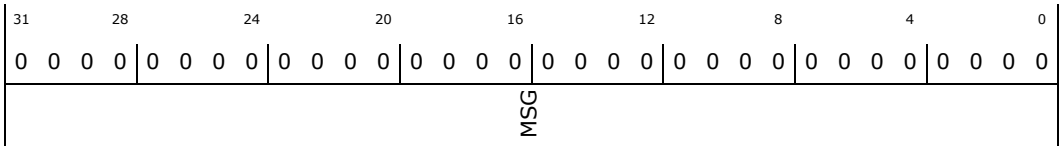
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1140h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.82 reg_HOST2ISH_MSG26_type (HOST2ISH_MSG26)—Offset 1144h

Message from HOST to ISH

Access Method

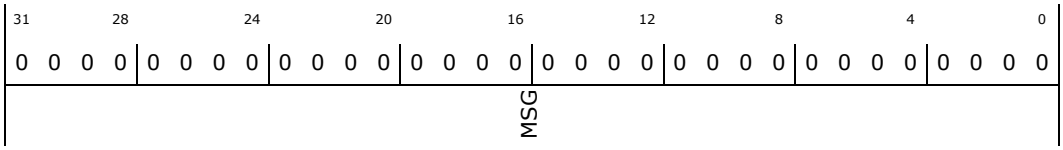
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1144h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.83 reg_HOST2ISH_MSG27_type (HOST2ISH_MSG27)—Offset 1148h

Message from HOST to ISH

Access Method

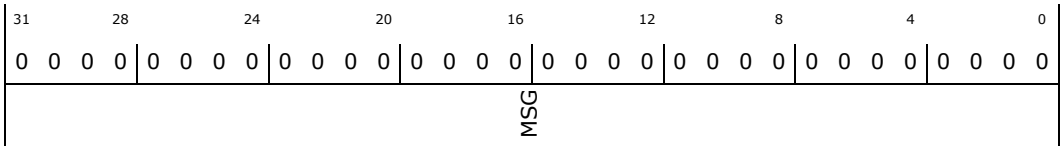
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1148h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.84 reg_HOST2ISH_MSG28_type (HOST2ISH_MSG28)—Offset 114Ch

Message from HOST to ISH

Access Method

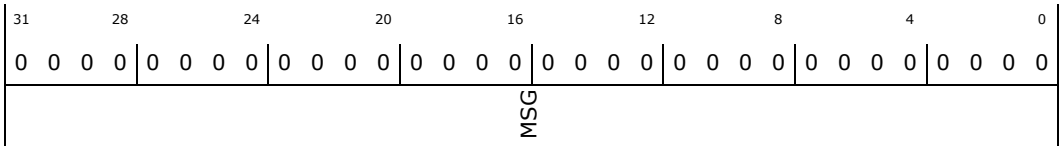
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 114Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.85 reg_HOST2ISH_MSG29_type (HOST2ISH_MSG29)—Offset 1150h

Message from HOST to ISH

Access Method

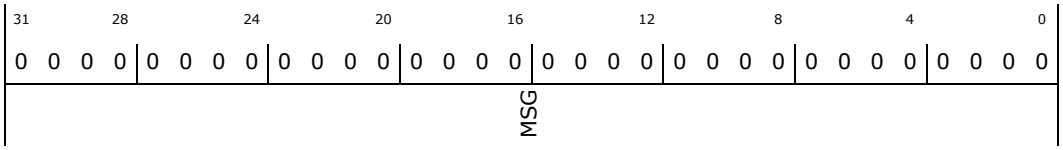
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1150h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.86 reg_HOST2ISH_MSG30_type (HOST2ISH_MSG30)—Offset 1154h

Message from HOST to ISH

Access Method

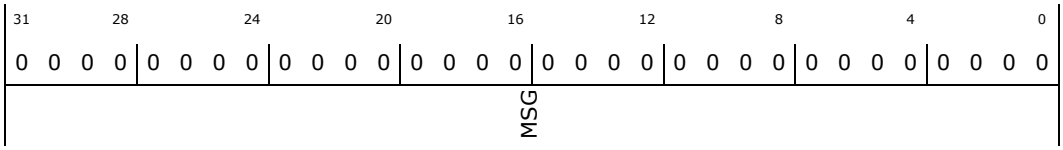
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1154h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.87 reg_HOST2ISH_MSG31_type (HOST2ISH_MSG31)—Offset 1158h

Message from HOST to ISH

Access Method

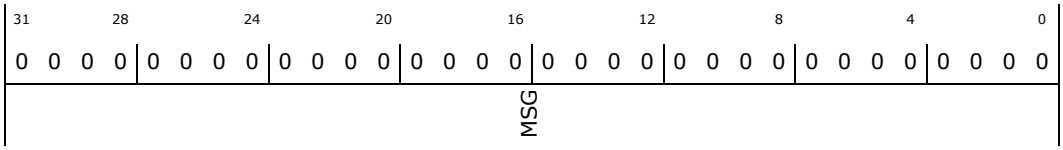
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1158h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.88 reg_HOST2ISH_MSG32_type (HOST2ISH_MSG32)—Offset 115Ch

Message from HOST to ISH

Access Method

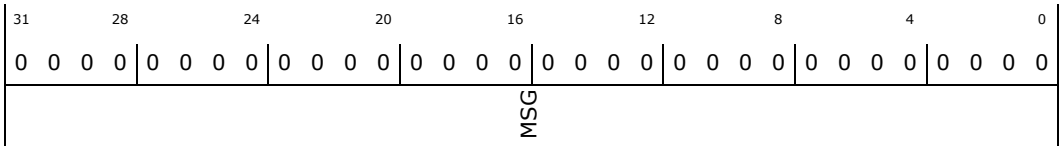
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 115Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.89 reg_ISH2SEC_MSG1_type (ISH2SEC_MSG1)—Offset 1160h

Message from ISH to SEC

Access Method

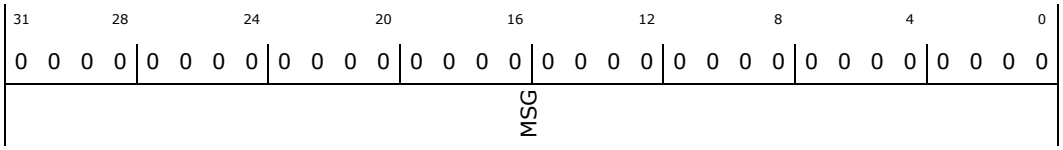
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1160h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.90 reg_ISH2SEC_MSG2_type (ISH2SEC_MSG2)—Offset 1164h

Message from ISH to SEC

Access Method

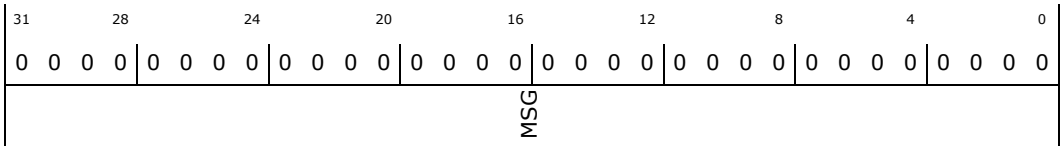
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1164h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.91 reg_ISH2SEC_MSG3_type (ISH2SEC_MSG3)—Offset 1168h

Message from ISH to SEC

Access Method

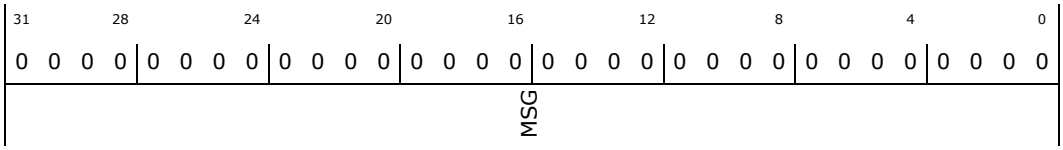
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1168h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.92 reg_ISH2SEC_MSG4_type (ISH2SEC_MSG4)—Offset 116Ch

Message from ISH to SEC

Access Method

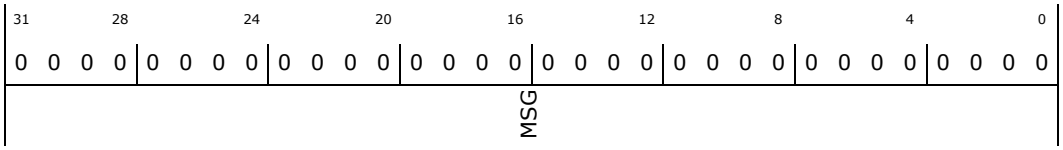
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 116Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.93 reg_ISH2SEC_MSG5_type (ISH2SEC_MSG5)—Offset 1170h

Message from ISH to SEC

Access Method

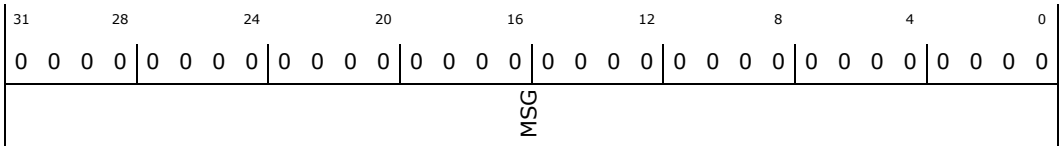
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1170h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.94 reg_ISH2SEC_MSG6_type (ISH2SEC_MSG6)—Offset 1174h

Message from ISH to SEC

Access Method

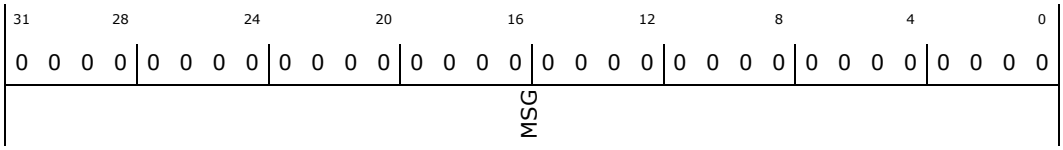
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1174h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.95 reg_ISH2SEC_MSG7_type (ISH2SEC_MSG7)—Offset 1178h

Message from ISH to SEC

Access Method

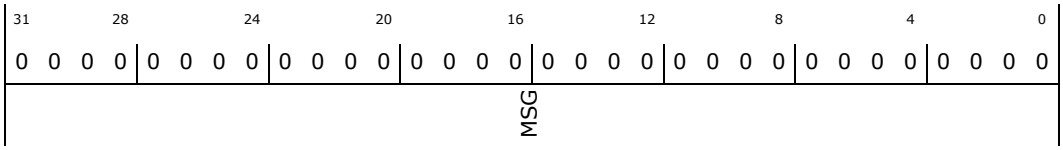
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1178h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.96 reg_ISH2SEC_MSG8_type (ISH2SEC_MSG8)—Offset 117Ch

Message from ISH to SEC

Access Method

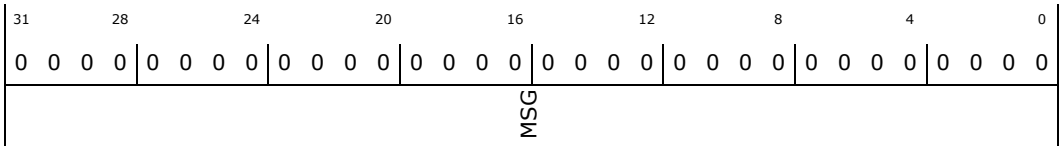
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 117Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.97 reg_ISH2SEC_MSG9_type (ISH2SEC_MSG9)—Offset 1180h

Message from ISH to SEC

Access Method

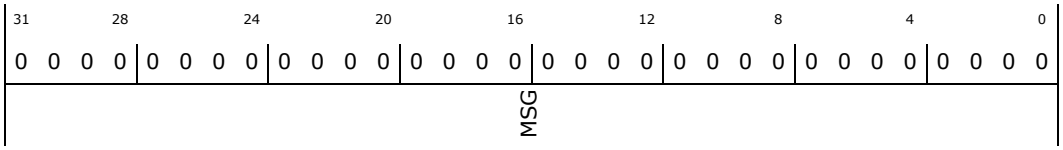
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1180h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.98 reg_ISH2SEC_MSG10_type (ISH2SEC_MSG10)—Offset 1184h

Message from ISH to SEC

Access Method

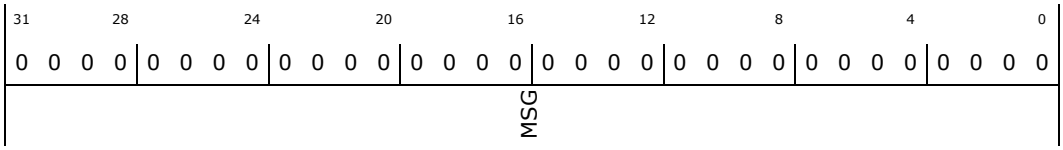
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1184h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.99 reg_ISH2SEC_MSG11_type (ISH2SEC_MSG11)—Offset 1188h

Message from ISH to SEC

Access Method

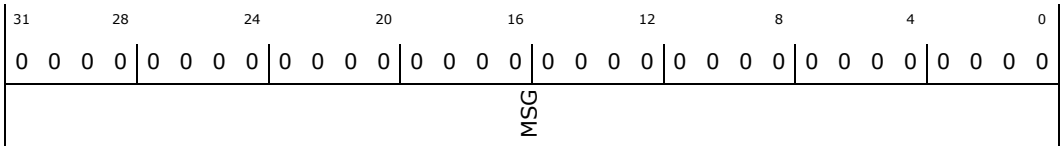
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1188h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.100 reg_ISH2SEC_MSG12_type (ISH2SEC_MSG12)—Offset 118Ch

Message from ISH to SEC

Access Method

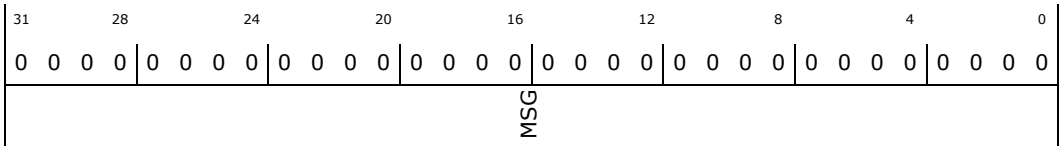
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 118Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.101 reg_ISH2SEC_MSG13_type (ISH2SEC_MSG13)—Offset 1190h

Message from ISH to SEC

Access Method

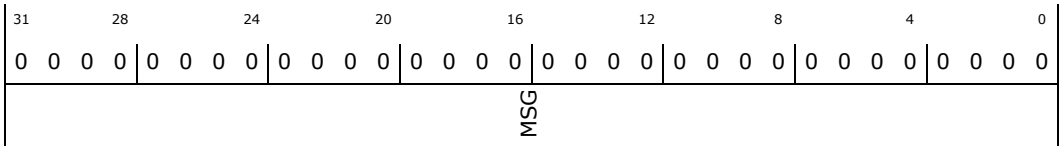
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1190h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.102 reg_ISH2SEC_MSG14_type (ISH2SEC_MSG14)—Offset 1194h

Message from ISH to SEC

Access Method

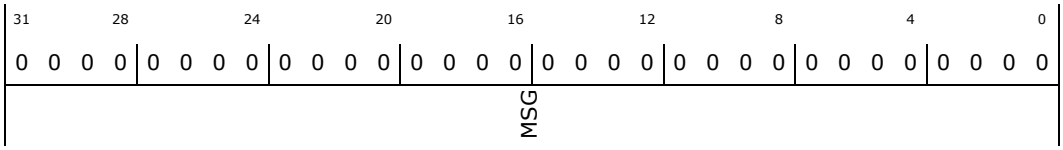
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1194h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.103 reg_ISH2SEC_MSG15_type (ISH2SEC_MSG15)—Offset 1198h

Message from ISH to SEC

Access Method

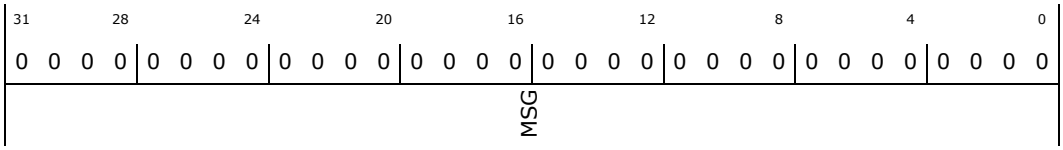
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1198h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.104 reg_ISH2SEC_MSG16_type (ISH2SEC_MSG16)—Offset 119Ch

Message from ISH to SEC

Access Method

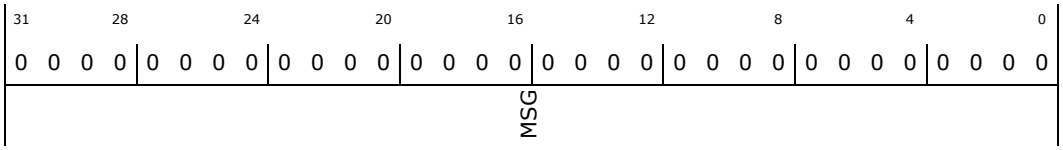
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 119Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.105 reg_ISH2SEC_MSG17_type (ISH2SEC_MSG17)—Offset 11A0h

Message from ISH to SEC

Access Method

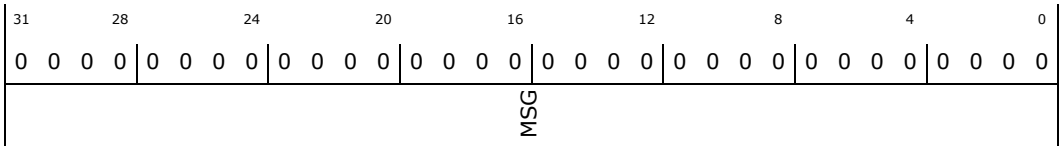
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11A0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.106 reg_ISH2SEC_MSG18_type (ISH2SEC_MSG18)—Offset 11A4h

Message from ISH to SEC

Access Method

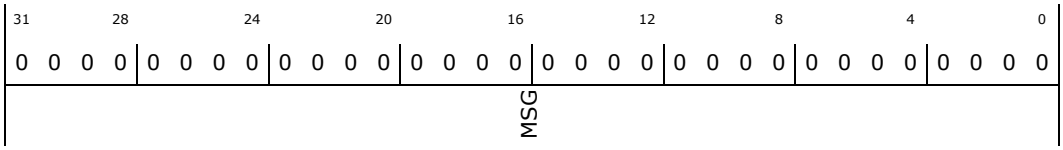
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11A4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.107 reg_ISH2SEC_MSG19_type (ISH2SEC_MSG19)—Offset 11A8h

Message from ISH to SEC

Access Method

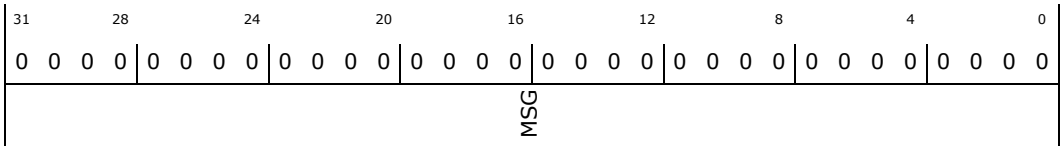
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11A8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.108 reg_ISH2SEC_MSG20_type (ISH2SEC_MSG20)—Offset 11ACh

Message from ISH to SEC

Access Method

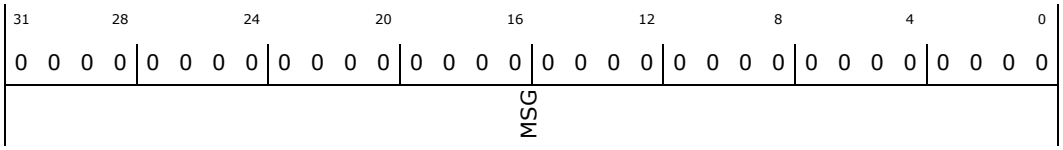
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11ACh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.109 reg_ISH2SEC_MSG21_type (ISH2SEC_MSG21)—Offset 11B0h

Message from ISH to SEC

Access Method

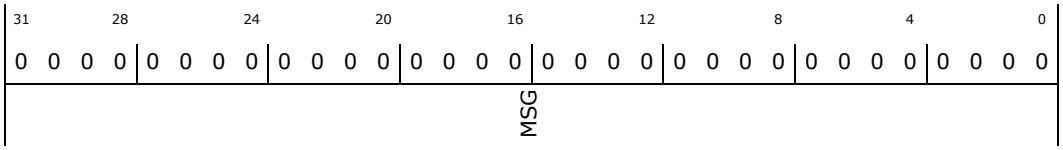
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11B0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.110 reg_ISH2SEC_MSG22_type (ISH2SEC_MSG22)—Offset 11B4h

Message from ISH to SEC

Access Method

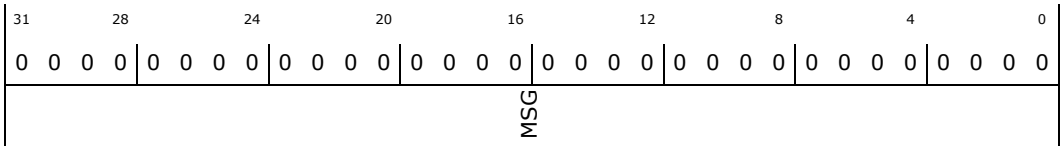
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11B4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.111 reg_ISH2SEC_MSG23_type (ISH2SEC_MSG23)—Offset 11B8h

Message from ISH to SEC

Access Method

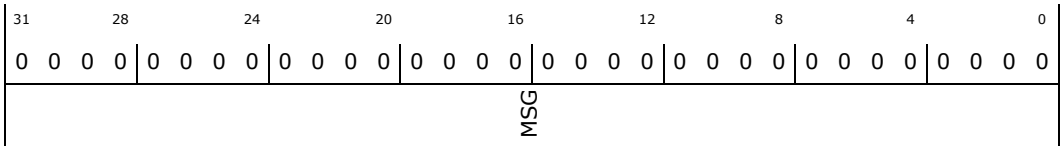
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11B8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.112 reg_ISH2SEC_MSG24_type (ISH2SEC_MSG24)—Offset 11BCh

Message from ISH to SEC

Access Method

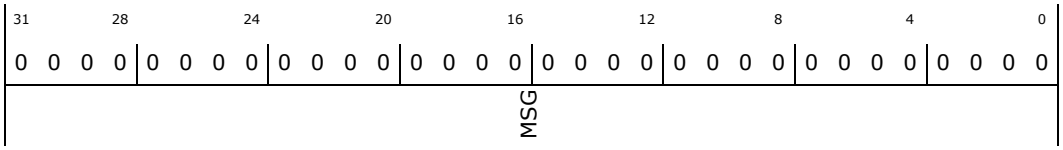
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11BCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.113 reg_ISH2SEC_MSG25_type (ISH2SEC_MSG25)—Offset 11C0h

Message from ISH to SEC

Access Method

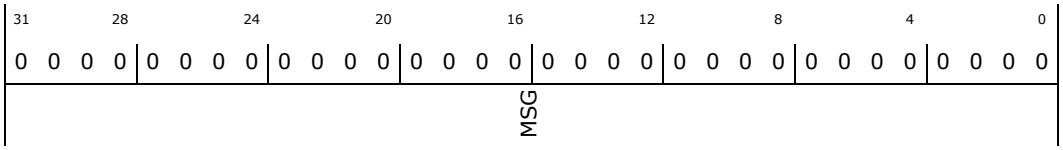
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11C0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.114 reg_ISH2SEC_MSG26_type (ISH2SEC_MSG26)—Offset 11C4h

Message from ISH to SEC

Access Method

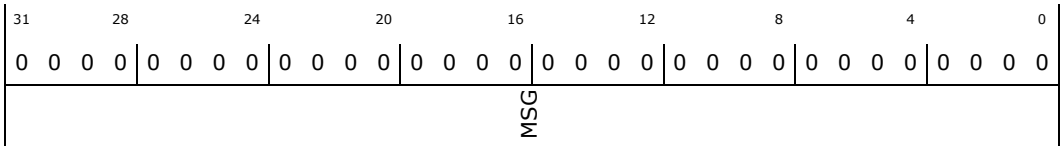
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11C4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.115 reg_ISH2SEC_MSG27_type (ISH2SEC_MSG27)—Offset 11C8h

Message from ISH to SEC

Access Method

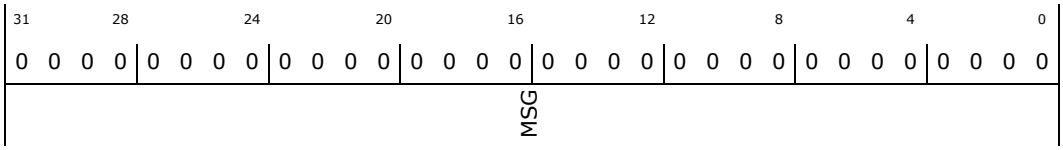
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11C8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.116 reg_ISH2SEC_MSG28_type (ISH2SEC_MSG28)—Offset 11CCh

Message from ISH to SEC

Access Method

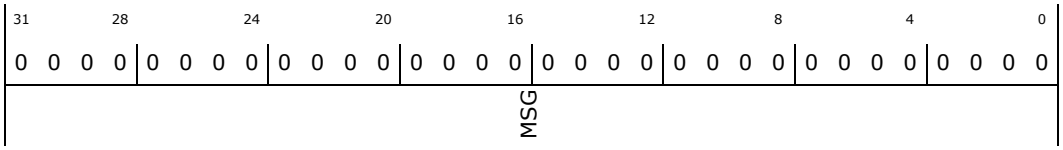
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11CCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.117 reg_ISH2SEC_MSG29_type (ISH2SEC_MSG29)—Offset 11D0h

Message from ISH to SEC

Access Method

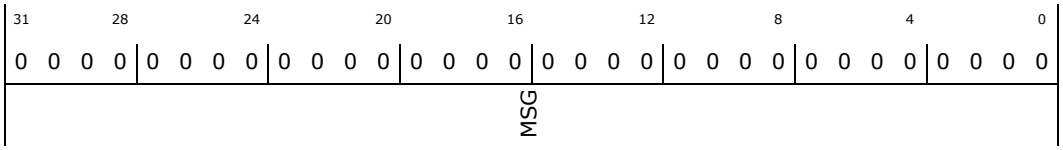
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11D0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.118 reg_ISH2SEC_MSG30_type (ISH2SEC_MSG30)—Offset 11D4h

Message from ISH to SEC

Access Method

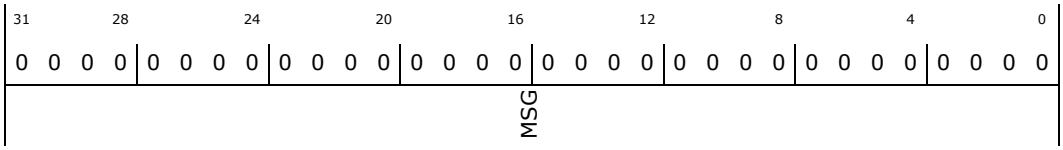
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11D4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.119 reg_ISH2SEC_MSG31_type (ISH2SEC_MSG31)—Offset 11D8h

Message from ISH to SEC

Access Method

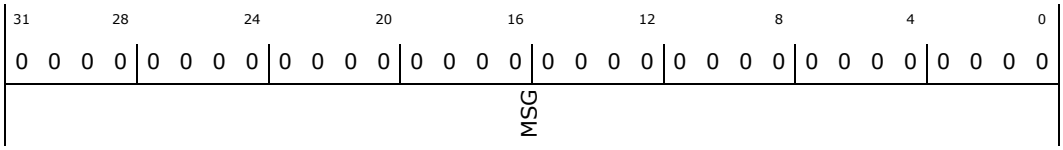
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11D8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.120 reg_ISH2SEC_MSG32_type (ISH2SEC_MSG32)—Offset 11DCh

Message from ISH to SEC

Access Method

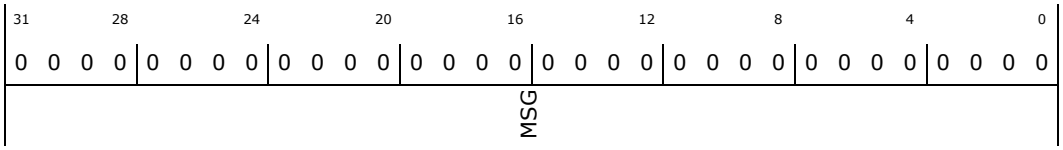
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11DCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.121 reg_SEC2ISH_MSG1_type (SEC2ISH_MSG1)—Offset 11E0h

Message from SEC to ISH

Access Method

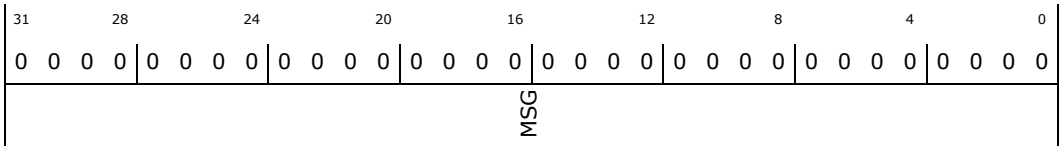
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11E0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.122 reg_SEC2ISH_MSG2_type (SEC2ISH_MSG2)—Offset 11E4h

Message from SEC to ISH

Access Method

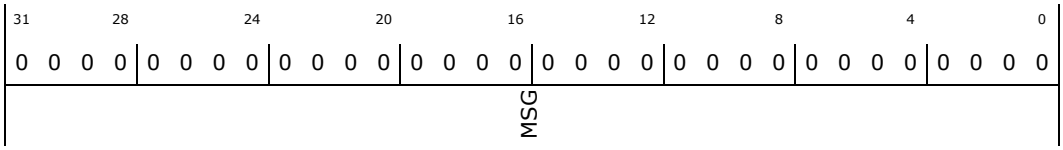
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11E4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.123 reg_SEC2ISH_MSG3_type (SEC2ISH_MSG3)—Offset 11E8h

Message from SEC to ISH

Access Method

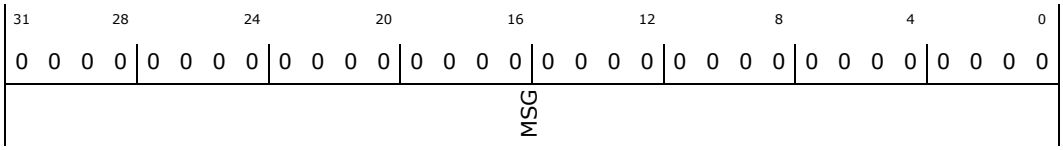
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11E8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.124 reg_SEC2ISH_MSG4_type (SEC2ISH_MSG4)—Offset 11ECh

Message from SEC to ISH

Access Method

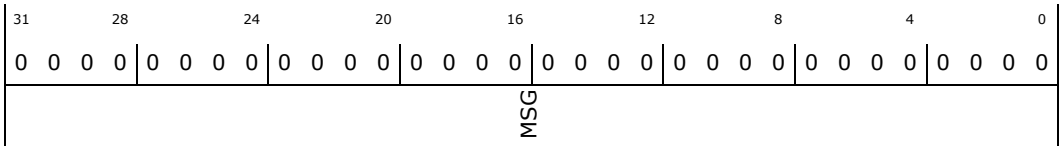
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11ECh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.125 reg_SEC2ISH_MSG5_type (SEC2ISH_MSG5)—Offset 11F0h

Message from SEC to ISH

Access Method

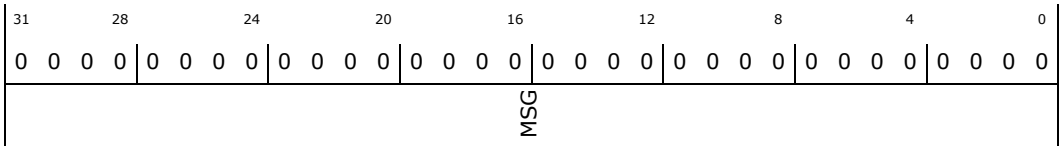
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11F0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.126 reg_SEC2ISH_MSG6_type (SEC2ISH_MSG6)—Offset 11F4h

Message from SEC to ISH

Access Method

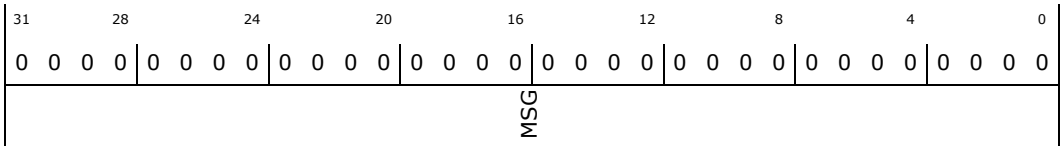
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11F4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.127 reg_SEC2ISH_MSG7_type (SEC2ISH_MSG7)—Offset 11F8h

Message from SEC to ISH

Access Method

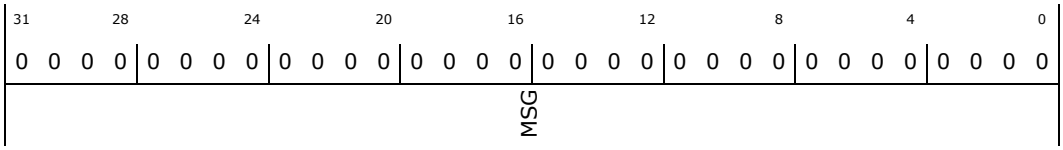
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11F8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.128 reg_SEC2ISH_MSG8_type (SEC2ISH_MSG8)—Offset 11FCh

Message from SEC to ISH

Access Method

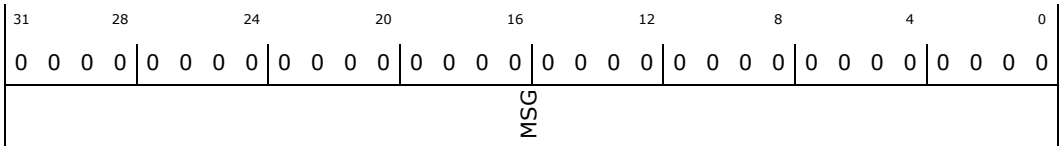
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11FCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.129 reg_SEC2ISH_MSG9_type (SEC2ISH_MSG9)—Offset 1200h

Message from SEC to ISH

Access Method

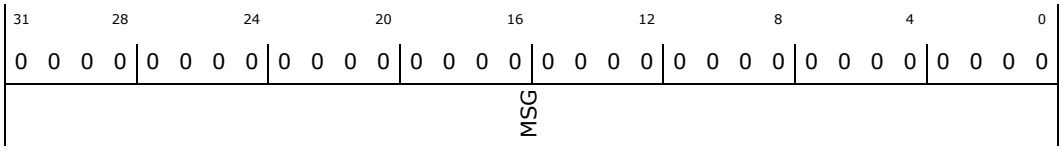
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1200h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.130 reg_SEC2ISH_MSG10_type (SEC2ISH_MSG10)—Offset 1204h

Message from SEC to ISH

Access Method

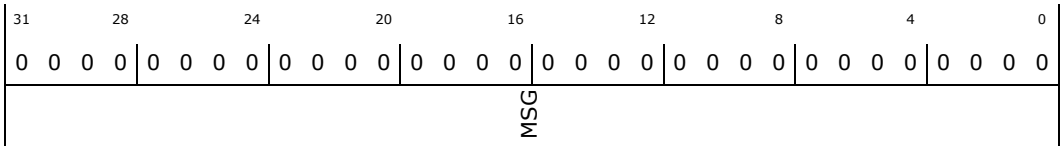
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1204h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.131 reg_SEC2ISH_MSG11_type (SEC2ISH_MSG11)—Offset 1208h

Message from SEC to ISH

Access Method

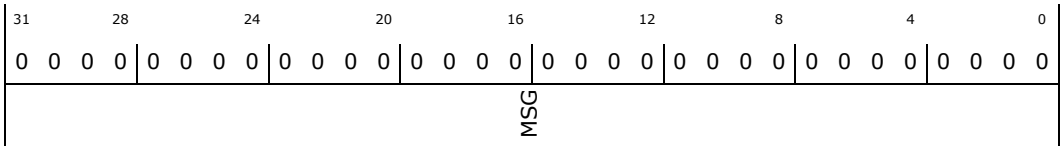
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1208h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.132 reg_SEC2ISH_MSG12_type (SEC2ISH_MSG12)—Offset 120Ch

Message from SEC to ISH

Access Method

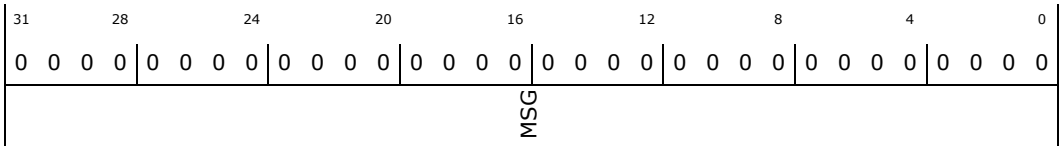
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 120Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.133 reg_SEC2ISH_MSG13_type (SEC2ISH_MSG13)—Offset 1210h

Message from SEC to ISH

Access Method

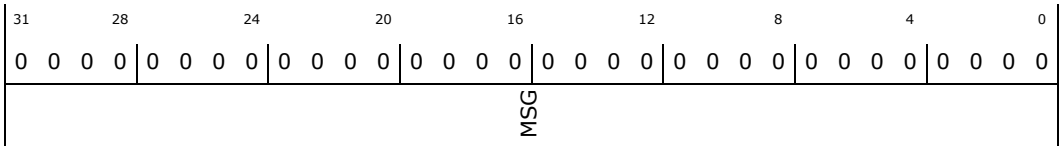
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1210h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.134 reg_SEC2ISH_MSG14_type (SEC2ISH_MSG14)—Offset 1214h

Message from SEC to ISH

Access Method

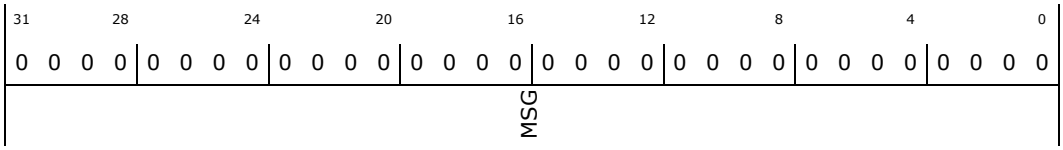
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1214h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.135 reg_SEC2ISH_MSG15_type (SEC2ISH_MSG15)—Offset 1218h

Message from SEC to ISH

Access Method

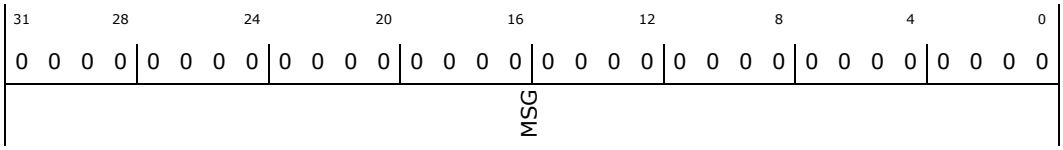
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1218h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.136 reg_SEC2ISH_MSG16_type (SEC2ISH_MSG16)—Offset 121Ch

Message from SEC to ISH

Access Method

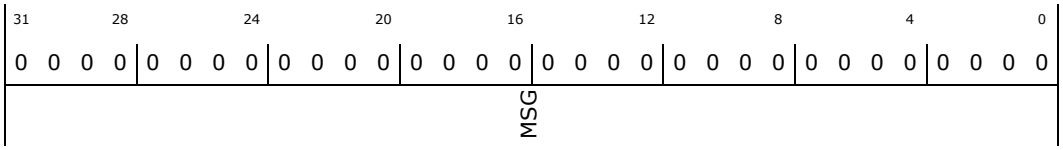
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 121Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.137 reg_SEC2ISH_MSG17_type (SEC2ISH_MSG17)—Offset 1220h

Message from SEC to ISH

Access Method

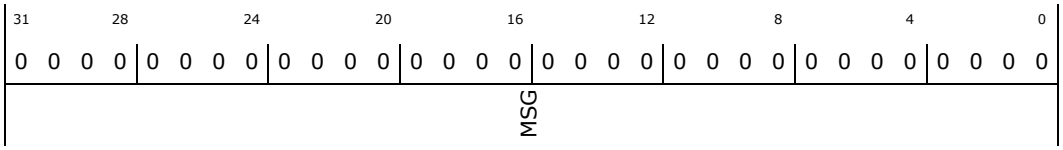
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1220h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.138 reg_SEC2ISH_MSG18_type (SEC2ISH_MSG18)—Offset 1224h

Message from SEC to ISH

Access Method

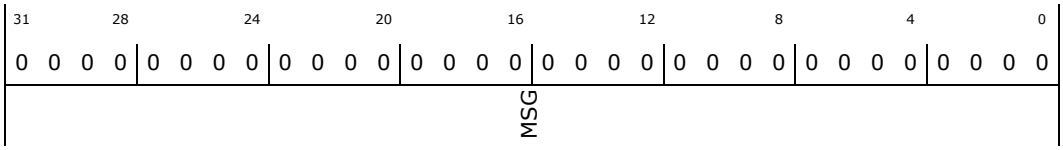
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1224h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.139 reg_SEC2ISH_MSG19_type (SEC2ISH_MSG19)—Offset 1228h

Message from SEC to ISH

Access Method

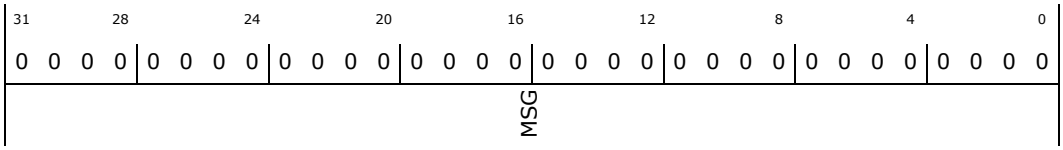
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1228h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.140 reg_SEC2ISH_MSG20_type (SEC2ISH_MSG20)—Offset 122Ch

Message from SEC to ISH

Access Method

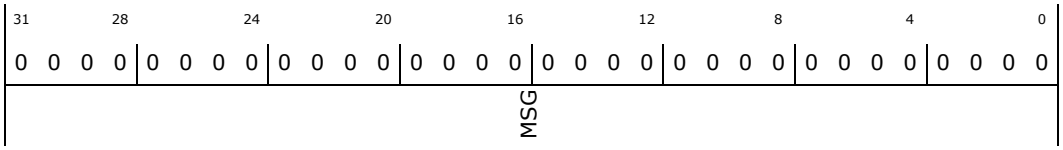
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 122Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.141 reg_SEC2ISH_MSG21_type (SEC2ISH_MSG21)—Offset 1230h

Message from SEC to ISH

Access Method

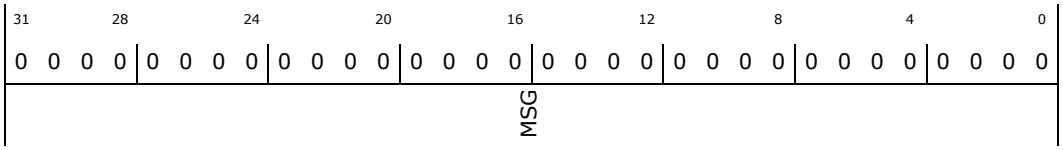
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1230h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.142 reg_SEC2ISH_MSG22_type (SEC2ISH_MSG22)—Offset 1234h

Message from SEC to ISH

Access Method

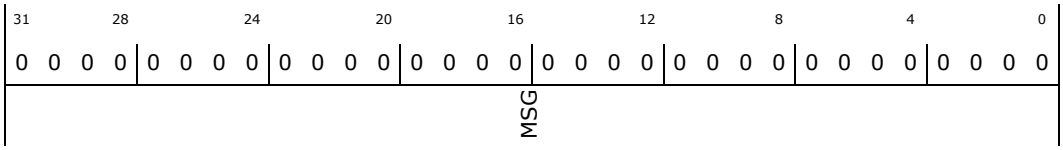
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1234h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.143 reg_SEC2ISH_MSG23_type (SEC2ISH_MSG23)—Offset 1238h

Message from SEC to ISH

Access Method

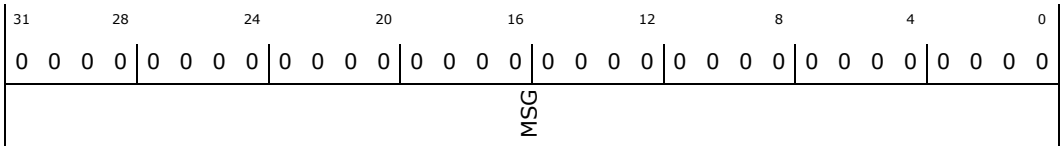
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1238h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.144 reg_SEC2ISH_MSG24_type (SEC2ISH_MSG24)—Offset 123Ch

Message from SEC to ISH

Access Method

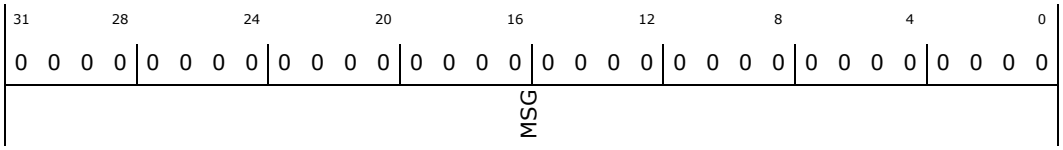
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 123Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.145 reg_SEC2ISH_MSG25_type (SEC2ISH_MSG25)—Offset 1240h

Message from SEC to ISH

Access Method

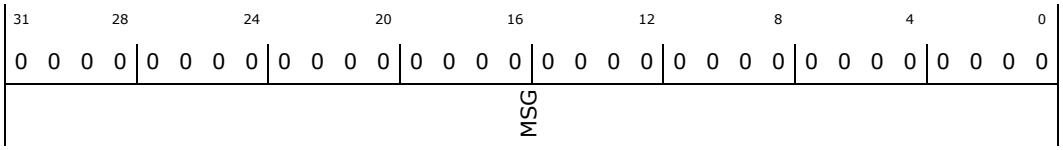
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1240h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.146 reg_SEC2ISH_MSG26_type (SEC2ISH_MSG26)—Offset 1244h

Message from SEC to ISH

Access Method

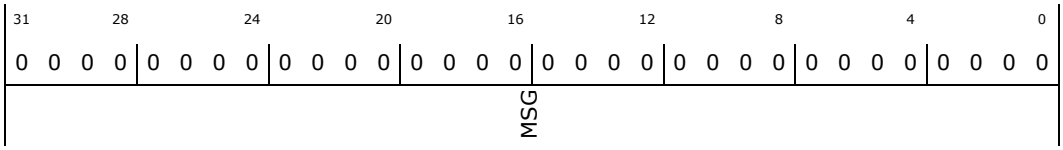
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1244h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.147 reg_SEC2ISH_MSG27_type (SEC2ISH_MSG27)—Offset 1248h

Message from SEC to ISH

Access Method

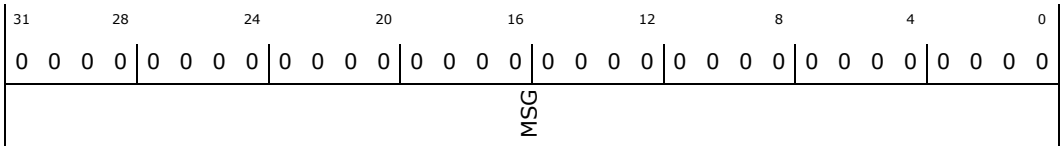
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1248h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.148 reg_SEC2ISH_MSG28_type (SEC2ISH_MSG28)—Offset 124Ch

Message from SEC to ISH

Access Method

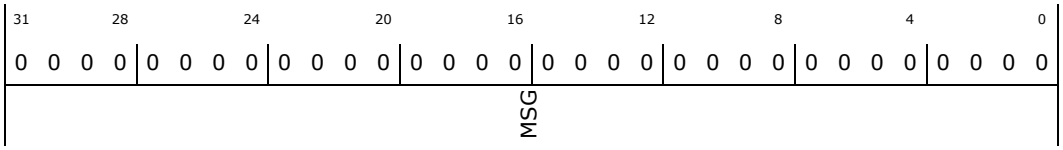
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 124Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.149 reg_SEC2ISH_MSG29_type (SEC2ISH_MSG29)—Offset 1250h

Message from SEC to ISH

Access Method

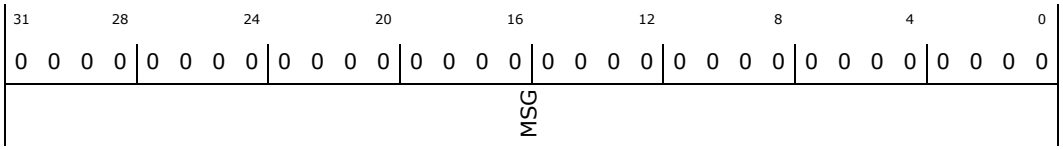
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1250h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.150 reg_SEC2ISH_MSG30_type (SEC2ISH_MSG30)—Offset 1254h

Message from SEC to ISH

Access Method

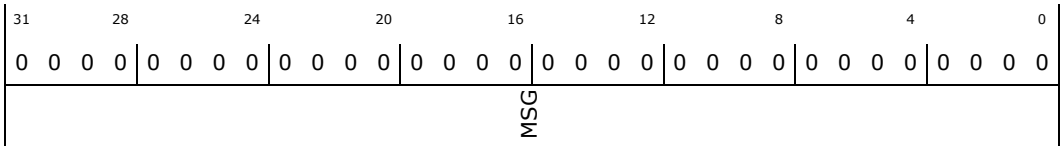
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1254h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.151 reg_SEC2ISH_MSG31_type (SEC2ISH_MSG31)—Offset 1258h

Message from SEC to ISH

Access Method

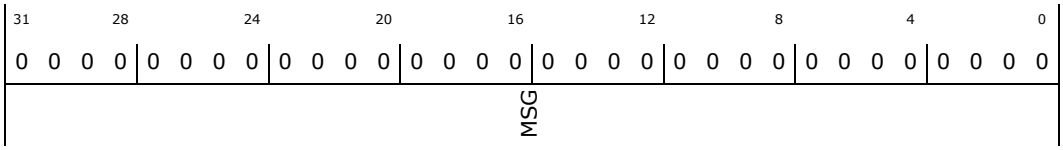
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1258h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.152 reg_SEC2ISH_MSG32_type (SEC2ISH_MSG32)—Offset 125Ch

Message from SEC to ISH

Access Method

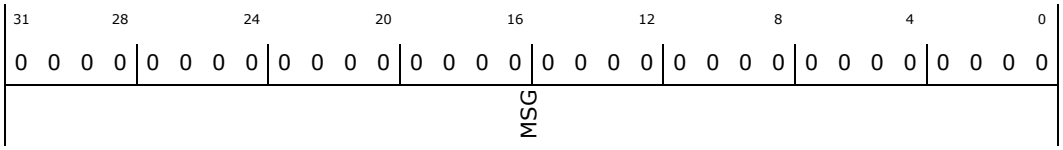
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 125Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.153 reg_ISH2PMC_MSG1_type (ISH2PMC_MSG1)—Offset 1260h

Message from ISH to PMC

Access Method

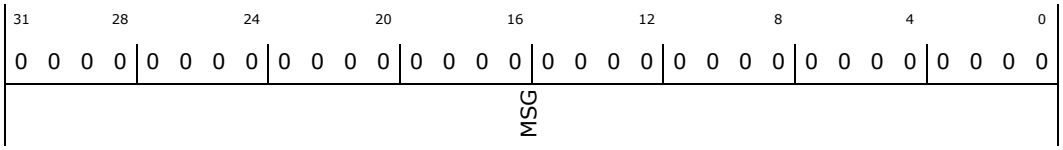
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1260h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.154 reg_ISH2PMC_MSG2_type (ISH2PMC_MSG2)—Offset 1264h

Message from ISH to PMC

Access Method

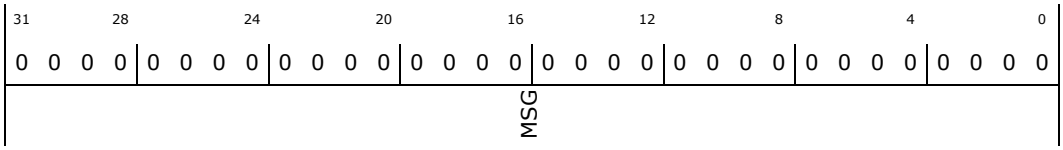
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1264h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.155 reg_ISH2PMC_MSG3_type (ISH2PMC_MSG3)—Offset 1268h

Message from ISH to PMC

Access Method

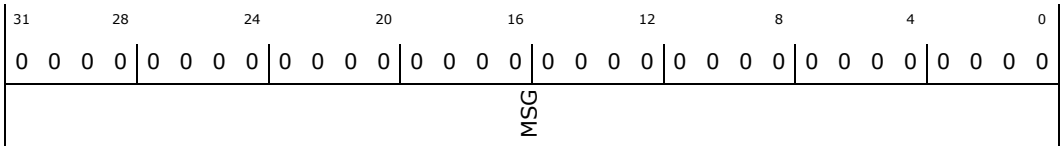
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1268h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.156 reg_ISH2PMC_MSG4_type (ISH2PMC_MSG4)—Offset 126Ch

Message from ISH to PMC

Access Method

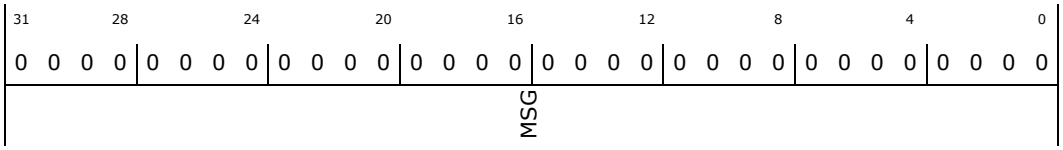
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 126Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.157 reg_ISH2PMC_MSG5_type (ISH2PMC_MSG5)—Offset 1270h

Message from ISH to PMC

Access Method

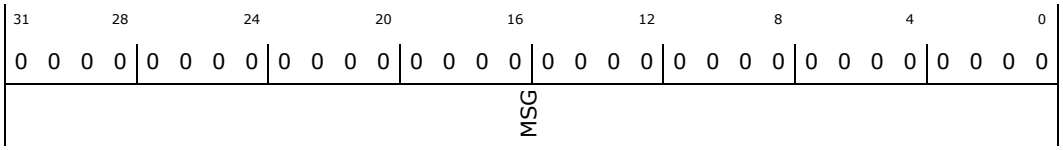
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1270h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.158 reg_ISH2PMC_MSG6_type (ISH2PMC_MSG6)—Offset 1274h

Message from ISH to PMC

Access Method

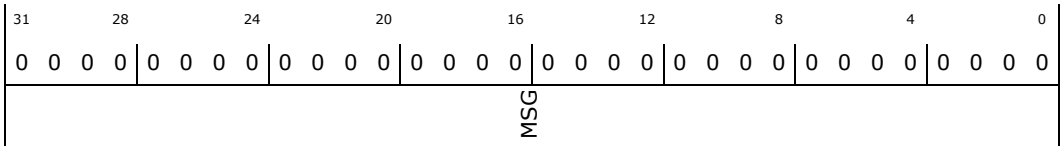
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1274h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.159 reg_ISH2PMC_MSG7_type (ISH2PMC_MSG7)—Offset 1278h

Message from ISH to PMC

Access Method

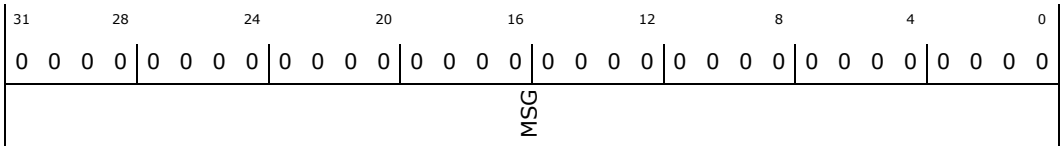
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1278h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.160 reg_ISH2PMC_MSG8_type (ISH2PMC_MSG8)—Offset 127Ch

Message from ISH to PMC

Access Method

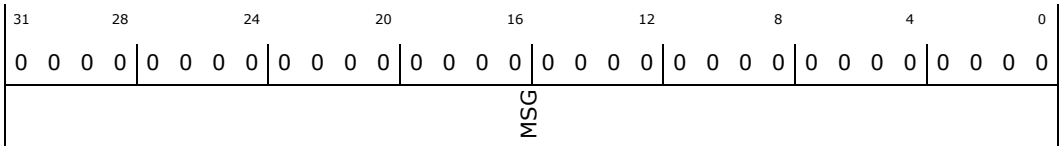
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 127Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.161 reg_ISH2PMC_MSG9_type (ISH2PMC_MSG9)—Offset 1280h

Message from ISH to PMC

Access Method

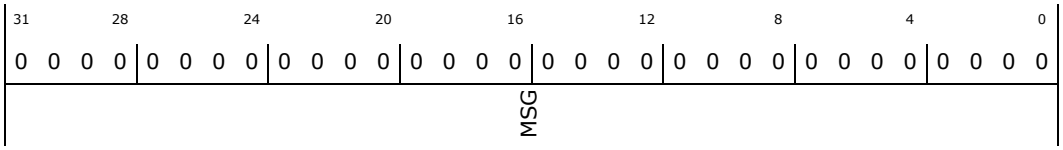
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1280h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.162 reg_ISH2PMC_MSG10_type (ISH2PMC_MSG10)—Offset 1284h

Message from ISH to PMC

Access Method

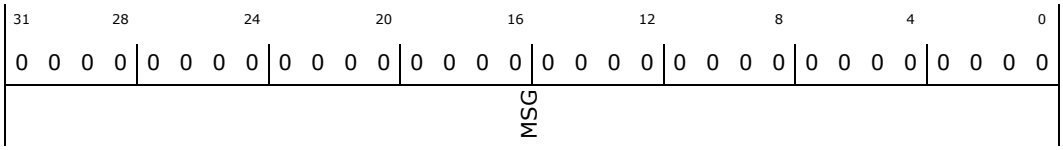
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1284h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.163 reg_ISH2PMC_MSG11_type (ISH2PMC_MSG11)—Offset 1288h

Message from ISH to PMC

Access Method

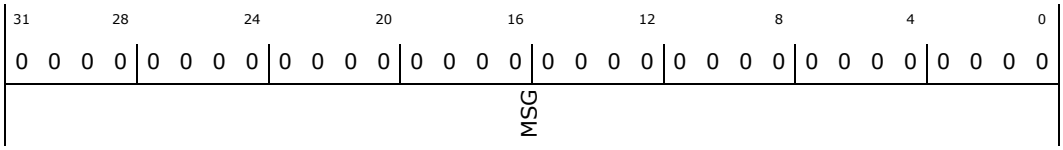
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1288h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.164 reg_ISH2PMC_MSG12_type (ISH2PMC_MSG12)—Offset 128Ch

Message from ISH to PMC

Access Method

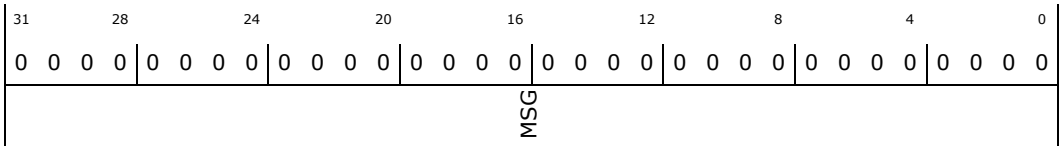
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 128Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.165 reg_ISH2PMC_MSG13_type (ISH2PMC_MSG13)—Offset 1290h

Message from ISH to PMC

Access Method

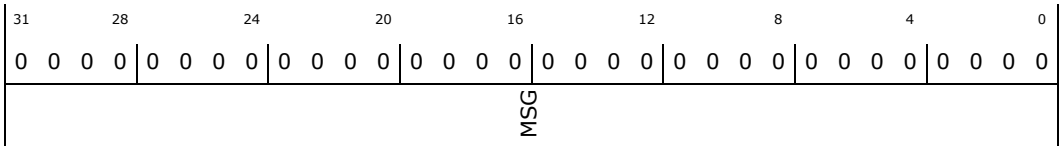
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1290h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.166 reg_ISH2PMC_MSG14_type (ISH2PMC_MSG14)—Offset 1294h

Message from ISH to PMC

Access Method

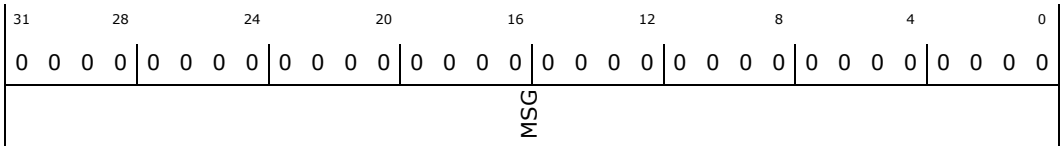
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1294h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.167 reg_ISH2PMC_MSG15_type (ISH2PMC_MSG15)—Offset 1298h

Message from ISH to PMC

Access Method

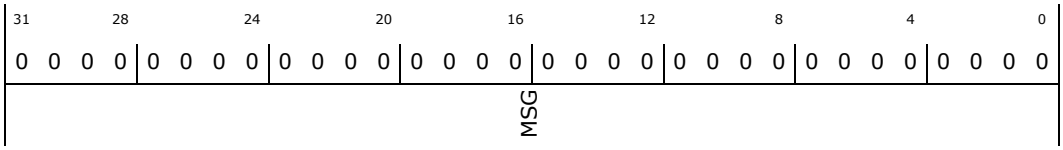
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1298h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.168 reg_ISH2PMC_MSG16_type (ISH2PMC_MSG16)—Offset 129Ch

Message from ISH to PMC

Access Method

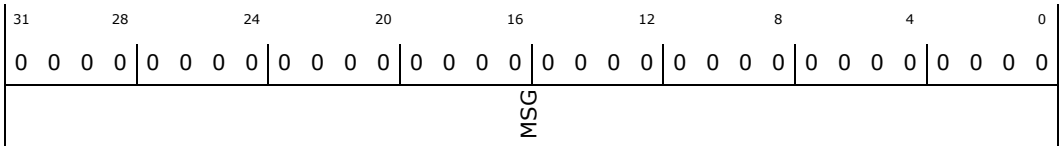
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 129Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.169 reg_ISH2PMC_MSG17_type (ISH2PMC_MSG17)—Offset 12A0h

Message from ISH to PMC

Access Method

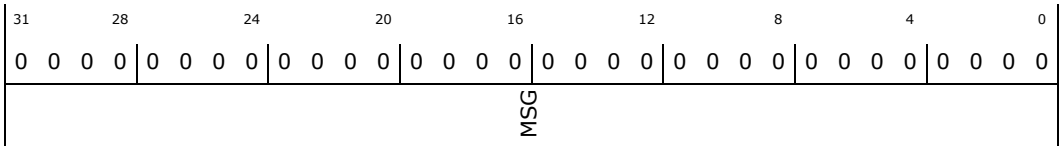
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12A0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.170 reg_ISH2PMC_MSG18_type (ISH2PMC_MSG18)—Offset 12A4h

Message from ISH to PMC

Access Method

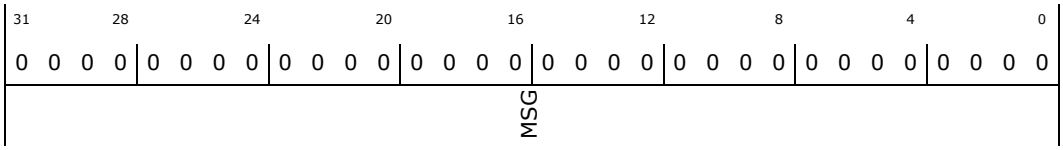
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12A4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.171 reg_ISH2PMC_MSG19_type (ISH2PMC_MSG19)—Offset 12A8h

Message from ISH to PMC

Access Method

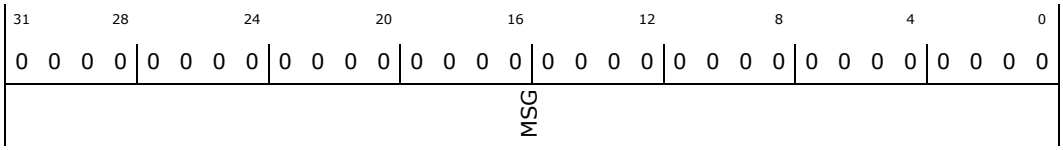
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12A8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.172 reg_ISH2PMC_MSG20_type (ISH2PMC_MSG20)—Offset 12ACh

Message from ISH to PMC

Access Method

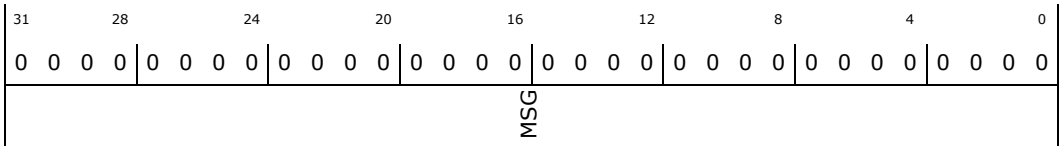
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12ACh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.173 reg_ISH2PMC_MSG21_type (ISH2PMC_MSG21)—Offset 12B0h

Message from ISH to PMC

Access Method

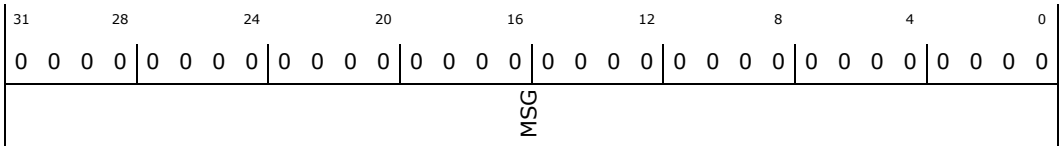
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12B0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.174 reg_ISH2PMC_MSG22_type (ISH2PMC_MSG22)—Offset 12B4h

Message from ISH to PMC

Access Method

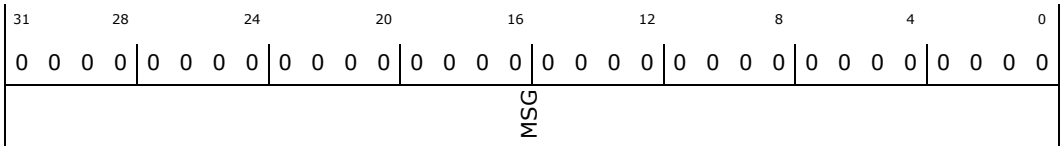
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12B4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.175 reg_ISH2PMC_MSG23_type (ISH2PMC_MSG23)—Offset 12B8h

Message from ISH to PMC

Access Method

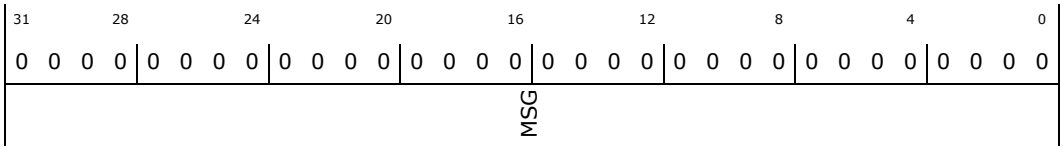
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12B8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.176 reg_ISH2PMC_MSG24_type (ISH2PMC_MSG24)—Offset 12BCh

Message from ISH to PMC

Access Method

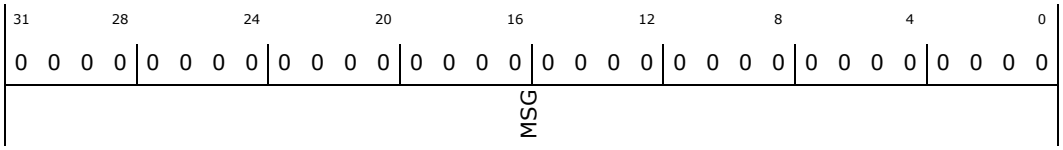
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12BCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.177 reg_ISH2PMC_MSG25_type (ISH2PMC_MSG25)—Offset 12C0h

Message from ISH to PMC

Access Method

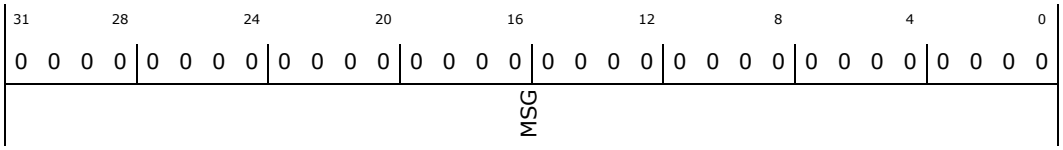
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12C0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.178 reg_ISH2PMC_MSG26_type (ISH2PMC_MSG26)—Offset 12C4h

Message from ISH to PMC

Access Method

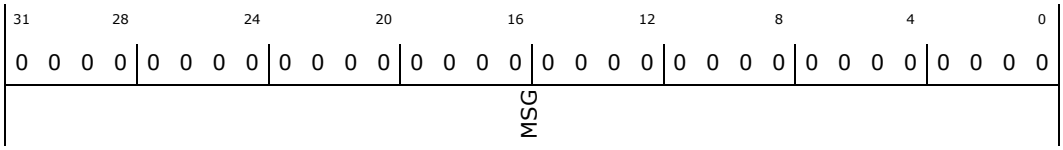
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12C4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.179 reg_ISH2PMC_MSG27_type (ISH2PMC_MSG27)—Offset 12C8h

Message from ISH to PMC

Access Method

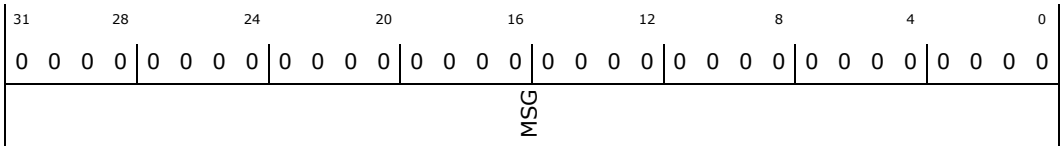
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12C8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.180 reg_ISH2PMC_MSG28_type (ISH2PMC_MSG28)—Offset 12CCh

Message from ISH to PMC

Access Method

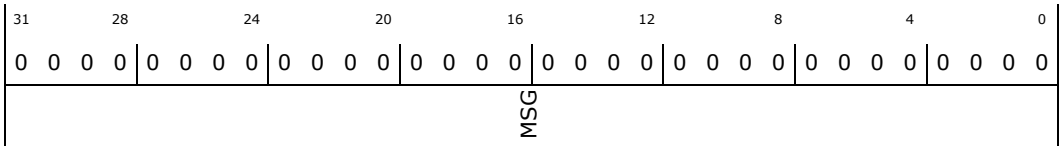
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12CCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.181 reg_ISH2PMC_MSG29_type (ISH2PMC_MSG29)—Offset 12D0h

Message from ISH to PMC

Access Method

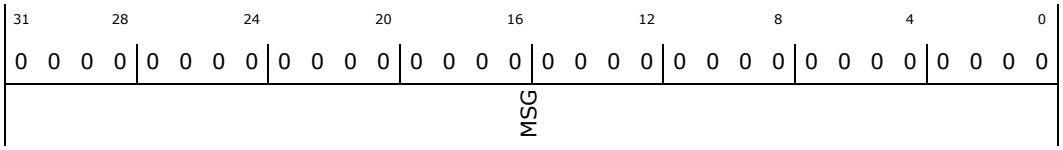
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12D0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.182 reg_ISH2PMC_MSG30_type (ISH2PMC_MSG30)—Offset 12D4h

Message from ISH to PMC

Access Method

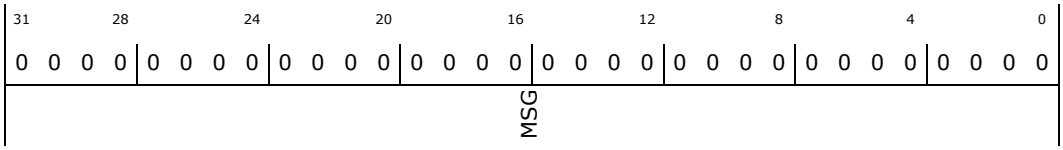
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12D4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.183 reg_ISH2PMC_MSG31_type (ISH2PMC_MSG31)—Offset 12D8h

Message from ISH to PMC

Access Method

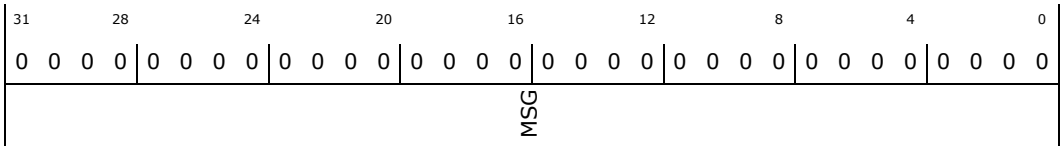
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12D8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.184 reg_ISH2PMC_MSG32_type (ISH2PMC_MSG32)—Offset 12DCh

Message from ISH to PMC

Access Method

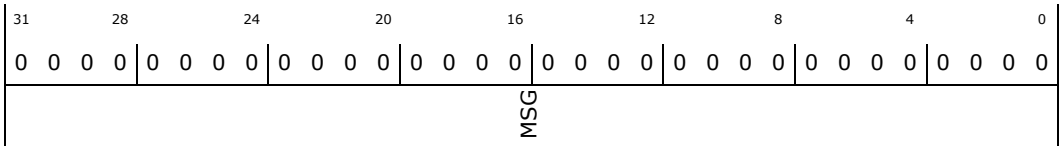
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12DCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.185 reg_PMC2ISH_MSG1_type (PMC2ISH_MSG1)—Offset 12E0h

Message from PMC to ISH

Access Method

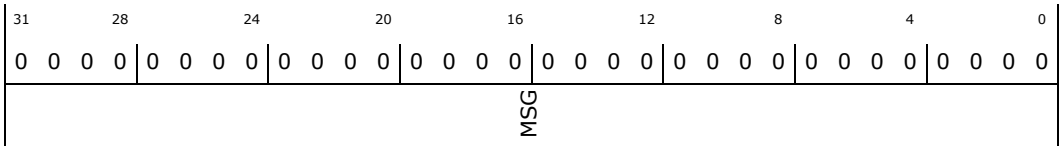
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12E0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.186 reg_PMC2ISH_MSG2_type (PMC2ISH_MSG2)—Offset 12E4h

Message from PMC to ISH

Access Method

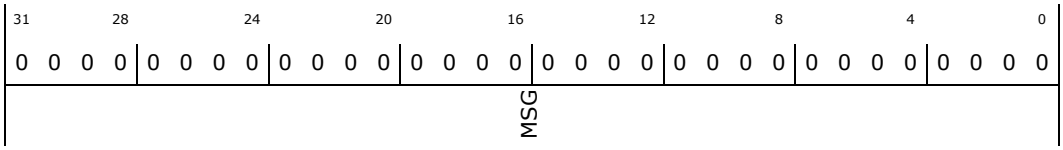
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12E4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.187 reg_PMC2ISH_MSG3_type (PMC2ISH_MSG3)—Offset 12E8h

Message from PMC to ISH

Access Method

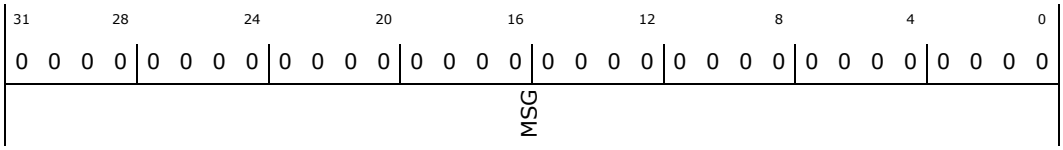
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12E8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.188 reg_PMC2ISH_MSG4_type (PMC2ISH_MSG4)—Offset 12ECh

Message from PMC to ISH

Access Method

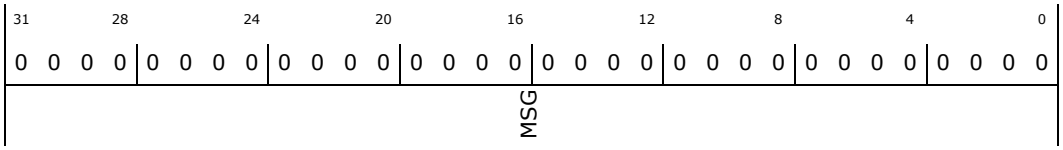
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12ECh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.189 reg_PMC2ISH_MSG5_type (PMC2ISH_MSG5)—Offset 12F0h

Message from PMC to ISH

Access Method

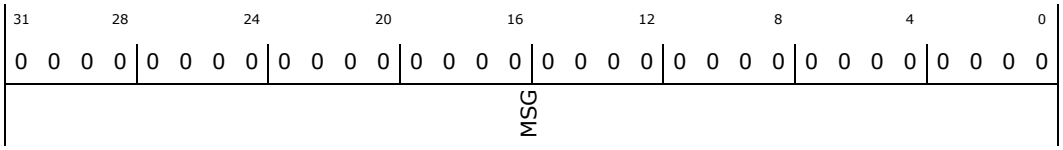
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12F0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.190 reg_PMC2ISH_MSG6_type (PMC2ISH_MSG6)—Offset 12F4h

Message from PMC to ISH

Access Method

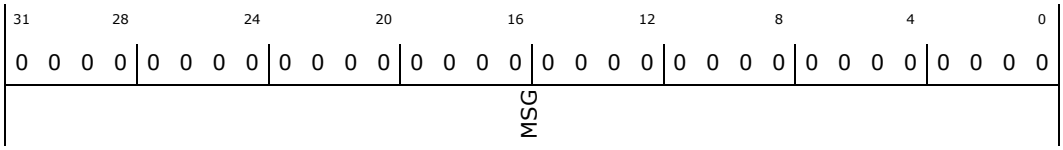
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12F4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.191 reg_PMC2ISH_MSG7_type (PMC2ISH_MSG7)—Offset 12F8h

Message from PMC to ISH

Access Method

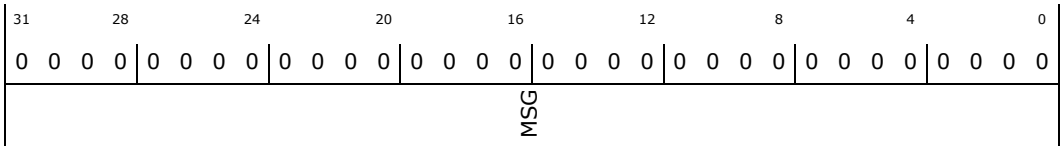
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12F8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.192 reg_PMC2ISH_MSG8_type (PMC2ISH_MSG8)—Offset 12FCh

Message from PMC to ISH

Access Method

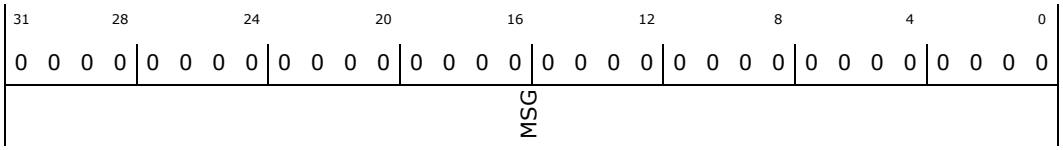
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 12FCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.193 reg_PMC2ISH_MSG9_type (PMC2ISH_MSG9)—Offset 1300h

Message from PMC to ISH

Access Method

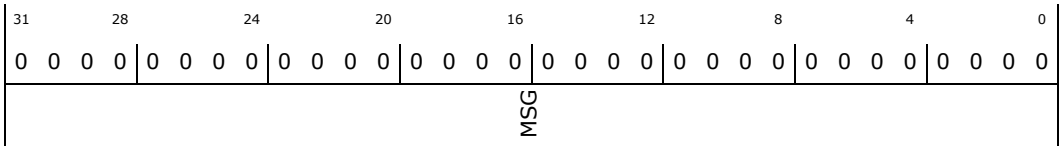
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1300h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.194 reg_PMC2ISH_MSG10_type (PMC2ISH_MSG10)—Offset 1304h

Message from PMC to ISH

Access Method

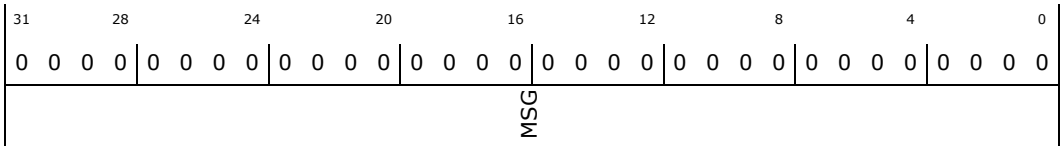
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1304h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.195 reg_PMC2ISH_MSG11_type (PMC2ISH_MSG11)—Offset 1308h

Message from PMC to ISH

Access Method

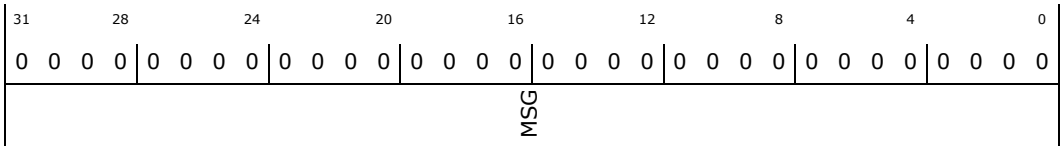
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1308h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.196 reg_PMC2ISH_MSG12_type (PMC2ISH_MSG12)—Offset 130Ch

Message from PMC to ISH

Access Method

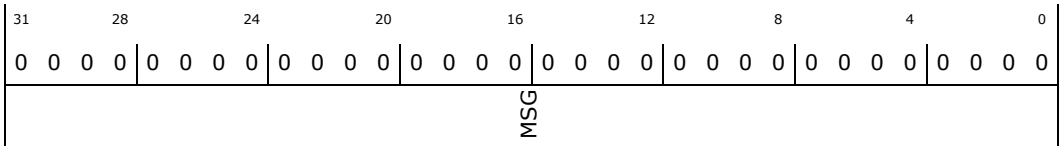
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 130Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.197 reg_PMC2ISH_MSG13_type (PMC2ISH_MSG13)—Offset 1310h

Message from PMC to ISH

Access Method

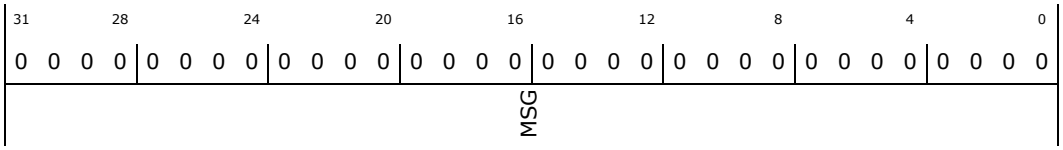
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1310h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.198 reg_PMC2ISH_MSG14_type (PMC2ISH_MSG14)—Offset 1314h

Message from PMC to ISH

Access Method

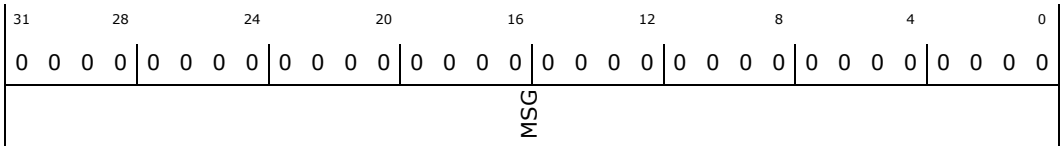
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1314h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.199 reg_PMC2ISH_MSG15_type (PMC2ISH_MSG15)—Offset 1318h

Message from PMC to ISH

Access Method

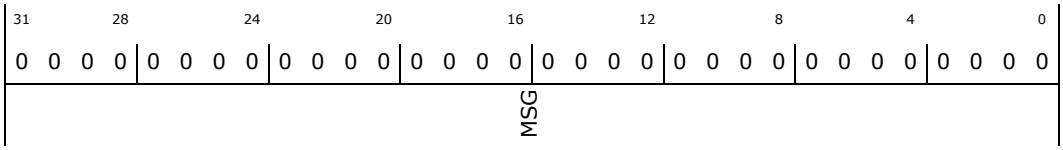
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1318h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.200 reg_PMC2ISH_MSG16_type (PMC2ISH_MSG16)—Offset 131Ch

Message from PMC to ISH

Access Method

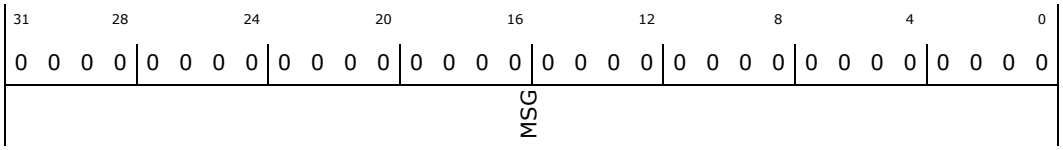
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 131Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.201 reg_PMC2ISH_MSG17_type (PMC2ISH_MSG17)—Offset 1320h

Message from PMC to ISH

Access Method

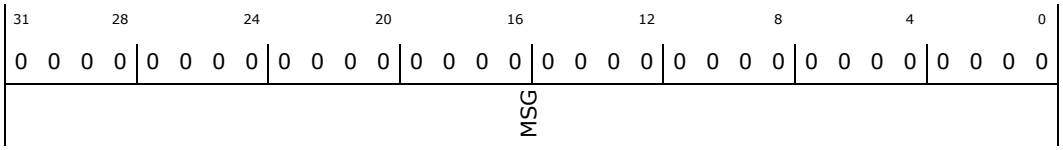
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1320h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.202 reg_PMC2ISH_MSG18_type (PMC2ISH_MSG18)—Offset 1324h

Message from PMC to ISH

Access Method

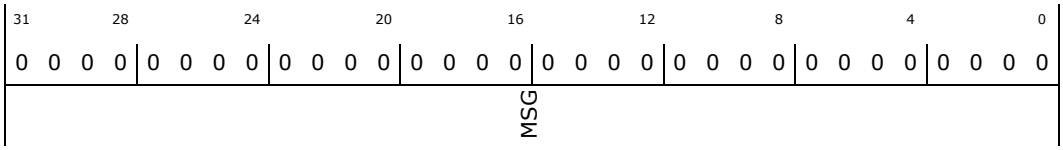
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1324h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.203 reg_PMC2ISH_MSG19_type (PMC2ISH_MSG19)—Offset 1328h

Message from PMC to ISH

Access Method

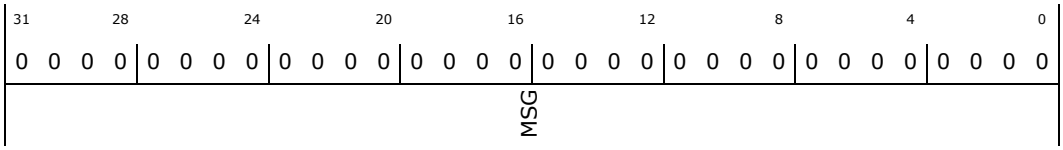
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1328h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.204 reg_PMC2ISH_MSG20_type (PMC2ISH_MSG20)—Offset 132Ch

Message from PMC to ISH

Access Method

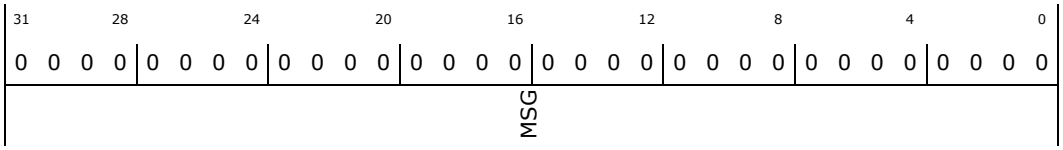
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 132Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.205 reg_PMC2ISH_MSG21_type (PMC2ISH_MSG21)—Offset 1330h

Message from PMC to ISH

Access Method

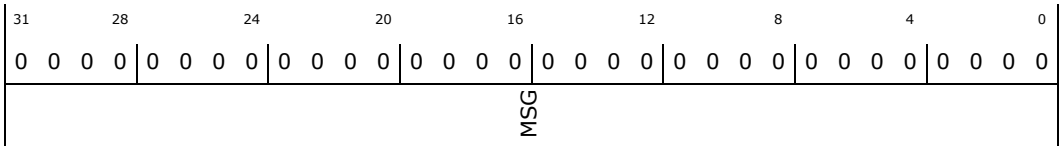
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1330h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.206 reg_PMC2ISH_MSG22_type (PMC2ISH_MSG22)—Offset 1334h

Message from PMC to ISH

Access Method

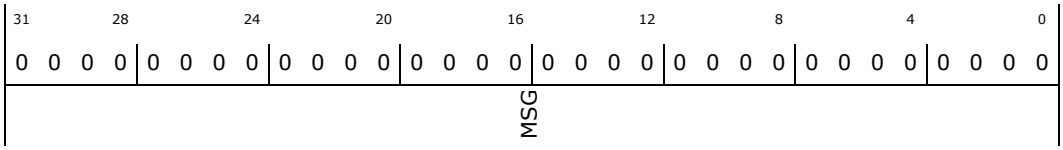
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1334h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.207 reg_PMC2ISH_MSG23_type (PMC2ISH_MSG23)—Offset 1338h

Message from PMC to ISH

Access Method

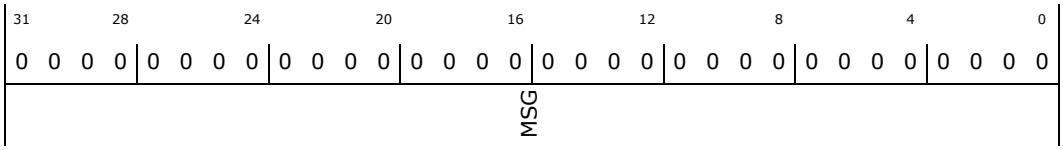
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1338h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.208 reg_PMC2ISH_MSG24_type (PMC2ISH_MSG24)—Offset 133Ch

Message from PMC to ISH

Access Method

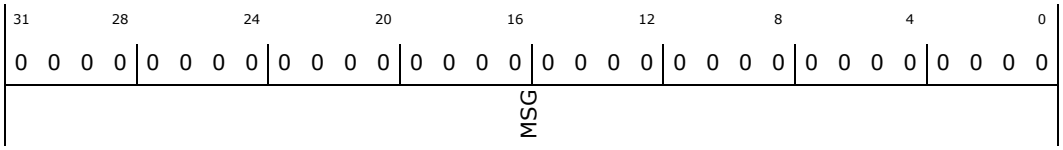
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 133Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.209 reg_PMC2ISH_MSG25_type (PMC2ISH_MSG25)—Offset 1340h

Message from PMC to ISH

Access Method

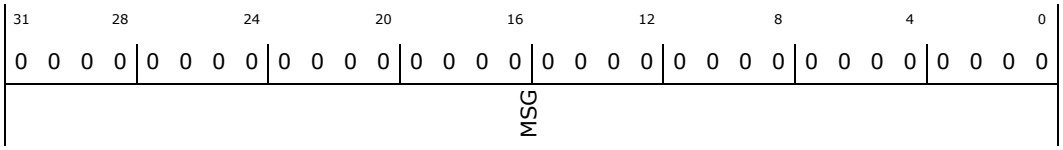
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1340h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.210 reg_PMC2ISH_MSG26_type (PMC2ISH_MSG26)—Offset 1344h

Message from PMC to ISH

Access Method

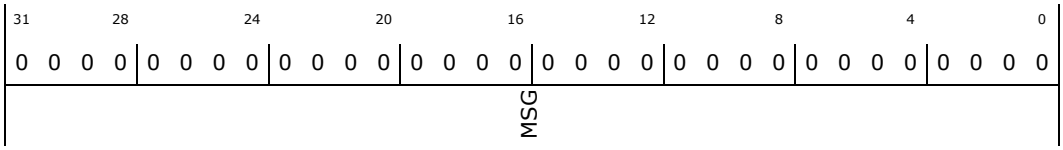
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1344h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.211 reg_PMC2ISH_MSG27_type (PMC2ISH_MSG27)—Offset 1348h

Message from PMC to ISH

Access Method

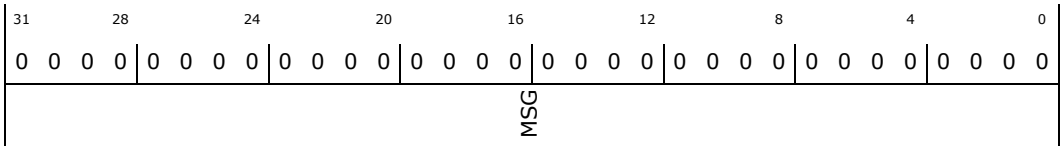
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1348h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.212 reg_PMC2ISH_MSG28_type (PMC2ISH_MSG28)—Offset 134Ch

Message from PMC to ISH

Access Method

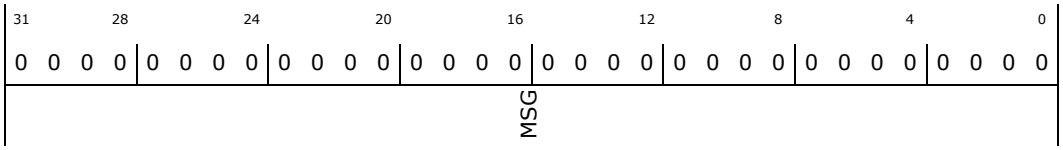
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 134Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.213 reg_PMC2ISH_MSG29_type (PMC2ISH_MSG29)—Offset 1350h

Message from PMC to ISH

Access Method

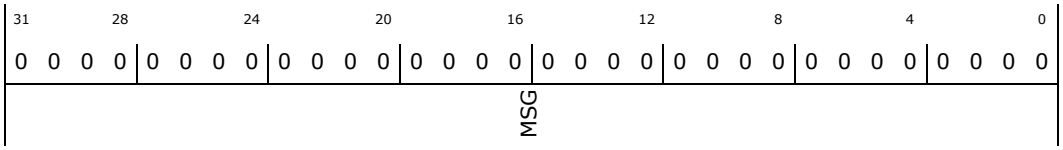
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1350h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.214 reg_PMC2ISH_MSG30_type (PMC2ISH_MSG30)—Offset 1354h

Message from PMC to ISH

Access Method

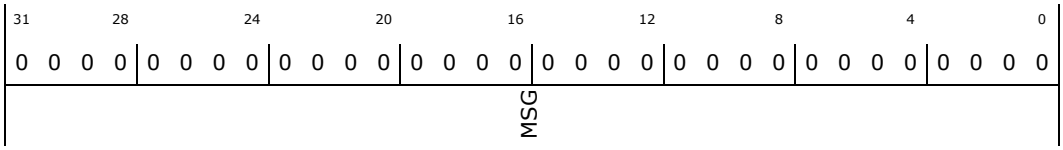
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1354h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.215 reg_PMC2ISH_MSG31_type (PMC2ISH_MSG31)—Offset 1358h

Message from PMC to ISH

Access Method

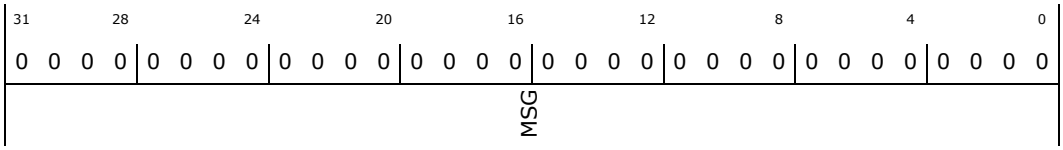
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1358h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.216 reg_PMC2ISH_MSG32_type (PMC2ISH_MSG32)—Offset 135Ch

Message from PMC to ISH

Access Method

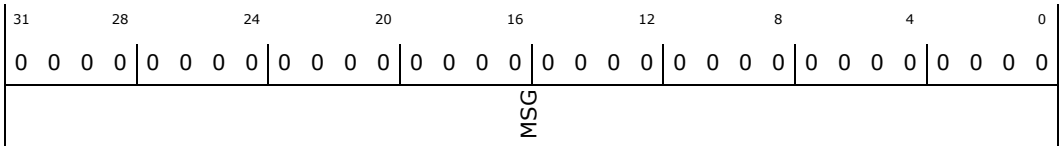
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 135Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**MSG:** ish_clk

12.3.217 reg_REMAP0_type (REMAP0)—Offset 1360h

REMAP0

Access Method

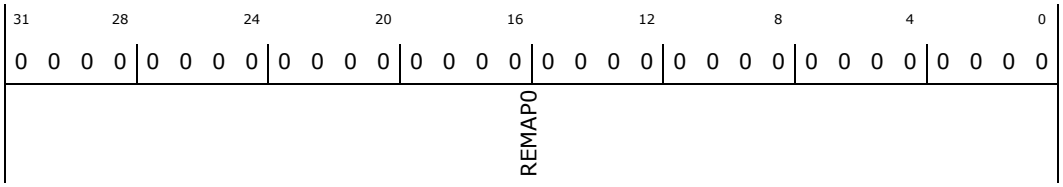
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1360h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**REMAP0:** ish_clk

12.3.218 reg_REMAP1_type (REMAP1)—Offset 1364h

REMAP1

Access Method

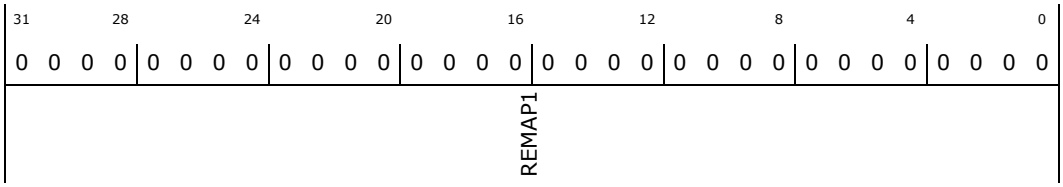
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1364h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**REMAP1:** ish_clk

12.3.219 reg_REMAP2_type (REMAP2)—Offset 1368h

REMAP2

Access Method

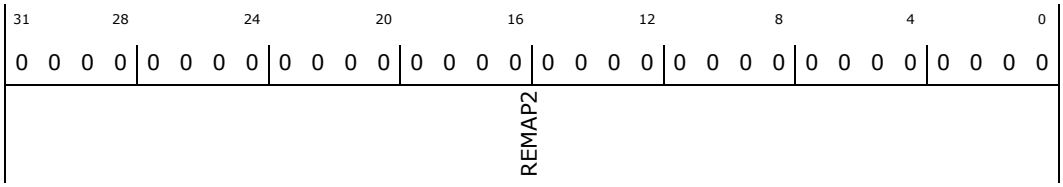
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1368h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**REMAP2:** ish_clk

12.3.220 reg_REMAP3_type (REMAP3)—Offset 136Ch

REMAP3

Access Method

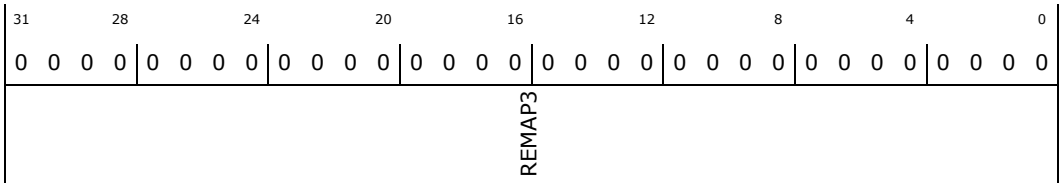
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 136Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**REMAP3:** ish_clk

12.3.221 reg_REMAP4_type (REMAP4)—Offset 1370h

REMAP4

Access Method

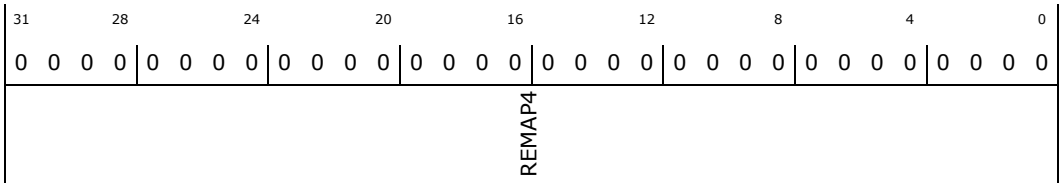
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1370h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**REMAP4:** ish_clk

12.3.222 reg_REMAP5_type (REMAP5)—Offset 1374h

REMAP5

Access Method

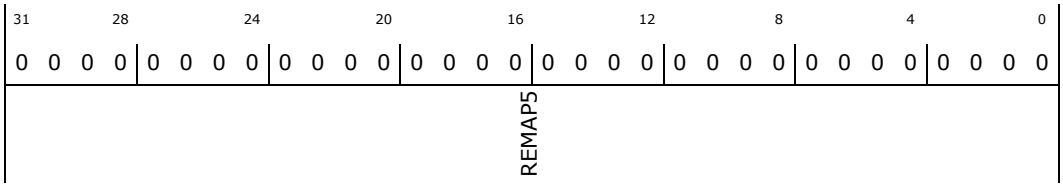
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1374h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**REMAP5:** ish_clk

12.3.223 reg_ISH_IPC_BUSY_CLEAR_type (ISH_IPC_BUSY_CLEAR)—Offset 1378h

Reserved

Access Method

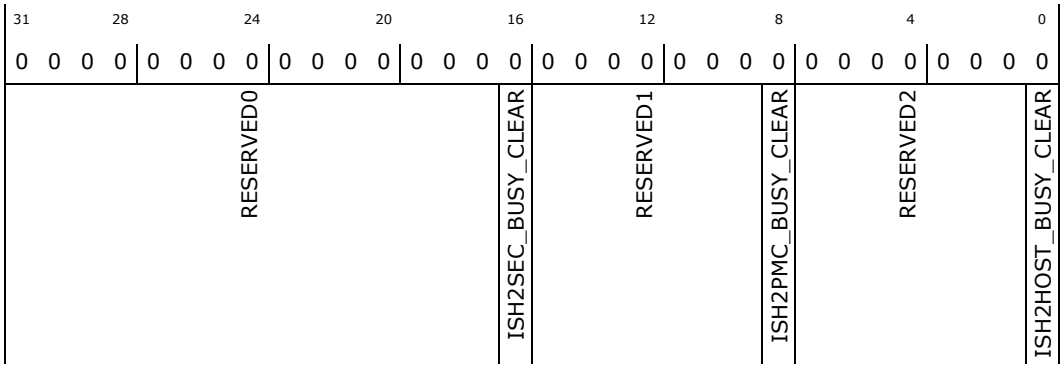
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1378h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0x0 RO	**RESERVED0:** ish_clk
16	0x0 RW/1C	**ISH2SEC_BUSY_CLEAR:** ish_clk
15:9	0x0 RO	**RESERVED1:** ish_clk
8	0x0 RW/1C	**ISH2PMC_BUSY_CLEAR:** ish_clk
7:1	0x0 RO	**RESERVED2:** ish_clk

Bit Range	Default & Access	Field Name (ID): Description
0	0x0 RW/1C	**ISH2HOST_BUSY_CLEAR:** ish_clk

12.3.224 reg_ISH_FUSE_type (ISH_FUSE)—Offset 137Ch

Reserved

Access Method

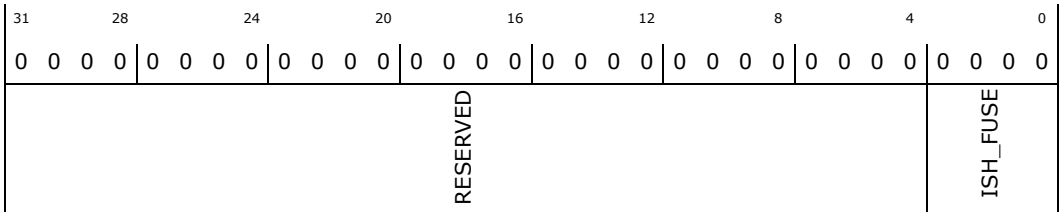
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 137Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**RESERVED:** ish_clk
3:0	0x0 RO	**ISH_FUSE:** ish_clk

12.3.225 reg_UMA_RANGE_LOWER_0_type (UMA_RANGE_LOWER_0)—Offset 1380h

UMA base address LSB register

Access Method

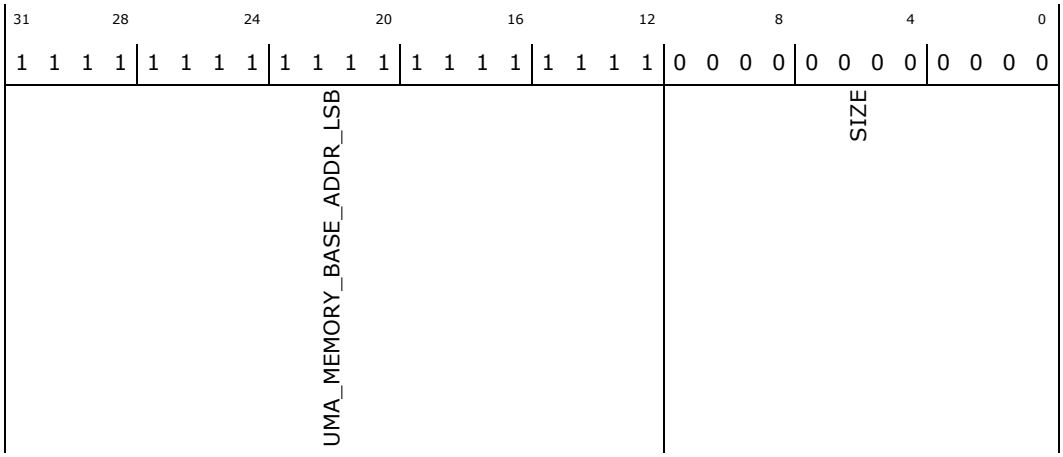
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1380h

Op Codes:

h - Read, h - Write

Default: FFFFF000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0xfffff RW	**UMA_MEMORY_BASE_ADDR_LSB:** ish_clk
11:0	0x0 RO	**SIZE:** ish_clk

12.3.226 reg_UMA_RANGE_LOWER_1_type (UMA_RANGE_LOWER_1)—Offset 1384h

UMA base address MSB register

Access Method

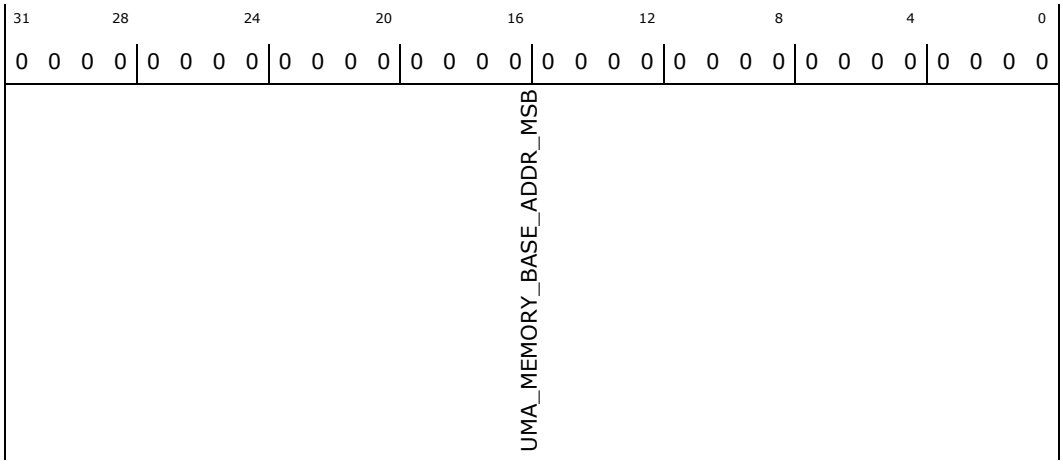
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1384h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**UMA_MEMORY_BASE_ADDR_MSB:** ish_clk

12.3.227 reg_UMA_RANGE_UPPER_0_type (UMA_RANGE_UPPER_0)—Offset 1388h

UMA limit address LSB register

Access Method

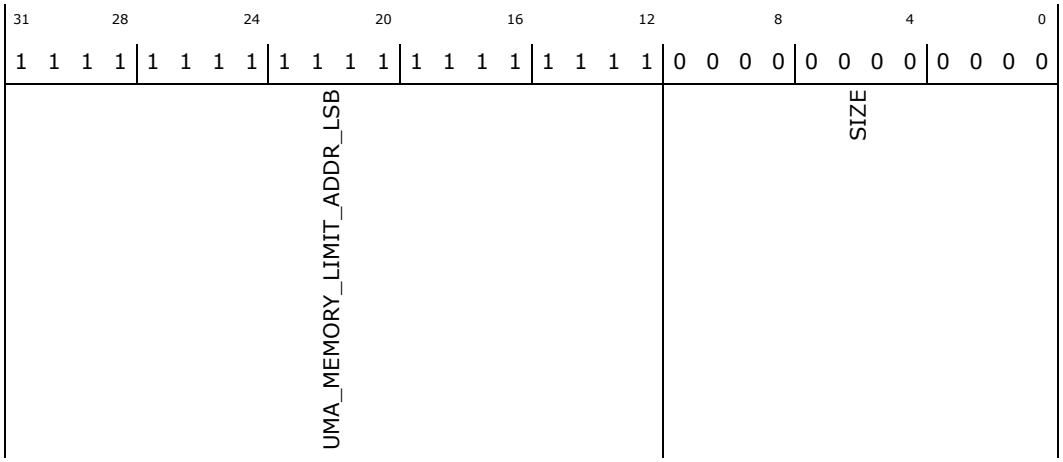
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1388h

Op Codes:

h - Read, h - Write

Default: FFFFF000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0xfffff RW	**UMA_MEMORY_LIMIT_ADDR_LSB:** ish_clk
11:0	0x0 RO	**SIZE:** ish_clk

12.3.228 reg_UMA_RANGE_UPPER_1_type (UMA_RANGE_UPPER_1)—Offset 138Ch

UMA limit address MSB register

Access Method

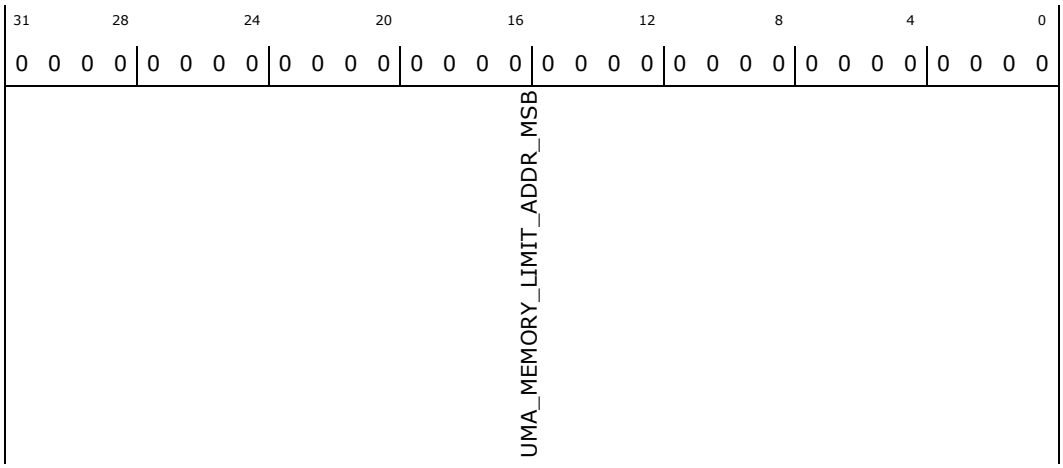
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 138Ch

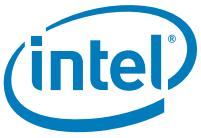
Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**UMA_MEMORY_LIMIT_ADDR_MSB:** ish_clk



12.4 IOSF2OCP PCI Configuration Registers

Table 123. Summary of ISH IOSF2OCP PCI Configuration Registers—0/10/0

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0–3h	4	"reg_DEVVENDID_type (DEVVENDID)—Offset 0h" on page 6543	22D88086h
4–7h	4	"reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h" on page 6543	00100000h
8–Bh	4	"reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h" on page 6544	00000006h
C–Fh	4	"reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch" on page 6545	00000000h
10–13h	4	"reg_BAR_type (BAR)—Offset 10h" on page 6545	00000000h
14–17h	4	"reg_BAR_HIGH_type (BAR_HIGH)—Offset 14h" on page 6546	00000000h
18–1Bh	4	"reg_BAR1_type (BAR1)—Offset 18h" on page 6547	00000000h
1C–1Fh	4	"reg_BAR1_HIGH_type (BAR1_HIGH)—Offset 1Ch" on page 6547	00000000h
2C–2Fh	4	"reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch" on page 6548	00000000h
30–33h	4	"reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 6548	00000000h
34–37h	4	"reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h" on page 6549	00000080h
3C–3Fh	4	"reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch" on page 6549	00000100h
80–83h	4	"reg_POWERCAPID_type (POWERCAPID)—Offset 80h" on page 6550	00030001h
84–87h	4	"reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h" on page 6551	00000008h
A0–A3h	4	"reg_GEN_REGRW1_type (GEN_REGRW1)—Offset A0h" on page 6552	00000000h
A4–A7h	4	"reg_GEN_REGRW2_type (GEN_REGRW2)—Offset A4h" on page 6552	00000000h
A8–ABh	4	"reg_GEN_REGRW3_type (GEN_REGRW3)—Offset A8h" on page 6552	00000000h
AC–AFh	4	"reg_GEN_REGRW4_type (GEN_REGRW4)—Offset ACh" on page 6553	00000000h
C0–C3h	4	"reg_GEN_INPUT_REG_type (GEN_INPUT_REG)—Offset C0h" on page 6553	00000000h
F8–FBh	4	"reg_MANID_type (MANID)—Offset F8h" on page 6554	00000000h

12.4.1 reg_DEVVENDID_type (DEVVENDID)—Offset 0h

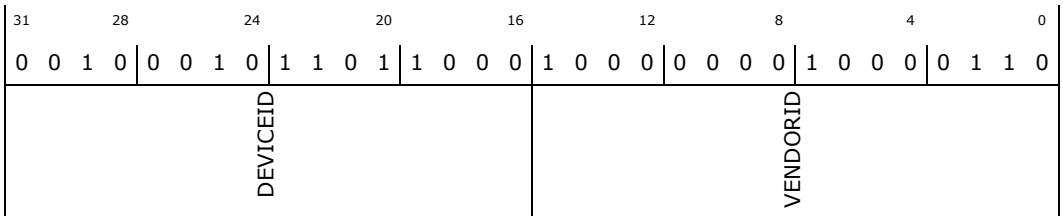
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + 0h

Default: 22D88086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x22d8 RO	**DEVICEID:** Reserved.
15:0	0x8086 RO	**VENDORID:** Reserved.

12.4.2 reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h

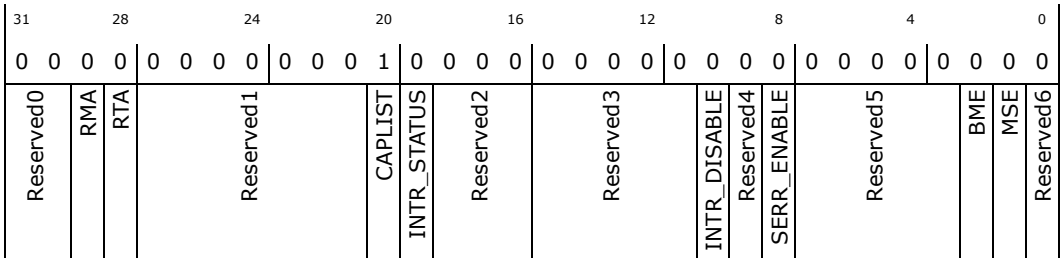
STATUSCOMMAND- Status and Command

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + 4h

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved0:** Reserved.
29	0x0 RW/1C	**RMA:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
28	0x0 RW/1C	**RTA:** Reserved.
27:21	0x0 RO	**Reserved1:** Reserved.
20	0x1 RO	**CAPLIST:** Reserved.
19	0x0 RO	**INTR_STATUS:** Reserved.
18:16	0x0 RO	**Reserved2:** Reserved.
15:11	0x0 RO	**Reserved3:** Reserved.
10	0x0 RW	**INTR_DISABLE:** Reserved.
9	0x0 RO	**Reserved4:** Reserved.
8	0x0 RW	**SERR_ENABLE:** Reserved.
7:3	0x0 RO	**Reserved5:** Reserved.
2	0x0 RW	**BME:** Reserved.
1	0x0 RW	**MSE:** Reserved.
0	0x0 RO	**Reserved6:** Reserved.

12.4.3 reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h

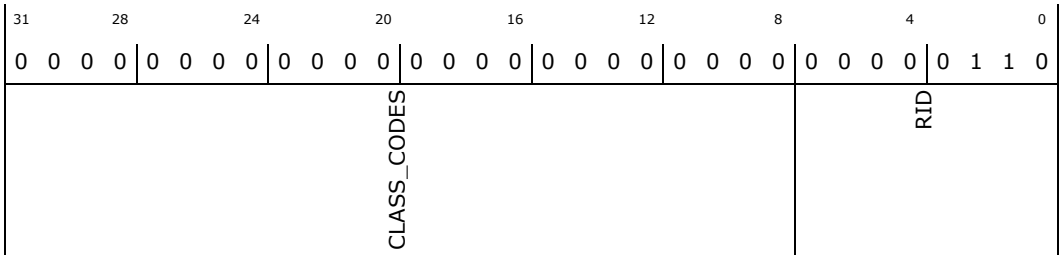
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + 8h

Default: 00000006h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** Reserved.
7:0	0x6 RO	**RID:** Reserved.

12.4.4 reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch

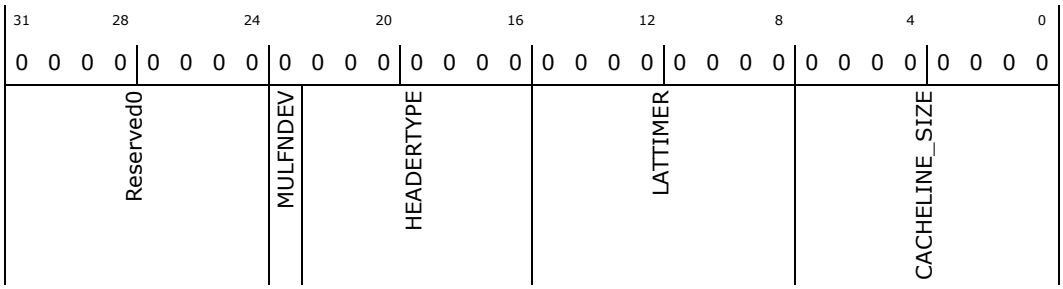
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved.
23	0x0 RO	**MULFNDEV:** Reserved.
22:16	0x0 RO	**HEADERTYPE:** Reserved.
15:8	0x0 RO	**LATTIMER:** Reserved.
7:0	0x0 RW	**CACHELINE_SIZE:** Reserved.

12.4.5 reg_BAR_type (BAR)—Offset 10h

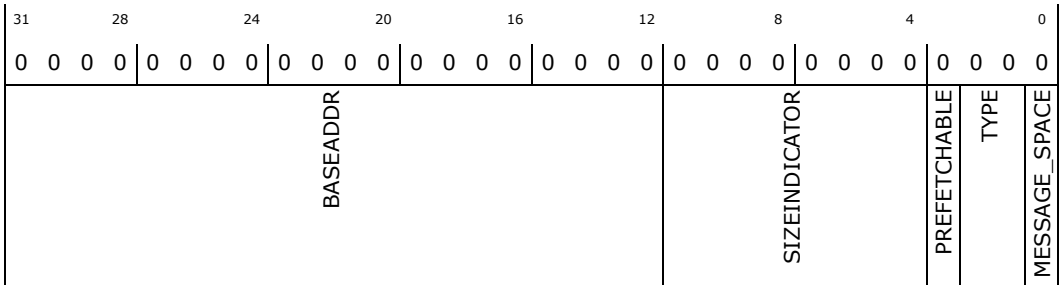
BAR -Base Address Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW/V	**BASEADDR:** Reserved.
11:4	0x0 RO	**SIZEINDICATOR:** Reserved.
3	0x0 RO	**PREFETCHABLE:** Reserved.
2:1	0x0 RO	**TYPE:** Reserved.
0	0x0 RO	**MESSAGE_SPACE:** Reserved.

12.4.6 reg_BAR_HIGH_type (BAR_HIGH)—Offset 14h

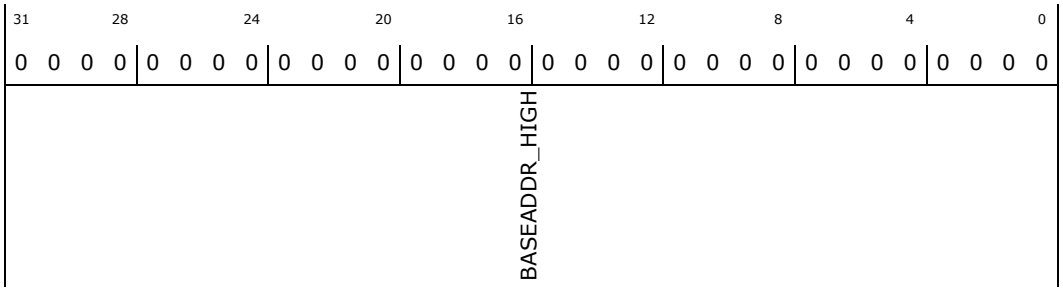
BAR -Base Address Register High

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + 14h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**BASEADDR_HIGH:** Reserved.

12.4.7 reg_BAR1_type (BAR1)—Offset 18h

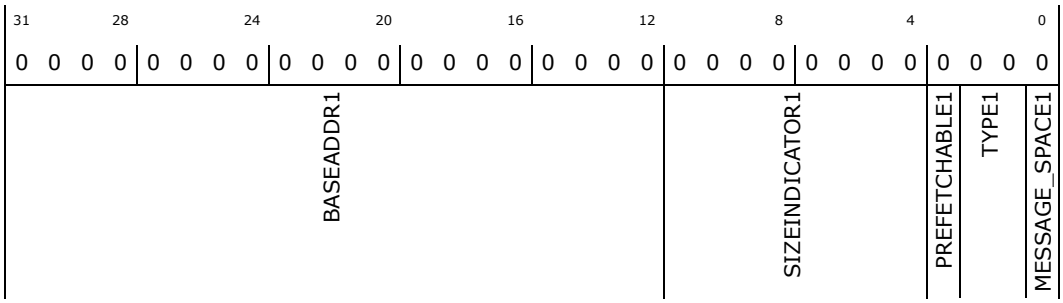
BAR1 -Base Address Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + 18h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Reserved.
11:4	0x0 RO	**SIZEINDICATOR1:** Reserved.
3	0x0 RO	**PREFETCHABLE1:** Reserved.
2:1	0x0 RO	**TYPE1:** Reserved.
0	0x0 RO	**MESSAGE_SPACE1:** Reserved.

12.4.8 reg_BAR1_HIGH_type (BAR1_HIGH)—Offset 1Ch

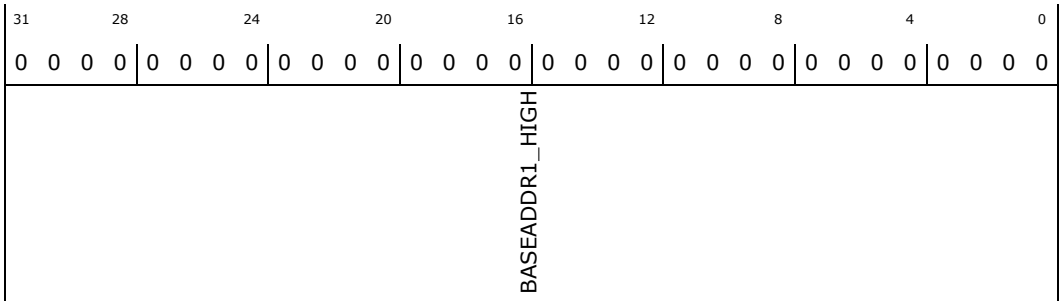
BAR1 -Base Address Register1 High

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + 1Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**BASEADDR1_HIGH:** Reserved.

12.4.9 reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch

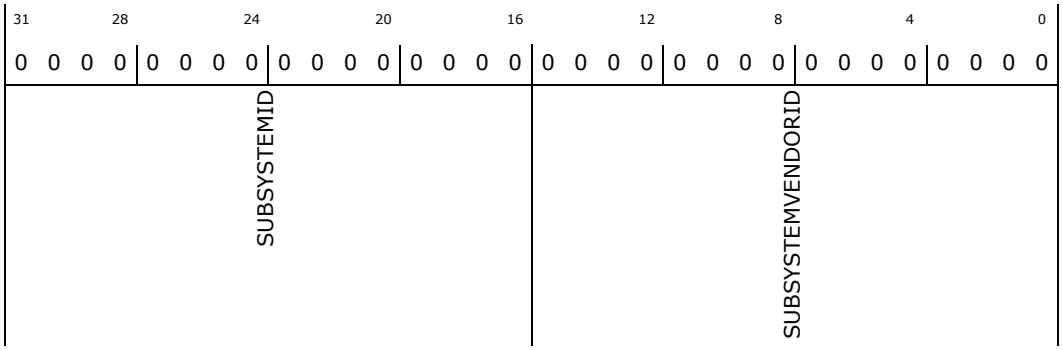
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Reserved.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Reserved.

12.4.10 reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h

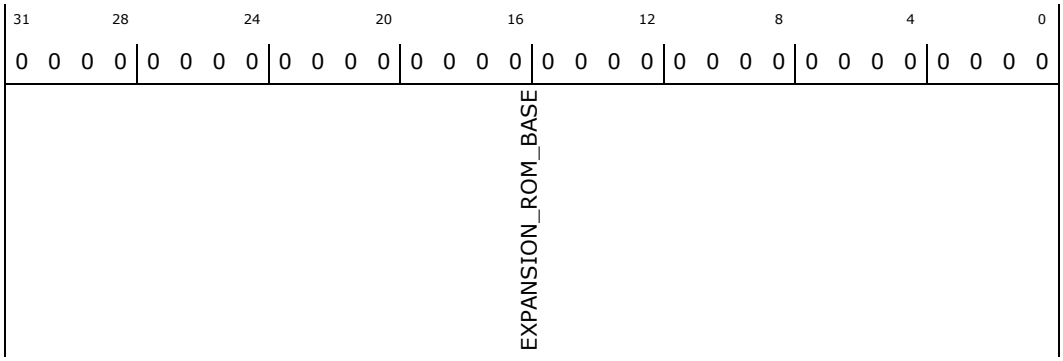
EXPANSION ROM base address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + 30h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** Reserved.

12.4.11 reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h

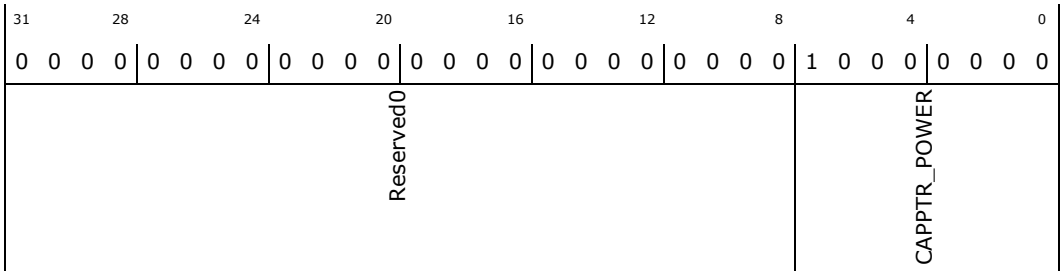
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + 34h

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved.
7:0	0x80 RO	**CAPPTR_POWER:** Reserved.

12.4.12 reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch

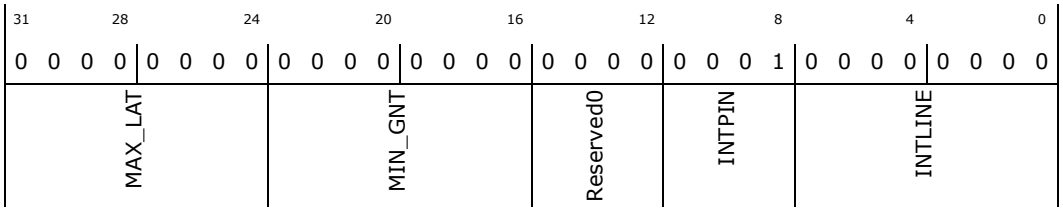
INTERRUPTREG - Interrupt Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + 3Ch

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Reserved.
23:16	0x0 RO	**MIN_GNT:** Reserved.
15:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x1 RO	**INTPIN:** Reserved.
7:0	0x0 RW	**INTLINE:** Reserved.

12.4.13 reg_POWERCAPID_type (POWERCAPID)—Offset 80h

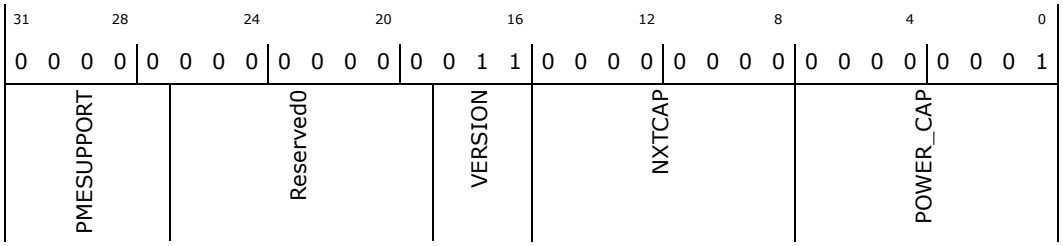
POWERCAPID - PowerManagement Capability ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + 80h

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** Reserved.
26:19	0x0 RO	**Reserved0:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
18:16	0x3 RO	**VERSION:** Reserved.
15:8	0x0 RO	**NXTCAP:** Reserved.
7:0	0x1 RO	**POWER_CAP:** Reserved.

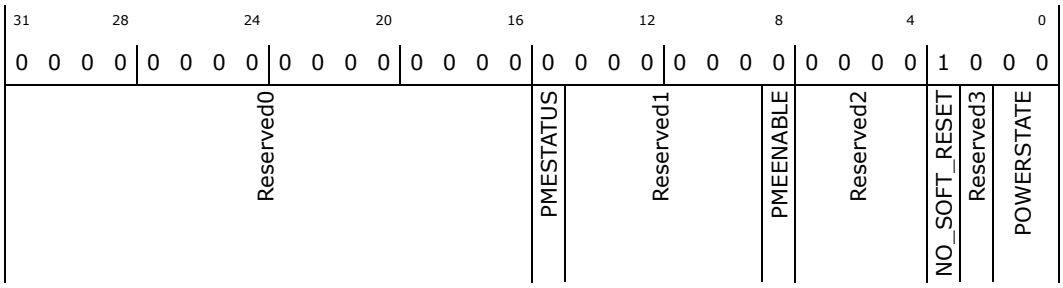
12.4.14 reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + 84h

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved.
15	0x0 RW/1C	**PMESTATUS:** Reserved.
14:9	0x0 RO	**Reserved1:** Reserved.
8	0x0 RW	**PMEENABLE:** Reserved.
7:4	0x0 RO	**Reserved2:** Reserved.
3	0x1 RO	**NO_SOFT_RESET:** Reserved.
2	0x0 RO	**Reserved3:** Reserved.
1:0	0x0 RW	**POWERSTATE:** Reserved.

12.4.15 reg_GEN_REGRW1_type (GEN_REGRW1)—Offset A0h

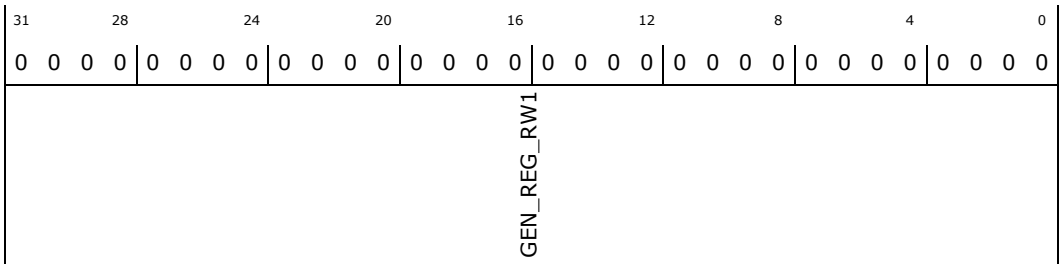
General Purpose Read Write Register1

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + A0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW1:** Reserved.

12.4.16 reg_GEN_REGRW2_type (GEN_REGRW2)—Offset A4h

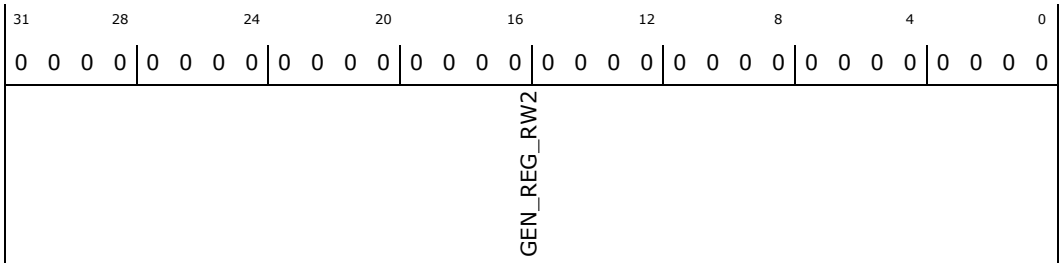
General Purpose Read Write Register2

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + A4h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW2:** Reserved.

12.4.17 reg_GEN_REGRW3_type (GEN_REGRW3)—Offset A8h

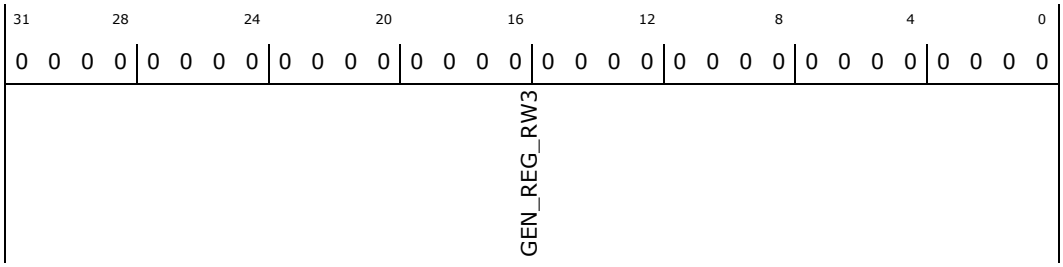
General Purpose Read Write Register3

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + A8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW3:** Reserved.

12.4.18 reg_GEN_REGRW4_type (GEN_REGRW4)—Offset ACh

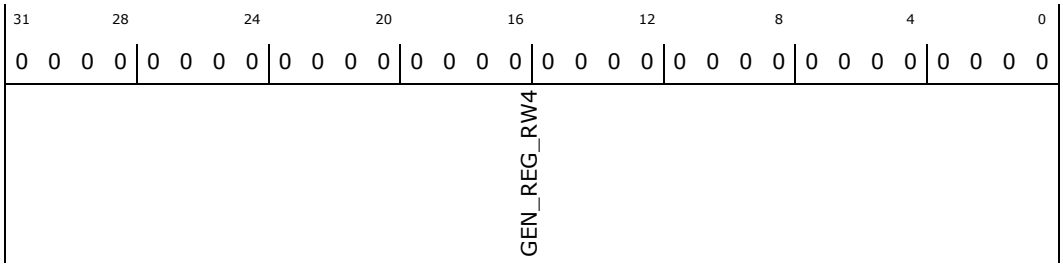
General Purpose Read Write Register4

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + ACh

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW4:** Reserved.

12.4.19 reg_GEN_INPUT_REG_type (GEN_INPUT_REG)—Offset C0h

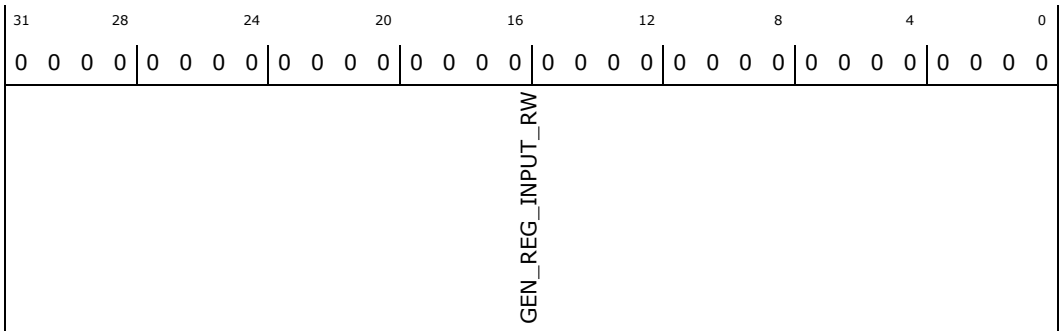
General Purpose Input Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + C0h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**GEN_REG_INPUT_RW:** Reserved.

12.4.20 reg_MANID_type (MANID)—Offset F8h

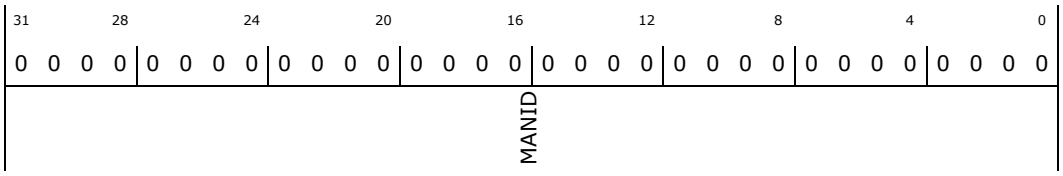
Manufacturers ID

Access Method

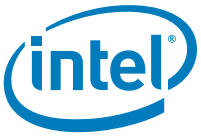
Type: PCI Configuration Register (Size: 32 bits)

Offset: [B:0, D:10, F:0] + F8h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Reserved.



12.5 IOSF2OCP PCI Message Registers

Table 124. Summary of IOSF2OCP PCI Message Bus Registers—0xB1

Offset	Register Name (Register Symbol)	Default Value
0–3h	"reg_DEVVENDID_type (DEVVENDID)—Offset 0h" on page 6557	22D88086h
4–7h	"reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h" on page 6557	00100000h
8–Bh	"reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h" on page 6558	00000006h
C–Fh	"reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch" on page 6559	00000000h
10–13h	"reg_BAR_type (BAR)—Offset 10h" on page 6560	00000000h
14–17h	"reg_BAR_HIGH_type (BAR_HIGH)—Offset 14h" on page 6560	00000000h
18–1Bh	"reg_BAR1_type (BAR1)—Offset 18h" on page 6561	00000000h
1C–1Fh	"reg_BAR1_HIGH_type (BAR1_HIGH)—Offset 1Ch" on page 6562	00000000h
2C–2Fh	"reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch" on page 6562	00000000h
30–33h	"reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h" on page 6563	00000000h
34–37h	"reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h" on page 6563	00000080h
3C–3Fh	"reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch" on page 6564	00000100h
80–83h	"reg_POWERCAPID_type (POWERCAPID)—Offset 80h" on page 6565	00030001h
84–87h	"reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h" on page 6565	00000008h
A0–A3h	"reg_GEN_REGRW1_type (GEN_REGRW1)—Offset A0h" on page 6566	00000000h
A4–A7h	"reg_GEN_REGRW2_type (GEN_REGRW2)—Offset A4h" on page 6567	00000000h
A8–ABh	"reg_GEN_REGRW3_type (GEN_REGRW3)—Offset A8h" on page 6567	00000000h
AC–AFh	"reg_GEN_REGRW4_type (GEN_REGRW4)—Offset ACh" on page 6568	00000000h
C0–C3h	"reg_GEN_INPUT_REG_type (GEN_INPUT_REG)—Offset C0h" on page 6568	00000000h
F8–FBh	"reg_MANID_type (MANID)—Offset F8h" on page 6569	00000000h

12.5.1 reg_DEVVENDID_type (DEVVENDID)—Offset 0h

DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

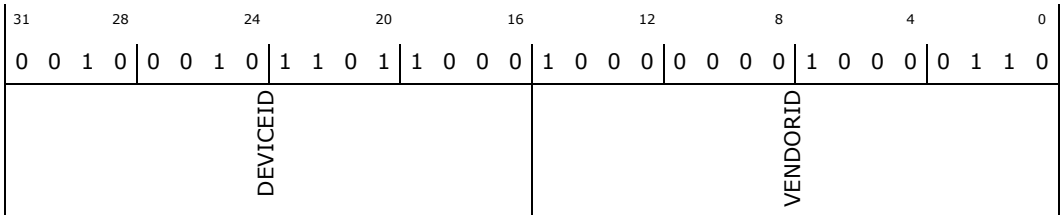
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 0h

Op Codes:

h - Read, h - Write

Default: 22D88086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x22d8 RO	**DEVICEID:** Reserved.
15:0	0x8086 RO	**VENDORID:** Reserved.

12.5.2 reg_STATUSCOMMAND_type (STATUSCOMMAND)—Offset 4h

STATUSCOMMAND- Status and Command

Access Method

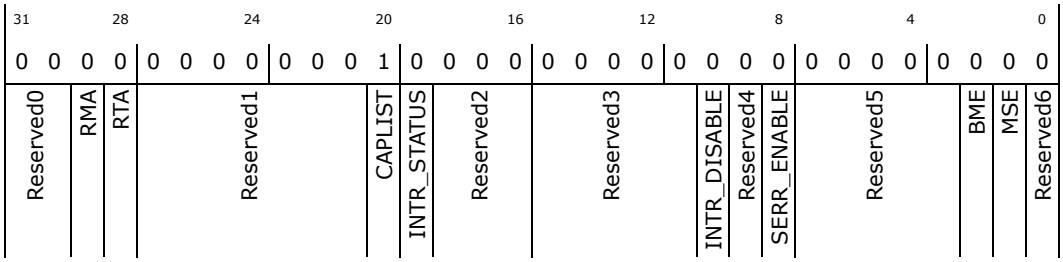
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 4h

Op Codes:

h - Read, h - Write

Default: 00100000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0x0 RO	**Reserved0:** Reserved.
29	0x0 RW/1C	**RMA:** Reserved.
28	0x0 RW/1C	**RTA:** Reserved.
27:21	0x0 RO	**Reserved1:** Reserved.
20	0x1 RO	**CAPLIST:** Reserved.
19	0x0 RO	**INTR_STATUS:** Reserved.
18:16	0x0 RO	**Reserved2:** Reserved.
15:11	0x0 RO	**Reserved3:** Reserved.
10	0x0 RW	**INTR_DISABLE:** Reserved.
9	0x0 RO	**Reserved4:** Reserved.
8	0x0 RW	**SERR_ENABLE:** Reserved.
7:3	0x0 RO	**Reserved5:** Reserved.
2	0x0 RW	**BME:** Reserved.
1	0x0 RW	**MSE:** Reserved.
0	0x0 RO	**Reserved6:** Reserved.

12.5.3 reg_REVCLASSCODE_type (REVCLASSCODE)—Offset 8h

REVCLASSCODE - Revision ID and Class Code

Access Method

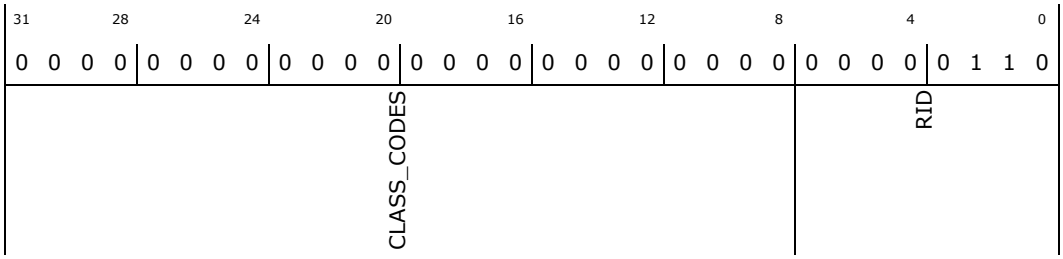
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 8h

Op Codes:

h - Read, h - Write

Default: 00000006h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**CLASS_CODES:** Reserved.
7:0	0x6 RO	**RID:** Reserved.

12.5.4 reg_CLLATHEADERBIST_type (CLLATHEADERBIST)—Offset Ch

CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

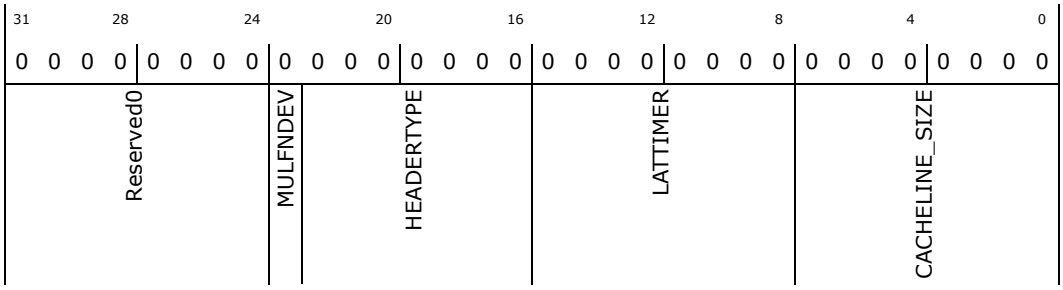
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**Reserved0:** Reserved.
23	0x0 RO	**MULFNDEV:** Reserved.
22:16	0x0 RO	**HEADERTYPE:** Reserved.
15:8	0x0 RO	**LATTIMER:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**CACHELINE_SIZE:** Reserved.

12.5.5 reg_BAR_type (BAR)—Offset 10h

BAR -Base Address Register

Access Method

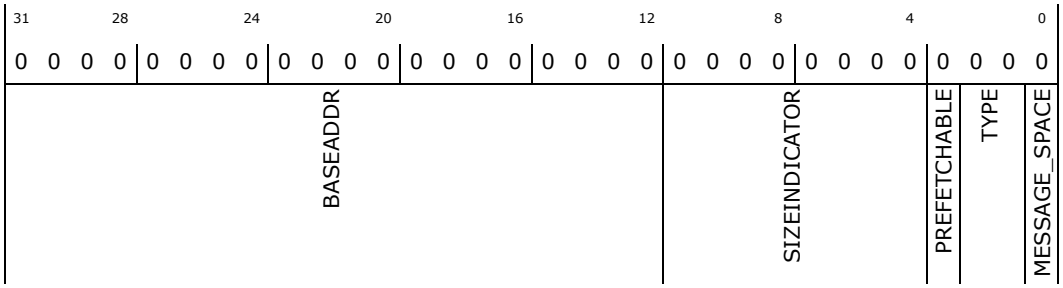
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW/V	**BASEADDR:** Reserved.
11:4	0x0 RO	**SIZEINDICATOR:** Reserved.
3	0x0 RO	**PREFETCHABLE:** Reserved.
2:1	0x0 RO	**TYPE:** Reserved.
0	0x0 RO	**MESSAGE_SPACE:** Reserved.

12.5.6 reg_BAR_HIGH_type (BAR_HIGH)—Offset 14h

BAR -Base Address Register High

Access Method

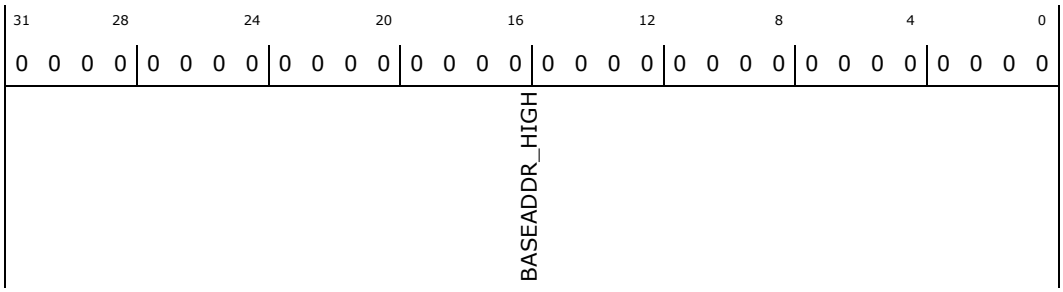
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 14h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**BASEADDR_HIGH:** Reserved.

12.5.7 reg_BAR1_type (BAR1)—Offset 18h

BAR1 -Base Address Register1

Access Method

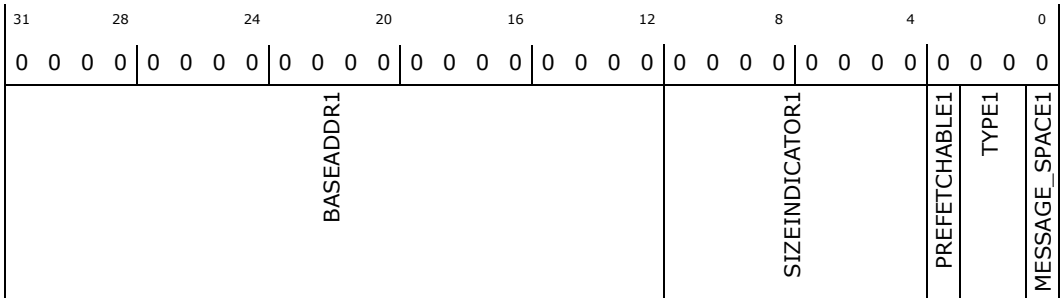
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 18h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RW	**BASEADDR1:** Reserved.
11:4	0x0 RO	**SIZEINDICATOR1:** Reserved.
3	0x0 RO	**PREFETCHABLE1:** Reserved.
2:1	0x0 RO	**TYPE1:** Reserved.
0	0x0 RO	**MESSAGE_SPACE1:** Reserved.

12.5.8 reg_BAR1_HIGH_type (BAR1_HIGH)—Offset 1Ch

BAR1 -Base Address Register1 High

Access Method

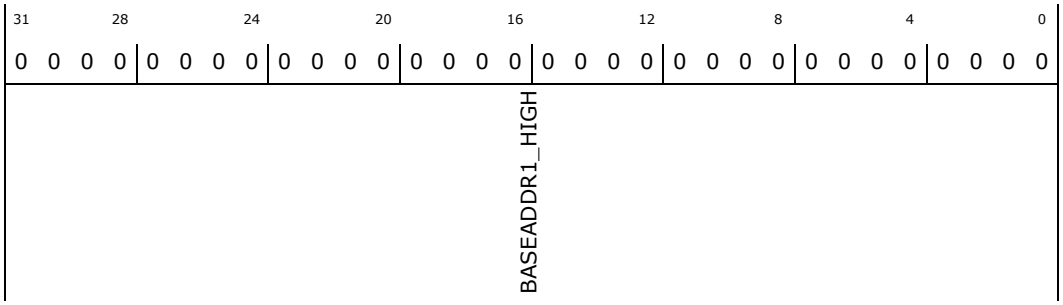
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**BASEADDR1_HIGH:** Reserved.

12.5.9 reg_SUBSYSTEMID_type (SUBSYSTEMID)—Offset 2Ch

SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

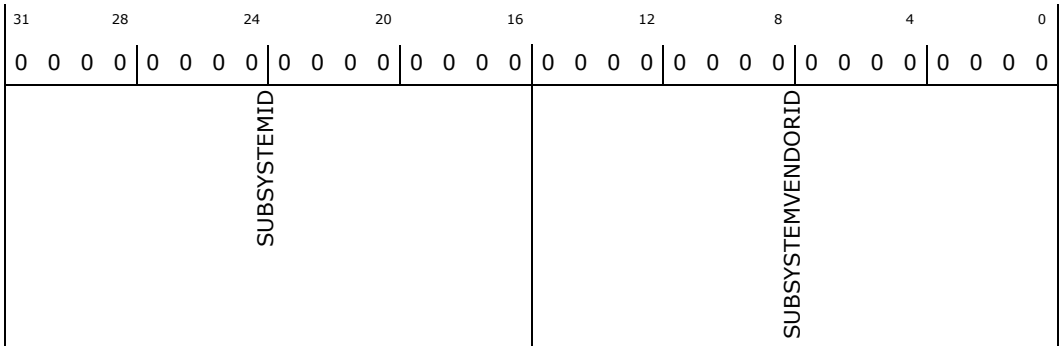
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 2Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RW/O	**SUBSYSTEMID:** Reserved.
15:0	0x0 RW/O	**SUBSYSTEMVENDORID:** Reserved.

12.5.10 reg_EXPANSION_ROM_BASEADDR_type (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address

Access Method

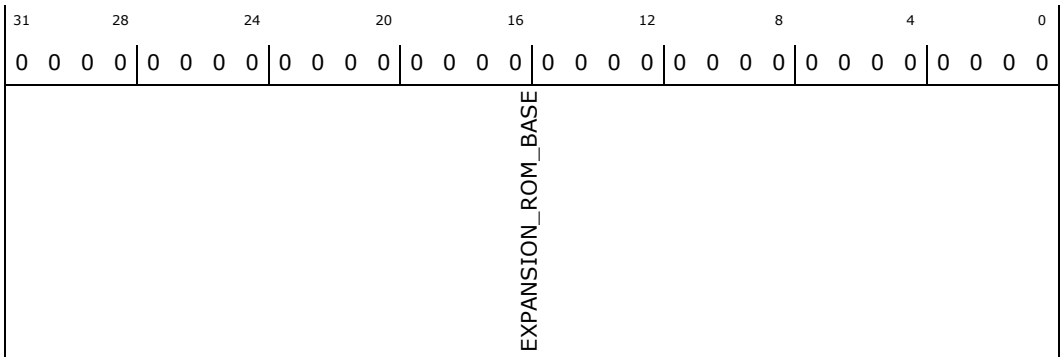
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 30h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**EXPANSION_ROM_BASE:** Reserved.

12.5.11 reg_CAPABILITYPTR_type (CAPABILITYPTR)—Offset 34h

CAPABILITYPTR - Capabilities Pointer

Access Method

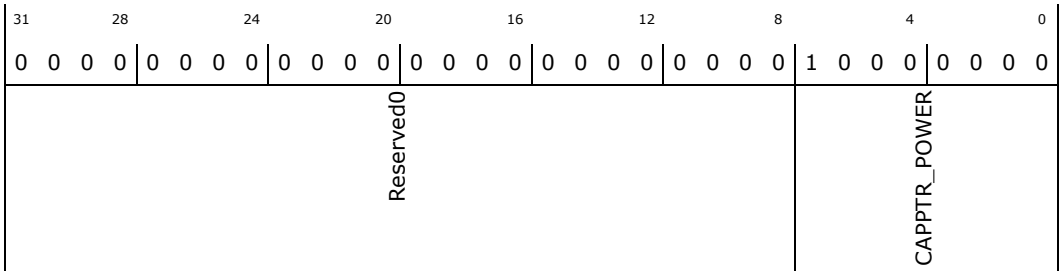
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 34h

Op Codes:

h - Read, h - Write

Default: 00000080h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved.
7:0	0x80 RO	**CAPPTR_POWER:** Reserved.

12.5.12 reg_INTERRUPTREG_type (INTERRUPTREG)—Offset 3Ch

INTERRUPTREG - Interrupt Register

Access Method

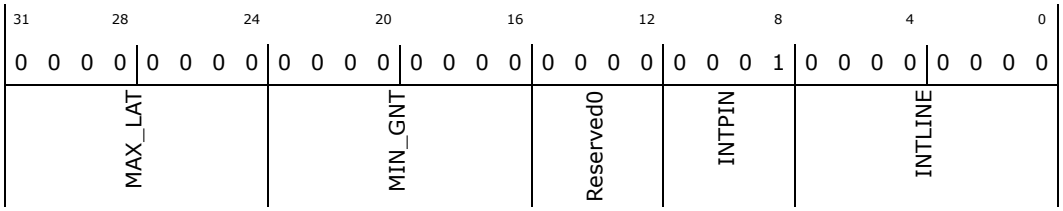
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 3Ch

Op Codes:

h - Read, h - Write

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RO	**MAX_LAT:** Reserved.
23:16	0x0 RO	**MIN_GNT:** Reserved.
15:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x1 RO	**INTPIN:** Reserved.
7:0	0x0 RW	**INTLINE:** Reserved.

12.5.13 reg_POWERCAPID_type (POWERCAPID)—Offset 80h

POWERCAPID - PowerManagement Capability ID

Access Method

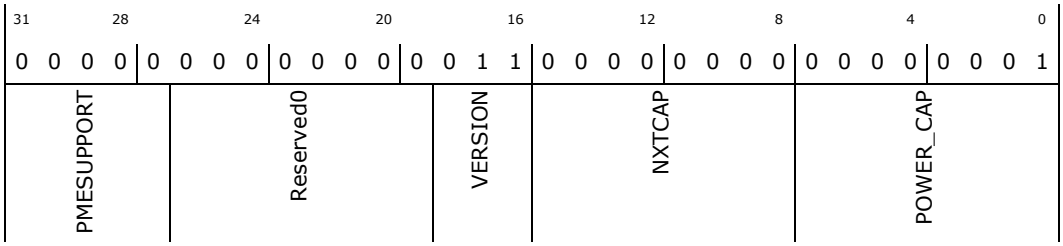
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 80h

Op Codes:

h - Read, h - Write

Default: 00030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0x0 RO	**PMESUPPORT:** Reserved.
26:19	0x0 RO	**Reserved0:** Reserved.
18:16	0x3 RO	**VERSION:** Reserved.
15:8	0x0 RO	**NXTCAP:** Reserved.
7:0	0x1 RO	**POWER_CAP:** Reserved.

12.5.14 reg_PMECTRLSTATUS_type (PMECTRLSTATUS)—Offset 84h

Access Method

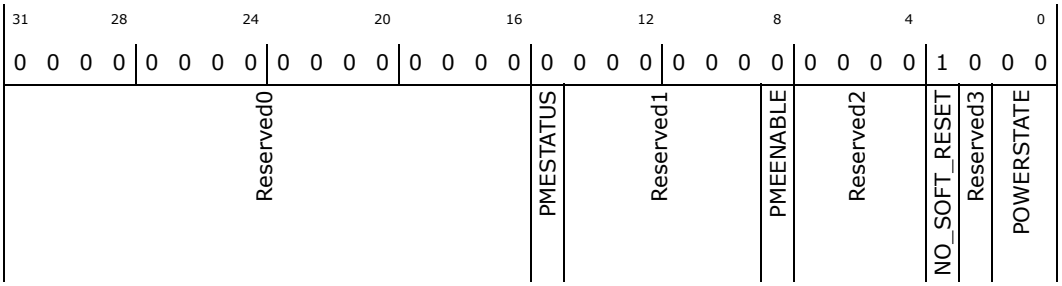
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 84h

Op Codes:

h - Read, h - Write

Default: 00000008h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0x0 RO	**Reserved0:** Reserved.
15	0x0 RW/1C	**PMESTATUS:** Reserved.
14:9	0x0 RO	**Reserved1:** Reserved.
8	0x0 RW	**PMEENABLE:** Reserved.
7:4	0x0 RO	**Reserved2:** Reserved.
3	0x1 RO	**NO_SOFT_RESET:** Reserved.
2	0x0 RO	**Reserved3:** Reserved.
1:0	0x0 RW	**POWERSTATE:** Reserved.

12.5.15 reg_GEN_REGRW1_type (GEN_REGRW1)—Offset A0h

General Purpose Read Write Register1

Access Method

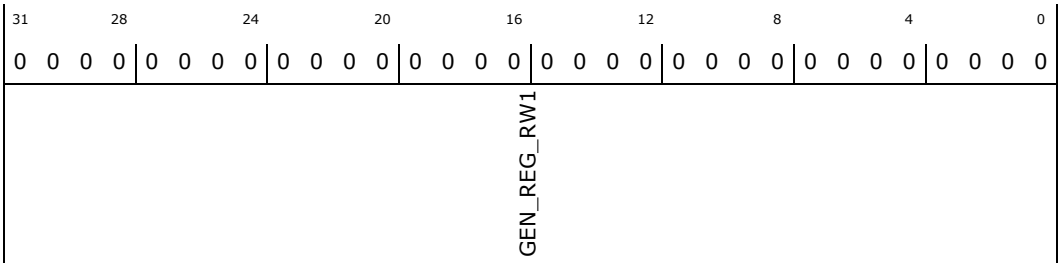
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + A0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW1:** Reserved.

12.5.16 reg_GEN_REGRW2_type (GEN_REGRW2)—Offset A4h

General Purpose Read Write Register2

Access Method

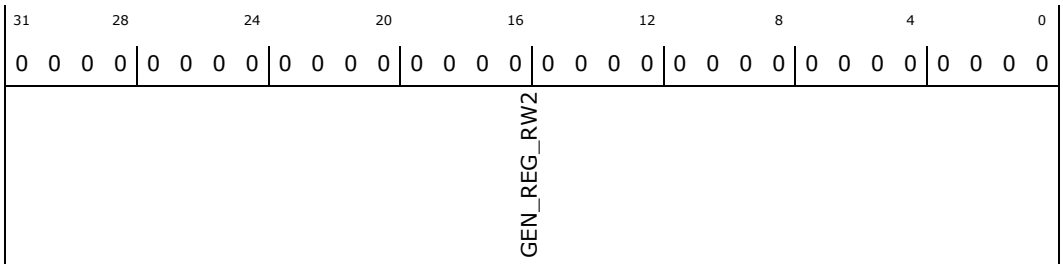
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + A4h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW2:** Reserved.

12.5.17 reg_GEN_REGRW3_type (GEN_REGRW3)—Offset A8h

General Purpose Read Write Register3

Access Method

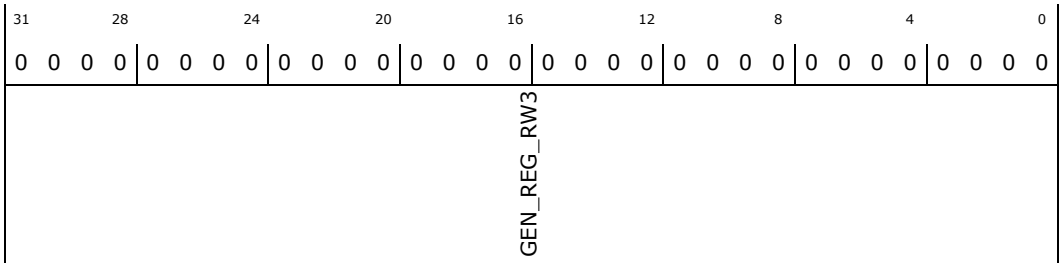
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + A8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW3:** Reserved.

12.5.18 reg_GEN_REGRW4_type (GEN_REGRW4)—Offset ACh

General Purpose Read Write Register4

Access Method

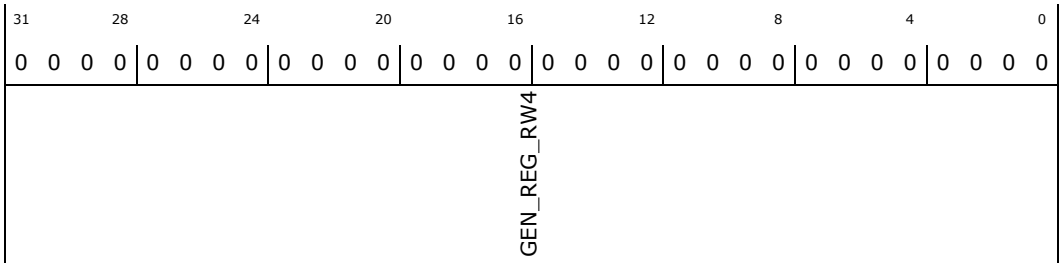
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + ACh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW4:** Reserved.

12.5.19 reg_GEN_INPUT_REG_type (GEN_INPUT_REG)—Offset C0h

General Purpose Input Register

Access Method

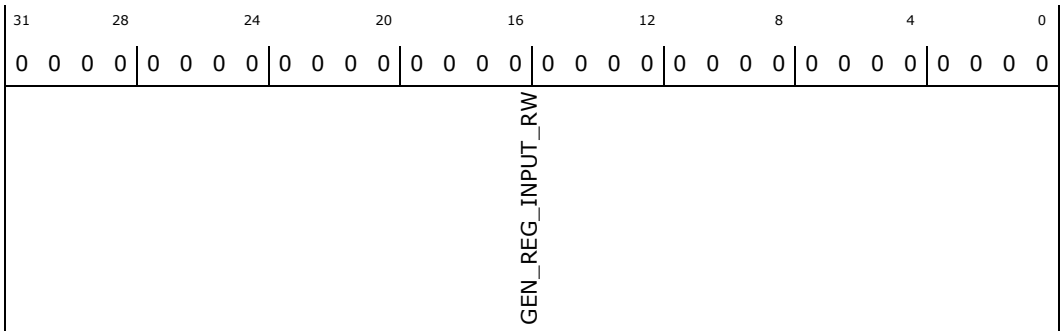
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + C0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**GEN_REG_INPUT_RW:** Reserved.

12.5.20 reg_MANID_type (MANID)—Offset F8h

Manufacturers ID

Access Method

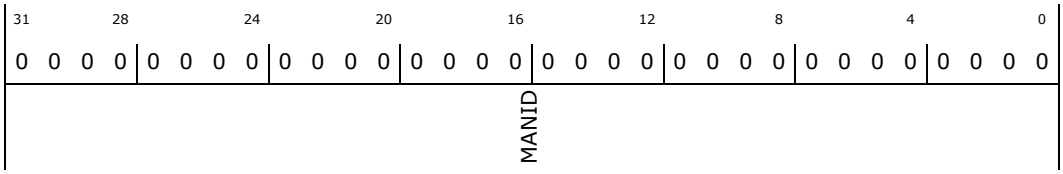
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + F8h

Op Codes:

h - Read, h - Write

Default: 00000000h

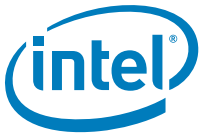


Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**MANID:** Reserved.

12.6 IOSF2OCP Private Address Map

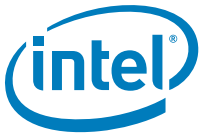
Table 125. Summary of IOSF2OCP Private Registers—0xB1

Offset	Register Name (Register Symbol)	Default Value
0–3h	"reg_IOSFCTL_type (IOSFCTL)—Offset 0h" on page 6574	0000000Fh
8–Bh	"reg_IOSFSTS_type (IOSFSTS)—Offset 8h" on page 6574	00000000h
10–13h	"reg_OCPCTL_type (OCPCTL)—Offset 10h" on page 6575	000000F1h
20–23h	"reg_FLSH_type (FLSH)—Offset 20h" on page 6575	00000000h
30–33h	"reg_RID_type (RID)—Offset 30h" on page 6576	00000000h
34–37h	"reg_CAPID_type (CAPID)—Offset 34h" on page 6576	00000000h
50–53h	"reg_SPARE_type (SPARE)—Offset 50h" on page 6577	00000000h
60–63h	"reg_IOSFSBA_type (IOSFSBA)—Offset 60h" on page 6577	00000000h
68–6Bh	"reg_UPARBGNTCNTVC0_type (UPARBGNTCNTVC0)—Offset 68h" on page 6578	00000001h
6C–6Fh	"reg_UPARBGNTCNTVC1_type (UPARBGNTCNTVC1)—Offset 6Ch" on page 6578	00000000h
70–73h	"reg_UPARBGNTCNTVC2_type (UPARBGNTCNTVC2)—Offset 70h" on page 6579	00000000h
74–77h	"reg_DNARBGNTCNT_T0_type (DNARBGNTCNT_T0)—Offset 74h" on page 6579	00000001h
78–7Bh	"reg_DNARBGNTCNT_T1_type (DNARBGNTCNT_T1)—Offset 78h" on page 6580	00000000h
7C–7Fh	"reg_DNARBGNTCNT_T2_type (DNARBGNTCNT_T2)—Offset 7Ch" on page 6581	00000000h
C8–CBh	"reg_IOREGSELBASE_type (IOREGSELBASE)—Offset C8h" on page 6581	00000000h
CC–CFh	"reg_IOREGSELLIMIT_type (IOREGSELLIMIT)—Offset CCh" on page 6582	00000000h
100–103h	"reg_PWBASE0_type (PWBASE0)—Offset 100h" on page 6582	00000000h
104–107h	"reg_PWLIMIT0_type (PWLIMIT0)—Offset 104h" on page 6583	00000000h
108–10Bh	"reg_PWBASE1_type (PWBASE1)—Offset 108h" on page 6583	00000000h
10C–10Fh	"reg_PWLIMIT1_type (PWLIMIT1)—Offset 10Ch" on page 6584	00000000h
110–113h	"reg_PWBASE2_type (PWBASE2)—Offset 110h" on page 6584	00000000h
114–117h	"reg_PWLIMIT2_type (PWLIMIT2)—Offset 114h" on page 6585	00000000h
118–11Bh	"reg_PWBASE3_type (PWBASE3)—Offset 118h" on page 6585	00000000h
11C–11Fh	"reg_PWLIMIT3_type (PWLIMIT3)—Offset 11Ch" on page 6586	00000000h
150–153h	"reg_MMIOSCUASSISTREG0_type (MMIOSCUASSISTREG0)—Offset 150h" on page 6586	00000000h
154–157h	"reg_MMIOSCUASSISTREG1_type (MMIOSCUASSISTREG1)—Offset 154h" on page 6587	00000000h
158–15Bh	"reg_MMIOSCUASSISTREG2_type (MMIOSCUASSISTREG2)—Offset 158h" on page 6588	00000000h



Offset	Register Name (Register Symbol)	Default Value
15C–15Fh	"reg_MMIOSCUASSISTREG3_type (MMIOSCUASSISTREG3)—Offset 15Ch" on page 6588	00000000h
1E0–1E3h	"reg_PMCTL_type (PMCTL)—Offset 1E0h" on page 6589	00000000h
200–203h	"reg_DEBUGCTL_type (DEBUGCTL)—Offset 200h" on page 6590	00000000h
280–283h	"reg_DEBUGSTS_type (DEBUGSTS)—Offset 280h" on page 6591	00000000h
400–403h	"reg_IOCFGCTL_type (IOCFGCTL)—Offset 400h" on page 6591	00000000h
408–40Bh	"reg_UPBRIDGEDATA_type (UPBRIDGEDATA)—Offset 408h" on page 6592	00000000h
410–413h	"reg_UPBRIDGECMD_type (UPBRIDGECMD)—Offset 410h" on page 6592	00000000h
414–417h	"reg_ILBCTL_type (ILBCTL)—Offset 414h" on page 6593	00000000h
420–423h	"reg_SMICMD_type (SMICMD)—Offset 420h" on page 6593	00000000h
424–427h	"reg_SMIADDR_type (SMIADDR)—Offset 424h" on page 6594	00000000h
428–42Bh	"reg_SMIDATA_type (SMIDATA)—Offset 428h" on page 6594	00000000h
42C–42Fh	"reg_SMISTS_type (SMISTS)—Offset 42Ch" on page 6595	00000002h
430–433h	"reg_IOSCUASSISTREG0_type (IOSCUASSISTREG0)—Offset 430h" on page 6595	FFFF0000h
434–437h	"reg_IOSCUASSISTREG1_type (IOSCUASSISTREG1)—Offset 434h" on page 6596	FFFF0000h
438–43Bh	"reg_IOSCUASSISTREG2_type (IOSCUASSISTREG2)—Offset 438h" on page 6597	FFFF0000h
43C–43Fh	"reg_IOSCUASSISTREG3_type (IOSCUASSISTREG3)—Offset 43Ch" on page 6597	FFFF0000h
440–443h	"reg_IOSCUASSISTREG4_type (IOSCUASSISTREG4)—Offset 440h" on page 6598	FFFF0000h
444–447h	"reg_IOSCUASSISTREG5_type (IOSCUASSISTREG5)—Offset 444h" on page 6599	FFFF0000h
448–44Bh	"reg_IOSCUASSISTREG6_type (IOSCUASSISTREG6)—Offset 448h" on page 6599	FFFF0000h
44C–44Fh	"reg_IOSCUASSISTREG7_type (IOSCUASSISTREG7)—Offset 44Ch" on page 6600	FFFF0000h
500–503h	"reg_PCICFGCTR1_type (PCICFGCTR1)—Offset 500h" on page 6600	00000100h
504–507h	"reg_PCICFGCTR2_type (PCICFGCTR2)—Offset 504h" on page 6601	00000000h

Offset	Register Name (Register Symbol)	Default Value
508–50Bh	"reg_PCICFGCTR3_type (PCICFGCTR3)—Offset 508h" on page 6602	00000000h
50C–50Fh	"reg_PCICFGCTR4_type (PCICFGCTR4)—Offset 50Ch" on page 6603	00000000h
510–513h	"reg_PCICFGCTR5_type (PCICFGCTR5)—Offset 510h" on page 6603	00000000h
514–517h	"reg_PCICFGCTR6_type (PCICFGCTR6)—Offset 514h" on page 6604	00000000h
518–51Bh	"reg_PCICFGCTR7_type (PCICFGCTR7)—Offset 518h" on page 6605	00000000h
51C–51Fh	"reg_PCICFGCTR8_type (PCICFGCTR8)—Offset 51Ch" on page 6606	00000000h
520–523h	"reg_CHCTRL_type (CHCTRL)—Offset 520h" on page 6606	00000000h
600–603h	"reg_GEN_REGRW1_type (GEN_REGRW1)—Offset 600h" on page 6607	00000000h
604–607h	"reg_GEN_REGRW2_type (GEN_REGRW2)—Offset 604h" on page 6607	00000000h
608–60Bh	"reg_GEN_REGRW3_type (GEN_REGRW3)—Offset 608h" on page 6608	00000000h
60C–60Fh	"reg_GEN_REGRW4_type (GEN_REGRW4)—Offset 60Ch" on page 6608	00000000h
610–613h	"reg_GEN_REGRW5_type (GEN_REGRW5)—Offset 610h" on page 6609	00000000h
614–617h	"reg_GEN_REGRW6_type (GEN_REGRW6)—Offset 614h" on page 6609	00000000h
618–61Bh	"reg_GEN_REGRW7_type (GEN_REGRW7)—Offset 618h" on page 6610	00000000h
61C–61Fh	"reg_GEN_REGRW8_type (GEN_REGRW8)—Offset 61Ch" on page 6610	00000000h
620–623h	"reg_GEN_REGRWO1_type (GEN_REGRWO1)—Offset 620h" on page 6611	00000000h
624–627h	"reg_GEN_REGRWO2_type (GEN_REGRWO2)—Offset 624h" on page 6611	00000000h
628–62Bh	"reg_GEN_REGRWO3_type (GEN_REGRWO3)—Offset 628h" on page 6612	00000000h
62C–62Fh	"reg_GEN_REGRWO4_type (GEN_REGRWO4)—Offset 62Ch" on page 6612	00000000h
630–633h	"reg_GEN_REGRWO5_type (GEN_REGRWO5)—Offset 630h" on page 6613	00000000h
634–637h	"reg_GEN_REGRWO6_type (GEN_REGRWO6)—Offset 634h" on page 6613	00000000h
638–63Bh	"reg_GEN_REGRWO7_type (GEN_REGRWO7)—Offset 638h" on page 6614	00000000h



Offset	Register Name (Register Symbol)	Default Value
63C–63Fh	"reg_GEN_REGRWO8_type (GEN_REGRWO8)—Offset 63Ch" on page 6614	00000000h
650–653h	"reg_FUSE1_type (FUSE1)—Offset 650h" on page 6615	00000000h
654–657h	"reg_FUSE2_type (FUSE2)—Offset 654h" on page 6615	00000000h
658–65Bh	"reg_FUSE3_type (FUSE3)—Offset 658h" on page 6616	00000000h
660–663h	"reg_STRAP1_type (STRAP1)—Offset 660h" on page 6616	00000000h
664–667h	"reg_STRAP2_type (STRAP2)—Offset 664h" on page 6617	00000000h
668–66Bh	"reg_STRAP3_type (STRAP3)—Offset 668h" on page 6617	00000000h
670–673h	"reg_FUSE_STRAP_CPL_STATUS_type (FUSE_STRAP_CPL_STATUS)—Offset 670h" on page 6618	00000000h

12.6.1 reg_IOSFCTL_type (IOSFCTL)—Offset 0h

Access Method

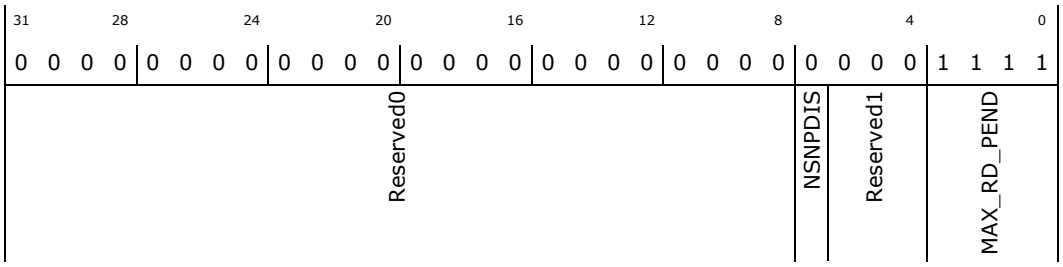
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 0h

Op Codes:

h - Read, h - Write

Default: 0000000Fh



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved.
7	0x0 RW	**NSNPDIS:** Reserved.
6:4	0x0 RO	**Reserved1:** Reserved.
3:0	0xf RW	**MAX_RD_PEND:** Reserved.

12.6.2 reg_IOSFSTS_type (IOSFSTS)—Offset 8h

Access Method

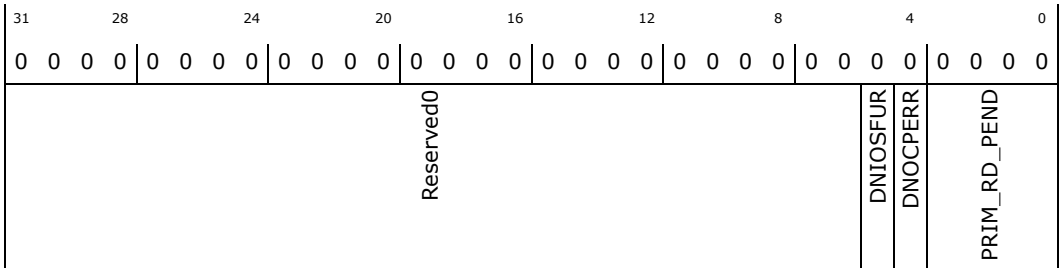
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**Reserved0:** Reserved.
5	0x0 RW/1C	**DNIOSFUR:** Reserved.
4	0x0 RW/1C	**DNOCPERR:** Reserved.
3:0	0x0 RO	**PRIM_RD_PEND:** Reserved.

12.6.3 reg_OCPCTL_type (OCPCTL)—Offset 10h

Access Method

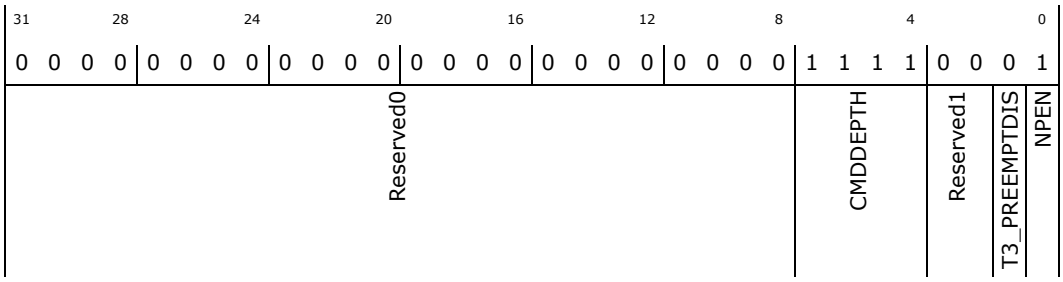
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10h

Op Codes:

h - Read, h - Write

Default: 000000F1h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved.
7:4	0xf RW	**CMDDEPTH:** Reserved.
3:2	0x0 RO	**Reserved1:** Reserved.
1	0x0 RW	**T3_PREEMPTDIS:** Reserved.
0	0x1 RW	**NPEN:** Reserved.

12.6.4 reg_FLSH_type (FLSH)—Offset 20h

Access Method

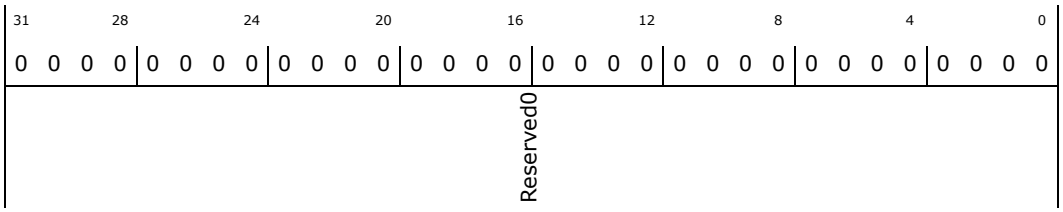
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 20h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved0:** Reserved.

12.6.5 reg_RID_type (RID)—Offset 30h

Access Method

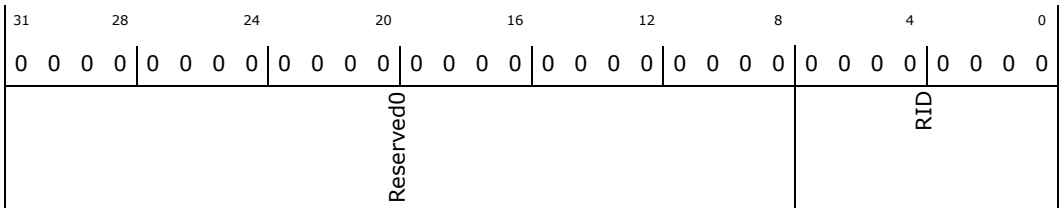
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 30h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved.
7:0	0x0 RO	**RID:** Reserved.

12.6.6 reg_CAPID_type (CAPID)—Offset 34h

Access Method

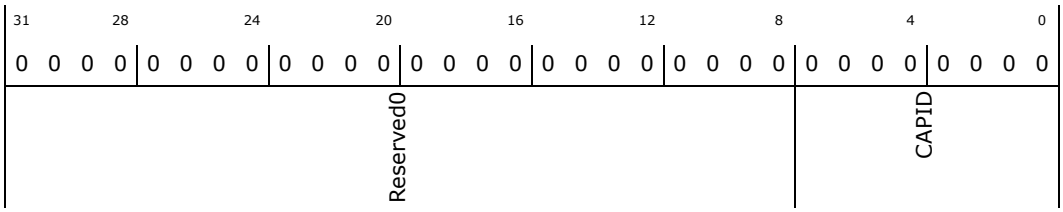
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 34h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved.
7:0	0x0 RO	**CAPID:** Reserved.

12.6.7 reg_SPARE_type (SPARE)—Offset 50h

Access Method

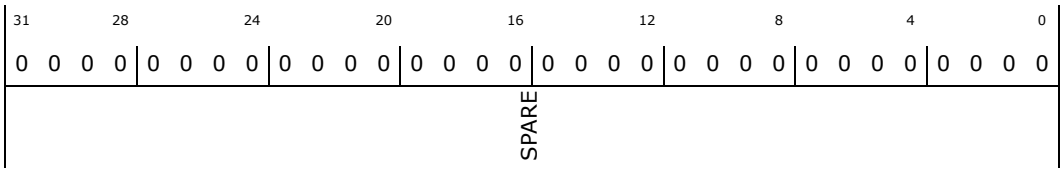
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 50h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**SPARE:** Reserved.

12.6.8 reg_IOSFSBA_type (IOSFSBA)—Offset 60h

Access Method

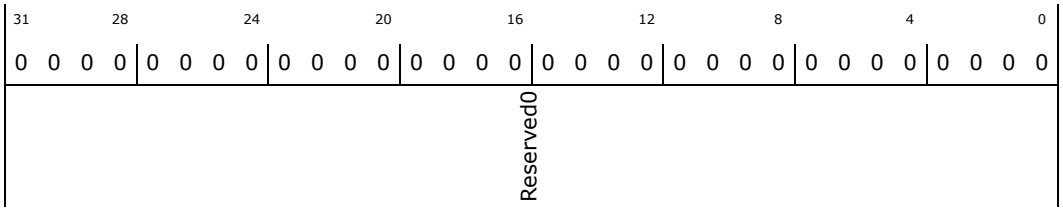
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 60h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved0:** Reserved.

12.6.9 reg_UPARBGNTCNTVC0_type (UPARBGNTCNTVC0)—Offset 68h

Access Method

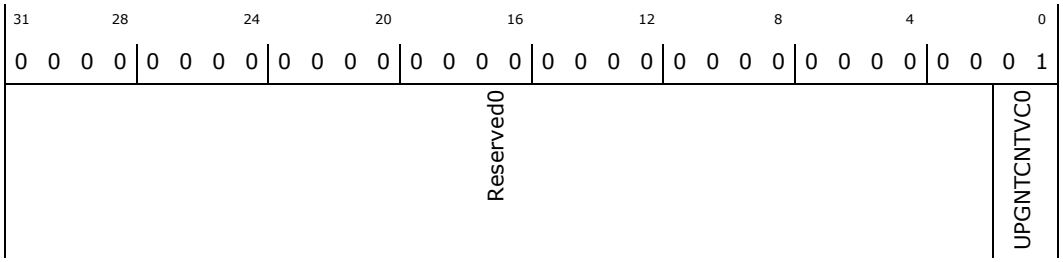
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 68h

Op Codes:

h - Read, h - Write

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved0:** Reserved.
1:0	0x1 RW	**UPGNTCNTVC0:** Reserved.

12.6.10 reg_UPARBGNTCNTVC1_type (UPARBGNTCNTVC1)—Offset 6Ch

Access Method

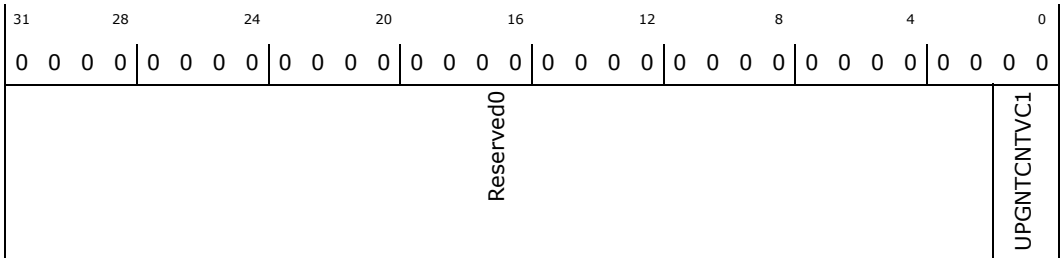
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 6Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved0:** Reserved.
1:0	0x0 RW	**UPGNTCNTVC1:** Reserved.

12.6.11 reg_UPARBGNTCNTVC2_type (UPARBGNTCNTVC2)—Offset 70h

Access Method

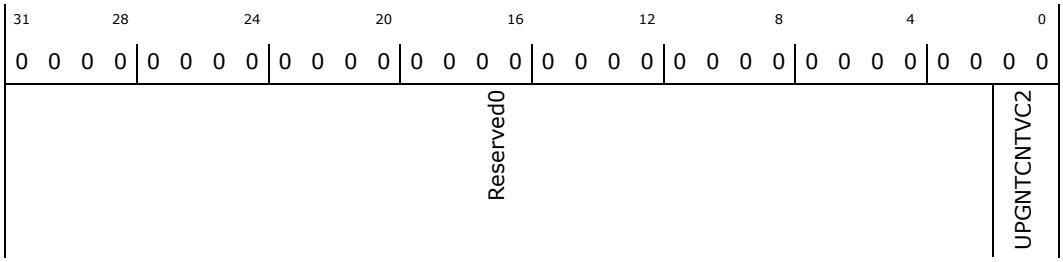
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 70h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved0:** Reserved.
1:0	0x0 RW	**UPGNTCNTVC2:** Reserved.

12.6.12 reg_DNARBGNTCNT_T0_type (DNARBGNTCNT_T0)—Offset 74h

Access Method

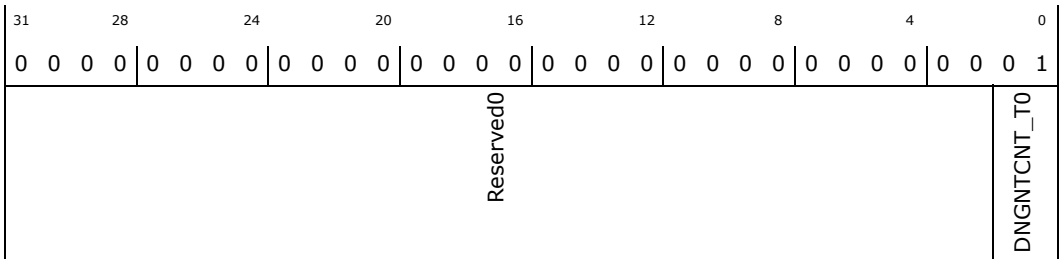
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 74h

Op Codes:

h - Read, h - Write

Default: 00000001h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved0:** Reserved.
1:0	0x1 RW	**DNGNTCNT_T0:** Reserved.

12.6.13 reg_DNARBGNTCNT_T1_type (DNARBGNTCNT_T1)—Offset 78h

Access Method

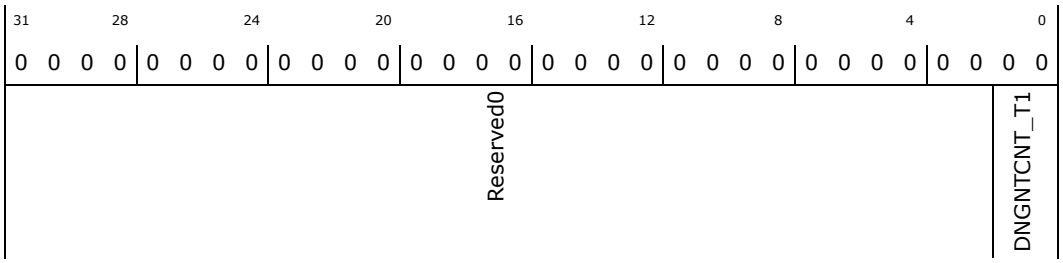
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 78h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved0:** Reserved.
1:0	0x0 RW	**DNGNTCNT_T1:** Reserved.

12.6.14 reg_DNARBGNTCNT_T2_type (DNARBGNTCNT_T2)—Offset 7Ch

Access Method

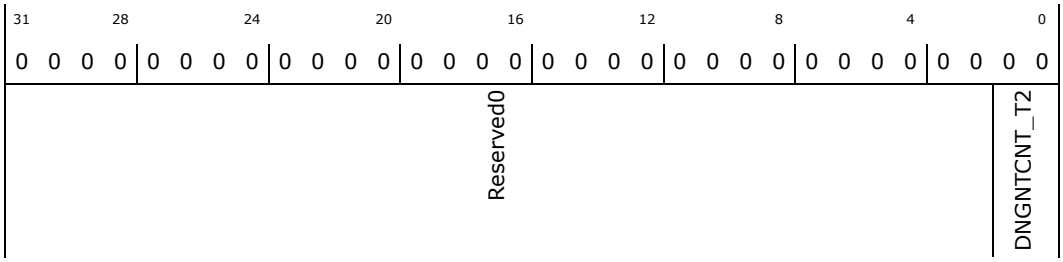
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 7Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved0:** Reserved.
1:0	0x0 RW	**DNGNTCNT_T2:** Reserved.

12.6.15 reg_IOREGSELBASE_type (IOREGSELBASE)—Offset C8h

Access Method

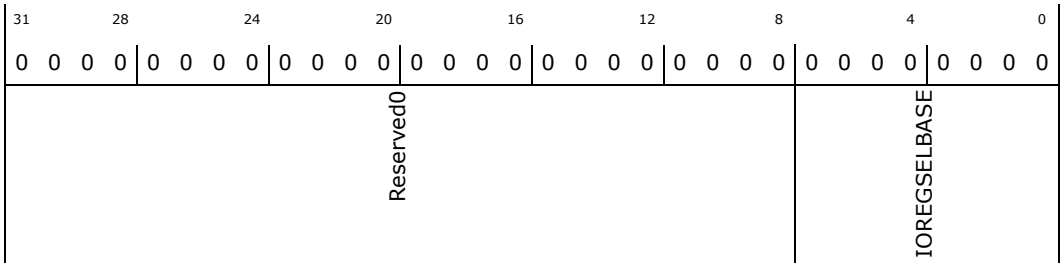
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + C8h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0x0 RO	**Reserved0:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7:0	0x0 RW	**IOREGSELBASE:** Reserved.

12.6.16 reg_IOREGSELLIMIT_type (IOREGSELLIMIT)—Offset CCh

Access Method

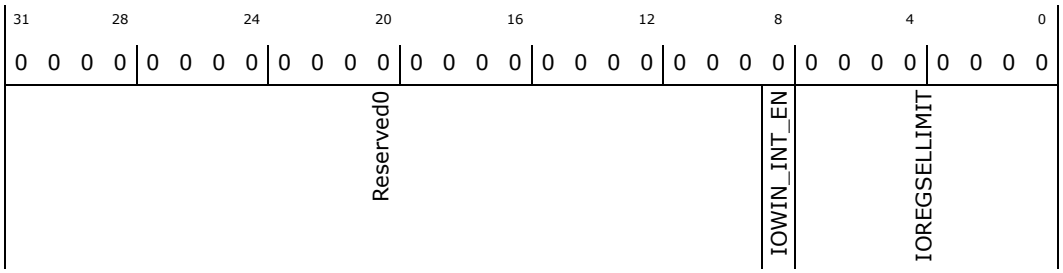
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + CCh

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0x0 RO	**Reserved0:** Reserved.
8	0x0 RW	**IOWIN_INT_EN:** Reserved.
7:0	0x0 RW	**IOREGSELLIMIT:** Reserved.

12.6.17 reg_PWBASE0_type (PWBASE0)—Offset 100h

Access Method

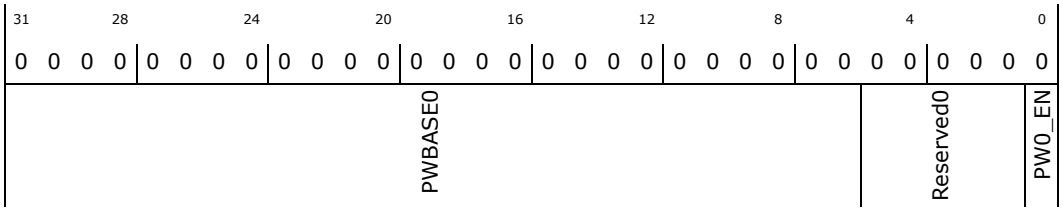
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 100h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**PWBASE0:** Reserved.
5:1	0x0 RO	**Reserved0:** Reserved.
0	0x0 RW	**PW0_EN:** Reserved.

12.6.18 reg_PWLIMIT0_type (PWLIMIT0)—Offset 104h

Access Method

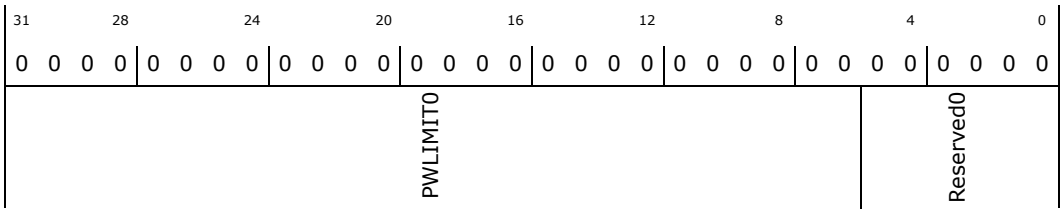
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 104h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**PWLIMIT0:** Reserved.
5:0	0x0 RO	**Reserved0:** Reserved.

12.6.19 reg_PWBASE1_type (PWBASE1)—Offset 108h

Access Method

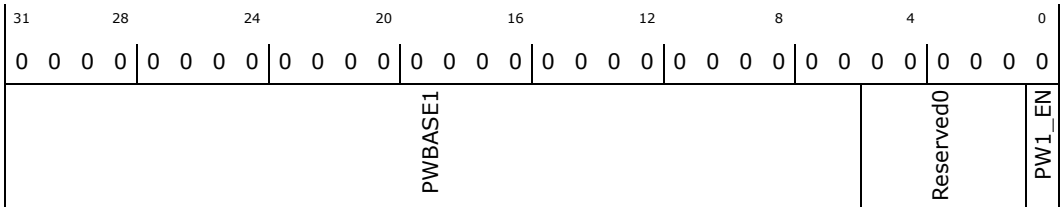
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 108h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**PWBASE1:** Reserved.
5:1	0x0 RO	**Reserved0:** Reserved.
0	0x0 RW	**PW1_EN:** Reserved.

12.6.20 reg_PWLIMIT1_type (PWLIMIT1)—Offset 10Ch

Access Method

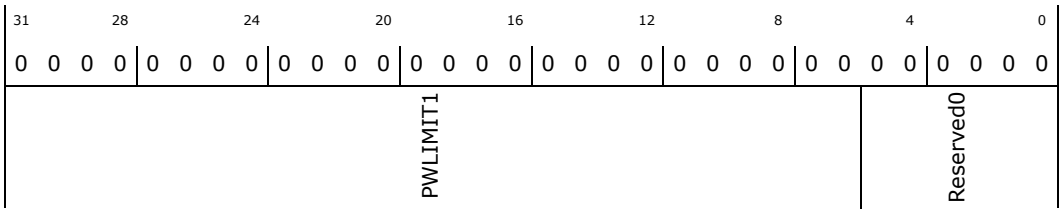
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 10Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**PWLIMIT1:** Reserved.
5:0	0x0 RO	**Reserved0:** Reserved.

12.6.21 reg_PWBASE2_type (PWBASE2)—Offset 110h

Access Method

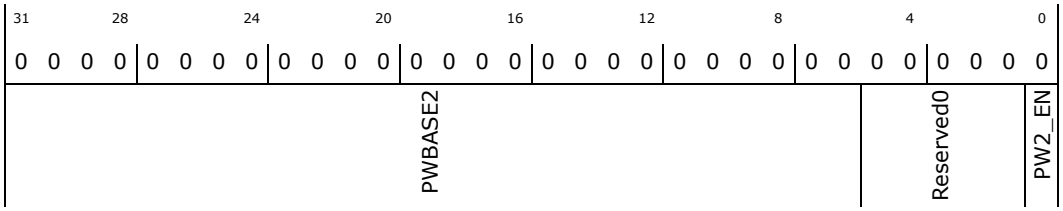
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 110h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**PWBASE2:** Reserved.
5:1	0x0 RO	**Reserved0:** Reserved.
0	0x0 RW	**PW2_EN:** Reserved.

12.6.22 reg_PWLIMIT2_type (PWLIMIT2)—Offset 114h

Access Method

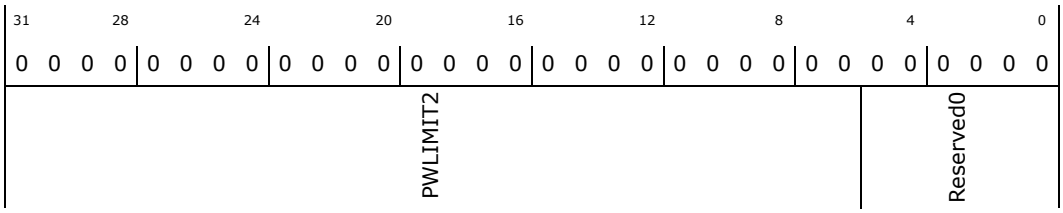
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 114h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**PWLIMIT2:** Reserved.
5:0	0x0 RO	**Reserved0:** Reserved.

12.6.23 reg_PWBASE3_type (PWBASE3)—Offset 118h

Access Method

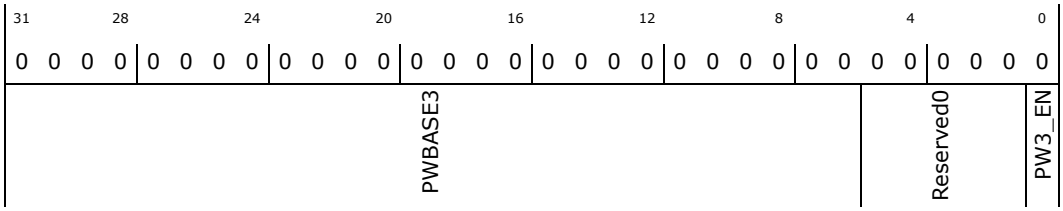
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 118h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**PWBASE3:** Reserved.
5:1	0x0 RO	**Reserved0:** Reserved.
0	0x0 RW	**PW3_EN:** Reserved.

12.6.24 reg_PWLIMIT3_type (PWLIMIT3)—Offset 11Ch

Access Method

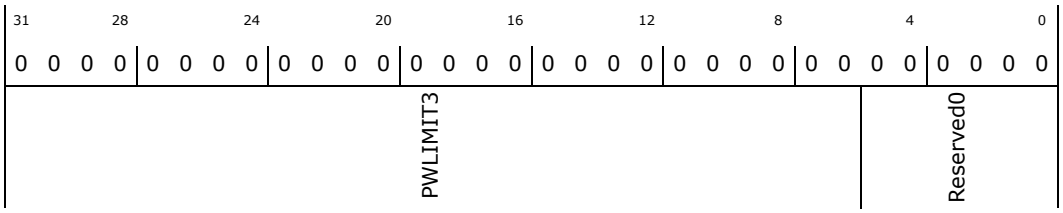
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 11Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RW	**PWLIMIT3:** Reserved.
5:0	0x0 RO	**Reserved0:** Reserved.

12.6.25 reg_MMIOSCUASSISTREG0_type (MMIOSCUASSISTREG0)—Offset 150h

Access Method

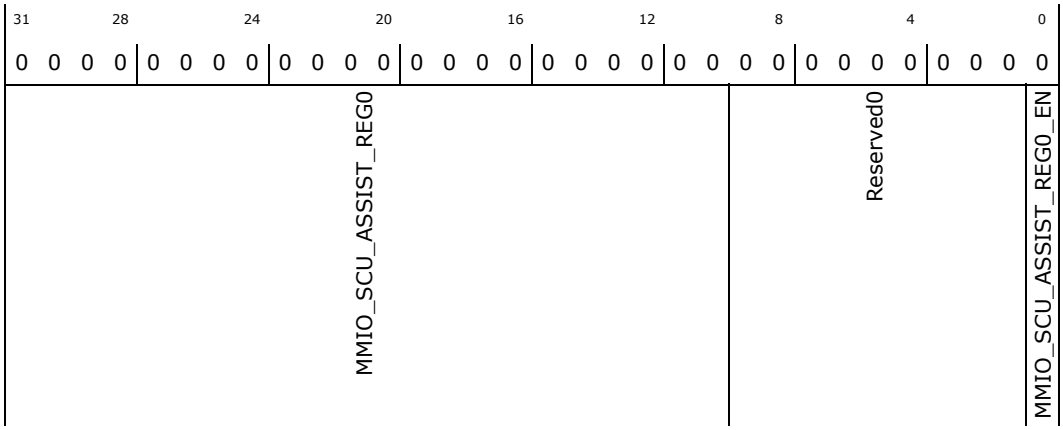
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 150h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**MMIO_SCU_ASSIST_REG0:** Reserved.
9:1	0x0 RO	**Reserved0:** Reserved.
0	0x0 RW	**MMIO_SCU_ASSIST_REG0_EN:** Reserved.

12.6.26 reg_MMIOSCUASSISTREG1_type (MMIOSCUASSISTREG1)—Offset 154h

Access Method

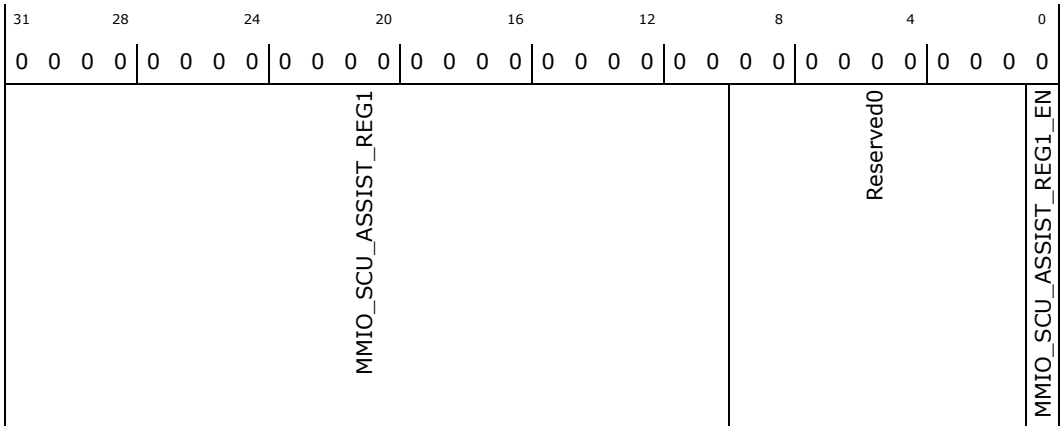
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 154h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**MMIO_SCU_ASSIST_REG1:** Reserved.
9:1	0x0 RO	**Reserved0:** Reserved.
0	0x0 RW	**MMIO_SCU_ASSIST_REG1_EN:** Reserved.

12.6.27 reg_MMIOSCUASSISTREG2_type (MMIOSCUASSISTREG2)—Offset 158h

Access Method

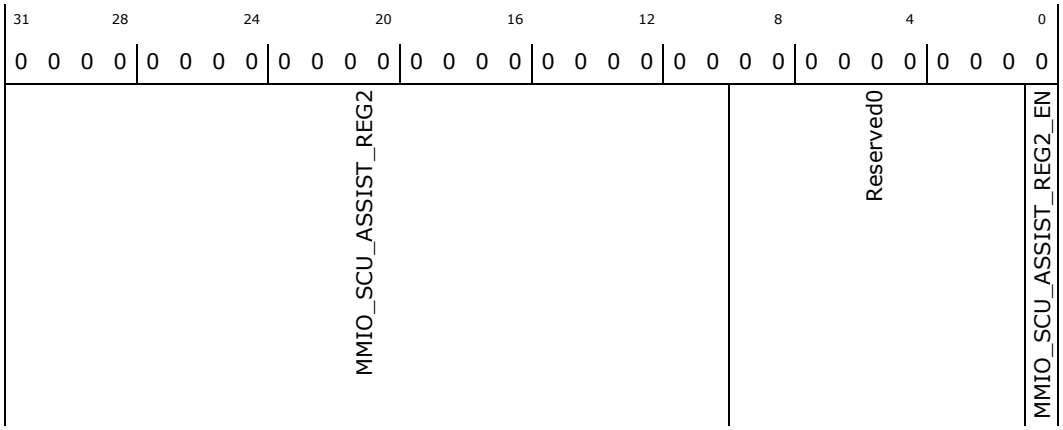
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 158h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**MMIO_SCU_ASSIST_REG2:** Reserved.
9:1	0x0 RO	**Reserved0:** Reserved.
0	0x0 RW	**MMIO_SCU_ASSIST_REG2_EN:** Reserved.

12.6.28 reg_MMIOSCUASSISTREG3_type (MMIOSCUASSISTREG3)—Offset 15Ch

Access Method

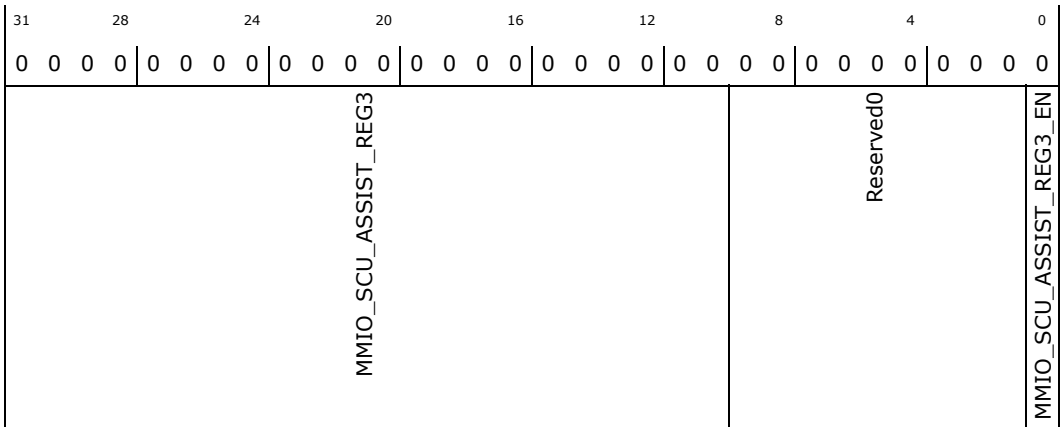
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 15Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0x0 RW	**MMIO_SCU_ASSIST_REG3:** Reserved.
9:1	0x0 RO	**Reserved0:** Reserved.
0	0x0 RW	**MMIO_SCU_ASSIST_REG3_EN:** Reserved.

12.6.29 reg_PMCTL_type (PMCTL)—Offset 1E0h

Access Method

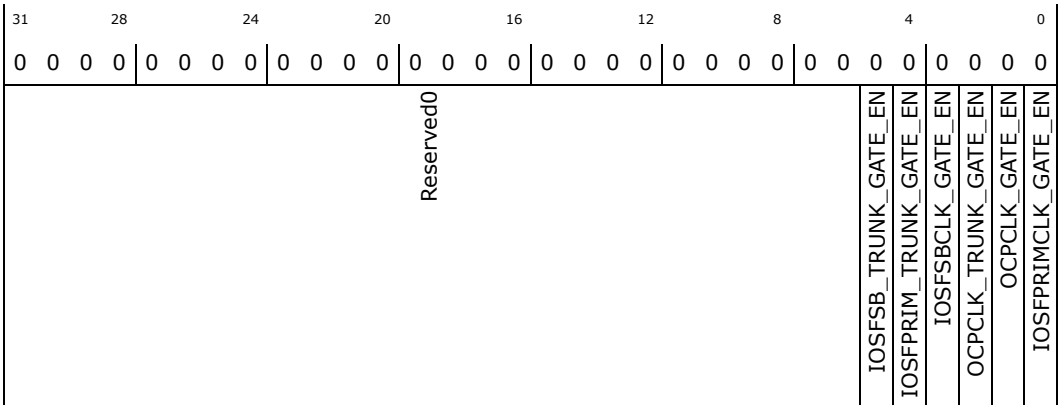
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 1E0h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0x0 RO	**Reserved0:** Reserved.
5	0x0 RW	**IOSFSB_TRUNK_GATE_EN:** Reserved.
4	0x0 RW	**IOSFPRIM_TRUNK_GATE_EN:** Reserved.
3	0x0 RW	**IOSFSBCLK_GATE_EN:** Reserved.
2	0x0 RW	**OCPCLK_TRUNK_GATE_EN:** Reserved.
1	0x0 RW	**OCPCLK_GATE_EN:** Reserved.
0	0x0 RW	**IOSFPRIMCLK_GATE_EN:** Reserved.

12.6.30 reg_DEBUGCTL_type (DEBUGCTL)—Offset 200h

Access Method

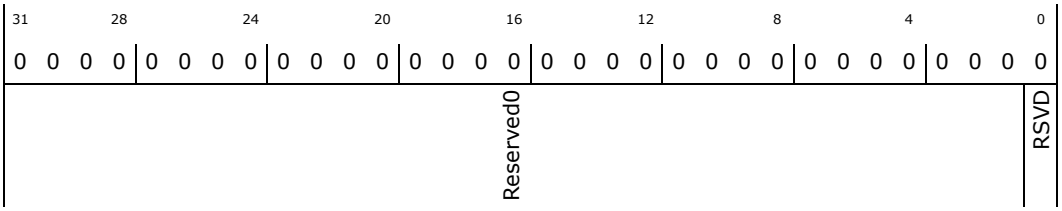
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 200h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0x0 RO	**Reserved0:** Reserved.
0	0x0 RO	**Reserved (RSVD):** Reserved.

12.6.31 reg_DEBUGSTS_type (DEBUGSTS)—Offset 280h

Access Method

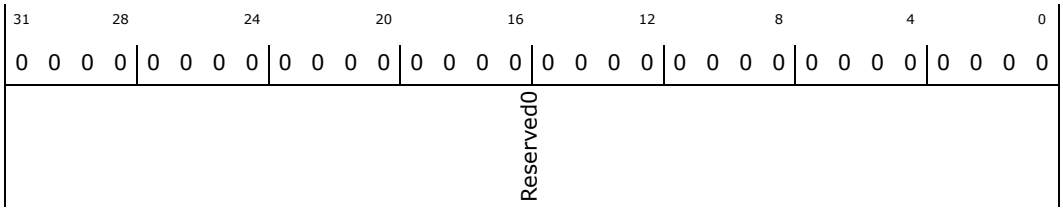
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 280h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved0:** Reserved.

12.6.32 reg_IOCFGCTL_type (IOCFGCTL)—Offset 400h

Access Method

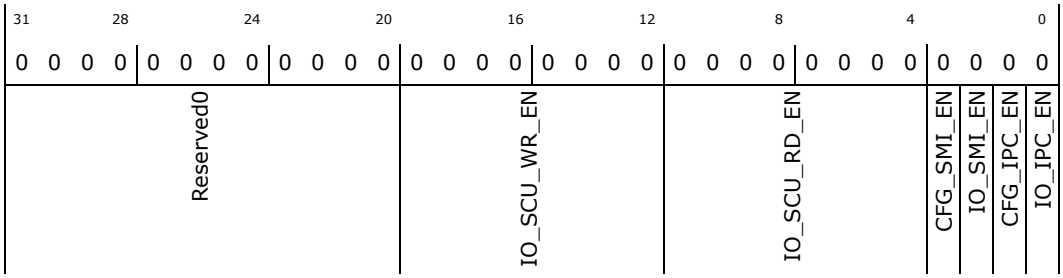
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 400h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0x0 RO	**Reserved0:** Reserved.
19:12	0x0 RW	**IO_SCU_WR_EN:** Reserved.
11:4	0x0 RW	**IO_SCU_RD_EN:** Reserved.
3	0x0 RW	**CFG_SMI_EN:** Reserved.
2	0x0 RW	**IO_SMI_EN:** Reserved.
1	0x0 RW	**CFG_IPC_EN:** Reserved.
0	0x0 RW	**IO_IPC_EN:** Reserved.

12.6.33 reg_UPBRIDGEDATA_type (UPBRIDGEDATA)—Offset 408h

Access Method

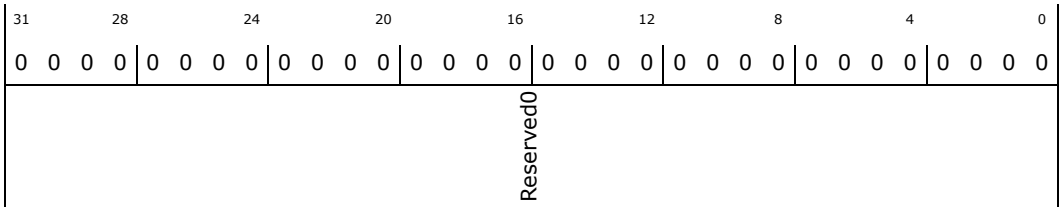
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 408h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Reserved0:** Reserved.

12.6.34 reg_UPBRIDGECMD_type (UPBRIDGECMD)—Offset 410h

Access Method

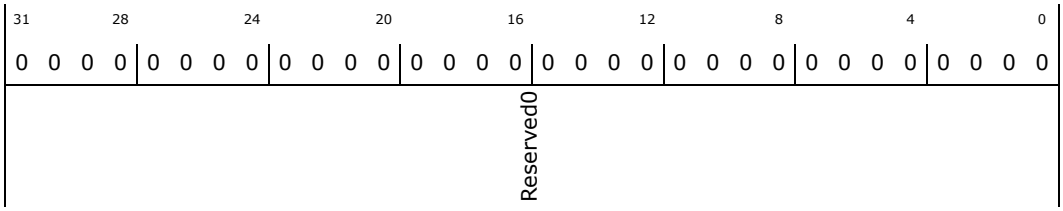
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 410h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 WO	**Reserved0:** Reserved.

12.6.35 reg_ILBCTL_type (ILBCTL)—Offset 414h

Access Method

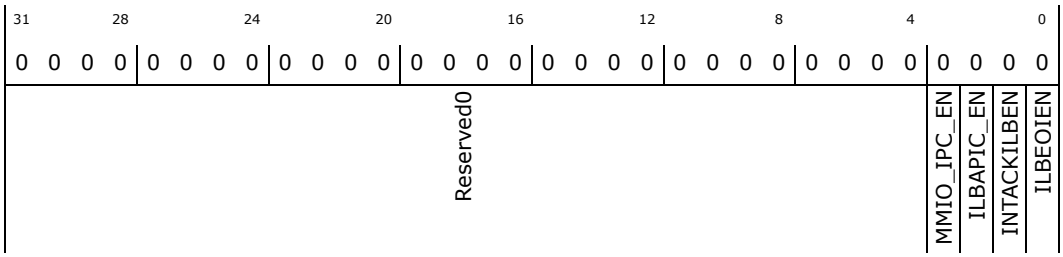
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 414h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0x0 RO	**Reserved0:** Reserved.
3	0x0 RW	**MMIO_IPC_EN:** Reserved.
2	0x0 RW	**ILBAPIC_EN:** Reserved.
1	0x0 RW	**INTACKILBEN:** Reserved.
0	0x0 RW	**ILBEOIEN:** Reserved.

12.6.36 reg_SMICMD_type (SMICMD)—Offset 420h

Access Method

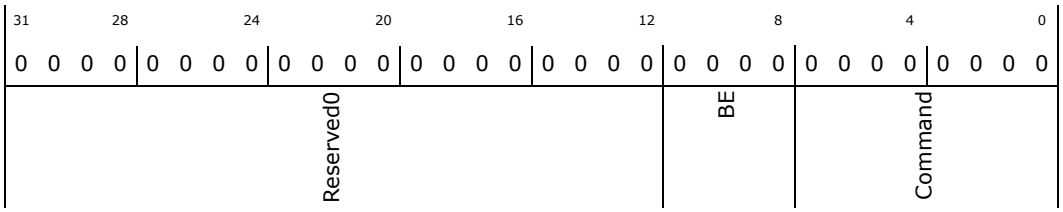
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 420h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x0 RO	**BE:** Reserved.
7:0	0x0 RO	**Command:** Reserved.

12.6.37 reg_SMIADDR_type (SMIADDR)—Offset 424h

Access Method

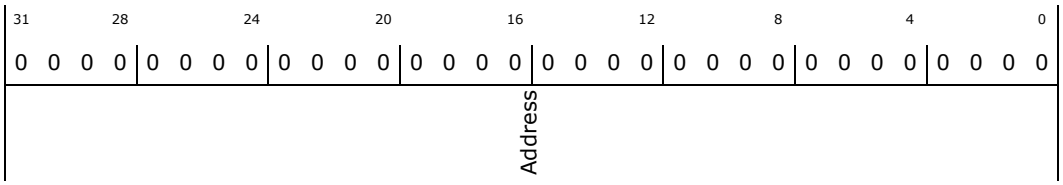
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 424h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Address:** Reserved.

12.6.38 reg_SMIDATA_type (SMIDATA)—Offset 428h

Access Method

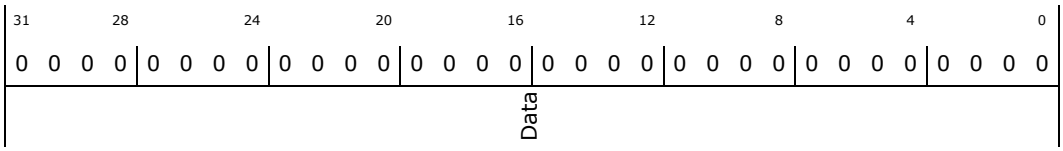
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 428h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RO	**Data:** Reserved.

12.6.39 reg_SMISTS_type (SMISTS)—Offset 42Ch

Access Method

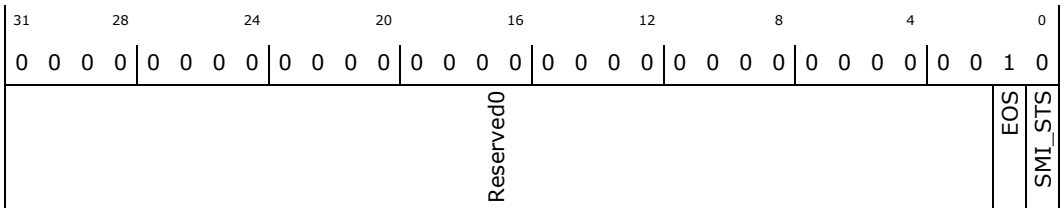
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 42Ch

Op Codes:

h - Read, h - Write

Default: 00000002h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved0:** Reserved.
1	0x1 RW/S	**EOS:** Reserved.
0	0x0 RW/1C	**SMI_STS:** Reserved.

12.6.40 reg_IOSCUASSISTREG0_type (IOSCUASSISTREG0)—Offset 430h

Access Method

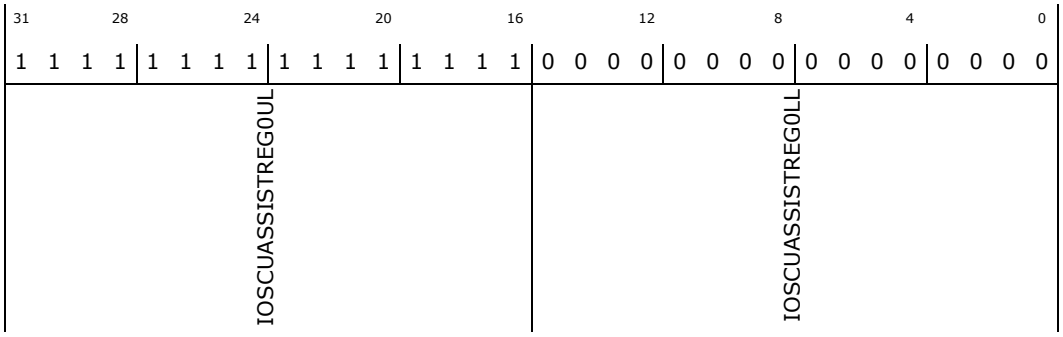
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 430h

Op Codes:

h - Read, h - Write

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RW	**IOSCUASSISTREG0UL:** Reserved.
15:0	0x0 RW	**IOSCUASSISTREG0LL:** Reserved.

12.6.41 reg_IOSCUASSISTREG1_type (IOSCUASSISTREG1)—Offset 434h

Access Method

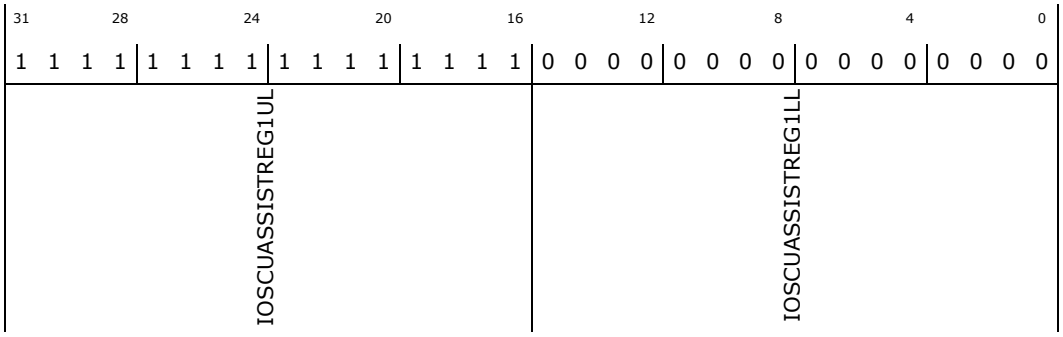
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 434h

Op Codes:

h - Read, h - Write

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RW	**IOSCUASSISTREG1UL:** Reserved.
15:0	0x0 RW	**IOSCUASSISTREG1LL:** Reserved.

12.6.42 reg_IOSCUASSISTREG2_type (IOSCUASSISTREG2)—Offset 438h

Access Method

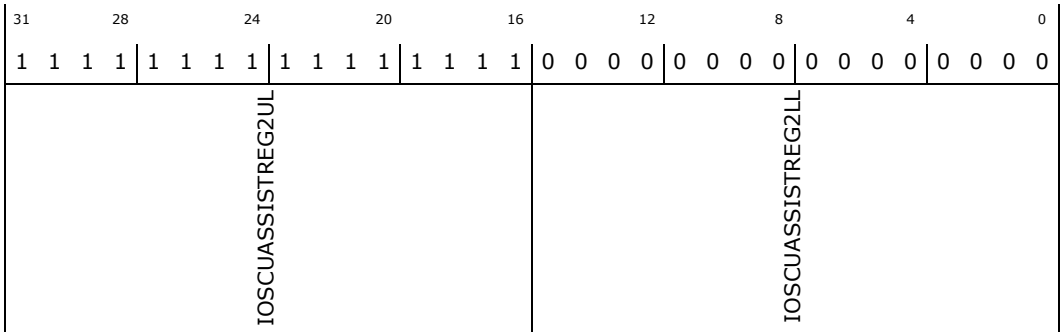
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 438h

Op Codes:

h - Read, h - Write

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RW	**IOSCUASSISTREG2UL:** Reserved.
15:0	0x0 RW	**IOSCUASSISTREG2LL:** Reserved.

12.6.43 reg_IOSCUASSISTREG3_type (IOSCUASSISTREG3)—Offset 43Ch

Access Method

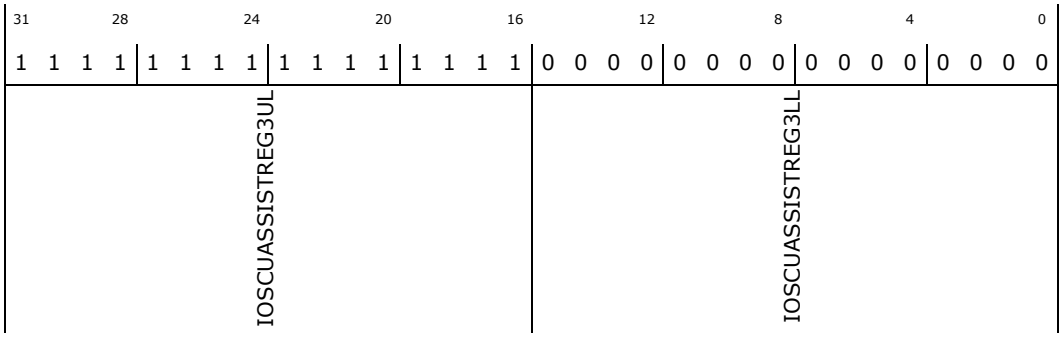
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 43Ch

Op Codes:

h - Read, h - Write

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RW	**IOSCUASSISTREG3UL:** Reserved.
15:0	0x0 RW	**IOSCUASSISTREG3LL:** Reserved.

12.6.44 reg_IOSCUASSISTREG4_type (IOSCUASSISTREG4)—Offset 440h

Access Method

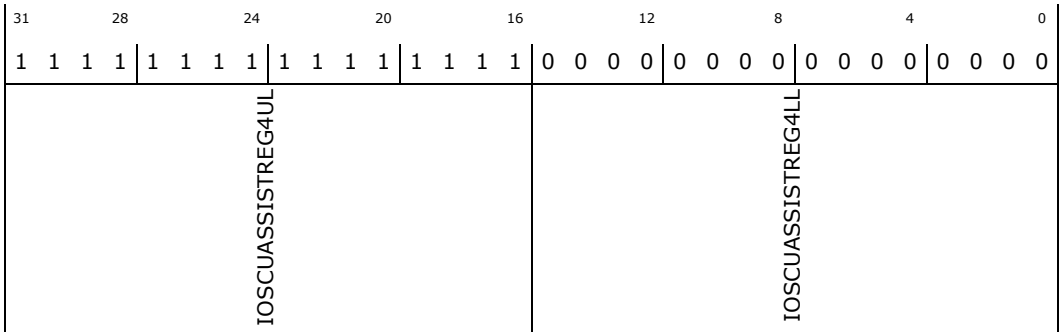
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 440h

Op Codes:

h - Read, h - Write

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RW	**IOSCUASSISTREG4UL:** Reserved.
15:0	0x0 RW	**IOSCUASSISTREG4LL:** Reserved.

12.6.45 reg_IOSCUASSISTREG5_type (IOSCUASSISTREG5)—Offset 444h

Access Method

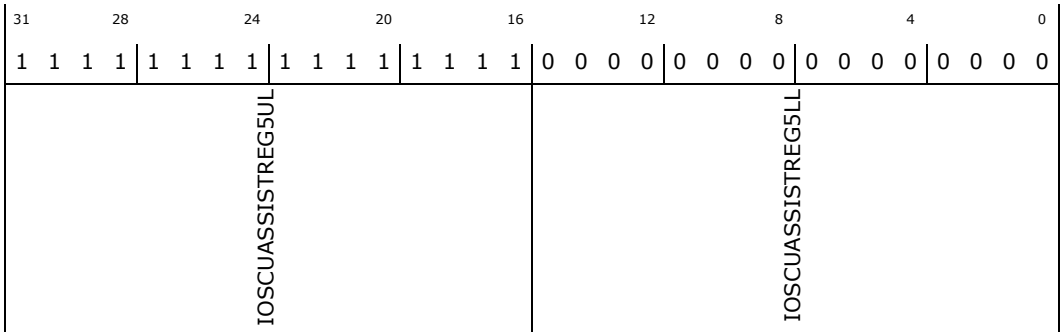
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 444h

Op Codes:

h - Read, h - Write

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RW	**IOSCUASSISTREG5UL:** Reserved.
15:0	0x0 RW	**IOSCUASSISTREG5LL:** Reserved.

12.6.46 reg_IOSCUASSISTREG6_type (IOSCUASSISTREG6)—Offset 448h

Access Method

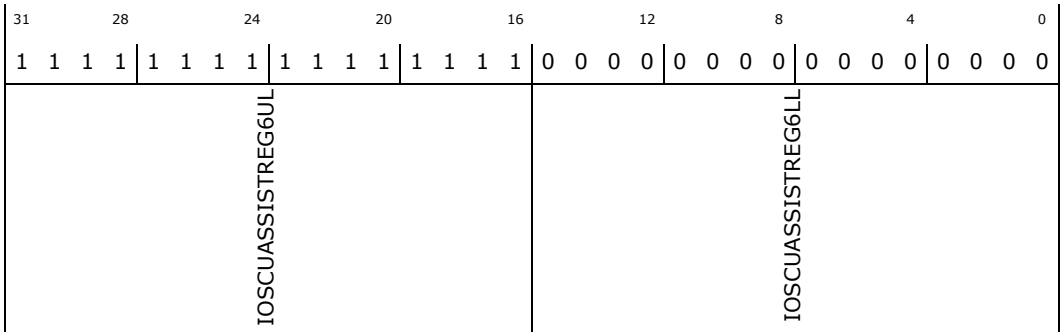
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 448h

Op Codes:

h - Read, h - Write

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RW	**IOSCUASSISTREG6UL:** Reserved.
15:0	0x0 RW	**IOSCUASSISTREG6LL:** Reserved.

12.6.47 reg_IOSCUASSISTREG7_type (IOSCUASSISTREG7)—Offset 44Ch

Access Method

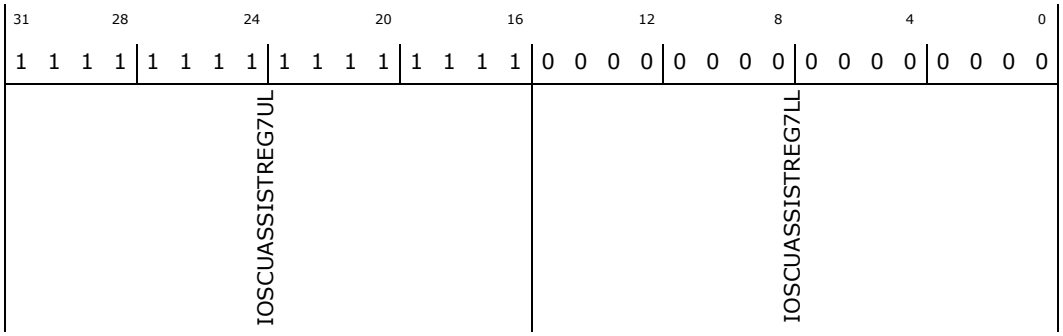
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 44Ch

Op Codes:

h - Read, h - Write

Default: FFFF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0xffff RW	**IOSCUASSISTREG7UL:** Reserved.
15:0	0x0 RW	**IOSCUASSISTREG7LL:** Reserved.

12.6.48 reg_PCICFGCTR1_type (PCICFGCTR1)—Offset 500h

Access Method

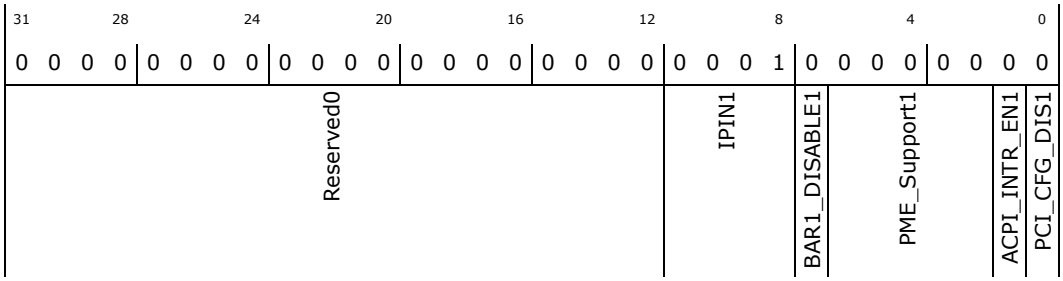
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 500h

Op Codes:

h - Read, h - Write

Default: 00000100h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x1 RW	**IPIN1:** Reserved.
7	0x0 RW	**BAR1_DISABLE1:** Reserved.
6:2	0x0 RW	**PME_Support1:** Reserved.
1	0x0 RW	**ACPI_INTR_EN1:** Reserved.
0	0x0 RW	**PCI_CFG_DIS1:** Reserved.

12.6.49 reg_PCICFGCTR2_type (PCICFGCTR2)—Offset 504h

Access Method

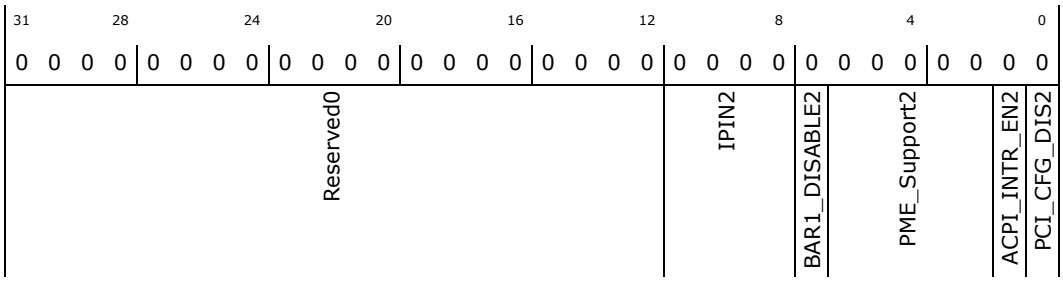
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 504h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved0:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11:8	0x0 RO	**IPIN2:** Reserved.
7	0x0 RO	**BAR1_DISABLE2:** Reserved.
6:2	0x0 RO	**PME_Support2:** Reserved.
1	0x0 RO	**ACPI_INTR_EN2:** Reserved.
0	0x0 RO	**PCI_CFG_DIS2:** Reserved.

12.6.50 reg_PCICFGCTR3_type (PCICFGCTR3)—Offset 508h

Access Method

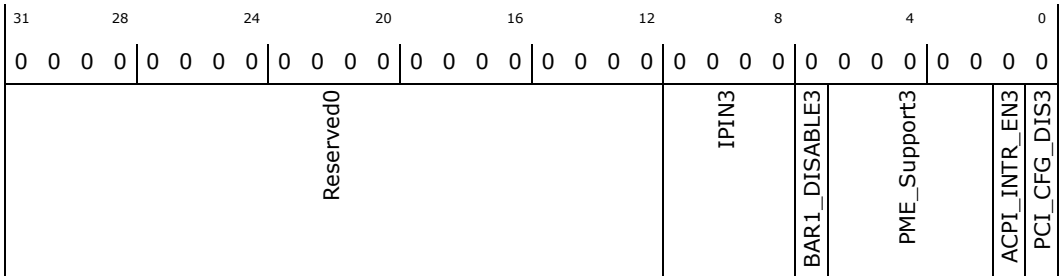
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 508h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x0 RO	**IPIN3:** Reserved.
7	0x0 RO	**BAR1_DISABLE3:** Reserved.
6:2	0x0 RO	**PME_Support3:** Reserved.
1	0x0 RO	**ACPI_INTR_EN3:** Reserved.
0	0x0 RO	**PCI_CFG_DIS3:** Reserved.

12.6.51 reg_PCICFGCTR4_type (PCICFGCTR4)—Offset 50Ch

Access Method

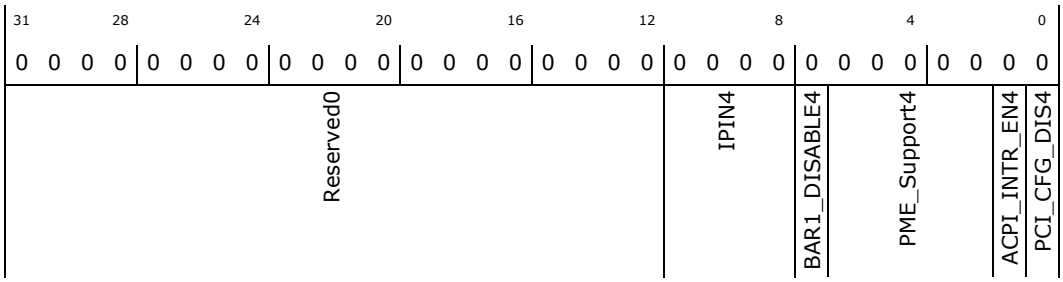
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 50Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x0 RO	**IPIN4:** Reserved.
7	0x0 RO	**BAR1_DISABLE4:** Reserved.
6:2	0x0 RO	**PME_Support4:** Reserved.
1	0x0 RO	**ACPI_INTR_EN4:** Reserved.
0	0x0 RO	**PCI_CFG_DIS4:** Reserved.

12.6.52 reg_PCICFGCTR5_type (PCICFGCTR5)—Offset 510h

Access Method

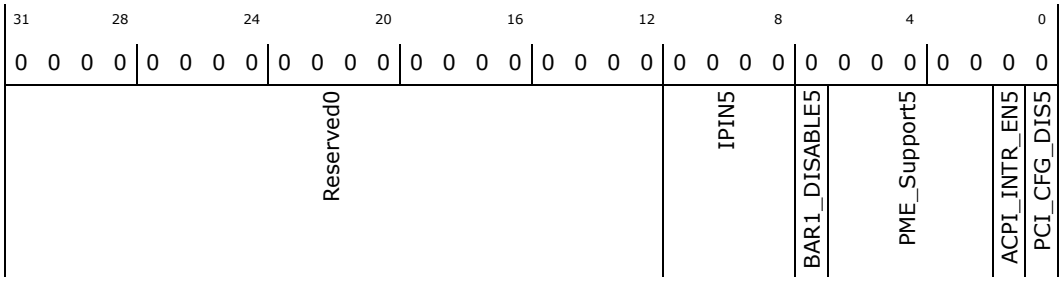
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 510h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x0 RO	**IPIN5:** Reserved.
7	0x0 RO	**BAR1_DISABLE5:** Reserved.
6:2	0x0 RO	**PME_Support5:** Reserved.
1	0x0 RO	**ACPI_INTR_EN5:** Reserved.
0	0x0 RO	**PCI_CFG_DIS5:** Reserved.

12.6.53 reg_PCICFGCTR6_type (PCICFGCTR6)—Offset 514h

Access Method

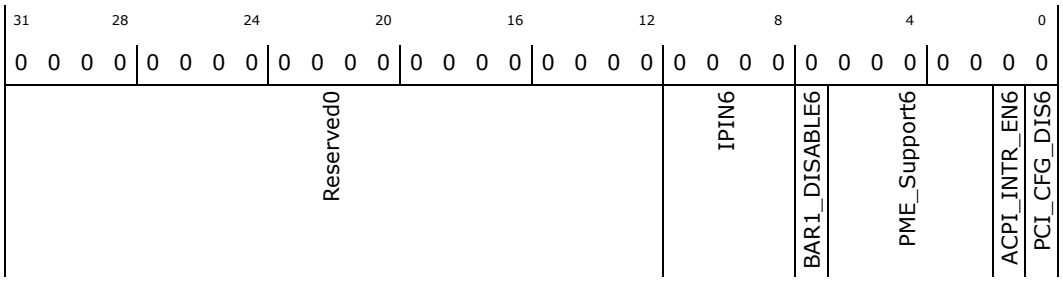
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 514h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved0:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11:8	0x0 RO	**IPIN6:** Reserved.
7	0x0 RO	**BAR1_DISABLE6:** Reserved.
6:2	0x0 RO	**PME_Support6:** Reserved.
1	0x0 RO	**ACPI_INTR_EN6:** Reserved.
0	0x0 RO	**PCI_CFG_DIS6:** Reserved.

12.6.54 reg_PCICFGCTR7_type (PCICFGCTR7)—Offset 518h

Access Method

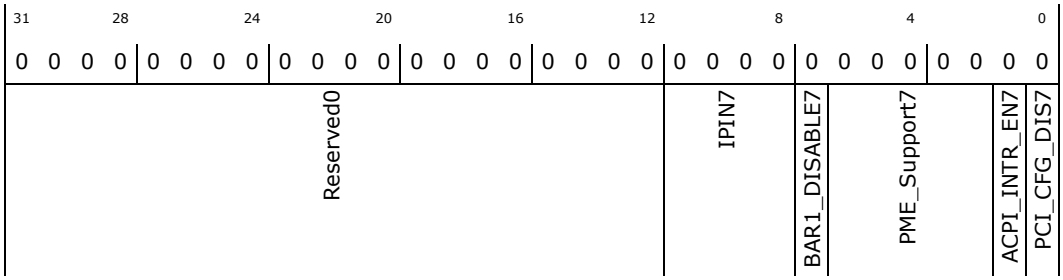
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 518h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x0 RO	**IPIN7:** Reserved.
7	0x0 RO	**BAR1_DISABLE7:** Reserved.
6:2	0x0 RO	**PME_Support7:** Reserved.
1	0x0 RO	**ACPI_INTR_EN7:** Reserved.
0	0x0 RO	**PCI_CFG_DIS7:** Reserved.

12.6.55 reg_PCICFGCTR8_type (PCICFGCTR8)—Offset 51Ch

Access Method

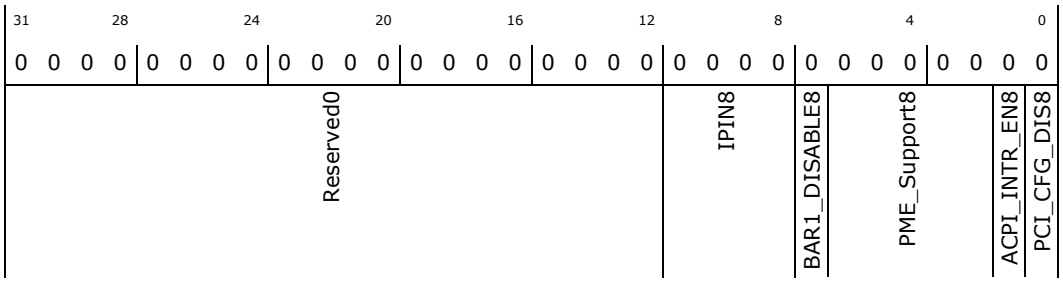
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 51Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0x0 RO	**Reserved0:** Reserved.
11:8	0x0 RO	**IPIN8:** Reserved.
7	0x0 RO	**BAR1_DISABLE8:** Reserved.
6:2	0x0 RO	**PME_Support8:** Reserved.
1	0x0 RO	**ACPI_INTR_EN8:** Reserved.
0	0x0 RO	**PCI_CFG_DIS8:** Reserved.

12.6.56 reg_CHCTRL_type (CHCTRL)—Offset 520h

Access Method

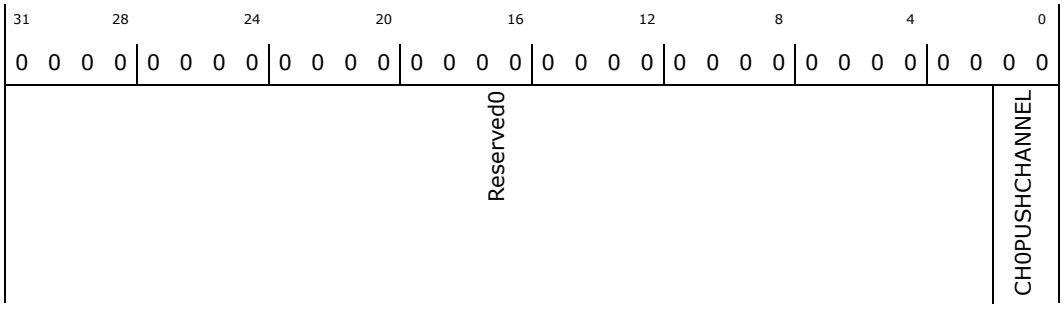
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 520h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0x0 RO	**Reserved0:** Reserved.
1:0	0x0 RW	**CH0PUSHCHANNEL:** Reserved.

12.6.57 reg_GEN_REGRW1_type (GEN_REGRW1)—Offset 600h

Access Method

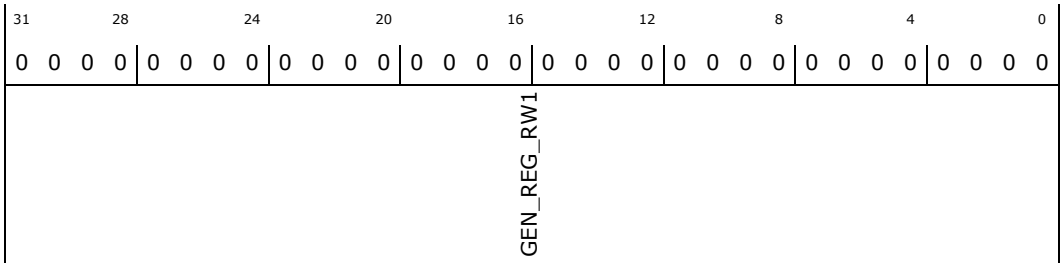
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 600h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW1:** Reserved.

12.6.58 reg_GEN_REGRW2_type (GEN_REGRW2)—Offset 604h

Access Method

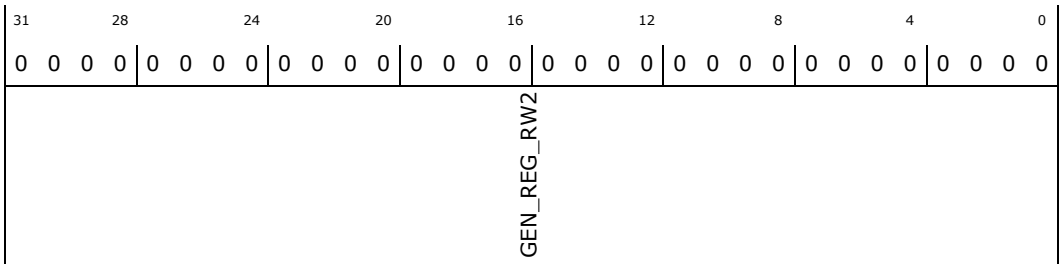
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 604h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW2:** Reserved.

12.6.59 reg_GEN_REGRW3_type (GEN_REGRW3)—Offset 608h

Access Method

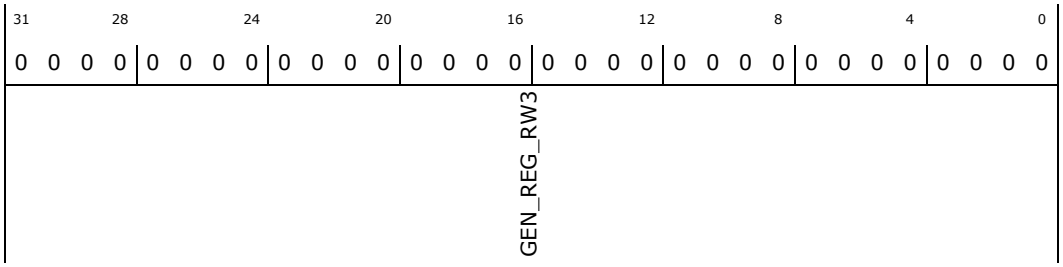
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 608h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW3:** Reserved.

12.6.60 reg_GEN_REGRW4_type (GEN_REGRW4)—Offset 60Ch

Access Method

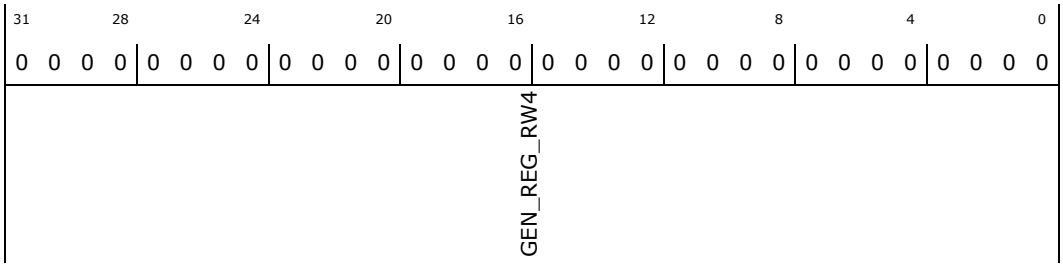
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 60Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW4:** Reserved.

12.6.61 reg_GEN_REGRW5_type (GEN_REGRW5)—Offset 610h

Access Method

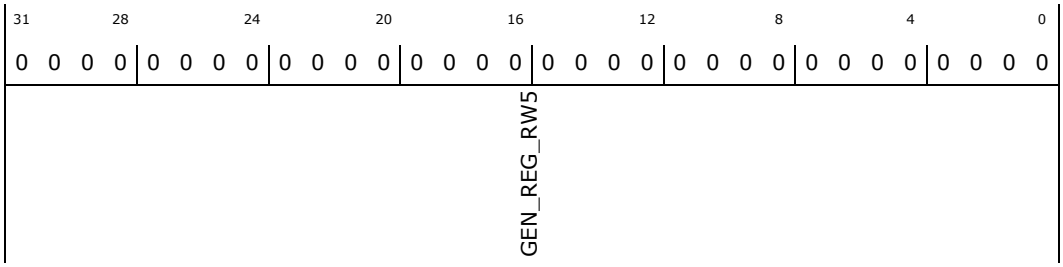
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 610h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW5:** Reserved.

12.6.62 reg_GEN_REGRW6_type (GEN_REGRW6)—Offset 614h

Access Method

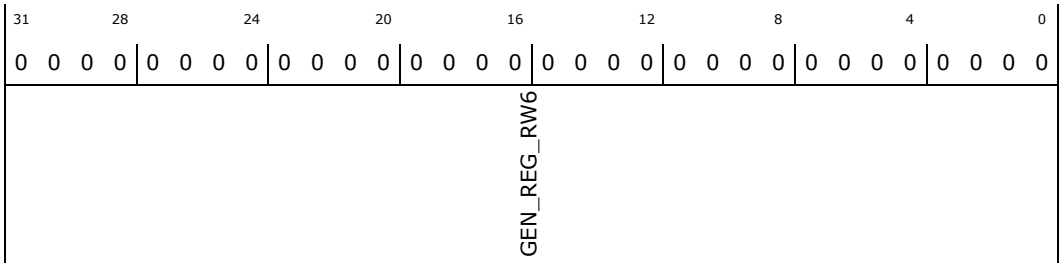
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 614h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW6:** Reserved.

12.6.63 reg_GEN_REGRW7_type (GEN_REGRW7)—Offset 618h

Access Method

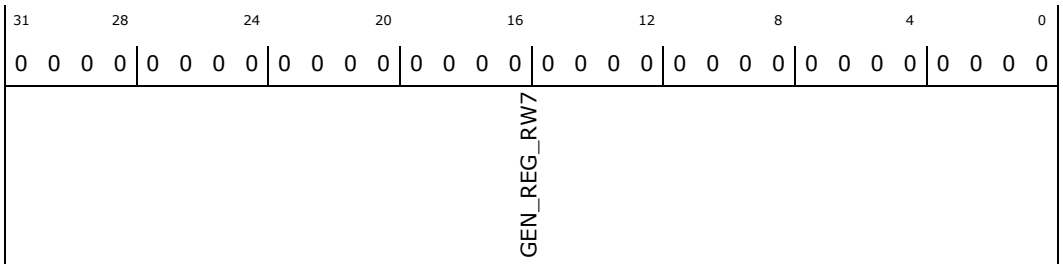
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 618h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW7:** Reserved.

12.6.64 reg_GEN_REGRW8_type (GEN_REGRW8)—Offset 61Ch

Access Method

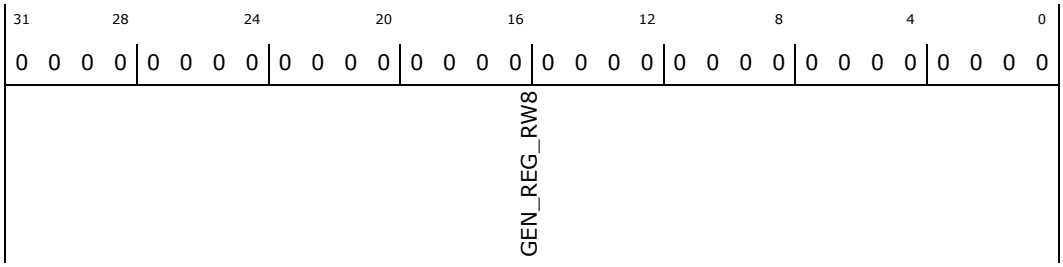
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 61Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW	**GEN_REG_RW8:** Reserved.

12.6.65 reg_GEN_REGRWO1_type (GEN_REGRWO1)—Offset 620h

Access Method

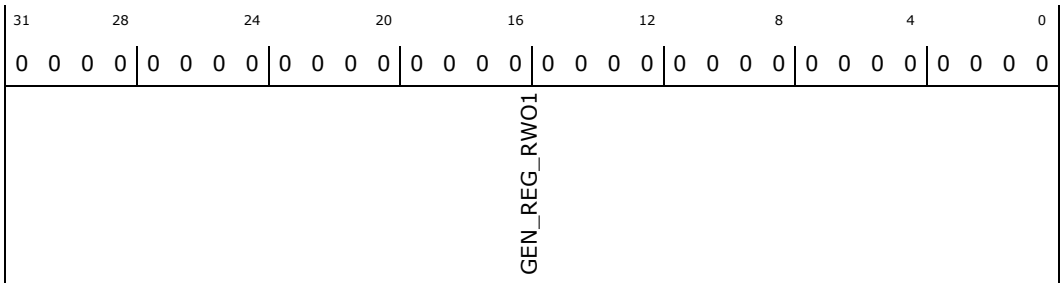
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 620h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/O	**GEN_REG_RWO1:** Reserved.

12.6.66 reg_GEN_REGRWO2_type (GEN_REGRWO2)—Offset 624h

Access Method

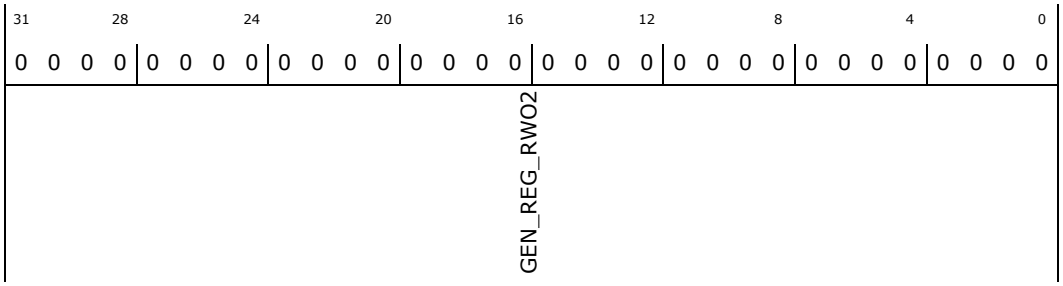
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 624h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/O	**GEN_REG_RWO2:** Reserved.

12.6.67 reg_GEN_REGRWO3_type (GEN_REGRWO3)—Offset 628h

Access Method

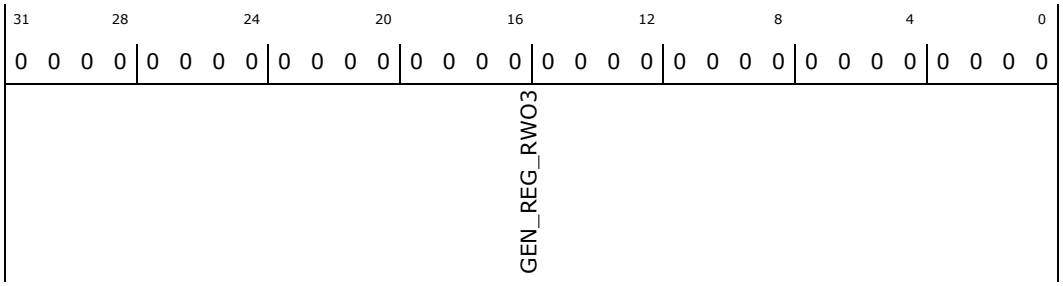
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 628h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/O	**GEN_REG_RWO3:** Reserved.

12.6.68 reg_GEN_REGRWO4_type (GEN_REGRWO4)—Offset 62Ch

Access Method

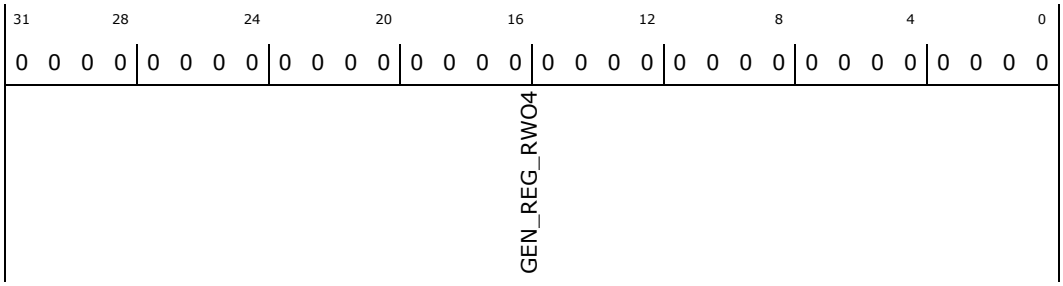
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 62Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/O	**GEN_REG_RWO4:** Reserved.

12.6.69 reg_GEN_REGRWO5_type (GEN_REGRWO5)—Offset 630h

Access Method

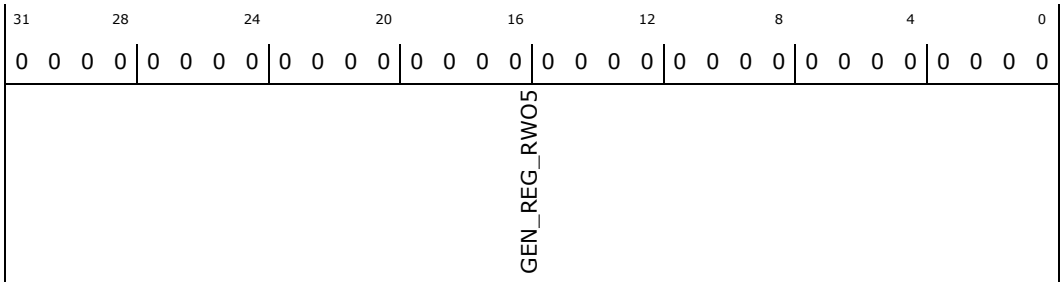
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 630h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/O	**GEN_REG_RWO5:** Reserved.

12.6.70 reg_GEN_REGRWO6_type (GEN_REGRWO6)—Offset 634h

Access Method

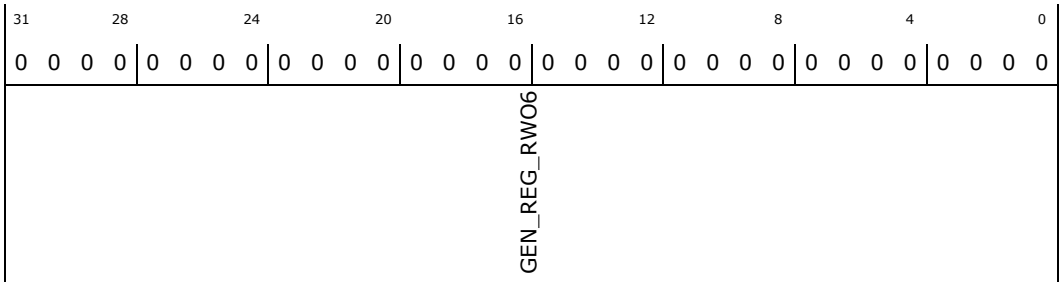
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 634h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/O	**GEN_REG_RWO6:** Reserved.

12.6.71 reg_GEN_REGRWO7_type (GEN_REGRWO7)—Offset 638h

Access Method

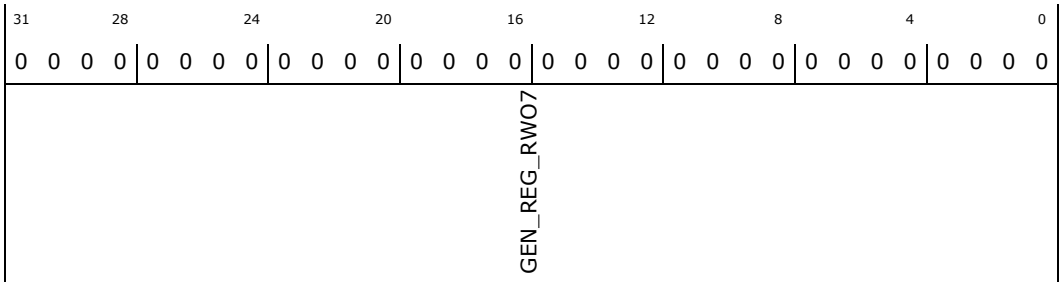
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 638h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/O	**GEN_REG_RWO7:** Reserved.

12.6.72 reg_GEN_REGRWO8_type (GEN_REGRWO8)—Offset 63Ch

Access Method

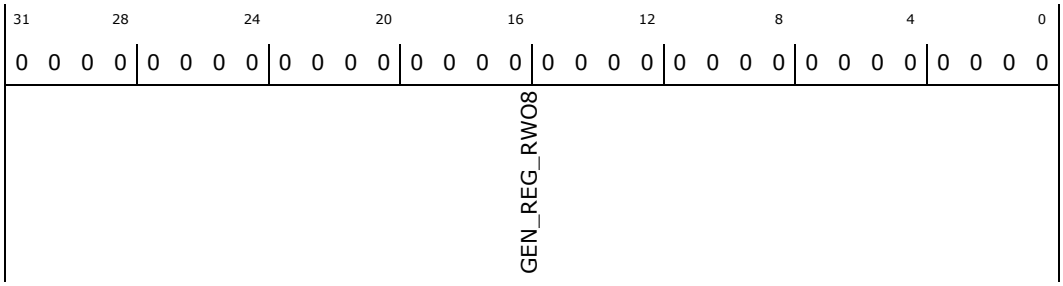
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 63Ch

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RW/O	**GEN_REG_RWO8:** Reserved.

12.6.73 reg_FUSE1_type (FUSE1)—Offset 650h

Access Method

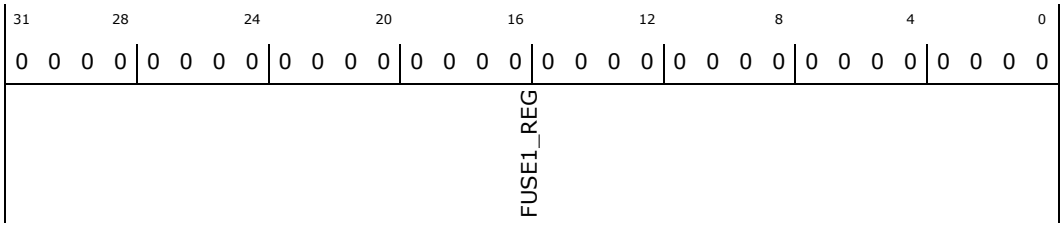
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 650h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RSV	**FUSE1_REG:** Reserved.

12.6.74 reg_FUSE2_type (FUSE2)—Offset 654h

Access Method

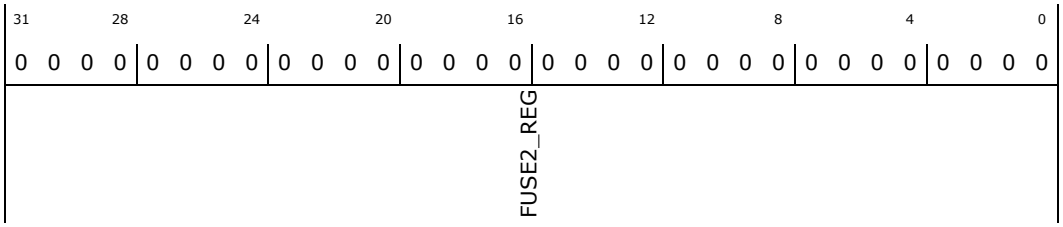
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 654h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RSV	**FUSE2_REG:** Reserved.

12.6.75 reg_FUSE3_type (FUSE3)—Offset 658h

Access Method

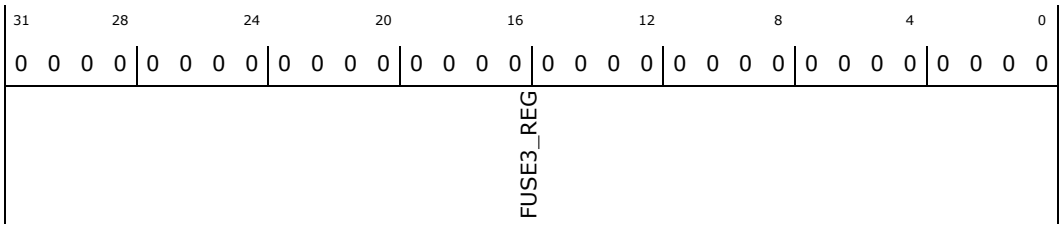
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 658h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RSV	**FUSE3_REG:** Reserved.

12.6.76 reg_STRAP1_type (STRAP1)—Offset 660h

Access Method

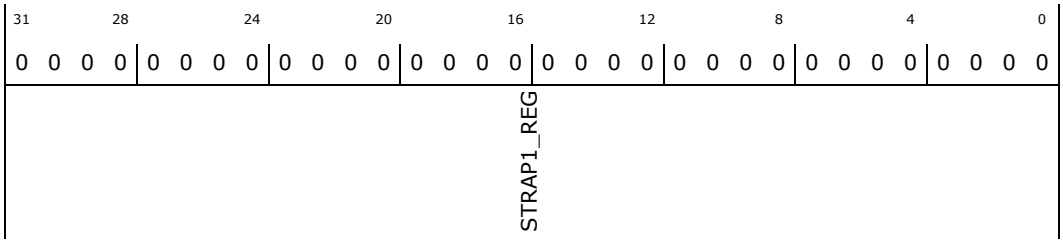
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 660h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RSV	**STRAP1_REG:** Reserved.

12.6.77 reg_STRAP2_type (STRAP2)—Offset 664h

Access Method

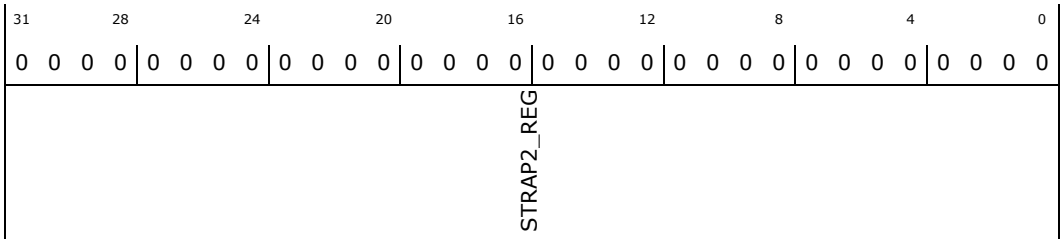
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 664h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RSV	**STRAP2_REG:** Reserved.

12.6.78 reg_STRAP3_type (STRAP3)—Offset 668h

Access Method

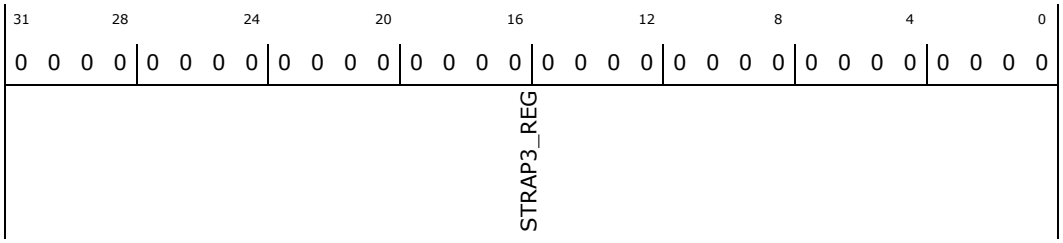
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 668h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0x0 RSV	**STRAP3_REG:** Reserved.

12.6.79 reg_FUSE_STRAP_CPL_STATUS_type (FUSE_STRAP_CPL_STATUS)—Offset 670h

Access Method

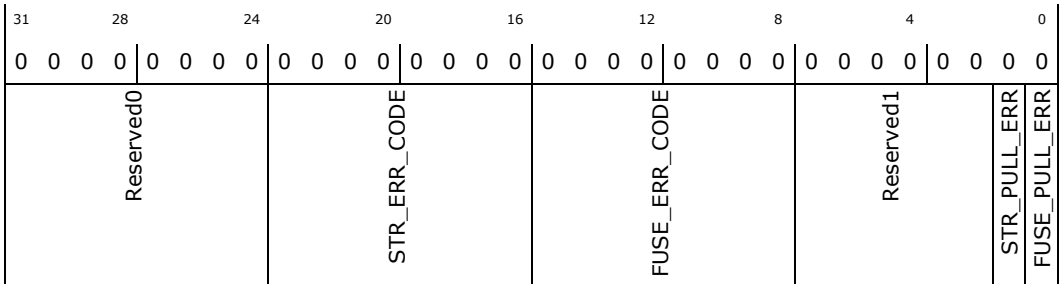
Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0xB1] + 670h

Op Codes:

h - Read, h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0x0 RSV	**Reserved0:** Reserved.
23:16	0x0 RSV	**STR_ERR_CODE:** Reserved.
15:8	0x0 RSV	**FUSE_ERR_CODE:** Reserved.
7:2	0x0 RSV	**Reserved1:** Reserved.
1	0x0 RSV	**STR_PULL_ERR:** Reserved.
0	0x0 RSV	**FUSE_PULL_ERR:** Reserved.